RF PERFORMANCE AND PROCESS DEVELOPMENT OF InP DHBTS USING NON-SELECTIVE EMITTER REGROWTH

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ABSTRACT

We report improvements in the growth and fabrication process of InP-based double heterojunction bipolar transistors (DHBTs) utilizing non-selective molecular beam epitaxy (MBE) regrown base-emitter junctions. This regrown emitter process produces a heterojunction bipolar transistor (HBT) structure with an emitter contact area much larger than the base-emitter junction, facilitating low emitter resistance even as deep submicron base-emitter junctions are used. In this report we present process development and regrowth surface preparation details relevant to emitter regrowth. Improvements to the regrowth surface and its effect on large-area dc characteristics and small-area RF device results are presented.

INTRODUCTION

High breakdown III-V HBTs have applications in analog and digital systems operating near and above 100 GHz clock rates. To achieve such clock rates, the AC current gain, f_t, and the power gain, f_{max}, cutoff frequencies must be several hundred GHz. HBTs achieve high f_t by reducing the epitaxial base and collector thickness to reduce transit times. Simultaneous lateral scaling and reduced contact resistances are also required to reduce capacitive charging delays in both f_t and f_{max} [1][2]. Recent examples of aggressive epitaxial and lateral scaling in InP mesa DHBTs include 370 GHz f_t and 459 GHz f_{max} using a 0.6×7 μm^2 emitter-base junction area [3], and 347 GHz f_t and 492 GHz f_{max} with a 0.6×5 μm^2 emitter junction [4]. Both DHBTs utilized similar base and collector thickness of 300Å and 1500Å, respectively.

In recent years, III-V HBTs have faced strong competition from SiGe-based HBTs. The advantages of InP HBTs over SiGe lie in the III-V material properties. The primary disadvantage is the immaturity of III-V device fabrication technology relative to its silicon counterpart. Silicon fabrication technology and the silicon bipolar device structure allow for high levels of parasitic reduction in SiGe-based HBTs compared to III-V HBTs. This allows SiGe-based HBTs to remain competitive despite the material advantages of III-V semiconductors. SiGe HBTs have been reported with f_t and f_{max} as high as 375 and 338 GHz, respectively, using emitter junction areas of 0.12×2.5 μm^2 [4][5]. Such small junction areas are permissible in this technology by using low-resistance polysilicon emitter contacts with contact area much wider than the base-emitter junction. Low emitter resistance is of crucial importance; each doubling of HBT logic speed demands a 4:1 reduction in emitter resistance normalized to the emitter junction area. SiGe HBT fabrication employs chemical vapor deposition (CVD) and diffusion to form the polysilicon emitter contact and base-emitter junction. The process generates an emitter contact area much wider than the deep sub-micron base-emitter junction. The emitter resistance, therefore, remains low even as the active junction area is reduced.

The higher carrier mobility and strong heterojunction advantages of III-V HBTs allow devices with much larger emitter junction area to perform at comparable bandwidths. Although III-V HBTs would benefit from scaling to dimensions used in SiGe HBTs [1], III-V HBT device structure and fabrication techniques impede advancements by radical scaling. The base-emitter junction of III-V HBTs are generally formed during device fabrication by dry/wet etch processes. We find these processes can be highly variable at deep submicron dimensions and result in low yield. Furthermore, deep submicron scaling of the emitter in a conventional mesa structure HBT rapidly increases emitter resistance as the emitter contact area is reduced.

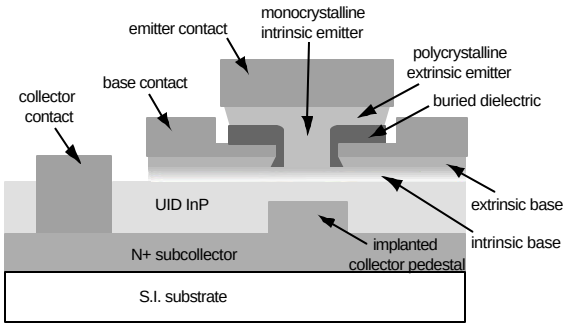

Figure 1. Proposed III-V HBT structure utilizing emitter regrowth and implanted collector pedestal. The collector pedestal is reported in [8]; the emitter-base junction process is described here.

The HBT structure shown in Figure 1 is proposed as an alternative to the conventional III-V mesa HBT structure. This alternative utilizes non-selective MBE regrowth to create a small-area emitter-base junction with a large, low-resistance emitter contact [6][7] analogous to that in a SiGe HBT device structure. The proposed III-V HBT also incorporates an implanted collector pedestal allowing

for reduced transit time in the intrinsic collector region while maintaining a thick extrinsic collector region for lower C_{cb}. The details of the III-V collector pedestal concept are presented elsewhere [8].

This report details the growth and fabrication aspects of InP-based DHBTs utilizing non-selective MBE regrowth to form the base-emitter junction and emitter cap. This regrown emitter process uses a low-resistivity polycrystalline InAs (poly-InAs) [9] extrinsic emitter to form an emitter contact with an area larger than that of the base-emitter junction. This structure facilitates low emitter resistance even when deep submicron base-emitter junctions are used. This work is intended as an initial step to parallel the highly scaled, low parasitic and high-yield aspects of SiGe bipolar transistors.

DEVICE STRUCTURE, GROWTH, AND FABRICATION

The HBT structure used in this work includes only the emitter regrowth and not the collector pedestal. A schematic cross-section of the regrown-emitter fabrication process is shown in Figure 2. The device is fabricated using a patterned base-collector template (Figure 2(a)) onto which the emitter and capping layers are regrown. The template is grown by MBE on a semi-insulating (100) InP substrate. The epitaxial structure is composed of a 3000/100Å InP/InGaAs n+ subcollector, 1100Å n- InP collector, 400Å n- grade and undoped setback layer, 400Å p+ InGaAs base, a 20Å InP p-type etch stop, and a 500Å p+ InGaAs base contact layer. N-type layers are silicon doped, the InGaAs base layers are carbon doped, and the p-type InP is beryllium doped.

A W/Ti/W refractory metal stack is sputtered on the base-collector template, patterned, and dry etched to form what will be a self-aligned base metal buried under isolation layers and the emitter regrowth. PECVD SiN_x is deposited over the entire wafer, and emitter-etch windows are lithographically defined in the centers of the refractory base contacts. Various submicron emitter widths are included on the mask, and the lengths are oriented perpendicular to the [011] direction. Using the single lithography as an etch mask, reactive ion etch (RIE) is used to remove the SiN_x and refractory metal layers from the emitter regrowth areas. After thoroughly cleaning the wafer of organic material, the base cap layer in the emitter regrowth window is selectively removed using an acid-based wet etchant. A second 1000Å PECVD SiN_x is then deposited over the wafer creating an insulative layer that will become the emitter sidewall. Strongly biased, low pressure RIE is used to form a 0.1 µm vertical SiN_x spacer in the emitter window to isolate the emitter regrowth from the base contact region. The 20Å InP etch stop is then selectively etched to expose the intrinsic base regrowth surface. A schematic of the base-collector template before regrowth is shown in Figure 2(b). An abrupt InP or graded InAlAs emitter structure is then regrown by MBE. The emitter is composed of lightly-doped and heavily-doped regions and heavily-doped InGaAs. The growth is then graded in four steps from the InP lattice-matched InGaAs to a 1500Å layer of low-resistance InAs contact material. The regrowth on the exposed base material is crystalline while that deposited on SiN_x is polycrystalline. Ti/Pt/Au/Pt metal is deposited over the emitter regrowth windows to form the emitter contacts. The excess regrown material with SiN_x underneath is dry-etched by inductively coupled plasma (ICP) and RIE, respectively, using the emitter metal as an etch mask as shown in Figure 2(c). Because the base refractory metal has low electrical conductivity, self-aligned Ti/Pd/Au metal is deposited onto the exposed portions of the refractory contacts to reduce feed resistance. The remaining fabrication processes include device isolation and collector contact deposition as shown in Figure 2(d). Polyimide is used as an insulating material and Au metallization forms the coplanar waveguide wiring.

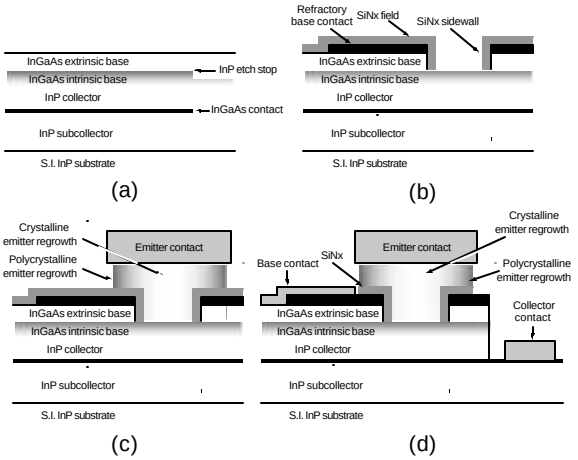

Figure 2. Cross-sectional schematic of regrown-emitter DHBT fabrication steps.

The non-selective regrown emitter process was initially demonstrated in an InAlAs/InGaAs/InP DHBT using a chirped superlattice (CSL) grade at the emitter-base interface [6][7]. In these works, a citric acid-based etchant was used to remove the base cap layer prior to the SiN_x sidewall deposition, and the thin InP etch stop was removed using a strong HCl-based etch prior to emitter regrowth. Subsequent investigation of the regrowth surface after these etch steps and an investigation into use of the CSL regrowth onto the process-exposed surface reveal major problems with the original fabrication process and epitaxial design choice. Shown in Figure 3(a) is an atomic force microscopy (AFM) scan of the base-collector template surface immediately after growth. The scan shows typical variations in the epitaxial surface roughness much less than the 10nm scale shown to the right of the scan image. The surface shown in Figure 3(b) is obtained when the selective, citric acid-based etchant is used to remove the 500Å InGaAs base cap layer. The citric acid etchant is composed of citric acid and H_2O_2 diluted in de-ionized water (DI) to obtain an InGaAs etch rate of 9Å/sec. The surface shown in Figure 3(b) was etched

for 60sec. An extended (90sec) etch in the citric-based etchant further degrades the surface as shown in Figure 3(c).

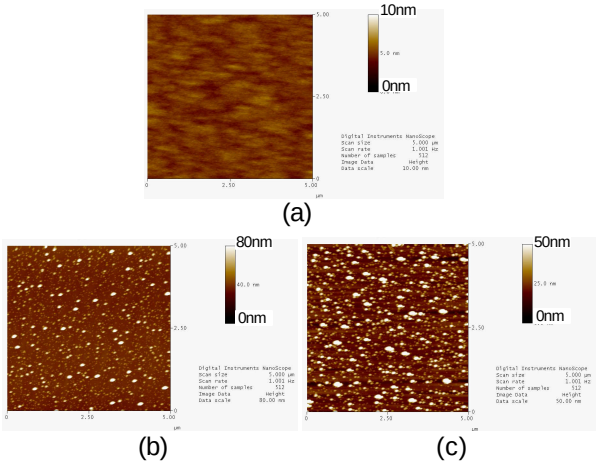

Figure 3. AFM images of **(a)** *as-grown* base-collector template surface, and citric:H_2O_2:DI etched surfaces after **(b)** 60 sec and **(c)** 90 sec.

Various etchants were tested to reduce the surface roughness after the 500Å InGaAs removal. The best results were obtained using a H_2SO_4:H_2O_2 etch diluted in DI to obtain an etch rate of 30Å/sec. Shown in Figure 4(a) is an AFM image of the surface following a 20sec etch in the H_2SO_4-based etch. Although the surface is still rough according to the 50nm scale, the topographic features are much smaller than those of the original citric etch process. Extended etching (35sec) of the base-collector template with the H_2SO_4-based etch is found to drastically increase the surface roughness as shown in Figure 4(b).

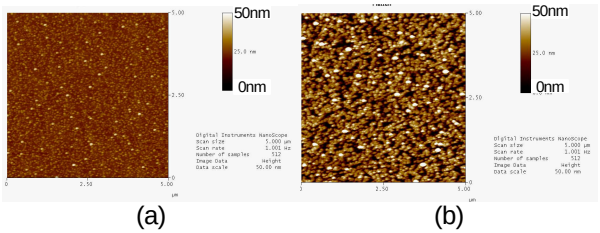

Figure 4. AFM images of H_2SO_4:H_2O_2:DI etched surfaces after **(a)** 20 sec and **(b)** 35 sec.

After removing the InGaAs capping layer, PECVD SiN_x is deposited and removed from the regrowth surface as the dielectric sidewalls are formed. The 20Å InP etch stop layer is then removed prior to regrowth. A strong HCl-based etch was used in the original fabrication process to remove the InP layer. Scans of the regrowth surface are shown in Figure 5 after the strong HCl etchant is used on the citric and H_2SO_4-etched surfaces fom Figures 3(b) and 4(a), respectively. The citric-etched surface in 5(a) shows increased roughness after the HCl etch. The H_2SO_4 etched surface in 5(b), however, is less rough after the HCl etch. In fact, most of this sample's surface is as smooth as the *as-grown* base-collector template in 3(a). Although large topographic feature are present, the overall smoothness of the H_2SO_4 etched surface suggests that the H_2SO_4-based InGaAs etchant is superior to the citric-based etchant when used with the strong HCl InP etch.

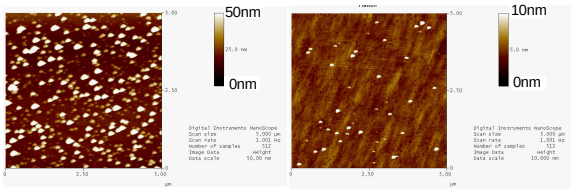

Figure 5. AFM images of regrowth surface after strong HCl etch on **(a)** 60 sec citric:H_2O_2:DI etched surface and **(b)** 20 sec H_2SO_4:H_2O_2:DI etched surface.

Experiments were conducted to further improve the regrowth surface left by the InP etch process. The etch process found as most successful in producing a smooth surface is based on techniques developed for MBE regrowth of InP onto InP and InGaAsP surfaces [10]. The process uses UV light-ozone oxidation followed by a weak (1:10) HF:DI oxide removal. Although it is estimated that the process removes only 20-40Å of material, our InP etch stop layer is only 20Å thick so the etch depth is sufficient. The surfaces left by the ozone and weak oxide etch process are shown below on a 10nm scale. The citric-based etched surface from Figure 3(b) is shown in Figure 6(a) following the ozone and weak HF etch. The surface is considerably improved compared to the surfaces shown in Figures 3(b) and 5(a). The H_2SO_4 etched surfaces from Figure 4(a) is shown in Figure 6(b). The large topographic features that appear in HCl-etched surface (Figure 5(b)) are no longer present. The ozone and weak HF etch appears to be superior to the strong HCl-based InP etch.

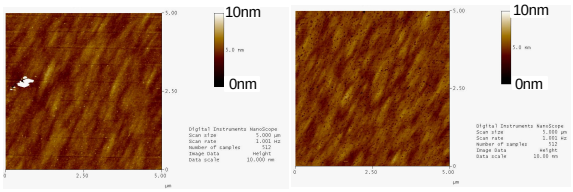

Figure 6. AFM images of regrowth surface after UV-ozone/weak HF etch on **(a)** 60 sec citric:H_2O_2:DI etched surface and **(b)** 20 sec H_2SO_4:H_2O_2:DI etched surface.

To summarize of the etch results, we find that the original regrown emitter process using a selective citric-based InGaAs etch followed by a strong HCl-based InP etch stop removal produces a 50nm RMS roughness at the emitter regrowth surface. An AFM image of this surface is shown in Figure 7(a). Beside it is the non-rectifying I-V characteristic produced by large-area (60×60 μm^2) emitter regrowth onto this surface. In contrast, the sulfuric-based InGaAs etch and UV-ozone/ weak HF InP etch process produces a surface with less than 10nm RMS roughness. The improved large-area rectifying characteristic is shown in Figure 7(b).

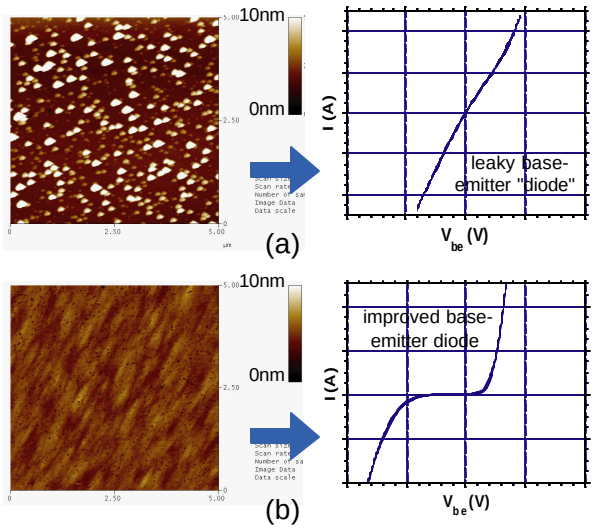

Figure 7. AFM images of **(a)** original and **(b)** improved base-emitter regrowth surfaces prior to emitter regrowth and corresponding base-emitter junction IV characteristics.

The emitter structure used in [6][7] includes an 300Å, 18-layer CSL grade from the InGaAs base to the InAlAs emitter. We find that initiating MBE regrowth using a ternary superlattice presents a challenge as strong three-dimensional growth is immediately observed in the MBE system's reflection-high energy electron diffraction (RHEED) signal. Weak two-dimensional reconstructions do form with the InAlAs emitter regrowth, but only after about 800Å of deposition. Initiation of strong island growth in the superlattice structure causes concern over the *actual* alloy compositions formed at the regrowth interface and over the non-planarity of the grading region.

A single-layer, InP abrupt emitter structure resolves these concerns by eliminating both the CSL and the use of ternaries near the heterojunction. We find InP regrowth to be far less prone to three-dimensional reconstruction, and the elimination of the ternary superlattice makes the regrowth less sensitive to composition and planarity effects. Strong two-dimensional reconstructions are observed by RHEED after less than 100Å of growth. This growth initialization trend is *similar* that observed on epi-ready InP substrates. The combination of simplified growth structure and the improved regrowth surface show dramatic improvements in large-area diode characteristics and in the RHEED signal during emitter regrowth.

Device Results and RF Performance

In our first account of small-area devices, we report a 160 GHz f_t and 140 GHz f_{max} for a graded emitter-base junction InAlAs/InGaAs/InP DHBT [7]. That device had an emitter junction area of 0.7×8 μm^2 and a CSL grade at the emitter-base interface. With the improvements described in this report, we have produced an abrupt emitter-base junction device with an InP emitter. By eliminating the multiple regrowth junctions and improving the regrowth surface preparation process, we demonstrate a 0.7×8 μm^2 regrown emitter HBT with a maximum f_t of 183 GHz and f_{max} of 165 GHz. The device has a small-signal current gain h_{21} of 17 and collector breakdown voltage V_{CEO} is near 6V. The complete details of this device are presented elsewhere [11].

Although improved from the original InAlAs emitter results, we do not believe that the full RF performance potential has yet been demonstrated. Several major issues are still known to exist in the regrown emitter fabrication process and, to a lesser extent, in the process steps following the regrowth process. The current improvements produce an epitaxial-smooth regrowth surface and are shown to improve the large-area diode characteristics. Revisions in the epitaxial design to reduce three-dimensional growth have successfully improved two-dimensional reconstructions observable by RHEED. We believe that the these improvements have lead to the advancements in RF performance described in this report.

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