Millimeter-Wave CMOS Circuit Design

Hisao Shigematsu, *Member, IEEE*, Tatsuya Hirose, Forrest Brewer, and Mark Rodwell, *Fellow, IEEE*

***Abstract*—We have developed a 27- and 40-GHz tuned amplifier and a 52.5-GHz voltage-controlled oscillator using 0.18-μm CMOS. The line-reflect-line calibrations with a microstrip-line structure, consisting of metal1 and metal6, was quite effective to extract the accurate S-parameters for the intrinsic transistor on an Si substrate and realized the precise design. Using this technique, we obtained a 17-dB gain and 14-dBm output power at 27 GHz for the tuned amplifier. We also obtained a 7-dB gain and a 10.4-dBm output power with a good input and output return loss at 40 GHz. Additionally, we obtained an oscillation frequency of 52.5 GHz with phase noise of −86 dBc/Hz at a 1-MHz offset. These results indicate that our proposed technique is suitable for CMOS millimeter-wave design.**

***Index Terms*—Millimeter wave, phase noise, tuned amplifier, voltage-controlled oscillator (VCO).**

I. Introduction

THE RAPID growth of wireless communication using, for example, mobile phones and wireless local area networks (LANs), has created a great demand for Si-based RF integrated circuits (RFICs), operating at microwave and millimeter-wave bands. These applications require a low production cost, thus, CMOS is the most attractive solution and the best component. However, the CMOS maximum oscillation frequency $f_{\max}$, an important parameter for analog circuits, is no higher than those of other devices, such as SiGe HBT and III–V devices. Therefore, it has been difficult to realize analog circuits, especially tuned amplifiers, which operate at close to millimeter-wave frequencies. The III–V devices have accurate parameters around these frequencies because they are fabricated on semi-insulating substrates, and it is easy to eliminate the parasitic parameters. However, CMOS has to be fabricated on a conductive substrate, and its parameters are not applicable to this frequency range. Amplifiers based on III–V and SiGe technologies have been reported. However, there have been very few reports about CMOS amplifiers [1]. In this paper, we propose an accurate parameter-extraction technique with a line-reflect-line (LRL) calibration for CMOS technology, and report a 27- and 40-GHz tuned amplifier and a 52.5-GHz voltage-controlled oscillator (VCO). This parameter-extraction technique provides us with accurate S-parameters of the intrinsic transistor and enables the precise design of the integrated circuits.

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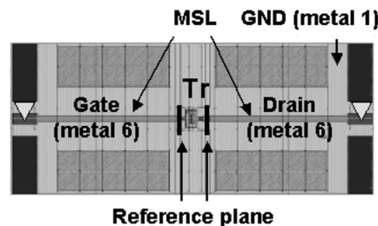

Fig. 1. Parameter-extraction pattern of the transistor.

II. Circuit Design

A. S-Parameter Extraction

The extraction of accurate parameters for transistors and transmission lines is important for millimeter-wave circuit design. To achieve this, we used a microstrip-line (MSL) structure, which consists of a metal1 ground and a metal6 signal line [2]. This line structure eliminates the effect of the conductive substrate and provides us with accurate characteristic impedance, allowing us to avoid unwanted differences between the simulation and measured values. The MSL characteristics, obtained through electric–magnetic (EM) simulation, agreed well with the measured results, even though our metal1 had slots to relax the stress. This enabled us to design the matching circuits more precisely. We prepared the parameter-extraction pattern for the transistor, as shown in Fig. 1.

This pattern consisted of an intrinsic transistor and outgoing electrode lines for the gate and drain, which uses metal6 with probe pads. We used LRL calibrations to extract the S-parameters. This method needs two lines of different lengths and an open pattern. Therefore, we also prepared on-wafer patterns. With this technique, we were able to set the calibration reference planes to the edges of the outgoing lines and obtain the intrinsic S-parameters. Yang *et al.* reported a measurement technique using line-reflect-reflect-match (LRRM) up to 110 GHz, but the reference plane is on the probe tips, as shown by the triangles in Fig. 1 [3]. Therefore, our extraction technique enables easier and more accurate measurement of the S-parameters of the intrinsic transistors [4].

Fig. 2 shows the frequency dependence of the $|h_{21}|^2$, maximum stable gain (MSG) and the maximum available gain (MAG). The profiles were very smooth, and the cutoff frequency f_T and maximum oscillation frequency $f_{\max}$ were 58 and 84 GHz. This indicates that we can obtain accurate S-parameters with this technique, and design the circuits precisely. Fig. 3 shows measured and simulated S_{11} and S_{22} from 0.25 to 110 GHz on a Smith chart.

The S-parameters turned smoothly up to 110 GHz, and no unwanted resonance could be seen up to 110 GHz. We extracted the transistor parameter and created the model. The model is

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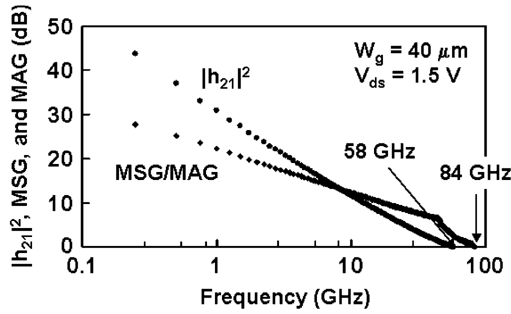

Fig. 2. $|h_{21}|^2$, MSG, and MAG of the intrinsic transistor from 0.25 to 110 GHz.

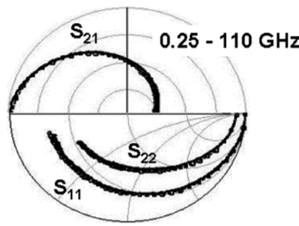

Fig. 3. Measured and simulated S_{11} and S_{22} from 0.25 to 110 GHz (dotted line: simulated data, solid line: measured data).

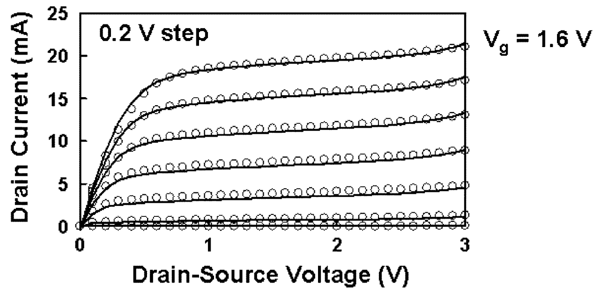

Fig. 4. Measured and simulated *I–V* (dotted lines: simulated data, solid lines: measured data).

in good agreement with the measured data shown in Fig. 3. Fig. 4 shows the measured and simulated *I–V* characteristics of the transistor with a gatewidth of 40 μm. The off-breakdown voltage is over 3 V, where the body is tied to the source terminal. The model is also a good agreement with the measured data in dc characteristics. We used this model for the following designs.

B. Tuned Amplifier Design

At millimeter-wave regions, the loss of the transmission line increases so the transistor's gain is very important for the CMOS amplifier design. A cascode configuration does not degrade the frequency-response at high-frequency regions due to the Miller effect. Therefore, it is superior to the single transistor configuration at high-frequency regions. Fig. 5 shows the MAG of the single and cascode transistors. The cascode configuration has a much larger stable gain than the single transistor configuration. We used the cascode configuration for the amplifier design.

Fig. 6 shows a schematic of the tuned amplifier. It consists of three stages with a cascode configuration. Each drain bias was applied through a quarter-wavelength line. Each gate bias was applied through the high-impedance resistor. We used

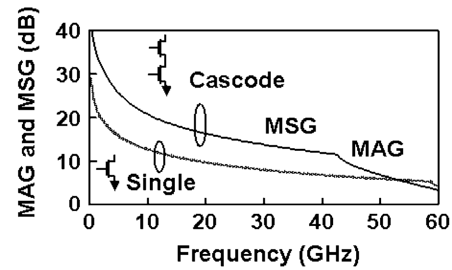

Fig. 5. MAG and MSG of the single and cascode transistors.

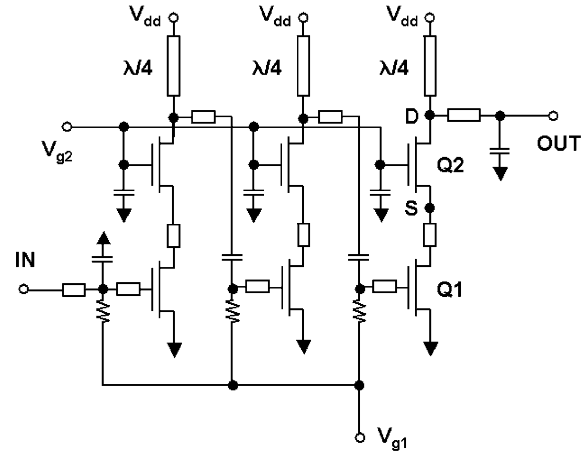

Fig. 6. Schematic of the tuned amplifier.

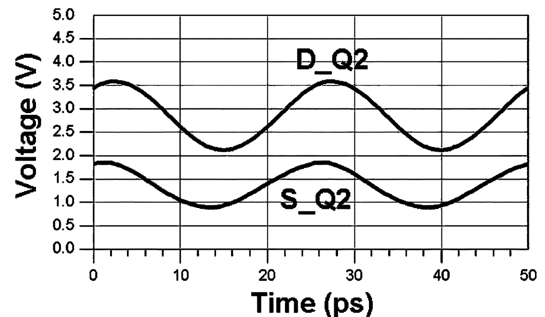

Fig. 7. Source and drain voltage of $Q2$ at 10-dBm input.

metal–insulator–metal (MIM) capacitors at the interstage. The design was based on gain matching, rather than power matching because of the insufficient gain of CMOS at millimeter-wave frequency range. We utilized a transmission line between $Q1$ and $Q2$ to stabilize each stage. The optimized 120-μm lengths exist for the stabilization of the amplifier. The amplifier stability factor was above 50.

Fig. 7 shows the simulated results for the source and drain voltage of $Q2$ at the saturated 10-dBm input at 40 GHz. The maximum drain–source voltage of $Q2$ is less than 1.7 V. Therefore, both transistors $Q1$ and $Q2$ operate under the breakdown voltage.

Next, we will mention the design for the transmission line. Fig. 8 shows the frequency dependence for the MSL and a coplanar-waveguide (CPW) line on an Si substrate. Fig. 9 shows their structures. For the MSL, metal1 was used for the ground planes and metal6 was used for the signal line. Metal1 shields the unwanted effects of the conductive substrate. The loss is

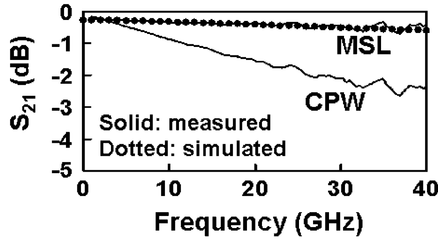

Fig. 8. Frequency dependence for the MSL and CPW on an Si substrate.

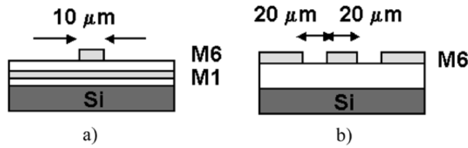

Fig. 9. Line structures on an Si substrate. (a) MSL (b) CPW.

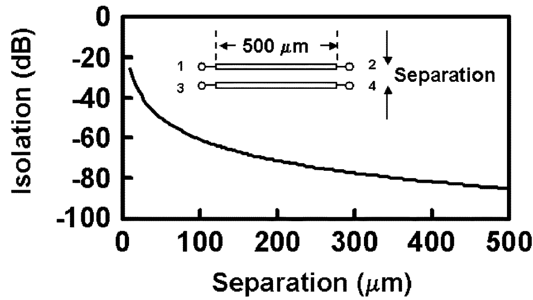

Fig. 10. Simulated isolation between two parallel lines at 40 GHz.

0.25 dB/mm for the MSL, and 2.3 dB/mm for the CPW at 40 GHz. The MSL had a much better performance than the CPW. The EM simulation result for the MSL was in good agreement with the measured one, as shown in this figure. The MSL structure can provide a precise design, and we applied it to the layout design.

When we use an MSL, we must consider the isolation between the adjacent lines because the coupling between the two adjacent lines changes the characteristic impedance. This degrades preciseness for the design, especially at millimeter-wave frequencies. Fig. 10 shows the simulated isolation between two parallel lines at 40 GHz. We obtained a −50-dB isolation at a distance of 50 μm. This distance was sufficient to retain the characteristic impedance. Here, the length of the parallel line was 500 μm. Even at a distance of 20 μm, we obtained a −30-dB isolation at 40 GHz. This value was more than adequate for the layout. However, we used a 50-μm separation to eliminate the unwanted effects of coupling completely this time.

C. VCO Design

Fig. 11 shows a schematic of the VCO. We chose a single-ended fundamental oscillator design to demonstrate the effectiveness of our technique. Recently, harmonics-type VCOs using CMOS technology have been reported to obtain a higher oscillation frequency [5]. This kind of VCO usually consists of two VCOs and combines each of the second harmonics of the output. The fundamental frequencies cancel each other out at the cross point. The highest oscillation frequency ever reported

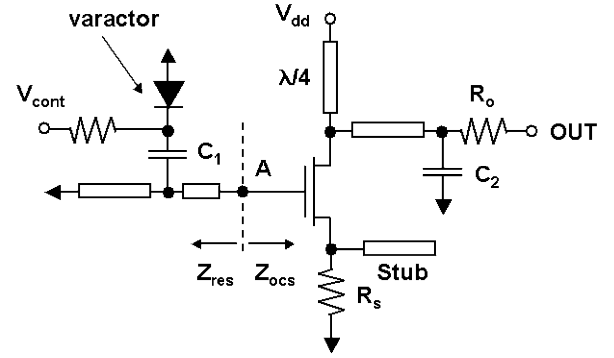

Fig. 11. Schematic of the VCO.

in a CMOS fundamental oscillator was 51 GHz without a special process, such as a high-resistivity substrate and buried and epi layers [6]. (This oscillator used 0.13-μm technology.)

We designed the VCO with 0.18-μm CMOS technology to overcome this oscillation frequency. If we obtain a higher oscillation frequency in the fundamental frequency, the oscillation frequency in the harmonics VCO also increases because this is the basis of the harmonics VCO design. We used a combination of the extrinsic source resistance of R_s and the parallel source stub to generate negative resistance around the target frequency. The tank inductor was made of an MSL to realize an accurate inductance. We used a multifinger CMOS diode for the varactors. To reduce the gate resistance, we used a multifinger transistor in the oscillator core. The gate resistance is a parameter that is very sensitive to the oscillation conditions. The resistor was located at the output port to realize impedance matching and isolation between the output and oscillator core. The drain bias was applied through the quarter-wavelength line at a fundamental frequency. Regarding the design procedure, we first determined the startup oscillation conditions with the extracted S-parameters as follows. The negative resistance generated by the oscillator must exceed the resistive losses of the resonator. This means that the VCO must have a net negative resistance

$$\mathrm{Re}\{Z_{\mathrm{osc}} + Z_{\mathrm{res}}\} < 0. \tag{1}$$

Also, we set the oscillation frequency according to the equation

$$\frac{\partial \mathrm{Im}\{Z_{\mathrm{osc}} + Z_{\mathrm{res}}\}}{\partial \omega} > 0 \tag{2}$$

where

$$\mathrm{Im}\{Z_{\mathrm{osc}} + Z_{\mathrm{res}}\} = 0. \tag{3}$$

Fig. 12 shows the simulated results for the VCO startup frequency at point A, with S-parameter analysis. In this method, the startup oscillation frequency is 53 GHz.

After setting the startup oscillation frequency, we also performed a harmonic-balance simulation with a large-signal model to compensate for the difference between the startup oscillation frequency and the steady-state one.

Fig. 13 shows the harmonic-balance simulation result of the VCO. The oscillation frequency of 52.7 GHz is slightly lower than that using S-parameter analysis. An output of approximately 0.3 V_{pp} was obtained.

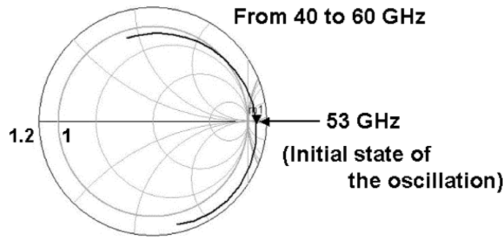

Fig. 12. Oscillation frequency simulations with S-parameters.

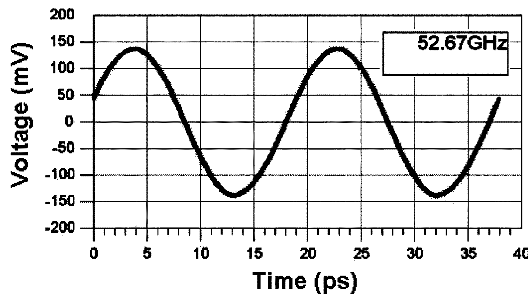

Fig. 13. Harmonic-balance simulations with the extracted model.

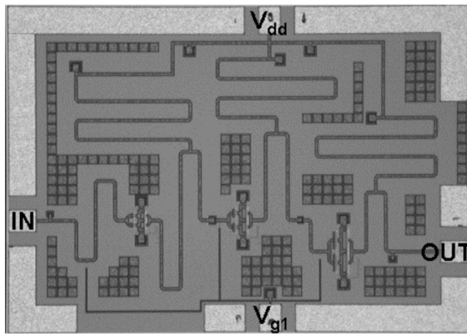

Fig. 14. 27-GHz tuned amplifier.

III. Circuit Measurements

The circuits were fabricated using a 0.18-μm mixed-signal process. In this process, metal6 was 2-μm thick to reduce losses. The measured transistor's cutoff frequency f_T and the maximum oscillation frequency $f_{\max}$ were 58 and 84 GHz, respectively. Fig. 14 shows a microphotograph of the 27-GHz tuned amplifier. The chip size was 1.2×1.7 mm and the power dissipation was 300 mW. We measured the S-parameters using an HP8510XF network analyzer.

Fig. 15 shows the frequency characteristics of the amplifier at a V_{dd} of 3 V. A small-signal gain of 17 dB was obtained at 27 GHz. This is the highest yet reported for a CMOS amplifier at 27 GHz. S_{11} and S_{22} were below -10 dB. The simulation agreed well with the measurements.

We also measured the $P_{\rm in}$–$P_{\rm out}$ characteristics at 27 GHz (Fig. 16). We used an HP1131 frequency synthesizer to generate the input signal, and the output signal was measured with an HP E4418B power meter. We obtained saturated power of 14 dBm at 27 GHz. As far as we know, this performance is the best ever reported for CMOS amplifiers. The simulation results with the large-signal model are also shown in this figure. This simulation agreed well with the measurements, as well as with the small-signal characteristics. Our amplifier can be applied to short-range wireless communication.

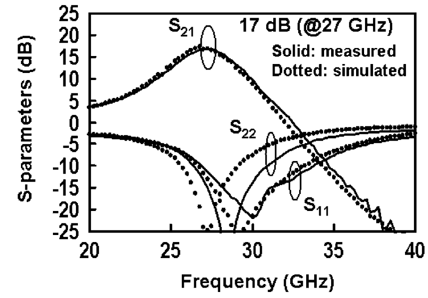

Fig. 15. Measured S-parameters of the 27-GHz tuned amplifier.

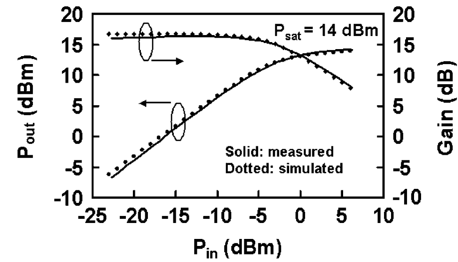

Fig. 16. Measured $P_{\rm in}$–$P_{\rm out}$ characteristics at 27 GHz.

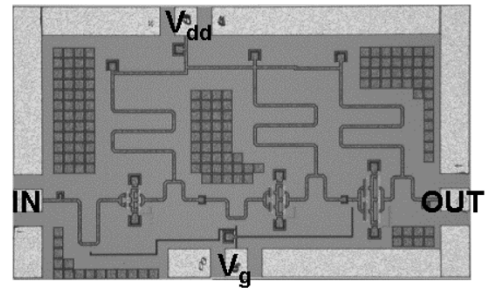

Fig. 17. 40-GHz tuned amplifier.

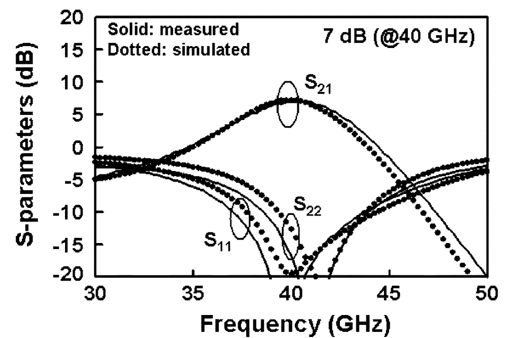

Fig. 18. Measured S-parameters of the 40-GHz tuned amplifier.

Fig. 17 shows a microphotograph of the 40-GHz tuned amplifier. The chip size was 1.2×1.7 mm and the power dissipation was 300 mW. The minimum separation between one line and the other line was 50 μm to prevent coupling, as previously mentioned.

Fig. 18 shows the frequency characteristics of the amplifier at V_{dd} of 3 V. A small-signal gain of 7 dB was obtained at 40 GHz. The impedance matching was done well for the input

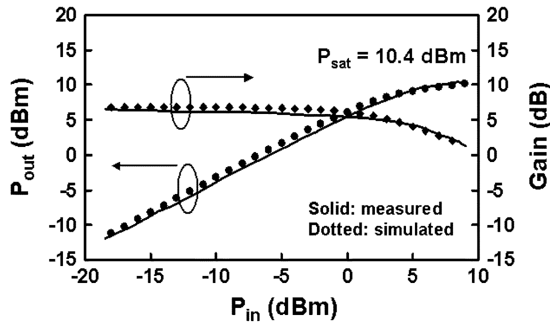

Fig. 19. Measured $P_{\rm in}$–$P_{\rm out}$ characteristics at 40 GHz.

TABLE I
PERFORMANCE COMPARISON

	Freq. (GHz)	Gain (dB)	P_{out} (dBm)	Technology
This work	27	17	14	0.18 μm
This work	40	7	10.4	0.18 μm
[7]	40	9.5	4 (P1dB)	90 nm SOI
[8]	20	5.8	1 (P1dB)	90 nm
[8]	40	6	-1.5	90 nm

and output, and S_{11} and S_{22} were below -15 dB. The simulation agreed well with the measurement, as well as with the 27-GHz tuned amplifier. This performance is comparable to the previous reported 90-nm silicon-on-insulator (SOI) CMOS amplifier [7]. This superior performance can be obtained without such advanced technology.

We also measured the $P_{\rm in}$–$P_{\rm out}$ characteristics at 40 GHz (Fig. 19). We obtained saturated power of 10.4 dBm at 40 GHz. As far as we know, this performance is the best yet reported for CMOS amplifiers. The simulation results with the large-signal model are also shown in this figure. The simulation agreed well with the measurements, as well as with the small-signal characteristics. These results indicate that our proposed technique is quite effective for the medium-power amplifier at millimeter-wave frequencies. Our amplifier is applicable to short-range wireless communication. Table I summarizes the current CMOS amplifiers.

Fig. 20 shows a microphotograph of the VCO. The chip size was 0.8 × 1.0 mm, and the power dissipation was 41 mW. Fig. 21 shows the measured oscillation spectrum of the VCO.

This measurement was done with waveguided (WG) tubes. The oscillator output signal was down-converted by the HP4211A mixer module, and the spectrum was measured by the HP2411 spectrum analyzer. We obtained an oscillation frequency of 52.5 GHz and output power of -8 dBm (after removing the WG tube loss). This oscillation frequency is the highest ever reported for a fundamental VCO without a high-resistivity substrate, such as an SOI structure, or buried and epi layers. The measured oscillation frequency is nearly equal to the simulated one. These results indicate our proposed LRL calibration design technique is promising for high-frequency designs. The control range was 100 MHz. In this study, we intended to use the loose coupling capacitor for the varactor to confirm the design accuracy and this causes the narrow control range. We can easily improve the frequency control range by changing the ratio of the coupling capacitor and varactor.

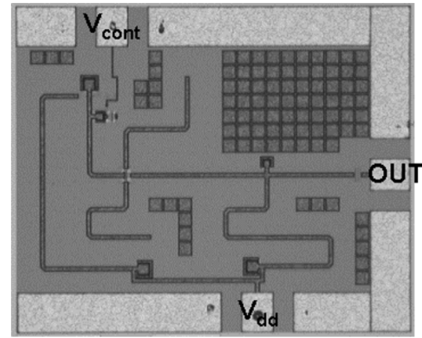

Fig. 20. 53-GHz VCO.

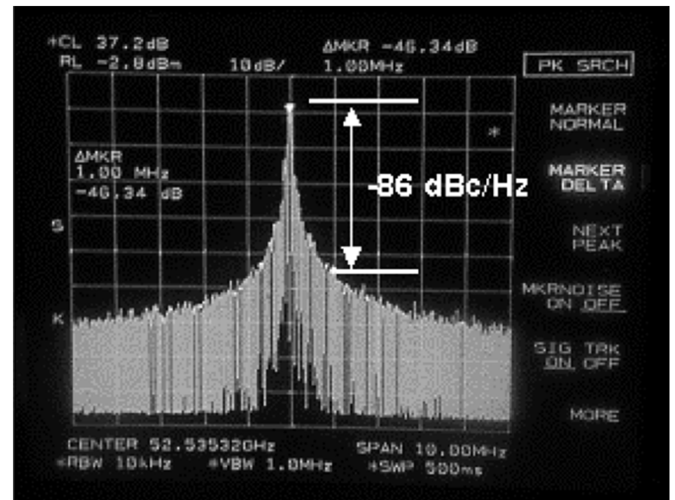

Fig. 21. Measured oscillation frequency of the VCO.

IV. CONCLUSION

We developed a CMOS tuned amplifier and VCO based on a 0.18-μm process. The LRL calibration technique along with an MSL structure consisting of metal1 and metal6 enabled us to extract the accurate S-parameters for the intrinsic transistor and realize the precise design. Using this method, we obtained a 17-dB gain and a 14-dBm output power with good input and output return loss at 27 GHz. We also obtained a 7-dB gain and a 10.4-dBm output power, with a good input and output return loss at 40 GHz. Additionally, we realized an oscillation frequency of 52.5 GHz, with phase noise of -86 dBc/Hz at 1-MHz offset for the VCO. These results indicate that our proposed technique is promising for millimeter-wave-circuit designs.

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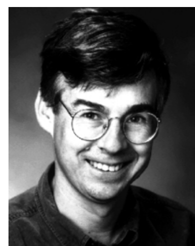

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Dr. Rodwell was the recipient of a 1989 NSF Presidential Young Investigator Award. His work on GaAs Schottky-diode ICs for subpicosecond/millimeter-wave instrumentation was awarded the 1997 IEEE Microwave Prize.