CMOS Circuit Design for Millimeter-Wave Applications

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Abstract - **We have developed a 27-GHz tuned amplifier and 52.5-GHz voltage-controlled oscillator (VCO) using 0.18-μm CMOS. We used LRL calibration to extract accurate S-parameters for an intrinsic transistor with a micro-strip line (MSL) structure consisting of metal1 and metal6. With this technique, we obtained a 17-dB gain and 14-dBm-output power at 27 GHz for the tuned amplifier. We also obtained an oscillation frequency of 52.5 GHz with phase noise of –86 dBc/Hz at a 1-MHz offset. These results indicate that our proposed technique is suitable for CMOS millimeter wave design.**

Index Terms – **VCO, tuned amplifier, phase noise, millimeter wave.**

I. INTRODUCTION

The rapid growth of wireless communication using, for example, mobile phones and wireless LANs, have created a great demand for Si-based RF-ICs operating at microwave and millimeter-wave bands. These applications require low production cost, so CMOS is the most attractive solution and the best candidate. However, the CMOS maximum oscillation frequency f_{max}, which is an important parameter for analog circuits, is no higher than those of other devices such as SiGe HBT and III-V devices. Therefore, it has been difficult to realize analog circuits, especially tuned amplifiers, which operate at close to millimeter-wave frequencies. The III-V devices have accurate parameters around these frequencies, because they are fabricated on semi-insulating substrates and it is easy to eliminate the parasitic parameters. But CMOS has to be fabricated on a conductive substrate and its parameters were not applicable up to this frequency range. Amplifiers based on III-V and SiGe technologies have been reported, however, there have been very few reports on CMOS amplifiers [1]. In this paper, we propose an accurate parameter extraction technique with the line-reflect-line (LRL) calibration for CMOS technology and report a 27-GHz tuned amplifier and a 52.5-GHz VCO. This parameter extraction technique provides us with accurate S-parameters of the intrinsic transistor and enables precise design of the integrated circuits.

II. CIRCUIT DESIGN

A. S-parameter Extraction

The extraction of accurate parameters for transistors and transmission lines is important for millimeter-wave-circuit design. To achieve this, we adopted the MSL structure, which consists of a metal1 ground and a metal6 signal line [2]. This line structure eliminated the effect of the conductive substrate and provided us an accurate characteristic impedance, so we avoided unwanted differences between simulation and measured values. The MSL characteristics obtained through EM simulation agreed well with measured results even though our metal1 had slots to relax the stress. This enabled us to design the matching circuits more precisely. We prepared the parameter extraction pattern for the transistor as shown in Figure 1.

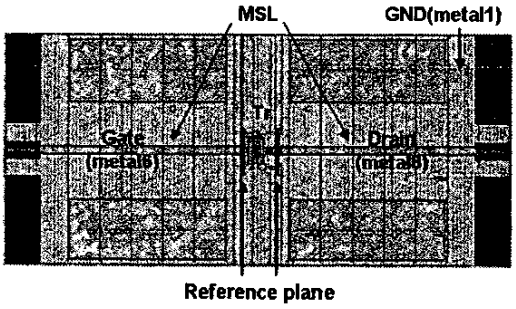

Figure 1 Parameter extraction pattern of the transistor.

This pattern consisted of the intrinsic transistor and the outgoing electrode lines for the gate and drain, which use metal6, with probe pads. We used LRL calibration to extract the S-parameters. This method needs two lines of

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different length and an open pattern. So, we also prepared on-wafer patterns. With this technique, we can set the calibration reference plane to the edge of the outgoing lines and obtain the intrinsic S-parameters. M. Yang et al. reported the measurement technique with LRRM up to 110 GHz, but the reference plane is on the probe tips [3]. Therefore, our extraction technique enables easier and more accurate measurement of the S-parameters of the intrinsic transistor.

Figure 2 shows the frequency-dependence of the $|h_{21}|^2$, maximum stable gain (MSG), and maximum available gain (MAG). Figure 3 shows S_{11} and S_{22} from 0.25 GHz to 110 GHz on a Smith Chart. As shown, the S-parameters turned smoothly up to 110 GHz and no unwanted resonance could be seen up to 110 GHz. We can obtain accurate S-parameters with this technique and design the circuits precisely. We also developed a large signal model to apply to the following designs.

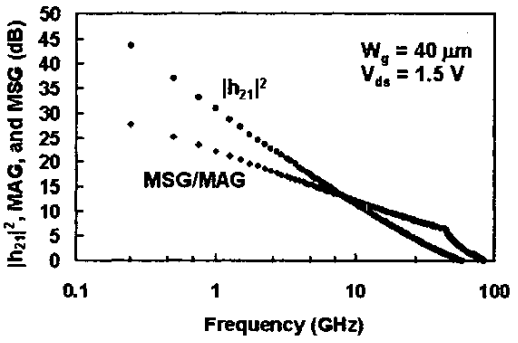

Figure 2 $|h_{21}|^2$, MSG, and MAG of the intrinsic transistor from 0.25 GHz to 110 GHz.

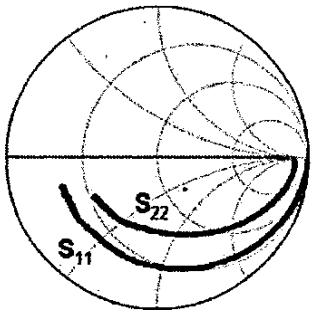

Figure 3 S_{11} and S_{22} of the intrinsic transistor from 0.25 GHz to 110 GHz.

B. Tuned Amplifier Design

The cascode configuration is superior to the single transistor configuration in that a higher gain was obtained. Figure 4 shows the schematic of the tuned amplifier. It consisted of three stages with the cascode configuration.

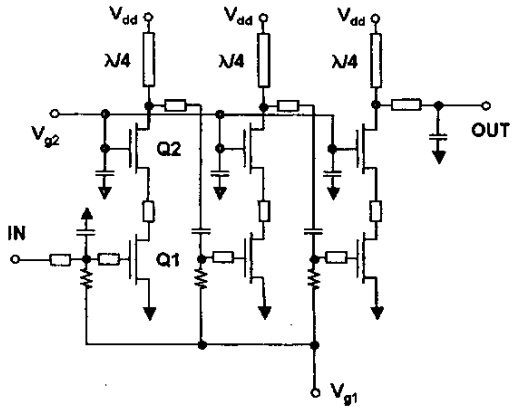

Figure 4 Schematic of the tuned amplifier

Each drain bias was applied through the quarter-wavelength line. Each gate bias was applied through the high impedance resistance. We used AC-coupling at the interstage. The design was based on gain matching, rather than power matching, because of the insufficient gain of CMOS near this frequency range. We utilized the transmission line between Q1 and Q2 to stabilize each stage. An optimized length exists for stabilization of an amplifier, and as this we chose 120 μm. The stability factor of the amplifier was above 50.

C. VCO Design

Figure 5 shows the schematic of the voltage control oscillator (VCO). We chose the single-ended fundamental oscillator design to demonstrate the effectiveness of our technique. Recently, harmonics-type VCOs with CMOS technology have been reported to obtain higher oscillation frequency [4]. This kind of VCO usually consists of two VCOs and combines each second harmonics of the output. The fundamental frequencies cancel each other at the cross point. The highest oscillation frequency ever reported in a CMOS fundamental oscillator is 51 GHz [5]. (This oscillator used 0.13-μm technology.) We designed the VCO to overcome this oscillation frequency. If we obtain a higher oscillation frequency in the fundamental frequency, the oscillation frequency in the harmonics VCO increases, because this is the basis of the harmonics VCO design. We used a combination of the extrinsic source resistance of R_s and the parallel source stub to generate negative resistance around the target frequency. The tank inductor was made of a MSL to realize the

accurate inductance. We used a multi-finger CMOS diode for the varactors. To reduce the gate resistance, a multi-finger transistor was used in the oscillator core. The gate resistance is a parameter that is very sensitive to the oscillation conditions. The resistor was located at the output port to realize impedance matching and isolation between the output and the oscillator-core. The drain bias was applied through the quarterwave length line at the fundamental frequency. Regarding the design procedure, we first determined the start-up oscillation condition with the extracted S-parameters as follows. The negative resistance generated by the oscillator must exceed the resistive losses of the resonator. This means that the VCO must have a net negative resistance:

$$\mathrm{Re}\{Z_{osc}+Z_{res}\}<0. \qquad (1)$$

Also, we set the oscillation frequency according to the equation

$$\frac{\partial \mathrm{Im}\{Z_{osc}+Z_{res}\}}{\partial \omega}>0, \qquad (2)$$

where

$$\mathrm{Im}\{Z_{osc}+Z_{res}\}=0. \qquad (3)$$

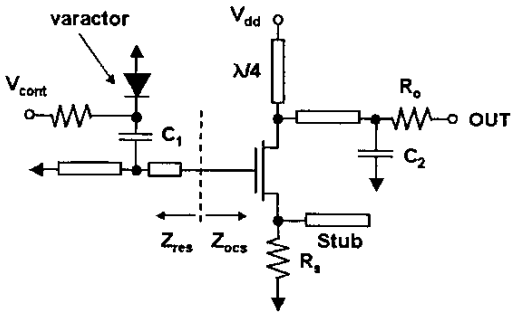

Figure 5 Schematic of the voltage control oscillator (VCO).

After setting the start-up oscillation frequency, we also performed a harmonic balance simulation with the large signal model because there is a difference between the start-up oscillation frequency and the steady one.

III. CIRCUIT MEASUREMENTS

The circuits were fabricated using a 0.18-μm mixed-signal process. In this process, metal6 is 2 μm thick to reduce losses. The measured transistor's cutoff frequency f_T and the maximum oscillation frequency f_{max} were 58 and 84 GHz, respectively. Figure 6 shows a microphotograph of the 27-GHz tuned amplifier. The chip size was 1.2 x 1.7 mm and its power dissipation was 300 mW. We measured the S-parameters using an HP8510XF network analyzer.

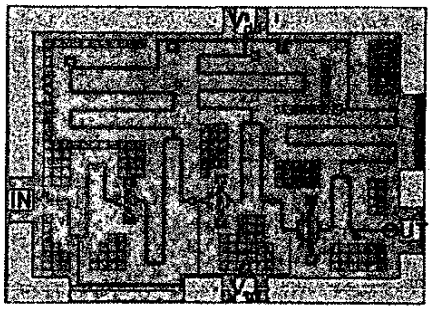

Figure 6 27-GHz tuned amplifier

Figure 7 shows the frequency characteristics of the amplifier at V_{dd} of 3 V. A small signal gain of 17 dB was obtained at 27 GHz. This is the highest yet reported for a CMOS amplifier at 27 GHz. S_{11} and S_{22} were below −10 dB. The simulation agreed well with the measurements.

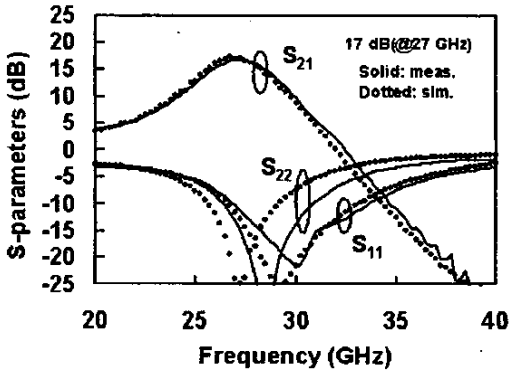

Figure 7 Measured S-parameters of the 27-GHz tuned amplifier

We also measured the P_{in}-P_{out} characteristics at 27 GHz (Figure 8). We used an HP1131 frequency synthesizer to generate the input signal, and the output signal was measured with an HP E4418B power meter. We obtained saturated power of 14 dBm at 27 GHz. As far as we know, this performance is the best yet reported for CMOS amplifiers. Simulation results with the large signal model are also shown in this figure. The simulation agreed well with the measurements as well as with the small signal

characteristics. Our amplifier is applicable to short-range wireless communication.

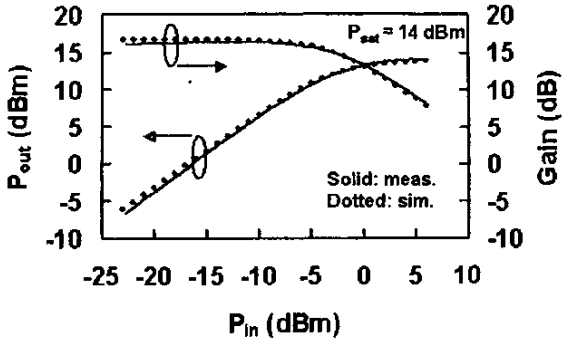

Figure 8 Measured P_{in}-P_{out} characteristics at 27 GHz

Figure 9 shows a microphotograph of the VCO. The chip size was 0.8 x 1.0 mm and its power dissipation was 41 mW. Figure 10 shows the measured oscillation spectrum of the VCO.

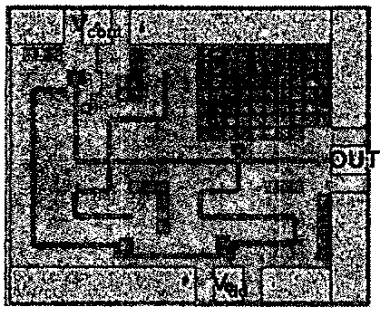

Figure 9 53-GHz VCO

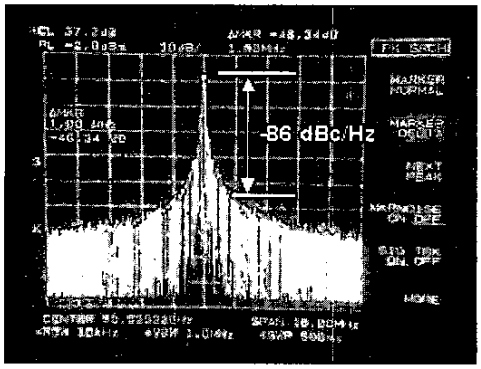

Figure 10 Measured oscillation frequency of the VCO.

This measurement was done with waveguided (WG) tubes. The oscillator output signal was down-converted by the HP4211A mixer module and its spectrum was measured by the HP2411 spectrum analyzer. An oscillation frequency of 52.5 GHz and output power of –8 dBm (after removing the WG tube loss) were obtained. This oscillation frequency is the highest yet reported for a fundamental VCO. The control range was 100 MHz. These results indicate our design technique with LRL calibration is promising for high frequency design.

IV. CONCLUSION

We developed a CMOS tuned amplifier and VCO based on a 0.18-μm process. The LRL calibration technique along with an MSL structure consisting of metal1 and metal6 enabled us to realize accurate S-parameters of the intrinsic transistor. Using this method, we obtained a 17-dB gain and 14-dBm output-power with good input and output return-loss. We also obtained an oscillation frequency of 52.5 GHz with phase noise of –86 dBc/Hz at a 1-MHz offset for the VCO. These results indicate that our proposed technique is promising for millimeter-wave-circuit design.

ACKNOWLEDGEMENT

We also thank Dr. M. Urteaga for variable discussions and Dr. Takigawa for their encouragement.

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