InP DHBT IC Technology with Implanted Collector-Pedestal and Electroplated Device Contacts

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We report the development of a wide bandwidth InP double heterojunction bipolar transistor technology that incorporates an ion implanted N^+ collector-pedestal for reduction of extrinsic collector-base capacitance C_{cb}. The technology also utilizes novel electroplating processes and dielectric sidewall spacers to eliminate traditional liftoff processes from the formation of a self-aligned base-emitter junction. Devices with 0.4 μm emitter junction widths demonstrate peak f_t and f_{max} values of over 370 GHz. Importantly, the devices also demonstrate a significant reduction (~35%) in C_{cb} versus HBTs with the same device footprint fabricated without a collector pedestal. Static frequency-divider circuits have been realized in the technology. A CML divide-by-two circuit demonstrated a maximum operating frequency of 128 GHz. This result demonstrated a ~20% improvement in operating frequency versus the same design realized in a non-collector-pedestal process.

Increasing HBT bandwidth requires vertical scaling of the transistor epitaxy and lateral scaling of the semiconductor junction dimensions. HBT scaling laws state that a $\sqrt{2}$:1 improvement in *all* relevant device figures-of-merit (f_t, f_{max}, digital logic speed) requires a ~2:1 reduction of emitter-base and collector-base junction widths [1]. In a typical mesa-HBT, the collector-base junction lies beneath the base Ohmic contacts and scaling of the junction is limited by the Ohmic transfer length. In silicon bipolar transistors, an ion implanted pedestal collector is employed to reduce extrinsic collector-base capacitance [2]. Recently, collector-pedestal transistors have been demonstrated in InP-based HBT technologies [3-5]. In the pedestal process, a depleted InP spacer layer is inserted between the N^+ sub-collector and the N^- collector drift region. A patterned N^+ link is implanted into the InP layer, and the emitter-base junction is subsequently aligned to the implanted region. Outside of the implanted region the collector depletion depth is increased and C_{cb} is reduced. Fig. 1 shows a schematic cross-section of an HBT with a collector-pedestal. In this work, we report device and circuit results from an industrial IC process that incorporates the implanted pedestal.

In this work, the pedestal process is implemented with two MBE growths on a semi-insulating InP substrate. The initial template growth consists of a 300 nm N^+ InP sub-collector capped with a 200 nm unintentionally doped InP spacer layer. A dielectric mask is used to define the pedestal region for ion implantation. A multiple-dose Si^+ implant is performed at elevated temperature (200°C) to improve dopant activation.

It has been observed that an n-type surface charge of order 10^{12} cm^{-2} will exist at the regrowth interface between the InP spacer layer and the collector drift region [3]. If this charge is not compensated, the InP spacer layer outside of the implanted pedestal will not be depleted and the desired reduction of C_{cb} will not be observed. Previously, compensation of this charge has been demonstrated with p-type pulse doping [3]. However, this approach is difficult to realize in practice, as it requires the interface charge and pulse doping levels be precisely controlled. Recently, Fe^+ ion implantation has been demonstrated as an effective method for compensating this interface charge [5]. Iron is a mid-level acceptor in InP, and provided the implanted dose is greater than the existing interface charge, collector current will be blocked from entering in the InP spacer layer outside of the Si^+ implanted pedestal.

In this work, a shallow Fe^+ compensation implant is applied to the wafer surface after defining the collector pedestal. A high temperature (700°C) anneal is performed to activate the implanted Si dopant and repair lattice damage. The remaining HBT layers are then grown on the wafer. The transistor epitaxy has an abrupt InP/InGaAs emitter-base junction with a 35 nm carbon doped base. The collector thickness is 120 nn, and the base-collector heterojunction grade consists of an InGaAs setback region followed by a InGaAs/InAlAs chirped superlattice [6].

After MBE regrowth, the process flow is identical to Rockwell Scientific's existing HBT IC process. In this process, electroplated contacts and dielectric sidewall spacers are used to produce a high-yield self-aligned base-emitter junction [7]. Optical lithography is used to pattern a submicron emitter contact that is formed with an Au-based electroplating process. Electroplating enables the formation of submicron features with large height to width ratios and straight sidewall profiles, characteristics that are difficult to achieve in evaporated liftoff processes. After performing a self-aligned emitter mesa etch, dielectric sidewalls are formed on the emitter contact. The sidewalls provide electrical isolation between the emitter and base contacts and passivate

the exposed base-emitter junction. The base Ohmic contacts are patterned surrounding the emitter contact, and an electroplating process is used to *selectively* deposit the base metal on the base semiconductor and not on the emitter contact or sidewalls. An SEM cross-section of a fabricated base-emitter junction is shown in Fig. 2. The remaining HBT process flow is similar to that of a standard triple-mesa HBT. The IC process includes: thin-film resistors, MIM capacitors, and three-levels of Au-based metallization separated by a spin-on dielectric (Benzocyclobutene, $e_r = 2.7$).

Fabricated transistors demonstrated a current gain ß of approximately 25, and a common-emitter breakdown voltage BV_{CEO} greater than 4.0V. RF device measurements were made from 1-50 GHz using an Agilent 8510 VNA. Fig. 3 shows the unilateral power gain (U) and short circuit current gain (h_{21}) of a measured HBT with an 0.4 x 5 μm^2 emitter junction dimensions and an as drawn pedestal dimension of 0.5 x 5 μm^2. The device bias conditions are I_c=12.4mA and V_{CE}= 1.75V. The extrapolated f_t and f_{max} of the device are 365 GHz and 390 GHz, respectively. At I_c=12.2mA and V_{CE}= 1.5V, the transistor exhibits a simultaneous f_t and f_{max} of greater than 370 GHz. We believe the f_t result represents the highest reported for a pedestal HBT.

Pedestal transistors exhibit a significant reduction in C_{cb} compared to our standard mesa-HBT process. Fig. 4 shows the extracted values of C_{cb} versus collect current for the collector-pedestal HBT of Fig. 3 and a device with an identical footprint fabricated in our standard HBT process. Both devices have nominal collector depletion thicknesses of 120nm. A 35% reduction in collector-base capacitance is observed due the pedestal process.

In digital logic circuits, a major contributor to gate delay is the time constant associated with charging of the C_{cb} through the load resistance ($C_{cb}\,\Delta V_{\log ic} / I_C$)[1]. The reduction of C_{cb} through the pedestal process is expected to improve digital logic speed. CML static frequency dividers have been fabricated utilizing the collector pedestal process. Details of design considerations for these ultra-high-speed digital circuits can be found in [8]. Fig. 5 shows the output spectrum of a divide-by-two circuit operating with a clock input of 128 GHz. The circuit consumes 304 mW of total power, with 206 mW attributed to the flip-flop core. Fig. 6 shows an input sensitivity plot for the collector pedestal divider, and the sensitivity plot for the identical circuit fabricated on a wafer without the collector pedestal. As in Fig. 4, both wafers have identical device footprints and 120nm collector depletion thicknesses. The addition of the collector pedestal is found to increase the maximum clock frequency by ~20% compared to the non-pedestal wafer (maximum frequency 105 GHz).

A wide bandwidth DHBT technology incorporating an implanted collector pedestal and electroplated device contacts has been described. Fabricated HBTs exhibit excellent RF figures-of-merit and a 35% reduction in collector-base capacitance versus devices fabricated without a collector pedestal. The reduction of C_{cb} has resulted in a >20% increase in the maximum clock frequency of a CML divider circuit. These results demonstrate the potential of the collector-pedestal technology to enable further scaling generations of InP HBTs.

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1. M. J.W. Rodwell et al, "Submicron scaling of HBTs," *IEEE Trans. Electron Devices,* vol. 48, no.11, Nov. 2001.
2. T.H. Ning, "History and Future of the Modern Silicon Bipolar Transistor," *IEEE Trans. Electron Devices,* vol. 48, no.11, Nov. 2001.
3. Y. Dong et al, "C_{bc} reduction in InP heterojunction bipolar transistors with selectively implanted collector pedestal," *Proceedings 2004 Device Research Conference,* June 21-24, Notre Dame.
4. J. Li et al, " A submicromenter 252 GHz f_T and 283 GHz f_{max} InP DHBT with reduce C_{BC} using selectively implanted buried subcollector (SIBS)," *IEEE Electron Device Letters,* vol. 26, no. 3, March 2005.
5. N. Parthasarathy et al, "Collector-pedestal InGaAs/InP DHBTs fabricated in a single-growth, triple-implant process," *IEEE Electron Device Letters,* vol. 27, no. 5, May 2006.
6. M. Dahlström et al, "Wideband DHBTs using a graded carbon-doped InGaAs base," *IEEE Electron Device Letters,* vol. 24, no.7, July 2003 pp. 433-435.
7. M. Urteaga et. al, "Deep submicron InP DHBT technology with electroplated emitter and base contacts," *Proceedings 2004 Device Research Conference,* June 21-24, Notre Dame.
8. Z. Griffith et al, "Transistor and circuit design for 100-200GHz ICs," *IEEE Journal of Solid-State Circuit,* vol 40, no. 10, Oct. 2005

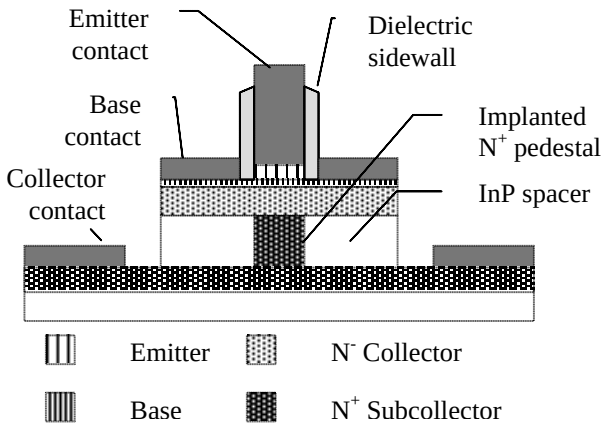

Fig. 1: Schematic cross-section of HBT with implanted collector pedestal .

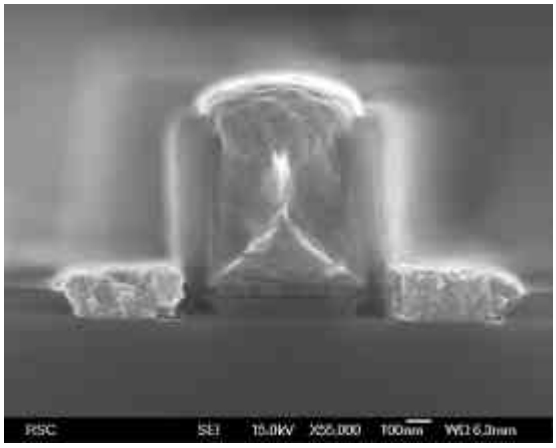

Fig.2: SEM cross-section of self-aligned base-emitter junction formed with electroplating processes

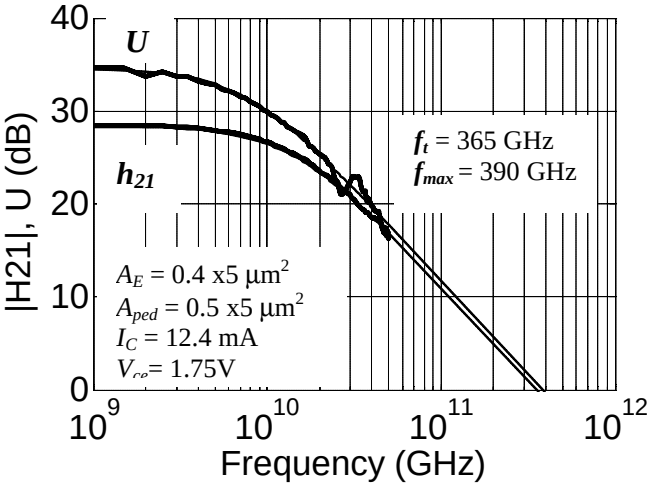

Fig. 3: RF Gains of collector-pedestal HBT

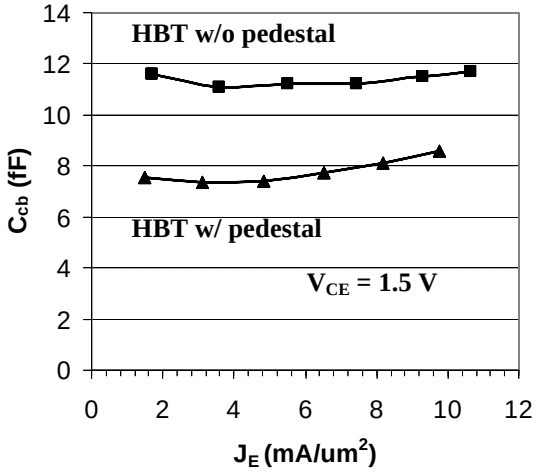

Fig.4: Measured collector-base capacitance versus collector current for HBTs with and without collector pedestal

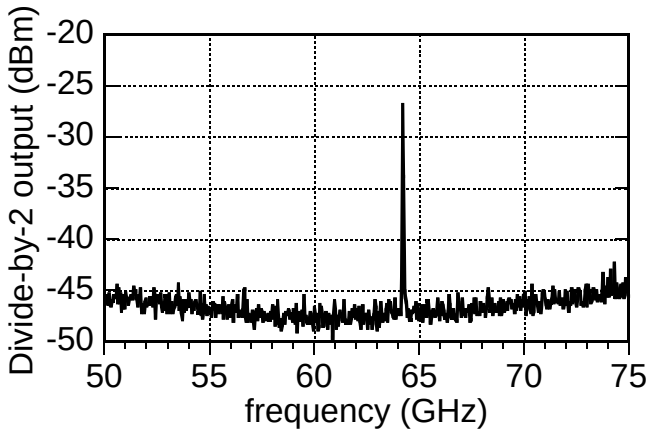

Fig. 5: Output spectrum of CML divide-by-two circuit with 128 GHz clock input.

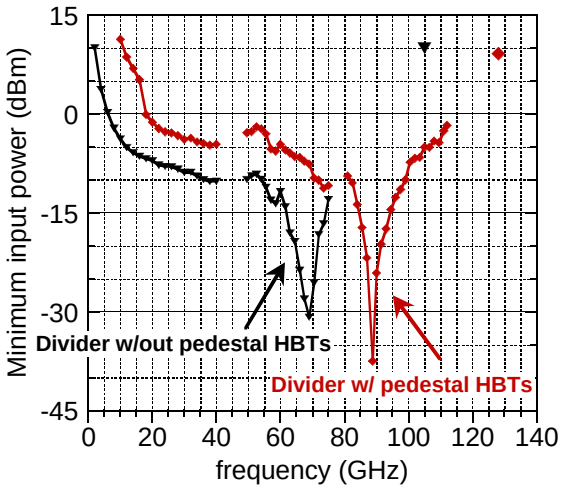

Fig. 6: Input sensitivity plot of CML divide-by-two circuit with and without collector pedestal implant