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Submicron InP-based HBTs for Ultra-high Frequency Amplifiers

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Transistor bandwidths are approaching terahertz frequencies. Paramount to high speed transistor operation is submicron device scaling. High bandwidths are obtained with heterojunction bipolar transistors by thinning the base and collector layers, increasing emitter current density, decreasing emitter contact resistivity, and reducing the emitter and collector junction widths. In mesa HBTs, minimum dimensions required for the base contact impose a minimum width for the collector junction, frustrating device scaling. We have fabricated HBTs with narrow collector junctions using a substrate transfer process. HBTs with submicron collector junctions exhibit extremely high f_{max} and high gains in mm-wave ICs. Transferred-substrate HBTs have obtained record 21 dB unilateral power gain at 100 GHz. If extrapolated at -20 dB/decade, the power gain cutoff frequency f_{max} is 1.1 THz. Recently-fabricated devices have shown unbounded unilateral power gain from 40-110 GHz, and f_{max} cannot be extrapolated from measurements. However, these devices exhibited high power gains at 220 GHz, the frequency limit of presently available microwave network analyzers. Demonstrated amplifier ICs in the technology include reactively tuned amplifiers at 175 GHz, lumped and distributed amplifiers with bandwidths to 85 GHz, and W-band power amplifiers

1. Introduction

Device scaling – the reduction of device layer thicknesses and lithographic feature dimensions – is essential to extending the operating frequency of transistor-based integrated circuits. The benefits of aggressive device scaling are illustrated in silicon CMOS technology where progressive reduction in transistor gate length has been essential to the rapid increases in microprocessor speeds. III-V compound semiconductors offer inherent material advantages over silicon. These advantages include higher electron mobilities, higher electron saturation drift velocities, and stronger heterojunctions than Si/SiGe. Extending transistor technology towards THz frequencies will require combining these material advantages with deep submicron device scaling.

The gate lengths of III-V-based high electron mobility transistors (HEMTs) have been scaled to submicron dimensions. InP-based InGaAs/InAlAs HEMTs have exhibited impressive high frequency performance. Devices in this technology

with 45 nm gate lengths have been reported with maximum current gain cut-off frequencies (f_τ) of over 400 GHz [1]. Separately, transistors with 100 nm gate lengths and maximum frequencies of oscillation (f_{max}) of 600 GHz have been reported [2]. HEMT-based multi-stage amplifiers with large power gains in the 140-220 GHz band have also been reported [3], [4], [5], [6], [7]. State-of-the-art HEMT amplifier results include: a 3-stage amplifier with 30 dB gain at 140 GHz [3], a 3-stage amplifier with 12-15 dB gain from 160-190 GHz [4], and a 6-stage amplifier with 20 $\pm$ 6 dB gain from 150-215 GHz [5].

In contrast to HEMTs, aggressive scaling of III-V heterojunction bipolar transistors (HBTs) has not been prevalent. InP and GaAs-based HBTs are typically fabricated with emitter widths of 1-2 μm, and collector junction widths of 3-5 μm. By comparison, state-of-the-art Si bipolar and Si/SiGe HBTs are fabricated with < 0.2 μm emitter-base junction width. SiGe devices with 0.14 μm emitter-base junction widths have been reported with 92 GHz f_τ and 108 GHz f_{max} [8]. Despite disadvantages in material properties, highly-scaled SiGe technologies will challenge III-V integrated circuits for market share in next generation >40 Gb/sec optical fiber communication systems.

The full benefits of scaling III-V HBTs are only realized if *all* transistor parasitics are simultaneously reduced. Devices with highly scaled emitter-base junctions have been fabricated for low power applications [9]; however, reduced emitter dimensions have not necessarily correlated to improvements in device bandwidth. The parasitic capacitance of the base-collector junction lying under the base Ohmic contacts presents the most severe limit to HBT scaling. The geometry of the mesa HBT used throughout the III-V community is such that the minimum size for base Ohmic contacts places a lower limit on the size of the collector-base junction, preventing submicron scaling. Approaches to facilitate scaling of the collector-base junction include: removal of excess collector semiconductor using a lateral-etch undercut [10], [11], definition of extremely narrow base contacts using $> 10^{20}/\text{cm}^3$ base layer doping [12], and substrate transfer to allow lithographic pattern definition on both sides of the base epitaxial layer.

We have developed a transferred-substrate HBT technology in an InP-based material system. The process allows the emitter-base and collector-base junctions to be simultaneously scaled to submicron dimensions, resulting in dramatic increases in f_{max}. A record unilateral power gain of 21 dB at 100 GHz has been measured in the technology [13]. Recently fabricated submicron devices have exhibited a small negative output conductance from 40-110 GHz, resulting in unbounded unilateral power gain in the 75-110 GHz band [14]. As a result, f_{max} cannot be extrapolated from these measurements. Other device results in the transferred-substrate technology include transistors with simultaneous 295 GHz f_τ and f_{max} [15], and double heterojunction transistors with 425 GHz extrapolated f_{max} and 8 V common-emitter breakdown voltage [16].

In this paper, general scaling laws for HBTs are reviewed. The transferred-substrate process is subsequently described as a means of realizing the potential of

a highly scaled III-V HBT for mm-wave applications. We then present an overview of our measurement and calibration methods for on-wafer device measurements, as these factors are critical for accurate characterization of submicron devices. Measured transistor results are then presented, and difficulties in extending low frequency device models to high frequencies are described. Finally, ultra-high frequency HBT amplifier design is discussed and results from the transferred-substrate technology are presented.

2. HBT Scaling

In general, transistor bandwidths are determined by carrier transit times and RC charging time constants. HBT transit times are reduced by decreasing the thicknesses of the base and collector epitaxial layers. Reduction of the HBT's epitaxial thicknesses will lead to an increase in base resistance and collector capacitance, unless accompanied by lateral scaling of the base and collector junction widths.

The simplified cross-section of a mesa HBT shown in fig. 1 illustrates the difficulty in scaling the transistor's collector-base junction. The patterned etches and metal depositions that form the HBT junctions result in a device structure where the collector-base junction must lie beneath the full area of the base Ohmic contacts. To obtain low base contact resistance, the base Ohmic contact must be at least one contact transfer length L_{contact} wide at the sides of the emitter stripe. In an InGaAs-base HBT with 400 Å base thickness and $5 \times 10^{19}/\text{cm}^3$ doping, $L_{\text{contact}} \simeq 0.4$ μm. Processing tolerances for lithographic alignment may further limit the minimum collector-base junction dimensions.

In contrast to the mesa HBT, a simplified cross-section of an idealized HBT structure is shown in fig. 2. Here, the width of the collector-base junction has been effectively de-coupled from the width of the base Ohmic contacts. Scaling of the collector-base junction width in this device is limited only by alignment tolerances between the emitter and collector stripes. Through substrate transfer, we are able to realize this idealized geometry by lithographically patterning both sides of the base epitaxy. The transferred-substrate process will be discussed further in the Section 3. Next, we will consider the factors that determine HBT bandwidth.

In literature, transistor bandwidth is commonly described by two figures-of-merit: the current gain cutoff frequency f_τ, and the power gain cutoff frequency f_{max}. Independent of f_τ, transistors cannot provide power gain at frequencies above f_{max}. Thus, f_{max} defines the maximum usable frequency of a transistor in narrowband reactively-tuned circuits. In more general analog and digital circuits, the transistor figures-of-merit may not accurately predict circuit performance. For instance, f_τ is commonly used to evaluate a transistor's potential in digital logic applications. However, a detailed charge-control analysis of switching times reveals that device current density, collector-base junction capacitance and emitter resistance make much larger fractional contributions to logic gate delay than they contribute to the emitter-collector forward delay $\tau_{ec} = 1/2\pi f_\tau$ [17]. In analog and digital circuits, f_τ and f_{max} are used to provide a first-order estimate of device

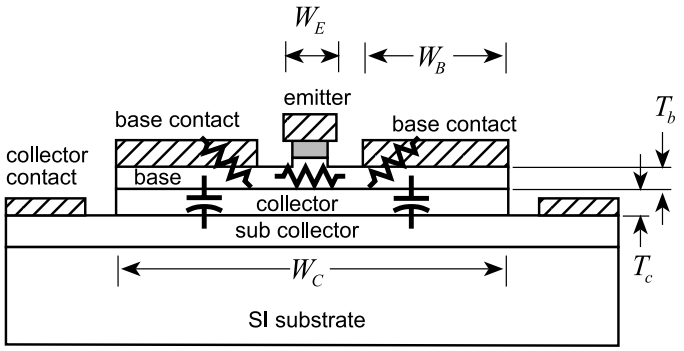
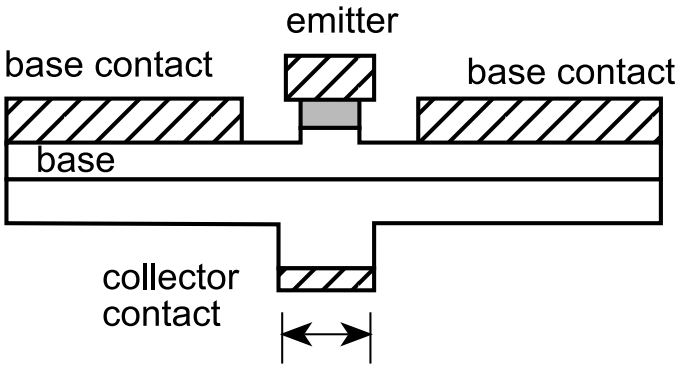


Figure 1: Cross-section of a typical mesa HBT. The emitter-base junction has width W_e, length L_e and area $A_e = L_e W_e$, while the collector-base junction has width W_c, length L_c and area $A_c = L_c W_c$



$$W_C = W_E = W$$

Figure 2: Cross-section of an idealized HBT with the collector-base junction lying only under the emitter. Such device structures can be formed using substrate transfer processes.

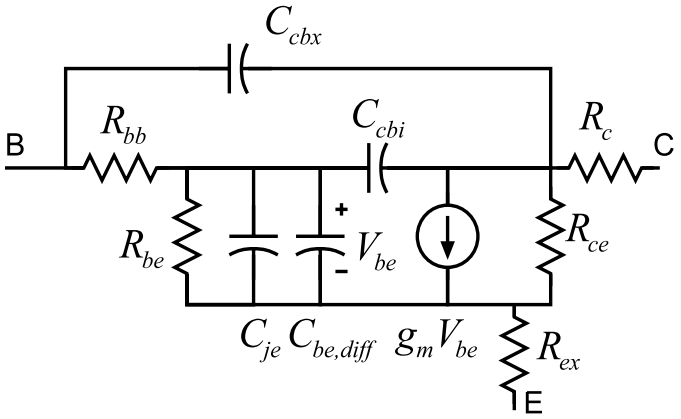


Figure 3: Hybrid-π small-signal HBT equivalent circuit. $C_{be,\mathrm{diff}} = g_m(\tau_b + \tau_c)$.

transit delays and of the magnitude of the dominant transistor parasitics.

We estimate below the cutoff frequencies from HBT parameters calculated from physical device properties and fit to a lumped-element device model. Experience has shown that a simple hybrid-π small-signal circuit model (fig. 3) is sufficient to describe all but the most highly scaled devices up to a frequency of 110 GHz. Concerns regarding the accuracy of model at higher frequencies and in describing highly scaled devices are discussed in section. 5. Those concerns notwithstanding, analysis using this first-order model proves excellent for determining those terms that limit transistor bandwidth.

The scaling analysis that follows has been presented in greater detail elsewhere [17], [18]. It is repeated here for completeness as the benefits of device scaling motivate our approach towards developing THz frequency electronics.

2.1. *Factors determining* f_τ

Our approach to HBT scaling is determined from the parameters that limit device bandwidth. The current-gain cutoff frequency is given by

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}\,(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb}, \tag{1}$$

where R_{ex} and R_c are the parasitic emitter and collector resistances, τ_b and τ_c are the base and collector transit times, C_{je} and C_{cb} are the emitter-base and base-collector junction capacitances, and I_c is the collector current.

Examining each term separately, we begin with the base transit time τ_b. If a linear grading of the base semiconductor bandgap energy with position is used to reduce τ_b, then [19]

$$\tau_b = \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right) - \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right)^2\left(1 - e^{-\Delta E/kT}\right)$$

$$+ \quad \frac{T_b}{v_{exit}} \left(\frac{kT}{\Delta E} \right) \left(1 - e^{-\Delta E/kT} \right) \ , \tag{2}$$

where ΔE is the grading in the base bandgap energy, T_b the base thickness, and D_n is the base minority carrier diffusivity. For a typical InGaAs base at $5 \times 10^{19}/\mathrm{cm}^3$ doping, 52 meV bandgap grading is sufficient to reduce τ_b by $\sim$ 2:1. For a thick base layer or a large v_{exit} , $\tau_b \propto T_b^2$; with InGaAs base layers below $\sim$400 Å thickness, the exit velocity term in eqn. 2 adds a significant correction.

The collector transit time τ_c is the mean delay of the collector displacement current, and in first order analysis is given by [20], [21]

$$\tau_c = \int_0^{T_c} \frac{(1 - x/T_c)}{v(x)} dx \equiv \frac{T_c}{2v_{\mathrm{eff}}}, \tag{3}$$

where $v(x)$ is the position-dependent electron velocity in the collector drift region and v_{eff} an effective electron velocity. τ_c is most strongly dependent upon the electron velocity in the proximity of the base, and becomes progressively less sensitive to the electron velocity as the electron passes through the collector [21]. In HBTs with thin epitaxial layers, nonequilibrium electron transport is observed in the collector drift region [22]. At low collector-base bias voltages, electrons may travel through a significant fraction of the collector drift region in the high velocity Γ-valley before acquiring sufficient kinetic energy (0.55 eV for InGaAs [23], 0.6eV for InP [24]) to scatter to the lower velocity satellite L-valley. As a result, $v(x)$ is fortuitously highest near the base. This velocity overshoot effect significantly reduces collector transit times and in thin InGaAs or InP layers (< 3000 Å), $v_{\mathrm{eff}} = 3$–5×10^7 cm/s. By contrast, measured saturation velocities in thick InGaAs drift layers are in the range of $v_{\mathrm{sat}} = 6$–9×10^6 cm/s [23].

Equation 3 assumes that $v(x)$ is not modulated by changes in carrier density. However, under high injection conditions, electrons screen the bound charge in the collector region and influence the electric field profile. Changes in carrier density alter the field profile and modulate $v(x)$. In the presence of velocity modulation the collector transit time is given by [25]

$$\tau_{c,sc} = \tau_c + J_c \frac{\partial \tau_c}{\partial J_c}, \tag{4}$$

where τ_c is defined in eqn. 3, and J_c is the collector current density. Equation 4 predicts a reduction in collector transit time with velocity modulation correlating a decrease of velocity with increasing current density. Despite these predictions, experimentally we have not measured an anomalous reduction in transit time at high current densities for InP-based HBTs.

The RC charging terms in eqn. 1 comprise a significant fraction of the total forward delay of submicron HBTs, and these terms must be considered in detail. Consider first the term $[kT/qI_c]C_{cb}$. The limits of collector current density are set by the onset of base pushout (the Kirk effect [26]). At high collector current densities,

electron space charge screening at the edge of the base-collector junction eventually leads to a collapse of the electric field. Holes may then diffuse into the collector effectively extending the base region and leading to an increase in base transit time and collector-base capacitance. It has been shown by Ishibashi that GaAs HBTs show improved f_τ when biased close to the Kirk threshold [22], as the reduced electric field at the collector-base junction edge increases velocity overshoot and reduces the collector transit time. We will ignore these considerations in considering the contribution of $[kT/qI_c]C_{cb}$ to f_τ.

From electrostatic considerations, the maximum collector current before base pushout is [17]

$$I_{c,max} = A_e(V_{cb} + \phi)4\epsilon v_{sat}/T_c^2 \propto A_e/T_c^2, \tag{5}$$

where v_{sat} is an (assumed) uniform electron velocity within the collector, and the collector doping N_d is choosen to obtain a fully-depleted collector at zero bias current and the applied V_{cb}. The collector capacitance is $C_{cb} = \epsilon A_c/T_c$. With the HBT biased at $I_{c,max} \propto 1/T_c^2$, $(kT/qI_C)C_{cb} \propto T_c\,(A_c/A_e)$. This delay term is thus minimized by scaling (reducing T_c), but bias current densities must increase in proportion to the square of the desired fractional improvement in f_τ.

The emitter charging time ($C_{je}[kT/qI_c]$ in eqn. 1) plays a significant role in determining f_τ. If we were to assume that C_{je} were simply a depletion capacitance, it would be reasonable to expect that this charging time could be minimized simply by making the emitter-base depletion region very thick, by use of very low emitter doping, combined with a thick bandgap grading region in the base-emitter heterojunction. The tradeoffs between the depletion capacitance and excessive charge storage in the depletion layer were considered in detail elsewhere and the results are repeated here [17]. Using methods similar to those used to derive the collector transit time [20], [21]

$$C_{je}/A_e = \epsilon/T_{eb} + \frac{\partial}{\partial V_{be}}\left[\int_0^{T_{eb}} (x/T_{eb})\, qn(x)dx\right], \tag{6}$$

where T_{eb} is depletion layer thickness and $n(x)$ is the electron density in the depletion region. The term $(kT/qI_c)C_{je}$ in eqn. 1 can be then written as

$$\begin{aligned}(kT/qI_c)C_{je} &= \left(\frac{\epsilon A_e}{T_{eb}}\right)\left(\frac{kT}{qI_c}\right) \\ &+ \frac{\Gamma T_{eb}T_b}{D_n}\int_0^1 \frac{n(\zeta T_{eb})}{n(T_{eb})}\zeta^2 d\zeta,\end{aligned} \tag{7}$$

where $\Gamma = kT/\Delta E - (kT/\Delta E - D_n/v_{exit}T_b)e^{-\Delta E/kT}$ is a factor involving the base bandgap grading ($\Gamma \simeq 1$ for an ungraded base) and $\zeta = x/T_{eb}$ is a normalized position variable.

The first term in eqn. 7 results from the depletion-layer capacitance, and is minimized using high bias current densities $J_e = I_e/A_e$; the second term reflects

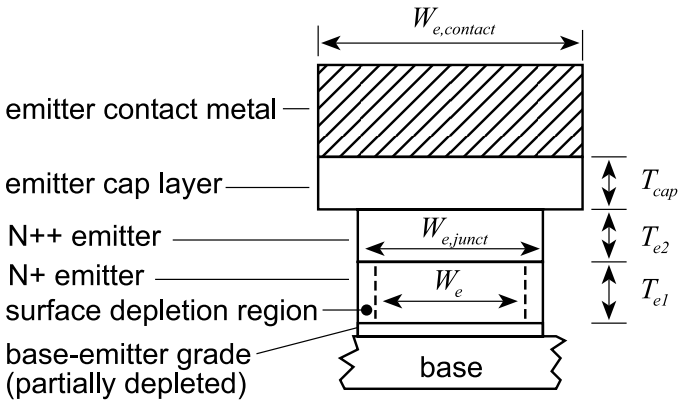


Figure 4: Cross-section of the emitter layers within a typical HBT, comprising an a heavily-doped semiconductor contact ("cap") layer, a low-resistance $N{+}{+}$ emitter layer, and the $N+$ emitter. Lateral depletion of the $N+$ emitter can be significant in submicron devices.

storage of mobile electron charge within the depletion layer, and is minimized by reducing $T_{eb}T_b$. This analysis clearly shows that the depletion region thickness cannot be indefinitely extended to reduce base-emitter junction capacitance, as charge storage in the region also contributes to the transistor's forward delay.

The delay term $R_{ex}C_{cb}$ is a major limit to HBT scaling for high f_τ. Because of the relative sizes of the emitter and collector Ohmic contacts, in a *well-designed* submicron HBT, R_c is 4:1 to 10:1 smaller than R_{ex} and R_cC_{cb} can be neglected in a first analysis. To calculate R_{ex}, we must consider the geometry of the emitter layer structure.

The emitter layer structure of a typical HBT (fig. 4) contains a heavily-doped and narrow-bandgap contact ("cap") layer, and a heavily-doped $N{+}{+}$ wide-bandgap emitter layer. A portion of the emitter layer may be more lightly ($N+$) doped for reduced junction capacitance, and may be of several hundred Å thickness to avoid dopant diffusion from the $N{+}{+}$ layer into the emitter-base junction. Accurately calculating the emitter resistance requires the consideration of the resistivity and dimensions of each of the emitter layers. For submicron emitters, the junction width $W_{e,junct}$ is significantly smaller than the contact width $W_{e,contact}$ due to lateral undercutting of the emitter during etching of the emitter-base junction. For simplicity in scaling analysis, we will approximate

$$R_{ex} \simeq \rho_e / A_e \tag{8}$$

where ρ_e is a fitted parameter, approximately $50\Omega{-}\mu\text{m}^2$ for submicron InAlAs/InGaAs HBTs fabricated to date at UCSB.

The $R_{ex}C_{cb}$ charging time can now be examined. Since $C_{cb} = \epsilon A_c / T_c$,

$$R_{ex}C_{cb} = \left(\frac{\epsilon\rho_e}{T_c}\right)\left(\frac{A_c}{A_e}\right). \tag{9}$$

This term can constitute a significant delay. In HBTs we have fabricated with 275 GHz peak f_τ, the substrate transfer process allows A_c/A_e to be kept small at 2.3:1, yet $R_{ex}C_{cb}$ still constitutes 11% of the total $1/2\pi f_\tau$ forward delay. In mesa HBTs (fig. 1) A_c/A_e is often larger than 2.3:1 and hence $R_{ex}C_{cb}$ will contribute a larger delay. Because $R_{ex}C_{cb} \propto 1/T_c$, thinning the collector to reduce τ_c also increases $R_{ex}C_{cb}$.

To increase HBT current gain cutoff frequencies, the base and collector layers must be thinned and the bias current density increased. Thinning the collector increases $R_{ex}C_{cb}$, imposing a limit to scaling. Limits to bias current density imposed by device reliability, and loss in breakdown voltage with reduced collector thickness, are two further potential limits to scaling. Finally, unless the device structure of fig. 1 is laterally scaled, vertical HBT scaling for increased f_τ will result in *reduced* power-gain cutoff frequencies f_{max}.

2.2. *Factors determining* f_{max}

In an HBT with base resistance R_{bb} and collector capacitance C_{cb}, the power-gain cutoff frequency is approximately $f_{max} \simeq (f_\tau/8\pi\tau_{cb})^{1/2}$. The base-collector junction is a distributed network, and τ_{cb} represents an effective, weighted time constant. Because the base-collector junction parasitics are distributed, calculation of τ_{cb} is complex. To simplify analysis, we will first roughly approximate $f_{max} \simeq (f_\tau/8\pi R_{bb}C_{cb})^{1/2}$, where $R_{bb}C_{cb}$ is the product of the base resistance and the full capacitance $C_{cb} = \epsilon A_c/T_c$ of the collector-base junction.

The base resistance R_{bb} is composed of the sum of contact resistance R_{cont}, base-emitter gap resistance R_{gap}, and spreading resistance under the emitter R_{spread}. With base sheet resistance ρ_s, and specific (vertical) contact access resistance ρ_v, we have

$$\begin{aligned} R_{bb} &= R_{cont} + R_{gap} + R_{spread} \\ R_{cont} &= \sqrt{\rho_s\rho_v}/2L_e \\ R_{gap} &= \rho_s W_{eb}/2L_e \\ R_{spread} &= \rho_s W_e/12L_e. \end{aligned} \tag{10}$$

The base-collector time constant is then

$$\begin{aligned} R_{bb}C_{cb} &= \left[(\sqrt{\rho_s\rho_v} + \rho_s W_{eb})\left(\frac{\epsilon}{2}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_c}{T_c}\right] \\ &+ \left[\left(\frac{\rho_s\epsilon}{12}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_c W_e}{T_c}\right]. \end{aligned} \tag{11}$$

Consider the influence of device scaling on the time constant $R_{bb}C_{cb}$. Decreasing the base thickness to reduce τ_b increases the base sheet resistivity ρ_s, increasing $R_{bb}C_{cb}$. Decreasing the collector thickness T_c to reduce τ_c directly increases $R_{bb}C_{cb}$, as is shown explicitly in eqn. 11.

Low $R_{bb}C_{cb}$, and consequently high f_{max}, is obtained by scaling the emitter and collector junction widths W_e and W_c to submicron dimensions. Reducing the emitter width W_e alone reduces towards zero the component of $R_{bb}C_{cb}$ associated with the base spreading resistance (the second term in eqn. 11). In the normal triple-mesa HBT (fig. 1), the minimum collector junction width W_c is set by the base Ohmic contacts which must be at least one contact transfer length ($L_{\text{contact}} = (\rho_v/\rho_s)^{1/2}$). As a result, the component of $R_{bb}C_{cb}$ associated with the base contact resistance (the first term in eqn. 11) has a minimum value, independent of lithographic limits, and consequently, $f_{\max}$ does not increase rapidly with scaling. Given this minimum $R_{bb}C_{cb}$, attempts to obtain high f_τ by thinning the collector have resulted in decreased f_{max}, frustrating efforts to improve HBT bandwidths.

If the parasitic collector-base junction is eliminated, f_{max} will instead increase rapidly with scaling. The collector-base junction need only be present where current flows, e.g. under the emitter. We have fabricated such a device (fig. 2) using a substrate transfer process. If we neglect processing alignment tolerances, the emitter and collector junctions can be of equal width, hence $W_c = W_e$. With submicron scaling of the emitter and collector junction widths, the first term in eqn. 11 dominates and scales as W_e. f_{max} then increases as the inverse square root of the process minimum feature size.

To more accurately predict f_{max}, the distributed nature of the base-collector junction parasitics must be considered. Figure 5 shows a distributed model of a transferred-substrate HBT. Using a small grid spacing, we have entered the resulting network into a microwave circuit simulator (HP-EESOF [27]) to calculate –without approximation– the HBT f_{max}. Alternatively, analytic expressions for f_{max} can be developed from hand analysis of the distributed network of fig. 5. Among these is the model of Vaidyanathan and Pulfrey [28], which provides good physical insight. We now consider the Vaidyanathan/Pulfrey model applied to a transferred-substrate HBT [29].

Figure 6 shows an equivalent circuit representing the Vaidyanathan/Pulfrey model of a transferred-substrate HBT. We define three capacitances. $C_{cb,e} = \epsilon L_e W_e/T_c$ is the capacitance of the collector junction lying under the emitter. $C_{cb,gap} = 2\epsilon L_e W_{eb}/T_c$ is the capacitance of the collector junction lying under the gap between the emitter and the base contact. $C_{cb,ext} = 2\epsilon L_e W_{cb}/T_c$ is the capacitance of the collector lying under the base Ohmic contacts. Components of the base resistance are as defined in eqn. 10, with the exception of two additional resistances $R_{vert} = \rho_v/2W_{cb}L_e$, and $R_{horiz} = \rho_s W_{cb}/2L_e$. R_{vert} represents the vertical access resistance through the base Ohmic contact over the path W_{cb}, and R_{horiz} represents the lateral sheet resistance over that same path.

The R_{vert}/R_{horiz} network approximates the distributed network charging $C_{cb,ext}$

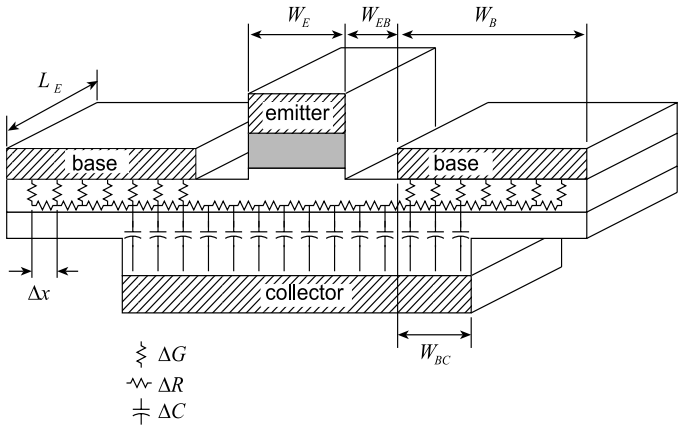


Figure 5: Distributed model of the HBT base-collector junction for accurate calculation of $R_{bb}C_{cbi}$. With mesh spacing Δx, $\Delta G = L_e\Delta x/\rho_c$, $\Delta R = \rho_s\Delta x/L_e$, and $\Delta C = \epsilon L_e\Delta x/T_c$

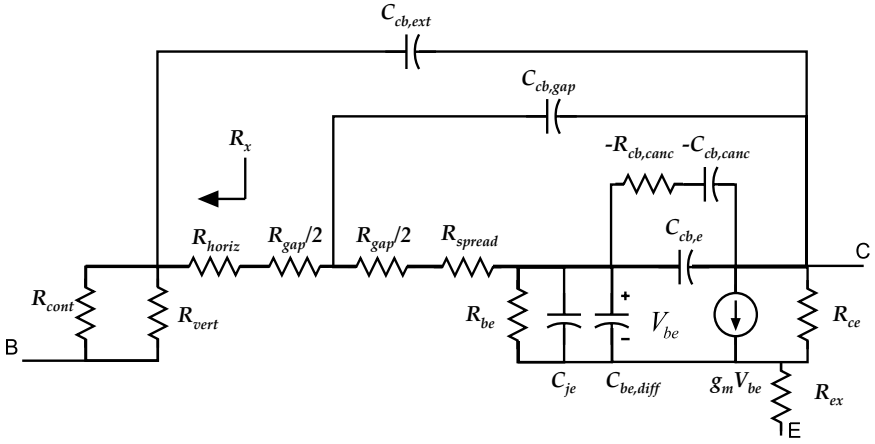


Figure 6: Lumped element circuit approximating the transistor mesh model of fig. 5. Terms $R_{cb,canc}$ and $C_{cb,canc}$ represent capacitance cancellation effect described by eqn. 16.

in the mesh model of fig. 5. This approximation is valid under the condition that $W_{cb} \leq L_{contact}$. If this condition does not hold, R_{vert} and R_{horiz} must be replaced by a finite element ladder network with a larger number of discrete elements, as in fig. 5. The model of fig. 6 further assumes that the total base width $W_b >> L_{contact}$. Typical geometries of transferred-substrates HBTs meet both of the aforementioned assumptions.

From fig. 6, we note that charging resistance seen by $C_{cb,e}$ and $C_{cb,gap}$ contains the component $R_x = R_{cont} \parallel R_{vert} + R_{horiz} = R_{cont}$. While the simplified lumped element model of fig. 6 approximates fig. 5 only if $W_{cb} \leq L_{contact}$, the relationship $R_x = R_{cont}$ is in general true even for $W_{cb} > L_{contact}$, as are the expressions for f_{max} presented below.

In the limit of zero collector series resistance, Vaidyanathan and Pulfrey's model, [28], [29] reduces to

$$f_{max} = \sqrt{\frac{f'_\tau}{8\pi\tau_{cb}}}, \tag{12}$$

where

$$\frac{1}{2\pi f'_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}\,(C_{je} + C_{cb}), \tag{13}$$

and

$$\begin{aligned} \tau_{cb} &= C_{cb,e}\,(R_{cont} + R_{gap} + R_{spread}) \\ &+ C_{cb,gap}\,(R_{cont} + R_{gap}/2) \\ &+ (R_{cont} \| R_{vert})\,C_{cb,ext} \end{aligned} \tag{14}$$

The model of fig. 6 accurately represents the distributed nature of the collector-base junction. We can approximate this network with the simple hybrid-π model of fig. 3 if we select C_{cbi} such that the correct transistor f_{max} is obtained. The components of fig. 3 are then given by $C_{cbi} = \tau_{cb}/R_{bb}$ and $C_{cbx} = C_{cb} - C_{cbi}$, where $C_{cb} = C_{cb,e} + C_{cb,gap} + C_{cb,ext}$.

Figure 7 compares the f_{max} of mesa and transferred-substrate HBTs, computed using the finite-element model. For the transferred-substrate device, f_{max} increases rapidly with deep submicron scaling. Experimentally, we observe a more rapid variation of predicted f_{max} with collector width than is shown, and fig. 7 predicts a higher f_{max} than is experimentally observed for mesa HBTs. Series resistance in the base metallization and collector series resistance [28] (not modeled above, and not present in Schottky-collector transferred-substrate HBTs) are possible explanations for the discrepancy.

At high collector current densities, differential space-charge effects in the collector space-charge region result in $C_{cb,e}$ smaller than $\epsilon A_e/T_c$, and increase the HBT f_{max} [30], [31]. In III-V materials at high fields, electron velocity $v(\mathcal{E})$ decreases with increasing electric field. Modulating the collector voltage V_{cb} modulates the collector transit time τ_c (eqn. 3), and partially modulates the space-charge in the

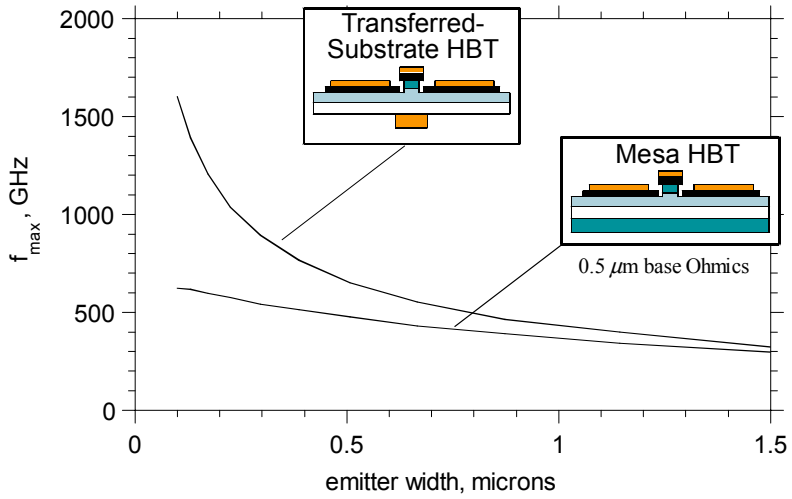


Figure 7: f_{max} calculated using finite-element model of the collector-base junction for transferred-substrate and mesa HBTs. Device parameters are same as fig 13.

collector drift region. This modulated space-charge partially screens the base from modulations in the collector applied field, and $C_{cb,e}$ is reduced to [31]

$$C_{cb,e} \quad = \quad \epsilon A_e/T_c - I_c \frac{d\tau_c}{dV_{cb}} \tag{15}$$

where $\epsilon\ A_e\ /\ T_c$ is the normal dielectric capacitance of the junction. Experimental data confirming C_{cb} cancellation will be shown in section 5.

The derivation of eqn. 15 is limited by the charge control assumption that changes in carrier concentration occur instantaneously. Clearly, this is not valid at frequencies approaching the inverse of the collector transit time. We now describe the dynamics of capacitance cancellation to first order in frequency, assuming a simplified velocity dependence $1/v(\mathcal{E}) \simeq \kappa_0 + \kappa_1 \mathcal{E}$. We further assume that the electric field induced by mobile collector charge is small compared to both the DC and AC applied field across the collector-base junction. Using a formalism similar to [20], [21], [31] it can then be shown that

$$\frac{dQ}{dV_{cb}} = \epsilon A_e/T_c - I_c \frac{d\tau_c}{dV_{cb}} \frac{1}{[1 + j\omega(2/3)\tau_c]} \tag{16}$$

where $d\tau_c/dV_{cb} = \kappa_1/2$. The term -$I_c$ $d\tau_c/dV_{cb}$ is the capacitance cancellation of eqn 15, while the terms in $j\omega$ represent the dynamics of this effect. The differential

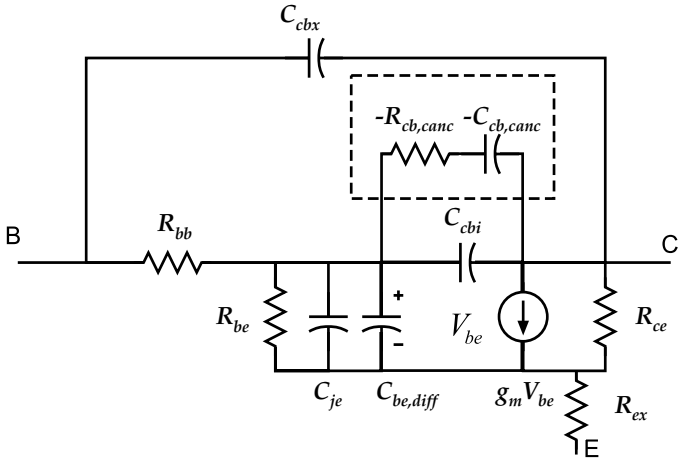


Figure 8: Modified hybrid-π small-signal HBT equivalent circuit with additional negative capacitance $C_{cb,canc}$ and negative resistance $R_{cb,canc}$ elements to account for dynamics of capacitance cancellation.

equation of eqn. 16 can be represented by an equivalent circuit model consisting of the dielectric junction capacitance $C_{cb,e}$ in parallel with the negative capacitance cancellation term, $C_{cb,canc} = -I_c \; d\tau_c/dV_{cb}$, in series with a negative resistance, $R_{cb,canc} = (3/2)\tau_c/C_{cb,canc}$. These terms are included in the Vaidyanathan/Pulfrey transistor model of fig. 6. We note that $C_{cb,canc}$ and $R_{cb,canc}$ are charged through the total base resistance $(R_{b,cont} + R_{gap} + R_{spread})$. The elements $C_{cb,canc}$ and $R_{cb,canc}$ can therefore appear in the approximate hybrid-π model appearing in shunt across C_{cbi}. A revised hybrid-π model including the capacitance cancellation terms is shown in fig. 8.

We caution that this derivation models only to the first order in frequency the dynamics of the space-charge redistribution in the collector region. However, the method, though approximate, is sufficient to predict that negative resistance effects should be observed, and may explain device results presented in section 5.1.

3. Transferred-substrate HBTs

We now consider the transferred-substrate process as a means of realizing a highly scalable HBT. Substrate transfer provides access to both sides of the device epitaxial material, which allows for the simultaneous definition of narrow emitter and collector stripes. With the extrinsic collector-base capacitance greatly reduced, aggressive lithographic scaling *without* epitaxial scaling greatly increases f_{max} at constant f_τ. If high values of both f_τ and f_{max} are sought, simultaneous lithographic and epitaxial scaling is required. Further improvements in device bandwidth will require operation at higher current densities and reduced emitter parasitic resistance.

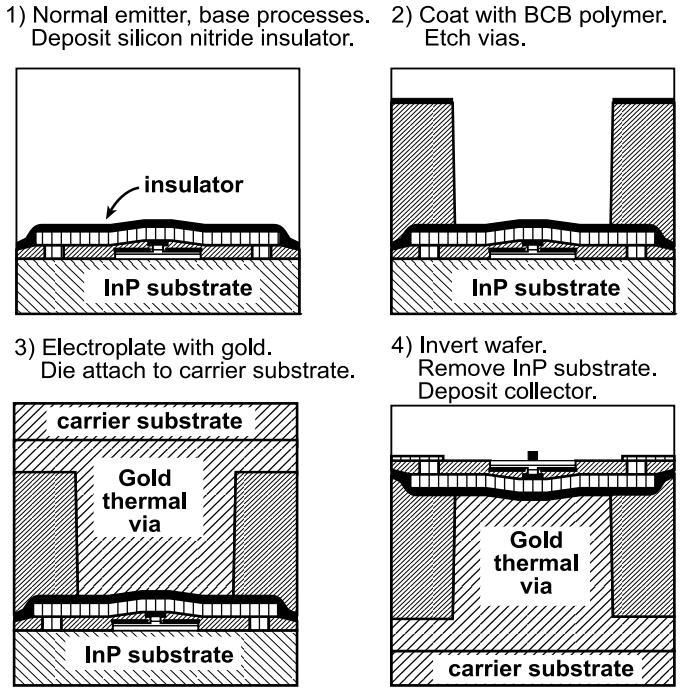


Figure 9: Transferred-substrate HBT process flow.

3.1. *Growth and fabrication*

The MBE epitaxial structure is grown on a Fe-doped semi-insulating InP substrates. Both single and double heterojunction transistors have been fabricated in the transferred-substrate technology. The single heterojunction transistors have an InAlAs/InGaAs emitter-base junction. The double heterojunction devices have an InP collector for increased breakdown, and may have an InP emitter for improved heat flow in the device. A chirped superlattice grade is used to smooth conduction band discontiniuties at the heterojunctions. The InGaAs base is typically 300–400 Å thick, has $2kT$ bandgap grading, and is Be-doped at $5{\times}10^{19}/\mathrm{cm}^3$. The transistor collector thickness is typically 2000-3000 Å and a N^+ pulse-doped layer placed 400 Å from the base delays the onset of base push-out at high collector current densities. High f_{max} devices are typically fabricated with Schottky collector contacts which provide zero collector series resistance [33].

Figure 9 shows the process flow. Standard fabrication processes [34] define the emitter-base junction, the base mesa, polyimide planarization, and the emitter contacts. The IC wiring environment consists of thin-film NiCr resistors, two levels of metal interconnects, and a PECVD Si_3N_4 insulator layer for MIM capacitors. The substrate transfer process commences with deposition the Benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness). Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metallize the vias and to form the ground

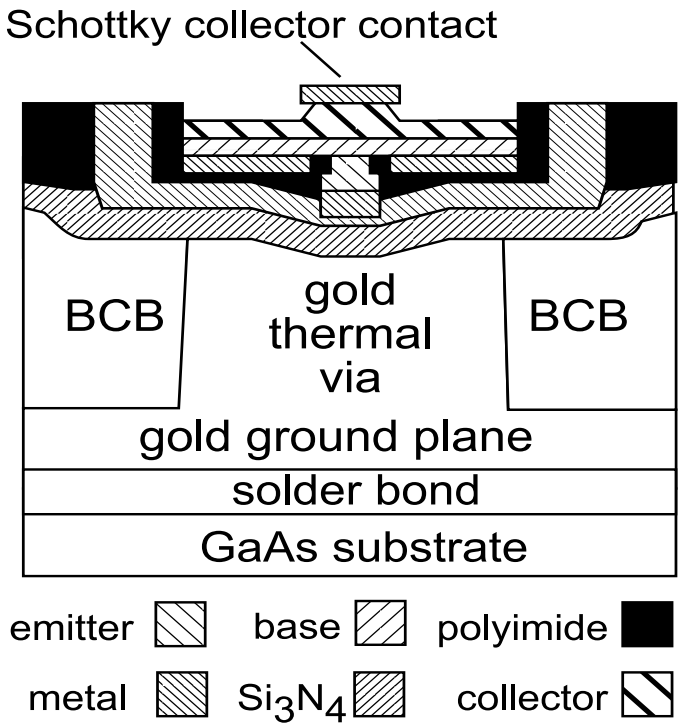
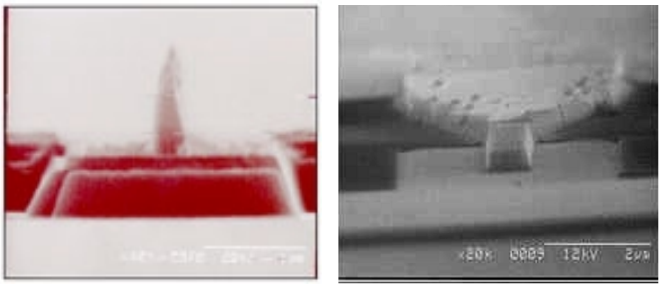


Figure 10: Schematic cross-section of a transferred-substrate HBT

plane. The wafer is then solder-bonded to a GaAs or AlN carrier substrate. The InP substrate is removed in HCl and Schottky collectors are deposited, completing the process. Fig. 10 shows a detailed device cross section.

Minimum device feature sizes are determine by the lithography system used in the process. The projection lithography system at UCSB can define emitter widths down to 0.5 μm. The relative sizes of the emitter and collector junctions are determined by lithographic alignment tolerances, and the collector stripe width must exceed the emitter stripe width by twice the lithographic alignment tolerance. Our projection lithography system aligns to 0.1–0.3 μm registration, depending on the time since maintenance. For deep submicron devices, a JEOL JBX electron-beam lithograpy system at UCSB is used. With this system, 0.2 μm emitter and 0.3 μm collector stripe widths have been realized. Collector alignment of better than 0.1 μm is acheived using local registration marks for each device.

For the emitter-base junction, deep submicron scaling requires tight control of lateral undercutting during the base contact recess etch. The undercut both narrows the emitter and defines the liftoff edge in the self-aligned base contact deposition. For InAlAs emitters, a combination dry and wet etch is used. A CH_4 / H_2 / Ar dry etch removes the N^+ InGaAs emitter contact layer and etches into the InAlAs emitter. A HCl/HBr/Acetic selective wet etch then removes the InAlAs



(a) (b)

Figure 11: E-beam HBT: HBT structure with 0.3 μm emitter-base junction (a), and 0.7 μm Schottky collector stripe (b)

emitter, stopping on the InAlAs/InGaAs emitter-base grade. A timed nonselective wet Citric/H_3PO_4/H_2O_2 etch then removes the base-emitter grade, etching ∼100 Å into the emitter. For recently fabricated InP emitter devices, an all wet etch process has been employed. A H_2O_2/H_3PO_4 etch removes the N^+ InGaAs emitter contact layer stopping on the InP emitter. A selective HCl/H_3PO_4 etch then removes the emitter semiconductor again stopping in the emitter-base grade. The same nonselective etch used for the InAlAs emitter is then used to etch into the base. For both emitter etch processes, a well controlled undercut of 0.1 μm is acheived.

The collector junction is defined by the stripe width of the deposited metal. Subsequent to collector deposition, a self-aligned wet etch of ∼1000 Å depth removes the collector junction sidewalls (eliminating fringing fields) and reduces the collector junction width by ∼2000 Å.

4. High Frequency Device Measurements

Prior to discussing transferred-substrate device results, we will consider issues related to high frequency device measurements. Submicron transistors have extremely small reverse transmission characteristics and low shunt output conductances. These features make device measurement and model extraction challenging even in the DC-50 GHz band covered by typical commercial vector network analyzers (VNAs). As state-of-the art transistor bandwidths far exceed this frequency range, we would like to measure device scattering parameters (S-parameters) at as high a frequency as possible. Presently, VNA test set extensions are available covering frequencies up to 220 GHz, and 325 GHz systems will soon be available.

Accurate device measurements at these frequencies requires that careful attention be paid to measurement and calibration methodology.

4.1. *Ultra-high frequency measurement systems*

The 140-220 GHz VNA measurement system used at UCSB consists of an Agilent HP8510C network analyzer interfaced with Oleson Microwave Lab millimeter wave VNA extensions. Frequency synthesizers in the VNA test system generate 17.5-27.5 GHz RF and 11.6-18.4 GHz LO signals that are sent to the Oleson extenders through microwave coaxial cables. A harmonic multiplier chain in the extenders upconverts the RF signal to the measurement frequency, and harmonic mixers downconvert stimulus and response signals obtained from a dual directional coupler at the extender's test ports. The IF signals ($<$ 300 MHz) are then sent back to the VNA for processing. Full two-port transmission and reflection measurements can be obtained with this system, and the dynamic range is greater than 50 dB. The test ports of the extenders are connected to on-wafer probes through short lengths of WR-5 rectangular waveguide. Due to the relatively high loss of the waveguide (12 dB/m), it is important to keep the the connection length as short as possible to preserve the measurement system's dynamic range. At UCSB, $\sim$ 50 cm of waveguide with two right angle bends is used. This arrangement is found to provide adequate loss and sufficient range of motion for probe manipulation. GGB Industries ground-signal-ground wafer probes are mounted onto probe station micromanipulators. A waveguide-to-microcoax transition is internal to the probes, and the insertion loss of the probes is better than 3 dB across the band. Internal bias-tees in the wafer probes allow for biasing of active devices through the center probe conductor.

4.2. *On-wafer calibration*

To underscore the importance of measurement calibration for submicron device measurements, consider that a state-of-the-art InP HBT with a 300 GHz f_τ has a total forward delay of 0.53 psec, the same delay as $\sim$ 100 μm length of transmission line in our on-wafer transmission line environment (ϵ_{eff}=2.2). One sees the importance of removing from transistor measurements the effects of all extraneous propagation delays and losses incurred in the measurment system up to the device under test.

An accurate VNA calibration will place the measurement reference planes precisely at the input and output of the device under test. However, standard 12-term VNA error corrections do not account for leakage and coupling between on-wafer probes. Highly scaled transistors have extremely small reverse transmission characteristics (S12) and excessive probe-to-probe coupling can easily corrupt device measurements. Probe-to-probe leakage can be accounted for using more complicated 15- or 16- term VNA error corrections [35], [36]. However, these corrections require precise characterization of calibration standards, and such characterizations are difficult to achieve for on-wafer elements, particularly at mm-wave frequencies.

The use of 15- or 16- term error corrections can be avoided if the wafer probes are spaced far enough apart to provide sufficient isolation. Probe isolation that is at least 20 dB lower than S12 of the transistor is sufficient for accurate device characterization [37]. Separation between wafer probes is achieved by adding lengths of 50 Ω on-wafer transmission line to the input and output of the device. At UCSB, a length of 230 μm transmission line at each port has been found to provide sufficient isolation.

Calibrating the network analyzer involves the measurement of various known calibration standards. A standard approach for device measurements is to utilize a separate calibration substrate that has on it an array of characterized calibration standards. These substrates are available commercially and cover various frequency ranges up to 110 GHz. The goal of these calibrations is to place the measurement reference planes at the wafer probe tips. There are several drawbacks to using this approach for precise device measurements.

As previously mentioned, the transistor is embedded on-wafer between lengths of transmission line. If we use a probe tip calibration, the effect of the embedding structures must be eliminated from the transistor measurements. An ad hoc approach often used is to measure the capacitance of an open circuit test structure and subtract this capacitance from the measured results. This approach can lead to considerable error as the pad capacitance may be of the same order as the input capacitance of a submicron device. This approach also ignores the series resistance of the embedding structure, and the series inductance which will have a considerable effect at mm-wave frequencies. A more precise determination of the electrical characteristics of the embedding structures may made by modeling the structures electromagnetically, or by measuring the test structures without devices and fitting the results to a lumped element model. In either case, this adds a level of complexity and the opportunity for further error in extracting device parameters.

The second drawback of probe-tip calibration approach is that calibration substrates generally have a different transmission line environment than the device under test [38]. A standard VNA calibration assumes that only a single propagation mode exists at the calibration reference plane for both measurement and calibration. The discontinuity at the probe/wafer interface does not meet these conditions, and the field distribution at the discontinuity will depend on the transmission line environment that is being coupled into. As such, the probe-tip calibration on the calibration substrate need not apply to the substrate of the device under test. We expect discrepancies to increase at higher frequencies as the wavelength approaches the size of the probe tips.

The alternative to probe-tip calibration is to calibrate to the ends of the on-wafer transmission lines. This places the measurement reference planes at the input and output of the device under test, but requires the realization of custom on-wafer calibration standards. Depending on the calibration used, different types of standards are required. Certain VNA calibrations, such as the commonly used Short-Open-Load-Through (SOLT) calibration, require precise characterization of

the electrical properties of the standards. Fringing fields and the distributed nature of the elements at mm-wave frequencies require that the elements be modeled electromagnetically or measured using an accurate on-wafer calibration. Again, this adds a level of complexity and the opportunity for further error in extracting device parameters.

The Through-Reflect-Line (TRL) calibration is well-suited for an on-wafer measurement environment [39]. The calibration uses two transmission line standards one of which is designated "through", the other is designated "line" and differs from the through line by some electrical length ΔL. The final "reflect" standard may be an open or short termination. An advantage of the TRL calibration is that the solution for the calibration error terms is overdetermined, and the reflection coefficient of the reflect standard and propagation constant of the line standard can also be calculated. The only physical property that must be known is the characteristic impedance of the line standard. The characteristic impedance can be determined analytically from transmission line models or electromagnetic simulations, or alternatively, it can be calculated from measurements of the line's capacitance and propagation constant [40], [41]. It is important to note that line loss will lead to a characteristic impedance that has frequency dependent real and imaginary parts. The imaginary part can be large at low frequencies and should be accounted for in the measurement calibration.

An often cited disadvantage of the TRL calibration is that one line standard can only cover a 1:8 frequency span, with the ideal ΔL being a quarter-wavelength at the center of the span. As such, multiple line standards are required to cover large frequency ranges, and low frequency line standards can take up a large amount of valuable wafer area. Multiple line standards may also be used to provide measurement redundancy in a band, and reduce the error due to probe placement repeatability [42].

Quantitatively assesing the accuracy of a microwave calibration is difficult. To partially verify the calibration accuracy, we have re-measured calibration standards after calibration in the 75-110 GHz and 140-220 GHz bands. Measurement of a through standard after calibration gives an indication of probe-placement repeatability, as the calibration defines the measurement reference planes to be at the center of the through line. In the 75-110 GHz band, the measurement of a through line showed better than 35 dB return loss, and S21 had < 0.2 dB amplitude variation and < 0.3 degrees of phase variation. In the 140-220 GHz band, measurement of a through line showed better than 30 dB return loss, and S21 had < 0.1 dB amplitude variation and < 1 degree of phase variation. As discussed previously, the TRL calibration does not assume a known reflection coefficient of the reflect standard. Measurement of the short or open reflection standard after calibration, therefore, provides a good indication of the quality of the calibration. In the 75-110 GHz band, measurement of the open standard showed < 0.25 dB amplitude variation and $<$ 1.5 degrees of phase variation. In the 140-220 GHz band, the calibration appeared slightly poorer. Measurement of the open standard showed < 0.4 dB amplitude

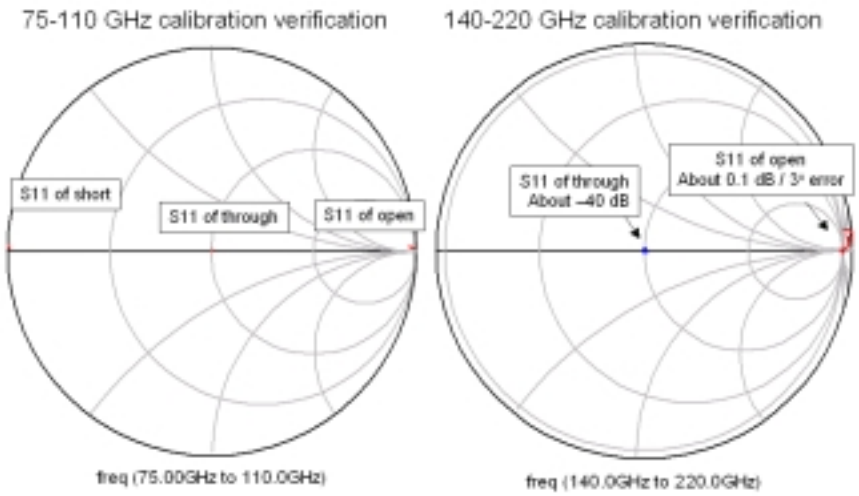


Figure 12: Calibration verifcation in the 75-110, and 140-220 Ghz bands. In the 75-110 GHz band, the accuracy is shuch taht the short, open and thru standards appear as barely-visible dots in the correct locations of the Smith chart.

variation and < 3 degrees of phase variation. Figure 12 shows measurements on a Smith chart of the calibration standards in both frequency bands.

Independent of re-measuring the calibration standards, a quantitative estimate of calibration accuracy would require measurement of known on-wafer elements. Measurements, to be presented in Section 6, show excellent agreement between electromagnetic simulations of passive matching network elements and measured results. Additionally, device measurements presented in the next section show smooth variation across all frequency bands.

5. Device Results

Depending on the circuit application transferred-substrate devices can be aggressively laterally-scaled for ultra-high f_{max}, or both laterally and vertically scaled for simultaneously high values of f_{max} and f_τ. As we are concerned here with high frequency tuned circuit applications, we will consider only those devices scaled for high f_{max}. These devices are typically fabricated with 400 Å base thicknesses for low base resistance, and 3000 Å thick collectors for low collector-base capacitance. This results in moderate, not high, f_τ.

Figure 13 shows microwave gains for a deep submicron single heterojunction transistor fabricated using electron-beam lithography, reported by Lee *et. al.* [43].

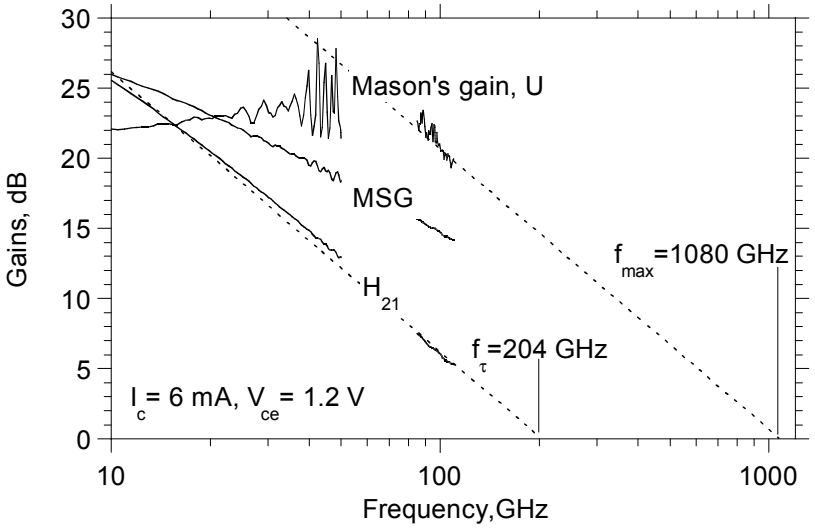


Figure 13: Gains of a 0.4 μm $\times$ 6 μm emitter and 0.7 μm $\times$ 10 μm collector HBT fabricated using electron-beam lithography. Theoretical -20 dB/decade (H_{21}, U) gain slopes are indicated. The device exhibits an *extrapolated* 1.08 THz f_{max}

The emitter and collector junction dimensions are 0.4 μm $\times$ 6 μm and 0.7 μm $\times$ 10 μm, respectively. The measurements were made in the 10-50 GHz and 75-110 GHz frequency bands using the TRL calibration described in the previous section. At the time these measurements were made, the 140-220 GHz measurement set-up had not yet been obtained. With the device biased at $V_{ce} = 1.2$ V and $I_c = 6$ mA ($J_e = 2.5 \times 10^5$ A/cm^2), the transistor exhibits an extrapolated f_τ of 204 GHz. Mason's invariant (unilateral) power gain is measured to be greater than 20 dB at 100 GHz. If we extrapolate at -20 dB/decade, an f_{max} of > 1 THz is predicted. However, recent device measurements have indicated that highly scaled devices do not show a well behaved roll-off with frequency in the unilateral gain. Prior to considering these device measurements, we discuss the use of the Mason's gain to predict transistor f_{max}.

For a general two-port network Mason's invariant (unilateral) power gain is given by [44]

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{12}G_{21})} \tag{17}$$

where Y_{21} and Y_{12} are network admittance parameters, and G_{11}, G_{22}, G_{12}, and G_{21} are the real parts of the admittance parameters. Mason's gain represents the power gain available from a network if it is unilateralized (reverse transmission =

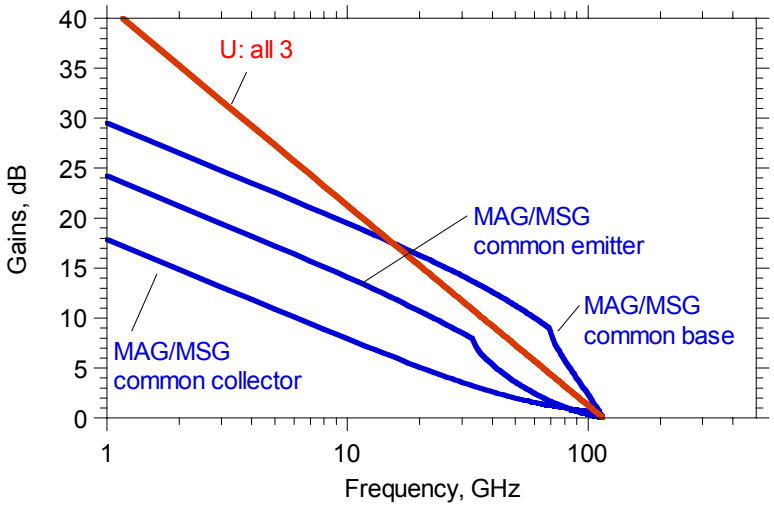


Figure 14: Variation of transistor gains with frequency, computed from a hybrid-π HBT model. Shown are the maximum available / maximum stable gains (MAG/MSG) in common-emitter, common-base, and common collector mode, and Mason's invariant, U, the unilateral gain

0) using lossless reactive feedback. The gain is invariant with respect to embedding the device in a lossless reciprocal network, and consequently is independent of pad inductive or capacitive parasitics and independent of the transistor configuration (common-emitter vs. common-base). For HBTs well-modeled by a hybrid-π equivalent circuit fig. 3, Mason's gain conforms closely to a -20 dB/decade variation with frequency (fig. 14). In marked contrast, the maximum available / maximum stable gain is a function of the transistor configuration, and shows no fixed variation with frequency. f_{max} is unique; at $f = f_{max}$ the MAG/MSG and U are both 0 dB.

Figure 15 shows microwave gains for a recently-fabricated submicron HBT. The emitter and collector junction dimensions are 0.3 μm $\times$ 18 μm and 0.7 μm $\times$ 18.4 μm, respectively. The device was characterized in the 6-45, 75-110, and 140-220 GHz frequency bands. The device is biased at $V_{ce} = 1.1$ V and $I_c = 5$ mA ($J_e = 1.1 \times 10^5$ A/cm^2). The transistor measurements show a negative unilateral power gain across across the 75-110 GHz band and over parts of the 140-220 GHz band. Above $\simeq$ 45 GHz, the unilateral power gain increases to infinity, and then becomes negative, a condition under which the addition of an appropriate small resistive attenuation results in infinite U.

From eqn. 17 we see that the denominator of the expression for Mason's gain

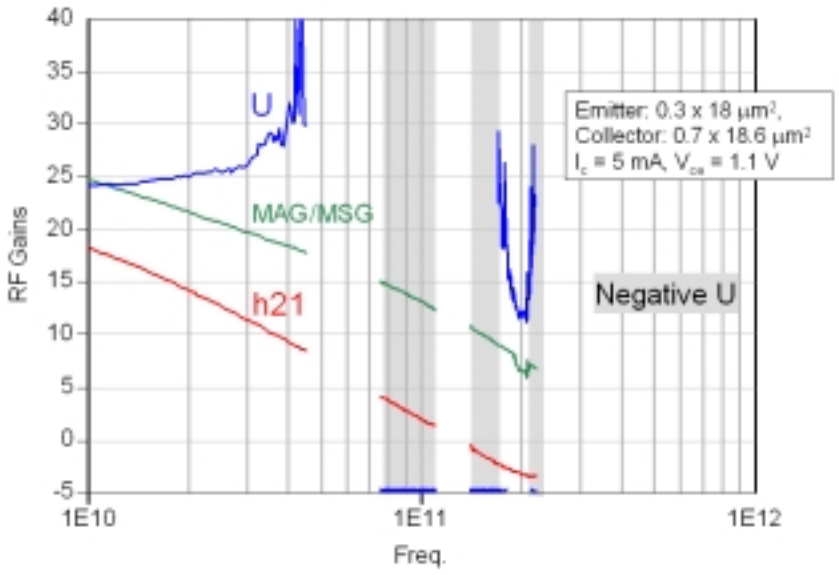


Figure 15: Gains of recently fabricated submicron HBT. In the indicated frequency bands, Mason's unilateral power gain U is unbounded as a result of a small negative output conductance G_{22}

can be negative if a device has a negative real output conductance G_{22} or a positive real feedback term G_{12}. The transistor of fig. 15 exhibits a *very* small negative output conductance that peaks at approximately -1 mS, leading to the observed negative unilateral gain. An HBT modeled by the hybrid-π transistor model cannot show a negative output conductance. We speculate that the effect arises from small secondary HBT transport effects in the collector region, either through the dynamics of base-collector capacitance cancellation as described in Section 2.2, or through weak IMPATT effects in the collector depletion region. These effects would not be seen in a typical III-V HBT because of the large positive output conductance arising from high-frequency feedback through R_{bb} and C_{cb}. In contrast, submicron transferred-substrate HBTs have an extremely small $R_{bb}C_{cbi}$ time constant, and such effects can be observed.

The dynamics of capacitance cancellation may well be the cause of the negative unilateral gain. A dramatic decrease in measured base-collector capacitance is observed with increased bias current. The *total* collector-base capacitance C_{cb} is determined from the measured variation with frequency of the imaginary part of the admittance parameter $\Im[Y_{12}] = j\omega C_{cb}$. The total C_{cb} determined from Y_{12} (fig. 17) shows a 2.4 fF decrease between 0.5 mA and 5 mA I_c. The decrease in C_{cb} results in greatly increased power gains at higher bias currents. Adding a series

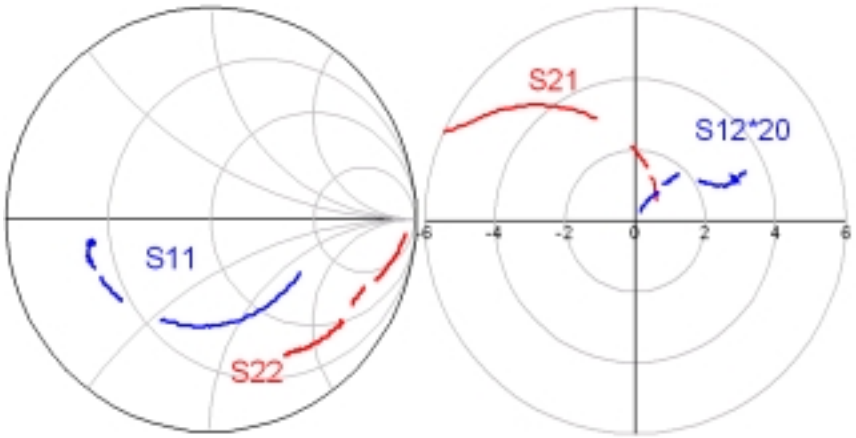


Figure 16: Measured S-parameters in 6-45, 75-110, and 140-220 GHz bands of transferred substrate HBT of fig. 16

negative resistance and negative capacitance across the base-collector of a hybrid-π transistor model with an RC time constant of 2 $\tau_c/3$, as shown in fig. 8, produces a device model with a negative output conductance. However, as of yet, we have been unable to fit a physically-based model of the dynamics of capacitance cancellation to measured S-parameters.

Another possible explanation for the negative output conductance is systematic errors in the microwave measurements. As discussed in sec. 4, a great deal of work in our group has been put towards developing an accurate calibration methodology. However, measurements of U are inherently difficult, as both products in the denominator of eqn. 17 approach zero for an HBT with small collector-base parasitics. Note that the transistor measurements showed little variation over a number of measurements with different calibrations. Further, the negative output conductance was observed for numerous devices of the same dimensions on the wafer. The transistor S-parameters also show relatively smooth variation across all of the measured frequency bands (fig. 16), showing no evidence of resonances or calibration artifacts. Ultimately, we hope to find further evidence of negative unilateral power gain in next-generation transistor designs.

A consequence of the observation of negative U is that we cannot predict f_{max} of these highly scaled devices from a -20 dB/decade extrapolation. Nevertheless, the maximum stable / maximum available gain of these devices is very high even at

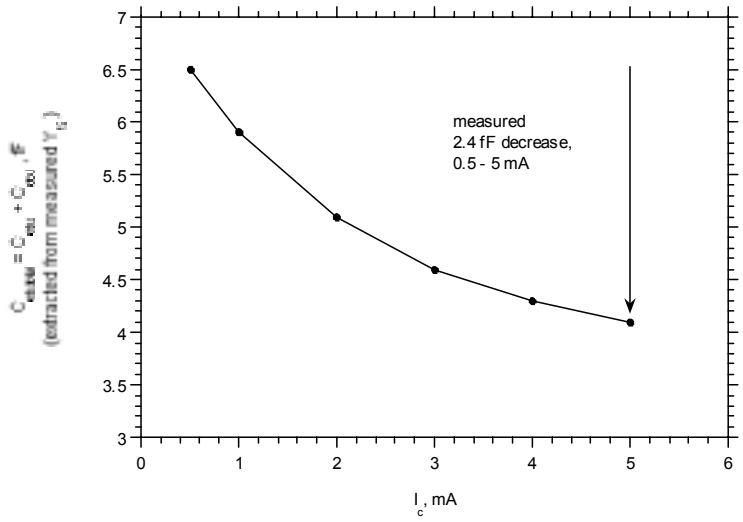


Figure 17: Collector-base capacitance extracted from Y_{12}, vs. emitter current

200 GHz. Ultimately, a higher frequency network analyzer and/or the development of higher-frequency amplifiers and oscillators is necessary to determine the usable bandwidth of the devices.

The results described above were for single heterojunction devices with a narrow bandgap InGaAs collectors. Recently, double heterojunction transistors have been fabricated with InP collectors for increased voltage breakdown. Figure 18 shows microwave gains and DC I-V characteristics for a double heterojunction transferred-substrate device with a 3000 Å thick collector [16]. The emitter and collector junctions are 0.4 μm $\times$ 8 μm and 1.2 μm $\times$ 8.75 μm, respectively. The device has extrapolated cutoff frequencies of f_τ = 139 GHz and f_{max} = 425 GHz. The common emitter breakdown voltage BV_{CEO} is 8 V at $J_e = 5.0 \times 10^4$ A/cm^2. The negative output conductance observed in single-heterojunction devices has not been observed in double heterojunction devices, possibly because these devices have not yet been scaled to deep submicron dimensions with e-beam lithography.

Using the double heterojunction process large area power transistors have recently been fabricated. A multi-finger common-base device with a total emitter area of 128 μm has been measured with an extrapolated f_{max} of 330 GHz [45]. The transistor has a breakdown voltage of 7 V and a maximum collector current of I_c = 100 mA. These power transistors are being used for W-band power amplifiers.

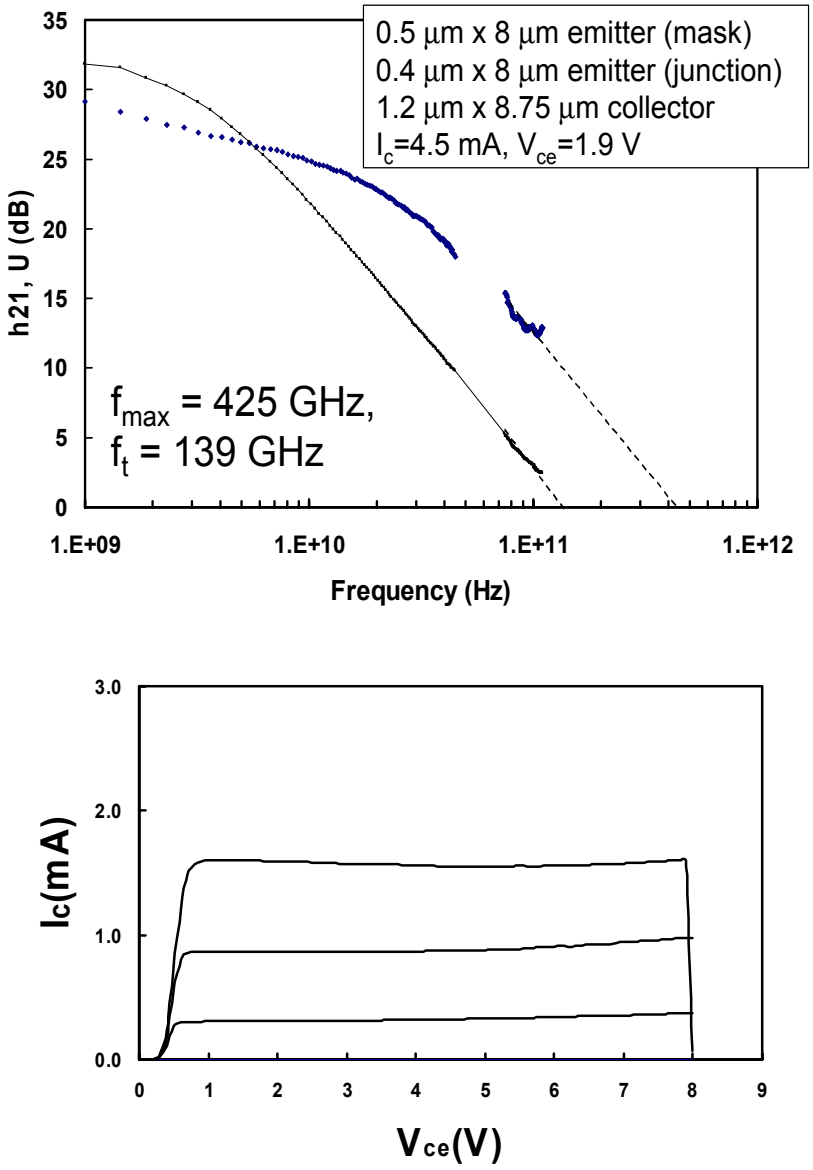


Figure 18: RF gains and DC I-V characteristics of double-heterojunction transistor

5.1. *Device modeling*

Figure 19 shows a small-signal hybrid-π model derived from 6-45 GHz measurements of a submicron HBT. The transistor had a 0.4 μm $\times$ 6 μm emitter junction area and 0.7 μm $\times$ 6.4 μm collector junction area. The model is for a bias condition of $V_{ce} = 1.2$ V and $I_c = 3.6$ mA ($J_e = 1.5 \times 10^5$ A/cm^2). To develop the model, the transistor S-parameters are measured at various DC bias conditions, and the measured Y-parameters are analyzed to extract the bias-dependent parameters, such as the transconductance and emitter-base diffusion capacitance, and the bias-indepent terms, such as the extrinsic emitter resistance.

In general, we observe that the hybrid-π model of a submicron HBT shows good correlation with measured S-parameters, h_{21}, and U in the DC-50 and 75-110 GHz bands [43]. The model parameters are also consistent with measured bulk and sheet resistivities and junction capacitances. Base-width modulation in HBTs is negligible, hence R_{ce} is very large. $C_{be,poly}$ is a metal-polyimide-metal overlap capacitance between the emitter and base contacts (sec. 10).

As previously discussed, the negative output conductance observed in recently fabricated submicron devices cannot be modeled with a standard hybrid-π model. Additionally, we have found that device models developed in the 6-45 GHz band show poor agreement with measured device parameters in the 140-220 GHz band. Figure 20 shows measured and modeled S_{11} and S_{22} in the 6-45 GHz and 140-220 GHz bands for the transistor of fig. 19. S_{12} and S_{21} are omitted from the graph for clarity, but show similiar discrepancy in the 140-220 GHz band. The poor agreement between model and measurements in the higher frequency band points to a weakness in extending the simple hybrid-π model to these frequencies.

The results of fig. 20 are for a highly scaled device and the discrepancy may be due to collector-transport effects not included in the model. Comparison of model and measurements for less highly scaled devices in the 140-220 GHz band have not been made at the time of this writing, and to the best of our knowledge no work has been done to characterize mesa HBTs in the 140-220 GHz band. It should be noted that the hybrid-π model approximates to first order in frequency the base and collector transit time effects. In contrast, the T-model (common-base) does not require such approximations. We note, however, that a T-model of the device, developed from 6-45 GHz measurements, also could not fit the measured S-parameters in the 140-220 GHz band.

At the time of this writing, a physically justifiable small-signal device model has not been developed for the 140-220 GHz band. This further complicates estimations of transistor bandwidth, as we cannot predict the power gain roll-off versus frequency. Higher frequency amplifier and oscillator designs will also be limited by the lack of a predictive model.

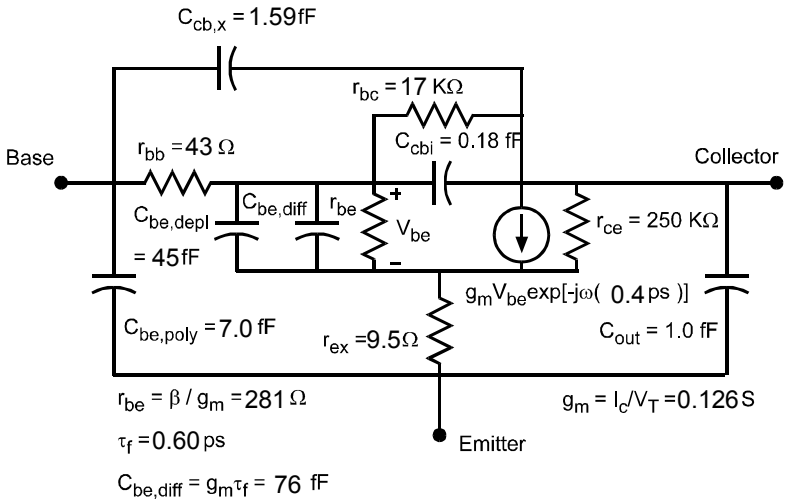


Figure 19: Device equivalent circuit model at $V_{ce} = 1.2$ V and $I_c = 3.6$ mA.

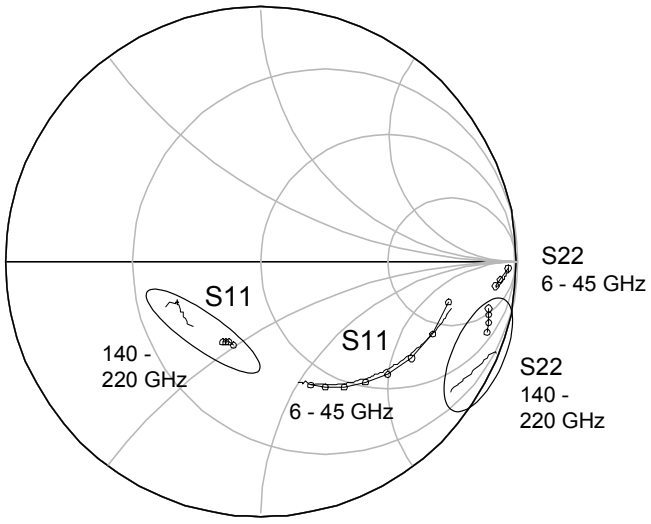


Figure 20: Measured (solid line) and modeled (circles) S11 and S22 in 6–45 GHz and 140–220 GHz bands of device of fig. 19.

6. HBT Amplifiers

6.1. *Amplifier Design*

Wideband analog amplifiers and high frequency tuned amplifiers have been fabricated in the transferred-substrate HBT technology. Prior to presenting amplifier results, we consider some of the design issues faced specifically in ultra-high frequency tuned amplifiers.

Because of process complexity and yield issues, first generation tuned amplifier designs have emphasized simple design strategies and low transistor counts. Circuit design is performed using Agilent's Advanced Design System software [46]. Small-signal transistor models are developed in-house using the procedures described in Section. 5.1. Large-signal model development is more complex, and physically based models have been developed for power amplifier designs. As described in the previous section, poor correlation has been found between the small-signal hybrid-π model and measurements in the 140-220 GHz band. First generation designs in this frequency band were shifted from their design frequencies due to model discrepancies [47], [48]. Improved designs are now being developed based on measured transistor S-parameters.

Tuned-amplifier designs have typically utilized transmission line matching networks, with lumped passive elements for stabilization and biasing. At mm-wave design frequencies, electromagnetic simulation of passive elements is essential. A planar method-of-moments electromagnetic simulator is used to model critical passive elements and transmission line discontinuities. The transferred substrate technology provides a low-dielectric (ϵ_{eff}=2.7) microstrip wiring environment with a thin substrate thickness (5 μm). Standard microstrip CAD models have been found adequate to describe straight sections of transmission line to the frequency limits of our measurement system. The design approach of utilizing electromagnetic simulation of unique passive elements with standard microstrip models has shown excellent agreement with measurements. Figure 21 shows modeled and measured S-parameters for the matching network of the single-stage amplifier described in the next section. A matching network test structure without an active device was realized on-wafer, and the model and measurements show good agreement across the 140-220 GHz band.

The 5 μm BCB microstrip dielectric used in the transferred substrate process was selected to provide a low inductance, low cross-talk wiring environment for densely packed mixed-signal IC applications. The thin dielectric also improves thermal heat-sinking, and provides low inductance access to the backside ground plane. In tuned amplifier design, these advantages are offset by the high resistive losses incurred in the transmission line matching networks. For the amplifier using the matching network of fig. 21, simulation of the circuit with lossless matching networks resulted a 2.0 dB increase in the gain. Given that resistive losses increase inversely with substrate thickness for a line of constant characteristic impedance, increasing the

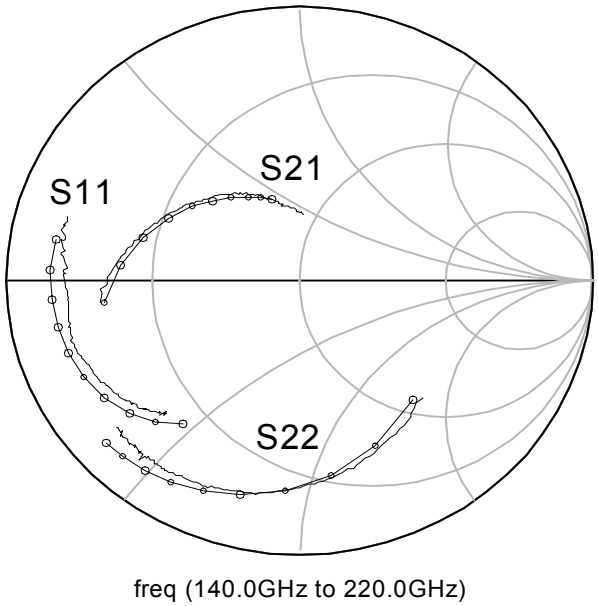


Figure 21: Measured (solid line) and modeled (circles) S-parameters of amplifier matching network in the 140–220 GHz band.

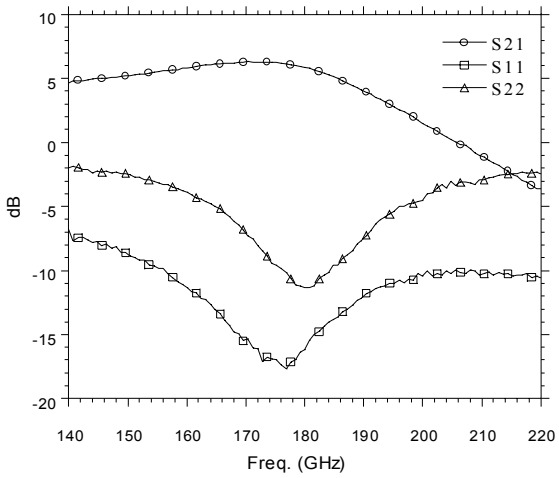
dielectric thickness may be beneficial for circuits utilizing transmission line matching networks.

6.2. *Amplifier results*

Figure 22 shows a chip photo and measured S-parameters of a single-stage G-band tuned amplifier [47], [48]. The transistor used in the design had an emitter junction area of 0.4 μm $\times$ 6 μm, and a collector stripe of 0.7 μm$\times$ 6.4 μm. The amplifier employed a simple common-emitter topology. Shunt-stub tuning at the input and output of the device was used to conjugately match the transistor at the intended design frequency. A shunt resistor at the output was used to ensure low frequency stability, and a quarter-wave line to a radial stub capacitor bypassed the resistor at the design frequency.

The amplifier exhibited a peak gain of 6.3 dB at 175 GHz, with a gain of better than 3 dB from 140 to 190 GHz. Both the input and output return loss were better than 10 dB at 175 GHz. The gain-per-stage of the amplifier is amongst the highest reported from any transistor technology in this frequency band. Multi-stage amplifier designs based on this first generation design are currently being fabricated. Simulations of three-stage amplifier designs predict a peak gain of 20 dB at 175 GHz.

W-band HBT amplifiers are being developed in the transferred-substrate technology for phased-array antenna applications. First-generation designs utilizing the



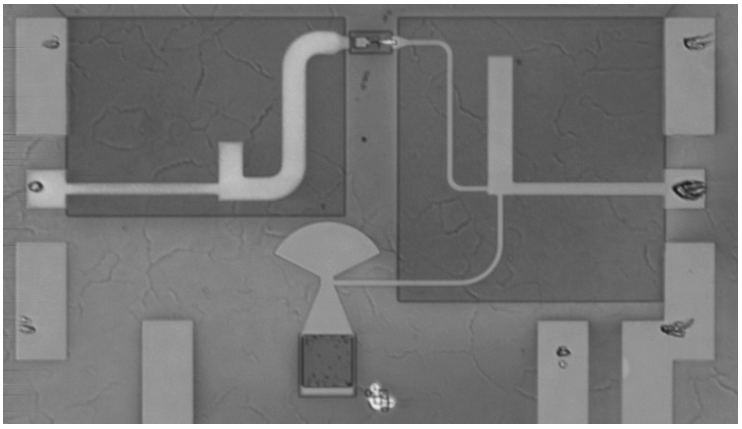


Figure 22: Single-stage tuned G-band amplifier with 6.3 dB gain at 175 GHz.

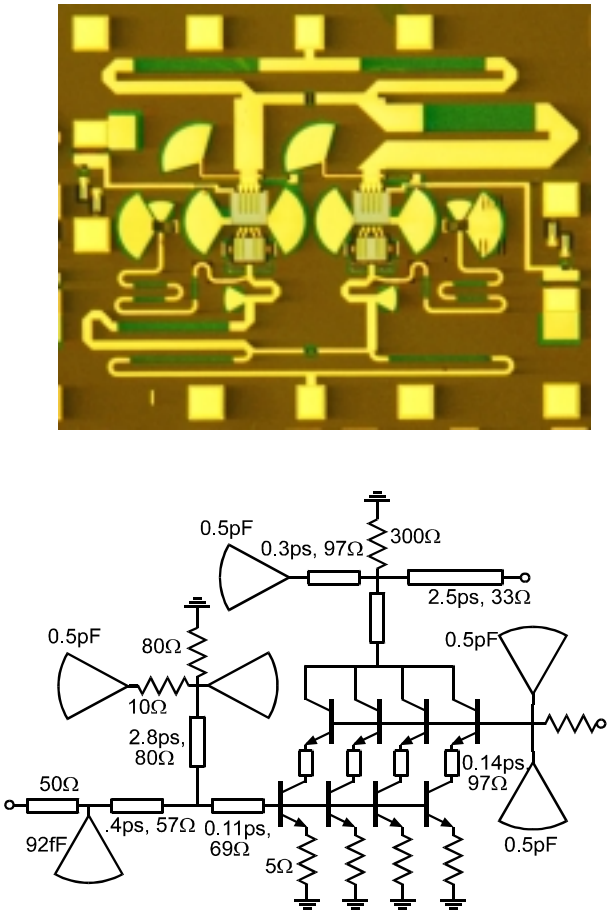


Figure 23: W-band balanced medium-power amplifier (chip photo) and schematic for cascode power amplifier. The balanced amplifier has 7 dB gain and produces 10.7 dBm saturated output power at 78 GHz. The cascode amplifier had 8.5 dB gain at 75 GHz with a 1 dB gain compression output power of 9.4 dBm

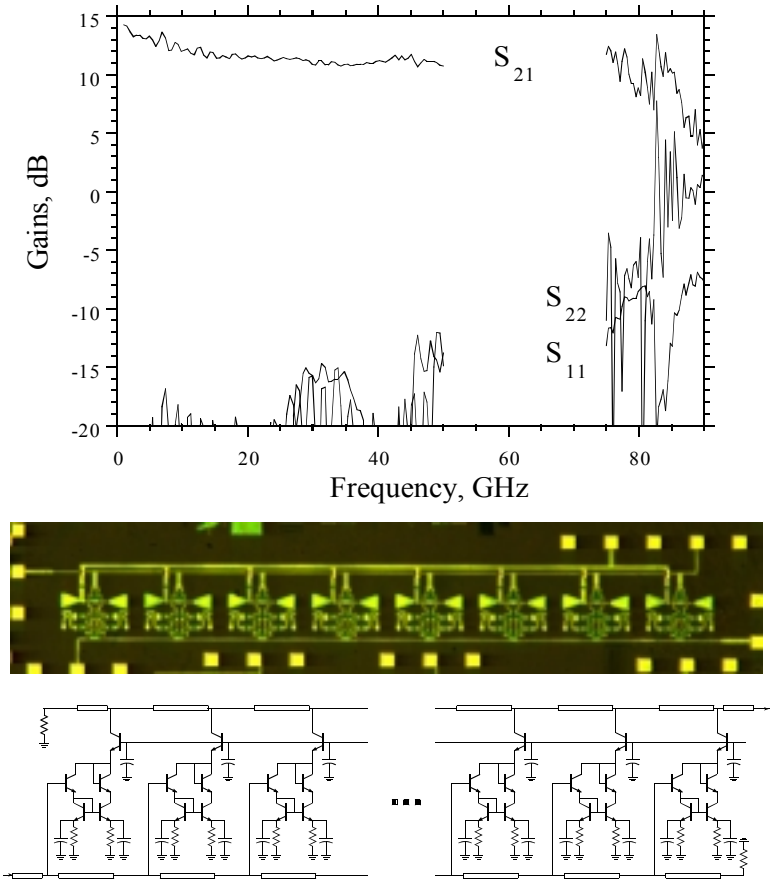


Figure 24: Distributed amplifier in the transferred-substrate process. The amplifier exhibits 11.5 dB gain and approximately 80 GHz bandwidth

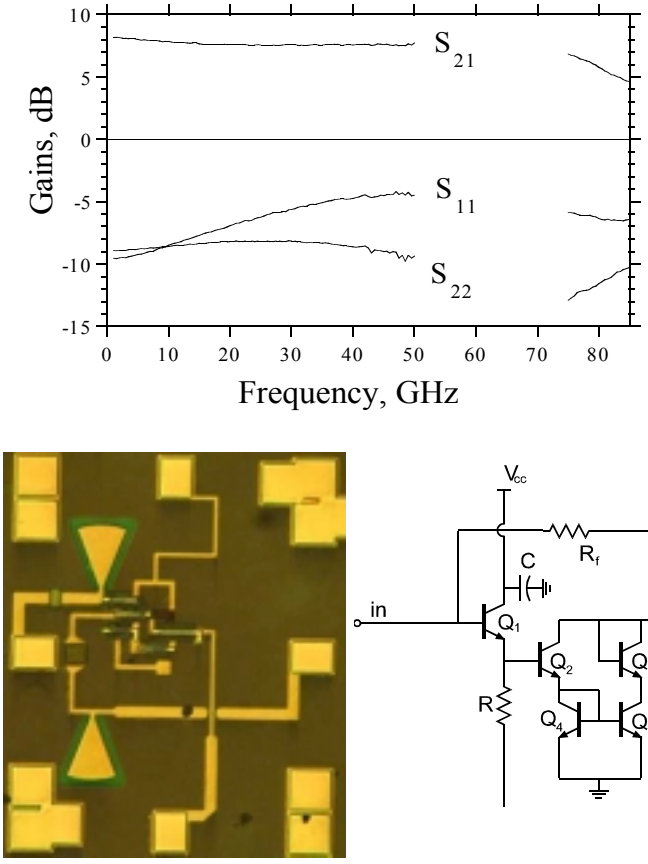


Figure 25: f_τ-doubler resistive feedback amplifier with 8.2 dB low-frequency gain and a DC-80 GHz 3-dB-bandwidth

single heterojunciton process were reported in [49] (fig. 23). A cascode amplifier exhibited 8.5 dB gain at 75 GHz with a 1 dB gain compression output power of 9.4 dBm. A balanced amplifier employing two cascode stages had a gain of 7.9 dB at 78 GHz and a 1 dB compression output power of 10.7 dBm. Second generation power amplifier designs using the higher breakdown InP double heterojunction technology have recently been fabricated [50]. A common-base power amplifier exhibited 8 dB gain and a saturated output power of greater than 16 dBm.

In addition to tuned amplifiers, broadband analog amplifiers for optical fiber receivers have also been fabricated. Results from this effort include: 80 GHz distributed amplifiers [51] (fig. 24), 50 GHz differential amplifiers [52], and Darlington and f_τ - doubler resistive feedback amplifiers (fig. 25) [53]. Greater than 400 GHz gain-bandwidth product has been obtain from a single Darlington stage [53].

7. Conclusions

Extending transistor bandwidths towards terahertz frequencies requires agressive device scaling. High bandwidths are obtained with heterojunction bipolar transistors by thinning the base and collector layers, increasing emitter current density, decreasing emitter contact resistivity, and reducing the emitter and collector junction widths. HBT amplifiers have been demonstrated in the 140-220 GHz band, and transistors show high levels of available gain at the frequency limits of state-of-the-art measurement systems. The physical characteristics of submicron HBTs make accurate measurement and modeling difficult. Next generation amplifier designs will require further scaling of minimum device feature sizes, and accurate modeling of active and passive circuit components.

Acknowledgments

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