Wide Bandwidth InP DHBT Technology Utilizing Dielectric Sidewall Spacers

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Abstract

We report device results from a wide bandwidth InP mesa-DHBT technology. In an effort to improve the manufacturability of submicron devices, the self-aligned base emitter junction is formed using dielectric sidewall spacers and a refractory base metal stack. Device performance has been optimized for high-speed digital and mixed-signal circuit applications An HBT with emitter junctions dimensions of 0.7 x 3.0 μm^2 exhibited peak f_τ and f_{max} values of 292 GHz, and 314 GHz, respectively, at J_E = 6 mA/μm^2 and V_{CB} = 0.4 V. Importantly for digital logic circuits, the device had a low collector-base capacitance (C_{cb} = 6.4 fF) resulting in a low collector-base capacitance to collector current ratio (C_{cb}/I_C ~ 0.5 psec/V).

I. Introduction

InP-based double heterojunction bipolar transistors (DHBTs) have applications in tuned millimeter-wave and high-speed mixed signal integrated circuits. Device requirements in these applications may differ drastically in terms of levels of integration and the device parameters that dominate circuit performance. In mixed signal applications, such as digital radar, transistor counts in complex ADCs and DACs may approach ~10,000 devices [1]. To compete with SiGe HBTs in this application space, InP HBTs must offer superior performance in a *manufacturable* process.

In HBT digital logic circuits, the minimum gate delay is not well correlated to one transistor figure-of-merit (f_τ or f_{max}). An analysis of the delay terms in an ECL (emitter coupled logic) gate reveals that certain RC charging constants have larger fractional contributions to the gate delay than to the HBT forward transit time (τ_{ec}=1/2πf_τ) [2]. A major contributor to the gate delay is the charging of the collector-base capacitance through the load resistor. Expressed in terms of the large signal voltage swing (ΔV_{logic}) and the HBT drive current (I_c) the delay term is given $\Delta V_{logic}C_{cb}/I_c$. Given that a minimum voltage swing is necessary to switch the logic gate, one sees the importance of minimizing the C_{cb}/I_c ratio for a digital logic device.

SiGe HBTs benefit from process flows that allow for deep submicron device scaling and careful control of extrinsic parasitic capacitances. SiGe HBTs also typically operate at much higher current densities (>10mA/μm^2) than their InP counterparts. These technology features are beneficial in the design of high-speed digital circuits, and point to directions for improving InP HBT technologies in order to take full advantage of their superior electron transport properties.

State-of-the-art InP HBTs are generally realized with submicron emitter junction dimensions. Examples of high-performance submicron HBTs include: an InP DHBT technology with f_τ and f_{max} of 350 GHz and 490 GHz, respectively [3], an InP single heterojunction HBT technology with a 452 GHz f_τ and a 155 GHz f_{max} [4], and an InP DHBT technology with f_τ and f_{max} simultaneously greater than 370 GHz [5].

High performance devices often rely on process steps that may not be amenable to the high levels of yield and integration necessary for some mixed-signal applications. For instance, undercut of semiconductor layers using wet chemical etching may be used to isolate the extrinsic base pad capacitance [3,4], or to form a shadow mask for the evaporation of a self-aligned base contact [4, 5]. One expects the degree of undercut to be difficult to control over full wafer diameters in a manufacturing environment.

In this work, we describe an InP HBT technology with process steps that have been implemented to improve the yield and manufacturability of submicron devices. A dielectric sidewall process with a refractory base metal has been used to form the self-aligned base-emitter junction, eliminating the standard self-aligned base-emitter liftoff process. Transistors with submicron emitter junction widths have been measured and exhibit simultaneous f_τ and f_{max} of close to 300 GHz. The transistors also support high current density operation ($J_E > 5$ mA/μm^2) and have a low collector-base capacitance to collector current ratio ($C_{cb}/I_c \sim 0.5$ ps/V).

II. Epitaxial Design

The transistor epitaxy is grown by molecular beam epitaxy by commercial vendor IQE. The emitter semiconductor thickness is kept thin (<1000Å) to facilitate the formation of a submicron emitter mesa using wet chemical etching. The carbon-doped InGaAs base is 400Å thick and includes ~52 meV of compositional grading to reduce the base transit time. Improvements in transistor f_τ could be realized through the use of thinner base layers. However, in addition to introducing concerns regarding device reliability, circuit simulations indicate minimal improvements in digital logic speed when reducing the base thickness at this technology node. The total collector thickness for the transistors is 1500Å, and the subcollector contains a minimum amount of InGaAs (50 Å) to minimize thermal resistance.

InGaAs/InAlAs chirped-superlattice grades are used at the emitter-base and collector-base junctions. As will be described later, the emitter-base grade serves as a passivation ledge in the HBT process flow. Proper design of the base-collector junction is critical for high current density operation. Details regarding the base-collector grade design used in this work can be found in [6].

III. Process Flow

A schematic cross-section of the HBT before dielectric planarization is shown in Figure 1. The process begins with the deposition of the emitter contact. In this work, electron-beam lithography is used to define the contact, which is deposited using electron-beam evaporation. The emitter contact is used as a mask for the wet chemical emitter mesa-etch. The thin emitter semiconductor layers are found to be effective in controlling the lateral undercut of the emitter semiconductor, with ~0.05μm undercut being observed. The emitter-mesa etch stops selectively in the base-emitter grade.

Dielectric sidewalls are deposited on the base-emitter grade, which serves a passivation ledge. The passivation of InP HBTs with PECVD deposited Si_xN_y and SiO_2 films has been reported to increase base-emitter leakage currents and degrade transistor current gain [7,8]. In literature the reported degree of the degradation has varied from severe at all currents densities [7], to less pronounced at only low current densities [8]. The

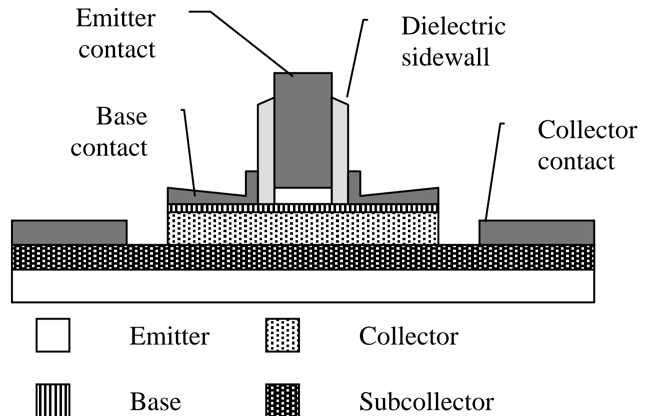


Fig. 1: *Schematic cross-section of HBT*

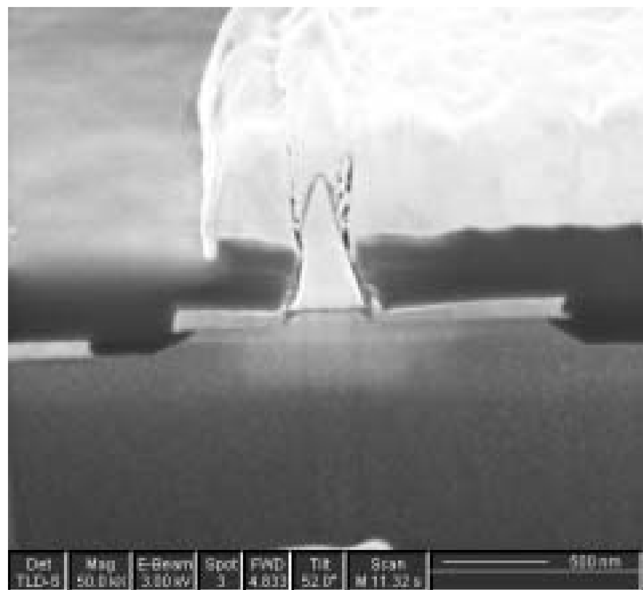


Fig. 2: *Focused ion beam cross-section of submicron HBT.*

increased leakage current has been attributed to pinning of the surface Fermi level along passivated surfaces [8]. Work in [9] suggests that the deposition of Si_xN_y tends to pull the surface Fermi level of InGaAs towards the conduction band, while the Fermi level of InAlAs was found to pin near midgap. For these reasons, the dielectric sidewalls were placed on the InAlAs-containing emitter-base grade, which is expected to be full depleted.

The sidewalls are formed by the conformal PECVD of a dielectric film, followed by an anisotropic reactive ion etch. The sidewall process allows for the base contact to be placed closely to the emitter junction (<1000 Å for this work), thereby minimizing the lateral access resistance. The deposition of the base Ohmic contact resembles the process reported in [10] for submicron GaAs HBTs. A thin reactive

metal is first electron-beam evaporated on the wafer to improve the contact resistivity. A sputtered tungsten film is then blanket deposited on the wafer. To break the resulting base-emitter short circuits, tungsten is removed from the top and sidewalls of the emitter using a planarization and etchback process. An SF_6-based RIE is used to etch the tungsten.

The base mesa is defined using a RIE etch to remove the tungsten in the field area, and a wet chemical etch to remove the base and collector semiconductor layers. To minimize the collector base capacitance, the width of the base mesa is aggressively scaled to ~ 0.5 µm on either side of the emitter contact.

`The remaining process flow is similar to that of a standard triple-mesa HBT, with particular attention paid to reducing device parasitics. Of critical importance is the minimization of the excess collector-base capacitance from the base pad that is required to contact the base metal. This capacitance may represent a large fraction of the total C_{cb} for a submicron device. In this work, a small (~1µm^2) base post is used, and the post is placed as close to the emitter contact as possible given lithographic alignment tolerances.

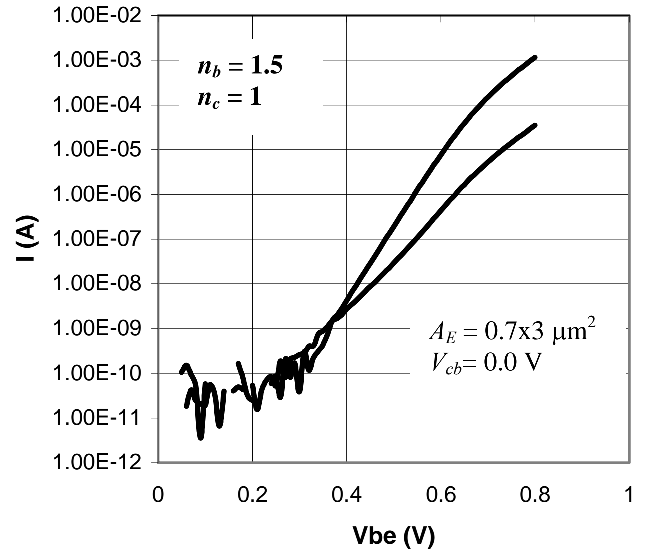
After collector contact definition and device isolation, the devices are passivated with a spin-on-polymer (BCB). An etchback process is used to expose device contact posts, and interconnect metal is then deposited. A focused ion beam (FIB) cross-section of a fabricated device is shown in Fig. 2.

IV. Device Measurements

Gummel characteristics of a submicron HBT are shown in Fig. 3. The emitter junctions dimensions for the device are A_E = 0.7x3 µm^2. Devices demonstrated a transistor current gain β of approximately 40, and a common emitter breakdown voltage BV_{CEO} greater than 4.5V. The base (n_b) and collector (n_c) ideality factors are 1.5 and 1, respectively. The low gummel crossover (~2nA) indicates the effectiveness of the base-emitter ledge.

RF device measurements were made from 1-50 GHz using an Agilent 8510 VNA. Calibration was performed using an off-wafer TRL calibration substrate, and the RF probe pads were deembedded from the device measurements. Fig. 4 shows the unilateral power gain (U) and short circuit current gain (h_{21}) of for the same device as Fig. 5. The device bias conditions are J_E=6 mA/µm^2 and V_{CB}= 0.4V. The extrapolated f_τ and f_{max} of the device are 292 GHz and 314 GHz, respectively.

Fig. 4 shows the transistor f_τ and f_{max} plotted versus current density at varying values of V_{CB}. The transistor is found to sustain high current density operation at low collector-base operating voltages, an important characteristic for transistors in ECL and CML logic circuits.



`*Fig 3: Gummel characteristics of submicron HBT*

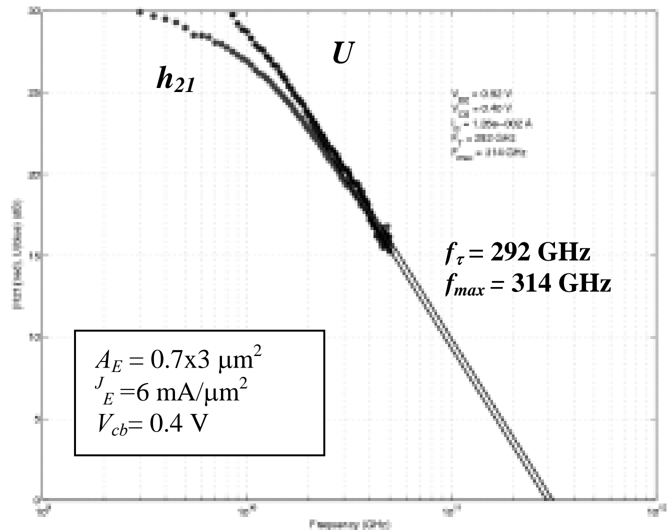
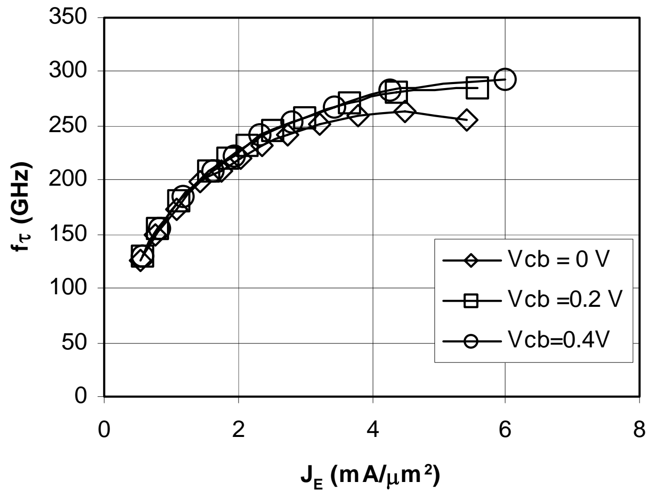
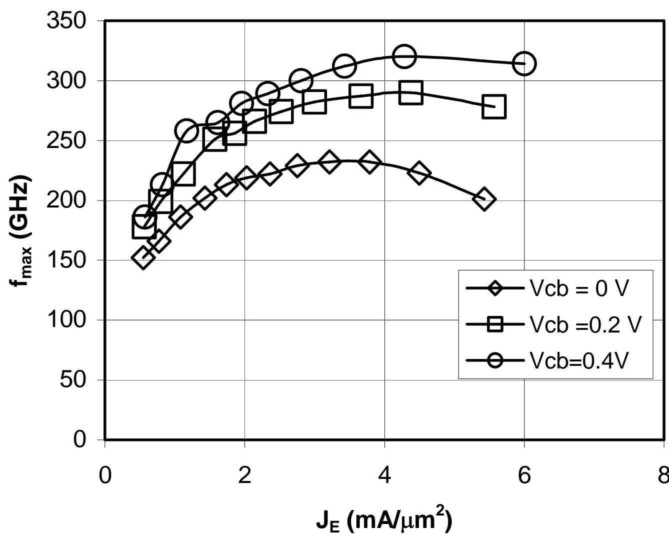


Fig 4: Measured RF gains of submicron HBT

As discussed previously, the collector-base capacitance plays a critical role in determining the digital logic speed. The collector-base capacitance of the transistor of Fig. 3 was extracted from the imaginary part of Y_{12} and is plotted versus current density in Fig. 6. With the collector fully depleted, the collector-base capacitance is 6.4 fF. At the bias conditions of Fig. 4, this results in a low C_{cb}/I_C ratio of 0.5 psec/V.



(a)



(b)

Fig 5: f_τ (a) and f_{max} (b) versus *J_E at varying V_{cb} for HBT of Fig. 3*

V. Conclusion

A wide bandwidth DHBT technology designed for mixed-signal and digital logic applications has been described. Process steps have been to improve the yield and manufacturability of deep submicron devices. Specifically, a dielectric sidewall process with a refractory base metal has been used to form the self-aligned base-emitter junction. Measured DHBTs are found to support high current density operation (J_E > 5 mA/μm^2) and have a low collector-base capacitance to collector current ratio (C_{cb}/I_c ~ 0.5). A simultaneous f_τ and f_{max} of close to 300 GHz has been obtained. Mixed-signal demonstration circuits are currently being fabricated in the technology to validate the transistor design approach.

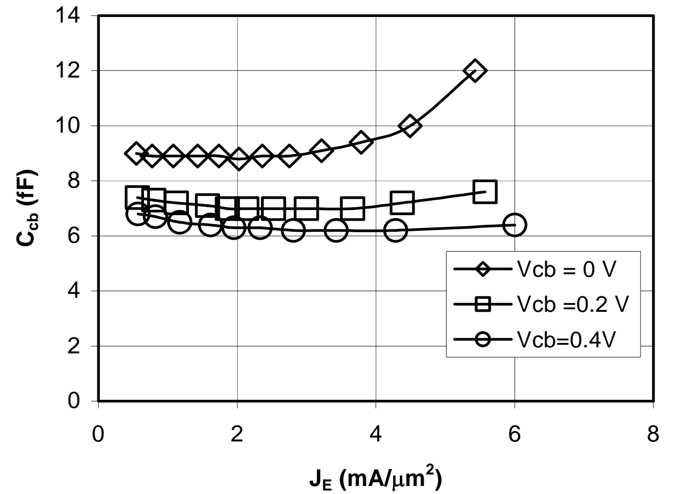


Fig 6: C_{cb} versus *J_E at varying V_{cb} for HBT of Fig. 3*

Acknowledgements

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