G-Band (140–220-GHz) InP-Based HBT Amplifiers

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***Abstract*—We report tuned amplifiers designed for the 140–220-GHz frequency band. The amplifiers were designed in a transferred-substrate InP-based heterojunction bipolar transistor technology that enables efficient scaling of the parasitic collector–base junction capacitance. A single-stage amplifier exhibited 6.3-dB small-signal gain at 175 GHz. Three-stage amplifiers were subsequently fabricated with one design demonstrating 12.0-dB gain at 170 GHz and a second design exhibiting 8.5-dB gain at 195 GHz.**

***Index Terms*—G-band electronics, InP heterojunction bipolar transistor (HBT), millimeter-wave amplifier.**

I. Introduction

Electronics in the 140–220-GHz frequency band have applications in wide-band communication systems, remote atmospheric sensing, and planetary exploration by unmanned space probes. Wide-bandwidth transistors with high available gain in this frequency range are realized through submicron scaling of lateral device dimensions. The gate lengths of InP-based high electron mobility transistors (HEMTs) have been scaled to deep-submicron dimensions, and high-gain G-band amplifiers have been reported in technologies utilizing these devices. State-of-the-art results in InP HEMT technologies include a three-stage amplifier with 30-dB gain at 140 GHz [1], a three-stage amplifier with 12–15-dB gain from 160–190 GHz [2], and a six-stage amplifier with 20 ± 6 dB from 150–215 GHz [3].

The vertical current flow in a III-V heterojunction bipolar transistor (HBT) presents challenges to device scaling that are not present in lateral transport HEMTs. Standard III-V HBT processes utilize a mesa fabrication technology that is inherently difficult to scale. In a mesa-HBT, a parasitic collector–base capacitance lies beneath the base ohmic contacts. The minimum width of these contacts is set by the ohmic contact transfer length, which is an inherent parameter of the material system that is not easily scaled. Lateral scaling of the emitter–base junction dimensions without a concurrent reduction in the base–collector junction dimensions will limit the HBT's high-frequency performance.

We have developed a transferred-substrate HBT technology that enables simultaneous scaling of the emitter–base and collector–base junction dimensions [4]. The technology has been used to demonstrate submicron single-heterojunction HBTs with record values of transistor power gain at 110 GHz [5]. Broad-band amplifiers designed in the technology have included an 80-GHz traveling-wave amplifier with 11.5-dB mid-band gain [6], and Darlington and f_τ-doubler resistive feedback amplifiers with 18-dB gain and >50-GHz bandwidth and 8.2-dB gain and 80-GHz bandwidth [7]. Recently, a double-heterojunction process utilizing an InP collector for improved breakdown voltage has been demonstrated [8]. W-band (75–110-GHz) power amplifiers in this technology have been fabricated with a common-base amplifier exhibiting 16-dBm saturated output power at 85 GHz and a cascode amplifier demonstrating >12-dBm saturated output power at 90 GHz [9].

In this paper, we describe tuned-amplifier designs for the 140–220-GHz band realized in the transferred-substrate HBT technology. A single-stage amplifier exhibited 6.3-dB small-signal gain at 175 GHz [10]. Two multistage amplifier designs were subsequently developed with one design demonstrating 12.0-dB gain at 170 GHz, and the second design demonstrating 8.5-dB gain at 195 GHz [11]. In Section II, the transferred-substrate device technology is described, and device results are presented. The amplifier designs are then discussed, and specific high frequency design issues are considered. Finally, the amplifier results are presented, and comparisons are made between measured results and circuit simulations.

II. Transferred-Substrate HBT Technology

A. Fabrication and Device Layer Structure

A brief overview of the transferred-substrate process and device layer structure is presented here. A more detailed review of the technology can be found in [4].

The HBTs used in this work incorporate an InAlAs–InGaAs emitter–base heterojunction with an InGaAs collector. The epitaxial material is grown by molecular beam epitaxy on a semi-insulating InP substrate. The 400-Å base layer is p+ beryllium-doped at 5×10^{19} cm^{-3} and includes approximately 50 meV of compositional grading to reduce base transit time. A 3000-Å collector thickness was used in this work.

Prior to substrate transfer, the HBT fabrication process is similar to that of a traditional mesa-HBT process. Technology features include self-aligned base contacts, polyimide device passivation, two levels of metal interconnects, MIM capacitors, and NiCr resistors.

After the definition of the final interconnect layer, a spin-on-polymer, benzocyclobutene (BCB) ($\varepsilon_r = 2.7$), is spun onto the wafer and serves as the microstrip transmission line dielectric. Vias are dry-etched in the BCB, and the BCB is simultaneously etched back to a final thickness of 5 μm. A gold ground

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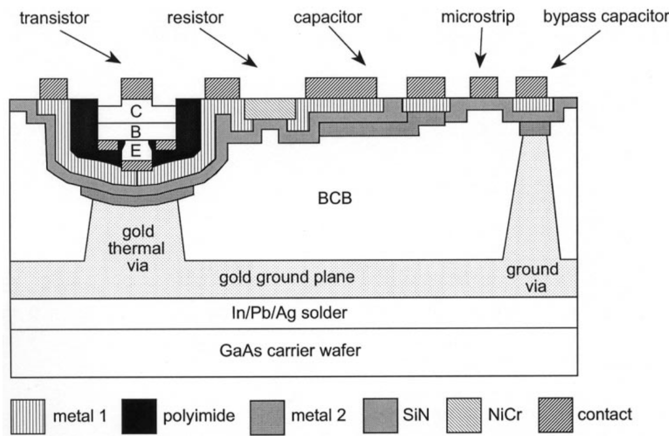

Fig. 1. Schematic cross section of transferred-substrate HBT technology.

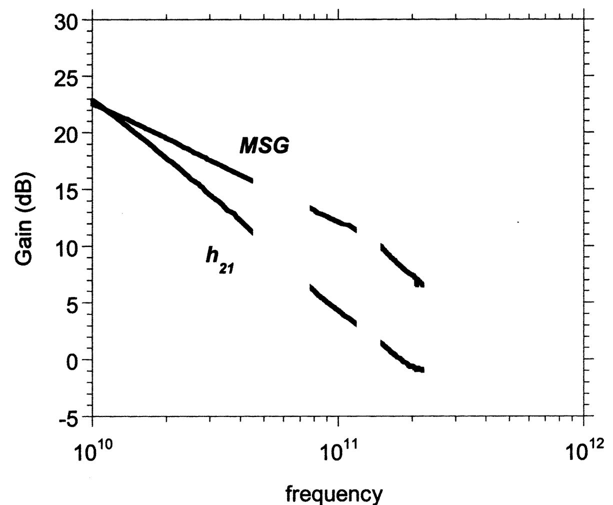

Fig. 2. HBT short-circuit current gain (h_{21}) and maximum stable power gain, measured in the 10–40, 75–110, and 140–220 GHz bands. Device dimensions: emitter junction 0.4 μm × 0.6 μm, collector junction 0.7 μm × 6.4 μm. Device bias conditions $V_{\mathrm{CE}} = 1.25$ V, $I_{\mathrm{C}} = 3.2$ mA.

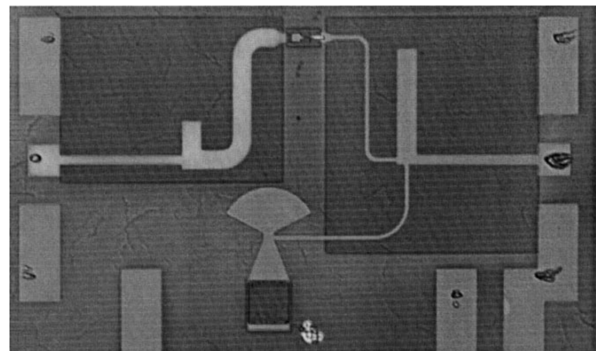

Fig. 3. Chip photograph of single-stage amplifier. Cell dimensions are 0.69 mm × 0.35 mm.

plane is electroplated on the BCB surface. The InP wafer is then mechanically bonded to a GaAs or AlN carrier wafer with the ground plane at the carrier wafer surface. A selective HCl etch removes the InP substrate, revealing the collector epitaxy. Schottky collector contacts can then be defined directly over the devices. In this work, electron-beam lithography was used to define emitter and collector stripes. A cross section of the transferred-substrate technology is shown in Fig. 1.

In practice, the transferred-substrate technology has been limited by the inability to scale the technology for production levels outside of a university clean-room setting. Current research efforts in InP HBTs are focusing on the development of low parasitic processes that are compatible with larger volume manufacturing. Recent work in scaled mesa-HBTs has produced an InP double-heterjunction transistor with extrapolated f_τ and $f_{\max}$ of 280 and >400 GHz, respectively [12]. The device had a measured maximum stable gain of ~5 dB at 175 GHz. In addition to its excellent RF performance, the device had a common-emitter breakdown voltage of 6 V, making it a promising candidate for millimeter-wave power applications.

B. Device Results

The transistors used in the amplifier designs had emitter junction areas of 0.4 μm × 6 μm and collector junction dimensions of 0.7 μm × 6.4 μm. Devices of that geometry have typical dc small-signal current gains, β, of 20, and common-emitter breakdown voltages, $\mathrm{BV}_{\mathrm{CEO}}$, of 1.5 V at a current density of 10^5 A/cm^2.

On-wafer RF measurements of transferred-substrate HBTs have been made to frequencies as high as 220 GHz. Making accurate RF measurements of submicron HBTs is particularly difficult because measurements of the small reverse transmission characteristics of the transistors (S_{12}) may be corrupted by coupling between on-wafer probes. This coupling is not accounted for in standard 12-term network analyzer error corrections. To minimize the coupling, devices can be embedded in lengths of on-wafer transmission line to increase the probe separation. In this work, a probe-to-probe separation of ~500 μm was employed.

Measurements are calibrated using a through-reflect-line (TRL) calibration with the calibration reference planes placed at the device terminals. A TRL calibration is referenced to the characteristic impedance of the line standard, and an accurate calibration requires a well-characterized single-mode transmission line environment. The transferred-substrate process provides a thin low-loss microstrip wiring environment, making it well suited for on-wafer device measurements. However, due to the thin substrate thickness, narrow conductor widths are required to realize a 50-Ω characteristic impedance, and resistive losses in the transmission lines are high. Electromagnetic simulations of the microstrip lines have been performed and corrections have been applied to measurements to account for the complex characteristic impedance of the line standard due to resistive losses.

Fig. 2 shows the maximum stable gain (MSG) and the short-circuit current gain h_{21} for a transistor measured from 10–45 GHz, 75–110 GHz, and 140–220 GHz. The device was biased at $I_{\mathrm{C}} = 3.2$ mA and $V_{\mathrm{CE}} = 1.25$ V. The bias conditions are identical to those used in the measured multistage amplifier designs.

We note that the Rollet stability factor k is less than unity to 220 GHz and that the power gain in the 140–220-GHz band still

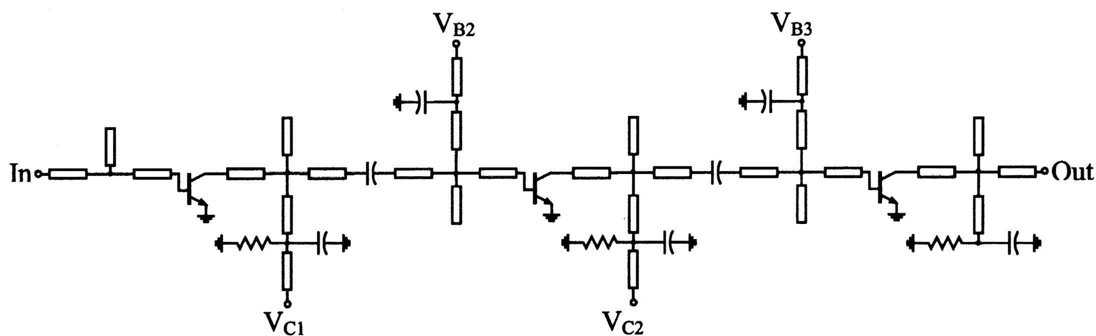

Fig. 4. Circuit schematic of multistage amplifier design.

represents the MSG of the device, and not the maximum available gain. The current gain cutoff frequency f_τ of the device was measured to be 180 GHz.

Mason's unilateral power gain U is generally used to extrapolate the maximum power gain cutoff frequency $f_{\max}$ of a transistor. For an HBT well modeled by a hybrid-pi transistor model, U will exhibit a 20-dB/decade rolloff independent of transistor configuration and the reactances associated with the on-wafer embedding network. We have observed that highly scaled InGaAs-collector HBTs may exhibit positive conductance in the common-emitter reverse conductance G_{12} and negative conductance in the output conductance G_{22}, which are trends that cannot be modeled by a standard hybrid-pi transistor model. Such transistors exhibit a peaking in the unilateral power gain, and under certain bias conditions, U may exhibit a singularity where it increases to infinity and then becomes negative. It is believed that these effects are the result of second-order transport phenomenon in the collector space charge region. These effects may not be observed in a standard III-V mesa-HBTs because the reverse transmission characteristics are dominated by the large extrinsic collector–base capacitance. A more detailed discussion of these results will be presented elsewhere [13].

A consequence of the observation of a singularity in the unilateral power gain is that we cannot extrapolate $f_{\max}$ from transistor power gain measurements. However, a MSG of >7 dB has been measured at 200 GHz, and the presented amplifier results verify the high available gain from the transistors at the frequency limits of currently available vector network analysis (VNA) systems.

III. Amplifier Designs

Both single-stage and multistage 140–220-GHz amplifiers have been realized in the transferred-substrate HBT technology. A chip photograph of a fabricated single-stage amplifier is shown in Fig. 3. The amplifier employed a common-emitter topology. Shunt-stub tuning at the input and output of the device was used to conjugately match the transistor at the intended design frequency of 200 GHz. A shunt resistor at the output was used to ensure low-frequency stability, and a quarter-wave line to a MIM capacitor bypasses the resistor at the design frequency. Bias T's built into the on-wafer probes provide dc bias to the input and output of the amplifier.

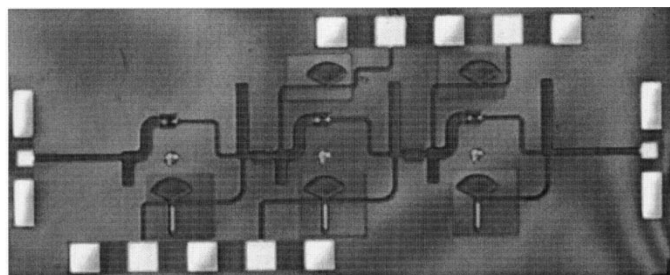

Fig. 5. Chip photograph of fabricated multistage amplifier. Cell dimensions are 1.66 mm $\times$ 0.59 mm.

A circuit schematic for the multistage amplifier design is shown in Fig. 4. The design consists of three cascaded common-emitter stages. The design was based on the first-generation single-stage amplifier design, and each stage was matched to a 50-Ω characteristic impedance. Interstage MIM capacitors with nominal values of 75 fF provide dc isolation between stages. To simplify the design, separate supply lines were used to provide dc bias to the base and collector of each device. A shunt resistor at the collector of each device was again used to ensure low-frequency stability, and a high-impedance quarter-wave line to a MIM capacitor bypasses the resistor at the intended design frequency. At the amplifier design frequencies, resistive losses in the transmission line matching networks are sufficient to stabilize the transistors. Two multistage amplifiers were designed with intended design frequencies of 175 and 200 GHz. A chip photograph of a fabricated multistage amplifier is shown in Fig. 5.

First-generation single-stage amplifiers were designed using a hybrid-pi transistor model developed from earlier generation submicron devices [5]. The model was developed from on-wafer S-parameter measurements from 1 to 50 and 75 to 110 GHz and extrapolated to the design frequency. Subsequent measurements of transistors in the 140–220-GHz band showed poor correlation with the transistor model. We were unable to determine the source of this discrepancy, and for second-generation multistage designs, measured transistor S-parameters were used for circuit simulations.

The circuits were designed using Agilent Technologies Advanced Design System software [14]. A planar method-of-moments EM simulator (Momentum) was used to model the unique MIM capacitor structures and any microstrip discontinuities (i.e., junctions and bends) in the circuit.

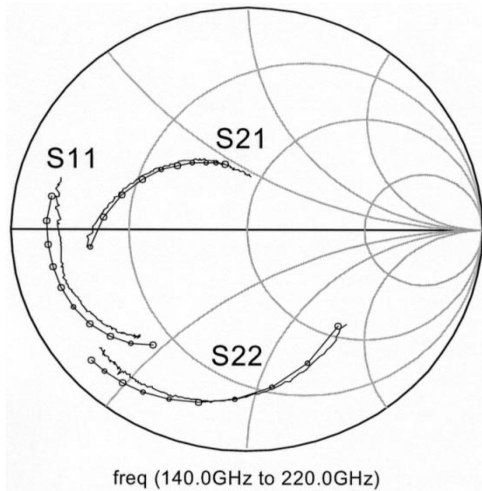

Fig. 6. Measured (solid) and modeled (circle) S-parameters of matching network test structure.

Standard microstrip CAD models were used to model the remaining transmission lines in the circuit. Test structures of the single-stage amplifier input and output matching networks cascaded together without an active device were included on wafer to verify the accuracy of the passive element models. The measured and modeled S-parameters of this test structure are shown in Fig. 6.

The good agreement between the measured and modeled results verifies the passive element design. The accuracy of the microstrip models at such high frequencies is attributed in part to the thin BCB dielectric substrate provided in the transferred substrate process. The thickness of the substrate (5 μm) was selected to provide a low inductance wiring environment for densely packed mixed-signal IC applications. Additionally, the thin dielectric improves thermal heat sinking and provides low inductance access to the backside ground plane. For high frequency tuned circuit applications, it was found that these advantages are offset by the high resistive losses incurred in the transmission line matching networks. A thicker substrate would require wider lines for a given impedance, reducing resistive losses. Simulation of the single-stage amplifier design with lossless transmission line matching networks resulted in a 2.0-dB increase in the gain.

IV. Amplifier Results

The amplifiers were measured on wafer from 140–220 GHz. The measurements were made using an HP 8510C VNA with Oleson Microwave Labs Millimeter Wave VNA Extensions. The test-set extensions are connected to GGB Industries coplanar wafer probes via short lengths of WR-5 waveguide. The amplifier measurements were calibrated on wafer using TRL calibration standards.

Fig. 7 shows the measured gain and input and output return loss of a single-stage amplifier design. The bias conditions for the transistor were $V_{\mathrm{CE}} = 1.2$ V and $I_{\mathrm{C}} = 4.8$ mA. The amplifier was found to have a peak gain of 6.3 dB at 175 GHz, with a gain of better than 3 dB from 140 to 190 GHz. Both the input and output return loss were better than 10 dB at 175 GHz.

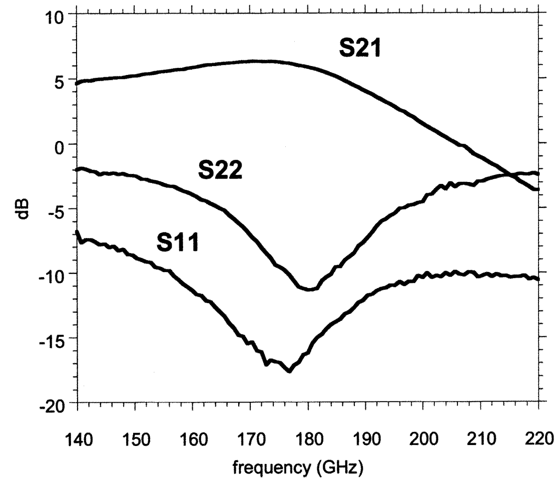

Fig. 7. Measured S-parameters of single-stage amplifier.

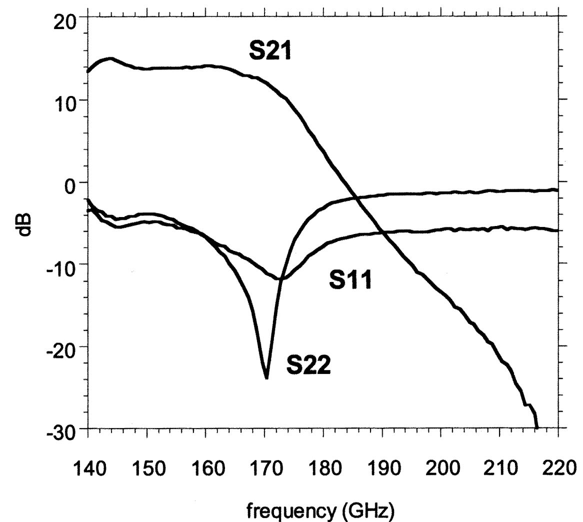

Fig. 8. Measured S-parameters of 175-GHz multistage amplifier.

Multistage amplifiers were fabricated in subsequent process runs. Fig. 8 shows the measured gain and input and output return loss of the 175-GHz amplifier design. Fig. 9 shows the same parameters measured for the 200-GHz amplifier design. For both amplifier designs, the transistors in the circuit were biased at $I_{\mathrm{C}} = 3.2$ mA and $V_{\mathrm{CE}} = 1.25$ V.

The 175-GHz amplifier design had a gain of 12.0 dB at the output match frequency of 170 GHz. A peak gain of 15.0 dB was measured at 144 GHz, and the gain was greater than 10 dB to 175 GHz. The 200-GHz amplifier design exhibited a gain of 8.5 dB at the output match frequency of 195 GHz. A peak gain of 11.7 dB was measured at 154 GHz and the gain was greater than 7.0 dB to 200 GHz.

Both multistage amplifier designs exhibited a downward shift of $\sim$5 GHz from their intended design frequency. The peak gains of the designs were also less than those predicted from simulations. The amplifier designs were based on measured device S-parameters from the first-generation single-stage amplifier process run. Transistor measurements from the multistage amplifier process run showed higher extrinsic emitter resistance and lower available power gain than the transistors

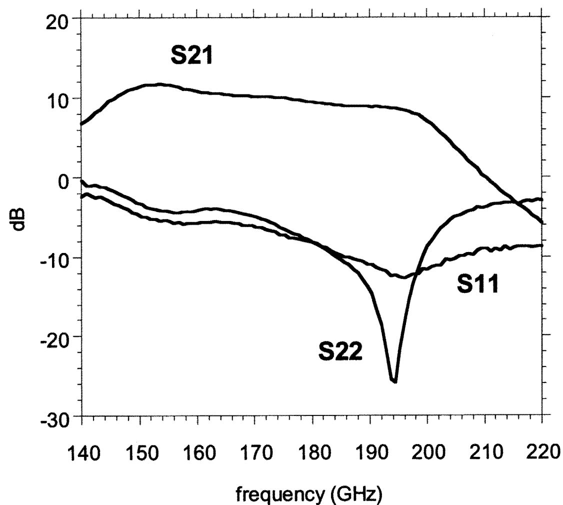

Fig. 9. Measured S-parameters of 200-GHz multistage amplifier.

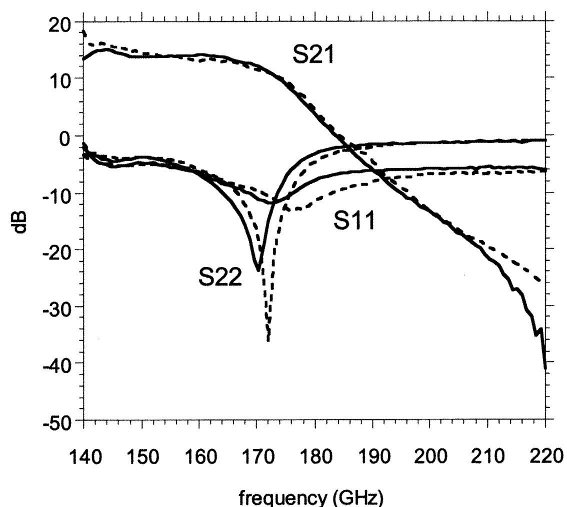

Fig. 10. S-parameters of measured 175-GHz amplifier (solid lines) and circuit simulation of amplifier using measured transistor S-parameters (dashes).

used in the design cycle. Single-stage amplifier designs on this wafer demonstrated a peak gain of 3.5 dB at 175 GHz.

Fig. 10 shows a circuit simulation of the 175-GHz multistage amplifier using measured transistor S-parameters from the multistage amplifier process run. The close agreement with measured amplifier results indicates that device variation is responsible for the downward shift from the design frequency and verifies the amplifier matching network design.

V. Conclusion

We have presented high-gain G-band amplifier designs in a transferred-substrate HBT technology. A single-stage amplifier was realized with 6.3-dB peak gain at 175 GHz. Two multistage designs were subsequently fabricated with gains of 12.0 and 8.5 dB at 170 and 195 GHz, respectively. The circuits demonstrate the potential for highly scaled low-parasitic HBT technologies to compete with HEMTs in ultra-high-frequency millimeter-wave circuit applications.

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