University of California
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mmWave Massive MIMO for Multiuser Communication: From System Design to Hardware Demonstration

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of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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Curriculum Vitæ

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4. **A. A. Farid**, et al., "135GHz CMOS / LTCC MIMO Receiver Array Tile Modules " 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021
5. M. Rodwell, **A. A. Farid**, et al.,"100-300GHz Wireless: ICs, Arrays, and Systems," 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021

6. **A. A. Farid**, et al., "Dynamic Range Requirements of Digital vs. RF and Tiled Beamforming in mm-Wave Massive MIMO" 2021 IEEE Radio and Wireless Symposium (RWS), 2021, pp. 46-48
7. et al **A. A. Farid**., "End-to-end 140 GHz Wireless Link Demonstration with Fully-Digital Beamformed System," 2021 IEEE International Conference on Communications Workshops (ICC Workshops), 2021, pp. 1-6
8. M. Abdelghany, **A. A. Farid**, et al.,"A design framework for all-digital mmWave massive MIMO with per-antenna nonlinearities," 2021 IEEE Transactions on Wireless Communications.
9. A. S. H. Ahmed, M. Seo, **A. A. Farid**, et al., "A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology," 2020 15th European Microwave Integrated Circuits Conference (EuMIC), 2021, pp. 1-4
10. A. S. H. Ahmed, M. Seo, **A. A. Farid**, et al. "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 492-495.
11. A. Simsek, A. S. H. Ahmed, **A. A. Farid**, et al., "A 140GHz Two-Channel CMOS Transmitter Using Low-Cost Packaging Technologies," 2020 IEEE Wireless Communications and Networking Conference Workshops (WCNCW), Seoul, Korea (South), 2020, pp. 1-3,
12. **A. A. Farid**, et al., "A Broadband Direct Conversion Transmitter/Receiver at D-band Using CMOS 22nm FDSOI," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019
13. M. Abdelghany, **A. A. Farid**, et al., "Towards All-digital mmWave Massive MIMO: Designing around Nonlinearities," 2018 52nd Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, USA, 2018
14. A. S. H. Ahmed, A. Simsek, **A. A. Farid**, et al., "A W-Band transmitter channel with 16dBm output power and a receiver channel with 58.6mW DC power consumption using heterogeneously integrated InP HBT and Si CMOS technologies," 2019 (IMS), Boston, MA, USA, 2019.
15. A. S. H. Ahmed, **A. A. Farid**, M. Urteaga and M. J. W. Rodwell, "204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), Madrid, 2018, pp. 29-32.

Patents

1. **Ali Farid**, et al., "Successive Approximation Register (SAR) Analog to Digital Converter (ADC) with Switchable Reference Voltage," *US Patent. 10461767*

2. **Ali Farid**, et al., "Successive approximation register (SAR) analog to digital converter (ADC) dynamic range extension," *US Patent. 10491232*
3. **Ali Farid**, et al., "Data Converters Systematic Error Calibration using on chip precise reference," *US Patent. 10630305*.
4. M.Aboudina, **Ali Farid**, et al., "Efficient successive approximation register analog to digital converter," *US Patent. 10735017* .

Abstract

mmWave Massive MIMO for Multiuser Communication: From System Design to Hardware Demonstration

by

Ali Ahmed Farid

Future trends in wireless communication systems show rapid growth in mobile data traffic. The number of subscribed users per mobile base station grows linearly with time. Emerging immersive media formats and applications (i.e., HD/UHD, 360 videos, AR/VR) requires a higher data rate and larger channel bandwidth. Millimeter-Wave massive multiuser multiple-input multiple-output (MU-MIMO) is a potential candidate for high-capacity, high data rate wireless base stations. The available mm-wave spectrum between 100GHz to 300GHz is large. The small carrier wavelength (λ) permits compact arrays with many antennas; hence spatial multiplexing can be utilized to increase the system capacity.

This thesis explores system architectures, transceiver circuit design, and high-performance packaging technologies suitable for mm-wave and sub-THz multiuser massive MIMO arrays. First, we present a comprehensive study between potential mm-wave MU-MIMO architectures (all-digital, hybrid, and fully-RF) in terms of system dynamic range requirement. We draw guidelines on the required system front-end 1-dB compression point and the required analog-to-digital converter resolution for each architecture. We also illustrate the impact of system power control and antenna load factor on relaxing the dynamic range requirements.

Next, we present the core elements for our massive MIMO arrays. We designed and tested a single-channel direct conversion transmitter (Tx) and a single-channel direct conversion receiver (RX) using Global-Foundries 22FD-SOI technology, with a record measured 3-dB modulation bandwidth of 20GHz. The Rx has 27dB conversion gain and -30dBm P-1dB. The Tx has a saturated output power (Psat) of 3dBm. Then, we used those transmitter and receiver chips and demonstrated two different packaging technologies in building our mm-wave MU-MIMO arrays. We designed, fabricated, and tested tiles of 8-elements transmitters/receivers, integrated with an on-package series fed patch antennas, assembled on high-performance laminate material and on Kyocera low permittivity ceramic interposer. We illustrate the pros and cons of each packaging technology and show the superiority of the ceramic interposers for mm-wave applications and highly dense arrays.

Finally, we integrated our MU-MIMO transmitter/receiver tiles with Xilinx ZCU111 FPGA and demonstrated the world's first mm-wave MU-MIMO arrays at 135GHz. Our transmitter MU-MIMO array has a record transmitter effective isotropic radiated power of 39dBm, a field of view of +/-15 degree. It can support a wide range of modulation schemes (i.e., QPSK, 16QAM). The integrated transmitter and receiver MU-MIMO arrays can be used for a broad range of applications, including single beam and multibeam phased arrays, wireless backhaul, imaging, and radar applications.

Contents

Curriculum Vitae **vi**

Abstract **ix**

List of Figures **xiv**

List of Tables **xxi**

1 Introduction **1**
1.1 Millimeter Wave Wireless Communication 1
1.2 Dissertation Contributions and Organization 4
1.3 Permissions and Attributions 7

2 Millimeter-Wave Multiuser Massive MIMO Architecture Choice: Digital, Hybrid or RF? **8**
2.1 Introduction 8
2.2 Beamforming Architectures 10
2.3 System Model and Users Distribution 11
2.3.1 System Model 11
2.3.2 Frontend nonlinearity and ADC Model 14
2.3.3 Digital Backend Engine 15
2.4 System Analysis and Results 15
2.4.1 ADC Specification 15
2.4.2 P1dB Specification 20
2.5 Why not Fully RF massive MU-MIMO? 23
2.6 Conclusions 24

3 Broadband transceiver design at D-band using GF 22nm FDSOI CMOS technology **25**
3.1 Introduction 25
3.2 Technology Characterization 26
3.2.1 Transistor Footprint 26

3.2.2 Transistor Characteristics 27
3.3 Receiver Architecture and Building Blocks 28
3.3.1 D-band LNA/PA 29
3.3.2 Down Conversion Mixer and TIA 31
3.3.3 Frequency Multiplier and 135 GHz LO Generation 35
3.4 Transmitter Architecture and Building Blocks 37
3.4.1 IQ Modulator 38
3.5 Transmitter and Receiver Measurement Results 39
3.5.1 Receiver Measurements 39
3.5.2 Transmitter Measurements 41
3.6 Conclusion 43

4 Packaging Technologies for mm-wave Massive MIMO Arrays 45
4.1 Introduction 45
4.1.1 Challenges for mm-Wave Packaging 48
4.2 IC-Package Interconnect Technologies 49
4.2.1 D-band Transmitter and Receiver Chips with GF Copper Pillars . 52
4.3 Packaging Material and Technology 56
4.4 A Fully Packaged D-Band MIMO Array on a High-Performance Laminate Material 57
4.4.1 PCB Stack Build-up 58
4.4.2 8-Elements Series-Fed Patch Antenna 59
4.4.3 MIMO 1-D Tile Frontend Development 61
4.4.4 MIMO 1-D Tile Backend Development 62
4.4.5 Integrated 1-D MIMO Tile on Astra MT77 High-performance Laminate 64
4.4.6 Assembly challenges with the MIMO tile on High-Performance PCB 65
4.5 Conclusion 66

5 Fully Packaged D-Band Tx/Rx Multiuser MIMO Tiles using LTCC Carriers 68
5.1 Introduction 68
5.2 Low Power Single Channel D-band Transmitter on LTCC Carrier 69
5.2.1 Ceramic Carrier Design 70
5.2.2 IC-Package Transition Loss 70
5.2.3 Series-Fed Patch Antenna 72
5.2.4 Integrated Single Channel CMOS Transmitter Testing 74
5.3 High-Power Single Channel D-band Transmitter on LTCC Carrier 77
5.3.1 InP PA housing in the ceramic carrier 78
5.3.2 CMOS/ InP PA transition design 79
5.3.3 InP PA to Series Fed Patch Antenna design 80
5.3.4 Integrated High-Power transmitter testing 80

5.4 High-Power 8-channels 135GHz MIMO Hub Transmitter Tile Module . . 87
5.4.1 MIMO Hub Transmitter Core 87
5.4.2 MIMO Hub Transmitter Backend 88
5.4.3 MIMO Hub Transmitter Module Integration 89
5.5 Low-Power 8-channels 135GHz MIMO Hub Transmitter Tile Module . . 91
5.6 Eight-channels 135GHz MIMO Hub Receiver Tile Module 92
5.7 conclusion 94

6 MIMO Demonstration 96
6.1 Introduction 96
6.2 Transmitter Array/Tile Demonstration 97
6.2.1 Array Radiation Pattern and EIRP 99
6.2.2 Transmitter Array Wireless Link 100
6.2.3 Multi-Beam Experiment 102
6.2.4 Transmitter Array Summary 103
6.3 Receiver Array/Tile Demonstration 104
6.3.1 Receiver Array Radiation pattern 105
6.3.2 Receiver Array Wireless Link 107
6.3.3 Receiver Array Summary 108

7 Conclusions and Future Work 110

Bibliography 112

end

List of Figures

1.1 Spatially multiplexed networks for multi-Gigabit mobile and residential/office communication [1]. 2
1.2 Approximate sketch of atmospheric attenuation vs. frequency for different cities [2]. 3
1.3 Array tile design for linear arrays providing beam steering in azimuth but not elevation [1]. 4

2.1 Multiuser massive MIMO beamforming architectures: (a) RF-beamforming (b) Array of subarrays (c) All-digital beamforming [11]. 9
2.2 (a) RF beamforming architectures (b) and corresponding radiation patterns, at the DFT outputs for a 32-point DFT (the fully RF architecture), for 2 parallel subarrays having 16-point DFTs, for 4 parallel subarrays having 8-point DFTs, and for 8 parallel subarrays having 4-point DFTs. [11]. 11
2.3 mmWave multiuser massive MIMO system model with a fixed frontend matrix, this matrix deploys N-point DFT for fully-RF, or N/M M-point DFT for hybrid or identity matrix for all-digital solution. [11]. 12
2.4 (a) Users distribution around base station (b) Normalized correlation between two users with spatial frequency difference of $\triangle\Omega$. Note that the closest users, depicted by red arrow, are separated by larger or equal to half the 3 dB beamwidth.) 13
2.5 (a)LNA, Mixer frontend non-linearity model capture both soft and hard compression (b) Histogram of I and Q baseband components along with ADC quantization bins. [16] 14
2.6 SNR at the array for each user(a)without power control (b) with 5-dB power control 16
2.7 BER that 95% of users achieve vs SNR at 100m (SNR_{min}) for $\beta = 1/2$ (a) using 3-bits ADC (b) using 4-bits ADC. (W/O power control) 17
2.8 ADC performance summary for different architecture and different load factors (W/O power control) 17

2.9 BER that 95% of users achieve vs SNR at 100m (SNR_{min}) for $\beta = 1/2$ (a) using 3-bits ADC (b) using 4-bits ADC. (With 5-dB power control) . 18
2.10 ADC performance summary for different architecture and different load factors (With 5-dB power control) 19
2.11 P1dB specification for different architectures and different load factors (W/O power control). 21
2.12 P1dB specification for different architectures and different load factors (With 5-dB power control). 22
2.13 (a) 8x8 Butler Matrix (b) 4x4 Analog Beamforming Matrix 23

3.1 SLVT Transistor footprint: (a) layout with gate relaxation. (b) parasitic extraction model. 26
3.2 Transistor characteristics (a) Transistor f_{max} and MAG referenced to bottom Metal layer (M1) and to the top Metal layer (AL) (b) Transistors noise figure (NF) and NF_{min} 27
3.3 D-band single-channel direct conversion receiver (a) circuit block diagram and (b) chip micrograph. The die area is 1.9mm x 0.76mm including pads. 28
3.4 (a) Circuit diagram of a 4-stage broadband LNA/PA using staggered tuning (b) EM modeling of the cross coupled pair 29
3.5 Single differential pair gain stage (a) test bench to select the neutralization capacitance value, (b)simulated K-factor & MAG Vs neutralization cap value 30
3.6 Single differential pair gain stage (a) test bench to select the neutralization capacitance value, (b)simulated K-factor & MAG Vs neutralization cap value 30
3.7 LNA/PA simulated (a) S-parameters and Noise Figure, (b)large signal gain and P_{sat} 31
3.8 Circuit diagram of the (I/Q) down conversion mixer, followed by TIA . 32
3.9 circuit diagram of pseudo-differential TIA 33
3.10 Integrated Mixer and TIA (a) schematic (b) conversion gain Vs LO power 34
3.11 TIA test structure (a) schematic for the single ended test structure (b) chip micrograph of the TIA (c)simulation vs. measurement for single ended TIA test structure 34
3.12 135GHz 9:1 LO frequency multiplier (a) Circuit schematic, (b) chip micrograph of multiplier test structure (c) measured saturated output power 35
3.13 (a) Test bench used to test multiplier output spectrum (b) multiplier output spectrum at 143GHz with 5GHz span 36
3.14 D-band single channel direct conversion transmitter (a) circuit block diagram (b) chip micrograph, including pads. The die area is 1.9mm x 0.76mm 37
3.15 IQ modulator using Gilbert cells. The (I, Q) LO ports are transformer-coupled. 38

3.16 Receiver on wafer testing setup (a) Conversion gain and linearity measurement setup, (b) IQ, RF, and LO signal feed with GGB probes 39
3.17 a) Receiver conversion gain vs. baseband frequency with a fixed LO frequency (b) Receiver conversion gain vs. LO frequency with fixed baseband frequency. 40
3.18 Receiver normalized output power vs. input power. 40
3.19 Transmitter measurement setup. 41
3.20 Transmitter characteristics. (a) Saturated output power as a function of carrier frequency, with a -3 dBm baseband input signal, this showing an 8 GHz RF tuning range. (b) Modulation sideband power as a function of modulation frequency, this showing a 8GHz (SSB) modulation bandwidth. 42
3.21 Transmitter output power as a function of input power, showing a typical 18dB gain. 42
3.22 Transmitter output spectrum with center frequency 141GHz and 100MHz input signal. 43

4.1 mm-wave/THz applications: (a) spatially multiplexed networks for multi-Gigabit mobile and residential/office communication and (b) THz radar and imaging systems supporting autonomous cars and driving in foul weather, with wideband links between cars and highway infrastructure to coordinate traffic. [1] 46
4.2 Spatially multiplexed network hub. (a) The hub has 4 faces, each a 256-element MIMO array,(b) the 256 elements are implemented by cascading 8 tiles of 8-elements . [1] 47
4.3 Comparison between IC-Package transition technologies for mm-wave applications 51
4.4 Illustrative drawing showing the procedures going the first design cycle to the second design cycle (a) chip with pads for on wafer testing (b) cartoon drawing for transmitter chips with GF copper pillars (c) PCB/ceramic carrier with solder mask opening at copper pillar locations (d) copper pillar structure 52
4.5 EM simulation using Ansys HFSS for a 135GHz transformer (a) while being open up to the air, (2) with a copper foil at 30μm distance, and (3) with copper foil at 30μm distance and with under-fill material in-between the transformer and the package 53
4.6 EM simulation results for a 135GHz inter-stage matching transformer (a) transformer's primary inductance (b) Primary turn resistance (c) primary turn quality factor (d) K-coupling coefficient 54
4.7 adding copper pillar to both transmitter and receiver chips 55
4.8 Stack build up for MIMO array on high-performance laminate 58

4.9 8-element series-fed microstrip patch antenna (a) CMOS/antenna co-design and modeling using Ansys HFSS (b) EM model of CMOS chip interface plus copper pillars (c) CMOS chip ground plane structure and model on Ansys 59
4.10 8-elements series-fed patch antenna simulation (a) realized gain in the broadside direction (b) simulated S11 on smith chart (c) Gain Vs Frequency 60
4.11 MIMO tile design on Isola Astra MT77 (a) Single Tx/Rx channel footprint (b) Two channels designed to fit in 2λ spacing (c) a tile of 8-elements . . 61
4.12 Antenna array simulation using Ansys HFSS (a) 8x8 antenna array test bench (b) simulated array directivity and realized gain (c) antenna array simulated 3-dB bandwidth (d) 3D drawing for the array's radiation pattern 62
4.13 1-D MIMO tile frontend 63
4.14 1-D MIMO tile backend 63
4.15 Integrated 1D MIMO Tile on High-performance Laminate (a) Module cartoon drawing for the side-view (b) PCB layout with 4-channels on the right and 4-channels on the left 64
4.16 Fabricated PCB (a) test structure for a single transmitter channel (b) MIMO module/tile of 8-channels 65

5.1 (a) D-band integrated transmitter module (b) transmitter architecture, and (c) micrograph of the IC with copper pillars with a die area of 1.25mm$\times$ 2mm. 69
5.2 Ceramic interposer layer stack. 70
5.3 (a) Cu stud flip-chip transition, (b) Simulated performance of the chip transition (copper pillar plus CPW transition) 71
5.4 (a) Flip-chip transmitter mounted on carrier with wafer probe connection (b), and measured Pin-Pout characteristics of the mounted transmitter compared to that of an otherwise identical transmitter tested by on-wafer probing. 71
5.5 Series-fed patch antenna (a) simulated antenna structure (b)smith chart of antenna matching network. 72
5.6 Series-fed patch antenna measurement setup (a) schematic of the testing setup (b) actual measurement setup 73
5.7 (a) Antenna measured gain and return loss vs. frequency, (b) measured antenna radiation pattern 73
5.8 Transmitter modulation bandwidth measurement setup (a) schematic of the testing setup (b) actual measurement setup 74
5.9 (a) measured transmitter frequency response, (b) and input-output power characteristics. 74
5.10 Transmitter module modulation characterization setup 75

5.11 Transmitter module measured modulation constellations and computed error vector magnitudes. Power levels are quoted relative to the saturated output power. 76
5.12 D-band transmitter module (a) micrograph and (b) schematic cross-section. 77
5.13 Power amplifier mounting in the ceramic carrier (a) with cavity and (b) without cavity. 78
5.14 CMOS transmitter to InP transition design (a) Impedance matching network on HFSS (b) Matching network S-parameters (c) InP-LTCC transition 79
5.15 CMOS transmitter to InP transition design (a) Impedance matching network on HFSS (b) Matching network S-parameters (c) InP-LTCC transition 80
5.16 (a) Integrated transmitter module Gain and EIRP measurement setup, (b) Transmitter module frequency response (c) Pout Vs Pin characteristic 81
5.17 Module radiation pattern in E & H planes 82
5.18 Integrated transmitter module output spectrum 82
5.19 Transmitter module modulation characterization 83
5.20 Transmitter module measured modulation constellations and computed error vector magnitudes. 84
5.21 Transmitter module measured error vector magnitude (a) vs. EIRP for different modulation constellations at 1GBaud symbol rate (b) vs. symbol rate for different modulation constellations at 21dBm EIRP. 85
5.22 An eight channels transmitter tile of heterogeneously integrated CMOS transmitter and InP Power amplifier, assembled on Kyocera Gl771 ceramic carrier (a) carrier design using ADS (b) manufactured LTCC carrier by Kyocera Japan 87
5.23 CMOS transmitter and InP power amplifiers assembled on Kyocera GL771 ceramic carrier 88
5.24 MIMO tile backend interface card (PCB) (a) PCB design using Altium (b) manufactured interface card (c) PCB stack of 6-layer 89
5.25 Eight-channel 135GHz MIMO hub transmitter array tile module: (a) photograph of the overall module, (b) cross-section diagram showing the interface printed circuit boards , the LTCC carrier, connectors, and ICs. The overall module is 450mm × 15mm, while the LTCC carrier is approximately 12 mm × 33 mm 90
5.26 Transmitter module per-channel EIRP testing setup 90
5.27 Transmitter module measured per-channel EIRP vs input signal power . 91
5.28 Low power 8-channel 135GHz MIMO hub transmitter array tile module: (a) photograph of the overall module, (b) cross-section diagram showing the interface printed circuit boards , the LTCC carrier, connectors, and ICs 92

5.29 an 8-channel receiver tile with CMOS chips assembled on Kyocera GL771 (a) tile design using ADS (b) manufactured and assembled tile by Kyocera San Diego 92
5.30 Eight-channel 135GHz MIMO receiver array tile module: (a) photograph of the overall module, (b) cross-section diagram showing the interface printed circuit boards , the LTCC carrier, connectors, and ICs, and. The overall module is 450mm × 15mm, while the LTCC carrier is approximately 12 mm × 25 mm. 93
5.31 Receiver module per-channel conversion gain testing setup 94
5.32 Measured gains of the receiver channels on the 4-channel module. 94

6.1 The array (a) 4-cascaded tiles forming array of 32-elements, producing horizontally-steered beams having narrow lateral and moderate vertical beam width. (b) cartoon drawing for array installed on basestation towers and users are primarily distributed laterally over the ground, but some distributed vertically in tall buildings (c) Given a maximum building height, the range R decreases rapidly as the elevation angle ϕ increases, hence vertical beam steering is not required. 97
6.2 Experimental configuration for transmitter array characterization. The eight FPGA DACs each generate modulated data on a 1GHz IF and eight IQ downconverters generate IQ signals that drive the transmitter array. A test receiver, mounted on a rotation stage 15cm from the array, down converts the signal to a 1GHz IF, and an ADC on the FPGA captures the signal. (a) actual setup (b) simplified drawing 98
6.3 Measured transmitter array EIRP, measured at saturation, as a function of angle of radiation, with the array aimed at broadside. The angle of radiation is in the H-plane. 99
6.4 Measured transmitter array beam patterns with the array aimed at 5^0, 3^0, 0^0, -3^0 and -5^0 scan angles. 100
6.5 Measured transmitter QPSK and 16QAM modulation constellations and computed error vector magnitude. 101
6.6 Computed error vector magnitude, in dB relative to the constellation's RMS amplitude, as a function of data rate. 102
6.7 Measurement of the array simultaneously transmitting two signal beams, the graph shows the power (EIRP) in each of the two signal beams as a function of the angle of radiation. 102

6.8 Experimental configuration for receiver array characterization. The FPGA generates modulated data on a 1GHz IF, an IQ downconverter and IQ upconverter then convert this to a 4GHz IF, and a mm-wave mixer translates this to 136GHz, with an 128GHz image outside the receiver passband. The test transmitter is mounted on a rotation stage 15cm from the array. The receiver array generates 1GHz IF signals, at quadrature phase between I and Q; the I-signals are captured by the FPGA. 104
6.9 Measured array patterns for (a) the four-channel receiver, taken with the test transmitter located at nine different angular positions and (b) the eight-channel receiver, taken with the test transmitter located at seven different angular positions. 106
6.10 Measured receiver QPSK and 16QAM modulation constellations and computed error vector magnitude. 107
6.11 Computed error vector magnitude, in dB relative to the constellation's RMS amplitude, as a function of data rate. 108

List of Tables

3.1 Comparison between state-of-the-art designs for near-140GHz transceivers. 44

4.1 Comparison between high-performance laminate materials. 57

5.1 Comparison with state-of-the-art D-band transmitters 86

6.1 Comparison between state-of-the-art D-band (110-170GHz) multi-channel links and transmitter modules 103

6.2 Comparison between state-of-the-art multi-channel receiver modules at D-frequency band (110-170GHz) 109

Chapter 1

Introduction

1.1 Millimeter Wave Wireless Communication

Wireless communication systems witnessed a substantial increase in mobile data traffic. This trend will continue to grow, fueled by new innovative applications, for example, the Internet of Things, machine-to-machine communication, and immersive media formats. Ericsson mobility report [3] showed that the number of subscribed users per base station grows linearly with time, and the anticipated number of subscribed users will reach 9 billion by 2026. As augmented reality (AR), virtual reality (VR), and 360 video contents, emerging media formats require very high data rates and larger channel bandwidth. It is expected that the traffic associated with AR/VR applications will increase by 20 folds in the next five years [4]. Advanced modulation schemes, like orthogonal frequency-division multiplexing [5] and complex coding techniques, as low-density parity-check [6], are utilized to improve spectral efficiency. However, the dramatic increase in the number of subscribed users is causing capacity saturation for wireless standards < 6 GHz.

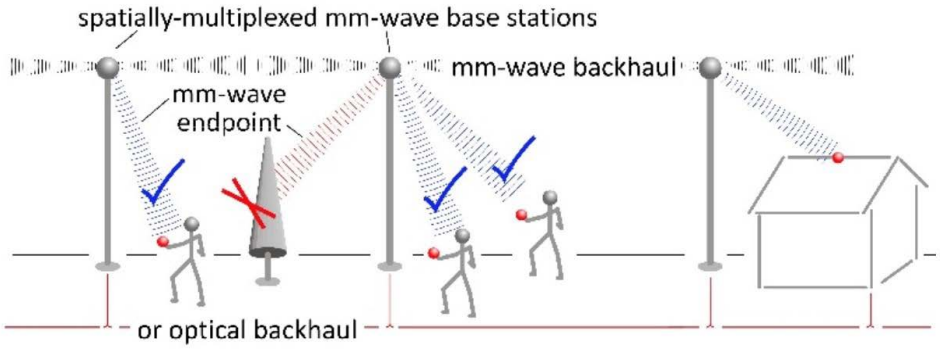


Figure 1.1: Spatially multiplexed networks for multi-Gigabit mobile and residential/office communication [1].

One potential solution to resolve the shortcomings of the existing communication systems and solve the channel capacity problem is to move to a higher frequency band. mm-Wave frequency band between 100GHz and 300GHz has a vast available spectrum; hence, we can use it to support very high data rates. The carrier wavelength is small; accordingly, we can build large arrays with many antennas in a small form factor. Those multiple antenna arrays can enhance the system capacity by utilizing spatial multiplexing (Fig. 1.1), where multiple beams are transmitted on multiple independent channels separated in space.

Building a reliable wireless communication system at the mm-wave frequency band is encountered by the fact that we have high atmospheric attenuation and high path loss (Fig. 1.2). Therefore, we need to build frontend modules with high output power and lower noise figures. Advanced silicon and III-V compounds technologies, with high power gain cut-off frequency f_{max}, made it possible to build complete transceivers above 100GHz [7] [8] [9]. However, to make those transceivers commercially affordable, we need low-cost, high-performance packaging technologies, which are very challenging to build at the mm-wave frequency range.

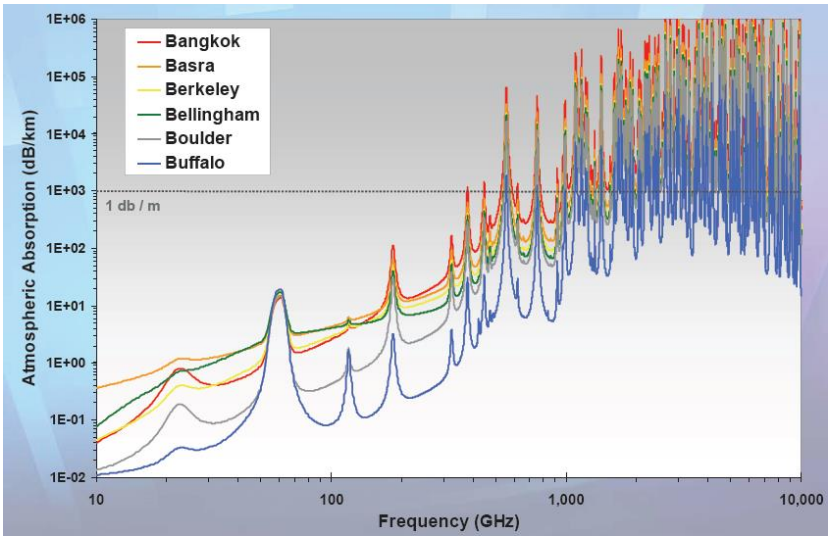


Figure 1.2: Approximate sketch of atmospheric attenuation vs. frequency for different cities [2].

Motivated by this background, this dissertation explores systems/ architectures, circuits, and packaging technologies suitable for very high data rates and high capacity applications. We built and demonstrate multiuser multiple-input multiple-output (MU-MIMO) arrays at D-frequency band ($135GHz$). We don't only provide a theoretical framework for building mm-wave multiuser massive MIMO arrays. Still, we go all the way from system analysis and design to building transmitters and receivers chips, then introducing, building, and fabricating two different packaging technologies for massive MIMO arrays at mm-wave frequencies (>100GHz). We show the design procedures for making massive MIMO arrays in a tileable fashion. We also illustrate the design steps for building high-gain, high-efficiency antennas on the package. The packaging approaches we pursued are intended to construct expandable arrays in a Lego-like fashion (Fig. 1.3), without the need to replace and substitute existing arrays. Finally, we show two different packaged MIMO arrays, one for short-range communication using CMOS only transmitters, and another array for long-range communication using a heterogeneously integrated CMOS transmitter +InP PA.

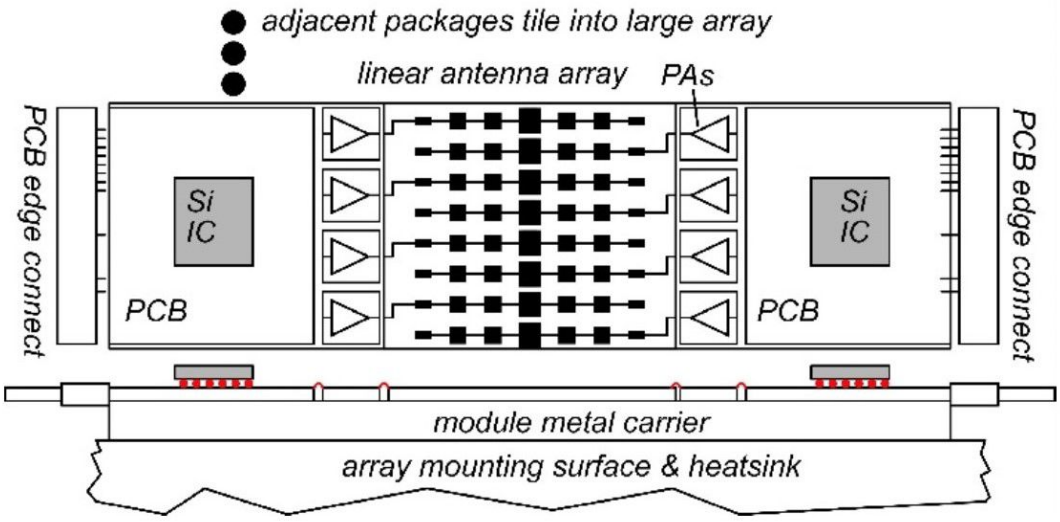


Figure 1.3: Array tile design for linear arrays providing beam steering in azimuth but not elevation [1].

To make our arrays compatible with a broad range of applications, we designed a low-cost PCB carrying the interface connectors to the digital backend. We integrated those low-cost PCBs with our MIMO transmitter/receiver tiles on the same module. We illustrate the capabilities of our MU-MIMO arrays by integrating our packaged Tx/Rx arrays with an FPGA evaluation board, and we did some link measurements with another commercial of the shelf transmitter and receivers. We calibrated the arrays and formed beams at different angles; we also showed that the array can support a broad range of modulation schemes with a record EIRP of 39dBm for the transmitter array.

1.2 Dissertation Contributions and Organization

Chapter 2 We introduce a comprehensive study of potential mm-wave MU-MIMO architectures from the linearity perspective. We compare between three different architectures: including fully digital, array of sub-arrays (hybrid), and fully RF, multiuser MIMO systems. We studied the specification on the frontend 1-dB compression point

(p_{1db}) and drew guidelines on the required analog-to-digital converter (ADC) number of bits for a base station uplink receiver. Our system model assumed a linear receiver array with uniform antenna spacing ($\lambda/2$) and uniform user distribution around the base station from 5m to 100m. We also studied a few different scenarios with power control and no power control and showed the impact of the antenna load factor on relaxing the linearity constraints.

Chapter 3 Based on the comparative study between potential MU massive-MIMO architectures, we concluded that all-digital architecture is the optimum architecture for our application. Hence, we designed and tested a single-channel direct conversion transmitter and a single-channel direct conversion receiver using GF 22FDSOI technology, without any RF, IF, or LO phase shifter since the beamforming is executed in the digital backend. In this chapter, we illustrate the capabilities of GF 22FDSOI technology. Then, we show the structure, circuit design, and measurement results for our transmitter, receiver chips, and some test structures. Finally, we conclude by comparing our Tx and Rx chips performance with the state-of-the-art transceivers designed at the same D frequency band.

Chapter 4 We present opportunities and challenges for mm-wave packaging technologies. We start by illustrating our perspective and approach in building mm-wave massive MIMO arrays in a tileable fashion. We show a few potential applications for our modular massive MIMO array. Then, we illustrate various IC-Package transition technologies and showing the pros and cons for each technology. Then, using the appropriate IC-Package transition technology (copper pillars) for our application, we illustrate the changes in our transceiver chips to accommodate those copper pillars. We pursued two different packaging approaches in parallel for the module development, where we built MIMO tiles

on a) high-performance, low permittivity laminate material and b) on a ceramic interposer. This chapter focus on building massive MIMO arrays on PCB (low permittivity laminate) and demystify all the challenges associated with this packaging approach.

Chapter 5 Here we focus on our second approach in building mm-wave massive MIMO arrays using ceramic carriers/interposers. We start by building a single channel CMOS transmitter integrated with a series-fed patch antenna on Kyocera LTCC carrier for the low-power MIMO module. Then, we illustrate the details and measurement results for our heterogeneously integrated high-power single channel transmitter on the same LTCC carrier. Next, we illustrate how to build the transmitter/receiver tiles of 8-channels using the same Kyocera carrier and build the MIMO module in a tileable fashion. We conclude this chapter by showing the structure and architecture of the integrated high-power MIMO module (tile) and the integrated receiver MIMO module.

Chapter 6 Here we illustrate the measurement results of the transmitter and receiver MIMO tiles. We start by showing an actual use case for our MIMO tiles and how to deploy our 1-D MIMO arrays in backhaul applications. Then, we show some measurement results for the high-power transmitter MIMO tile, including the array radiation pattern, Error vector magnitude for different modulation schemes, and radiation pattern for two beams transmitted simultaneously. Then, we show similar link measurement results for the receiver array while retrieving a single beam transmitted using another commercial of the shelf transmitter. We conclude by summarizing the pros and cons of using LTCC carriers in building mm-wave multiuser massive MIMO arrays and the efficacy of our tile approach in scaling up MIMO arrays.

The pros and cons of our first-generation packaged MIMO modules are shown in **Chapter 7**. We also show our current efforts in building the next-generation packaged arrays.

1.3 Permissions and Attributions

The material in this dissertation is partly based on the following publications. The dissertation author is the primary contributor to these published works and the co-authors have approved the use of the material for this dissertation.

1. **A. A. Farid**, et al., "A 27.5dBm EIRP D-Band Transmitter Module on a Ceramic Interposer" 2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Atlanta, GA, USA, 2021

2. **A. A. Farid**, et al., "A Packaged 135GHz 22nm FD-SOI CMOS Transmitter on an LTCC Carrier" 2021 IEEE International Microwave Symposium (IMS), Atlanta, GA, USA, 2021

3. **A. A. Farid**, et al., "Dynamic Range Requirements of Digital vs. RF and Tiled Beamforming in mm-Wave Massive MIMO" 2021 IEEE Radio and Wireless Symposium (RWS), 2021, pp. 46-48

4. **A. A. Farid**, et al., "A Broadband Direct Conversion Transmitter/Receiver at D-band Using CMOS 22nm FDSOI," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, MA, USA, 2019

5. **A. A. Farid**, et al., "An 8-Channel 135GHz CMOS/InP/LTCC MIMO Transmitter Array Tile Module with 38.5dBm EIRP" 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021

6. **A. A. Farid**, et al., "135GHz CMOS / LTCC MIMO Receiver Array Tile Modules" 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021

Chapter 2

Millimeter-Wave Multiuser Massive MIMO Architecture Choice: Digital, Hybrid or RF?

2.1 Introduction

As mm-wave multiuser massive MIMO is proposed as a potential candidate to improve wireless systems capacity and support very high data rate wireless links [10], one critical question arises; what is the optimal multiuser massive MIMO architecture?

Empowered by the recent advance in silicon CMOS technology, low power and compact mm-wave transceivers are made available, paving the way for a separate RF chain for each antenna, enabling simultaneous formation of many independent beams. Once an RF chain is available for each antenna, it is possible to realize all-digital MIMO processing. However, a major concern is the received signal dynamic range. Specifically, given that an RF chain, with its ADC, may carry many user signals, can it deal with a presumably large dynamic range without compromising sensitivity or error rate [11]

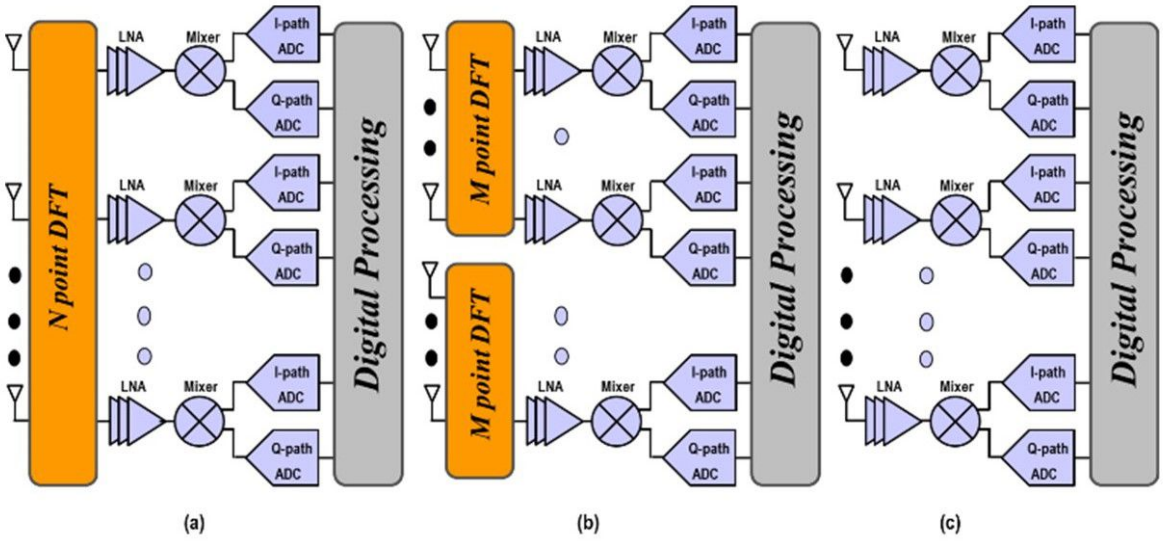


Figure 2.1: Multiuser massive MIMO beamforming architectures: (a) RF-beamforming (b) Array of subarrays (c) All-digital beamforming [11].

In this chapter, we compare all-digital MIMO processing with two other architectures which employ analog preprocessing to reduce the effective number of users served by an RF chain. The first is RF beamforming (Fig. 2.1a), in which the signals from the N antennas are first converted to signals from the array's N resolvable angular signal directions. This is expected to reduce the dynamic range prior to ADC, since fewer users fall into each beam. Subsequent digital processing then separates the signals from the individual users, these being distributed in random positions not corresponding to the array's N resolvable directions. The second is tiled RF beamforming (Fig. 2.1b), in which the signals are separated by coarse angular direction by RF processing in each array tile, with subsequent digital processing.

Recent work shows the feasibility of all-digital mmWave multiuser MIMO processing [12] and provides an analytical framework for determining allowable levels of non-linearity. Here we compare the requirements on the frontend (LNA and Mixer) P1dB and ADC resolution across the three architectures

2.2 Beamforming Architectures

In the RF beamforming architecture, a discrete Fourier transform (DFT) is performed at the receiver input (Fig. 2.1a). This DFT can be Implemented by a passive Butler Matrix [13] or a physical or Rotman lens [14]. The complexity of Butler matrices increases as Nlog(N), where N is the number of antennas, making these unattractive for massive MIMO systems having many antennas. Thus, we also investigate tiled subarray beamforming (Fig. 2.1b) to determine whether this relaxes either the required linearity of the RF chains or the required ADC resolution. In this approach, the array uses M tiles, each with an N/M-point DFT (e.g. a Butler matrix). Finally, we consider the all-digital array (Fig. 2.1c). In all cases, the final MIMO processing is digital, with N digitized I/Q streams being processed [15]. The goal of RF beamforming and tiled RF beamforming is to reduce the dynamic range per RF chain, not to reduce the number of RF chains, unlike prior work on hybrid analog/digital MIMO architectures.

Consider not the radiation pattern of the full array, but that of the individual tile DFT beamformer outputs, the latter showing the spatial distribution of users carried by each RF channel. Fig. 2.2 compares this pattern for the three proposed architectures, given a system with 32 antennas. As designs progress from all-digital to fully RF, the radiation pattern at the DFT output progresses from being isotropic to highly directional. This implies that in RF and hybrid architectures, each individual RF chain carries signals from fewer users than in the RF chains in an all-digital array. Given finite RF component 1dB gain compression points and finite ADC resolution, these signals will cross-modulate, degrading the receiver sensitivity. Further, in RF and hybrid architectures, the signal from a given user is carried by fewer RF chains than in an all-digital array. Consequently, the cross-modulation between any two particular user signals occurs in fewer RF channels,

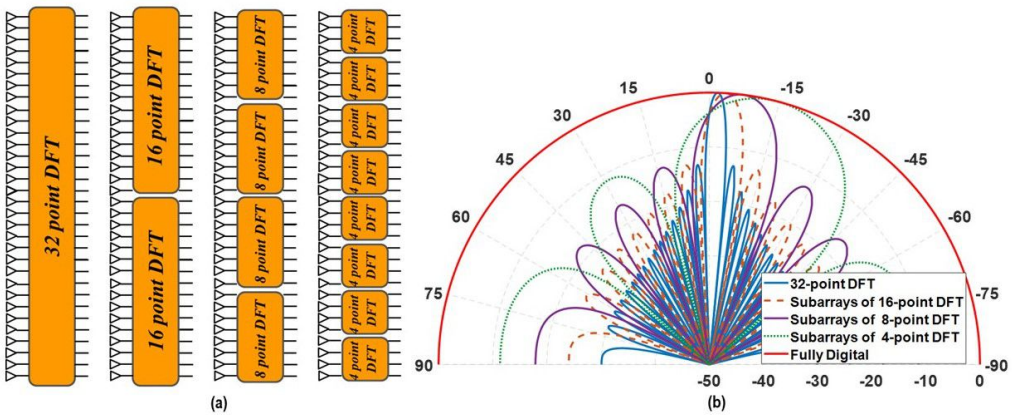


Figure 2.2: (a) RF beamforming architectures (b) and corresponding radiation patterns, at the DFT outputs for a 32-point DFT (the fully RF architecture), for 2 parallel subarrays having 16-point DFTs, for 4 parallel subarrays having 8-point DFTs, and for 8 parallel subarrays having 4-point DFTs. [11].

and is less suppressed by averaging than cross-modulation across many channels. We seek to determine which architecture suffers the smallest sensitivity degradation from these receiver nonlinearities.

2.3 System Model and Users Distribution

2.3.1 System Model

Our system is a linear (1-D) uplink MIMO array with a uniform $\lambda/2$ antenna spacing (Fig. 2.3). We constrain the field of view to (-60, 60) degree, hence no grating lobes appear in the array radiation pattern. Users are randomly distributed, with a uniform spatial probability distribution around the base station, between 5-100m range (Fig. 2.4a). For example; for an array with K users, the location of any user can be described by the following equations

$$R_k = \sqrt{R_{\min}^2 + \text{uniRand}_{0\to 1}\left(R_{\max}^2 - R_{\min}^2\right)} \tag{2.1}$$

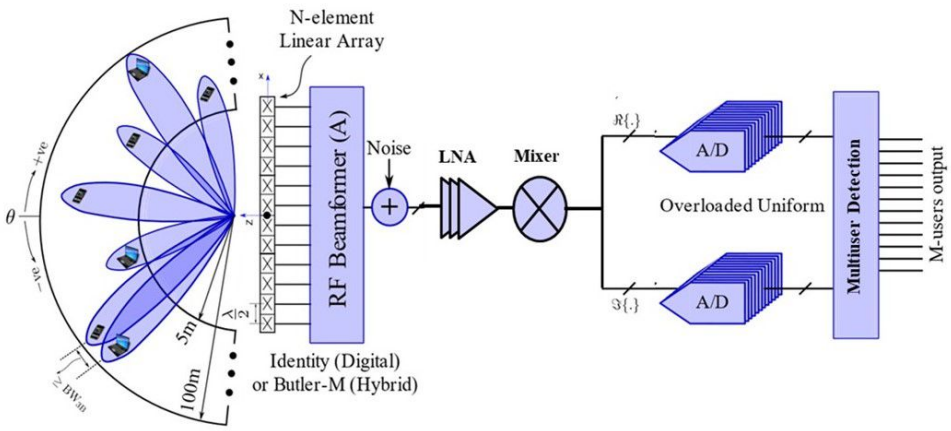


Figure 2.3: mmWave multiuser massive MIMO system model with a fixed frontend matrix, this matrix deploys N-point DFT for fully-RF, or N/M M-point DFT for hybrid or identity matrix for all-digital solution. [11].

$$\Theta_k = rand(-60^0, 60^0) \tag{2.2}$$

Where in this case study $R_{\min} = 5m$ and $R_{\max} = 100m$

To suppress statistical fluctuations in the computed system performance arising from this random user distribution, for each set of system parameters under study, 1000 simulations are run, each with a different random user distribution. To avoid excessive interference between users, we enforce a minimum angular separation between users equal to the array 3-dB beamwidth, as shown in Fig. 2.4b [16]. The minimum angular separation between any 2 users can be defined by $\triangle\Omega_{min}$

$$\Omega_k = \frac{2\pi}{\lambda} d_x sin\theta_k \tag{2.3}$$

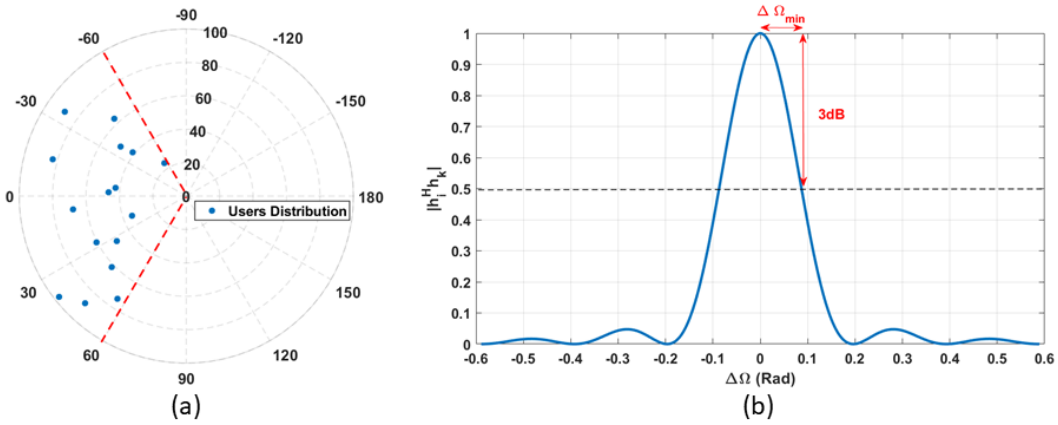


Figure 2.4: (a) Users distribution around base station (b) Normalized correlation between two users with spatial frequency difference of $\triangle\Omega$. Note that the closest users, depicted by red arrow, are separated by larger or equal to half the 3 dB beamwidth.)

where the spatial frequency Ω_k defines the angular location of user K, and the cross correlation between adjacent channels is constrained by

$$h_i^k h_k = \frac{1}{N} \sum_{n=0}^{N-1} e^{j(\Omega_i - \Omega_k)n} \tag{2.4}$$

$$|h_i^H h_k| = \frac{1}{N} \frac{\sin(\pi N \Delta\Omega_{i,k})}{\sin(\pi \Delta\Omega_{i,k})} < \frac{1}{2} \tag{2.5}$$

We assume line of sight (LOS) propagation between the users and the base station. The carrier frequency is 140 GHz and the data rate is 10 Gb/s/user. There are 16 users and either 32 or 64 antennas, giving load-factors β of 1/2 and 1/4. We assume a two different scenarios a) No power control and b)power control with 5dB precision, such that the power received at the array for each user is random, uniformly distributed over a 5dB range. Stated SNRs are that of users with power at the minimum extreme of the probability distribution.

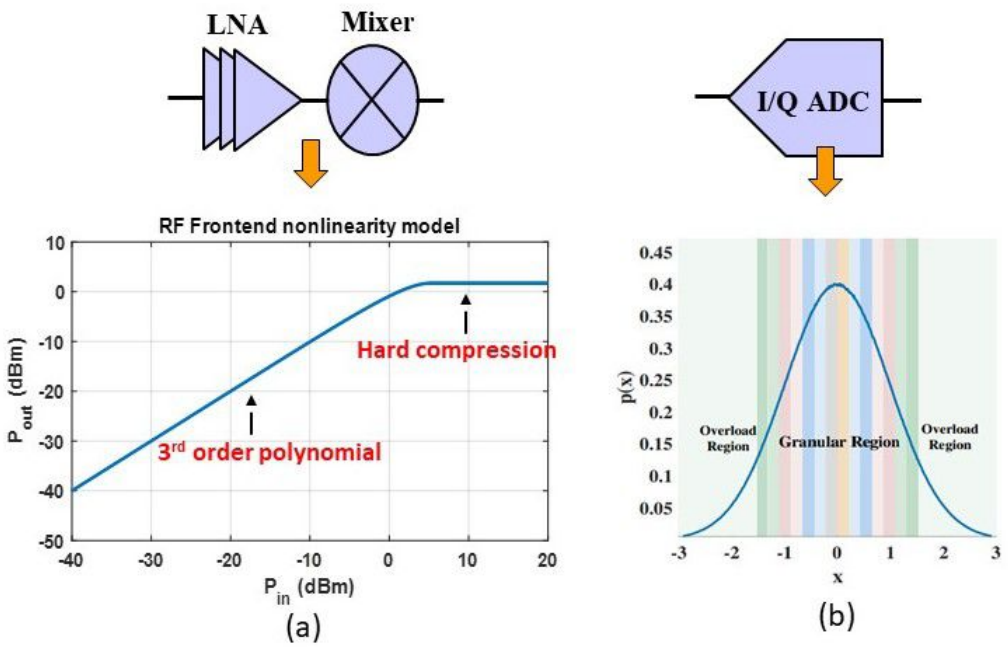


Figure 2.5: (a)LNA, Mixer frontend non-linearity model capture both soft and hard compression (b) Histogram of I and Q baseband components along with ADC quantization bins. [16]

2.3.2 Frontend nonlinearity and ADC Model

The nonlinearity of the low noise amplifier (LNA) and mixer are modelled by a saturated third order polynomial function with a unity gain, which can be expressed as a function of the 1-dB compression point (P_{1dB}) by

$$g(y(t)) = \begin{cases} y(t)(1 - \dfrac{0.44|y(t)|^2}{3P_{1dB}}) & if |y(t)|^2 \leq \dfrac{P_{1dB}}{0.44} \\ \dfrac{y(t)}{|y(t)|}\sqrt{P_{1dB}} & if |y(t)|^2 > \dfrac{P_{1dB}}{0.44} \end{cases} \tag{2.6}$$

For the quantizer, we use a uniform ADC which is preceded by automatic gain control (AGC) to fill the ADC dynamic range, optimizing the AGC gain to minimize the mean square quantization error, assuming a Gaussian input signal with zero mean and unity variance [16].

2.3.3 Digital Backend Engine

The digital backend processing is based on linear minimum mean square error receiver which can be represented by

$$z = E[xy^H]E[yy^H]^{-1}y \tag{2.7}$$

where x is the transmitted signal and y is the received signal at the antennas input.

2.4 System Analysis and Results

In this section we specify the required frontend P1dB and ADC resolution for each of the predefined architectures in section 2.2, using the system model described in section 2.3. We consider a massive MIMO system supporting 16 users and using QPSK modulation scheme. Our system metric is to achieve uncoded bit error rate (BER) of 10^{-3} which is adequate for a reliable performance using any of the well-established channel coding algorithms. In our analysis we considered two different scenarios;

a)Base station without power control; such that power received at the array for each user is random, uniformly distributed, and equivalent to the user distance from base station. As shown in Fig 2.6a

b)Base station with 5-dB power control; such that the power received at the array for each user is random, uniformly distributed over a 5dB range. As shown in Fig 2.6b

2.4.1 ADC Specification

In analyzing the required ADC resolution, nonlinearity in the RF chain is removed by setting its 1dB gain compression point to infinity. We then compute the receiver sensitivity as a function of the ADC resolution.

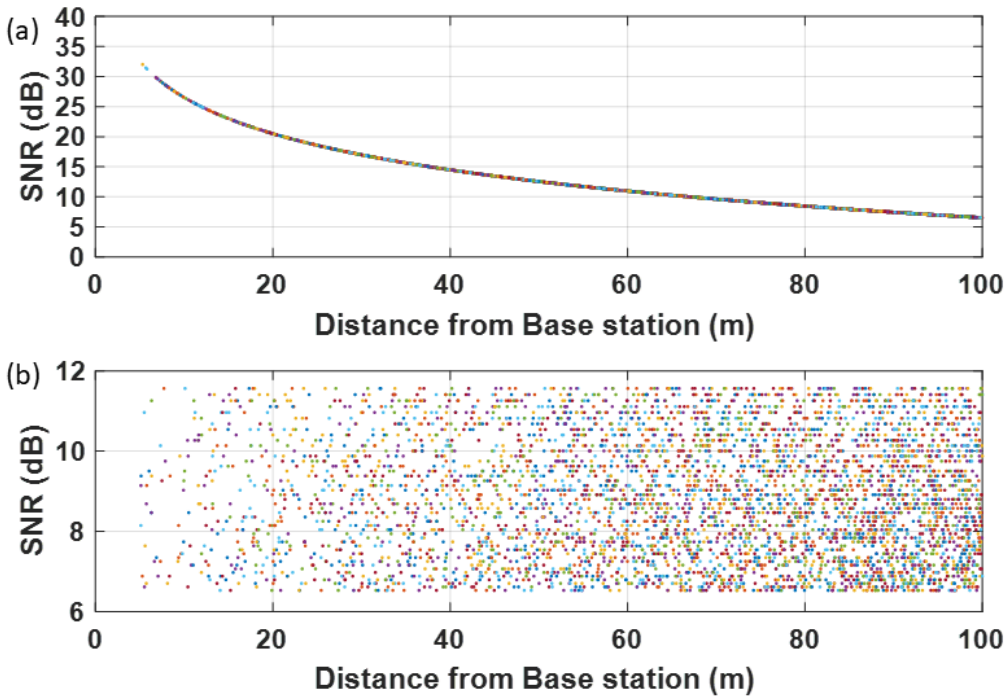


Figure 2.6: SNR at the array for each user(a)without power control (b) with 5-dB power control

1- Without Power Control:

Fig. 2.7a plots the maximum bit error rate (BER) experienced by 95% of the users, as a function of SNR_{min} , the SNR of a user whose received power at the minimum of the probability distribution associated with furthest user from the base station. The system has 16 users and 32 antennas, and the ADC resolution is 3 bits. Error rate vs. SNR is plotted for an all-digital beamformer, a full-RF beamformer, and tiled beamformers with either 4, 8, or 16 RF channels per tile (subarray). Going from all-digital to hybrid, then Fully RF architecture we can see improvement in the system's BER. However, only the Fully RF architecture can fulfill BER better than 10^{-3} for 95% of the users, with a relatively high SNR_{min} requirement of 20dB. In contrast, with 4-bits ADC resolution (Fig. 2.7b), all the proposed architectures can achieve the required raw BER of 10^{-3} for 95%, with a reasonable requirement on the SNR_{min}. The required SNR is 2dB smaller

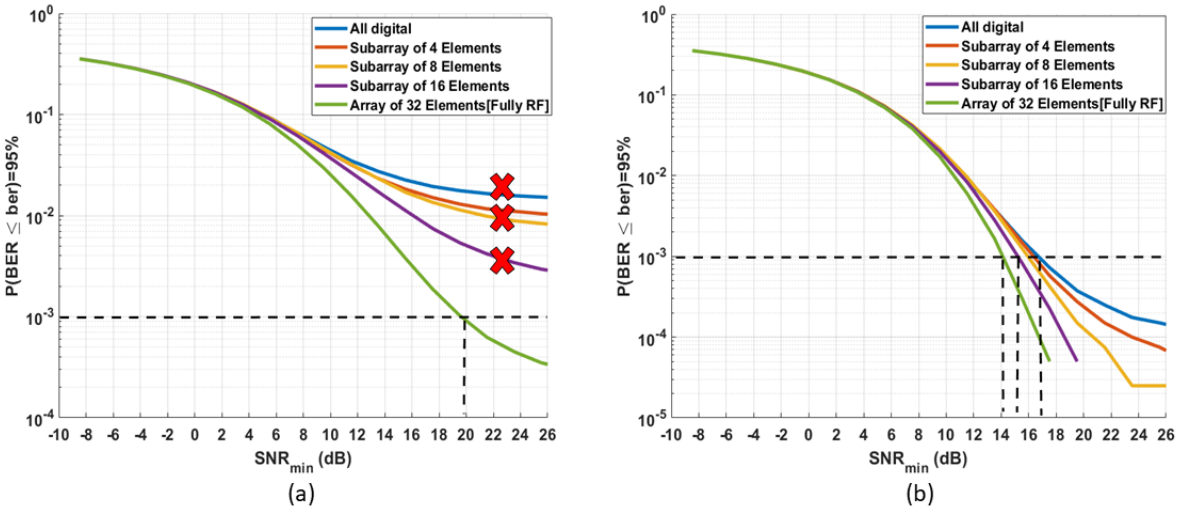


Figure 2.7: BER that 95% of users achieve vs SNR at 100m (SNR_{min}) for $\beta = 1/2$ (a) using 3-bits ADC (b) using 4-bits ADC. (W/O power control)

for the fully RF beamformer than for the fully digital beamformer. Which reflects that the efficacy of the fully-RF or hybrid architecture is marginal for higher resolution ADCs

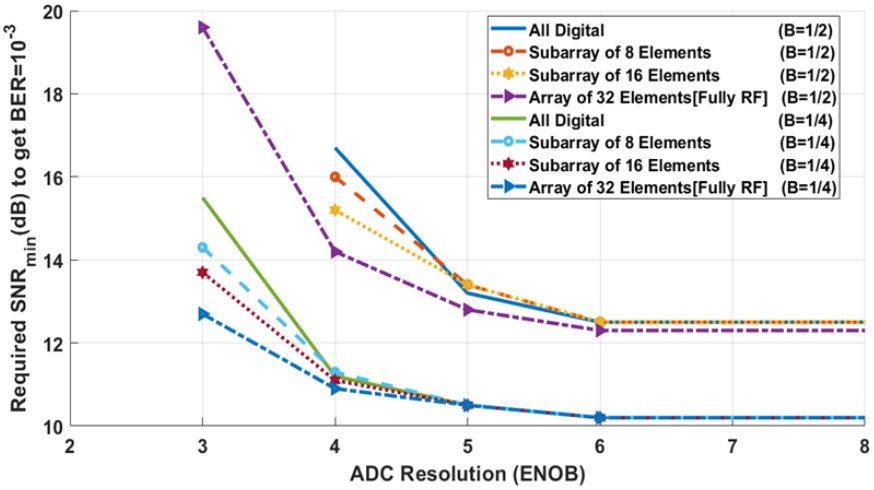


Figure 2.8: ADC performance summary for different architecture and different load factors (W/O power control)

Fig. 2.8 plots, as a function of ADC resolution, the SNR_{min} required for $< 10^{-3}$ BER for 95% of the users. In all cases, there are 16 users, but there are either 32 or 64 antennas

(load factors β of 1/2 and 1/4). The beamformers are all-digital, all-RF, or are tiled, with subarrays of 8, 16, or 32 elements. At β=1/2, the lowest ADC resolution to achieve the required BER is 4-bits, with a marginal relaxation on the SNR requirement going from all-digital to fully RF. At β=1/2 and using 3-bits ADC, the fully RF architecture is the only viable solution. At β=1/4, the lowest ADC resolution to achieve the required BER is 3-bits, with the same marginal relaxation on the SNR requirement going from all-digital to fully RF. Note that, as a consequence of spatial oversampling, lower load factors β require fewer bits of ADC resolution.

2-With 5 dB Power Control:

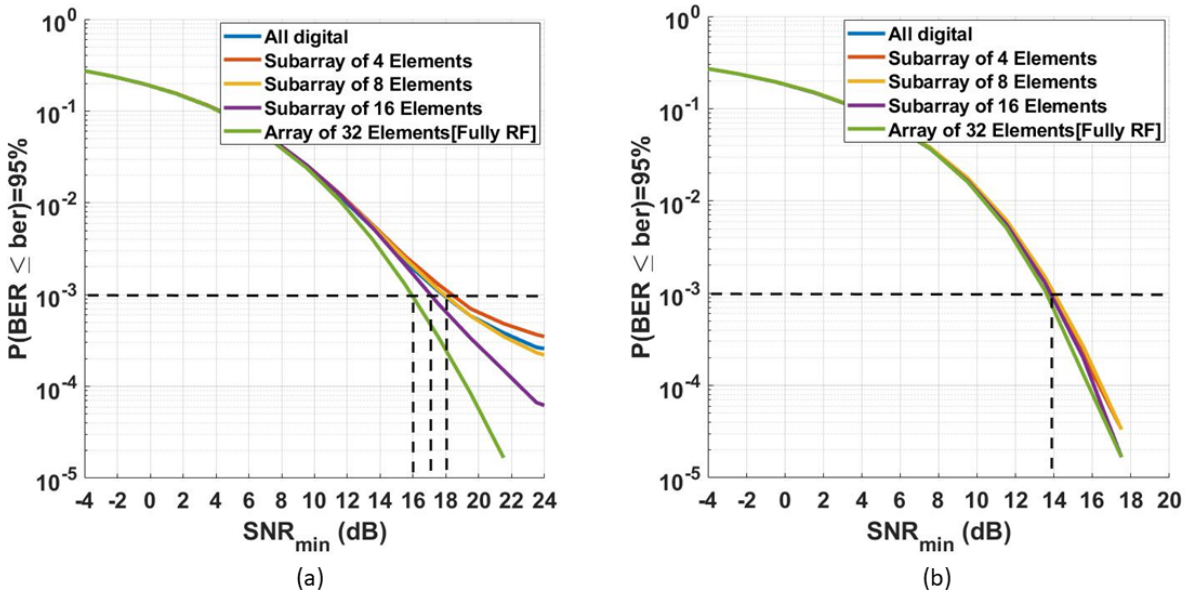


Figure 2.9: BER that 95% of users achieve vs SNR at 100m (SNR_{min}) for $\beta = 1/2$ (a) using 3-bits ADC (b) using 4-bits ADC. (With 5-dB power control)

Fig. 2.9a plot the maximum bit error rate (BER) experienced by 95% of the users, as a function of SNR_{min} , the SNR of a user whose received power at the minimum of the probability distribution associated with power leveling. The system has 16 users and

32 antennas, and the ADC resolution is 3 bits. Error rate vs. SNR is plotted for an all-digital beamformer, a full-RF beamformer, and tiled beamformers with either 4, 8, or 16 RF channels per tile (subarray). At better than 10^{-3} BER for 95% of the users, the required SNR is 2dB smaller for the fully RF beamformer than for the fully digital beamformer, with the various tiled beamformers requiring SNR intermediate between these limits. In contrast, with 4-bits ADC resolution (Fig. 2.9b), all five beamformers considered require almost identical SNR.

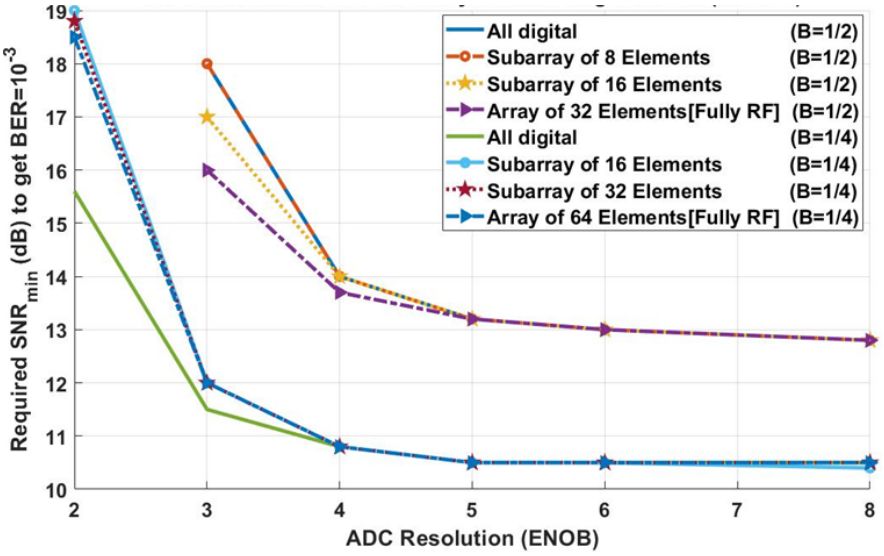


Figure 2.10: ADC performance summary for different architecture and different load factors (With 5-dB power control)

Fig. 2.10 plots, as a function of ADC resolution, the SNR_{min} required for $< 10^{-3}$ BER for 95% of the users. In all cases, there are 16 users, but there are either 32 or 64 antennas (load factors β of 1/2 and 1/4). The beamformers are all-digital, all-RF, or are tiled, with subarrays of 8, 16, or 32 elements. If the ADC resolution is set to cause at most 2dB sensitivity (required SNR) degradation, then, for all beamformers considered, the required ADC resolution differs by less than 1/3 bit. At 1dB maximum sensitivity degradation, the difference in required ADC resolution for the various beamformers is

negligible. These simulations show that the fully-RF and tiled beamformer architectures, as compared to all-digital beamforming, do not provide a significant advantage in required ADC resolution.

Note that at lower β factor ($\beta <= 1/4$) and no power control (Fig .2.8) we noticed that the fully RF is still slightly better compared to all-digital architecture using low-resolution ADCs (i.e., 3-bits ADC). However, at the same small load factor $\beta <= 1/4$ and using power control (Fig. 2.10) we noticed that the all-digital is slightly better than fully-RF architecture using low-resolution ADCs. This is happening because we have two competing factors; Peak-to-average power ratio (PAPR) and quantization noise. In the absence of power control, the dominant factor is the peak-to-average power ratio; that is why the fully-RF is always slightly better than all other architecture. However, once we introduce power control, the PAPR is slightly relaxed, and the quantization noise equally contributes to the system's sensitivity. Hence, with power control and a small load factor, the quantization noise is the dominant factor affecting the system's sensitivity. Once we use all-digital architecture, the quantization noise is averaged out on a larger number of channels, and the all-digital architecture wins in this comparison.

2.4.2 P1dB Specification

Analysis for the required 1dB gain compression points is similar. Infinite ADC resolution is assumed, and we compute the receiver sensitivity versus the RF channel's 1dB gain compression point. The required 1dB gain compression points are computed relative to the average, over time and over the random user spatial distribution, of the RF chain's signal power. The average RF signal power is set by the received power and the number of users, and is the same for all beamformer architectures considered.

1-Without Power Control:

Fig. 2.11 plots, as a function of the RF chain 1dB gain compression point relative to the average RF signal power, the SNRmin required for $< 10^{-3}$ BER for 95% of the users. Again, there are 16 users, 32 or 64 antennas (β =1/2 or 1/4), and the beamformers are all-digital, all-RF, or are tiled with subarrays of 8, 16, or 32 elements. For a load factor of 1/2 and 1/4, compared to all-RF beamforming, all-digital beamforming requires approximately 5dB greater P1dB in the RF signal chain. The requirement on the frontend non-linearity, represented by P1dB, is relaxed going from all-digtal, to subarray (with 8 or 16 channels per tile) to fully-RF. Note that the requirement on the P_{1dB}/P_{Avg} is relaxed by 4dB going from β=1/2 to β=1/4, due to spatial oversampling.

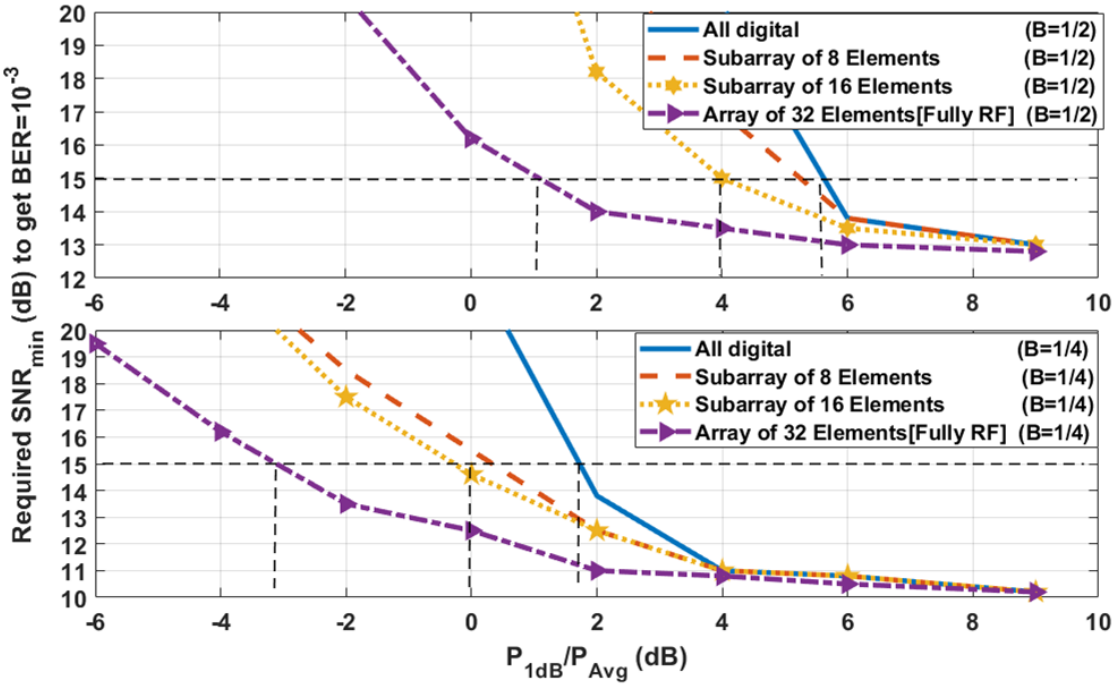


Figure 2.11: P1dB specification for different architectures and different load factors (W/O power control).

2-With 5-dB Power Control:

Fig. 2.12 shows that for a load factor of 1/2, compared to all-RF beamforming, all-digital beamforming requires approximately 1.5dB greater P1dB in the RF signal chain. In contrast, for a load factor of 1/4, compared to all-RF beamforming, all-digital beamforming requires approximately 2dB smaller P1dB. At either load factor considered, the tiled require 1-3dB greater P1dB. than either the RF or digital beamformers; there is no benefit in P1dB for the tiled

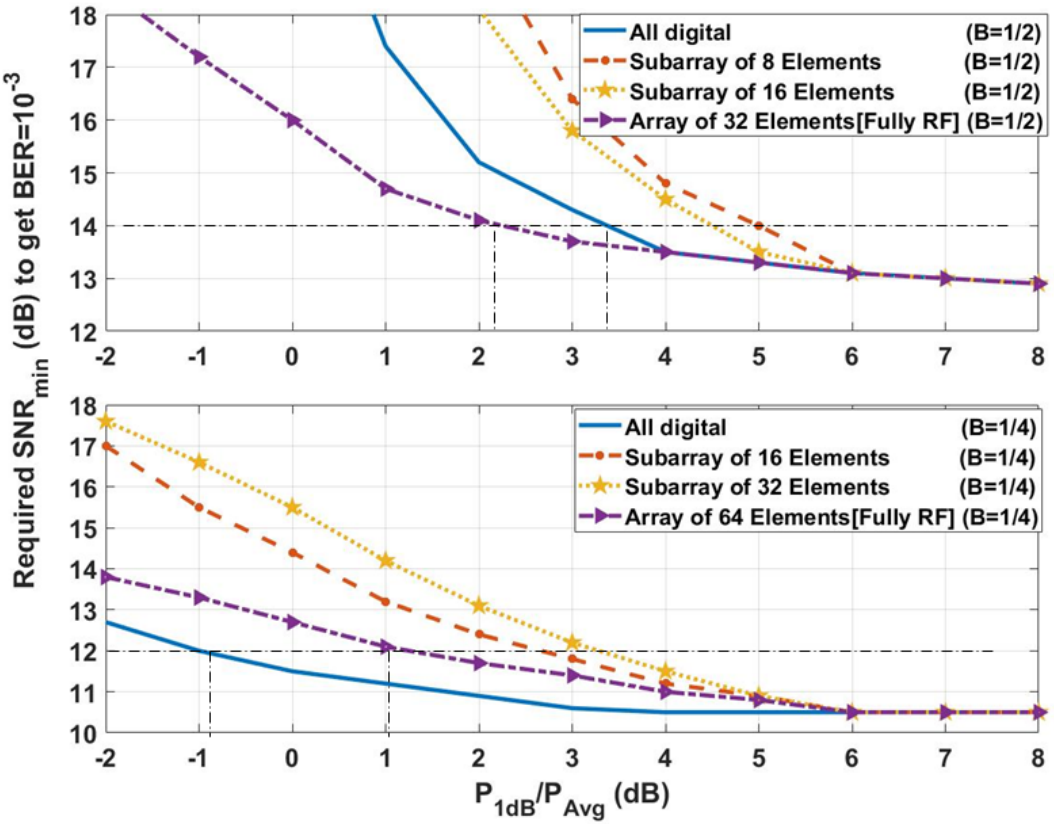


Figure 2.12: P1dB specification for different architectures and different load factors (With 5-dB power control).

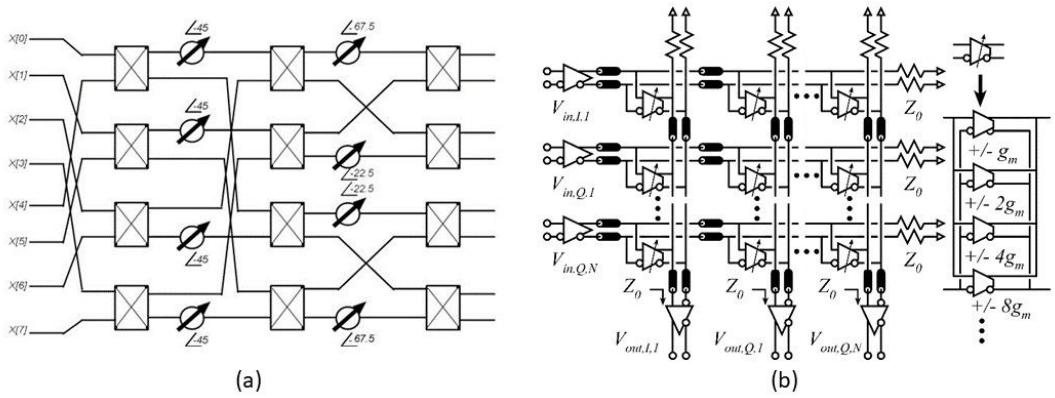


Figure 2.13: (a) 8x8 Butler Matrix (b) 4x4 Analog Beamforming Matrix

2.5 Why not Fully RF massive MU-MIMO?

From the previous sections we concluded that the all-digital beamforming does not require significantly greater ADC resolution or RF chain dynamic range than RF or tiled (hybrid) beamforming. Here we will illustrate another draw back on deploying fully-RF beamforming for multi-user massive MIMO.

Fig. 2.13 shows two different hardware architectures for implementing fully-RF beamforming matrices at the RF frontend. The Butler matrix has a few impairments which make it bad choice for massive MIMO architecture. Butler matrices have complex antenna routing, the number of direction couplers increase with Nlog(N), number of phase shifters increase with $N/2log(N)$, on top of that it is a passive structure with high insertion loss and high noise figure, this noise figure increases with $NlogN$. So, placing this structure in the frontend will heavily degrade the systems sensitivity and conversion gain. Similarly, the Analog beamforming matrices for multiuser arrays suffer from quantized gain, limited bandwidth, frequency dependent gain, I/Q routing complexity and I/Q imbalance.

2.6 Conclusions

This chapter compared a few potential mm-wave MU-massive MIMO architectures, including all-digital, hybrid (Array of subarrays), and fully-RF. We considered two different scenarios with power control and no power control. We conclude that the

- All-digital beamforming does not require significantly greater ADC resolution or RF chain dynamic range than RF or tiled (hybrid) beamforming.
- Fully RF beamforming complicates the frontend design (Area, power, NF, Antenna routing)
- All-digital beamforming with lower β is superior to fully RF and tiled beamforming architectures

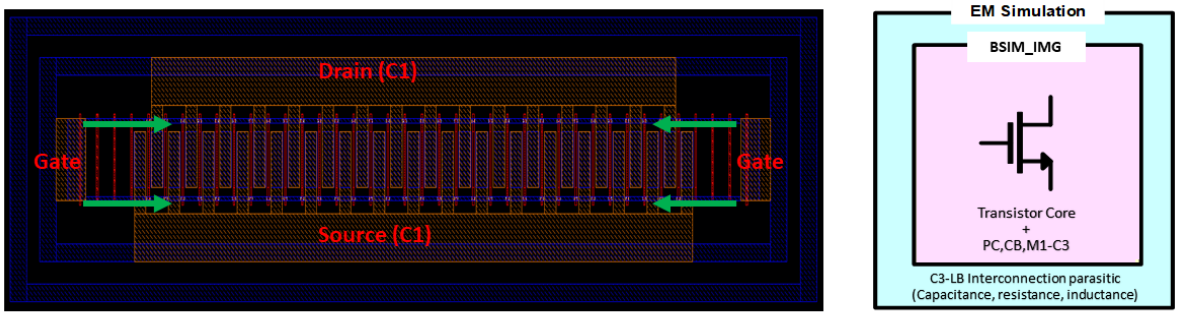
Hence, we build our hardware using the outcome of this study, and in the next few chapters, we will show the details of our all-digital massive MU-MIMO array.

Chapter 3

Broadband transceiver design at D-band using GF 22nm FDSOI CMOS technology

3.1 Introduction

From our system-level analysis (chapter 2), we concluded that the all-digital architecture is the optimum choice for mm-wave multiuser massive MIMO arrays from the linearity and power consumption perspective. Hence, the is no need to build RF, IF, or LO phase shifters in the frontend RF chain, and all the beamforming will be executed at the digital back-end, using any of the well-known digital beamforming techniques [18] [17]. In this chapter, a broadband single-channel transmitter and receiver at D-band are presented. These are designed to serve within 135GHz MIMO transceiver arrays/modules. Hence the baseband (I, Q) transmitter input and receiver output signals will be linear superpositions of data streams which must be subsequently separated by a baseband beamformer.



(a) (b)

Figure 3.1: SLVT Transistor footprint: (a) layout with gate relaxation. (b) parasitic extraction model.

3.2 Technology Characterization

The single-channel transmitter and receiver are designed using Global Foundries 22nm-FDSOI technology. The reported power gain cut-off frequency (f_{max}) and current gain cut-off frequency (f_t) for this technology are 230GHz and 240GHz, respectively, both referenced to the top metal layer [19]. The stack used provides 10 metal layers.

3.2.1 Transistor Footprint

The footprint of the core device used in this design is based on a super-low threshold voltage $SLVT$ NMOS with 32 fingers (Fig. 3.1a). The gate finger pitch is increased 2:1 above minimum to reduce C_{ds} and C_{gs} and to allow the placement of sufficient vias to satisfy electro-migration limits, when operating at $0.3mA/\mu m$ at 110^0C. Both the drain and gate are routed up to the top metal layer. The source is directly connected to ground through the lower 4 metal layers to reduce the source inductance. In our design and simulation the transistor is modeled as shown in Fig. 3.1b, where the BSIM model is used to capture the transistor parasitics from the substrate layer up to the fifth top metal layer, then we used EM tools (ADS Momentum) to model the stack from the fifth metal layer to the top Aluminum metal layer.

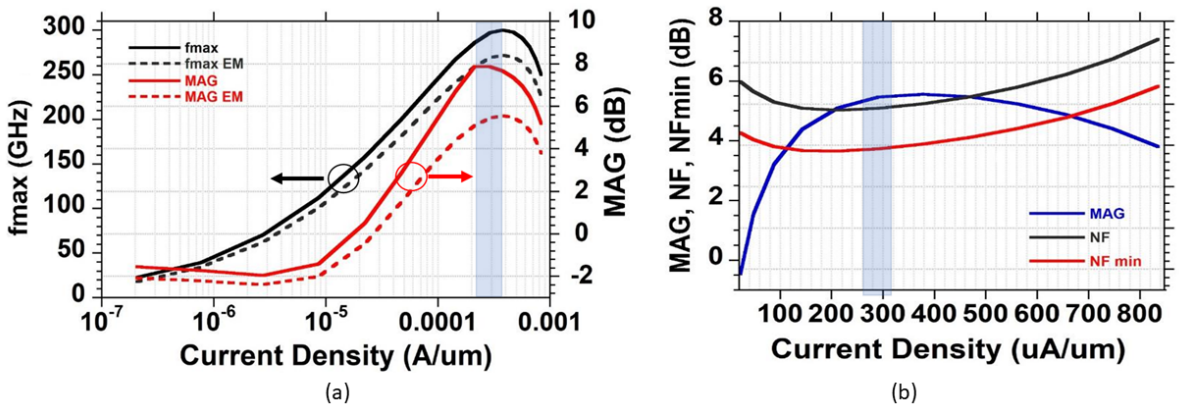


Figure 3.2: Transistor characteristics (a) Transistor f_{max} and MAG referenced to bottom Metal layer (M1) and to the top Metal layer (AL) (b) Transistors noise figure (NF) and NF_{min}

3.2.2 Transistor Characteristics

A single NMOS device is simulated in a common source configuration; to characterize the device f_{max} and Maximum available gain (MAG). At the optimum bias condition, with 0.8V supply and 0.55V gate bias, the transistor has a simulated f_{max} of 300GHz referenced to the bottom layer (M1). It drops to 250GHz when referencing the top Aluminum layer (LB) (Fig. 3.2). The simulated MAG of a single device at 135GHz is 5.5dB, including the routing losses of the LB layer. The simulated minimum noise figure NF_{min} =4dB and increase to 5dB when matched to 50Ω input impedance. Note that the SLVT device has the highest f_{max} in the 22FDX design kit, but this comes at the expense of the higher noise figure. In our transceiver design, we used the SLVT device, since the simulated f_{max} is almost twice the desired design frequency. Other devices in the 22FDX kit has lower f_{max} and f_t.

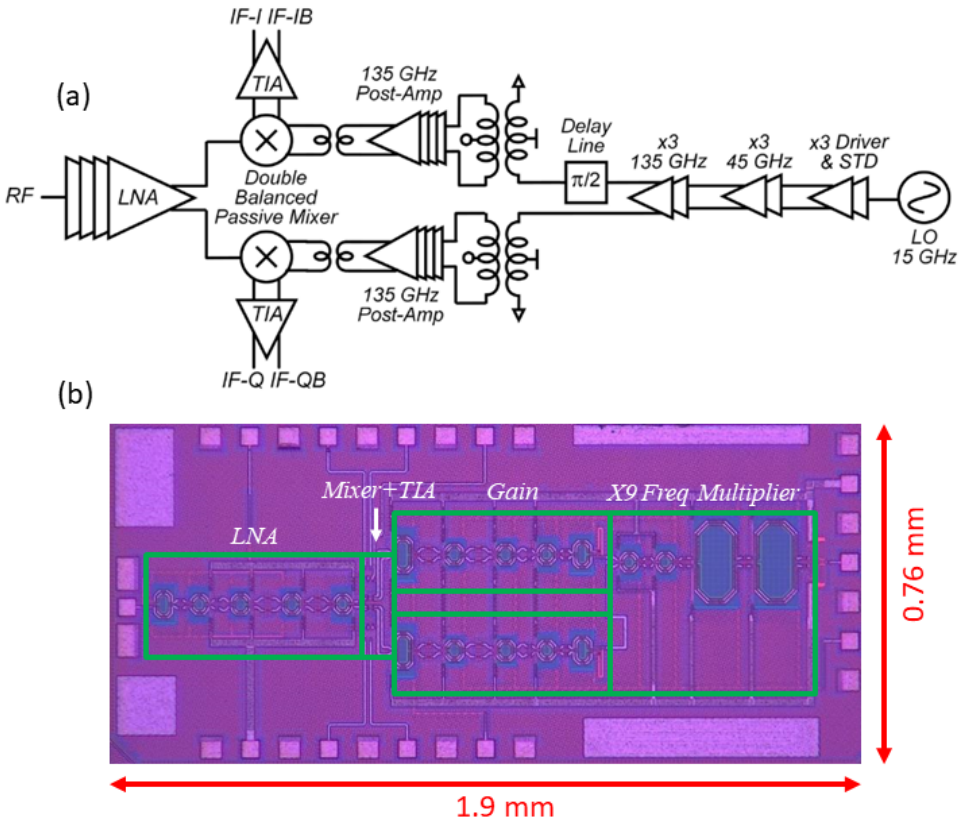


Figure 3.3: D-band single-channel direct conversion receiver (a) circuit block diagram and (b) chip micrograph. The die area is 1.9mm x 0.76mm including pads.

3.3 Receiver Architecture and Building Blocks

A direct conversion receiver (Fig. 3.3) consists of a 4-stage broadband Low-Noise-Amplifier (LNA) and a double-balanced passive mixer, followed by a pseudo-differential wideband transimpedance amplifier (TIA), for both in-phase (I) and quadrature phases (Q). The mixer is driven by an on-chip LO multiplier (x9), where the LO input signal is driven from an external source with -3dBm input power at 15GHz. The (I, Q) LO signals are generated by adding a ($\lambda/4$) delay line in the LO signal path, introducing a 90^0 phase shift.

3.3.1 D-band LNA/PA

A 4-stage fully differential common source LNA (Fig. 3.4a) is designed using a cross coupled pair with capacitive neutralization to boost the maximum available gain. The neutralization uses alternate polarity metal-oxide-metal (APMOM) capacitor (Fig. 3.4b). A center tapped transformer converts the single-ended input to a differential signal. Transformer center- taps provide DC bias feeds. For broad bandwidth, tuning of the inter-stage matching networks is staggered in frequency.

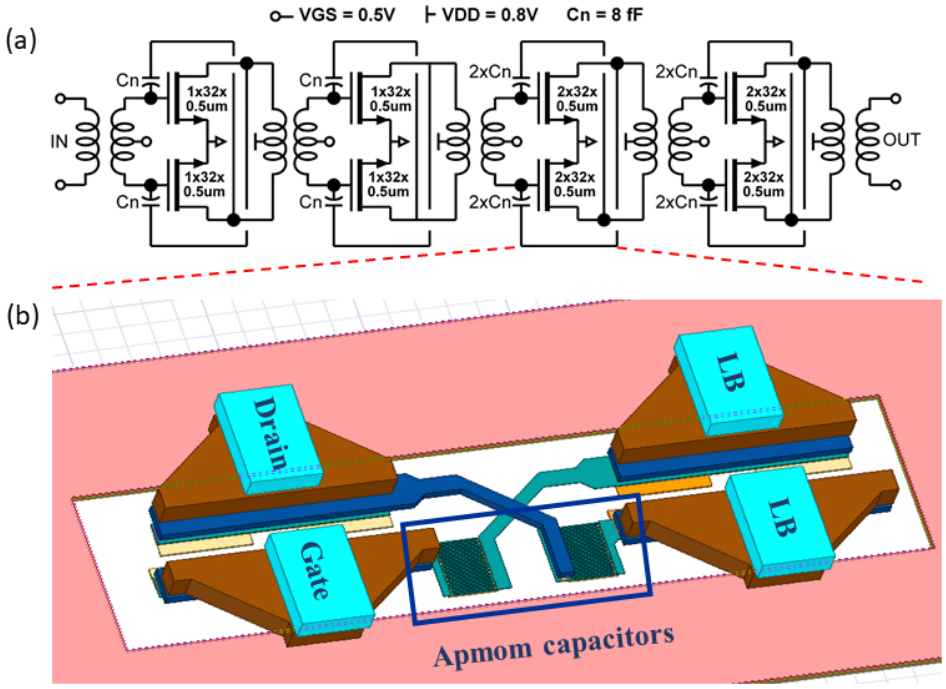
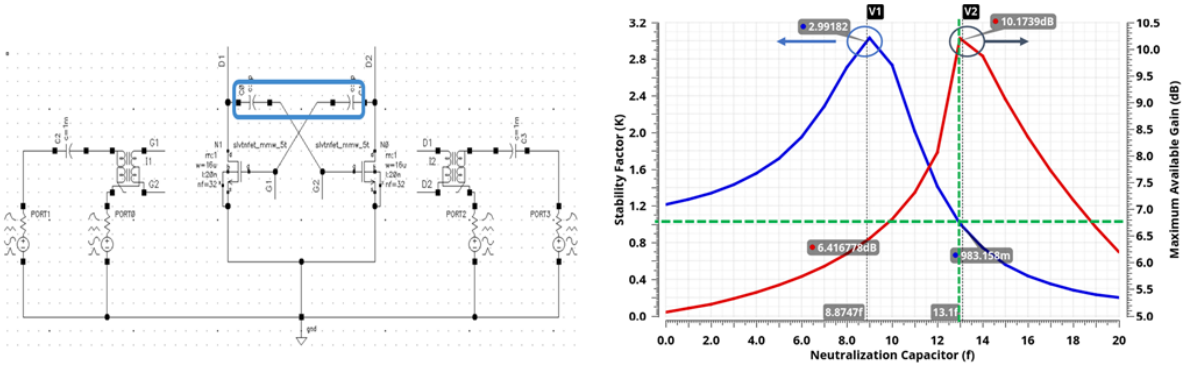


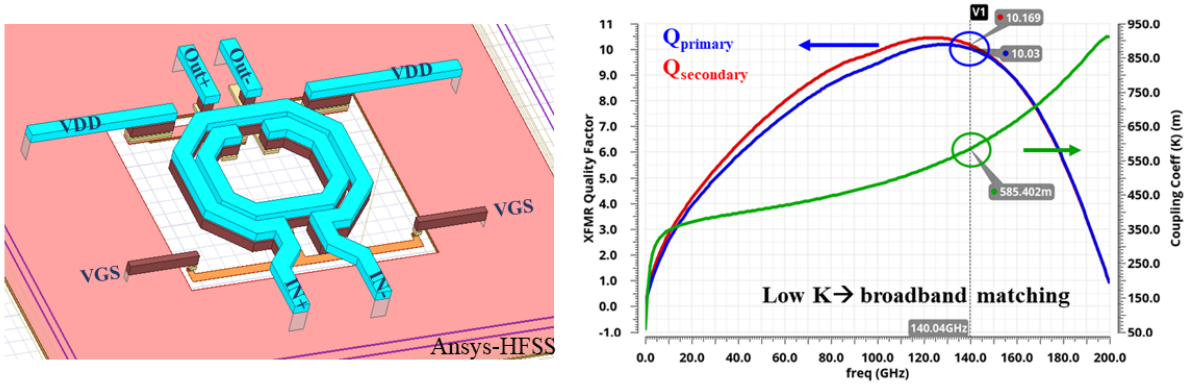
Figure 3.4: (a) Circuit diagram of a 4-stage broadband LNA/PA using staggered tuning (b) EM modeling of the cross coupled pair

We designed this amplifier to be used as an LNA in the Rx chain and as a PA in the Tx chain, so the first stage device sizing was chosen to fulfil minimum noise figure. However, we increased the last two stages device sizing to increase the saturated output power.



(a) (b)

Figure 3.5: Single differential pair gain stage (a) test bench to select the neutralization capacitance value, (b)simulated K-factor & MAG Vs neutralization cap value



(a) (b)

Figure 3.6: Single differential pair gain stage (a) test bench to select the neutralization capacitance value, (b)simulated K-factor & MAG Vs neutralization cap value

Neutralization Capacitor: The neutralization cap value should be carefully chosen [20] [21] to boost the gain and guarantee that each stage is unconditionally stable. Fig. 3.5a shows the test bench used to simulate the MAG and stability factor versus different neutralization cap values. Fig. 3.5b shows that the cap value in our design should be bounded between 8fF and 11fF to guarantee a stability factor (K) >1 while simultaneously boosting the MAG by 1 to 2 dBs. In our design, we used an 8fF APMOM cap to work in the safe region and keep some margin for the EM tool imprecise modeling.

Interstage Matching Transformer: The transformers are stacked using the top two wiring layers and were simulated using Keysight Momentum (Fig. 3.6a). For broadband design, in addition to staggering tuning interstage matching, we used a lower quality factor transformer with Q=10, as shown in Fig. 3.6b, with a nominal K factor $\simeq 0.6$. To avoid any potential instability all transformers were designed with self resonance frequency $>$ 200GHz

LNA/PA Simulation Results This LNA/PA draws 55 mA from a 0.8V supply, with a simulated gain of 16-dB and 40GHz 3-dB bandwidth. The simulated noise figure (NF) is 8.5dB (Fig. 3.7a). This relatively high NF is dominated by the noise contribution of the SLVT device, as shown in Fig. 3.2, and the insertion loss of the input matching balun. The simulated saturated output power P_{sat}=4dBm (Fig. 3.7b), limited by the device's current capability and the 2.5dB output balun insertion loss.

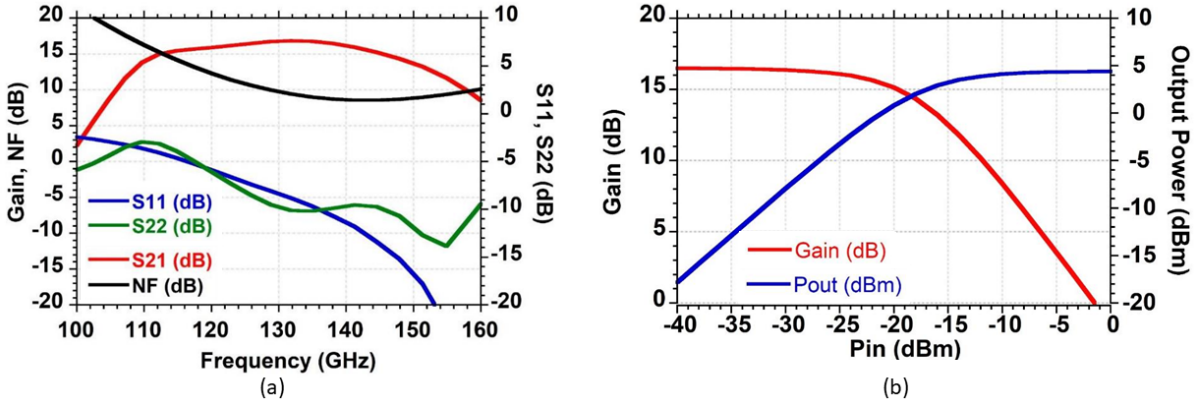


Figure 3.7: LNA/PA simulated (a) S-parameters and Noise Figure, (b)large signal gain and P_{sat}

3.3.2 Down Conversion Mixer and TIA

A pair of double balanced passive mixers (Fig. 3.8) down-convert the D-band signal to (I, Q) baseband. The differential output of the LNA (RF^+ and RF^-) drives both

mixer inputs through a transformer. The quadrature (I, Q) LO signals are converted to differential form by transformers before driving the FET mixer gates, and the mixer gate bias is driven through the transformer's center tap. The mixer (I, Q) outputs are DC-coupled to transimpedance amplifiers. The outputs of the LO multiplier are passed through a 4-stage post-amplifier before driving the mixer LO ports (Fig. 3.3a) to ensure sufficient LO drive power. Note that a passive mixer architecture was chosen for our application to support higher frontend P_{1dB}. The switches drain/source bias voltages come from the self-biased transimpedance amplifier (TIA), as shown in the next section.

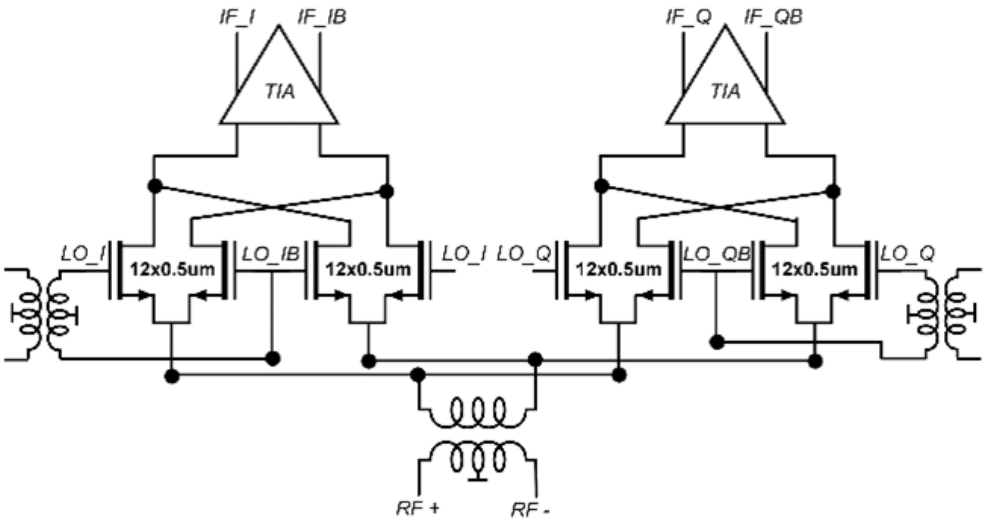


Figure 3.8: Circuit diagram of the (I/Q) down conversion mixer, followed by TIA

Transimpedance Amplifier (TIA): A pseudo-differential transimpedance amplifier provides the receivers' baseband gain. A three-stage voltage amplifier is first formed by an input self-biased gm stage cascaded with two voltage- gain stages formed from gm cells with local resistive feedback; adding global shunt resistive feedback forms a transimpedance amplifier (Fig. 3.9).

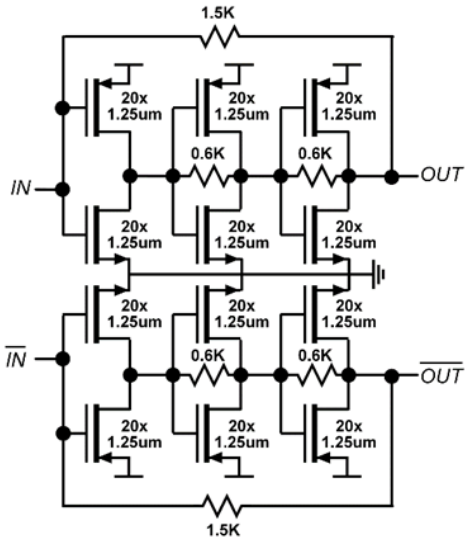


Figure 3.9: circuit diagram of pseudo-differential TIA

Integrated Mixer-TIA simulation results We integrated the down-conversion mixer with the TIA (Fig. 3.10) to check for the entire structure conversion gain and the optimum required LO output power. With TIA 50Ω load impedance the simulated conversion gain (Fig. 3.10 c) is 11-dB at an LO power of 0 to 3 dBm. The simulated mixer conversion loss is relatively high (9-dB) due to the small switch size. This smaller switch size was chosen to relax the requirement on the LO driving power, with a compromise on a relatively higher conversion loss. The TIA gain can compensate for the conversion loss. However, a higher LO power requires more gain stages at D-band, which is more power hungry and has a larger footprint. Note that while integrating the mixer with the TIA the feedback factor β should be < 1 to guarantee the stability of the RX chain. This condition was easily fulfilled in our design due to the small mixer's output impedance (from the TIA side).

TIA test structure measurement A test structure for a single ended TIA Fig. 3.11 was measured using on wafer probing. Fig. 3.11c shows the agreement in (S21) gain

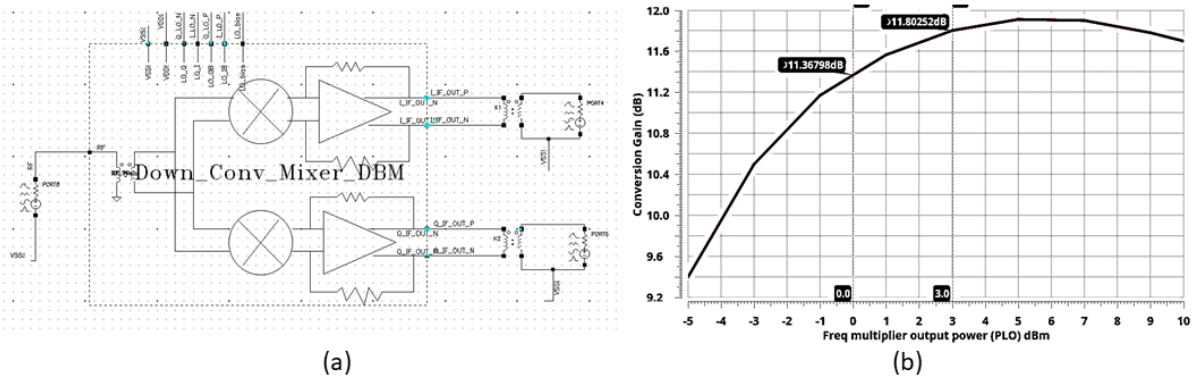


Figure 3.10: Integrated Mixer and TIA (a) schematic (b) conversion gain Vs LO power

between simulation and measurement. There is some discrepancy in the 3-dB bandwidth between simulation (22GHz) and measurement (17GHz), which may be due to errors in parasitic extraction. The measured S-parameters shows a notch at DC, this is because the test structure is a single ended, and the supply capacitance in the test structure resonates with the DC supply probe inductance. In the Rx chain, the design is less sensitive to supply inductance, as the design is pseudo-differential.

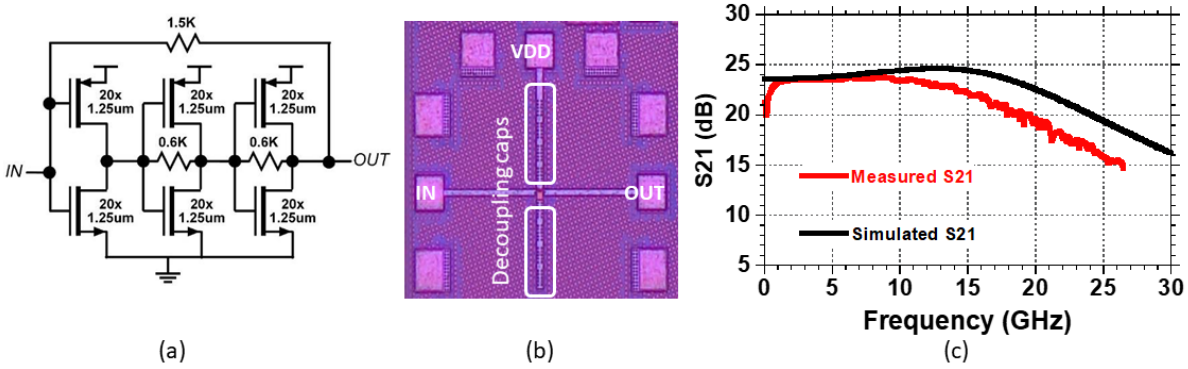


Figure 3.11: TIA test structure (a) schematic for the single ended test structure (b) chip micrograph of the TIA (c)simulation vs. measurement for single ended TIA test structure

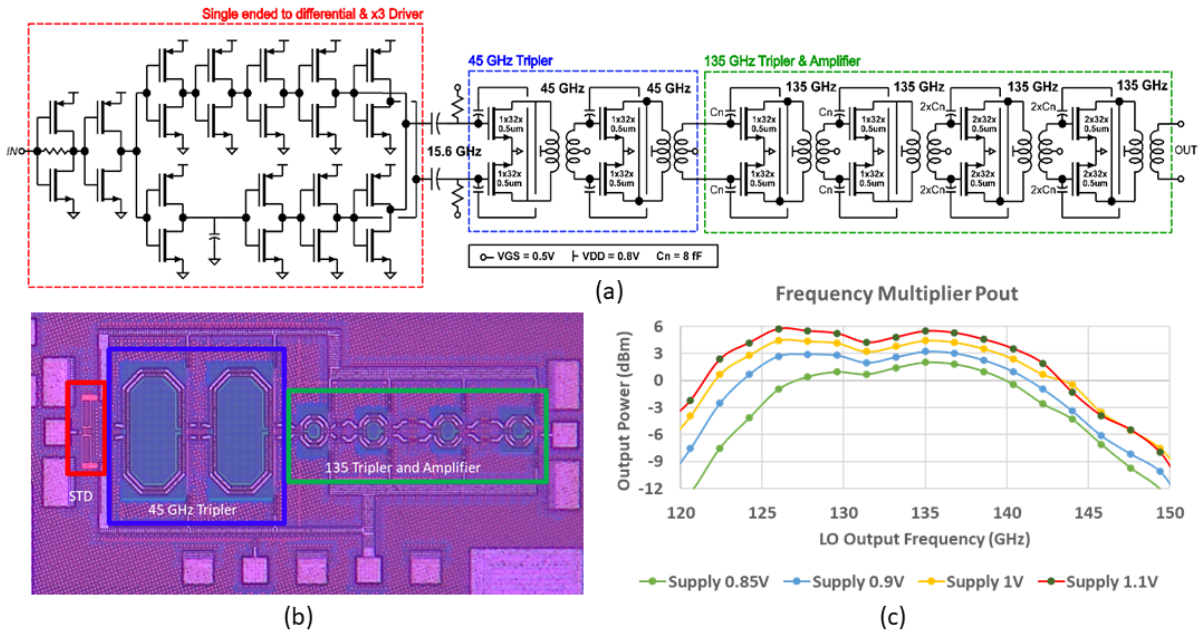


Figure 3.12: 135GHz 9:1 LO frequency multiplier (a) Circuit schematic, (b) chip micrograph of multiplier test structure (c) measured saturated output power

3.3.3 Frequency Multiplier and 135 GHz LO Generation

Both transmitter and receiver employ a 9:1 frequency multiplier to generate a 135GHz LO signal; using an external reference at 15GHz with -3dBm input power. The multiplier design consists of an inverter-based single ended to differential (STD) converter, followed by two cascaded 3:1 frequency multipliers (Fig. 3.12a). A fully differential structure reduces even harmonic generation and reduces supply coupling. The x3 frequency multipliers use a cross coupled pairs with capacitive neutralization, these driven into saturation to generate the third harmonic. The output of the first x3 multiplier is tuned at 45GHz (3rd harmonic of the input signal at 15GHz), while the second x3 multiplier is tuned at 135GHz. The topology and element values within the second 3:1 frequency multiplier are similar to those of the LNA/PA stages. The supply voltage of the entire chain is 0.8V. The simulated saturated output power is 3dBm and the simulated 3-dB bandwidth is 25GHz.

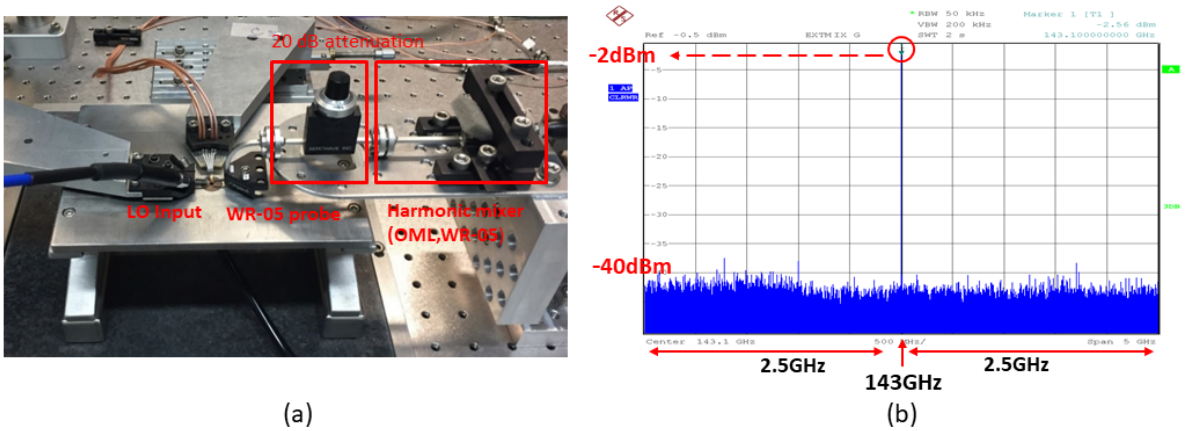


Figure 3.13: (a) Test bench used to test multiplier output spectrum (b) multiplier output spectrum at 143GHz with 5GHz span

A multiplier test structure (Fig. 3.12b) was tested using on-wafer probing, with the output connected to Virginia diode PM4 power meter. The saturated output power P_{sat} was measured for different supply voltage. At nominal bias conditions and 0.85V supply P_{sat}=2.8dBm , this saturated output power goes to 6dBm at 1.1V supply. The measured 3-dB bandwidth is 18GHz compared to 25GHz in simulation. We speculate that the discrepancy between the simulated and measured 3-dB bandwidth is due to inaccuracy in EM modeling of the metal filling close to the transformers and multiplier passive structures. The total power consumption of multiplier and the following 4 cascaded gain stages is 140mWatt from 0.85V supply.

The spectral purity of the frequency multiplier was tested using the test bench shown in Fig. 3.13a, where the multiplier output is connected to G-band harmonic mixer, and the mixer output is connected to a R & S spectrum analyzer. The result shows a clear spectrum over 5GHz span (Fig. 3.13b).

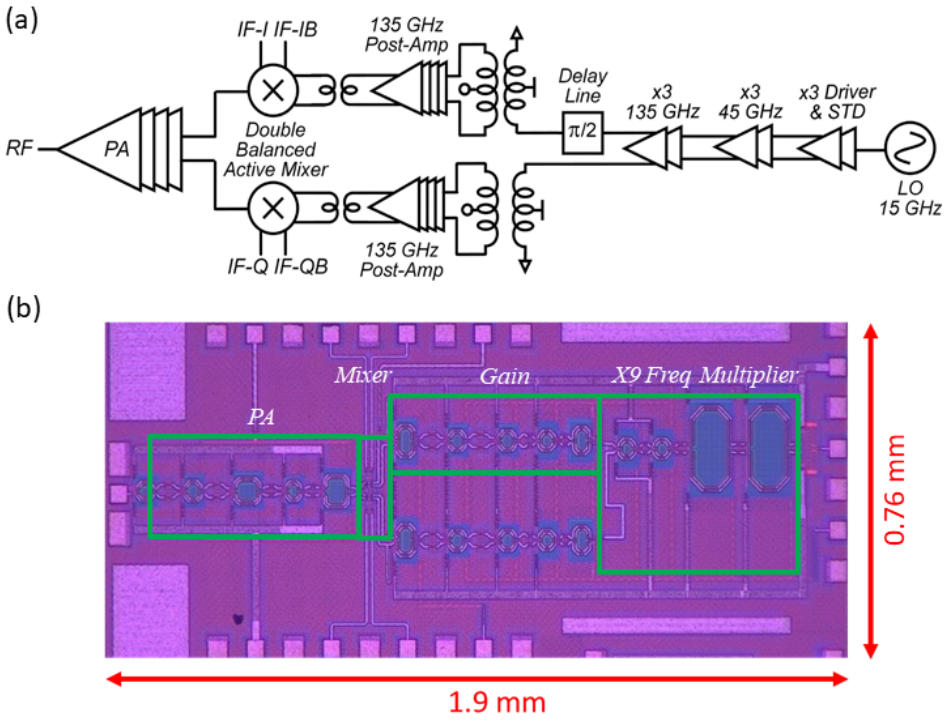


Figure 3.14: D-band single channel direct conversion transmitter (a) circuit block diagram (b) chip micrograph, including pads. The die area is 1.9mm x 0.76mm

3.4 Transmitter Architecture and Building Blocks

In the direct conversion transmitter (Fig. 3.14), a pair of double-balanced Gilbert-cell mixers upconverts the (I, Q) baseband signals to D-band. The (I, Q) signals are then summed and drive a broadband power amplifier. The LO multiplier is the same as that in the receiver. The power amplifier has the same 4-stages of cross coupled pair with capacitive neutralization, similar to the LNA, while the output stage is loadline matched to 50Ω impedance. An active Gilbert cell was used in the transmitter chain to drive the minimum required input power for the PA to drive it into saturation.

3.4.1 IQ Modulator

A pair of Gilbert cells serve as the IQ modulator (Fig. 3.15). The baseband inputs are DC coupled, while the LO and RF output ports are transformer-coupled. The tail and the baseband input stages were externally biased using bias Ts, with 350mV tails bias voltage, and the baseband signal was superimposed on a 450mV DC bias. A supply voltage of 800mV was driven through the center tap of the output matching transformer. The tail, base, and supply voltages were chosen to guarantee that the mixer is always working in the saturation region to avoid driving any stage into the triode region and introduce undesired non-linearity [22]. Despite being active stage, the gain of this Gilbert cell is less than 2dB in simulation. The gain is limited due to the small input impedance of the power amplifier. Note that a single supply voltage of 0.85V was used; hence, there is no room to add an output resistance for the Gilbert cell, as this will limit the headroom voltage on all the active devices and drive them into the triode region, introducing significant non-linearity.

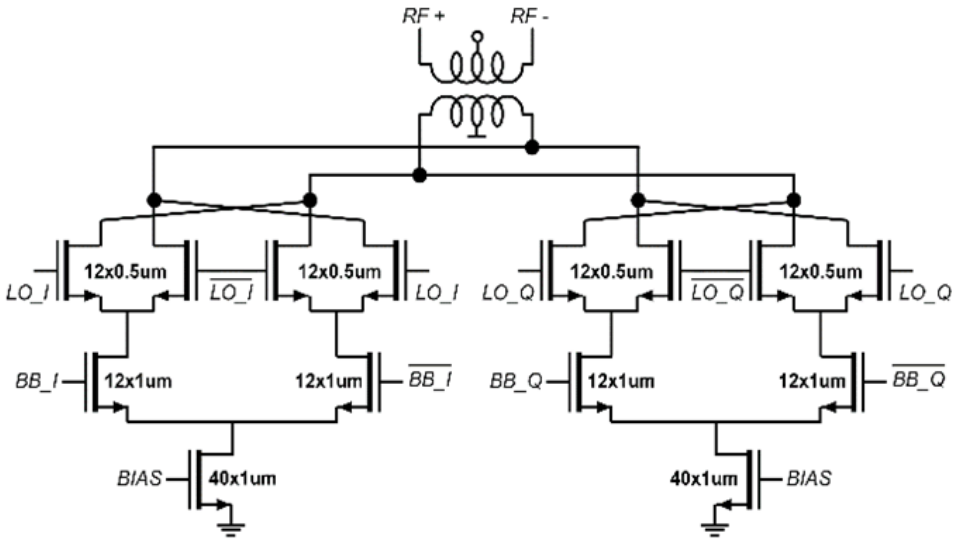


Figure 3.15: IQ modulator using Gilbert cells. The (I, Q) LO ports are transformer-coupled.

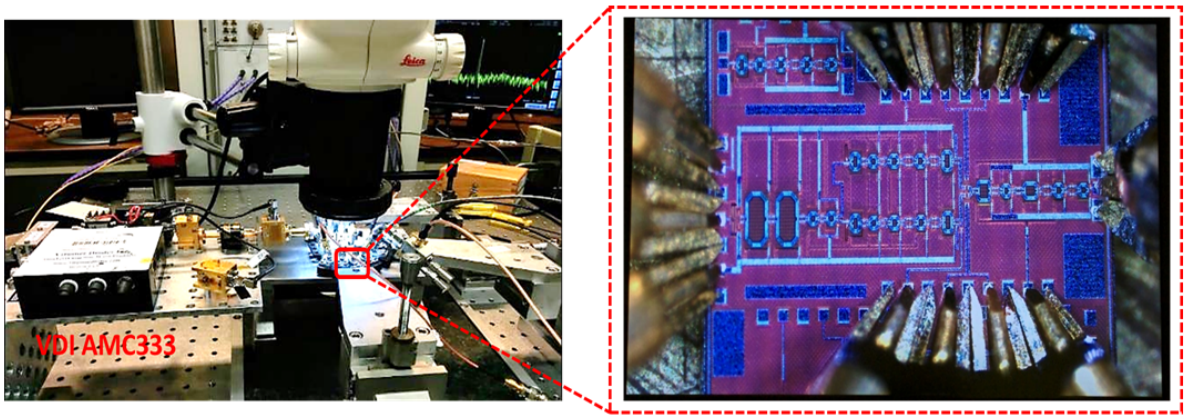


Figure 3.16: Receiver on wafer testing setup (a) Conversion gain and linearity measurement setup, (b) IQ, RF, and LO signal feed with GGB probes

3.5 Transmitter and Receiver Measurement Results

3.5.1 Receiver Measurements

Transmitter and receiver channels are fully characterized using on wafer probing. The receiver conversion gain is measured using Virginia diodes AMC 333 as the input signal source, followed by GGB (90-140 GHz) probe, to excite receiver input port (Fig. 3.16). The two differential outputs are terminated by 50Ω impedances during measurement.

Fig. 3.17a shows the measured conversion gain with LO signal fixed at 134GHz and 135GHz, while the input signal is swept from 122GHz to 155GHz. This measures the receiver modulation bandwidth. The measured gain is 27dB, after de-embedding probe loses and correcting for single ended to differential conversion. The 3-dB bandwidth is 20GHz. There is a good agreement between the measured and simulated gain. However, the simulated 3-dB BW is 1.5:1 larger than the measured, which might be explained as inaccuracy in apmom capacitor modeling in EM simulations, in addition to the limitation in the TIA 3-dB BW, as shown in section 3.3.2. Fig. 3.17b. shows the frequency

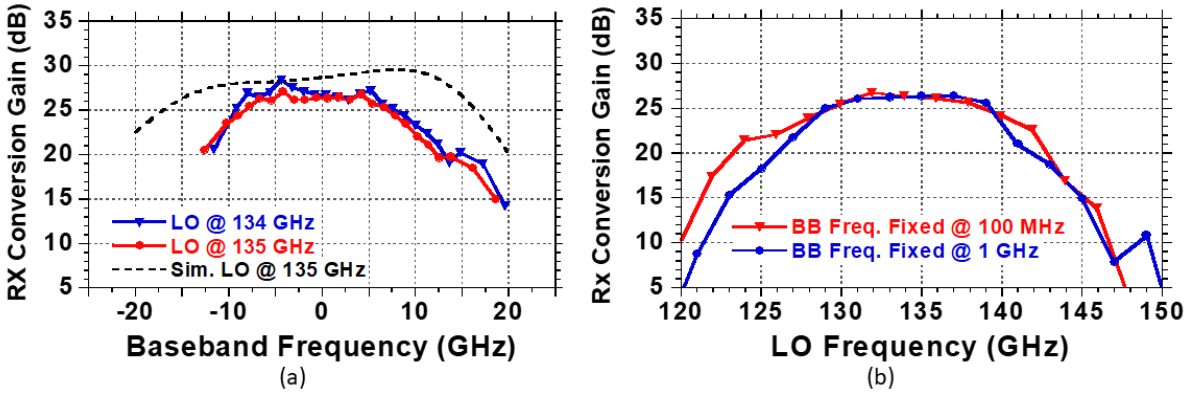


Figure 3.17: a) Receiver conversion gain vs. baseband frequency with a fixed LO frequency (b) Receiver conversion gain vs. LO frequency with fixed baseband frequency.

dependent conversion gain, with a fixed baseband frequency, where the RF and LO signals are swept to keep the baseband frequency fixed at either 1GHz or 100MHz. This measures the receiver RF tuning range. The 3-dB bandwidth here is limited to 10GHz; the smaller bandwidth than in the prior measurement reflects the tuning range of the LO source.

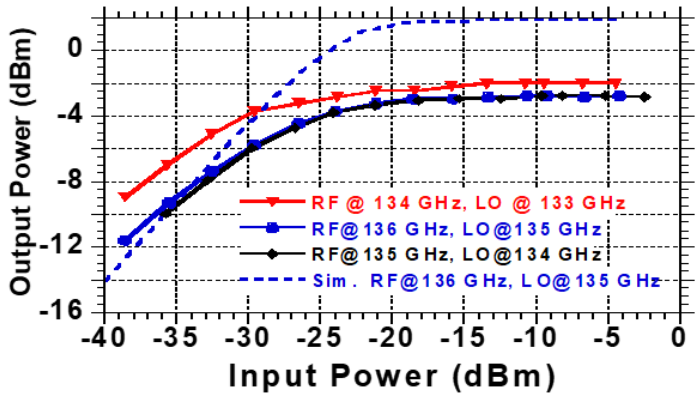


Figure 3.18: Receiver normalized output power vs. input power.

Receiver 1-dB compression point is measured (Fig. 3.18) at different LO frequencies. The measured input P1dB is -30dBm, which is slightly smaller than the simulated -26dBm. The receiver compression point is limited by the TIA drive capability, as this stage drives 50 Ω.

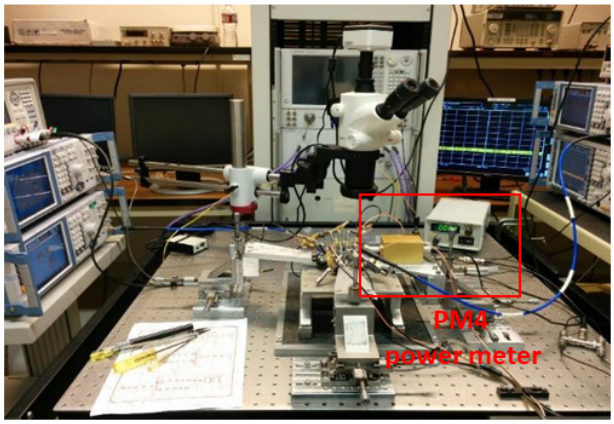


Figure 3.19: Transmitter measurement setup.

3.5.2 Transmitter Measurements

Transmitter saturated output power is measured using Erickson PM4 power meter (Fig. 3.19), where external signal generators drive the I and Q mixer inputs. To determine the transmitter saturated output power as a function of frequency, the transmitter was first driven by -3 dBm signals at 1, 2, or 5GHz at the (I, Q) ports, and the LO was swept from 125GHz to 145GHz (Fig. 3.20a). The saturated output power is 2.8dBm with a 3-dB bandwidth of 8 GHz. This determines the trasmitter frequency tuning range. Fig. 3.20b shows the normalized modulation sideband power with the baseband input frequency swept and the LO frequency held fixed. This measures the transmitter modulation response.

The output spectrum was measured using an OML M05HWD harmonic mixer and a Rohde & Schwarz spectrum analyzer. There is a good agreement between the simulated and measured 3-dB bandwidth. Fig. 3.21 shows the gain compression characteristics as a function of carrier frequency. This particular measurement shows approximately -7dBm LO leakage, because of incorrectly set DC levels at the transmitter baseband input ports.

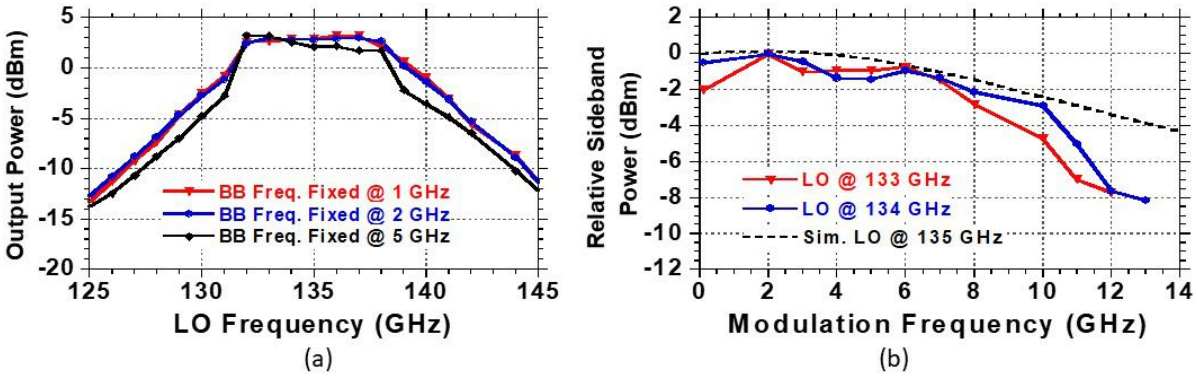


Figure 3.20: Transmitter characteristics. (a) Saturated output power as a function of carrier frequency, with a -3 dBm baseband input signal, this showing an 8 GHz RF tuning range. (b) Modulation sideband power as a function of modulation frequency, this showing a 8GHz (SSB) modulation bandwidth.

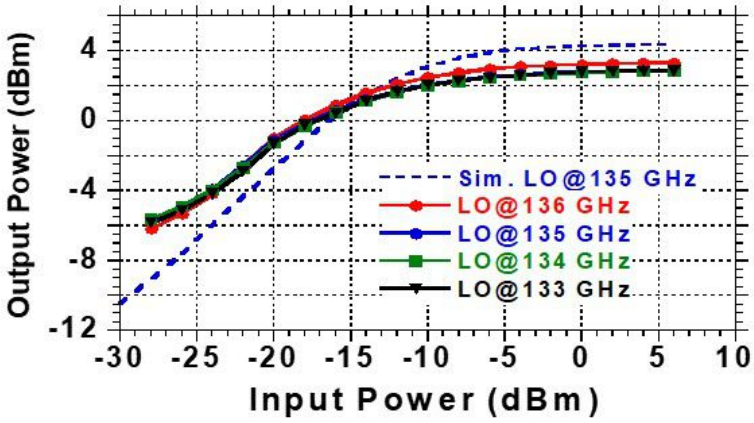


Figure 3.21: Transmitter output power as a function of input power, showing a typical 18dB gain.

Fig. 3.22 shows the transmitter output spectrum with a 141GHz LO, a -6dBm 100 MHz input to the baseband I port, and only DC bias input to the baseband Q port, this producing I-phase but not Q-phase output modulation. With correct input DC levels (Fig. 3.22), LO suppression is 23dB. The second harmonic is supressed by 24dB relative to the fundamental output signal.

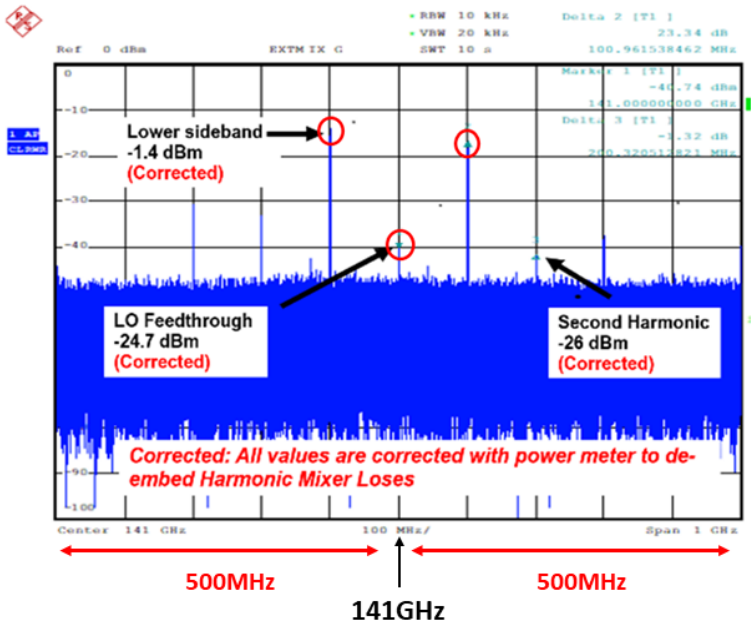


Figure 3.22: Transmitter output spectrum with center frequency 141GHz and 100MHz input signal.

3.6 Conclusion

A broadband single-channel transmitter and receiver at D-band using CMOS 22nm FDSOI are demonstrated. Conversion gain of the entire receive channel is 27dB with a 3-dB bandwidth of 20GHz. The transmitter shows conversion gain of 18dB with a saturated output power of 2.8dBm. The transmitter and receiver consumes 196mW, and 198mW respectively from a 0.8V supply, both dominated by the 137mW LO multiplier DC power consumption. The transmitter and receiver both have bandwidth sufficient for 10 GBaud transmission. A comparison to the state of the art transceivers at D-band is shown in Table 3.1. This is the first sub-mm-Wave transmit/receive chain using 22nm FDSOI with the lowest supply voltage (0.8V) and highest bandwidth at the D-band.

The transmitter and receiver chain reported in this chapter are to be used as the key building block for our multiuser massive MIMO array. However, we tested those

Table 3.1: Comparison between state-of-the-art designs for near-140GHz transceivers.

	Heller, MTT 2016 [23]	Simsek, BCICTs 2018 [7]	Yang, RFIC 2014 [24]	Lee, RFIC 2018 [25]	**This Work**
Technology	28nm CMOS	45nm SOI CMOS	40nm SOI-CMOS	40nm CMOS	22nm SOI-CMOS
Frequency (GHz)	102-128	140	155	118	135
Conversion Gain (dB)	36-38	18 Rx - Tx	23 Rx - Tx	13 Tx	27 Rx 18 Tx
3dB BW (GHz)	18 Rx	12 Rx 8 Tx$^{\$\$}$	9 Rx - Tx	14 Tx	20 Rx 8 Tx$^{\$\$}$
NF (dB)	8.4-10.4	5.5*	20*	-	8.5*
Pdc (mW)	51	125 Rx 120 Tx	345 Tx/Rx	271	198 Rx 196 Tx
Tx Psat (dBm)	NA	-2	-10	4.5	2.8
Integration	Rx	Tx/Rx	Tx/Rx	Tx	Tx/Rx

*simulated, $$ single sideband

chips using on-wafer probing. Hence a low-cost, high-performance packaging technology is required to house those transmitter and receiver chips. In the next chapter, we will present our effort in building a reliable packaging technology for our D-band massive MIMO array. We will also show the changes we employed in the CMOS chips to be compatible with the packaging solution.

Chapter 4

Packaging Technologies for mm-wave Massive MIMO Arrays

4.1 Introduction

Our end goal from this effort is to build mm-wave multiuser massive MIMO arrays for high capacity, high data rate wireless communication systems. Fig. 4.1a shows one potential application for our massive MIMO arrays with the array installed in wireless backhaul (network hub) supporting high data rate wireless links to multiple end-users; through spatial multiplexing. Fig. 4.1b shows another potential application for our module, with the MIMO array installed on a car to support autonomous driving mode. This MIMO array at the mm-wave frequency ($>$ 100GHz) has a small carrier wavelength and high directivity; hence it can support very high-resolution images (TV-like resolution to see through fog and rain). A few more potential applications are illustrated in [1].

To deploy those mm-wave massive MIMO arrays/modules, in addition to the silicon technology and the transceiver chips illustrated in chapter 3, we need low-cost, high-

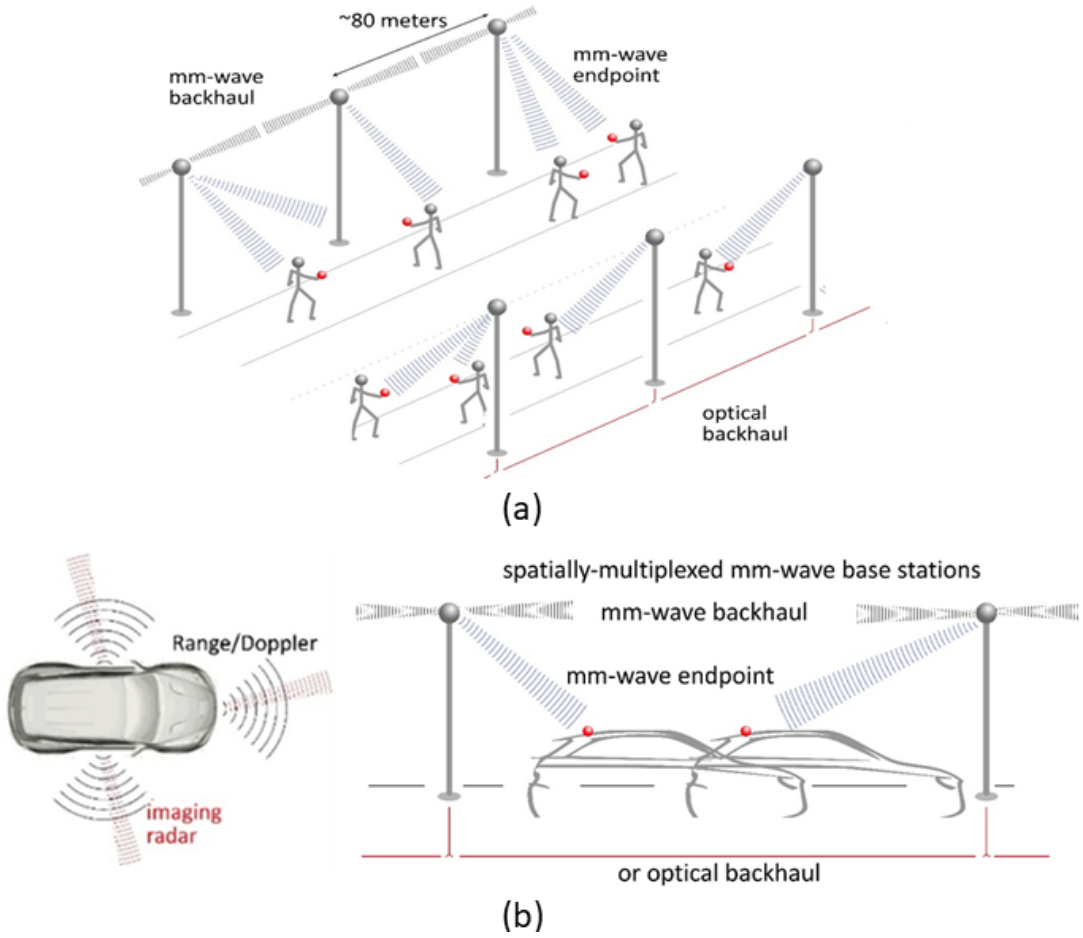


Figure 4.1: mm-wave/THz applications: (a) spatially multiplexed networks for multi--Gigabit mobile and residential/office communication and (b) THz radar and imaging systems supporting autonomous cars and driving in foul weather, with wideband links between cars and highway infrastructure to coordinate traffic. [1]

performance packaging technologies. This chapter illustrates our vision for building mm-wave massive MIMO arrays in a tileable/modular fashion. We introduce two different packaging technologies for building mm-wave arrays. In addition, we address some of the critical questions every designer will encounter while building modules and arrays for mm-wave applications; these include technology choice, packaging material, assembly challenges, and the economics for building arrays.

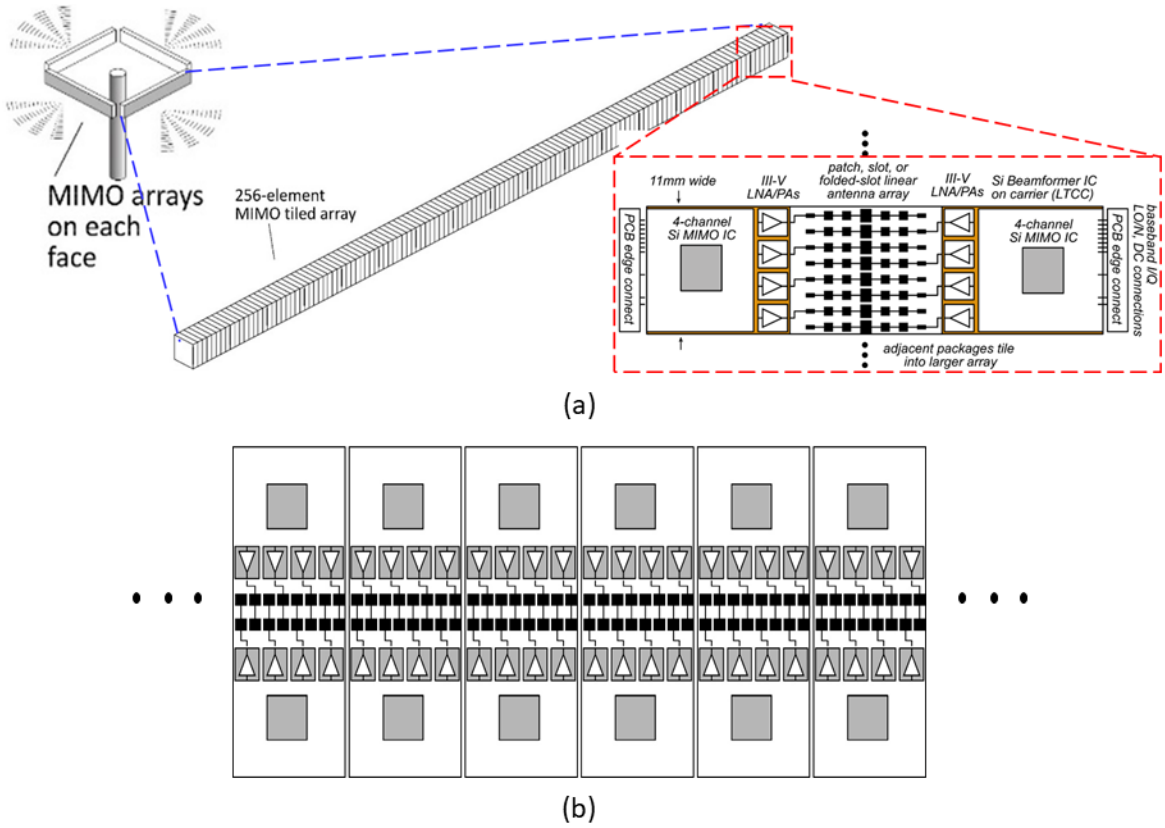


Figure 4.2: Spatially multiplexed network hub. (a) The hub has 4 faces, each a 256-element MIMO array,(b) the 256 elements are implemented by cascading 8 tiles of 8-elements . [1]

We designed a modular packaging technology implemented in a Lego-like fashion, suitable for massive linear arrays. Fig. 4.2a shows a cartoon drawing for a four-sided MIMO hub for a high-capacity network. Each side carries a linear array of 256 elements. In our design, those 256 elements are implemented in a tileable fashion, with every single tile carries eight transmitter/receiver elements. Then, we cascade those tiles, as shown in Fig. 4.2b, to deploy our massive MIMO array. This packaging architecture is economically friendly since we can increase/decrease the array size without displacing or installing new infrastructure. On top of that, it can fit a broad range of applications, where the array can be used in a single beam or multibeam phased array systems, and can be implemented on large, medium, small scale arrays.

Given that we are building a modular approach, we have a limitation on the module width to keep a constant antenna pitch. This means that we have to fit the chips routing, DC, and RF connectors in the tile width. This is a huge constraint at mm-wave frequencies, with the free-space wavelength of $\sim$ 2.2mm at 135GHz! In the next few sections we will illustrate how to build dense arrays, with uniform antenna spacing, while maintaining a wide field of view (F.O.V).

4.1.1 Challenges for mm-Wave Packaging

The advance in silicon and III-V compounds made it possible to build high-frequency transceivers for mm-wave applications, with good performance, decent power consumption, and small form factor. However, the packaging technologies are not improving at the same rate as the silicon technologies. This made it challenging for mm-wave designers to have a complete packaged solution without suffering from a significant loss in the chip to package transition. Before pursuing any packaging effort, the module designer must be aware of the five pillars of mm-wave packaging, these includes

- **IC-package Interconnect**
- **Packaging material and technology**
- **Heat removal and management**
- **Assembly challenges and consideration**
- **Packaging Economics**

In the next few sections we will illustrate the opportunities and challenges associated with each of the aforementioned packaging pillars.

4.2 IC-Package Interconnect Technologies

Few different routing technologies have been widely used to down bond the transceiver chips to the module/package, these include:

- **Wire-bond/Ball bond**:

  Wire bonding is a well-established technology to build the IC-package transition, where a thin gold, copper, or aluminum wire is routed from the chip pad to the module/PCB. The wire bond can be modeled as an inductance, and this inductance is typically negligible at the low-frequency range $<$ 5GHz. For high-frequency applications, the wire-bond impedance becomes much harder to match, and the associated insertion loss is high. Recent effort shows a W-band wire bond transition with more than 2-dB transition loss [26] [27]. Another effort at D-band shows a CMOS transmitter down bonded to a low-cost PCB and integrated with a series fed-patch antenna through wirebond routing with a 2.5dB transition loss [28] [29]. This high insertion loss at the mm-wave frequency (>2.5dB) and the difficulty in the impedance matching make wirebond transition a non-appealing technology for mm-wave applications above 100GHz, especially if another better transition technology is available.

- **C4 Flip-chip**:

  Flip-chip is a more advanced packaging and transition technology, where solder bumps are deposited on the chip pads on the wafer topside during the final stage of wafer processing. In contrast to wire-bonding, where the chip is mounted upright, in this technology, the chip is flipped over such that the chip pads are aligned with matching pads on the external circuit. The main advantage of C4 flip-chip technology is that the bump diameter is small; hence the inductance associated

with the bump is small and can be easily matched. In addition, C4 bumps can be placed with a very fine pitch of 100μm or less; this allows the placement of a large number of bumps for dense arrays. This transition technology is widely deployed in high-frequency applications up to 100GHz. Recent efforts [30] [31] show a W-band and D-band transceivers down bonded to organic interposer or high performance PCB using C4 bumps with a decent transition loss.

- **Copper Pillars**

  Flip-chip bonding using copper pillars is an advanced technology version from C4 bumps. The biggest asset in copper pillars technology is that the Cu-studs has smaller diameters and shorter heights compared to C4 bumps, hence the impedance associated with each stud is remarkably negligible, even for mm-wave applications ($>$ 100GHz). This technology is widely used for at low frequency, especially for microprocessors with very large number of pins, due to the very fine pitch of the copper pillar technology. Some assembly vendor can place cu-pillars with a very small pitch down to 30μm [32]. The draw back of this technology is that it is very hard to assemble copper pillars with small diameter, and special protective measures should be executed during the solder re-flow process to secure bonding the pillars at the exact location on the PCB/package.

- **Contact Less transition**

  This new technology fits mm-wave applications, where the signal is coupled from an on-chip antenna to an on-package antenna. This technology does not require any physical routing between the chip and package, and no special surface finish material for the package is required. However, this technology needs a very precise alignment between the chip and package. Moreover, the gap between the chip and the package should be minimal to avoid severe attenuation and transition loss.

Recent effort shows a packaged D-band transmitter using this new technology with 3-dB transition loss [33]

Fig. 4.3 show a summary of a few different IC-Package transition technologies and the pros and cons for each technology. Due to the high transition loss associated with the contactless technology, and the high cost of the micromachined waveguide interface, we sidelined those two techniques. Our module design options were either the low-cost wire bonding technology, C4 flip-chip bonding, or the Cu-stud (copper pillar technology). By comparing the three available options, the copper pillar transition was the most appealing technology for our module design, due to the high density of the copper pillars and the small insertion loss associated with those advanced copper pillars. On top of that, we get free access to GF advanced copper pillar for our CMOS transmitter and receiver chips, so we used this advanced technology to down bond our CMOS to our MIMO module.

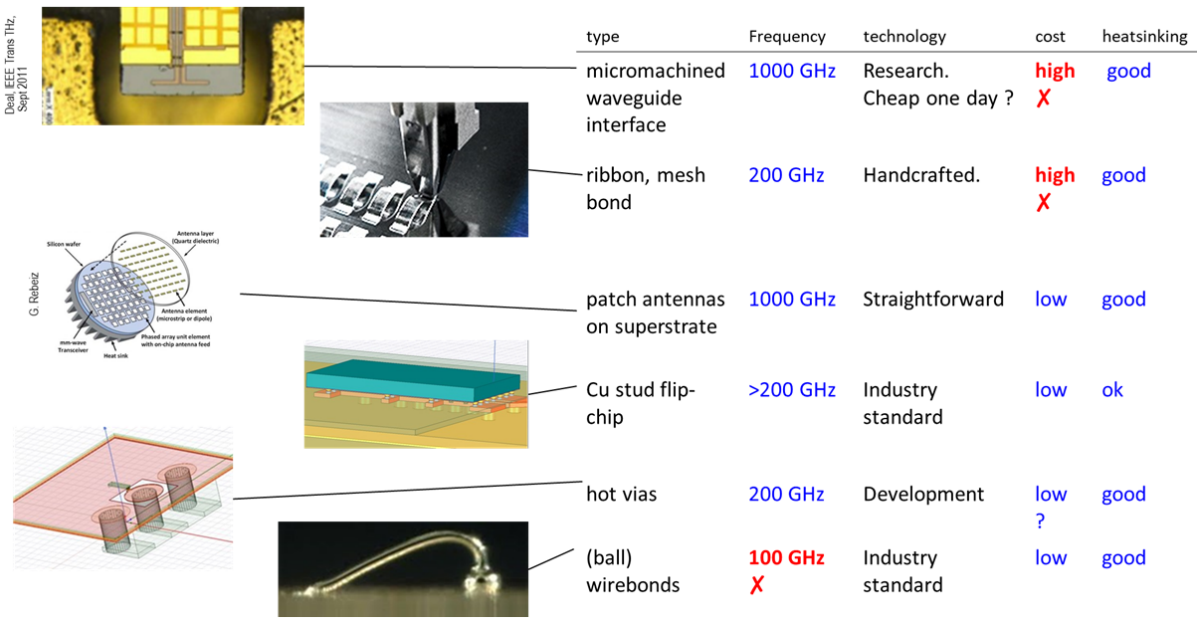


Figure 4.3: Comparison between IC-Package transition technologies for mm-wave applications

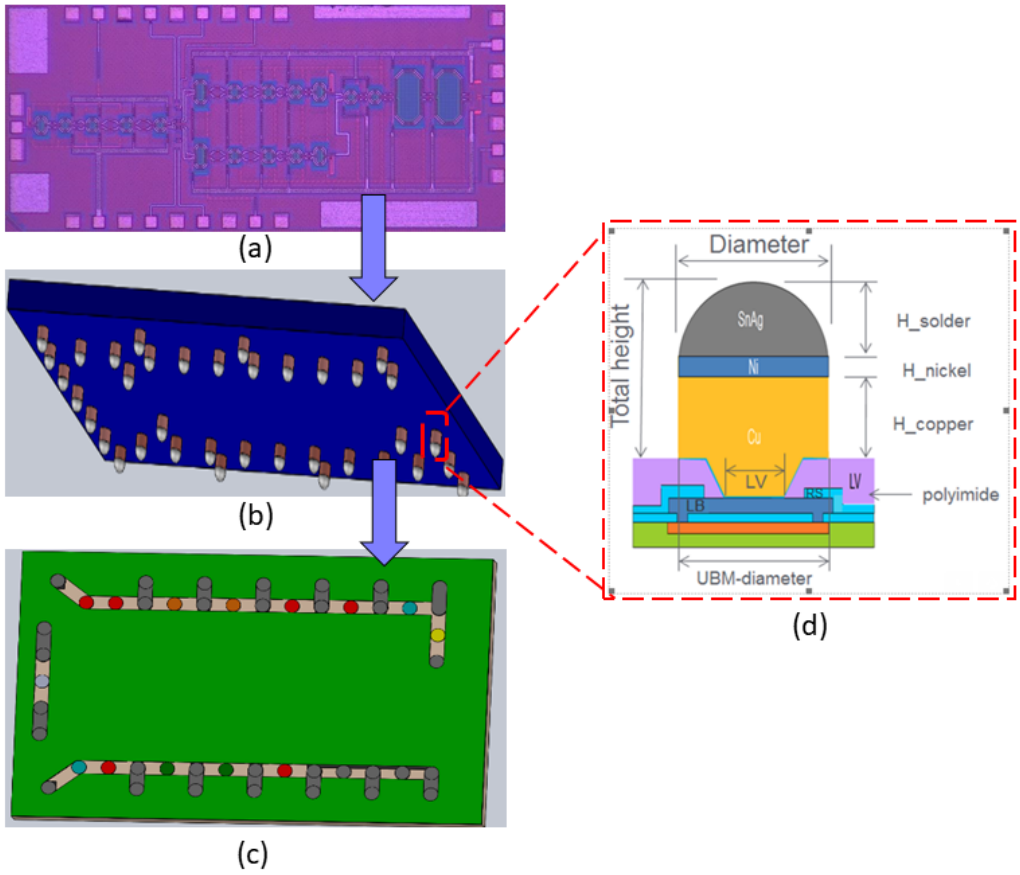


Figure 4.4: Illustrative drawing showing the procedures going the first design cycle to the second design cycle (a) chip with pads for on wafer testing (b) cartoon drawing for transmitter chips with GF copper pillars (c) PCB/ceramic carrier with solder mask opening at copper pillar locations (d) copper pillar structure

4.2.1 D-band Transmitter and Receiver Chips with GF Copper Pillars

The transmitter and receiver chips reported in chapter 3 were designed to be tested using on-wafer probing. We went through a second design cycle to make the chips compatible with the packaging technology and to add GF advanced copper pillar, with the structure shown in Fig .4.4d. In contrast to the first design cycle, both the transmitter and receiver chips will be flipped on a package instead of being placed in an upright position for on-wafer testing, as shown in Fig. 4.4

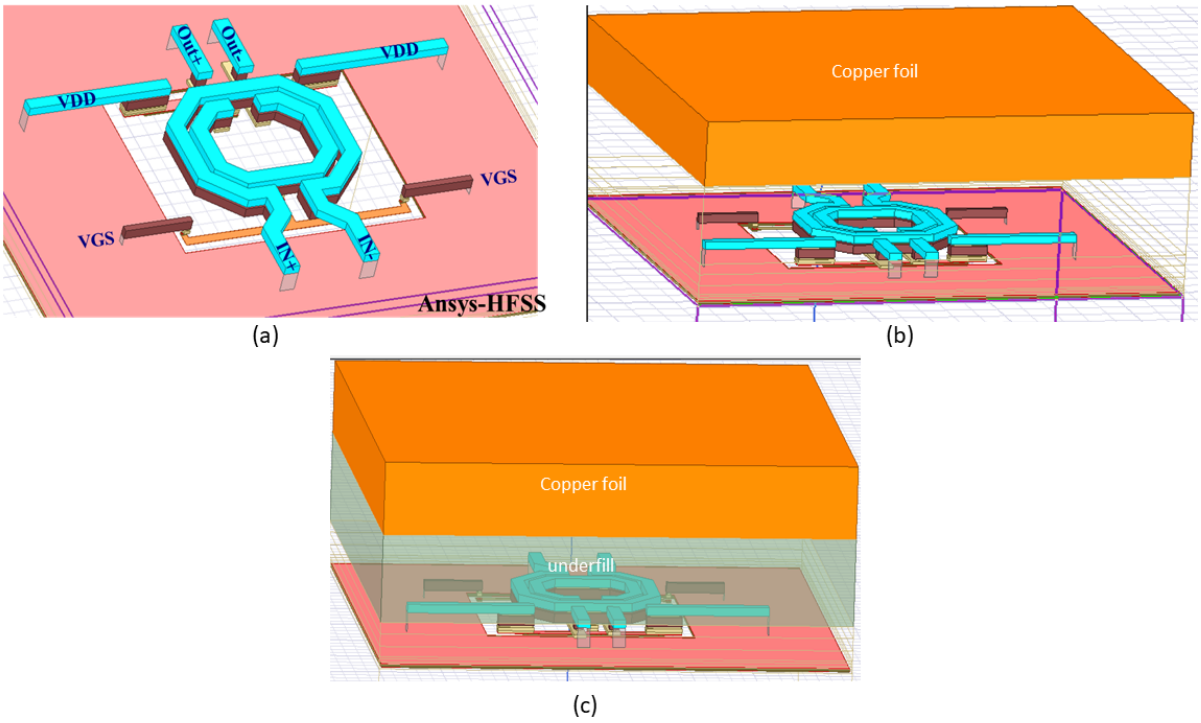


Figure 4.5: EM simulation using Ansys HFSS for a 135GHz transformer (a) while being open up to the air, (2) with a copper foil at 30μm distance, and (3) with copper foil at 30μm distance and with under-fill material in-between the transformer and the package

In the first generation of the transmitter and receiver chips, all the passive components were facing the air. However, in the second design cycle, all the passive structures will face either a copper foil or another dielectric material with different permittivity compared to air. To assess the required design effort from the first to the second design cycles, we picked some of the passive components and evaluated their performance in three different scenarios; (1) while being open up to the air, (2) with a copper foil at 30μm distance (equivalent to the copper pillar height), and (3) with copper foil at 30μm distance and with underfill material between the passive structure and the package. Fig. 4.5 shows an example for a 135GHz transformer simulated in the three scenarios mentioned above. The EM simulation results (Fig.4.6) show a minimal deviation in the transformer parameters (L, R, Q, K). The maximum deviation in the transformer's quality factor is $< 8\%$ and

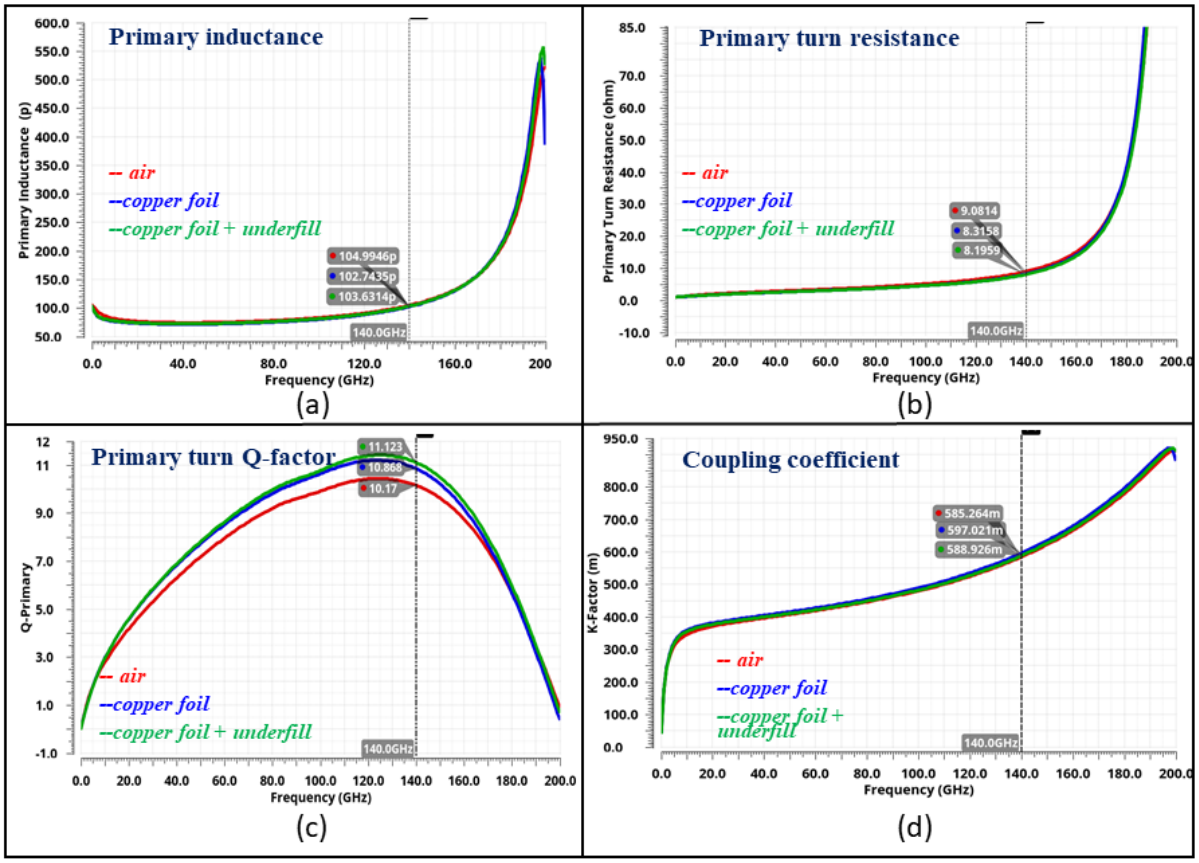


Figure 4.6: EM simulation results for a 135GHz inter-stage matching transformer (a) transformer's primary inductance (b) Primary turn resistance (c) primary turn quality factor (d) K-coupling coefficient

3% for the inductance value. Our understanding is that the minimal variation in the transformer parameters between the three scenarios is due to the fact that the spacing between the transformer turns (primary and secondary turns) is much smaller than the spacing between the transformer and the copper foil, in addition to the small transformer size at 135GHz (with an average transformer diameter of $< 40\mu$m).

We repeated the EM simulation for the passive structures in the first stage of the frequency multiplier, with a center frequency of 45GHz. We found that the deviation in the transformer parameter increases, such that the deviation in the transformer's quality factor changes by 18% and the inductance change by 14%. However, since the

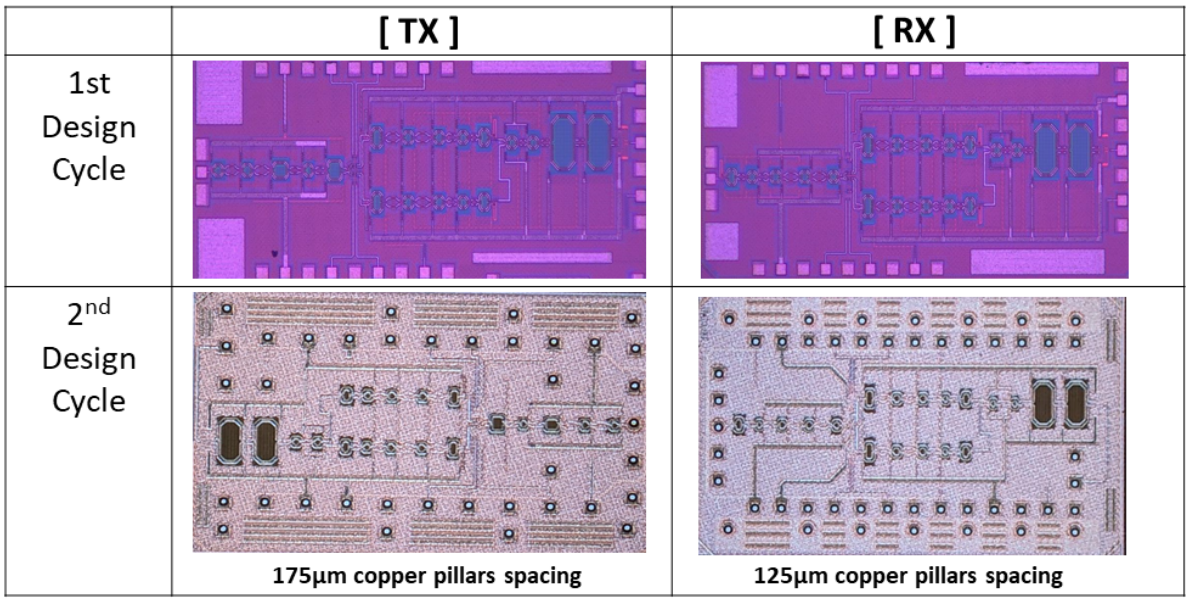


Figure 4.7: adding copper pillar to both transmitter and receiver chips

transmitter and receiver chips have a very broad bandwidth of 20GHz, we kept all the passive components the same. The only change from the first design cycle to the second design cycle was replacing the on-chip pads with copper pillar pads and adding ESD protection circuits. Fig. 4.7 shows the transmitter and receiver chips with copper pillars. The pillar pitch on the transmitter chip is 175 μm and 125 μm for the receiver chip. The tight spacing between the copper pillars imposes a very stringent requirement on the assembly process, and this will be covered in detail in this chapter and chapter 5.

4.3 Packaging Material and Technology

For low-frequency applications, low-cost PCB using FR4 material was the dominant packaging technology to build modules and arrays. However, for high frequency and mm-Wave applications, FR4 material has a high permittivity ε_r and high loss tangent σ, causing high trace impedance and significant loss in routing signals, making Fr4 material completely undesirable material for mm-wave applications. For our module design, we need packaging technology to host both the transceiver chips and a high-performance, high-efficiency antenna. In addition, we need to build a dense array in a tileable fashion; this means that we need to fit all the DC, IQ, LO signals connectors and routing, for all channels, in a small footprint and keep a uniform antenna spacing between the MIMO channels. In this endeavor, there are two different packaging approaches; either to build the module on a high-performance laminate material with low permittivity ε_r or to use a ceramic carrier or organic carriers with relatively low ε_r as an interposer.

In our module design efforts, we pursued in parallel the two aforementioned packaging approaches, where we built a MIMO tile on high-performance laminate material and on a Kyocera low temperature co-fired ceramic (LTCC) interposer [34]. This chapter will focus on building MIMO arrays in tileable fashion on high-performance laminate materials, and we will cover the MIMO tile on the ceramic interposer in Chapter 5. For each approach, we will illustrate the procedures for building modules of single-channel and multi-channel, chip-antenna interface design, the assembly challenges, heat management, and how to get the heat out of the module. Then we will conclude by illustrating array scaling economics.

4.4 A Fully Packaged D-Band MIMO Array on a High-Performance Laminate Material

Toward building a fully packaged MIMO tile, a high-performance laminate material with low ε_r and low σ is required. In addition, the material should be durable and compatible with the CMOS transceivers copper pillars. We did a comparative study between a broad range of high-performance laminate materials (Table. 4.1). We find that the optimum choice for our application is Isola Astra MT77 since this material has a good permittivity, low loss tangent, and is compatible with the copper pillar technology. Note that Tachonic TSM-DS3 has the lowest loss tangent, but this is a Teflon-based material and has a very soft surface; hence it will not be compatible with copper studs, and the module surface can be easily deformed during the assembly process.

Table 4.1: Comparison between high-performance laminate materials.

Material	CTE (X/Y) ppm/^{0}C	Young's Modulus	CTE (Z) ppm/^{0}C	Decomp by Temp (td)	ε_r	σ
Isola Astra-MT77	12∼22	2784 KSI (lengthwise) 2526 KSI (crosswise)	50-70	360^{0}C	3	0.0017
Isola I_Tera MT	12∼22	3060 KSI (lengthwise) 2784 KSI (crosswise)	50	360^{0}C	3.45	0.0031
Isola Tachyon-G100	15	2551 KSI (lengthwise) 2417 KSI (crosswise)	45	360^{0}C	3.02	0.0021
Taconic TSM-DS3	10 (X-dir) 16 (Y-dir)	983 KSI (lengthwise) 973 KSI (crosswise)	23	526^{0}C	3	0.0011
Megtron-6	14∼16	NA	45	410^{0}C	3.63	0.004

4.4.1 PCB Stack Build-up

Fig. 4.8 shows the stack build-up of the 1-D MIMO array on a high-performance laminate material. The PCB has 3-dielectric layers of Isola Asta MT77 and four metal layers. The CMOS chip is flipped on the PCB top layer using GF advanced copper pillars. The connectors for the transmitter/receiver IQ signals, LO signal, and DC supplies are surface mounted to the PCB top metal layer. The top metal layer is also used to route the transmitter/receiver IQ and LO signals, and the third metal layer is used to route the DC bias and supply voltage. The second and fourth metal layers (L2 and L4) are used as ground planes. Eight elements series-fed patch antenna is also routed and designed on the PCB top metal layer (L1). We picked a 4-mils top dielectric layer to minimize the diameter of the via from L1 to L2 (via diameter is an aspect ratio for the dielectric thickness), such that we can place a sufficient number of vias in a small footprint. This small via diameter is critical to maximize the routing density and to build a dense array in a small footprint. The fourth metal layer (L4) has a dual function, where we used it as a ground plane and to take the heat out of the module and dispose of the heat to the metal carrier attached below the module.

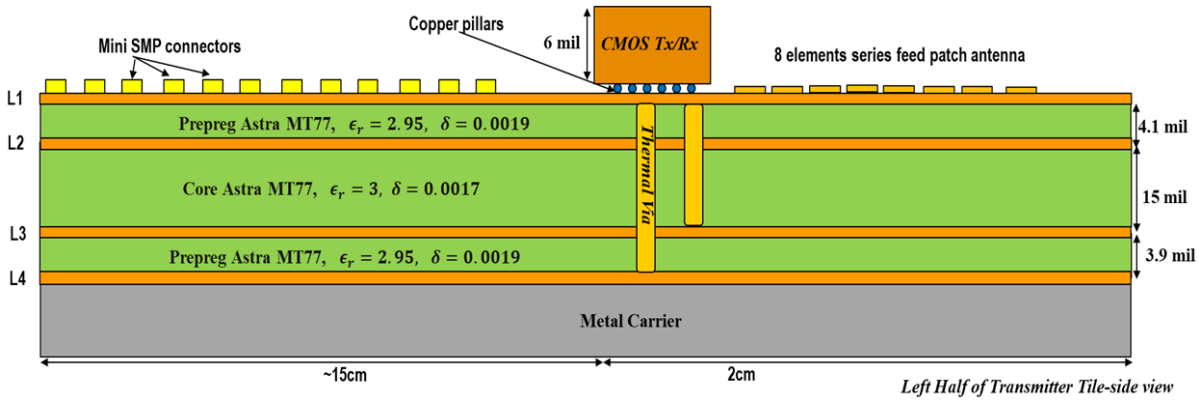


Figure 4.8: Stack build up for MIMO array on high-performance laminate

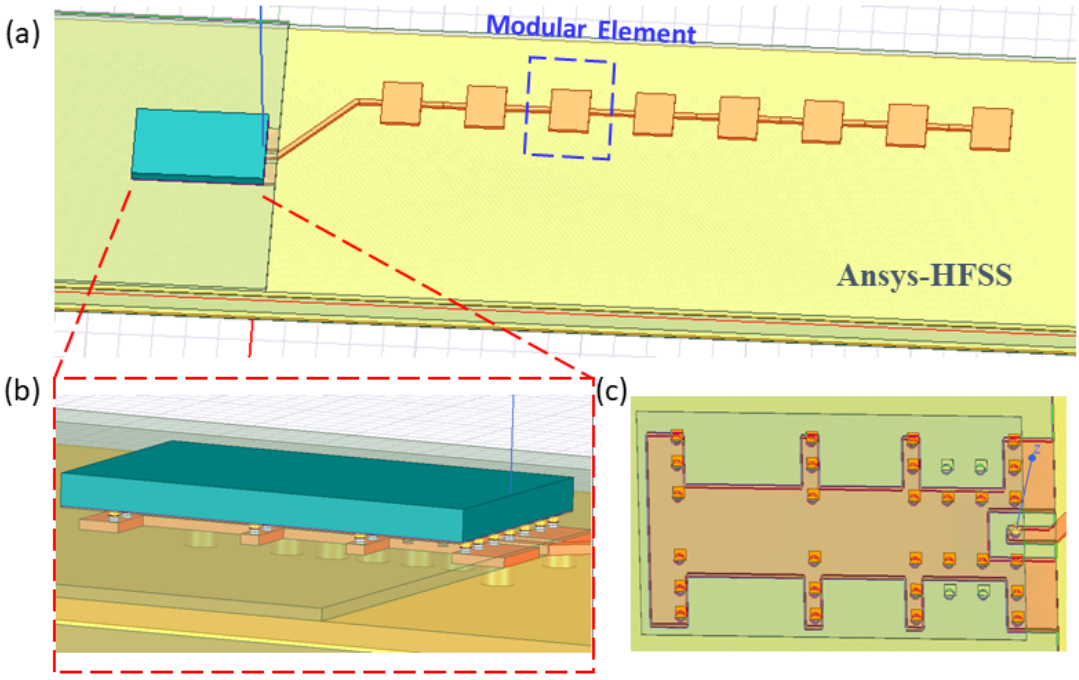


Figure 4.9: 8-element series-fed microstrip patch antenna (a) CMOS/antenna co-design and modeling using Ansys HFSS (b) EM model of CMOS chip interface plus copper pillars (c) CMOS chip ground plane structure and model on Ansys

4.4.2 8-Elements Series-Fed Patch Antenna

An 8-elements series-fed patch antenna design using the concept illustrated in [35] and modeled using Ansys HFSS (Fig. 4.9). We designed the antenna in a modular fashion, where each modular element (Fig. 4.9a) length and width are defined based on the equations illustrated in [36]. The patches are connected in series and matched by a microstrip line. We used the minimum width for this TL (76μm) to minimize the non-useful radiations from this transmission line. In addition, the length of the TL should be one λ such that the radiation patterns from all the series-connected patches are added constructively. Otherwise, the beam could squint. It is preferable to do impedance matching between the elements. For infinite series fed patches, each element has the same load impedance, which is the input impedance for the following element. However, the last one does not have the same load impedance for a limited number of elements.

We can design a load termination by adding a dummy element after selecting it's width and length to give the required termination. However, we did not see a huge impact, so we did not include a dummy element after the last patch.

The antenna input impedance was matched to the CMOS chip 50Ω output impedance using a $\lambda/4$ microstrip line. The copper pillars at the output of the CMOS chip is modeled as part of the impedance matching network (Fig. 4.9b). To guarantee an accurate EM modeling for the CMOS/antenna co-design we precisely modeled the ground plane below the CMOS chip, as shown in Fig. 4.9c. The simulated antenna realized gain is 14dB (Fig. 4.10a) and the simulated S11 is better than -8dB from 125GHz to 140GHz (Fig. 4.10b) with simulated 3-dB bandwidth of 7 GHz (Fig. 4.10c)

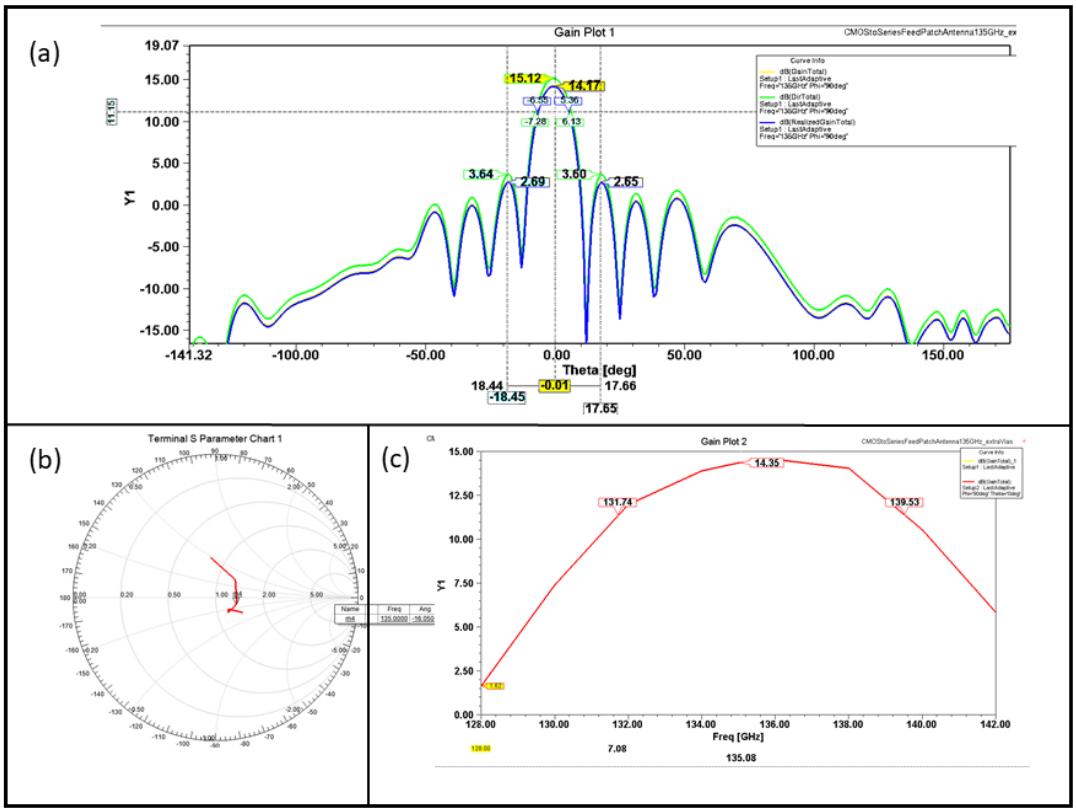


Figure 4.10: 8-elements series-fed patch antenna simulation (a) realized gain in the broadside direction (b) simulated S11 on smith chart (c) Gain Vs Frequency

4.4.3 MIMO 1-D Tile Frontend Development

We used the stack shown in Fig. 4.8 and developed a single transmitter channel (Fig. 4.11a), where the IQ and LO signals are routed on the top metal layer, and the transmitter output is connected to an 8-elements series-fed patch antenna. Due to the coarse lithographic resolution of the PCB approach with a minimum trace width/space of 3mil/3mil, a single channel transmitter fits in a 2λ spacing. To build the 8-channels tile, we need to minimize the antenna spacing to maximize the field of view (F.O.V) without grating lobes. If we keep cascading channels next to each other, a tile of 8-channel will fit in 16λ spacing, and the minimum antenna pitch will be 2λ. This will minimize the array F.O.V and will not be area efficient. In our module design, we managed to fit two transmitter channels in 2λ spacing, as shown in Fig. 4.11b. Then we keep cascading the channels as shown in Fig. 4.11c to build the tile of 8-elements. This approach helped us to shrink the tile width to 8λ and at the same time improve the array F.O.V by keeping the antenna spacing equals to one λ.

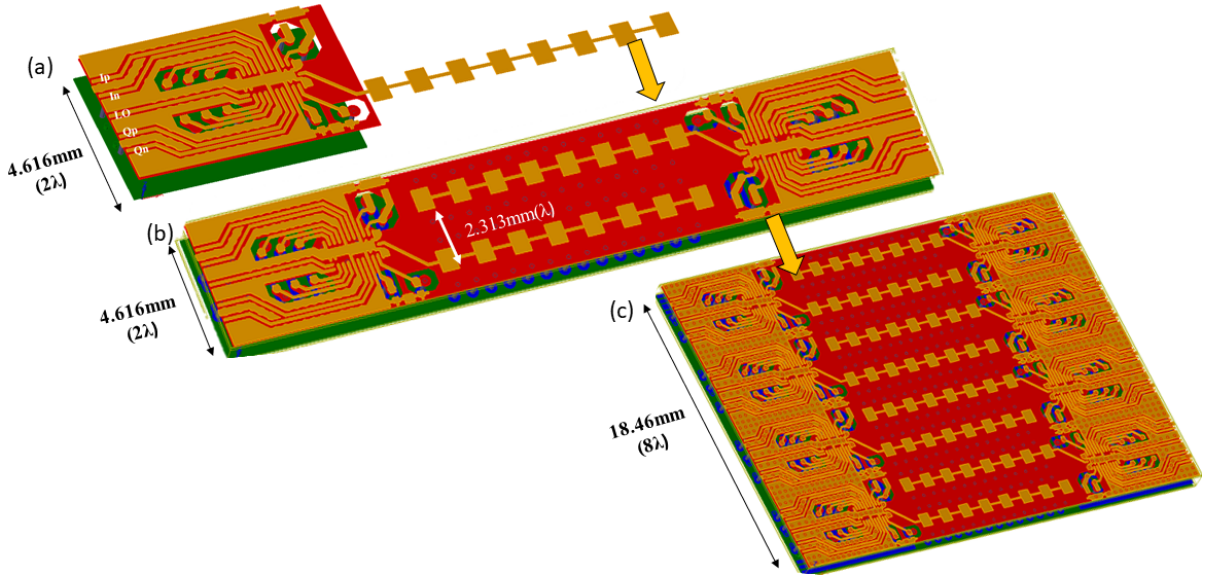


Figure 4.11: MIMO tile design on Isola Astra MT77 (a) Single Tx/Rx channel footprint (b) Two channels designed to fit in 2λ spacing (c) a tile of 8-elements

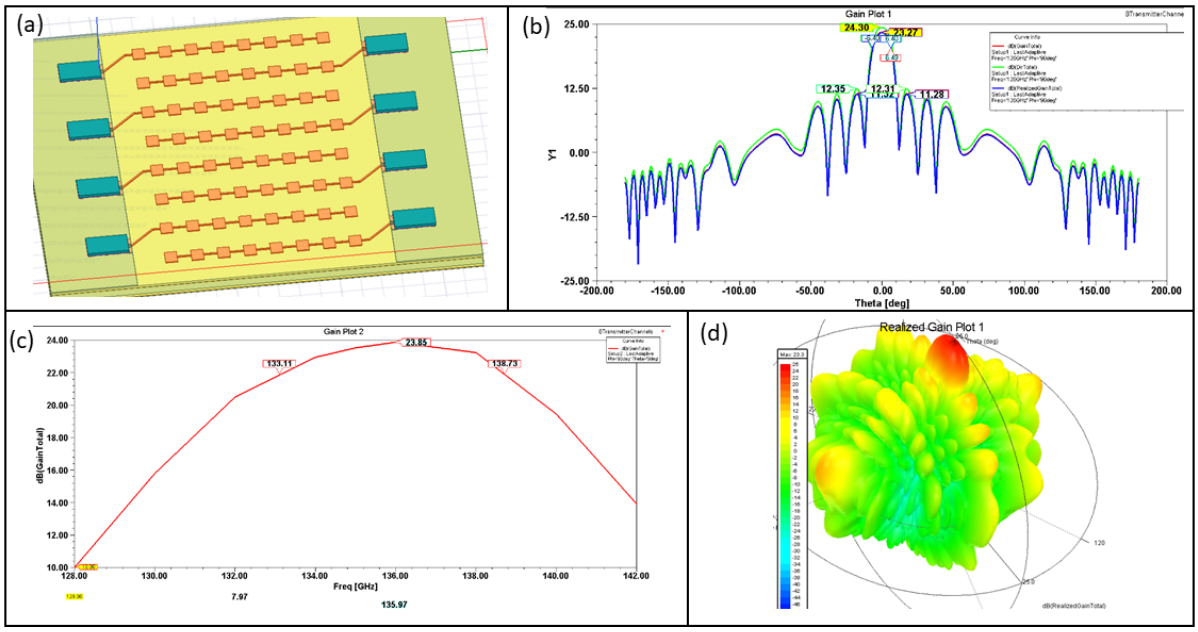


Figure 4.12: Antenna array simulation using Ansys HFSS (a) 8x8 antenna array test bench (b) simulated array directivity and realized gain (c) antenna array simulated 3-dB bandwidth (d) 3D drawing for the array's radiation pattern

We simulated the 8x8 antenna array using Ansys HFSS, including the CMOS chip transitions (Fig. 4.12a). The array has 24.3dB directivity, 23dB realized gain (Fig. 4.12b), and 7GHz 3-dB bandwidth. Thanks to the low permittivity and low loss tangent of the Isola Astra MT77 material, the array shows an 80% radiation efficiency in simulation.

4.4.4 MIMO 1-D Tile Backend Development

Fig. 4.13 shows the core of the 1-D MIMO tile with eight transmitter or receiver channels, 4-channels on the right, and 4-channels on the left. Each Tx/Rx channel is connected to an 8-elements series-fed patch antenna. We designed this tile to be part of the massive MIMO array. Hence, we need the frontend to be compatible with a broad range of applications, such that the Tile frontend can be integrated with FPGA evaluation kits, Arbitrary wave generators, or any custom-designed digital backend. In this endeavor we designed the module backend on the same PCB, and used the broadband Rosenberger

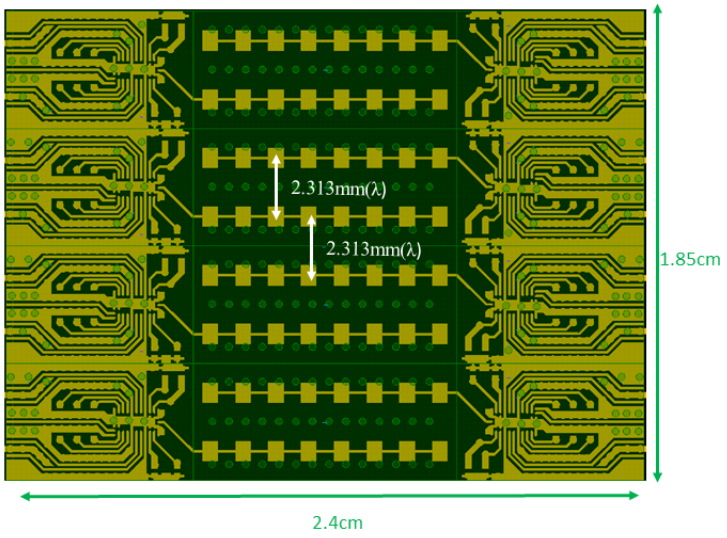


Figure 4.13: 1-D MIMO tile frontend

connectors for all the I,Q and LO signals. The module backend has the same exact width as the tile frontend . All the IQ signals are routed on the top metal layer in a Coplaner waveguide (CPW) structure to minimize the coupling between different IQ signals. The LO signal is implemented on the third metal layer and a single input LO signal coming from a Rosenberger connector is split into 4 signals using corporate splitter.

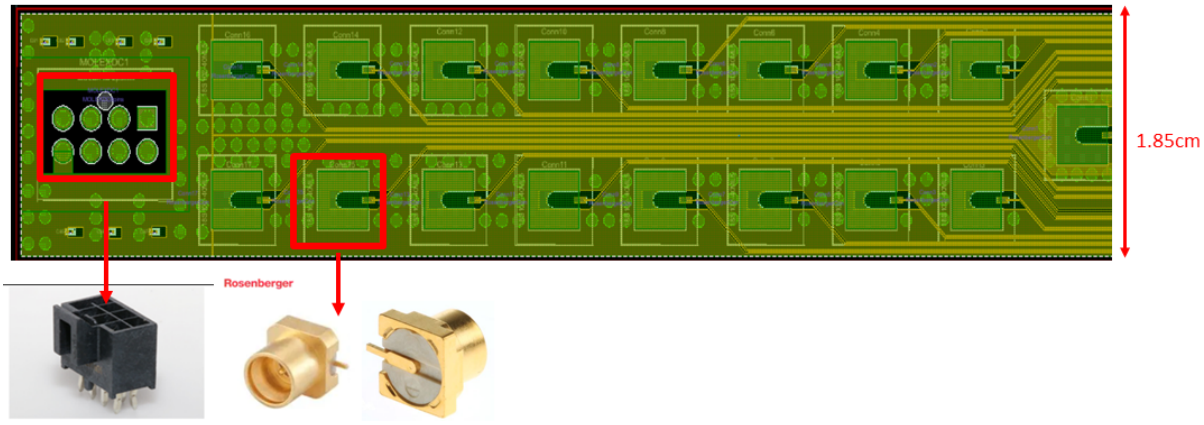


Figure 4.14: 1-D MIMO tile backend

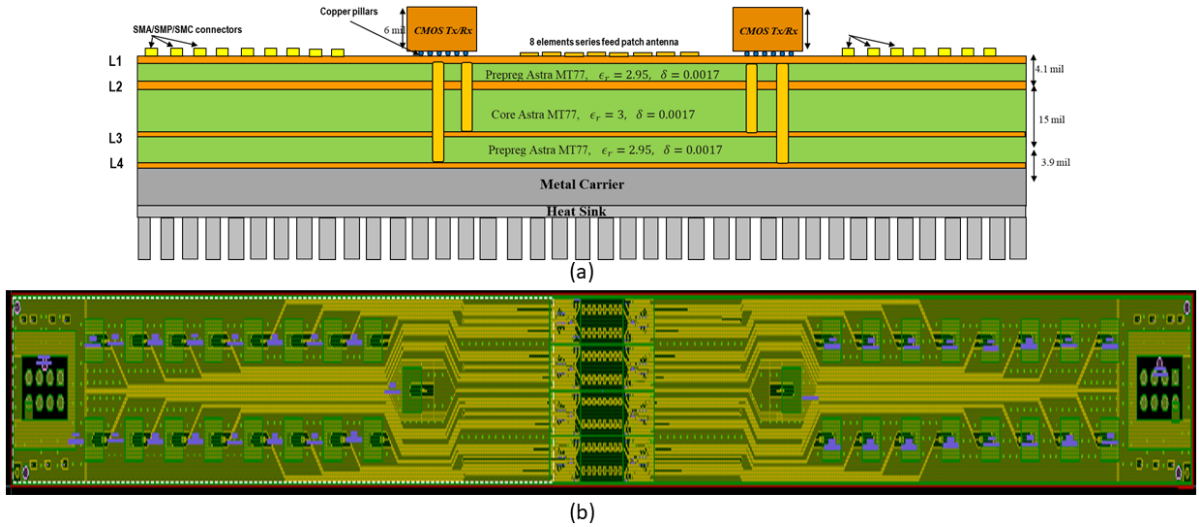


Figure 4.15: Integrated 1D MIMO Tile on High-performance Laminate (a) Module cartoon drawing for the side-view (b) PCB layout with 4-channels on the right and 4-channels on the left

4.4.5 Integrated 1-D MIMO Tile on Astra MT77 High-performance Laminate

The integrated MIMO module on PCB is shown in Fig. 4.15 with 8-transmitter or receiver channels. There are four channels on the right and four channels on the left. Each channel has a differential I, Q signals are driven using Rosenberger (18S102) connectors. The DC bias and supply voltage are driven using Molex's low-cost DC connector. The integrated module is down bonded on a metal carrier; then, a heat sink takes the heat out of the module. The metal carrier is also a stiffener to improve the mechanical stability of the module and make it more resistant to any external force

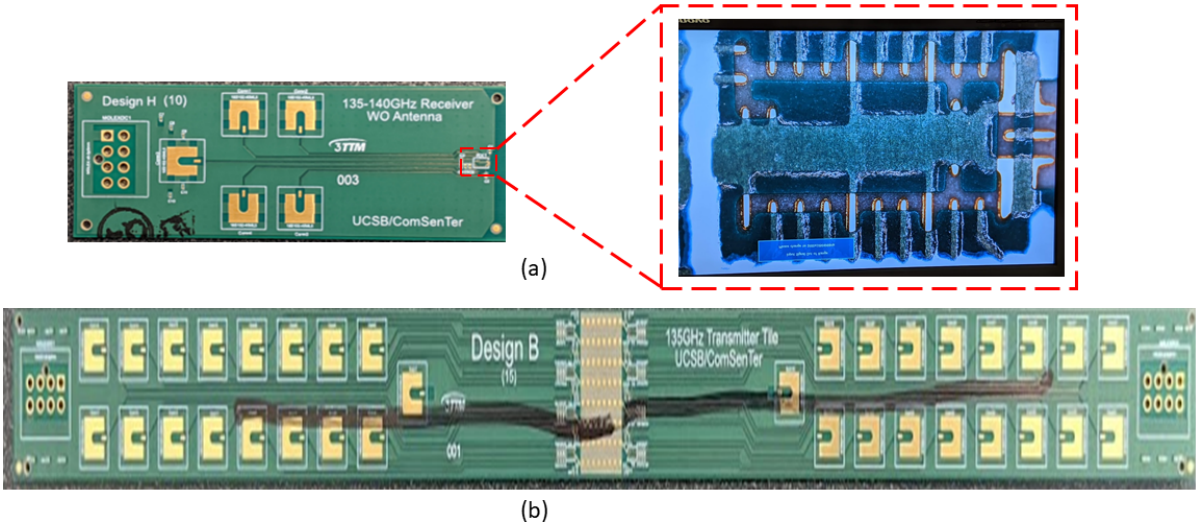


Figure 4.16: Fabricated PCB (a) test structure for a single transmitter channel (b) MIMO module/tile of 8-channels

4.4.6 Assembly challenges with the MIMO tile on High-Performance PCB

We fabricated the MIMO tile on a high-performance laminate at a TTM PCB manufacturing facility. Then, we sent the module and some test structures (Fig. 4.16) for another assembly house to down bonded the CMOS chips on the tile. We encountered an unexpected failure with this module, and all the assembly houses failed to down-bond the CMOS chips on either the module or the test structure. This mainly happened because of the following reasons:

- **PCB traces were over-etched:** The typical value for PCB trace width/space is 5/5mil. Once we switch to a more advanced lithographic resolution, as we did here by pursuing a design with trace width/space of 3/3mils, most PCB manufacturing facilities suffer from poor quality control, and the final trace width is typically over-etched. The majority of PCB manufacturing facilities are not yet ready to pursue a satisfactory lithographic resolution as small as 3/3mil or less. Then will be a

bottleneck in building dense arrays for mm-wave applications.

- **Solder mask openings were two times larger than the copper pillar diameter:** To secure landing the copper pillars at the designated location on the PCB, we need a solder mask opening on the PCB with a diameter one-to-one with the copper pillar diameter. However, since we are using a very advanced copper pillars technology with 50μm diameter, this was impossible from the PCB manufacturing perspective to have a solder mask opening that small and the minimum solder mask opening on our PCB was 150 μm.

- **The solder dome of the copper pillar wicks away during the solder reflow process:** Due to the wide solder mask opening on the PCB, nothing controls the solder dome from wicking away during the solder reflow process. During the assembly process, the solder dome is entirely absorbed by the PCB copper or move along the trace; this leads to either an open circuit between the chip and the PCB or the copper pillar land on a wrong destination

4.5 Conclusion

In this chapter, we illustrated our vision toward building mm-wave Massive MIMO arrays in a tileable fashion. We showed some potential applications for our massive MIMO array. Then, we introduced some critical aspects in building modules and packaged solutions for mm-wave applications. We illustrated some IC-package transition technologies and explained the pros and cons of each technology. Then, we showed in detail the procedure for building our MIMO array in a tileable fashion on a high-performance laminate. Finally, we concluded by illustrating the assembly challenges in building the integrated array using PCB approach. Until PCB manufacturers develop a reliable PCB fabrication

technology with a fine lithographic resolution ($\leq$ 3mil), building dense mm-wave arrays (>100GHz) with uniform antenna spacing (λ /2) will not be available using the PCB manufacturing technology.

Chapter 5

Fully Packaged D-Band Tx/Rx Multiuser MIMO Tiles using LTCC Carriers

5.1 Introduction

In chapter 4 we illustrated two different approaches in building massive MIMO arrays in a tileable fashion; this includes building the array on either a high-performance laminate (Chapter 4.4) or on a low temperature co-fired ceramic carrier (LTCC Interposer). This chapter focuses on building a tileable mm-wave multiuser massive MIMO array on Kyocera ceramic interposer. We present two transmitter tiles, one for short-range communications using CMOS-only transmitters. Another tile for long-range communication using a heterogeneously integrated CMOS transmitter with high output power InP Power amplifiers [37] [38] [39]. We also present a fully integrated CMOS-based receiver tile on an LTCC carrier. This chapter explains in detail the procedures for building a single channel transmitter or receiver on a ceramic interposer, then illustrates how to build a tile of 8-elements and how to build massive MIMO arrays using those tiles.

5.2 Low Power Single Channel D-band Transmitter on LTCC Carrier

In this section we present a single channel direct conversion CMOS transmitter flip-chip bonded on a low-temperature-cofired ceramic (LTCC) interposer using 50μm diameter copper pillars (section 4.2.1), thereby connecting to an 8-element series-fed patch antenna on the carrier (Fig. 5.1). The transmitter module has 13dBm saturated EIRP, and 6-GHz 3-dB modulation bandwidth. Measurements of the transmitter's modulation constellations shows that it can support 16Gbps using 16QAM and 15Gbps using 64-QAM.

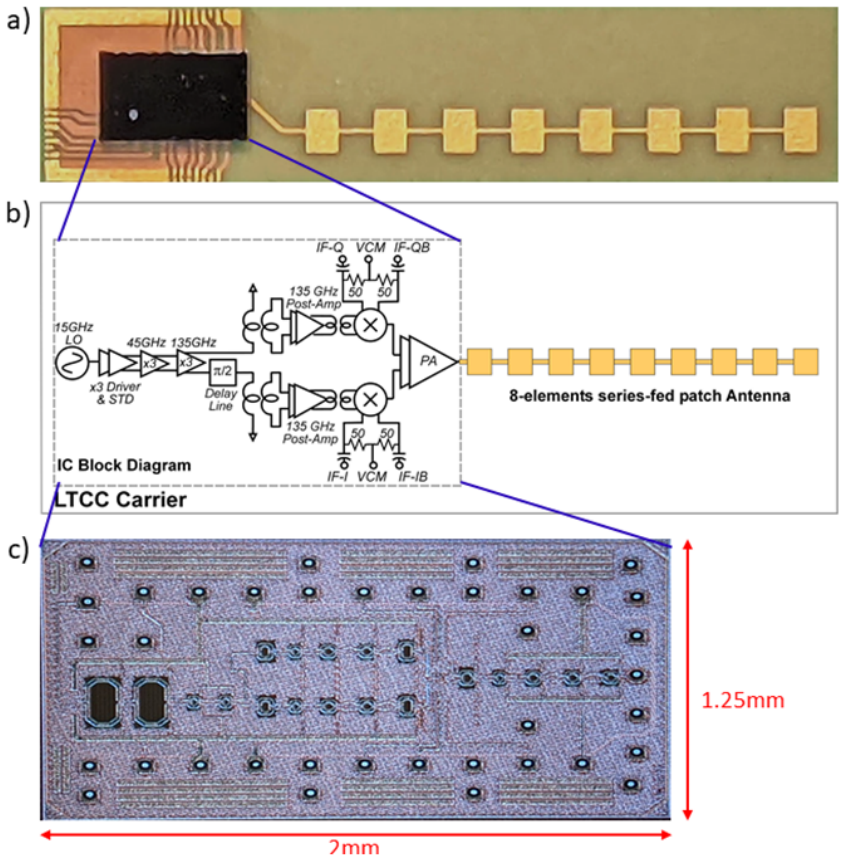


Figure 5.1: (a) D-band integrated transmitter module (b) transmitter architecture, and (c) micrograph of the IC with copper pillars with a die area of 1.25mm× 2mm.

5.2.1 Ceramic Carrier Design

The ceramic carrier (Fig. 5.2) has 3 dielectric layers of Kyocera GL771 (ε_r=5.2 , loss tangent δ=0.003) and has 4 metal layers. The top metal layer (ME3) routes the transmitter I/Q and LO signals and forms the series-fed patch antenna. The 2nd lowest metal layer (ME1) routes the supply and bias voltages. ME2 and ME0 are used as ground planes. A ceramic coat, with 75μm openings at the copper pillar locations, was added to prevent the solder dome on the copper pillar from excessively wicking away during solder bonding. Nevertheless, given the minimum 75μm ceramic coat openings, for reliable bonding it was necessary to add additional solder on pad (SOP) to the ceramic carrier.

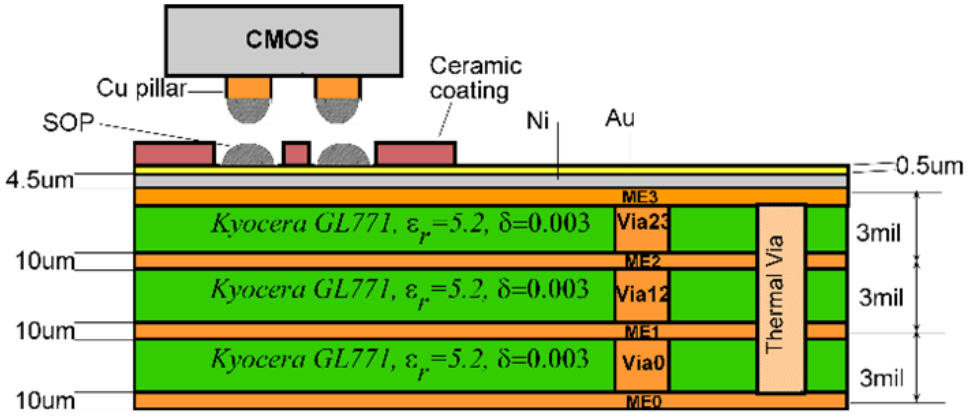


Figure 5.2: Ceramic interposer layer stack.

5.2.2 IC-Package Transition Loss

Fig. 5.3a shows the copper stud flip-chip transition. The CPW center conductor on the LTCC carrier is 50μm width, while the ground-ground separation is 150μm. The CPW line section is 220μm length. Fig. 5.3b shows the simulated performance of the chip transition in Ansys HFSS, which shows a simulated 1.15dB insertion loss and -7.1dB return loss at 135 GHz.

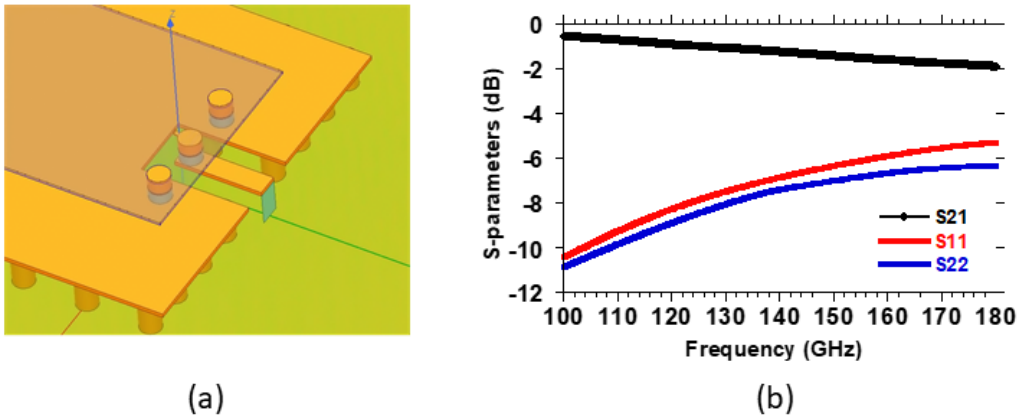


Figure 5.3: (a) Cu stud flip-chip transition, (b) Simulated performance of the chip transition (copper pillar plus CPW transition)

To characterize the transition loss of the flip-chip interface, a CMOS transmitter was flip chip bonded to an LTCC carrier (Fig. 5.4a), with the transmitter saturated output power (1.95dBm) measured with a probe contacting the LTCC carrier. This measurement was then compared to the transmitter saturated output power (2.8dBm) measured by directly probing an IC (Fig. 3.21) of identical design, operating at the same bias condition. The measured 0.85dB difference is close to the simulated 1.15dB simulated transition loss, shown in Fig. 5.3b, for the combined attenuation of the copper pillar interface and 220μm of the CPW on the LTCC carrier.

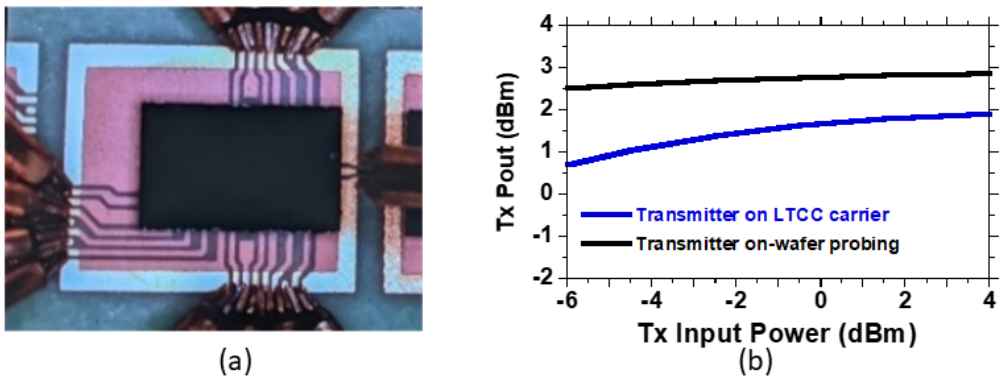


Figure 5.4: (a) Flip-chip transmitter mounted on carrier with wafer probe connection (b), and measured Pin-Pout characteristics of the mounted transmitter compared to that of an otherwise identical transmitter tested by on-wafer probing.

5.2.3 Series-Fed Patch Antenna

An 8-elements series-fed microstrip patch antenna [40] was designed on the LTCC carrier and simulated using Ansys HFSS, with antenna dimensions shown in Fig. 5.5a. A quarter-wave transformer matches the antenna to the transmitter output 50Ω, where the matching network includes the 30μm height, 50μm diameter copper pillar on the CMOS side.

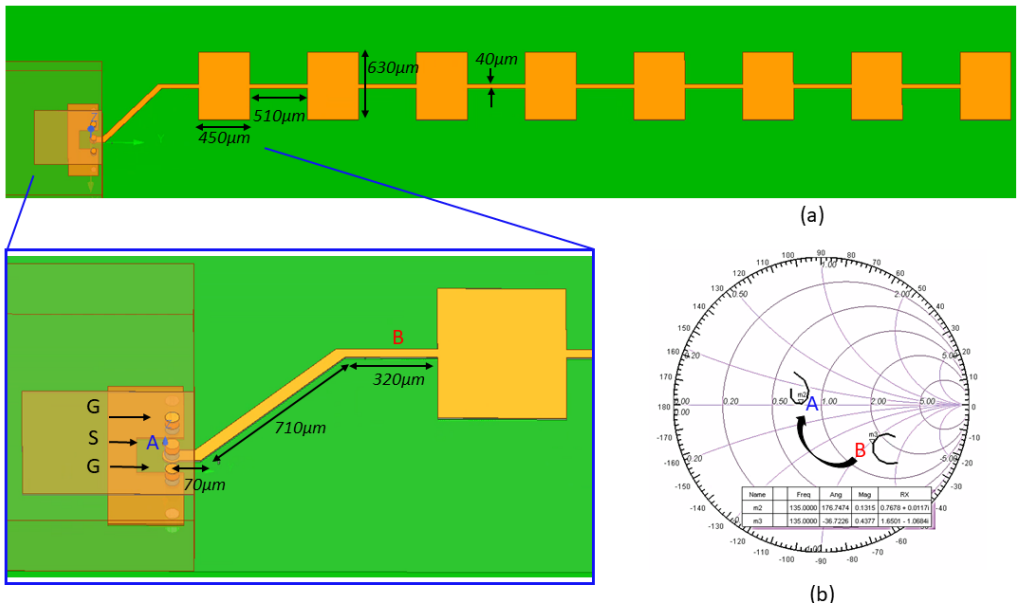


Figure 5.5: Series-fed patch antenna (a) simulated antenna structure (b)smith chart of antenna matching network.

A test structure of this 8-elements series fed-patch antenna was tested using the setup shown in Fig. 5.6. The antenna input was driven using Virginia diode VNAx6.5 source, with a single input tone from 130GHz to 140GHz. A D-band standard gain horn antenna captured the radiated signal at a 15cm distance. The horn antenna is connected to an OML D-band harmonic mixer, and the output of the mixer is connected to a spectrum analyzer.

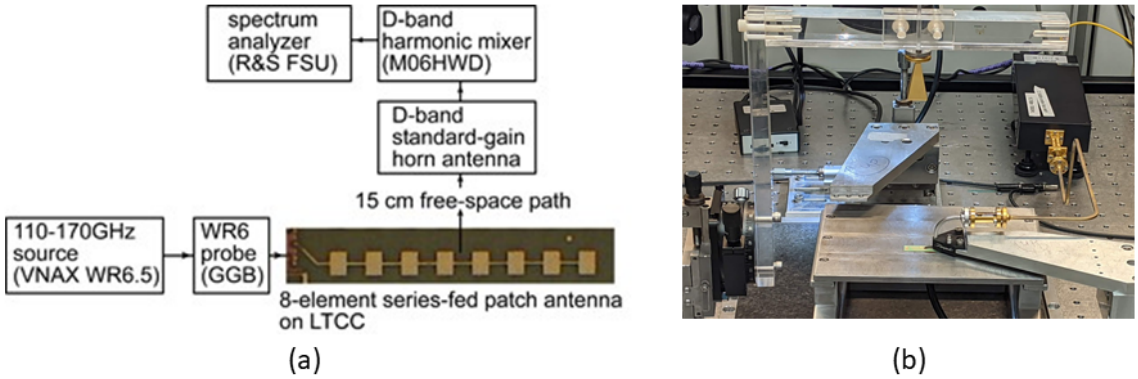


Figure 5.6: Series-fed patch antenna measurement setup (a) schematic of the testing setup (b) actual measurement setup

Fig. 5.7a shows measured antenna gain of 11 dB and 3-dB bandwidth of 6GHz. The measured antenna gain is 1dB below simulation, while the measured return loss (S11) is 12dB. Fig. 5.7b shows the measured antenna far field radiation pattern at 135GHz. The antenna has 12^o E-plane 3 dB beam width, while the sidelobes are suppressed by 12 dB.

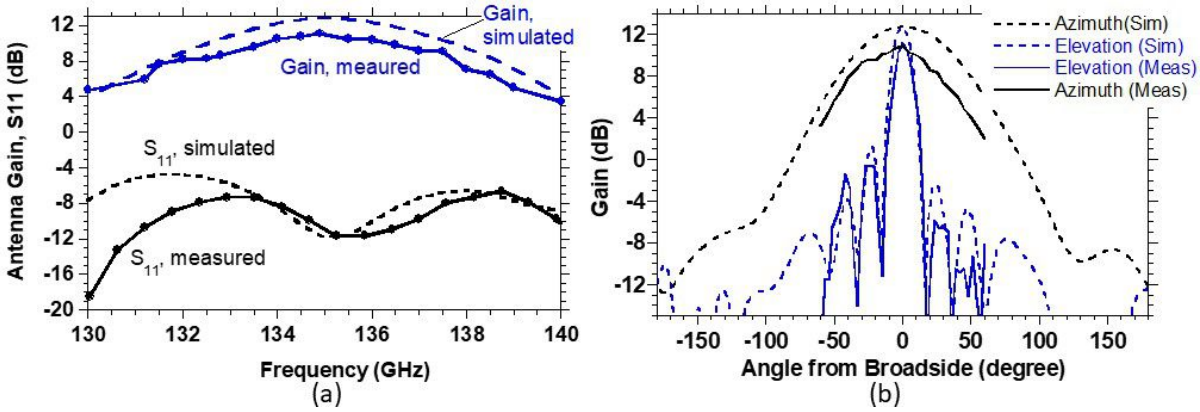


Figure 5.7: (a) Antenna measured gain and return loss vs. frequency, (b) measured antenna radiation pattern

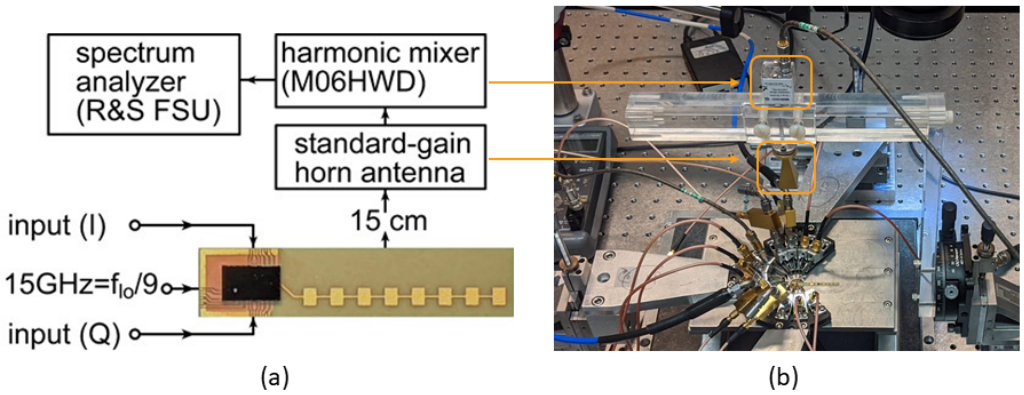


Figure 5.8: Transmitter modulation bandwidth measurement setup (a) schematic of the testing setup (b) actual measurement setup

5.2.4 Integrated Single Channel CMOS Transmitter Testing

The integrated single-channel transmitter module was first characterized, using the setup shown in Fig. 5.8, with swept-frequency and swept-power measurements. The LO is fixed at 135GHz, the Tx input signal was swept from 0.1 to 10GHz, and the transmitter upper and lower sideband powers were captured using a spectrum analyser and D-band harmonic mixer. The module has 6GHz modulation bandwidth (Fig. 5.9a) at the 3dB points (131-137GHz). The measured saturated EIRP (Fig. 5.9b) is 13dBm, with 8.4dBm EIRP at the output 1-dB compression point

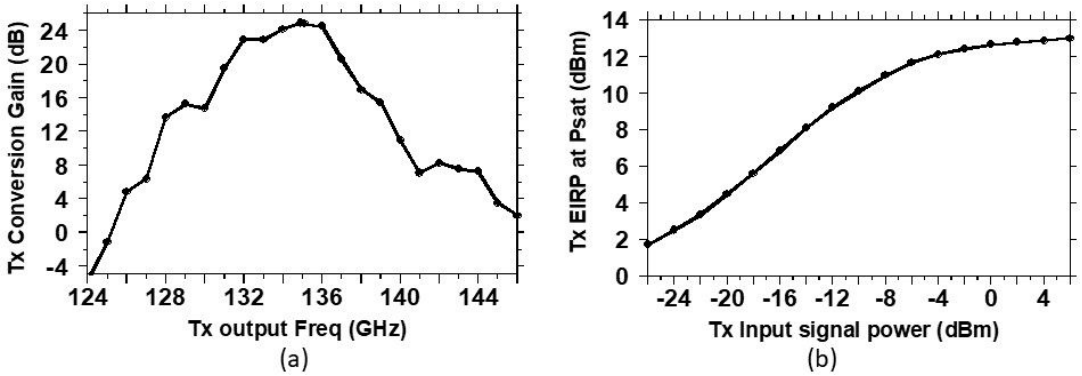


Figure 5.9: (a) measured transmitter frequency response, (b) and input-output power characteristics.

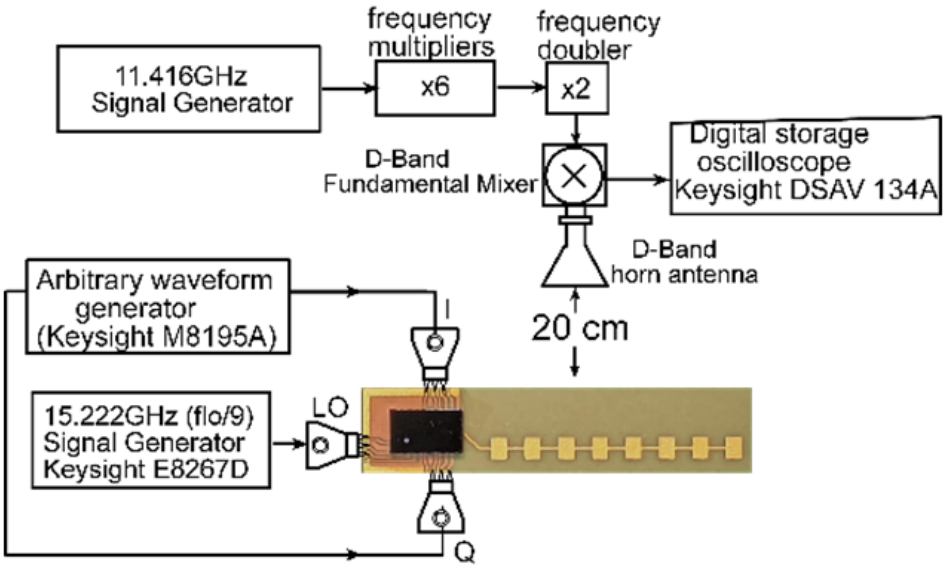


Figure 5.10: Transmitter module modulation characterization setup

Modulation performance of the transmitter module was then characterized (Fig. 5.10) using an arbitrary waveform generator (AWG) for the transmitter input signals and monitoring the module output at 20cm propagation distance using a horn antenna, a D-band fundamental mixer for frequency down conversion, and a digital storage oscilloscope (DSO) for signal acquisition. The AWG was set to generate different signal constellations modulating a 2GHz IF, (to facilitate the testing and avoid calibrating for I& Q mismatch), with the transmitter module then upconverting this modulated signal to a 137GHz carrier. The DSO demodulates the received signal and, after adaptive equalization, displays the modulation constellation and computes the error vector magnitude (EVM). With the current setup, measurements of the transmitter's modulation constellations show that it can support 16Gbps using 16QAM and 15Gbps using 64-QAM (Fig. 5.11) [42]. Note that the stated EVM magnitudes are referenced to the constellation's RMS amplitude.

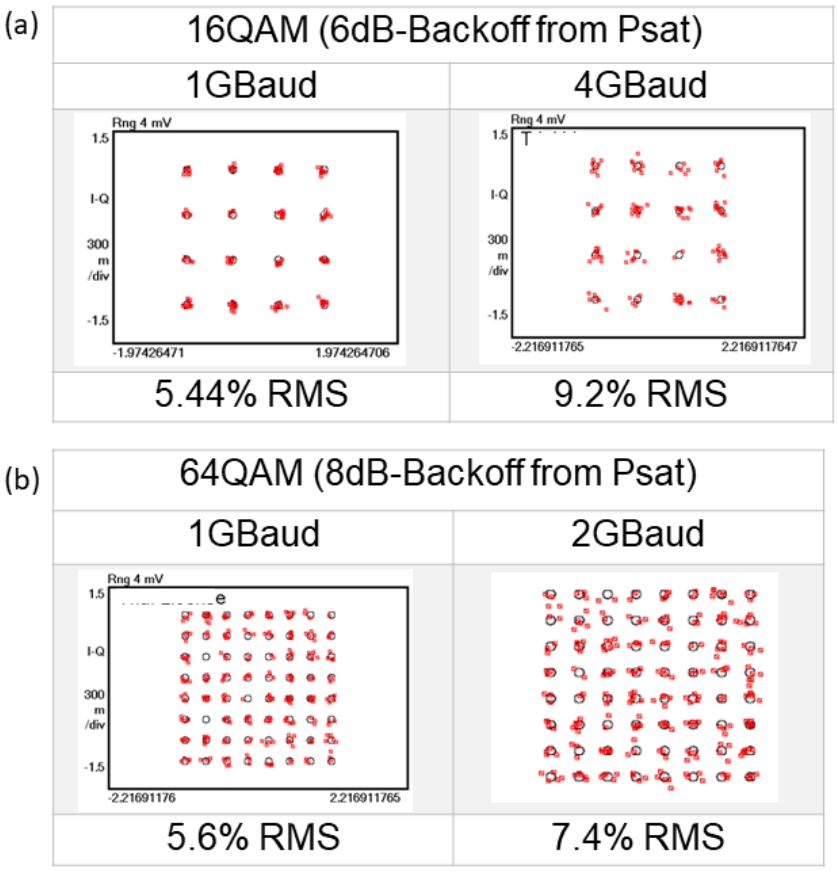


Figure 5.11: Transmitter module measured modulation constellations and computed error vector magnitudes. Power levels are quoted relative to the saturated output power.

This integrated transmitter module shows the efficacy of the ceramic carrier approach in building mm-wave packaged solutions, also shows the superiority of the advanced copper pillar technology in building IC-package transitions with a record transition loss, compared to other transition technologies mentioned in Chapter 4.2.

5.3 High-Power Single Channel D-band Transmitter on LTCC Carrier

Toward building a high-power massive MIMO array for long-range communications, we built a high-power single-channel transmitter on the same Kyocera GL771 carrier. This high-power transmitter module is a heterogenous integration between our 22FDX CMOS transmitter [41] and a high-power InP HBT power amplifier [39] having 20.5dBm Psat and 20% peak PAE. The CMOS chip is attached to the ceramic carrier using GF advanced copper pillars (section 4.2.1). The InP PA is attached to the carrier using silver-filled epoxy (84-1LMISNB), while its input, output, and power supplies are connected to the carrier using 1mil diameter Au wire bonds. The PA output is connected to an 8-element, series-fed patch antenna on the carrier (Fig .5.12).

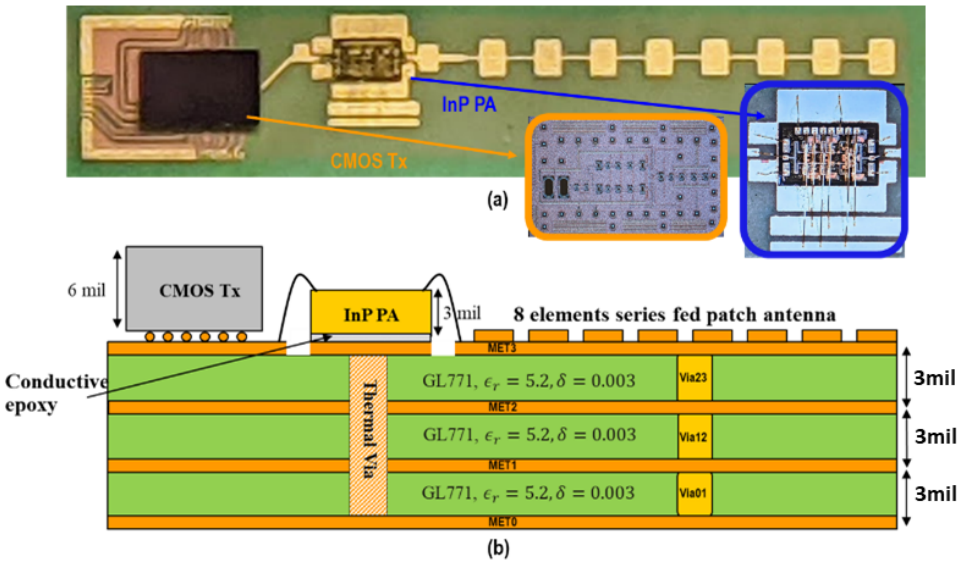


Figure 5.12: D-band transmitter module (a) micrograph and (b) schematic cross-section.

The LTCC carrier (Kyocera GL771) has 3 dielectric layers, each with ε_r=5.2 ,δ=0.003, and 4 metal layers. The dielectric constant is relatively low for LTCC, reducing skin-

effect and substrate dielectric mode coupling losses in transmission-lines and antennas. The top metal layer (MET3) forms the antenna and microstrip signal lines routing the mm-wave, I/Q baseband, and LO reference signals. MET2 and MET0 serve as ground planes, while MET1 routes supply and bias voltages. Thermal vias are placed below the InP IC to reduce the PA's operating temperature and thereby avoid degrading its output power.

5.3.1 InP PA housing in the ceramic carrier

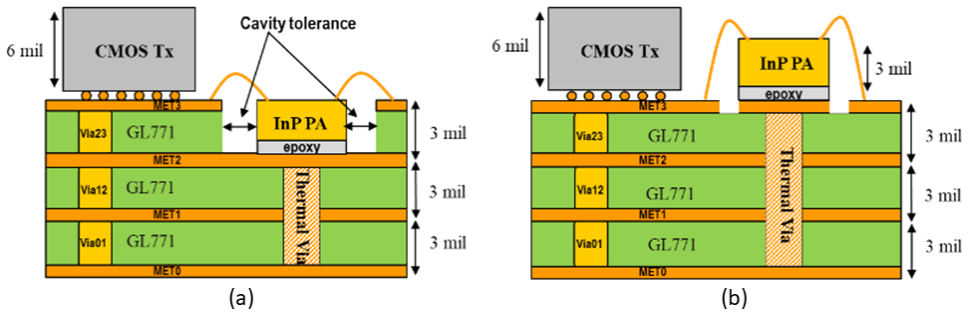


Figure 5.13: Power amplifier mounting in the ceramic carrier (a) with cavity and (b) without cavity.

Wire bond parasitics will reduce the PA gain and the power it delivers to the antenna. The PA can be either mounted within a cavity (Fig. 5.13a) or on the LTCC top surface (Fig. 5.13b). While cavity mounting avoids the 3mil bond wire height difference associated with the thickness of the InP die, the +/-150μm (6mil) lateral tolerance in the cavity dimensions increases the necessary lateral distance spanned by the wire bond. Surface mounting ultimately allowed a shorter bond, and hence was selected. The minimum wire bond length is set by the PA die thickness and by the amount of lateral extrusion of the die-attach epoxy from under the IC.

5.3.2 CMOS/ InP PA transition design

The PA input wire bonds (Fig. 5.14a) are Au with 150μm length and 1-mil diameter. Though InP-LTCC bonds are provided for both signal and ground, the ground bonds have only minor effect, as the RF ground-return currents on the LTCC MET2 ground plane, after passing through the LTCC MET2-MET3 vias, mainly pass through MET3 (Fig. 5.14c) to the InP IC back surface, and then through InP through-substrate vias (TSV's) to the InP IC top surface ground plane. A network (Fig. 5.14a) on the LTCC carrier compensates for the wire bond parasitics, matching the PA input to the CMOS 50Ω output impedance. The network has 2.6dB simulated insertion loss at 135GHz (Fig. 5.14b), including the loss from the wire bond, the 1mm total interconnect length, and the CMOS copper pillars (30μm height and 50μm diameter). The network has 8GHz 1-dB bandwidth.

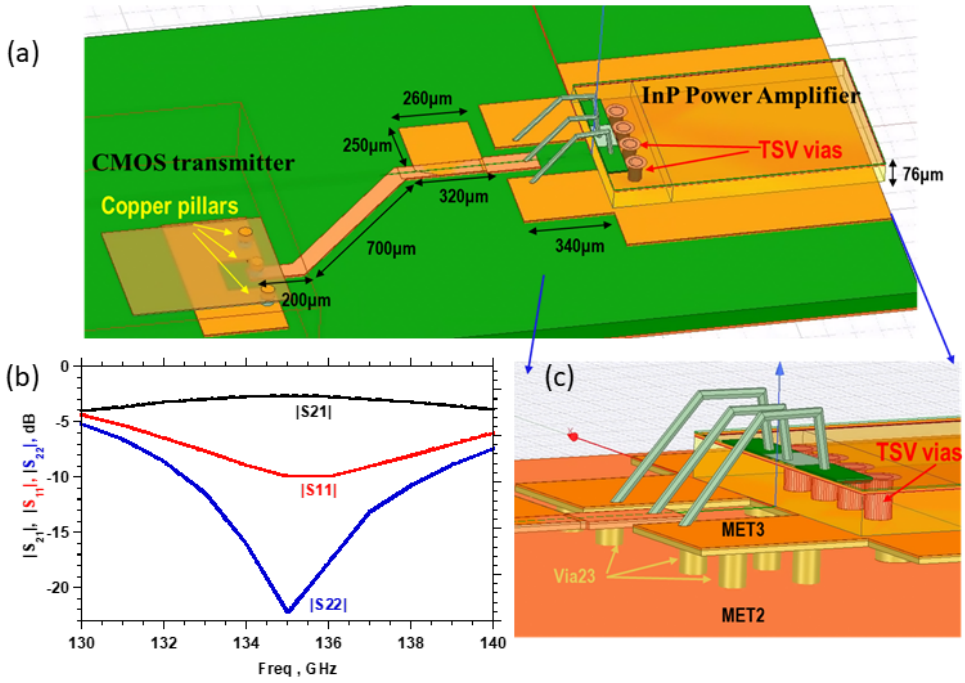


Figure 5.14: CMOS transmitter to InP transition design (a) Impedance matching network on HFSS (b) Matching network S-parameters (c) InP-LTCC transition

5.3.3 InP PA to Series Fed Patch Antenna design

The eight-element series-fed patch antenna, designed using Ansys HFSS, was matched (Fig. 5.15a) to the InP PA output, including the wire-bonds, using a stepped-impedance transmission line. The simulated antenna gain, from the PA output node, is 12dB with 6GHz 3-dB bandwidth (Fig. 5.15c) and -15dB simulated return loss (S11). A test structure for the same series fed patch antenna (Fig. 5.7) shows a measured gain of 11dB and 12^o E-plane 3-dB beam width. [42]

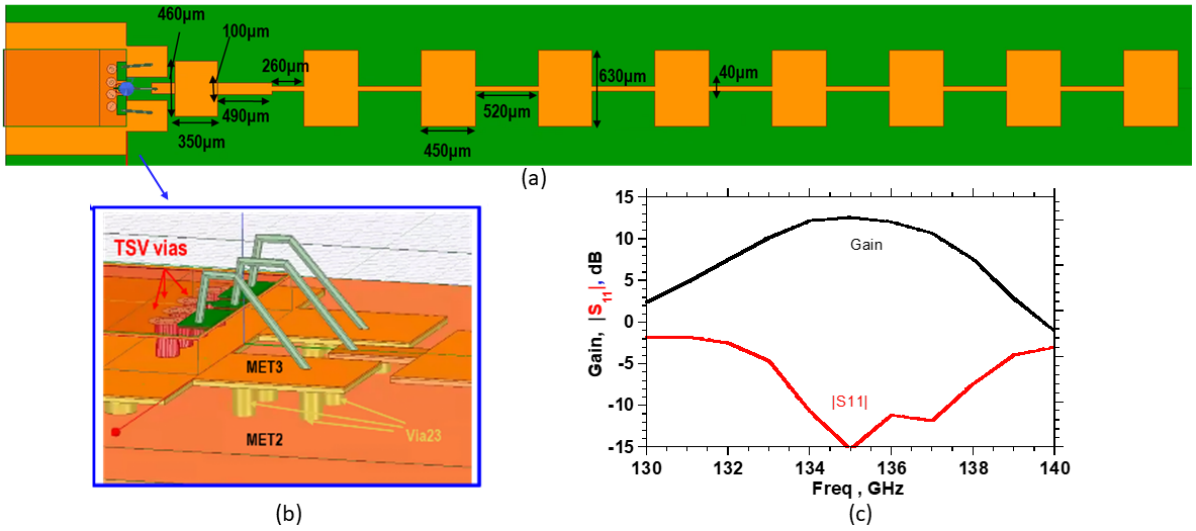


Figure 5.15: CMOS transmitter to InP transition design (a) Impedance matching network on HFSS (b) Matching network S-parameters (c) InP-LTCC transition

5.3.4 Integrated High-Power transmitter testing

The integrated transmitter module was tested using the setup of Fig. 5.16a. The module conversion gain, and modulation bandwidth were measured at a fixed 135GHz LO frequency, while the baseband (I or Q) signal is swept from 100MHz to 10GHz. The transmitted signal's upper and lower side bands are captured using a D-band harmonic mixer and spectrum analyser calibrated against a power meter. The measurement (Fig.

5.16b) shows 6GHz 3-dB modulation bandwidth and 36dB conversion gain. The saturated EIRP is measured using the same setup, fixing the LO at 135GHz and the baseband signal at 100MHz while sweeping the baseband signal power from -26dBm to 6dBm. The measured saturated EIRP is 27.5dBm (Fig. 5.16c).

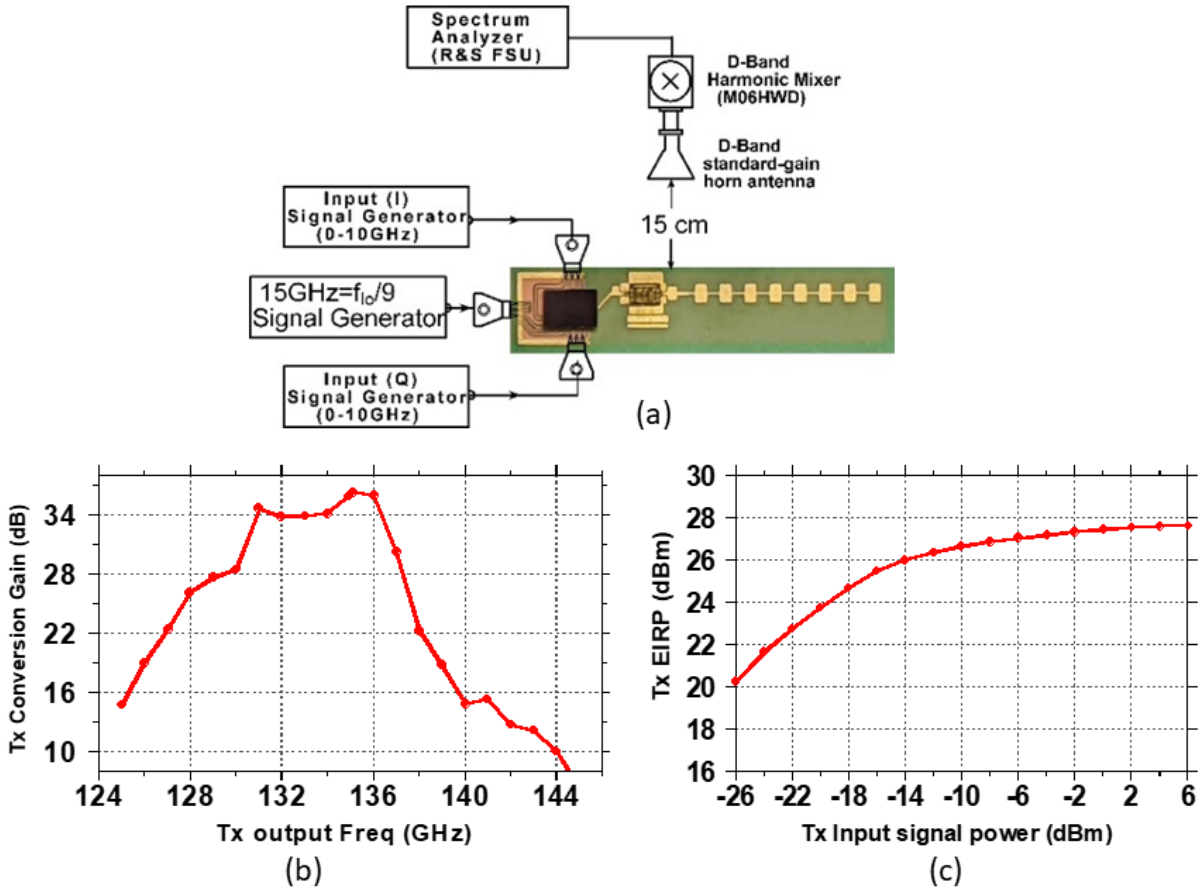


Figure 5.16: (a) Integrated transmitter module Gain and EIRP measurement setup, (b) Transmitter module frequency response (c) Pout Vs Pin characteristic

The transmitter's radiation pattern (Fig. 5.17) was also measured using the setup of Fig. 5.16a while placing the receiver antenna on a rotating arm and moving it in both elevation and azimuth. The maximum EIRP is at 4 degrees from broadside

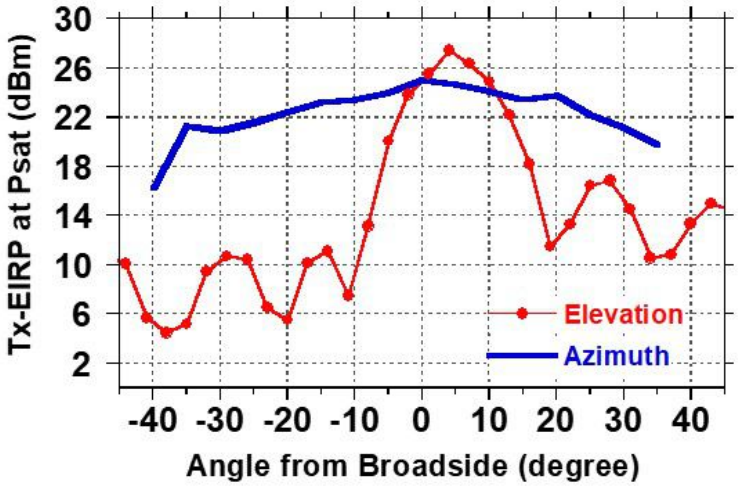


Figure 5.17: Module radiation pattern in E & H planes

To test spectral purity, a baseband signal (I or Q) was applied at 1GHz while fixing the LO at 135GHz. The upper and lower sidebands and the LO feedthrough were captured using a harmonic mixer and spectrum analyser (Fig. 5.18). The LO feedthrough is suppressed by 13dB relative to the LSB

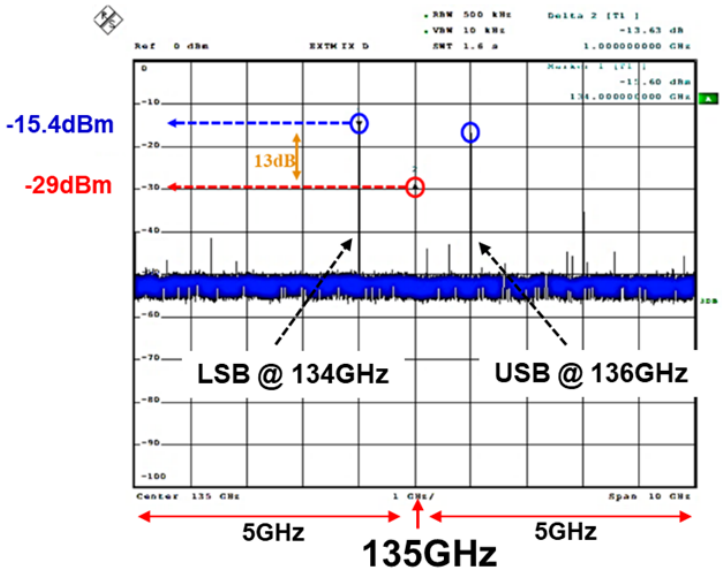


Figure 5.18: Integrated transmitter module output spectrum

Modulation performance of the transmitter module was then characterized (Fig. 5.19) using an arbitrary waveform generator (AWG) for the transmitter input signals, and monitoring the module output at 15cm propagation distance using a horn antenna, a D-band fundamental mixer for frequency down conversion, and a digital storage oscilloscope (DSO) for signal acquisition. The AWG was set to generate different signal constellations modulating a 4GHz IF, with the transmitter module then upconverting this modulated signal to a 134GHz carrier. The D-band fundamental mixer down-converts the received signal to a 4GHz IF. The DSO demodulates the received signal, and, after adaptive equalization, displays (Fig. 5.20) the modulation constellation and computes the error vector magnitude (EVM). The stated EVM magnitudes are referenced to the constellation's RMS amplitude. Under 5Gbaud, 64QAM modulation (30Gbps), the module shows 8.5% RMS error vector magnitude (EVM) at 21.5dBm EIRP. Note that this measured EVM is due to the combined non-linearity and noise for both our integrated transmitter module and the commercial of the shelf receiver.

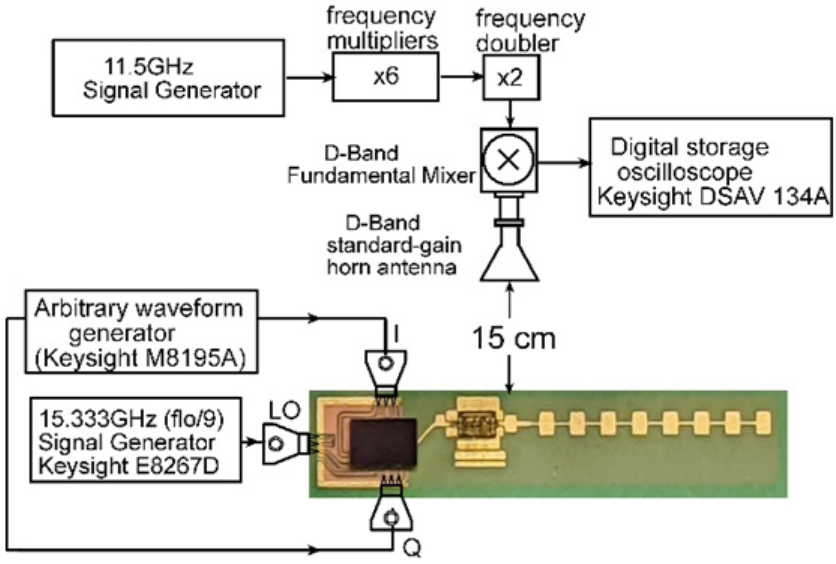


Figure 5.19: Transmitter module modulation characterization

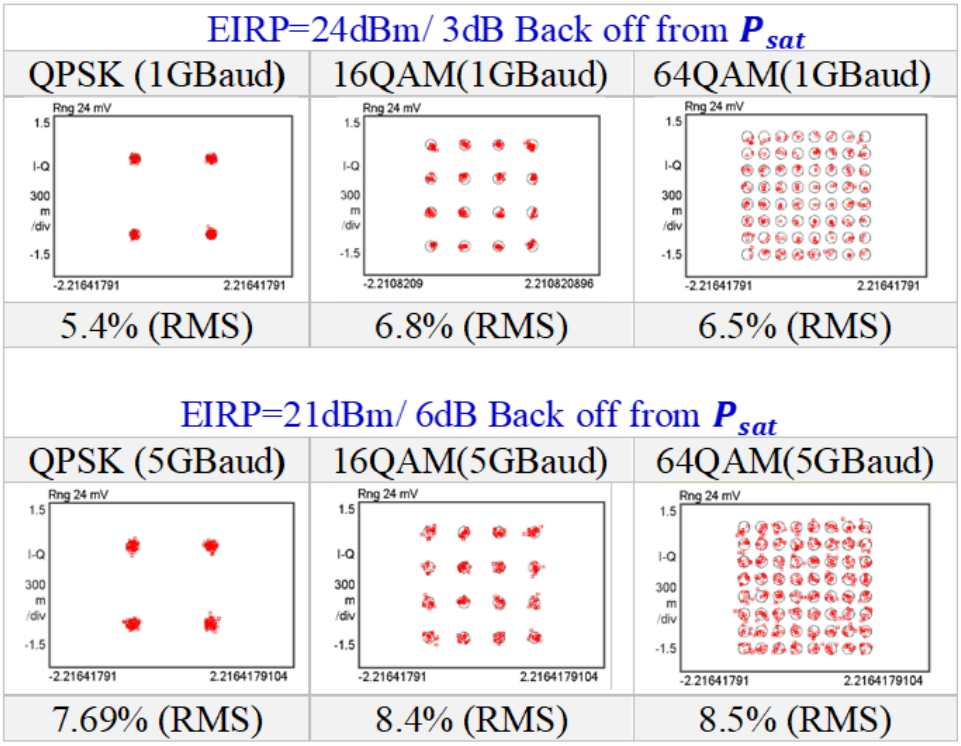


Figure 5.20: Transmitter module measured modulation constellations and computed error vector magnitudes.

For each of the supported modulation schemes, the RMS error vector magnitude was measured (Fig. 5.21a) at different output power while fixing the data rate at 1GBaud. Similarly, the RMS error vector magnitude was measured as a function of symbol rate at a fixed 21dBm EIRP of 21dBm (Fig. 5.21b). This shows that at 1GBaud date rate we can retrieve either QPSK, 16QAM or 64QAM with a reasonably high EIRP up to 25dBm and with decent system EVM-RMS of 7%. For 5GBaud and 21dBm EIRP the three modulation schemes can be retrieved with a decent EVM-RMS $\leq$ 8.5%.

The integrated transmitter module consumes 760mW (200mW in the CMOS transmitter and 560mW in the InP PA). Table 2 compares the transmitter module with recent published packaged modules in D-band. This integrated heterogeneously integrated transmitter has the highest reported EIRP and highest efficiency compared to the state of

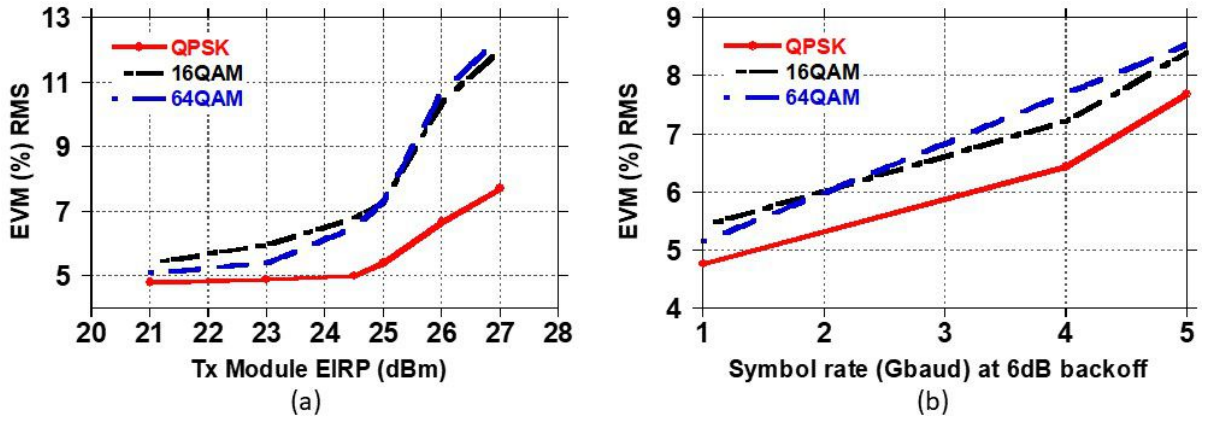


Figure 5.21: Transmitter module measured error vector magnitude (a) vs. EIRP for different modulation constellations at 1GBaud symbol rate (b) vs. symbol rate for different modulation constellations at 21dBm EIRP.

the art packaged single channel D-band transmitters. The integrated transmitter module has 3-dB bandwidth of 6GHz, mainly limited by the 3-dB BW of the series fed patch antenna. The module has 36dB conversion gain (17dB from the CMOS transmitter, 19dB from the InP PA, 10dB gain from the antenna, and 3dB wirebond insertion loss at the power amplifier input/output).

In summary, both the low power and high power single-channel transmitters assembled on Kyocera ceramic interposers show the efficacy in building mm-wave transceivers on LTCC carriers, with decent transition loss and good antenna performance. The assembly issues associated with the ceramic carrier addressed in section 5.2.1 and 5.3.1 are manageable, compared to the complete failure in the PCB approach (Chapter 4). Based on the excellent outcome of this experiment, we decided to move on with this packaging technology and build our transmitter and receiver tile for the massive MIMO arrays, as shown in the next section.

Table 5.1: Comparison with state-of-the-art D-band transmitters

	Ito [46] [BCICST'19]	Singh [47] [RFIC'20]	Simsek[29] [RWS'20]	Carpenter [48] [MTT'16]	This Work [RFIC2021]
Package Technology	Silica based with WR-6 transition	Radio on Glass with WR-6 transition	Radio on PCB (Astra MT77)	No	LTCC Interposer
IC Technology	70nm GaAs mHEMT	0.13μm SiGe-BICMOS	45nm CMOS SOI	0.25μm InP DHBT	22nm-FDSOI + 0.25μm InP HBT
Antenna Integration	No	No	Antenna on PCB	No	Antenna on Ceramic carrier
Frequency (GHz)	142-157	115-155 (LB) 135-170 (HB)	142-147	110-160	131-137
Tx Gain	12dB	17dB (LB) 18dB (HB)	NA	24dB	36dB
EIRP (dBm) at Psat	-	-	14dBm	-	27.5dBm
Tx-Psat	8dBm	13dBm	2dBm	9dBm	17dBm*
Tx Pdc (mW)	1100	1350 (LB) 2100 (HB)	-	170	760
Peak data rate/ Modulation	10Gb/s (128QAM) EVM (N/A)	42-Gb/s (128-QAM) EVM (4.4%)	10Gb/s (QPSK) EVM (NA)	20-Gb/s^{++} 32QAM EVM (10.6%)	30Gb/s (64QAM) EVM-RMS (8.5%)
P_{out} at Peak data rate	NA	0.5dBm	2dBm	NA	11dBm*

*calculated as (EIRP-antenna gain), ++ Link include Tx and RX ** EIRP from combing two transmitter channels

5.4 High-Power 8-channels 135GHz MIMO Hub Transmitter Tile Module

5.4.1 MIMO Hub Transmitter Core

The core of the high power transmitter module integrates eight RF channels on an LTCC carrier, each channel having the 22nm FDSOI CMOS IC for baseband-RF conversion, an InP HBT power amplifier, and a linear microstrip patch antenna array. Fig. 5.22 shows the ceramic interposer carrying the 8-transmitter channels, with 4-channels on the left and 4-channels on the right. We chose this floor plan to minimize the antenna spacing and enhance the array field of view. Thanks to the fine lithographic resolution of the Kyocera LTCC carrier of 40μm/40μm trace width/space, we achieved a uniform antenna spacing equals 0.65λ. The CMOS transmitters are down-bonded to the LTCC carrier using GF copper pillars, the InP is attached to the carrier using conductive epoxy. The input, output, and DC supplies for the InP PA are through Au wirebonds, as shown in Fig. 5.23.

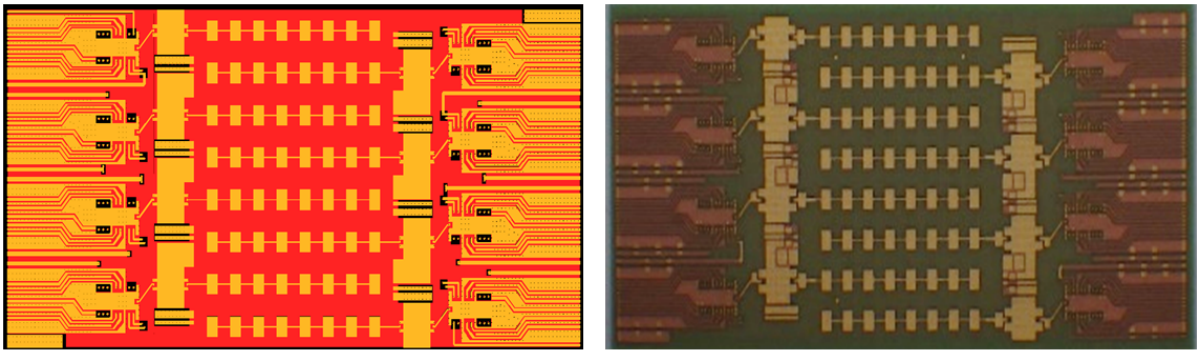


Figure 5.22: An eight channels transmitter tile of heterogeneously integrated CMOS transmitter and InP Power amplifier, assembled on Kyocera Gl771 ceramic carrier (a) carrier design using ADS (b) manufactured LTCC carrier by Kyocera Japan

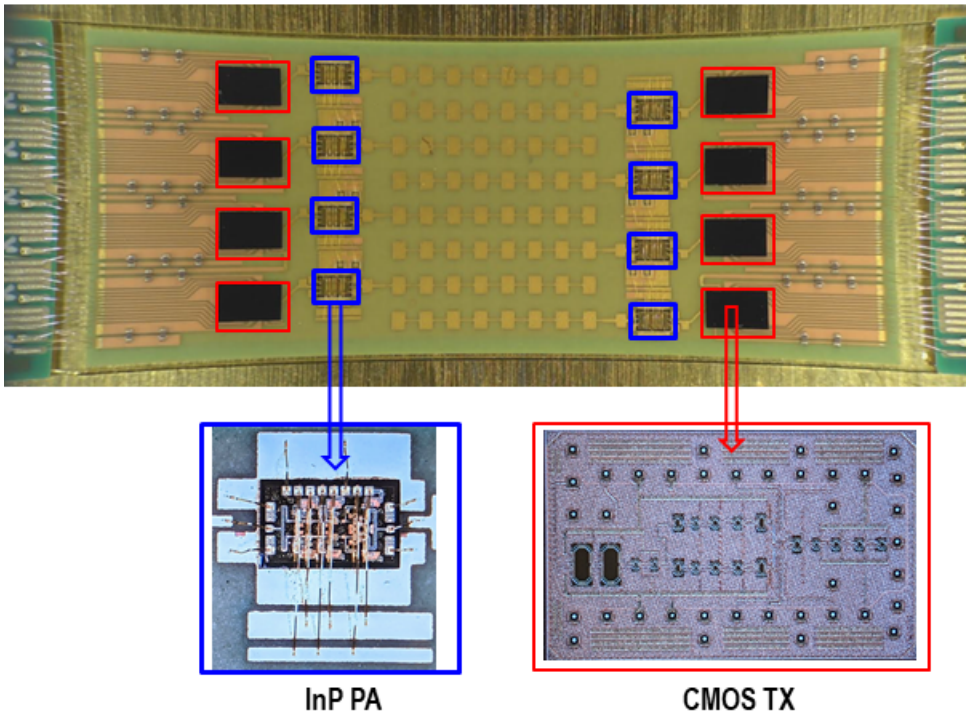
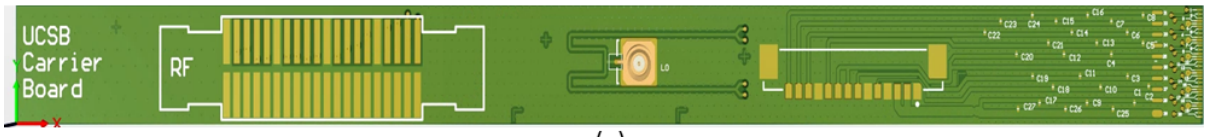


Figure 5.23: CMOS transmitter and InP power amplifiers assembled on Kyocera GL771 ceramic carrier

5.4.2 MIMO Hub Transmitter Backend

Due to the ceramic interposer's small manufacturable footprint, we could not fit the connectors to the digital backend on the same interposer. We designed a six-layer PCB (Fig. 5.24) carrying the DC, baseband IQ, and LO signal connectors. This PCB is later connected to the LTCC using wire bonds. Due to the harsh requirement to keep a uniform antenna spacing between tiles of 0.65λ, the PCB should have the same width as the ceramic interposer. This imposes the longitudinal PCB shape shown in Fig. 5.24. The PCB laminate material is Tachyon 3313 with ε_r=3.3 and loss tangent δ=0.003. All the I, Q signals on the PCB have a 50Ω trace impedance, and all connectors are attached to the PCB using surface mount technology.



(a)

(b)

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5	
1	L1_Top		Signal	1oz	1.4mil		
	Dielectric 1	Tachyon 3313	Core		5mil	3.29	0.003
2	L2_GND		Signal	1/2oz	0.7mil		
	Dielectric 2	Tachyon 3313	Prepreg		5.1mil	3.29	0.003
3	L3RF1		Signal	1/2oz	0.7mil		
	Dielectric 3	Tachyon 3313	Core		5mil	3.29	0.003
4	L4_GND		Signal	1/2oz	0.7mil		
	Dielectric 4	Tachyon 3313	Prepreg		5.1mil	3.29	0.003
5	L3RF2		Signal	1/2oz	0.7mil		
	Dielectric 5	Tachyon 3313	Core		5mil	3.29	0.003
6	Bottom Layer		Signal	1/2oz	0.7mil		

(c)

Figure 5.24: MIMO tile backend interface card (PCB) (a) PCB design using Altium (b) manufactured interface card (c) PCB stack of 6-layer

5.4.3 MIMO Hub Transmitter Module Integration

We integrated the LTCC carrier and the PCB carrying the interface connectors on a gold plated copper bar (Fig. 5.25). This copper bar acts as a common ground plane between the LTCC carrier and PCB board. In addition, copper has good thermal conductivity, so the copper bar can help get the heat out of the module. The IQ, LO, and DC signals are routed from the LTCC carrier to the PCB using Aluminum wire bonds. There are two PCB cards in the module, one carrying the IQ, LO, and DC signals to the left half of the module, and the other doing the same for the right half of the module.

We tested the integrated transmitter module to verify the functionality of the module and the yield of the assembly process. We excited one single channel at a time with a single tone at 100MHz, with the LO signal fixed at 135GHz. We measured the out-

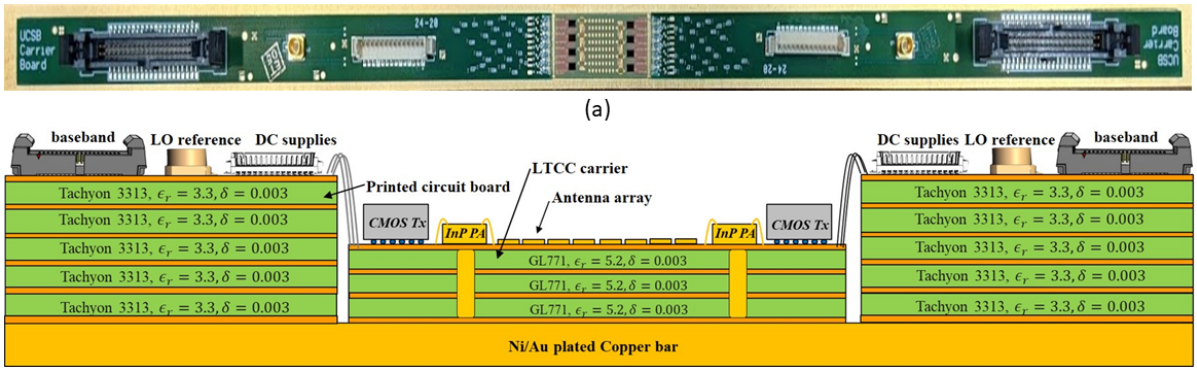


Figure 5.25: Eight-channel 135GHz MIMO hub transmitter array tile module: (a) photograph of the overall module, (b) cross-section diagram showing the interface printed circuit boards , the LTCC carrier, connectors, and ICs. The overall module is 450mm × 15mm, while the LTCC carrier is approximately 12 mm × 33 mm

put power at a 15cm distance, using D-band harmonic mixer connected to a spectrum analyzer (Fig. 5.26). The measurements show that all the 8-transmitter channels are correctly biased. However, because of assembly difficulties, two of the eight channels have very low gain. Two other channels have EIRP well below the 27.5dBm measured independently on a single-channel test structure(Fig. 5.27).

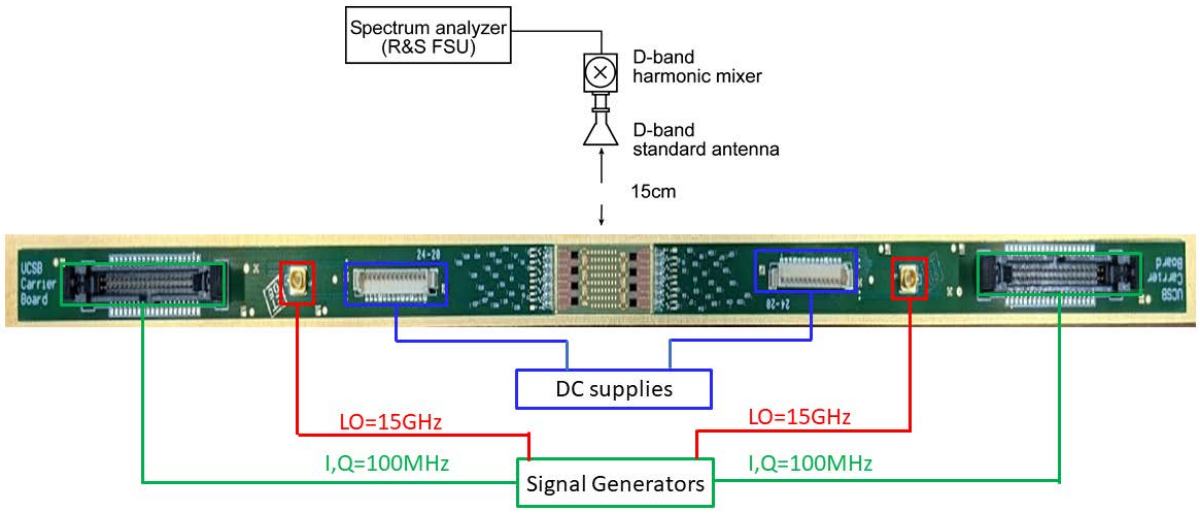


Figure 5.26: Transmitter module per-channel EIRP testing setup

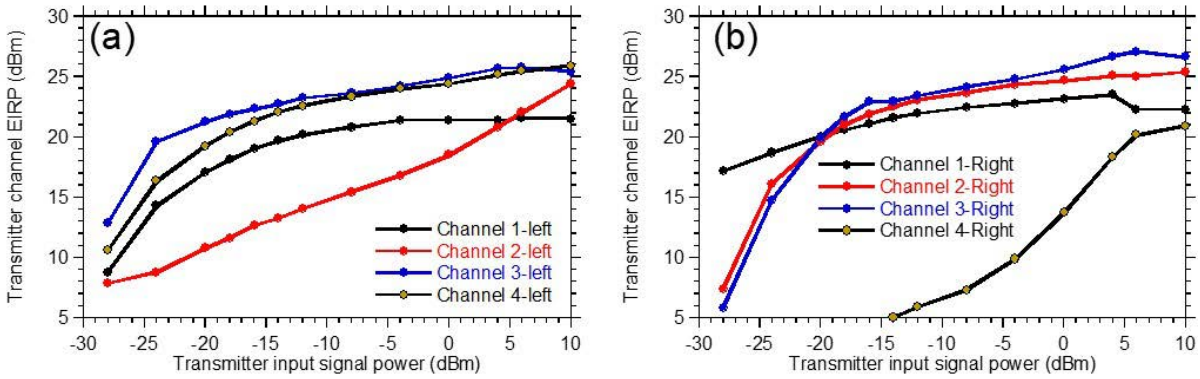


Figure 5.27: Transmitter module measured per-channel EIRP vs input signal power

Despite the yield in the assembly process and the poor performance of 2-channels out of 8, this module can still retrieve 8- independent beams simultaneously. We can use the integrated transmitter module in either a single beam or multibeam applications; we will illustrate this in Chapter 6. Note that the yield in the assembly process is mainly coming from the small diameter of the CMOS chips copper pillars and how to secure mounting pillars in the exact location on the LTCC carrier.

5.5 Low-Power 8-channels 135GHz MIMO Hub Transmitter Tile Module

We designed another 8-channels MIMO transmitter tile for short-range communication. It has a similar structure as the high power transmitter MIMO tile but without the high-power InP power amplifiers (Fig. 5.28). We tested this module, but only 4 out of the 8-transmitter channels work fine due to some assembly difficulties. So, we sidelined this low power transmitter module and used the high-power transmitter module for our demonstration, as shown in Chapter 6.

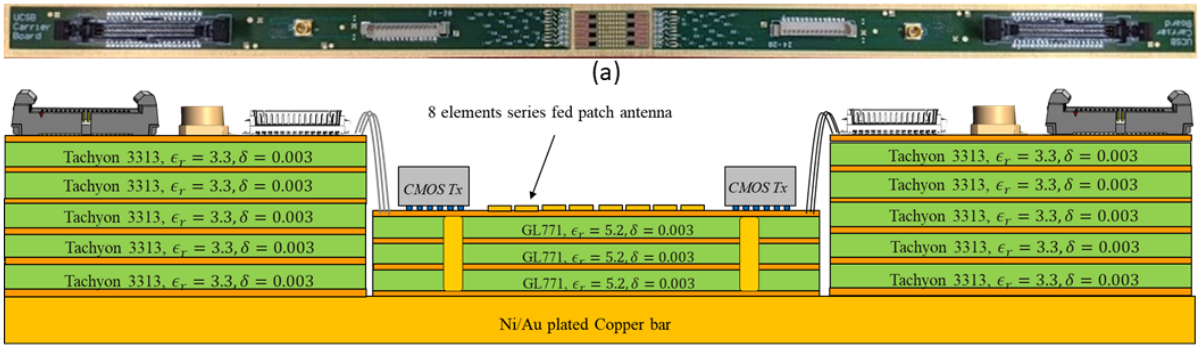


Figure 5.28: Low power 8-channel 135GHz MIMO hub transmitter array tile module: (a) photograph of the overall module, (b) cross-section diagram showing the interface printed circuit boards , the LTCC carrier, connectors, and ICs

5.6 Eight-channels 135GHz MIMO Hub Receiver Tile Module

The receiver module has an array of eight antennas, at 0.65λ pitch, each being a linear microstrip patch array. These antennas feed eight single-channel receiver ICs, in Global Foundries 22nm SOI CMOS that down convert the received RF signals, generating differential baseband IQ signals (Fig. 5.29). The LTCC carrier is connected to another low-cost PCB carrying the IQ, LO, DC bias connectors, as showin in Fig. 5.30.

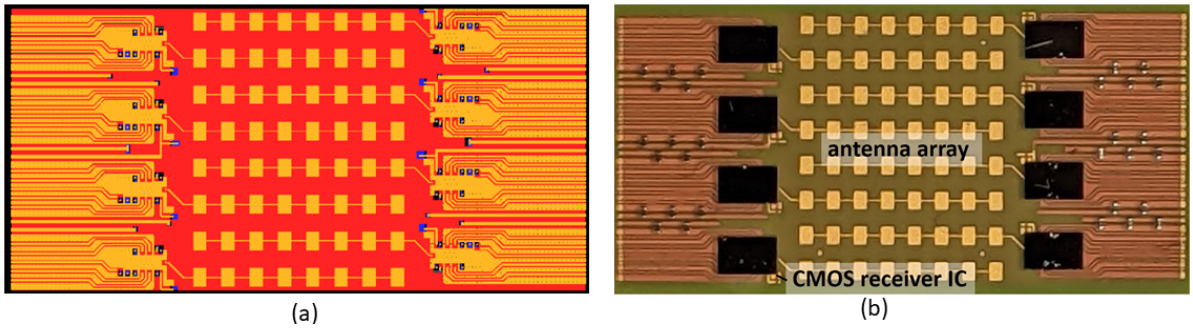


Figure 5.29: an 8-channel receiver tile with CMOS chips assembled on Kyocera GL771 (a) tile design using ADS (b) manufactured and assembled tile by Kyocera San Diego

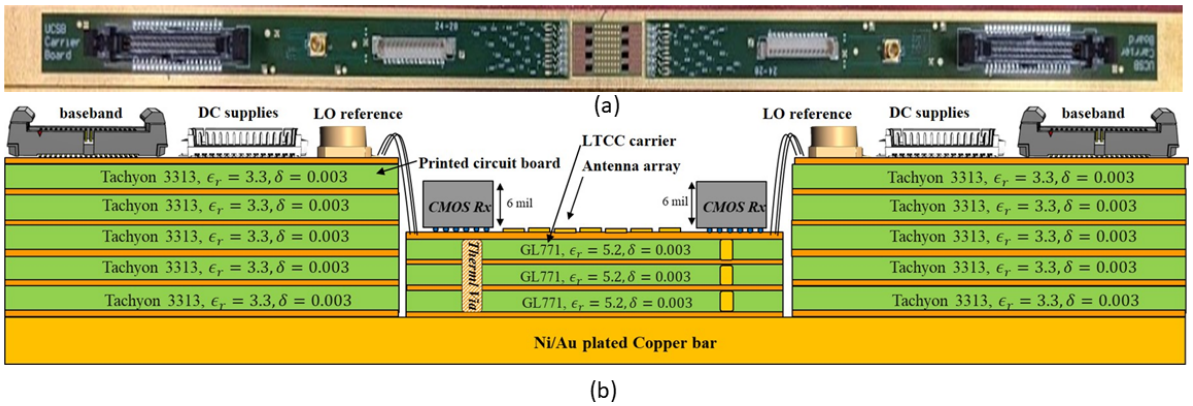


Figure 5.30: Eight-channel 135GHz MIMO receiver array tile module: (a) photograph of the overall module, (b) cross-section diagram showing the interface printed circuit boards , the LTCC carrier, connectors, and ICs, and. The overall module is 450mm × 15mm, while the LTCC carrier is approximately 12 mm × 25 mm.

Two eight-channel receiver modules were constructed; both have assembly defects. In one, four of the eight channels function, resulting in a 4-element array at 1.3λ pitch. In the second, all eight channels function with 0.65λ antenna pitch, but excessive DC supply lead resistance prevents proper biasing for high-data-rate operation. We tested the 4-channels receiver module using the setup shown in Fig. 5.31. A commercial of the shelf transmitter at 15cm distance transmits a single tone at 135.1GHz, and the receiver IQ outputs are connected to a spectrum analyzer. After de-embedding the path loss and setup losses, Fig. 5.32 shows the gain versus received power for the channels on the 4-channel module. This 6-dB difference in the measured conversion gain between the 4-channel can be explained as a consequence of different solder joint impedance for the IQ signals and different supply voltage per channel.

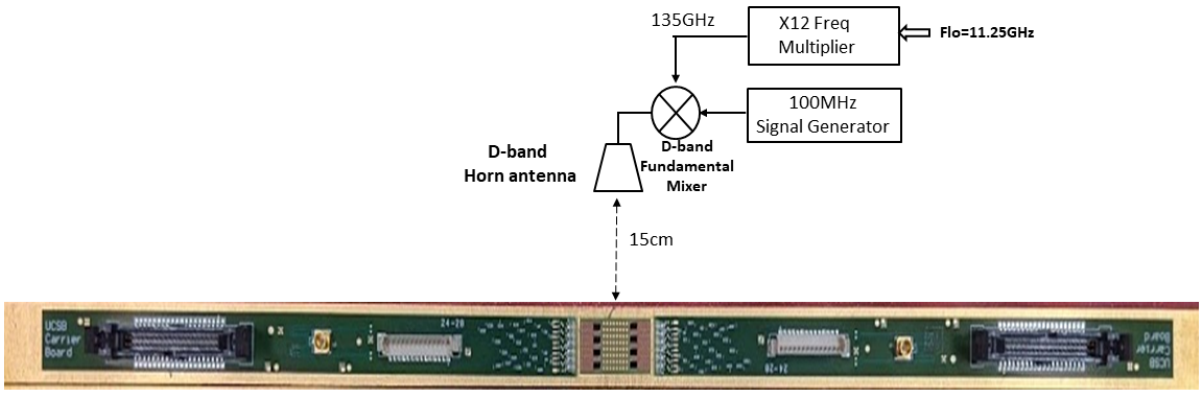


Figure 5.31: Receiver module per-channel conversion gain testing setup

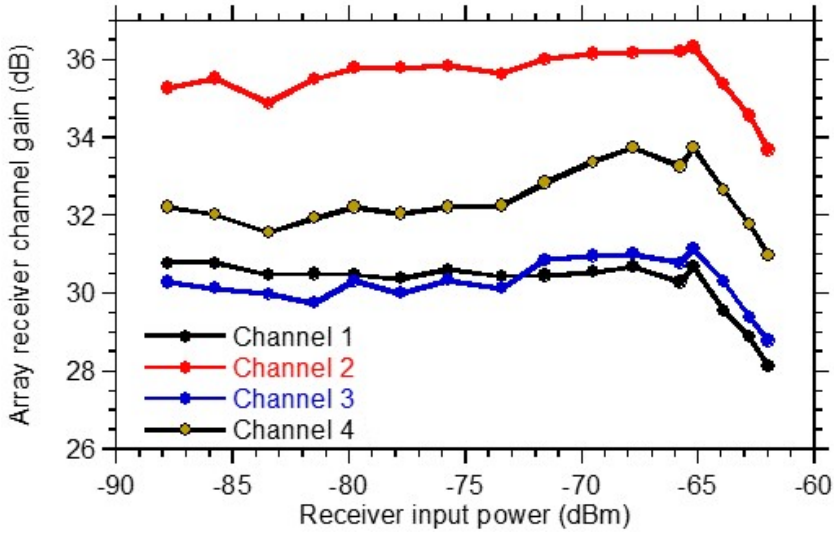


Figure 5.32: Measured gains of the receiver channels on the 4-channel module.

5.7 conclusion

In this chapter, we illustrated in detail the procedures of building mm-wave packaged arrays on ceramic carriers. We started by building low-power and high-power single channel transmitters on Kyocera GL771 ceramic carrier. We illustrated the assembly challenges to secure bonding the copper pillars at the designated location, and how to minimize the wirebond losses associated with routing the InP PA on the ceramic carrier. Then, we compared our high-power packaged single-channel transmitter with the state-

of-the-art packaged transmitters at the same D-frequency band. We showed that our single-channel transmitter has the highest reported EIRP and can support up to 30Gb/s data rate. Next, we illustrated the procedure to build transmitter and receiver arrays in tile using ceramic interposers. We presented some basic measurements for both the transmitter and receiver modules. We showed a fully functional transmitter tile of 8-elements and a fully functional receiver tile of 4-elements. In the next chapter, we will use the transmitter and receiver tiles and demonstrate some wireless links at 135GHz.

Chapter 6

MIMO Demonstration

This chapter focuses on illustrating application and use cases for our transmitter and receiver MIMO tiles, and how to deploy the tiles to build multiuser massive MIMO arrays. We demonstrate wireless link between the our fully packaged transmitter and receiver tiles with another commercial of the shelf transceivers

6.1 Introduction

The transmitter and receiver tile modules are design for use in sets to form 32-element or larger horizontal linear array (Fig. 6.1a) that simultaneously receives many incident signals, separating them (Fig. 6.1b) by their horizontal angle of incidence θ. If most users are on the ground, with fewer in tall buildings, a linear (1D) array better separates user signals than a 2D array. Even with a small vertical -3dB beam width and no vertical beam steering, signals from the top of moderately tall buildings can be received because, given some maximum height, as the elevation angle ϕ increases, the received signal strength will increase if the antenna is designed so that its gain decreases less rapidly than at large ϕ (Fig. 6.1c).

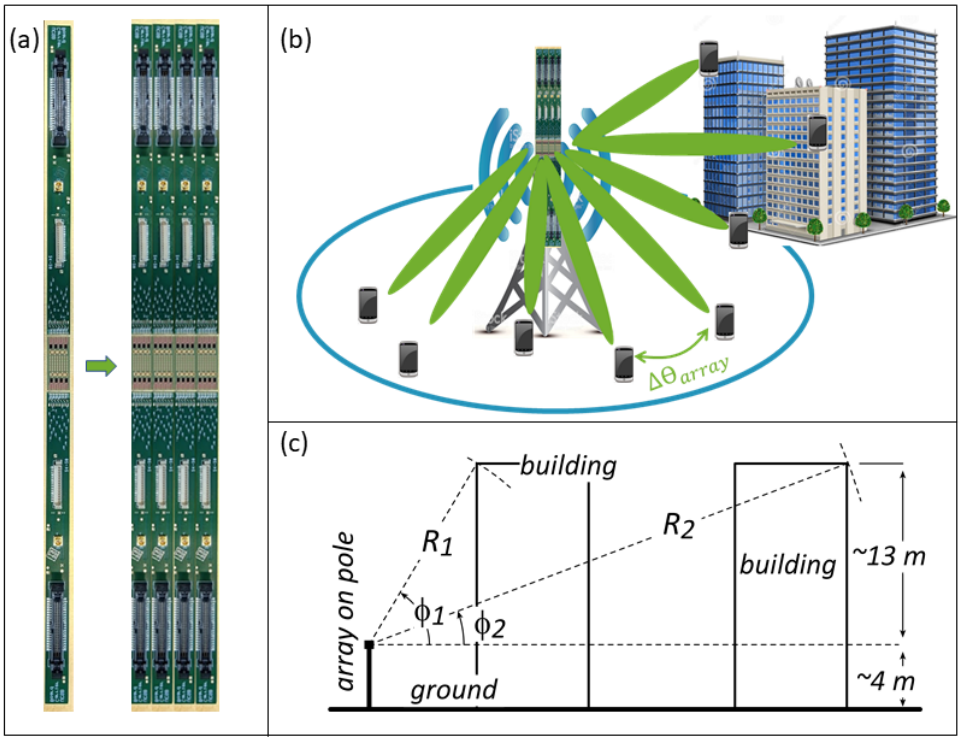


Figure 6.1: The array (a) 4-cascaded tiles forming array of 32-elements, producing horizontally-steered beams having narrow lateral and moderate vertical beam width. (b) cartoon drawing for array installed on basestation towers and users are primarily distributed laterally over the ground, but some distributed vertically in tall buildings (c) Given a maximum building height, the range R decreases rapidly as the elevation angle ϕ increases, hence vertical beam steering is not required.

We designed our MIMO arrays for use with MIMO digital beamforming [15] [49] [11], which form the array's IQ output signals, determines the data and direction of the received signals. System link budget analysis is reported in [1].

6.2 Transmitter Array/Tile Demonstration

To test the transmitter array (Fig. 6.2), a PC running MATLAB generates each channel's baseband transmitted signal and sends this to an FPGA (ZCu111). From these signals, the FPGA generates modulated signals at a 1GHz IF. External IQ demodulators (ADI LTC5594) then convert the 1GHz IF FPGA outputs to IQ baseband. The required

sixteen baseband signals are thus generated by an FPGA having only 8 DACs. A test receiver, mounted on a rotation stage 15cm from the array, down converts the signal to a 1GHz IF, and an ADC on the FPGA captures this signal

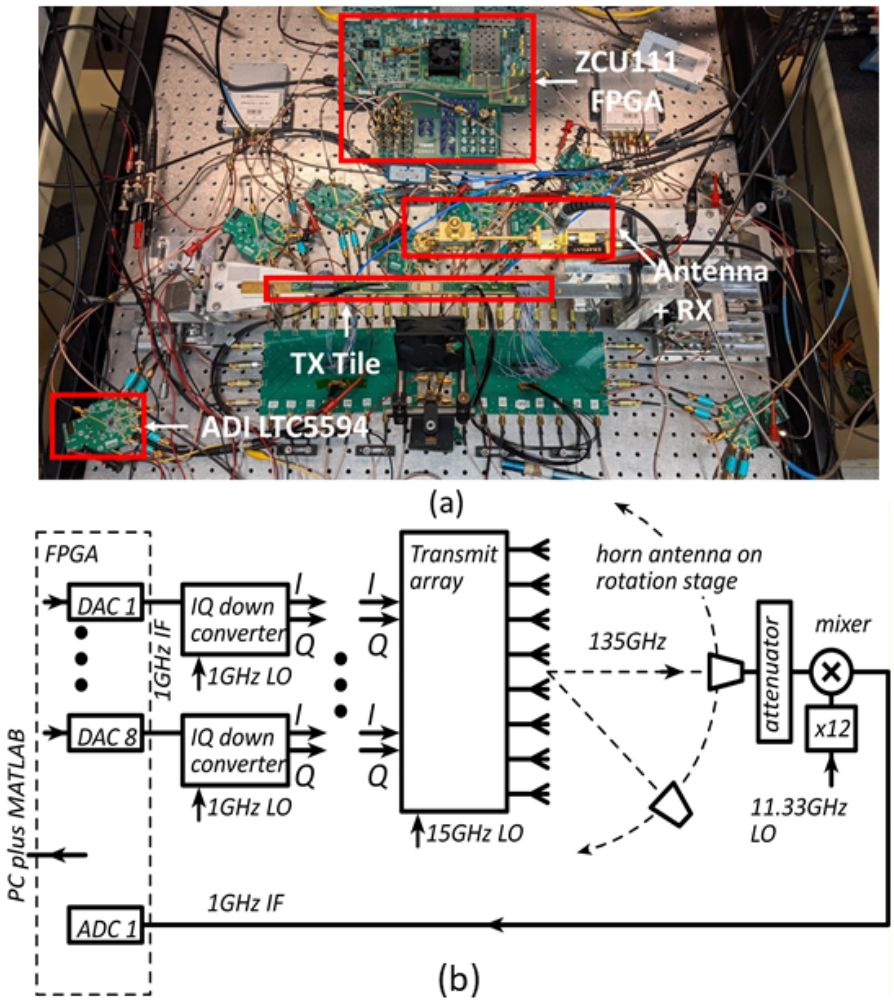


Figure 6.2: Experimental configuration for transmitter array characterization. The eight FPGA DACs each generate modulated data on a 1GHz IF and eight IQ downconverters generate IQ signals that drive the transmitter array. A test receiver, mounted on a rotation stage 15cm from the array, down converts the signal to a 1GHz IF, and an ADC on the FPGA captures the signal. (a) actual setup (b) simplified drawing

6.2.1 Array Radiation Pattern and EIRP

To form and aim beams, the array must be calibrated, i.e. differences between channel gains and phases are measured and then corrected for. Given the very strong differences between channel gains (Fig. 5.27), only phase errors were calibrated. Device drivers and calibration procedures were adapted from Pi-Radio open-source code [50] [51]. These first measure the per-channel fractional timing offsets of the modulating data streams and the channel-channel variations in the LO phase. The resulting calibration factors are applied to the transmitter drive signals to perform beamforming and data transmission experiments.

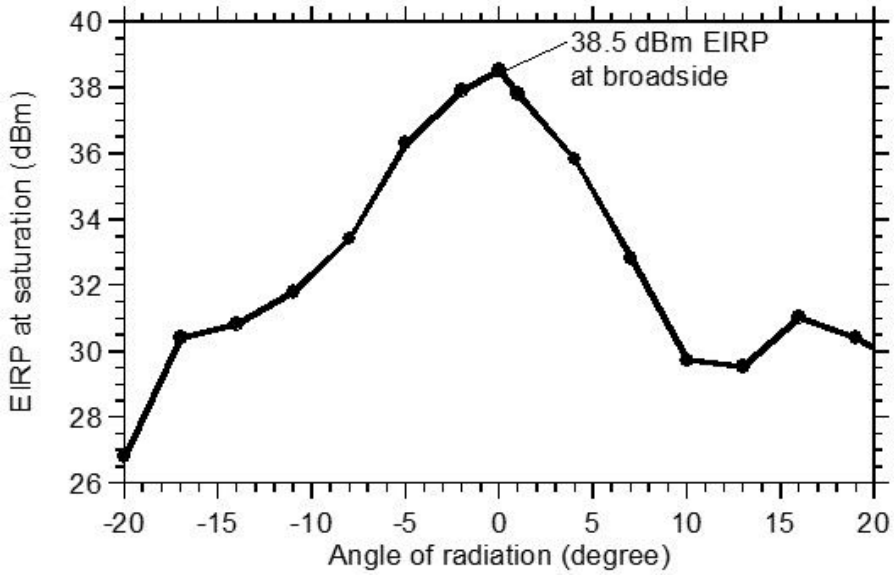


Figure 6.3: Measured transmitter array EIRP, measured at saturation, as a function of angle of radiation, with the array aimed at broadside. The angle of radiation is in the H-plane.

Having calibrated the array, the drive signals to the 8 channels were then set to direct a CW signal to broadside (Fig. 6.3), and the horn antenna then rotated to measure the radiated power density as a function of angle in the H-plane. The 38.5dBm peak EIRP is record for an array in D-band. Yet, this EIRP is limited by assembly difficulties; had

each of the 8 transmitter channels functioned with the same performance as in [43], the EIRP would have been 46dBm.

Then we measured the array radiation pattern and the array field of view; by controlling the phase of the incoming signal from the FPGA. We steered the beam from -15 to 15 degrees and captured the transmitted beam using the same setup shown in Fig. 6.2. We observed that at larger scan angles, the beam pattern degrades. Also, since this measurement was done in an open room (not an anechoic chamber), we suffered from evident multi-path reflections, thus contributed to limiting the array F.O.V.

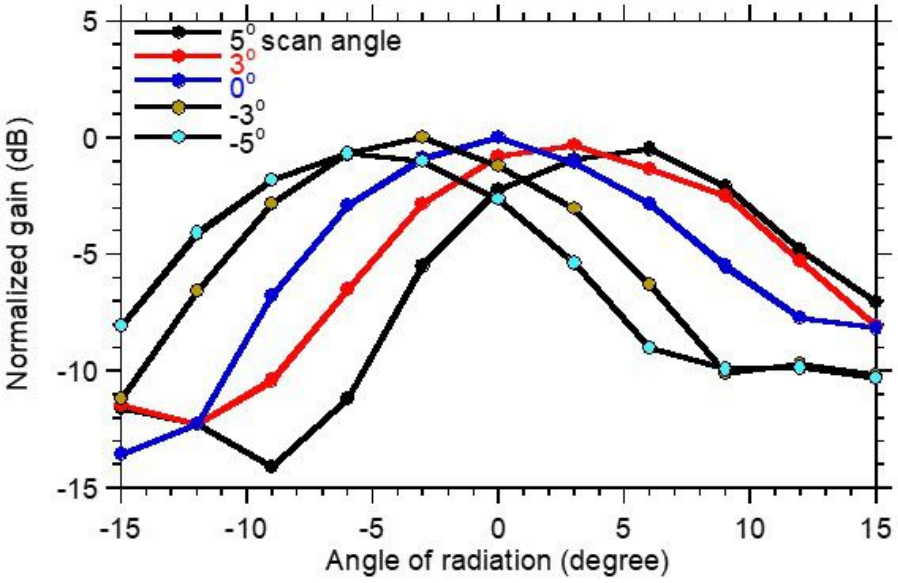


Figure 6.4: Measured transmitter array beam patterns with the array aimed at 5^0, 3^0, 0^0, -3^0 and -5^0 scan angles.

6.2.2 Transmitter Array Wireless Link

Fig. 6.5 shows data transmission experiments. The data is transmitted using OFDM, with 960 kHz subcarrier spacing. In single-beam operation, there is -13.5dB RMS error vector magnitude in 1.34Gb/s QPSK transmission, and -13dB error vector magnitude in

1.92Gb/s 16QAM transmission, measured at an EIRP of 38dBm. These EVM numbers include the non-linearity and noise contribution from our integrated packaged transmitter module, the commercial of shelf receiver,and ADI IQ demodulators (LTC5594).

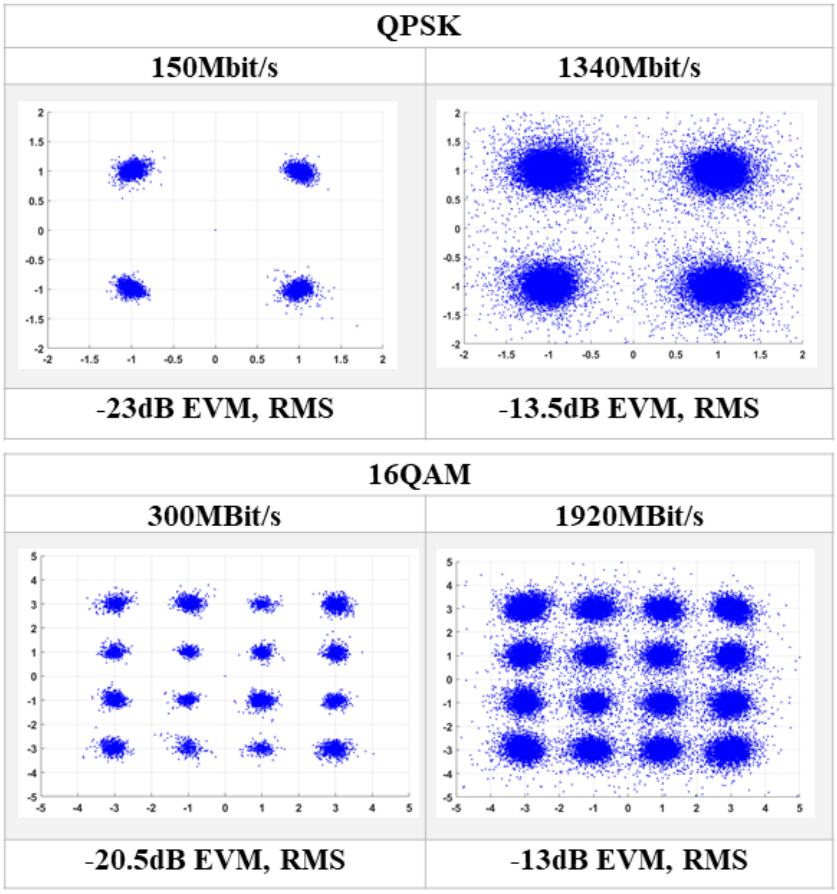


Figure 6.5: Measured transmitter QPSK and 16QAM modulation constellations and computed error vector magnitude.

Fig. 6.6 shows the error vector magnitude as a function of data rate. Data rates are limited both by the FGPA sample rate and by the bandwidth of the multi-pin base-band IQ signal connectors; without these limits, the single-channel module operated to 5 GBaud [43]

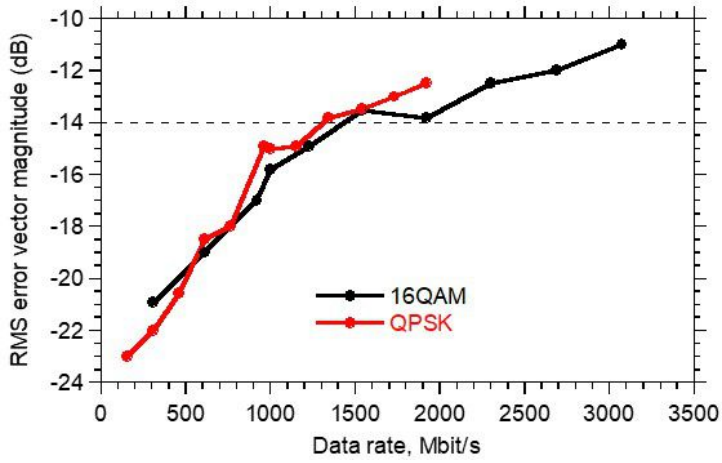


Figure 6.6: Computed error vector magnitude, in dB relative to the constellation's RMS amplitude, as a function of data rate.

6.2.3 Multi-Beam Experiment

The FPGA was then programmed to generate IQ drive signals for the array corresponding to two independent transmitted data streams, aimed at angles of -8^0 and $+2^0$. The FPGA then recognizes these two signals by correlating the received signal against each of the two transmitted data streams. Fig. 6.7 shows the resulting measured radiation pattern in two-beam operation.

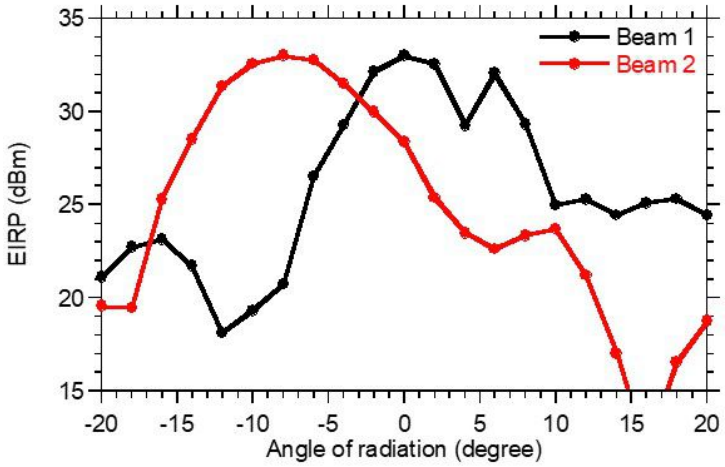


Figure 6.7: Measurement of the array simultaneously transmitting two signal beams, the graph shows the power (EIRP) in each of the two signal beams as a function of the angle of radiation.

Table 6.1: Comparison between state-of-the-art D-band (110-170GHz) multi-channel links and transmitter modules

result	[52]	[47]	[53]	[31]	[54]	[55]	this work
Freq., GHz	148	115-155 135-170	140	113	135	140	135
IC	CMOS	SiGe	CMOS	CMOS	SiGe	CMOS	CMOS, InP HBT
Package	PCB	glass	quartz super-strate	PCB	PCB and lens	PCB	LTCC
Type	1-beam-array	single-channel	1-beam-array	single-channel	2×2 LOS MIMO	MIMO$	MIMO
TX/RX	TX	TX, RX	TX	TX, RX	TX, RX	TX, RX	TX
channels	2	1	8	2	2	4,8,16	8
Psat		13dBm			2.5dBm	2dBm	20.5dBm
EIRP	3.8dBm		32dBm	0dBm	28dBm	17-27	38.5dBm
Data	85Gb/s	36Gb/s 8Gb/s	16Gb/s 18Gb/s	80Gb/s per channel	2× 16Gb/s	6Gb/s	1.3Gb/s 1.9Gb/s
Format	64QAM	64QAM 256QAM	QPSK 64QAM	16QAM	QPSK	16QAM	QPSK 16QAM
EVM		-23dB -30dB	6.25% 5.5%				-13.5dB -13dB
Link	air	WR-6	air	air	air	air	air
Distance	5cm			10cm	6cm	15m	15cm

*calculated. $MIMO-compatible digital beamforming: 1 beam demonstrated

6.2.4 Transmitter Array Summary

Table .6.1 compares state-of-the-art packaged D-band (110-170GHz) transmitters and transmitter/receiver link demonstrations. We report a 8-channel MIMO hub transmitter array tile module using a CMOS frequency conversion ICs, InP HBT power amplifiers, and a microstrip patch antenna array on an LTCC substrate. The module is designed to tile into larger arrays to serve high-data-rate endpoint links to multiple mobile users. Record 38.5dBm EIRP, data transmission, beam steering, and 2-beam operation have been demonstrated. The present results, both beam steering angle and EIRP, are limited

by assembly difficulties; had each of the 8 transmitter channels functioned with the same performance as in [43], the EIRP would have been 46dBm. Modules designed for easier assembly, and with wider-bandwidth baseband connectors, are in fabrication.

6.3 Receiver Array/Tile Demonstration

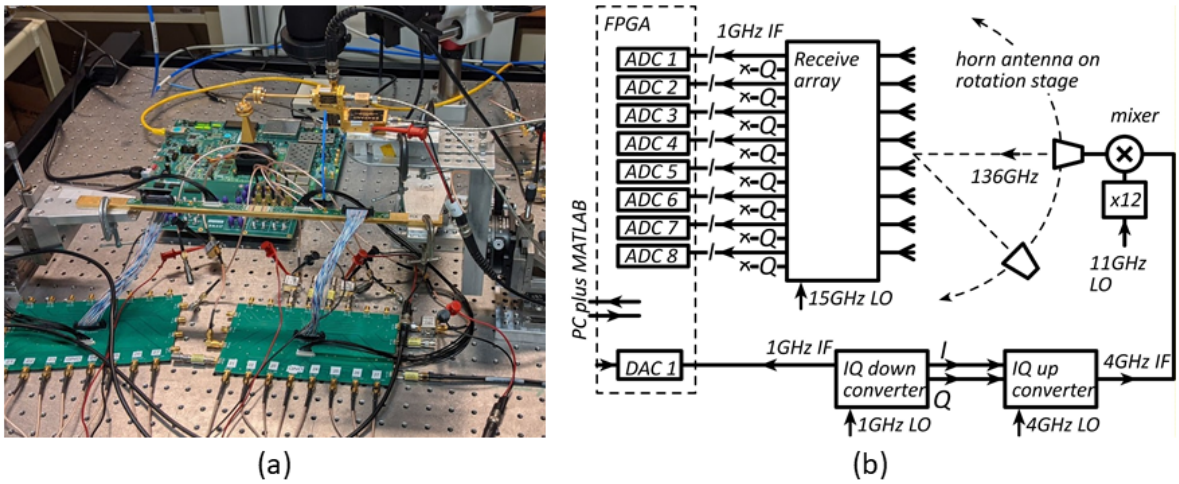


Figure 6.8: Experimental configuration for receiver array characterization. The FPGA generates modulated data on a 1GHz IF, an IQ downconverter and IQ upconverter then convert this to a 4GHz IF, and a mm-wave mixer translates this to 136GHz, with an 128GHz image outside the receiver passband. The test transmitter is mounted on a rotation stage 15cm from the array. The receiver array generates 1GHz IF signals, at quadrature phase between I and Q; the I-signals are captured by the FPGA.

To test the receiver array (Fig. 6.8), a PC running MATLAB generates a numerical description of a 1GHz bandwidth OFDM waveform and transfers it to an FPGA, which generates the analog waveform on a 1GHz IF. An IQ downconverter (ADI ADL5380) and upconverter (ADI ADL5375) then shift the signal to a 4GHz IF. The signal is them mixed against a 132GHz LO to generate a 136GHz drive signal, plus an 128GHz image response that lies outside the receiver passband. A horn antenna, on a rotation stage at 15cm range, illuminates the array with the 136GHz drive signal. If the receiver were to convert its signals to baseband, then its 16 IQ outputs would have to be digitized, yet the

FPGA only has eight ADCs. Instead, the receiver array LO is offset so that its outputs are at a 1GHz IF. The quadrature phase outputs are then redundant, and the eight array channels are monitored by the eight FPGA DACs. Note that two eight-channel receiver modules were constructed; both have assembly defects.

6.3.1 Receiver Array Radiation pattern

Two eight-channel receiver modules were constructed; both have assembly defects. In one, four of the eight channels function, resulting in a 4-element array at 1.3λ pitch. In the second, all eight channels function, but excessive DC supply lead resistance prevents proper biasing for high-data-rate operation. Fig. 5.32 shows the gain, versus received power, for the channels on the 4-channel module.

To form and aim beams, the array must be calibrated, i.e. differences between channel gains and phases are measured and then corrected for. Given the significant differences between channel gains, only phase errors were calibrated. Device drivers and calibration procedures were adapted from Pi-Radio open-source code [50] [51]. These first measure the per-channel fractional timing offsets of the received data streams and the channel-channel variations in the signal phase. The resulting calibration factors are applied to the receiver output signals to perform beamforming and data transmission experiments.

Having calibrated the arrays, radiation patterns were then generated for the 4-element and 8-element arrays (Fig. 6.9). In each measurement, the illuminating horn antenna is positioned at some particular angular of incidence, and the array then computes the received power as a function of direction. This demonstrates digital beamforming. The 4-element array (Figure 6a) shows 12^0 3-dB H-plane (horizontal) beam width, but, because of the 1.3λ element spacing, only 20^0 angular steering range before the appearance of

grating lobes. The 8-element array shows 12^0 3-dB H-plane (horizontal) beam width and over 56^0 angular steering range.

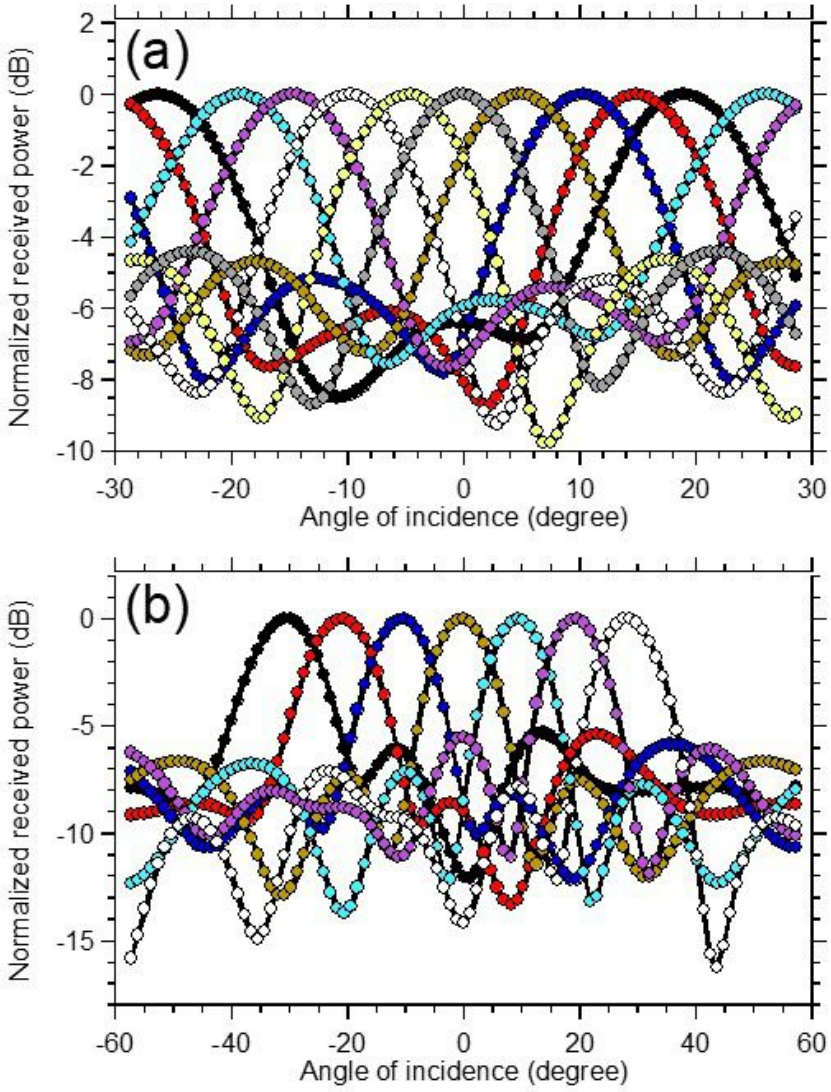


Figure 6.9: Measured array patterns for (a) the four-channel receiver, taken with the test transmitter located at nine different angular positions and (b) the eight-channel receiver, taken with the test transmitter located at seven different angular positions.

6.3.2 Receiver Array Wireless Link

Fig. 6.10 shows data transmission experiments. The data is transmitted using OFDM, with 960 kHz subcarrier spacing. In single-beam operation, there is -15.7dB RMS error vector magnitude in 1.34Gb/s QPSK transmission, and -15.6dB error vector magnitude in 1.92Gb/s 16QAM transmission.

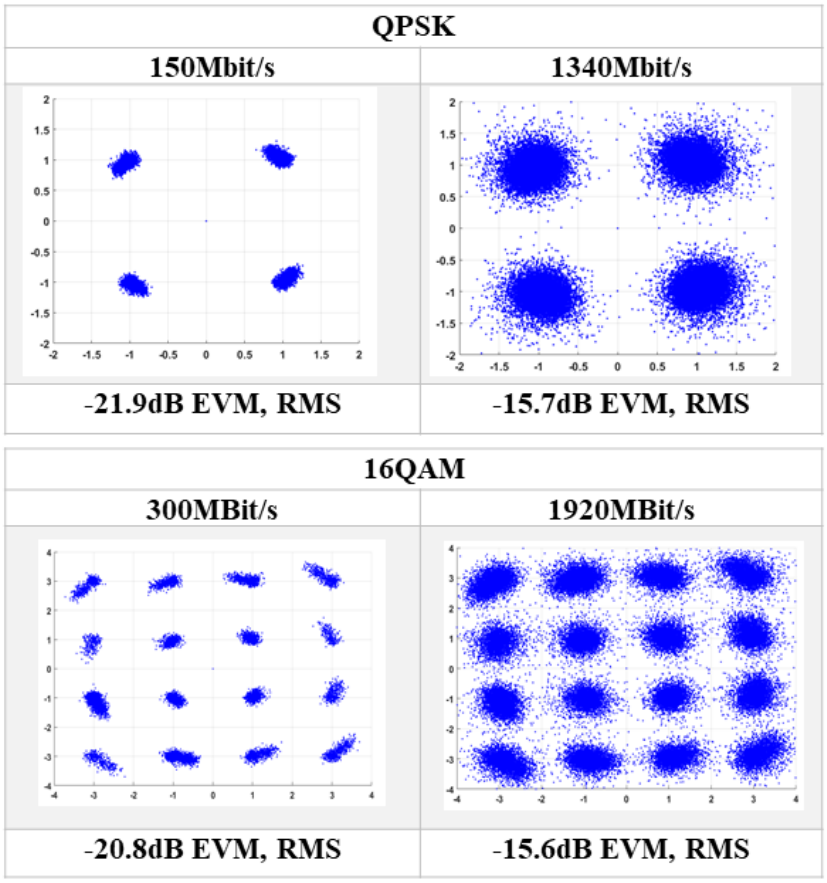


Figure 6.10: Measured receiver QPSK and 16QAM modulation constellations and computed error vector magnitude.

Fig. 6.11 shows the error vector magnitude as a function of data rate. Similar to the transmitter module, data rates are limited both by the FGPA sample rate and by the bandwidth of the multi-pin baseband IQ signal connectors. The measured EVM

is due to the combined noise and non-linearity of ; the packaged receiver module, the commercial of the shelf receiver, and ADI IQ modulators and demodulators (ADL5375 and ADL5380).

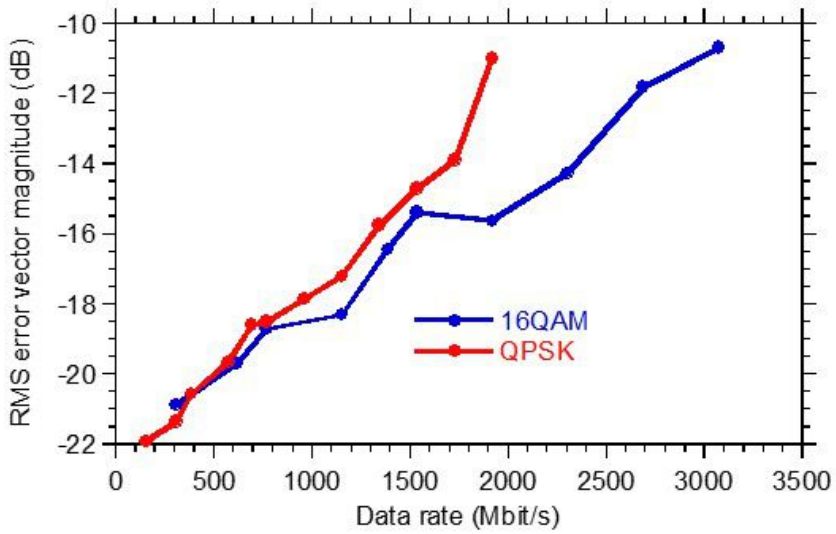


Figure 6.11: Computed error vector magnitude, in dB relative to the constellation's RMS amplitude, as a function of data rate.

6.3.3 Receiver Array Summary

Table. 6.2 compares state-of-the-art packaged D-band (110-170GHz) multi-channel receivers and transmitter/receiver link demonstrations. We report a 8-channel MIMO hub receiver array tile module using CMOS receivers and a microstrip patch antenna array on an LTCC substrate. The module is designed to tile into larger arrays to serve high-data-rate endpoint links to multiple mobile users. Digital beamforming has been is demonstrated with the arrays, showing 12^0 3-dB beam width and 56^0 angular steering range, and data transmission has been demonstrated at up to 1.92Gb/s. With the construction of several of these modules, high-capacity D-band MIMO hub receivers should be feasible.

Table 6.2: Comparison between state-of-the-art multi-channel receiver modules at D-frequency band (110-170GHz)

Result	[31]	[54]	[55]	[56]	This work
Freq, GHz	113	135	140	130-170	140
IC	CMOS	SiGe	CMOS	SiGe	CMOS
Package	PCB	PCB and lenses	PCB	Glass	LTCC
Type	single channel	2×2 LOS MIMO	MIMO$	single-beam-array	MIMO
TX/RX	TX,RX	TX, RX	TX, RX	TX, RX	RX
channels	2	2	4, 8,16	8*	4 (8)
Data	80Gb/s per channel	2×16Gb/s	6Gb/s		2Gb/s 3Gb/s
Format	16QAM	QPSK	16QAM		QPSK 16QAM
EVM					-15.7dB -15.6dB
Link	air	air	air		air
Distance	10cm	6cm	15m		15cm

$MIMO-compatible digital beamforming: 1 beam demonstrated *No experimental data shown for the array.

Chapter 7

Conclusions and Future Work

This thesis introduced fully packaged D-band (135GHz) MIMO arrays for multiuser communications. Those arrays can be utilized in a broad range of applications targeting very high data rates and high-capacity wireless systems. We started our efforts by analyzing a few potential architectures for mm-wave multiuser massive MIMO. We compared between those architectures from the linearity perspective and illustrated why we pursued the all-digital architecture. Then, we show our procedures in building broadband transmitters and receivers using the low-cost CMOS technology (GF 22FDSOI). Next, we explored two different packaging technologies and fabricated tiles using low-cost PCB and ceramic interposers. We illustrated the pros and cons of each packaging technology. Finally, we built transmitter and receiver arrays in tiles and used those tiles to demonstrate wireless links at 135GHz.

Future directions and efforts include building the same transmitter and receiver arrays using cheaper packaging technologies and replacing the copper pillars with C4 bumps. Despite the outstanding performance of the copper pillars and the exceptionally low transition loss (¡1dB) of this technology, it proved hard to assemble and need tiresome

protective measures to secure landing the pillars at the right location during the assembly process.

In our wireless link measurements, the maximum data rate was limited by the baseband connectors. This low bandwidth connector will be replaced in the second generation of our MIMO tiles. Also, we demonstrate a wireless link for a single transmitter and single receiver tile. Future directions include cascading multiple tiles to cover a longer distance and support a higher data rate.

Bibliography

[1] M. J. W. Rodwell, "100-340GHz Spatially Multiplexed Communications: IC, Transceiver, and Link Design," 2019 IEEE 20th International Workshop on Signal Processing Advances in Wireless Communications (SPAWC), 2019, pp. 1-5

[2] M. J. Rosker and H. B. Wallace,"Imaging Through the Atmosphere at Terahertz Frequencies," 2007 IEEE/MTT-S International Microwave Symposium, 2007, pp. 773-776

[3] www.ericsson.com/en/mobility-report.

[4] Rachid El Hattachi and Javan Erfanian. 5G White Paper. Tech. rep.

[5] J. Salz and S. B. Weinstein,"Fourier transform communication system",(New York, NY, USA), Association for Computing Machinery, 1969.

[6] R. Gallager, "Low-density parity-check codes," IRE Transactions on Information Theory vol. 8, no. 1, pp. 21-28, 1962.

[7] A. Simsek, S. Kim and M. J. W. Rodwell, "A 140 GHz MIMO Transceiver in 45 nm SOI CMOS," 2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2018, pp. 231-234

[8] S. Li and G. M. Rebeiz, "A 134-149 GHz IF Beamforming Phased-Array Receiver Channel with 6.4-7.5 dB NF Using CMOS 45nm RFSOI," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2020, pp. 103-106

[9] A. Townley et al., "A Fully Integrated, Dual Channel, Flip Chip Packaged 113 GHz Transceiver in 28nm CMOS supporting an 80 Gb/s Wireless Link," 2020 IEEE Custom Integrated Circuits Conference (CICC), 2020, pp. 1-4

[10] T. L. Marzetta, "Massive MIMO: An Introduction," in Bell Labs Technical Journal, vol. 20, pp. 11-22, 2015

[11] A. A. Farid, M. Abdelghany, U. Madhow and M. J. W. Rodwell, "Dynamic Range Requirements of Digital vs. RF and Tiled Beamforming in mm-Wave Massive MIMO," 2021 IEEE Radio and Wireless Symposium (RWS), 2021, pp. 46-48

[12] M. Abdelghany, A. A. Farid, U. Madhow and M. J. W. Rodwell, "Towards All-digital mmWave Massive MIMO: Designing around Nonlinearities," 2018 52nd Asilomar Conference on Signals, Systems, and Computers, 2018, pp. 1552-1557

[13] H. Moody, "The systematic design of the Butler matrix," in IEEE Transactions on Antennas and Propagation, vol. 12, no. 6, pp. 786-788, November 1964

[14] Y. Gao, M. Khaliel, F. Zheng and T. Kaiser, "Rotman Lens Based Hybrid Analog–Digital Beamforming in Massive MIMO Systems: Array Architectures, Beam Selection Algorithms and Experiments," in IEEE Transactions on Vehicular Technology, vol. 66, no. 10, pp. 9134-9148, Oct. 2017

[15] M. Abdelghany, U. Madhow and A. Tölli, "Beamspace Local LMMSE: An Efficient Digital Backend for mmWave Massive MIMO," 2019 IEEE 20th International Workshop on Signal Processing Advances in Wireless Communications (SPAWC), 2019, pp. 1-5

[16] M. Abdelghany, A. A. Farid, M. E. Rasekh, U. Madhow and M. J. W. Rodwell, "A design framework for all-digital mmWave massive MIMO with per-antenna nonlinearities," in IEEE Transactions on Wireless Communications, doi: 10.1109/TWC.2021.3069378.

[17] M. Abdelghany, M. E. Rasekh and U. Madhow, "Scalable Nonlinear Multiuser Detection for mmWave Massive MIMO," 2020 IEEE 21st International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)

[18] M. Abdelghany, U. Madhow and M. Rodwell, "An Efficient Digital Backend for Wideband Single-Carrier mmWave Massive MIMO," 2019 IEEE Global Communications Conference (GLOBECOM), 2019, pp. 1-6

[19] M. Sadegh Dadash, S. Bonen, U. Alakusu, D. Harame and S. P. Voinigescu, "DC-170 GHz Characterization of 22nm FDSOI Technology for Radar Sensor Applications," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), 2018, pp. 158-161

[20] Z. Wang, P. Chiang, P. Nazari, C. Wang, Z. Chen and P. Heydari, "A CMOS 210-GHz Fundamental Transceiver With OOK Modulation," in IEEE Journal of Solid-State Circuits, vol. 49, no. 3, pp. 564-580, March 2014, doi: 10.1109/JSSC.2013.2297415.

[21] Deferm, N., Reynaert, P. Differential and common mode stability analysis of differential mm-wave CMOS amplifiers with capacitive neutralization. Analog Integr Circ Sig Process 80, 1–12 (2014). https://doi.org/10.1007/s10470-014-0295-z

[22] Behzad Razavi. 2011. RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series) (2nd. ed.). Prentice Hall Press, USA.

[23] Heller, E. Cohen and E. Socher, "A 102–129-GHz 39-dB Gain 8.4-dB Noise Figure I/Q Receiver Frontend in 28-nm CMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 5, pp. 1535-1543, May 2016, doi: 10.1109/TMTT.2016.2547390.

[24] Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin and G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS," 2014 IEEE Radio Frequency Integrated Circuits Symposium, Tampa, FL, 2014, pp. 365-368.

[25] C. J. Lee et al., "A 120 GHz I/Q Transmitter Front-end in a 40 nm CMOS for Wireless Chip to Chip Communication," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, 2018, pp.192-195

[26] S. Jameson and E. Socher, "A Wide-Band CMOS to Waveguide Transition at mm-Wave Frequencies With Wire-Bonds," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 9, pp. 2741-2750, Sept. 2015

[27] S. Jameson and E. Socher, "A 67-110GHz CMOS to WR-10 waveguide transition using wirebonds and wideband microstrip launcher," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), 2014, pp. 1-4

[28] A. Simsek, A. S. H. Ahmed, A. A. Farid, U. Soylu and M. J. W. Rodwell, "A 140GHz Two-Channel CMOS Transmitter Using Low-Cost Packaging Technologies," 2020 IEEE Wireless Communications and Networking Conference Workshops (WCNCW), 2020, pp. 1-3

[29] A. Simsek et al., "A 146.7 GHz Transceiver with 5 GBaud Data Transmission using a Low-Cost Series-Fed Patch Antenna Array through Wirebonding Integration," 2020 IEEE Radio and Wireless Symposium (RWS), 2020, pp. 68-71

[30] E. Naviasky, L. Iotti, G. LaCaille, B. Nikolić, E. Alon and A. Niknejad, "14.1 A 71-to-86GHz Packaged 16-Element by 16-Beam Multi-User Beamforming Integrated Receiver in 28nm CMOS," 2021 IEEE International Solid- State Circuits Conference (ISSCC), 2021, pp. 218-220

[31] A. Townley et al., "A Fully Integrated, Dual Channel, Flip Chip Packaged 113 GHz Transceiver in 28nm CMOS supporting an 80 Gb/s Wireless Link," 2020 IEEE Custom Integrated Circuits Conference (CICC), 2020, pp. 1-4

[32] amkor.com/technology/copper-pillar/

[33] M. Sawaby, N. Dolatsha, B. Grave, C. Chen and A. Arbabian, "A Fully Packaged 130-GHz QPSK Transmitter With an Integrated PRBS Generator," in IEEE Solid-State Circuits Letters, vol. 1, no. 7, pp. 166-169, July 2018

[34] global.kyocera.com/prdct/semicon/material/

[35] C. Balanis , Antenna Theory: Analysis and Design. Wiley, fourth ed., 2016.

[36] www.pasternack.com/t-calculator-microstrip-ant.aspx

[37] A. S. H. Ahmed, A. A. Farid, M. Urteaga and M. J. W. Rodwell, "204GHz Stacked-Power Amplifiers Designed by a Novel Two-Port Technique," 2018 13th European Microwave Integrated Circuits Conference (EuMIC), 2018, pp. 29-32

[38] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter and M. J. W. Rodwell, "A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology," 2020 15th European Microwave Integrated Circuits Conference (EuMIC), 2021, pp. 1-4

[39] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter and M. J. W. Rodwell, "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 492-495

[40] J. R. James, P. S. Hall, and C. Wood. Microstrip Antenna Theory and Design. The Institution of Electrical Engineers, London, U. K., 1981.

[41] A. A. Farid, A. Simsek, A. S. H. Ahmed and M. J. W. Rodwell, "A Broadband Direct Conversion Transmitter/Receiver at D-band Using CMOS 22nm FDSOI," 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2019, pp. 135-138

[42] A. A. Farid, A. S. H. Ahmed, A. Simsek, M. J. W. Rodwell, "A Packaged 135GHz 22nm FD-SOI Transmitter on an LTCC Carrier" IEEE International Microwave Symposium (IMS),2021, 6-11 June, Atlanta and virtual

[43] A. A. Farid, A. S. H. Ahmed, A. Simsek, M. J. W. Rodwell,"A 27.5dBm EIRP D-Band Transmitter Module on a Ceramic Interposer", IEEE Radio-Frequency IC Symposium (RFIC),2021, 7-9 June, Atlanta and virtual.

[44] A. A. Farid, A. S. H. Ahmed, A. Dhanajay, M. J. W. Rodwell "An 8-Channel 135GHz CMOS/InP/LTCC MIMO Transmitter Array Tile Module with 38.5dBm EIRP" 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021

[45] A. A. Farid, A. S. H. Ahmed, A. Dhanajay, M. J. W. Rodwell "135GHz CMOS / LTCC MIMO Receiver Array Tile Modules" 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021

[46] M. Ito, T. Okawa and T. Marumoto, "D-band Transceiver Utilizing 70-nm GaAs-mHEMT Technology for FDD System," 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), Nashville, TN, USA, 2019, pp. 1-4

[47] A. Singh et al., "A D-Band Radio-on-Glass Module for Spectrally-Efficient and Low-Cost Wireless Backhaul," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Los Angeles, CA, USA, 2020, pp. 99-102

[48] S. Carpenter, D. Nopchinda, M. Abbasi, Z. S. He, M. Bao, T. Eriksson, and H. Zirath, "A D-Band 48-Gbit/s 64-QAM/QPSK Direct-Conversion I/Q Transceiver Chipset," IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 4, pp. 1285–1296, April 2016.

[49] S. H. Mirfarshbafan, A. Gallyas-Sanhueza, R. Ghods and C. Studer, "Beamspace Channel Estimation for Massive MIMO mmWave Systems: Algorithm and VLSI Design," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 5482-5495, Dec. 2020

[50] github.com/pi-radio/Pi-Radio-v1-NRT

[51] dl.acm.org/doi/abs/10.1145/3411276.3412195

[52] A. Hamani, F. Foglia-Manzillo, A. Siligaris, N. Cassiau, B. Blampey, F. Hameau, C. Dehos, A. Clemente, J. L. Gonzalez-Jimenez, "An 84.48 Gb/s CMOS D-band Multi-Channel TX System-in-Package", IEEE Radio-Frequency IC Symposium (IMS). 7-9 June, Atlanta and virtual

[53] S. Li, Z. Zhang, B. Rupakula and G. M. Rebeiz "An Eight-Element 140 GHz Wafer-Scale Phased-Array Transmitter with 32 dBm Peak EIRP and ¿ 16 Gbps 16QAM and 64QAM Operation", 2021 IEEE/MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, 2021.

[54] M. Sawaby et al., "A Fully Integrated 32 Gbps 2x2 LoS MIMO Wireless Link with UWB Analog Processing for Point-to-Point Backhaul Applications," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2020, pp. 107-110

[55] S. Abu-Surra et al., "End-to-end 140 GHz Wireless Link Demonstration with Fully-Digital Beamformed System," 2021 IEEE International Conference on Communications Workshops (ICC Workshops), 2021, pp. 1-6

[56] M. Elkhouly et al., "D-band Phased-Array TX and RX Front Ends Utilizing Radio-on-Glass Technology," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2020

[57] M. Rodwell et al., "100-300GHz Wireless: ICs, Arrays, and Systems," 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021

[58] M. Seo et al., "A 200 GHz InP HBT Direct-Conversion LO-Phase-Shifted Transmitter/Receiver with 15 dBm Output Power," 2021 IEEE International Microwave Symposium (IMS), 2021, 6-11 June, Atlanta and virtual