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Schottky Diode Integrated Circuits for Sub-Millimeter-Wave Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philisophy
in
Electrical and Computer Engineering
by
Scott Thomas Allen

Committee in charge:

Professor Mark Rodwell, Chairperson
Professor Steve Long
Professor Umesh Mishra
Professor Robert York

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The dissertation of Scott Thomas Allen
is approved:

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_____
Committee Chairperson

July 29, 1993

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Vita

- June 21, 1965: born in Long Beach, California
- May, 1987: B.S., with distinction, Electrical Engineering, Cornell University
- February, 1989: M.S., Electrical and Computer Engineering, University of Massachusetts, Amherst
- 1987-1990: Design Engineer at the General Electric (now Martin Marietta) Electronics Laboratory in Syracuse, NY
- August 4, 1990: married Sheri DeFrees
- 1990-1994: Research Assistant, Department of Electrical and Computer Engineering, U.C. Santa Barbara

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Abstract

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by
Scott Thomas Allen

Using Schottky varactor diodes on GaAs, sampling circuits with bandwidths of 725 GHz have been fabricated and measured. The sampling circuits are integrated with nonlinear transmission lines, which are traveling-wave structures that generate the subpicosecond electrical pulses necessary to strobe the sampling circuits. This bandwidth was obtained by combining a number of technologies had been developed: varactor diodes with RC cutoff frequencies above 4 THz, coplanar waveguide transmission lines with the center conductor elevated off the substrate, and ways of minimizing all parasitics. Other applications of these technologies include a 100 Gbit/sec mux/demux circuit and 200 GHz traveling wave amplifiers.

By applying what had been learned from the varactor diodes, a novel device structure, a Schottky-collector resonant tunneling diode (RTD), was developed in the AlAs/GaAs system. By changing the collector from an ohmic to a Schottky contact, the scaling laws that are used for other devices are now applicable to the RTD. With 0.1 m Schottky fingers, a maximum frequency of oscillation of 900 GHz was attained, more than twice that of a conventional RTD. By applying this technique to AlAs/InGaAs on InP, RTDs with fmax above 2 THz have been tested. The long range goal of the project is to build oscillator arrays for generating power above 1 THz.

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Chapter 1

Introduction

With the recent advances in the performance of high speed transistors [1], device operating bandwidths have increased far beyond the available measuring instrument bandwidth. This limits the ability to understand the high frequency physics of the devices and also makes it difficult to design circuits that can take advantage of their available bandwidth. To overcome this measurement limitation, sampling circuits with bandwidths exceeding those of the fastest transistors are necessary.

The first necessary component of a high frequency sampling circuit is a strobe signal for the sampling bridge that has a pulse width much shorter than the time response of the signal that is being sampled. The technology that enables the electrical generation of subpicosecond pulses is the nonlinear transmission line (NLTL) [2]. An NLTL is formed in an integrated circuit on GaAs by using reverse biased Schottky diodes as nonlinear capacitances to load down a coplanar waveguide transmission line. The variable capacitance of the diodes results in a voltage dependent velocity for waves traveling on the NLTL, and this variable velocity causes the falling edge of a signal to be compressed. The step function generated by the NLTL can then be differentiated to form a pulse, and this pulse is used to strobe the sampling circuits.

The second component of a sampling circuit is the sampling bridge, which can be readily implemented with two Schottky diodes and two holding capacitors [3]. For this part of the circuit, it is the RC cutoff frequency of the diodes that sets the frequency response. The overall sampling circuit bandwidth is the convolution of the aperture time of the strobe pulse generated by the NLTL and the RC time constant of the sampling bridge.

Figure 1.1 shows the historical development of sampling circuit technology.

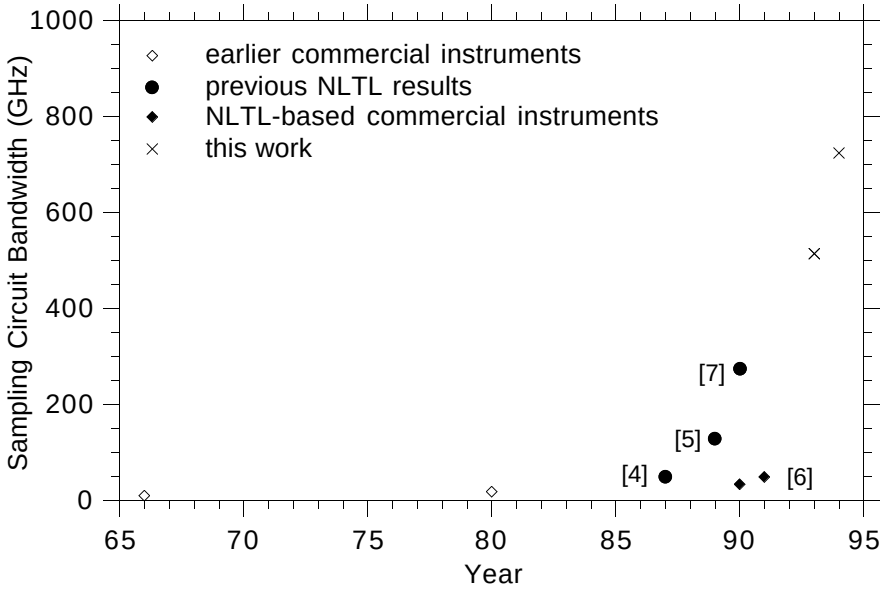

Figure 1.1: Historical development of sampling circuit technology. With the advent of GaAs based NLTLs in 1987, the growth has been rapid, with commercial instruments operating to 50 GHz and prototype instruments demonstrated at 250 GHz.

Prior to the advent of GaAs based NLTLs, sampling circuit bandwidths had remained less than 20 GHz. The first demonstration of NLTLs came in 1987 [4] and since then this technology has been incorporated into commercial instruments that are now available with bandwidths up to 50 GHz [6].

In earlier work on this technology at U.C. Santa Barbara, NLTLs had been used to generate step functions with $10\% - 90\%$ fall times of 1.3 ps [7]. These were combined with sampling circuits that had an overall bandwidth of 250 GHz. These sampling circuits were then used in a variety of high frequency instrumentation systems, including a free space spectroscopy system with 250 GHz bandwidth [8] and a network analyzer system that is capable of calibrated two port measurements to 200 GHz [9].

The purpose of this work was to extend the bandwidth of the sampling circuits so that future generations of the measurement systems can operate well into the sub-millimeter wave frequency range. The first important improvement needed was to increase the RC cutoff frequency of the Schottky diodes that were used in both the NLTLs and the sampling bridge. By changing the doping

profiles of the diodes and scaling down their geometries, a substantial improvement in circuit speed was obtained: the NLTLs produced step functions with $10\% - 90\%$ fall times of 0.68 ps and the sampling circuits had bandwidths of 515 GHz.

In order to extend the bandwidth even further, the other component of the NLTL, the coplanar waveguide, had to be improved. At extremely high frequencies, both the loss of the line and the phase velocity have a significant impact on the edge speed of the step function that is being generated. In order to address both of these issues, a novel coplanar waveguide structure was developed in which the center conductor was elevated off the semiconductor substrate. Often in high speed integrated circuits the interconnections are made with air bridges in order to reduce the capacitive loading of the wiring. This concept was extended even further for the NLTLs by having the center conductor for the entire length of the transmission line suspended above the GaAs in order to simultaneously reduce parasitics, reduce loss, and increase the electrical wavelength of the signals. Coupling this air line technology with the high speed diodes resulted in NLTLs that generated step functions with $10\% - 90\%$ fall times of 0.48 ps and sampling circuits with 725 GHz bandwidth.

The limitation on the edge speed is now believed to be the saturation velocity of the electrons in the GaAs. The pulse formation on the NLTL occurs because the depletion edge of the Schottky diodes moves with changing reverse bias, and with the step functions now being generated, it is the speed at which the depletion edge responds to the applied signal that is determining the edge speed. This limitation can be overcome by using diodes with more heavily doped layers, because the distance that the depletion edge has to move for a given change in bias is inversely proportional to the doping level in the semiconductor. By increasing the doping in the diodes and extending the air bridged coplanar waveguide technique to air bridged microstrip lines, it should be feasible to fabricate 2 THz sampling circuits with only limited further technology development.

As a result of the studies on high frequency Schottky diodes, a new concept for resonant tunneling diodes (RTDs) was developed. It was found that by replacing the ohmic collector contact of the conventional RTD with a Schottky contact, the scaling laws that were used to increase the frequency performance of the varactor diodes could also be applied to RTDs. By scaling the Schottky collector to deep submicron geometries using electron beam lithography, RTDs in the GaAs/AlAs system were fabricated that had a maximum frequency of oscillation of 900 GHz, as computed from the measured dc and microwave parameters. By applying this same technique to the InGaAs/AlAs system on InP, RTDs with oscillation

frequencies as high as 3 THz are expected.

The long range goal of the RTD technology is to fabricate oscillator arrays operating at 1 THz. In order to accomplish this in an integrated circuit environment, the air line technology developed for the NLTLs may be required because parastics can become dominant at such high frequencies. By making the contact to the RTDs with a line suspended in air, the parasitics are minimized because all the fringing fields are in air instead of the substrate, greatly reducing the capacitance. This is another application of the air lines that demonstrates their importance as a technology for integrated circuits in the sub-millimeter wave frequency range.

This dissertation is organized essentially in the chronological order of the development of the work. Chapter 2 discusses the theory of NLTLs and sampling circuits and shows some circuit simulations that were used in their design. Chapter 3 describes the details of the process flow and the dc and microwave characterization of the Schottky diodes. Chapter 4 discusses the initial 515 GHz results and contains an analysis of what the limitations were. Chapter 5 explains the development of the air line technology and the 725 GHz sampling circuits that resulted from it, and chapter 6 contains a discussion of how the frequency response can be further improved. Chapter 7 changes the focus and describes the work on the Schottky-collector RTDs that was an outgrowth of the work on the Schottky varactor diodes discussed in chapter 3. Chapter 8 summarizes the results of this thesis project and outlines the directions of future developments.

Chapter 2

Circuit Analysis and Design

The nonlinear transmission lines and sampling circuits fabricated for this work were integrated together on-wafer, so it was important to develop technology that was applicable to both. The co-integration of the sampling circuits was required because the electrical waveforms generated by the NLTLs had bandwidths far exceeding those of any commercially available test instrument, so it was necessary to also fabricate a measuring circuit with commensurate speed. Secondly, because one of the primary applications of these circuits is in measurement systems, it is the combined response of the NLTL and sampling circuit that is of most significance.

The mathematics of the operation of NLTLs and their limitations was originally worked out by Landauer [10] and later applied to GaAs integrated circuits by Rodwell [2]. The discussion here about the NLTLs and sampling circuits draws heavily from the latter work.

2.1 Nonlinear Transmission Line Theory

NLTLs implemented on GaAs consist of sections of high impedance transmission line periodically loaded with reverse-biased Schottky diodes that provide a voltage-variable capacitance to the system (figure 2.1 (a)). Figure 2.1 (b) shows the equivalent circuit model for the line where L_l and C_l are the inductance and capacitance per unit length of the line, respectively, and C_d and R_s are the capacitance and series resistance of the varactor diodes.

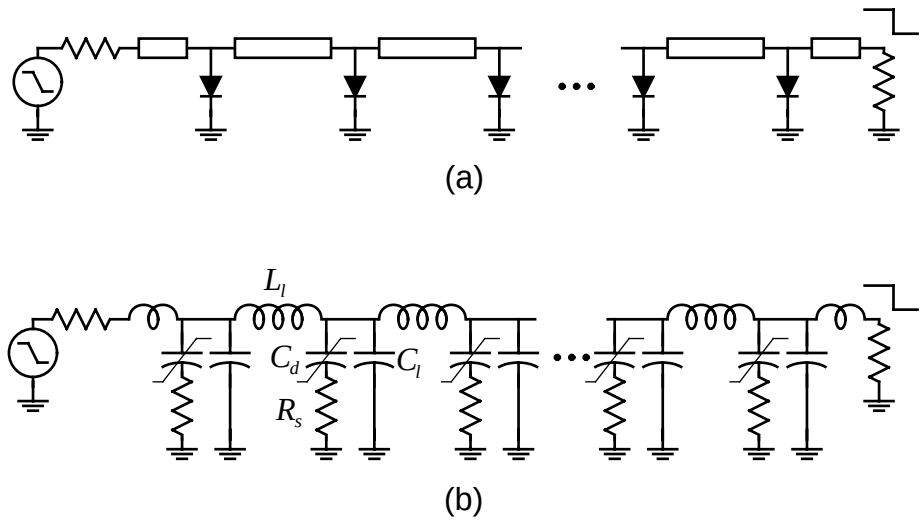

Figure 2.1: (a) Schematic diagram of NLTL. (b) Equivalent circuit model.

2.1.1 Shock Wave Formation

Because the capacitance of the diodes is a function of the voltage across them, the propagation delay of a wave traveling down the line, T_d, is also a function of the voltage:

$$T_d = \sqrt{L_l \cdot [C_l + C_d(V)]} \tag{2.1}$$

It is this dependence of propagation delay on voltage that leads to shock wave formation because the peak of the waveform, V_h, is traveling more slowly than the trough of the waveform, V_l, and so the falling edge of the wave is compressed as it propagates down the line. The SPICE simulation in figure 2.2 shows the evolution of a slow step function into a shock wave as it travels down the NLTL. The total compression of the line, ΔT_d, is defined to be the difference in propagation delays for waves traveling with the minimum and maximum velocities:

$$\Delta T_d = T_d\,(V_h) - T_d\,(V_l) \tag{2.2}$$

The minimum fall time attainable can be derived from energy balance considerations on the transmission line [11] and is limited by the $R_s C_d$ time constant of the Schottky diodes. For diodes with uniform doping the limit is

$$T_{fall}(10\% - 90\%) = \frac{8.8 C_d(0) R_s}{\sqrt{1 - (V_l/\phi_{bi})} - 1} \tag{2.3}$$

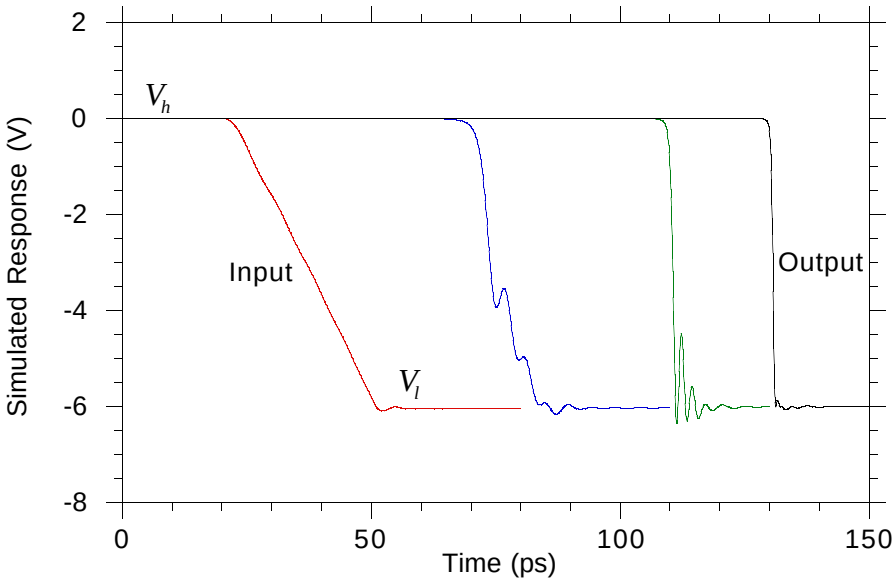

Figure 2.2: SPICE simulation showing the formation of a shock wave as it propagates down the NLTL.

For diodes with a doping level of $N_D = 1.0 \cdot 10^{17}$ cm^{-3}, a Schottky barrier height of $\phi_{bi} = 0.8$ V, and a Schottky contact width of 1 μm, $C_d R_s = 76$ fs and the minimum $T_{fall} = 0.34$ ps. This can be reduced to 0.25 ps by increasing the doping level to $3.0 \cdot 10^{17}$ cm^{-3}; the details of the diode design will be discussed in chapter 3.

A number of useful parameters for the NLTL can be defined in terms of the average capacitance, or large signal capacitance, C_{ls}, that the wave sees over its entire voltage swing:

$$C_{ls} = \frac{1}{V_h - V_l} \int_{V_l}^{V_h} C_d(V) dV \tag{2.4}$$

This leads naturally to a definition for the large signal characteristic impedance of the line, which is the effective loaded impedance of the NLTL under large signal drive:

$$Z_{ls} = \sqrt{\frac{L_l}{C_l + C_{ls}}} \tag{2.5}$$

If $Z_{ls} = Z_{load}$ then the shock wave is passed to the load without reflection or distortion; and similarly, if $Z_{ls} = Z_{gen}$ then the signal from the generator is launched on the NLTL with no reflection.

One of the other limitations on the shock edge speed besides the diode R_sC_d time constant is that because of the periodic nature of the line, there is a Bragg frequency above which energy cannot propagate, analogous to the forbidden electron energy bands in a periodic crystal. The Bragg frequency, f_{Br}, is defined in terms of C_{ls} as [2]

$$f_{Br} = \frac{1}{\pi\sqrt{L_l \cdot (C_l + C_{ls})}} \tag{2.6}$$

The ringing that can be seen on the waveform in figure 2.2 is at f_{Br} because at this frequency all the energy is reflected and strong standing waves form. It is important in the design of the NLTL to keep f_{Br} well above the highest frequency at which there would be any significant energy.

2.1.2 Line Loss

There are two contributions to the loss of an NLTL, the loss from the diodes and the resistive loss in the transmission line. There is no radiation loss because the capacitive loading of the diodes is large enough that the wave veloctiy on the NLTL is slower than it would be in the GaAs so no energy can be coupled into a substrate mode. The loss per section of NLTL is given by:

$$S_{21} = \exp\left[\frac{-\omega^2 C_{ls}^2 R_s Z_{ls}}{2} - \frac{R_l}{2Z_{ls}}\right] \tag{2.7}$$

The first term in the loss expression is the effect of the resistive loading of the diodes. The power loss from a shunt conductance loading on a transmission line, G_{load}, is given by the simple expression $e^{-Z_0 G_{load}}$. In order to calculate the effect of the diode loading on the NLTL, a series to parallel transformation is made to find the real part of the input admittance of the diode, which yields the term $\omega^2 C_{ls}^2 R_s$ in equation 2.7. In order to make this component of the loss small, the RC cutoff frequency of the diode needs to be made high; chapter 3 contains a detailed discussion of this diode optimization.

The second term in the equation for loss on the NLTL is from the resistive loss on the metal transmission line, R_l, which can become quite significant at high frequencies where the skin depth is small. There are a number of design strategies that can be employed to minimize this component of the loss.

The first is to determine an impedance for the unloaded coplanar waveguide (CPW) that will minimize the overall loss. As the intrinsic capacitance of the CPW line becomes small compared to the capacitance of the loading diodes, the

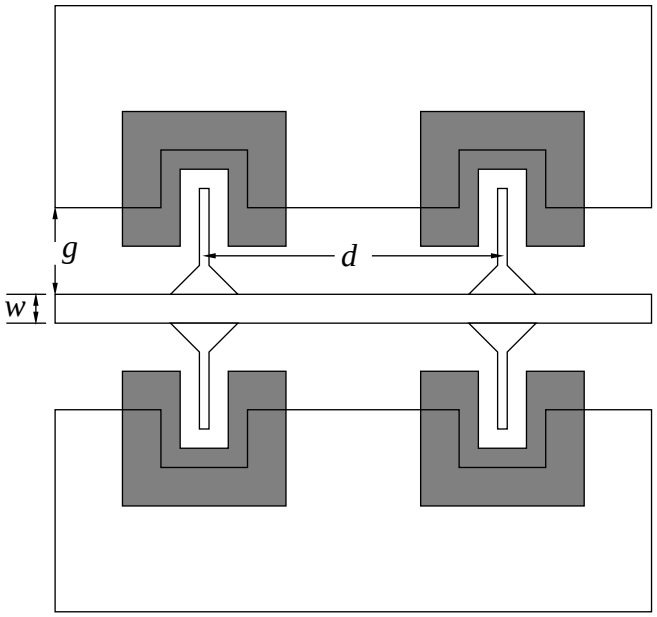

Figure 2.3: Layout of NLTL cell. The length of the cell, d, is reduced to increase f_{Br}, and all other parameters are scaled proportionately.

amount of compression for the wave increases (equation 2.1), so the length of the line decreases. The tradeoff is that as the impedance of the interconnecting sections of transmission lines is increased, the width of the center conductor of the CPW decreases, increasing its resistive loss. It was found in earlier studies that a line impedance of $Z_l = 75\ \Omega$ minimizes the line loss [12].

The second design feature on which to concentrate is the cell layout for each section of the NLTL. Figure 2.3 shows two cells on the NLTL. This figure does not show the cross-over air bridges that tie the two ground planes together because they are not an integral part of the NLTL design but are necessary to prevent unwanted modes from propagating on the ground planes. The inductance and capacitance of the line for each section are $L_l = Z_l d/v_{cpw}$ and $C_l = d/(Z_l v_{cpw})$, where d is the spacing between the diodes and v_{cpw} is the wave velocity on the coplanar line. As d is reduced, the area of the diode is also reduced proportionately to maintain a constant Z_{ls}, and so f_{Br} increases as $1/d$. The tradeoff is that as d is reduced to increase f_{Br}, the horizontal dimensions of the cell must also be decreased to maintain a reasonable length-to-width aspect ratio of $d > (2g + w)$; otherwise, the sections of interconnecting metal could not legitimately be modeled as sections of transmission line.

In coplanar waveguide, the line impedance is a function of the ratio of the center conductor width to the separation between the ground planes, and on GaAs is given by [13]:

$$Z_l = 11.3\Omega \cdot \ln\left(2\frac{1+\sqrt[4]{1-k^2}}{1-\sqrt[4]{1-k^2}}\right) \tag{2.8}$$

where $k = w/(w+2g)$, so as g decreases, w must decrease proportionately and the resistive loss in the center conductor goes up. Because of this tradeoff between R_l and f_{Br}, the correct design strategy is to make f_{Br} no higher than is necessary for each cell. At the input end of the line, where the harmonic content of the shock wave is relatively low, f_{Br} can also be low and so the cell can be large. The cell size can then be tapered along the line to accommodate the increasing harmonics of the shock wave, and thus the center conductor is never any narrower than necessary and R_l is minimized. The edge speed of the shock wave on the line decreases in proportion to the distance it has travelled, so the harmonic content of the signal is increasing at the inverse of this. In order to accomodate this the Bragg frequency of the NLTL is increased exponentially down the line.

Reducing loss on the NLTL is extremely important because the effect is more than just to decrease the amplitude of the signal on the line. A more subtle effect, but one that can be even more detrimental to the edge speed of the shock wave, is that as the amplitude decreases, the peak of the wave is no longer near 0 V. This is illustrated by figure 2.4 which shows how the signal decays and remains centered about the negative dc bias applied to the line. The problem with this is that the region of strong nonlinearity for the diodes is near 0 V (figure 2.5), so as the size of the signal decreases, the compression on the line is also reduced because the fractional change in capacitance seen by the signal is smaller. To compensate for this loss in compression, the NLTL must be made longer, which compounds the problem.

2.2 NLTL Design

The first shock lines designed for this work were based on diodes with 1 μm wide Schottky contacts and a doping of $N_D = 1.0 \cdot 10^{17}$ cm^{-3}. These diodes had a reverse breakdown voltage of -12 V and a 3:1 change in capacitance for reverse bias swing of 0 to -6 V; the details of the diode design will be discussed in the next chapter. The CPW used for the interconnects was chosen to be 75 Ω in

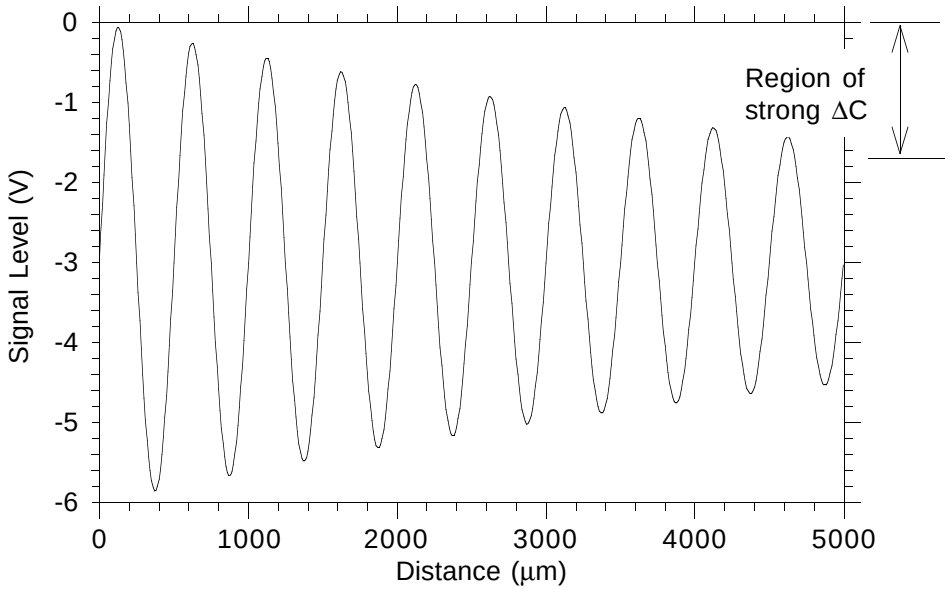

Figure 2.4: The loss on the line results in the signal not swinging all the way to 0 V, so the strong nonlinearity of the diodes in this region is not seen.

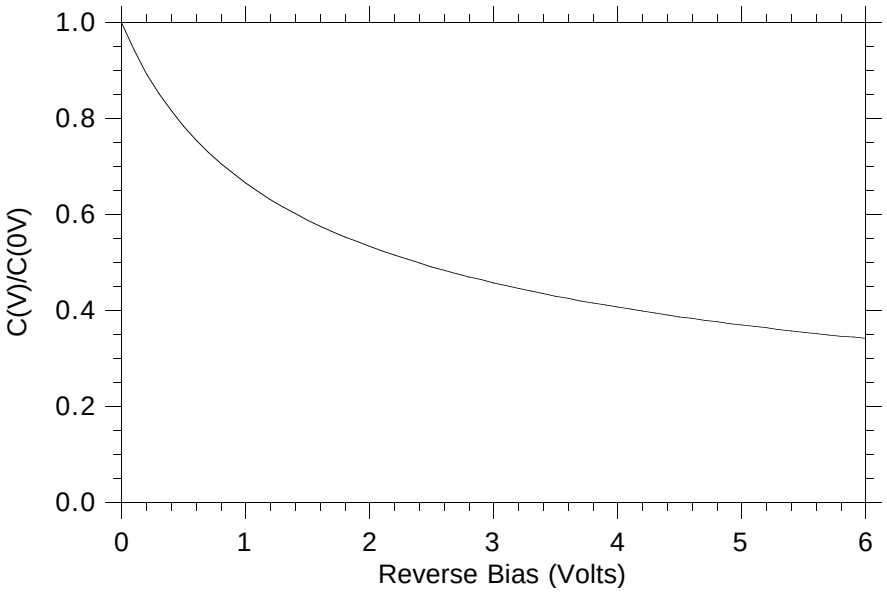

Figure 2.5: Reverse bias C-V characteristics of a uniformly doped diode showing that the capacitance varies most rapidly near 0 V.

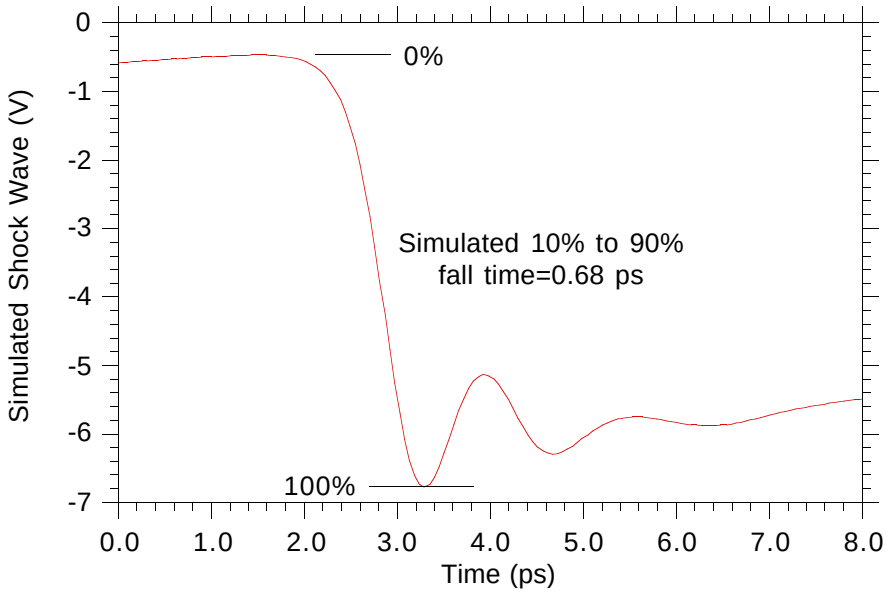

Figure 2.6: SPICE simulation of the designed NLTL showing an output fall time of 0.68 ps.

order to minimize the power loss on the NLTL from the metallic losses in the center conductor. In order to keep the lines short to further reduce loss, a drive frequency of 30 GHz was chosen because the faster the fall time of the input signal, the less compression the lines need. The Bragg frequency was tapered exponentially from an initial value of 250 GHz to a final value of 800 GHz at the output end of the line. The large signal impedance of the line was chosen to be 40 Ω. This is close enough to the 50 Ω system impedance that power loss due to mismatch is negligible, 2%, but has the advantage of increasing the compression of the line by the ratio 50/40. Appendix A contains the computer program that was used to generate the SPICE file and the layout file for these lines. The simulated waveform from SPICE, shown in figure 2.6, has $T_{fall} = 0.68$ ps.

2.3 Sampling Circuits

The sampling circuits were designed to be as synergistic with the NLTLs as possible. The samplers consist of three components: a two-diode sampling bridge, a balun/differentiator, and an NLTL strobe pulse generator. The resistors in the samplers were designed using the $N+$ buried layer of the Schottky diodes and

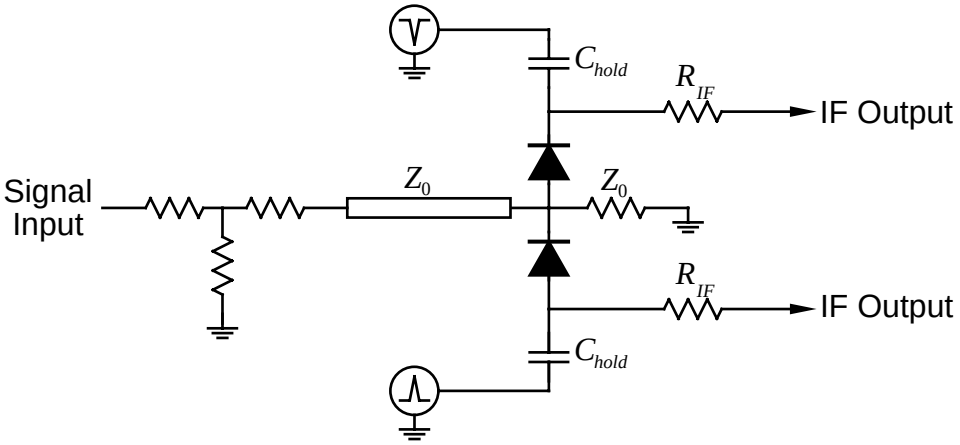

Figure 2.7: Schematic diagram of two diode sampling bridge.

the capacitors were implemented with reverse biased diodes, so no new mask layers were required.

Figure 2.7 is a schematic diagram of the two diode sampling bridge. The input signal is first attenuated to a level compatible with diode sampling and is then applied through a 50 Ω transmission line to the node between the two sampling diodes, which are normally off, and is terminated with a 50 Ω load. When the diodes are momentarily driven into forward conduction by the symmetric strobe pulses, the input signal partially charges the hold capacitors. If the repetition frequency of the input signal is a multiple of the strobe frequency, at each successive strobe interval the sampling diodes will further charge the holding capacitors and cause the output voltage, sampled through the IF resistors, to asymptotically approach that of the input voltage. If the repetition frequency of the strobe signal is offset from that of the test signal by Δf, then the sampled waveform is mapped out in equivalent time at a repetition rate of Δf.

The strobe pulse for the sampling circuits is generated using the output of an NLTL and a balun/differentiator network. A balun is a network that converts a balanced signal to an unbalanced one and vice versa and is required here because symmetric positive and negative strobe pulses are needed to gate the sampling diodes. A differentiator is needed to convert the step function output of the NLTL into a pulse. Figure 2.8 shows the layout of the circuit that accomplishes both of these functions.

The NLTL implemented in CPW intersects a coplanar strip line (CPS) at a right angle. The ground planes of the CPW are connected to one conductor of the CPS and the center conductor of the CPW is connected through a 50 Ω load

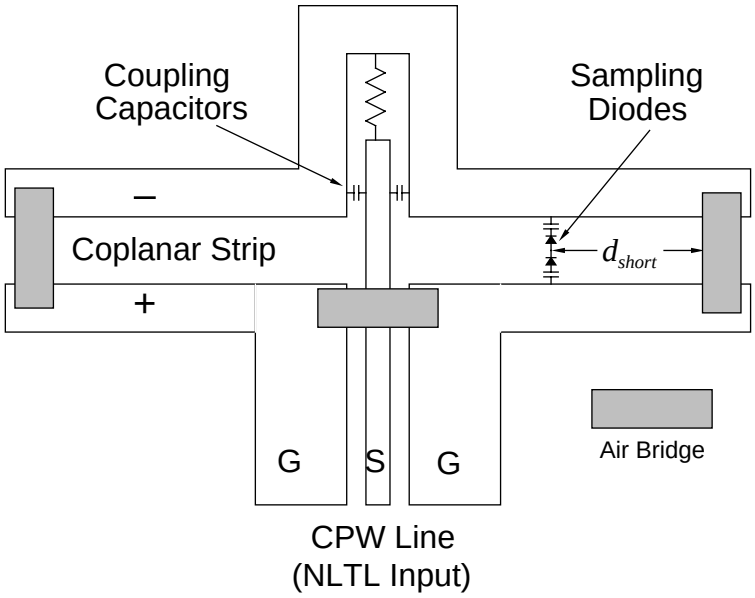

Figure 2.8: Balun/differentiator circuit that is used to convert the step function of an NLTL into symmetric strobe pulses for the sampling diodes.

to the other conductor of the CPS. The CPS lines are shorted at equal distances from the CPW center conductor so that the CPW line is loaded symmetrically.

The simplest way to analyze the circuit is to look at the two constituent pieces independently. First consider the balun network that couples the CPW signal to the balanced CPS line. The shorted lines are acting as inductive stubs in the ground planes of the CPW and the CPS modes are generated by the return currents of the CPW. The schematic diagram of this is shown in 2.9 (a) and the equivalent circuit model for is shown in figure 2.9 (b). From the equivalent circuit, the amplitude of the pulse across the stubs can be found:

$$V_{pulse} = \frac{Z_{stub}/2}{R_{gen} + Z_O + Z_{stub}/2} V_{gen} \tag{2.9}$$

Since it is difficult to make the impedance of CPS line on GaAs much higher than 100 Ω, the amplitude of the pulse is limited to 1/3 of V_{gen}. By adding the coupling capacitor C_c to the network, high frequency signals bypass the load resistor and the voltage of the pulse is increased. The value of C_c is determined using SPICE to simulate the sampling circuit and is chosen as a compromise between the size of the strobe pulse and the size of the reflection back to the NLTL.

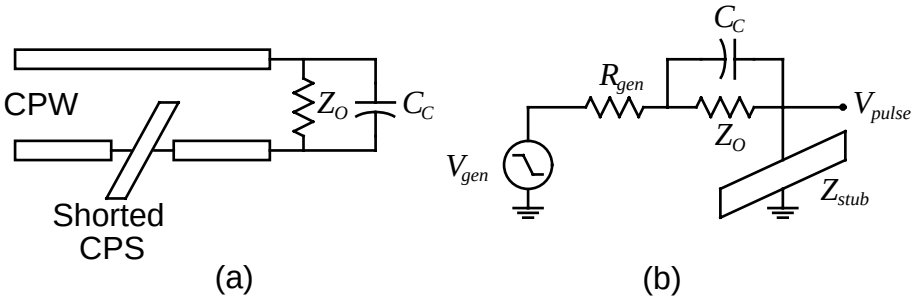

Figure 2.9: (a) Schematic diagram of the balun showing the CPS as an inductive stub in the CPW ground return. (b) Equivalent circuit.

To understand the differentiation, consider the CPS lines alone. Since they are short circuited, the forward traveling step functions are reflected back with reversed polarities and pulses are formed by the superposition of the forward and reflected waves. With the short placed at a distance d_{short} away from the plane of the sampling diodes, an impulse is generated at the diodes of a duration equal to the round-trip delay $t_{rt} = 2d_{short}/v_{cpw}$. Because the CPS lines are terminated in the 50 Ω of the NLTL, multiple strobe pulses do not occur.

The sampling bridge and the differentiator are combined into a compact layout by using the ground planes of the CPW signal line as the coplanar strip lines for the strobe signal. Using reverse biased diodes for the hold and coupling capacitors and air bridges for the crossovers, as shown in figure 2.10, the entire sampling circuit can be implemented in a layout that is suitable for use with sub-millimeter waves.

The sampling circuit rise time is determined by the signal line RC time constant and the aperture time of the strobe pulse. The two sampling diodes load the signal line in parallel, so the 10% to 90% rise time is

$$T_{RC} = 2.2 \cdot \left(\frac{Z_0 + R_s}{2} \right) \cdot 2C_d \tag{2.10}$$

The aperture time is determined by a combination of the fall time of the shock wave from the NLTL, the round trip delay of the shorted-line differentiating network, the sampling diode capacitance, and the amount of reverse bias on the sampling diodes. The round-trip time of the differentiator should be approximately equal to the fall time of the shock wave. Larger round-trip times broaden the strobe pulse while shorter times reduce the amplitude without significantly reducing the impulse duration.

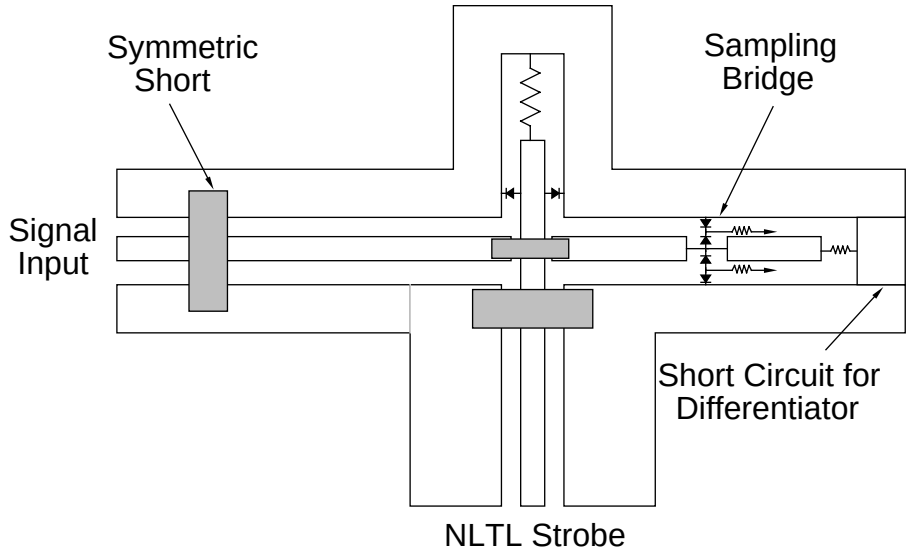

Figure 2.10: The sampling bridge and differentiator are combined in a compact layout that is suitable for use with sub-millimeter waves.

In the absence of sampling diode parasitics to broaden the strobe pulse duration, it will have a full width at half maximum, FWHM, equal to the NLTL output fall time. Increasing the diode reverse bias decreases the duration of the forward conduction, and with a reverse bias that approaches the peak amplitude of the strobe pulse, the aperture time can be reduced to a fraction of the impulse duration. Figure 2.11 is a SPICE simulation that shows a 0.14 ps aperture time for the sampling circuit. The circuit file used for the simulation can be found in Appendix B, and uses a strobe pulse with a 10% to 90% fall time of 1.0 ps, a differentiator round trip time of 1.0 ps, sampling diodes with 3 fF of capacitance each, and a reverse bias of 1 V.

A schematic diagram of the circuit used for testing is shown in figure 2.12. The signal being tested comes from one NLTL and a second NLTL is used to strobe the sampling diodes. The measured signal is then the convolution of the shock wave on the NLTL and the pulse response of the sampling circuit. Because these are both limited by the same diode RC time constants, it is usually a good approximation to assume that their contributions to the measured signal are equal, and so it is straightforward to calculate a deconvolved shock edge speed and sampling circuit bandwidth.

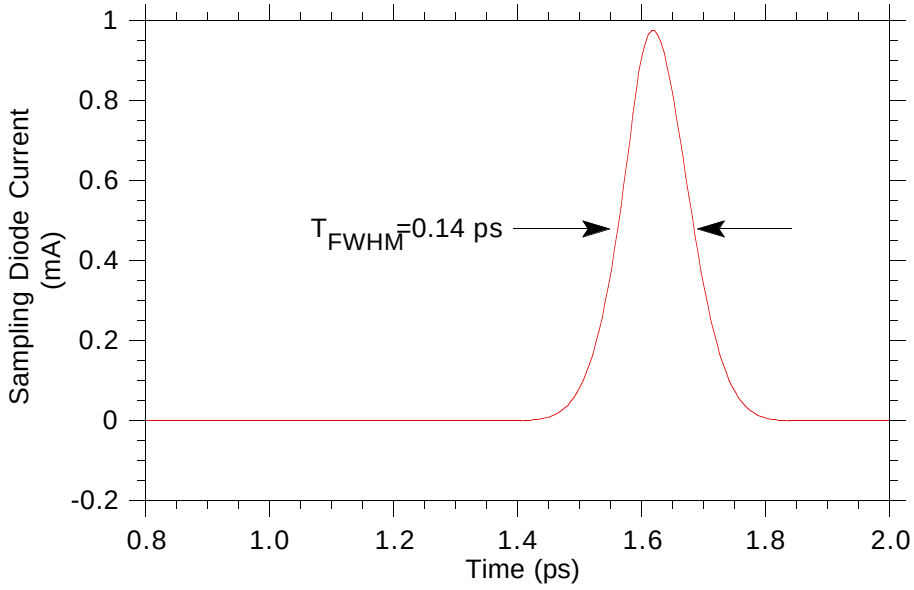

Figure 2.11: SPICE simulation of the sampling circuit showing the aperture time of the strobe pulse.

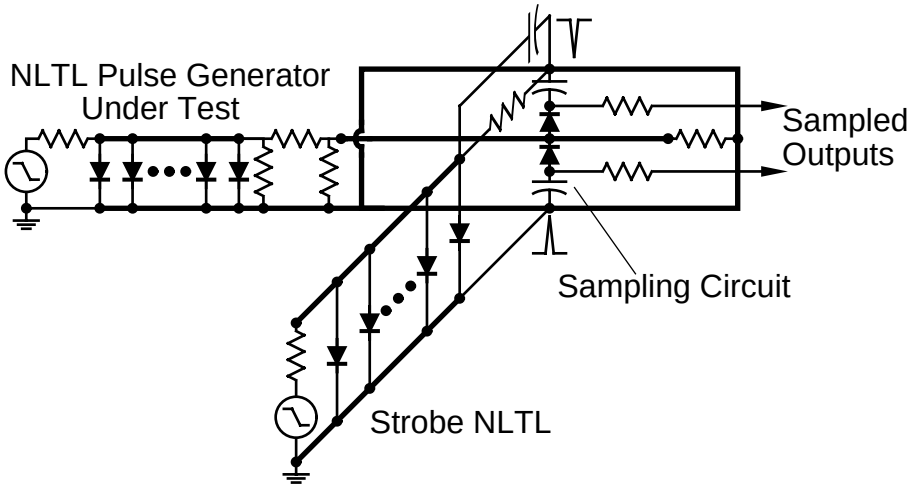

Figure 2.12: Schematic diagram of test circuit showing one NLTL as the test signal and a second NLTL as the strobe signal.

Chapter 3

Schottky Varactor Diodes

Schottky diodes are used in a number of millimeter wave and sub-millimeter wave applications. They are used to both generate and receive signals at frequencies above the operational range of transistors. As mixer diodes, they have been used to detect signals as high as 25 THz [14]. Their other common application is as multipliers, where the nonlinearity of their C-V curve is used to generate harmonics to produce power at frequencies unattainable directly with a solid state oscillator, typically used in the 300 GHz to 1 THz range [15]. For use in NLTLs, it is this nonlinearity of their C-V curve under reverse bias that is important because it is the variable capacitance that produces the variable propagation delay for a wave traveling down the line. In designing a varactor for this application, both the nonlinearity of the capacitance and the RC cutoff frequency of the diode are of primary concern.

3.1 Planar Diode Parasitics

A brief discussion of the diode fabrication is warranted at the outset because the parasitics of the diode are a function of its geometry and physical implementation. The planar diode is designed specifically for ease of integration into circuits where the devices must be densely packed. Figure 3.1 shows a cross-sectional view of the planar Schottky diode that was fabricated for this work. It consists of a Schottky contact to an $N-$ active region and recessed ohmic contacts to a heavily doped buried $N+$ layer. Areas outside where the diodes will be are rendered semi-insulating with a proton implantation. The active area of the diodes are defined by the intersection of the Schottky metal and the regions protected during the proton implantation. With this diode geometry the circuit layout is

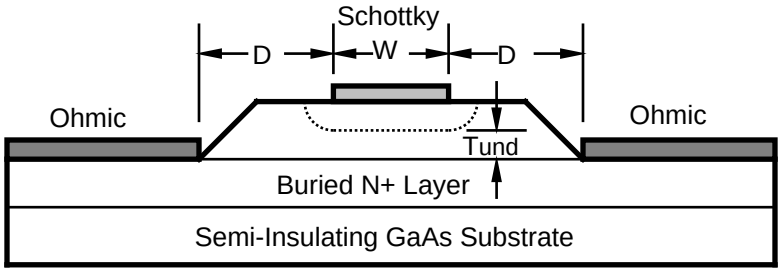

Figure 3.1: Cross section of a planar Schottky diode fabricated for use in a high frequency integrated circuit.

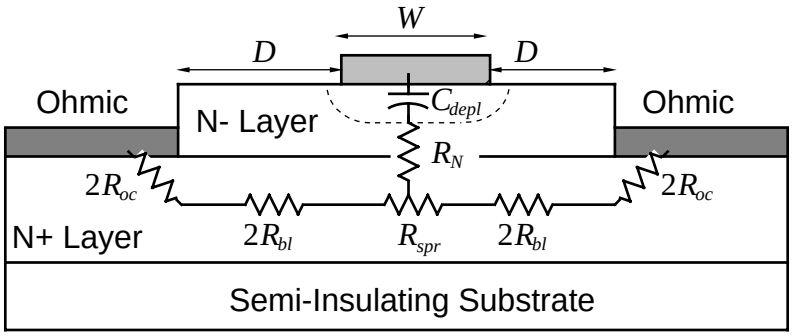

Figure 3.2: Schematic cross section of a planar diode illustrating the various components of the series resistance.

compact and the extrinsic parasitics are minimized, which is important for high frequency operation in integrated circuits.

Figure 3.2 shows a cross-sectional schematic of a planar diode and its associated equivalent circuit elements when under reverse bias. The Schottky contact has width W, the diode stripe length into the plane of the page is L, and the separation between the Schottky and ohmic contacts is D. The capacitance under the Schottky contact, $C = \varepsilon WL/d$, is from the depleted space charge region, whose depth, d, is a function of the applied reverse bias:

$$d = \sqrt{\frac{2\varepsilon}{qN_D} \cdot \left(V_{bi} - V_{bias} - \frac{kT}{q} \right)} \tag{3.1}$$

The resistance in series with this capacitance, R_s, can be modeled as the sum of four components. The first element, R_{N-}, is the vertical resistance through

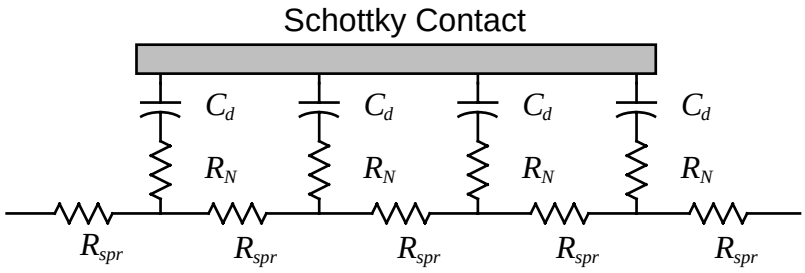

Figure 3.3: Schematic diagram illustrating the distributed nature of the resistance underneath the Schottky contact.

the undepleted portion of the $N-$ active layer. While the amount of undepleted material will be a function of bias, the value at 0 V bias is used as a conservative value because this will be the largest resistance:

$$R_{N-} = \frac{1}{WL} \cdot \rho_{N-} \cdot T_{und} \tag{3.2}$$

where ρ_{N-} is the resistivity of the material in the $N-$ active layer and T_{und} is the thickness of the undepleted region at 0 V bias. Because this resistance is a vertical resistance, it is an area term and so is inversely proportional to WL.

The second component of the series resistance is the spreading resistance, R_{spr}, that accounts for the spreading of the current flow under the Schottky contact into the buried $N+$ layer:

$$R_{spr} = \frac{1}{12} \cdot \frac{W}{L} \cdot \frac{\rho_{N+}}{T_{N+}} \tag{3.3}$$

where ρ_{N+} is the resistivity of the $N+$ layer and T_{N+} is the thickness of the layer. A factor of $W/4$ comes from the fact that the current will travel only half the contact width as it spreads out to either side and that these resistances are in parallel. An additional factor of $1/3$ arises from the distributed nature of the capacitance and resistance under the contact (figure 3.3) that is analogous to the spreading resistance in the base of a bipolar transistor or the distributed resistance of the gate finger of a MESFET.

The third component, R_{bl}, comes from the resistance of the buried layer due to the separation between the Schottky and ohmic contacts:

$$R_{bl} = \frac{1}{2} \cdot \frac{D}{L} \cdot \frac{\rho_{N+}}{T_{N+}} \tag{3.4}$$

and again the factor of 1/2 arises because there are two in parallel. The final component of the series resistance, R_{oc}, is from the ohmic contacts:

$$R_{oc} = \frac{1}{2L}\sqrt{\rho_{cont} \cdot \frac{\rho_{N+}}{T_{N+}}} \tag{3.5}$$

where ρ_{cont} is the specific contact resistivity.

Because R_{spr}, R_{bl}, and R_{oc} are inversely proportional to L and the capacitance is proportional to $W \cdot L$, decreasing W and increasing L to maintain a constant diode area reduces R_s in proportion to C and consequently increases f_{cls}, which is defined using the large signal capacitance of the diode (section 2.1.1):

$$f_{cls} = 1/2\pi C_{ls} R_s \tag{3.6}$$

This is analogous to the design of the base-emitter junction of a bipolar transistor where the dominant resistance is the base resistance, which is also a periphery dependent term, so by decreasing the emitter stripe width, the $R_{base}C_{eb}$ time constant is reduced. Figure 3.4 is a family of curves that illustrates how f_{cls} depends on both the doping in the $N-$ region and the geometry of the diodes. For any particular level of doping, f_{cls} can be greatly increased by reducing the Schottky contact width.

The design of the doping profile in the $N-$ region involved a tradeoff among three important parameters: cutoff frequency, breakdown voltage, and fractional change in capacitance. Increasing the doping level reduces R_{N-} but limits the breakdown voltage, V_{br}, which is either caused by avalanching or tunneling when the surface electric field $\approx 1 \cdot 10^6$ V/cm. Making the layer thicker leads to a larger change in capacitance because the depletion edge movement does not become pinned by the $N+$ layer, but this increases R_{N-} and hence reduces f_{cls}. Hyperabrupt doping profiles in which the doping decreases exponentially with distance [12] give large changes in capacitance but again at the expense of R_{N-}. The goal of this work was to obtain as high an f_{cls} as possible, so only uniformly doped diodes were analyzed.

The curves in figure 3.4 are for uniformly doped diodes where the $N-$ layer was designed to be thick enough to give a 3:1 change in capacitance over a 6 V swing. The dashed line shows how the avalanche breakdown voltage decreases as the $N-$ doping increases. Because of the tradeoff between f_{cls} and V_{br}, the doping level is determined by the maximum reverse bias voltage that the diodes must sustain.

Equation 3.6 for the diode cutoff frequency is valid at low frequencies, but neglects several high frequency phenomenon that adversely affect the series resistance of the diode. The following discussion of these effects is taken directly

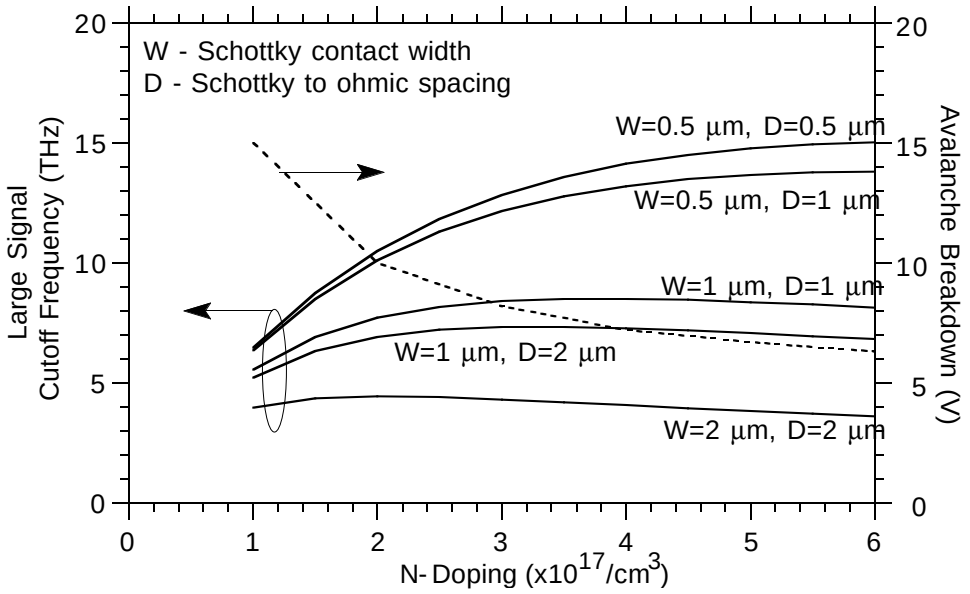

Figure 3.4: Family of curves for uniformly doped diodes illustrating the dependence of the large signal cutoff frequency on geometry and doping level.

from the work by Champlin and Eisenstein [16] and also includes their references to original work.

Dickens [17] was the first to treat this problem in the context of a Schottky diode and showed that the high-frequency extension of the spreading resistance is an impedance Z that for circular geometries given by:

$$Z = \frac{1}{2\pi\sigma a}\arctan(b/a) + \frac{(1+j)}{2\pi\sigma\delta}\ln(b/a) \tag{3.7}$$

where b and a are the radii of the semiconductor and contact, respectively, σ is the dc conductivity of the semiconductor and δ is the skin depth

$$\delta = \sqrt{\frac{2}{\omega\mu_o\sigma}} \tag{3.8}$$

in which μ_o is the magnetic permeability.

Equation 3.7 is based on two assumptions that are not generally valid for semiconductors in the sub-millimeter wave region. They are

$$\omega << \omega_{dr} = \frac{\sigma}{\varepsilon} \tag{3.9}$$

where ω_{dr} is the dielectric relaxation frequency and

$$\omega << \omega_{scat} = \frac{q}{m^* \mu_e} \tag{3.10}$$

where ω_{scat} is the scattering frequency, m_e^* is the effective mass of the electrons and μ_e is their mobility. Making assumption 3.9 is tantamount to ignoring the displacement current and is the usual assumption that leads to 3.8. Assumption 3.10 is equivalent to ignoring the inertial mass behavior of the carriers in their response to an applied electric field [18].

Both assumptions can be removed from 3.7 by replacing the dc conductivity σ with the complex quantity

$$\sigma' + j\omega\varepsilon = \sigma \left\{ \frac{1}{1 + j\,(\omega/\omega_{scat})} + j\,\{\omega/\omega_d\} \right\} \tag{3.11}$$

and by replacing $(1+j)/\delta$ with the actual propagation constant of the semiconductor material:

$$\gamma = \sqrt{j\omega\mu_o}\sqrt{\sigma' + j\omega\varepsilon} = \frac{(1+j)}{\delta} \left\{ \frac{1}{1 + j\,(\omega/\omega_{scat})} + j\,\{\omega/\omega_d\} \right\}^{1/2} \tag{3.12}$$

Substituting 3.11 and 3.12 into 3.7 and assuming $(b/a) \gg 1$ leads to $Z = Z_s + Z'$ where Z_s is the complex bulk-spreading impedance given by

$$Z_s = \frac{1}{4\sigma a} \left\{ \frac{1}{1 + j\,(\omega/\omega_{scat})} + j\,\{\omega/\omega_d\} \right\}^{-1} \tag{3.13}$$

and Z' is the complex skin-effect impedance. With a buried $N+$ layer doped as heavily as possible, $N_D \approx 5.0 \cdot 10^{18}$ cm^{-3} and $\rho_{N+} = 7.5\ \Omega\cdot\ \mu$m, the skin depth at 1 THz is 1.4 μm. Since the layer is only 1.0 μm thick, the current crowding effect will be negligible in the frequency range of interest, and Z' can be neglected.

An equivalent circuit model including Z_s is shown in figure 3.5. These high frequency effects can be modeled by adding two elements to the equivalent circuit model: a displacement capacitance $C_{dis} = 1/R_s\omega_{dr}$ and an inertial inductance $L_{scat} = R_s/\omega_{scat}$ The parallel $L_{scat}C_{dis}$ circuit is resonant at the plasma frequency given by:

$$\omega_{pl} = 2\pi f_{pl} = \frac{1}{\sqrt{C_{dis}L_{scat}}} = \sqrt{\omega_{dr}\omega_{scat}} \tag{3.14}$$

For the diodes used in this work, the $N-$ active region was doped at a level of either $N_D = 1.0 \cdot 10^{17}$ cm^{-3} or $N_D = 3.0 \cdot 10^{17}$ cm^{-3}, for which $f_p = 3.0$ THz

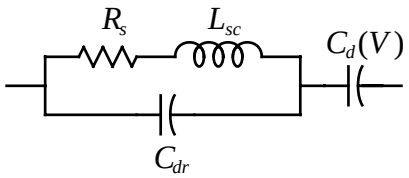

Figure 3.5: Equivalent circuit model of a Schottky diode that includes the effects of the displacement capacitance and inertial inductance.

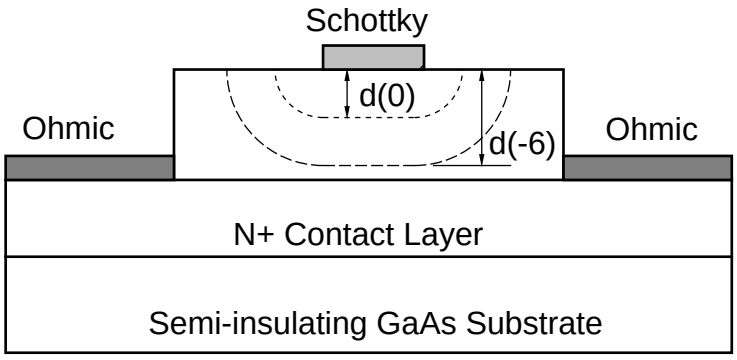

Figure 3.6: Cross section of a diode illustrating how the lateral extent of the depletion region increases with increasing reverse bias.

and 5.2 THz, respectively. Because the operating frequencies of the circuits are well below these, the use of the simple RC model to calculate f_{cls} as a figure of merit is valid, and so the curves in figure 3.4 remain useful as design tools.

Other factors, though, limit how far W can be effectively reduced. As W approaches dimensions similar to the $N-$ layer thickness, the lateral extent of the depletion region around the edges becomes significant, and effectively increases the area of the diode (figure 3.6), a problem that has been solved analytically by others [19]. The real problem for the NLTL application is that as the depletion depth increases under reverse bias, the lateral depletion region becomes proportionately larger, flattening out the C-V curve. This effect was eliminated by using a self-aligned etch to remove the $N-$ layer not directly under the Schottky contact, so there was no material remaining to laterally deplete (figure 3.7.)

Figure 3.8 illustrates the utility of this etching technique. The solid line shows the measured capacitance of a large area diode, 100 μm x 100 μm where edge effects are negligible. The dotted line shows the C-V curve for a 1 μm diode

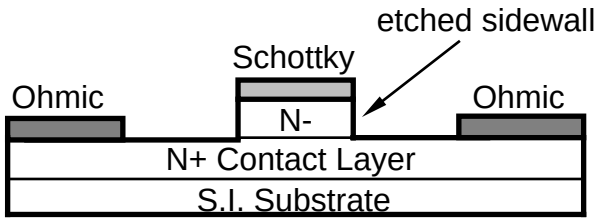

Figure 3.7: Cross section of a diode after the sidewalls have been etched.

before etching, and it can be seen that these diodes suffered a significant reduction in fractional change in capacitance. The dashed line is for the same diode after the self-aligned etch, showing that its C-V characteristics now conform to those of a large area diode, both in terms of 0 bias capacitance and voltage variation. With the addition of this processing step, the advantages in f_{cls} of a narrow Schottky contact can be obtained without sacrificing the nonlinearity of the diode.

3.2 Diode Fabrication

The Schottky diodes were formed with the first three process steps consisting of making the ohmic contacts to the $N+$ layer, implant isolating the wafer, and then depositing the Schottky metal. A thick layer of interconnect metal was used to form all of the transmission lines, and this deposition was followed by a two step air bridge process. The statistical yield of this six mask process was very high and tended to have more of a binary distribution: either the processing went find or there was a major failure such as the metal not lifting off. Both of the sampling diodes in each circuit must be operational, but because of the nature of the NLTL, if one or two of the diodes along the line were open, the performance would not be affected very much. If any were shorted, though, the line would be nonfunctional. No precise records were kept, but 80% is a reasonable estimate of the number of functioning circuits on a two inch wafer. Appendix C contains the detailed process flow sheets that were used for the fabrication.

3.2.1 Epitaxial Growth

The layer structures for the Schottky diodes were grown by molecular beam epitaxy and the material was purchased from a commercial vendor, Quantum

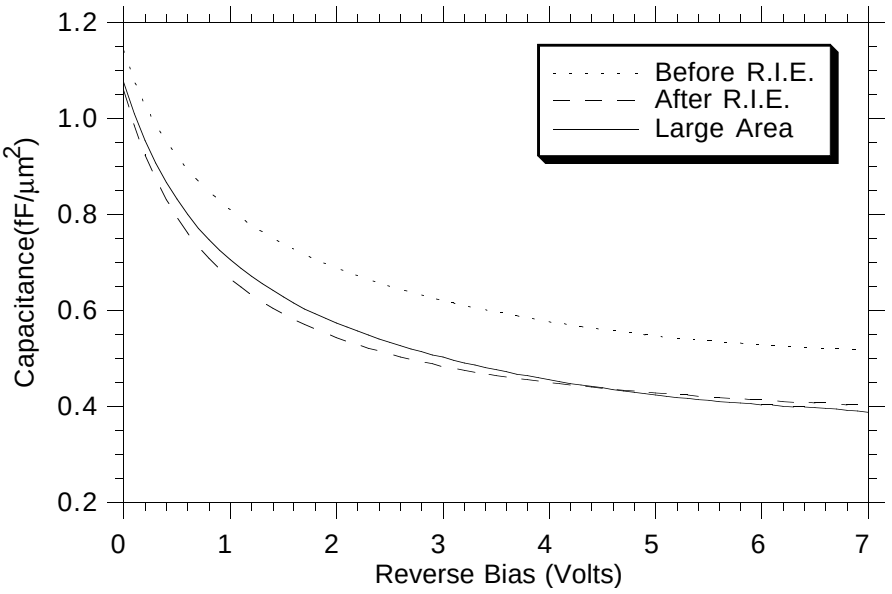

Figure 3.8: C-V curves of a 1 μm diode before and after sidewall removal compared to a large area device.

Epitaxial Design, Inc. The layers were grown on two-inch semi-insulating $\langle 100 \rangle$ GaAs substrates, and because of the size and complexity of the integrated circuits, the processing was done on the whole wafers. The 1 μm buried $N+$ layer was doped as heavily as possible with Si, and special care during growth was taken to ensure a high activation level of the dopants. Typical resistivity of the material was $\rho_{N+} = 7.5\ \Omega \cdot \mu$m. The $N-$ region was doped with $N_D = 1.0 \cdot 10^{17}$ cm^{-3} and was 350 nm thick so that it would be completely depleted at a reverse bias of 6 V. Polaron profiling data was always supplied with the wafers in order to verify the doping level in the active layer.

3.2.2 Ohmic Contacts

Formation of the ohmic contacts had to be the first step in the processing because it required a high temperature anneal. This annealing would destroy Schottky contacts and also anneal out the lattice damage that was intentionally introduced during proton implantation. The ohmic contacts were patterned in photoresist on the surface of the wafer and the $N-$ material was etched away using NH_4OH:H_2O_2:H_2O in a ratio of 3.5:22:266. An electron beam evaporator

was then used to deposit the metalization layer consisting of an 800 Å eutectic layer of Au and Ge, 100 Å of Ni and a 3000 Å cap layer of Au [20]. After liftoff, the contacts were alloyed in a rapid thermal annealer for 60 seconds at 400° C. Typical values from this process were $R_c = 20\ \Omega \cdot \mu$m and sheet resistance of $R_{sh} = 7.5\ \Omega/\Box$, giving a specific contact resistance of $\rho_c = 6 \cdot 10^{-7}\ \Omega \cdot$ cm^2. These are typical values for the process, with a wafer-to-wafer spread of $\pm 5\ \Omega \cdot \mu$m for R_c and $\pm 0.5\ \Omega/\Box$ for R_{sh}. The best specific contact resistance obtained was $\rho_c = 2 \cdot 10^{-7}\ \Omega \cdot$cm^2.

3.2.3 Proton Isolation

The second step in the process was to make the substrate semi-insulating everywhere except where the active diodes would eventually be. This provided the isolation between the diodes and also provided a low loss material on which to form the transmission lines. Ionized hydrogen atoms at energies as high as 200 KeV were implanted into the wafer, causing lattice damage. A damaged lattice contains trap sites for the electrons and these traps turn the doped layers into semi-insulating material if their density is high enough.

There were two important aspects to the design of the implantation. The first was that the dose and energy of the incident ions be sufficient to give good isolation. The second requirement was that the mask in the regions that were being protected during the implantation be sufficient to completely block the incident ions. The design of the implant profile was based data taken from a study of proton implantation performed by D'Avanzo [21]. His data showed that the peak of the ion distribution occurs at 0.65 μm per 100 KeV of incident energy. The statistical spread of the ions about this peak was taken from the calculated range statistics compiled by Gibbons [22]. At an incident energy of 200 KeV, the 2σ width is 0.15 μm, so the maximum depth at which sufficient damage can be done with a flux of 200 KeV protons is $\approx 1.45\ \mu$m. This sets an upper limit for the total thickness of the doped layers, which is why a 1.0 μm buried $N+$ layer was chosen.

The graph in figure 3.9 shows how the implant parameters were calculated. A simple triangular approximation to the implant profile was used in which the triangles have their apex at the peak of the proton distribution and return to 0 by the 2σ point. D'Avanzo's data showed that about 3 damaged lattice sites were induced per incident proton, and an additional factor of 3 was included in the implant design to give a large safety margin. This resulted in isolation that varied from 2 M$\Omega/\Box$ to 10 M$\Omega/\Box$ from wafer to wafer.

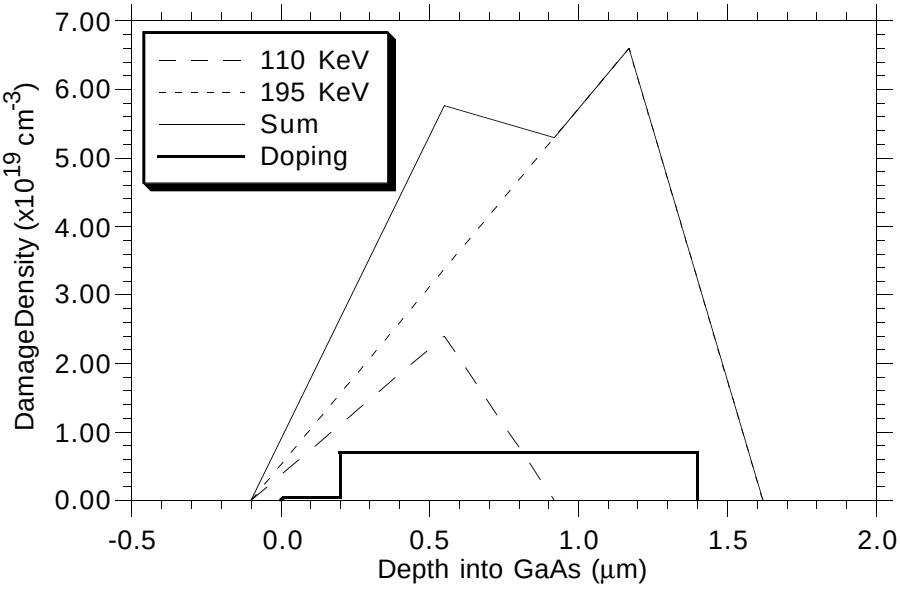

Figure 3.9: Approximation for the damage profile of the hydrogen implantation.

The implant mask had to be designed to block the highest energy protons of about 200 KeV. Gold was chosen because it is the densest of the metals, aside from platinum, that are routinely used in the fabrication process. Using a less dense metal would require a prohibitively thick implant mask. Using the range statistics for protons in Au and the requirement that the number of protons getting through was beyond the 3σ point of the distribution, a mask thickness of 1.6 μm was determined.

After the implantation process, the Au mask must be removed, so a sacrificial layer needed to be placed underneath it. Polyimide was chosen for this purpose, because if cured at the proper temperature ($\approx 240^\circ$ C), it becomes hard enough to provide a base that can withstand the subsequent photolithography and Au evaporation, yet this temperature is not high enough to crosslink the polymers and so the polyimide can still be removed. One problem that was encountered, though, was that although the polyimide was not completely cured during oven baking, it became very difficult to remove after the ion implantation, possibly due to heating during the implantation process. As a result of this, the surface of the GaAs was often damaged during the polyimide removal, as shown by the photograph of the surface in figure 3.10. The surface roughness was not polyimide that remained but actually pits in the GaAs from material that was

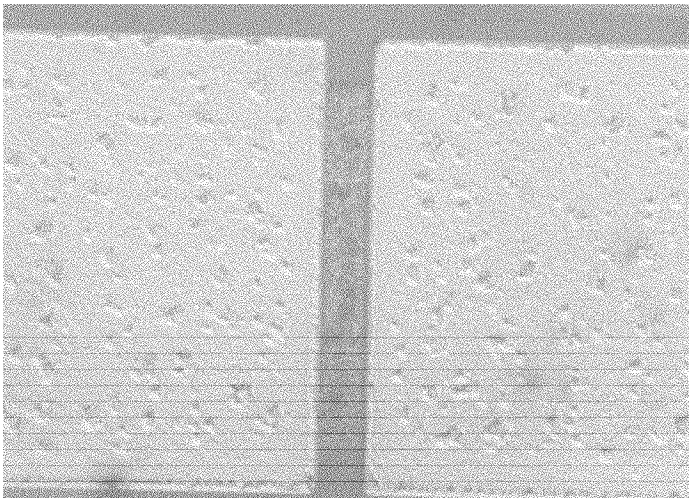

Figure 3.10: Photograph of the surface of the wafer after removing polyimide. The two ohmic pads have a particularly rough surface after alloying because of carbon contamination in the Au. The etch pits in the GaAs between them are clearly visible and caused a degradation in the diode's performance.

removed along with the polyimide. This surface roughness was on the order of 200 Å and was sufficient to degrade the diode ideality factors and breakdown voltage.

The solution to this was to coat the wafer with 1000 Å of SiO_2 before applying polyimide. A cross sectional view of the complete implant mask is shown in figure 3.11. After removing the polyimide, the SiO_2 was etched in a buffered HF solution, and the undamaged GaAs surface resulted in an improvement in diode ideality factor and breakdown characteristics.

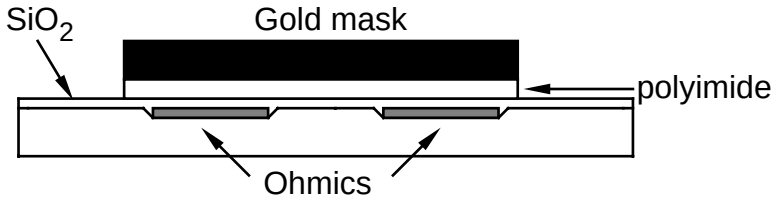

Figure 3.11: Details of the implant mask showing the protective SiO_2 coating, the sacrificial polyimide layer and the 1.6 μm thick Au mask.

3.2.4 Schottky Contacts

After removing the implant mask, the next process step was to form the Schottky contacts. In order to define 1 μm wide diode fingers, it was necessary to use thin photoresist for the lithography, and this limited the thickness of the metal that could then be lifted off. Because thick metal, at least greater than one skin depth, is desirable for the transmission lines to keep the loss low, it was decided to pattern the diodes and the interconnect metal in two different process steps. It was found that a 20 second oxygen plasma etch after patterning the photoresist resulted in an improvement in the diodes' ideality factors, probably because there had been a very thin film of photoresist remaining that was degrading the Schottky contacts. This plasma etch was performed using the higher frequency system, 13.5 MHz instead of 30 KHz, because the lower momentum of the incident ions causes less damage to the surface of the wafer [23]. The idea was to remove a thin layer of photoresist but not cause any ion induced damage to the $N-$ active regions of the diodes.

The evaporated Schottky metal consisted of a thin 150 Å adhesion layer of Ti, 500 Å of Pt serving as a diffusion barrier, and then 0.5 μm of Au. The active area of the diodes was defined by the intersection of the Schottky metal and the regions that were masked during the implantation. For the interconnect metal, the Au was thickened to 1.5 μm. Figure 3.12 summarizes these first three process steps.

3.2.5 Sidewall Etch

For reasons discussed in section 3.1, it was necessary to remove the sidewalls from the diodes. This was done using a Cl_2 reactive ion etch (RIE) [24]. With a base pressure in the chamber of $1.0 \cdot 10^{-6}$ mTorr, an etching pressure of 1 mTorr of Cl_2 and 300 W of RF power, vertical sidewalls for the 300 nm depth of the $N-$ region were readily attained. Although Au is sputtered by a Cl_2 etch, the amount removed in 2 minutes was not enough to cause any problems, and so a self-aligned etch could be done using the Schottky metal itself as the etch mask with no other lithography steps required. The resulting improvements to the C-V characteristics of the 1 μm diodes were shown in figure 3.8.

Another benefit from the Cl_2 etch was an improvement in the breakdown characteristics of the diodes. Before etching, the breakdown voltage, V_{br}, for diodes with large peripheries was lower than that of very small diodes and was also much softer, probably due to a surface leakage phenomenon. After etching, V_{br} of the larger diodes converged to that of the smaller diodes, as shown in table

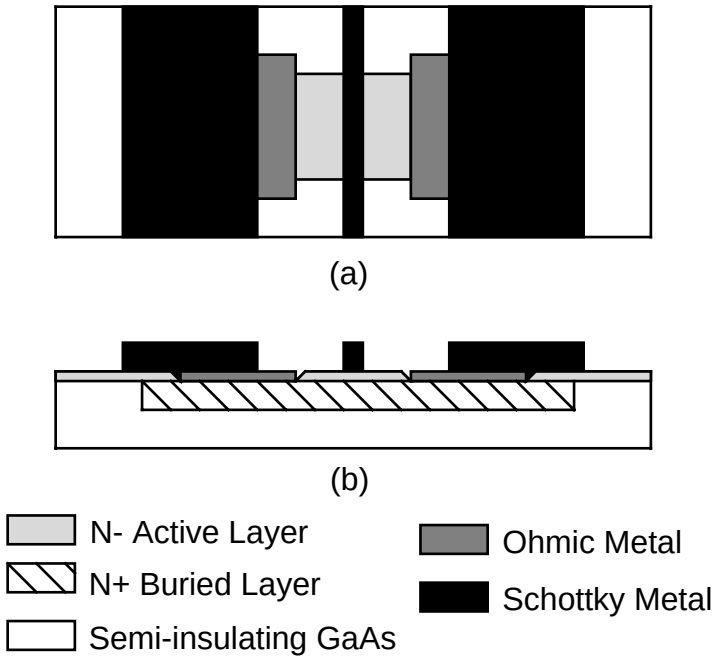

Figure 3.12: Top view (a) and cross section view (b) of a diode after the first three process steps.

Diode Geometry	V_{br} (V) Before RIE	V_{br} (V) After RIE
1x2	13.3	14.1
1x5	11.5	13.5
2x27	9.9	12.7
2x42	9.7	12.7
4x3	9.9	12.9
4x10	9.9	12.9

Table 3.1: Breakdown characteristics were improved by the RIE sidewall etch so that V_{br} of larger diodes converged to that of the smallest.

3.1 which lists V_{br} before and after etching for a number of different geometry diodes.

One problem with recess etching is that it can leave surface states on the exposed semiconductor surface. If these surface states have long charging times, the result will be that there is a difference in the static and dynamic C-V characteristics, similar to the frequency dispersion in the output conductance of HEMTs [25]. This is not a phenomenon that can be measured using the normal C-V profiling technique because it would require changing the dc bias at a rate faster than the time constants of the surface states. The performance of the diodes could only be measured indirectly by how well the NLTLs worked, and it was found that the sidewall etching greatly improved the circuit performance, leading to the conclusion that the improvement in C-V characteristics carried over to high frequency operation.

As a further attempt to determine if surface states were having an effect, some devices were passivated after the Cl_2 etch. They were cleaned in dilute solutions of NH_4OH:H_2O and HCl:H_2O and then passivated with 800 Å of SiN deposited at 250° C in a P.E.C.V.D. system. This passivation process significantly lowered the zero bias capacitance, which was attributed to undercutting at the metal-semiconductor interface during the wet etching. Because of this problem, all subsequent circuits were fabricated without passivation.

Another method that was investigated as a way to eliminate the sidewall capacitance problem was to use a shallow ion implantation to neutralize the $N-$ doping not protected by the Schottky metal. Oxygen was implanted at 130 KeV and a dose of $4.4 \cdot 10^{11}$ cm^{-2}, but the transverse straggle of the ions under the

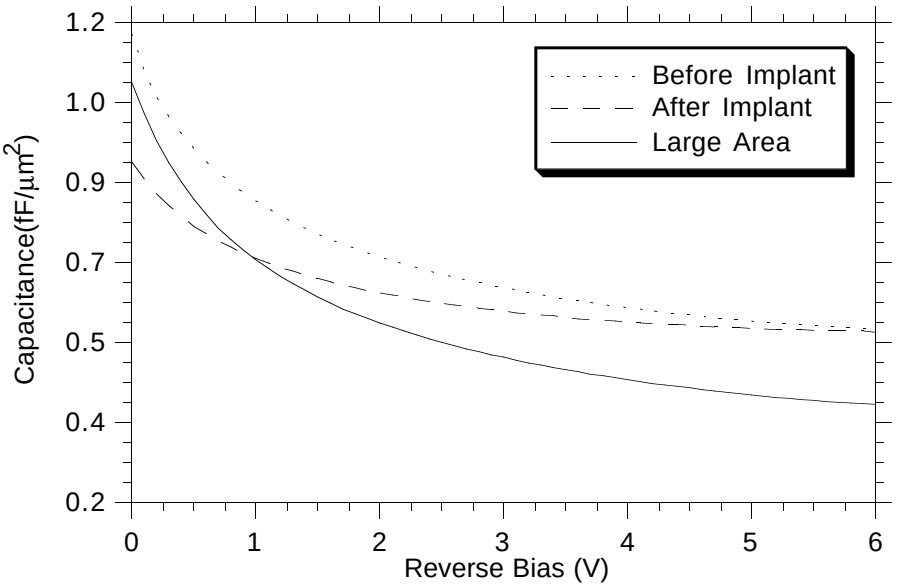

Figure 3.13: C-V curves showing how the capacitance of a 1 μm diode was reduced after the oxygen implant.

Schottky contact substantially reduced the diode capacitance. The results of this experiment are shown in figure 3.13 which compares the C-V profile of a 1 μm diode before and after implantation to that of a large area diode. Similar results were obtained with a dual energy hydrogen implantation of $1.4 \cdot 10^{13}$ cm^{-2} at 15 KeV and $1.8 \cdot 10^{12}$ cm^{-2} at 5 KeV.

3.2.6 Air Bridges

The final step in the process flow was to form crossover air bridges. These were not necessary for diode operation, but were used in the sampling circuit to provide a second layer of interconnect metal and were also used to tie together the ground planes of the coplanar waveguide in order to suppress any parasitic coplanar strip modes. Figure 3.14 illustrates the details of the process flow and also shows a cross section view of a completed air bridge.

The first step was to pattern the post holes where the air bridges would contact the interconnect metal. Next a flash layer of titanium and gold was sputtered to cover the entire wafer because the air bridges were to be electroplated and this requires a continuous conducting surface across the wafer. The

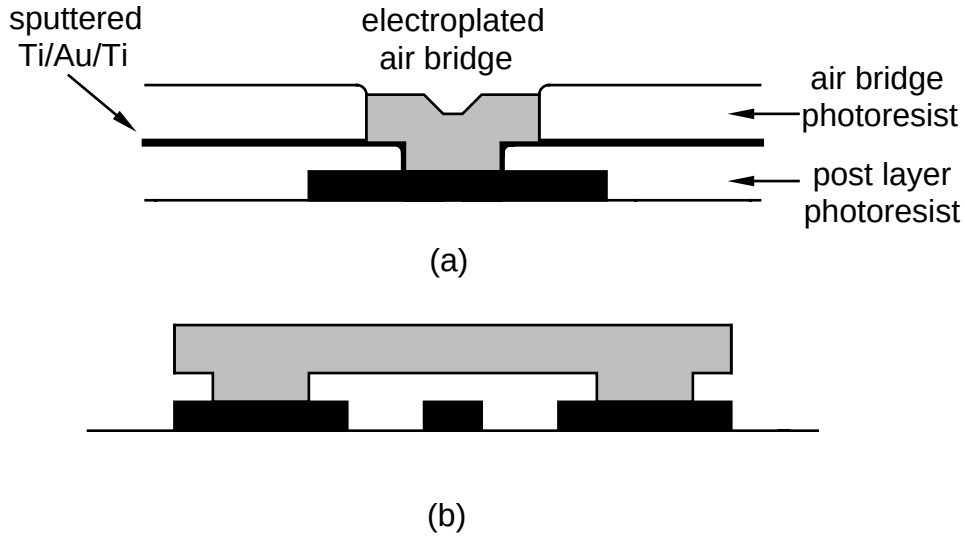

Figure 3.14: (a) Processing details for the air bridges and (b) cross section after completion.

third step was to pattern the air bridges in a layer of photoresist applied on top of the flash layer. During electroplating, only those areas not covered by photoresist plated, and this is how the 3 μm thick air bridges were formed. The final process step was to remove the photoresist and flash layer from the rest of the wafer, leaving the crossovers suspended in air. Because the bridges were 3 μm above the interconnect metal and the gap was entirely air, the capacitance from these was negligible.

3.3 Diode Characterization

The first measurements taken on the diodes were usually capacitance-voltage curves which are a way of checking the doping profile in the $N-$ active region. By comparing the measured C-V data of large area 100 μm x 100 μm diodes to that predicted by equations 3.1, the exact value of the doping level could be determined. As shown in figure 3.8, the C-V curves of both large area diodes and 1 μm were compared to quantify the effect of the sidewall capacitance on the narrow Schottky contacts.

Current vs. voltage curves were measured in both the forward and reverse directions in order to give a complete dc characterization of the diodes. The

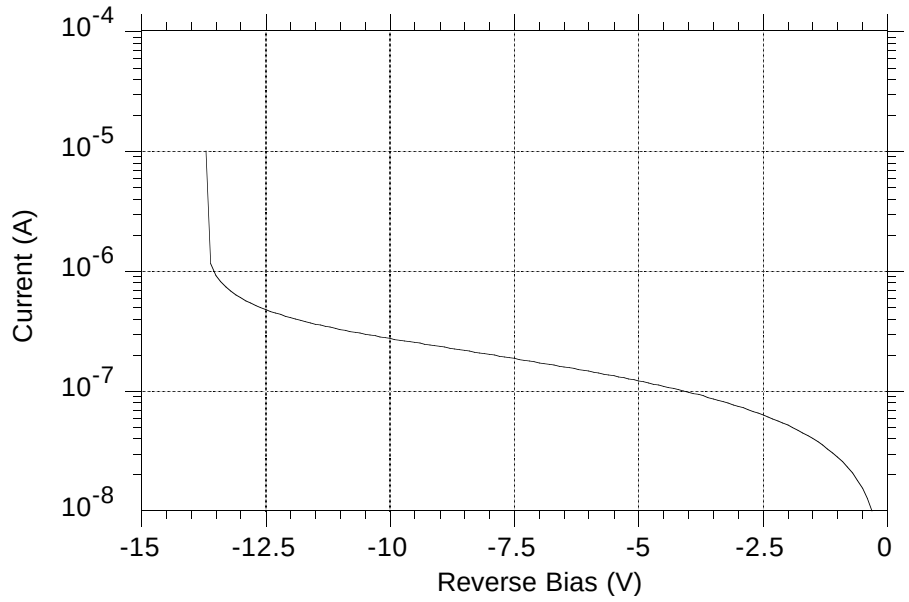

Figure 3.15: Reverse breakdown measurement on a 1 μm x 3 μm diode with $N- = 1.0 \cdot 10^{17}$ cm^{-3}.

diodes on which these measurements were made were contacted with pads that were configured to be used with microwave probes, so both dc and microwave measurements could be made on the same test devices. These test structures were laid out to include diodes of all the different geometries used in the circuits, such as the 1 μm x 3 μm diodes used in the sampling circuits and the very large 2 μm x 100 μm diodes at the input end of the NLTLs.

3.3.1 DC Measurements

The reverse breakdown voltage, V_{br}, was determined by measuring the I-V curves of diodes under negative bias. These measurements for 1 μm x 3 μm diodes with two different doping levels, $N- = 1.0 \cdot 10^{17}$ cm^{-3} and $N- = 3.0 \cdot 10^{17}$ cm^{-3} are shown in figure 3.15 and figure 3.16, respectively. In both cases, the avalanching occurs when the maximum electric field in the diode is within 5% of the theoretical breakdown field predicted for diodes with these doping levels [26]. As discussed in section 3.2.5, after the Cl_2 sidewall etch, V_{br} for all of the different geometry diodes was essentially the same.

I-V measurements on the diodes under forward bias enabled the extraction

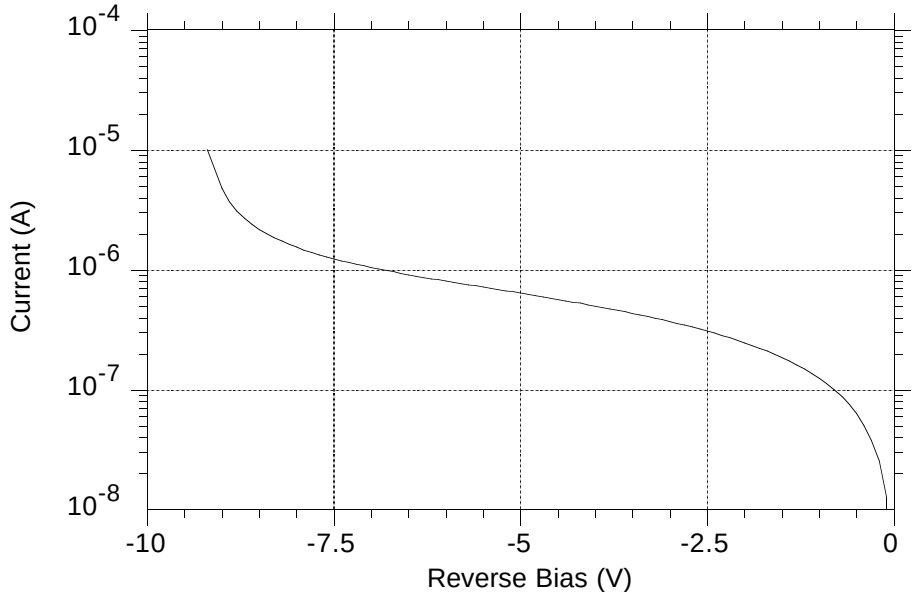

Figure 3.16: Reverse breakdown measurement on a 1 μm x 3 μm diode with $N- = 3.0 \cdot 10^{17}$ cm^{-3}.

of a number of important parameters. For a Schottky diode, the current under forward bias is given by the expression:

$$I_F = I_{ss} \cdot \left[\exp\left(\frac{qV_F}{nkT}\right) - 1\right] \tag{3.15}$$

where I_{ss} is the reverse saturation current, V_F is the forward voltage across the junction of the diode and n is the ideality factor. A plot of the forward I-V curve of a 1 μm x 3 μm diode with $N- = 1.0 \cdot 10^{17}$ cm^{-3} is shown in figure 3.17 on a linear plot, which makes the turn on voltage of the diode very clear, but the other important parameters are more readily extracted by looking at a log-linear plot as shown in figure 3.18.

The linear region of the I-V curve on the logarithmic scale will have a slope that is inversely proportional to the ideality factor, so from two points in this region the values of I_{ss} and n can be determined. The diodes typically had an ideality factor of $n = 1.15$ and a reverse saturation current density of $5 \cdot 10^{-15}$A/cm^2. The ideality factor was very uniform across a wafer, but I_{ss} usually varied from 2 to $7 \cdot 10^{-15}$ A/cm^2.

When the forward current through the diode becomes large, the curve deviates from a straight line because the voltage across the junction is not the same

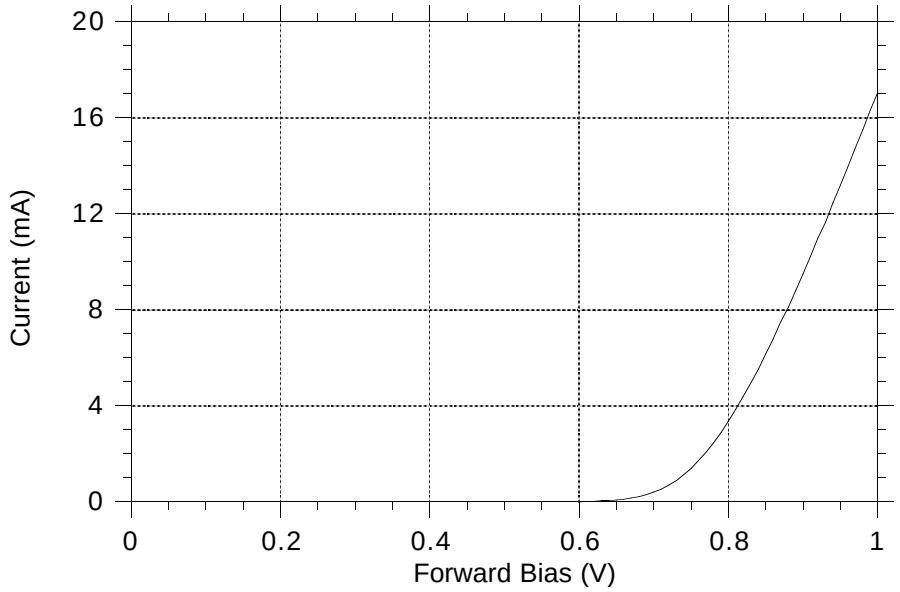

Figure 3.17: Forward I-V curve of a 1 μm x 3 μm diode.

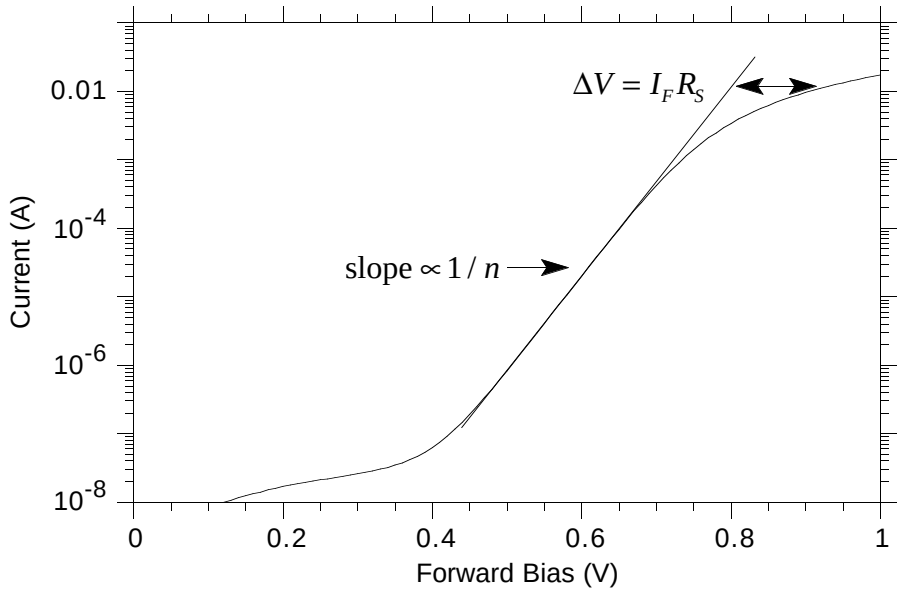

Figure 3.18: The forward I-V curve of a 1 μm x 3 μm diode plotted with current on a logarithmic scale.

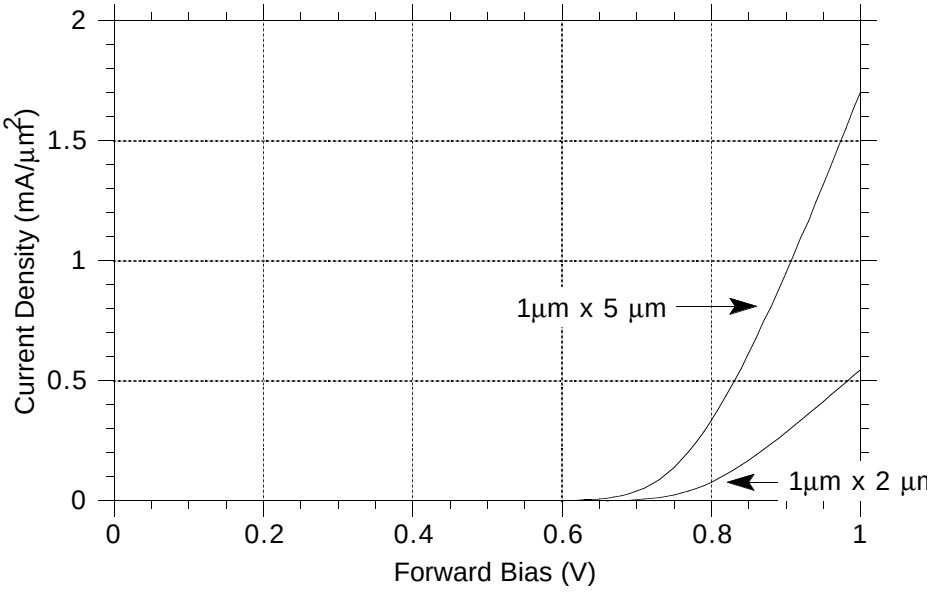

Figure 3.19: Forward J-V curves of a 1 μm x 5 μm and a 1 μm x 2 μm diode illustrating the effect of the large R_s of small diodes.

as the applied voltage due to the voltage drop across the series resistance of the diode: $V_F = V_{app} - I_F R_s$. By calculating the deviation of the I-V curve from a straight line, the value of R_s can be determined.

These measurements led to the important discovery that very small diodes had extremely large values of R_s, more than 5 times what was predicted. This is illustrated in figure 3.19 which compares the forward current density curves of a 1 μm x 5 μm diode to a 1 μm x 2 μm diode. From the equations in section 3.1, the 1 μm x 2 μm diode should have had 2.5 times the R_s of the 1 μm x 5 μm diode, but instead it was about 10 times as high. This high resistance for the small diodes can be ascribed to the lateral straggle of the protons during the ion implantation process. The material along the mask edges is damaged by the ions that scatter in the horizontal direction, and when this damaged material becomes a significant fraction of the total diode stripe length, the series resistance of the diode is greatly increased.

Test structures were designed to quantify the impact of this transverse straggle. Resistors of varying widths were defined by the implant mask, and by plotting the measured resistance as a function of the mask width, an effective width of each resistor was determined. The encroachment seen in the $N+$ layer

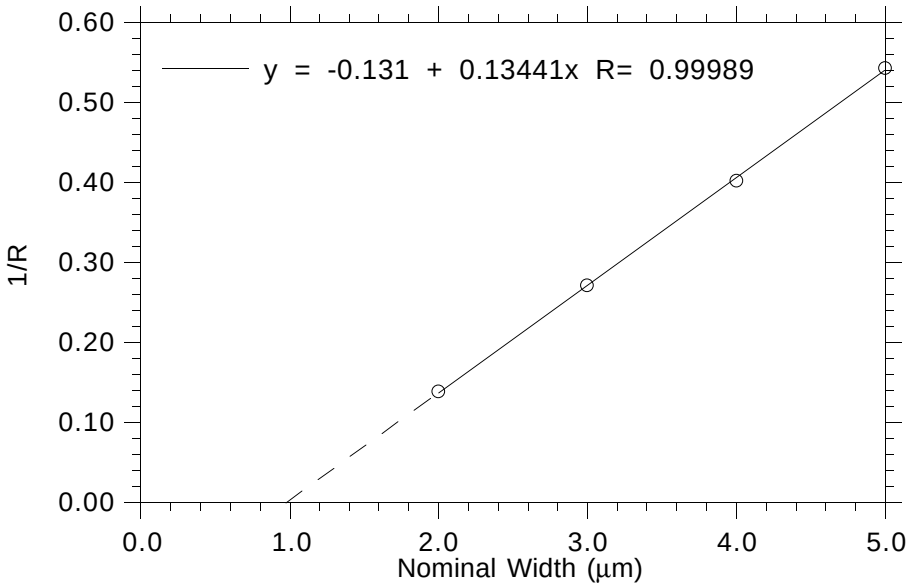

Figure 3.20: Measured resistance of resistors defined by the implant mask. The x-intercept indicates that 1 μm of material on each resistor had been severely damaged during implantation.

resistors (figure 3.20) of 1 μm indicates that effectively 0.5 μm of material along each edge was being completely isolated during implantation. This is a measurement of the effect of the straggle all the way through the 1 μm $N+$ region. It is reasonable to assume that the effect was worse in the first 300 nm of lightly doped material, explaining why it was found that diodes with a stripe length less than 3 μm suffered from a severe degradation of series resistance.

3.3.2 Microwave Measurements

Microwave data was obtained by measuring the S-parameters of the diodes from 50 MHz to 40 GHz. Because the cutoff frequency of the diodes was so high, there were two critical steps required in order to accurately extract values for the junction capacitance and series resistance. First of all, because the series resistance was so small, the measured S- parameters were very near the edge of the Smith chart, so a very accurate calibration was required because even 0.2 dB ripple in the calibration would make the diode appear to have gain. Secondly, the capacitance of the large pads that were used to contact the diodes

was comparable to the intrinsic capacitance of the diodes being measured and so the data for the diodes had to be carefully deembedded from the effects of the pads.

It was found that the calibration technique commonly used with microwave probes, the open-short-load-through (OSLT) method, was not sufficient for this application. In this method, three defined standards are measured on each of the two ports. A precise 50 Ω load and a short circuit are measured, and then the probes are raised in the air to make the open circuit measurement. If a full two-port calibration is required, the probes are then contacted to a very short through line. The problem with this method is that for measuring the open the probes are in air, which has a lower dielectric constant than the substrate and hence lower capacitance, and so a negative capacitance is defined for that measurement to account for the difference. This calibration method works well for low-Q devices up to about 20 GHz, but the measured reflection coefficient of a high-Q device always goes outside the Smith chart between 30 and 40 GHz because the approximations made during the calibration are not sufficiently accurate.

A second calibration technique that is sometimes used is the line-reflect-line (LRL) method, which does not suffer from the drawbacks of the OSLT method. In an LRL calibration, two transmission lines of lengths differing by a quarter wavelength are measured, followed by the measurement of a high reflection standard. Because the value of the reflection standard does not have to be precisely defined, this method does not require the same approximations made for OSLT. The drawbacks to this technique are that the lines need to be precisely 50 Ω at all frequencies, which means that the calibration degrades at high frequencies where dispersion effects alter the line impedance. The second problem is that the lowest frequency that can be measured is limited by the longest length of line used as a standard, typically giving a lower bound of about 2 GHz.

The calibration technique that was used for this work was the line-reflect-match (LRM) method that was developed by Cascade Microtech [27]. This is a hybrid of the two earlier techniques that overcomes the drawbacks of each. A very short line, 1 ps electrical length, is measured for the through standard, so it will not have dispersion problems. The reflection standard is the same as for the LRL in that it must be a high reflection but does not have to be precisely defined. The third calibration measurement is to terminate both probes in precise 50 Ω loads that are mathematically treated as infinite delay lines. This eliminates both the dispersion problem and the lower frequency limit suffered using the LRL method.

After accurately calibrating the system, the second step when making the

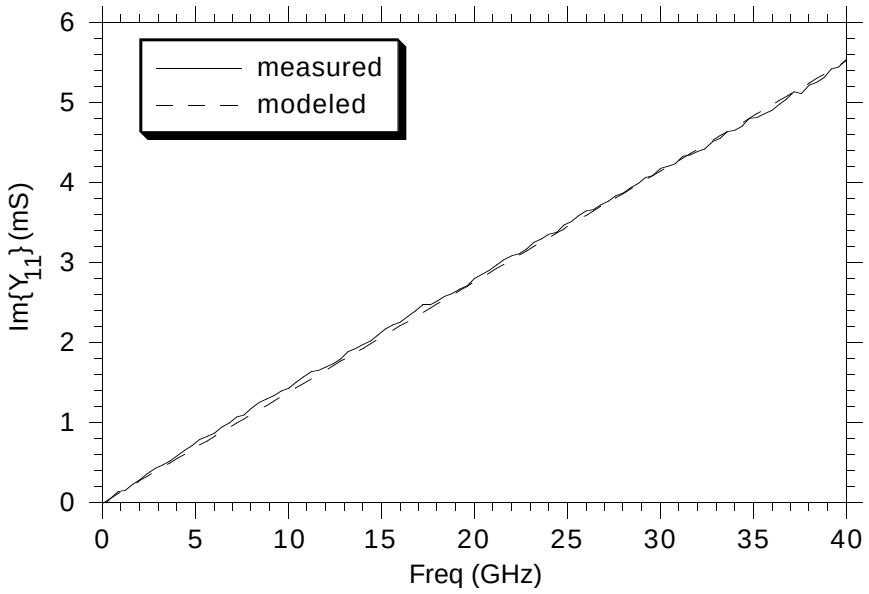

Figure 3.21: The capacitance of the pads is determined by fitting a straight line to the imaginary part of the input admittance.

microwave measurements was to account for the effects of the pads that were used to contact the diodes. This was done by first measuring the pads when they were open circuited and then shorting them together across where the device under test would be. In the first case, only a capacitance should be measured, so the imaginary part of the input admittance should be a straight line as a function of frequency and have a slope equal to the capacitance. The data for the open standard is shown in figure 3.21, where the linear fit from 50 MHz to 40 GHz for $C_{pad} = 22$ fF is almost perfect.

The inductance of the pads was determined taking the measured data from the shorted standard and subtracting off the capacitance determined from the open standard. The remaining part should look purely inductive since the resistance is negligible, and so the imaginary part of the impedance should be linear with frequency and have a slope equal to the inductance. This data is shown in figure 3.22, and a value of $L_{short} = 45$ pH gives an extremely good fit.

The parameters of the diode under test were deembedded from the pads by subtracting off the capacitance and inductance determined from the two standards, as shown in the equivalent circuit in figure 3.23.

Near the edge of the Smith chart, all the circles of constant resistance are

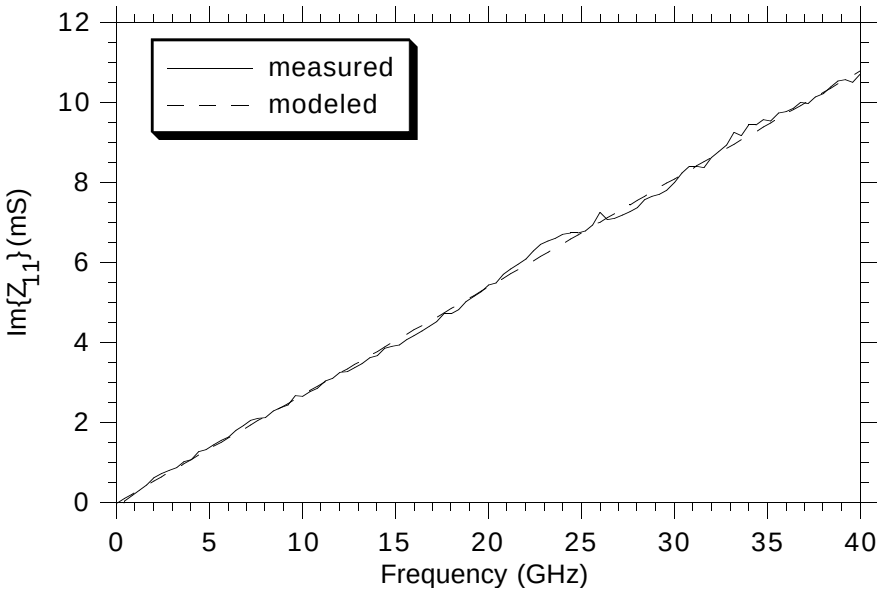

Figure 3.22: The inductance of the pads is determined by fitting a straight line to the imaginary part of the impedance after subtracting off the pad capacitance.

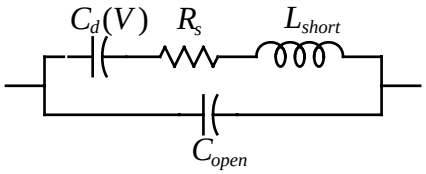

Figure 3.23: Circuit model used to deembed the diode under test from the pads.

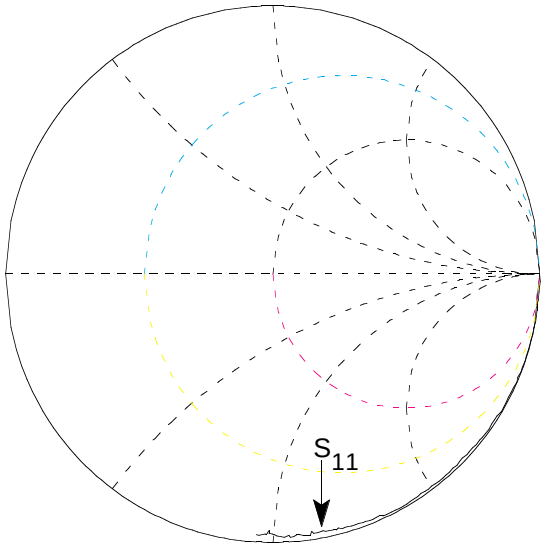

Figure 3.24: Smith Chart showing the deembedded data for a 2 μm x 42 μm diode at $0V$ bias.

extremely close together, and so it is difficult to reliably identify a small R_s. This can be seen in figure 3.24 where the measured diode impedance is barely distinguishable from the edge of the Smith Chart. This also illustrates the importance of having an extremely good calibration.

In order to extract the small signal parameters of the diode, it was instructive to consider the admittance of the device instead of the impedance:

$$Y = \frac{\omega^2 C^2 R_s}{1 + \omega^2 C^2 R_s^2} + \frac{j\omega C}{1 + \omega^2 C^2 R_s^2} \tag{3.16}$$

At frequencies $\omega << 1/CR_s$, this reduces to $Y = \omega^2 C^2 R_s + j\omega C$. The capacitance is now readily determined because the imaginary part of the admittance is linear with frequency and has a slope of C. The real utility in examining the admittance instead of the impedance comes when determining R_s. The conductance of the diode at frequencies well below f_c is directly proportional to the diode area, so examining the real part of the admittance on a large device provides for reliable extraction of R_s. Figure 3.25 shows the measured and modeled capacitance of a 2 μm x 42 μm diode at 0 V bias. The extracted capacitance of 84 fF is very close to the theoretical value of 89 fF calculated for a diode with

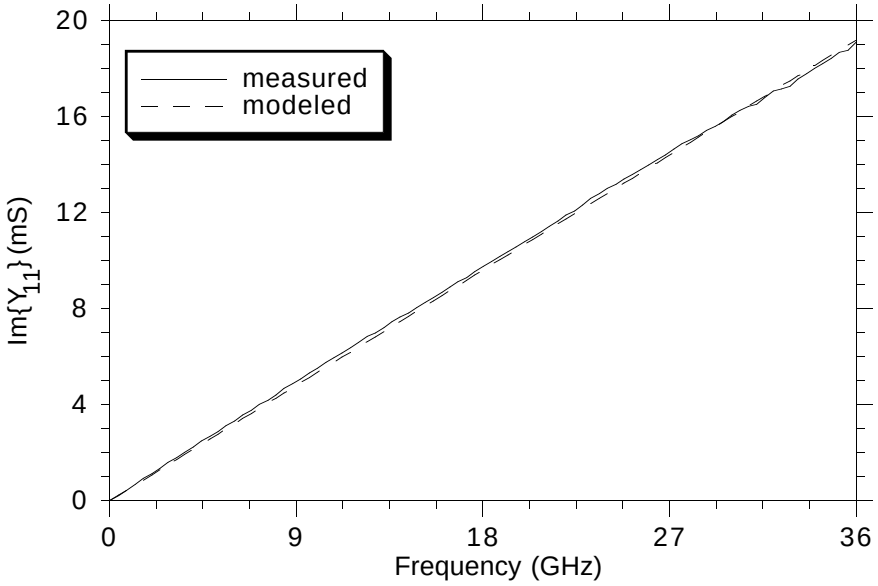

Figure 3.25: Measured and modeled capacitance of a 2 μm x 42 μm diode.

$N- = 1.0 \cdot 10^{17}$ cm^{-3}. The measurements were made on this diode because it was the test diode that had the largest area.

By knowing the diode capacitance accurately, R_s can be determined by fitting a curve to the measured conductance, as shown in figure 3.26. The curve is parabolic with frequency, as predicted by equation 3.16, and the value of $R_s = 1.2$ Ω determined by a least-squares fit is only 10% higher than is calculated from the bulk dc parameters using the equations in section 3.1. Using these measured values and applying the scaling rules from section 3.1, the 1 μm diodes have a large signal cutoff frequency of 4.1 THz.

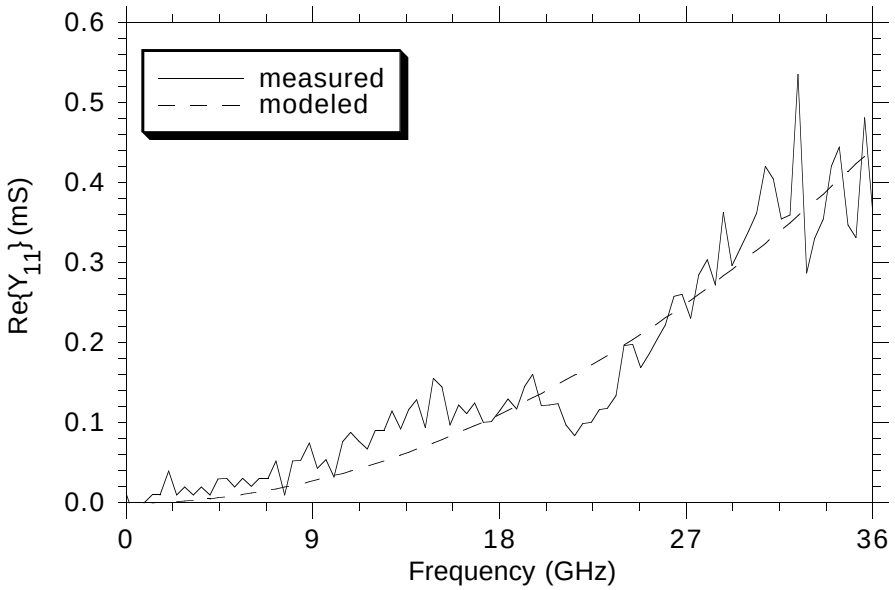

Figure 3.26: Measured and modeled conductance of the diode, showing the quadratic frequency dependence.

Chapter 4

NLTL Characterization

After the circuits had been fabricated, a number of different measurements were made to characterize them. The first diagnostics were on the test diodes, and the details of these measurements were covered in the previous chapter. The next set of measurements was characterization of the NLTLs using a microwave network analyzer. For this purpose, some of the NLTLs were not connected to sampling circuits but instead had microwave probe pads on each end. Most of the important parameters that characterize an NLTL can be determined from these measurements. The final step in the testing was to measure the two NLTLs integrated with a sampling circuit, as diagrammed in figure 2.12.

4.1 Microwave Measurements

The first easily measured parameter is the small signal impedance of the NLTL as a function of bias. Figure 4.1 shows the measured reflection coefficient of the NLTL at 0 V and -6 V bias. Figure 4.2 shows that the input and output reflection coefficients were virtually identical. The shapes of the curves is readily understood. At low frequencies, where the loss of the line is small, the measured impedance is just the 50 Ω load transformed through the impedance of the line. As the loss increases at higher frequencies, the effect of the 50 Ω termination is no longer seen and the measured impedance converges to the characteristic impedance of the line. This causes the center of the circles to shift with frequency, and the high frequency loss also causes the radius of the circles to spiral inward.

These lines were designed to have $Z_{ls} = 40\ \Omega$, so the small signal design impedances were $Z(0V) = 31\ \Omega$ and $Z(-6V) = 46\ \Omega$. The measured values as determined from the curves in figures 1.1 and 1.2 were $Z(0V) = 29\ \Omega$ and

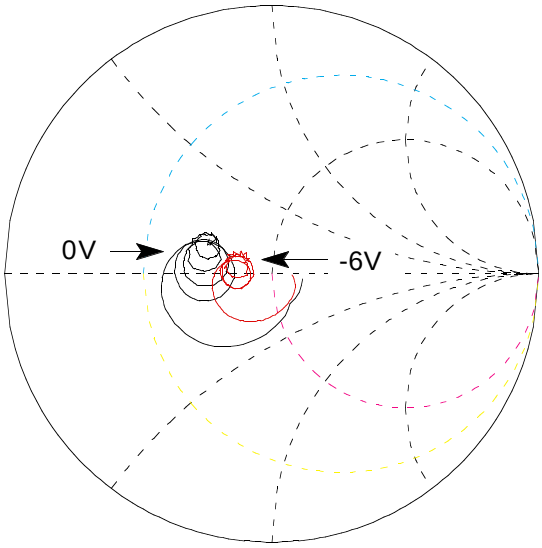

Figure 4.1: Measured S_{11} of NLTL at 0 V and -6 V bias.

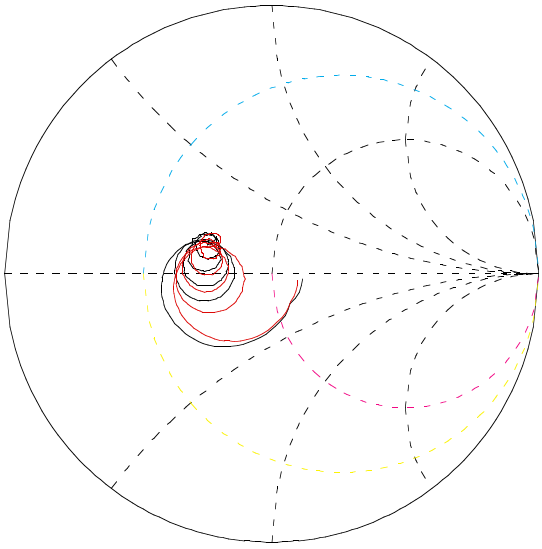

Figure 4.2: The input and output impedance of the line were essentially identical.

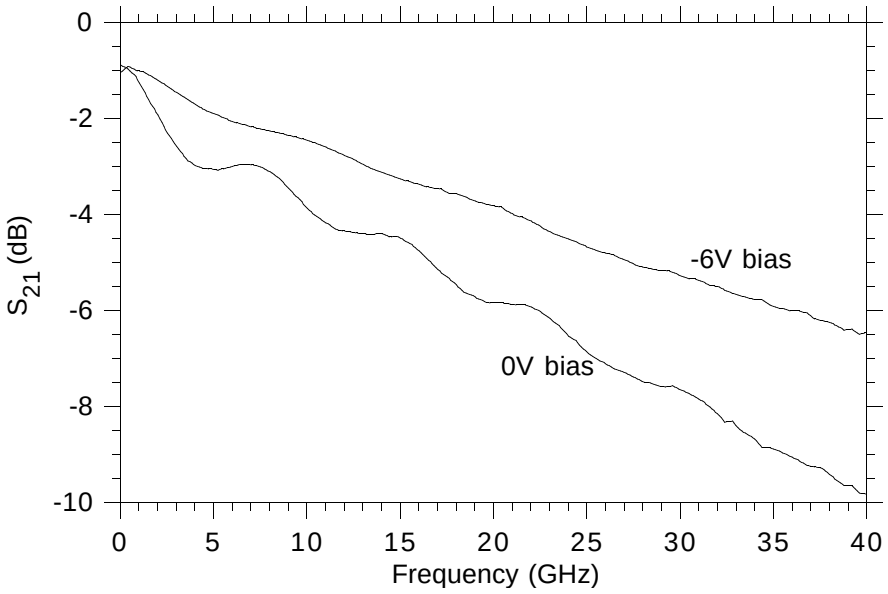

Figure 4.3: Network analyzer measurement of loss on the NLTL when biased at two different biases.

$Z(-6V) = 39\ \Omega$, smaller than the design values. One explanation for the lower impedance is that the parastic capacitances from the cell layout were loading down the line. With this as a premise, the calculated values of capacitance necessary to produce the measured impedances were $C_{par} = 99$ pF/m at 0 V and $C_{par} = 89$ pF/m at -6 V, a difference of only 10% at the two biases. An estimate of 95 pF/m therefore seems reasonable.

Another parameter that is readily measured on the network analyzer is the loss of the line. Figure 4.3 shows the measured transmission through the line at 0 V and -6 V. This measured S_{21} consists of three components: the resistive loss of the transmission line, the diode RC loss, and the impedance mismatch.

For comparison to the measured data, the NLTL loss was calculated using equation 2.7. The transmission line's resistance, R_l, was calculated using the skin effect approximation, and at low frequencies, where the metal is less than a skin depth thick, a modified form for the surface resistivity, R_s, was used [28]:

$$R_s = \frac{1}{2\sigma\delta} \cdot \frac{e^{h/\delta} - \cos(h/\delta) + \sin(h/\delta)}{\cosh(h/\delta) - \cos(h/\delta)} \tag{4.1}$$

where σ is the conductivity of the gold, h is the thickness, and δ is the skin depth.

Freq (GHz)	Bias (V)	Measured S_{21} (dB)	Calculated S_{21} (dB)	Line Loss (dB)	Metal Loss (dB)	Diode Loss (dB)
10	0	-3.9	-4.3	3.7	3.6	0.1
10	-6	-2.4	-2.8	2.7	2.7	0.0
40	0	-9.8	-9.3	8.7	7.3	1.4
40	-6	-6.4	-6.3	5.6	5.4	0.2

Table 4.1: Comparison of measured and predicted values of small signal NLTL loss.

The diode loss was calculated using the values of C_d and R_s that were determined from the network analyzer measurements described in section 3.3.2. The impedance of the line was taken from the measured data, because this has a significant impact on the amount of loss. The impedance mismatch effect on S_{21} was then accounted for, and the three effects were combined to give a predicted value for S_{21}. The results are summarized in table 4.1, and it can be seen that the predictions are in very close agreement with the measured data.

The most important parameter of an NLTL is the change in propagation delay of a wave as the bias on the line changes from 0 V to -6 V, because it is this difference that causes the shock wave formation. This net change in delay, or total amount of compression on the line, is how much the fall time of a signal would be reduced if the NLTL had ideal behavior. In reality, the reduction in fall time is not this large, but it is still a useful parameter to measure because it shows if the lines are behaving as designed. It is a way to make a linear measurement that characterizes the nonlinearity of the line.

Figure 4.4 shows the measured propagation delay of an NLTL when it is biased at 0 V and -6 V. The standing wave pattern is due to the impedance mismatch of the line and becomes less severe at -6 V where the line is much closer to 50 Ω. The propagation delay, T_d, is determined from the measured phase of S_{21}:

$$T_d = \frac{d\phi(S_{21})}{d\omega} \tag{4.2}$$

The total ΔT_d as measured this way is 15 ps but the design value was 20 ps, so the line did not have the correct amount of compression. There were two likely explanations for this discrepancy. The first was that the diodes did not have the right capacitance, but the measurements on both the large area and the 1 μm diodes after the sidewall etch showed that the deviation from theory in the

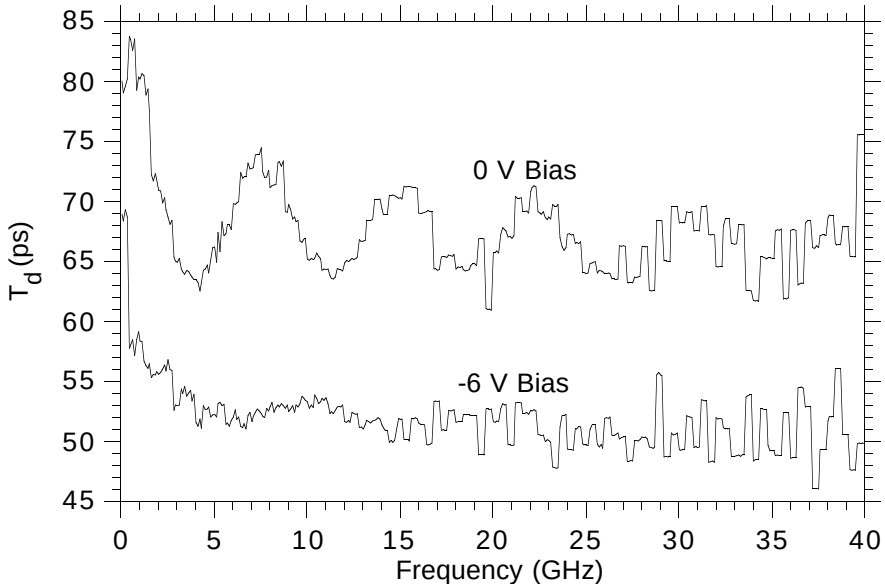

Figure 4.4: The net change in delay of the NLTL is determined by the difference in phase delay when biased at 0 V and -6 V.

C-V characteristics was too small to account for the large reduction in the line compression.

The second possibility was that the parasitic capacitance identified from the impedance measurements was sufficient to cause the reduction in compression. If a parasitic capacitance has increased the line capacitance to a significant fraction of the diode capacitance, then the change in delay with diode bias will be smaller (equation 2.1.) To account for the 25% reduction in line compression, the extra capacitance would have to be 93 pF/m, which is in extremely close agreement with the value deduced from the impedance measurements.

The origin of this capacitance can be seen by examining the cell layout shown in figure 4.5 which shows a cell at the output end of the line that is designed to have $f_{Br} = 800$ GHz. The Schottky contacts of the diodes are on either side of the center conductor of the CPW and the ohmic contacts are embedded in the ground planes. There is significant fringing capacitance between the pads that connect to the Schottky fingers and the ground planes because the lateral dimensions have become so small at the output end of the line. The spacing between the diodes with $f_{Br} = 800$ GHz is 25 μm, so in order for the line to have an average $C_{par} = 94$ pF/mm as determined from the network analyzer data,

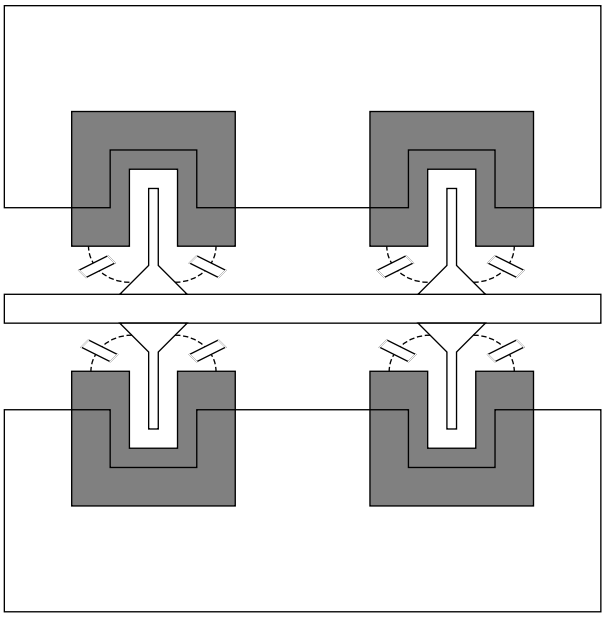

Figure 4.5: Cell layout at the output end of the NLTL where $f_{Br} = 800$ GHz. The fringing capacitance becomes large because of the small lateral dimensions.

there needs only be 2.2 fF extra capacitance in this cell. This is a completely reasonable value given the geometry of the cell.

4.2 Sampling Circuit Measurements

The circuits had been designed to be driven at 30 GHz because the high drive frequency allows the lines to be shorter and thus have lower loss. Two different sampling circuits were designed. The first had a differentiator circuit with a round-trip time of 2 ps and the more aggressive design had only a 1 ps differentiator. Because the lines had less compression than designed, a drive frequency of 40 GHz was used. It was found that the edges produced were fast enough to strobe the samplers with the 1 ps differentiator and that the improved bandwidth of these samplers had an impact on the measured edge speed. Figure 4.6 is a scanning electron microscope (SEM) photomicrograph showing the output ends of the two NLTLs coming in to the sampling circuit and figure 4.7 is a close-up showing the sampling circuit. The two air bridges at the edges of the photograph are the ones that provide the short circuit for the 1 ps differentiator.

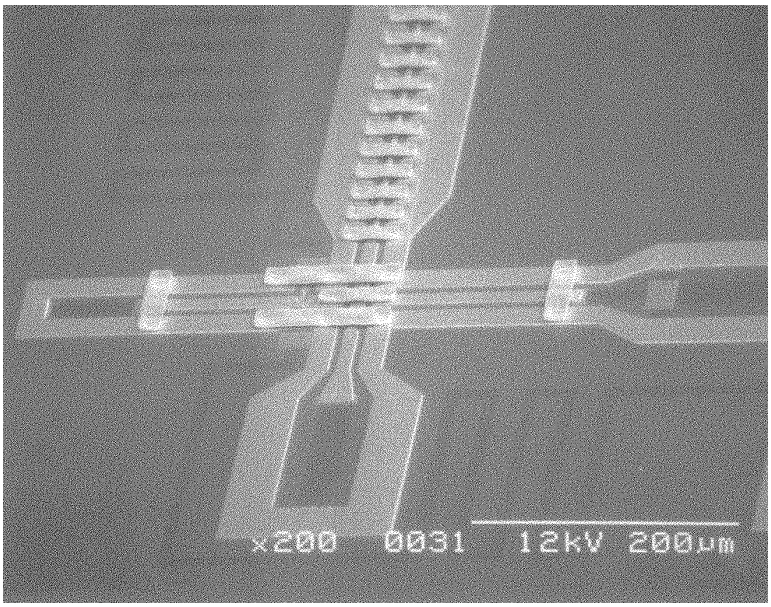

Figure 4.6: SEM photomicrograph showing the output end of the two NLTLs coming in to the sampling circuit.

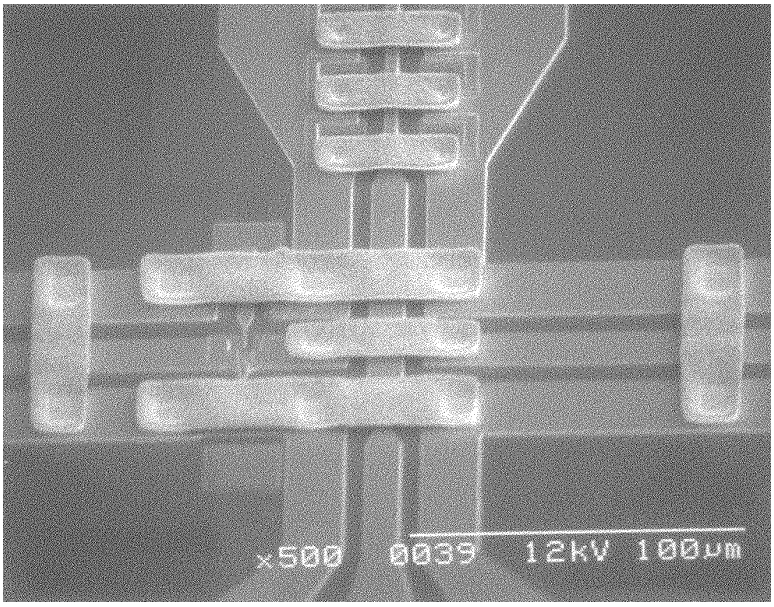

Figure 4.7: Close-up view of the sampling circuit. The two air bridges at the edges of the photograph are the ones that provide the short circuit for the 1 ps differentiator.

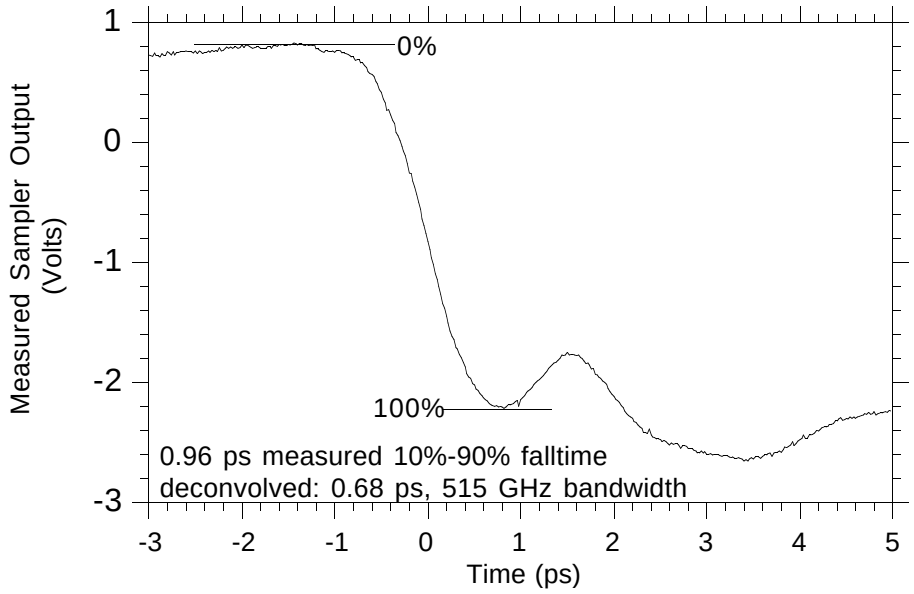

Figure 4.8: Falling edge of the shock wave, with a measured $T_{10-90} = 0.96$ ps. Deconvolved edge speed is 0.68 ps and sampler bandwidth is 515 GHz.

Figure 4.8 shows an expanded view of the falling edge of the measured shock wave which has a 10% to 90% fall time of 0.96 ps. This measured response is the convolution of the shock wave on the NLTL and the pulse response of the sampler. If these two contributions are assumed to be equal (see section 2.3) then a straightforward sum-of-squares deconvolution gives $T_{10-90} = 0.68$ ps and the sampling circuit has a bandwidth of 515 GHz.

Figure 4.9 shows two periods of the waveform. The nonlinearity of the line is well illustrated by this figure when it is considered that the input drive signal was a sine wave. The ringing on the shock wave that can be seen has a frequency of 720 GHz, lower than the design Bragg frequency of 800 GHz. If an additional capacitance on the line of 94 pF/mm was present due to parasitics as determined from the network analyzer data, then the Bragg frequency should have been lowered to 715 GHz, in extremely close agreement with the observed ringing.

The loss on the lines was significant and had to be overcome in order to measure the fast response. As discussed in section 2.1.2, the loss in shock amplitude leads to a reduction in the amount of compression the wave undergoes while traveling down the line. In order to compensate for the line loss, the NLTL was gradient biased such that the peak of the waveform was always near 0 V. This

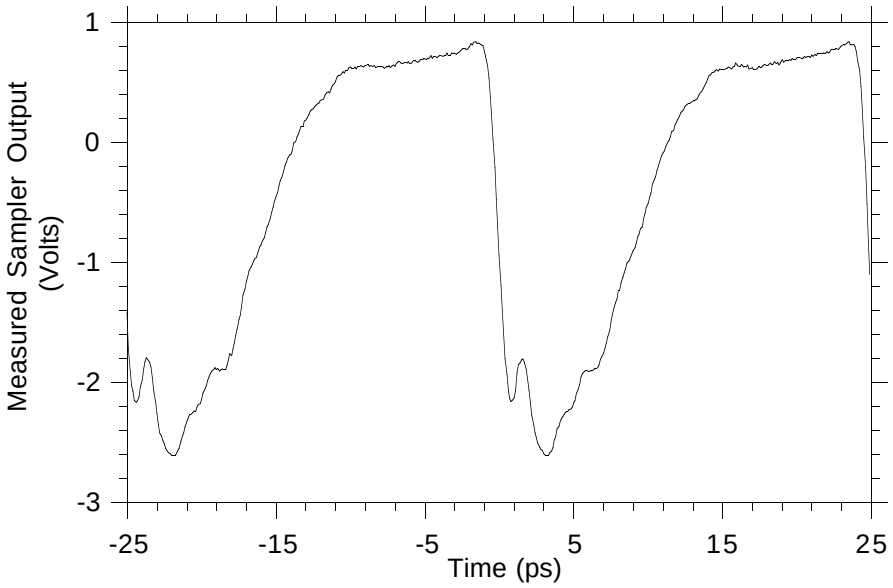

Figure 4.9: Two periods of the measured signal showing the ringing on the output at $f_{Br} = 720$ GHz.

was accomplished by bringing down a needle probe at the output end of the line to provide a second dc bias port. Because the dc probe has a very high inductive impedance, it had no effect on the high frequency signal. By biasing the output end of the line at a less negative voltage than the input, the effect of the line loss on compression was negated. While this method was effective, it was not a good long term solution because the difference in voltage between the input and output forced a large current to flow down the center conductor. At the output end of the line where the center conductor was narrow, the current level was as high as $1 \cdot 10^6$ A/cm^2 which would cause electromigration problems in the Au.

4.3 Limitations

The purpose in carefully analyzing the circuits was twofold. The first was to identify how and why the lines differed from their designed values and the second was to determine which parameters of the NLTL needed to be improved in order to increase the circuit performance. The measured edge speed of 0.68 ps was in very close agreement with what had been predicted with SPICE (see figure 2.6), but it was attained under very different drive conditions than had been used in

the simulation.

The small cells at the output end of the line contributed a number of limitations to the shock line performance, especially the parasitic capacitance and loss. Referring back to figure 4.5, it can be seen that the diodes are physically as close as they can be without having one diode interact with the one in the adjacent cell. This layout limitation put an upper limit on the Bragg frequency that could be attained, since f_{Br} is inversely proportional to the diode spacing. Because f_{Br} was further reduced by the parasitic capacitance of the cell, it became one of the significant limitations to the NLTL speed. The other detrimental effects of the capacitance on the shock wave have been discussed previously.

The other major limitation of the NLTLs that produced the 0.68 ps edge was the loss, much of which came from the narrow transmission line at the output end of the NLTL. One of the results of this, the loss of compression, was offset by using the gradient biasing technique. The other problem which this did not help was that it made the breakdown requirements of the diodes on the line very high. In order to get a 3 V step function at the output end of the line, a sine wave with a peak to peak voltage of 12 V needed to be applied at the input end. As discussed extensively in section 3.1, a large V_{Br} requires lighter doping in the $N-$ region of the diodes and this increases the series resistance of the diodes. If the loss on the NLTL could be reduced, the breakdown requirements for the diodes loading the line would diminish, and diodes with a higher f_{cls} could be used (figure 3.4). This would further reduce the loss on the line and also increase the speed of the shock edge that could be obtained, according to equation 2.3.

There was also one major limitation to the sampling circuit bandwidth, the RC rise time of the sampling diodes, as given in equation 2.10. One way this could be improved would be by using diodes with a lower series resistance, which could be done if the breakdown requirements could be reduced, as described above. The second way would be to make the sampling diodes smaller so that the capacitance of each diode would be reduced. The problem with that is that, as discussed in section 3.3.1, when the diode stripe length is less than 3 μm, the ion implantation causes significant damage to the $N-$ region and greatly degrades the diode's performance. This need to reduce the area of the sampling diodes meant that a new technique had to be developed in order to make very small diodes that could maintain their cutoff frequency.

Chapter 5

NLTLs With Air Bridged Transmission Lines

It was found from the analysis of the results of the NLTLs that produced the 0.68 ps edge that the cell layout at the end of the lines was placing a severe limitation on the high frequency operation of the lines. The proposed solution was to fabricate a transmission line with the center conductor elevated above the substrate because this addresses the two critical problems of parasitic capacitance and low Bragg frequency. Air bridged interconncections have often been used in high frequency ICs to reduce the capacitive loading of the wiring, but for the NLTL application, the technique had to be extended much further. Figure 5.1 is a cross-sectional view of a coplanar line with such a geometry and shows the contours of equipotential as determined by a quasi-static electromagnetic simulator [29].

Because the electric field lines for this structure are predominantly in air, the capacitance per unit length of the transmission line is decreased, resulting in an increase in velocity of the waves on the line, $v = 1/\sqrt{L_{line}C_{line}}$. With an increase in the wave velocity, for the same physical separation between the diodes, the electrical separation increases, increasing f_{Br}. An additional benefit from the lower capacitance is that a wider center conductor is needed to obtain the same characteristic impedance, so the resistive loss goes down. Others have used this feature in an attempt to reduce the loss at the low frequency end of the line [30], but this effect is partly offset by the fact that the line must be longer because of the increased velocity. The real impact of the air lines is at the output end of the line where the parasitics are severe and the high Bragg frequency is needed.

With the center conductor suspended in air, it becomes possible to contact

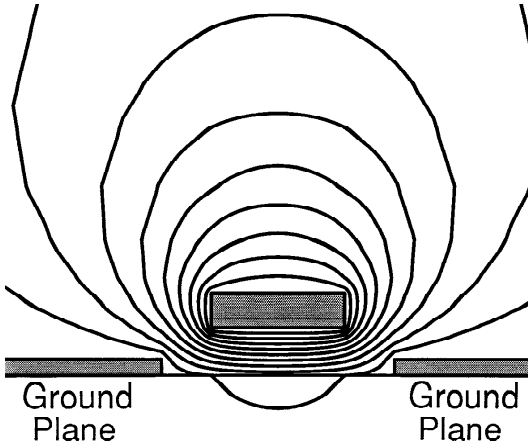

Figure 5.1: Quasi-static simulation showing the lines of equipotential for a coplanar waveguide with the center conductor elevated 3 μm above the GaAs substrate.

the Schottky diodes on the NLTL without touching the GaAs substrate, so the parasitic capacitance from the diode pads will be substantially reduced. Figure 5.2 is a cross-sectional diagram of the NLTL showing how this can be accomplished. The support for the air bridged transmission line is provided by the Schottky diodes, and the contacts to them are made with a pad that remains in air.

5.1 Process Development

The process was based on the electroplated air bridge process that was described in section 3.2.6. Measurements showed that the resistivity of the plated gold was the same as for evaporated gold, so using the plated air bridges as the center conductor would not adversely affect the loss. The part of the process that needed development was a method for keeping the contacts to the diodes suspended in air. This was accomplished by using a planarizing layer of polyimide before the electroplating process. The details of the process flow are illustrated in figure 5.3. The polyimide process development relied heavily on a process flow developed for ridge waveguide lasers [31] and is similar to one that is used to contact the emitters of high speed HBTs [32].

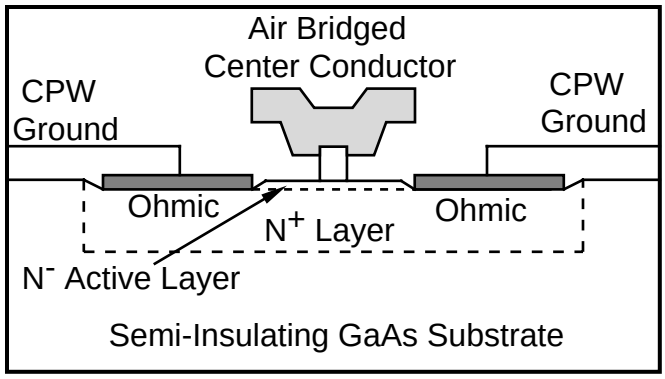

Figure 5.2: The air bridged center conductor contacts the Schottky diodes without touching the GaAs substrate, so the parasitic pad capacitance is greatly reduced.

After finishing the first three process steps described in section 3.2 so that the Schottky diode fabrication was complete, a 1 μm layer of polyimide was applied to the wafer (figure 5.3 (a)). The polyimide was partially cured at a temperature not high enough to crosslink the polymers because the final step in the process flow was to remove the polyimide. Next, a layer of 3 μm thick photoresist was applied to provide a further degree of surface planarization (figure 5.3 (b)). These layers were then etched in an oxygen RIE system where the etch depth could be monitored with a laser. The dielectric layers on the surface of the wafer formed an impedance match for the laser beam and so as the layers were etched, a strong standing wave pattern was observed in the power of the reflected light. Because both the refractive indices and the etch rates of the polyimide and photoresist were almost identical, the standing wave pattern could be used to determine the amount of material that had been removed. It was found that after the laser signal went through 22 complete cycles of the standing wave pattern, the tops of the Schottky diodes were exposed (figure 5.3 (c)).

The air bridge process was then carried out as before. After patterning the post holes for contacting the tops of the diodes and interconnect metal, a thin flash layer of Ti/Au/Ti was sputtered (figure 5.3 (d)). The air bridges were patterned with 3 μm thick photoresist on top of the flash layer, the first layer of Ti was etched, and the lines were electroplated (figure 5.3 (e)). The final steps involved removing the photoresist and flash layers and then removing all of the polyimide so that the electroplated lines were left suspended completely in air (figure 5.3 (f)).

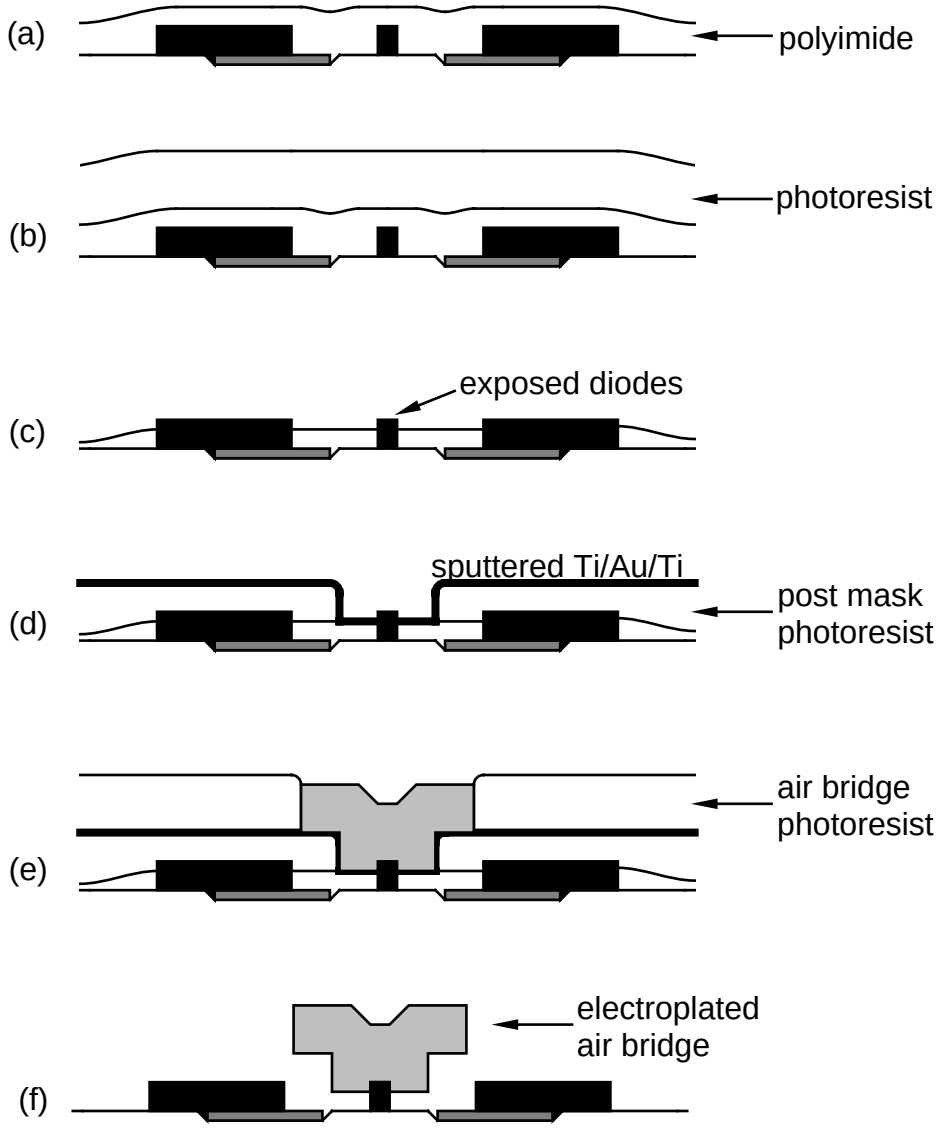

Figure 5.3: Process flow for air bridged transmission lines.

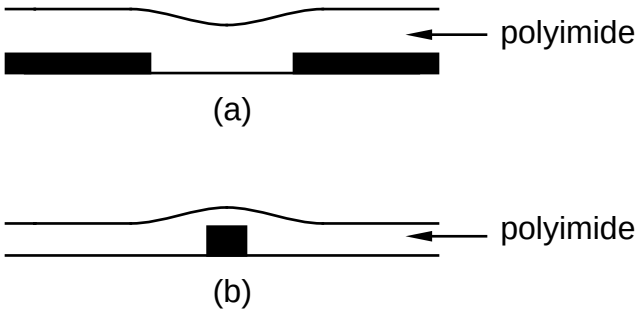

Figure 5.4: (a) When there is a small gap in a large plane of metal, the polyimide in the gap is thick, but still dips. (b) When there is a small feature in an open area, the polyimide on top of the metal is thin.

The term "planarization" for this technique is somewhat of a misnomer. The polyimide conforms to the local features of the wafer in a manner that can be described as a spatial low pass filter, with the polyimide following slow but not rapid variations in surface topography, and this is best understood by way of illustration. When there is a small gap in an otherwise uninterrupted plane of metal, the polyimide is still very thick when measured from the surface of the wafer but will dip in the region of the gap, figure 5.4 (a). When there is a small metal feature in an otherwise vacant area, the polyimide will form a bump that will be thin when measured from the top of the metal, figure 5.4 (b). This geometric dependence is of utmost importance when designing the circuit layout, because it governs which features will be exposed first when the polyimide is etched.

It was desired to have 1 μm of polyimide left after the O_2 etch, so in order to cleanly expose the tops of the Schottky diodes, the metalization had to be $\approx$ 1.5 μm thick. Making 1 μm features that were 1.5 μm high required a new photolithography process because it was difficult to accurately define 1 μm lines in photoresist that is very thick. The solution was to use a surface imaging technique, where a thin layer of photoresist was used to define the pattern and a second layer underneath was used to give the thickness. This process flow is diagrammed in figure 5.5. The first layer is 2 μm of SAL-PL1 [33] which is a photoresist that is sensitive to light at the deep UV wavelength of 210 nm. The SAL is cured at 200 °C and then the second layer, a thin positive photoresist, is applied (figure 5.5 (a)). Because the SAL is cured at a high temperature and is only sensitive to deep UV light, the top layer of resist can be patterned using

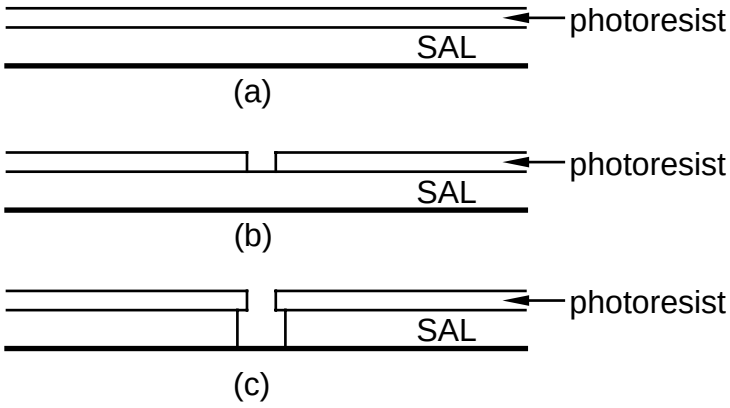

Figure 5.5: (a) 2 μm of SAL-PL1 is applied and then a thin layer (< 1 μm) of positive photoresist. (b) The 1 μm lines are defined in the top layer of resist. (c) The SAL is flood exposed and developed to give a crisp liftoff edge.

the normal photolithography at 365 nm described in section 3.2 (figure 5.5 (b)). After completing this, the wafer is flood exposed at 210 nm and then placed in SAL developer. The flood exposure is long enough to cause some undercutting of the SAL layer, and so a crisp liftoff pattern is defined (figure 5.5 (c)). Appendix D contains detailed process flow sheets for both the 1 μm lithography and the polyimide air bridge process.

5.2 Electrical Characterization

The electrical characteristics of the air bridged transmission lines were determined by measuring a set of lines with a microwave network analyzer. The baseline designs for 75 Ω transmission lines were taken from the results of the quasi-static simulator [29] and then a set of lines was fabricated with perturbations around the nominal dimensions. A cross section of the air lines with the important dimensions defined is shown in figure 5.6. The center conductor, w, was made of differing widths, 8, 12 and 16 μm, because the cell tapering discussed in section 2.1.2 was still applicable. The height off the substrate, h, was chosen to be 3 μm. A sensitivity analysis using the quasi-static simulator showed that with the center conductor this far off the substrate, the characteristics of the line would not be very sensitive to deviations in dimensions due to processing control. Table 5.2 summarizes the measured characteristics of the

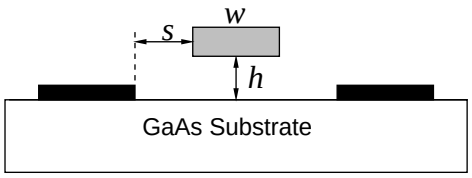

Figure 5.6: Cross section of air line, showing relevant dimensions. w is the width of the center conductor, s,, is the separation between the center conductor and ground, and h is the height above the substrate. h was fixed at 3 μm and the ground planes were always made $2(w + 2s)$.

Width w (μm)	Spacing s (μm)	Impedance Z_0 (Ω)	Velocity vel (10^8 m/s)	Loss at 40 GHz α (dB/mm)
8	3	69	2.21	0.38
8	5	76	2.15	0.33
12	4.5	65	2.07	0.32
12	6.5	72	2.00	0.28
12	8.5	76	1.94	0.25
16	9	70	1.90	0.24
16	11	73	1.81	0.22
16	13	75	1.78	0.22

Table 5.1: Extracted parameters from network analyzer measurements of air lines, with $h = 3.0\mu$m.

lines. Both the line impedances and velocities were about 15% lower than what had been predicted by the quasi-static simulator, which was close enough that the desired 75 Ω lines were within the design space covered. Note also that the loss on the lines did not decrease proportionately with increasing w because of current crowding effects along the edges of the wide center conductors.

A set of calibration standards for the line-reflect-line technique (section 3.3.2) was designed along with the transmission lines so that all of the effects of the pad parasitics would be calibrated out of the measured S-parameter data. Figures 5.7 and 5.8 show typical comparisons of the measured S_{21} data to the model from which the line velocities and attenuation were extracted. Figure 5.9 compares the measured and modeled S_{11} data from which the line impedance was determined.

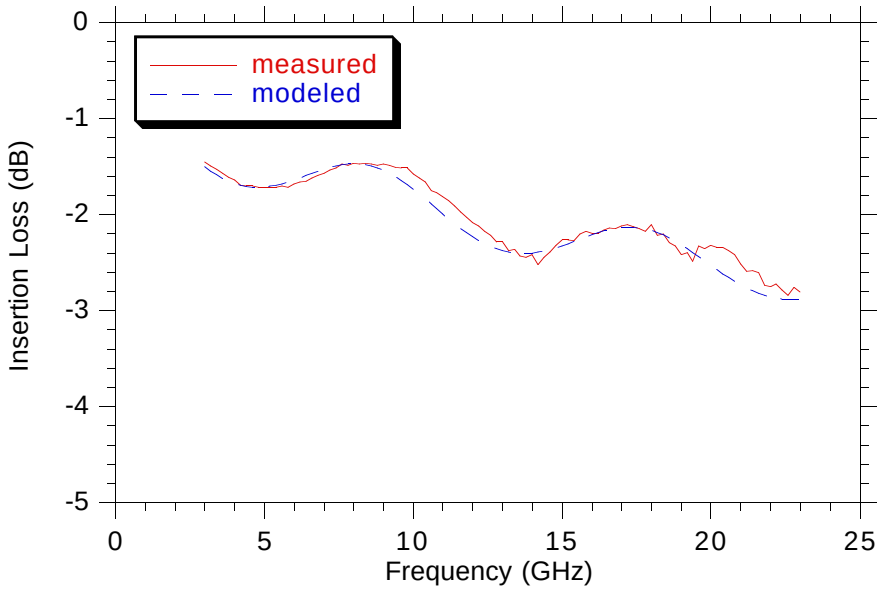

Figure 5.7: Magnitude of S_{21} from which the loss was determined

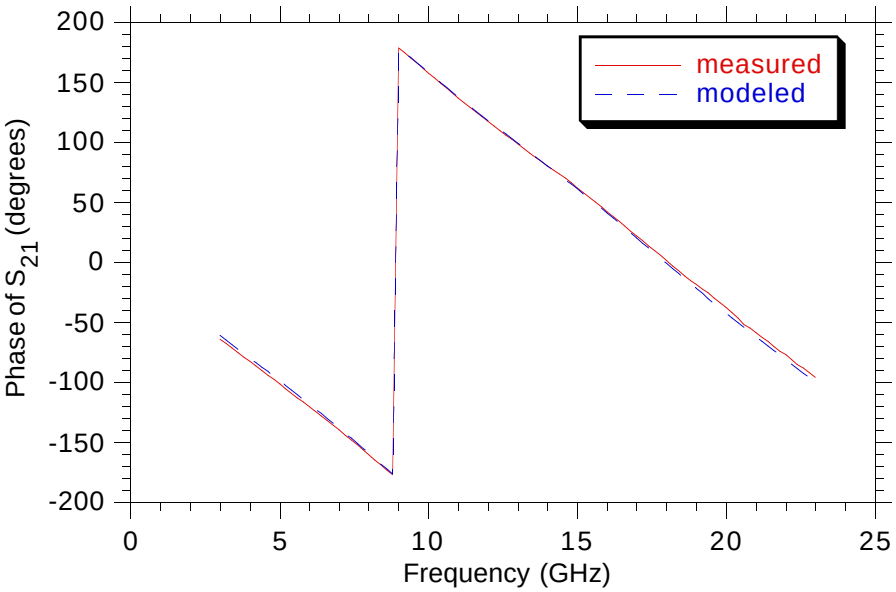

Figure 5.8: Phase of S_{21} from which the velocity was determined.

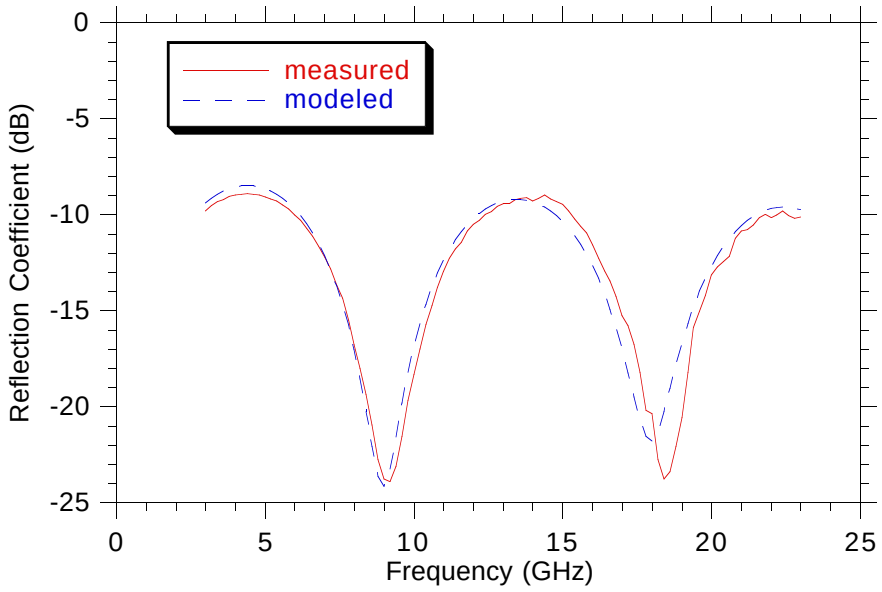

Figure 5.9: Magnitude of S_{11} from which the line impedance was determined.

5.3 Small Diodes

An additional advantage of using the air bridged transmission lines was that it became feasible to fabricate very small diodes that did not suffer from ion implantation damage as described in section 3.3, which was very important for increasing the bandwidth of the sampling circuit. A top view and side view of a 1 μm x 1 μm sampling diode are shown in figure 5.10. A very small Schottky contact can be made in the middle of a large active region and then contacted from the top with an air bridge. Because the area of the diode is defined only by the size of the Schottky contact, the ion implantation mask can be kept well away from this region. This geometry has the added advantage that there is substantial two dimensional spreading of the current in the region between the Schottky and ohmic contacts, and so the periphery-dependent terms of the series resistance are lower than predicted by equations (3.3-3.5). For diodes where the resistance in the $N-$ region is small, this has a significant impact on f_{cls}. For diodes with $N_D = 3.0 \cdot 10^{17}$ cm^{-3}, 1 μm x 1 μm sampling diodes had a cutoff frequency of over 10 THz.

The advantages in making a small diode also help at the output end of the NLTL. Because the velocity on the air lines is twice what it is for conventional

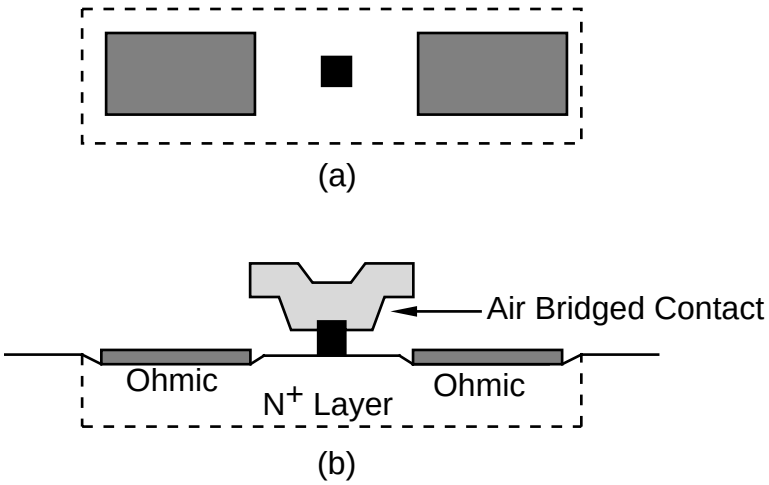

Figure 5.10: Cross section of 1 μm x 1 μm diode that can be contacted from the top with an air bridge.

CPW on GaAs, the Bragg frequency at the output end of the line can be doubled from 750 to 1500 GHz, and this requires a small diode. By placing the Schottky contacts for the diodes directly under the air bridged center conductors, small diodes could easily be incorporated into the NLTL. A perspective drawing of this is shown in figure 5.11 and an S.E.M. photomicrograph of the output end of the NLTL after fabrication is shown in figure 5.12.

5.4 NLTL Design

The air bridged transmission lines solved most of the problems that had been identified as limiting the performance of the 515 GHz circuits, but while they helped to reduce the loss, they did not eliminate it. The biggest problem remaining, then, was the dc walkoff problem described in section 2.1.2 where the nonlinearity of the varactors is lost due to signal attenuation. This effect can be counteracted by engineering the lines so that they have no voltage loss even though they have power loss. The power on a transmission line is

$$P = \frac{V^2}{Z_0} \tag{5.1}$$

where V is the voltage on the line and Z_0 is its characteristic impedance. If the impedance at the output end of the line is larger than the impedance at the

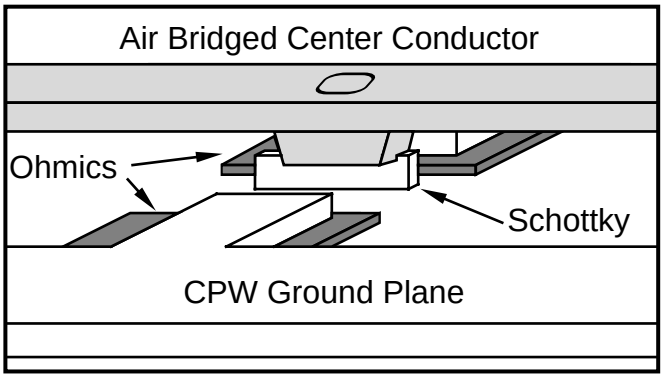

Figure 5.11: Perspective drawing showing the air bridged center conductor contacting the top of a Schottky diode.

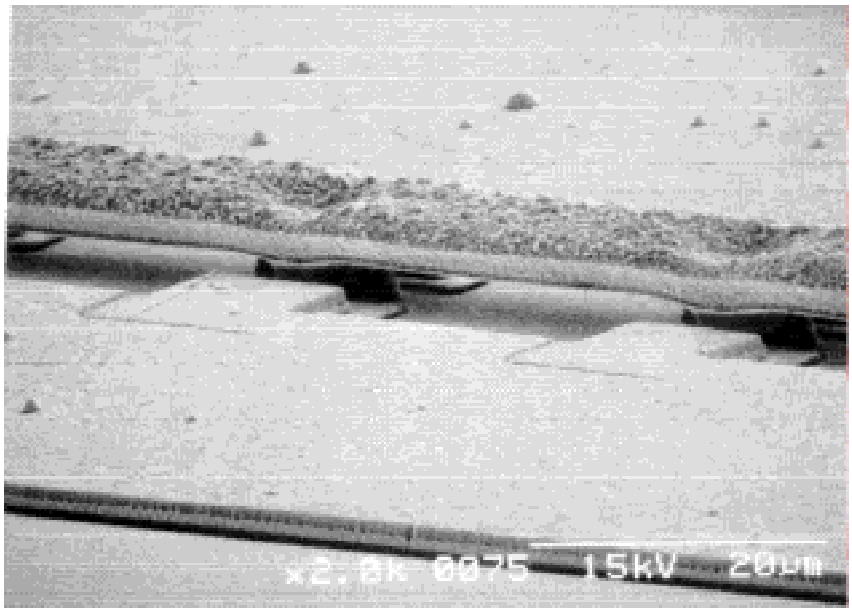

Figure 5.12: S.E.M. of fabricated NLTL at the high Bragg frequency end of the line.

Diode Doping	Compr ΔT_d (ps)	Start f_{Br} (GHz)	End f_{Br} (GHz)	Start Z_{ls} (Ω)	End Z_{ls} (Ω)
1e17	20	260	1500	20	44
1e17	25	260	1500	20	47
3e17	20	260	1500	20	44
3e17	25	260	1500	20	47

Table 5.2: Important design parameters for the air bridged NLTLs with impedance tapering.

input end by the ratio of the powers,

$$\frac{Z_{out}}{Z_{in}} = \frac{P_{in}}{P_{out}} \tag{5.2}$$

then the voltage at the two ends of the line will be the same.

Others have used impedance tapering on NLTLs to match them to a low impedance driver source [34], but for this work the large signal impedance of the lines was tapered to exactly compensate for the power loss on the line so that a large voltage swing would be maintained down the whole line. Because each section of the NLTL was designed to have a higher Bragg frequency and larger Z_{ls} than the preceding section, there was no closed-form expression for determining the parameters of each section of the NLTLs. To design the lines, a computer program was written where the starting Bragg frequency, the ending Bragg frequency, the number of line sections and the starting Z_{ls} were all specified. The parameters for the NLTL were generated by determining the first section of the line, calculating its loss, increasing Z_{ls} proportionately for the next section, increasing f_{Br} and then designing that section of the line. This was done iteratively and the propagation delay for each section was summed. The specified number of sections for the line had to be varied until the desired amount of compression for the entire line was obtained. The computer program that was used can be found in Appendix E along with the output files that included the line parameters, a SPICE file and a layout file. Table 5.2 summarizes the line parameters of four different lines that were designed.

The impedance tapering was based on the calculated loss at 40 GHz because it is the voltage swing at the fundamental frequency that is driving the diodes. Overcompensating for the loss at the drive frequency would be counterproductive because the diodes would be driven into reverse breakdown. The loss at higher

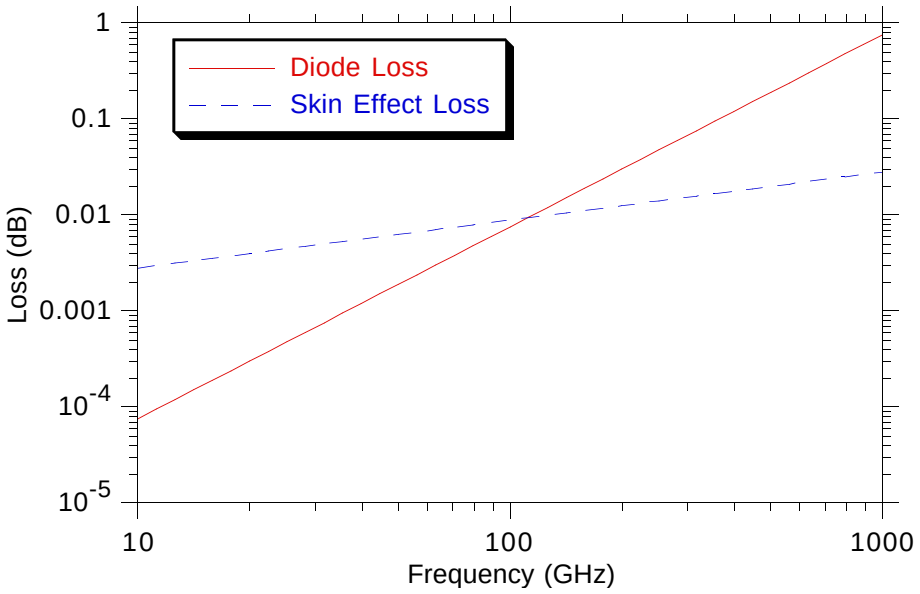

Figure 5.13: Loss mechanisms on a unit cell at the output end of the line, showing that the diode loss becomes dominant above 100 GHz.

frequencies cannot be offset; it can only be minimized. One of the deficiencies of SPICE is that it cannot model the frequency dependent skin effect loss on the transmission lines. To model the loss at the fundamental frequency, a lumped resistor was added after each section of transmission line that was equal to the calculated resistance at 40 GHz. Figure 5.13 shows the diode loss and the skin effect loss of the last cell of the NLTL. Because the skin effect loss is $\propto \sqrt{f}$ and the diode loss is $\propto f^2$, above 100 GHz the diode RC loss becomes dominant. This is accounted for in the SPICE simulation, so all the important loss phenomenon are being modeled.

5.5 Network Analyzer Data on NLTLs

As discussed previously, network analyzer data on test lines provides the most valuable insight to the operation of the lines, so after fabricating the new lines on diodes with $N_D = 1 \cdot 10^17$ cm^{-3}, the same set of data was taken as before. Figure 5.14 shows the measured T_d for the line at 0 V and -6 V bias. This line was designed to have 20 ps of compression and this is almost exactly what the microwave data shows. This indicates that the air lines were successful

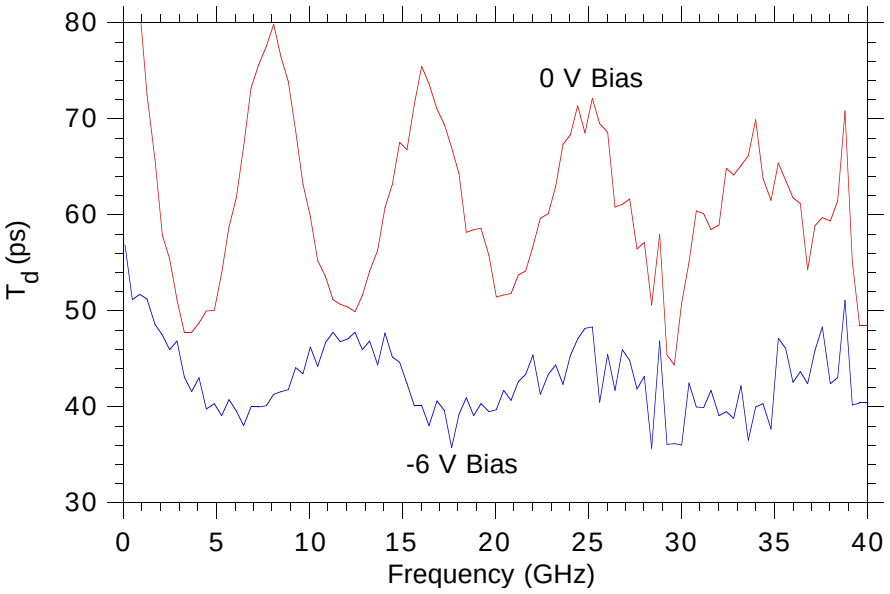

Figure 5.14: Network analyzer data showing the measured delay of an NLTL when biased at 0 V and -6 V.

in eliminating the parasitic capacitance that had caused a 25% reduction in compression on the earlier generation of NLTLs. Lines designed to have 25 ps of compression also had measured delays equal to the design value.

Figure 5.15 shows the measured S_{11} and S_{22} of the line, and it is readily apparent that the impedances at the input and output ends of the line are different. For comparison, figure 5.16 shows the same impedance measurements for one of the previous generation of lines where Z_{ls} was constant along the line. Because of the impedance tapering, it was not possible to extract an exact value for the input and output impedance, but the apparent values were close enough to the design values to believe that the lines were behaving as intended.

5.6 Measured Sampling Circuit Results

The sampling circuits were designed with two different sizes of diodes: 1.5 μm x 1.5 μm and 1.0 μm x 1.0 μm using the technique described in section 5.3. The reason for using the larger diodes for some of the samplers was in case the processing yield on the 1.0 μm x 1.0 μm was low. This did not turn out to be a problem, so the only advantage of having the larger diodes was to compare

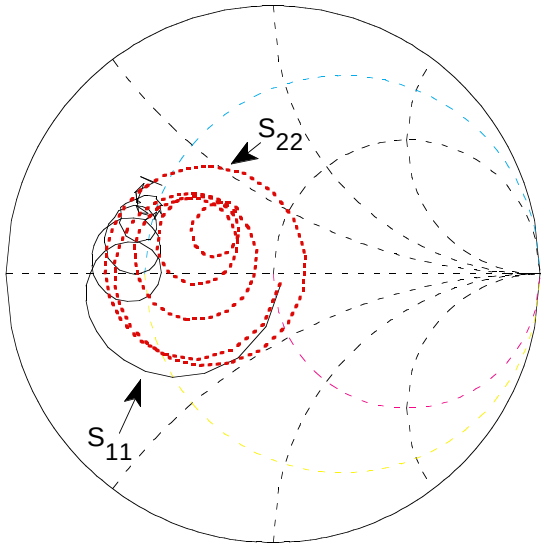

Figure 5.15: Measured input and output impedance of an NLTL designed with a tapered Z_{ls}.

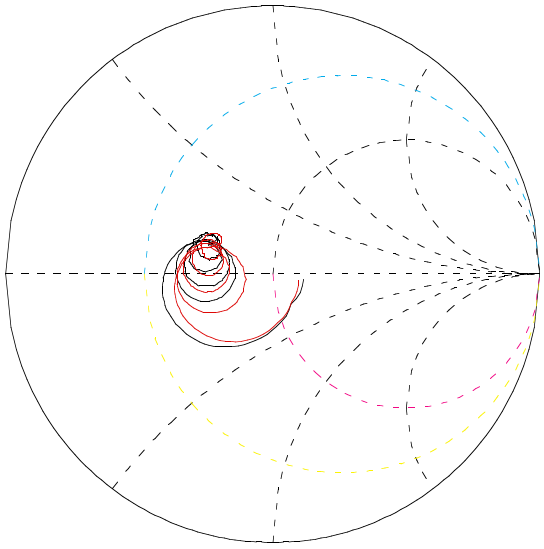

Figure 5.16: Measured input and output impedance of an NLTL from an earlier design where Z_{ls} was constant.

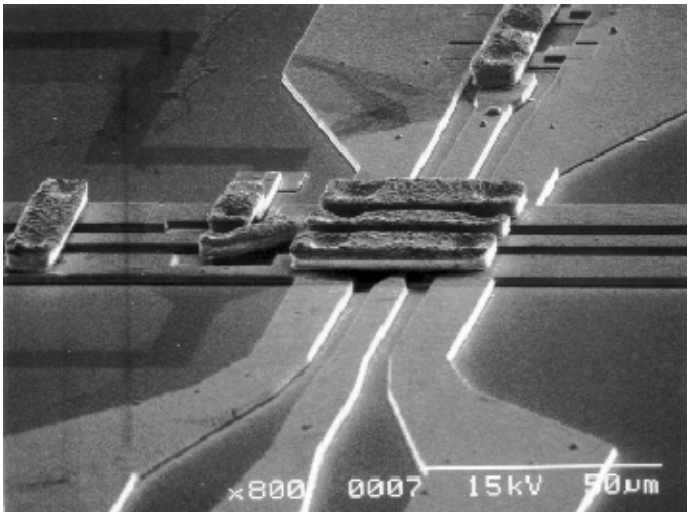

Figure 5.17: S.E.M. image of the sampling circuits with 1.0 μm x 1.0 μm diodes contacted by air bridges. The distance between the diodes and the differentiator air bridge is only 0.6 ps round trip.

the effect of sampling circuit bandwidth on the measured edge speed. For both types of samplers, the differentiator was designed to have a round trip time of 0.6 ps, which was as short as could be comfortably incorporated into the layout. Figure 5.17 shows an S.E.M. of the sampling circuit. The sampling diodes are not visible, but the air bridges contacting them can be seen in the middle of the photograph. The extremely short distance between the sampling diodes and the differentiator air bridge is very evident.

The measured waveform from a line with 1.0 μm x 1.0 μm sampling diodes and 20 ps of compression is shown in figure 5.18 and has a 10% to 90% fall time of 0.68 ps. If the same assumption was made as before that the NLTL and sampling circuit were providing equal contributions to the measured signal, then the sampling circuit has a deconvolved bandwidth of 725 GHz. However, the sampling circuit bandwidth did not appear to be limiting the measured performance. The same edge speed was measured with sampling circuits having both 1.0 μm x 1.0 μm diodes and 1.5 μm x 1.5 μm diodes. Since this changes the RC rise time of the sampling circuit by more than a factor of 2, this indicates that this was not the limiting time constant in the circuit. Edge speeds measured with the older style sampler, with 1.0 μm x 3.0 μm diodes and a 1.0 ps differentiator, were substantially slower with T_{10-90} of 0.92 ps. The new sampling circuits were improved enough to apparently have no impact on the measured shock wave.

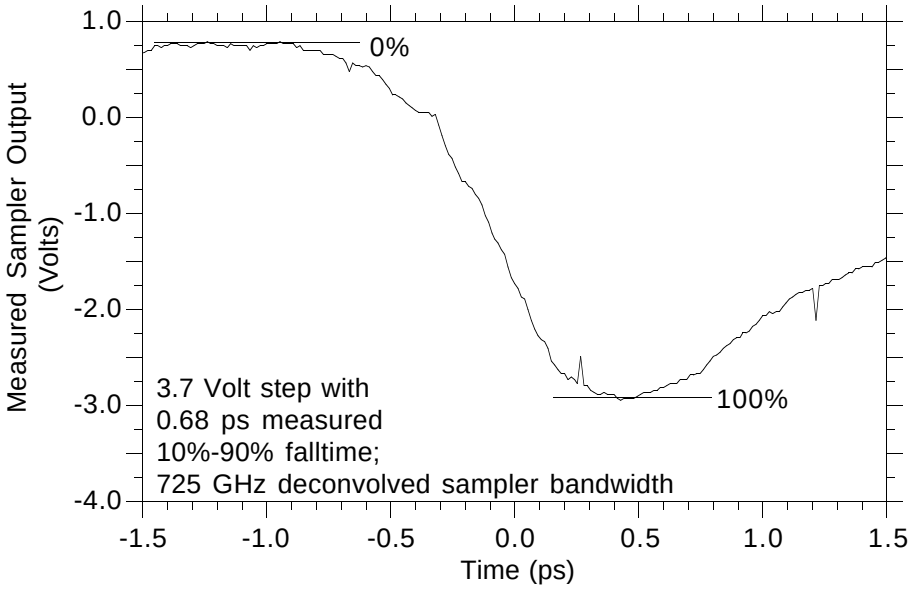

Figure 5.18: Measured waveform with a 10% to 90% fall time of 0.68 ps. Assuming equal contributions of the NLTL and sampler, the sampling circuits have a deconvolved bandwidth of 725 GHz.

The other significant feature of the measurements to discuss is the effect of the impedance tapering. The measured edge has a peak-to-peak voltage 3.7 V, which is 35% larger than was measured on the previous generation of lines. Even more importantly, attempts to improve the circuit performance by using gradient biasing were futile, so the problem with dc walkoff had been solved. Also, the 20 ps lines gave slightly faster edges than the 25 ps lines. The loss of the 25 ps lines was enough larger that the impedance tapering was not enough to completely compensate for the power loss and this affected the performance of the line.

5.7 Limitations

All of the measurements indicated that the air bridged transmission lines had solved the problems identified from the previous generation of circuits. These lines had the right amount of compression, the sampling circuits with 1.0 μm x 1.0 μm diodes were substantially faster, there clearly was no Bragg ringing on the waveform in figure 5.18, and gradient dc biasing was no longer necessary.

The measured edge speed, however, was slower than any of the time constants in the circuit would predict. This is attributed to a velocity saturation effect on the depletion edge movement at the output end of the line.

From the measured voltage swing of the shock wave, it was calculated that the depletion edge of the diodes at the output end of the line moved 145 nm in the 0.68 ps 10% to 9 % fall time, giving it an average velocity of $2.1 \cdot 10^7$ cm/sec, which is the typical maximum velocity for electrons in GaAs. Normally depletion edge movement is considered to be an event that occurs within a dielectric relaxation time, but this is only true when it is a small signal phenomenon. In the case of the NLTL, where large voltage swings are present, the edge of the depletion region has to physically move the entire 145 nm, and so the small signal analysis is no longer valid.

This velocity saturation problem has also been encountered by people working with high frequency varactor multipliers [35]. In these studies, it was found that the measured power and efficiency of the multipliers under high drive powers were significantly smaller than had been predicted even though the predictions were reasonably accurate at lower drive powers. Careful calculations showed that the power began to saturate at drive levels where the depletion edge movement exceeded about $2 \cdot 10^7$ cm/sec. In follow up work, varactor diodes were designed specifically to address this problem by increasing the doping levels, and the result was an increase in output power of 300% for the same size device [36].

The solution to this problem in the context of NLTLs is the same: to use diodes with heavier doping. The distance the depletion edge moves is inversely proportional to the doping (equation 2.1), so by increasing the doping level from 1 to $3 \cdot 10^{17}$ cm^{-3}, for the same voltage swing the depletion edge only has to move $\sqrt{3}$ as far. It was in anticipation of this problem that on the same mask set lines were designed with both levels of diode doping. The experiments with the initial process run on the heavier doped diodes did not lead to conclusive results. The 1 μm diodes had anomalously high capacitance per unit area, and since the sampling diodes would have $\sqrt{3}$ more capacitance any way, it appeared that the measurements were sampler limited. Attempts are being made to find a way to simultaneously have fast diodes at the output end of the line and still have low capacitance sampling diodes. This will be the focus of the work that carries on from this thesis project.

Chapter 6

Future Development of NLTLs

In order to get beyond 725 GHz, the diode design tradeoffs have become more complicated. On the NLTL, increasing the doping in the N- region leads to an increase in speed because the shock wave fall time is limited by the RC product (equation 2.3) and the resistance of the diode decreases faster than the capacitance increases. The situation is not the same in the sampling circuit. Each sampling diode is effectively loaded by a 50 Ω termination and so when the diode resistance becomes small compared to 50 Ω, reducing R_s further has little effect. This means that as the doping in the diode is increased, the sampling circuit charging time is increasing as $C_d \cdot 50\ \Omega$ and the sampling circuit bandwidth begins to decrease with increasing diode doping.

This was apparently the problem with the first attempt to make the circuits with diodes doped at $N- = 3.0 \cdot 10^{17}$ cm$^{-}3$. With only $\sqrt{3}$ more capacitance, this was not expected to be a problem yet, but because the diode capacitance per unit area was anomalously high, it was enough to slow down the sampler. This conclusion that the speed was sampler limited was corroborated by the fact that the signals measured with the 1 μm x 1 μm diodes were faster than those measured by the 1.5 μm x 1.5 μm diodes.

The proposed solution was to have two different types of diodes on the line: one that was lightly doped in the sampling region and another that was doped with $N- = 3.0 \cdot 10^{17}$ cm^{-3} on the rest of the line. To make things even better, a hyperabrupt doping profile was used for the lightly doped layer, allowing for three different diodes to be used in the circuit, as shown in figure 6.1. At the input end of the line, the hyperabrupt doping profile gives 14 V breakdown and a 4:1 change in capacitance at the expense of diode cutoff frequency. This layer was then etched off at the output end of the line where the fast diodes were

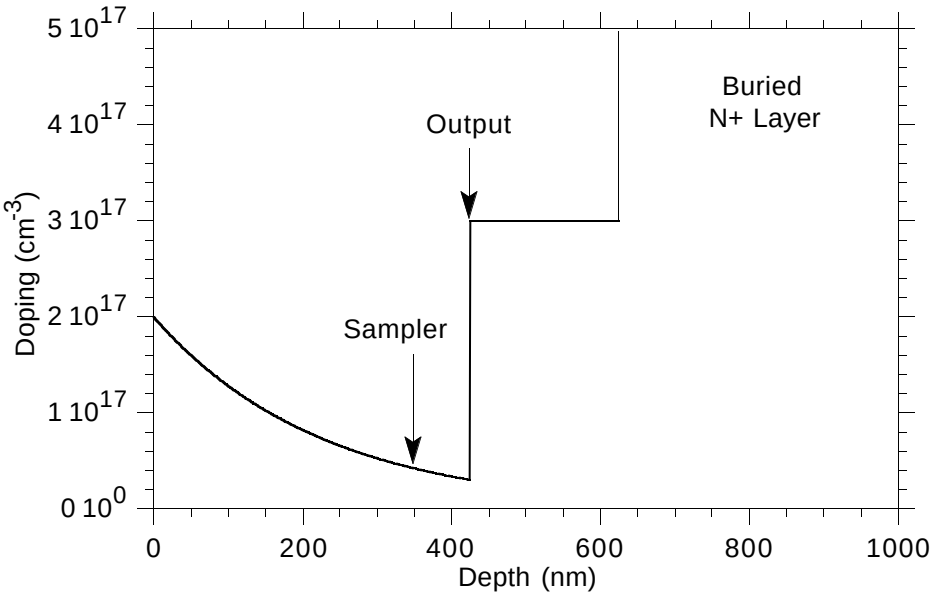

Figure 6.1: Three step doping profile used in an attempt to make faster samplers. At the input end of the line, the hyperabrupt diodes have a large breakdown voltage and strong nonlinearity at the expense cutoff frequency. At the output end of the line the breakdown is lower but the diodes are extremely fast. The sampling diodes are designed to have as small a capacitance as possible.

needed. The velocity saturation limit of these diodes is 0.39 ps (0.68 ps/$\sqrt{3}$), which is the edge speed predicted by the SPICE simulation that includes all the other effects. To make the sampling diodes, the hyperabrupt layer was etched down until only 150 nm of extremely lightly doped material was left, giving them a very small capacitance and a smaller rise time of only 120 fs.

The measured waveform from these circuits is shown in figure 6.2 and has an extremely slow fall time of 1.6 ps. At this point, the circuits should not be diode limited on either the NLTL or the sampling circuit and so there must be something more fundamental wrong with them. There was a very strong interference signal on which the sampled waveform was superimposed, and the outputs from the two sampling diodes were significantly different. The conclusion from this is that the sampling circuit layout needs to be changed in order to suppress the interference signal and achieve a better balance between the two sampling diodes. It is not understood at this time why this problem wasn't as severe with the more lightly doped diodes that produced the 725 GHz result.

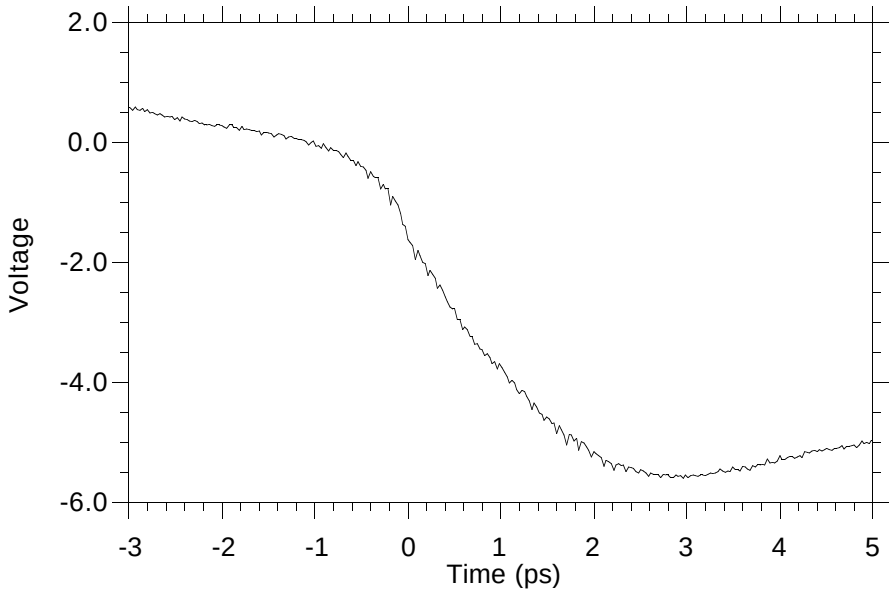

Figure 6.2: Measured waveform from the three step wafer showing a very slow edge speed of 1.6 ps.

6.1 Reaching 2 THz Bandwidth

If the problems with the sampling circuit layout can be easily fixed, then the approach for pushing the technology to 2 THz would follow almost the exact same route as the path from 500 GHz to 1 THz. The requirements are: (1) a smaller RC time constant for the diodes at the output end of the line; (2) a shorter depletion edge movement for these diodes; (3) a higher Bragg frequency at the output end; and (4) smaller sampling diodes.

Solutions to the last two are the easiest because they do not require any epitaxial doping profile design or any new technology development. To increase the Bragg frequency, the air bridged coplanar waveguide technology can readily be extended to making air microstrip lines. By connecting the two CPW ground planes together underneath the center conductor, the line becomes microstrip with all field lines in air and so the velocity must be $3{\cdot}10^8$ m/s, 50% higher than for the CPW lines. With the diode spacing at the end of the line reduced to 18 μm, f_{Br}=2800 GHz.

The area of the sampling diodes can be reduced by going to electron beam lithography. Using the technology developed for the submicron Schottky collec-

tors discussed in the next chapter, sampling diodes can be defined that are as small as 0.25 μm x 1.0 μm. The E-beam lithography will also help with the Bragg frequency issue. One of the limits to how closely packed the diodes can be is the alignment tolerances that required for contact lithography. By using E-beam written diodes at the output end of the line, the registration error between the Schottky fingers and ohmic pads becomes negligible. Reducing the diode spacing to 18 μm from 25 μm then creates no problems at all. Also, because the transmission line is completely shielded from the semiconductor, there is no need to worry about an ion implantation mask in this region, and so another alignment tolerance is eliminated.

6.2 Diode Design

Addressing the first two issues is much more difficult because the constraints on the diode have become much more severe. The tradeoff between speed and breakdown has become unmanageable. A two step doping profile will be required: one at the input end of the line that has sufficient breakdown and a second one at the output end of the line that meets the speed requirements. The best solution would be to use one of the 725 GHz lines discussed in the previous chapter as a driver for a high speed output stage. With a 0.68 ps, 4 V incident edge, the output stage would not need much compression nor have to sustain very large voltages.

Because these proposed strategies are essentially technology that has already been demonstrated for this thesis project, almost the entire burden falls on the high speed diode design. A simple calculation sets the starting point for the design. A 2 THz shock wave has a 10% to 90% fall time of 175 fs, 3.9 times faster than the measured 0.68 ps edge. Assuming velocity saturation, the doping has to be increased by the square of this, so the $N-$ doping would have to become $1.6 \cdot 10^{18}$ cm^{-3}. The activation of dopants at this high a doping level becomes quite variable, and so a different approach is required.

The solution proposed here is to use a delta-doped diode where a sheet of Si dopants is deposited at the plane at which the 0 bias depletion depth is desired, making this distance insensitive to the other doping parameters. If the saturation velocity remains at $2{\cdot}10^7$ cm/sec, the depletion edge can only move 30 nm in 160 fs. The best compromise for the diode design is to have this result in a 2:1 capacitance change instead of the 3:1 used previously. Because the amount of compression needed in the output section of line will be small, it is preferable to trade speed for nonlinearity in the diode.

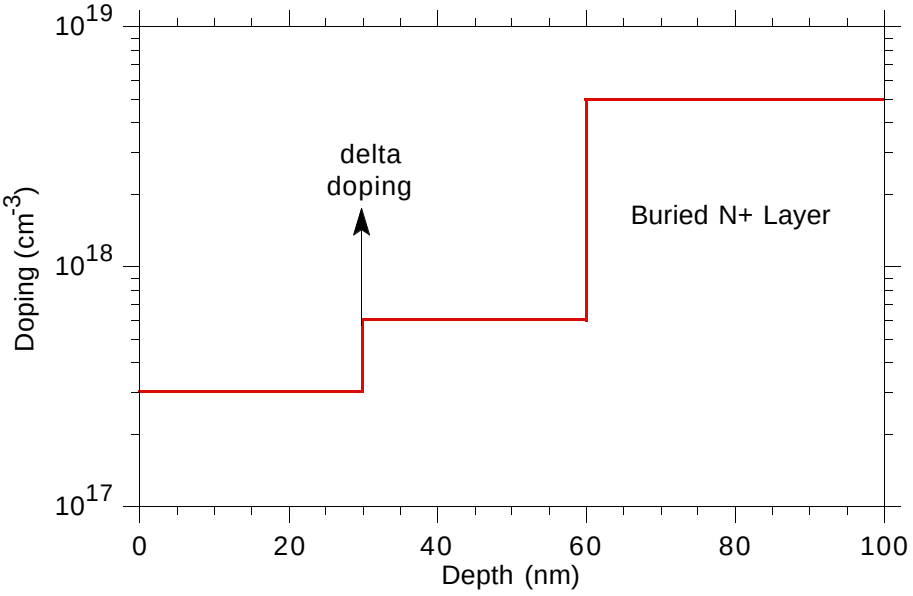

Figure 6.3: Doping profile of proposed diode which has C_{jo}=3.8 fF and $R_s = 5$ $\Omega \cdot \mu$m^2

The proposed doping profile is shown in figure 6.3. The surface is doped with $N = 3.0 \cdot 10^{17}$ cm^{-3} because the breakdown properties of this material were well characterized during this thesis work. Next comes a sheet of donors at 30 nm with $\sigma = 3.5 \cdot 10^{12}$ cm^{-2}, a value within the range of what is commonly used for delta-doped HEMTs. The next layer is again 30 nm thick, which defines the depletion edge movement, and is doped $N = 6.0 \cdot 10^{17}$ cm^{-3}. Figure 6.4 shows the electric field profile of the diode at the punch through voltage of 2.9 V. The maximum electric field at this point is $8.7 \cdot 10^5$ V/cm, which is the measured breakdown field of the diodes doped with $N = 3.0 \cdot 10^{17}$ cm^{-3}.

Once again, the tradeoff between R and C that was discussed in chapter 2 is no longer valid because the capacitance is being determined independently from the doping level by the placement of the delta doping. The E- beam diodes provide the solution to the problem. The thin heavily doped region reduces the vertical resistance in the diode to 1 $\Omega \cdot \mu$m^2, so the resistance becomes dominated by the periphery dependent terms. By scaling the diode to 0.25 μm width and reducing the Schottky to ohmic separation to 1.0 μm, the total resistance of the diode becomes 5 $\Omega \cdot \mu$m^2. Figure 6.5 shows a SPICE simulation using this diode. With a 4 V, 1 ps input step, a 170 fs shock wave is generated, meeting

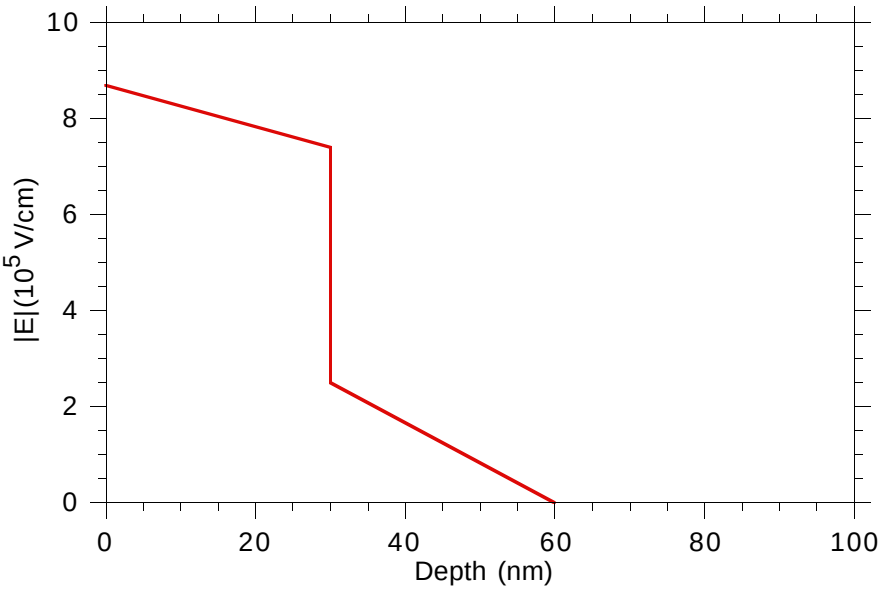

Figure 6.4: E-field profile of the proposed diodes at the punch-through voltage.

the design goal of 2 THz. A sampling circuit with 0.25 μm x 1.0 μm diodes on this material will have an RC time constant of 120 fs. The narrow depletion region is important for the sampling diodes as well or else their response time would also become transit time limited at these very high speeds.

The one problem with the proposed design is how to integrate it into a two-step doping profile. The delta-doped diode must be on the bottom because any series resistance from a diode underneath it would ruin any of its speed advantages. This means that the top layer must be etched off at the output end of the line and in the sampling circuit. The technological challenge here is that 200 to 300 nm of material must be etched off and then the etch has to stop very precisely in order to define the 30 nm 0-bias depletion depth for the buried diode. This should be manageable with a slow H_3PO_4 based etch that etches at 50 nm/min, but it is not trivial. A dry etch is not workable because without a heterojunction there is no way to use a laser to monitor the etch depth.

6.3 Conclusion

There is still some work to be done to push the sampling circuit bandwidth to 1 THz, but if these problems, which are believed to be relatively minor, can be

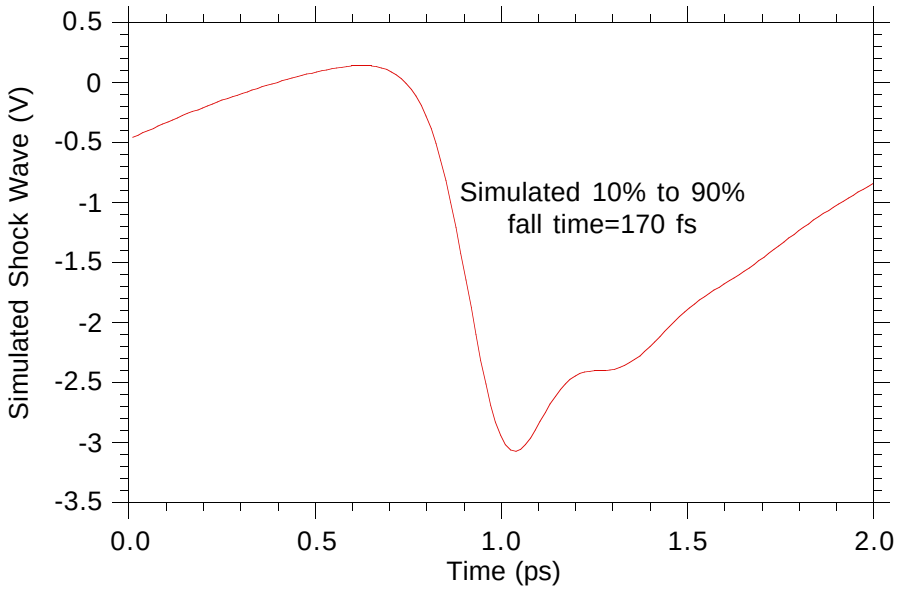

Figure 6.5: SPICE simulation of 170 fs shock wave using the proposed diode. The line is designed assuming air microstrip transmission lines, f_{Br}=2800 GHz, and ΔT_d=0.8 ps. The input signal is a 3 V, 0.8 ps step function.

worked out, then the path to 2 THz is straightforward. By going to E-beam sampling diodes and air microstrip lines, only the varactor diode performance remains as a limit. It is possible that at time scales < 200 fs and distances $<$ 300 Å, there will be significant deviations in device performance from what has been already observed, so the diode design may not have to be as aggressive as the one proposed. The project becomes one that is primarily an exploration of high frequency device physics and should be both interesting to the researcher and valuable to the scientific community.

Chapter 7

Schottky-Collector Resonant Tunneling Diodes

Resonant tunneling diodes (RTDs) are of interest because they have a region of negative differential resistance that can be used in circuits to generate oscillations at frequencies well above the operating range of transistors. In the AlAs/GaAs system, oscillation have been reported at frequencies as high as 420 GHz [37]. In the InAs/AlSb system, waveguide oscillators have been operated as high as 712 GHz [38].

In this work a new type of RTD, the Schottky-collector resonant tunneling diode (SRTD) was investigated. The idea behind this device was that by replacing the conventional ohmic contacted collector with a Schottky contact, all of the advantages of device scaling that had been studied for the varactor diodes could now be applied to the RTD. SRTDs with 0.1 μm wide Schottky collectors similar to those used for T-gate HEMTS [39] were fabricated in the AlAs/GaAs system. From their measured dc and microwave parameters a maximum frequency of oscillation, f_{max}, of 900 GHz was calculated, at least twice as high as for any previously reported RTD in this material. By applying the Schottky collector technique to RTDs in the material system of AlAs/InGaAs latticed matched to InP, an f_{max} greater than 2 THz is expected.

7.1 Theory of RTD Operation

The conduction band diagram of an RTD is shown in figure 7.1. The quantum well region is formed with two layers of a wide bandgap material, typically AlAs, on either side of a well that is usually 40 to 60 Å wide. The shaded region in

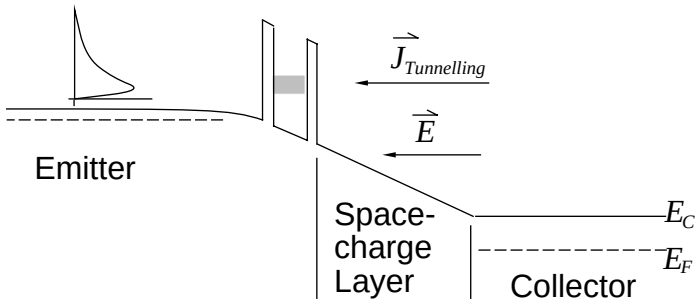

Figure 7.1: Conduction band diagram of an RTD under forward bias. The shaded region represents the quasi-bound state in the quantum well. The energy distribution of the electrons in the emitter is also indicated.

the quantum well in the figure represents the energy level of the quasi-bound state in the well. On one side of the quantum well is an undoped space-charge region which the electrons transit under high electric field. On the other side of the quantum well is the emitter which provides the source of electrons for the tunneling process. The curve above the emitter in the figure represents the energy distribution of the electrons.

As indicated in the diagram, a forward voltage is applied to the diode to create an electric field across the quantum well and space-charge regions. As the energy level of the qausi- bound state in the well is lowered with respect to the electrons in the emitter, an increasing number of electrons are available to participate in the tunneling process and the current through the diode increases. This continues until the electric field across the diode is such that the energy level of the bound state coincides with the energy level at which the peak in the emitter electron distribution occurs. Beyond that point, a fewer number of electrons are available to tunnel and the current actually decreases for increasing voltage. This is the phenomenon that gives rise to the region of negative differential resistance. Beyond a certain level, the barriers become low enough that there is a substantial amount of thermionic emission over them and the current again begins to rise with a continued increase in the voltage (figure 7.2).

The important points of the curve are the peak current, I_p, the voltage at which this occurs, V_p, the minimum, or valley, current, I_v, and the valley voltage, V_v. One of the parameters that is used to characterize an RTD is the peak to valley ratio (PVR) of the current, I_p/I_v. The other key parameter is the negative conductance, G_n of the diode. For calculating the diode's f_{max}, the small signal G_n is used, and this is taken to be the maximum of the slope in the negative

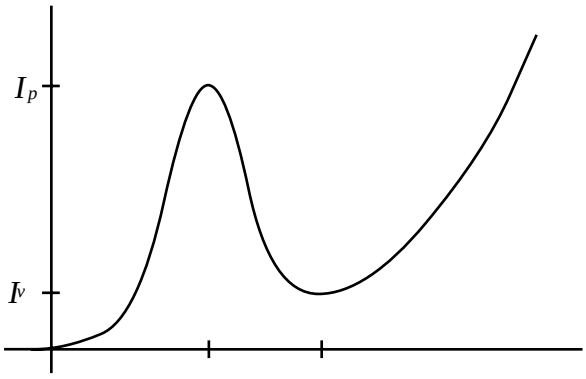

Figure 7.2: I-V curve of a typical RTD. The peak current, I_p, occurs at a voltage V_p and the minimum current, I_v, occurs at the valley voltage, V_v.

differential resistance (NDR) region. A large signal negative conductance can also be defined as the average negative conductance over the entire NDR region:

$$-G_{nls} = \frac{I_p - I_v}{V_p - V_v} \tag{7.1}$$

In designing the quantum well structure, there is usually a direct tradeoff between the two parameters I_p and PVR, and these both impact G_n. For example, increasing the doping level in the emitter increases the peak current density, but because there are more electrons at the higher energies, the thermionic emission over the barriers becomes significant at lower biases and the valley current is not as low, so the PVR is reduced. The same tradeoff occurs if the barriers are made thinner. In a quantum well with thin barriers, the energy band for the quasi-bound state broadens so more electrons can take place in the tunneling process. This leads to an increase in the peak current density, but also reduces the sharpness of the resonance, and so again the PVR is reduced.

There are different design strategies for different applications. When the RTD is going to be used for switching applications such as in a logic circuit, it is important to have the valley current be as small as possible [40], so the PVR is of primary importance here. For sub-millimeter wave oscillators the design emphasis is different. For this application another important parameter is the available current $I_p - I_v$ because this is directly related to the power available from the diode when it is oscillating in the NDR region. In terms of available current, there are diminishing returns for increasing the PVR. With a PVR of 2, half of the peak current is available in the NDR region, and with a PVR

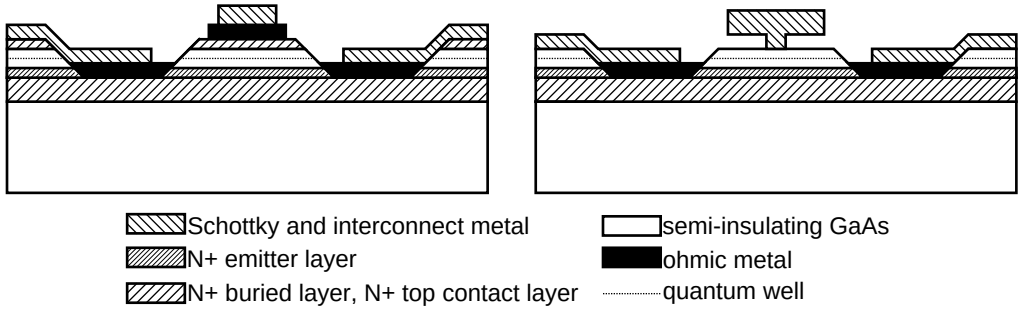

Figure 7.3: Cross-sectional views comparing the structures of (a) the conventional RTD; and (b) the Schottky-collector RTD.

of 5, this increases to 80%. Increasing the PVR from 5 to ∞ will only result in an increase of 20% in available current. It is much more advantageous to increase the peak current at the expense of the PVR. In fact, for the very thin barriers that are desirable for high frequency oscillators (see section 7.2), the peak current increases more rapidly than the PVR degrades, so both G_n and the available current are increased by thinning the barriers.

Figure 7.3 shows cross-sectional diagrams that compare the structures of the conventional RTD and the Schottky-collector RTD. For the conventional device, two ohmic contacts are made in parallel to the heavily doped buried $N+$ layer. On top of this layer is grown the emitter, which is typically doped at about $N_D = 1 \cdot 10^{18}$ cm^{-3} and governs the electron flux across the quantum well. Next is grown a thin spacer layer, followed by the quantum well structure. After this comes the undoped space- charge region and then another heavily doped $N+$ layer to which the top ohmic contact is made. The structure for the SRTD is similar except the top $N+$ layer and ohmic contact are eliminated and instead a Schottky contact is made directly to the space-charge region.

To see how this eliminates the resistance at the collector contact it is instructive to compare the band diagrams of the two devices (figure 7.4). Electron transport through the quantum well region and space-charge layer is identical in the two devices, with equal currents transported for equal electric fields across the well and space-charge layer. After crossing the space-charge layer, electrons are collected by an $N+$ layer in the conventional RTD and must then cross the resistive top ohmic contact. In the SRTD, after crossing the space-charge region, the electrons drop over the potential step $q\phi_b$ at the metal semiconductor interface. The top ohmic contact resistance is eliminated at the expense of an additional voltage drop equal to the height of the potential drop, which is 0.8 V

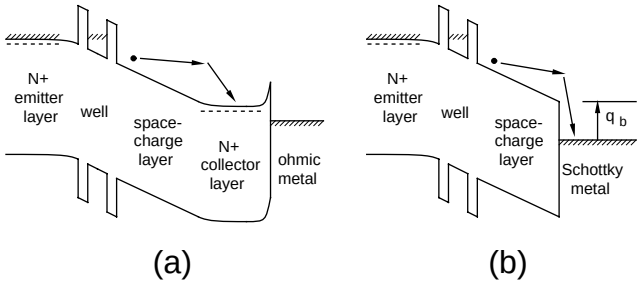

Figure 7.4: Band diagrams for (a) a conventional RTD and (b) a Schottky-collector RTD.

for GaAs.

It is important to understand that the SRTD is not the same as a conventional RTD in series with a Schottky diode. This is best illustrated by again comparing the band diagram of the SRTD (figure 7.4 (b)) to that of the standard Schottky diode (figure 7.5). In a Schottky diode, the height of the potential barrier seen by the electrons in the semiconductor is governed by the applied forward bias, V_f. Because of the Fermi-Dirac distribution of electrons, there is an exponential dependence of current on applied voltage:

$$I_f \cong I_{ss} \exp\left(\frac{qV_f}{kT}\right) \tag{7.2}$$

From this the familiar expression for the small signal junction impedance, r_{junct}, is derived:

$$r_{junct} = \frac{dV_f}{dI_f} = \frac{kT}{qI_f} \tag{7.3}$$

In the Schottky-collector RTD under forward bias, there is no potential barrier to the electrons at the metal semiconductor interface. Because ϕ_b is independent of the current flow under normal operating conditions, $d\phi_b/dI = 0$ and so the Schottky contact has added no differential impedance to the RTD.

The only possible detrimental effect that the Schottky contact could have would be if there were significant quantum mechanical reflection of the electrons at the interface because of the large change in potential and effective mass. If the probability of reflection at the interface is p, then the round trip time across the space-charge region would be increased by a factor on the order of $(1+p)/(1-p)$. If p were large, this could increase the transit time enough to impact the frequency response of the device.

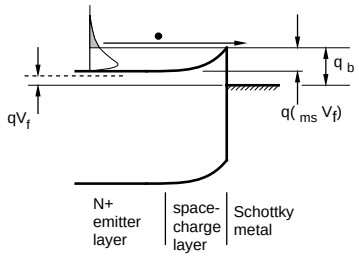

Figure 7.5: Band diagram of a conventional Schottky diode.

To quantify this effect, the reflection probability at the interface was calculated using the following assumptions. Parabolic bands in the semiconductor and monocrystalline metal were assumed so that a standard effective mass approximation could be made for the electrons [41]. A potential step of 1.4 eV was used because the effective mass approximation requires that the energy difference used in the calculation be the energy between the bottoms of the conduction bands and the 0.8 eV Schottky barrier height is between the GaAs conduction band and the Fermi level in the metal, not the conduction band. Assuming the electrons lose a minimal amount of energy while crossing the 350 Å space-charge layer, the reflection probability is only 3%. Even if the incident electron energy is as low as 0.1 eV above the conduction band, the reflection probability remains less than 13%. This estimate is in line with measurements on Schottky mixers with cutoff frequencies as high as 25 THz [14]. The incident electron energy in these devices are generally much lower than in the SRTD and the measured results are not consistent with large contributions from reflections.

7.2 Increasing RTD Bandwidth

The benefits of the Schottky collector towards improving f_{max} of the RTD can be understood by examining the small signal equivalent circuit model of an RTD when biased in the NDR region (figure 7.6). It consists of the extrinsic parasitic series resistance, R_s, the parallel plate capacitance from the undoped space-charge region, C, the effective negative resistance of the diode, $R_n = 1/G_n$, and an inductance associated with the quantum well, L_{qw}, that accounts for the time required for an electron to tunnel through the double barrier structure.

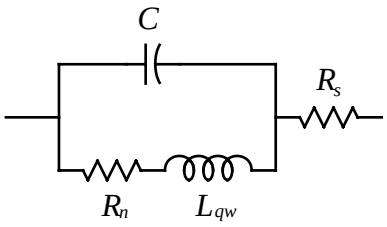

Figure 7.6: Small signal equivalent circuit model of an RTD when biased in the negative differential resistance region.

If L_{qw} is neglected, there is a simple expression for f_{max} of the RTD:

$$f_{max} = \frac{1}{2\pi R_n C}\sqrt{\frac{|R_n| - R_s}{R_s}} \tag{7.4}$$

In order to make f_{max} high, the $1/R_nC$ product should be maximized. This is done by designing the quantum well region to give the device a large peak-to-valley ratio and as high a current density as possible, limited by thermal constraints. Changing the width of the space-charge layer has little impact on this. The capacitance changes linearly with the width, but because the current through the diode is a function of the electric field across the space-charge layer, the voltage required to attain I_p and I_v also changes linearly with the width, and so the R_nC product is independent of this dimension.

Having adjusted the quantum well design accordingly, f_{max} is then limited by the series resistance. The purpose of the Schottky collector is to make this as small as possible. Replacing the collector ohmic with a Schottky contact eliminates that resistance, but the more beneficial result is that the Schottky contact can be scaled to submicron dimensions to further reduce the remaining components of the parasitic resistance. This is almost identical to the scaling effects that were described for the Schottky varactor diode in section 3.1, and the reason for this can be seen by examining figure 7.7, which is a cross-sectional diagram of the SRTD showing the various components of the parasitics.

The capacitance is not voltage dependent as it is for the varactor diode but is instead fixed by the width of the undoped region between the Schottky contact and the emitter layer: $C = \varepsilon WL/d$ where d is the sum of the thicknesses of the space-charge region and double barrier quantum well. When d becomes an appreciable fraction of W, there will be signifcant lateral extent of the electric field under the Schottky contact, and it becomes more appropriate to analyze the diode in terms of an effective contact width, $W_{eff} = W + 2d$.

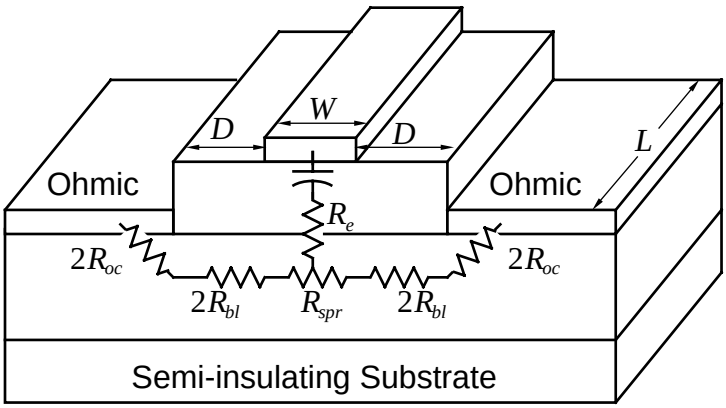

Figure 7.7: Cross-sectional diagram of an SRTD showing the components of the parasitics, almost identical to those of a Schottky varactor.

The vertical resistance through the emitter layer, R_e, has the same functional form as the resistance through the undepleted $N-$ region of the varactor. For the RTD, the doping in this region is chosen to determine the electron flux across the quantum well, but it can made extremely thin to keep R_e small:

$$R_e = \frac{\rho_e T_e}{W_{eff} L} \tag{7.5}$$

The next two components of the series resistance are identical to those discussed in section 3.1:

$$R_{bl} = \frac{1}{2} \cdot \frac{D}{L} \cdot \frac{\rho_{N+}}{T_{N+}} \tag{7.6}$$

$$R_{oc} = \frac{1}{2L} \sqrt{\rho_{cont} \cdot \frac{\rho_{N+}}{T_{N+}}} \tag{7.7}$$

There is also a spreading resistance in the SRTD that accounts for the current spreading out in the buried $N+$ layer, and when the Schottky contact width is reduced to submicron dimensions, the current flow in this region is very two dimensional. In this case, the spreading resistance can be approximated as

$$R_{spr} = \frac{\rho_{N+}}{\pi L} \cdot \ln\left(\frac{T_{N+}}{W_{eff}}\right) \tag{7.8}$$

For submicron Schottky collectors, there will be an additional resistance and inductance along the collector finger, analogous to the gate resistance and inductance in an FET. To minimize these parasitics, a T-gate structure was used

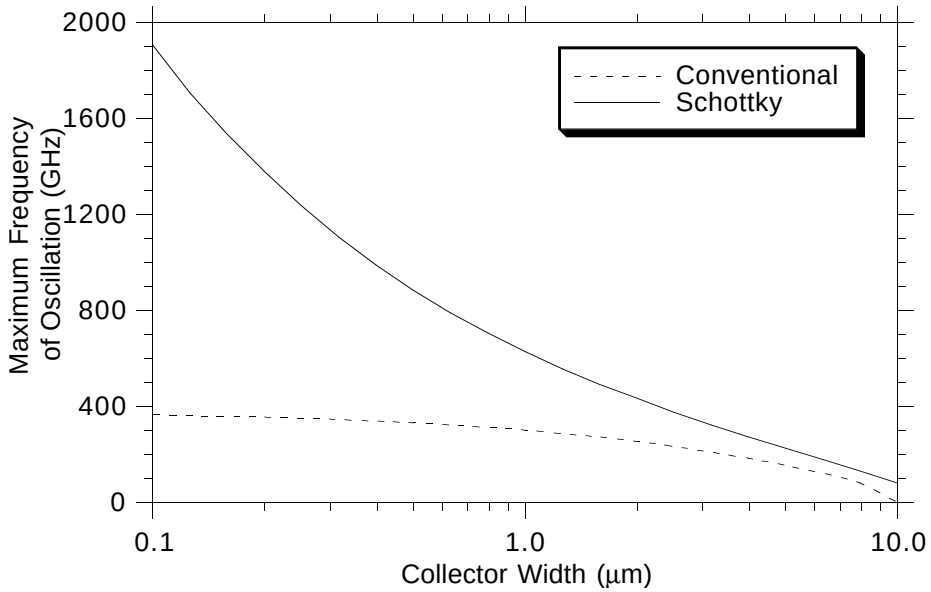

Figure 7.8: Dependence of f_{max} on collector contact width for the conventional RTD (dashed line) and Schottky-collector RTD (solid line), when τ_{qw} is neglected.

to increase the cross-sectional area of the collector finger, and it will be shown later that these terms had negligible impact on the f_{max} of the RTD's.

Because R_{spr}, R_{bl} and R_{oc} are inversely proportional to L, and C and R_n are proportional to $W \cdot L$, decreasing W and increasing L to maintain a constant diode area greatly reduces R_s and results in a substantial increase in f_{max}. This is illustrated in figure 7.8 which uses equation 7.4 to show how f_{max} increases as the Schottky contact width is decreased. For the conventional ohmic-contacted device, there is little improvement in the frequency response as W is reduced below about 1 μm because the resistance becomes dominated by the top ohmic contact, which is an area term. However, for the SRTD, the dominant resistances are all periphery dependent terms, so as the diode's periphery-to-area ratio is increased, f_{max} continues to increase.

When $R_s \ll R_n$, the transit time across the quantum well, τ_{qw}, can no longer be neglected. To leading order, the effect of the transit time delay on the current-voltage relation for the RTD can be described by the differnetial equation:

$$i(t) + \tau_{qw}\frac{\partial i(t)}{\partial t} = -\frac{1}{R_n}v(t) \tag{7.9}$$

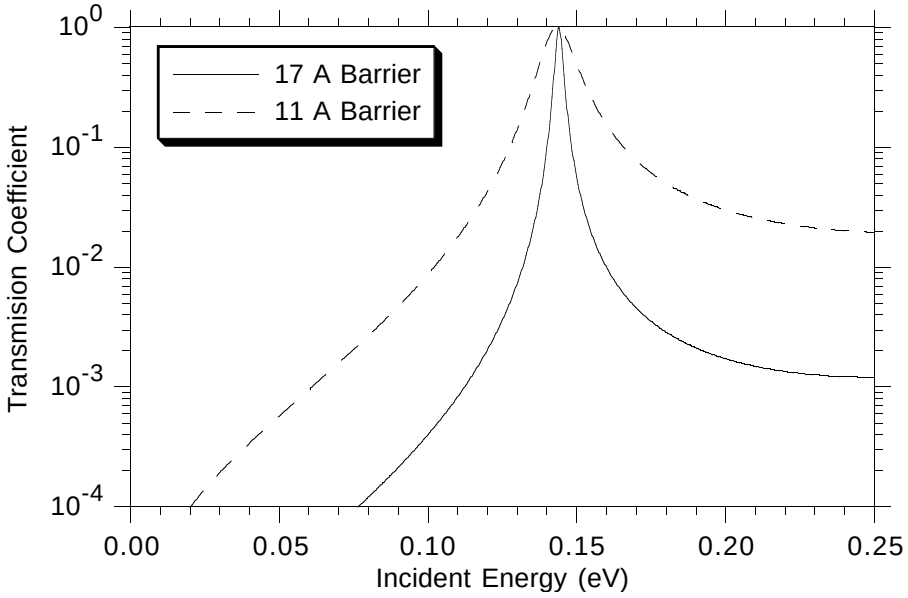

Figure 7.9: Transmission probability of electrons through a double barrier structure compared for two different barrier widths.

This is the equation of a series RL network where $R = -R_n$ and $L = -\tau_{qw}R_n$ and thus the quantum well inductance is defined to be $L_{qw} = -\tau_{qw}R_n$ (negative in the NDR region). When this model was first proposed, a series of experiments was performed on RTDs intentionally designed to have very large values of L_{qw} and the measured results confirmed the validity of the model [42]. Theoretical calculations of this lifetime show that it decreases exponentially as the barrier regions are thinned [43]. The explanation for this is that the tunneling time for an electron to get either in or out of the bound state in the well is given by the uncertainty relation $\tau = \hbar/\Delta E$ where ΔE is the width in energy of the transmission probability. As the barriers are made thinner, the energy band over which tunneling occurs broadens, ΔE increases, and $\tau_{qw} = 2\hbar/\Delta E$ decreases.

Figure 7.9 compares the transmission probability as a function of energy for quantum wells with two different barrier thicknesses. These calculations were performed at the flat band condition for quantum wells having a 45 Å GaAs well bounded by AlAs barriers of either 17 Å or 11 Å. For the thinner barriers, the resonant peak is wider and less sharp. This translates to a shorter well lifetime, higher current density and a lower PVR.

SRTDs with various AlAs barrier thicknesses were fabricated. Table 7.2 sum-

AlAs (Å)	J_p (mA/μm^2)	PVR	G_n (mS/μm^2)	τ_{qw} (fs)
11	2.0	0	0	110
14	1.4	2.0	4.5	220
17	1.0	2.2	3.2	440

Table 7.1: Measured RTD paramters for quantum wells with various barrier widths.

marizes their important parameters. The RTDs with only 11 Å barriers showed no NDR region. The RTDs with 5 monolayer barriers, 14 Å, were superior to those with 17 Å barriers not only in terms of quantum well lifetime but also for negative conductance because the peak current density increased more than the PVR decreased. The calculated values of τ_{qw} are taken from a numerical analysis of these quantum wells when the RTD was in forward bias [44].

For Schottky-collector RTDs with extremely small R_s, the effect of τ_{qw} on f_{max} is dramatic, as shown in figure 7.10. For SRTDs with a 0.1 μm collector width and AlAs barriers of 14 Å, there is almost a 2:1 reduction in f_{max}. The f_{max} of the diodes is now limited by the intrinsic transport properties of the device. In other words, it has become an f_τ limited device instead of an f_{max} limited device. When L_{qw} is included, there is no longer a simple expression for f_{max}. Instead, the definition of f_{max} must be used where $f_{max} = \omega_{max}/2\pi$ is defined to be that frequency at which the real part of the diode's conductance becomes zero:

$$\omega_{max}^4 \tau_{qw}^2 C^2 R_n^2 R_s + \omega_{max}^2 \left(C^2 R_n^2 R_s + 2\tau_{qw} C R_n R_s \right) - R_n + R_s = 0 \qquad (7.10)$$

7.3 Processing

The layer structure was grown by molecular beam epitaxy on a semi-insulating GaAs substrate and consisted of a 1 μm, $5 \cdot 10^{18}$ cm^{-3} $N+$ buried contact layer, a 500 Å, $1 \cdot 10^{18}$ cm^{-3} emitter, a nominally undoped spacer layer, the double barrier structure consisting of 14 Å AlAs barriers (5 monolayers) and a 45 Å GaAs well, and a 350 Å undoped space-charge layer to which the Schottky contacts were made.

Ohmic contacts were formed to the $N+$ layer with a recess etch, a self-aligned AuGe/Ni/Au liftoff and subsequent anneal, as described in section 3.2.2. The

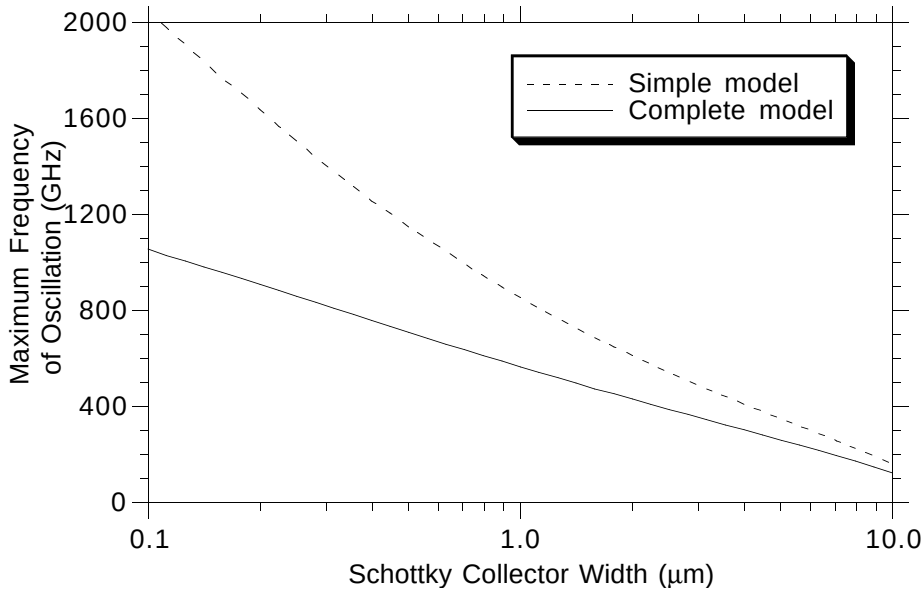

Figure 7.10: Comparison of f_{max} for SRTDs with and without the effect of the quantum well lifetime.

0.1 μm Schottky collectors were defined using an electron beam T-gate process developed for HEMTs at the Jet Propulsion Laboratory. The trilayer resist consisted of 496 K molecular weight PMMA diluted to 2.5% concentration, a PMMA/PMAA 9% copolymer, and a top layer of very dilute 2300 K PMMA. The collector process also incorporated air bridges fabricated by using a low enough dose of electrons in these regions to avoid exposing the base PMMA layer [45], which meant that the active area of the diodes was defined by the actual contact area of the 0.1 μm footprint, not by the size of the etched mesas (figure 7.11). The air bridged part of the E-beam finger was flared out in order to minimize the series resistance and inductance along it.

The devices were mesa isolated using a wet H_3PO_4:H_2O_2 etch and were etched long enough so that the E-beam air bridges were undercut completely. Half of the devices were then passivated with 1200 Å of SiN in an electron-cyclotron resonance system at 160 °C. Ti/Pt/Au interconnect metal was deposited, and contacts to the tops of the mesas were formed with electroplated air bridges using the process described in section 3.2.6. An S.E.M. photograph of a multi-finger SRTD is shown in figure 7.12.

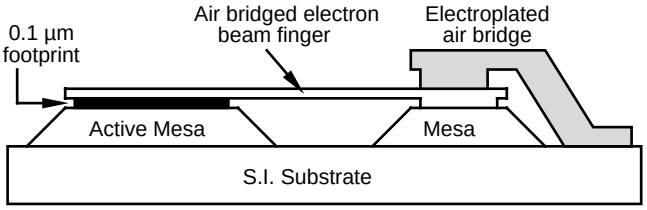

Figure 7.11: Side view of SRTD. The active area of the diode is defined by the 0.1 μm footprint of the E-beam finger. The top of the collector finger is used to air bridge to a second mesa to provide isolation.

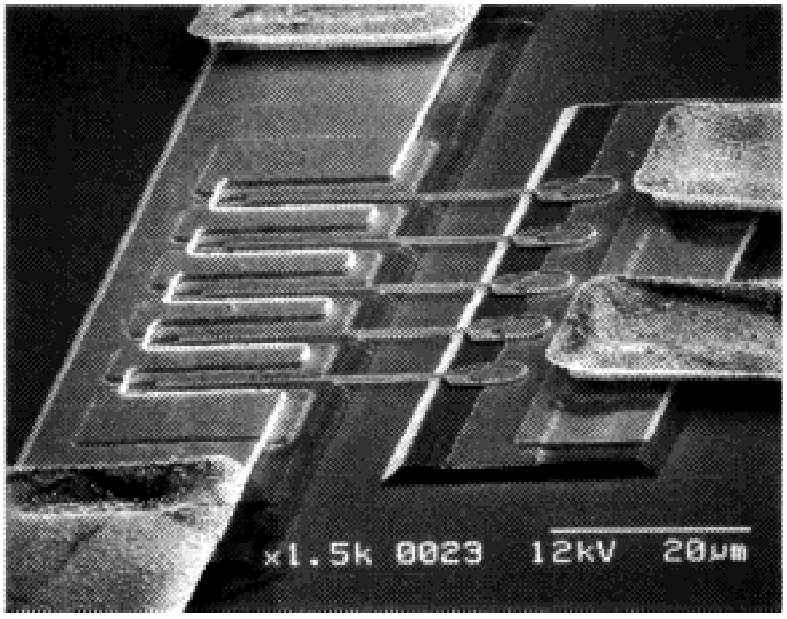

Figure 7.12: S.E.M. of a completed SRTD. Each of the 6 fingers has a 0.1 μm x 20 μm footprint.

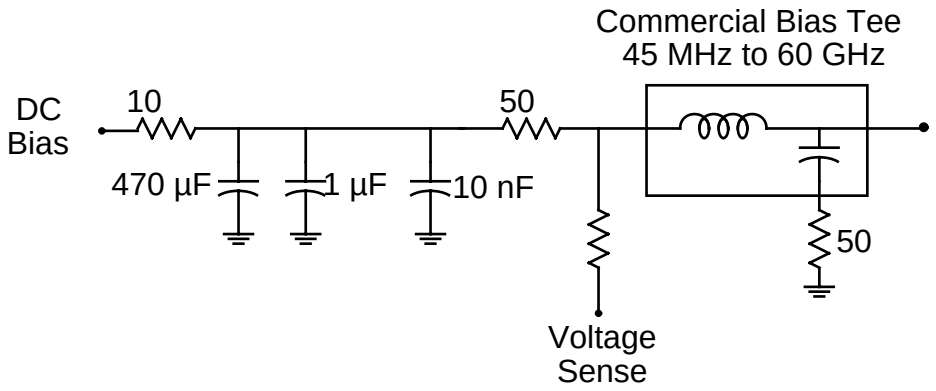

Figure 7.13: Biasing network used to stabilize RTDs.

7.4 Measured Results

The devices were laid out with 50 Ω coplanar waveguide feed structures so that conventional microwave probes could be used for testing. With the use of a bias tee network that presented the RTDs with a 50 Ω source impedance over at least the dc to 60 GHz bandwidth (figure 7.13), diodes with areas $\leq 1.0\ \mu m^2$ were stable even when biased in the NDR region, so accurate dc and microwave measurements could be made. Because the RTDs form a parallel resonant circuit with the admittance of the bias source, as long as the source conductance of 17 to 20 mS was greater than the negative conductance of the RTD, the system should have been stable. However, because the RTDs had an f_{max} much higher than the bandwidth of the bias network, it was found that only diodes with $G_n < 7$ mS could be successfully stabilized because above 60 GHz the RTDs were not presented with a well-controlled bias admittance. The dc I-V curve of a stabilized 1.0 μm^2 SRTD is shown in figure 7.14. The passivated diodes had a $1.4 \cdot 10^5$ A/cm^2 peak current density, assuming a 0.2 μm collector width, a 2.0:1 PVR and -4.5 mS/μm^2 peak negative conductance.

Because of the lateral fringing of the electric field under the Schottky contact, the effective width of it was greater than had been lithographically defined. By comparing the capacitance of large area diodes to that of unpassivated diodes with 0.1 μm E-beam fingers, an effective collector width of 0.20 μm was determined. Passivated diodes had a capacitance of 2.8 fF/μm^2, including the additional parasitics of the SiN layer. The capacitance of the 0.1 μm SRTDs was determined using a microwave network analyzer (NWA). The calibration and deembedding was done using the techniques discussed in section 3.3.2. The

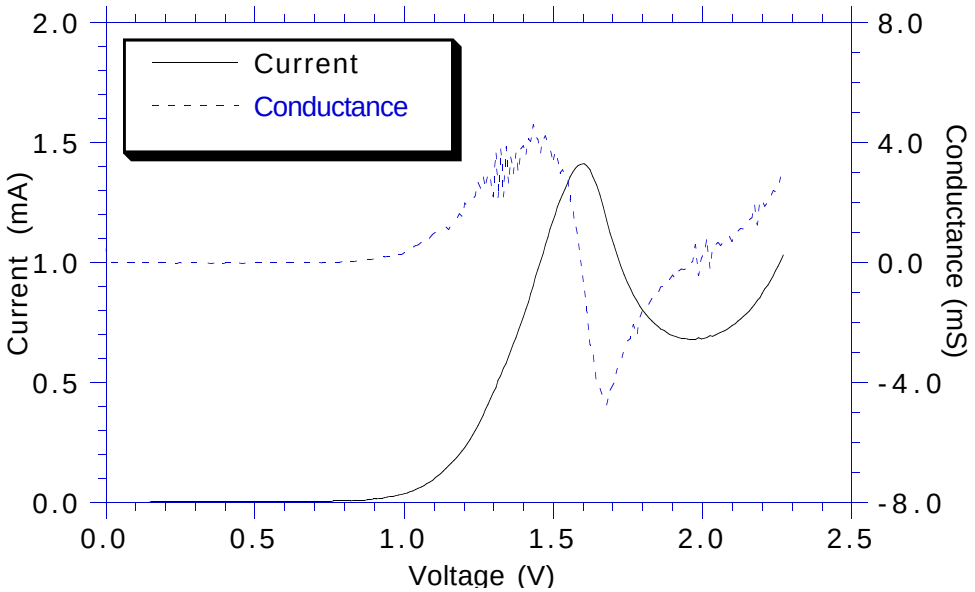

Figure 7.14: Stabilized dc curves of a 1.0 μm^2 SRTD.

diodes were measured at 0 V bias because devices with areas > 1 μm^2 were not stable in the 50 Ω system when forward biased. Figure 7.15 shows the plot of extracted capacitance as a function of the RTD area. A linear fit to the data gives a capacitance of 2.5 fF/μm^2. The capacitance under forward bias will be slightly larger than this because electrons will accumulate in the 100 Å spacer layer that precedes the quantum well. Taking this into account, the measured value was in agreement with the predicted value.

When calculating the parasitics of the diodes, it is important to specify their geometry because the air bridged collector adds some additional resistance and inductance, and its effect on f_{max} depends on what fraction of the total parasitics it contributes. The resistance of the T-shaped finger was measured to be 0.15 Ω/μm and the inductance was measured to be 2.3 pH /μm. In the region of the active device, these elements are distributed and so their effective values are R_{fing} =0.05 Ω/μm and L_{fing} = 1.15 pH/μm. The distance that the narrow finger extended outside the active region was made as small as possible in order to keep the extrinsic parasitics minimal. This distance was limited by the ability to undercut it with the isolation etch, and it was found that 3 μm was a good design value. For use in oscillator arrays, given the G_n and capacitance of these diodes, an area of 3 μm^2 is optimum. Table 7.2 lists all the parasitic element

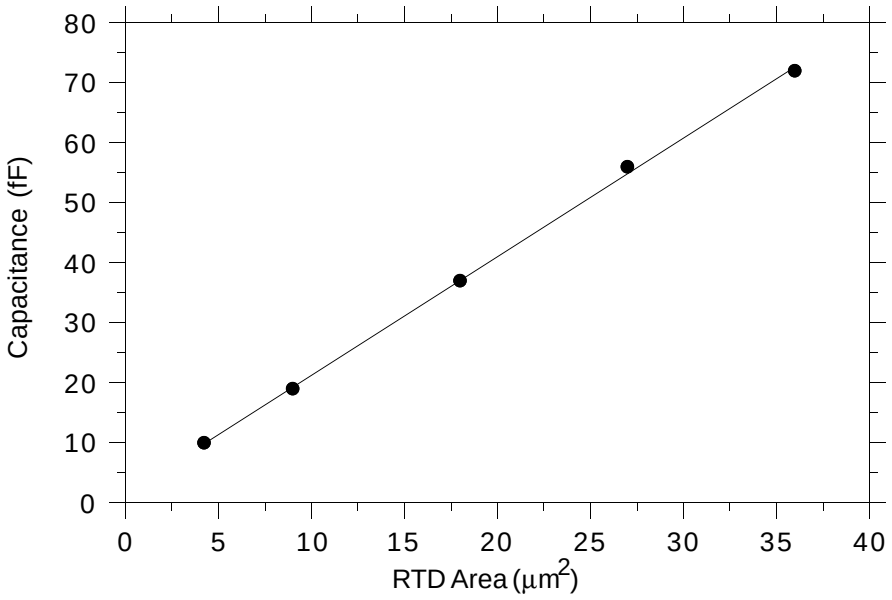

Figure 7.15: Measured SRTD capacitance at 0 V bias as a function of diode area.

values for a diode of this size assuming that is designed with two collector fingers each 7.5 μm long. Using $\tau_{qw} = 220$ fs, an f_{max} of 900 GHz is computed.

Microwave measurements with the RTDs in forward bias were also made on the small devices that could be stabilized. The difficulty in this measurement was that very small signal power levels were needed. As can be seen from figure 7.2, the negative conductance curve is very steep, and so it is important to be making a truly small signal measurement in order to accurately measure G_n. This proved to be problematic on the NWA. Figure 7.16 shows the NWA power output as a function of frequency. The frequencies from 20 to 40 GHz are generated by using a doubler, and because of the gain slope in the system, in order to have sufficient power at 40 GHz the power at 20 GHz is 10 dB higher. This jump in power at 20 GHz was enough to drive the RTDs into large signal operation, and so there was a step in the measured value of G_n between 19.9 and 20.0 GHz.

This problem was circumvented by making the measurements with two different calibrations: the first from 0.1 to 19.9 GHz and the second from 20.1 to 40 GHz. The network analyzer has a power slope compensation capability, so the power output could be leveled for the upper frequency band. The two different calibrations could be stored and then instantaneously recalled, so the

Component	Value
R_{oc}	0.63 Ω
R_{bl}	0.46 Ω
R_{spr}	0.23 Ω
R_e	0.33 Ω
R_{fing}	0.19 Ω
R_{ext}	0.30 Ω
L_{fing}	4.3 pH
L_{ext}	4.6 pH

Table 7.2: Parasitics of a 3 μm^2 SRTD designed with two collector fingers each 7.5 μm long.

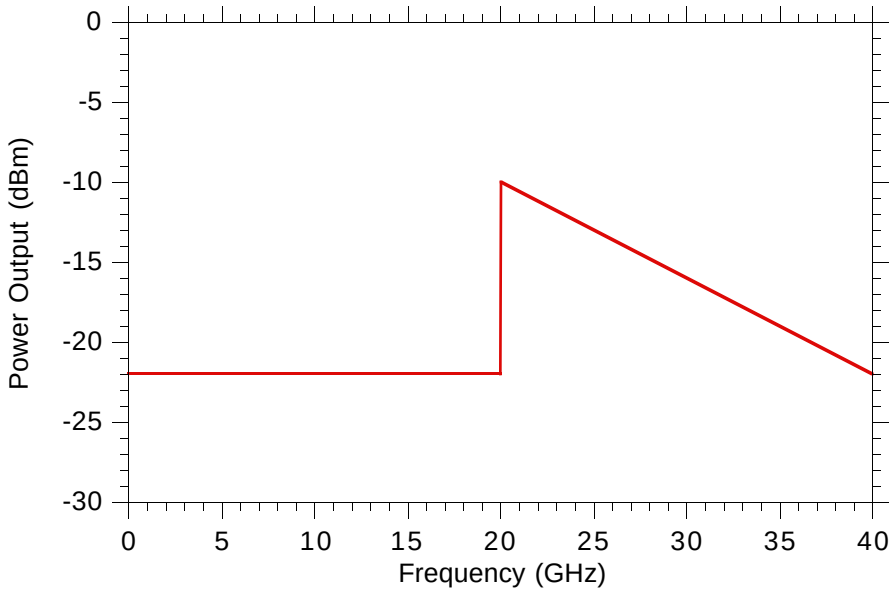

Figure 7.16: Power output of network analyzer. There is a 10 dB jump in power at 20 GHz in order to drive the frequency doubler.

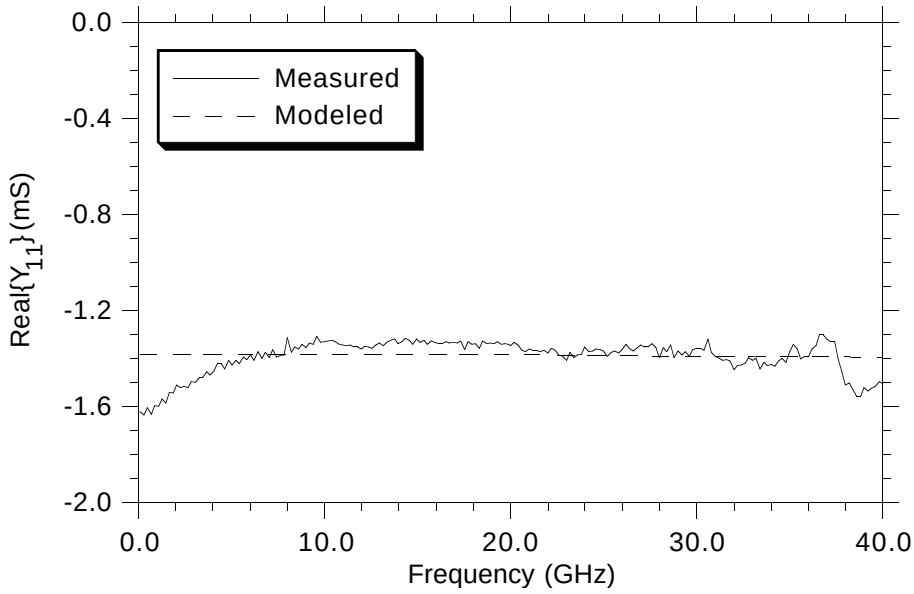

Figure 7.17: Network analyzer data showing the flat negative conductance to 40 GHz. The ripples are attributed to variations in signal power.

RTDs could be biased up and then measured sequentially over the two different frequency ranges. The measured data is shown in figure 7.17.

The negative conductance has some bumps in it due to the imperfect correction for the NWA's output power, but the curve is essentially flat to 40 GHz and G_n is in agreement with the measured dc value. Because the rolloff of the $G(\omega)$ is to second and fourth order in frequency (equation 7.10), measurements to only a small fraction of the device's bandwidth do not permit an extrapolation to f_{max} as is usually done for transistors which have an f_{max} curve that rolls off predictably at 6 dB/octave. Given existing instrument limitations, f_{max} can be experimentally verified only by building oscillators and testing them at sub-mm-wave frequencies. Oscillators up to 500 GHz have been designed with these devices and are presently awaiting fabrication.

Chapter 8

Conclusion

By improving each of the individual components that are integrated to form an NLTL and sampler, the circuit bandwidth was increased by a factor of 3 to 725 GHz. The 1 μm 4 THz Schottky diodes were the first step towards that end and improved circuit performance to 500 GHz. By using the air bridged transmission line to reduce loss, eliminate pad parasitics and increase the Bragg frequency the circuit bandwidth was pushed up to 725 GHz. These circuits are a solid technology that can incorporated into a new generation of measurement instruments. They no longer require a gradient dc biasing scheme and they do not have to be driven to the limits of diode breakdown to produce subpicosecond edges, so they are well-suited for system level applications.

The network analyzers require two sampling circuits on each channel in order to separate incident and reflected waves [9], so some layout modifications would be required, but even with the increased complexity, the sampler bandwidth should remain above 600 GHz. The 3.7 V step functions generated by the NLTLs are sufficiently large to strobe both of the samplers. By using this technology, the bandwidth limits as the system level work is pushed towards the sub-millimeter-wave range will not come from the sampling circuits.

8.1 Air Bridged Transmission Lines

The air bridged transmission lines have already been incorporated into other designs. The first application where these were required was a multiplexer circuit for 100 Gb/sec data transmission that was based primarily on an earlier generation of NLTLs. A simplified schematic diagram of the four diode sampling bridge is shown in figure 8.1. The design constraints on such a bridge are more severe

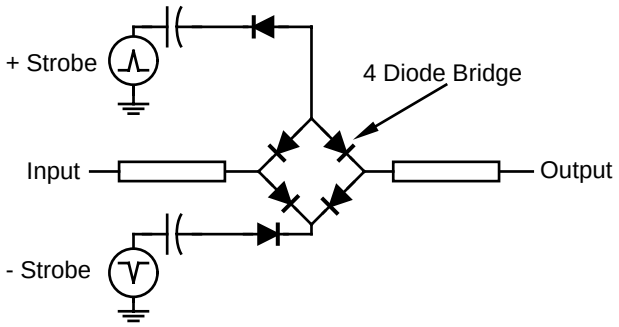

Figure 8.1: Schematic diagram of a four diode bridge designed for 100 Gb/sec switching.

than on the simpler two diode bridge. First of all, the diodes need to be smaller because there are now twice as many that have to be charged by the strobe pulses. Secondly, in order to have good isolation between the input and output when the bridge is turned off, the diodes need to be small so that the capacitive coupling through them is small. To meet these requirements the diodes in the bridge needed to be 1.5 μm x 1.5 μm, and the only way to successfully make these is to make small dots and contact them from the top with a suspended air bridge.

The other circuit that has been designed with the air coplanar waveguide is a traveling wave amplifier (TWA) based on 0.1 μm AlInAs/InGaAs/InP HEMTS [1] that has 200 GHz bandwidth. A schematic diagram of a TWA is shown in figure 8.2. The basic design principle of a TWA is very similar to the NLTL in that the gate and drain capacitances of the transistors are incorporated into synthetic transmission lines designed to have a loaded impedance of 50 Ω. These lines also have a Bragg frequency, and without using the air lines to increase the wave velocity, it would have been physically impossible to reach 200 GHz because the transistors would have been overlapping.

These two examples illustrate the versatility of the air bridged transmission lines. While they were developed specifically for the nonlinear transmission line application, they address issues that are of concern in most high frequency circuits. The air lines are an enabling technology that will find many applications as integrated circuits push into the millimeter and sub-millimeter wave ranges.

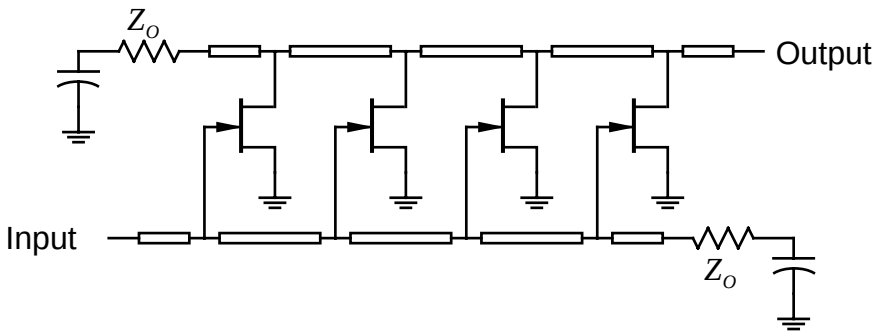

Figure 8.2: Schematic diagram of a traveling wave amplifier. The design principle is similar to an NLTL in that synthetic transmission lines are formed using the gate and drain capacitances of the transistors.

8.2 Future Development of Schottky-Collector RTDs

The 900 GHz RTDs fabricated as part of this thesis work are the first step towards the long range goal of building solid state oscillators that produce milliwatts of power at 1 THz. In order to accomplish this goal, there are a number of important advances that still need to be made. The first is to apply the Schottky collector concept to RTDs made with AlAs/InGaAs quantum wells lattice matched to InP. RTDs in this material system have higher peak current densities and higher peak-to-valley ratios [46] and hence more negative conductance. The quantum well lifetime is also about a factor of 2 lower than for comparable structures in AlAs/GaAs, so 0.1 μm SRTDs fabricated with AlAs/InGaAs should have $f_{max} > 2$ THz. The power out of an RTD oscillator is proportional to $1 - (f/f_{max})^2$, so reasonable amounts of power are still available at $f_{max}/2$, which means that a 2 THz device should be adequate for a 1 THz oscillator.

The second component that needs to be developed is a stabilizing element that can be integrated with the SRTDs on wafer. For measuring discrete devices, an external 50 Ω bias network was a simple solution but is unacceptable for use with sub-mm- wave oscillators. The dc stability of the RTDs also puts a size constraint on them. In order to be stable in a 50 Ω system, $|G_n| < 20$ mS, which limits the area of the diode and, hence, the power. In order to get appreciable amounts of power, an array of antenna coupled RTDs will be necessary.

Building dense oscillator arrays at frequencies above 500 GHz may require the use of the air bridged transmission line technology developed for the NLTLs.

In many simple oscillators, the resonant element in the network is a quarter wave open circuited transmission line. Because a quarter wave length at 1 THz on GaAs is only 28 μm, doubling the wave velocity using the air lines is probably a requirement for this type of oscillator topology. Another benefit of the air line technology is the ability to contact very small diodes without adding any parasitics. In order to have a very small, very clean layout at 1 THz, it may be necessary to adapt this to the RTDs. This is another potential applications for the air lines illustrate the fact that the technology is not limited to the NLTLs for which it was developed but that it addresses the problems encountered in a variety of sub-mm-wave integrated circuits.

Appendix A

Design Files for Subpicosecond Shock Lines

Following are the programs that were used to design the shock lines described in detail in chapter 4. Section A.1 contains the c program that was used to generate the SPICE file and the layout file that was readable by an Academy macro. Section A.2 contains the listing of the SPICE file. Section A.3 contains the data for the layout file that is readable by an Academy macro program.

A.1 C Program for File Generation

```
#include <stdio.h>
#include <ctype.h>
#include <string.h>
#include <math.h>

#define PI 3.141592654  /* pi   */
#define V 113.3893419   /* Velocity in GaAs um/ps */

/* This program generates a Spice file and a layout file */
/* It creates both ground plane diode cells  */
/* and center conductor diode cells */
/* Modified 8/26/92 by Scott Allen */

main() {
int n,i,w,l,lastw;
```

```
float fb0,fbx,zls,zl,tcomp,rs,cjo,phi,m,iss,in,floss;
float vmax,vmin,cmax,cmin,qmax,qmin,cls,t0,tx,a0,cr;
float tline,k,lline,x,y,z,lng,area,sq,fb,lngb,atten,lam;
char a[128],b[128],fsim[64],flay[64],t[1];
FILE *fs,*fl;

/*************************************************************************
*/
/* Introduction */
/*************************************************************************
*/
printf("This program will generate NLTLs for you.\n");
printf("You can either do a homogeneous line, or an\n");
printf("inhomogeneous line.  The difference is that\n");
printf("you enter either starting and ending bragg\n");
printf("frequencies (which determine the number of\n");
printf("sections and the tapering rule), or define\n");
printf("the number of sections and the tapering rule\n");
printf("(tapering rule = 1 for homogeneous line).\n");
printf("This programme uses a 6th order polynomial cap.\n\n");
printf("Please enter starting Bragg frequency (GHz)  : ");
scanf("%s",a);
fb0=atof(a);
printf("Please enter ending Bragg frequency (GHz)    : ");
scanf("%s",a);
fbx=atof(a);
printf("Please enter line compression (ps)           : ");
scanf("%s",a);
tcomp=atof(a);
printf("Please enter large signal impedance (ohms)   : ");
scanf("%s",a);
zls=atof(a);
printf("Please enter line impedance (ohms)           : ");
scanf("%s",a);
zl=atof(a);

/*************************************************************************
*/
```

```
/* Get the diode data */
/*********************************************************************
*/

/* Diode Parameters (1X1 diode)  (ff, ohms) */
printf("\nDefault Diode Parameters: (1 um X 1 um)\n");
rs=29.26;
        cjo=1.84;
        phi=0.80;
        m=0.50;
        iss=1;
        in=1.2;
printf("Series resistance:      RS = %f ohm X um^2\n",rs);
printf("Zero-bias capacitance: CJO = %f fF / um^2\n",cjo);
printf("Barrier potential:     PHI = %f V\n",phi);
printf("Grading constant:        M = %f\n",m);
printf("Saturation current:    ISS = %f pA / um^2\n",iss);
printf("Ideality factor:         N = %f\n",in);

printf("\nDo you want to change them?");
scanf("%s",a);
if (a[0] == 'y') {
printf("Please enter RS = ");
scanf("%s",a);
rs=atof(a);
printf("Please enter CJO = ");
scanf("%s",a);
cjo=atof(a);
printf("Please enter PHI = ");
scanf("%s",a);
phi=atof(a);
printf("Please enter M = ");
scanf("%s",a);
m=atof(a);
printf("Please enter ISS = ");
scanf("%s",a);
iss=atof(a);
printf("Please enter N = ");
```

```
scanf("%s",a);
in=atof(a);
}

printf("\nPlease enter maximum then minimum voltage:\n");
printf("(reverse bias max then min e.g. 6 then 0.\n");
scanf("%s",a);
vmax=atof(a);
scanf("%s",a);
vmin=atof(a);

cmin=cjo/exp(m*log(1+vmax/phi));
cmax=cjo/exp(m*log(1+vmin/phi));

qmin=phi*cjo*exp((1-m)*log(1+vmin/phi))/(1-m);
qmax=phi*cjo*exp((1-m)*log(1+vmax/phi))/(1-m);

cls=(qmax-qmin)/(vmax-vmin);
t0=(1000*zls)/(PI*fb0*zl);
tx=(1000*zls)/(PI*fbx*zl);
a0=(zl/zls)*(zl/zls)-1;
cr=sqrt(a0)*(sqrt(1/a0+cmax/cls)-sqrt(1/a0+cmin/cls));
tline=tcomp/cr;

if(fbx != fb0) {
k=(tline-t0)/(tline-tx);
n=(0.5+log(tx/t0)/log(k));
lline=V*((t0-k*tx)/(1-k));
}
else {
k=1;
n=0.5+tline/t0;
lline=V*n*t0;
}

printf("\nThe line has the following parameters:\n\n");
printf("Large Signal Capacitance   : %f ff/um^2\n",cls);
printf("Compression ratio          : %f\n",cr);
```

```
printf("Tapering factor            : %f\n",k);
printf("Number of sections         : %d\n",n);
printf("Total line length          : %f um\n\n",lline);

printf("Please enter circuit file name: ");
scanf("%s",fsim);
strcpy(flay,fsim);
strcat(fsim,"_sim.ckt");
strcat(flay,"_lay.ckt");
printf("\nThere will be two files: *_sim.ckt and *_lay.ckt\n");
fs=fopen(fsim,"w");
fl=fopen(flay,"w");
printf("\nDo you want to include tranmission line loss?");
scanf("%s",a);
floss=10;
if (a[0] == 'y') {
printf("\nEnter skin loss frequency (GHz) : ");
scanf("%s",b);
floss=atof(b);
}

/*  Write the files */

fprintf(fs,"! SPICE file for NLTL with %.2f GHz initial Bragg frequency,\n",fb0);
fprintf(fs,"! %.2f GHz final Bragg frequency and %f tapering rule,\n",fbx,k);
fprintf(fs,"! and %.2f ps total compression.\n",tcomp);
fprintf(fs,"DIM\n");
fprintf(fs,"   LNG UM\n");
fprintf(fs,"CKT\n");

fprintf(fl,"! Academy file for NLTL with %.2f GHz initial Bragg
frequency,\n",fb0);
fprintf(fl,"! %.2f GHz final Bragg frequency and %f tapering rule,\n",fbx,k);
fprintf(fl,"! and %.2f ps total compression.\n",tcomp);
fprintf(fl,"DIM\n");
fprintf(fl,"   LNG UM\n");
fprintf(fl,"CKT\n");
/* initialize lastw to max width */
```

```
lastw=14;

x=((0.5*exp(zl/11.33893419)-1)/(0.5*exp(zl/11.33893419)+1));
y=x*x*x*x;
z=(1-sqrt(1-y))/(2*sqrt(1-y));
for(i=1;i<n+2;i++) {
lng=V*t0*exp((i-1)*log(k));
lngb=lng*(1+k)/2;
area=1e6*((1-(zls/zl)*(zls/zl))/(PI*fb0*zls))*exp((i-1)*log(k))/cls;
w=1+200/(1+2*z);

/* Determine aspect ratio, type and design rule */

while (lng < w*(1.5*(1+z*2))) {
w--;
}
if (w < 3) {
w=3;
}
if (area > 24.5) {
l=2;
lam=3;
if (w == lastw ) {
      strcpy(t,"A");
}
else {
strcpy(t,"D");
}
}
else if (area > 7.5) {
l=1;
lam=3;
if (w == lastw ) {
      strcpy(t,"A");
}
else {
strcpy(t,"D");
}
```

```
}
else if (area > 5.75) {
w=2;
l=1;
lam=2;
strcpy(t,"C");
}
else  {
w=1;
l=1;
lam=2;
strcpy(t,"C");
}
sq += lng/w;
lastw =w;
fb=fb0*exp((1-i)*log(k));
if (a[0] == 'n') {
atten=0;
}
else {
atten=8.685889638*sqrt(floss*PI*1e9*2.44e-8*4*PI*1e-
7)/(2*zls*w);
}

fprintf(fl,"   NLTL%s_U%d  %d  %d  Z=%.2f W=%d ADI=%.2f
LLI=%.2f LAM=%.1f LAMS=%d LAMO=2 !
fb=%.2f\n",t,i,i,i+1,zl,w,area,lng,lam,l,fb);
if(i==1) {
fprintf(fs,"   TLINP_T0 201 1 Z=%.2f L=%.2f K=7 A=%e
F=%f\n",zl,lng/2,atten,floss);
}
fprintf(fs,"   S1PA_D%d  %d  0  [MODEL=MIKE%d AREA=%.2f] !
fb=%.2f\n",i,i,l,area,fb);
if(i==n+1) {
fprintf(fs,"   TLINP_T%d  %d  %d  Z=%.2f L=%.2f K=7 A=%e
F=%f\n",i,i,i+1,zl,lng/2,atten,floss);
}
else {
```

```
fprintf(fs,"   TLINP_T%d  %d  %d  Z=%.2f L=%.2f K=7 A=%e
F=%f\n",i,i,i+1,zl,lngb,atten,floss);
}
}
fprintf(fl,"   DEF2P 1 %d NLTL%d\n",i,i-1);
fprintf(fl,"! Total number of squares is %.2f\n",sq);

fprintf(fs,"   DEF2P  201  %d  NLTL\n",i);
fprintf(fs,"! Total number of squares is %.2f\n",sq);
fprintf(fs,"MODEL\n");
fprintf(fs,"   MIKE D RS=%f CJO=%fE-15 VJ=%f &\n",rs,cjo,phi);
fprintf(fs,"          M=%f IS=%fE-12 N=%f\n",m,iss,in);
fprintf(fs,"SOURCE\n");
fprintf(fs,"   NLTL RES_RIN  201 202 R=50\n");
fprintf(fs,"   NLTL IVS_VIN  202  0  TRAN=SIN(-6 14 9E9 0 0 90)\n");
fprintf(fs,"   NLTL RES_RL   %d  0  R=50\n",i);
fprintf(fs,"CONTROL\n");
fprintf(fs,"   NLTL TRAN 10E-12 2E-9\n");
fprintf(fs,"SPICEOUT\n");
fprintf(fs,"   NLTL TRAN V(ALL)\n");

fclose(fs);
fclose(fl);
printf("Do you want to do it again? ");
scanf("%s",t);
if (t[0]=='n' || t[0]=='N')
exit(0);
main();
}
```

A.2 SPICE File

```
! SPICE file for NLTL with 125.00 GHz initial Bragg frequency,
! 800.00 GHz final Bragg frequency and 0.984789 tapering rule,
! and 60.00 ps total compression.
DIM
   LNG UM
CKT
```

```
TLINP_T0 201 1 Z=75.00 L=77.00 K=7 A=0.000000e+00 F=10.000000
S1PA_D1  1  0  [MODEL=MIKE2 AREA=48.47] ! fb=125.00
TLINP_T1  1  2  Z=75.00 L=152.83 K=7 A=0.000000e+00 F=10.000000
S1PA_D2  2  0  [MODEL=MIKE2 AREA=47.73] ! fb=126.93
TLINP_T2  2  3  Z=75.00 L=150.50 K=7 A=0.000000e+00 F=10.000000
S1PA_D3  3  0  [MODEL=MIKE2 AREA=47.01] ! fb=128.89
TLINP_T3  3  4  Z=75.00 L=148.21 K=7 A=0.000000e+00 F=10.000000
S1PA_D4  4  0  [MODEL=MIKE2 AREA=46.29] ! fb=130.88
TLINP_T4  4  5  Z=75.00 L=145.96 K=7 A=0.000000e+00 F=10.000000
S1PA_D5  5  0  [MODEL=MIKE2 AREA=45.59] ! fb=132.90
TLINP_T5  5  6  Z=75.00 L=143.74 K=7 A=0.000000e+00 F=10.000000
S1PA_D6  6  0  [MODEL=MIKE2 AREA=44.89] ! fb=134.96
TLINP_T6  6  7  Z=75.00 L=141.55 K=7 A=0.000000e+00 F=10.000000
S1PA_D7  7  0  [MODEL=MIKE2 AREA=44.21] ! fb=137.04
TLINP_T7  7  8  Z=75.00 L=139.40 K=7 A=0.000000e+00 F=10.000000
S1PA_D8  8  0  [MODEL=MIKE2 AREA=43.54] ! fb=139.16
TLINP_T8  8  9  Z=75.00 L=137.28 K=7 A=0.000000e+00 F=10.000000
S1PA_D9  9  0  [MODEL=MIKE2 AREA=42.88] ! fb=141.31
TLINP_T9  9  10  Z=75.00 L=135.19 K=7 A=0.000000e+00 F=10.000000
S1PA_D10  10  0  [MODEL=MIKE2 AREA=42.22] ! fb=143.49
TLINP_T10  10  11  Z=75.00 L=133.13 K=7 A=0.000000e+00 F=10.000000
S1PA_D11  11  0  [MODEL=MIKE2 AREA=41.58] ! fb=145.71
TLINP_T11  11  12  Z=75.00 L=131.11 K=7 A=0.000000e+00 F=10.000000
S1PA_D12  12  0  [MODEL=MIKE2 AREA=40.95] ! fb=147.96
TLINP_T12  12  13  Z=75.00 L=129.11 K=7 A=0.000000e+00 F=10.000000
S1PA_D13  13  0  [MODEL=MIKE2 AREA=40.33] ! fb=150.24
TLINP_T13  13  14  Z=75.00 L=127.15 K=7 A=0.000000e+00 F=10.000000
S1PA_D14  14  0  [MODEL=MIKE2 AREA=39.71] ! fb=152.56
TLINP_T14  14  15  Z=75.00 L=125.21 K=7 A=0.000000e+00 F=10.000000
S1PA_D15  15  0  [MODEL=MIKE2 AREA=39.11] ! fb=154.92
TLINP_T15  15  16  Z=75.00 L=123.31 K=7 A=0.000000e+00 F=10.000000
S1PA_D16  16  0  [MODEL=MIKE2 AREA=38.51] ! fb=157.31
TLINP_T16  16  17  Z=75.00 L=121.43 K=7 A=0.000000e+00 F=10.000000
S1PA_D17  17  0  [MODEL=MIKE2 AREA=37.93] ! fb=159.74
TLINP_T17  17  18  Z=75.00 L=119.59 K=7 A=0.000000e+00 F=10.000000
S1PA_D18  18  0  [MODEL=MIKE2 AREA=37.35] ! fb=162.21
TLINP_T18  18  19  Z=75.00 L=117.77 K=7 A=0.000000e+00 F=10.000000
S1PA_D19  19  0  [MODEL=MIKE2 AREA=36.78] ! fb=164.72
```

```
TLINP_T19  19  20  Z=75.00 L=115.98 K=7 A=0.000000e+00 F=10.000000
S1PA_D20  20  0  [MODEL=MIKE2 AREA=36.22] ! fb=167.26
TLINP_T20  20  21  Z=75.00 L=114.21 K=7 A=0.000000e+00 F=10.000000
S1PA_D21  21  0  [MODEL=MIKE2 AREA=35.67] ! fb=169.84
TLINP_T21  21  22  Z=75.00 L=112.47 K=7 A=0.000000e+00 F=10.000000
S1PA_D22  22  0  [MODEL=MIKE2 AREA=35.13] ! fb=172.47
TLINP_T22  22  23  Z=75.00 L=110.76 K=7 A=0.000000e+00 F=10.000000
S1PA_D23  23  0  [MODEL=MIKE2 AREA=34.59] ! fb=175.13
TLINP_T23  23  24  Z=75.00 L=109.08 K=7 A=0.000000e+00 F=10.000000
S1PA_D24  24  0  [MODEL=MIKE2 AREA=34.07] ! fb=177.84
TLINP_T24  24  25  Z=75.00 L=107.42 K=7 A=0.000000e+00 F=10.000000
S1PA_D25  25  0  [MODEL=MIKE2 AREA=33.55] ! fb=180.58
TLINP_T25  25  26  Z=75.00 L=105.79 K=7 A=0.000000e+00 F=10.000000
S1PA_D26  26  0  [MODEL=MIKE2 AREA=33.04] ! fb=183.37
TLINP_T26  26  27  Z=75.00 L=104.18 K=7 A=0.000000e+00 F=10.000000
S1PA_D27  27  0  [MODEL=MIKE2 AREA=32.54] ! fb=186.21
TLINP_T27  27  28  Z=75.00 L=102.59 K=7 A=0.000000e+00 F=10.000000
S1PA_D28  28  0  [MODEL=MIKE2 AREA=32.04] ! fb=189.08
TLINP_T28  28  29  Z=75.00 L=101.03 K=7 A=0.000000e+00 F=10.000000
S1PA_D29  29  0  [MODEL=MIKE2 AREA=31.55] ! fb=192.00
TLINP_T29  29  30  Z=75.00 L=99.49 K=7 A=0.000000e+00 F=10.000000
S1PA_D30  30  0  [MODEL=MIKE2 AREA=31.07] ! fb=194.97
TLINP_T30  30  31  Z=75.00 L=97.98 K=7 A=0.000000e+00 F=10.000000
S1PA_D31  31  0  [MODEL=MIKE2 AREA=30.60] ! fb=197.98
TLINP_T31  31  32  Z=75.00 L=96.49 K=7 A=0.000000e+00 F=10.000000
S1PA_D32  32  0  [MODEL=MIKE2 AREA=30.14] ! fb=201.04
TLINP_T32  32  33  Z=75.00 L=95.02 K=7 A=0.000000e+00 F=10.000000
S1PA_D33  33  0  [MODEL=MIKE2 AREA=29.68] ! fb=204.14
TLINP_T33  33  34  Z=75.00 L=93.58 K=7 A=0.000000e+00 F=10.000000
S1PA_D34  34  0  [MODEL=MIKE2 AREA=29.23] ! fb=207.30
TLINP_T34  34  35  Z=75.00 L=92.15 K=7 A=0.000000e+00 F=10.000000
S1PA_D35  35  0  [MODEL=MIKE2 AREA=28.78] ! fb=210.50
TLINP_T35  35  36  Z=75.00 L=90.75 K=7 A=0.000000e+00 F=10.000000
S1PA_D36  36  0  [MODEL=MIKE2 AREA=28.34] ! fb=213.75
TLINP_T36  36  37  Z=75.00 L=89.37 K=7 A=0.000000e+00 F=10.000000
S1PA_D37  37  0  [MODEL=MIKE2 AREA=27.91] ! fb=217.05
TLINP_T37  37  38  Z=75.00 L=88.01 K=7 A=0.000000e+00 F=10.000000
S1PA_D38  38  0  [MODEL=MIKE2 AREA=27.49] ! fb=220.40
```

```
TLINP_T38  38  39  Z=75.00 L=86.67 K=7 A=0.000000e+00 F=10.000000
S1PA_D39  39  0  [MODEL=MIKE2 AREA=27.07] ! fb=223.81
TLINP_T39  39  40  Z=75.00 L=85.36 K=7 A=0.000000e+00 F=10.000000
S1PA_D40  40  0  [MODEL=MIKE2 AREA=26.66] ! fb=227.27
TLINP_T40  40  41  Z=75.00 L=84.06 K=7 A=0.000000e+00 F=10.000000
S1PA_D41  41  0  [MODEL=MIKE2 AREA=26.25] ! fb=230.78
TLINP_T41  41  42  Z=75.00 L=82.78 K=7 A=0.000000e+00 F=10.000000
S1PA_D42  42  0  [MODEL=MIKE2 AREA=25.85] ! fb=234.34
TLINP_T42  42  43  Z=75.00 L=81.52 K=7 A=0.000000e+00 F=10.000000
S1PA_D43  43  0  [MODEL=MIKE2 AREA=25.46] ! fb=237.96
TLINP_T43  43  44  Z=75.00 L=80.28 K=7 A=0.000000e+00 F=10.000000
S1PA_D44  44  0  [MODEL=MIKE2 AREA=25.07] ! fb=241.64
TLINP_T44  44  45  Z=75.00 L=79.06 K=7 A=0.000000e+00 F=10.000000
S1PA_D45  45  0  [MODEL=MIKE2 AREA=24.69] ! fb=245.37
TLINP_T45  45  46  Z=75.00 L=77.86 K=7 A=0.000000e+00 F=10.000000
S1PA_D46  46  0  [MODEL=MIKE1 AREA=24.32] ! fb=249.16
TLINP_T46  46  47  Z=75.00 L=76.67 K=7 A=0.000000e+00 F=10.000000
S1PA_D47  47  0  [MODEL=MIKE1 AREA=23.95] ! fb=253.01
TLINP_T47  47  48  Z=75.00 L=75.50 K=7 A=0.000000e+00 F=10.000000
S1PA_D48  48  0  [MODEL=MIKE1 AREA=23.58] ! fb=256.91
TLINP_T48  48  49  Z=75.00 L=74.36 K=7 A=0.000000e+00 F=10.000000
S1PA_D49  49  0  [MODEL=MIKE1 AREA=23.22] ! fb=260.88
TLINP_T49  49  50  Z=75.00 L=73.23 K=7 A=0.000000e+00 F=10.000000
S1PA_D50  50  0  [MODEL=MIKE1 AREA=22.87] ! fb=264.91
TLINP_T50  50  51  Z=75.00 L=72.11 K=7 A=0.000000e+00 F=10.000000
S1PA_D51  51  0  [MODEL=MIKE1 AREA=22.52] ! fb=269.00
TLINP_T51  51  52  Z=75.00 L=71.01 K=7 A=0.000000e+00 F=10.000000
S1PA_D52  52  0  [MODEL=MIKE1 AREA=22.18] ! fb=273.16
TLINP_T52  52  53  Z=75.00 L=69.93 K=7 A=0.000000e+00 F=10.000000
S1PA_D53  53  0  [MODEL=MIKE1 AREA=21.84] ! fb=277.38
TLINP_T53  53  54  Z=75.00 L=68.87 K=7 A=0.000000e+00 F=10.000000
S1PA_D54  54  0  [MODEL=MIKE1 AREA=21.51] ! fb=281.66
TLINP_T54  54  55  Z=75.00 L=67.82 K=7 A=0.000000e+00 F=10.000000
S1PA_D55  55  0  [MODEL=MIKE1 AREA=21.18] ! fb=286.01
TLINP_T55  55  56  Z=75.00 L=66.79 K=7 A=0.000000e+00 F=10.000000
S1PA_D56  56  0  [MODEL=MIKE1 AREA=20.86] ! fb=290.43
TLINP_T56  56  57  Z=75.00 L=65.78 K=7 A=0.000000e+00 F=10.000000
S1PA_D57  57  0  [MODEL=MIKE1 AREA=20.54] ! fb=294.92
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```
TLINP_T57  57  58  Z=75.00 L=64.77 K=7 A=0.000000e+00 F=10.000000
S1PA_D58  58  0  [MODEL=MIKE1 AREA=20.23] ! fb=299.47
TLINP_T58  58  59  Z=75.00 L=63.79 K=7 A=0.000000e+00 F=10.000000
S1PA_D59  59  0  [MODEL=MIKE1 AREA=19.92] ! fb=304.10
TLINP_T59  59  60  Z=75.00 L=62.82 K=7 A=0.000000e+00 F=10.000000
S1PA_D60  60  0  [MODEL=MIKE1 AREA=19.62] ! fb=308.80
TLINP_T60  60  61  Z=75.00 L=61.86 K=7 A=0.000000e+00 F=10.000000
S1PA_D61  61  0  [MODEL=MIKE1 AREA=19.32] ! fb=313.57
TLINP_T61  61  62  Z=75.00 L=60.92 K=7 A=0.000000e+00 F=10.000000
S1PA_D62  62  0  [MODEL=MIKE1 AREA=19.03] ! fb=318.41
TLINP_T62  62  63  Z=75.00 L=60.00 K=7 A=0.000000e+00 F=10.000000
S1PA_D63  63  0  [MODEL=MIKE1 AREA=18.74] ! fb=323.33
TLINP_T63  63  64  Z=75.00 L=59.08 K=7 A=0.000000e+00 F=10.000000
S1PA_D64  64  0  [MODEL=MIKE1 AREA=18.45] ! fb=328.32
TLINP_T64  64  65  Z=75.00 L=58.18 K=7 A=0.000000e+00 F=10.000000
S1PA_D65  65  0  [MODEL=MIKE1 AREA=18.17] ! fb=333.39
TLINP_T65  65  66  Z=75.00 L=57.30 K=7 A=0.000000e+00 F=10.000000
S1PA_D66  66  0  [MODEL=MIKE1 AREA=17.90] ! fb=338.54
TLINP_T66  66  67  Z=75.00 L=56.43 K=7 A=0.000000e+00 F=10.000000
S1PA_D67  67  0  [MODEL=MIKE1 AREA=17.62] ! fb=343.77
TLINP_T67  67  68  Z=75.00 L=55.57 K=7 A=0.000000e+00 F=10.000000
S1PA_D68  68  0  [MODEL=MIKE1 AREA=17.36] ! fb=349.08
TLINP_T68  68  69  Z=75.00 L=54.72 K=7 A=0.000000e+00 F=10.000000
S1PA_D69  69  0  [MODEL=MIKE1 AREA=17.09] ! fb=354.47
TLINP_T69  69  70  Z=75.00 L=53.89 K=7 A=0.000000e+00 F=10.000000
S1PA_D70  70  0  [MODEL=MIKE1 AREA=16.83] ! fb=359.95
TLINP_T70  70  71  Z=75.00 L=53.07 K=7 A=0.000000e+00 F=10.000000
S1PA_D71  71  0  [MODEL=MIKE1 AREA=16.58] ! fb=365.51
TLINP_T71  71  72  Z=75.00 L=52.26 K=7 A=0.000000e+00 F=10.000000
S1PA_D72  72  0  [MODEL=MIKE1 AREA=16.32] ! fb=371.16
TLINP_T72  72  73  Z=75.00 L=51.47 K=7 A=0.000000e+00 F=10.000000
S1PA_D73  73  0  [MODEL=MIKE1 AREA=16.08] ! fb=376.89
TLINP_T73  73  74  Z=75.00 L=50.69 K=7 A=0.000000e+00 F=10.000000
S1PA_D74  74  0  [MODEL=MIKE1 AREA=15.83] ! fb=382.71
TLINP_T74  74  75  Z=75.00 L=49.92 K=7 A=0.000000e+00 F=10.000000
S1PA_D75  75  0  [MODEL=MIKE1 AREA=15.59] ! fb=388.62
TLINP_T75  75  76  Z=75.00 L=49.16 K=7 A=0.000000e+00 F=10.000000
S1PA_D76  76  0  [MODEL=MIKE1 AREA=15.35] ! fb=394.62
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```
TLINP_T76  76  77  Z=75.00 L=48.41 K=7 A=0.000000e+00 F=10.000000
S1PA_D77  77  0  [MODEL=MIKE1 AREA=15.12] ! fb=400.72
TLINP_T77  77  78  Z=75.00 L=47.67 K=7 A=0.000000e+00 F=10.000000
S1PA_D78  78  0  [MODEL=MIKE1 AREA=14.89] ! fb=406.91
TLINP_T78  78  79  Z=75.00 L=46.95 K=7 A=0.000000e+00 F=10.000000
S1PA_D79  79  0  [MODEL=MIKE1 AREA=14.66] ! fb=413.20
TLINP_T79  79  80  Z=75.00 L=46.23 K=7 A=0.000000e+00 F=10.000000
S1PA_D80  80  0  [MODEL=MIKE1 AREA=14.44] ! fb=419.58
TLINP_T80  80  81  Z=75.00 L=45.53 K=7 A=0.000000e+00 F=10.000000
S1PA_D81  81  0  [MODEL=MIKE1 AREA=14.22] ! fb=426.06
TLINP_T81  81  82  Z=75.00 L=44.84 K=7 A=0.000000e+00 F=10.000000
S1PA_D82  82  0  [MODEL=MIKE1 AREA=14.00] ! fb=432.64
TLINP_T82  82  83  Z=75.00 L=44.15 K=7 A=0.000000e+00 F=10.000000
S1PA_D83  83  0  [MODEL=MIKE1 AREA=13.79] ! fb=439.32
TLINP_T83  83  84  Z=75.00 L=43.48 K=7 A=0.000000e+00 F=10.000000
S1PA_D84  84  0  [MODEL=MIKE1 AREA=13.58] ! fb=446.11
TLINP_T84  84  85  Z=75.00 L=42.82 K=7 A=0.000000e+00 F=10.000000
S1PA_D85  85  0  [MODEL=MIKE1 AREA=13.37] ! fb=453.00
TLINP_T85  85  86  Z=75.00 L=42.17 K=7 A=0.000000e+00 F=10.000000
S1PA_D86  86  0  [MODEL=MIKE1 AREA=13.17] ! fb=460.00
TLINP_T86  86  87  Z=75.00 L=41.53 K=7 A=0.000000e+00 F=10.000000
S1PA_D87  87  0  [MODEL=MIKE1 AREA=12.97] ! fb=467.10
TLINP_T87  87  88  Z=75.00 L=40.90 K=7 A=0.000000e+00 F=10.000000
S1PA_D88  88  0  [MODEL=MIKE1 AREA=12.77] ! fb=474.32
TLINP_T88  88  89  Z=75.00 L=40.28 K=7 A=0.000000e+00 F=10.000000
S1PA_D89  89  0  [MODEL=MIKE1 AREA=12.58] ! fb=481.64
TLINP_T89  89  90  Z=75.00 L=39.66 K=7 A=0.000000e+00 F=10.000000
S1PA_D90  90  0  [MODEL=MIKE1 AREA=12.39] ! fb=489.08
TLINP_T90  90  91  Z=75.00 L=39.06 K=7 A=0.000000e+00 F=10.000000
S1PA_D91  91  0  [MODEL=MIKE1 AREA=12.20] ! fb=496.64
TLINP_T91  91  92  Z=75.00 L=38.47 K=7 A=0.000000e+00 F=10.000000
S1PA_D92  92  0  [MODEL=MIKE1 AREA=12.01] ! fb=504.31
TLINP_T92  92  93  Z=75.00 L=37.88 K=7 A=0.000000e+00 F=10.000000
S1PA_D93  93  0  [MODEL=MIKE1 AREA=11.83] ! fb=512.10
TLINP_T93  93  94  Z=75.00 L=37.30 K=7 A=0.000000e+00 F=10.000000
S1PA_D94  94  0  [MODEL=MIKE1 AREA=11.65] ! fb=520.01
TLINP_T94  94  95  Z=75.00 L=36.74 K=7 A=0.000000e+00 F=10.000000
S1PA_D95  95  0  [MODEL=MIKE1 AREA=11.47] ! fb=528.04
```

```
TLINP_T95  95  96  Z=75.00 L=36.18 K=7 A=0.000000e+00 F=10.000000
S1PA_D96  96  0  [MODEL=MIKE1 AREA=11.30] ! fb=536.20
TLINP_T96  96  97  Z=75.00 L=35.63 K=7 A=0.000000e+00 F=10.000000
S1PA_D97  97  0  [MODEL=MIKE1 AREA=11.13] ! fb=544.48
TLINP_T97  97  98  Z=75.00 L=35.09 K=7 A=0.000000e+00 F=10.000000
S1PA_D98  98  0  [MODEL=MIKE1 AREA=10.96] ! fb=552.89
TLINP_T98  98  99  Z=75.00 L=34.55 K=7 A=0.000000e+00 F=10.000000
S1PA_D99  99  0  [MODEL=MIKE1 AREA=10.79] ! fb=561.43
TLINP_T99  99  100  Z=75.00 L=34.03 K=7 A=0.000000e+00 F=10.000000
S1PA_D100  100  0  [MODEL=MIKE1 AREA=10.63] ! fb=570.10
TLINP_T100  100  101  Z=75.00 L=33.51 K=7 A=0.000000e+00 F=10.000000
S1PA_D101  101  0  [MODEL=MIKE1 AREA=10.47] ! fb=578.91
TLINP_T101  101  102  Z=75.00 L=33.00 K=7 A=0.000000e+00 F=10.000000
S1PA_D102  102  0  [MODEL=MIKE1 AREA=10.31] ! fb=587.85
TLINP_T102  102  103  Z=75.00 L=32.50 K=7 A=0.000000e+00 F=10.000000
S1PA_D103  103  0  [MODEL=MIKE1 AREA=10.15] ! fb=596.93
TLINP_T103  103  104  Z=75.00 L=32.00 K=7 A=0.000000e+00 F=10.000000
S1PA_D104  104  0  [MODEL=MIKE1 AREA=10.00] ! fb=606.15
TLINP_T104  104  105  Z=75.00 L=31.52 K=7 A=0.000000e+00 F=10.000000
S1PA_D105  105  0  [MODEL=MIKE1 AREA=9.84] ! fb=615.51
TLINP_T105  105  106  Z=75.00 L=31.04 K=7 A=0.000000e+00 F=10.000000
S1PA_D106  106  0  [MODEL=MIKE1 AREA=9.69] ! fb=625.02
TLINP_T106  106  107  Z=75.00 L=30.56 K=7 A=0.000000e+00 F=10.000000
S1PA_D107  107  0  [MODEL=MIKE1 AREA=9.55] ! fb=634.67
TLINP_T107  107  108  Z=75.00 L=30.10 K=7 A=0.000000e+00 F=10.000000
S1PA_D108  108  0  [MODEL=MIKE1 AREA=9.40] ! fb=644.48
TLINP_T108  108  109  Z=75.00 L=29.64 K=7 A=0.000000e+00 F=10.000000
S1PA_D109  109  0  [MODEL=MIKE1 AREA=9.26] ! fb=654.43
TLINP_T109  109  110  Z=75.00 L=29.19 K=7 A=0.000000e+00 F=10.000000
S1PA_D110  110  0  [MODEL=MIKE1 AREA=9.12] ! fb=664.54
TLINP_T110  110  111  Z=75.00 L=28.75 K=7 A=0.000000e+00 F=10.000000
S1PA_D111  111  0  [MODEL=MIKE1 AREA=8.98] ! fb=674.81
TLINP_T111  111  112  Z=75.00 L=28.31 K=7 A=0.000000e+00 F=10.000000
S1PA_D112  112  0  [MODEL=MIKE1 AREA=8.84] ! fb=685.23
TLINP_T112  112  113  Z=75.00 L=27.88 K=7 A=0.000000e+00 F=10.000000
S1PA_D113  113  0  [MODEL=MIKE1 AREA=8.71] ! fb=695.81
TLINP_T113  113  114  Z=75.00 L=27.45 K=7 A=0.000000e+00 F=10.000000
S1PA_D114  114  0  [MODEL=MIKE1 AREA=8.57] ! fb=706.56
```

```
   TLINP_T114  114  115  Z=75.00 L=27.04 K=7 A=0.000000e+00 F=10.000000
   S1PA_D115  115  0  [MODEL=MIKE1 AREA=8.44] ! fb=717.47
   TLINP_T115  115  116  Z=75.00 L=26.63 K=7 A=0.000000e+00 F=10.000000
   S1PA_D116  116  0  [MODEL=MIKE1 AREA=8.32] ! fb=728.56
   TLINP_T116  116  117  Z=75.00 L=26.22 K=7 A=0.000000e+00 F=10.000000
   S1PA_D117  117  0  [MODEL=MIKE1 AREA=8.19] ! fb=739.81
   TLINP_T117  117  118  Z=75.00 L=25.82 K=7 A=0.000000e+00 F=10.000000
   S1PA_D118  118  0  [MODEL=MIKE1 AREA=8.06] ! fb=751.24
   TLINP_T118  118  119  Z=75.00 L=25.43 K=7 A=0.000000e+00 F=10.000000
   S1PA_D119  119  0  [MODEL=MIKE1 AREA=7.94] ! fb=762.84
   TLINP_T119  119  120  Z=75.00 L=25.04 K=7 A=0.000000e+00 F=10.000000
   S1PA_D120  120  0  [MODEL=MIKE1 AREA=7.82] ! fb=774.63
   TLINP_T120  120  121  Z=75.00 L=24.66 K=7 A=0.000000e+00 F=10.000000
   S1PA_D121  121  0  [MODEL=MIKE1 AREA=7.70] ! fb=786.59
   TLINP_T121  121  122  Z=75.00 L=24.29 K=7 A=0.000000e+00 F=10.000000
   S1PA_D122  122  0  [MODEL=MIKE1 AREA=7.59] ! fb=798.74
   TLINP_T122  122  123  Z=75.00 L=12.05 K=7 A=0.000000e+00 F=10.000000
   DEF2P  201  123  NLTL
! Total number of squares is 1328.93
MODEL
   MIKE2 D RS=58.260000 CJO=1.840000E-15 VJ=0.800000 &
          M=0.500000 IS=1.000000E-12 N=1.200000
   MIKE1 D RS=29.260000 CJO=1.840000E-15 VJ=0.800000 &
          M=0.500000 IS=1.000000E-12 N=1.200000
SOURCE
   NLTL RES_RIN  201 202 R=50
   NLTL IVS_VIN  202  0  TRAN=SIN(-6 6 12E9 0 0 90)
   NLTL RES_RL   123  0  R=50
CONTROL
   NLTL TRAN 10E-12 2E-10
SPICEOUT
   NLTL TRAN V(123)
```

A.3 Layout File

```
! Academy file for NLTL with 125.00 GHz initial Bragg frequency,
! 800.00 GHz final Bragg frequency and 0.984789 tapering rule,
! and 60.00 ps total compression.
```

```
DIM
   LNG UM
CKT
   NLTLA_U1  1  2  Z=75.00 W=14 ADI=48.47 LLI=154.00 LAM=3.0 LAMS=2
LAMO=2 ! fb=125.00
   NLTLA_U2  2  3  Z=75.00 W=14 ADI=47.73 LLI=151.65 LAM=3.0 LAMS=2
LAMO=2 ! fb=126.93
   NLTLA_U3  3  4  Z=75.00 W=14 ADI=47.01 LLI=149.35 LAM=3.0 LAMS=2
LAMO=2 ! fb=128.89
   NLTLA_U4  4  5  Z=75.00 W=14 ADI=46.29 LLI=147.08 LAM=3.0 LAMS=2
LAMO=2 ! fb=130.88
   NLTLA_U5  5  6  Z=75.00 W=14 ADI=45.59 LLI=144.84 LAM=3.0 LAMS=2
LAMO=2 ! fb=132.90
   NLTLD_U6  6  7  Z=75.00 W=13 ADI=44.89 LLI=142.64 LAM=3.0 LAMS=2
LAMO=2 ! fb=134.96
   NLTLA_U7  7  8  Z=75.00 W=13 ADI=44.21 LLI=140.47 LAM=3.0 LAMS=2
LAMO=2 ! fb=137.04
   NLTLA_U8  8  9  Z=75.00 W=13 ADI=43.54 LLI=138.33 LAM=3.0 LAMS=2
LAMO=2 ! fb=139.16
   NLTLA_U9  9  10  Z=75.00 W=13 ADI=42.88 LLI=136.22 LAM=3.0 LAMS=2
LAMO=2 ! fb=141.31
   NLTLA_U10  10  11  Z=75.00 W=13 ADI=42.22 LLI=134.15 LAM=3.0 LAMS=2
LAMO=2 ! fb=143.49
   NLTLD_U11  11  12  Z=75.00 W=12 ADI=41.58 LLI=132.11 LAM=3.0 LAMS=2
LAMO=2 ! fb=145.71
   NLTLA_U12  12  13  Z=75.00 W=12 ADI=40.95 LLI=130.10 LAM=3.0 LAMS=2
LAMO=2 ! fb=147.96
   NLTLA_U13  13  14  Z=75.00 W=12 ADI=40.33 LLI=128.12 LAM=3.0 LAMS=2
LAMO=2 ! fb=150.24
   NLTLA_U14  14  15  Z=75.00 W=12 ADI=39.71 LLI=126.17 LAM=3.0 LAMS=2
LAMO=2 ! fb=152.56
   NLTLA_U15  15  16  Z=75.00 W=12 ADI=39.11 LLI=124.25 LAM=3.0 LAMS=2
LAMO=2 ! fb=154.92
   NLTLD_U16  16  17  Z=75.00 W=11 ADI=38.51 LLI=122.36 LAM=3.0 LAMS=2
LAMO=2 ! fb=157.31
   NLTLA_U17  17  18  Z=75.00 W=11 ADI=37.93 LLI=120.50 LAM=3.0 LAMS=2
LAMO=2 ! fb=159.74
   NLTLA_U18  18  19  Z=75.00 W=11 ADI=37.35 LLI=118.67 LAM=3.0 LAMS=2
```

```
LAMO=2 ! fb=162.21
   NLTLA_U19  19  20  Z=75.00 W=11 ADI=36.78 LLI=116.87 LAM=3.0 LAMS=2
LAMO=2 ! fb=164.72
   NLTLA_U20  20  21  Z=75.00 W=11 ADI=36.22 LLI=115.09 LAM=3.0 LAMS=2
LAMO=2 ! fb=167.26
   NLTLA_U21  21  22  Z=75.00 W=11 ADI=35.67 LLI=113.34 LAM=3.0 LAMS=2
LAMO=2 ! fb=169.84
   NLTLD_U22  22  23  Z=75.00 W=10 ADI=35.13 LLI=111.61 LAM=3.0 LAMS=2
LAMO=2 ! fb=172.47
   NLTLA_U23  23  24  Z=75.00 W=10 ADI=34.59 LLI=109.92 LAM=3.0 LAMS=2
LAMO=2 ! fb=175.13
   NLTLA_U24  24  25  Z=75.00 W=10 ADI=34.07 LLI=108.24 LAM=3.0 LAMS=2
LAMO=2 ! fb=177.84
   NLTLA_U25  25  26  Z=75.00 W=10 ADI=33.55 LLI=106.60 LAM=3.0 LAMS=2
LAMO=2 ! fb=180.58
   NLTLA_U26  26  27  Z=75.00 W=10 ADI=33.04 LLI=104.98 LAM=3.0 LAMS=2
LAMO=2 ! fb=183.37
   NLTLA_U27  27  28  Z=75.00 W=10 ADI=32.54 LLI=103.38 LAM=3.0 LAMS=2
LAMO=2 ! fb=186.21
   NLTLD_U28  28  29  Z=75.00 W=9 ADI=32.04 LLI=101.81 LAM=3.0 LAMS=2
LAMO=2 ! fb=189.08
   NLTLA_U29  29  30  Z=75.00 W=9 ADI=31.55 LLI=100.26 LAM=3.0 LAMS=2
LAMO=2 ! fb=192.00
   NLTLA_U30  30  31  Z=75.00 W=9 ADI=31.07 LLI=98.73 LAM=3.0 LAMS=2
LAMO=2 ! fb=194.97
   NLTLA_U31  31  32  Z=75.00 W=9 ADI=30.60 LLI=97.23 LAM=3.0 LAMS=2
LAMO=2 ! fb=197.98
   NLTLA_U32  32  33  Z=75.00 W=9 ADI=30.14 LLI=95.75 LAM=3.0 LAMS=2
LAMO=2 ! fb=201.04
   NLTLA_U33  33  34  Z=75.00 W=9 ADI=29.68 LLI=94.29 LAM=3.0 LAMS=2
LAMO=2 ! fb=204.14
   NLTLA_U34  34  35  Z=75.00 W=9 ADI=29.23 LLI=92.86 LAM=3.0 LAMS=2
LAMO=2 ! fb=207.30
   NLTLD_U35  35  36  Z=75.00 W=8 ADI=28.78 LLI=91.45 LAM=3.0 LAMS=2
LAMO=2 ! fb=210.50
   NLTLA_U36  36  37  Z=75.00 W=8 ADI=28.34 LLI=90.06 LAM=3.0 LAMS=2
LAMO=2 ! fb=213.75
   NLTLA_U37  37  38  Z=75.00 W=8 ADI=27.91 LLI=88.69 LAM=3.0 LAMS=2
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```
LAMO=2 ! fb=217.05
   NLTLA_U38  38  39  Z=75.00 W=8 ADI=27.49 LLI=87.34 LAM=3.0 LAMS=2
LAMO=2 ! fb=220.40
   NLTLA_U39  39  40  Z=75.00 W=8 ADI=27.07 LLI=86.01 LAM=3.0 LAMS=2
LAMO=2 ! fb=223.81
   NLTLA_U40  40  41  Z=75.00 W=8 ADI=26.66 LLI=84.70 LAM=3.0 LAMS=2
LAMO=2 ! fb=227.27
   NLTLA_U41  41  42  Z=75.00 W=8 ADI=26.25 LLI=83.41 LAM=3.0 LAMS=2
LAMO=2 ! fb=230.78
   NLTLD_U42  42  43  Z=75.00 W=7 ADI=25.85 LLI=82.14 LAM=3.0 LAMS=2
LAMO=2 ! fb=234.34
   NLTLA_U43  43  44  Z=75.00 W=7 ADI=25.46 LLI=80.89 LAM=3.0 LAMS=2
LAMO=2 ! fb=237.96
   NLTLA_U44  44  45  Z=75.00 W=7 ADI=25.07 LLI=79.66 LAM=3.0 LAMS=2
LAMO=2 ! fb=241.64
   NLTLA_U45  45  46  Z=75.00 W=7 ADI=24.69 LLI=78.45 LAM=3.0 LAMS=2
LAMO=2 ! fb=245.37
   NLTLA_U46  46  47  Z=75.00 W=7 ADI=24.32 LLI=77.26 LAM=3.0 LAMS=1
LAMO=2 ! fb=249.16
   NLTLA_U47  47  48  Z=75.00 W=7 ADI=23.95 LLI=76.08 LAM=3.0 LAMS=1
LAMO=2 ! fb=253.01
   NLTLA_U48  48  49  Z=75.00 W=7 ADI=23.58 LLI=74.93 LAM=3.0 LAMS=1
LAMO=2 ! fb=256.91
   NLTLA_U49  49  50  Z=75.00 W=7 ADI=23.22 LLI=73.79 LAM=3.0 LAMS=1
LAMO=2 ! fb=260.88
   NLTLA_U50  50  51  Z=75.00 W=7 ADI=22.87 LLI=72.66 LAM=3.0 LAMS=1
LAMO=2 ! fb=264.91
   NLTLD_U51  51  52  Z=75.00 W=6 ADI=22.52 LLI=71.56 LAM=3.0 LAMS=1
LAMO=2 ! fb=269.00
   NLTLA_U52  52  53  Z=75.00 W=6 ADI=22.18 LLI=70.47 LAM=3.0 LAMS=1
LAMO=2 ! fb=273.16
   NLTLA_U53  53  54  Z=75.00 W=6 ADI=21.84 LLI=69.40 LAM=3.0 LAMS=1
LAMO=2 ! fb=277.38
   NLTLA_U54  54  55  Z=75.00 W=6 ADI=21.51 LLI=68.34 LAM=3.0 LAMS=1
LAMO=2 ! fb=281.66
   NLTLA_U55  55  56  Z=75.00 W=6 ADI=21.18 LLI=67.30 LAM=3.0 LAMS=1
LAMO=2 ! fb=286.01
   NLTLA_U56  56  57  Z=75.00 W=6 ADI=20.86 LLI=66.28 LAM=3.0 LAMS=1
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```
LAMO=2 ! fb=290.43
   NLTLA_U57  57  58  Z=75.00 W=6 ADI=20.54 LLI=65.27 LAM=3.0 LAMS=1
LAMO=2 ! fb=294.92
   NLTLA_U58  58  59  Z=75.00 W=6 ADI=20.23 LLI=64.28 LAM=3.0 LAMS=1
LAMO=2 ! fb=299.47
   NLTLA_U59  59  60  Z=75.00 W=6 ADI=19.92 LLI=63.30 LAM=3.0 LAMS=1
LAMO=2 ! fb=304.10
   NLTLA_U60  60  61  Z=75.00 W=6 ADI=19.62 LLI=62.34 LAM=3.0 LAMS=1
LAMO=2 ! fb=308.80
   NLTLD_U61  61  62  Z=75.00 W=5 ADI=19.32 LLI=61.39 LAM=3.0 LAMS=1
LAMO=2 ! fb=313.57
   NLTLA_U62  62  63  Z=75.00 W=5 ADI=19.03 LLI=60.46 LAM=3.0 LAMS=1
LAMO=2 ! fb=318.41
   NLTLA_U63  63  64  Z=75.00 W=5 ADI=18.74 LLI=59.54 LAM=3.0 LAMS=1
LAMO=2 ! fb=323.33
   NLTLA_U64  64  65  Z=75.00 W=5 ADI=18.45 LLI=58.63 LAM=3.0 LAMS=1
LAMO=2 ! fb=328.32
   NLTLA_U65  65  66  Z=75.00 W=5 ADI=18.17 LLI=57.74 LAM=3.0 LAMS=1
LAMO=2 ! fb=333.39
   NLTLA_U66  66  67  Z=75.00 W=5 ADI=17.90 LLI=56.86 LAM=3.0 LAMS=1
LAMO=2 ! fb=338.54
   NLTLA_U67  67  68  Z=75.00 W=5 ADI=17.62 LLI=56.00 LAM=3.0 LAMS=1
LAMO=2 ! fb=343.77
   NLTLA_U68  68  69  Z=75.00 W=5 ADI=17.36 LLI=55.14 LAM=3.0 LAMS=1
LAMO=2 ! fb=349.08
   NLTLA_U69  69  70  Z=75.00 W=5 ADI=17.09 LLI=54.30 LAM=3.0 LAMS=1
LAMO=2 ! fb=354.47
   NLTLA_U70  70  71  Z=75.00 W=5 ADI=16.83 LLI=53.48 LAM=3.0 LAMS=1
LAMO=2 ! fb=359.95
   NLTLA_U71  71  72  Z=75.00 W=5 ADI=16.58 LLI=52.66 LAM=3.0 LAMS=1
LAMO=2 ! fb=365.51
   NLTLA_U72  72  73  Z=75.00 W=5 ADI=16.32 LLI=51.86 LAM=3.0 LAMS=1
LAMO=2 ! fb=371.16
   NLTLD_U73  73  74  Z=75.00 W=4 ADI=16.08 LLI=51.07 LAM=3.0 LAMS=1
LAMO=2 ! fb=376.89
   NLTLA_U74  74  75  Z=75.00 W=4 ADI=15.83 LLI=50.30 LAM=3.0 LAMS=1
LAMO=2 ! fb=382.71
   NLTLA_U75  75  76  Z=75.00 W=4 ADI=15.59 LLI=49.53 LAM=3.0 LAMS=1
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LAMO=2 ! fb=388.62
   NLTLA_U76  76  77  Z=75.00 W=4 ADI=15.35 LLI=48.78 LAM=3.0 LAMS=1
LAMO=2 ! fb=394.62
   NLTLA_U77  77  78  Z=75.00 W=4 ADI=15.12 LLI=48.04 LAM=3.0 LAMS=1
LAMO=2 ! fb=400.72
   NLTLA_U78  78  79  Z=75.00 W=4 ADI=14.89 LLI=47.31 LAM=3.0 LAMS=1
LAMO=2 ! fb=406.91
   NLTLA_U79  79  80  Z=75.00 W=4 ADI=14.66 LLI=46.59 LAM=3.0 LAMS=1
LAMO=2 ! fb=413.20
   NLTLA_U80  80  81  Z=75.00 W=4 ADI=14.44 LLI=45.88 LAM=3.0 LAMS=1
LAMO=2 ! fb=419.58
   NLTLA_U81  81  82  Z=75.00 W=4 ADI=14.22 LLI=45.18 LAM=3.0 LAMS=1
LAMO=2 ! fb=426.06
   NLTLA_U82  82  83  Z=75.00 W=4 ADI=14.00 LLI=44.49 LAM=3.0 LAMS=1
LAMO=2 ! fb=432.64
   NLTLA_U83  83  84  Z=75.00 W=4 ADI=13.79 LLI=43.82 LAM=3.0 LAMS=1
LAMO=2 ! fb=439.32
   NLTLA_U84  84  85  Z=75.00 W=4 ADI=13.58 LLI=43.15 LAM=3.0 LAMS=1
LAMO=2 ! fb=446.11
   NLTLA_U85  85  86  Z=75.00 W=4 ADI=13.37 LLI=42.49 LAM=3.0 LAMS=1
LAMO=2 ! fb=453.00
   NLTLA_U86  86  87  Z=75.00 W=4 ADI=13.17 LLI=41.85 LAM=3.0 LAMS=1
LAMO=2 ! fb=460.00
   NLTLA_U87  87  88  Z=75.00 W=4 ADI=12.97 LLI=41.21 LAM=3.0 LAMS=1
LAMO=2 ! fb=467.10
   NLTLD_U88  88  89  Z=75.00 W=3 ADI=12.77 LLI=40.58 LAM=3.0 LAMS=1
LAMO=2 ! fb=474.32
   NLTLA_U89  89  90  Z=75.00 W=3 ADI=12.58 LLI=39.97 LAM=3.0 LAMS=1
LAMO=2 ! fb=481.64
   NLTLA_U90  90  91  Z=75.00 W=3 ADI=12.39 LLI=39.36 LAM=3.0 LAMS=1
LAMO=2 ! fb=489.08
   NLTLA_U91  91  92  Z=75.00 W=3 ADI=12.20 LLI=38.76 LAM=3.0 LAMS=1
LAMO=2 ! fb=496.64
   NLTLA_U92  92  93  Z=75.00 W=3 ADI=12.01 LLI=38.17 LAM=3.0 LAMS=1
LAMO=2 ! fb=504.31
   NLTLA_U93  93  94  Z=75.00 W=3 ADI=11.83 LLI=37.59 LAM=3.0 LAMS=1
LAMO=2 ! fb=512.10
   NLTLA_U94  94  95  Z=75.00 W=3 ADI=11.65 LLI=37.02 LAM=3.0 LAMS=1
```

```
LAMO=2 ! fb=520.01
   NLTLA_U95  95  96  Z=75.00 W=3 ADI=11.47 LLI=36.45 LAM=3.0 LAMS=1
LAMO=2 ! fb=528.04
   NLTLA_U96  96  97  Z=75.00 W=3 ADI=11.30 LLI=35.90 LAM=3.0 LAMS=1
LAMO=2 ! fb=536.20
   NLTLA_U97  97  98  Z=75.00 W=3 ADI=11.13 LLI=35.35 LAM=3.0 LAMS=1
LAMO=2 ! fb=544.48
   NLTLA_U98  98  99  Z=75.00 W=3 ADI=10.96 LLI=34.82 LAM=3.0 LAMS=1
LAMO=2 ! fb=552.89
   NLTLA_U99  99  100  Z=75.00 W=3 ADI=10.79 LLI=34.29 LAM=3.0 LAMS=1
LAMO=2 ! fb=561.43
   NLTLA_U100  100  101  Z=75.00 W=3 ADI=10.63 LLI=33.77 LAM=3.0 LAMS=1
LAMO=2 ! fb=570.10
   NLTLA_U101  101  102  Z=75.00 W=3 ADI=10.47 LLI=33.25 LAM=3.0 LAMS=1
LAMO=2 ! fb=578.91
   NLTLA_U102  102  103  Z=75.00 W=3 ADI=10.31 LLI=32.75 LAM=3.0 LAMS=1
LAMO=2 ! fb=587.85
   NLTLA_U103  103  104  Z=75.00 W=3 ADI=10.15 LLI=32.25 LAM=3.0 LAMS=1
LAMO=2 ! fb=596.93
   NLTLA_U104  104  105  Z=75.00 W=3 ADI=10.00 LLI=31.76 LAM=3.0 LAMS=1
LAMO=2 ! fb=606.15
   NLTLA_U105  105  106  Z=75.00 W=3 ADI=9.84 LLI=31.27 LAM=3.0 LAMS=1
LAMO=2 ! fb=615.51
   NLTLA_U106  106  107  Z=75.00 W=3 ADI=9.69 LLI=30.80 LAM=3.0 LAMS=1
LAMO=2 ! fb=625.02
   NLTLA_U107  107  108  Z=75.00 W=3 ADI=9.55 LLI=30.33 LAM=3.0 LAMS=1
LAMO=2 ! fb=634.67
   NLTLA_U108  108  109  Z=75.00 W=3 ADI=9.40 LLI=29.87 LAM=3.0 LAMS=1
LAMO=2 ! fb=644.48
   NLTLA_U109  109  110  Z=75.00 W=3 ADI=9.26 LLI=29.41 LAM=3.0 LAMS=1
LAMO=2 ! fb=654.43
   NLTLA_U110  110  111  Z=75.00 W=3 ADI=9.12 LLI=28.97 LAM=3.0 LAMS=1
LAMO=2 ! fb=664.54
   NLTLA_U111  111  112  Z=75.00 W=3 ADI=8.98 LLI=28.53 LAM=3.0 LAMS=1
LAMO=2 ! fb=674.81
   NLTLA_U112  112  113  Z=75.00 W=3 ADI=8.84 LLI=28.09 LAM=3.0 LAMS=1
LAMO=2 ! fb=685.23
   NLTLA_U113  113  114  Z=75.00 W=3 ADI=8.71 LLI=27.66 LAM=3.0 LAMS=1
```

```
LAMO=2 ! fb=695.81
   NLTLA_U114  114  115  Z=75.00 W=3 ADI=8.57 LLI=27.24 LAM=3.0 LAMS=1
LAMO=2 ! fb=706.56
   NLTLA_U115  115  116  Z=75.00 W=3 ADI=8.44 LLI=26.83 LAM=3.0 LAMS=1
LAMO=2 ! fb=717.47
   NLTLA_U116  116  117  Z=75.00 W=3 ADI=8.32 LLI=26.42 LAM=3.0 LAMS=1
LAMO=2 ! fb=728.56
   NLTLA_U117  117  118  Z=75.00 W=3 ADI=8.19 LLI=26.02 LAM=3.0 LAMS=1
LAMO=2 ! fb=739.81
   NLTLA_U118  118  119  Z=75.00 W=3 ADI=8.06 LLI=25.62 LAM=3.0 LAMS=1
LAMO=2 ! fb=751.24
   NLTLA_U119  119  120  Z=75.00 W=3 ADI=7.94 LLI=25.23 LAM=3.0 LAMS=1
LAMO=2 ! fb=762.84
   NLTLA_U120  120  121  Z=75.00 W=3 ADI=7.82 LLI=24.85 LAM=3.0 LAMS=1
LAMO=2 ! fb=774.63
   NLTLA_U121  121  122  Z=75.00 W=3 ADI=7.70 LLI=24.47 LAM=3.0 LAMS=1
LAMO=2 ! fb=786.59
   NLTLA_U122  122  123  Z=75.00 W=3 ADI=7.59 LLI=24.10 LAM=3.0 LAMS=1
LAMO=2 ! fb=798.74
   DEF2P 1 123 NLTL122
! Total number of squares is 1328.93
```

Appendix B

Sampling Circuit SPICE File

```
Sampler
* simulation of strobe part with 2 diodes
* Modified from Masa's HRsampler file
VS 1 0 PULSE(0 -12 5P 1.2P)
RS 1 2 50
* Length of line to monitor reflections
T2 2 0 0 3 Z0=50 TD=15P K=1 A=0 F=1MEG
R1 3 10 50
* Set cap to balnace + and - of reflected wave
C2 3 10 30F
* Set dc bias so that diodes draw 1 mA
V1 5 4 1.47
V2 0 9 1.47
* Lenght of line before diodes
T3 10 0 0 4 Z0=100 TD=0.385P K=1 A=0 F=1MEG
* Two-diode model and parasitic resistances
D1 6 5 DMOD
D2 6 5 D2
Rd 7 6 24.6
Rd1 7 8 24.6
D3 9 8 DMOD
D4 9 8 D2
* Asymmetric shorted lines
T1 4 0 0 0 Z0=100 TD=0.5P K=1 A=0 F=1MEG
T4 10 0 0 0 Z0=100 TD=0.885P K=1 A=0 F=1MEG
```

```
.MODEL DMOD D IS=51F RS=0.00 CJO=0.0000F VJ=0.800 M=0.500 BV=10
.MODEL D2 D IS=0 CJO=3.00F VJ=0.800 M=0.500 BV=10
.TRAN .05P 60P 0 .05P
.FILE TRAN V(2) V(4) V(5) V(6) V(7) I(D1) I(D2)
.END


out
   tran
   re[i[d1]] gr1
grid
 tran
 range 2.0e-11 2.2e-11 2e-13
 gr1
```

Appendix C

Detailed Process Flow

I. Self-Aligned Ohmic Contacts (Mask Layer 1, Ohmic, Dark-Field)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent e ruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer

5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)

C. Exposure

1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 10.5 sec. (79 mJ)
3. Use hard-contact (HP mode) and use our own O-ring

D. Development

1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2

E. Oxygen Plasma Descum of Photoresist

1. 300mT of O2
2. power = 100W at high frequency (13.56 MHz)
3. run for 15 seconds

F. Recess Etch

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids or bases. Wear face shield at all times while at acid hood.

1. Mix etchant

a. NH4OH : H2O2 : H2O :: 5.8 : 1 : 83
b. 21 ml : 3.6 ml : 300 ml (graduated cylinder, pipette, cylinder)
c. Use magnetic stirrer bar to agitate solution 30 min. before etch

2. Mix a dilute slution of NH4OH : H2O :: 1 : 10
3. Dektak wafer, measure photoresist thickness
4. Dip in dilute NH4OH for 20 sec.
5. Rinse in DI for 3 min.
6. Etch in NH4OH : H2O2 : H2O solution for 20 or 30 seconds

   Etch rate: Masa sees 53/sec
   Scott sees 70/sec

7. Rinse in running DI for 3 min.
8. Blow dry with N2
9. Use Dektak to determine etch depth and rate

10. Etch to get to N+ region, repeating steps 6 to 9, rotating wafer 180 after
every 30 sec of etching
G. Evaporation
1. Place wafer in E-Beam mount
2. Use aluminum ring to mask wafer edges. Only tighten the screws enough to barely hold the wafer. If the ring comes down tightly against the
wafer, the wafer will crack.
3. Make sure the crystal monitor reads <18; change if necessary
4. Pump down to at least 2 X 10-6 torr
5. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a.	Ge	108	2-3 1.75
b.	Au	102	2-3 1.90
c.	Ge	63	2-3 1.75

If the thicknesses have not been quite right, adjust the last Au thickness to give the correct stochiometric ratio of Ge:Au = 1: 1.977

d.	Au	236	2-3 1.90
e.	Ni	100	2-3 1.75
f.	Au	3000	5 1.95

(use 2 steps; allow wafer to cool for 5 min. between)
H. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--
1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2
I. Rapid Thermal Anneal
Safety Note: A wafer that is removed from the RTA is contaminated with arsenic. Rinse your wafer thoroughly under running DI. Also, if you have used

our own Si wafer, rinse it thoroughly as well before putting it away.
1. Program RTA for the following:
a. delay 20 sec.
b. ramp 30 C/sec. to 400 C
c. sustain 60 sec. 400 C
d. delay 150 sec. to cool
2. Place wafer in center of Si holder
3. Run Program
4. Rinse wafer in DI for 2 min.
5. Inspect under microscope. You should be able to see the change in the surface. If there was no change, run the program again at 10 higher temperature for 30 more seconds.
6. Measure TLM pattern, should get RC 20 m, RSH 4 /sq
7. If you don't get typical values 50%, consider changing program

II. Ion Implantation Mask (Mask Layer 2, Isolation, Dark-Field)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover
B. Silicon Dioxide Application
1. Clean the chamber as recommended on the instructions
a. 300mT of CF4 at 300W for 20 min.
2. Before turning off the CF4, set the RF power to 4 Watts
a. Switch the power toggle switch to "Low"

b. Turn on the multimeter and set it to read on the 200 mV scale
c. Adjust the power until the meter reads 4.0
d. Turn off power, then turn off CF4
3. Vacuum the chamber for 30 min. and then purge twice
4. Vent the chamber and load the wafer
5. Set the heater to 270C
6. Turn on the gases according to the directions and set as follows:
a. N2O: flow rate =25.0 sccm; set point 25.3
b. SiH4: flow rate = 70.0 sccm; set point 71.3
7. Set the controller to auto and set chamber pressure to 770mT
8. Turn on RF power and set to 5W. (The power fluctuates a lot, so monitor it carefully and keep it as close to 5W as possible.)
9. Run for 10 minutes
10. Shut down the system according to the directions
11. Allow the stage to cool to less than 100C before removing wafer
12. Use ellipsometer to measure film thickness and index
a. Thickness should be 1000
b. Index should be 1.49
13. Proceed with polyimide application immediately
C. Polyimide Application
Safety Note: The vapors from polyimide are extremely harmful. Never breathe if you put your head under the hood.
1. Mix adhesion promoter in a dropper bottle
a. One part QZ 3289 concentrate
b. Nine parts QZ 3290 dilutant
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum
4. Blow off with N2
5. Apply adhesion promoter to cover wafer
6. Spin at 5 krpm for 30 sec.
7. Let evaporate for 2 min. on chuck then blow off with N2
8. Apply Probromide 284 to cover wafer with syringe and filter
9. Spin at 6 krpm for 30 sec. (gives 1.4 m film)
10. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
11. Hard bake polyimide in petri dish without cover
Using programmable oven:
a. 90C for 30 min.
b. ramp to 170C at 5C per min.

c. hold at 170C for 40 min.
d. ramp to 240C at 2C per min.
e. hold at 240C for 20 min.
f. ramp to 170C at 2C per min

Using discrete temperature ovens:

a. 90C oven for 40 min.
b. 170C oven for 40 min. (use oven back in E-beam area)
c. ramp to 240C oven, hold for 20 min. (= 50 min. total)
d. ramp down to 170C (takes about 30 min.)

D. Oxygen Plasma

1. Set for 100 W, 300 mTorr of O2
2. Run for 1 min. (etches 0.4 m of polyimide)

E. Photoresist Application

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)

F. Exposure

1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 10.5 sec. (79 mJ)
3. Use hard-contact (HP mode) and use our own O-ring

G. Development

1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2
9. Dektak photoresist to make sure it is 1.8m thick

H. Evaporation

1. Place wafer in E-Beam mount

2. Use aluminum ring to mask wafer edges. Only tighten the screws enough to barely hold the wafer. If the ring comes down tight against the
wafer, the wafer will crack.
3. Use boom to lower sample, increasing deposition rate by a factor of 3.1
4. Make sure the crystal monitor reads <18; change if necessary
5. Pump down to at least 2 X 10-6 torr
6. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a.	Ti	2003.1=65	2-3 1.75
b.	Au	16,0003.1=5160	5-7 1.90

(use 2 steps; allow wafer to cool for 8 min. between)
I. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--
1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight.
Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Do not use ultrasonic or other mechanical means for this liftoff. It will cause some of the isolation pads to come off the polyimide.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2
J. Polyimide Post Bake (in petri dish without cover)
Using programmable oven:
a. 170C for 15 min.
b. ramp to 240C at 2C per min.
c. hold at 240C for 30 min.
d. ramp to 170C at 2C per min
Using discrete temperature ovens:
a. 170C oven for 15 min. (use oven in E-beam area)
b. ramp to 240C oven, hold for 30 min. (= 65 min. total)
c. ramp to 170C (takes about 30 min.)
K. Polyimide Etch
1. 10 min. cool down
2. Set O2 plasma for 100 W, 300 mTorr of O2 only

3. Run for 8 min. to remove all polyimide from exposed areas
4. Inspect under microscope
4. Run longer if necessary in 30 or 60 sec. steps
L. Ion Implantation
1. First call, then send via Federal Express to:
Myriam Brors
IICO Corp.
3050 Oakmead Village Drive
Santa Clara, Ca 95051
(408) 727-2547
2. Typical implant (Change implant profile to fit your epi structure)
Implantation Species Dose Energy Off Angle
Proton (H+) 1.7X1015 cm-2 180 keV 7
Proton (H+) 4X1014 cm-2 110 keV 7
keep beam current 100 A to minimize heating
M. Strip Polyimide
1. Put wafer in suspended holder and heat polyimide thinner 90C
(Set temp control to 2.5 to maintain 90C)
2. Allow wafer to soak in hot thinner for 60 min. with stirrer bar = 3-4
3. Put wafer in room temperature polyimide stripper for 10 min.
4. If some Au remains, put back in hot thinner for 60 min. as in steps 1 &
2
5. Put hot thinner into ultrasonic bath and run for 1 min.
a. By this time, all pieces of gold should be gone; goto 6.
b. If some gold pads remain, goto step 3
6. Put in room temperature stripper for 10 min.
7. Put back in hot thinner with stirrer bar for 10 min.
8. Follow with ACE, METH, ISO in squirt bottles
9. Rinse in running DI for 3 min.
10. Inspect under microscope
11. If more gold remains, repeat entire process, steps 1 to 9
N. Oxygen Plasma Clean
1. Set O2 plasma for 300 mTorr and 300 W
2. Run for 10 minutes
3. Inspect under microscope
4. If any scum remains, run in plasma for longer. IMPORTANT: Any
scum left on the oxide surface will still be left on your wafer surface
after

oxide removal. Make sure that you have a pure surface before proceeding.

O. Silicon Dioxide Removal

Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.

1. Put wafer in straight Buffer HF for 2 min.
2. Rinse in running DI for 3 min.
3. Inspect under microscope
4. Etch again in 30 sec. intervals as necessary

III. High Resolution Schottky Metal (Mask Layer 6, Dark-Field)

A. Solvent Cleaning

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. Photoresist Application

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4110 with syringe and filter to cover wafer
5. Spin at 6 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover

7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
C. Exposure
1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 7.5 sec. (57 mJ)
3. Use hard-contact (HP mode) and use our own O-ring
D. Development
1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 4 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 45 sec.
6. Develop in second beaker for 15 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2
E. Oxygen Plasma Descum of Photoresist
1. 300mT of O2
2. power = 100W at high frequency (13.56 MHz)
3. run for 15 seconds
F. Evaporation
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of
concentrated bases. Wear face shield at all times while at acid hood.
1. Mix a dilute solution of NH4OH : H2O :: 1 : 10
2. Dip in dilute NH4OH for 20 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer in E-Beam mount
6. Use aluminum ring to mask wafer edges. Only tighten the screws enough to barely hold the wafer. If the ring comes down tight against the
wafer, the wafer will crack.
7. Use boom to lower sample, increasing deposition rate by a factor of 3.1
8. Make sure the crystal monitor reads <18; change if necessary
9. Pump down to about 7 X 10-7 torr
10. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)	
a.	Ti	2003.1=65 2-3	1.75	

b. Pt 5003.1=165 2-3 2.15
c. Au 4,3403.1=1400 4-6 1.95
(use 2 steps; allow wafer to cool for 5 min. between)
G. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--
1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2

IV. Schottky Contacts and Interconnect Metal (Mask Layer 0, Dark-Field)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover
B. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring

3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)

C. Exposure

1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 10.5 sec. (79 mJ)
3. Use hard-contact (HP mode) and use our own O-ring

D. Development

1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2

E. Oxygen Plasma Descum of Photoresist

1. 300mT of O2
2. power = 100W at high frequency (13.56 MHz)
3. run for 15 seconds

F. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute soultion of NH4OH : H2O :: 1 : 10
2. Dip in dilute NH4OH for 20 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer in E-Beam mount
6. Use aluminum ring to mask wafer edges. Only tighten the screws enough to barely hold the wafer. If the ring comes down tight against the wafer, the wafer will crack.
7. Use boom to lower sample, increasing deposition rate by a factor of 3.1
8. Make sure the crystal monitor reads <18; change if necessary

9. Pump down to about 7 X 10-7 torr
10. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a.	Ti 2003.1=65	2-3	1.75
b.	Pt 5003.1=165	2-3	2.15
c.	Au 10,0003.1=3230	4-6	1.95

(use 2 steps; allow wafer to cool for 5 min. between)

G. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--

1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2

V. Silicon Nitride Capacitors (Mask Layer 3, Nitride, Dark-Field)

A. Solvent Cleaning

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. Oxygen Plasma and Ammonium Hydroxide Surface Prep

1. Set Plasma Etch system for 100 W, 300 mTorr of O2
2. Run for 1 min.
3. Mix a dilute solution of NH4OH : H2O :: 1 : 10
4. Dip in dilute NH4OH for 20 sec.

C. Nitride Deposition

1. Cleaning chamber

a. Put selection switch "PEIIA/PEIIB" to "PEIIA"
b. Open CF4 tank
c. Vacuum chamber < 50 mTorr
d. Sw gas #1 on, adjust 300 mTorr
e. RF on, adjust power to 300W, allow 5 to 20 min. (for 1 hour deposition)
f. Sw gas #1 off, RF power back to 0, RF Sw off, Close CF4 tank
g. If different kind of film is used before, clean the chamber and
h. deposit desired film on test wafer and pre-coat chamber

2. Loading Sample

a. Turn on PEII-A and PEII-B (Both should be always on)
b. Put selection switch "PEIIA/PEIIB" to "PEIIB"
c. Open desired gas tank, SiO2=Silane+N2O,SiN=Silane+N
d. Sol'n close, Vent open
e. Load sample
f. Don't put sample close to the center hole. You may lose your
g. sample.
h. Vent close, Sol'n open, wait pressure < 50 mTorr
i. Turn on Heater, check and adjust set point, wait for desired temperature
j. SiN --> 285C
k. takes 20 min, (5 min in series run)

3. Set controller (for SiN)

a. Set the SW on rear panel of PEIIA to "DEP"
b. PEIIA Gas#1 SW (CF4) on
c. PEIIB SW on front panel N2 (#3) and SiH4 (#2) on, See green
d. LED on.
e. PEIIB SW on rear panel N2 (#3) and SiH4 (#2) on
f. Set display channel to 3(N2)
g. Set flow rate dial #1 to 0.71 (always), make sure the flow rate is 25.0
h. Set display channel to 2 (SiH4)

i. Set flow rate dial #1 to 1.40 (always), make sure the flow rate is 45.0
If not, adjust trimmer with screw driver
j. Set valve controller "auto," wait until pressure become 660 mTorr adjust "setpoint" on exhaust valve controller
k. RF power on, Adjust power to 3 W, Start timer ,
5. Open chamber
a. Decrease RF power, RF power off
b. Set valve controller to "manual"
c. PDIIB SW of N2 and SiH4 on rear panel off, wait pressure < 0.01 Torr
d. PDIIB only N2 on, wait until pressure become stabilize then turn off N2 gas
e. Repeat that procedure 2 times, vent SiH4 completely
f. Sol'n valve close, vent open
6. Shut down procedure
a. Set valve controller to "manual"
b. Valve controller power off
c. PDIIB 2 SW of N2 and SiH4 on rear panel off
d. Heater sw off
e. PDII main power off
f. N2O gas SiH4 gas close
7. Use ellipsometer to measure film thickness and index
a. Thickness should be 850
b. Index should be 2.05
D. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
E. Exposure
1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 10.5 sec. (79 mJ)

3. Use hard-contact (HP mode) and use our own O-ring
F. Development
1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2
G. Etch Nitride
1. Set Plasma Etch system for 100 W, 300 mTorr of CF4
2. Run for 6 min.
H. Remove Photoresist
1. Use beaker of ACE with stirrer bar

VI. Air Bridges and Posts (Mask Layers 4 & 5, Post & AB, both Dark-Field)

NOTE: You must proceed from steps A. to I. without stopping!
A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover
B. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never

breathe if you put your head under the hood. Always hold your breath when you
open the refrigerator that has the large bottles of photoresist.
1. Cool down after dehydration, 10 min.
2. Use our own bowl and chuck without O-ring
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply AZ P4330-RS with syringe and filter to cover wafer
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
C. Exposure #1: Post Mask
1. Cool down after soft bake, 10 min.
2. Set exposure of 7.5 mW for 12.5 sec. (94 mJ)
3. Use hard-contact (HP mode) and use our own O-ring
D. Development
1. Mix AZ400 : DI H2O :: 1 : 4
2. 2 beakers of diluted developer in temperature control bath (20 C)
3. Develop in first beaker for 45 sec.
4. Develop in second beaker for 15 sec.
5. Rinse in running DI water for 3 min.
6. Blow dry with N2
7. Oxygen plasma descum
a. 300mT of O2
b. power = 100W at high frequency (13.56 MHz)
c. run for 15 seconds
8. Post Bake in 120 C oven for 30 min. in petri dish without cover
E. Gold Etch
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of
concentrated acids. Wear face shield at all times while at acid hood.
1. Mix new etchant every time: KI2/I2/H2O : H2O, 1 : 5
2. Etch for 5 sec.
3. Rinse in running DI for 3 min.
F. Sputter Flash Layer (Tom ex. 8668)
1. Loading Sample
a. Use special sample holder for Ti/Au, (stored in the right cabinet under the table at your left hand side.)
b. Mount your sample on the holder

c. Turn off ion gage (IG1, on the second panel from the top)
d. Flip toggle switch to "Vent" (on the second panel from the top)
e. Wait 40 sec, open the chamber door
f. Mount sample holder on the turn table
g. Rotate the turn table and put the sample over the Ti gun (#4, right hand side)
h. Close the chamber door
i. Flip the toggle switch to "Pump"
j. Capacitance manometer turns on automatically (first panel from the top)
k. Make sure ion gage turns on below 20 mTorr
l. Pump down to less than 5x10-6 (Wait for 30 ~ 40 min)
2. Set up
a. Zero the capacitance manometer (Use screw driver, coarse and fine)
b. Write down base pressure
c. Turn off filament with switch IG1
d. Turn on Argon, Gas selector (Adjust flow rate to 25)
e. Turn on orifice
f. Adjust pressure (use micrometer on the backside of the chamber) to 10 mT (See Cap. manometer)
g. Check DC power supply on
h. Key on power supply to "Prog", (at "Lock, you can not change setting)
3. Ti Layer
a. Adjust power level to 0.1 kW (Push "Level" and turn "Modify" knob)
b. Check ramp time 1 min, (Push "Level" and turn "Modify" knob)
c. Set timer for 1 min. and 30 sec. for 100 thick Ti (growth rate is
70 /min under this condition)
d. Set S-Gun to No. 4
e. Turn on plasma ("Output" on)
f. Open shutter, Start timer
g. Close shutter when done
h. Turn off plasma
4. Au Layer
a. Set S-Gun to No. 2

b. Rotate the sample holder to Au gun (#2)
(Rotate knob 360 with screw driver)
c. Adjust power level (0.2 kW)
d. Set timer for 3 minutes and 10 seconds for 2000 thick Au
(deposition rate is 643 /min)
e. Turn on plasma
f. Open shutter
g. Close shutter when done
h. Turn off plasma
5. Ti Layer
a. Set back to Ti gun (#4)
b. Rotate the sample holder back to Ti gun (#4)
c. Adjust power level back to 0.1 kW
d. Set timer for 4 minutes and 30 seconds for 300 thick Ti
e. Turn on plasma
f. Open shutter
g. Close shutter when done
6. Shut off
a. Turn off plasma
b. Mass flow control (Argon) off
c. Orifice off
d. Flip the toggle switch to "Vent"
e. Take out samples
f. Vacuum the system
g. Flip the toggle switch to "Pump"
G. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Immediately take wafer from sputtering machine to photoresist bench
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4330-RS with syringe and filter to cover wafer
5. Spin at 6 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
H. Exposure #2: AB Mask
1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 14 sec. (105 mJ)

3. Use hard-contact (HP mode) and use our own O-ring
I. Development
1. Mix AZ 400K : DI :: 1:4
2. 2 beakers of diluted developer in temperature control bath (20 C)
3. Develop in first beaker for 45 sec.
4. Develop in second beaker for 15 sec.
5. Rinse in running DI water for 3 min.
6. Blow dry with N2
7. Oxygen plasma descum
a. 300mT of O2
b. power = 100W at high frequency (13.56 MHz)
c. run for 15 seconds
8. Post Bake in 120 C oven for 30 min. in petri dish without cover
J. Plating Preparation
1. Clean tweezers, anode, thermometer and magnet with ISO and DI water
2. Rinse wafer in running DI for 3 min.
3. Heat 800 ml of plating solution in beaker with short stirrer bar to 45C
(temp setting = 2.0 to maintain 45C)
K. Titanium Etch
Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF
hood, and keep glassware away.
1. Dektak photoresist and record initial thickness
2. Use a swab with ACE to remove the photoresist on one edge of the wafer. This is used to make the electrical contact.
3. Mix HF : DI H2O, 1 : 20
4. Etch top layer of Ti 30 sec. (10 sec. after surface appears gold)
5. Rinse in running DI for 3 min.
L. Gold Plating
1. The plating rate depends on the size of the wafer and the number of air bridges on it, as well as the age of the plating solution. Start with a plating current of 50A for a 2 inch wafer, or scale down proportionally for smaller pieces.
2. Plate for 15 minutes with stirrer bar set to 3 and T=45C.
3. Rinse in running DI for 3 minutes
4. Blow dry with N2
5. Dektak the photoresist and calculate how much the depth has changed

6. Adjust the current to get a plating rate of 1.8m/hr.
7. Repeat steps 2 to 6 to keep close track of the plating rate
8. Plate until the top of the air bridges are even with the photoresist, for a total thickness of 3m

M. First Photoresist Layer Removal
1. Flood expose top layer for 60 sec.
2. 2 beakers of AZ 400K:DI, 1 : 1
3. Develop in first beaker for 60 sec.
4. Develop in second beaker for 30 sec.
5. Rinse in running DI water for 3 min.
6. Blow dry with N2

N. Etch First Titanium Layer
1. Use HF : DI H2O, 1 : 20 from before
2. Etch for 30 sec. with moderate agitation
3. Etch for 10 seconds after gold appears
4. Rinse in running DI water for 3 min.
5. Blow dry with N-2

O. Etch Gold Layer
1. Mix new etchant: KI2/I2/H2O : DI, 1:1
2. Etch initially for 5 sec., using stirrer bar
3. Rinse in running DI for 3 min.
4. Blow dry with N2
5. Inspect under microscope
6. If some Au is still left, etch for another 3 sec.
7. Repeat steps 2 through 6 as necessary, rotating the wafer each time

P. Etch Bottom Titanium Layer
1. use HF : DI H2O, 1 : 20 from before
2. Etch for 30 sec. with moderate agitation
3. Etch for 10 seconds after gold appears
4. Rinse in running DI water for 3 min.
5. Blow dry with N-2

Q. Remove Bottom Photoresist Layer
1. Use ACE in beaker with stirrer bar for 3 min.
2. Follow with ACE, METH, ISO in squirt bottles
3. Rinse in running DI for 3 min.
4. Blow dry with N2

Appendix D

Air Line Process Flow

I. Self-Aligned Ohmic Contacts (Mask Layer 1, Ohmic, Dark-Field)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.

6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
C. Exposure
1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 9.5 sec. (71.25 mJ)
3. Use hard-contact (HP mode) and use our own O-ring
D. Development
1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2
E. Oxygen Plasma Descum of Photoresist
1. 300mT of O2
2. power = 100W at high frequency (13.56 MHz)
3. run for 15 seconds
F. Recess Etch
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of
concentrated acids or bases. Wear face shield at all times while at acid hood.
1. Mix etchant
a. NH4OH : H2O2 : H2O :: 5.8 : 1 : 83
b. 21 ml : 3.6 ml : 300 ml (graduated cylinder, pipette, cylinder)
c. Use magnetic stirrer bar to agitate solution 30 min. before etch
2. Mix a dilute slution of NH4OH : H2O :: 1 : 10
3. Dektak wafer, measure photoresist thickness
4. Dip in dilute NH4OH for 20 sec.
5. Rinse in DI for 3 min.
6. Etch in NH4OH : H2O2 : H2O solution for 20 or 30 seconds
Etch rate: 60 - 70 /sec
7. Rinse in running DI for 3 min.
8. Blow dry with N2
9. Use Dektak to determine etch depth and rate
10. Etch to get to N+ region, repeating steps 6 to 9, rotating wafer 180

after
every 20 sec of etching
G. Evaporation
1. Place wafer in E-Beam mount
2. Make sure the crystal monitor reads <15; change if necessary
3. Pump down to at least 2 X 10-6 torr
4. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a.	Ge	108	2-3 1.75
b.	Au	102	2-3 1.90
c.	Ge	63	2-3 1.75

If the thicknesses have not been quite right, adjust the last Au thickness to give the correct stochiometric ratio of Ge:Au = 1: 1.977

d.	Au	236	2-3	1.90
e.	Ni	100	2-3	1.75
f.	Au	3000	5	1.95

(use 2 steps; allow wafer to cool for 5 min. between)
H. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--
1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2
I. Rapid Thermal Anneal
Safety Note: A wafer that is removed from the RTA is contaminated with arsenic. Rinse your wafer thoroughly under running DI. Also, if you have used
our own Si wafer, rinse it thoroughly as well before putting it away.
1. Program RTA for the following:
a. delay 20 sec.
b. ramp 30 C/sec. to 400 C
c. sustain 60 sec. 400 C

d. delay 150 sec. to cool
2. Place wafer in center of Si holder
3. Run Program
4. Rinse wafer in DI for 2 min.
5. Inspect under microscope. You should be able to see the change in the surface. If there was no change, run the program again at 10 higher
temperature for 30 more seconds.
6. Measure TLM pattern, should get RC 20 m, RSH 4 /sq
7. If you don't get typical values 50%, consider changing program

II. Ion Implantation Mask (Mask Layer 2, Isolation, Dark-Field)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover
B. Silicon Dioxide Application
1. Clean the chamber and coat
a. 30 min clean, 20 min coat: program = 30SIOCLN.prc
2. Deposit 1000: program = SIO10.prc
3. Use ellipsometer to measure film thickness and index
a. Thickness should be 1000
b. Index should be 1.49
4. Proceed with polyimide application immediately
C. Polyimide Application
Safety Note: The vapors from polyimide are extremely harmful. Never

breathe if you put your head under the hood.
1. Mix adhesion promoter in a dropper bottle
a. One part QZ 3289 concentrate
b. Nine parts QZ 3290 dilutant
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum
4. Blow off with N2
5. Apply adhesion promoter to cover wafer
6. Spin at 5 krpm for 30 sec.
7. Let evaporate for 2 min. on chuck then blow off with N2
8. Apply Probromide 284 to cover wafer with syringe and filter
9. Spin at 6 krpm for 30 sec. (gives 1.4 m film)
10. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
11. Hard bake polyimide in petri dish without cover
Using programmable oven:
a. 90C for 30 min.
b. ramp at 5C per min.to 170C
c. hold at 170C for 40 min.
d. ramp at 2C per min. to 240C
e. hold at 240C for 20 min.
f. ramp at 2C per min to 170C
Using discrete temperature ovens:
a. 90C oven for 40 min.
b. 170C oven for 40 min. (use oven back in E-beam area)
c. ramp to 240C oven, hold for 20 min. (= 50 min. total)
d. ramp down to 170C (takes about 30 min.)
D. Oxygen Plasma
1. Set for 100 W, 300 mTorr of O2
2. Run for 1 min. (etches 0.1 m of polyimide)
E. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover

7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
F. Exposure
1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 10.5 sec. (79 mJ)
3. Use hard-contact (HP mode) and use our own O-ring
G. Development
1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2
9. Dektak photoresist to make sure it is 1.8m thick
H. Evaporation
1. Place wafer in E-Beam mount
2. Use boom to lower sample, increasing deposition rate by a factor of 3.1
3. Make sure the crystal monitor reads <12; change if necessary
4. Pump down to at least 2 X 10-6 torr
5. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a.	Ti 2003.1=65	2-3	1.75
b.	Au 16,0003.1=5160	5-7	1.90

(use 2 steps; allow wafer to cool for 8 min. between)
I. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--
1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Do not use ultrasonic or other mechanical means for this liftoff. It will cause some of the isolation pads to come off the polyimide.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2

J. Polyimide Post Bake (in petri dish without cover)
Using programmable oven:
a. 170C for 15 min.
b. ramp at 2C per min. to 240C
c. hold at 240C for 30 min.
d. ramp at 2C per min. to 170C
Using discrete temperature ovens:
a. 170C oven for 15 min. (use oven in E-beam area)
b. ramp to 240C oven, hold for 30 min. (= 65 min. total)
c. ramp to 170C (takes about 30 min.)
K. Polyimide Etch
1. 10 min. cool down
2. Set O2 plasma for 100 W, 300 mTorr of O2 only
3. Run for 8 min. to remove all polyimide from exposed areas
4. Inspect under microscope
4. Run longer if necessary in 30 or 60 sec. steps
L. Ion Implantation
1. First call, then send via Federal Express to:
Michael Siu
IICO Corp.
3050 Oakmead Village Drive
Santa Clara, Ca 95051
(408) 727-2547
2. Typical implant (Change implant profile to fit your epi structure)
Implantation Species Dose Energy Off Angle
Proton (H+) 1.7X1015 cm-2 180 keV 7
Proton (H+) 4X1014 cm-2 110 keV 7
keep beam current 100 A to minimize heating
M. Strip Polyimide
1. Put wafer in suspended holder and heat polyimide thinner 90C
(Set temp control to 2.7 to maintain 90C)
2. Allow wafer to soak in hot thinner for 60 min. with stirrer bar = 3-4
3. Put wafer in room temperature polyimide stripper for 10 min.
4. If some Au remains, put back in hot thinner for 60 min. as in steps 1 &
2
5. Put hot thinner into ultrasonic bath and run for 1 min.
a. By this time, all pieces of gold should be gone; goto 6.
b. If some gold pads remain, goto step 3

6. Put in room temperature stripper for 10 min.
7. Put back in hot thinner with stirrer bar for 10 min.
8. Follow with ACE, METH, ISO in squirt bottles
9. Rinse in running DI for 3 min.
10. Inspect under microscope
11. If more gold remains, repeat entire process, steps 1 to 9

N. Oxygen Plasma Clean
1. Set O2 plasma for 300 mTorr and 300 W
2. Run for 10 minutes
3. Inspect under microscope
4. If any scum remains, run in plasma for longer. IMPORTANT: Any scum left on the oxide surface will still be left on your wafer surface after oxide removal. Make sure that you have a pure surface before proceeding.

O. Silicon Dioxide Removal
Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.
1. Put wafer in straight Buffer HF for 2 min.
2. Rinse in running DI for 3 min.
3. Inspect under microscope
4. Etch again in 30 sec. intervals as necessary

III. (Option 1) High Resolution Schottky Metal (1 m lines, 1.5 m thick Au) (Mask Layer 0, Dark-Field)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.

5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. Photoresist Application

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)

C. Exposure

1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 9.5 sec. (71.25 mJ)
3. Use hard-contact (HP mode) and use our own O-ring

D. Development

1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
3. 10 min. toluene soak
4. Blow off toluene with N2
5. Develop in first beaker for 60 sec.
6. Develop in second beaker for 30 sec.
7. Rinse in running DI water for 3 min.
8. Blow dry with N2

E. Oxygen Plasma Descum of Photoresist

1. 300mT of O2
2. power = 100W at high frequency (13.56 MHz)
3. run for 15 seconds

F. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of NH4OH : H2O :: 1 : 10
2. Dip in dilute NH4OH for 20 sec.
3. Rinse in DI for 3 min.

4. Blow dry with N2
5. Place wafer in E-Beam mount
6. Use boom to lower sample, increasing deposition rate by a factor of 3.1
7. Make sure the crystal monitor reads <14; change if necessary
8. Pump down to about 7 X 10-7 torr
9. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a.	Ti 2003.1=65	2-3	1.75
b.	Pt 5003.1=165	1.0	2.05
c.	Au 14,3003.1=4613	4-6	1.75

(use 2 steps; allow wafer to cool for 5 min. between)

G. Liftoff (in order of severity) -->> DO NOT LET ACE DRY ON WAFER! <<--
1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N2

III. (Option2) High Resolution Schottky Metal (1 m lines, 1.5 m thick Au)
(Mask Layer 0, Dark-Field)

A. Solvent Cleaning

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.

4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. PMGI Application

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply SAL110-PL1 with syringe and filter to cover wafer
5. Spin at 3.5 krpm for 30 sec.
6. Hot plate bake, 200 C, 5 min.
7. Clean the bowl and chuck with ACE while wafer is baking
8. Let wafer cool for 5 min. before applying next layer
9. Wafer on spinner chuck with vacuum, blow with N2
10. Apply SAL110-PL1 with syringe and filter to cover wafer
11. Spin at 3.5 krpm for 30 sec.
12. Hot plate bake, 200 C, 5 min.
13. Clean the bowl and chuck with ACE while wafer is baking

C. Photoresist Application

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after hot plate, 5 min.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply AZ P4110 with syringe and filter to cover wafer
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90 C, 30 min. in petri dish without cover
6. Clean the bowl and chuck with ACE (wear a Silver Shield glove)

D. Exposure

1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 8.0 sec. (60 mJ)
3. Use hard-contact (HP mode) and use our own O-ring

E. Development

1. 2 beakers of AZ 400K : DI :: 1:4 in temperature control bath (20 C)
2. Develop in first beaker for 45 sec.
3. Develop in second beaker for 20 sec.

4. Rinse in running DI water for 3 min.
5. Blow dry with N2

F. Deep UV Flood Expose

1. Turn on power switch and push start button
2. Let it warm up for 5 minutes in constant power mode
3. Change to constant intensity mode and measure
4. Set exposure time for 300 sec.
5. Flood expose wafer and set to slow rotation

G. PMGI Development

1. SAL-101 developer, do not dilute
2. Develop for 2 min.
3. Rinse in running DI for 3 min.
4. Blow dry with N2

H. Second Deep UV Flood Expose

1. Set exposure time for 20 sec.
2. Flood expose wafer and set to slow rotation
3. Shut off power and then turn back on
4. Let the fan run for 5 min. with the lamp off

I. Second PMGI Development

1. Use the same SAL-101 developer, do not dilute
2. Develop for 1 min.
3. Rinse in running DI for 3 min.
4. Blow dry with N2

J. Oxygen Plasma Descum of Photoresist

1. 300mT of O2
2. power = 100W at high frequency (13.56 MHz)
3. run for 15 seconds

K. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of NH4OH : H2O :: 1 : 10
2. Dip in dilute NH4OH for 20 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer in E-Beam mount
6. Use boom to lower sample, increasing deposition rate by a factor of 3.1

7. Make sure the crystal monitor reads <14; change if necessary
8. Pump down to < 7 X 10-7 torr
9. Deposit material:

	Material	Thickness()	Dep. Rate (/sec)
a. Ti	2003.1=65	2-3	1.75
b. Pt	5003.1=165	1.0	2.05
c. Au	14,3003.1=4613	4-6	1.75

(use 2 steps; allow wafer to cool for 5 min. between)

L. Liftoff
1. Suspend wafer in beaker of Shipley 1165 Remover, heated to 100 C
2. Stirrer bar set to speed of 3.5
3. Patterns should appear in 2 min., liftoff should take 1 hr.
4. Rinse in ACE, METH, then ISO with squirt bottle
5. Rinse in running DI water for 3 min.
6. Blow dry with N2

IV. R.I.E. Sidewall Etch (No Mask needed)

A. Solvent Cleaning

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover

B. Cl2 R.I.E. Etch
1. Load machine according to instructions
2. Pump down to 1x10-6
3. Etch conditions:

a. Cl2 flow rate = 7.0 sccm

b. chamber pressure = 1.0 mTorr
c. P=60W (this is what is controlled)
d. Voltage = 350 V
4. Etch rate is 1200/min

V. Polyimide Planarization (No Mask needed)

A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover
B. Polyimide Application
Safety Note: The vapors from polyimide are extremely harmful. Never breathe if you put your head under the hood.
1. Mix adhesion promoter in a dropper bottle
a. One part QZ 3289 concentrate
b. Nine parts QZ 3290 dilutant
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum
4. Blow off with N2
5. Apply adhesion promoter to cover wafer
6. Spin at 5 krpm for 30 sec.
7. Let evaporate for 2 min. on chuck then blow off with N2
8. Apply Probromide 284 to cover wafer with syringe and filter
9. Spin at 4 krpm for 30 sec. (gives 1.8 m film)
10. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
11. Hard bake polyimide in petri dish without cover

Using programmable oven:

a. 90C for 30 min.
b. ramp at 5C per min. to 170C
c. hold at 170C for 40 min.
d. ramp at 2C per min. to 240C
e. hold at 240C for 30 min.
f. ramp at 2C per min. to 170C

Using discrete temperature ovens:

a. 90C oven for 40 min.
b. 170C oven for 40 min. (use oven back in E-beam area)
c. ramp to 240C oven, hold for 30 min. (= 60 min. total)
d. ramp down to 170C (takes about 30 min.)

C. Photoresist Application

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood. Always hold your breath when you
open the refrigerator that has the large bottles of photoresist.

1. Use our own bowl and chuck without O-ring
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply AZ P4330-RS with syringe and filter to cover wafer
4. Spin at 5 krpm for 30 sec.
5. Soft Bake, 90C, 30 min. in petri dish without cover
6. Clean the bowl and chuck with ACE (wear a Silver Shield glove)

D. O2 R.I.E. Etch

1. Load machine according to instructions
2. Pump down to 1x10-6
3. Set up laser monitor
a. Look for diffraction pattern to identify beam
b. Set up chart recorder for 1 hour and 200mV
4. Etch conditions:
a. O2 flow rate = 7.0 sccm
b. chamber pressure = 10 mTorr
c. P=60W (this is what is controlled)
d. Voltage = 350 V
5. Etch for 23.5 cycles

E. O2 Plasma Cleanup

1. Inspect to see if all metal is clear
2. Etch as needed to expose all Au

a. 300mT of O2
b. power = 200W at low frequency
c. run for 2 min. intervals

VI. Posts and Air Bridges (Mask Layers 4 & 5, Post & AB, both Dark-Field)

NOTE: You must proceed from steps A. to I. without stopping!
A. Solvent Cleaning
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
1. Check the resistivity of the D.I. water. It should be > 17M.
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N2
8. Dehydration bake, 120C, 30 min. in petri dish without cover
B. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood. Always hold your breath when you
open the refrigerator that has the large bottles of photoresist.
1. Cool down after dehydration, 10 min.
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
C. Exposure #1: Post Mask
1. Cool down after soft bake, 10 min.

2. Set exposure of 7.5 mW for 9.5 sec. (71.25 mJ)
3. Use hard-contact (HP mode) and use our own O-ring
D. Development
1. Mix AZ400 : DI H2O :: 1 : 4
2. 2 beakers of diluted developer in temperature control bath (20 C)
3. Develop in first beaker for 45 sec.
4. Develop in second beaker for 15 sec.
5. Rinse in running DI water for 3 min.
6. Blow dry with N2
7. Oxygen plasma descum
a. 300mT of O2
b. power = 100W at high frequency (13.56 MHz)
c. run for 20 seconds
8. Post Bake in 120 C oven for 30 min. in petri dish without cover
E. Gold Etch
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of
concentrated acids. Wear face shield at all times while at acid hood.
1. Mix new etchant every time: KI2/I2/H2O : H2O, 1 : 5
2. Etch for 5 sec.
3. Rinse in running DI for 3 min.
F. Sputter Flash Layer (Tom ex. 8668)
1. Loading Sample
a. Use special sample holder for Ti/Au, (stored in the right cabinet under the table at your left hand side.)
b. Mount your sample on the holder
c. Turn off ion gage (IG1, on the second panel from the top)
d. Flip toggle switch to "Vent" (on the second panel from the top)
e. Wait 40 sec, open the chamber door
f. Mount sample holder on the turn table
g. Rotate the turn table and put the sample over the Ti gun (#4, right hand side)
h. Close the chamber door
i. Flip the toggle switch to "Pump"
j. Capacitance manometer turns on automatically (first panel from the top)
k. Make sure ion gage turns on below 20 mTorr
l. Pump down to less than 5x10-6 (Wait for 30 ~ 40 min)

2. Set up
a. Zero the capacitance manometer (Use screw driver, coarse and fine)
b. Write down base pressure
c. Turn off filament with switch IG1
d. Turn on Argon, Gas selector (Adjust flow rate to 25)
e. Turn on orifice
f. Adjust pressure (use micrometer on the backside of the chamber) to 10 mT (See Cap. manometer)
g. Check DC power supply on
h. Key on power supply to "Prog", (at "Lock, you can not change setting)
3. Ti Layer
a. Adjust power level to 0.1 kW (Push "Level" and turn "Modify" knob)
b. Check ramp time 1 min, (Push "Level" and turn "Modify" knob)
c. Set S-Gun to No. 4
d. Turn on plasma ("Output" on)
e. Open shutter, Start timer
f. Run for 4 min and 30 sec for 300 thick Ti
g. Close shutter when done
h. Turn off plasma
4. Au Layer
a. Set S-Gun to No. 2
b. Rotate the sample holder to Au gun (#2)
(Rotate knob 360 with screw driver)
c. Adjust power level (0.2 kW)
d. Turn on plasma
e. Open shutter
f. Run for 1 minutes and 40 seconds for 1100 thick Au
g. Close shutter when done
h. Turn off plasma
5. Ti Layer
a. Set back to Ti gun (#4)
b. Rotate the sample holder back to Ti gun (#4)
c. Adjust power level back to 0.1 kW
d. Turn on plasma
e. Open shutter

f. Run for 1 minutes and 30 seconds for 100 thick Ti
g. Close shutter when done
6. Shut off
a. Turn off plasma
b. Mass flow control (Argon) off
c. Orifice off
d. Set up photoresist application before venting
e. Flip the toggle switch to "Vent"
f. Take out samples
g. Vacuum the system
h. Flip the toggle switch to "Pump"
G. Photoresist Application
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
1. Immediately take wafer from sputtering machine to photoresist bench
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply AZ P4330-RS with syringe and filter to cover wafer
5. Spin at 6 krpm for 30 sec.
6. Soft Bake, 90 C, 30 min. in petri dish without cover
7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
H. Exposure #2: AB Mask
1. Cool down after soft bake, 10 min.
2. Use exposure of 7.5 mW for 14 sec. (105 mJ)
3. Use hard-contact (HP mode) and use our own O-ring
I. Development
1. Mix AZ 400K : DI :: 1:4
2. 2 beakers of diluted developer in temperature control bath (20 C)
3. Develop in first beaker for 60 sec.
4. Develop in second beaker for 60 sec.
5. Rinse in running DI water for 3 min.
6. Blow dry with N2
7. Inspect for green scum in post holes: develop more if needed
8. Flood expose for 2 minutes
9. Oxygen plasma descum
a. 300mT of O2
b. power = 100W at high frequency (13.56 MHz)
c. run for 15 seconds

10. Post Bake in 115 C oven for 30 min. in petri dish without cover
J. Plating Preparation
1. Clean tweezers, anode, thermometer and magnet with ISO and DI water
2. Rinse wafer in running DI for 3 min.
3. Heat 800 ml of plating solution in beaker with short stirrer bar to 45C (temp setting = 2.0 to maintain 45C)
K. Titanium Etch
Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.
1. Dektak photoresist and record initial thickness
2. Use a swab with ACE to remove the photoresist on one edge of the wafer. This is used to make the electrical contact.
3. Mix HF : DI H2O, 1 : 20
4. Etch top layer of Ti 25 sec. (10 sec. after surface appears gold)
5. Rinse in running DI for 3 min.
L. Gold Plating
1. The plating rate depends on the size of the wafer and the number of air bridges on it, as well as the age of the plating solution. Start with a plating current of 1.5mA for a 2 inch wafer, or scale down proportionally for smaller pieces.
2. Plate for 15 minutes with stirrer bar set to 3 and T=45C.
3. Rinse in running DI for 3 minutes
4. Blow dry with N2
5. Dektak the photoresist and calculate how much the depth has changed
6. Adjust the current to get a plating rate of 1.8m/hr.
7. Repeat steps 2 to 6 to keep close track of the plating rate
8. Plate until the top of the air bridges are even with the photoresist, for a total thickness of 3m

M. First Photoresist Layer Removal
1. 2 beakers of AZ 400K:DI, 1 : 1
2. Develop in first beaker for 60 sec.
3. Develop in second beaker for 30 sec.

4. Rinse in running DI water for 3 min.
5. Blow dry with N2
6. Inspect fop scum and use O2 plasma if necessary
a. 300mT of O2
b. power = 200W at low frequency
c. run for 3 minutes
N. Etch First Titanium Layer
1. Use HF : DI H2O, 1 : 20 from before
2. Etch for 30 sec. with moderate agitation
3. Etch for 10 seconds after gold appears
4. Rinse in running DI water for 3 min.
5. Blow dry with N-2
O. Etch Gold Layer
1. Mix new etchant: KI2/I2/H2O : DI, 1:1
2. Etch initially for 5 sec., using stirrer bar
3. Rinse in running DI for 3 min.
4. Blow dry with N2
5. Inspect under microscope
6. If some Au is still left, etch for another 3 sec.
7. Repeat steps 2 through 6 as necessary, rotating the wafer each time
P. Etch Bottom Titanium Layer
1. use HF : DI H2O, 1 : 20 from before
2. Etch for 30 sec. with moderate agitation
3. Etch for 10 seconds after gold appears
4. Rinse in running DI water for 3 min.
5. Blow dry with N-2
Q. Remove Bottom Photoresist Layer
1. Use ACE in beaker with stirrer bar for 5 min.
2. Follow with ACE, METH, ISO in squirt bottles
3. Rinse in running DI for 3 min.
4. Blow dry with N2
R. Polyimide Removal
a. Heat polyimide thinner to 90C
b. Use stirrer bar and etch polyimide for 2 hours; rotate wafer at 1 hour

Appendix E

Air Line Generation Programs

This appendix contains all the programs for generating NLTLs with air bridged transmission lines and tapered impednaces. The SPICE files contains lumped resistors to model the loss at the drive frequency.

E.1 C Program

```
/*  This program generates a shock line with a tapered              */
/*  large signal impedance using an air bridge center conductor.     */
/*  written by Scott Allen, March 23, 1993                          */

#include <stdio.h>
#include <ctype.h>
#include <string.h>
#include <math.h>

#define PI 3.141592654   /* pi   */

main() {
int n; /* total number of cells = n+1 */
int i; /* counter to keep track of current cell */
int w; /* width of center conductor */
float weff; /* effective width for use in loss calculation */
float fb0, fbx; /* starting and ending Bragg frequencies */
float zls0, zls; /* starting & current large signal impedance */
float zl; /* interconnect line impedance */
```

```
float tcomp; /* total compression desired */
float cjo, phi, m; /* diode parameters to get C-V */
float rs, rs1, rs2; /* series resistance */
float iss, in;  /* dc diode parameters */
float vmax, vmin; /* max and min voltage across diode */
float cmax, cmin; /* max and min capacitance of diode */
float qmax, qmin; /* max and min charge across diode */
float cls; /* large signal capacitance */
float cline, lline; /* C and L per unit length of interconnect line */
float k; /* tapering factor for Bragg frequency */
float lng,lngb, totlng; /* length of section, avg. of 2 adjacent, & total */
float area, fb; /* diode area required to get current fb */
float floss; /* frequency at which loss is calculated */
float Rsurf; /* surface loss on metal, normalized to 1um width */
float vatten, totatten; /* voltage attenuation and running total */
float T, delT; /* section delay and total delay */
float beta; /* constant factor to adjust impedance scaling */
float totarea; /* running toal of the diode area */
float gtog[20]; /* ground to ground spacing for each width */
float vel[20]; /* velocity in m/s for each width */
float atten; /* attenuation per um for SPICE file */
float keff; /* keff for SPICE file */
float prevlng; /* length of previous section of line */
char macro[1]; /* type of macro to use */
char a[128],b[128],fsim[64],flay[64],fprnt[64],t[1];
FILE *fs,*fl,*fp;

/*************************************************************/
/* Define line parameters */

fb0 = 260;
fbx = 1500;
tcomp = 15;
zls0 = 40;
zl = 75; /* accounts for effect of parasitic C on line */
beta = 0.0; /* Zo tapering exactly offsets line loss */
```

```
/*************************************************************/
/* Diode Parameters (1X1 diode)  (ff, ohms)        */

printf("\nDefault Diode Parameters: (1 um X 1 um)\n");
rs1 = 69.0;
rs2 = 105.0; /* 2um x 1um diode for large areas */
        cjo = 1.09;
        phi = 0.80;
        m = 0.50;
        iss = 1;
        in = 1.2;

/*  Calculate the relevant C-V parameters */
vmax = 6;
vmin = 0;
cmin = cjo/exp(m*log(1+vmax/phi));
cmax = cjo/exp(m*log(1+vmin/phi));
qmin = phi*cjo*exp((1-m)*log(1+vmin/phi))/(1-m);
qmax = phi*cjo*exp((1-m)*log(1+vmax/phi))/(1-m);
  cls = (qmax-qmin)/(vmax-vmin);
printf("cls = %.2f\n",cls);

/*************************************************************/
/*      Initialize the lookup table for velocity and spacing   */

gtog[7] = 19.0;
gtog[8] = 22.0;
gtog[9] = 25.0;
gtog[10] = 28.0;
gtog[11] = 31.0;
gtog[12] = 34.0;
gtog[13] = 37.0;
gtog[14] = 40.0;
gtog[15] = 43.0;
gtog[16] = 46.0;
/* Use pahse velocity from measured line and then take 90% of it to */
/* account for the capacitive loading of the parasitics   */
vel[7] = 2.15e8*0.9;
```

```
vel[8] = 2.10e8*0.9;
vel[9] = 2.05e8*0.9;
vel[10] = 2.00e8*0.9;
vel[11] = 1.95e8*0.9;
vel[12] = 1.90e8*0.9;
vel[13] = 1.85e8*0.9;
vel[14] = 1.80e8*0.9;
vel[15] = 1.75e8*0.9;
vel[16] = 1.70e8*0.9;


/*************************************************************/
/*  Get the names for the output file  */

printf("Please enter circuit file name: ");
scanf("%s",fsim);
strcpy(flay,fsim);
strcpy(fprnt,fsim);
strcat(fsim,"_sim.ckt");
strcat(flay,"_lay.ckt");
strcat(fprnt,".out");

fs=fopen(fsim,"w");
fl=fopen(flay,"w");
fp=fopen(fprnt,"w");

fprintf(fp,"i\tw\tlng\tzls\tdelT\tarea\tfb\n");

fprintf(fs,"! SPICE file for NLTL with %.2f GHz initial Bragg frequency,\n",fb0);
fprintf(fs,"! %.2f GHz final Bragg frequency,\n",fbx);
fprintf(fs,"! and %.2f ps total compression.\n",tcomp);
fprintf(fs,"DIM\n");
fprintf(fs,"   LNG UM\n");
fprintf(fs,"CKT\n");

fprintf(fl,"! Academy file for NLTL with %.2f GHz initial Bragg
frequency,\n",fb0);
fprintf(fl,"! %.2f GHz final Bragg frequency,\n",fbx);
```

```
fprintf(fl,"! and %.2f ps total compression.\n",tcomp);
fprintf(fl,"DIM\n");
fprintf(fl,"   LNG UM\n");
fprintf(fl,"CKT\n");


/*****************************************************************/
/* Calculate the surface resistivity assuming infinite thickness */
/*  because the air bridges are 3um thick = 6 skin depths at 40 */

floss = 40;
Rsurf = sqrt(floss*PI*1e9*2.44e-8*4*PI*1e-7);

/*****************************************************************/
/* Main body of program  */

printf("Please enter number of cells    : ");
scanf("%s",a);
n=atof(a);

zls = zls0;
w = 16;
delT = 0;
totatten = 0;
totarea = 0;
totlng = 0;
prevlng = 0.0;
k = exp(log(fbx/fb0)/(n-1));
fb = fb0/k;

for(i=1; i <= n; i++) {
fb = fb*k;

lng = 1e-3*zls/(PI*fb*zl)*vel[w]; /* in units of microns */
while ((lng < 2*gtog[w]) & (w > 7)) {
w--;
lng = 1e-3*zls/(PI*fb*zl)*vel[w];
}
```

```
if ((w==7) & (lng>35)) {
                          w=8;
lng = 1e-3*zls/(PI*fb*zl)*vel[w];
}
totlng += lng;

area = (1-zls*zls/zl/zl)/(fb*zls*PI*cls*1e-6);
totarea += area;

if (w > 8) {
weff = 9.0;
}
else {
weff=0.9*w;
}

/* Choose the layout macro to use */
if (area > 30.2) {
strcpy(macro,"A");
rs=rs2;
}
if ((area > 13.2) & (area <= 30.2)) {
strcpy(macro,"B");
rs=rs1;
}
if (area <= 13.2) {
strcpy(macro,"C");
rs=rs1;
}



vatten = (Rsurf/(2*zls*weff)*lng) +
  (2e-12*PI*PI*floss*floss*area*cls*cls*rs*zls);
totatten += 8.686*vatten;

lline = 1e-6*zl/vel[w];
cline = 1e-6*1/zl/vel[w];
```

```
T = sqrt(lng*lline*(lng*cline+area*cmax*1e-15)) -
sqrt(lng*lline*(lng*cline+area*cmin*1e-15));
delT += 1e12*T;


printf("%d\t%d\t%.1f\t%.1f\t%.1f\t%.1f\t%.1f\n",i,w,lng,zls,delT,area,fb);

fprintf(fp,"%d\t%d\t%.1f\t%.1f\t%.1f\t%.1f\t%.1f\n",i,w,lng,zls,delT,area,fb);

atten = Rsurf*lng/weff;
keff = (3.0e8/vel[w])*(3.0e8/vel[w]);
lngb = (lng+prevlng)/2.0;
if (i==1) {
lngb=lng;
}


  fprintf(fl,"   NLTL%s_U%d  %d  %d  W=%d GAP=%.1f ADI=%.1f
LLI=%.1f  ! fb=%.1f\n",macro,i,i,i+1,w,gtog[w]/2,area,lng,fb);

if(i==1) {
fprintf(fs,"   TLINP_T0 201 1 Z=%.2f L=%.0f K=%.2f A=0.00
F=0.00\n",zl,lng/2,keff);
}
fprintf(fs,"   S1PA_D%d  %d  0  [MODEL=VARACT%s AREA=%.1f] !
fb=%.2f\n",i,i,macro,area,fb);
fprintf(fs,"   RES_R%d   %d   %d   R=%.4f\n",i,i,300+i,atten);
if(i==n) {
fprintf(fs,"   TLINP_T%d  %d  %d  Z=%.2f L=%.0f K=%.2f
A=0.00 F=0.00\n",i,300+i,i+1,zl,lng/2,keff);
}
else {
fprintf(fs,"   TLINP_T%d  %d  %d  Z=%.2f L=%.0f K=%.2f
A=0.00 F=0.00\n",i,300+i,i+1,zl,lng,keff);
}

prevlng = lng;
zls = exp(beta*vatten)*zls;
```

```
}

printf("Total attenuation:  %.2f\n",totatten);
fprintf(fp,"Total attenuation:  %.2f\n",totatten);
printf("Total diode area:  %.2f\n",totarea);
fprintf(fp,"Total diode area:  %.2f\n",totarea);
printf("Total line length:  %.2f\n",totlng);
fprintf(fp,"Total line length:  %.2f\n",totlng);

fprintf(fl,"   DEF2P 1 %d NLTL%d\n",i,i-1);

fprintf(fs,"   DEF2P  201  %d  NLTL\n",i);
fprintf(fs,"MODEL\n");
fprintf(fs,"   VARACTA D RS=%f CJO=%fE-15 VJ=%f &\n",rs2,cjo,phi);
fprintf(fs,"           M=%f IS=%fE-12 N=%f\n",m,iss,in);
fprintf(fs,"   VARACTB D RS=%f CJO=%fE-15 VJ=%f &\n",rs1,cjo,phi);
fprintf(fs,"           M=%f IS=%fE-12 N=%f\n",m,iss,in);
fprintf(fs,"   VARACTC D RS=%f CJO=%fE-15 VJ=%f &\n",rs1,cjo,phi);
fprintf(fs,"           M=%f IS=%fE-12 N=%f\n",m,iss,in);
fprintf(fs,"SOURCE\n");
fprintf(fs,"   NLTL RES_RIN  201 202 R=50\n");
fprintf(fs,"   NLTL IVS_VIN  202 204  TRAN=SIN(0 12 30E9 0 0 90)\n");
fprintf(fs,"   NLTL RES_RL   %d  204  R=50\n",i);
fprintf(fs,"   NLTL IVS_VDC1 204 0 DC=-3.3\n");
fprintf(fs,"CONTROL\n");
fprintf(fs,"   NLTL TRAN 10E-12 2E-10\n");
fprintf(fs,"SPICEOUT\n");
fprintf(fs,"   NLTL TRAN V(201) V(30) V(60) V(%d)\n",i);

fclose(fs);
fclose(fl);
fclose(fp);
}
```

E.2 Line Parameters

```
i w lng zls delT area fb
```

```
1 12 55.8 20.0 0.7 102.1 260.0
2 12 55.7 20.5 1.3 96.9 266.6
3 12 55.6 20.9 1.9 92.1 273.4
4 12 55.5 21.4 2.5 87.5 280.3
5 12 55.3 21.9 3.1 83.1 287.4
6 12 55.1 22.4 3.7 79.1 294.7
7 12 54.8 22.8 4.3 75.2 302.1
8 12 54.6 23.3 4.8 71.6 309.8
9 12 54.3 23.7 5.3 68.2 317.7
10 12 53.9 24.2 5.8 65.0 325.7
11 12 53.6 24.7 6.3 61.9 334.0
12 12 53.2 25.1 6.8 59.0 342.4
13 12 52.8 25.6 7.3 56.3 351.1
14 12 52.4 26.0 7.7 53.7 360.0
15 12 52.0 26.4 8.2 51.3 369.1
16 12 51.5 26.9 8.6 49.0 378.5
17 12 51.1 27.3 9.0 46.8 388.1
18 11 51.9 27.7 9.4 44.7 397.9
19 11 51.4 28.2 9.8 42.7 408.0
20 11 50.9 28.6 10.2 40.8 418.4
21 11 50.4 29.0 10.6 39.0 429.0
22 11 49.8 29.4 10.9 37.4 439.9
23 11 49.3 29.9 11.3 35.7 451.0
24 11 48.7 30.3 11.6 34.2 462.4
25 11 48.2 30.7 11.9 32.8 474.2
26 11 47.6 31.1 12.3 31.4 486.2
27 11 47.0 31.5 12.6 30.0 498.5
28 10 47.6 31.8 12.9 28.8 511.1
29 10 46.9 32.2 13.2 27.6 524.1
30 10 46.3 32.6 13.4 26.5 537.4
31 10 45.6 32.9 13.7 25.5 551.0
32 10 45.0 33.3 14.0 24.4 565.0
33 10 44.3 33.6 14.2 23.5 579.3
34 10 43.7 34.0 14.5 22.5 594.0
35 10 43.0 34.3 14.7 21.6 609.1
36 10 42.4 34.6 15.0 20.8 624.5
37 9 42.7 35.0 15.2 20.0 640.3
38 9 42.1 35.3 15.4 19.2 656.6
```

```
39 9 41.4 35.6 15.6 18.5 673.2
40 9 40.8 35.9 15.9 17.8 690.3
41 9 40.1 36.2 16.1 17.1 707.8
42 9 39.4 36.6 16.3 16.4 725.7
43 9 38.8 36.9 16.4 15.8 744.1
44 9 38.1 37.2 16.6 15.2 763.0
45 8 38.4 37.4 16.8 14.7 782.3
46 8 37.8 37.8 17.0 14.1 802.2
47 8 37.2 38.2 17.2 13.5 822.5
48 8 36.6 38.5 17.3 13.0 843.4
49 8 36.0 38.9 17.5 12.5 864.7
50 8 35.5 39.2 17.6 12.0 886.7
51 8 34.9 39.5 17.8 11.5 909.1
52 8 34.3 39.8 17.9 11.0 932.2
53 8 33.7 40.2 18.1 10.6 955.8
54 8 33.1 40.5 18.2 10.2 980.1
55 7 33.3 40.8 18.3 9.8 1004.9
56 7 32.8 41.1 18.5 9.4 1030.4
57 7 32.3 41.5 18.6 9.1 1056.5
58 7 31.7 41.8 18.7 8.7 1083.3
59 7 31.2 42.2 18.8 8.3 1110.7
60 7 30.6 42.5 18.9 8.0 1138.9
61 7 30.1 42.8 19.0 7.7 1167.8
62 7 29.6 43.1 19.2 7.4 1197.4
63 7 29.1 43.4 19.3 7.1 1227.7
64 7 28.5 43.7 19.4 6.8 1258.9
65 7 28.0 44.0 19.5 6.6 1290.8
66 7 27.5 44.3 19.5 6.3 1323.5
67 7 27.0 44.6 19.6 6.1 1357.1
68 7 26.5 44.9 19.7 5.9 1391.5
69 7 26.0 45.2 19.8 5.6 1426.7
70 7 25.5 45.5 19.9 5.4 1462.9
71 7 25.0 45.7 20.0 5.2 1500.0
Total attenuation:  3.62
Total diode area:  2175.54
Total line length:  2993.02
```

E.3 SPICE File

```
! SPICE file for NLTL with 260.00 GHz initial Bragg frequency,
! 1500.00 GHz final Bragg frequency,
! and 20.00 ps total compression.
DIM
   LNG UM
CKT
   TLINP_T0 201 1 Z=75.00 L=28 K=3.08 A=0.00 F=0.00
   S1PA_D1  1  0  [MODEL=VARACTA AREA=102.1] ! fb=260.00
   RES_R1   1   301   R=0.3850
   TLINP_T1  301  2  Z=75.00 L=56 K=3.08 A=0.00 F=0.00
   S1PA_D2  2  0  [MODEL=VARACTA AREA=96.9] ! fb=266.59
   RES_R2   2   302   R=0.3844
   TLINP_T2  302  3  Z=75.00 L=56 K=3.08 A=0.00 F=0.00
   S1PA_D3  3  0  [MODEL=VARACTA AREA=92.1] ! fb=273.35
   RES_R3   3   303   R=0.3836
   TLINP_T3  303  4  Z=75.00 L=56 K=3.08 A=0.00 F=0.00
   S1PA_D4  4  0  [MODEL=VARACTA AREA=87.5] ! fb=280.28
   RES_R4   4   304   R=0.3825
   TLINP_T4  304  5  Z=75.00 L=55 K=3.08 A=0.00 F=0.00
   S1PA_D5  5  0  [MODEL=VARACTA AREA=83.1] ! fb=287.39
   RES_R5   5   305   R=0.3813
   TLINP_T5  305  6  Z=75.00 L=55 K=3.08 A=0.00 F=0.00
   S1PA_D6  6  0  [MODEL=VARACTA AREA=79.1] ! fb=294.67
   RES_R6   6   306   R=0.3798
   TLINP_T6  306  7  Z=75.00 L=55 K=3.08 A=0.00 F=0.00
   S1PA_D7  7  0  [MODEL=VARACTA AREA=75.2] ! fb=302.14
   RES_R7   7   307   R=0.3781
   TLINP_T7  307  8  Z=75.00 L=55 K=3.08 A=0.00 F=0.00
   S1PA_D8  8  0  [MODEL=VARACTA AREA=71.6] ! fb=309.80
   RES_R8   8   308   R=0.3763
   TLINP_T8  308  9  Z=75.00 L=55 K=3.08 A=0.00 F=0.00
   S1PA_D9  9  0  [MODEL=VARACTA AREA=68.2] ! fb=317.66
   RES_R9   9   309   R=0.3742
   TLINP_T9  309  10  Z=75.00 L=54 K=3.08 A=0.00 F=0.00
   S1PA_D10  10  0  [MODEL=VARACTA AREA=65.0] ! fb=325.71
   RES_R10   10   310   R=0.3720
```

```
TLINP_T10  310  11  Z=75.00 L=54 K=3.08 A=0.00 F=0.00
S1PA_D11  11  0  [MODEL=VARACTA AREA=61.9] ! fb=333.97
RES_R11   11   311   R=0.3696
TLINP_T11  311  12  Z=75.00 L=54 K=3.08 A=0.00 F=0.00
S1PA_D12  12  0  [MODEL=VARACTA AREA=59.0] ! fb=342.43
RES_R12   12   312   R=0.3671
TLINP_T12  312  13  Z=75.00 L=53 K=3.08 A=0.00 F=0.00
S1PA_D13  13  0  [MODEL=VARACTA AREA=56.3] ! fb=351.12
RES_R13   13   313   R=0.3644
TLINP_T13  313  14  Z=75.00 L=53 K=3.08 A=0.00 F=0.00
S1PA_D14  14  0  [MODEL=VARACTA AREA=53.7] ! fb=360.02
RES_R14   14   314   R=0.3615
TLINP_T14  314  15  Z=75.00 L=52 K=3.08 A=0.00 F=0.00
S1PA_D15  15  0  [MODEL=VARACTA AREA=51.3] ! fb=369.15
RES_R15   15   315   R=0.3585
TLINP_T15  315  16  Z=75.00 L=52 K=3.08 A=0.00 F=0.00
S1PA_D16  16  0  [MODEL=VARACTA AREA=49.0] ! fb=378.50
RES_R16   16   316   R=0.3554
TLINP_T16  316  17  Z=75.00 L=52 K=3.08 A=0.00 F=0.00
S1PA_D17  17  0  [MODEL=VARACTA AREA=46.8] ! fb=388.10
RES_R17   17   317   R=0.3522
TLINP_T17  317  18  Z=75.00 L=51 K=3.08 A=0.00 F=0.00
S1PA_D18  18  0  [MODEL=VARACTA AREA=44.7] ! fb=397.94
RES_R18   18   318   R=0.3581
TLINP_T18  318  19  Z=75.00 L=52 K=2.92 A=0.00 F=0.00
S1PA_D19  19  0  [MODEL=VARACTA AREA=42.7] ! fb=408.03
RES_R19   19   319   R=0.3547
TLINP_T19  319  20  Z=75.00 L=51 K=2.92 A=0.00 F=0.00
S1PA_D20  20  0  [MODEL=VARACTA AREA=40.8] ! fb=418.37
RES_R20   20   320   R=0.3511
TLINP_T20  320  21  Z=75.00 L=51 K=2.92 A=0.00 F=0.00
S1PA_D21  21  0  [MODEL=VARACTA AREA=39.0] ! fb=428.98
RES_R21   21   321   R=0.3475
TLINP_T21  321  22  Z=75.00 L=50 K=2.92 A=0.00 F=0.00
S1PA_D22  22  0  [MODEL=VARACTA AREA=37.4] ! fb=439.85
RES_R22   22   322   R=0.3438
TLINP_T22  322  23  Z=75.00 L=50 K=2.92 A=0.00 F=0.00
S1PA_D23  23  0  [MODEL=VARACTA AREA=35.7] ! fb=451.01
```

```
RES_R23   23   323   R=0.3400
TLINP_T23  323  24  Z=75.00 L=49 K=2.92 A=0.00 F=0.00
S1PA_D24  24  0  [MODEL=VARACTA AREA=34.2] ! fb=462.44
RES_R24   24   324   R=0.3361
TLINP_T24  324  25  Z=75.00 L=49 K=2.92 A=0.00 F=0.00
S1PA_D25  25  0  [MODEL=VARACTA AREA=32.8] ! fb=474.16
RES_R25   25   325   R=0.3322
TLINP_T25  325  26  Z=75.00 L=48 K=2.92 A=0.00 F=0.00
S1PA_D26  26  0  [MODEL=VARACTA AREA=31.4] ! fb=486.19
RES_R26   26   326   R=0.3282
TLINP_T26  326  27  Z=75.00 L=48 K=2.92 A=0.00 F=0.00
S1PA_D27  27  0  [MODEL=VARACTB AREA=30.0] ! fb=498.51
RES_R27   27   327   R=0.3241
TLINP_T27  327  28  Z=75.00 L=47 K=2.92 A=0.00 F=0.00
S1PA_D28  28  0  [MODEL=VARACTB AREA=28.8] ! fb=511.15
RES_R28   28   328   R=0.3280
TLINP_T28  328  29  Z=75.00 L=48 K=2.78 A=0.00 F=0.00
S1PA_D29  29  0  [MODEL=VARACTB AREA=27.6] ! fb=524.11
RES_R29   29   329   R=0.3236
TLINP_T29  329  30  Z=75.00 L=47 K=2.78 A=0.00 F=0.00
S1PA_D30  30  0  [MODEL=VARACTB AREA=26.5] ! fb=537.40
RES_R30   30   330   R=0.3192
TLINP_T30  330  31  Z=75.00 L=46 K=2.78 A=0.00 F=0.00
S1PA_D31  31  0  [MODEL=VARACTB AREA=25.5] ! fb=551.02
RES_R31   31   331   R=0.3147
TLINP_T31  331  32  Z=75.00 L=46 K=2.78 A=0.00 F=0.00
S1PA_D32  32  0  [MODEL=VARACTB AREA=24.4] ! fb=564.99
RES_R32   32   332   R=0.3102
TLINP_T32  332  33  Z=75.00 L=45 K=2.78 A=0.00 F=0.00
S1PA_D33  33  0  [MODEL=VARACTB AREA=23.5] ! fb=579.31
RES_R33   33   333   R=0.3057
TLINP_T33  333  34  Z=75.00 L=44 K=2.78 A=0.00 F=0.00
S1PA_D34  34  0  [MODEL=VARACTB AREA=22.5] ! fb=594.00
RES_R34   34   334   R=0.3012
TLINP_T34  334  35  Z=75.00 L=44 K=2.78 A=0.00 F=0.00
S1PA_D35  35  0  [MODEL=VARACTB AREA=21.6] ! fb=609.06
RES_R35   35   335   R=0.2967
TLINP_T35  335  36  Z=75.00 L=43 K=2.78 A=0.00 F=0.00
```

```
S1PA_D36  36  0  [MODEL=VARACTB AREA=20.8] ! fb=624.50
RES_R36   36   336   R=0.2922
TLINP_T36  336  37  Z=75.00 L=42 K=2.78 A=0.00 F=0.00
S1PA_D37  37  0  [MODEL=VARACTB AREA=20.0] ! fb=640.33
RES_R37   37   337   R=0.2948
TLINP_T37  337  38  Z=75.00 L=43 K=2.64 A=0.00 F=0.00
S1PA_D38  38  0  [MODEL=VARACTB AREA=19.2] ! fb=656.57
RES_R38   38   338   R=0.2902
TLINP_T38  338  39  Z=75.00 L=42 K=2.64 A=0.00 F=0.00
S1PA_D39  39  0  [MODEL=VARACTB AREA=18.5] ! fb=673.21
RES_R39   39   339   R=0.2857
TLINP_T39  339  40  Z=75.00 L=41 K=2.64 A=0.00 F=0.00
S1PA_D40  40  0  [MODEL=VARACTB AREA=17.8] ! fb=690.28
RES_R40   40   340   R=0.2811
TLINP_T40  340  41  Z=75.00 L=41 K=2.64 A=0.00 F=0.00
S1PA_D41  41  0  [MODEL=VARACTB AREA=17.1] ! fb=707.78
RES_R41   41   341   R=0.2765
TLINP_T41  341  42  Z=75.00 L=40 K=2.64 A=0.00 F=0.00
S1PA_D42  42  0  [MODEL=VARACTB AREA=16.4] ! fb=725.72
RES_R42   42   342   R=0.2720
TLINP_T42  342  43  Z=75.00 L=39 K=2.64 A=0.00 F=0.00
S1PA_D43  43  0  [MODEL=VARACTB AREA=15.8] ! fb=744.12
RES_R43   43   343   R=0.2675
TLINP_T43  343  44  Z=75.00 L=39 K=2.64 A=0.00 F=0.00
S1PA_D44  44  0  [MODEL=VARACTB AREA=15.2] ! fb=762.99
RES_R44   44   344   R=0.2630
TLINP_T44  344  45  Z=75.00 L=38 K=2.64 A=0.00 F=0.00
S1PA_D45  45  0  [MODEL=VARACTB AREA=14.7] ! fb=782.33
RES_R45   45   345   R=0.3310
TLINP_T45  345  46  Z=75.00 L=38 K=2.52 A=0.00 F=0.00
S1PA_D46  46  0  [MODEL=VARACTB AREA=14.1] ! fb=802.17
RES_R46   46   346   R=0.3259
TLINP_T46  346  47  Z=75.00 L=38 K=2.52 A=0.00 F=0.00
S1PA_D47  47  0  [MODEL=VARACTB AREA=13.5] ! fb=822.50
RES_R47   47   347   R=0.3208
TLINP_T47  347  48  Z=75.00 L=37 K=2.52 A=0.00 F=0.00
S1PA_D48  48  0  [MODEL=VARACTC AREA=13.0] ! fb=843.36
RES_R48   48   348   R=0.3158
```

```
TLINP_T48  348  49  Z=75.00 L=37 K=2.52 A=0.00 F=0.00
S1PA_D49  49  0  [MODEL=VARACTC AREA=12.5] ! fb=864.74
RES_R49   49   349   R=0.3107
TLINP_T49  349  50  Z=75.00 L=36 K=2.52 A=0.00 F=0.00
S1PA_D50  50  0  [MODEL=VARACTC AREA=12.0] ! fb=886.66
RES_R50   50   350   R=0.3056
TLINP_T50  350  51  Z=75.00 L=35 K=2.52 A=0.00 F=0.00
S1PA_D51  51  0  [MODEL=VARACTC AREA=11.5] ! fb=909.14
RES_R51   51   351   R=0.3006
TLINP_T51  351  52  Z=75.00 L=35 K=2.52 A=0.00 F=0.00
S1PA_D52  52  0  [MODEL=VARACTC AREA=11.0] ! fb=932.19
RES_R52   52   352   R=0.2956
TLINP_T52  352  53  Z=75.00 L=34 K=2.52 A=0.00 F=0.00
S1PA_D53  53  0  [MODEL=VARACTC AREA=10.6] ! fb=955.82
RES_R53   53   353   R=0.2906
TLINP_T53  353  54  Z=75.00 L=34 K=2.52 A=0.00 F=0.00
S1PA_D54  54  0  [MODEL=VARACTC AREA=10.2] ! fb=980.05
RES_R54   54   354   R=0.2857
TLINP_T54  354  55  Z=75.00 L=33 K=2.52 A=0.00 F=0.00
S1PA_D55  55  0  [MODEL=VARACTC AREA=9.8] ! fb=1004.90
RES_R55   55   355   R=0.3285
TLINP_T55  355  56  Z=75.00 L=33 K=2.40 A=0.00 F=0.00
S1PA_D56  56  0  [MODEL=VARACTC AREA=9.4] ! fb=1030.38
RES_R56   56   356   R=0.3231
TLINP_T56  356  57  Z=75.00 L=33 K=2.40 A=0.00 F=0.00
S1PA_D57  57  0  [MODEL=VARACTC AREA=9.1] ! fb=1056.50
RES_R57   57   357   R=0.3178
TLINP_T57  357  58  Z=75.00 L=32 K=2.40 A=0.00 F=0.00
S1PA_D58  58  0  [MODEL=VARACTC AREA=8.7] ! fb=1083.28
RES_R58   58   358   R=0.3124
TLINP_T58  358  59  Z=75.00 L=32 K=2.40 A=0.00 F=0.00
S1PA_D59  59  0  [MODEL=VARACTC AREA=8.3] ! fb=1110.75
RES_R59   59   359   R=0.3072
TLINP_T59  359  60  Z=75.00 L=31 K=2.40 A=0.00 F=0.00
S1PA_D60  60  0  [MODEL=VARACTC AREA=8.0] ! fb=1138.91
RES_R60   60   360   R=0.3019
TLINP_T60  360  61  Z=75.00 L=31 K=2.40 A=0.00 F=0.00
S1PA_D61  61  0  [MODEL=VARACTC AREA=7.7] ! fb=1167.78
```

```
   RES_R61   61   361   R=0.2967
   TLINP_T61  361  62  Z=75.00 L=30 K=2.40 A=0.00 F=0.00
   S1PA_D62  62  0  [MODEL=VARACTC AREA=7.4] ! fb=1197.39
   RES_R62   62   362   R=0.2915
   TLINP_T62  362  63  Z=75.00 L=30 K=2.40 A=0.00 F=0.00
   S1PA_D63  63  0  [MODEL=VARACTC AREA=7.1] ! fb=1227.74
   RES_R63   63   363   R=0.2863
   TLINP_T63  363  64  Z=75.00 L=29 K=2.40 A=0.00 F=0.00
   S1PA_D64  64  0  [MODEL=VARACTC AREA=6.8] ! fb=1258.87
   RES_R64   64   364   R=0.2812
   TLINP_T64  364  65  Z=75.00 L=29 K=2.40 A=0.00 F=0.00
   S1PA_D65  65  0  [MODEL=VARACTC AREA=6.6] ! fb=1290.79
   RES_R65   65   365   R=0.2761
   TLINP_T65  365  66  Z=75.00 L=28 K=2.40 A=0.00 F=0.00
   S1PA_D66  66  0  [MODEL=VARACTC AREA=6.3] ! fb=1323.51
   RES_R66   66   366   R=0.2711
   TLINP_T66  366  67  Z=75.00 L=28 K=2.40 A=0.00 F=0.00
   S1PA_D67  67  0  [MODEL=VARACTC AREA=6.1] ! fb=1357.06
   RES_R67   67   367   R=0.2661
   TLINP_T67  367  68  Z=75.00 L=27 K=2.40 A=0.00 F=0.00
   S1PA_D68  68  0  [MODEL=VARACTC AREA=5.9] ! fb=1391.47
   RES_R68   68   368   R=0.2612
   TLINP_T68  368  69  Z=75.00 L=27 K=2.40 A=0.00 F=0.00
   S1PA_D69  69  0  [MODEL=VARACTC AREA=5.6] ! fb=1426.75
   RES_R69   69   369   R=0.2563
   TLINP_T69  369  70  Z=75.00 L=26 K=2.40 A=0.00 F=0.00
   S1PA_D70  70  0  [MODEL=VARACTC AREA=5.4] ! fb=1462.92
   RES_R70   70   370   R=0.2515
   TLINP_T70  370  71  Z=75.00 L=26 K=2.40 A=0.00 F=0.00
   S1PA_D71  71  0  [MODEL=VARACTC AREA=5.2] ! fb=1500.01
   RES_R71   71   371   R=0.2467
   TLINP_T71  371  72  Z=75.00 L=13 K=2.40 A=0.00 F=0.00
   DEF2P  201  72  NLTL
MODEL
   VARACTA D RS=105.000000 CJO=1.090000E-15 VJ=0.800000 &
          M=0.500000 IS=1.000000E-12 N=1.200000
   VARACTB D RS=69.000000 CJO=1.090000E-15 VJ=0.800000 &
          M=0.500000 IS=1.000000E-12 N=1.200000
```

```
   VARACTC D RS=69.000000 CJO=1.090000E-15 VJ=0.800000 &
          M=0.500000 IS=1.000000E-12 N=1.200000
SOURCE
   NLTL RES_RIN  201 202 R=50
   NLTL IVS_VIN  202 204  TRAN=SIN(0 11.2 30E9 0 0 90)
   NLTL RES_RL   72  204  R=50
   NLTL IVS_VDC1 204 0 DC=-3.3
CONTROL
   NLTL TRAN 10E-12 2E-10
SPICEOUT
   NLTL TRAN V(201) V(30) V(60) V(72)
```

E.4 Layout File

```
! Academy file for NLTL with 260.00 GHz initial Bragg frequency,
! 1500.00 GHz final Bragg frequency,
! and 25.00 ps total compression.
DIM
   LNG UM
CKT
   NLTLA_U1  1  2  W=12 GAP=17.0 ADI=102.1 LLI=55.8  ! fb=260.0
   NLTLA_U2  2  3  W=12 GAP=17.0 ADI=96.9 LLI=55.7  ! fb=266.6
   NLTLA_U3  3  4  W=12 GAP=17.0 ADI=92.1 LLI=55.6  ! fb=273.4
   NLTLA_U4  4  5  W=12 GAP=17.0 ADI=87.5 LLI=55.5  ! fb=280.3
   NLTLA_U5  5  6  W=12 GAP=17.0 ADI=83.1 LLI=55.3  ! fb=287.4
   NLTLA_U6  6  7  W=12 GAP=17.0 ADI=79.1 LLI=55.1  ! fb=294.7
   NLTLA_U7  7  8  W=12 GAP=17.0 ADI=75.2 LLI=54.8  ! fb=302.1
   NLTLA_U8  8  9  W=12 GAP=17.0 ADI=71.6 LLI=54.6  ! fb=309.8
   NLTLA_U9  9  10  W=12 GAP=17.0 ADI=68.2 LLI=54.3  ! fb=317.7
   NLTLA_U10  10  11  W=12 GAP=17.0 ADI=65.0 LLI=53.9  ! fb=325.7
   NLTLA_U11  11  12  W=12 GAP=17.0 ADI=61.9 LLI=53.6  ! fb=334.0
   NLTLA_U12  12  13  W=12 GAP=17.0 ADI=59.0 LLI=53.2  ! fb=342.4
   NLTLA_U13  13  14  W=12 GAP=17.0 ADI=56.3 LLI=52.8  ! fb=351.1
   NLTLA_U14  14  15  W=12 GAP=17.0 ADI=53.7 LLI=52.4  ! fb=360.0
   NLTLA_U15  15  16  W=12 GAP=17.0 ADI=51.3 LLI=52.0  ! fb=369.1
   NLTLA_U16  16  17  W=12 GAP=17.0 ADI=49.0 LLI=51.5  ! fb=378.5
   NLTLA_U17  17  18  W=12 GAP=17.0 ADI=46.8 LLI=51.1  ! fb=388.1
   NLTLA_U18  18  19  W=11 GAP=15.5 ADI=44.7 LLI=51.9  ! fb=397.9
```

```
NLTLA_U19  19  20  W=11 GAP=15.5 ADI=42.7 LLI=51.4  ! fb=408.0
NLTLA_U20  20  21  W=11 GAP=15.5 ADI=40.8 LLI=50.9  ! fb=418.4
NLTLA_U21  21  22  W=11 GAP=15.5 ADI=39.0 LLI=50.4  ! fb=429.0
NLTLA_U22  22  23  W=11 GAP=15.5 ADI=37.4 LLI=49.8  ! fb=439.9
NLTLA_U23  23  24  W=11 GAP=15.5 ADI=35.7 LLI=49.3  ! fb=451.0
NLTLA_U24  24  25  W=11 GAP=15.5 ADI=34.2 LLI=48.7  ! fb=462.4
NLTLA_U25  25  26  W=11 GAP=15.5 ADI=32.8 LLI=48.2  ! fb=474.2
NLTLA_U26  26  27  W=11 GAP=15.5 ADI=31.4 LLI=47.6  ! fb=486.2
NLTLB_U27  27  28  W=11 GAP=15.5 ADI=30.0 LLI=47.0  ! fb=498.5
NLTLB_U28  28  29  W=10 GAP=14.0 ADI=28.8 LLI=47.6  ! fb=511.1
NLTLB_U29  29  30  W=10 GAP=14.0 ADI=27.6 LLI=46.9  ! fb=524.1
NLTLB_U30  30  31  W=10 GAP=14.0 ADI=26.5 LLI=46.3  ! fb=537.4
NLTLB_U31  31  32  W=10 GAP=14.0 ADI=25.5 LLI=45.6  ! fb=551.0
NLTLB_U32  32  33  W=10 GAP=14.0 ADI=24.4 LLI=45.0  ! fb=565.0
NLTLB_U33  33  34  W=10 GAP=14.0 ADI=23.5 LLI=44.3  ! fb=579.3
NLTLB_U34  34  35  W=10 GAP=14.0 ADI=22.5 LLI=43.7  ! fb=594.0
NLTLB_U35  35  36  W=10 GAP=14.0 ADI=21.6 LLI=43.0  ! fb=609.1
NLTLB_U36  36  37  W=10 GAP=14.0 ADI=20.8 LLI=42.4  ! fb=624.5
NLTLB_U37  37  38  W=9 GAP=12.5 ADI=20.0 LLI=42.7  ! fb=640.3
NLTLB_U38  38  39  W=9 GAP=12.5 ADI=19.2 LLI=42.1  ! fb=656.6
NLTLB_U39  39  40  W=9 GAP=12.5 ADI=18.5 LLI=41.4  ! fb=673.2
NLTLB_U40  40  41  W=9 GAP=12.5 ADI=17.8 LLI=40.8  ! fb=690.3
NLTLB_U41  41  42  W=9 GAP=12.5 ADI=17.1 LLI=40.1  ! fb=707.8
NLTLB_U42  42  43  W=9 GAP=12.5 ADI=16.4 LLI=39.4  ! fb=725.7
NLTLB_U43  43  44  W=9 GAP=12.5 ADI=15.8 LLI=38.8  ! fb=744.1
NLTLB_U44  44  45  W=9 GAP=12.5 ADI=15.2 LLI=38.1  ! fb=763.0
NLTLB_U45  45  46  W=8 GAP=11.0 ADI=14.7 LLI=38.4  ! fb=782.3
NLTLB_U46  46  47  W=8 GAP=11.0 ADI=14.1 LLI=37.8  ! fb=802.2
NLTLB_U47  47  48  W=8 GAP=11.0 ADI=13.5 LLI=37.2  ! fb=822.5
NLTLC_U48  48  49  W=8 GAP=11.0 ADI=13.0 LLI=36.6  ! fb=843.4
NLTLC_U49  49  50  W=8 GAP=11.0 ADI=12.5 LLI=36.0  ! fb=864.7
NLTLC_U50  50  51  W=8 GAP=11.0 ADI=12.0 LLI=35.5  ! fb=886.7
NLTLC_U51  51  52  W=8 GAP=11.0 ADI=11.5 LLI=34.9  ! fb=909.1
NLTLC_U52  52  53  W=8 GAP=11.0 ADI=11.0 LLI=34.3  ! fb=932.2
NLTLC_U53  53  54  W=8 GAP=11.0 ADI=10.6 LLI=33.7  ! fb=955.8
NLTLC_U54  54  55  W=8 GAP=11.0 ADI=10.2 LLI=33.1  ! fb=980.1
NLTLC_U55  55  56  W=7 GAP=9.5 ADI=9.8 LLI=33.3  ! fb=1004.9
NLTLC_U56  56  57  W=7 GAP=9.5 ADI=9.4 LLI=32.8  ! fb=1030.4
```

```
   NLTLC_U57  57  58  W=7 GAP=9.5 ADI=9.1 LLI=32.3  ! fb=1056.5
   NLTLC_U58  58  59  W=7 GAP=9.5 ADI=8.7 LLI=31.7  ! fb=1083.3
   NLTLC_U59  59  60  W=7 GAP=9.5 ADI=8.3 LLI=31.2  ! fb=1110.7
   NLTLC_U60  60  61  W=7 GAP=9.5 ADI=8.0 LLI=30.6  ! fb=1138.9
   NLTLC_U61  61  62  W=7 GAP=9.5 ADI=7.7 LLI=30.1  ! fb=1167.8
   NLTLC_U62  62  63  W=7 GAP=9.5 ADI=7.4 LLI=29.6  ! fb=1197.4
   NLTLC_U63  63  64  W=7 GAP=9.5 ADI=7.1 LLI=29.1  ! fb=1227.7
   NLTLC_U64  64  65  W=7 GAP=9.5 ADI=6.8 LLI=28.5  ! fb=1258.9
   NLTLC_U65  65  66  W=7 GAP=9.5 ADI=6.6 LLI=28.0  ! fb=1290.8
   NLTLC_U66  66  67  W=7 GAP=9.5 ADI=6.3 LLI=27.5  ! fb=1323.5
   NLTLC_U67  67  68  W=7 GAP=9.5 ADI=6.1 LLI=27.0  ! fb=1357.1
   NLTLC_U68  68  69  W=7 GAP=9.5 ADI=5.9 LLI=26.5  ! fb=1391.5
   NLTLC_U69  69  70  W=7 GAP=9.5 ADI=5.6 LLI=26.0  ! fb=1426.7
   NLTLC_U70  70  71  W=7 GAP=9.5 ADI=5.4 LLI=25.5  ! fb=1462.9
   NLTLC_U71  71  72  W=7 GAP=9.5 ADI=5.2 LLI=25.0  ! fb=1500.0
   DEF2P 1 72 NLTL71
```

E.5 Academy Macros

```
! Macro Programs for Air Bridged Lines
!  Scott Allen   10/93
!
! Definitions for the different point types
!
iboc = 3  ! point type for begin open contour
ibccf= 4  ! point type for begin closed contour, filled
ibcce= 5  ! point type for begin closed contour, empty
ibcir= 6  ! point type for begin circle (give center)
ibhol= 7  ! point type for begin hole (give center x,y)
icon = 8  ! point type for connecting point
iarc = 9  ! point type for begin arc (give radius, sweep angle in degrees)
icen = 10 ! point type for end arc (give center x,y)
ieoc = 11 ! point type for end open contour
iecc = 12 ! point type for end closed contour
iecir= 13 ! point type for end circle (give radius, 2nd value ignored)
iiso = 14 ! point type for isolated point
!
! Definitions of the different layers
```

```
!
schint    = 0      ! schottky contacts and interconnect
ohmic     = 1      ! ohmic metal
isolation = 2      ! ion implant isolation
nitride   = 3      ! silicon nitride mask
post      = 4      ! air bridge post & capacitor contact
ab        = 5      ! air bridge
hr        = 6      ! high-res mask, 1 um features
!
!-------------------------------------------------------------------------------
!
! Line Layout Program for MACRO "NLTLA"
! Air bridged center conductor, ground plane diodes, 2um Schottky fingers
! Line tapers down to 8um at the diode
! Written by Scott Allen 10/93
!
defelem "NLTLA",2,"w","gap","adi","lli"
real w,gap,adi,lli,ldi,ctr,dx,dy,g
lli=int(0.5+lli)
w=int(0.5+w)
lam=int(0.5+lam)
ldi=0.5*int(0.5+adi/2)+.5  !add 0.5um to account for ion straggle
! Find center of the line section:
ctr=0.5*lli
g=2*(w+2*gap)
!
! Air Bridged Center Conductor
level ab
dy=(w-8)/2
dx=(lli-22)/2-dy ! 18 is total width of where ohmics are
point ibccf,0,w/-2
node n1,0,0
point icon,0,w/2
point icon,dx,w/2
point icon,dx+dy,w/2-dy
point icon,lli-dx-dy,w/2-dy
point icon,lli-dx,w/2
point icon,lli,w/2
```

```
node n2,lli,0
point icon,lli,w/-2
point icon,lli-dx,w/-2
point icon,lli-dx-dy,w/-2+dy
point icon,dx+dy,w/-2+dy
point iecc,dx,w/-2
!
! Post to Schottky Diode
level post
dx=2.5
dy=2.5
point ibccf,ctr-dx,dy
point icon,ctr+dx,dy
point icon,ctr+dx,-dy
point iecc,ctr-dx,-dy
!
! Schottky Diodes and Ground Plane
level schint
dx=1   ! center of Schottky stripe
dy=12 !  4 from center line + 2 for spacing + 2 for ohmics
! diode stripe
point ibccf,ctr-dx,dy+ldi
point icon,ctr+dx,dy+ldi
point icon,ctr+dx,-dy-ldi
point iecc,ctr-dx,-dy-ldi
! upper ground plane
dx=5   ! center of Schottky to ohmic
point ibccf,0,gap
point icon,0,(gap+g)
point icon,lli,(gap+g)
point icon,lli,(gap)
point icon,ctr+dx+4,(gap)
point icon,ctr+dx+4,(dy+ldi+8)
point icon,ctr-dx-4,(dy+ldi+8)
point iecc,ctr-dx-4,(gap)
!lower ground plane
point ibccf,0,-gap
point icon,0,-(gap+g)
```

```
point icon,lli,-(gap+g)
point icon,lli,-(gap)
point icon,ctr+dx+4,-(gap)
point icon,ctr+dx+4,-(dy+ldi+8)
point icon,ctr-dx-4,-(dy+ldi+8)
point iecc,ctr-dx-4,-(gap)
!
! Ohmics
level ohmic
dx=5  ! center of Schottky stripe to ohmic
dy=8  ! edge of ohmic: 4 + 2um space
! upper ohmic
point ibccf,ctr-dx,(dy)
point icon,ctr-dx-8,(dy)
point icon,ctr-dx-8,(dy+ldi+18)
point icon,ctr+dx+8,(dy+ldi+18)
point icon,ctr+dx+8,(dy)
point icon,ctr+dx,(dy)
point icon,ctr+dx,(dy+ldi+8)
point iecc,ctr-dx,(dy+ldi+8)
!lower ohmic
point ibccf,ctr-dx,-(dy)
point icon,ctr-dx-8,-(dy)
point icon,ctr-dx-8,-(dy+ldi+18)
point icon,ctr+dx+8,-(dy+ldi+18)
point icon,ctr+dx+8,-(dy)
point icon,ctr+dx,-(dy)
point icon,ctr+dx,-(dy+ldi+8)
point iecc,ctr-dx,-(dy+ldi+8)
! ground straps
point ibccf,ctr+dx+8,dy
point icon,ctr+dx+6,dy
point icon,ctr+dx+6,-dy
point iecc,ctr+dx+8,-dy
!
level isolation
dy=12 ! 4 + 2 spacing + 2 ohmics
point ibccf,ctr-17,dy
```

```
point icon,ctr-17,(dy+ldi+12)
point icon,ctr+17,(dy+ldi+12)
point iecc,ctr+17,dy
!
point ibccf,ctr-17,-dy
point icon,ctr-17,-(dy+ldi+12)
point icon,ctr+17,-(dy+ldi+12)
point iecc,ctr+17,-dy
!
end define
!
!-------------------------------------------------------------------------
!
! Line Layout Program for MACRO "NLTLB"
! Air bridged center conductor, ground plane diodes, 1um Schottky fingers
! Line tapers down to 8um at the diode
! Written by Scott Allen 10/93
!
defelem "NLTLB",2,"w","gap","adi","lli"
real w,gap,adi,lli,ldi,ctr,dx,dy,g
lli=int(0.5+lli)
w=int(0.5+w)
lam=int(0.5+lam)
ldi=0.5*int(0.5+adi)+.5  ! add 0.5um to account for ion straggle
! Find center of the line section:
ctr=0.5*lli
g=2*(w+2*gap)
!
! Air Bridged Center Conductor
level ab
dy=(w-8)/2
dx=(lli-21)/2-dy   ! 17um is total width of where ohmics are
point ibccf,0,w/-2
node n1,0,0
point icon,0,w/2
point icon,dx,w/2
point icon,dx+dy,w/2-dy
point icon,lli-dx-dy,w/2-dy
```

```
point icon,lli-dx,w/2
point icon,lli,w/2
node n2,lli,0
point icon,lli,w/-2
point icon,lli-dx,w/-2
point icon,lli-dx-dy,w/-2+dy
point icon,dx+dy,w/-2+dy
point iecc,dx,w/-2
!
! Post to Schottky Diode
level post
dx=2.5
dy=2.5
point ibccf,ctr-dx,dy
point icon,ctr+dx,dy
point icon,ctr+dx,-dy
point iecc,ctr-dx,-dy
!
! Schottky Diodes and Ground Plane
level schint
dx=0.5   ! center of Schottky stripe
dy=12 ! 8/2 from center line + 2 for spacing + 2 for ohmics
! diode stripe
point ibccf,ctr-dx,dy+ldi
point icon,ctr+dx,dy+ldi
point icon,ctr+dx,-dy-ldi
point iecc,ctr-dx,-dy-ldi
! 1 x 3 cross post
point ibccf,ctr-1.5,0.5
point icon,ctr+1.5,0.5
point icon,ctr+1.5,-0.5
point iecc,ctr-1.5,-0.5
! upper ground plane
dx=4.5  ! spacing from center of Schottky to ohmic
point ibccf,0,gap
point icon,0,(gap+g)
point icon,lli,(gap+g)
point icon,lli,(gap)
```

```
point icon,ctr+dx+4,(gap)
point icon,ctr+dx+4,(dy+ldi+8)
point icon,ctr-dx-4,(dy+ldi+8)
point iecc,ctr-dx-4,(gap)
!lower ground plane
point ibccf,0,-gap
point icon,0,-(gap+g)
point icon,lli,-(gap+g)
point icon,lli,-(gap)
point icon,ctr+dx+4,-(gap)
point icon,ctr+dx+4,-(dy+ldi+8)
point icon,ctr-dx-4,-(dy+ldi+8)
point iecc,ctr-dx-4,-(gap)
!
! Ohmics
level ohmic
dx=4.5  ! center of Schottky stripe to ohmic
dy=8  ! edge of ohmic: 8/2 + 2um space
! upper ohmic
point ibccf,ctr-dx,(dy)
point icon,ctr-dx-8,(dy)
point icon,ctr-dx-8,(dy+ldi+18)
point icon,ctr+dx+8,(dy+ldi+18)
point icon,ctr+dx+8,(dy)
point icon,ctr+dx,(dy)
point icon,ctr+dx,(dy+ldi+8)
point iecc,ctr-dx,(dy+ldi+8)
!lower ohmic
point ibccf,ctr-dx,-(dy)
point icon,ctr-dx-8,-(dy)
point icon,ctr-dx-8,-(dy+ldi+18)
point icon,ctr+dx+8,-(dy+ldi+18)
point icon,ctr+dx+8,-(dy)
point icon,ctr+dx,-(dy)
point icon,ctr+dx,-(dy+ldi+8)
point iecc,ctr-dx,-(dy+ldi+8)
! ground straps
point ibccf,ctr+dx+8,dy
```

```
point icon,ctr+dx+6,dy
point icon,ctr+dx+6,-dy
point iecc,ctr+dx+8,-dy
!
level isolation
dy=12 ! 8/2 + 2 spacing + 2 ohmics
point ibccf,ctr-17,dy
point icon,ctr-17,(dy+ldi+12)
point icon,ctr+17,(dy+ldi+12)
point iecc,ctr+17,dy
!
point ibccf,ctr-17,-dy
point icon,ctr-17,-(dy+ldi+12)
point icon,ctr+17,-(dy+ldi+12)
point iecc,ctr+17,-dy
!
end define
!
!-------------------------------------------------------------------------
!
! Line Layout Program for MACRO "NLTLC"
! Air bridged center conductor, center diodes, 1um Schottky fingers
! Written by Scott Allen 10/93
!
defelem "NLTLC",2,"w","gap","adi","lli"
real w,gap,adi,lli,ldi,ctr,dx,dy,g
lli=int(0.5+lli)
w=int(0.5+w)
lam=int(0.5+lam)
ldi=0.5*int(0.5+adi)
! Find center of the line section:
ctr=0.5*lli
g=2*(w+2*gap)
!
! Air Bridged Center Conductor
level ab
dy=(w-9)/2
dx=ctr-ldi-2-dy
```

```
point ibccf,0,w/-2
node n1,0,0
point icon,0,w/2
point icon,lli,w/2
node n2,lli,0
point iecc,lli,w/-2
!
! Post to Schottky Diode
level post
dx=3.5
dy=2.5
point ibccf,ctr-dx,dy
point icon,ctr+dx,dy
point icon,ctr+dx,-dy
point iecc,ctr-dx,-dy
!
! Schottky Diodes and Ground Plane
level schint
dy=.5
! diode stripe
point ibccf,ctr-ldi,dy
point icon,ctr+ldi,dy
point icon,ctr+ldi,-dy
point iecc,ctr-ldi,-dy
! upper ground plane
dx=3   ! center of Schottky to ohmic
point ibccf,0,gap
point icon,0,(gap+g)
point icon,lli,(gap+g)
point iecc,lli,(gap)
!lower ground plane
point ibccf,0,-gap
point icon,0,-(gap+g)
point icon,lli,-(gap+g)
point iecc,lli,-(gap)
! Extra metal on ohmic pads
dy=4.5
point ibccf,ctr-ldi,dy
```

```
point icon,ctr-ldi,gap
point icon,ctr+ldi,gap
point iecc,ctr+ldi,dy
!
point ibccf,ctr-ldi,-dy
point icon,ctr-ldi,-gap
point icon,ctr+ldi,-gap
point iecc,ctr+ldi,-dy
!
! Ohmics
level ohmic
dx=2
dy=2.5
! upper ohmic
point ibccf,ctr-ldi-dx,(dy)
point icon,ctr-ldi-dx,(gap+6)
point icon,ctr+ldi+dx,(gap+6)
point iecc,ctr+ldi+dx,(dy)
!lower ohmic
point ibccf,ctr-ldi-dx,-(dy)
point icon,ctr-ldi-dx,-(gap+6)
point icon,ctr+ldi+dx,-(gap+6)
point iecc,ctr+ldi+dx,-(dy)
!
level isolation
dx=4
point ibccf,ctr-ldi-dx,gap+4
point icon,ctr+ldi+dx,gap+4
point icon,ctr+ldi+dx,-gap-4
point iecc,ctr-ldi-dx,-gap-4
!
end define
!-------------------------------------------------------------------------
! Line layout for center conductor didoes in normal Schottky metal
!    Written by Mike Case 7/92
!
defelem "NLTLD",2,"z","w","adi","lli","lam","lams","lamo"
real z,x,y,w,adi,lli,b,g,ldi,lam,ctr,lams,lamo
```

```
lli=0.5*int(0.5+2*lli)
w=int(0.5+w)
lam=int(0.5+lam)
lams=int(0.5+lams)
lamo=int(0.5+lamo)
ldi=int(0.5+adi/lams)
ctr=0.5*int(0.5+lli)
! Check it out
if w < lams then
     w=lams
end if
! Find gap
x=sqr(1-((0.5*exp(z/11.33893419)-1)/(0.5*exp(z/11.33893419)+1))^4)
! X=w/(w+2b)
y=(1-x)/(2*x)
b=0.5*int(0.5+2*y*w)
! Find ground width
g=2*int(0.5+w/x)
level schint
! Center
if w = lams then
     point ibccf,0,w/-2
     node n1,0,0
     point icon,0,w/2
     point icon,lli,w/2
     node n2,lli,0
     point iecc,lli,w/-2
else
     point ibccf,0,w/-2
     node n1,0,0
     point icon,0,w/2
     point icon,ctr-ldi/2-2*lam,w/2
     point icon,ctr-ldi/2-2*lam,lams/2
     point icon,ctr+ldi/2+2*lam,lams/2
     point icon,ctr+ldi/2+2*lam,w/2
     point icon,lli,w/2
     node n2,lli,0
     point icon,lli,w/-2
```

```
     point icon,ctr+ldi/2+2*lam,w/-2
     point icon,ctr+ldi/2+2*lam,lams/-2
     point icon,ctr-ldi/2-2*lam,lams/-2
     point iecc,ctr-ldi/2-2*lam,w/-2
end if
! Upper ground
point ibccf,0,w/2+b
point icon,0,w/2+b+g
point icon,lli,w/2+b+g
point icon,lli,w/2+b
point icon,ctr+ldi/2,w/2+b
point icon,ctr+ldi/2,lams/2+lamo+lam
point icon,ctr-ldi/2,lams/2+lamo+lam
point iecc,ctr-ldi/2,w/2+b
! Lower ground
point ibccf,0,-1*(w/2+b)
point icon,0,-1*(w/2+b+g)
point icon,lli,-1*(w/2+b+g)
point icon,lli,-1*(w/2+b)
point icon,ctr+ldi/2,-1*(w/2+b)
point icon,ctr+ldi/2,-1*(lams/2+lamo+lam)
point icon,ctr-ldi/2,-1*(lams/2+lamo+lam)
point iecc,ctr-ldi/2,-1*(w/2+b)
! Now ohmics
level ohmic
! Upper
point ibccf,ctr-ldi/2-lam,lams/2+lamo
point icon,ctr-ldi/2-lam,w/2+b+lam
point icon,ctr+ldi/2+lam,w/2+b+lam
point iecc,ctr+ldi/2+lam,lams/2+lamo
! Lower
point ibccf,ctr-ldi/2-lam,-1*(lams/2+lamo)
point icon,ctr-ldi/2-lam,-1*(w/2+b+lam)
point icon,ctr+ldi/2+lam,-1*(w/2+b+lam)
point iecc,ctr+ldi/2+lam,-1*(lams/2+lamo)
! finally, the ion implant
level isolation
if ldi < 8 then
```

```
        point ibccf,ctr-4,-1*(w/2+b+8*lam)
        point icon,ctr-4,-1*(w/2+b+2*lam)
        point icon,ctr-ldi/2,-1*(w/2+b+2*lam)
        point icon,ctr-ldi/2,w/2+b+2*lam
        point icon,ctr-4,w/2+b+2*lam
        point icon,ctr-4,w/2+b+8*lam
        point icon,ctr+4,w/2+b+8*lam
        point icon,ctr+4,w/2+b+2*lam
        point icon,ctr+ldi/2,w/2+b+2*lam
        point icon,ctr+ldi/2,-1*(w/2+b+2*lam)
        point icon,ctr+4,-1*(w/2+b+2*lam)
        point iecc,ctr+4,-1*(w/2+b+8*lam)
else
        point ibccf,ctr-ldi/2,-1*(w/2+b+2*lam)
        point icon,ctr-ldi/2,w/2+b+2*lam
        point icon,ctr+ldi/2,w/2+b+2*lam
        point iecc,ctr+ldi/2,-1*(w/2+b+2*lam)
end if
end define
```

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