University of California

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Transferred Substrate Heterojunction Bipolar Transistors

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of the requirements for the degree of
Doctor of Philisophy
in
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by
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Abstract

Transferred Substrate
Heterojunction Bipolar Transistors

by
Uddalak Bhattacharya

Transferred substrate heterojunction bipolar transistors (HBTs) have been fabricated in the InAlAs/InGaAs material system. The substrate transfer process is the key fabrication step which distinguishes the transferred substrate HBT from the more typical double mesa HBT. The process of substrate transfer allows access to both the emitter and the collector sides of the transistor epitaxial film. Lithographically defined emitter and collector contacts having narrow widths and aligned to each other are possible due to the substrate transfer process. The collector width is independent of the width of the base mesa. The emitter and the collector can be scaled in proportion to deep submicron dimensions. As a result, the collector-base capacitance is greatly reduced. Scaling the collector leads to a large decrease in the collector-base resistance-capacitance time-constant and a consequent large increase in the power gain cutoff frequencies (f_{max}) of transferred substrate HBTs. Demonstration devices with emitter widths of 1 μm show encouraging performance in terms of f_{max}. The maximum value of f_{max} obtained in this thesis work is 170 GHz.

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Chapter 1

Introduction

Heterojunction bipolar transistors (HBTs) have high transconductance, extremely reproducible DC parameters and wide bandwidth. These attributes make HBTs the device of choice for many precision high speed circuits. Important HBT applications include analog-to-digital conversion, fiber-optic transmission, and microwave frequency synthesis. These are all medium-scale integrated circuits operating at frequencies of several tens of GHz and incorporating both precision broadband analog and very high clock-rate digital subcircuits.

High electron mobility transistors (HEMTs) with short gate lengths (~ 0.1 μm) are presently the largest bandwidth three terminal devices. HEMTs with a power gain cutoff frequency (f_{max}) of 450 GHz have been reported in [1]. The superior bandwidths of HEMTs is a result of the rapid improvement in HEMT bandwidth with deep submicron scaling.

Reducing the lithographic dimensions and/or the semiconductor layer thicknesses of a device is termed device scaling. Scaling pertinent device dimensions is central to high frequency semiconductor device design. With several important semiconductor devices, the device bandwidth increases as critical lithographic dimensions and layer thicknesses are reduced. Examples of highly scaled devices with large bandwidths are 0.1 μm gate length high electron mobility transistors (HEMTs), 0.25 μm gate length complementary metal-oxide-semiconductor (CMOS) transistors, 0.1 μm Schottky-collector resonant tunnel diodes (SRTDs) and submicron Schottky diodes used as submillimeter wave mixers.

It is remarkable that scaling emitter dimensions below $\sim$1 μm does not improve the device bandwidth of HBTs significantly. Consequently, HBTs are not fabricated with deep submicron dimensions except where bias currents have to

be limited for low power operation. A device with smaller emitter width does not generally have a higher bandwidth.

In lateral transport devices such as MESFETs and HEMTs, device scaling is achieved by shortening the gate length. Both transit times and device parasitics are improved. Therefore, a larger bandwidth results due to scaling.

Vertical transport devices in general require both vertical scaling of the semiconductor layers and lateral scaling of the contact structures to obtain large device bandwidths. The Schottky diode serves as a concise example (figure 1.1). Carrier transit time through the depletion region of a Schottky diode is proportional to the thickness of the region. Consequently, the bandwidth of a Schottky diode having a thick depletion region is limited by carrier transit time. Vertical scaling of the depletion region will reduce carrier transit time. Advanced epitaxial growth techniques such as molecular beam epitaxy (MBE) can be used to obtain very thin semiconductor layers that are then required.

Although transit time can be reduced by scaling the depletion layer thickness, the device capacitance increases. Given a fixed series resistance, extreme vertical scaling of the Schottky diode will result in a device whose bandwidth is limited by the resistance-capacitance (RC) time-constant.

Lateral scaling can be used in such a situation to lower the RC time-constants. A Schottky contact with a narrower width will have a lower capacitance, a lower spreading resistance, and an unchanged ohmic contact resistance (figure 1.1). The RC time-constant is thus reduced.

In vertical devices, the device capacitance is proportional to the device area, and the resistance inversely proportional to the device periphery. Consequently, transit times are reduced by thinning the semiconductor layers and RC time-constants decreased by decreasing the lithographic dimensions.

Advanced lithographic techniques like electron-beam lithography can be used to fabricate small area contacts with a large periphery-to-area ratio. Optimum bandwidth for the Schottky diodes is obtained when the carrier transit time is equal to the RC time-constant of the device.

We have described above the scaling principles for the Schottky diode. There are vertical transport devices like resonant tunnel diodes (RTDs) and HBTs where the method of application of lateral scaling is not as straightforward. The geometry of a RTD is similar to the Schottky diode except that the top contact is an ohmic contact having the same size as the device mesa. Like a Schottky diode, transit time through the space-charge regions of a RTD can be reduced by thinning down the pertinent layers. Resistance due to the bottom ohmic contact

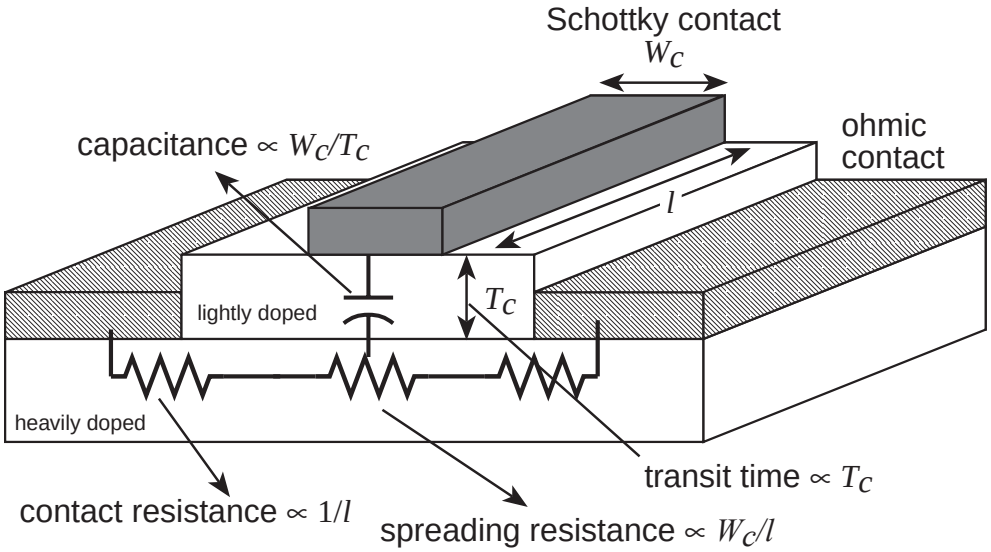


Figure 1.1: Scaling a Schottky diode

can be reduced by having a device mesa with a large periphery-to-area ratio.

Yet, in the RTD, there is one RC time-constant which does not scale. The top ohmic contact resistance is inversely proportional to the contact area. The device capacitance is proportional to the contact area. The product, therefore, is independent of scaling. In an otherwise optimized device, this RC time-constant becomes dominant and further scaling does not improve device bandwidth.

We can render the device scalable by a small structural change. If the top ohmic contact is replaced by a Schottky contact [2], then scaling principles similar to a Schottky diode can be applied. In the modified RTD, there is no contact resistance due to the top Schottky contact. The remaining RC charging time-constants behave as those of the Schottky diode. Bandwidth of Schottky-collector RTDs then consequently increase when the top Schottky contact is scaled in area. Schottky contacts defined by electron-beam lithography can achieve periphery-to-area ratios far superior than device mesas defined by etching processes. The combined effect makes the Schottky collector RTD (SRTD) a highly scalable device. SRTDs having 0.1 μm width Schottky contacts with significantly improved device bandwidth (f_{max}) of 2200 GHz (estimated) has been reported in [3]. A similarly scaled normal RTD would have an f_{max} of 800 GHz.

With HBTs one has to go a step further. Like most other vertical devices HBT bandwidth is determined by a combination of a transit time and an RC

charging time. The RC charging times again are controlled by lateral dimensions. Lateral scaling in HBTs requires narrow emitter and collector contacts with large periphery-to-area ratios. The emitter and collector contacts must also be aligned to each other. The width of the emitter and collector contacts should be approximately the same and independent of the width of the base mesa. Scaling the emitter and collector widths of this structure increases the device bandwidth significantly.

Such scaling is the subject of this thesis. A cross-section of a scalable HBT with the above mentioned features and a Schottky collector contact is shown in figure 1.2. As will be discussed in chapter 2, an ohmic collector transferred substrate HBT will also be a scalable device. The Schottky collector provides additional advantages of zero collector contact resistance and ease of fabrication for deep submicron dimension contacts.

For extreme lateral scaling using the full power of the lithographic tools for the definition of the collector and emitter, it is necessary to gain access to both sides of the epitaxial structure. Therefore, a process of substrate transfer has to be followed. This is the key process step which distinguishes the transferred substrate HBT from the more typical double mesa HBT. The substrate transfer process makes it possible to realize the geometry of figure 1.2. In this thesis, initial work on transferred substrate HBTs with Schottky collector contacts is reported and analyzed. Devices with emitter widths of 1 μm have been fabricated which show encouraging performance in terms of device bandwidth f_{max}. Subsequent to the work of this thesis, continued development of the device has lead to record values of f_{max} for an HBT.

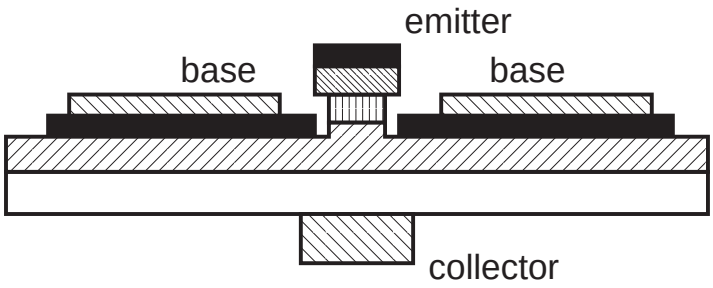


Figure 1.2: Cross-section of a transferred substrate HBT

Chapter 2

High speed InP HBTs

The design of high speed HBTs will be discussed in this chapter with emphasis on HBTs which may be grown on a InP substrate. The focus of this dissertation is the application of lateral scaling to HBTs for the purpose of improvement in device bandwidth. The scaling laws that are applicable to transferred substrate HBTs will be discussed in detail. These laws relate the device power gain cutoff frequency (f_{max}) of transferred substrate HBTs to the pertinent device dimensions. In addition, other design issues including transit times, base resistance, collector-base capacitance, base pushout threshold current, collector breakdown, and current gain (β) degradation with emitter scaling will be discussed. The discussion will be in the form of brief reviews of published work. Lateral scaling of HBTs can thus be placed in context of the bigger goal of fabricating a high performance HBT. It is expected that the transferred substrate HBT will incorporate all the advances in HBT technology with the added advantage of its scalability.

2.1 Transferred substrate HBT

The cross-section of a transferred substrate HBT is shown in figure 1.2. Transferred substrate HBTs have lithographically defined, narrow emitter and collector contacts aligned to each other. This is the special feature of the transferred substrate HBT in contrast to the double mesa HBT. The fabrication of transferred substrate HBTs requires access to the emitter and the collector sides of the epitaxial film. The process of substrate transfer allows this access and is an essential step in the fabrication process. With the structure of the transferred

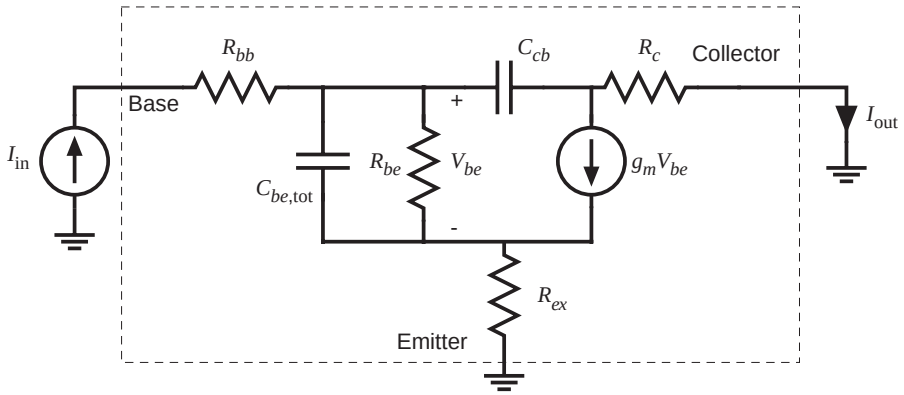


Figure 2.1: Hybrid-π model for an HBT showing schematically the configuration for calculating short circuit current gain.

substrate HBT, it is possible to scale both the emitter and the collector contacts to deep submicron dimensions. The scaling reduces the base-resistance-collector-base-capacitance time-constant and increases the power gain cutoff frequency f_{max} significantly.

2.1.1 Scaling law

A simple hybrid-π model of a HBT is shown in figure 2.1 with the model components related to the device parameters and biasing conditions. The expression for short circuit current gain corresponding to this device model is

$$A_I = \frac{-\beta}{1 + j\omega\beta\left[(1/g_m)\left(C_{be,\mathrm{tot}} + C_{cb}\right) + (R_{ex} + R_c)C_{cb}\right]} \tag{2.1}$$

under the following conditions: DC short circuit current gain $\beta \gg 1$, $\omega C_{cb} \ll g_m/(1 + g_m R_{ex})$, and only first order terms in angular frequency ω considered.

The short circuit current gain cutoff frequency f_τ corresponds to the frequency at which the magnitude of A_I is unity. Near this frequency, the imaginary part of the denominator in (2.1) is much larger than unity. The expression

for f_τ as a function of device parameters and biasing conditions is therefore approximately

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{be} + C_{cb}) + (R_{ex} + R_c)C_{cb}. \tag{2.2}$$

Here τ_b is the base transit time, τ_c the collector transit time, kT/q the thermal voltage, I_c the collector current, C_{be} the base-emitter depletion capacitance, C_{bc} the collector-base capacitance, R_{ex} the emitter contact resistance, and R_c the collector contact resistance. If under scaling, the ratio between the emitter and the collector widths is maintained, the collector fringing capacitance is negligible, and the emitter current density is maintained at a fixed level, then each term in the above equation is independent of lateral scaling. The short circuit current gain cutoff frequency is therefore independent of scaling.

The power gain cutoff frequency f_{max} is another important figure-of-merit of high-frequency HBT performance. F_{max} not only depends on f_τ, but also on the base-resistance-collector-base-capacitance time constant as

$$f_{max} = \frac{1}{2}\sqrt{f_\tau f_{cb}} \tag{2.3}$$

where

$$f_{cb} = \frac{1}{2\pi R_{bb} C_{cb}}. \tag{2.4}$$

R_{bb} is the base resistance and C_{cb} is the collector-base capacitance. No matter how large the value of f_τ is, power gain is available only at frequencies below f_{max}. Hence, to improve device bandwidth, not only is it important to improve f_τ, but also f_{cb}. Scaling a transferred substrate HBT improves f_{cb} significantly.

The collector-base capacitance C_{cb} is proportional to the width of the collector W_c if fringing capacitance is negligible (figure 2.2); $C_{cb} = \epsilon l W_c / T_c$, where l is the length of the collector or the emitter stripe and T_c is the thickness of the collector depletion region. If a constant ratio is maintained between the emitter and the collector widths, C_{cb} is proportional to the emitter width W_e.

To determine f_{max}, we must next calculate the base resistance. The base resistance R_{bb} has three components. These are, the contact resistance from the base ohmic contact, the sheet resistance from the gap between the emitter mesa and the base ohmic contact, and the spreading resistance of the base layer underneath the emitter mesa. The contact resistance is equal to $\sqrt{\rho_{bc}\rho_{bs}}/2l$ where ρ_{bc} is the specific contact resistance per unit area of the metal-simiconductor

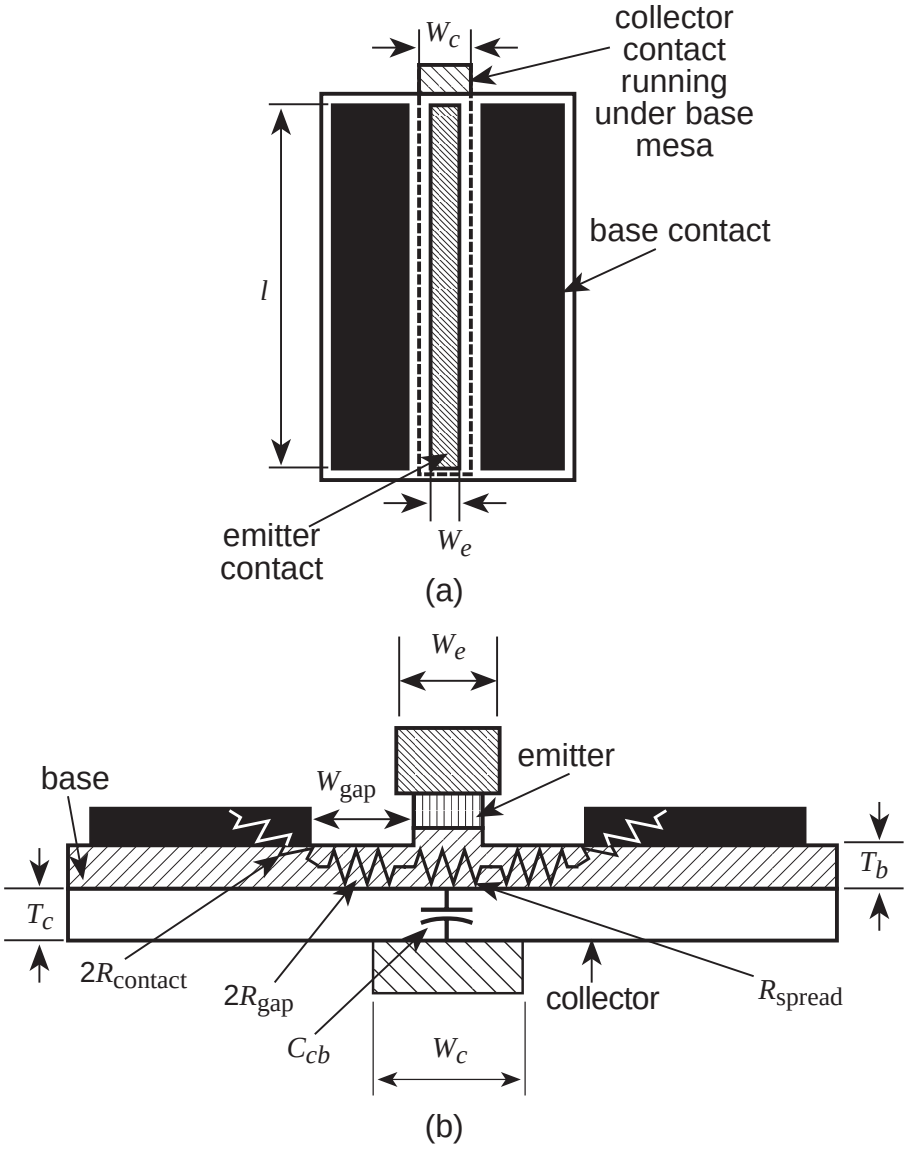


Figure 2.2: Transferred substrate HBT: (a) top view, (b) cross-section.

interface (units of Ω-cm^2), and ρ_{bs} is the base sheet resistivity (units of Ω/□). The gap resistance is given by $\rho_{bs}W_{\text{gap}}/2l$ where W_{gap} is the separation between the emitter mesa and the base ohmic contact. The spreading resistance is given by $\rho_{bs}W_e/12l$. For HBTs fabricated with a self aligned base-emitter process, W_{gap} $\simeq 0.1\mu$m and R_{gap} is negligible. We note also that R_{spread} is proportional to the emitter width W_e, but that R_{contact} is independent of W_e. Hence, for narrow-emitter devices, the base resistance is dominated by R_{contact} and is independent of W_e. The traditional "base spreading resistance" is not an appropriate description for the R_{bb} of a typical narrow emitter HBT.

Noting that $R_{bb} \simeq R_{\text{contact}} = \sqrt{\rho_{bc}\rho_{bs}}/2l$, and $C_{cb} = \epsilon l W_c/T_c$ (where $W_c \propto W_e$), the $R_{bb}C_{cb}$ time constant is proportional to W_e. This when used in (2.4) yields the relationship

$$f_{cb} \propto \frac{1}{W_e}. \tag{2.5}$$

Referring (2.5) back to (2.3), it is observed that the maximum frequency of oscillation f_{max} depends on W_e as

$$f_{max} \propto \frac{1}{\sqrt{W_e}}. \tag{2.6}$$

Device bandwidth increases as the inverse square root of the device minimum feature size. This is the scaling law for transferred substrate HBTs.

Let us now consider the f_{max} of a more standard HBT structure. The cross section of a double mesa HBT is shown in figure 2.3. Unlike the transferred substrate HBT, in a double mesa HBT, C_{cb} is proportional to the width of the base mesa which in turn is much wider than and independent of W_e. R_{bb}, as before, is independent of the emitter width for sufficiently narrow emitters. Therefore the $R_{bb}C_{cb}$ time constant is independent of W_e, and hence, so is f_{max}. Device bandwidth does not significantly improve as the emitter width is reduced. We note that the collector-base junction area of the double mesa HBT is further increased by the presence of a base contact pad area necessary to bring interconnect metalization onto the base ohmic metal.

A comparison of the improvement in f_{max} between a transferred substrate HBT and a double mesa HBT under scaling is shown in figure 2.4. It is observed that below emitter widths of ~ 1 μm, bandwidth of the transferred substrate HBT improves rapidly. In marked contrast, there is no significant improvement with scaling in the bandwidth of the double mesa HBT.

The projections of figure 2.4 were generated using the prior analysis. The expression for f_τ is evaluated assuming that the base and collector transit times are

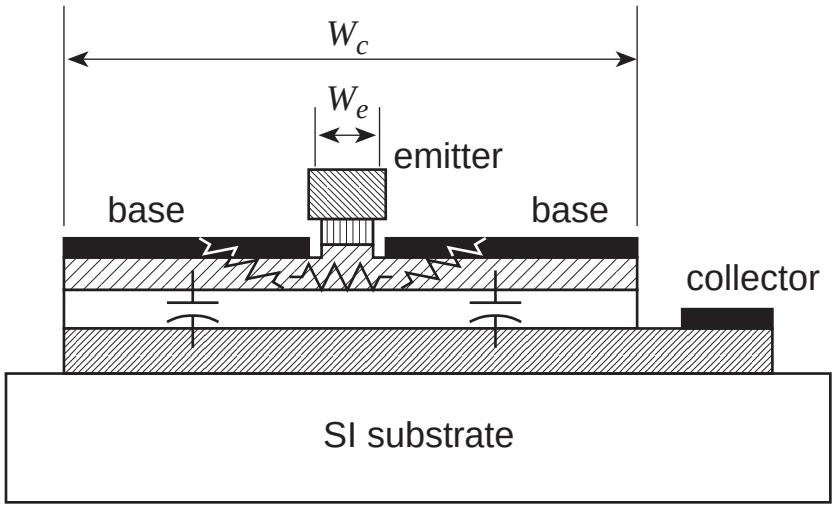


Figure 2.3: Cross-section of a double mesa HBT

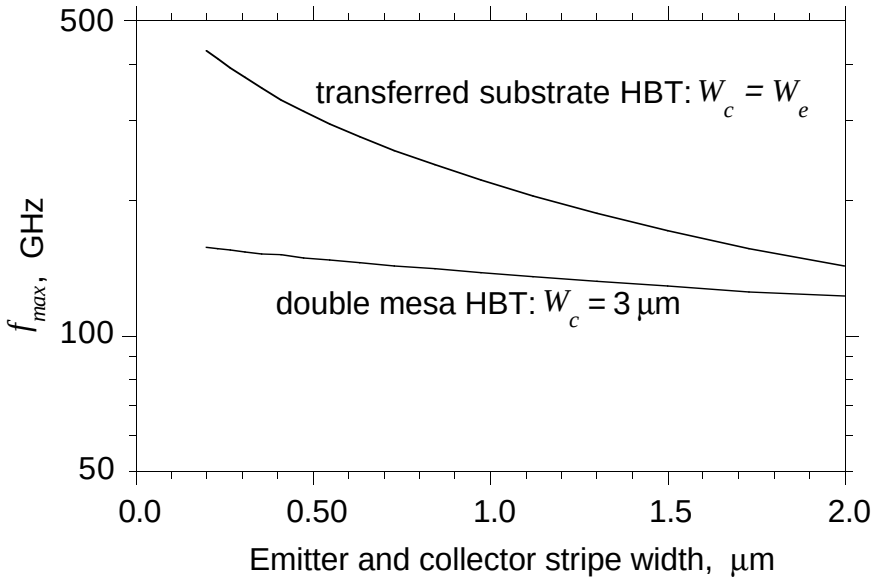


Figure 2.4: Comparison of the projected bandwidth of a transferred substrate HBT to a double mesa HBT

the only significant components. R_{bb} and C_{cb} are evaluated using experimentally obtained material parameters (from [4]) and the geometry of each HBT structure. The material parameters are as follows: 800 Å InGaAs base Be doped to $5 \times 10^{19}/\text{cm}^3$ with $\rho_{bs} = 500\Omega/\square$ and $\rho_{bc} = 7 \times 10^{-7}\Omega - \text{cm}^2$, 2700 Å InGaAs collector Si doped to $1 \times 10^{16}/\text{cm}^3$ (fully depleted), and $\tau_b + \tau_c = 1.32$ psec.

The parameters used above to compute the scaling properties of HBTs are representative of HBTs produced by industrial research laboratories in the early 1990's. There have been recent improvements in HBT material, particularly in improved ability to define and control base thicknesses below 500 Å, and in the resistivity of ohmic contacts. Grading the bandgap of the InGaAs base can substantially reduce the base transit time. For these reasons, the curves of figure 2.4 are now highly conservative for both double mesa and transferred substrate HBTs. InP/InGaAs double heterostructure bipolar transistors have been reported ([5]) with f_τ and f_{max} both over 220 GHz. Very recently, in a continuation beyond this thesis work on transferred substrate HBTs, B. Agarwal has obtained 277 GHz f_{max} in a transferred substrate device with a ~ 1.5 μm collector width. Figure 2.4 nevertheless remains a good guide of the relative performance obtainable with the two devices.

There is a secondary benefit in scaling Schottky collector transferred substrate HBTs over double mesa HBTs. The former shows improvement in f_τ due to lateral scaling. The expression (2.2) for f_τ maybe re-arranged as

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}C_{be} + \left(R_{ex} + R_c + \frac{kT}{qI_c}\right)C_{cb} \tag{2.7}$$

The Schottky collector eliminates the collector contact resistance R_c [3]. Further, C_{cb} is low for a highly scaled collector. This results in a moderate improvement in f_τ.

The scaling law of (2.6) suggests that the operating bandwidth of HBTs can be increased without bounds by lithographic scaling alone. In fact, to obtain usable devices, vertical scaling of the epitaxial layer thicknesses must accompany the lithographic scaling.

First, let us consider the transfer function of the collector-base junction:

$$I_c(j\omega) \sim \frac{\exp(-j\omega\tau_c)\sin(\omega\tau_c)}{\omega\tau_c} \simeq 1 - j\omega\tau_c + \text{O}(\omega^2\tau_c^2) \simeq 1 - j\omega\tau_c. \tag{2.8}$$

The latter approximation is necessary to develop the hybrid-π equivalent circuit model from which the expressions for f_τ and f_{max} are derived. If the collector is

sufficiently thick, and the device scaled to deep submicron dimensions, then the simplified expression for f_{max} may be such that $2\pi f_{max}\tau_c \sim 1$. The expressions for f_τ and f_{max} in this case are unreliable. But with a $T_c = 3000$ Å collector, $\tau_c \simeq 0.3$ psec, the approximation for the collector transit time is reliable for frequencies exceeding 500 GHz.

A more serious consideration is the question of the utility of a device with $f_\tau \ll f_{max}$. Only in the cases of oscillators and narrowband reactively matched amplifiers is f_{max} the single determinant of transistor performance in the circuit. In general transistor circuits, all the transistor parasitics will have some impact, and the combination of f_τ and f_{max} as figures-of-merit provide a useful first indication of potential device performance in the circuit. Devices with $f_{max} \ll f_\tau$, obtained by thinning the epitaxial layers *without* lateral lithographic scaling will show circuit bandwidth determined by R_{bb} and C_{cb}. Devices with $f_{max} \gg f_\tau$ (e.g. devices with relatively thick epitaxial layers and significant lateral lithographic scaling) will show circuit bandwidth dominated by $(\tau_b + \tau_c)$. Reduction of $(\tau_b + \tau_c)$ is obtained by thinning the epitaxial layers, which unfortunately increases $R_{bb}C_{cb}$. The transferred substrate HBT allows for the subsequent reduction of $R_{bb}C_{cb}$. A device having high values for *both* f_τ and f_{max} is thus possible.

The cross-section of the transferred substrate HBT in figure 2.2 shows a direct Schottky contact to the collector depletion layer. An ohmic collector contact having the same width as the Schottky contact will also scale the device in the same way. A transferred substrate HBT with an Ohmic collector contact is shown in figure 2.5. It is observed that the band structure of the two devices are almost identical except for an extra potential drop across the collector-base junction of the Schottky-collector device. This potential drop, due to the Schottky contact, is the difference between the work function of the metal Schottky contact and the electron affinity of the collector semiconductor. A Schottky collector contact improves f_τ because of the absence of a collector contact resistance (expression (2.7)). It is also easier to fabricate deep submicron Schottky collector contacts (e.g. 0.1 μm T-gate) than deep submicron Ohmic contacts.

Several approaches have been reported for reducing the collector-base capacitance of HBTs, and thereby improving f_{max}. One approach is the reduction of the width of the base mesa [5]. This relies on improvements in base contact technology because a narrow base mesa results in a smaller base ohmic contact area. The base contact width must be at least one transfer length if the contact resistance is to be kept small. In contrast, the transferred substrate technique

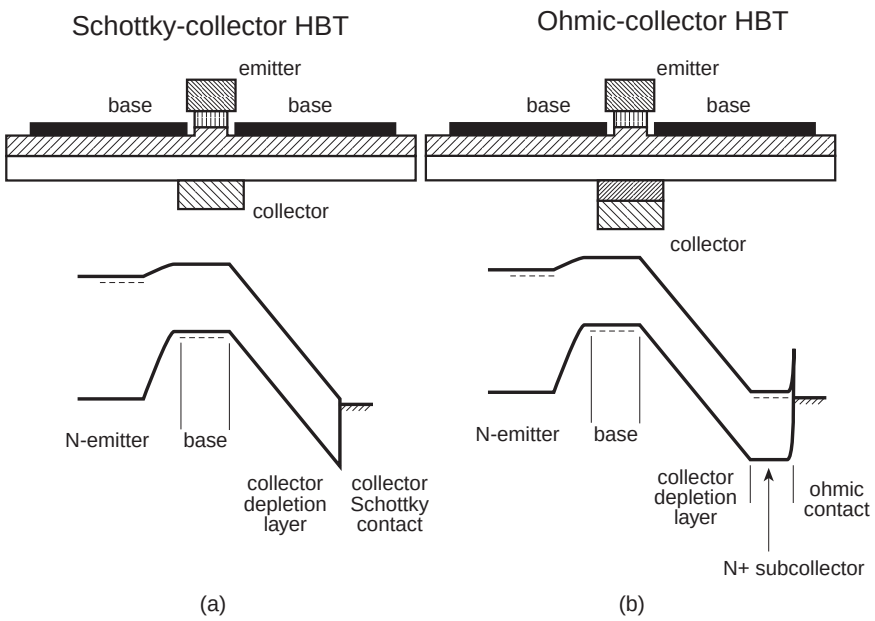


Figure 2.5: Transferred substrate HBTs: (a) Schottky collector, (b) Ohmic collector.

provides independent control of the base and collector contact widths. There has been other approaches to make the collector contact width independent of the size of the base mesa, such as selective etching to undercut the collector [6], collector isolation implant [7], and selective lateral oxidation of the emitter [8] for a collector up growth. However, for deep submicron scaling, powerful fine line lithography is likely to be the technique of choice for defining the collector and emitter contacts of HBTs.

2.2 Base resistance

While scaling provides a means of increasing device bandwidth with a given technology, device bandwidth is also heavily dependent upon base contact technology. A thick, heavily doped base layer is required for low base resistance. A thick base layer minimizes the sheet resistance ρ_{bs} and hence reduces the contact resistance $\sqrt{\rho_{bc}\rho_{bs}}/2l$. A thin, lightly doped base layer is required for low base transit time. These two seemingly conflicting requirements may be simultaneously satisfied if the portion of the base under the emitter - the intrinsic base - is made thin and only moderately doped while the region of the base below its ohmic contact - the extrinsic base - is made thick and is doped very heavily. Making the intrinsic base thin increases the spreading resistance component of the base resistance, but this spreading component is also reduced rapidly as the emitter stripe width is decreased.

The idea of having an extrinsic base which is not only heavily doped but also with a wider bandgap than the intrinsic base was proposed in [9]. HBTs with similar structure have been reported [10], where the extrinsic base has been regrown after the fabrication of the emitter mesa. Very low values of specific contact resistance ($\rho_{bc} = 5 \times 10^{-8}$ Ω-cm^2) was reported for the extrinsic base. More significantly, the specific contact resistance at the regrown interface was reported to be a low 7×10^{-8} Ω-cm^2. There was no significant difference in the interface contact resistance between a regrown homojunction and a regrown heterojunction.

The conduction band bending at the interface (figure 2.6) both due to the doping gradient and the heterojunction will help confine the electrons injected from the emitter to within the intrinsic base. This was pointed out in [9]. HBT DC current gain improves because electron recombination at the base ohmic contact and the exposed base surface reduces.

The redistribution of p-dopants in the intrinsic base during high temperature

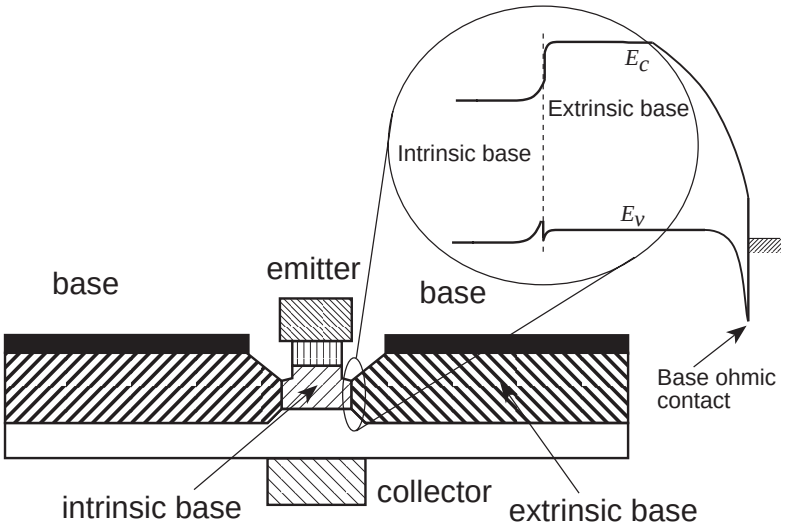


Figure 2.6: Possible transferred substrate HBT with a regrown extrinsic base.

regrowth is a concern. With a sufficiently low doping in the intrinsic base, [10] reports good performance of HBTs fabricated with regrown extrinsic base.

Other approaches of defining the extrinsic base include acceptor implantation coupled with rapid thermal annealing [11], diffusion of p-dopants [12], and appropriate graded gap contact structures using MBE regrowth [13]. We anticipate that these refinements to the base contact structure will be incorporated in the future work on the transferred substrate HBT. A possible transferred substrate HBT with a regrown base is shown in figure 2.6. There is an abrupt heterojunction between the narrow bandgap intrinsic base and the wide bandgap extrinsic base which is again graded back to a narrow bandgap material under the base ohmic contact.

2.3 Collector-base capacitance

Collector-base capacitance in transferred substrate HBTs is small because of the highly scaled collector. To obtain the maximum advantage of scaling, certain issues should be addressed. Fringing capacitance due to the fringing fields around the collector contact needs to be considered when the collector contact width becomes comparable to the collector thickness.

We can evaluate the effect of these fringing fields through reference to an

analogous problem. The collector-base structure of a transferred substrate HBT is similar to a microstrip transmission line, with the base layer corresponding to the microstrip ground plane and the collector contact to the microstrip signal line. The collector semiconductor is the substrate for this microstrip structure. Using a commercial microwave circuit design software in which the capacitance per unit length of microstrip lines are tabulated, it has been found that the fringing field spreads by an amount approximately equal to the separation between the signal line and the ground plane if the dielectric constant of the substrate is large compared to the dielectric constant of the environment in which the structure is located. Fringing electric field in the collector-base junction is illustrated in figure 2.7(a).

Using this model, the collector-base capacitance is related to W_c and T_c as follows.

$$C_{cb} \propto \frac{W_c + T_c}{T_c} = 1 + \frac{W_c}{T_c} \tag{2.9}$$

When the collector width is reduced to the collector space-charge-layer thickness, further reduction in W_c leads to minimal improvements in C_{cb} and f_{max}. To circumvent the scaling limits imposed by these fringing fields, we eliminate them. The high-dielectric-constant semiconductor surrounding the collector contact is removed by a simple self-aligned etch (figure 2.7(b)), and $C_{cb} = \epsilon l W_c/T_c$ is now proportional to the collector linewidth W_c. The full advantage of scaling can now be realized.

If collector material is not removed around the collector contact, then any undepleted collector material adjacent to the collector contact is a cause for serious concern. The entire undepleted region will act as the collector electrode and contribute to the collector-base capacitance in a situation similar to a double mesa HBT. If a transferred substrate HBT is designed to have an undepleted collector layer under some bias conditions, then it should be etched away in the areas surrounding the collector contact to the depth of the depleted portion of the collector. In figure 2.5 the ohmic collector transferred substrate HBT has the subcollector confined within the extent of the collector contact. Any undepleted region should be similarly treated.

Base pushout under high-current operation increases the collector-base capacitance. The increase in capacitance has been analytically estimated in [14]. Measurements on transferred substrate HBTs, reported in chapter 4, also show this effect. The reduction in f_{max} due to increased C_{cb} is quite rapid compared to the reduction in f_τ due to increased base transit time.

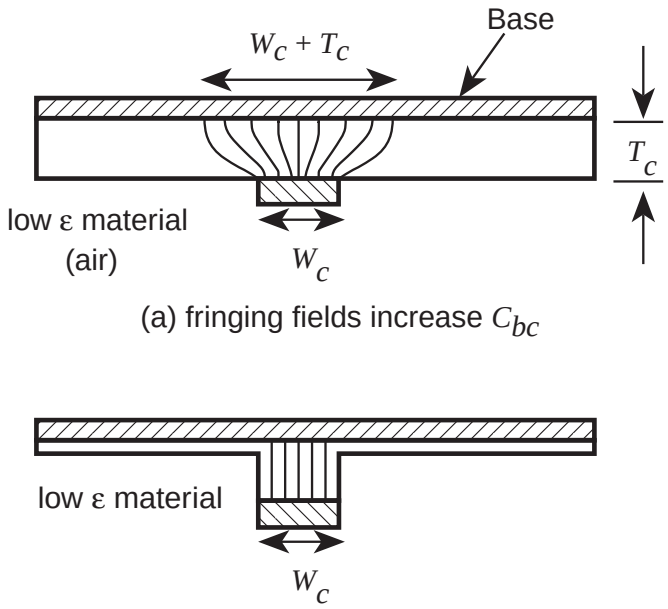


Figure 2.7: Effect of fringing fields on collector-base capacitance.

2.4 Carrier transit times

Base and collector transit times, although not significantly affected by the scaling of the lateral device dimensions, are important in determining the high frequency performance of HBTs. It is necessary to incorporate improved base and collector material structures which reduce transit times in the design of any large bandwidth HBT. It is anticipated that this will be done with the future work on the transferred substrate HBT.

2.4.1 Base transit time

A thin and lightly doped base will in general reduce the base transit time. What remains to be designed is the base-emitter heterojunction and the nature of the semiconductor in the base.

The base-emitter heterojunction can be abrupt, partially graded, or fully graded. The tradeoff between a fully graded and an abrupt junction has been discussed in [9]. While a fully graded heterojunction significantly improves the emitter injection ratio of a bipolar over that of an abrupt heterojunction, the conduction band discontinuity of the latter provides a launching ramp for electrons into the base with a large kinetic energy and potentially obtain high velocities during base transit. A compromise between these two beneficial effects may be obtained by partially grading the base-emitter heterojunction so that the launching ramp exists in a diminished form while the bandgap energy difference available for hole blocking provides satisfactory values of current gain. It has been argued in [15] that this structure combined with a graded bandgap base is desirable because the quasi-electric field due to bandgap grading in the base will aid electron transport in the base and the result will be an overall decrease in the base transit time. The band diagram of such a structure is illustrated in figure 2.8(a). The purpose of the small $\Delta\epsilon_c$ would be to bring the electrons to the high drift velocity instantaneously. Both the launching ramp $\Delta\epsilon_c$ and the total potential drop $\Delta\epsilon_b$ have to be kept small enough such that the electrons do not transfer to the higher potential energy, low mobility valleys due to the combined effect. It has also been argued in [15] that a small launching ramp with a graded base might be preferable to a large launching ramp uniform base device. This is because, in a heavily doped base with different scattering mechanisms, an electron injected with a very high kinetic energy may lose its energy very rapidly and traverse a greater proportion of the base with a low velocity.

A sloping conduction band limits the amount of kinetic energy loss at any point and provides a field that aids the electrons.

The above predictions have been validated by experimental evidence and Monte Carlo simulations [17]. Experiments with devices having the band structure of figure 2.8(b) have been reported in [17]. The conduction band discontinuity of the abrupt base-emitter heterojunction is varied by using emitters of different energy band gaps (alloy composition of $In_{0.52}(Ga_{1-x}Al_x)_{0.48}As$ is varied) . In this way electrons with different injection energies were injected into an uniform InGaAs base which was 500 Å thick and Be doped to $2 \times 10^{19}/cm^3$. Monte Carlo simulations of these structures yielded values of τ_b and τ_c which when summed were close to the experimentally obtained values of $(\tau_b + \tau_c)$. The base transit time, in the simulations decreased from ≈ 0.35 to 0.25 psec when the injection energy increased from 0.18 to 0.30 eV. The base transit time increased slightly for injection energies above 0.30 eV.

Results from Monte Carlo simulations on structures shown in figure 2.8(c) have been reported in [16]. Both the emitters and bases were composed of different alloy compositions of $In_{0.53}(Ga_{1-x}Al_x)_{0.47}As$. The base doping was fixed at $1 \times 10^{19}/cm^3$. A ΔE_T of 0.24 eV and a base thickness of 600 Å was considered. For the range $0.25 \leq \Delta E_B/\Delta E_T \leq 0.75$ (launcher with a graded base) the value of τ_b was a low 0.15 psec and varied only slightly. It increased sharply to more than 0.3 psec for $\Delta E_B/\Delta E_T = 0$ (launcher with uniform base) and to more than 0.2 psec for $\Delta E_B/\Delta E_T = 1$ (graded base with no launcher). The velocity profile also obtained from the same simulation shows a much larger average velocity in the base for the case where there is a graded base with a launcher than the other two extremes. Experiments with a similar band structure have been reported in [18]. HBTs with InP emitters and 650 Å thick bases Zn doped to $4 \times 10^{19}/cm^3$ were used. The base was a linear grade of the alloy $In_xGa_{1-x}As$ where x varied from 0.46 at the emitter-base junction to 0.53 at the collector-base junction. This yields a value of $\Delta E_B = 40$ meV. Measurements on such a HBT was conducted and compared to another with an uniform base and all other conditions remaining the same. The $(\tau_b + \tau_c)$ of the graded base HBT was smaller by 0.22 psec with the peak f_τ being approximately 180 GHz.

2.4.2 Collector transit time

Minimizing the collector transit time without a proportional increase in collector-base capacitance is possible if the overshoot velocity of the electrons entering

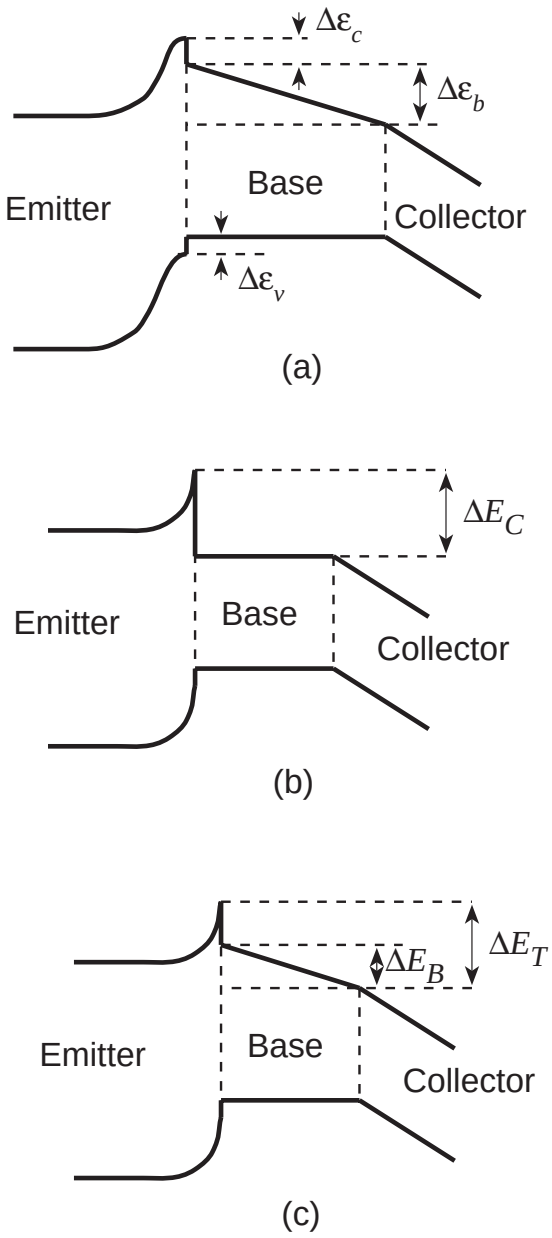


Figure 2.8: Base energy band structure design (a) after [15] (b) after [17] (c) after [16].

the collector from the base can be maintained over larger distances within the collector depletion region. This conclusion has been arrived at in [19] with a two-step velocity profile as shown in figure 2.9(a). A more general derivation illustrating this point follows.

An arbitrary velocity profile in the collector region is assumed as in figure 2.10(a). The collector region has a geometry similar to a parallel plate capacitor. As an electron traverses the collector drift region, displacement current will flow, as governed by Maxwell's relationships for the continuity of the total (transport + displacement) current. If an unit impulse of current (e.g. an unit quantity of charge) enters the collector at $t = 0$, some current $i_c(t)$ will flow in the collector contact. We refer to $i_c(t)$ as the impulse response of the collector space-charge region. The impulse response corresponding to the velocity profile of figure 2.10(a) is shown in figure 2.10(b). Since the electron position $x(t)$ within the collector varies with time, the current $i_c(t)$ can be written after a change of variables as $i_c(x)$. Maxwell's equations relate the displacement current to the velocity profile as

$$i_c(x) = \frac{v(x)}{T_c}, \tag{2.10}$$

where $v(x) = \partial x(t)/\partial t|_{\text{electrons}}$ is the electron velocity at a distance x away from the base edge and T_c is the thickness of the collector space charge region. To generate the impulse response shown in figure 2.10(b), the time required by the sheet of charge to move a distance x has to be calculated and this is given by

$$t(x) = \int_0^x \frac{dy}{v(y)}. \tag{2.11}$$

The current $i_c(t)$ as a function of time has the same profile of the velocity $v(t)$ as a function of time and $i_c(t)$ flows throughout the duration of the time of flight of the sheet of electrons, t_f.

The Fourier transform $I_c(j\omega)$ of the impulse response $i_c(t)$ is the system transfer function. To the first order in frequency, the system transfer function can be approximated as

$$I_c(j\omega) \triangleq \int_0^{t_f} i_c(t) \exp(-j\omega t) dt \simeq \int_0^{t_f} i_c(t)(1 - j\omega t) dt, \tag{2.12}$$

where ω is the angular frequency.

$$I_c(j\omega) \simeq \int_0^{t_f} i_c(t) dt - j\omega \int_0^{t_f} t i_c(t) dt$$

$$= \int_0^{t_f} i_c(t)dt \left[1 - j\omega \frac{\int_0^{t_f} t i_c(t)dt}{\int_0^{t_f} i_c(t)dt}\right] \tag{2.13}$$

Since $i_c(t)$ is a unit impulse of current and delivers a unit of charge,

$$I_c(j\omega) \simeq 1 - j\omega\tau_c \tag{2.14}$$

where the collector transit time τ_c is

$$\tau_c = \frac{\int_0^{t_f} t i_c(t)dt}{\int_0^{t_f} i_c(t)dt}. \tag{2.15}$$

We have just shown that the collector transit time τ_c is the centroid of the displacement current $i_c(t)$.

There is a substantial distinction between the collector transit time τ_c, which is the centroid of $i_c(t)$, and the electron time of flight t_f. The collector transit time is not equally sensitive to the electron velocity at all points within the collector. As an example, if the velocity profile of figure 2.9(a) is considered, the collector transit time is

$$\tau_{c,a} = \frac{1}{2} \cdot \left[\frac{T_o}{v_o} + \frac{T_s(T_o/v_o + T_s/v_s)}{T_o + T_s}\right]. \tag{2.16}$$

The same expression has been obtained in [19]. For the velocity profile in figure 2.9(b), the collector transit time is

$$\tau_{c,b} = \frac{1}{2} \cdot \left[\frac{T_s}{v_s} + \frac{T_o(T_s/v_s + T_o/v_o)}{T_s + T_o}\right]. \tag{2.17}$$

For $v_o/v_s = 8$ and $T_o/T_c = 0.5$, the ratio of the collector transit times for the two velocity profiles is $\tau_{c,a}/\tau_{c,b} = 0.44$, although the time of flight for the electrons through the collector space charge region is the same in both cases. The important physical conclusion we draw from this analysis: collector transit time is strongly dependent upon electron velocity entering the collector drift region and only moderately sensitive to the electron velocity leaving the region.

It has been mentioned in the previous subsection that non-equilibrium electron transport through the base is desirable for reduction in the base transit

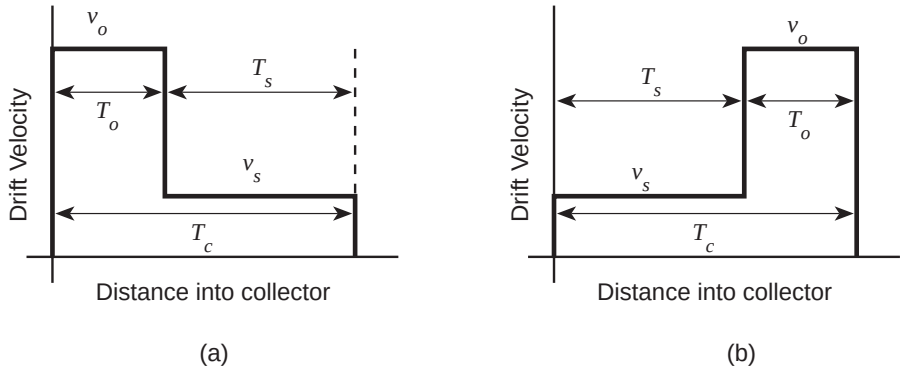


Figure 2.9: Drift velocity profiles in the collector.

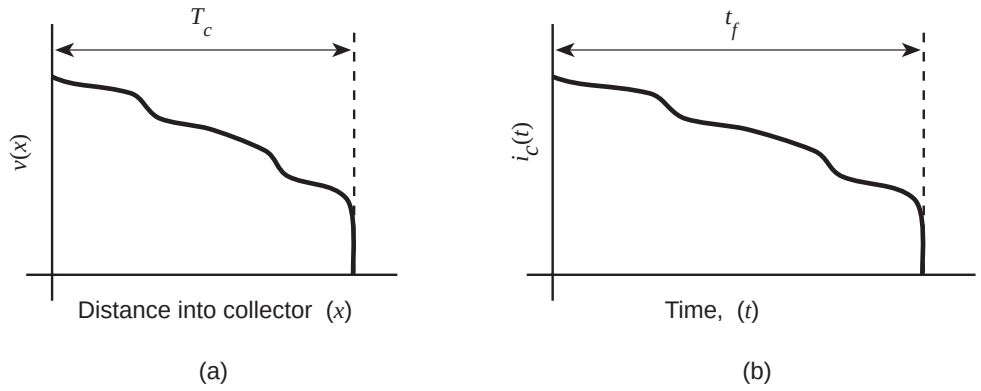


Figure 2.10: (a) Electron velocity in the collector as a function of position. (b) Impulse response of the system.

time. The base and collector transit times are not completely independent of each other because an electron exiting the base with sufficient kinetic energy can transfer easily to the higher energy valleys in the collector. It has been shown by Monte Carlo simulations and experiments in [16] and [17] that the injection conditions at the base-emitter junction and the thickness of the base influence both the base and the collector transit times. Even if the electrons do not transfer to the higher energy valleys in the base, they may do so readily in the collector if they did not get relaxed in the base. With base dopings of the order of $10^{19}/\text{cm}^3$, and base thicknesses below 1000 Å, the injection condition at the emitter-base junction influences the collector transit time. For a fixed base width, there is a minimum in $(\tau_b + \tau_c)$ for a particular injection condition. Base and collector design should therefore be done with an aim to minimize the sum of base and collector transit times. To obtain maximum advantage of non-equilibrium transport through the base and the collector, it is necessary to keep the electron kinetic energy within bounds at all times.

2.5 Base pushout

A large accumulation of space charge electrons in the collector depletion region, when comparable to the fixed positively charged donor concentration can lead to a large reduction in the collector electric field at the vicinity of the base junction. Under such a condition, the neutral base edge moves into the collector depletion region and the base width increases significantly compared to the designed value. The result is a large increase in both the total carrier transit time and the collector-base capacitance.

Base pushout should be avoided because it greatly degrades the high frequency performance of HBTs. Peak f_τ and f_{max} values are obtained at bias conditions where the low current impairments associated with the emitter charging time are of magnitude comparable to the high current impairments associated with base pushout (the Kirk effect). The Kirk effect threshold is therefore of major importance in determining peak device bandwidth.

It is observed that since $1/2\pi f_\tau = \tau_b + \tau_c + (kT/qI_c)C_{be}$, f_τ increases with increasing collector current densities. It is highly desirable that $(kT/qI_c)C_{be}$ be $\ll (\tau_b + \tau_c)$ at operating biases, but this requires currents that can easily be beyond the threshold of the Kirk effect. An HBT whose high frequency performance is limited by base pushout and not by transit times and resistance capacitance time-constants is not utilizing the full potential of the device.

The dependence of the base pushout threshold current density on collector parameters will be described in this paragraph. A collector structure with uniform bandgap, an uniform n-doping of N_d, and a thickness T_c is considered. On one end of the collector is a heavily p-doped base and on the other end is a heavily n-doped subcollector. Saturated velocity electron transport is assumed throughout the collector space charge region with a velocity v_{sat}. No lateral spreading of electrons in the collector is considered. The electric field in the collector space charge region with and without the presence of collector current is shown in figure 2.11. In the presence of electrons higher in density than the positively charged donor atoms, the slope of the electric field profile changes sign. With a sufficiently large number of electrons, the electric field at the edge of the base goes to zero. This is the threshold for base pushout and the current density corresponding to this condition is $J_{c,\max}$. The integral of the electric field vs. position ($\int_{\text{collector}} \mathcal{E}(x)dx$), e.g. the area under the electric field profile graphed in figure 2.11, is the sum of the applied collector-base voltage V_{cb} and the junction potential ϕ. Poisson's equation is applied to the net charge density ($J_{c,\max}/(qv_{\text{sat}}) - N_d$), to relate it to V_{cb} as

$$V_{cb} + \phi = \frac{q(J_{c,\max}/qv_{\text{sat}} - N_d)T_c^2}{2\epsilon}. \tag{2.18}$$

Re-arranging, the expression for $J_{c,\max}$ is

$$J_{c,\max} = \left(\frac{2\epsilon(V_{cb} + \phi)}{T_c^2} + qN_d\right) v_{\text{sat}}. \tag{2.19}$$

This derivation follows [20].

The threshold value of collector current for base pushout increases with the collector doping density, the electron velocity through the collector, and the applied collector-base voltage. The doping density in the collector should therefore be as high as possible. This conflicts with the requirements of maintaining a fixed depletion depth at a particular bias condition and of a low electric field in the collector. The collector-base voltage is limited by device breakdown and design for the highest breakdown voltage for the material system should be made without sacrificing transit times. Improving carrier velocity through the collector depletion region improves the current threshold for base pushout. It has been experimentally shown in [17] that devices which show larger collector transit times, also show Kirk effect (base pushout leading to reduced f_τ) at lower collector current densities.

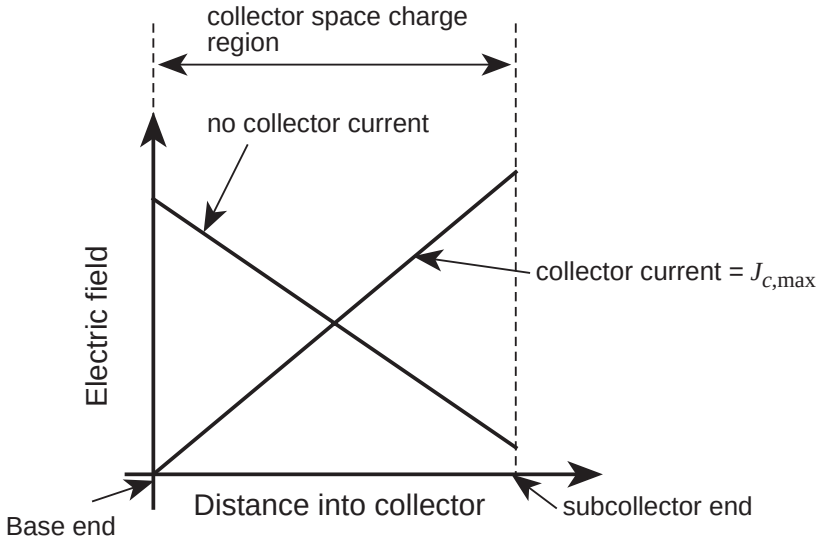


Figure 2.11: Electric field profiles in the collector space charge region in the presence and absence of collector current.

The Kirk effect can be partially suppressed by appropriate collector doping. Increased n-doping over a short distance adjacent to the base will provide a large electric field in that region as shown in figure 2.12. The n-doped region is thin. Hence, even though the electric field is high in that region, the total potential drop across the collector changes by a small amount due to its insertion in the collector layer. This structure has been reported in [21].

2.6 Collector breakdown

A lower collector breakdown voltage may not permit the collector-base voltage to be increased to the extent that is required to prevent base pushout at a high current density. A larger collector breakdown voltage is therefore helpful in obtaining a high HBT bandwidth.

The collector-base junction reverse saturation current I_{CO}, measured with the emitter open, influences collector breakdown significantly in the common emitter mode. I_{CO} is multiplied by the current gain β and appears in the collector current as

$$I_c = \beta I_b + \beta I_{CO}. \tag{2.20}$$

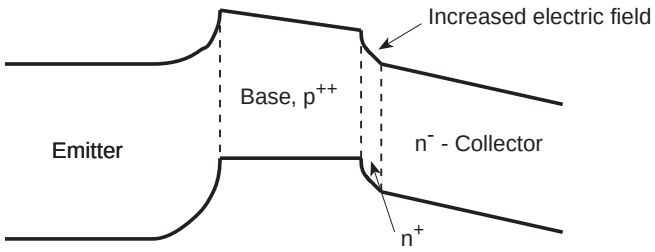


Figure 2.12: Band diagram of the structure to partially suppress base pushout. (after [21]).

If there is an avalanche multiplication factor M in the collector region, the expression for the collector current is

$$I_c = \left[\frac{\alpha M}{1-\alpha M}\right] I_b + \left[\frac{M}{1-\alpha M}\right] I_{CO} \tag{2.21}$$

where $\alpha = \beta/(1+\beta)$. Larger values of the current gain β, multiplication factor M, and I_{CO} can potentially cause a large increase in the collector current leading to breakdown.

For a particular choice of collector material, the multiplication factor is larger if the electric field in the collector is large and the carriers gain kinetic energy over a sufficient distance to create electron-hole pairs by impact ionization. We consider a transferred substrate HBT with a InGaAs collector doped to $1\times10^{16}/\text{cm}^3$ and a thickness of 2700 Å at a current density of 10^5 A/cm^2. The measured breakdown at this current density with a common emitter configuration occurs below $V_{ce} = 1.6$ V. For an approximate V_{be} of 0.7 V, the collector-base applied voltage is 0.9 V. The built-in potential is approximately 0.55 V and hence, the total potential drop across the collector is approximately 1.45 V. The net charge in the collector is calculated considering the n-doping concentration and the electrons due to the collector current assuming a saturated velocity of 5×10^5 m/s for the electrons in the collector. Poisson's equation is applied to the net charge density in the collector and the electric field is calculated. Near the base, the electric field is 4.9×10^6 V/m and near the collector contact the field is 5.8×10^6 V/m. These electric fields are much smaller in magnitude compared to the observed breakdown fields of reverse biased InGaAs PIN photodiodes.

Other than impact ionization in the collector, contributions to I_{CO} can be from Zener (band to band) tunneling, hole tunneling from the collector Schottky

contact, and thermal generation in the collector region. The possible contributions to I_{CO} are illustrated in figure 2.13.

Large electric fields may appear near the collector contact, under the condition of base pushout, as is indicated in figure 2.14. Under such conditions, the tunneling components of I_{CO} may become large. Avalanche multiplication can also be significant depending on the presence of large electric fields over significant distances.

Thermal generation of carriers in the collector depletion region is a significant contributor to I_{CO} for narrow bandgap semiconductors. Thermal generation is proportional to the intrinsic carrier concentration n_i, which in turn depends on the bandgap E_g as $n_i \propto \exp(-E_g/2kT)$. Measured values of I_{CO} for narrow and wide bandgap HBTs have been reported in [22]. The difference in bandgap was the only difference in the compared HBT structures. The narrow bandgap (InGaAs) collector showed significantly larger values of I_{CO} as compared to the wide bandgap (GaAs) collector. The temperature dependence of I_{CO} for the narrow bandgap device was large compared to the wide bandgap device at low collector-base bias voltages. Between 25 °C and 125 °C there is an increase of $\sim 10^3$:1 in I_{CO} for the device with the InGaAs collector. A wider bandgap collector is therefore desirable for reducing the thermal generation component of I_{CO}.

Evidence of Zener tunneling current in the measured I_{CO} of devices with narrow bandgap collectors has been reported in [22]. Zener tunneling was observed at higher values of collector-base bias voltages (V_{cb}) and resulted in "softer" reverse breakdown characteristics of the collector-base diodes. Significant increase in I_{CO} was observed with increasing V_{cb}. In contrast, I_{CO} of devices with GaAs collectors showed much lower dependence on V_{cb} and the breakdown characteristics were abrupt. Wider bandgap collectors were found to suppress Zener tunneling.

With Schottky collector contacts, the possibility of hole tunneling from the collector contact (as in figure 2.13) exists. A high electric field near the collector contact creates a narrow tunneling barrier for the holes. In such a situation, hole tunneling current can contribute significantly to I_{CO}. With the experiments conducted so far with Schottky collector transferred substrate HBTs, it has not been possible to estimate the extent of hole tunneling. Appropriately graded wider bandgap collectors (figure 2.16) can be used to provide a larger barrier for hole tunneling and thereby suppress this effect.

The common emitter characteristics of a transferred substrate HBT is shown

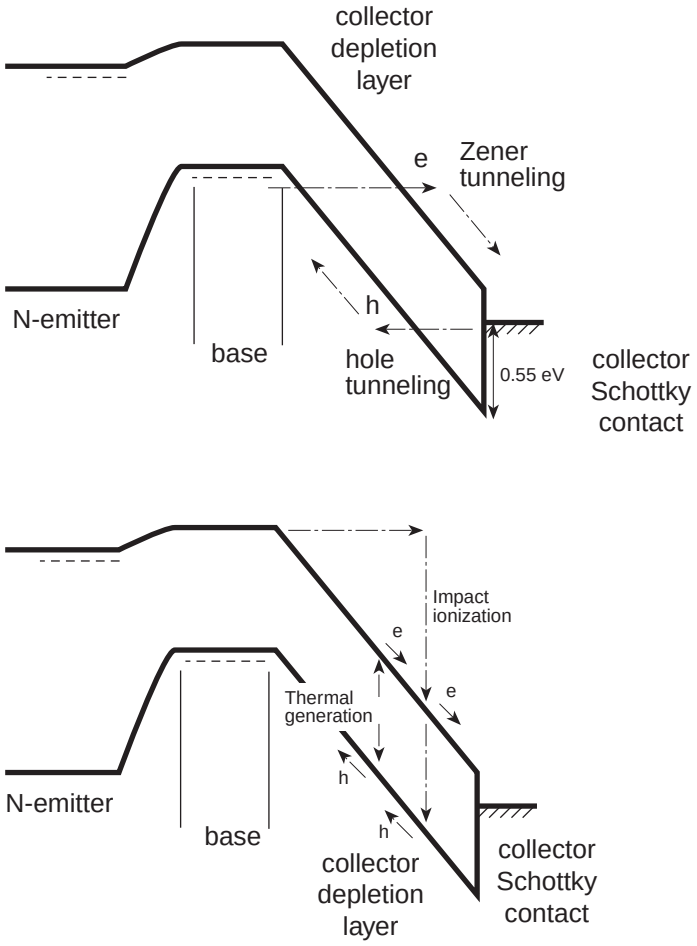


Figure 2.13: Possible contributions to I_{CO}.

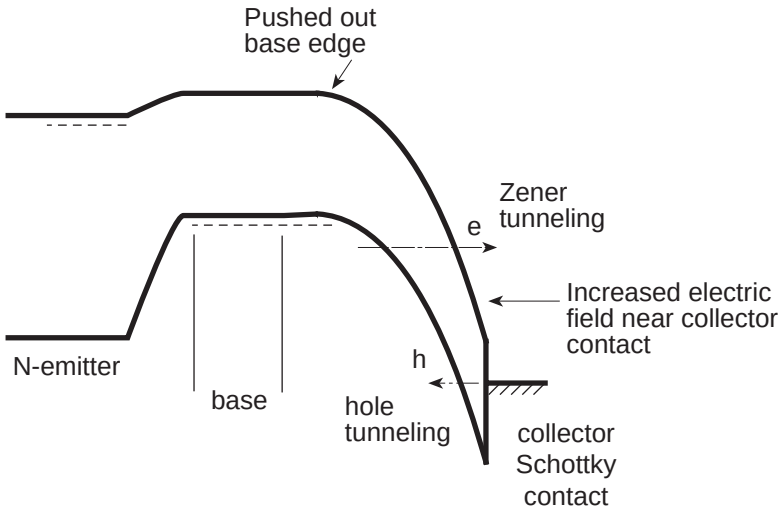


Figure 2.14: Enhancement in tunneling due to base pushout.

in figure 2.15. The breakdown voltage decreases with increased collector current. This phenomena has also been reported for double mesa HBTs with narrow bandgap collectors. The dependence of breakdown voltage on collector current is significantly less with wider bandgap collectors. The common emitter characteristics reported in [22] show lower breakdown voltages at higher temperatures for a InGaAs collector HBT. A similarly designed GaAs collector showed the opposite trend. This supports the conclusion that impact ionization is responsible for breakdown in wider bandgap semiconductors. In narrow bandgap semiconductors, increase in the various components of I_{CO} in direct relation to the increase in collector current is a likely cause for collector breakdown.

Improvement in collector breakdown voltage by using a larger bandgap collector has been widely reported in literature (recently in [23]). Transferred substrate HBTs should also be able to benefit from larger bandgap collectors. A possible structure is shown in figure 2.16. The delta dopings are used to create electric fields which counteract the quasi-electric fields associated with bandgap grading. Near the collector contact, the wider bandgap semiconductor is graded back to the narrow bandgap material so that maximum barrier for hole tunneling is obtained, suppressing hole tunneling. The wider bandgap collector will also suppress Zener tunneling.

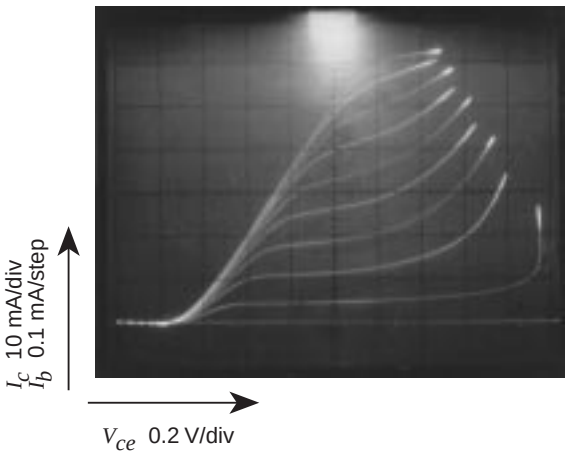


Figure 2.15: Common emitter characteristics showing lowering of breakdown voltage with increasing collector current.

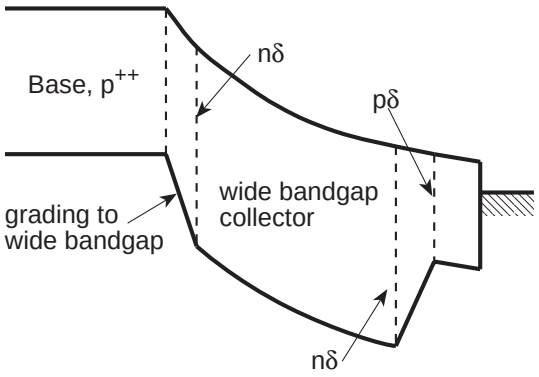


Figure 2.16: Wide bandgap collector for Schottky collector transferred substrate HBTs.

2.7 Current gain degradation with scaling

Diffusion is isotropic. Electrons can diffuse both vertically and laterally within the base layer. The applied V_{be} forces a boundary condition of a specified electron density at the junction. An electron concentration gradient exists both vertically and laterally. The boundary condition at the collector junction is electron density $n \sim 0$ and so also at the base ohmics. The boundary condition at the exposed surface is $J_{\text{rec}} = v_s n$ where v_s is the surface recombination velocity and n is the concentration of electrons at the surface.

Low surface recombination velocity is necessary to improve current gain. Recombination velocity of electrons on exposed surfaces of InGaAs base material is known to be less than that of GaAs. This is one of the important reasons for choosing the InAlAs/InGaAs material system for this work. The surface passivation material around the base-emitter junction which is in contact with the bare base material has significant effect on the recombination rate. This is experimentally shown in [24]. Abrupt InP/InGaAs HBTs which were passivated with polyimide showed current gains above 100 for an emitter geometry of 2 μm $\times$ 20 μm. The current gain did not change significantly over a range of emitter currents from 1 mA to approximately 50 mA. The ideality factor for collector current was 1.4. In contrast, a silicon dioxide passivated device with a similar structure showed current gains varying from 10 to approximately 50 over the same current range. The ideality factor was close to 2. This shows that polyimide is superior to silicon dioxide as a passivating material for InGaAs base HBTs.

The aspect ratio between the base thickness and the emitter width influences current gain. If the aspect ratio is large, the fraction of the injected electrons spreading laterally in the base is large and the periphery recombination current increases, degrading current gain. A thinner base is therefore desired. For a fixed base thickness, a larger vertical velocity through the base mitigates the lateral diffusion problem because the electrons spread laterally to a lesser extent and hence, there is less lateral recombination. Experiments illustrating this effect have been reported in [18]. Abrupt InP/InGaAs HBTs of similar structure were fabricated where one set of devices had a graded bandgap base and the other set had an uniform base. This was the only difference. The graded base devices not only had a larger value of f_τ, but also had a larger value of DC current gain.

Extrinsic base structures as shown in figure 2.6 help to confine carriers within the intrinsic base. This reduces the lateral recombination current component.

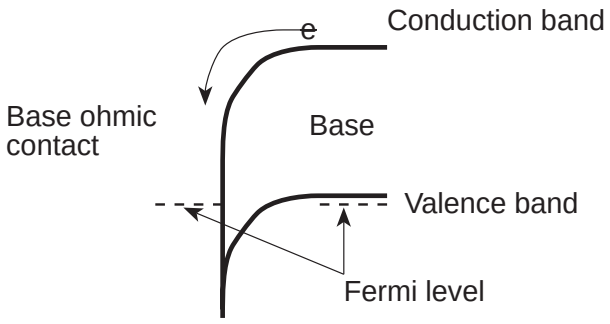


Figure 2.17: Band diagram at the base ohmic contact.

The DC current gain should improve with extrinsic base structures which are more heavily doped and/or of a wider bandgap than the intrinsic base. If the extrinsic base is a regrown structure then the recombination current at the interface between the intrinsic base and the extrinsic base may be of concern. Recent work [25] has shown that this is small and current gains above 100 have been reported for devices with emitter dimensions of 1.6 μm $\times$ 4.6 μm at current densities of 10^5 A/cm^2.

The proximity of the base contact metal to the emitter mesa edge is also a potential cause for lower current gain. The band diagram in figure 2.17 shows a possible means by which electrons in the vicinity of the base contact may recombine at the base ohmic contact. If the base ohmic contact is sufficiently far from the edge of the emitter mesa, there will be relatively fewer electrons and the fraction of the electrons lost this way will be reduced. The associated penalty is an increase in the base resistance. An optimum distance between the base ohmic contact and the emitter has to be found. This effect has been observed in the course of experiments and will be discussed in detail in chapter 4.

Transferred substrate HBTs with a 1 μm emitter width and a nominal base thickness of 300 Å have current gains between 35 and 40. It might be difficult to scale the base thickness in proportion to the emitter width for deep submicron scaling. The techniques described above which mitigate the effect of a large aspect ratio will be important for deep submicron scaling of transferred substrate HBTs.

2.8 The transferred substrate HBT

The emitter and collector contacts of a transferred substrate HBT can be scaled laterally to deep submicron dimensions with a consequent large increase in device bandwidth. This has to be viewed in association with the other improvements suggested above while surveying the work of other groups. The final intention is to incorporate the best possible layer structure from speed considerations, with the best possible contact technology to a highly scaled device.

Improving device performance is greatly facilitated by making all device parameters independent of each other so that all can be independently chosen at best possible values. To this end, the transferred substrate HBT geometry makes the collector-base capacitance independent of the base resistance by making the former independent of the size of the base mesa. It is also necessary to strive to make other parameters independent of each other.

A device structure including most of the improvements mentioned above is shown in figure 2.18. However, at this stage of the work, only very few of these features have been incorporated in transferred substrate HBTs.

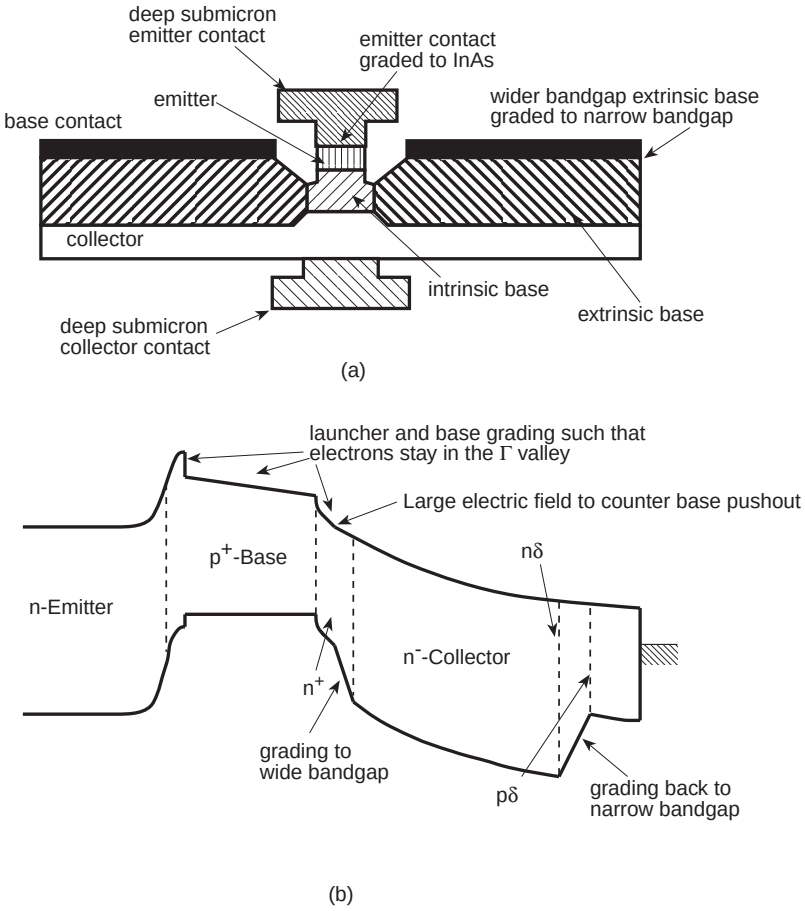


Figure 2.18: Improved transferred substrate HBT: (a) structure, (b) band diagram.

Chapter 3

Material growth and device fabrication

The materials used to fabricate transferred substrate HBTs were grown at the MBE facilities of the University of California, Santa Barbara. Significant time was spent in characterizing and optimizing material growth for improved device performance. Experiments performed in this area and their results will be presented in this chapter. This is an ongoing effort involving several researchers, past and present. All materials used in this thesis work were grown by Dr. M.J. Mondry or Dr. L. Samoska.

The fabrication of transferred substrate HBTs was the biggest challenge faced in this thesis work. The fabrication aspect of the work will be described in detail in this chapter. The discussion will include the various steps involved in the fabrication process, the problems encountered, and the solutions to those problems. The layout of the devices and mask design will also be discussed.

3.1 Material growth

The InAlAs/InGaAs material system was chosen for the fabrication of transferred substrate HBTs. The materials were grown by MBE, lattice matched to semi-insulating InP substrates.

3.1.1 Layer structure

A layer structure typical of that used in this thesis work is shown in figure 3.1(a). The band diagram corresponding to this layer structure at zero bias is shown in figure 3.1(b). The layer structure closely follows the designs of [26]. In chapter 2 potential future enhancements to the simple material design of figure 3.1 has been discussed; these have not yet been incorporated into transferred substrate HBTs.

Figure 3.1 also shows the substrate temperatures during growth. The emitter cap, the emitter and the grade are grown at a relatively high substrate temperature. The temperature is progressively reduced during the base growth and is maintained at a lower value during collector growth. This reduces Be movement into the collector.

The band diagram corresponding to the layer structure of figure 3.1(a) under bias is shown in figure 3.2. The biasing conditions are as follows: base-emitter voltage $V_{be} = 0.7$ V, collector-emitter voltage $V_{ce} = 1.2$ V, and a emitter current density of 1×10^5 A/cm^2. The collector current density is assumed to be the same as the emitter current density. The effect of the electrons in the collector space charge layer due to the collector current is included while calculating the electric field and the electrostatic potential in the collector space charge layer. An electron velocity of 5×10^5 m/s is assumed in the collector.

3.1.2 Be movement with growth direction

A major consideration in material growth is the movement of Be base dopant towards the emitter and the collector. A large Be movement in the direction of the emitter degrades emitter injection efficiency. On the collector side, Be movement increases the base thickness and decreases the collector thickness. A thicker neutral base will not have a proportionally lower resistance because significant portions of it will be lightly doped. Overall, there is a degradation in device performance if Be migrates out to a large extent from the intended region in the base.

There is significant migration of the Be base dopant into the collector depletion region. Capacitance voltage measurements of large area collector-base diodes and subsequent extraction of the doping profile showed between 300 and 400 Å migration of Be into the 3000 Å collector. A typical extracted doping profile is shown in figure 3.3. As observed in figure 3.3, the Be migration front has a smooth variation of Be concentration with position. A single distance param-

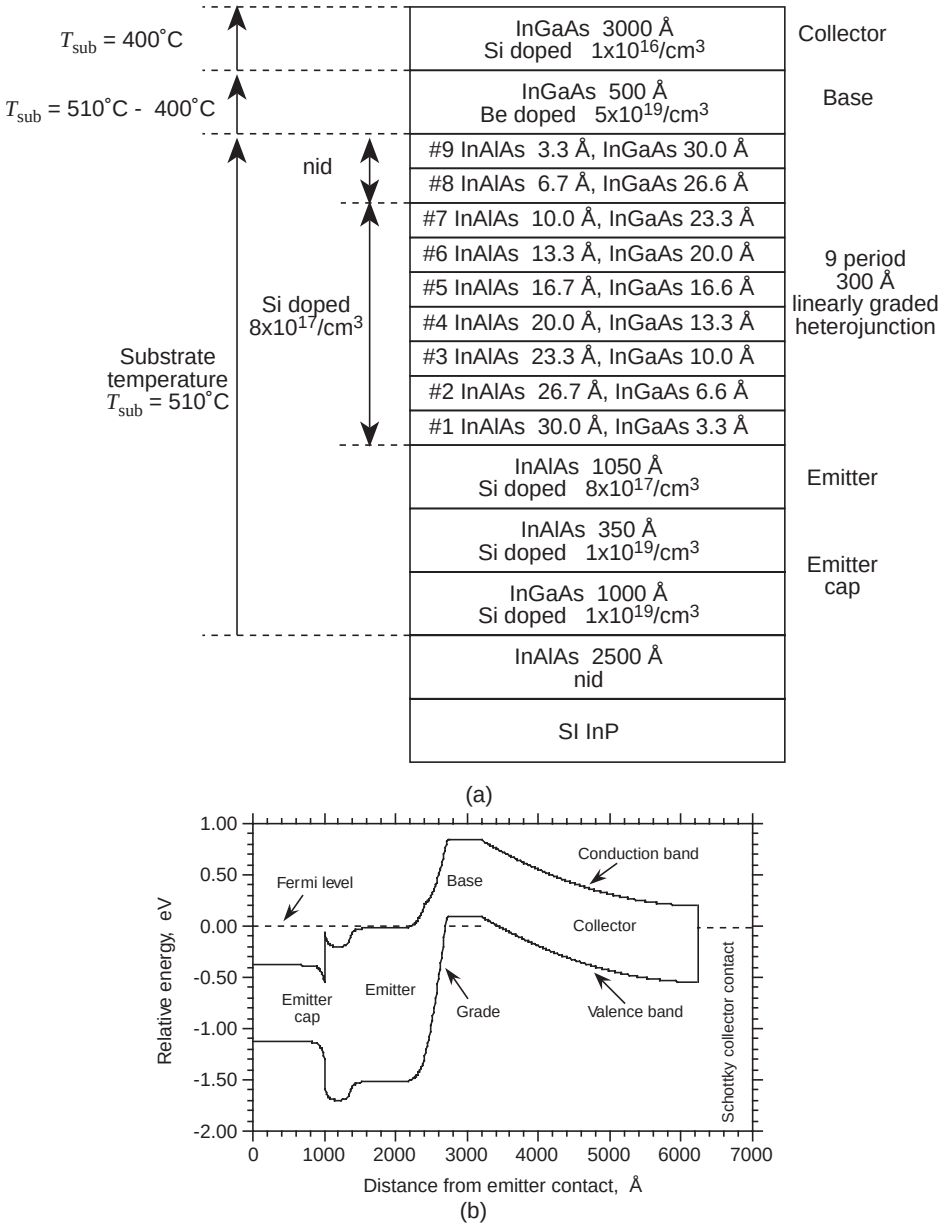


Figure 3.1: (a) Layer structure with growth conditions. (b) Band diagram. This structure was grown by Dr. L. Samoska at the MBE facilities of the University of California, Santa Barbara.

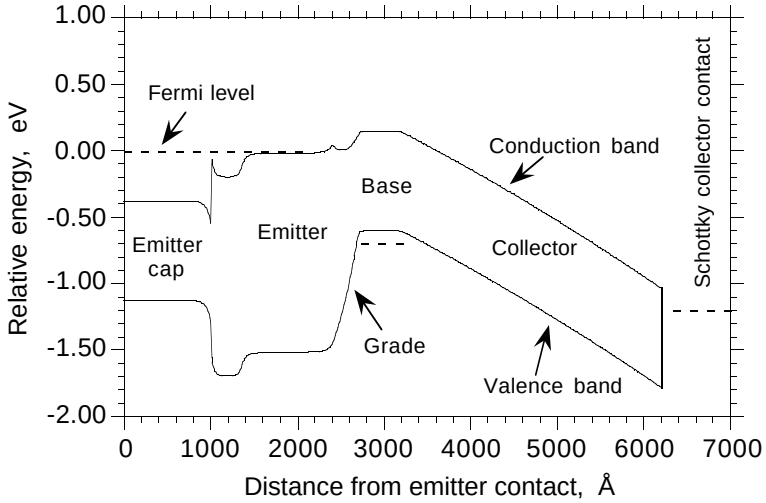


Figure 3.2: Band diagram of a transferred substrate HBT under bias. The bias conditions are: $V_{be} = 0.7$ V, $V_{ce} = 1.2$ V, and $J_c = 1 \times 10^5$ A/cm^2.

eter cannot describe this profile. The collector-base junction is determined by depletion into the Be acceptor population by the applied collector base bias. This generally results in a junction located approximately at the point of $\sim 10^{17}$/cm^3. This concentration is used to define the Be migration distance.

All materials used in this thesis work were grown collector-up as shown in the layer structure of figure 3.1. It is evident that ~ 300 Å Be movement has taken place in the direction of the collector. A similar movement towards the emitter would have suppressed the heterojunction barrier. Hence, the Be movement is asymmetric.

An experiment was conducted to determine if the growth direction was responsible for this significant asymmetry. The layer structure used for this experiment is shown in figure 3.4(a). Two sets of diodes with the p^+-n^--metal structure were fabricated. One set was fabricated on the wafer as grown. A Schottky contact was made to the top n-doped InGaAs layer and an ohmic contact to the p^+ InGaAs layer. The other set was fabricated from the same epitaxial material after the epitaxial film was flipped using the substrate transfer process. The Schottky contact in the latter set was made to the bottom n-doped

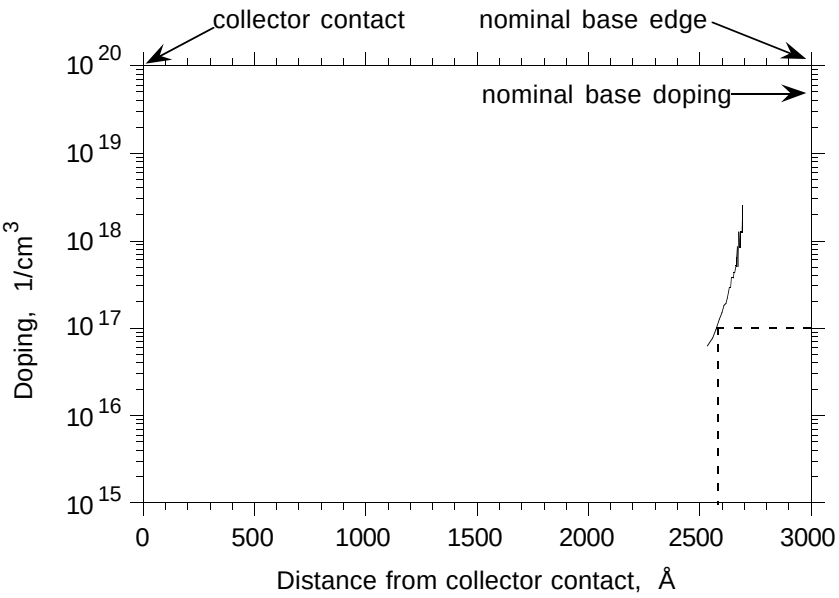


Figure 3.3: Extracted doping profile from large area, reverse-biased collector-base diodes.

InGaAs layer. The band diagram across these devices is shown in figure 3.4(b). The extracted doping profiles from the two sets of diodes are shown in figure 3.5. The two profiles are similar. There is no significant growth direction dependence in Be movement. The extent of the Be movement is somewhat higher than that observed in the collector side of HBTs. This is possibly due to the higher growth temperature of the test sample compared to the HBT growths. We conclude that the asymmetry in Be movement between the emitter and collector directions is a result of the hetero-interface. This observation has been confirmed by recent experiments of Dr. L. Samoska with double heterostructure (InAlAs/InGaAs/InAlAs) HBTs. In these devices, minimal Be movement is observed into either the emitter or the collector heterojunction.

3.1.3 Be migration and setback layers

In the literature there are a range of results reported for Be movement into the emitter. Excessive Be movement will increase the required V_{be} and degrade the emitter injection efficiency, possibly catastrophically. Because of such Be

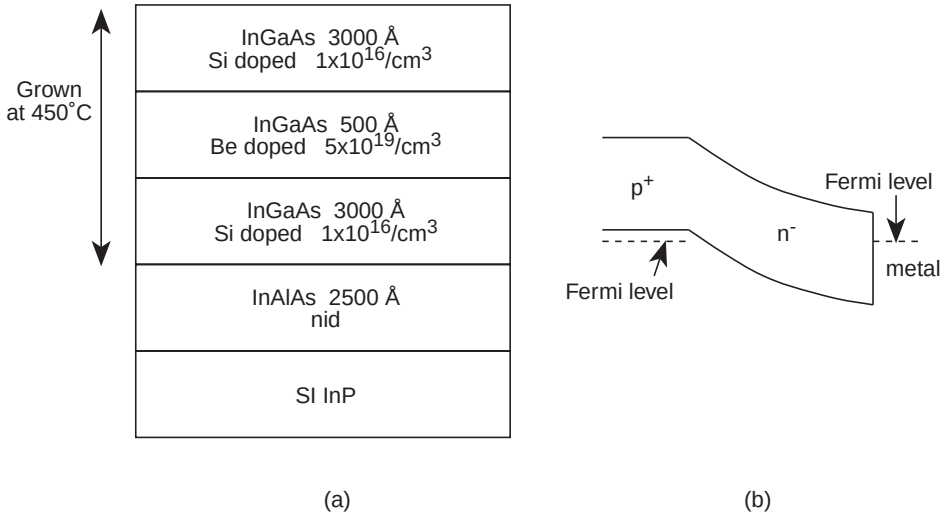


Figure 3.4: (a) The layer structure used to investigate the dependence of Be migration on growth direction. (b) Band diagram of the fabricated diodes.

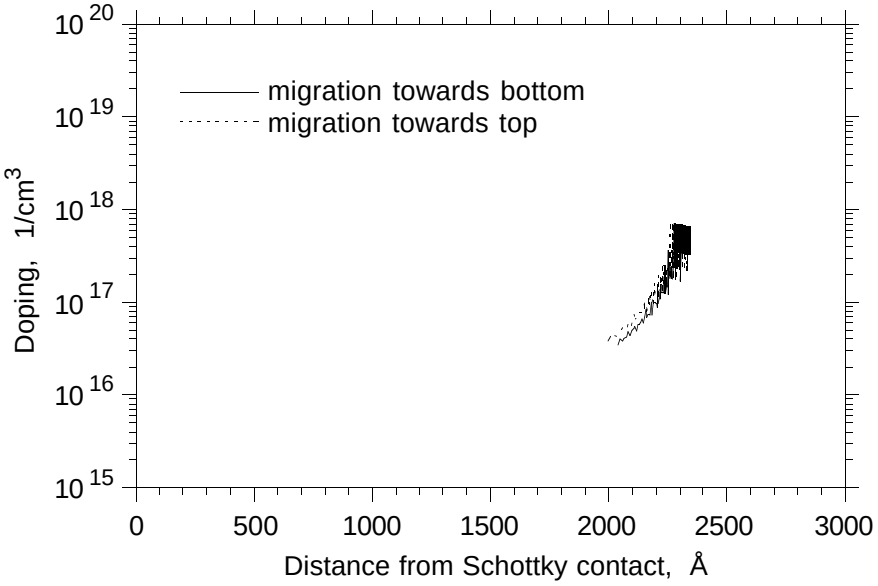


Figure 3.5: Extracted doping profile from two sets of p^+-n^--metal devices.

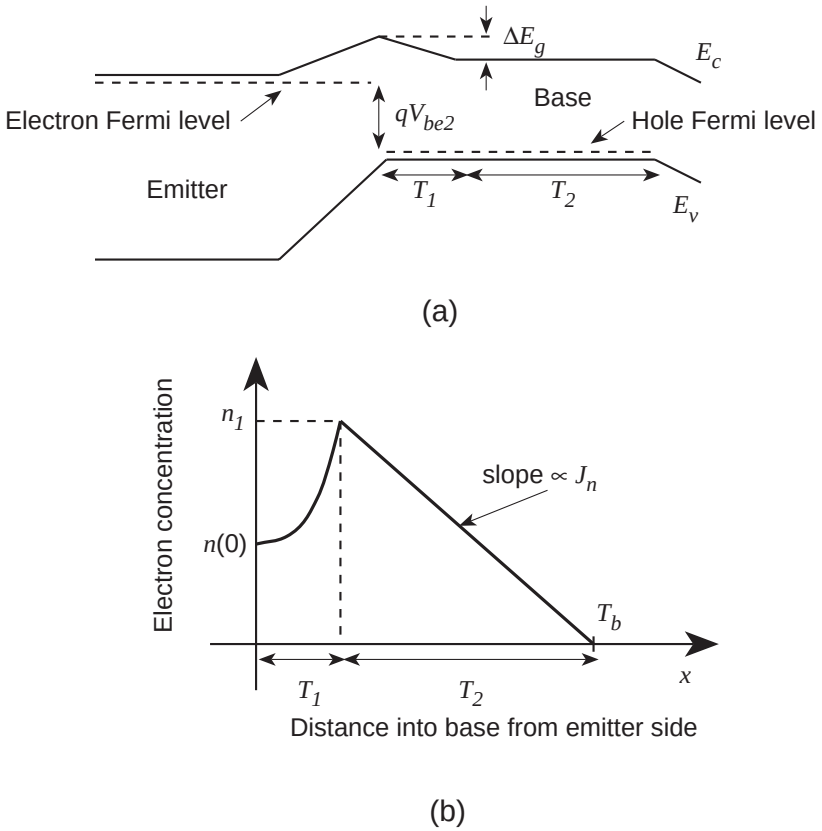


Figure 3.6: Be movement into the emitter-base graded heterojunction. (a) Band diagram. (b) Electron concentration profile in the base.

movement, several reported HBTs (e.g. [29]) have used growth setback layers between the emitter and the base. In our work, these setback layers were initially used but were found to be unnecessary and to degrade transistor performance. A detailed analysis of these effects therefore follows.

Graded heterojunction without setback layers

In a graded heterojunction HBT, the movement of Be into the grade causes an increase in the base-emitter voltage required to maintain a fixed current density. Experimental observation of this effect has been reported in [27]. An explanation is given below.

A simplified case with reference to figure 3.6 is considered. There is no setback

layer between the base layer and the graded heterojunction. Be is assumed to have moved a distance T_1 into the grade, doping this region to the same level N_a as the base. A peak of height ΔE_g is created in the conduction band. In this approximate analysis, the effective density of states in the conduction band N_c and the valence band N_v and electron diffusion constant D_n are assumed to be constant in the p-doped regions. The p-doping is assumed to be non-degenerate and the hot electron effects are ignored.

Under these assumptions the electron concentration is calculated from the Boltzmann statistics and the drift-diffusion equation. An electron concentration profile is shown in figure 3.6(b). In the uniform bandgap region of the base, the electron concentration follows a constant slope profile with the electron current J_n being proportional to the slope. In the graded bandgap region the electron density is reduced and follows the profile

$$n(x) = n_1 \left[\frac{T_1}{T_2 \alpha} + \left(1 - \frac{T_1}{T_2 \alpha} \right) \exp \left\{ -\alpha \left(1 - \frac{x}{T_1} \right) \right\} \right] \tag{3.1}$$

where $\alpha = \Delta E_g / kT$. The point $x = 0$ is the leftmost point to which Be has moved. Expression (3.1) is obtained by solving for constant current J_n the drift diffusion equation

$$J_n = q \mu_n n(x) \mathcal{E} + q D_n \frac{dn(x)}{dx} \tag{3.2}$$

with the boundary condition $n(T_1) = n_1$. The electric field $\mathcal{E} = \Delta E_c / q T_1 = \Delta E_g / q T_1$ because the material is of constant p-doping. The electron concentration at $x = 0$ is therefore lower than the value at the edge of the uniform-bandgap base region by the factor

$$\frac{n(0)}{n_1} = \exp(-\alpha) \left[1 + \frac{T_1}{T_2} \left(\frac{\exp(\alpha) - 1}{\alpha} \right) \right]. \tag{3.3}$$

Let V_{be1} be the applied base-emitter voltage for a particular value of n_1 (and hence J_n) in the case where there has been no movement of Be outside the uniform base. According to the Shockley boundary conditions

$$n_1 = n_{p0} \exp \left(\frac{q V_{be1}}{kT} \right) \tag{3.4}$$

where n_{p0} is the thermal equilibrium concentration of electrons at the edge of the uniform base. Let V_{be2} be the applied base-emitter voltage, for maintaining

the same J_n, in the case where Be has moved partially into the grade as shown in figure 3.6. Then,

$$n(0) = n_{p0} \exp\left(-\frac{\Delta E_g}{kT}\right) \exp\left(\frac{qV_{be2}}{kT}\right) = n_{p0} \exp(-\alpha) \exp\left(\frac{qV_{be2}}{kT}\right). \tag{3.5}$$

From (3.4) and (3.5), the ratio

$$\frac{n(0)}{n_1} = \exp(-\alpha) \exp\left(\frac{q\Delta V_{be}}{kT}\right) \tag{3.6}$$

where $\Delta V_{be} = V_{be2} - V_{be1}$ is the increase in V_{be} due to the movement of Be into the grade given that a fixed value of electron current has to be maintained. Using (3.6) in (3.3), the expression for ΔV_{be} is obtained as

$$\Delta V_{be} = \frac{kT}{q} \ln\left[1 + \frac{T_1}{T_2}\left(\frac{\exp(\alpha) - 1}{\alpha}\right)\right], \tag{3.7}$$

where $\alpha = \Delta E_g / kT$.

This relationship can now be used to evaluate Be movement in the HBTs studied herein. The layer structures used in this project have a 300 Å linearly graded region between InAlAs (emitter, bandgap = 1.45 eV) and InGaAs (base, bandgap = 0.75 eV). If, for a 500 Å intended base thickness, Be has moved 100 Å into the grade, an increase in base-emitter voltage of 135 mV is expected under the simplified assumptions of the derivation.

The expression (3.7) and more general cases can be obtained by using the following modified Moll-Ross current relation as derived in [28].

$$J_n = -\frac{q \exp\left(\frac{qV_{be}}{kT}\right)}{\int_B \left(\frac{p}{D_n n_i^2}\right) dx} \tag{3.8}$$

Effect of setback layers

Low-temperature growth has been reported in the literature to suppress Be movement. In our HBT experiments, low growth temperatures and significant setback layer thicknesses have lead to larger transit times and lower current gain. The setback is inserted with the purpose of compensating for Be movement and hence is lightly doped compared to the base. If the design of the setback is incorrect,

such that the Be movement is less than the full setback layer thickness, an undepleted and lightly doped base setback layer may result. This increases base transit time, as is now shown.

Let us consider figure 3.7. Here D_n is the base diffusion constant for the electrons. N_{a1} and N_{a2} are the setback and base layer doping respectively. T_1 and T_2 are the setback and base layer thickness respectively. The diffusion constant D_n is assumed to be the same at all points within the base and the doping is approximated as non-degenerate. A two-step doping profile as shown in figure 3.7(a) is assumed for the case where the setback is doped lightly compared to the base.

There is an increase in the stored electron charge in the lightly doped setback layer as compared to the case where the setback and the base have the same doping level. A fixed electron current density J_n is maintained in both of these cases. The base transit time is given by the relation

$$\tau_b \triangleq \frac{Q_{\text{stored}}}{J_n}. \tag{3.9}$$

The base transit time for the case with setback increases by the ratio

$$1 : 1 + \frac{2T_1T_2}{T_b^2}\left(\frac{N_{a2}}{N_{a1}} - 1\right) \tag{3.10}$$

compared to the situation where the setback becomes doped as strongly as the base and $T_b = T_1 + T_2$. The ratio of transit times is even higher,

$$1 : 1 + \left(\frac{T_1}{T_2}\right)^2 + \frac{2T_1N_{a2}}{T_2N_{a1}}, \tag{3.11}$$

when compared to a situation of no setback and $T_b = T_2$.

In our experiments, the electron transit time ($= \tau_b + \tau_c$) through a device with a 100 Å spacer layer nominally doped to $2 \times 10^{18}/\text{cm}^3$ was 2.6 psec. For this device, the base layer thickness was 600 Å with a doping of $5 \times 10^{19}/\text{cm}^3$. A similar structure with no setback layer, as in figure 3.1, had $\tau_b + \tau_c = 1.1$ psec. If the nominal values of the layer thicknesses and dopings (given above) are used in (3.11), the factor by which the base transit increases is found to be 9.4:1. This factor will decrease if significant amounts of Be migrates to the setback layer. We therefore conclude that small setback layers, if lightly doped, can radically increase the base transit time.

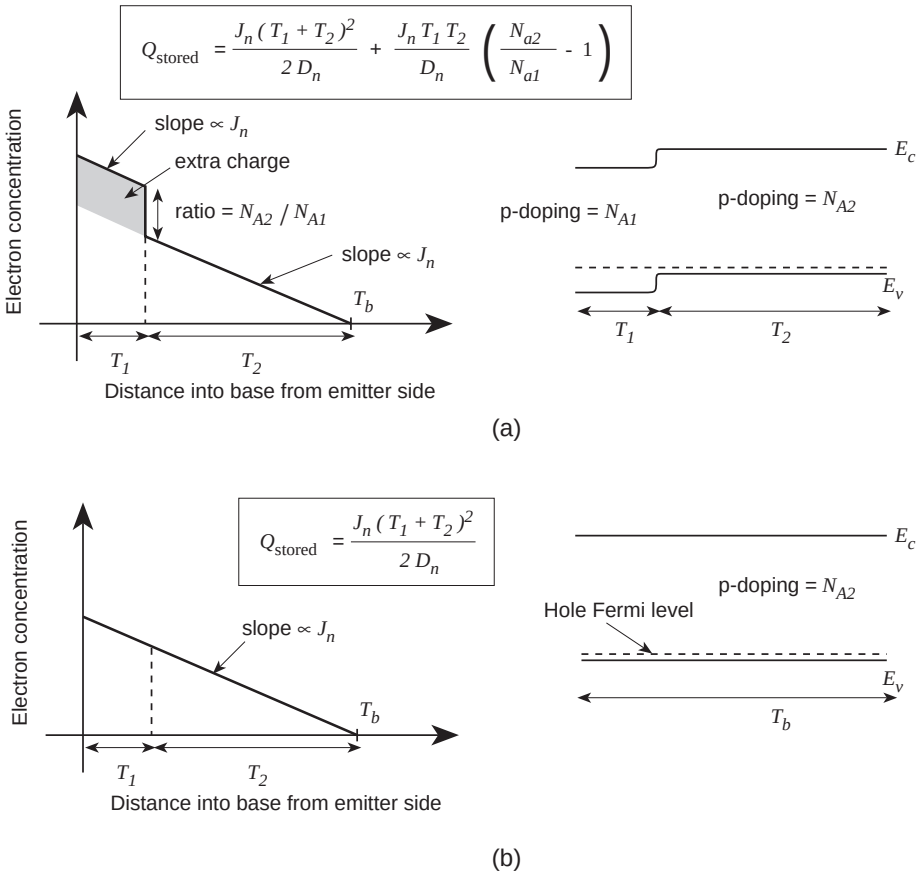


Figure 3.7: Electron concentration in the base and band diagrams for the case (a) with lightly doped setback and (b) setback doped as heavily as the base.

The expressions (3.10) and (3.11) can also be derived from the Moll-Ross relation for the base transit time.

$$\tau_b = \frac{1}{D_n} \int_0^{T_b} \frac{1}{N_a(x)} \left[\int_x^{T_b} N_a(y) dy \right] dx \tag{3.12}$$

Setback layers may also cause the $n = p$ plane in the emitter-base junction to be in a narrower bandgap material than the case without setback. This is the plane of maximum electron-hole recombination for equal electron and hole lifetimes according to the Sah-Noyce-Shockley model for recombination within depletion regions. For a recombination level close to the middle of the energy

gap, the recombination rate is proportional to the intrinsic carrier concentration n_i, which in turn depends on the bandgap energy E_g as $n_i \propto \exp(-E_g/2kT)$. With no setback layer, there would be Be movement into the grade. The n=p plane would move to a wider bandgap material within the grade. As a result, the recombination rate would be reduced and the current gain of the HBT would be improved. The relation between increased Be movement into the grade and improved current gain has been experimentally observed in [27].

In our experiments, devices with larger setback layers have generally shown poor DC current gain. Figure 3.8 compares the Gummel plots of devices with and without base setback layers. The layer structures of these devices are similar to figure 3.1. The region of difference is highlighted in figure 3.8. The base current in the case with setback (figure 3.8(b)) shows a large increase in its value compared to the no-setback case, but it is not clear that this increase is due to the movement of the $n = p$ plane to narrower-bandgap material. If this happened, the collector current plot would have shifted to the left. As observed in figure 3.8, the collector current plots at lower currents are almost the same for both structures with and without setback. The probable reason for the large base current is processing problems with the base-emitter junction at the time when the devices with the base setback layer were fabricated. At that time, processing difficulties often lead to the filaments of emitter metal contacting the edge of the emitter-base mesa. It is suspected that this resulted in spurious Schottky contacts which caused the observed leakage.

The processing problems notwithstanding, an interesting conclusion can be arrived at by observing the collector currents in figure 3.8. At lower V_{be} the collector currents are almost identical. For the material grown at our MBE facility, with 5×10^{19} /cm^3 Be doping in the base layer, there is no evidence of Be movement into the emitter-base heterojunction despite the absence of a base setback layer.

3.2 Fabrication

Discrete transferred substrate HBTs have been fabricated. The fabrication process is summarized in figure 3.9. HBT material is grown collector up and the first step is the deposition of metal Schottky contacts directly on the collector depletion layer. In the next step, the InP substrate is inverted and attached to a GaAs substrate by means of epoxy. The host InP substrate is then etched away using a selective etch that does not etch GaAs. Subsequently, a normal HBT

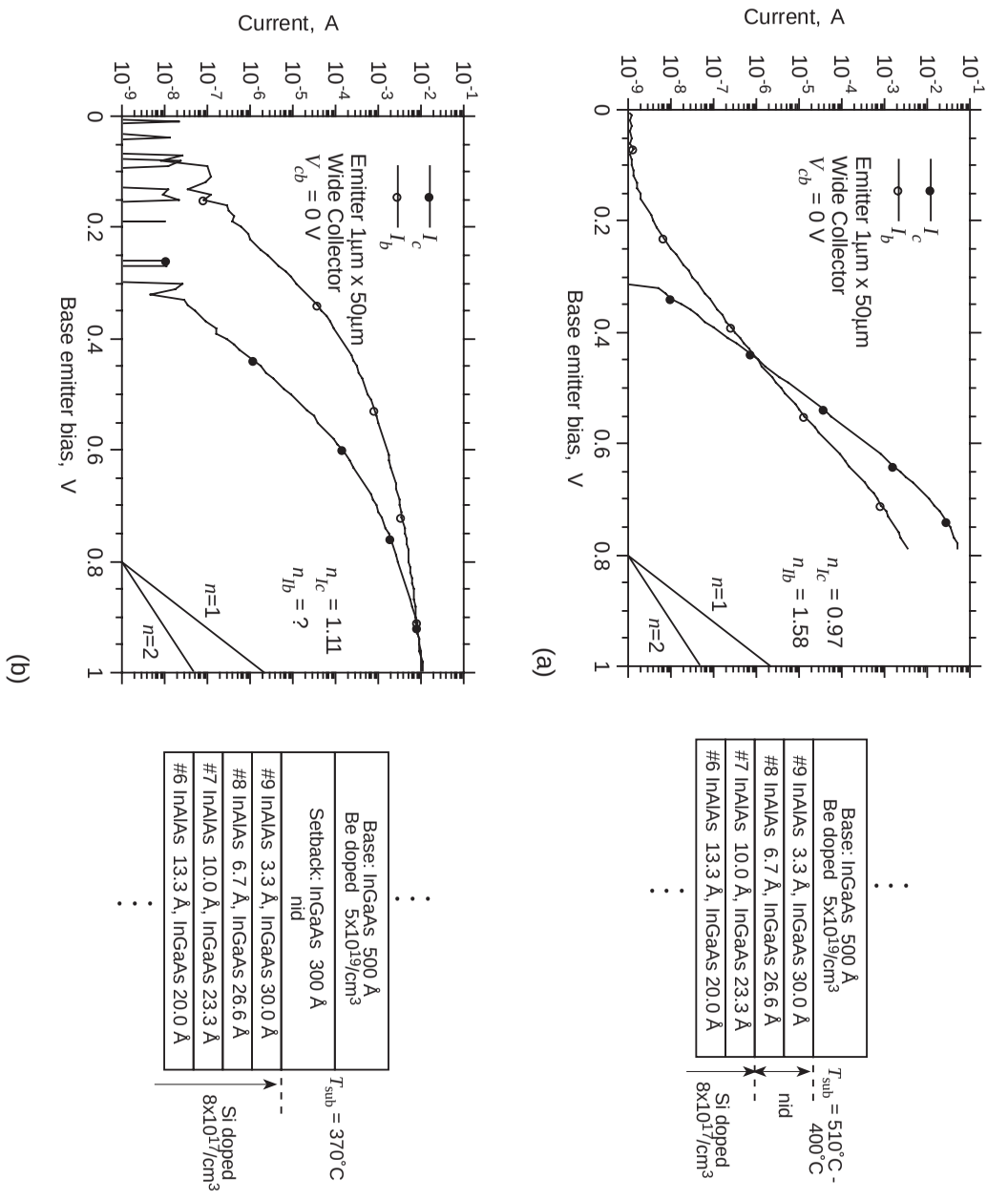


Figure 3.8: Gummel plots of devices (a) without setback, and (b) with setback.

fabrication sequence is followed to complete the fabrication process.

The following subsections contain a detailed description of the important steps in the fabrication process. This includes the problems encountered in developing the process and their solutions. An extremely detailed process description is given in the appendix.

3.2.1 Collector definition

The first step is the definition of the collector Schottky contact by a photoresist liftoff process depositing Ti/Pt/Au. This step also defines the emitter, base, and collector pads which will be used in probing the completed device. Alignment marks required for aligning subsequent structures to the collector are also defined at this time.

A recess etch to remove semiconductor from around the collector finger, if necessary, is conducted at this time. A wet etch can be performed if the undercut under the collector finger is tolerable. If the collector finger is narrow, or, if the undercut significantly changes the emitter to collector width ratio, then reactive ion etching (RIE) is necessary to reduce the undercut. In either case, the collector contact acts as the etching mask. The etch depth is controlled such that it is contained within the collector depletion layer.

The collector definition and the recess etching steps are illustrated in figure 3.10.

3.2.2 Substrate transfer

In this step, the InP wafer is inverted and attached to the GaAs wafer using epoxy. The InP wafer is subsequently etched away to expose the emitter side of the epitaxial film. Other methods of substrate transfer have been reported; e.g. using Van-der-Waals forces to bond epitaxial films on different substrates after detaching the films from the host substrate by epitaxial liftoff [30]. A detailed description of the substrate transfer process using epoxy follows.

A two-component epoxy is used. The two components are available, in the proportion in which they should be mixed, in vacuum packs separated by a membrane. Before use, this membrane is removed and the two components are mixed while still in the vacuum pack. This prevents air bubbles from entering the epoxy while mixing, which otherwise could create voids in the bond between the two wafers. After mixing, the epoxy is spread on the InP wafer and a GaAs

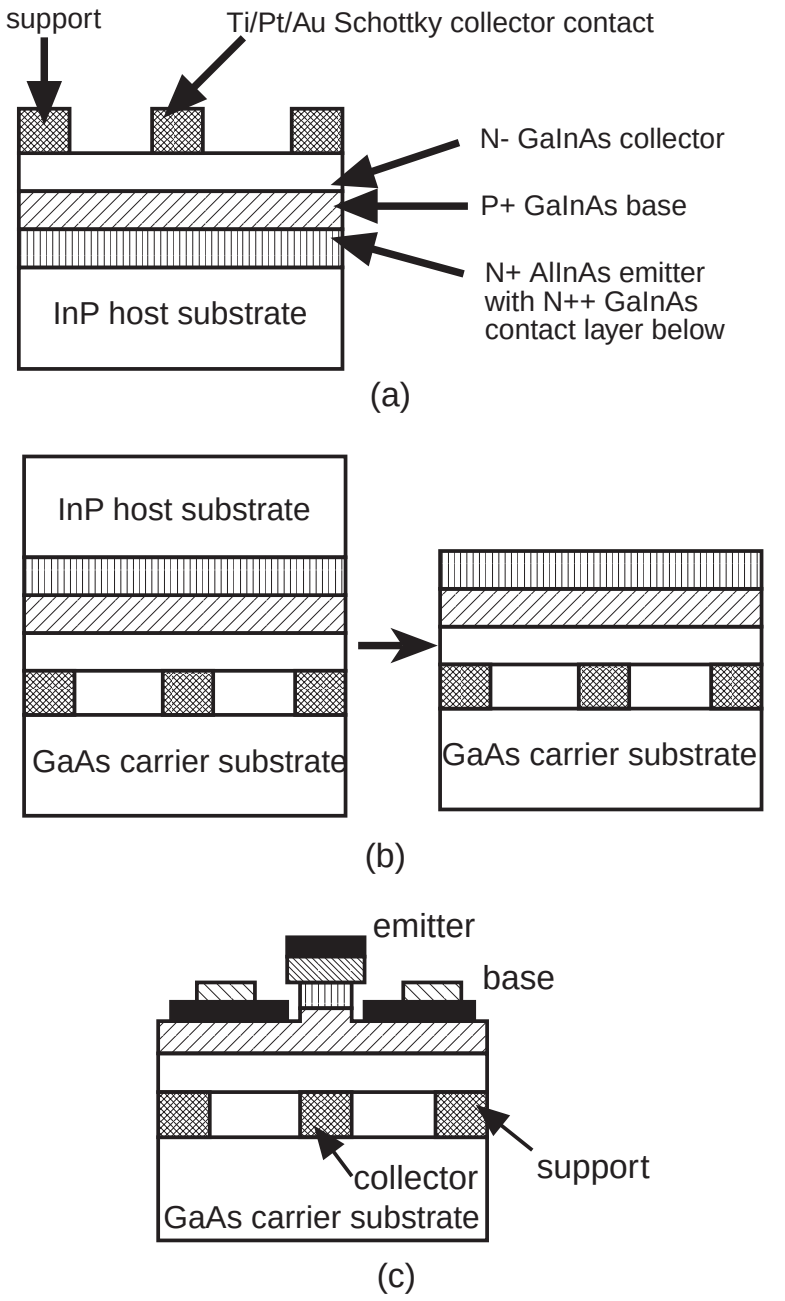


Figure 3.9: Transferred substrate HBT fabrication: (a) collector definition, (b) substrate transfer, (c) double mesa HBT process.

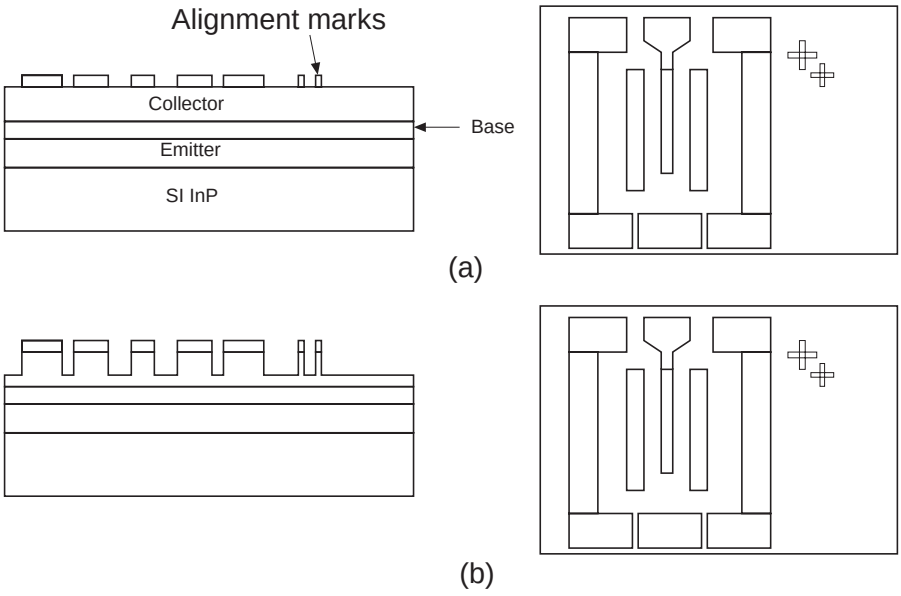


Figure 3.10: Processing on the collector side: (a) collector definition; (b) collector recess etch.

piece, slightly smaller in dimensions, is placed over it. The GaAs piece is moved around to ensure that the epoxy completely fills up the space between the two wafers without any voids.

The combination of the InP and the GaAs wafer is then transferred to the bonding fixture whose cross-section is shown in figure 3.11. The bonding fixture is a vacuum chamber which has a metal base and a flexible silicone rubber top. A metal chuck is fixed to the metal base on which the wafer combination is placed. A dome sits on the wafer combination and is in contact with the silicone rubber top. Under vacuum, the rubber top is stretched due to the atmospheric pressure and the force is conveyed uniformly to the wafer assembly by the dome. After the evacuation of the chamber, there is a waiting period. During this time, it is expected that any air bubbles within the epoxy will be removed and the pressure will create a thin, uniform layer of epoxy between the two substrates.

The epoxy is cured through a thermal cycle. A hot plate is used for this purpose. The rise in temperature is limited to prevent stresses from building up in the wafer assembly due to the mismatch in the thermal expansion coefficients of the two substrates and the epoxy layer. The cooling process after the thermal cycle is done gradually to prevent sudden contraction of any material. Vacuum

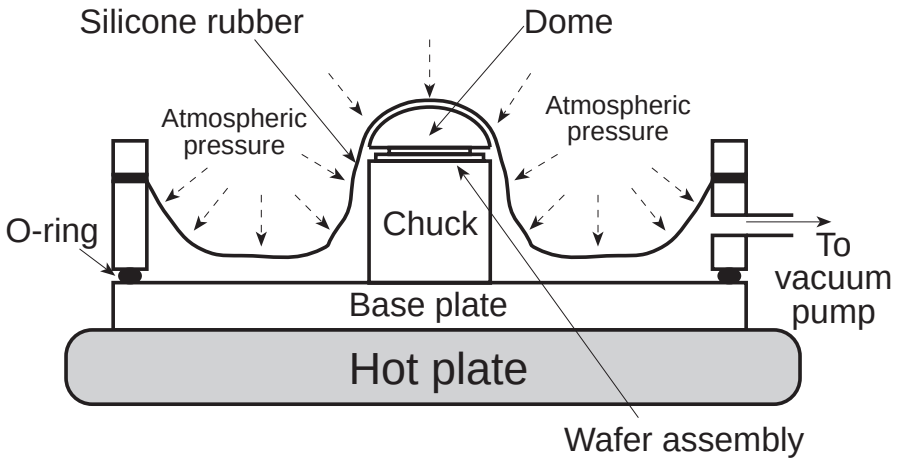


Figure 3.11: The bonding fixture.

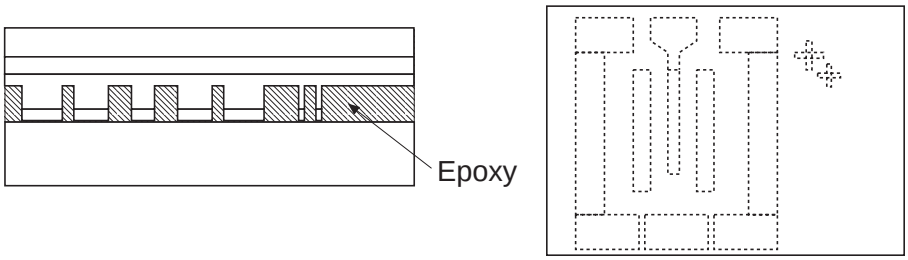


Figure 3.12: Substrate transfer.

is not broken till the wafer assembly has cooled down to the room temperature.

At this point, the InP substrate is removed selectively in a aqueous solution of HCl. The InAlAs buffer layer (shown in figure 3.1) is also removed by the same etch. This etch stops very selectively on the InGaAs emitter cap layer. The wafer cross-section at this stage is illustrated in figure 3.12.

Certain precautions are necessary to ensure a good quality of epitaxial film at the end of the substrate transfer process. All surfaces should be flat and cleaned of particles. Large particles and non-flat surfaces cause non-uniformity in the applied pressure and cracks are likely to appear on the epitaxial film. When the wafer assembly is under pressure, epoxy will squeeze out from the sides. The back of the smaller GaAs wafer will be coated with a thin layer of epoxy. This is tolerable, but the reverse situation where epoxy coats the back of the InP wafer

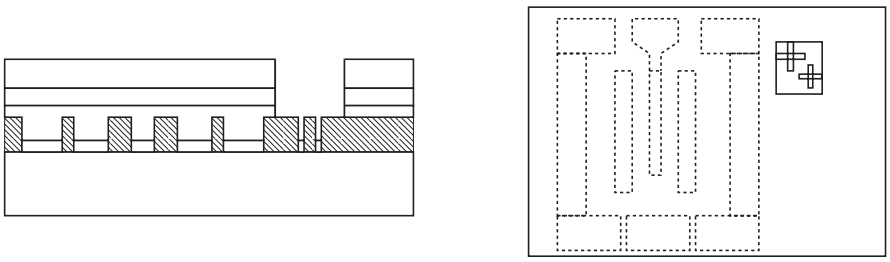


Figure 3.13: Exposing alignment marks.

is not acceptable. It is difficult to remove cured epoxy and this could lead to unsatisfactory removal of the InP substrate. It is necessary to remove the InP substrate cleanly. Subsequent to substrate removal, a critical step to define the emitters using fine contact-lithography has to be performed.

Following the substrate removal step, the alignment marks that were defined in the collector contact layer are exposed by etching vias through the transferred epitaxial film. This is necessary because the subsequent structures (e.g. emitter contacts, base contacts etc.) have to be aligned to the collector. The epitaxial layers cover the alignment marks before vias are etched. A normal aligner cannot be used to locate them. An infrared (IR) aligner with backside illumination is used. Infrared light passes through the GaAs substrate and the epitaxial layers and is imaged by an infrared camera. The metal pattern from the collector contact step is thus visible by contrast. The epoxy layer scatters some light and the image of the metal pattern is not sharp. However, this mask step for defining the vias, has a large alignment tolerance. After patterning photoresist, vias are etched down to the alignment marks. The condition of the wafer after this process step is illustrated in figure 3.13.

3.2.3 Self-aligned emitter-base process

With the alignment marks accessible, the subsequent lithographic steps can be performed. The first step is the definition of the emitter contacts. Good alignment between the emitters and the collectors is essential. After the definition of the emitter contacts, a self-aligned emitter-base process is performed.

The emitter mesa is defined by a combination of dry and wet etches. Ti/Pt/Au/Si is lifted off during the definition of the emitter contact. Si acts as the mask protecting the emitter contact metal from sputtering during the dry etching of

the emitter layer. A combination of $CH_4/H_2/Ar$ gasses is used for dry etching through the InGaAs cap layer and partially through the InAlAs emitter. The intensity of a laser beam reflected from the etched surface is monitored. The trace is an unique signature dependent on the layer structure of the material. Hence, it is an accurate tool to decide the end-point of the dry etching process. The end-point is reproducible from run to run. After the completion of dry etching, any remaining Si on the emitter contact is removed by CF_4 plasma.

A selective wet etch is next performed. The etchant etches InAlAs with a large selectivity compared to InGaAs. This is a timed etch used to define the amount of lateral undercut desired under the emitter contact. Since this etch is selective on the basis of Al versus Ga content of the material, it stops at a point in the graded emitter-base junction where the Ga content becomes large enough. The vertical distance etched is small compared to the desired undercut. Over-etching therefore occurs in the vertical direction. This has the beneficial effect of making the surface uniform by removing any non-uniformity left behind by the dry etch. An uniform surface very close to the base is thus exposed. A short, timed, and non-selective etch is used next to reach the base.

The combination of dry and wet etches used to define the emitter mesa has several benefits. The wet etch that follows the dry etch removes damage in the semiconductor due to the dry etch process. The selective wet etch stops accurately near thin base layers. A controlled undercut of the emitter mesa is possible, as opposed to an excessive undercut in a completely wet etched process. This comparison is shown in figure 3.14. The process of defining the emitter mesa with a combination of dry and wet etches, as described above, was developed by R. Pullela and Q. Lee.

Next, the base contact (Ti/Pt/Au) is evaporated. Negative photoresist and a light field mask is used for base contact lithography. The thickness of the deposited metal is kept small ($\sim$ 1200 Å) to ensure a clean break with the emitter contact metal. The condition of the wafer, at this stage, is shown in figure 3.15.

The metal liftoff processes for the emitter and the base contacts required careful consideration. The emitter contact structure should have a large aspect ratio so that it can be planarized and airbridge contacts to the emitter can be fabricated. (The airbridge process will be described in a subsequent section.) A large aspect ratio requires a tall metal structure and hence, a tall photoresist profile. If the photoresist profile has an undercut as in figure 3.16(b), the evaporated metal will extend to the point where the undercut in the photoresist meets

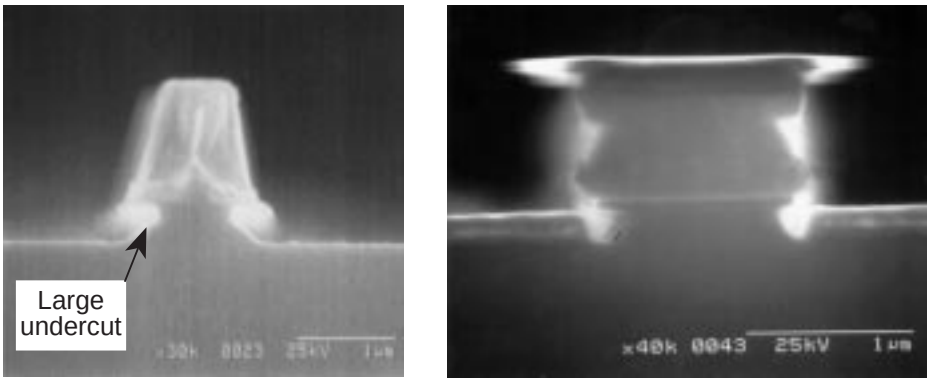


Figure 3.14: Cross-section of the emitter-mesa undercut: (a) large for a completely wet etched process; (b) small for a dry and wet etch combination.

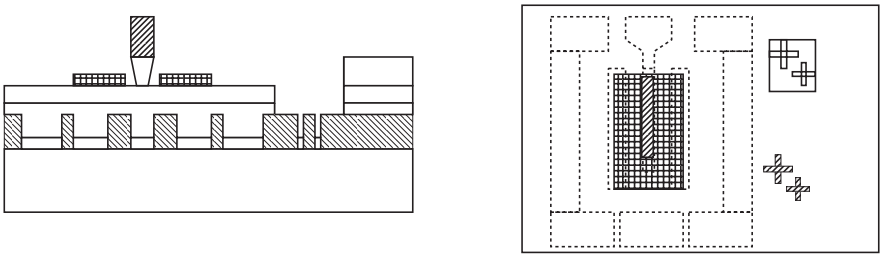


Figure 3.15: Self-aligned emitter-base structure.

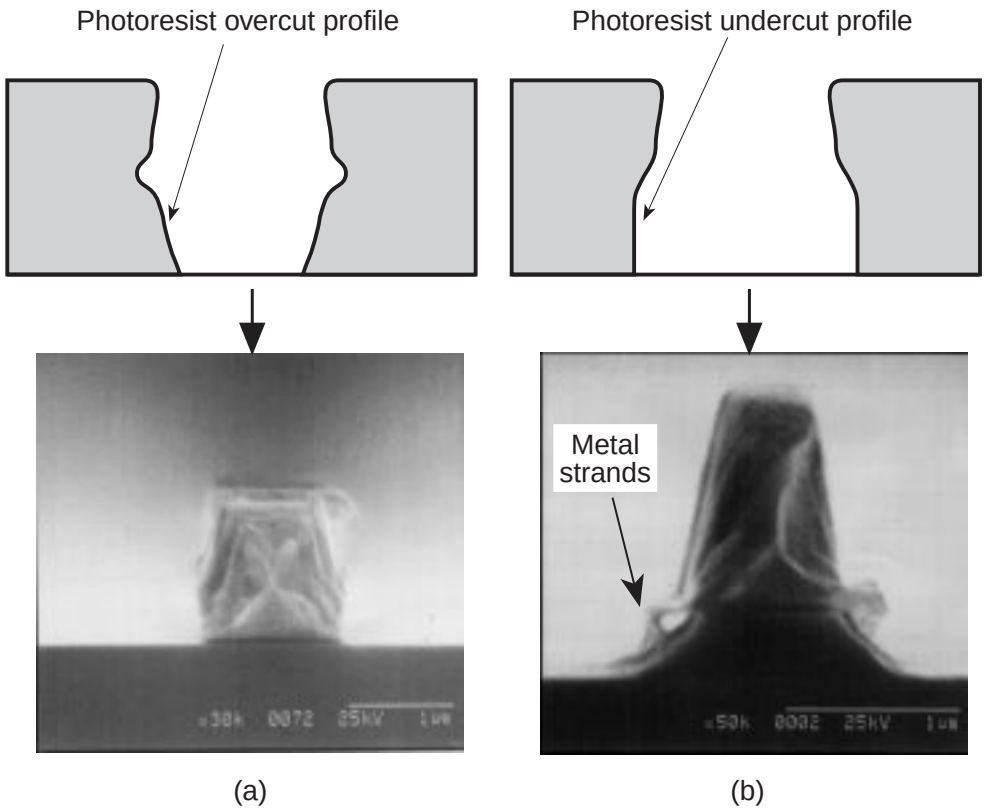


Figure 3.16: The cross-sections of emitter contact profiles: (a) desirable photoresist profile with overcut; (b) undesirable photoresist profile with undercut.

the wafer surface. Around the tall emitter contact which is defined by the gap on the top of the photoresist profile, a thin layer of metal will exist on the wafer surface to the extent of the undercut. This thin layer of metal, upon fabrication of the emitter mesa, will hang down in strands (shown in figure 3.16(b)) and create a short with the base contact metal deposited self-aligned to the emitter. To avoid the metal strands, the photoresist profile for the emitter contact should have an overcut as shown in figure 3.16(a).

Shorts between the emitter and base contacts were also found to occur if positive photoresist was used to define the base contacts. Photoresist within the emitter undercut will remain unexposed. Unexposed positive photoresist will not be removed during photoresist development. This unwanted photoresist smoothes out the otherwise overhanging emitter metal profile and allows base-

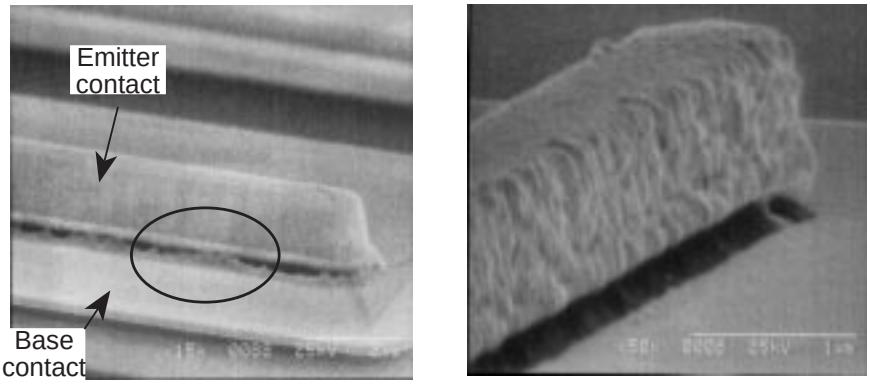


Figure 3.17: (a) Unclean break at the base-emitter edge when positive photoresist is used. (b) Clean break with negative photoresist.

emitter shorts to form during the metal evaporation for the self-aligned base contacts. This is shown in figure 3.17(a). The problem is eliminated by using negative photoresist as shown in figure 3.17(b).

A base contact very close to the emitter mesa edge is a site for electron recombination and hence, may lead to poor current gain. It might therefore be necessary to space the base contact away from the emitter mesa edge by a short distance. If this distance is large then base resistance increases through the introduction of a gap resistance R_{gap} (described in chapter 2).

A self-aligned emitter-base process, which controls the amount of spacing between the self-aligned base contact and the emitter mesa, will be described next. This process was used during some early HBT runs. It is not presently used, but will be described because of potential future value in deep submicron HBT fabrication.

The emitter contact is first planarized using a thick photoresist combined with a O_2 plasma etch-back. This is done prior to the emitter mesa etch with the emitter cap still in place. The emitter cap is used as a continuous conducting layer to electroplate the tops of the exposed emitter contacts. By controlling the plating rate and duration, the width of the plated top can be precisely controlled. When plating is complete, the photoresist is removed. The emitter contact is then T-shaped with the T-top fabricated self-aligned to the T-bottom. The steps of this process and the final structure are illustrated in figure 3.18.

Frequently, T-gate processes use electron-beam lithography because there is

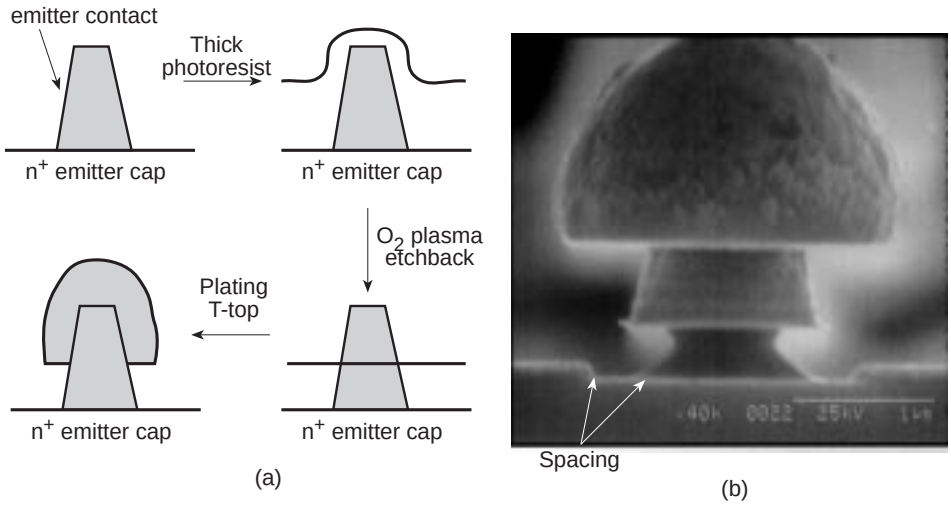


Figure 3.18: (a) Sequence of steps for T-emitter formation. (b) Final structure showing the spacing between the base contact and the emitter mesa.

a tight alignment tolerance between the T-bottom and the T-top. This self-aligned method requires no tolerance and hence, sophisticated lithographic tools are not required. Yet, controlled overhangs in the deep submicron range can be obtained. The overhang determines the spacing between the base contact and the emitter mesa.

The T-shaped emitters are not currently used because the process described above is suitable if the emitter mesa is completely wet etched. The dry etch process that is currently used would create an emitter mesa of the size of the T-top, which is undesirable. A modified sequence of steps that would make this process compatible with the current technique of etching the emitter mesa is as follows: deposition of the emitter contact, the emitter mesa etch, the emitter contact planarization, blanket sputtering of a continuous conducting metal film, planarization of the emitter contact again to expose the emitter top, generating the T-top by electroplating, and the removal of all the planarizing layers and the sputtered metal layer.

3.2.4 Device isolation and ohmic contact sintering

Devices are isolated by etching through the base and the collector epitaxial layers down to the epoxy surface. This is illustrated in figure 3.19. The emitter region

is protected by photoresist during this etch and the base contact defines the size of the base mesa. All semiconductor around the base contact is removed exposing the pad structures laid down during the deposition of the collector contacts. Figure 3.20 is a scanning electron micrograph of a device at this stage.

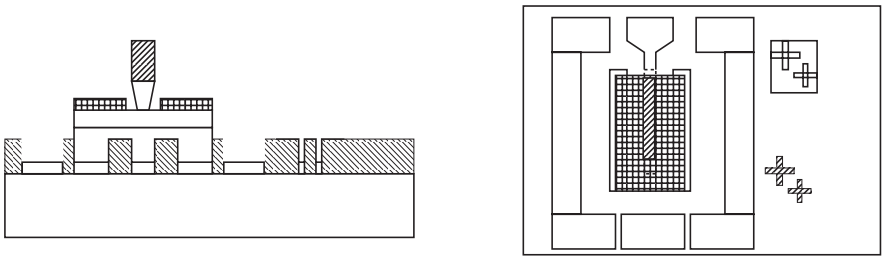


Figure 3.19: Device after isolation.

Ohmic contacts can be sintered after device isolation. A complete film has been found to crack if subjected to the thermal cycle required for sintering the ohmic contacts (300 °C for 1 minute), in a rapid thermal annealer. The device isolation step relieves strain in the film by removing most of the epitaxial film, leaving a few isolated islands in the form of the base mesas. Sintering after the isolation etch maintains the integrity of the devices.

3.2.5 Contact structures

In the remaining process, structures that connect the emitter and the base contacts to the probe pads are fabricated. Additional metal is deposited on the pad structure defined in the collector step to make them suitable for contact probing. Electroplated airbridges are used to connect the emitter finger and the base contact to the respective pads. In the first step of the airbridge process the device is planarized using a combination of polyimide and thick photoresist. The polyimide-photoresist combination is etched in a O_2 RIE, with a laser monitor used to monitor the etch-back depth. The etching is stopped when the top of the emitter fingers are just exposed. This condition is correlated with the interference pattern produced by the laser beam interacting with the polyimide-photoresist layers. Following planarization, a standard electroplated airbridge process, with two masks to define the airbridge posts and spans, is used to provide contacts to the HBT emitter and base.

Device fabrication is complete at this point. This is a 9 mask, 12 step process.

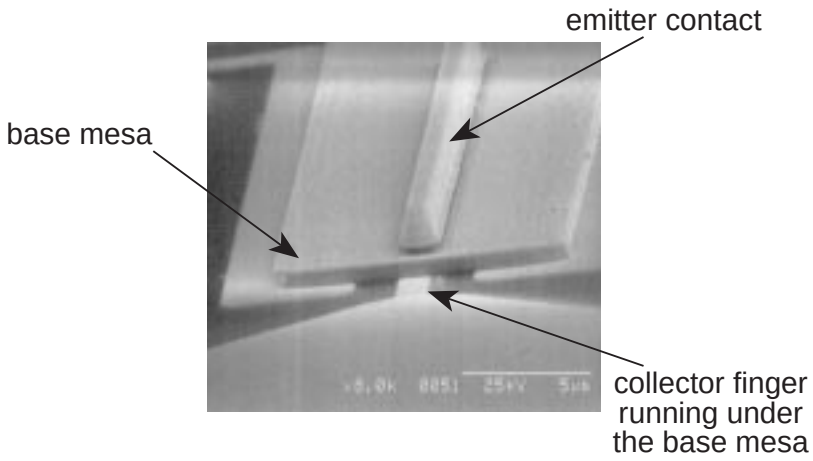


Figure 3.20: An SEM of a device after isolation.

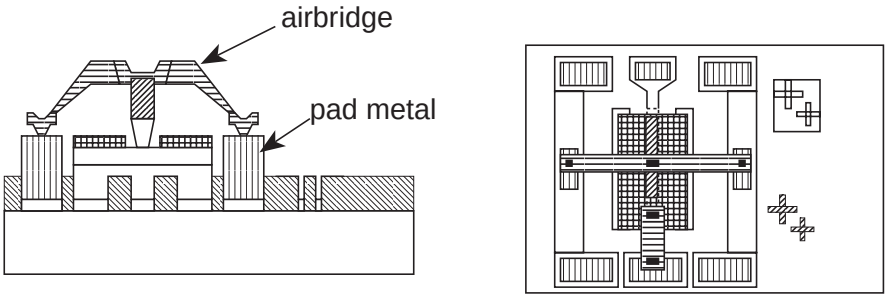


Figure 3.21: The completed device.

The completed device is schematically shown in figure 3.21. A scanning electron micrograph of a completed device is shown in figure 3.22 and a cross-section is shown in figure 3.23. Figure 3.24 shows a top-view and figure 3.25 shows an array of devices.

The fabrication of HBTs with similar layer structures, but without the epitaxial transfer process, has been described in [31].

3.2.6 Mask design and test structures

The contact mask aligners presently used in this process have large alignment tolerances (1 - 2 μm). Such contact aligners are seriously out of date; a modern projection lithography system can define 0.25 μm features at $\sim$ 300 Å registration

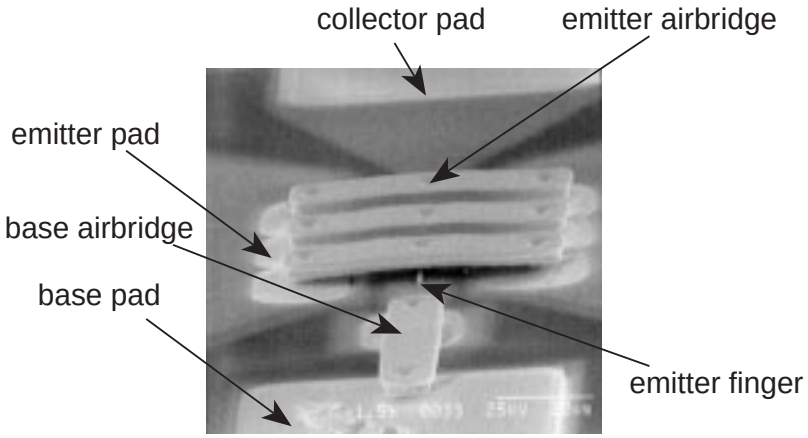


Figure 3.22: An SEM of a completed device.

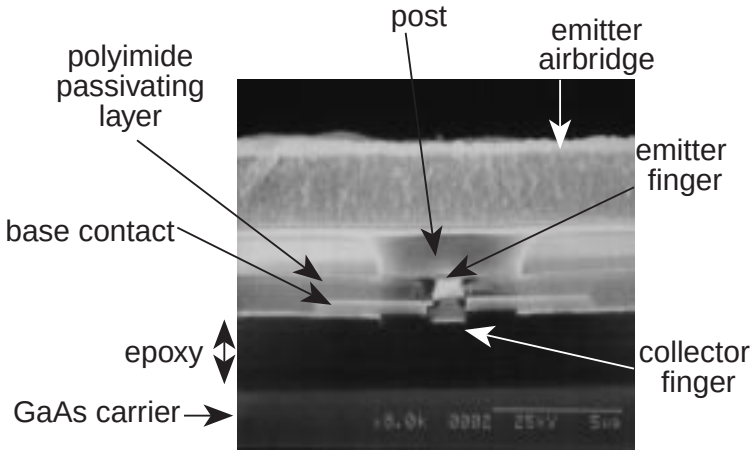
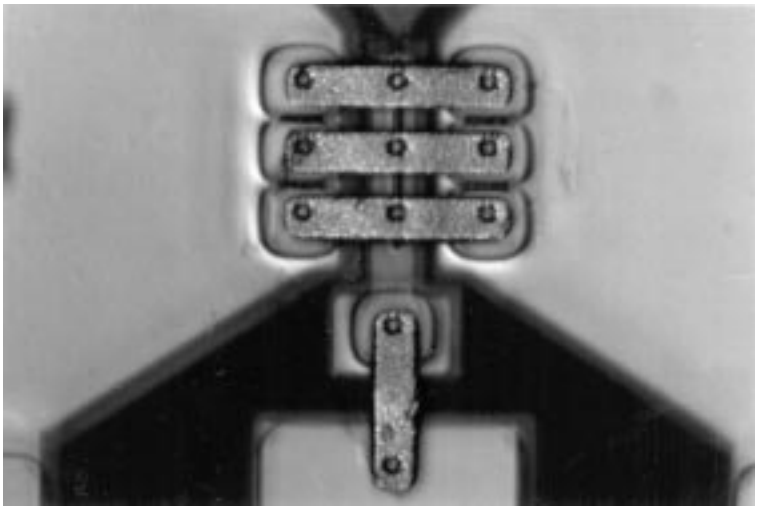
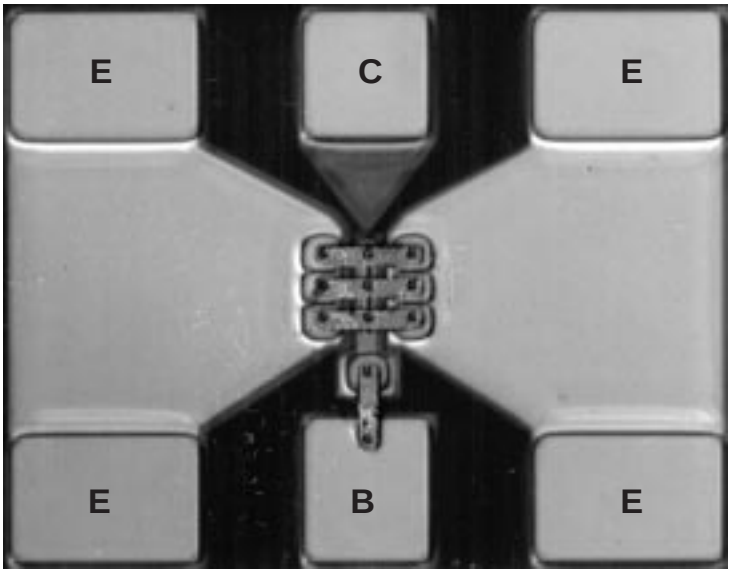


Figure 3.23: An SEM of a cross-section of a completed device.



(a)



(b)

Figure 3.24: (a) Top view of a completed device. (b) Device with the pads.

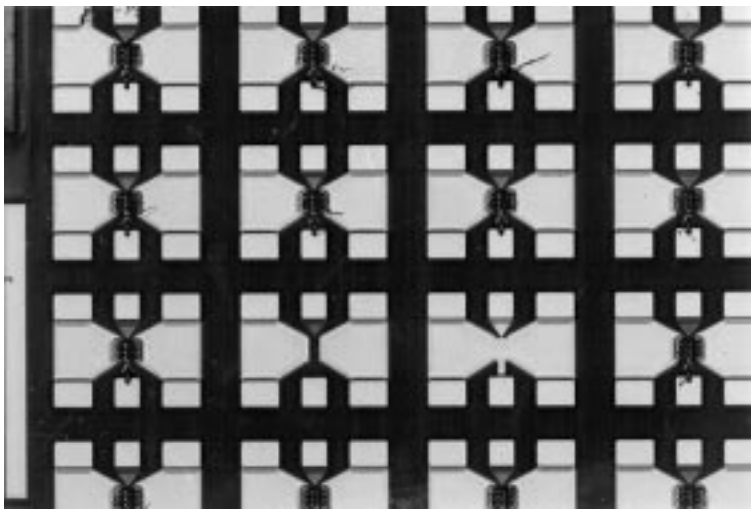


Figure 3.25: An array of completed devices.

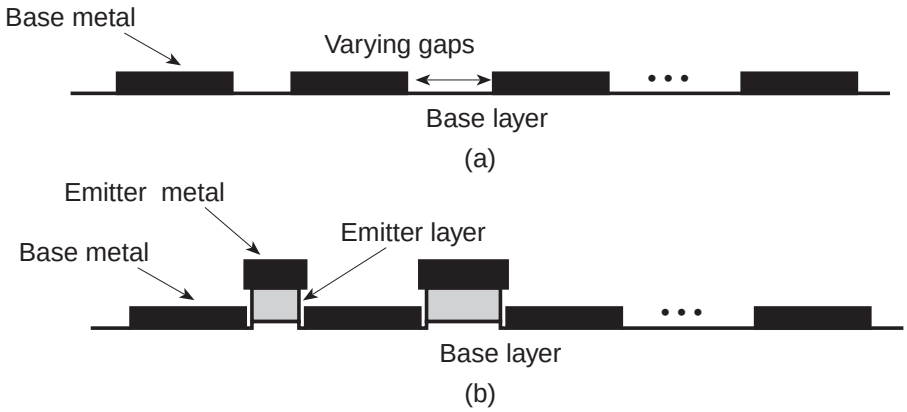


Figure 3.26: Cross-section of (a) normal base TLM structure, (b) modified base TLM structure.

tolerance. The limitations of the available lithographic tools are circumvented by staggering the emitter and collector contacts during mask design. The emitter and collector contacts are intentionally mis-aligned along a column of devices in steps of 0.5 μm over a range between $\pm$ 1.5 μm in a direction perpendicular to the fingers. Columns span in the direction parallel to the emitter/collector fingers. At least one of the devices in this range is adequately aligned and such devices are used for measurements.

Mask design also involves test structures. Large area collector-base diodes have been designed to evaluate the extent of Be movement from the base region to the collector (discussed earlier in this chapter). TLM patterns are used to determine the base layer sheet and contact resistance. A modification of the TLM structure is used to determine the extent to which the base region was etched during the emitter mesa formation. This structure is shown in figure 3.26. The modified TLMs have the emitter layer and the entire base layer in the spacings that separate the TLM contacts. The ratio of the sheet resistance obtained from this structure to that obtained from a normal base TLM gives the extent to which the base layer has been etched. It is important to know this ratio when fabricating HBTs with (300 - 500 Å) thin base layers.

Chapter 4

Results and observations

Both DC and RF measurements have been carried out on the transferred substrate HBTs. A curve tracer has been used for obtaining the common emitter characteristics. The Gummel plots have been obtained using a semiconductor parameter analyzer. The scattering parameters (S-parameters) of transferred substrate HBTs were measured on a 0-40 GHz network analyzer. F_τ, f_{max}, and other frequency dependent parameters were calculated from the S-parameters. The results of these measurements and their implications will be discussed in this chapter.

4.1 DC measurements

DC characterization included contact and sheet resistivity measurements, DC common emitter characteristics and Gummel plots. Since transferred substrate HBTs have large bandwidth (f_{max}), devices readily oscillate during DC measurements. This is avoided by using a measurement setup (figure 4.1) with shielded connections and controlled microwave impedances. Microwave probes are used to contact the devices even during DC characterization. These are coplanar transmission line probes whose center conductor connects the base or the collector and the ground connectors connect the emitter pads. The arrangement of the pads is shown in figure 3.24(b). A bias-T is used with the probes to provide isolation from the biasing/measurement sources through the inductor and termination in 50 Ω through the capacitor. In this manner the device is presented with 50 Ω source and load impedances over the microwave bandwidth. If the device is stable in a 50 Ω system, it will not oscillate during probing.

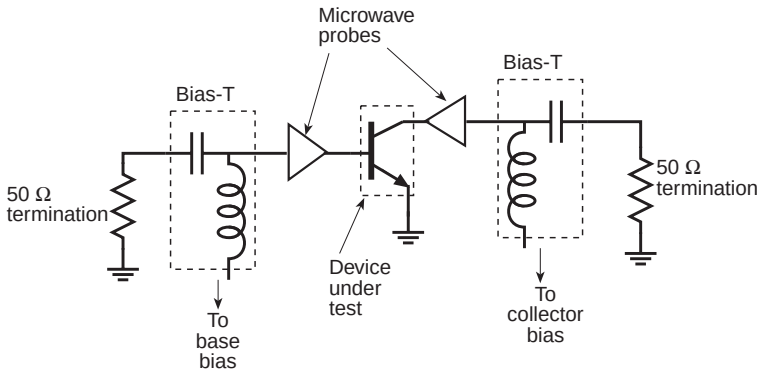


Figure 4.1: Schematic of the setup used for DC measurements.

4.1.1 Gummel plots

Gummel plots are plots of I_c and I_b versus V_{be} with the currents plotted on a log scale. The current gain β, leakage currents, ideality factors, and series resistances are readily determined from such plots. A typical Gummel plot of a recently fabricated structure is shown in figure 4.2. The collector current ideality factor is close to unity - to within the precision to which we know the device temperature. The base current ideality factor is 1.58.

4.1.2 Common emitter characteristics

Common emitter characteristics are influenced by the emitter to collector width ratio and the recess etching of the collector. The spreading of the electrons in the collector region depends on these two geometric factors. The lateral electron spreading within the collector determines the slope in the linear part of the common emitter characteristics and the saturation voltage. This is discussed below.

In figure 4.3, two bias points in the linear region of the common emitter characteristics of an HBT are chosen and the corresponding curvatures in the band structure of the collector are shown. The collector space charge layer thickness T_c is assumed not to change between these two bias points. Saturated velocity transport for electrons in the collector region is assumed with velocity $v_{\rm sat}$.

A change in the applied voltage across the space charge region ($\Delta V_{cb} = V_{cb2} - V_{cb1}$) results in a change in the collector current density required for base

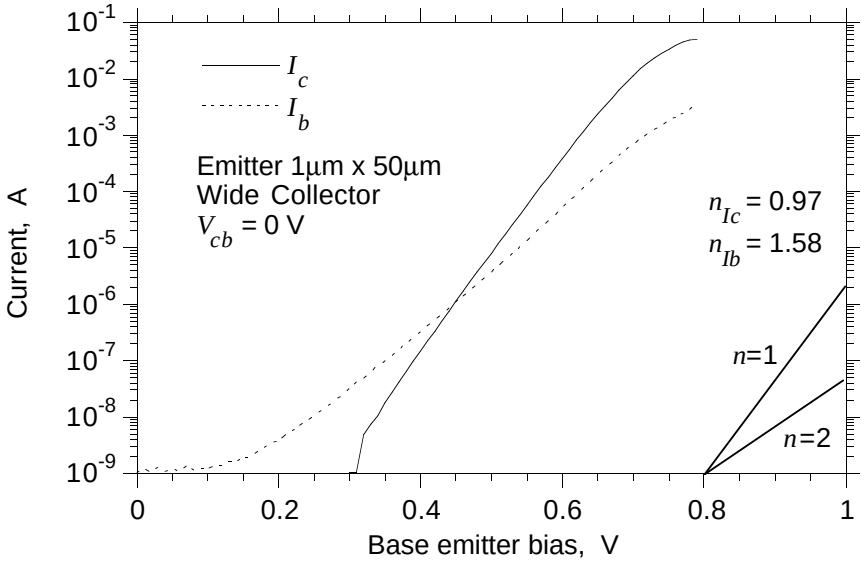


Figure 4.2: Gummel plots from a recent device.

pushout ($\Delta J_c = J_{c2} - J_{c1}$). At the onset of base pushout the DC current gain will drop, and the transistor common emitter characteristics are observed to collapse.

The curvature of the energy bands ($q\partial^2\phi/\partial x^2$) is related to the current flowing through the collector space charge region by the Poisson's equation as

$$\frac{\partial^2\phi}{\partial x^2} = \frac{J_c/v_{sat} - qN_d}{\epsilon}. \tag{4.1}$$

Here $\phi(x)$ is the potential in the collector at a distance x from the base end, and N_d is the doping in the collector. Increased voltage across the collector can support a larger curvature in the energy bands and hence (from (4.1)), a larger collector current density. Calculating the total potential drop across the collector (using (4.1)), and considering only the changes in voltage and current the following relation is obtained.

$$\Delta V_{cb} = \Delta J_c \left(\frac{T_c^2}{2\epsilon v_{\rm sat}} \right) \tag{4.2}$$

The changes in voltage and current density across the collector space charge region are linearly related. When changes in voltage and current are considered,

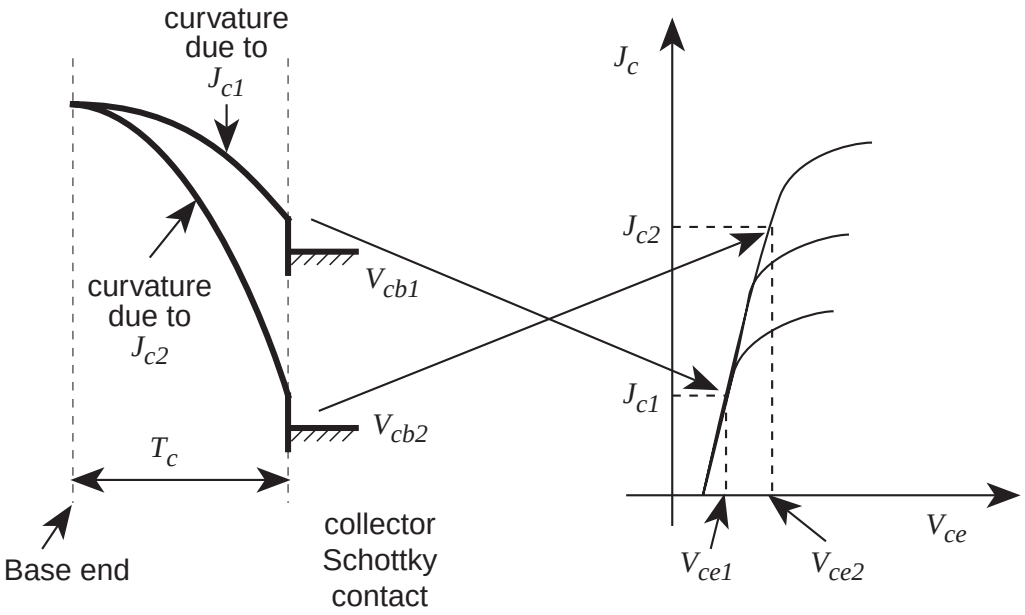


Figure 4.3: Curvature of the conduction band in the collector region at the indicated bias conditions.

the proportionality constant becomes

$$R_{sc} = \frac{T_c^2}{2\epsilon A_e v_{\text{sat}}} \tag{4.3}$$

where A_e is the emitter area (assuming that electrons do not spread laterally in the collector region). The proportionality constant has units of Ohms, and R_{sc} is termed the space charge resistance. R_{sc} determines the slope in the linear region of the common emitter characteristics, but as discussed above, it is not an Ohmic resistance.

If the electrons are prevented from spreading by recess etching the collector, and if the collector and emitter widths are equal, the area term in the above equation is indeed equal to the emitter area. Alternatively, if the emitter area is large compared to the emitter periphery, the proportion of current which has spread laterally will be small even if the collector is not recess etched. In these two cases the area of current flow in the collector is the same as the emitter area and the emitter area can be used to calculate space charge resistance.

A device with an emitter size of 1 μm $\times$ 25 μm and a recess etched collector of 1 μm width (common emitter characteristics shown in figure 4.4) has

a space charge resistance of 23.3 Ω. A device on the same wafer with a much lower emitter periphery-to-area ratio (A_e = 5 μm × 10 μm) has a space charge resistance of 12.5 Ω. The factor of approximately 2:1 in the R_{sc} values of these two devices is exactly that expected given the same ratio of their emitter areas. The saturated velocity for electrons in the collector calculated from this data is 5×10^5 m/s assuming T_c = 2700 Å. Measurements of $(\tau_b + \tau_c)$ with differing base thicknesses also allow us to determine v_{sat}, which was found to be 3.2×10^5 m/s. Approximations in the value of T_c used in these calculations is a likely cause for the discrepancy.

In figure 4.4 the common emitter characteristics of three devices with the same emitter size of 1 μm × 25 μm and collector widths of 1 μm, 2 μm, and 11 μm are shown. All of these devices have recess-etched collectors. R_{sc} decreases with larger width collectors because the electrons can spread laterally in the collector and thereby increase the effective area term that determines the resistance R_{sc}.

For narrow collector widths, the recess etched devices show smaller space charge resistance when compared to devices that are not recess etched but having the same collector and emitter widths. An example is shown in figure 4.5. Without the recess etch, electrons spread laterally into the regions where there is no collector contact underneath. The lateral spreading of the current flux is due to the presence of a large electron space charge between the collector contact and the base under high current operation. This is schematically illustrated in figure 4.6. The Coulomb repulsion between the electrons will cause the electrons to spread. Once electrons are driven laterally, the fields driving their transport back to the collector contact are small.

To further explore the saturation characteristics of devices without collector recess etches, a simulation of the electric field on the ground plane of a stripline structure (figure 4.7) has been performed. One-half of this symmetrical structure is similar to the geometry of the collector-base junction of the devices that are not recess etched. The analogy is not perfect. In the simulated stripline structure, there is a ground plane above and below the signal line and the structure is assumed to be in an uniform di-electric medium. As observed in figure 2.7, the non-recess etched collector-base junction represents a microstrip structure with the base layer analogous to a ground plane and the collector contact analogous to the signal line. The di-electric constants of the materials on the two sides of the collector contact are different. The stripline structure is used because it is easier to compute the electric fields on the ground plane of the structure and the electric field profile has a resemblance to that of a microstrip line.

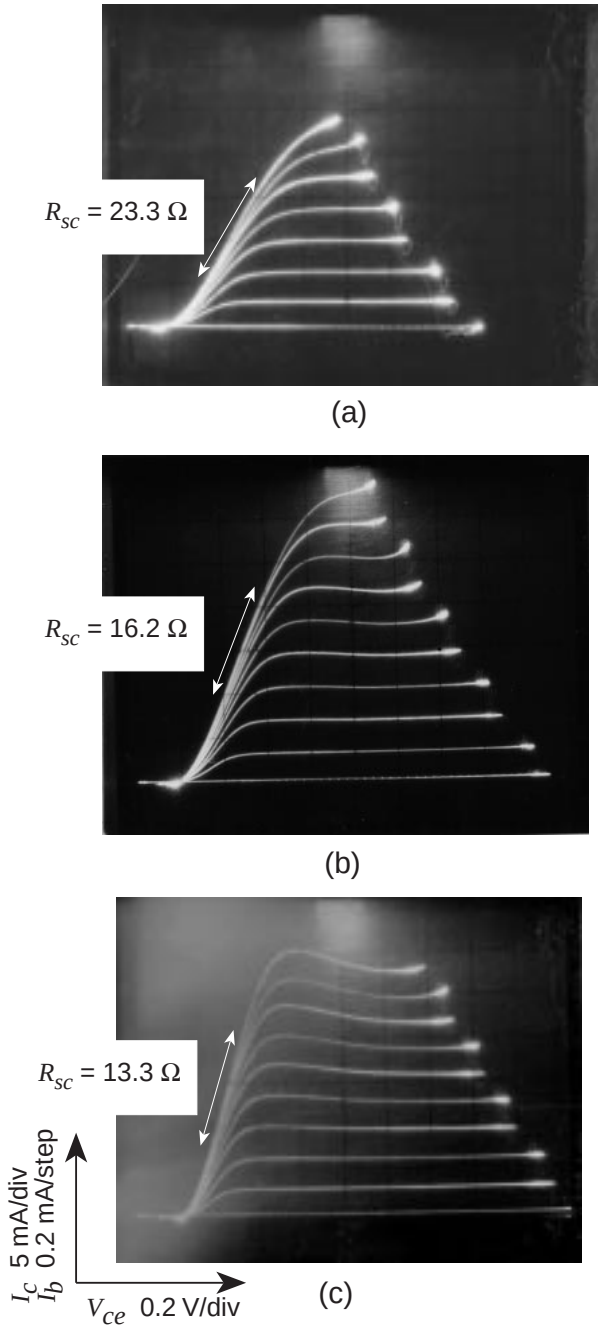


Figure 4.4: Common emitter characteristics of devices with emitter size of 1 μm $\times$ 25 μm and recess etched collectors having widths of (a) 1 μm, (b) 2 μm, and (c) 11 μm.

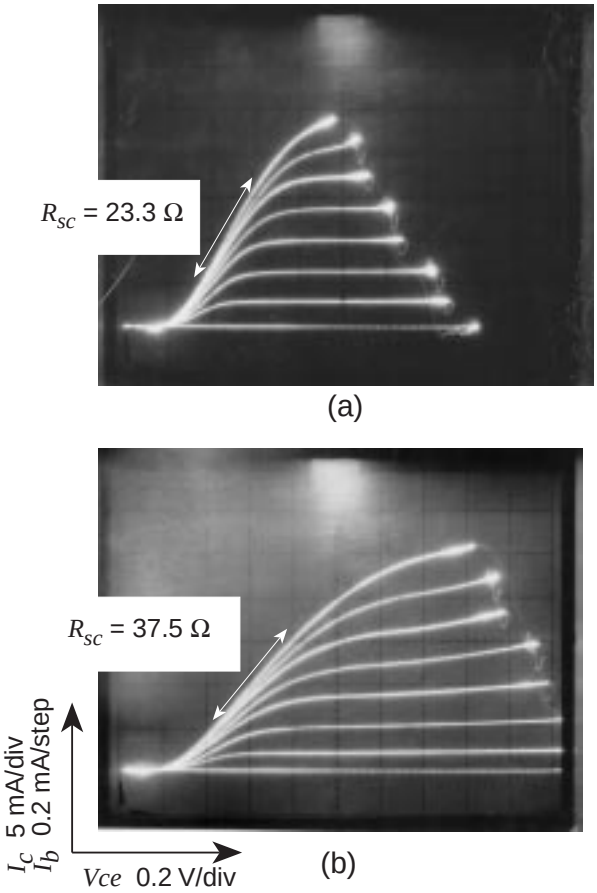


Figure 4.5: Common emitter characteristics of devices with the same emitter and collector contact widths of 1 μm. Emitter length is 25 μm. (a) Collector recess etched. (b) Collector not recess etched.

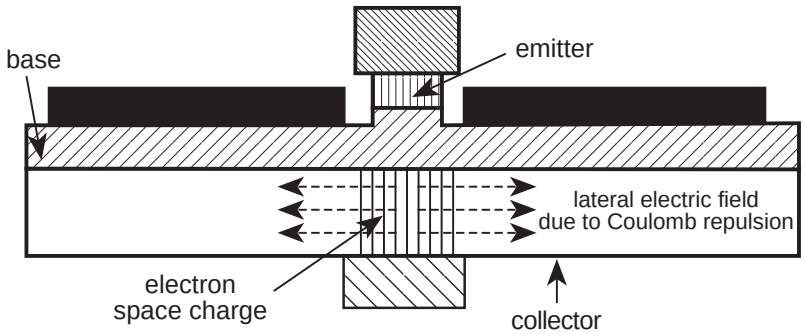


Figure 4.6: Lateral spreading of electrons in collectors that are not recess etched.

On the other hand, in recess etched collectors, the electric field is confined in the high di-electric constant material directly under the collector contact (figure 2.7). The electric field profile in such a structure is similar to the field profile in a parallel plate capacitor.

The electric field on the ground plane of the stripline structure at a point directly below the edge of the signal line (figure 4.7) is 72% of the electric field in a parallel plate structure with the same separation and same voltage across the plates. The electric field decreases further on the stripline structure at positions farther away from the signal line. The electrons not only spread in an un-recessed collector, the vertical electric field driving them towards the collector contact is also smaller. This is true for devices with equal collector and emitter widths.

In devices with collector widths of 2 μm and emitter widths of 1 μm, the lowering of electric field at the base end in the region of interest should be much less than the case of equal emitter and collector widths discussed above. The region of interest is the portion of the base layer directly under the emitter. Yet, the space charge resistance decreases significantly (27 Ω to 16 Ω) between a non-recess etched and a recess etched device. An even larger decrease in R_{sc} is observed between a non-recess etched device with a 2 μm collector width and a 11 μm collector width device. This shows that the spreading due to lateral electric fields generated by Coulomb repulsion is the dominant cause for electron spreading in the collector.

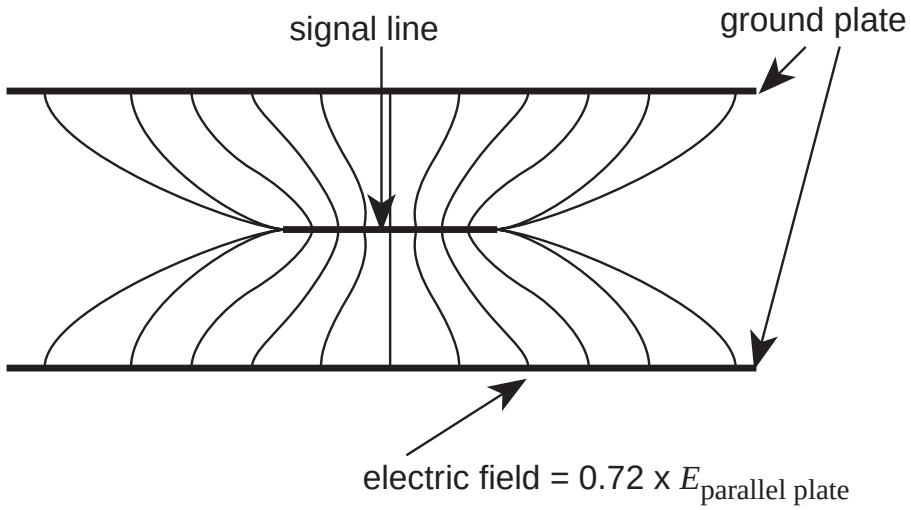


Figure 4.7: Electric fields in a stripline structure.

4.1.3 Current gain and emitter periphery-to-area ratio

Current gain (β) decreases with increasing periphery-to-area ratio of the emitter. The relation between the current gain and the emitter periphery-to-area ratio (from [32]) is as follows.

$$\frac{1}{\beta} = \frac{1}{\beta_0} + \frac{J_{B,p}}{J_c} \cdot \frac{P}{A} \tag{4.4}$$

Here β_0 is the bulk current gain when the periphery component of the current injected to the base is negligible. $J_{B,p}$ is the periphery recombination component of the base current and J_c is the collector current divided by the emitter area. P/A denotes the periphery-to-area ratio of the emitter.

Figure 4.8 shows a plot of $1/\beta$ vs. P/A. The devices considered in figure 4.8 have emitter sizes of 5 μm $\times$ 10 μm, 2 μm $\times$ 25 μm, and 1 μm $\times$ 50 μm. The layer structure of these devices is similar to that shown in figure 3.1 except that the base thickness in this case is nominally 300 Å. A linear fit is obtained to the observed β values for devices with base contacts self-aligned and non-self-aligned to the emitter. For the non-self-aligned devices there are only two data points and hence the extraction of $J_{B,p}$ is not robust.

It is observed that for the self-aligned devices the bulk current gain is 120 and the periphery recombination current density $J_{B,p}$ is 5.67 μA/μm at a J_c of 6×10^4 A/cm^2. It is also observed that the periphery recombination current for

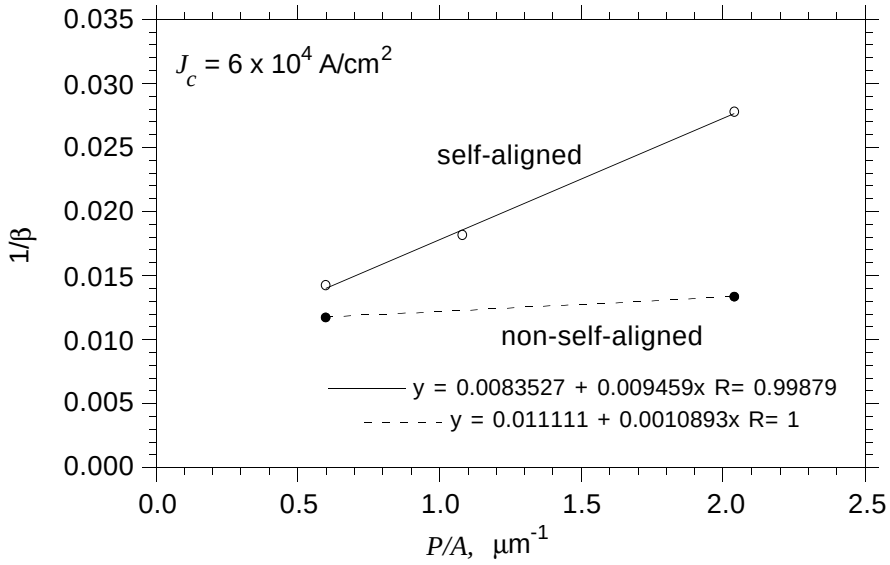


Figure 4.8: Variation of $1/\beta$ vs. P/A for self-aligned and non-self-aligned devices with a nominal base thickness of 300 Å.

the non-self-aligned devices is significantly smaller than the self-aligned devices. This is most likely due to the proximity of the base contact edge to the emitter mesa in the self-aligned devices, approximately 0.2 μm, compared to 2 μm for the non-self-aligned devices. The base contact edge acts as a site for electron recombination. Choice of appropriate spacing between the emitter mesa and the base contact edge will be an issue in further scaling of transferred substrate HBTs as was discussed in chapter 2.

Similar trends have also been observed with devices with a nominal 500 Å base thickness except that β values of both self-aligned and non-self-aligned devices were lower. A smaller base transit time in the thinner base and hence, a smaller lateral spread of the electrons in the base, is a probable reason for this observation. The fact that among non-self-aligned devices also an increase in β was observed, shows that the InGaAs base surface contributes to recombination.

Figure 4.9 shows the Gummel plots of a self-aligned and a non-self-aligned device with the same emitter geometry and fabricated on the same wafer. The collector currents of the two devices are almost indistinguishable at lower current densities. The base current of the non-self-aligned device is lower, but with approximately the same ideality factor as the self-aligned device. From this we can conclude that electron recombination at the contacts is the dominant determinant of β in the self-aligned devices. Despite this, the base ideality factor is not unity.

There is another recombination process, smaller in effect compared to the recombination at the contacts. This is observed in figure 4.10. The base currents of a self-aligned and a non-self-aligned device are compared. Both of these devices have a low periphery-to-area ratio. The non-self-aligned device shows lower ideality factor at higher currents. Therefore, there is a recombination process with lower ideality factor and whose effect can be observed when the base contacts are far away from the emitter mesa and the periphery-to-area ratio of the emitter is low. This recombination process affects the areal component of the injected current and not the peripheral component.

The highest current gains obtained with self-aligned transferred substrate HBTs have been in the range 35-40. This was obtained with devices having a nominal base thickness of 300 Å. The emitter size was 1 μm $\times$ 25 μm and the collector size was 2 μm $\times$ 29 μm. With the same emitter size, but with a narrower (1μm) collector, the current gain was observed to be lower at higher current densities. The detrimental effect of misalignment between the collector and emitter has greater effect when the collector is narrow. Also, the collector

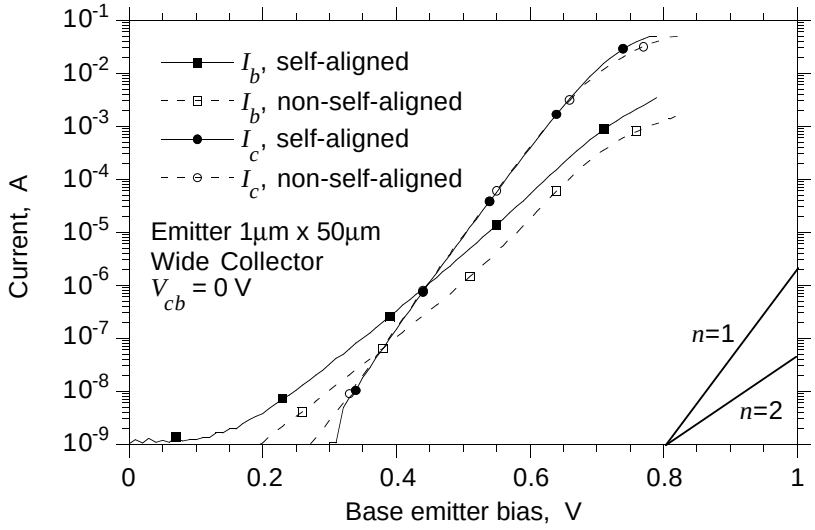


Figure 4.9: Gummel plots of self-aligned and non-self-aligned devices with the same emitter geometry.

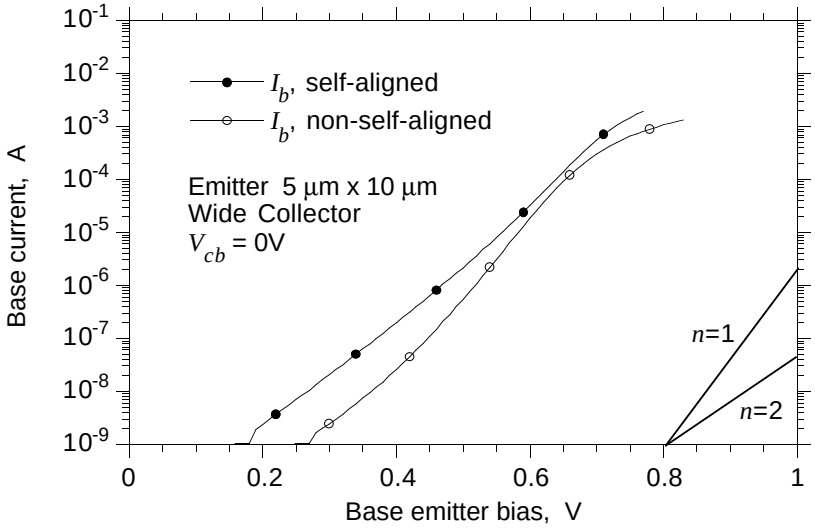


Figure 4.10: Comparison of the base currents of a self-aligned and a non-self-aligned device with low emitter periphery-to-area ratio.

current is more confined with a narrower collector. This results in a lower base pushout current threshold and hence, poorer current gains at higher currents.

4.2 RF measurements

Scattering parameter measurements were performed on a microwave network analyzer, from which a variety of secondary parameters were determined.

4.2.1 Short circuit current gain and unilateral power gain

Short circuit current gain h_{21} is defined as the AC small signal current gain of the device with the output short-circuited. The unilateral gain U (Mason's gain) is the power gain obtained from the transistor after first rendering it unilateral with a lossless reactive feedback network, and then subsequently providing impedance matches at the device input and output with lossless reactive networks. For reasonably accurate device equivalent circuit models, h_{21} and U vary as -20 dB/decade and pass through the unity gain points, the short circuit current gain cutoff frequency (f_τ) and the power gain cutoff frequency (f_{max}). Thus, h_{21} and U are useful for the extrapolation of f_τ and f_{max} respectively. The relations between the device parameters and f_τ and f_{max} are given in chapter 2 (equations (2.2), (2.3), and (2.4)).

Figure 4.11 shows the variation of the short circuit current gain and unilateral power gain with frequency for two of the best devices measured. The highest value of f_{max} obtained in this thesis work is 170 GHz with an f_τ of 120 GHz (figure 4.11(a)). This was obtained with the layer structure shown in figure 3.1, an emitter width of 1 μm, and a collector width of 2 μm. The highest value of f_τ obtained is 140 GHz with a device of similar structure and geometry except for a nominal base thickness of 300 Å. The f_{max} for this device is 165 GHz (figure 4.11(b)). Although this device has a higher value of f_τ, increased base resistance is the cause for the lower value of f_{max}. Base resistance was higher because of the higher sheet resistance due to a thinner base and also due to a higher than usual contact resistance for this fabrication run.

The onset of base pushout combined with breakdown limitations prevented f_τ from being higher than 140 GHz. The value of f_τ is limited by both emitter charging time and transit times rather than only the latter. Plots of $1/2\pi f_\tau$ vs. $1/I_c$ are shown in figure 4.13. For the device with a 300 Å base thickness it is observed that the transit times ($\tau_b + \tau_c$) equal 0.84 psec, while the emitter

charging time (τ_{ec}) is 0.3 psec at the highest current limited by Kirk effect. Thinning the base layer did not increase the device bandwidth (f_{max}) because the full benefit of the reduced transit times, as compared to the thicker base, could not be utilized.

The comparison of f_{max} values between devices fabricated on the same wafer with two different collector widths is shown in figure 4.12. This indicates that a narrow collector is effective in increasing device bandwidth. It is to be noted that the increase is less than the ratio of the square roots of the collector widths, $\sqrt{11} : \sqrt{2}$. The reason for this will be discussed in a later subsection.

4.2.2 Transit times

The sum of the base and collector transit times has been obtained from a linear fit to the data points $1/2\pi f_\tau$ plotted versus $1/I_c$. The expression (2.2), for f_τ, is the basis for this calculation. Plots for two of the best devices with 500 Å and 300 Å nominal base thicknesses are shown in figure 4.13. Among the points shown, the fit has been made to the points measured at lower collector currents leaving out a few points at higher currents. At higher currents the transit time increases due to base pushout.

The intercept of the fitted lines in figure 4.13, on the y-axis is the sum $\tau_b + \tau_c + R_{ex}C_{cb}$. With narrow collector width HBTs, C_{cb} is small and the time-constant $R_{ex}C_{cb}$ is usually significantly smaller than the sum of the transit times. The collector-base capacitance for the thicker base device has been measured to be 42 fF. Both of these devices have not been recess etched. An estimate of R_{ex} (described later) shows it to be about 2.16 Ω. The $R_{ex}C_{cb}$ time-constant is then 90 fsec. The sum of the transit times is therefore estimated to be $\sim$ 0.92 psec for the device with 500 Å nominal base thickness and $\sim$ 0.75 psec for the device with 500 Å nominal base thickness.

An estimate of the base and collector transit times can be made from the two values of $\tau_b + \tau_c$ obtained for the two different base thicknesses under the following assumptions. The base transit time is assumed to be

$$\tau_b = \frac{T_b^2}{2D_n} + \frac{T_b}{v_{sat}}. \tag{4.5}$$

The collector transit time is assumed to be

$$\tau_c = \frac{T_c}{2v_{sat}}. \tag{4.6}$$

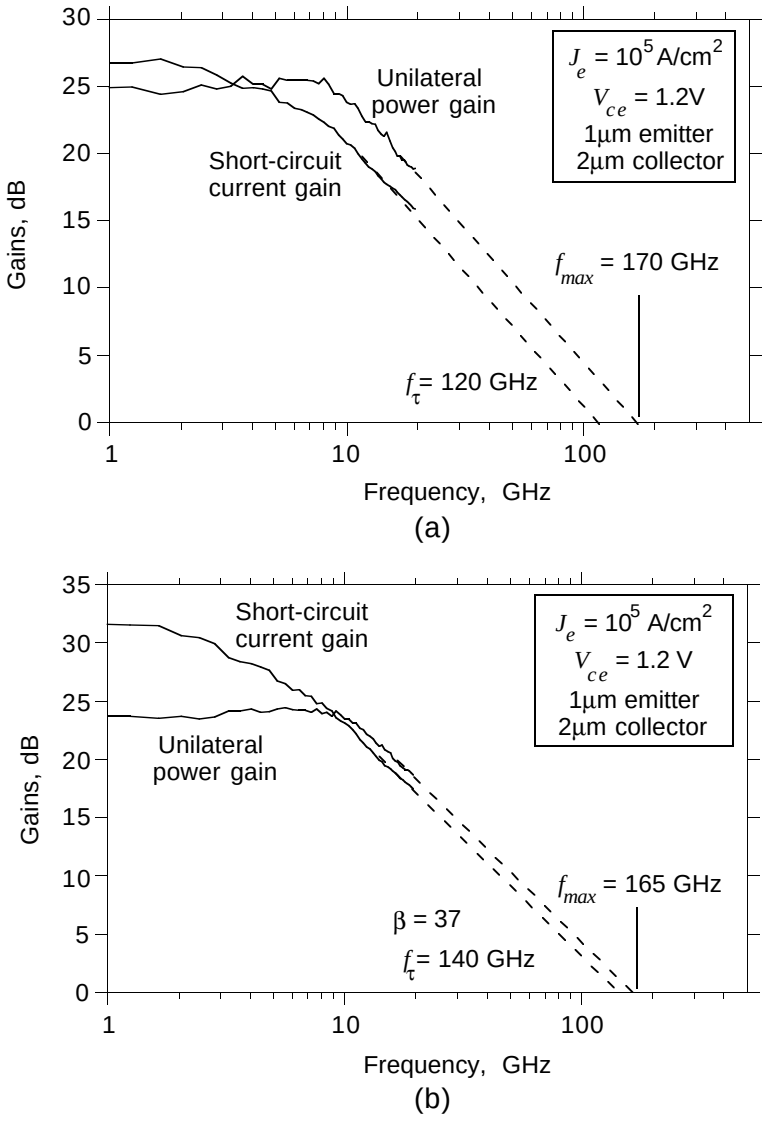


Figure 4.11: Best results obtained with transferred substrate HBTs in this thesis work: (a) highest f_{max}, (b) highest f_τ.

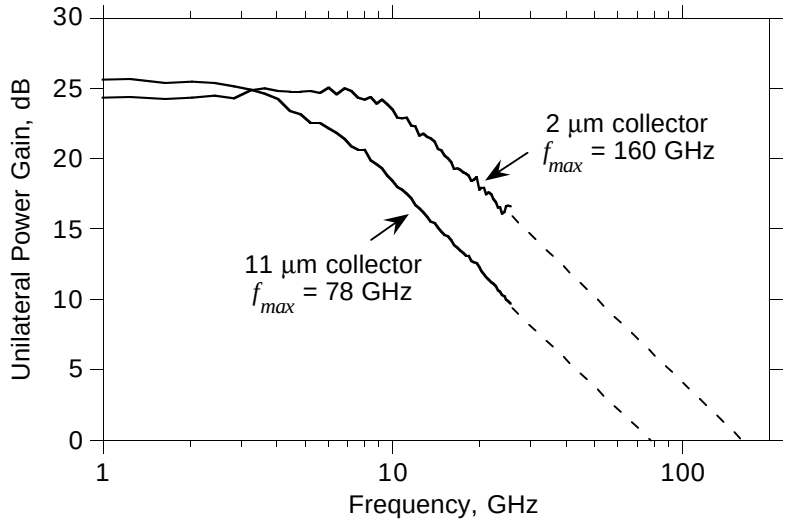


Figure 4.12: Comparison of f_{max} for devices with narrow and wide collector contacts with the same emitter geometry and same bias.

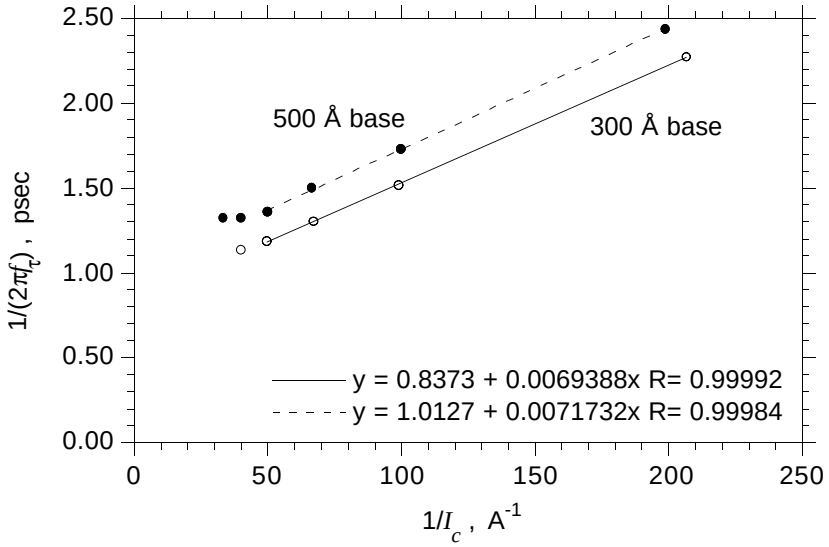


Figure 4.13: Transit times through devices with different base thicknesses. Emitter contact width is 1 μm and collector contact width is 2 μm.

The Be movement on the collector side is 300 Å and this is a part of the neutral base. The entire base region including the Be migration front in the collector is uniformly doped. Under these assumptions, the base transit time is 0.50 psec for the nominally 500 Å thick base, and 0.33 psec for the nominally 300 Å thick base. The collector transit time is 0.42 psec and the electron velocity in the collector ($v_{\text{eff}} = T_c/2\tau_c$) is 3.2×10^5 m/s.

The base and collector transit times obtained above are approximate. The transit times are sensitive to the assumptions of the base and collector thicknesses. In our case, uncertainty in the determination of the Be movement into the collector leads to uncertainty in the calculated transit times. The expression used for base transit time, $T_b^2/2D_n + T_b/v_{sat}$, is quite approximate in the case of Be outmigration because of the resulting non-uniform base doping. Unfortunately, the exact Gummel integral expression cannot be used because breakdown limits in C-V profiling prevent measurement of the full Be movement profile. The exact doping profile is required to calculate the base transit time. The expression (4.5) for base transit time may not hold where electron velocity through the base ($= T_b/\tau_b$) approaches the thermal velocity of the electrons.

The slopes of the fitted lines in figure 4.13 are proportional to the sum of the collector-base and base-emitter depletion capacitances. The slopes of the two fitted lines in figure 4.13 are similar in value. This is expected because both of the devices have similar geometry and layer structure except for the difference in base thickness. From the slope of the fitted lines and using the directly measured value for C_{cb}, the base-emitter depletion capacitance C_{be} is estimated to be 229 fF. For a nominal emitter area of 25 μm^2, the depletion capacitance per unit area for the base-emitter junction during transistor operation is 9.2 fF/μm^2.

4.2.3 Collector widths and base pushout

A narrow collector width prevents the collector current from spreading laterally. A narrower collector device will therefore have a lower collector current threshold for base pushout. In the next few paragraphs, the effect of the collector width on f_τ and f_{max} will be discussed. It will be observed that the collector width dependent base pushout phenomena is the dominant effect controlling the RF performance of transferred substrate HBTs.

Figure 4.14 shows the variation of f_τ with biasing conditions for a 1 μm and a 2 μm collector width device with the same emitter width of 1 μm. It is observed that at higher current densities and lower collector-emitter bias voltages the

device with the narrower collector width has significantly lower values of f_τ due to base pushout. At higher bias voltages and lower current densities the values of f_τ are similar in both cases.

The device bandwidth f_{max} is also strongly impacted by base pushout. Base pushout not only increases τ_b but also increases C_{cb}. The variation of f_τ and f_{max} with bias is plotted in figure 4.15. The device under consideration has an emitter width of 1 μm and a collector width of 2 μm. The inferred collector-base time-constant ($R_{bb}C_{cb}|_{\text{inferred}} = f_\tau/8\pi f_{max}^2$) is also shown. This time-constant increases with higher current densities and lower collector-emitter bias voltage as is expected in the case of base pushout.

Figure 4.16 shows that the increase in the inferred time-constant ($R_{bb}C_{cb}|_{\text{inferred}}$) is indeed due to the increase in C_{cb}. The extracted collector-base capacitance has the same nature of variation as $R_{bb}C_{cb}|_{\text{inferred}}$. The capacitance exhibits very similar variation with bias. C_{cb} is extracted from the admittance parameter Im[Y_{12}], by assuming a hybrid-π transistor model where the base resistance R_{bb} has been first de-embedded. R_{bb} can be independently found from the scattering parameter S_{11}.

The collector-base capacitance under bias for a collector width of 2 μm and 1μm is compared in figure 4.17. Both of these devices have an emitter width of 1 μm. As expected, the device with the narrower collector width shows much larger fractional increase in collector-base capacitance as compared to the device with the wider collector width. This becomes more prominent at higher current densities and lower bias voltages. Collector-base capacitances of these two devices have also been extracted with no current flowing through the collector region. The collector-base junction was reverse biased and the base-emitter junction was shorted. The values obtained were 16 fF for the 1 μm wide collector and 30 fF for the 2 μm wide collector. These values are close to those obtained for the active transistor at low current densities (figure 4.17).

The change in the inferred collector-base time-constant with bias has been found to be due to the collector-base capacitance alone. The base resistance is neither expected nor observed to change.

4.2.4 Collector widths and inferred time-constants

The inferred time-constant ($R_{bb}C_{cb}|_{\text{inferred}}$) does not increase proportionally with the collector width for wider collector devices. This observation will be discussed in the following paragraphs.

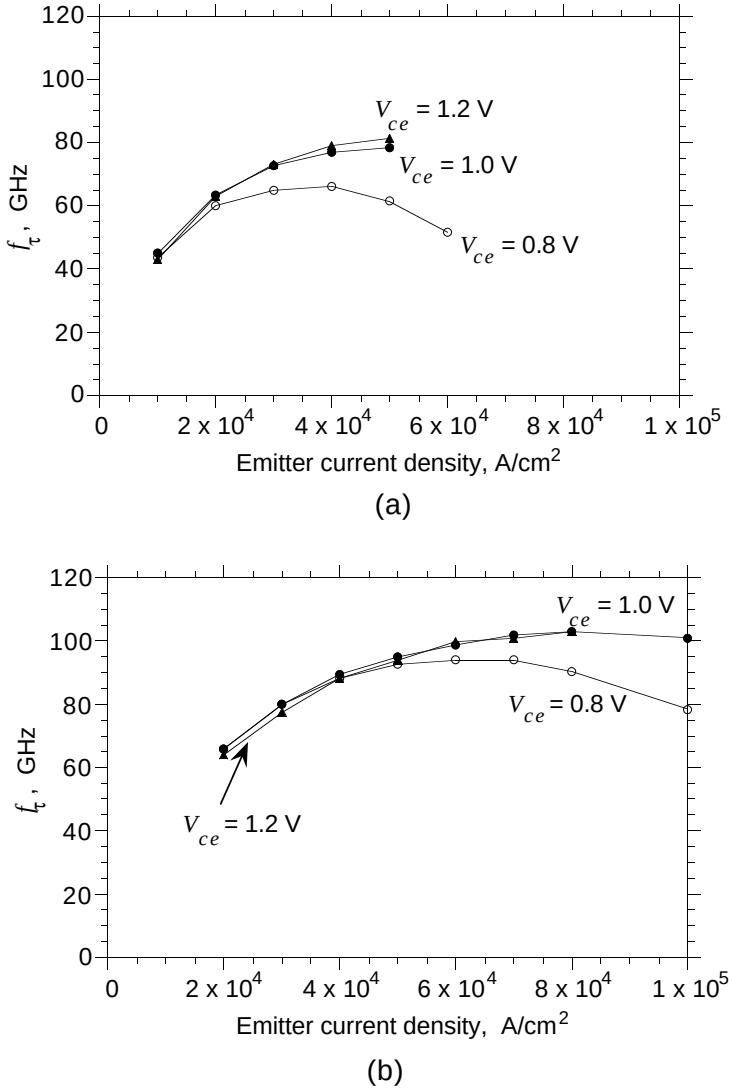


Figure 4.14: Variation of f_τ with bias for collector widths of (a) 1 μm and (b) 2 μm.

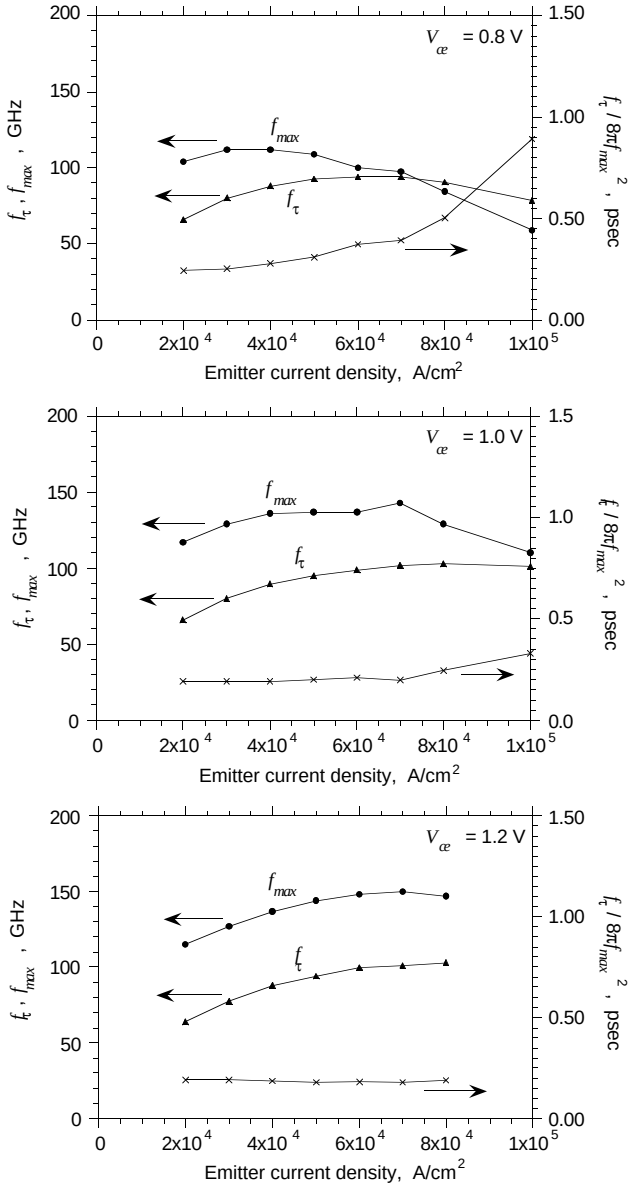


Figure 4.15: Variation of f_τ, f_{max}, and inferred collector-base time-constant with bias.

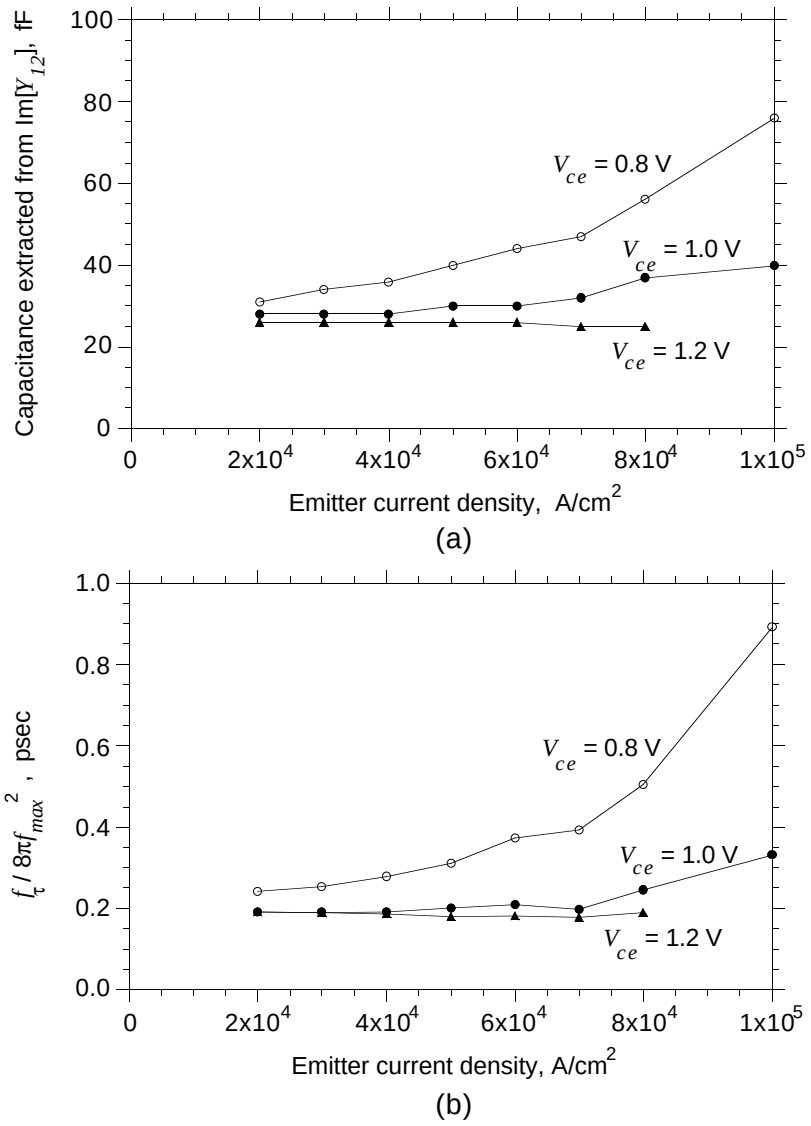


Figure 4.16: Variation with bias: (a) extracted collector-base capacitance, (b) inferred collector-base time-constant.

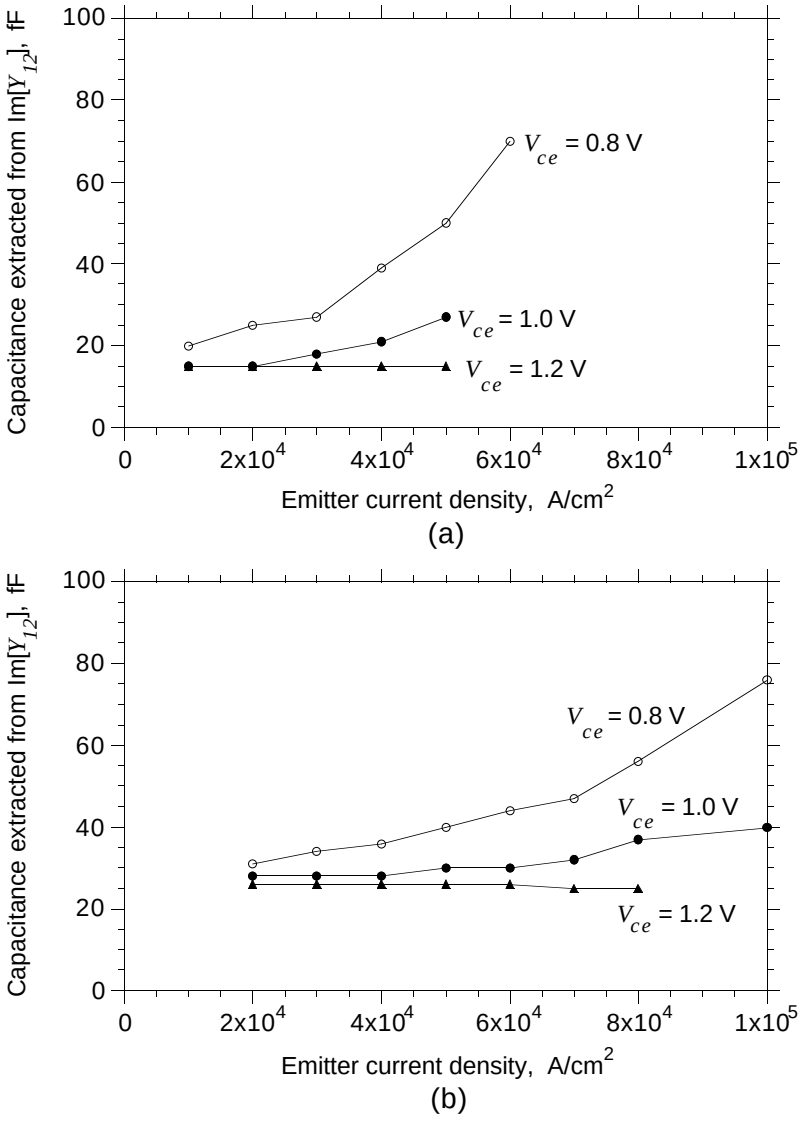


Figure 4.17: Variation of collector-base capacitance with bias in devices with collector widths of (a) 1 μm and (b) 2 μm. Emitter width = 1 μm.

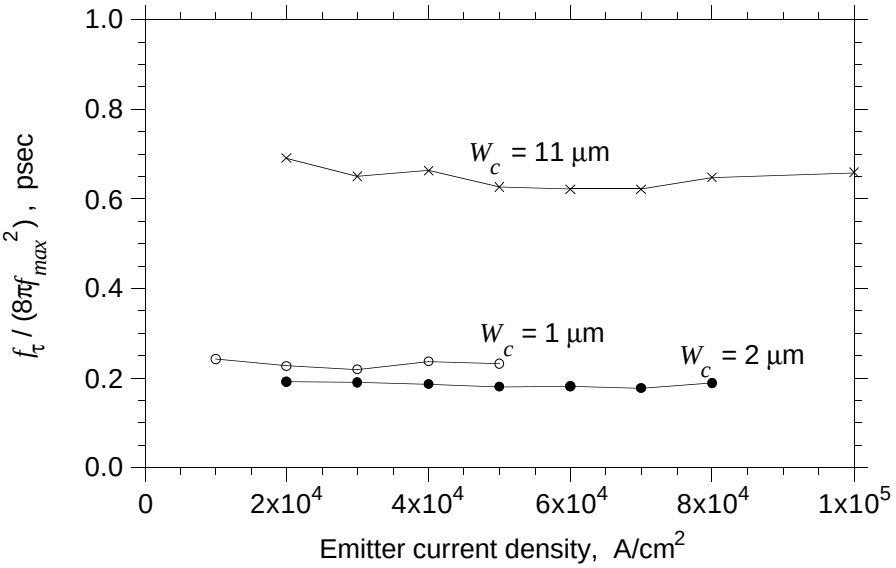


Figure 4.18: Variation of inferred collector-base time-constant with bias for different collector contact widths.

Figure 4.18 shows $R_{bb}C_{cb}|_{\text{inferred}}$ of transistors with collector widths of 1 μm, 2 μm, and 11 μm. This data is obtained under bias conditions where base pushout is not evident. Instead of increasing by the ratio of the collector widths, the time-constants increase by a smaller ratio.

The reason for the above mentioned observation is the distributed nature of the collector-base time-constant. For collectors wider than the emitter, the capacitance under the base contacts is charged by a smaller resistance compared to the total base resistance. This makes the simple hybrid-π model of figure 4.19(a) inadequate. A more sophisticated model as shown in figure 4.19(c) is required. R_{bb1}, R_{bb2}, C_{cbi}, and C_{cbx} do not correspond 1:1 with specific resistances and capacitances within the transistor structure, but instead are elements of a 4-parameter fitting to a physically distributed structure. More resistance-capacitance stages may be needed to accurately model the distributed resistance and capacitance of the base-collector structure.

S-parameters can be used to estimate the total base resistance independent of the inferred time-constant. If the model of figure 4.19(c) is assumed, then it is possible to find a frequency range where C_{be} provides a low impedance

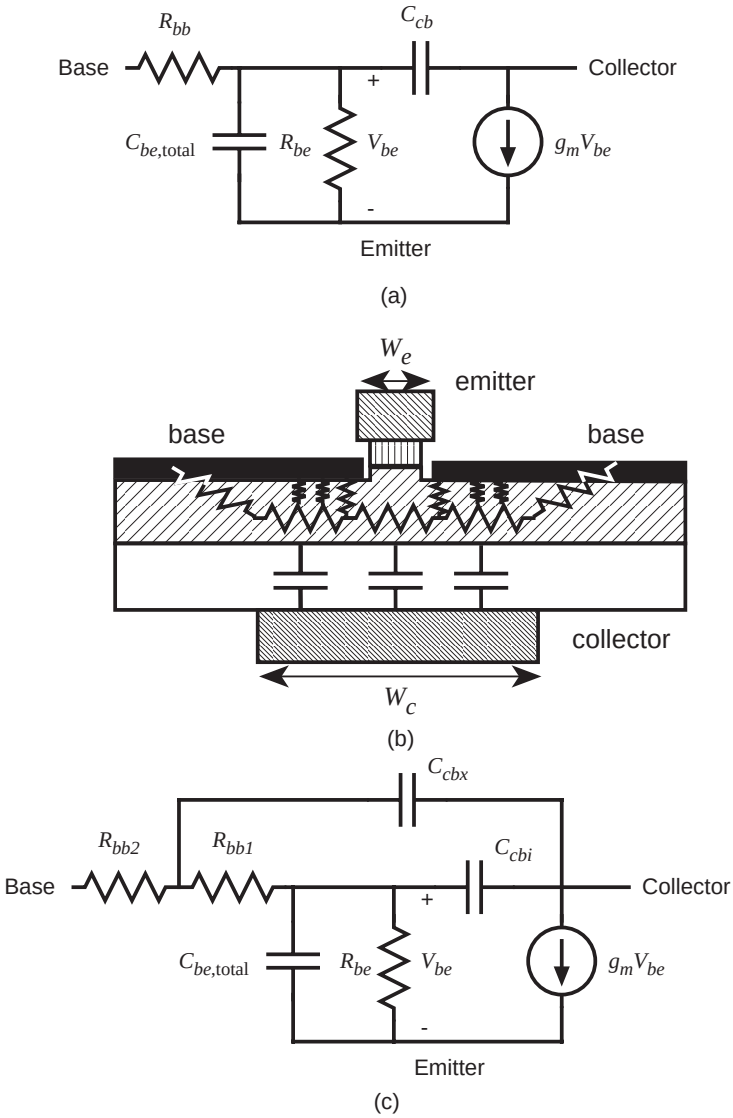


Figure 4.19: Transistor models: (a) simple hybrid-π model, (b) distributed nature of the base resistance and collector-base capacitance, (c) modified hybrid-π model to include the distributed nature of the base resistance and the collector-base capacitance for wider collectors.

and C_{cbi} and C_{cbx} provide high impedance compared to R_{bb1} and R_{bb2}. This is because $C_{be} \gg C_{cbi} + C_{cbx}$. Under such conditions, the HBT input impedance is $R_{bb1} + R_{bb2}$, and is therefore readily determined from microwave measurements. In the presence of a emitter contact resistance (not shown in figure 4.19), the input impedance is $R_{bb1} + R_{bb2} + R_{ex}$. The Smith chart (figure 4.20) shows S_{11} for 1 μm, 2 μm, and 11 μm collector width HBTs. In all cases S_{11} will intersect the resistance axis at similar values giving similar $(R_{bb1} + R_{bb2} + R_{ex})$. For example, the 2 μm device when extrapolated will intersect the resistance axis at approximately 12 Ω. The emitter contact resistance (discussed in the next subsection) has been estimated to be approximately 2 Ω. The total base resistance is therefore 10 Ω.

TLM structures (described in chapter 3) on the base layer are used for the determination of the sheet resistance of the base layer and the contact resistance of the base ohmic contacts. For the fabrication run corresponding to the devices shown in the Smith chart of figure 4.20, the sheet resistance (ρ_{bs}) of the complete base layer was 450 $\Omega/\Box$ and the average contact resistance (R_{contact}) was 500 Ω-μm. For the emitter contact of size 1 μm $\times$ 25 μm, the spreading resistance ($= \rho_{bs} W_e / 12l$) is 1.5 Ω and the contact resistance ($= R_{\text{contact}}/2l$) is 10 Ω. The total base resistance is therefore 11.5 Ω, which is close to the value of 10 Ω obtained from the S_{11} measurements discussed above.

Let us consider the S_{11} traces of the device with the 11 μm wide collector and the device with the 2 μm wide collector in the Smith chart of figure 4.20. The similarity in the S_{11} traces can be easily noticed. The input impedance and hence, the base resistance of these two devices are therefore similar. The ratio of the inferred time-constants (figure 4.18) is less than 11:2. Therefore, the inferred time-constant of the devices with wider collectors does not increase in the same proportion as the collector width because the resistance charging the extrinsic part of the collector-base capacitance is lower.

There is some discrepancy in the S_{11} traces between the device with a collector width of 1 μm and the device with a collector width of 2 μm. This is most likely due to the variability of base contact resistance or emitter contact resistance across the wafer.

It is has been the observation over several fabrication runs, that for an emitter width of 1 μm, devices with collector widths of 2 μm have significantly larger bandwidth (f_{max}) than devices with collector widths of 1 μm. The discussion in the above paragraphs provide reasons for this. The penalty in terms of increased inferred collector-base charging time-constant goes up less than 2:1 for the wider

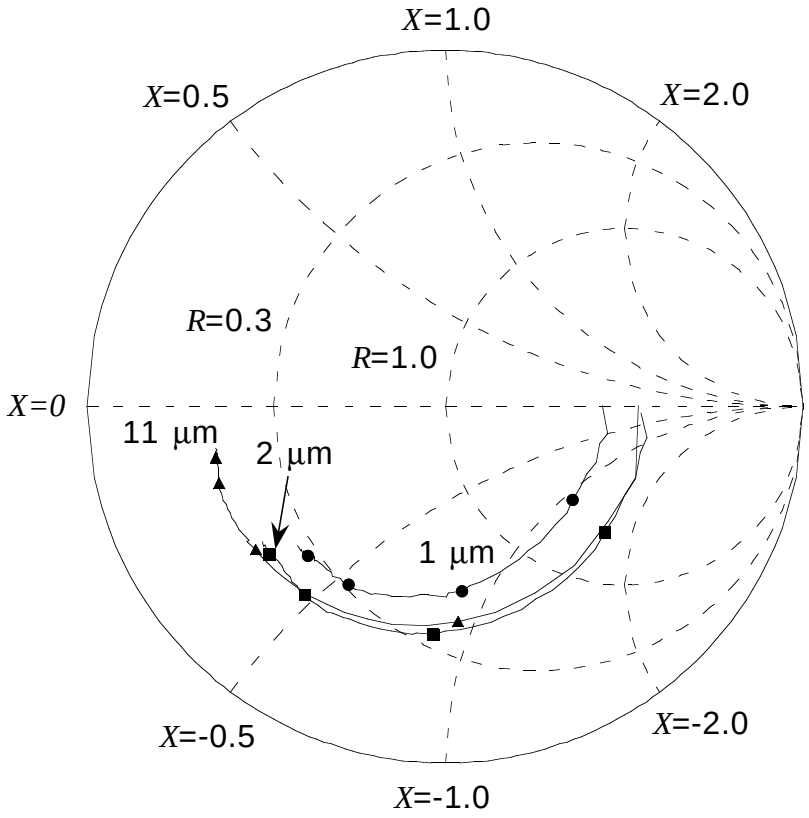


Figure 4.20: Variation of S_{11} with frequency for different collector width devices having the same emitter width of 1 μm. Bias conditions: $I_c = 5$ mA, $V_{ce} = 1.2$ V.

collector. At the same time, the base pushout threshold current is higher for wider collector devices and significantly better f_τ values can be obtained. The optimum emitter to collector width ratio appears to be close to 0.5. More experiments with varying ratios around 0.5 are needed to arrive at the exact optimum. Further scaling of the emitter and collector widths, maintaining this optimum ratio, can then be conducted to improve bandwidth. If along with lateral scaling, the vertical scaling of the layer structure is not undertaken, then the ratio has to be re-optimized to account for electron spreading in the collector for deep submicron scaling.

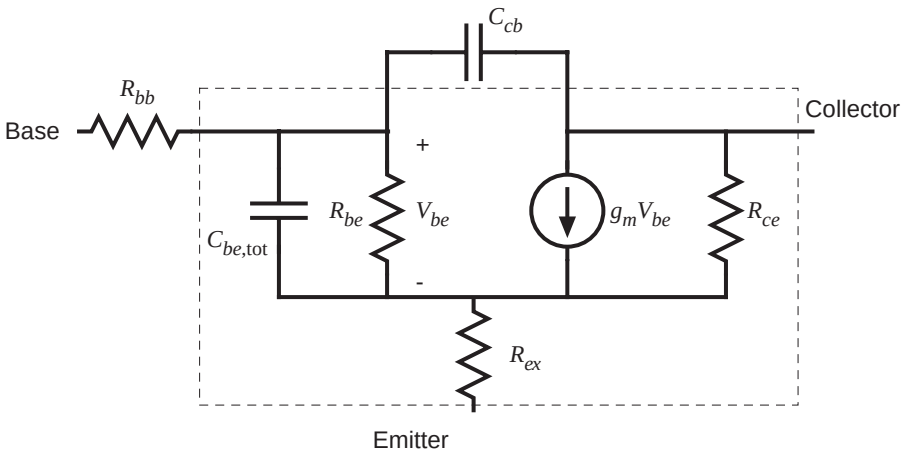
Recently fabricated transferred substrate HBTs by B. Agarwal, with emitter and collector widths of ~ 0.7 μm and ~ 1.5 μm respectively, have shown f_{max} of approximately 280 GHz with f_τ of approximately 130 GHz. The inferred time-constant is significantly less for these devices compared to the value reported for a similar geometry device in figure 4.18. Investigation of the reasons for this low value of inferred time-constant may lead to a new optimum emitter-to-collector contact width ratio.

4.2.5 Emitter resistance

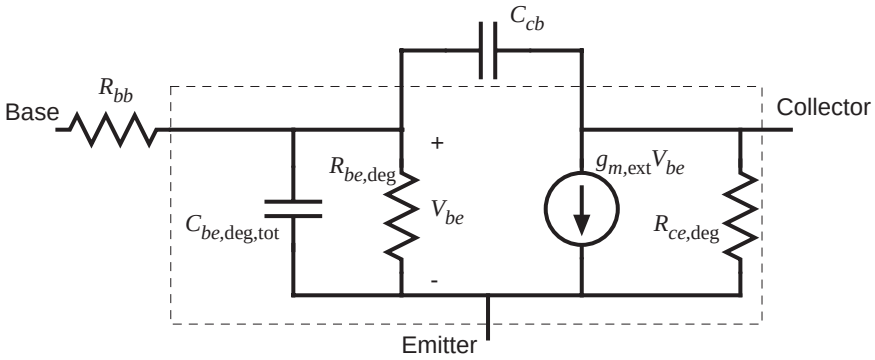
The hybrid-π model of the transistor inclusive of the emitter resistance R_{ex}, can be converted to an equivalent hybrid-π model with degenerate values of the parameters. This conversion is valid for frequencies $f \ll f_\tau$, $R_{ex} \ll R_{be}$, and $R_{ex} \ll R_{ce}$. If R_{bb} is subtracted from the modified equivalent circuit then mag$[Y_{21}]$ gives the degenerate transconductance $g_{m,\text{ext}}$ of the equivalent circuit. The equivalent circuits are shown in figure 4.21. The relation between $g_{m,\text{ext}}$ and g_m which involves R_{ex} is as follows:

$$\frac{1}{g_{m,\text{ext}}} = \frac{1 + g_m R_{ex}}{g_m} = \frac{kT}{qI_c} + R_{ex} \tag{4.7}$$

where $g_m = qI_c/kT$. The estimated R_{bb} is subtracted from the measured S-parameter model of the circuit and mag$[Y_{21}]$ is extracted from the resultant. The latter is plotted against $1/I_c$ and the plot is shown in figure 4.22. The intercept on the y-axis of the line fitted to the data points gives the value of R_{ex} which is found to be 2.16 Ω. Assuming a nominal emitter area of 25 μm^2, the emitter contact resistance is 54 Ω-μm^2.



(a)



(b)

Figure 4.21: Hybrid-π equivalent circuit: (a) with R_{ex} explicitly, (b) effect of R_{ex} included in degenerate component values.

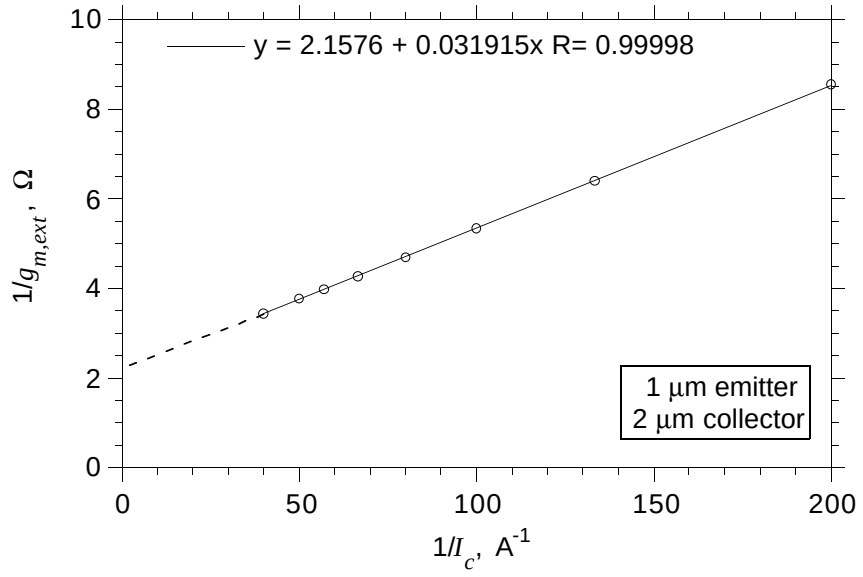


Figure 4.22: Estimation of R_{ex} from the variation of $g_{m,\text{ext}}$ with I_c.

4.3 Equivalent circuit

An equivalent hybrid-π model for a transferred substrate HBT is shown in figure 4.23. This corresponds to an emitter size of 1 μm $\times$ 25 μm and a collector contact size of 2 μm $\times$ 29 μm. A collector current of 15 mA is assumed which results in an emitter current density of 6×10^4 A/cm^2. At this bias point $g_m = qI_c/kT \simeq 0.6$ S. The current gain β is approximately 22 for the modeled device and $R_{be} = \beta/g_m \simeq 37\ \Omega$. The transit times $(\tau_b + \tau_c)$ for this device was found to be 1.1 psec. Therefore, base-emitter diffusion capacitance $C_{be,\text{diff}} = g_m(\tau_b + \tau_c) = 0.66$ pF. The base-emitter depletion capacitance is 0.21 pF. The base resistance as measured from extrapolated S_{11} plots is 10 Ω. The total collector-base capacitance from reverse bias collector-base diode measurements is 30 fF for this device. The inferred charging time-constant is 0.2 psec. Therefore $C_{cbi} \approx R_{bb}C_{cb}|_{\text{inferred}}/R_{bb} = 20$ fF. The balance of C_{cb} appears as $C_{cbx} = C_{cb} - C_{cbi} =$ 10 fF. The distributed nature of the collector-base resistance-capacitance time-constant has been modeled by three elements, two capacitors and one resistor. A better model of this distributed structure will have more elements and an optimizing program may be used to obtain the fitted element values. The emitter

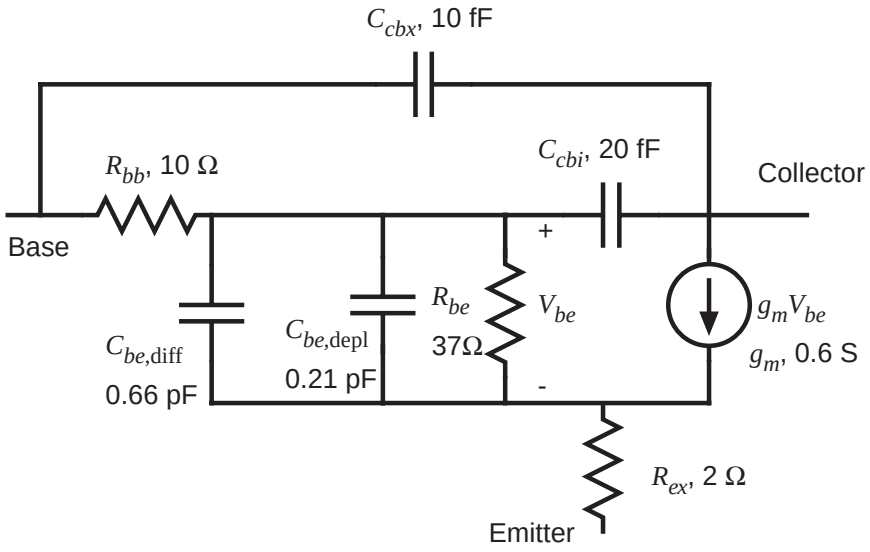


Figure 4.23: Hybrid-π model of a transferred substrate HBT with an emitter contact size of 1 μm $\times$ 25 μm, and a collector contact size of 2 μm $\times$ 29 μm, at a collector current of 15 mA.

resistance was found to be 2 Ω. Output conductance (and hence R_{ce}) could not be extracted in a robust manner and is ignored in this model.

The parameters R_{ex}, C_{cbi} and C_{cbx} are dependent on accurate extraction of R_{bb}. Since the estimate for R_{bb} is approximate, the values of R_{ex}, C_{cbi} and C_{cbx} are also approximate.

A simulation of the frequency response of the modeled circuit has been performed. The simulated and the measured values of S_{11} and h_{21} show good correlation. There is significant discrepancy between the simulated and the measured values of the other S-parameters and U. This is because of the inability to extract the output conductance in a robust manner. Only the quantities that are mostly dependent on the input side elements of the model, in the frequency range of measurement, have shown good correlation between the simulated and the measured values. In the -20 dB/decade rolloff region of U, the measured and modeled values match. Since h_{21} also shows good correlation, the extrapolated values of f_{max} and f_τ for the equivalent circuit are similar to the measured values.

Chapter 5

Conclusion

5.1 Achievements

Transferred substrate HBTs have been fabricated in the InAlAs/InGaAs material system. A complete fabrication process for demonstration devices has been developed. This includes the critical process of substrate transfer. The substrate transfer process is required for gaining access to both the emitter and collector sides of the epitaxial film. This access is essential for fabricating lithographically defined emitter and collector contacts aligned to each other.

The typical geometry of transferred substrate HBTs allows both the collector and emitter contacts to have a large periphery-to-area ratio. It has been shown that, with collector contacts having a large periphery-to-area ratio, there is a large reduction in the (base-resistance)(collector-base capacitance) time-constant and a consequent increase in the device bandwidth f_{max}. The geometry of the transferred substrate HBTs also results in a scalable device. The scaling law for transferred substrate HBTs has been derived. Device bandwidth increases as the inverse square root of the emitter or collector contact width.

The demonstration devices show encouraging performance in terms of device bandwidth. Low inferred collector-base charging time-constant values demonstrate the effectiveness of the narrow collector contacts in transferred substrate HBTs. An f_{max} value of 170 GHz was obtained for devices fabricated as a part of this thesis work. In an extension beyond this work, B. Agarwal has obtained transferred substrate HBTs with an f_{max} value of approximately 277 GHz.

The effect of narrow collector geometry on device performance has been investigated. It has been observed that the lateral spreading of electrons in the

collector region has significant influence on both DC and RF performance of transferred substrate HBTs. It is concluded that an optimum emitter to collector width ratio exists for maximum device bandwidth.

The base ohmic contact is a site for significant recombination and has a degrading effect on current gain. This has been demonstrated by comparing devices with self-aligned and non-self-aligned emitter-base structures. The placement of the base ohmic contact with respect to the emitter mesa will be important in deep submicron scaling of transferred substrate HBTs.

Material growth experiments have been conducted in association with Dr. M.J. Mondry and Dr. L. Samoska. The purpose of these experiments were to characterize the movement of Be from the base region, towards the emitter and the collector. Modifications to the device layer structure have been made during the course of this thesis work and significant improvement in device performance has been obtained. Lowering base transit time and improving DC current gain were the goals of the growth experiments in this work. The first reported transferred substrate HBT had a f_τ of 22 GHz and a DC current gain of 2.7. The best f_τ obtained in this work is 140 GHz and a DC current gain of 37 for the same device.

Approximate element values for modeling transferred substrate HBTs have been extracted from device measurements. A preliminary hybrid-π transistor model has been presented.

5.2 Future work

5.2.1 Integrated circuits

One immediate goal is to build integrated circuits. The required process must be highly different from that of this thesis. Work on this process has been in progress for the past twelve months and has so far yielded high performance devices.

One of the prime concerns for ICs is heat dissipation. In the device cross-section shown in figure 3.23 it is observed that there is a layer of epoxy several microns thick between the device and the GaAs substrate. It has been shown by J. Guthrie that epoxy is a very poor conductor of heat compared to the conventional semiconductor substrates. A high device density IC process will require better means of heat dissipation.

The final size of the epitaxial film transferred from the InP substrate to the

GaAs substrate is approximately 1 cm^2. Significantly larger areas are essential for fabricating complex ICs. Techniques for transferring normal wafer size epitaxial films have to be incorporated in the fabrication process. Such processes are in commercial use for the purpose of transferring epitaxial films containing finished ICs on to better thermally conducting substrates.

Lithographic tools better than the contact aligners used in this work are needed. Since a high degree of alignment between the emitter and collector is essential, alignment tolerance of ~ 0.25 μm is required at the minimum for devices with emitter widths of 1 μm. The method of staggering the relative positions of emitter and collector contacts, to achieve good alignment for a few devices (as used in this work), is not suitable for a high yield IC process. Electron-beam lithography or steppers will be required.

Large device bandwidth is obtained at higher current densities. Hence, improvement in device breakdown voltage at higher current densities will be necessary. The operating bias range of current devices between breakdown and Kirk effect threshold is small. Modifications in the layer structure which increases the threshold current at which Kirk effect occurs (e.g. the structure shown in figure 2.12) will also help in increasing the operating range of the devices.

Optimizing circuit performance and the implementation of high performance circuits depend on accurate device models. A preliminary model has been presented in this thesis. Accurate SPICE models have to be developed for use in circuit simulation programs. Uncertainty in the extraction of device parameters has been a problem. Improved extraction techniques are needed. Lesser variability in device characteristics on the same wafer and from run to run is expected to improve the reliability of the models.

5.2.2 Highly scaled high performance devices

Bandwidth of transferred substrate HBTs improve significantly under deep submicron scaling. Work is currently underway to achieve this. The primary requirement for deep submicron scaling is powerful tools for lithography. Deep submicron emitter and collector contacts will have to be fabricated by electron-beam lithography or steppers. The preferred lithography system should not only have fine linewidth capabilities (of the order of 0.2 μm) but also comparable alignment tolerances.

Enhancements in the etching processes are necessary. High resolution dry etching processes are required for the fabrication of submicron emitter and col-

lector mesas. It is expected that along with lateral scaling, vertical scaling of layer structures will be undertaken. If the base layer is made thinner, there will be increased demands on the accuracy of monitoring the etch process and on the uniformity of the etch process used to expose the base layer.

Future work will involve the incorporation of the advances in HBT technology in transferred substrate HBTs. This has been discussed in chapter 2. It is important to reduce base resistance because of its direct influence on transistor bandwidth. Regrown base structures are being considered. A regrown structure may also improve current gain by preventing the lateral spread of electrons in the base. Maintaining current gain will be an important issue in deep submicron scaling of transferred substrate HBTs. Lower electron transit times are desired. Devices with graded bandgap base layers, for the purpose of lowering base transit time, are expected to be fabricated soon. The onset of Kirk effect prevents the lowering of emitter charging time and the full benefit of low transit times is yet to be realized for the devices reported in this work. A high electric field region at the collector base junction (as in figure 2.12) can suppress Kirk effect. This is obtained by having a thin, highly n-doped depleted region in the collector adjacent to the base. The increase of collector-base capacitance due to Kirk effect is also prevented by using this structure. Such a structure has been incorporated in recent devices fabricated by B. Agarwal which show impressive device bandwidths. The emitter-base heterojunction is being re-designed to reduce emitter depletion capacitance. This should also help in reducing the emitter charging time. A wide bandgap collector has generally been reported to increase HBT breakdown voltage. There is an ongoing effort to fabricate transferred substrate HBTs with wide bandgap collectors.

5.3 Open questions

There are several open questions regarding the best way of laterally scaling an HBT. The plot showing the calculated values of f_{max} for a double mesa HBT under deep submicron scaling (figure 2.4) shows small improvement in bandwidth with emitter scaling. The calculations are based on the simple assumption that the size of the base mesa is unchanged and the entire base resistance charges the collector-base capacitance.

The base mesa may also be scaled with the size of the emitter in a double mesa HBT. The extent of the base contact around the emitter must be at least one transfer length so that the base ohmic contact resistance does not increase

significantly. With improvement in base contact technology, the base mesa size of double mesa HBTs is expected to decrease resulting in improvement in device bandwidth. On the other hand, contact structures to the base ohmic contact force a minimum size of the base mesa. This will hinder extreme scaling of the base mesa. In transferred substrate HBTs the collector base capacitance is independent of the size of the base mesa.

An emitter to collector width ratio of 1:1 has been found to be non-optimal for transferred substrate HBTs; collector width larger than the emitter width is required. Although the bandwidth levels predicted in figure 2.4 for the transferred substrate HBT should be achievable with the corresponding collector contact widths, the demand on emitter scaling will be larger. This might limit scaling on the higher bandwidth end (lower emitter dimension) of the plot. However, recent reports of transferred substrate HBTs with bandwidth near 300 GHz show that the degree of scaling required to achieve 500 GHz may be less severe than predicted in figure 2.4. Other planned improvements in transferred substrate HBT device structure should help to reduce the demand on scaling alone for increasing device bandwidth.

The penalty for wider collector contacts in terms of increased effective collector-base charging time-constant is less than proportional to the increase in the width of the collector. The part of the collector capacitance under the base contact is charged through a smaller resistance. A double mesa HBT will therefore have better performance than predicted in figure 2.4.

With similar technological improvements in double mesa and transferred substrate HBTs the device bandwidths are likely to be finally determined by the minimum size of the base mesa obtainable in double mesa HBTs and the maximum emitter-to-collector width ratio obtainable in transferred substrate HBTs without degrading high frequency performance. A thorough investigation of the spreading of electrons in the collector region and the exact extent of their impact on device characteristics will yield the optimum emitter-to-collector ratio for transferred substrate HBTs. When this is compared with the narrowest base mesa possible without significant increase in base resistance, the extent to which one gains by using a transferred substrate HBT in terms of collector width will be known. An accurate model of the distributed nature of the base resistance and collector base capacitance can then predict the extent of increase in bandwidth with the transferred substrate HBT. At that point it will be possible to decide on the best method of scaling HBTs.

Appendix A

Process flow

A.1 Collector Contacts

Mask Layer: Collector, Dark Field.

A **Wafer Cleaving**

1. Cleave InP quarter wafer to form a rectangular piece which fits the chuck to be used for wafer bonding.
2. Keep track of the major flat.

B **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.

5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

C **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.

D **Exposure**

1. Cool down after soft bake, 10 min.
2. Edge bead removal necessary.
3. Orient collector stripes perpendicular to the major flat.
4. Expose at 7.5 mW/cm^2 for 8 sec.
5. Use hard-contact (HP mode) and use O-ring.

E **Development**

1. Toluene soak: 4 min.
2. AZ 400K : DI :: 1:4
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist remains develop again in steps of 5 sec.

F **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

G **Metal Evaporation**

1. Dilute NH_4OH (1:15) dip for 30 sec. just before loading the evaporator.
2. Place wafer in E-Beam mount.
3. Make sure the crystal monitor reads < 10; change if necessary.
4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	200	2-3	1.65
Pt	500	1	1.90
Au	4300	$\sim$25	1.55
Si	250	2-3	1.65

H **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

I **Collector Recess Etch, Dry**

1. Clean Si wafer, washers, both chucks, and shield with ISO.
2. O_2 plasma clean (20sccm at 125 mTorr, 500V bias for 30 min.).
3. Precoat chamber (CH_4/H_2/Ar 4/20/10 sccm at 125 mTorr, 500V bias for 30 min.).
4. Load wafer and align laser monitor, then pump down to low 10^{-6} Torr.

5. Etch (CH_4/H_2/Ar 4/20/10 sccm at 75 mTorr, 500V bias) until desired stop point is reached. Stop point can be decided by laser monitor pattern or etch time. Do not etch into the base region.
6. Remove polymer (O_2 50 sccm at 125 mTorr, 200V bias for a quarter of etch time).
7. Vent chamber and remove sample.

A.2 Epitaxial Transfer

No mask required

A **Wafer Cleaving**

1. Cleave a piece of mechanical grade GaAs wafer so that it fits well within the InP piece. About 3 mm of space is required all around to accommodate the movement of the GaAs piece on the InP wafer.

B **Solvent Cleaning**
Both InP and GaAs wafers need cleaning.
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

C **Epoxy Bonding**
While the dehydration bake is going on the following should be done to keep the bonding fixture ready.

1. Cover the top of the chuck with aluminum foil.
2. Cut out three circles of aluminum foil slightly larger in size to the base of the dome.
3. Mix the two components of epoxy thoroughly while still in the pouch.
4. Keep a squirt bottle of ACE, the ACE rinse beaker, 10 Q-tips, 2 droppers and scissors ready.

After the dehydration bake the following should be done.

1. Cool down after dehydration, 10 min.
2. Lay the two pieces on wipes and blow with N2 to make sure that there are no dust particles.
3. Slit the pouch and using the droppers place minimal amount of epoxy on the InP substrate.
4. Place the GaAs piece on it, tap it in and move it around until epoxy can be seen from all the four sides.
5. Wipe of extra epoxy from the sides using the Q-tips. If the amount of epoxy is excessive then as a last resort use ACE soaked Q-tips and ACE rinse. Avoid getting epoxy on the back of the InP wafer.
6. Place the combined piece on the chuck. Cover it with the aluminum foil circles and carefully place the dome above it so as not to move one wafer with respect to the other.
7. Apply vacuum. Observe the movement of the dome. If it is excessive then break the vacuum and readjust the two pieces. Breaking vacuum too many times is not a good idea.
8. Keep the wafer pressed at room temperature for at least 45 min. Fixture on hotplate.
9. Set T=140° C on the hotplate.
10. After 30 min set it to 90° C.
11. After 15 more mins take the fixture off the hotplate and place it on the large metal plate behind the bench. Let it cool for atleast 1 hr and 15 min.

12. Break vacuum. Peel of the aluminum foils that are stuck to the bonded wafers. This might require some force and should be done carefully so as not to break the wafers.

D **Substrate Removal**

1. 3:1::HCl:DI - mix well.
2. Place the bonded pieces in a basket with the back of the InP wafer facing up. item Suspend the basket in the solution - no stirring.
3. Make sure that bubbles are appearing from all over the surface.
4. Observe from time to time to see if InP clumps are forming. If so remove the wafer from the solution and try to remove the cause for this.
5. Stop only after shiny InGaAs surface has appeared all over the wafer. This should take ∼1hr. Rinse in DI and blow dry.
6. Parts of the epitaxial film will be flapping freely on the sides. This should go away by the time rinsing and blow drying are done.
7. Small strips of epitaxial film will remain attached to the GaAs wafer, held by the epoxy that would have welled up along the sides. A little pressure from the scribing needle on the sides should be enough to disengage these strips from the GaAs wafer.
8. Observe under microscope. Surface should be clean and smooth without any particles.

Caution: The bubbles that form during etching are those of a very toxic gas (phosphine) . Keep the sash of the hood down while etching the InP substrate. While taking periodic looks hold your breath at all times.

A.3 Exposing Alignment Marks

Mask Layer: Align, Dark Field.

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near

your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake, 10 min.
2. May do an edge bead removal if contact is poor.
3. Backside (IR) aligner should be made ready. Use the proper baseplate and chuck for the backside aligner. A vacuum connection has to be made. The camera and the monitor should be turned on. **Caution:** Before flipping the selection switch to automatic(IR mode) make sure that the baseplate is changed - otherwise the IR lamp will smash into the baseplate.
4. Using the microscope lamp make sure that the wafer is making good contact. Then go into separation, turn down the microscope lamp, turn up the IR lamp and align using the monitor. When alignment is done turn up the microscope lamp again and verify contact.

5. Use exposure of 7.5 mW/cm^2 for 7.5 sec. (57 mJ).

D **Development**

1. AZ 400K : DI :: 1:4
2. Develop for 60 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Etching Vias**

1. Mix the phosphoric acid etch as follows: 12 ml of phosphoric acid in 200 ml of DI - mix well. Add 4 ml of peroxide. If the bottle looks nearly empty and/or old be sure to fill it up with fresh peroxide from the main bottle.
2. Mix a dilute solution of NH_4OH : H_2O :: 1 : 15.
3. Dip in dilute NH_4OH for 20 sec.
4. Rinse in DI for 3 min.
5. Blow dry with N_2.
6. Stirring at 100 rpm suspend the wafer in the etchant in a basket.
7. The etch rate should be around 1000 Å/min. Stop when the alignment marks look quite clear to the eye.
8. Rinse in DI for 3 min.
9. Observe under microscope to make sure that all the alignment marks are clearly exposed. If not repeat etching for suitable amounts of time.
10. Remove photoresist using ACE and do a squirt clean.
11. Dektak along a few alignment mark vias to see if the epilayer thickness corresponds to the design value.

A.4 Emitter Contacts

Mask Layer: Emitter, Dark Field.

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ P4110 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake, 10 min.
2. Edge bead removal necessary.
3. Expose at 7.5 mW/cm^2 for 8 sec. Good contact between wafer and mask necessary. Check for fringes in the photoresist after contact.

4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. Toluene soak: 4 min.
2. AZ 400K : DI :: 1:4
3. Develop for 60 sec.
4. Rinse in running DI water for 3 min.
5. Blow dry with N_2.
6. If some photoresist remains develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Metal Evaporation**

1. Dilute NH_4OH (1:15) dip for 30 sec. just before loading the evaporator.
2. Place wafer in E-Beam mount. Cover the egdes of the wafer where photoresist has been removed due to edge bead removal.
3. Make sure the crystal monitor reads < 10; change if necessary.
4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	200	2-3	1.65
Pt	500	1	1.90
Au	7800	$\sim$25	1.55
Si	500	2-3	1.65

G **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.

2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

A.5 Emitter Mesa Etch

No mask required.

A **Oxygen Plasma Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 15 sec.

B **Surface Preparation**

1. Mix a dilute solution of NH_4OH : H_2O :: 1 : 10.
2. Dip in dilute NH_4OH for 10 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N_2.

C **Dry Etch**

1. Clean Si wafer, washers, both chucks, and shield with ISO.
2. O_2 plasma clean (20 sccm at 125 mTorr, 500V bias for 30 min.).
3. Precoat chamber (CH_4/H_2/Ar 4/20/10 sccm at 125 mTorr, 500V bias for 30 min.).
4. Load wafer and align laser monitor, then pump down to low 10^{-6} Torr.

5. Etch ($CH_4/H_2/Ar$ 4/20/10 sccm at 75 mTorr, 500V bias) until desired point in InAlAs layer is reached. This is determined from the signature on the laser monitor output plot.
6. Increase pressure to 125 mTorr.
7. Continue to etch until desired stop point reached. Determined again from laser monitor output plot.
8. Remove polymer (O_2 50 sccm at 125 mTorr, 200V bias for a quarter of etch time).
9. Vent chamber and remove sample.

D **Si Removal**

1. 300 mTorr of CF_4.
2. Power = 100W at low frequency.
3. run for 3 min.
4. Check that Si has been removed with optical microscope.
5. Remove samples, clean chamber for 10 minutes with O_2 (300W, 300 mTorr).
6. Replace samples and do standard descum (O_2 at 100W, 300 mTorr for 15 sec.).

E **Selective Etch for InAlAs**

1. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$
2. Dip in dilute NH_4OH for 10 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N_2.
5. Mix Solution B - $HCl:H_2O$ :: 4:1.
6. Mix Solution A - HBr:Acetic acid :: 1:1.
7. Mix Solution A:B::1:1.
8. Stirring at 300 rpm, etch for 10 sec.
9. Rinse in DI for 3 min.
10. Blow dry with N_2.

F **Nonselective Etch**

1. Mix etchant as follows: 55 ml of 1M citric acid in 220 ml DI. Mix well. Add 5 ml peroxide from our bottle using our peroxide beaker and our pipette. Mix well. Add 1 ml phosphoric acid. Mix well.
2. Stirring at 300 rpm etch for 25 sec. by suspending the wafer vertically in a holder.
3. Rinse in DI for 3 min.
4. Blow dry with N_2.

A.6 Base Contacts

Mask Layer: Base, Light Field.

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Photoresist Application and Exposure**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Wafer on spinner chuck with vacuum; blow with N_2.

3. Apply EIR 5214 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Hot Plate Bake, 95° C, 1 min.
6. Cool down for 10 min.
7. Expose at 7.5 mW/cm^2 for 10 sec. Use vacuum-contact (HP mode) and use O-ring.
8. Hot Plate Bake, 105° C, 1 min.
9. Flood Expose at 7.5 mW/cm^2 for 30 sec.

C **Development**

1. AZ 400K : DI :: 1:5.5.
2. Develop for 35 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec.

D **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

E **Metal Evaporation**

1. Mix HCl:H_2O :: 1:10.
2. Dip in dilute HCl for 10 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N_2.
5. Place wafer in E-Beam mount.
6. Make sure the crystal monitor reads < 10; change if necessary.
7. Pump down to at least 1×10^{-6} Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	200	2-3	1.65
Pt	500	1	1.90
Au	500	∼25	1.55

F **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

A.7 Base Mesa/Isolation Etch and Sintering

Mask Layer: Padetch, Dark Field.

A **Solvent Cleaning**

Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.

Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.

4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ P4210 with syringe and filter to cover wafer.
4. Spin at 5.5 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.

C **Exposure**

1. Cool down after soft bake, 10 min.
2. Edge bead removal as necessary.
3. Expose at 7.5 mW/cm^2 for 10.5 sec (79 mJ).
4. Use hard-contact (HP mode) and use O-ring.

D **Development**

1. AZ 400K : DI :: 1:4
2. Develop for 90 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec.

E **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

F **Etching**

1. Mix etchant as follows: 55 ml of 1M citric acid in 220 ml DI. Mix well. Add 5 ml peroxide from our bottle using our peroxide beaker and our pipette. Mix well. Add 1 ml phosphoric acid. Mix well.
2. Stirring at 300 rpm etch for 25 sec. by suspending the wafer vertically in a holder.
3. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 15$.
4. Dip in dilute NH_4OH for 20 sec.
5. Rinse in DI for 3 min.
6. Blow dry with N_2.
7. Stirring at 300 rpm suspend the wafer in the etchant in a basket.
8. Stop when the collector pads look quite clear to the eye.
9. Rinse in DI for 3 min.
10. Observe under microscope to make sure that all collector pads are clearly exposed. If not repeat etching for suitable amounts of time.
11. Remove photoresist using ACE and do a squirt clean.

G **Sintering**

1. Prepare RTA by loading the program for 300° C, 1 min. sinter. Also make sure forming gas is flowing at prescribed rate and prescribed pressure.
2. Run the program several times until the temperature stabilizes at 300° C, during the 1 min. period.
3. Sinter the wafer. **Caution:** After sinter and trial runs, turn off the forming gas and use a face mask before opening the chamber.

A.8 Pad Metal

Mask Layer: Empad, Dark Field.

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near

your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.
2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Photoresist Application and Exposure**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 10 min.
2. Wafer on spinner chuck with vacuum; blow with N_2.
3. Apply OCG 825 with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.
6. Cool down for 10 min.
7. Flood expose at 7.5 mW/cm^2 for 2.5 sec.
8. Toluene soak for 2 min.
9. Wafer on spinner chuck with vacuum; blow with N_2.
10. Apply AZ 4110 with syringe and filter to cover wafer.
11. Spin at 6 krpm for 30 sec.
12. Soft Bake, 90° C, 30 min. in petri dish without cover.
13. Cool down for 10 mins
14. Edge bead removal as necessary.
15. Use hard-contact (HP mode) and use O-ring
16. Expose at 7.5 mW/cm^2 for 8 sec.

C **Development**

1. AZ 400K : DI :: 1:4.
2. Develop for 60 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. If some photoresist remains develop again in steps of 5 sec. Undercut in the bottom photoresist layer should be clearly visible.

D **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

E **Preparation for Metal Evaporation**

1. Mix the phosphoric acid etch as follows: 12 ml of phosphoric acid in 200 ml of DI - mix well. Add 4 ml of peroxide. If the bottle looks nearly empty and/or old be sure to fill it up with fresh peroxide from the main bottle.
2. Stirring at 200 rpm suspend the wafer in the etchant using a basket for 3 min.
3. Rinse in DI for 3 min.
4. Blow dry with N_2.
5. Mix HF :H_2O:: 1 : 20.
6. Etch top layer of Ti $\sim$ 30 sec.
7. Rinse in running DI for 3 min.
8. Blow dry with N_2.

Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.

F **Metal Evaporation**

1. Place wafer in E-Beam mount.
2. Make sure the crystal monitor reads < 10; change if necessary.
3. Pump down to at least 1×10^{-6} Torr.
4. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec.)	Approx. Vernier
Ti	200	2-3	1.65
Au	5000	∼25	1.55

G **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

A.9 Polyimide Planarization

Mask Layer: Postetch, Dark Field.

A **Solvent Cleaning**
Cleanliness Caution: New bottles of solvents out of the cabinet are dirty. Wipe down with a towel and change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always have tweezers in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 5 min.

2. Hot ISO 5 min.
3. Running DI 3 min.
4. Blow dry with N_2.
5. Dehydration bake, 120° C, 30 min. in petri dish without cover.

B **Polyimide Application**
Safety Note: The vapors from polyimide are extremely harmful. Never breathe if you put your head under the hood.

1. Mix adhesion promoter in a dropper bottle.
   (a) One part QZ 3289 concentrate.
   (b) Nine parts QZ 3290 dilutant.
2. Wafer on spinner chuck with vacuum
3. Blow off with N_2.
4. Apply adhesion promoter to cover wafer
5. Spin at 5 krpm for 30 sec.
6. Let evaporate for 2 min. on chuck then Blow off with N_2.
7. Apply Probromide 284 to cover wafer with syringe and filter.
8. Spin at 4 krpm for 30 sec. (gives $\sim$ 1.8 μm film).
9. Hard bake polyimide in petri dish without cover. Cover the base of the petri dish with aluminum foils so that the polyimide under the wafer does not get stuck to the dish.
10. Use programmable oven as follows:
    (a) 90° C for 30 min.
    (b) ramp at 5° C per min. to 170° C.
    (c) hold at 170° C for 40 min.
    (d) ramp at 2° C per min. to 240° C.
    (e) hold at 240° C for 30 min.
    (f) ramp at 2° C per min. to 170° C.

C **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down for atleast 15 min.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ P4330-RS with syringe and filter to cover wafer.
4. Spin at 5 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.

D **Exposure**

1. Cool down after soft bake, 10 min.
2. Edge bead removal as necessary.
3. Expose at 7.5 mW/cm^2 for 15 sec (112 mJ).
4. Use hard-contact (HP mode) and use O-ring.

E **Development**

1. AZ 400K : DI :: 1:4
2. Develop for 90 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.

F **Hardbake**

1. Hardbake photoresist at 120° C for 30 min.

G O_2 **RIE**

1. Load machine according to instructions.
2. Pump down to 1×10^{-6} Torr.
3. Set up laser monitor
   (a) Look for diffraction pattern to identify beam.
   (b) Set up chart recorder for 1 hour and ∼500 mV.
4. Etch conditions:
   (a) flow rate = 7.0 sccm.
   (b) O_2 chamber pressure = 10 mTorr.

(c) P = 60 W (this is what is controlled).
(d) Voltage = 350 V.

5. Etch for 19 cycles

H O_2 **Plasma Cleanup**

1. Inspect under SEM to see if all metal is clear.
2. Etch as needed to expose all Au.
   (a) 300 mTorr of O_2.
   (b) Power = 200 W at low frequency.
   (c) run for 2 min. intervals.

A.10 Post

Mask Layer: Post, Dark Field.

A **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Wafer on spinner chuck with vacuum; blow with N_2.
2. Apply AZ 4210 with syringe and filter to cover wafer.
3. Spin at 5.5 krpm for 30 sec.
4. Soft Bake, 90° C, 30 min. in petri dish without cover.

B **Exposure**

1. Cool down for 10 min.
2. Edge bead removal as necessary.
3. Use hard-contact (HP mode) and use O-ring
4. Expose at 7.5 mW/cm^2 for 10 sec (75 mJ).

C **Development**

1. AZ 400K : DI :: 1:4.

2. Develop for 75 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. Some post holes will be deep. make sure that photoresist is gone from those places. If not develop further in steps of 10 sec.

D **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.
3. Run for 20 sec.

E **Postbake**

1. Post Bake in 120° C oven for 30 min. in petri dish without cover.

F **Gold Etch**
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids. Wear face shield at all times while at acid hood.

1. Mix new etchant every time: KI_2/I_2:H_2O ::1 : 5.
2. Etch for 5 sec.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2.

G **Sputter Flash Layer**

1. Load sample in the sputtering machine. Make sure that the Ti and Au sources are at their respective positions
2. Pump down to less than 5×10^{-6} Torr.
3. Setup Ar flow rate at 25 sccm and chamber pressure at 10 mTorr.
4. Sputter 300 Å Ti layer (Power = 0.1 KW, Time = 4 min 30 sec.).
5. Sputter 1100 Å Au layer (Power = 0.2 KW, Time = 1 min 40 sec.).
6. Sputter 100 Å Ti layer (Power = 0.1 KW, Time = 1 min 30 sec.).
7. Prepare for spinning the next layer of photoresist.
8. Vent chamber and remove sample.

A.11 Airbridge

Mask Layer: AB, Dark Field.

A **Photoresist Application**
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Immediately take the wafer from the sputtering machine to the spinner.
2. Wafer on spinner chuck with vacuum; blow with N_2.
3. Apply AZ 4330-RS with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 90° C, 30 min. in petri dish without cover.

B **Exposure**

1. Cool down for 10 min.
2. Edge bead removal as necessary.
3. Use hard-contact (HP mode) and use O-ring
4. Expose at 7.5 mW/cm^2 for 14 sec (105 mJ).

C **Development**

1. AZ 400K : DI :: 1:4.
2. Develop for 120 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. Inspect for green scum in the post holes. Develop more if needed.
6. Flood expose for 2 min.

D **Oxygen Plasma Photoresist Descum**

1. 300 mTorr of O_2.
2. Power = 100W at low frequency.

3. Run for 20 sec.

E **Postbake**

1. Post Bake in 115° C oven for 30 min. in petri dish without cover.

F **Plating Preparation**

1. Clean tweezers, anode, thermometer and magnet with ISO and DI water.
2. Rinse wafer in running DI for 3 min.
3. Heat 800 ml of plating solution in beaker with short stirrer bar to 45° C.

G **Titanium Etch**

Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.

1. Dektak photoresist to record initial thickness.
2. Use a swab with ACE to remove the photoresist on one edge of the wafer. This is used to make the electrical contact.
3. Mix HF :H_2O:: 1 : 20.
4. Etch top layer of Ti $\sim$ 25 sec. (10 sec. after bright gold appears.)
5. Rinse in running DI for 3 min.
6. Blow dry with N_2.

H **Gold Plating**

1. The plating rate depends on the size of the wafer and the number of air bridges on it, as well as the age of the plating solution. Start with a plating current of 0.5 mA for a 1 cm^2 wafer.
2. Plate for 15 min.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2.
5. Dektak the photoresist and calculate the thickness of plated gold.

6. Adjust the current to get a plating rate of 1.8 μm/hr.
7. Repeat above mentioned steps.
8. Plate until the top of the air bridges are even with the photoresist.

I **Airbridge Photoresist Layer Removal**

1. Mix AZ 400K:DI::1 : 1.
2. Develop for 90 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N_2.
5. Inspect for scum and use O_2 plasma if necessary.
   (a) 300 mTorr of O_2.
   (b) Power = 200W at low frequency.
   (c) Run for 3 min.

J **First Titanium Layer Removal**
Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.

1. Use HF :H_2O:: 1 : 20 from before.
2. Etch top layer of Ti $\sim$ 30 sec. with moderate agitation (10 sec after gold appears).
3. Rinse in running DI for 3 min.
4. Blow dry with N_2.

K **Gold Layer Removal**
Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated acids. Wear face shield at all times while at acid hood.

1. Mix new etchant every time: $KI_2/I_2/H_2O$ ::1 : 1.
2. Etch for 5 sec.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2.

5. Inspect under microscope. If some Au is still left, etch for another 3 sec.

L **Second Titanium Layer Removal**
Safety Note: When working with HF, always wear a new pair of our own yellow safety gloves. Wear a face shield at all times when working near the HF hood, and keep glassware away.

1. Use HF :H_2O:: 1 : 20 from before.
2. Etch Ti layer for $\sim$ 30 sec. with moderate agitation (10 sec after gold from the pads appear clearly).
3. Rinse in running DI for 3 min.
4. Blow dry with N_2.

M **Post Photoresist Layer Removal**

1. Use ACE in beaker for 5 min.
2. Follow with ACE, METH, ISO in squirt clean.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2.

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