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Santa Barbara

Nonlinear Transmission Lines for
Picosecond Pulse, Impulse and
Millimeter-Wave Harmonic Generation

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philosophy

in

Electrical and Computer Engineering

by

Michael Garth Case

Committee in charge:

Professor Mark Rodwell, Chairperson

Professor John Bowers

Professor Umesh Mishra

Professor Robert York

July 2, 1993

The Dissertation of Michael Garth Case
is approved:

Committee Chairperson

July 29, 1993

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Vita

- 20 October 1966, Born in Ventura, California
- 23 August 1986, Married Kimberly
- 1988–1989 Student Assistant, Electrical and Computer Engineering Department, University of California at Santa Barbara
- June 1989, B. S., Electrical and Computer Engineering, University of California at Santa Barbara
- 1989–1993 Research Assistant, Electrical and Computer Engineering Department, University of California at Santa Barbara
- March 1991, M. S., Electrical and Computer Engineering, University of California at Santa Barbara

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Abstract

Nonlinear Transmission Lines for Picosecond Pulse, Impulse and Millimeter-Wave Harmonic Generation

by
Michael Garth Case

Recent advances in semiconductor and optical technology have demonstrated a need for higher speed and wider bandwidth signal generation and measurement techniques. Digital systems with gate delays as low as 25 ps and both electrical and optical data rates as high as 40 GB/s have been reported. The availability of mm-wave components allows more compact, wider communications bandwidths. Currently, broadband electrical signal generators and measurement devices are limited to about 50 GHz. This work describes the theory, design considerations, fabrication, and measurements of nonlinear transmission lines (NLTLs) which are GaAs integrated circuits capable of increasing the range of broadband measurements and signal generation.

Nonlinear transmission lines (NLTLs) are high-impedance waveguides which are periodically loaded with reverse-biased diodes. These diodes appear as voltage-variable capacitors (varactors) and cause the propagation delay through the NLTL to depend on the wave amplitude. Nonlinearity arises from the voltage-dependent propagation characteristics of the NLTL. Dispersion arises from the periodicity of the NLTL. Depending on the design of the structure (nonlinearity, dispersion, and input waveform), one can generate a variety of waveforms. Measurements include 1.8 ps duration, 5 V amplitude step-functions, 5.1 ps duration, 11 V amplitude impulses, and mm-wave harmonic multipliers with as little as 6 dB conversion loss. An added utility of these devices is the ease with which they can be integrated with other device technologies (e.g. HEMTs or HBTs).

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Chapter 1

Introduction

Recent advances in both optical and mm-wave semiconductor devices and systems have demonstrated their applicability in a variety of very high speed, wide bandwidth systems. Digital communication rates as high as 40 GHz should be possible with modulated semiconductor lasers [16]. Digital logic gates have propagation delays as low as 25 ps per gate [30] and are capable of clock rates approaching 40 GB/s [19]. Transistors with cutoff frequencies in excess of 300 GHz have been reported [28]. As mm-wave components become available, the smaller wavelengths allow smaller antennae and finer spatial resolution. Automobile collision avoidance [32] and low visibility aircraft landing systems [9] are now becoming feasible using V- and W-band radar. NASA is investigating molecular resonances in the ozone layer at THz frequencies to analyze its depletion.

In order to modulate laser diodes and generate test waveforms for digital systems, large amplitude, short duration pulses and impulses are needed. Photoconductive switches can produce very fast (0.2 ps) electrical transients with several volt amplitudes [21], or pulses as large as 700 V with a 1 ps rise time [29]. Photoconductive switches require a very high speed, high power (expensive) laser system to transduce an optical to an electrical pulse. Impulses can be generated electrically by step recovery diodes which typically produce 10 V pulses, but these are limited to 10–20 ps transition times [35]. Resonant tunneling diode (RTD) pulse generators are capable of 2 ps transitions, but are limited to small voltage swings ($\approx 0.5 V_{p-p}$) [22, 14] and require very high current densities which limits device lifetime.

Characterization of high speed digital and broadband analog systems requires measurement capabilities exceeding those of the system. Oscilloscopes can measure broadband waveforms up to 50 GHz [47] and network analyzers are capable

of broadband measurements to 60 GHz [48]. Vector network analyzers are capable of up to 110 GHz measurements [42], but these require waveguide fixtures and their associated narrow bandwidth. Network analysis has been performed to 1 THz [39], but is an insertion gain measurement only and is restricted to quasi optical systems.

This dissertation describes the underlying theory, design considerations, and measurements of three types of nonlinear transmission lines (NLTLs) capable of electrically generating picosecond transition pulses, mm-wave harmonics, and picosecond duration impulses. The performance of the devices reported exceeds that of conventional electrical wave shaping devices. These NLTLs have direct applications in a variety of high speed, wide bandwidth systems including picosecond resolution sampling circuits, laser and switching diode drivers, test waveform generators, and mm-wave sources.

One significant advantage NLTLs have over other electrical pulse generating circuits is their integrability with other circuitry. NLTLs are GaAs integrated circuits consisting of waveguide periodically loaded with reverse biased Schottky diodes. Since the capacitance changes with applied voltage, the propagation characteristics depend on the wave amplitude. These devices exhibit dispersion due to the periodicity of the loading diodes. Depending on device technology and design, NLTLs could be integrated with an HEMT, HBT, or other process which allows Schottky diodes. As will be shown, depending on the interaction between the effects of nonlinearity, dispersion, and parasitics, devices can be designed to efficiently generate broadband mm-wave harmonics or pulses or impulses with < 1 ps transition times.

Chapter 2

Nonlinear Transmission Line Theory

The NLTL has three fundamental and quantifiable characteristics just as any nonideal transmission line. These are nonlinearity, dispersion, and dissipation. Along with some other characteristics (e.g. impedance, length, etc.), they define a transmission line's behavior with arbitrary stimulation. What distinguishes one class of line from another is the *degree* to which these characteristics occur and interact. For example, optical fiber has very small nonlinearity and dissipation but moderate dispersion; a small amplitude impulse will spread on propagation due to the dispersion while a large amplitude impulse may become compressed due to the nonlinearity. This work is focused on the properties of microwave transmission lines periodically loaded by diodes.

2.1 Dispersion, Nonlinearity, and Dissipation

NLTLs consisting of coplanar waveguide (CPW) [3] (figure 2.1) periodically loaded with reverse biased Schottky diodes provide nonlinearity due to the voltage dependent capacitance, dispersion due to the periodicity, and dissipation due to the finite conductivity of the CPW conductor and series resistance of the diodes. A schematic diagram of the circuit is shown in figure 2.2. An approximate equivalent circuit consisting of series inductors and shunt capacitors (figure 2.3) is much easier to analyze than the transmission line circuit. There are significant differences between the two circuits however. These are most evident in their dispersion relationships.

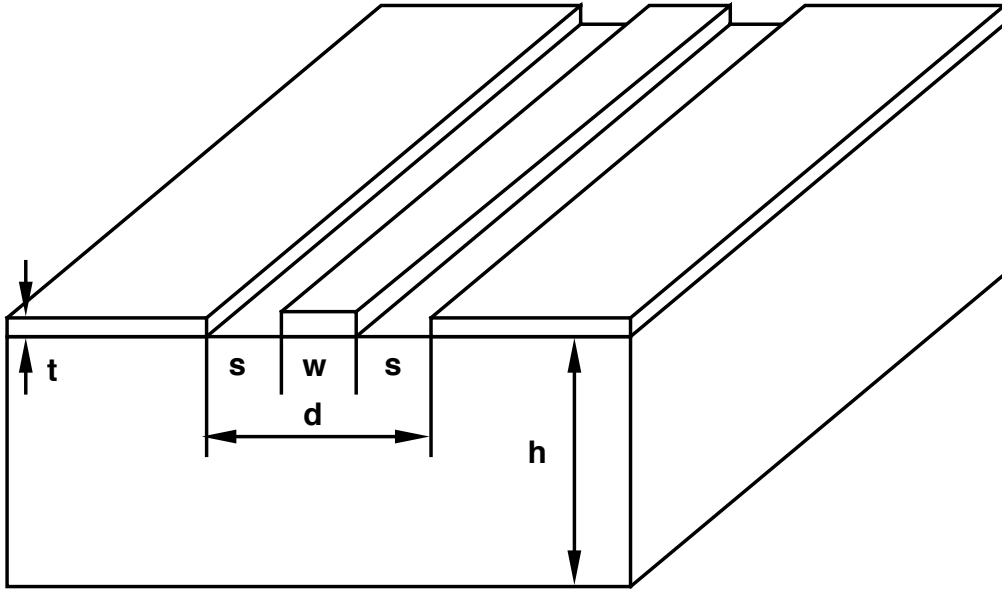


Figure 2.1: A metallic coplanar waveguide (CPW) on a dielectric substrate is patterned by photolithography.

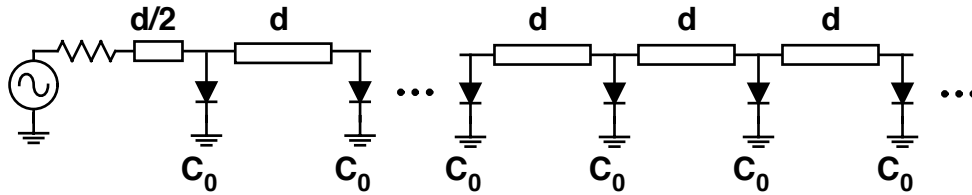


Figure 2.2: Circuit diagram for the nonlinear transmission line consisting of series transmission line section loaded with reverse-biased diodes.

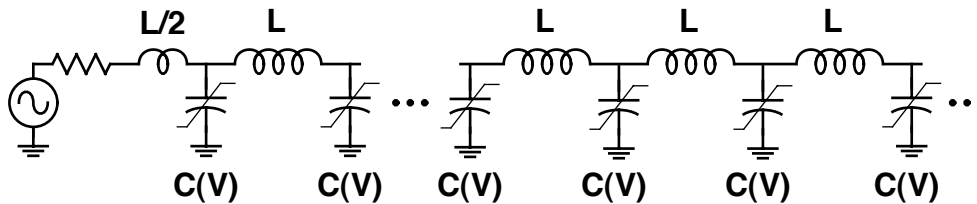


Figure 2.3: Circuit diagram for the LC equivalent of the nonlinear transmission line.

2.1.1 Dispersion

Dispersion is a variation in phase velocity with frequency. The dispersion relationship for the CPW NLTL can be derived from a unit cell's transmission matrix. Transmission matrices (or $ABCD$ matrices) are convenient for cascading circuits together. To determine characteristic impedance and dispersion relationships for an arbitrary reciprocal network having the transmission matrix

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}, \quad (2.1)$$

one sets the determinant of

$$\begin{bmatrix} A - e^{-\gamma d} & B \\ C & D - e^{-\gamma d} \end{bmatrix} \quad (2.2)$$

to zero where γ is the complex propagation constant and d is the physical length of the whole network. This being the case, the propagation constant and characteristic impedance can be determined from $\cosh(\gamma d) = (A + D)/2$ and $Z_{ABCD} = \pm\sqrt{B/C}$ respectively.

For the lossless CPW NLTL cell (figure 2.4a), the characteristic $ABCD$ matrix is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{\omega d}{2v_0}\right) & jZ_0 \cos\left(\frac{\omega d}{2v_0}\right) \\ \frac{j}{Z_0} \cos\left(\frac{\omega d}{2v_0}\right) & \cos\left(\frac{\omega d}{2v_0}\right) \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ j\omega C_0 & 1 \end{bmatrix} \cdot \begin{bmatrix} \cos\left(\frac{\omega d}{2v_0}\right) & jZ_0 \cos\left(\frac{\omega d}{2v_0}\right) \\ \frac{j}{Z_0} \cos\left(\frac{\omega d}{2v_0}\right) & \cos\left(\frac{\omega d}{2v_0}\right) \end{bmatrix} \quad (2.3)$$

and results in the transcendental equation,

$$\cos(kd) = \cos\left(\frac{\omega d}{v_0}\right) - \frac{\omega Z_0 C_0}{2} \sin\left(\frac{\omega d}{v_0}\right) \quad (2.4)$$

for dispersion and

$$Z_{ABCD} = \sqrt{\frac{\sin\left(\frac{\omega d}{v_0}\right) + \frac{\omega Z_0 C_0}{2} \left(\cos\left(\frac{\omega d}{v_0}\right) - 1\right)}{\sin\left(\frac{\omega d}{v_0}\right) + \frac{\omega Z_0 C_0}{2} \left(\cos\left(\frac{\omega d}{v_0}\right) + 1\right)}} \quad (2.5)$$

for impedance where k is the propagation constant for the NLTL cell (imaginary part of γ), d is the physical length of line, ω is the angular frequency,

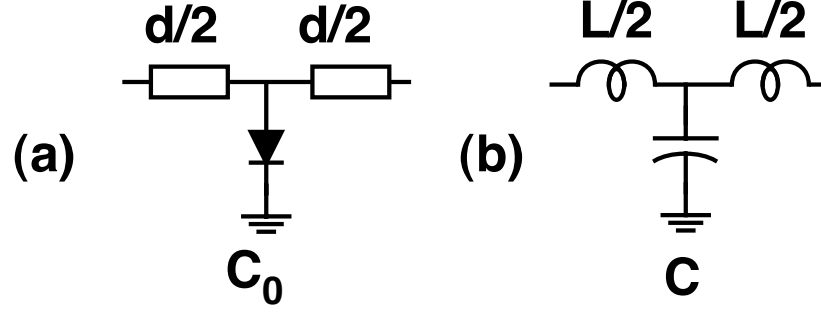


Figure 2.4: “T” models for the nonlinear transmission line unit cell: (a) for the transmission line circuit, and (b) for the LC equivalent.

v_0 is the phase velocity of the CPW, Z_0 is the characteristic impedance of the CPW, and C_0 is the loading capacitance, here assumed to be a constant (i.e. no nonlinearity).

Using the LC equivalent of the NLTL cell (figure 2.4b), much simpler $ABCD$ matrices

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & j\omega\frac{L}{2} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & j\omega\frac{L}{2} \\ 0 & 1 \end{bmatrix} \quad (2.6)$$

result in much simpler dispersion

$$\omega^2 = \frac{2}{LC} (1 - \cos(kd)) \quad (2.7)$$

and impedance

$$Z_{NLTL} = \sqrt{\frac{L}{C} - \frac{\omega^2 L^2}{4}} \quad (2.8)$$

relationships. L and C are the equivalent series inductance and shunt capacitance respectively. At low frequencies ($d < \lambda/8$), the CPW NLTL can be approximated as an LC NLTL by substituting $L \approx \tau Z_0$ and $C \approx \tau/Z_0 + C_0$.

Both dispersion relationships exhibit lowpass characteristics, and signals at frequencies above the lowpass corner are strongly attenuated (k is imaginary). This lowpass corner is called the Bragg frequency since the reflections from this one-dimensional electrical lattice bear a similarity to the reflections seen in x-ray scattering in a periodic crystal lattice. At the Bragg frequency ($2\pi f_B = \omega_B$) the propagation factor $kd = \pi$ and $Z_0 = 0$. It is easy to determine $\omega_B = 2/\sqrt{LC}$ for equation 2.7, but equation 2.4 is not readily solved. Figures 2.5 and 2.6 show

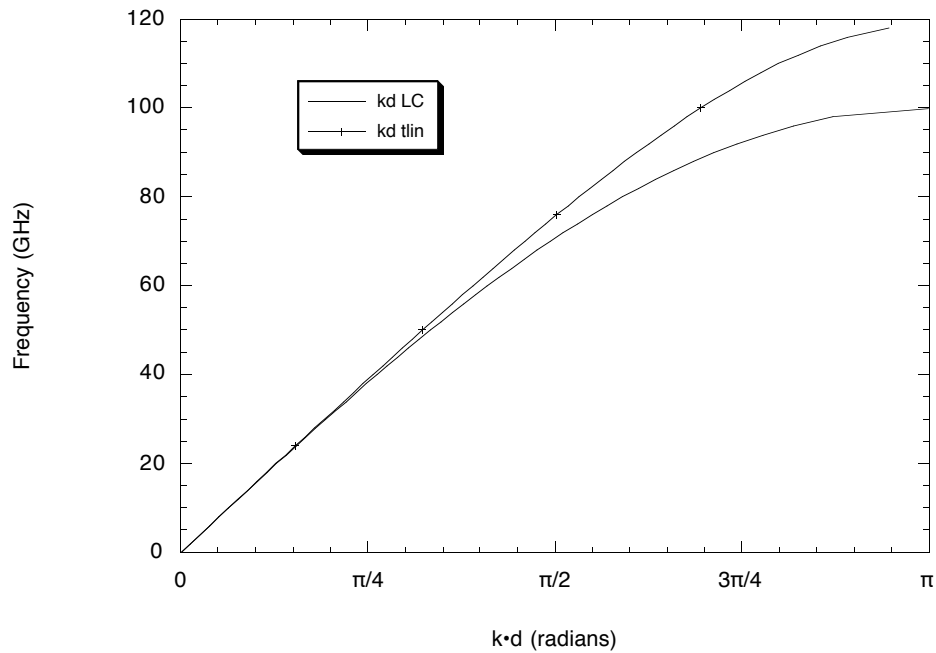


Figure 2.5: Dispersion diagram for transmission line and LC equivalent models for a typical NLTL unit cell. Cutoff frequency for the transmission line circuit is 20% higher than the LC model.

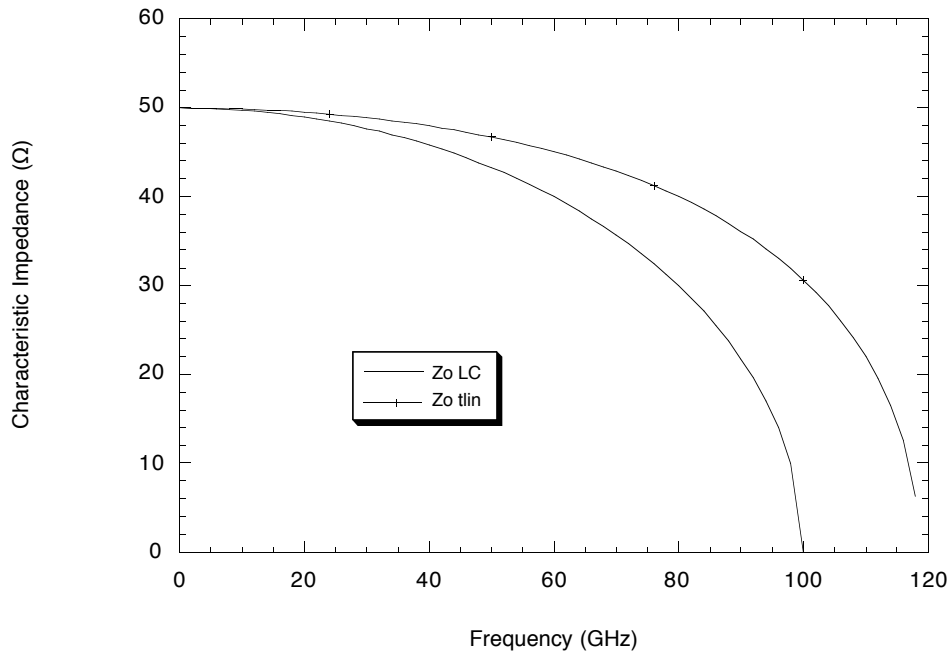


Figure 2.6: Characteristic impedance as a function of frequency for the transmission line and LC models of a typical NLTL cell.

comparisons between the CPW and LC types of dispersion and characteristic impedance respectively for an example NLTL section having $Z_0 = 75\ \Omega$, $v_0 = 113\ \mu\text{m}/\text{ps}$, $d = 240\ \mu\text{m}$, and $C_0 = 35.4\ \text{fF}$ ($\tau = d/v_0 = 2.12\ \text{ps}$, $L = 159\ \text{pH}$ and $C = 63.7\ \text{fF}$). The most striking difference is the Bragg frequency: it is 100 GHz for the LC line and 120 GHz for the CPW line. The low frequency characteristics are very similar for the two models, but as frequencies approach f_B , the models differ significantly. These are indications of the LC model's range of applicability.

2.1.2 Nonlinearity

Diodes present two sources of nonlinearity: conductive and reactive. The conductive nonlinearity is evident in the $I(V)$ curves and the reactive nonlinearity is evident in the $C(V)$ curves (see appendix A for typical plots). Many microwave, mm-wave, and sub- mm-wave components use the conductive nonlinearity for mixing [26], harmonic conversion [33], and switching [31]. Such modulated conductance devices can suffer from loss due to the dissipative nature of the nonlinearity, but by relying on a modulated reactance, very low loss and good impedance matching can be achieved.

The nature of the diode's $C(V)$ characteristics depends wholly on the epitaxial structure of the diode. For a given doping profile (assumed to be exclusively N -type, homogeneous material), the approximate capacitance can be determined by

$$\phi - V = \int_0^{x_d(V)} \frac{qx_d}{\varepsilon} N_D(x_d) dx_d \quad (2.9)$$

then computing the capacitance as $C(V) = \varepsilon A/x_d(V)$ where ϕ is the barrier potential, V is the applied voltage, x_d is the depletion depth, q is the electron charge, ε is the dielectric constant, and $N_D(x_d)$ is the N -type doping concentration as a function of depletion depth. For arbitrary doping profiles, solutions to equation 2.9 often require numerical methods and result in ordered pairs of $C(V)$ data. This data can then be fitted to any desired functional relationship. The most common function applied to diode $C(V)$ curves is

$$C_j(V) = \frac{C_{j0}}{(1 - V/\phi)^M} \quad (2.10)$$

where C_j is the fitted junction capacitance, C_{j0} is the zero-bias junction capacitance, V is the junction potential, ϕ is the fitted barrier potential, and M is

the grading coefficient ($M = 0.5$ and $\phi =$ the true barrier potential in the case of a uniformly doped diode). This capacitance model is found in most circuit simulators. A polynomial fit allows harmonic balance algorithms to converge more rapidly, but the diode's nonlinear $I(V)$ characteristics are lost.

For a generalized doping profile, some type of capacitance curve fitting is needed if one desires to simulate a circuit incorporating such diodes. The choice of model depends on the application. Circuit simulations were mentioned above, but mathematical modeling of the entire system requires different considerations. Both Ikezi and Hirota model nonlinear transmission lines, but Ikezi deals exclusively with ferroelectric material loading parallel-plate waveguide, while Hirota deals with LC lattices. Ikezi assumes either $C(V) = C(1 - 2\beta V)$ [18] or $C(V) = C(1 - 3\beta V^2)$ [17] depending on his approach. Hirota [15] uses the model $C(V) = C_{j0}/(1 - V/V_0)$. For most diodes, Hirota's $C(V)$ characteristic fits more accurately than Ikezi's; unfortunately, he allows only two fitting parameters (C_{j0} and V_0), while the standard model provides three.

2.1.3 Dissipation

There are two main sources of dissipation in an NLTL. These are diode series resistance and metallic losses. Diode losses arise from the nonzero contact and bulk resistances of the structure while metallic losses arise from the geometry and finite conductivity of the CPW. Another source of loss is radiation, where some portion of the propagating energy is coupled into the substrate; but this loss mechanism is much less significant in an NLTL than the other two. Most simulators do not allow frequency dependent loss (e.g. skin loss) at the same time as nonlinearity. LIBRA [40] is one notable exception. LIBRA uses harmonic balance techniques which allow nonlinearity in the frequency-domain simulation. Unfortunately, LIBRA often gives convergence problems while attempting NLTL characterizations. Mathematical models for NLTL propagation become unworkable in the presence of loss. Minimizing loss both increases device efficiency and reduces discrepancies between model and measurement.

The sources of diode resistance are examined in detail in chapter three. The result is an equivalent resistance (R_S) in series with the diode's junction capacitance ($C_j(V)$). In order to get a feel for the effect of this resistance, first consider small-signal effects. The series RC network has an equivalent shunt RC network (figure 2.7) where the resistance and capacitance values are different.

$$G_{shunt} = \frac{\omega^2 C_{series}^2 R_{series}}{1 + \omega^2 C_{series}^2 R_{series}^2} \approx \omega^2 C_{series}^2 R_{series} \quad (2.11)$$



Figure 2.7: A diode is modeled as a series RC network. This series network has an equivalent shunt network, with different component values.

$$C_{shunt} = \frac{C_{series}}{1 + \omega^2 C_{series}^2 R_{series}^2} \approx C_{series} \quad (2.12)$$

Small-signal loss for a shunt conductance is $\alpha = G_{shunt}/2Y_{NLTL}$ where α is the loss in nepers and Y_{NLTL} is the characteristic admittance ($1/Z_{NLTL}$) of the loaded NLTL. The result is loss which increases with the square of frequency.

Metallic loss on a CPW is treated extensively by Hoffmann [3]. He considers the nonuniform current distribution across the center conductor and ground planes and finite field penetration into thin substrates. Unfortunately, his formulae relating CPW geometry, frequency, material parameters, and loss are very complicated. Robert York has developed a simpler relationship (assuming uniform current distribution in the center conductor and ignoring ground plane resistance)

$$\alpha = \frac{\ell}{4w\sigma\delta Z_{NLTL}} \left(\frac{e^{t/\delta} - \cos(t/\delta) + \sin(t/\delta)}{\cosh(t/\delta) - \cos(t/\delta)} \right) \quad (2.13)$$

where α is the loss in nepers, ℓ is the line length, w is the width of CPW center conductor, σ is the metal conductivity, t is the metal thickness, $\delta = \sqrt{2/(\omega\mu_0\sigma)}$ (μ_0 is the permeability of free space), and Z_{NLTL} is the impedance of the loaded NLTL. At frequencies where the metal thickness is greater than δ , skin loss varies as the square root of frequency.

Radiation loss is thoroughly treated by Rutledge [5]. Radiation loss can occur when the guided mode propagates at a velocity higher than the bulk mode. This occurs in unloaded CPW since $v_{CPW} \approx c\sqrt{2/(1 + \epsilon_R)}$ and $v_{bulk} = c/\sqrt{\epsilon_R}$ where ϵ_R is the relative dielectric constant of the substrate. Since loading the CPW with capacitance slows the wave down ($v_{NLTL} = \ell/\sqrt{LC}$), radiation loss can usually be ignored.

At low frequencies, loss is dominated by CPW resistivity. At high frequencies, loss is dominated by diode series resistance. Figure 2.8 shows the relative

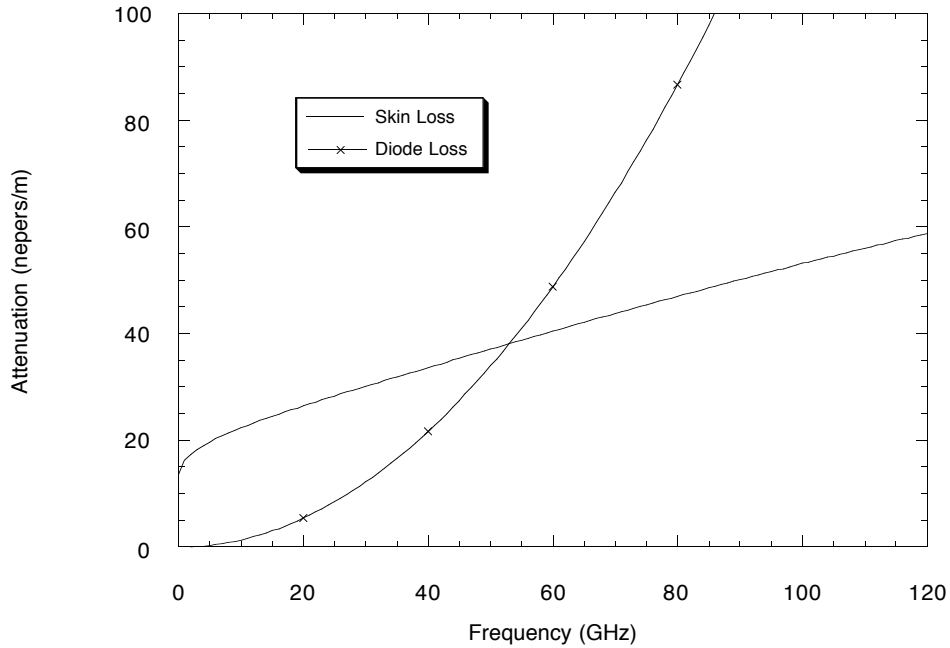


Figure 2.8: The two dominant sources of loss in an NLTL are skin loss and diode loss. These are shown for a typical NLTL cell as a function of frequency.

importance of the two types of loss for the example NLTL section in figure 2.4 using $1 \mu\text{m}$ thick gold CPW with $18 \mu\text{m}$ center conductor and $53 \mu\text{m}$ center conductor to ground plane spacing. These formulae only apply for the NLTL at frequencies well below the Bragg frequency. The relation $\alpha = G_{shunt}/2Y_{NLTL}$ and equation 2.13 apply only to continuous structures ($\omega \ll \omega_B$). In order to determine the exact effects of diode and skin loss on the NLTL, one must introduce loss into the $ABCD$ matrices (equation 2.3) and extract the real part of γ . This is a chore best left to a computer. As frequencies approach f_B , the loss becomes very large.

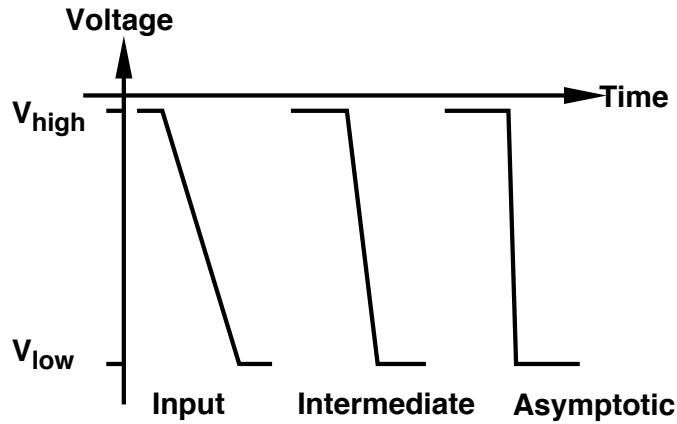


Figure 2.9: Sketch representing shock wave formation for a pulse launched on an NLTL.

2.2 The Case of Weak Dispersion: Shocks

Mark Rodwell [4] has done extensive analyses on the Schottky diode loaded CPW in the absence of dispersion and loss. In this case, one need only consider the LC equivalent circuit, well below the Bragg frequency. For such an NLTL, the small-signal propagation delay decreases for increasing reverse bias voltage. The effect is to steepen the falling edge of a waveform to some asymptotic limit on propagation through the NLTL. The solution to the dispersionless and lossless problem was through the method of characteristics [1]. For an input pulse with fall time $T_{f,in}$ over a voltage swing from V_{low} to V_{high} , this solution predicts the output pulse fall time to be either zero or $T_{f,in} - \ell \left(\sqrt{LC(V_{high})} - \sqrt{LC(V_{low})} \right)$ (ℓ is the line length and L and $C(V)$ are inductance and capacitance per unit length), whichever is greater (see figure 2.9).

Rodwell determined that the effective loading capacitance of the diode over the pulse's voltage swing is a constant, as is the effective NLTL impedance. This results in the so called *large-signal* capacitance

$$C_{LS} \equiv \frac{\Delta Q}{\Delta V} = \frac{1}{V_{high} - V_{low}} \int_{V_{high}}^{V_{low}} C_j(V) dV \quad (2.14)$$

and impedance

$$Z_{LS} = \sqrt{\frac{L}{C_{LS} + C_{line}}} \quad (2.15)$$

(which one should match to the driving source's impedance e.g. 50Ω) where L is the inductance, $C_j(V)$ is the diode capacitance, and C_{line} is the additional capacitance due to the CPW ($C_{line} = \tau/Z_0$). In the presence of weak dispersion and diode loss, the minimum fall time is modified from zero to

$$T_{f,\min} \approx \frac{3.38C_{LS}^2 Z_{LS} R_{series} + 0.245Z_{LS}^2 (C_{line} + C_{LS})^2}{\sqrt{L(C_{line} + C_j(V_{high}))} - \sqrt{L(C_{line} + C_j(V_{low}))}} \quad (2.16)$$

by the expand-compress model where all parameters apply to the entire NLTL. Fall times in the vicinity of 1 ps should be possible. Skin loss can also affect the ultimate speed of the shock, but a quantitative analysis is difficult and simulation does not allow this type of loss. One can reduce the skin loss by increasing the center conductor width of the CPW. This can only be done if the diode connections introduce minimal parasitic effects. Skin loss reduction is accomplished by tapering the Bragg frequency of the NLTL along its length. The input to the line uses a low Bragg frequency (waveform harmonics are low and center conductor is wide) while the output of the line uses a high Bragg frequency (waveform harmonics are high, center conductor is narrow). This method minimizes the total skin loss.

2.3 The Case of Strong Dispersion: Solitons

If dispersion can no longer be treated as a perturbation in the analysis, a new approach is required. First, consider the linear case with dispersion. Even the LC model's dispersion relation is difficult to incorporate into characteristic propagation equations inclusive of nonlinearity. One may use a Taylor expansion of the LC model dispersion relation to arrive at an even more approximate version of the dispersion relationship

$$\omega^2 \approx \left(\frac{\omega_B}{2}\right)^2 \left[(kd)^2 - \frac{1}{12} (kd)^4 \right]. \quad (2.17)$$

This equation bears the first higher-ordered dispersion term above the dispersionless case (i.e. $\omega^2 = k^2 v_{group}^2$) that allows forward and reverse traveling waves. Such waves have the familiar linear propagation characteristics of

$V_{forward}e^{j(\omega t - kz)}$ and $V_{reverse}e^{j(\omega t + kz)}$. This dispersion relation can be broken into two branches for the forward and reverse directions of propagation easily by using operator notation.

Let the operator D_a represent partial differentiation with respect to variable a . Assuming linear wave propagation, equation 2.17 then represents the characteristic equation for the differential equation

$$\left(D_t^2 - \left(\frac{\omega_B d}{2} \right)^2 D_x^2 - \frac{1}{12} \left(\frac{\omega_B d^2}{2} \right)^2 D_x^4 \right) V(x, t) = 0 \quad (2.18)$$

for a forward or reverse traveling wave. Decomposition into a forward and reverse branch can then be approximated by the two differential equations

$$\left(D_t - \frac{\omega_B d}{2} D_x - \frac{\omega_B d^3}{48} D_x^3 \right) V(x, t) = 0 \quad (2.19)$$

for the forward wave and

$$\left(D_t + \frac{\omega_B d}{2} D_x + \frac{\omega_B d^3}{48} D_x^3 \right) V(x, t) = 0 \quad (2.20)$$

for the reverse wave, assuming that the term $(\omega_B d^3/48)^2 D_x^6 V(x, t)$ is small in comparison to the other terms (first order dispersion). The dispersion relationship (for the forward traveling linear wave) is now

$$\omega = \frac{\omega_B d}{2} k - \frac{\omega_B d^3}{48} k^3. \quad (2.21)$$

This dispersion relation is somewhat further from the exact CPW NLTL dispersion (equation 2.4), changing the Bragg frequency from ω_B for the LC model to $\omega_{B,new} = \omega_B (\pi/2 - \pi^3/48) \approx 0.925 \omega_B$. This is only a 7% reduction. Compare to the 20% reduction resulting from CPW to LC modeling.

With the partial differential equation 2.19, one can introduce nonlinearity and hope for a solution. Assuming a differential equation equivalent to 2.19 in the linear case

$$\frac{1}{C} \frac{\partial Q}{\partial t} - \frac{\omega_B d}{2} \frac{\partial V}{\partial x} - \frac{\omega_B d^3}{48} \frac{\partial^3 V}{\partial x^3} = 0, \quad (2.22)$$

nonlinearity is introduced by setting $Q(V) = C_0 V_0 \ln(1 + V/V_0)$ so that

$$\frac{\partial Q}{\partial t} = \frac{C_0}{1 + V/V_0} \frac{\partial V}{\partial t} \quad (2.23)$$

resulting in the Hirota [15] model for capacitance ($C(V) = C_0/(1 + V/V_0)$). So long as $1 + V/V_0 \neq 0$ it can be distributed to get

$$\frac{C_0}{C} \frac{\partial V}{\partial t} - \left(1 + \frac{V}{V_0}\right) \frac{\omega_B d}{2} \frac{\partial V}{\partial x} - \left(1 + \frac{V}{V_0}\right) \frac{\omega_B d^3}{48} \frac{\partial^3 V}{\partial x^3} = 0. \quad (2.24)$$

One further assumption is required before equation 2.24 is in a recognizable form. That is assuming that the nonlinearity factor present in the dispersion term can be neglected. Without this assumption, the mathematics become intractable. The resulting equation

$$\frac{C_0}{C} \frac{\partial V}{\partial t} - \left(1 + \frac{V}{V_0}\right) \frac{\omega_B d}{2} \frac{\partial V}{\partial x} - \frac{\omega_B d^3}{48} \frac{\partial^3 V}{\partial x^3} = 0 \quad (2.25)$$

is known as the modified KdV equation [24] in honor of D. J. Korteweg and G. deVries who studied soliton effects in water waves. Stable impulse waves are characterized by equation 2.25 that propagate in the nonlinear and dispersive medium of the NLTL.

To summarize the assumptions employed to achieve equation 2.25:

1. LC modeling of the NLTL is adequate in terms of the dispersion relationship.
2. Taylor expansion of the LC model dispersion relationship is sufficiently accurate.
3. Decomposition of the dispersive wave equation 2.18 into separate bi-directional wave equations implies $(\omega_B d^3/48)^2 D_x^6 V(x, t)$ is small.
4. Nonlinearity affects only the velocity term, leaving the dispersion term unaffected.
5. Dissipation is ignored.

The net result is a nonlinear differential equation which contains the *first order dispersion* and *first order nonlinearity* effects.

Hirota provides two important results: propagation characteristics of the soliton and a description of soliton-soliton interaction. Solitons of the form

$$V_n(t) = V_{max} \operatorname{sech}^2 \left(\frac{1.763(t - nT_D)}{T_{FWHM}} \right) \quad (2.26)$$

where $V_n(t)$ is the time dependent voltage at the n^{th} diode, V_{max} is the peak voltage, T_D is the time delay through each section of line given by

$$T_D = \frac{1}{\pi f_B \sqrt{\ln(1 + V_{max}/V_0)}} \sinh^{-1} \left(\sqrt{\frac{V_{max}}{V_0}} \right), \quad (2.27)$$

and the soliton's full width at half maximum duration T_{FWHM} is given by

$$T_{FWHM} = \frac{1.763}{\pi f_B \sqrt{\ln(1 + V_{max}/V_0)}}. \quad (2.28)$$

These equations imply that a soliton of any amplitude can exist, but a given amplitude forces a specific duration and that a larger amplitude soliton both travels faster (equation 2.27) and has shorter duration (equation 2.28) than a smaller one. These equations assume that an effective characteristic impedance $Z_{eff} = \sqrt{L/C_{eff}}$ (which one should match to the driving system, e.g. 50Ω) and the Bragg frequency $f_B = 1/\pi\sqrt{LC_{eff}}$ where $C_{eff} \equiv \Delta Q/\Delta V$ is the effective capacitance over a voltage swing of ΔV (c.f. shocks).

Soliton-soliton interaction is quite complicated quantitatively, but some important qualitative observations can be made. Solitons propagate undistorted after collisions. When two solitons collide (necessarily of differing amplitudes), the resulting nonlinear superposition has a smaller amplitude and longer duration than the larger of the two interacting solitons. The details are left with Hirota [15]. The fundamental property of solitons on NLTLs that can be used to achieve impulse compression or harmonic conversion is the fact that a waveform with longer duration than that given by equation 2.28 for its amplitude will decompose into two or more solitons of differing amplitudes and propagation velocities. At least one of these decomposed solitons will have larger amplitude and shorter duration than the input waveform [11].

The number of solitons decomposed from the input waveform is roughly equal to the product of twice the Bragg frequency and the T_{FWHM} of the input impulse ($N \approx 2f_B \cdot T_{FWHM,in}$). As an example of decomposition, simulations of an NLTL with 16 GHz Bragg frequency being driven by 6 V amplitude raised-cosine impulses of 62.5 ps (figure 2.10) and 94 ps (figure 2.11) duration are shown. For this line, $V_0 \approx 5$ V, $Z_{eff} = 50 \Omega$, $Z_0 = 75 \Omega$, and $T_{FWHM}(6V) \approx 39.5$ ps, shorter than the duration of the input impulses; decomposition into two and three solitons is predicted and simulated.

A further example of the aforementioned soliton properties is shown in figure 2.12. The NLTL is the same as in figures 2.10 and 2.11, but the input signal

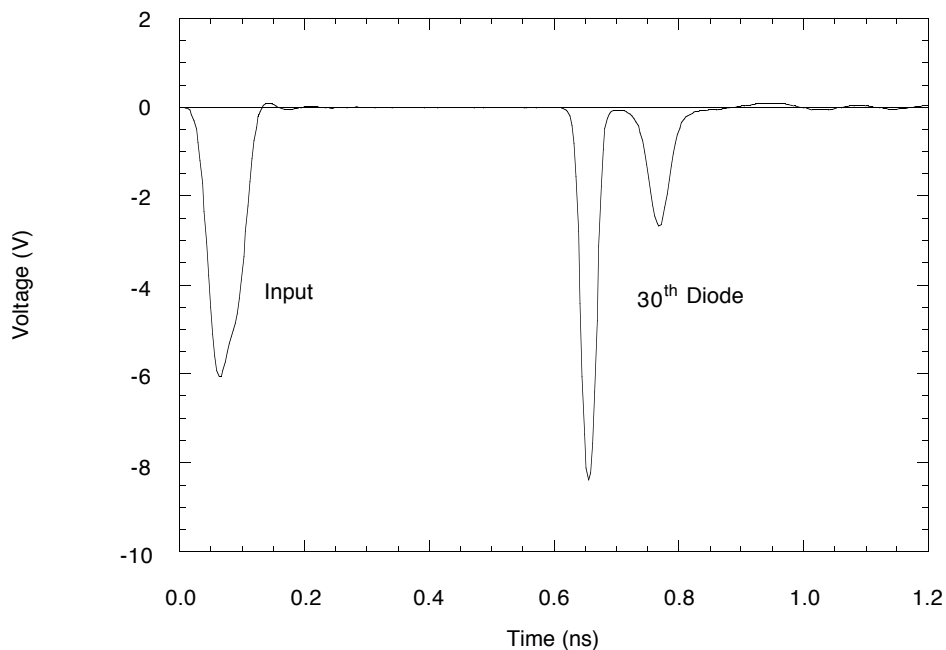


Figure 2.10: SPICE simulation of two-to-one impulse compression on a $f_B = 16$ GHz soliton NLTL. The input impulse is $6V_{p-p}$ and 62.5 ps wide while the larger output impulse is $8.4V_{p-p}$ and 27.7 ps wide after 30 diodes.

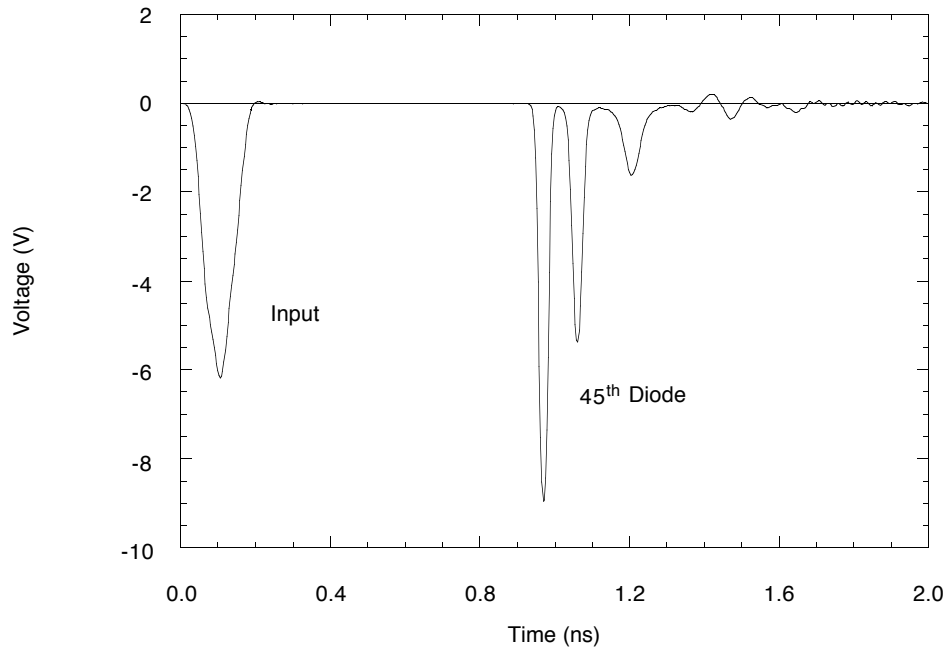


Figure 2.11: SPICE simulation of three-to-one impulse compression on a $f_B = 16$ GHz soliton NLTL. The input impulse is $6V_{p-p}$ and 93.8 ps wide while the larger output impulse is $9.0V_{p-p}$ and 28.0 ps wide after 45 diodes.

is a pair of $6V_{p-p}$, 62.5 ps wide raised cosine impulses separated by 1 ns. Just as in figure 2.10, each impulse decomposes into a pair of solitons, becoming fully separated by the 100th diode. The larger solitons propagate faster than the smaller ones. At the 241st diode, the larger soliton decomposed from the second input impulse has overtaken the smaller soliton decomposed from the first input impulse. The resulting superposition of large and small soliton has the same amplitude and width as the input impulses. By the 350th diode, both of the larger solitons have overtaken the smaller ones.

Homogeneous (constant Bragg frequency) soliton lines are useful for low order (2 to 4 times) distributed harmonic conversion (DHG) with sinusoidal drive or impulse compression [10]. As the number of decomposed solitons increases, so does the length required to allow them to separate since their amplitudes are very similar to one another. As the frequency components of the input impulse become much less than the Bragg frequency, the small dispersion limit prevails and shocks are formed. To achieve higher orders of impulse compression and harmonic conversion, inhomogeneous lines are required. Such lines do not have a constant Bragg frequency over their length.

2.4 Inhomogeneous Soliton Lines

High orders of impulse compression (or equivalently harmonic conversion) require the NLTL to have a Bragg frequency much higher than the frequency components of the input waveform. If one were to launch an impulse with 6 V amplitude and 100 ps duration into an NLTL with $f_B = 100$ GHz, a very large number (≈ 20) of secondary impulses will be decomposed from the input impulse on propagation through the NLTL. These impulses will all have nearly the same amplitude (≈ 6 V) and will all be traveling at nearly the same propagation velocity and having nearly the same impulse width (≈ 6.3 ps). It would take such a long NLTL for these impulses to separate that dissipation would reduce the output waveform to zero volts before complete separation occurred. One approaches the weak dispersion case under these circumstances, and the resulting waveform would correspond to the superposition of the large number of nearly identical solitons or equivalently a shock waveform.

In order to achieve higher ratios of impulse compression or harmonic conversion than allowed by homogeneous soliton lines, a different approach is required. A small ratio of impulse compression producing only two solitons from a single input impulse allows for a relatively short NLTL. The two output solitons have a significant difference in amplitude, hence a significant difference in velocity.

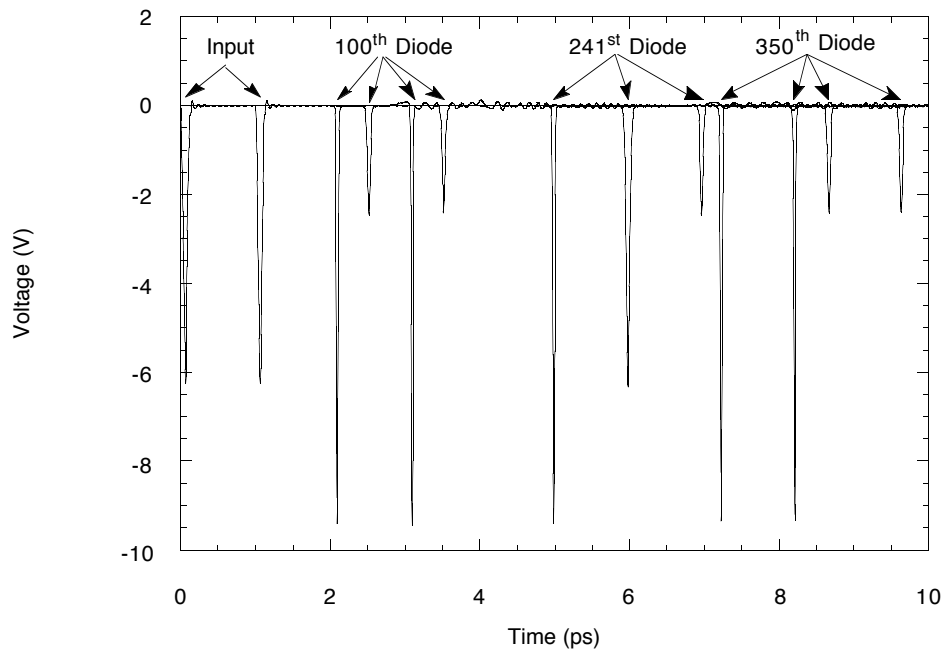


Figure 2.12: SPICE simulation demonstrating soliton decomposition and recombination on a $f_B = 16$ GHz soliton NLTL. The input is a pair of $6V_{p-p}$, 62.5 ps wide impulses separated by 1 ns. Just as in figure 2.10, each impulse separates into a pair of solitons (100th diode). Since larger solitons travel faster, the larger soliton decomposed from the second input impulse recombines with the smaller soliton separated from the first input impulse. By the 350th diode, both of the larger solitons have overtaken the smaller ones.

The output of this line can then be driven into another line with a higher f_B . By cascading successively higher Bragg lines, high orders of compression can be achieved with reasonable NLTL length. How does one go about tapering the NLTL?

Consider an NLTL with 16 GHz Bragg frequency. A raised-cosine impulse of 62.5 ps width will decompose into two solitons, and the width of the larger one will be less than 39 ps. Now consider driving the input of another NLTL having a 32 GHz Bragg frequency with the output of the first line. At that point each of the solitons from the first line will correspond to a superposition of two solitons on the second line, and compress the main impulse to less than 19 ps. The required lengths of each NLTL depends on the relative velocity of the individual solitons. This is best determined experimentally or in simulation due to the approximate form of the characteristic equations. Figure 2.13 shows the simulated output waveform of a cascaded NLTL consisting of a 30 diode, 16 GHz Bragg line being driven into a long, 32 GHz Bragg line.

One problem with the cascaded NLTL approach is that there is a substantial secondary impulse train arising from the final stage of compression. This secondary impulse train is exaggerated and of a greater extent if more stages of higher Bragg frequency NLTL are cascaded. In order to suppress this secondary impulse train and consolidate the waveform, a continuous progression of Bragg frequencies can be used [34]. Here, a very small amount of compression occurs in each section of the NLTL; but instead of maintaining a fixed f_B for several diodes, each diode section has a slightly higher f_B than the previous. The resulting waveform consists of a highly compressed impulse followed by a “tail” of superimposed, very small undesired impulses. This still does not answer the question of how to taper the NLTL’s Bragg frequency. Ideally, one should approximate the cascaded NLTLs in a continuous fashion, i.e. in simulation, find the length of line needed to fully separate a 2-to-1 compression, then take this output and drive another 2-to-1 compression line, etc. until the desired amount of compression is achieved. Then some kind of functionality for the Bragg frequency vs. either the diode number or physical line length can be determined. At this point, one can evaluate the tapering rule and vary it to optimize the compression efficiency.

Of course, one can fit just about any function to an arbitrary set of data. The easiest function to apply to the tapered NLTL is the geometric progression, particularly for computerized NLTL generation. Here, the n^{th} section of line has $f_{B,n} = f_{B,0}/k^n$ where $k < 1$. A simulation of a line having initial Bragg frequency of 16 GHz, 54 diodes, and $k = 0.956755$ is shown in figure 2.14. A more complete

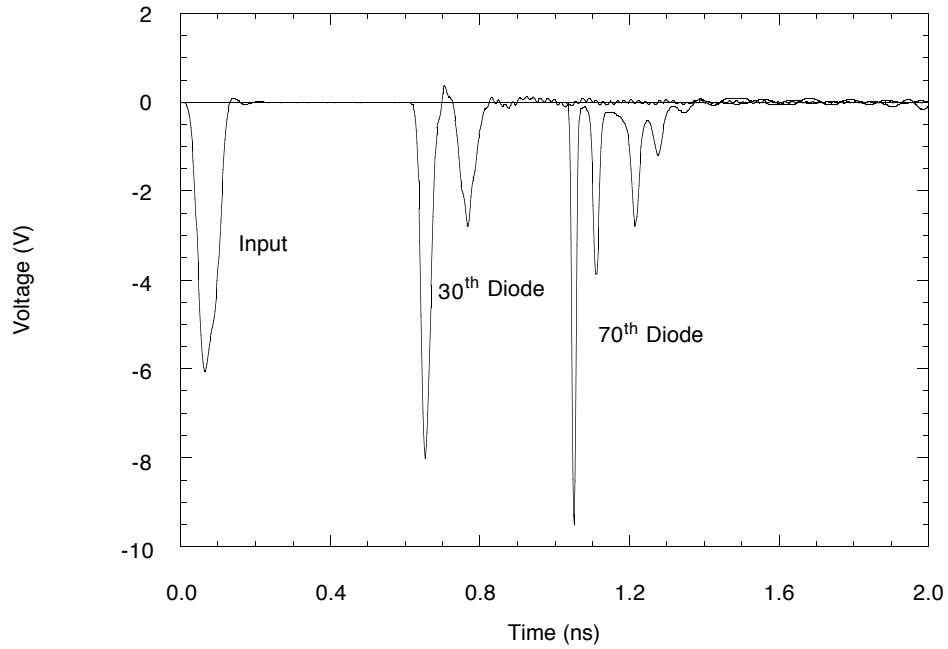


Figure 2.13: SPICE simulation of four-to-one impulse compression on a cascaded pair of soliton NLTLs having $f_B = 16$ GHz and $f_B = 32$ GHz. The input impulse is $6V_{p-p}$ and 62.5 ps wide while the larger output impulse is $9.5V_{p-p}$ and 13.8 ps wide after 70 diodes. The first line has 30 diodes.

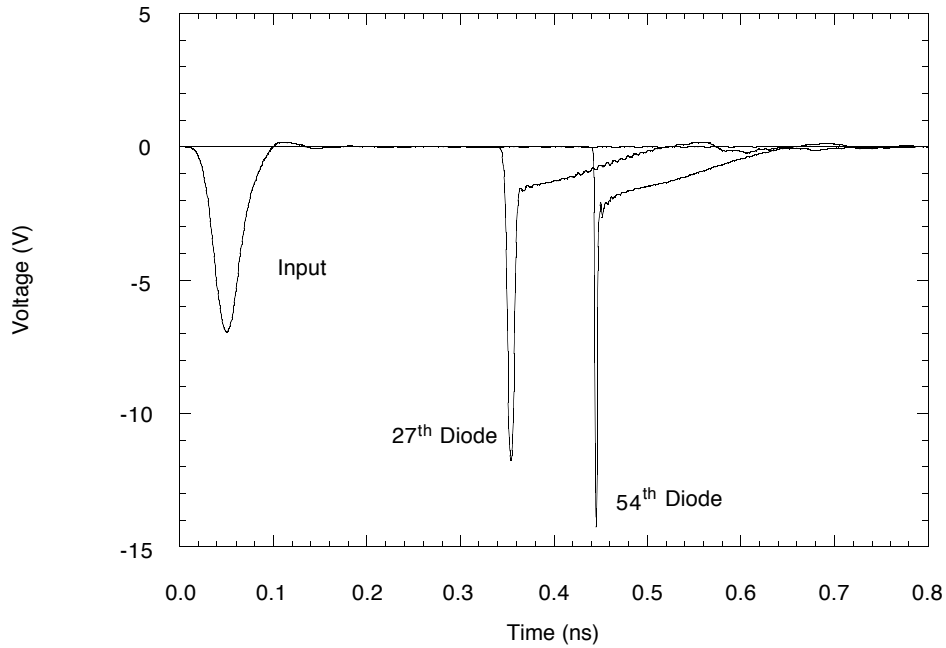


Figure 2.14: SPICE simulation of continuously tapered NLTL having $f_{B,0} = 16$ GHz, 54 diodes, and $k = 0.956755$. The input impulse is $6V_{p-p}$ and 41.7 ps wide while the output impulse is $11.9V_{p-p}$ and 2.91 ps wide. There is a 2.3 V pedestal as a result of the impulse compression.

study of the varying effects of the tapering rule (k), starting and ending Bragg frequencies, line length, and input frequency on the output waveform is done in chapter four.

2.5 Comparing Shock, DHG, and Impulse Compression NLTLs

The preceding sections describe the fundamentals of NLTL characteristics. Depending on the relationship between the input signal harmonic components and the NLTL Bragg frequency determines the mode of operation. The relationship

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between the amplitude of the signal and the characteristic of the nonlinearity also plays an important role in NLTL operation. The three modes of operation are:

1. **Shocks:** these lines are characterized as having a very high f_B to f_{signal} ratio. Discrete or continuous tapering of the Bragg frequency reduces CPW loss by allowing wider center conductors at the NLTL input. Smaller center conductors are needed for high Bragg frequencies in order to minimize layout parasitics.
2. **DHGs:** these lines typically have a single f_B or use cascaded NLTLs. The Bragg frequencies are kept at a fixed ratio to the signal. Higher harmonic conversion ratios than 4 : 1 result in reduced efficiency since all lower harmonics are also generated. These lines can also be used for high repetition rate impulse compression.
3. **Impulse Compressors:** high orders of impulse compression are best achieved by continuously tapering the f_B of the NLTL. Here, the Bragg frequency of the line is maintained just above the harmonic components of the signal.

It is important to keep in mind the method used to characterize the NLTL. The approach used here discussed soliton interactions almost exclusively. This lead to some complicated and possibly unfamiliar mathematics, but the time-domain responses of the NLTLs were fairly straightforward to characterize. One could use the frequency domain to analyze these circuits (c.f. LIBRA) by considering the dispersion, dissipation, and nonlinearity in the Fourier domain. This will lead to more accurate results (no approximations for dispersion or dissipation), at the expense of increased complexity. The soliton interaction description will be maintained throughout this dissertation, but is certainly not the only method useful for NLTL analysis.

Depending on the f_B to f_{signal} ratio, the type of NLTL can be determined. The input signal amplitude must be sufficient to excite the nonlinearity of the diodes, several times the barrier potential (or fitted characteristic voltage). Now that the NLTL theory of operation has been established, the next step is to examine the physical realization of the NLTL and the consequences of monolithic layout.

Chapter 3

The Physical NLTL

The nonlinear transmission line (NLTL) is a monolithic integrated circuit fabricated on a semiconductor substrate consisting of reverse biased Schottky diodes interconnected by coplanar waveguides (CPWs). NLTLs can be designed for a variety of applications, but all suffer from parasitic effects of lossy CPW, parasitic series resistance of diodes and other parasitics from layout. What follows is a discussion of the nature of the nonidealities of the NLTL components and reasons for choosing particular types of diodes and layout geometries.

3.1 Interconnections

The motivation for this work is generation of large amounts of power at very high frequencies and large amplitude, short duration impulses. In order to make an NLTL work at sub-mm-wave frequencies, a low loss transmission line is required. Currently, there are several types of monolithically integrable transmission lines: microstrip, CPW (figure 2.1), stripline, suspended substrate line, coplanar strips (CPS), and slotline [3]. One must consider the nature of the NLTL in order to choose the proper interconnect.

Slotline has a very low characteristic impedance, so would be a poor choice for 50Ω systems since diode loading reduces the NLTL impedance. Coplanar strips have a very high impedance, but these lines require a balanced signal. This is a problem since the sampling circuits used to measure the NLTL outputs [31] and most high frequency circuits require an unbalanced signal referenced to a common ground. Stripline requires symmetric dielectric on both sides of the conductor, hence is inappropriate for monolithic integration. Suspended substrate is very similar to microstrip, but requires the structure to be suspended

in a grounded box. This is good for packaged devices, but does not work for the much more convenient on-wafer measurements. That leaves microstrip, the industry standard, and coplanar waveguide.

Microstrip has been around for a long time [8], and there is a tremendous resource of mathematical models and simulation equivalents for different lines, discontinuities, and the like [40]. Microstrip is essentially a strip of metal on an insulator that has a back plane of grounded metal. This structure is ideal for inserting devices in series with the line, but in order to place an element in shunt, a *via hole* must be drilled through the substrate and metal plated through to make the ground connection. Via holes introduce parasitic inductance, fabrication difficulties and layout problems due to their size (on the order of 100 μm diameter). But microstrip is still the industry standard for microwave and mm-wave circuits. Due to foreseeable processing and layout difficulties, coplanar waveguide was chosen.

Coplanar waveguide offers convenient shunt (and series) element placement. CPW allows a reasonable range of impedances and has relatively low loss. Unfortunately, there are very few and inadequate CPW discontinuity models, so one must try to minimize the discontinuities and reduce sources of parasitic effects associated with NLTL layout. One effect that can be characterized but not included in many nonlinear simulations is metallic loss.

Metallic or skin loss occurs in metal due to the finite conductivity of the metal. Electromagnetic fields penetrate the metal and current flows near the surface resulting in series resistance (and inductance). Since the penetration depth varies with frequency, so does the loss. The loss in nepers is $\alpha = R_{series}/2Z_{NLTL}$ where Z_{NLTL} is the impedance of the diode loaded CPW. This formula applies only to a continuous transmission line, i.e. dispersionless where Z_{NLTL} is independent of frequency. An approximate formula for this loss is given in equation 2.13 and shown in figure 2.8, but this does not take the frequency dependent propagation effects of the NLTL into account. In order to determine these effects, one must extract the real part of γ from the *ABCD* matrices. Including equation 2.5 in $\alpha = R_{series}/2Z_{NLTL}$ is a good approximation (applicable only for skin loss, not diode loss). A computer is best suited to perform the complex algebra required. Figure 3.1 shows the difference between the loss determined from equation 2.13 with and without frequency dependent Z_{NLTL} (equation 2.5) and the complex computation for an $f_B = 100$ GHz NLTL cell using $75\ \Omega$ CPW, $Z_{LS} = 50\ \Omega$, 1 μm thick gold, 18 μm wide center conductor, and 53 μm center conductor to ground plane spacing.

Now, with a better understanding of the reasons for using CPW and the

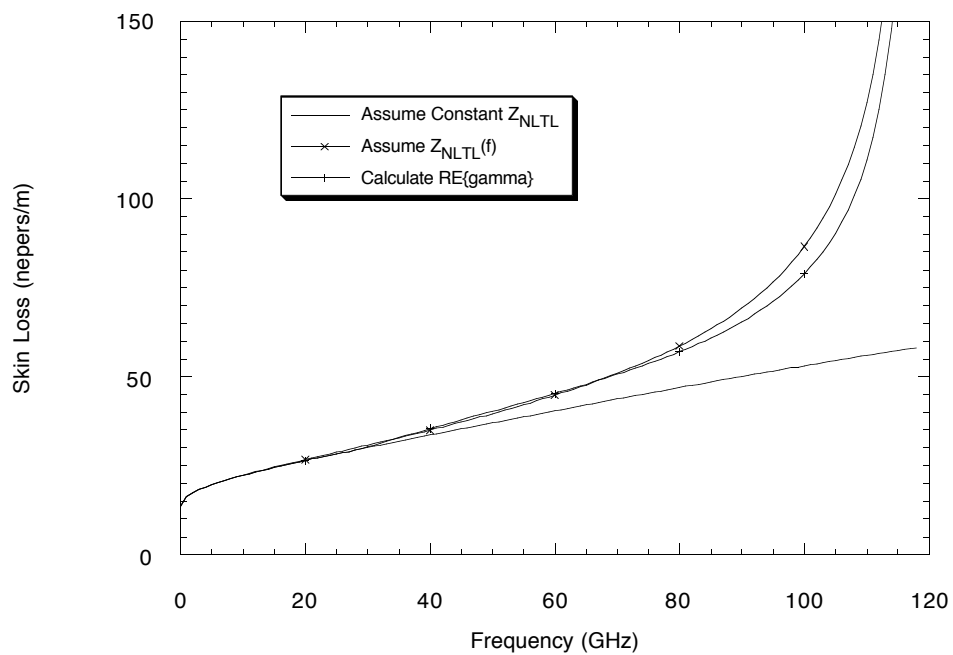


Figure 3.1: Metallic loss vs. frequency for a typical NLTL cell considering three loss models: NLTL impedance is constant with frequency, impedance varies with frequency, and $ABCD$ matrix extraction.

nature of its loss, one must choose the proper impedance. First consider a shock NLTL (one can ignore dispersion and impedance is nearly constant). The total skin loss is proportional to the number of squares of metal in the center conductor, assuming the loss due to the ground plane is negligible. A large number of squares results if the center conductor is very small (high impedance CPW) or if the center conductor is very wide since low impedance CPW necessitates a longer NLTL to achieve the same amount of compression. One can determine the total number of squares of metal for a given NLTL design as a function of interconnect impedance and find a minimum. Compression on an NLTL is the difference in delay as the reverse bias changes from minimum to maximum (T_{comp}), and a figure of merit is the *normalized* compression

$$\kappa \equiv \frac{T_{comp}}{\tau_{line}} = \frac{\tau_{max} - \tau_{min}}{\tau_{line}} \approx \frac{\sqrt{L(C_{line} + C_j(V_{high}))} - \sqrt{L(C_{line} + C_j(V_{low}))}}{\sqrt{LC_{line}}} \quad (3.1)$$

and

$$\kappa = \sqrt{a} \left[\sqrt{\frac{1}{a} + \frac{C_j(V_{high})}{C_{LS}}} - \sqrt{\frac{1}{a} + \frac{C_j(V_{low})}{C_{LS}}} \right] \quad (3.2)$$

where

$$a = \frac{C_{LS}}{C_{line}} = \left(\frac{Z_0}{Z_{LS}} \right)^2 - 1, \quad (3.3)$$

and large signal parameters are as defined in chapter two. The total number of squares of metal for an NLTL is the length divided by the width of the center conductor. The center conductor width is

$$w \approx d \sqrt{1 - \left[\frac{\frac{1}{2} \exp\left(\frac{Z_0}{30} \sqrt{\varepsilon_{eff}}\right) - 1}{\frac{1}{2} \exp\left(\frac{Z_0}{30} \sqrt{\varepsilon_{eff}}\right) + 1} \right]^4} \quad (3.4)$$

where d is the distance from ground to ground and $\varepsilon_{eff} \approx (1 + \varepsilon_R)/2$ is the effective CPW dielectric constant. One can choose a typical NLTL cell (fixing f_B , T_{comp} , d , and Z_{LS}) and vary Z_0 to find the minimum number of squares (ℓ/w).

The number of squares in the center conductor of an NLTL is

$$N = \frac{v_{CPW} T_{comp}}{w \kappa} \propto \frac{1}{w(Z_0) \kappa(Z_0)}. \quad (3.5)$$

Equation 3.5 is a very complicated function of Z_0 , but can be plotted (figure 3.2). This function is independent of f_B and inversely proportional to d . As will

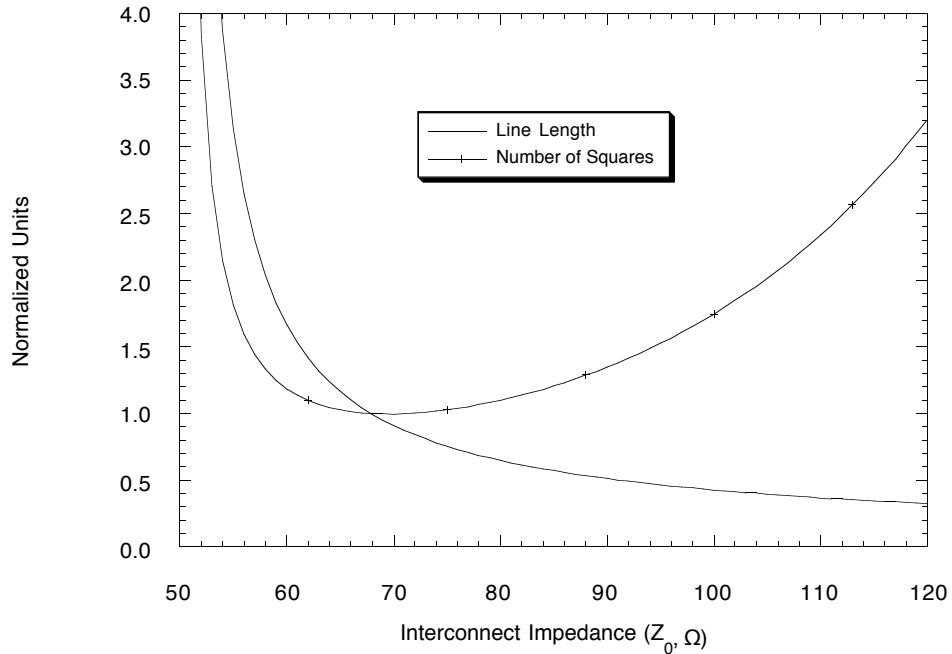


Figure 3.2: Normalized number of squares and line length for an NLTL using hyperabrupt diodes with $V_H = 14$ V and $Z_{NLTL} = 50 \Omega$.

be seen later, the Bragg frequency is indirectly related to d by layout parasitics: a higher f_B requires a smaller d to keep parasitics small. There is clearly a minimum number of squares near $Z_0 = 70 \Omega$, but as Z_0 approaches Z_{LS} , the line length increases rapidly. In early NLTL designs [4], $Z_0 = 90 \Omega$. By using a lower interconnect impedance, skin loss can be reduced but the penalty is greater length.

3.2 The Diode and its Model

NLTLs use the capacitive nonlinearity of diodes for their operation. Diode loss limits the transition speed of a shock NLTL, efficiency of a DHG, and duration of an impulse line while a greater change in capacitance over a voltage swing reduces the needed NLTL length to achieve the same nonlinear effect. There is a wealth

of information about different material systems and types of diodes using them. In order to determine the best diode for the job, consider the requirements. The substrate must have low loss since CPW will be used to make interconnections. The diodes should have very low series resistance. P-N junction diodes require two ohmic contacts while Schottky diodes only need one; since contact resistance can be very significant, particularly for the small top contact areas of the P-N diodes, Schottkys are a better choice. Reverse breakdown is also an important issue, especially for soliton devices, since the waveforms grow in amplitude on compression.

There is much more information available about GaAs properties and processing techniques than any other semiconductor material system (except for Si and Ge) and it is used in a wide variety of microwave and mm-wave ICs. Both Si and Ge have low bandgaps hence provide lossy dielectrics and leaky Schottky contacts. Silicon has a significantly lower electron mobility which limits the diode cutoff frequency. GaAs is the best choice in order to reduce the number of free variables. The doping profile can be adjusted to provide a large change in capacitance, high breakdown voltage, and low series resistance. This leads to three respective figures of merit for the NLTL diode: $\Delta C/C_{LS}$, V_{BR} , and $f_{C,LS} = 1/(2\pi R_{series}C_{LS})$. The doping profile ties all of these together.

3.2.1 Diode Nonlinearity

A uniformly doped diode has a capacitance that varies as $1/\sqrt{1 - V/\phi}$. In order to get a larger change in capacitance with voltage, the doping profile must decrease with increasing depth. This causes the depletion edge to descend more rapidly as the applied voltage increases. For example, one could place a sheet of doped material near the surface forcing the depletion edge to remain at a constant depth until some reverse bias is achieved. One then places a thick intrinsic layer, and finally a heavily doped collector. The resulting $C(V)$ curve would be a step-function transition between C_{max} and C_{min} at the chosen reverse bias voltage. There are some problems with this otherwise ideal $C(V)$ curve: very low breakdown voltage due to the sheet of charge near the surface which induces very high electric field intensities, and very high series resistance through the intrinsic region. A convenient compromise between the uniform doping and planar doping profiles that covers a continuum between the two is the exponentially tapered doping profile [25] $N_D(x_d) = N_0 e^{-x_d/x_0}$. Since the doping decreases with increasing depth, the general term *hyperabrupt* will be applied to this diode. The

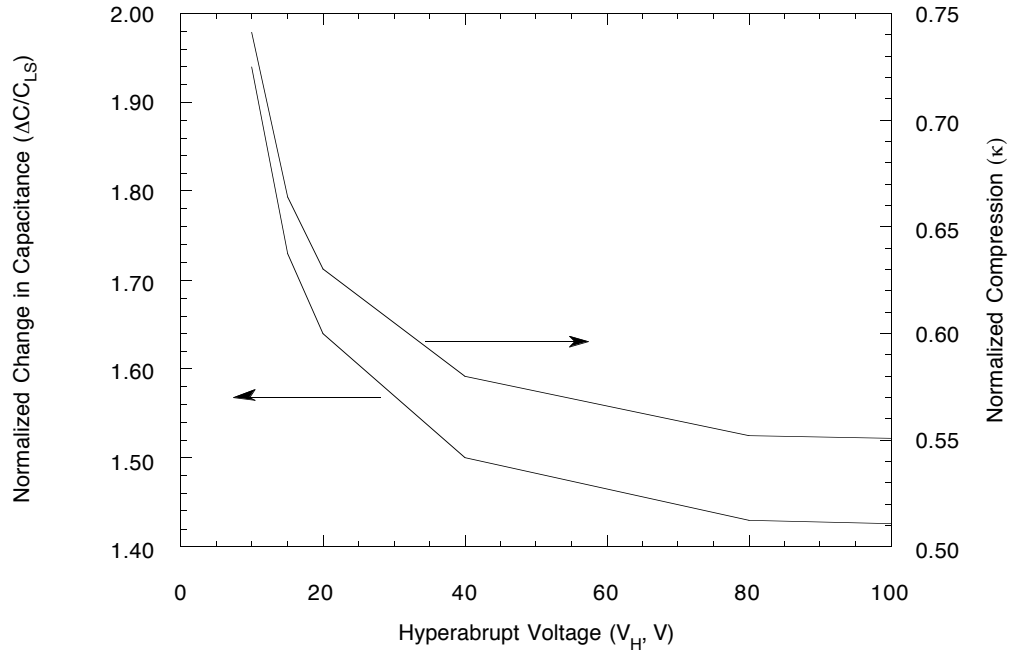


Figure 3.3: Normalized change in capacitance ($\Delta C/C_{LS}$) and compression (κ) as a function of the hyperabrupt voltage V_H assuming $Z_0 = 75 \Omega$ and a -6-0 V swing.

$V(x_d)$ relationship can be determined from equation 2.9

$$V(x_d) - \phi = \frac{qN_0x_0^2}{\varepsilon} \left[1 - e^{-x_d/x_0} (1 + x_d/x_0) \right], \quad (3.6)$$

then $C(V) = \varepsilon A/x_d(V)$ (A is the diode area). A new parameter $V_H \equiv qN_0x_0^2/\varepsilon$ is the hyperabrupt characteristic voltage and reflects the abruptness of the doping and capacitance profiles. Figure 3.3 shows the figure of merit $\Delta C/C_{LS}$ as a function of its only free variable, V_H , assuming a -6- 0 V swing.

The large-signal capacitance can be determined by integrating the depletion

region charge

$$C_{LS} = \frac{A}{V_{high} - V_{low}} \int_{x_d(V_{high})}^{x_d(V_{low})} qN_D(x_d)dx_d = \frac{qN_0x_0A \left(e^{-x_d(V_{high})/x_0} - e^{-x_d(V_{low})/x_0} \right)}{V_{high} - V_{low}}, \quad (3.7)$$

and the figure of merit is then

$$\frac{\Delta C}{C_{LS}} = \frac{\varepsilon}{qN_0x_0} \cdot \frac{(V_{high} - V_{low}) \left(\frac{1}{x_d(V_{high})} - \frac{1}{x_d(V_{low})} \right)}{\left(e^{-x_d(V_{high})/x_0} - e^{-x_d(V_{low})/x_0} \right)}. \quad (3.8)$$

3.2.2 Series Resistance and Loss

Figure 3.4 shows a diagram of a typical Schottky diode and its parasitic resistances. Diode active areas can be isolated from one another either by the mesa process or by ion implantation. The mesa process causes large differences in surface height and devices are typically large in area. The ion implantation process renders exposed areas semi-insulating due to generation of midband defects and devices can be very small ($1 \times 4 \mu\text{m}$ diodes have been successfully processed). Ion implantation was chosen since a planar surface allows fewer transmission line discontinuities. One disadvantage of ion implantation is that there is a limited depth the ions can penetrate, about $1.4 \mu\text{m}$. A detailed explanation of the ion implant will be given in chapter four.

As shown in figure 3.4, R_N is the resistance through the undepleted diode, R_{SP} is the spreading resistance, R_{N+} is the buried N+ layer resistance, and R_C is the contact resistance. The total resistance $R_{series} = R_N + (R_{SP} + R_{N+} + R_C)/2$. In terms of the diode dimensions, the total series resistance per unit length of the diode is

$$R_{series} \approx \frac{\int_0^{T_N} \rho(N_D(x_d)) dx_d}{\lambda_S} + \frac{1}{2} \left(\frac{R_{sheet}\lambda_S}{24} + R_{sheet}\lambda_O + R_{contact} \right) \quad (3.9)$$

where $\rho(N_D(x_d))$ is the resistivity of GaAs as a function of the doping concentration, T_N is the hyperabrupt layer thickness, λ_S is the Schottky width, λ_O is the Schottky-ohmic spacing, R_{sheet} is the sheet resistivity of the N+ collector layer, and $R_{contact}$ is the contact resistance in $\Omega \cdot \mu\text{m}$. By fitting curves found in standard semiconductor references [7], one can fit $\rho(N_D(x_d))$ to an integrable form. This gives a pessimistic (high) value for the undepleted diode resistance

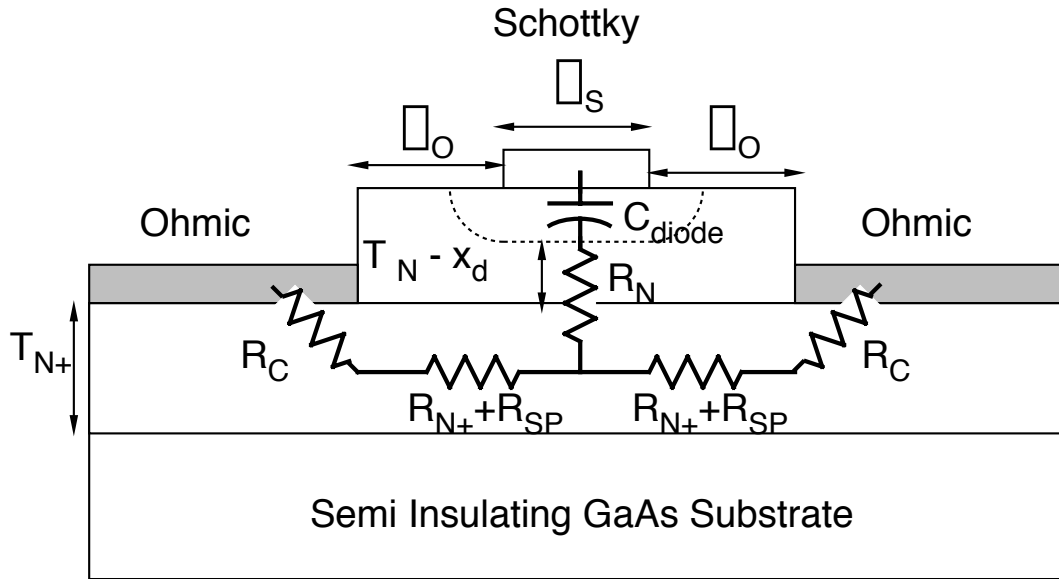


Figure 3.4: Cross sectional view of the ion implant isolated Schottky diode showing geometrical structure and sources of parasitic resistances.

(R_N) by integrating from the zero bias depletion depth through the rest of the diode. There are several independent variables: λ_S , λ_O , T_N , T_{N+} and R_{sheet} and ρ which are functions of the doping. By choosing a particular punch through voltage (voltage at which the hyperabrupt layer is completely depleted), the hyperabrupt layer thickness can be determined and $T_{N+} = 1.4\mu\text{m} - T_N$.

The important factor here is the large signal diode cutoff frequency $f_{C,LS} = 1/(2\pi R_{series} C_{LS})$ which is a function of V_H , N_0 , λ_S , λ_O , R_{sheet} , $R_{contact}$, and the doping. This figure of merit is plotted as a function of N_0 for various values of V_H , λ_S , and λ_O assuming T_N corresponds to a depletion depth for 7 V reverse bias, $R_{sheet} = 7.5\Omega/\square$, and $R_{contact} = 20\Omega \cdot \mu\text{m}$. Figure 3.5 shows $f_{C,LS}$ vs. surface doping for fixed design rules and several values of V_H . Figures 3.6–3.8 show how design rules effect the cutoff frequency. Clearly, heavier doping, more uniform epi, and smaller design rules provide the lowest series resistance, but the price paid is low breakdown voltage, low diode nonlinearity, and difficult processing. The compromise that was used is $V_H = 14\text{ V}$, $N_0 = 2 \cdot 10^{17}\text{cm}^{-3}$, $\lambda_S = 2\mu\text{m}$, and $\lambda_O = 3\mu\text{m}$ providing $f_{C,LS} = 2.0\text{ THz}$ and $\kappa = 0.745$ using 75Ω interconnects.

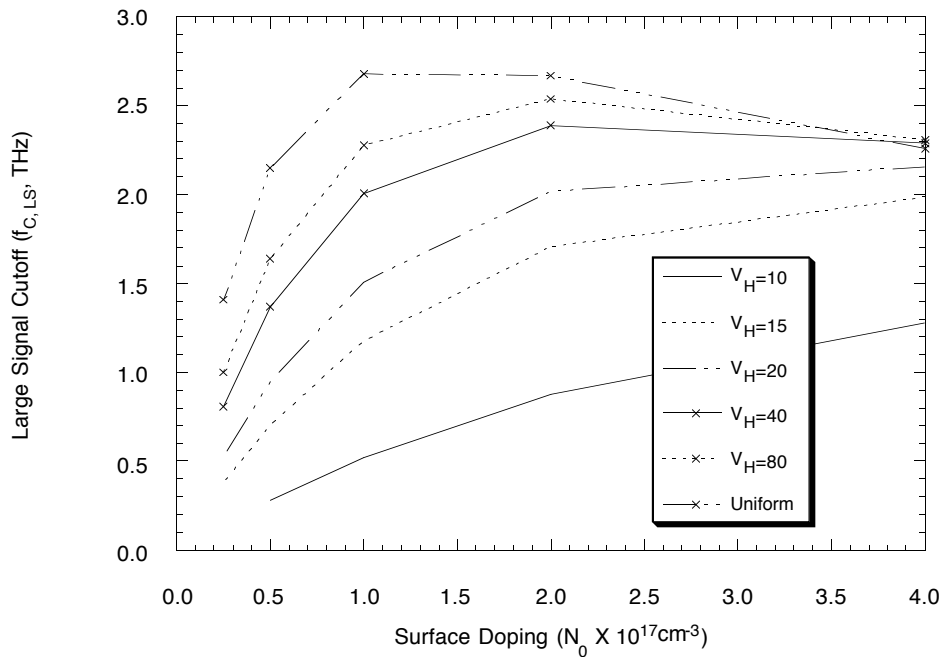


Figure 3.5: $f_{c,LS}$ vs. surface doping for several values of V_H using $\lambda_S = \lambda_O = 3\mu\text{m}$. Larger values of V_H can allow larger cutoff frequencies.

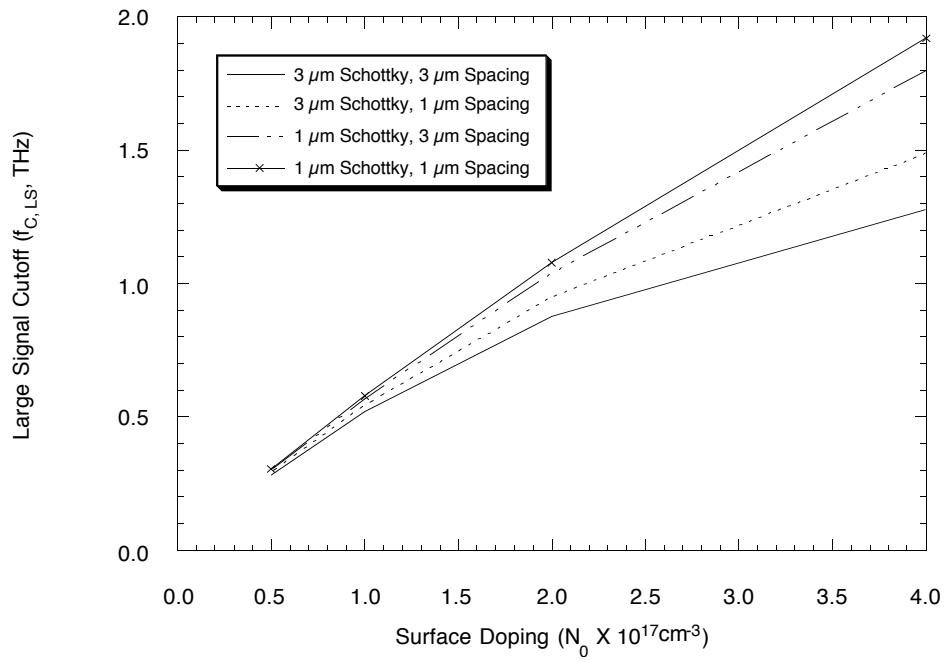


Figure 3.6: $f_{C,LS}$ vs. surface doping for $V_H = 10$ V and four different combinations of design rules.

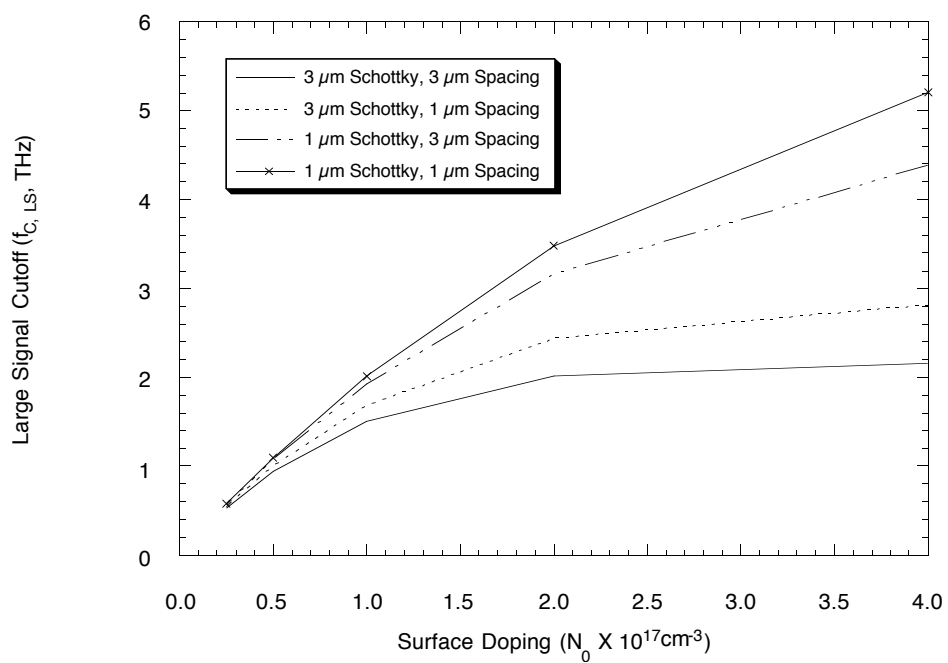


Figure 3.7: $f_{c,LS}$ vs. surface doping for $V_H = 20$ V and four different combinations of design rules.

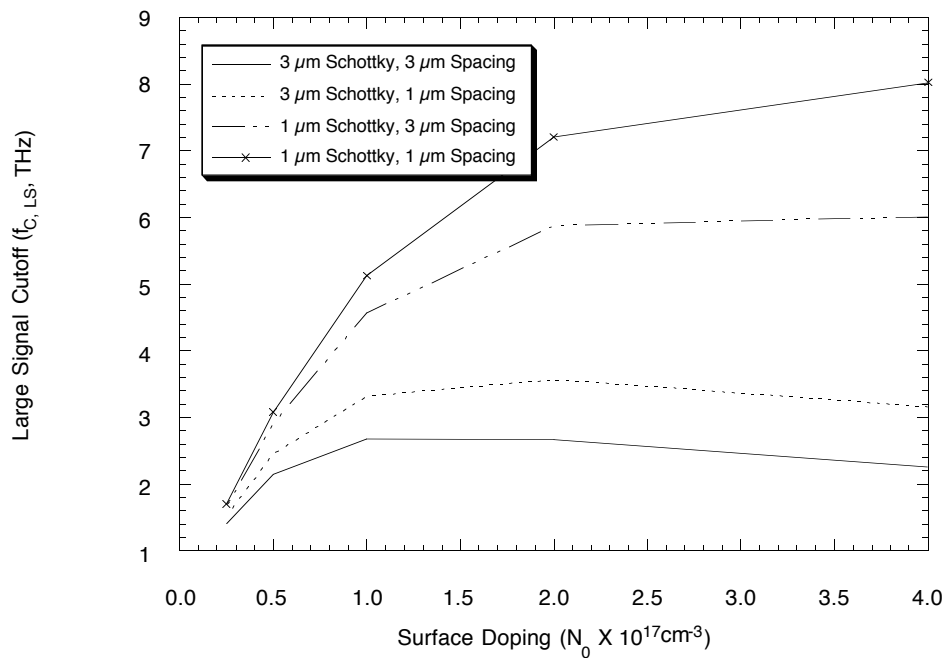


Figure 3.8: $f_{c,LS}$ vs. uniform doping for four different combinations of design rules.

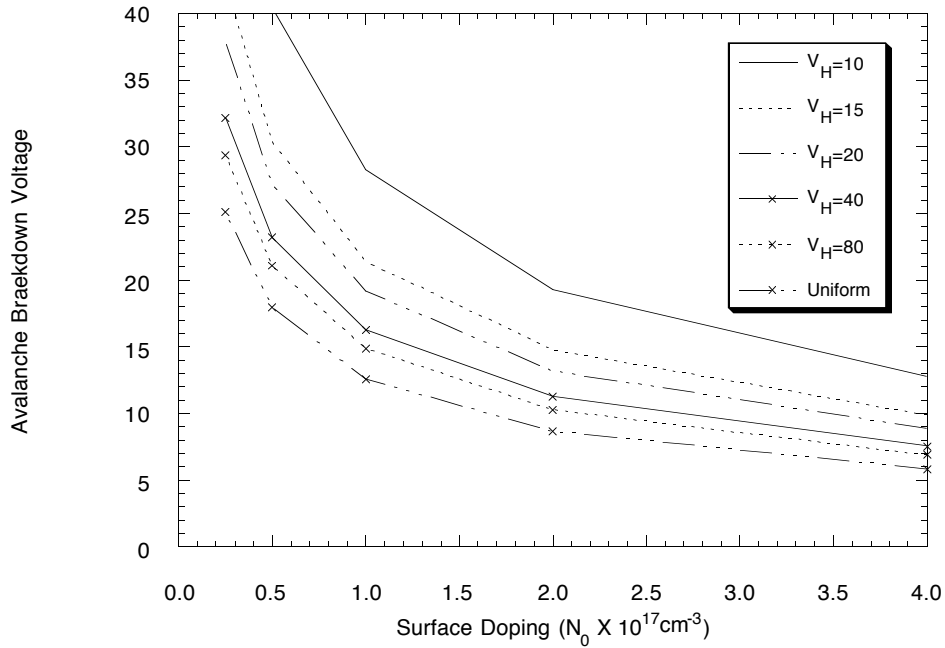


Figure 3.9: DC breakdown voltage vs. surface doping for several values of V_H .

3.2.3 Avalanche Breakdown

Avalanche breakdown occurs when the electric field within the device accelerates electrons so much that they ionize and multiple collisions with other electrons occur and the scattered electrons become themselves ionized. This is called impact ionization. For a uniform diode, breakdown voltages are tabulated. By determining the field within the device as a function of applied voltage ($\vec{\nabla}V = -\vec{E}$ and $\vec{\nabla}\vec{E} = \rho/\epsilon$) one finds the peak field magnitude at the metal-semiconductor interface. One can then approximate the breakdown field vs. doping relationship [7] as some function and find out at what voltage the interface field magnitude equals the breakdown field for the surface doping. This voltage will then be V_{BR} , the breakdown voltage which is plotted in figure 3.9 for a variety of diode designs.

The above discussion considers the static case. Consider the rapid transition of the NLTL impulse compressor where the waveform peaks in the picosecond

time frame. Since electrons must build up successive collisions to reach noticeable currents, some delay can be expected. If the buildup time is slow, the NLTL voltage can exceed V_{BR} . Borrowing some analysis from impact ionization avalanche transit time diodes (IMPATT) [7], the dynamic response of avalanche breakdown can be approximated. The total current through the device is the sum of electron and hole currents

$$I = I_n + I_p = qv_{sat}n + qv_{sat}p. \quad (3.10)$$

The continuity relationships are

$$\frac{\partial n}{\partial t} = \frac{1}{q} \frac{\partial I_n}{\partial x} + \bar{\alpha}v_{sat}(n + p) \quad (3.11)$$

for electrons and

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \frac{\partial I_p}{\partial x} + \bar{\alpha}v_{sat}(n + p) \quad (3.12)$$

for holes, assuming that the displacement current is negligible (i.e. $\partial E/\partial t \ll qv_{sat}(n+p)/\epsilon$), the electrons and holes have the same ionization rate ($\alpha_n = \alpha_p = \bar{\alpha}$), electrons travel at the saturated velocity (v_{sat}) in the ionized region, and that there is some depth over which impact ionization is occurring (x_A). Combining equations 3.10, 3.11, and 3.12 results in

$$\frac{\partial n}{\partial t} + \frac{\partial p}{\partial t} = \left(\frac{\partial I_n}{\partial t} + \frac{\partial I_p}{\partial t} \right) \frac{1}{qv_{sat}} = \frac{1}{q} \left(\frac{\partial I_n}{\partial x} - \frac{\partial I_p}{\partial x} \right) + 2\bar{\alpha}v_{sat}(n + p). \quad (3.13)$$

Now, assuming $\partial I_n/\partial t + \partial I_p/\partial t = \partial I/\partial t$, equation 3.13 can be reduced to

$$\frac{1}{v_{sat}} \frac{\partial I}{\partial t} = \left(\frac{\partial I_n}{\partial x} - \frac{\partial I_p}{\partial x} \right) + 2\bar{\alpha}I. \quad (3.14)$$

By integrating with respect to x over the ionization region ($x = 0$ to $x = x_A$) one obtains

$$\tau_A \frac{\partial I}{\partial t} = [I_n - I_p]_0^{x_A} + 2\bar{\alpha}x_A I \quad (3.15)$$

where $\tau_A = x_A/v_{sat}$ is the characteristic avalanche time. Assuming that diffusion occurs outside the avalanche region ($n\mu E \gg D_n \partial n/\partial x$), the boundary conditions $I_p = I_{p,s}$ and $I_n = I - I_{p,s}$ at the metal-semiconductor interface, and $I_n = I_{n,s}$ and $I_p = I - I_{n,s}$ at the avalanche region edge (x_A) provide two solutions:

$$I(t) = \frac{I_s}{1 - M} \left(1 - M e^{-t/\tau_A} \right) \quad (3.16)$$

if $V < V_{BR}$ and $M < 1$, or

$$I(t) = \frac{I_s}{M-1} (Me^{t/\tau_A} - 1) \quad (3.17)$$

if $V > V_{BR}$ and $M > 1$. The subscript s indicates saturation currents and V_{BR} occurs when $M = 1$ which is defined as

$$M \equiv \bar{\alpha}x_A \equiv \int_0^\infty \alpha(E(x_d))dx_d. \quad (3.18)$$

Equation 3.16 exhibits current decaying with time (decreasing ionization) while equation 3.17 indicates ionization buildup. One can approximate $\alpha(E)$, perform the integration, and find the avalanche characteristic time τ_A .

For my standard diode, $\tau_A \approx 0.4$ ps and decreases very slowly with increased reverse bias; however, this is not the time required for substantial avalanche current buildup. The current grows exponentially with time at a rate defined by τ_A . One must define a critical current, I_{crit} (occurring at time t_{crit}), which represents the threshold between acceptable and unacceptable current magnitudes. The critical time is

$$t_{crit} = \tau_A \ln \left(\frac{1}{M} + \frac{M-1}{M} \frac{I_{crit}}{I_s} \right) \quad (3.19)$$

and varies only slightly with increasing reverse bias. Figure 3.10 shows how t_{crit} varies with increased reverse bias and different ratios of I_{crit}/I_s . For the standard hyperabrupt diodes, t_{crit} is 4–5 ps. This is a surprisingly long time which suggests that the impulse peak can indeed exceed the breakdown voltage for a short period of time; however, it is short enough that breakdown cannot be ignored.

3.2.4 Electron Velocity Limits

The depletion edge under the Schottky contact must move as the applied voltage changes, corresponding to electron movement caused by the applied electric field. If the applied voltage changes rapidly, the depletion edge must move rapidly. Since the electrons must move at some finite velocity, this imposes a “slew rate” limit where a voltage transition has a minimum duration or maximum rate:

$$\left. \frac{\partial V}{\partial t} \right|_{\max} \approx \frac{\partial V}{\partial x} \cdot \left. \frac{\partial x}{\partial t} \right|_{\max} \quad (3.20)$$

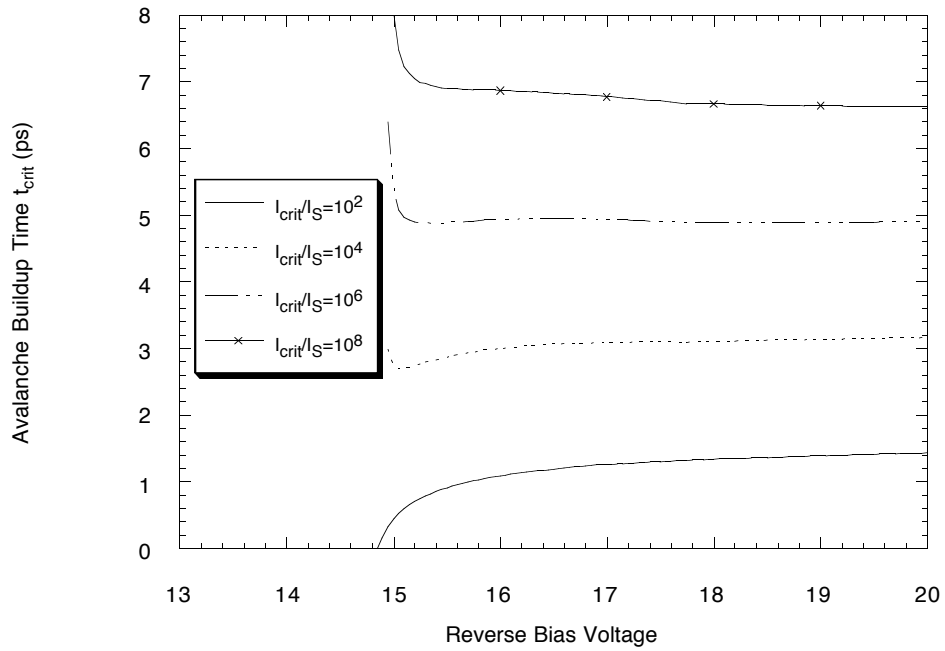


Figure 3.10: Avalanche buildup time (t_{crit}) for the standard $V_H = 14$ V, $N_0 = 2 \cdot 10^{17} \text{cm}^{-3}$ diode. I_S is typically $1 \text{ pA}/\mu\text{m}^2$, so a reasonable value for I_{crit}/I_S is 10^5 – 10^6 giving t_{crit} a value of 4–5 ps.

where $\partial V/\partial x$ can be determined from equation 3.6.

Under very small-signal excitation, electrons move as dielectric relaxations and the effective velocity is close to the dielectric velocity ($c/\sqrt{\epsilon_R}$). In bulk material (large dimensions, times $\gg 1$ ps), electrons follow a predictable velocity vs. electric field characteristic which indicates a saturated velocity at high field intensities near 10^5 m/s. The NLTL imposes conditions which match neither situation. The time scale is ≈ 1 ps and voltages are fairly large. Under large signal excitation, electrons can move at very high rates over short distances. Electron velocities of $8 \cdot 10^5$ m/s have been observed over distances of $\approx 200 \text{ \AA}$ [27] in very short gate-length transistors.

The fastest NLTL waveforms observed have shown electron velocities on the order of $2 \cdot 10^5$ m/s. This clearly indicates that the electrons can move faster than the electron saturation velocity in an NLTL. The actual electron transport dynamics are not easily determined but appear to impose no limit on the observed waveform. If the electron transport did impose a limit, one should observe an initial high electron velocity followed by a slower bulk response. The observed waveforms show smooth transitions. As the speed of the NLTL increases, electron velocity limits may be observed and impose a limit.

3.3 The NLTL Cell

The NLTL cell consists of a diode connected between the center conductor and ground at the junction between two sections of CPW. There are many possibilities for a good layout, but two configurations have been examined carefully. These are the “signal” diode (figure 3.11) and the “ground” diode (figure 3.12). Both designs have additional capacitance in shunt with the diode and a parasitic inductance in series with the diode. These parasitics arise from the metal fins used to connect the diode to CPW and in the case of the ground diode, additional inductance arises from the notches in the ground plane. There are also other propagating modes that can exist on either NLTL layout: coplanar strip mode (the two ground planes at different potentials), microstrip mode (potential difference between CPW ground and back plane ground), and slab mode (guided wave propagating through the substrate). Energy can be coupled from the desired CPW mode into any of the other modes under the proper conditions.

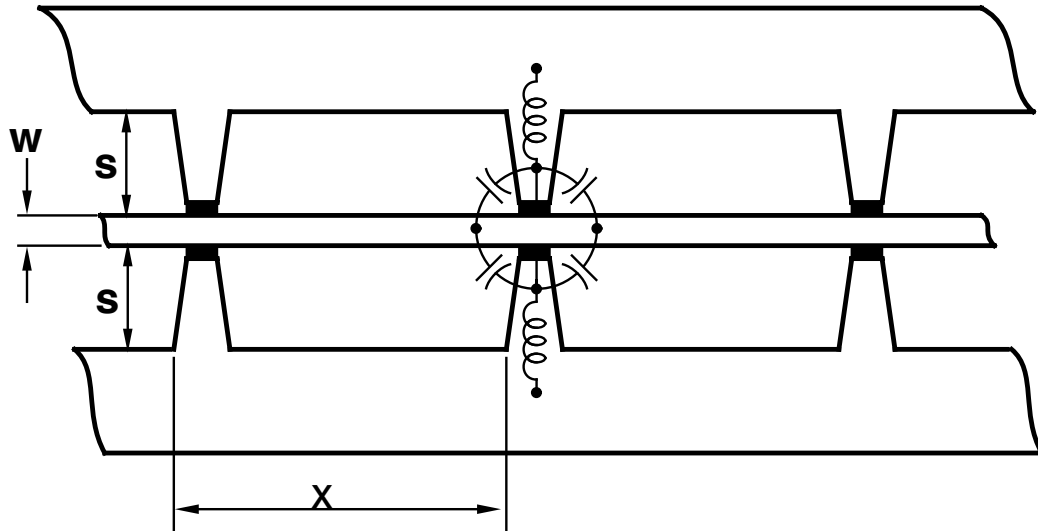


Figure 3.11: Diagram of a signal diode NLTL cell showing parasitic inductance and capacitance from layout.

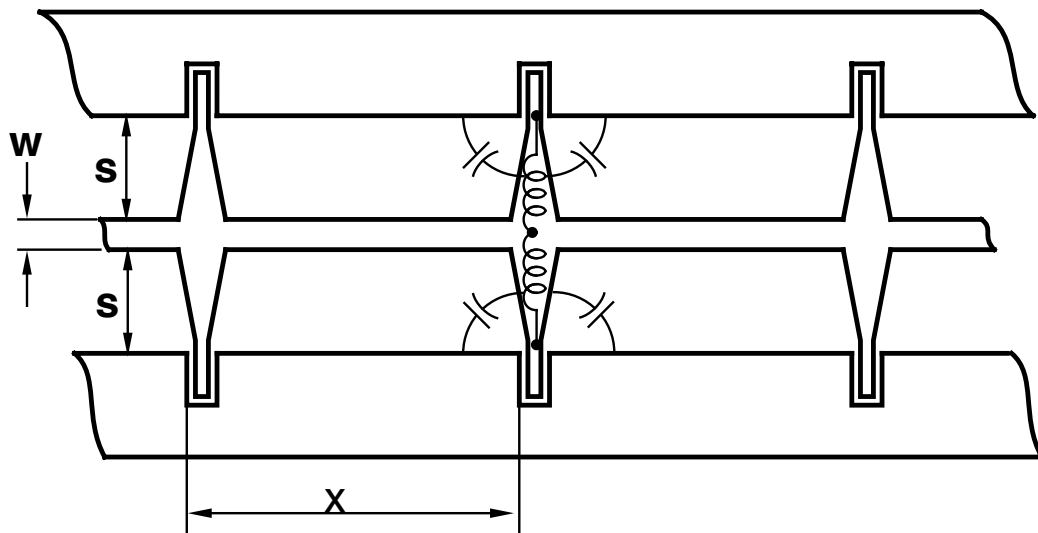


Figure 3.12: Diagram of a ground plane diode NLTL cell showing parasitic inductance and capacitance from layout.

3.3.1 Undesired Modes and Radiation

Coupling from one mode to another by means of matched velocities is termed radiation and can cause resonances or loss. Radiation can occur between modes only if the propagation velocities of the modes are the same or if the boundary conditions allow its excitation. If one assumes a perfectly balanced CPW, diode loading, and launch, only a CPW mode will be excited. Broadband velocity matching only occurs between the CPW mode and oblique slab modes if the CPW velocity is greater than that of the slab mode. Radiation loss varies as

$$\alpha_{rad} \propto \left(1 - \left(\frac{c}{\sqrt{\varepsilon_R} v_{NLTL}}\right)^2\right)^2 \approx \left(1 - \left(\frac{Z_0}{Z_{LS}}\right)^2 \left(\frac{1 + \varepsilon_R}{2\varepsilon_R}\right)\right)^2 \quad (3.21)$$

representing a semi-cone of radiation propagating into the substrate at an angle $\theta = \cos^{-1} \left((Z_0/Z_{LS}) \sqrt{(1 + \varepsilon_R)/2\varepsilon_R} \right)$. While solitons do not propagate at the same speed as shocks, one can determine their speed based on the Bragg frequency and amplitude and calculate the radiation loss (if they travel faster than the slab mode) with equation 3.21. Clearly, if $v_{NLTL} < c/\sqrt{\varepsilon_R}$, θ is imaginary and no radiation loss will occur. For most NLTL designs, this is the case and radiation loss (into the slab mode) can be ignored.

Coupling to other propagating modes can be a problem. If the diodes are not symmetric in a ground diode cell or the center conductor is not in the exact center, the CPS mode can be excited. This mode is suppressed in the signal diode cell since the buried $N+$ layer ties the two ground planes together. The CPS mode can be suppressed further by using air bridges to tie the two grounds together.

The microstrip mode can be excited if there is a difference between the ground potential of the microwave generator and the back plane. It can also arise from resistive drops in the ground plane due to forward conduction or breakdown in the diodes. This mode can be suppressed by using a microwave absorber instead of metal for the back plane, but this will also attenuate the CPW mode slightly. In general, one should compare the waveforms with and without a microwave absorber back plane to determine if there is a problem.

3.3.2 Layout Parasitics

The parasitic shunt capacitance and series inductance arising from the diode fins is difficult to compute. An electromagnetic simulation is required for all but the crudest approximations. Since the precise dimensions of the NLTL cell influences

the parasitic component values, only generalizations will be made. Uddalak Bhattacharya has done some electromagnetic simulations of both cell structures using Sonnet Software [40]. Due to the preliminary nature of the simulations, he has only modeled the shunt effects of the fins, omitting the inductance in series with the diode. He has found that a signal diode cell designed for $f_B = 800$ GHz, $Z_{LS} = 50 \Omega$, $d = 40 \mu\text{m}$, and $Z_0 = 90 \Omega$ has roughly the same parasitic capacitance (≈ 1.1 fF) as a ground diode cell designed for $f_B = 600$ GHz, $Z_{LS} = 50 \Omega$, $d = 48 \mu\text{m}$, and $Z_0 = 75 \Omega$. Since the value of capacitance is comparable, the effects will be more noticeable for the $Z_0 = 90 \Omega$ line than the $Z_0 = 75 \Omega$.

The parasitic capacitance has readily characterized effects: increase in C_{LS} and decrease in $\Delta C/C_{LS}$. This will reduce the normalized compression, impedance, and Bragg frequency of the NLTL cell while increasing the loss from both diode and CPW. Minimization of the parasitic capacitance both improves performance and reduces the need for modeling its effects.

Both fin and ground plane notch sources of parasitic inductance can be lumped together in series with the diode. This series inductor increases the impedance of the diode as frequency increases, reducing the effective cutoff frequency, increasing the loss, and disturbing the dispersion of the structure. Unfortunately, only a rough approximation of the series inductance can be given since a complete circuit including the shunt connected diode is required in the electromagnetic simulation to give this inductance a precise value. The inductance of a rectangular piece of metal on $\mu_R = 1$ material in henrys is

$$L_{fin} \approx 2 \cdot 10^{-7} \ell \left(\ln \left(8.9686 \frac{\ell}{w} \right) + \frac{w}{3\ell} - 1.25 \right) \quad (3.22)$$

where w is the width and ℓ is the length of the rectangle in meters. The ground plane notches can be modeled as short-circuited slot lines. In order to get a feel for the effects of series inductance, figures 3.13 and 3.14 shows the imaginary and real parts of γ vs. frequency for a $f_B = 100$ GHz, $Z_{LS} = 50 \Omega$, $Z_0 = 75 \Omega$, and standard diode NLTL cell with typical parasitic inductance including all nonideal effects except parasitic capacitance. Again, Bragg frequency is reduced and loss increases.

In order to minimize parasitic capacitance inductance, the CPW dimensions must be reduced. Unfortunately, this has the detrimental effect of increasing skin loss. There is a tradeoff between the two effects. If the diode spacing is small (high f_B), one must use a small width CPW which increases skin loss but maintains small layout parasitics. By using electromagnetic simulation on

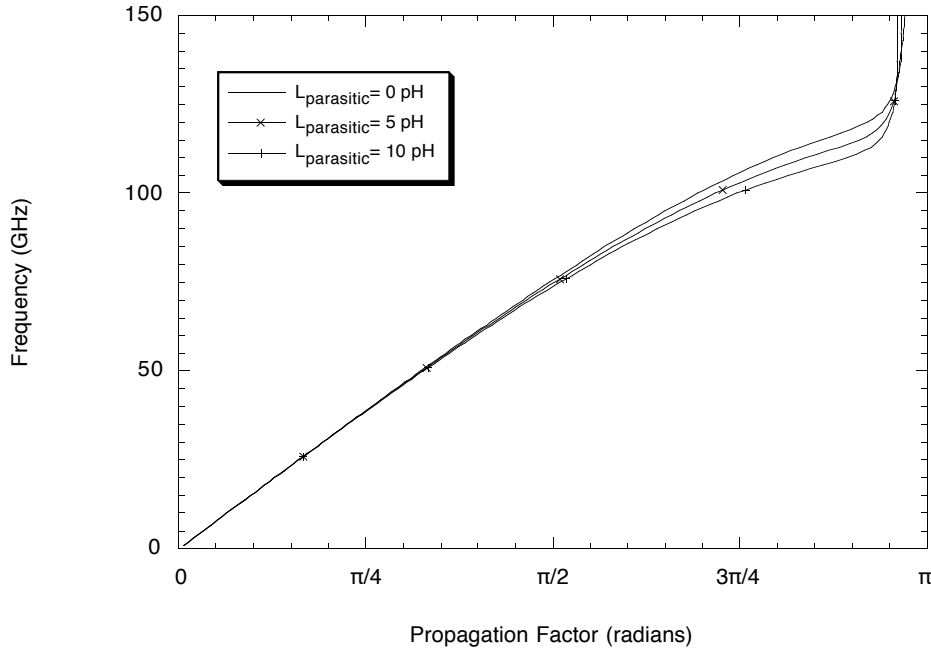


Figure 3.13: Propagation constant ($\beta\ell$, radians) vs. frequency showing the effect of added series inductance. The Bragg frequency is reduced and loss increases.

several CPW dimension and Bragg frequency cells, some generalizations could be made, but would this procedure is very arduous. Lacking this, one must use some other rule. My rule is that if the diode spacing is less than $1.5 \times d$, then d must be incrementally reduced. This can be done to its lithographic limit ($2 \mu\text{m}$), which sets a limit to the maximum f_B .

3.4 Fundamental Limits

All of the undesirable effects discussed so far can be controlled and modeled. If one takes into account the layout parasitics associated with the design, recalculates the pertinent parameters (f_B , loss, etc.), then redesigns the cell, one can achieve the desired characteristics through iteration. This is a laborious procedure but may be necessary as layout parasitics become large perturbations.

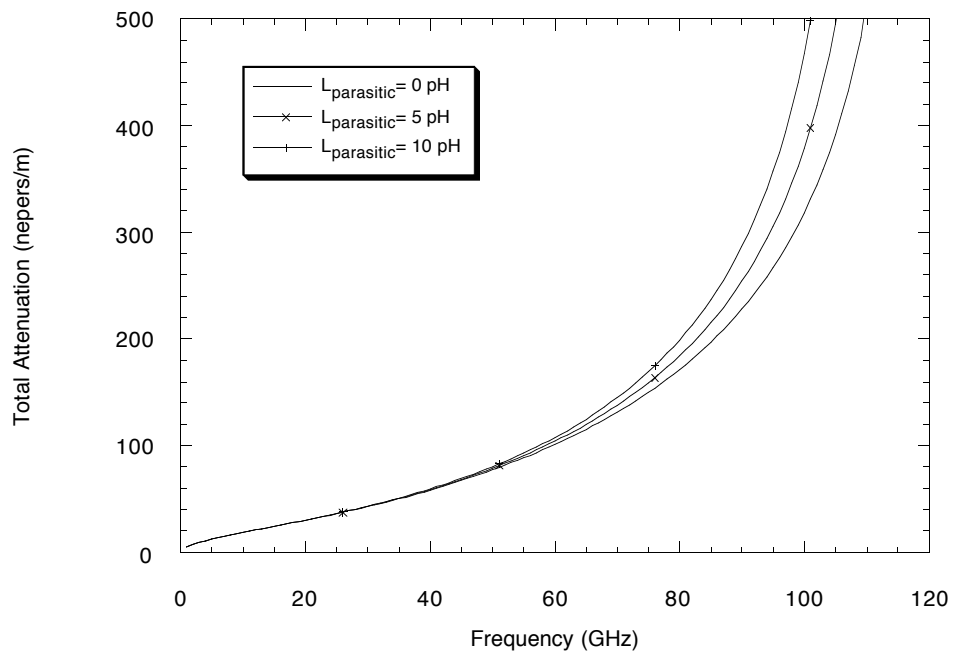


Figure 3.14: Dissipation (α , nepers/m) vs. frequency showing the effect of added series inductance. The Bragg frequency is reduced and loss increases.

The effects of diode cutoff frequency have been discussed and one can choose devices with cutoff frequencies well into the THz regime; but in this regime semiconductor materials may not be able to be considered as lumped resistors as discussed in equation 3.9. Another problem is the ability to place a diode between transmission line sections. For very high Bragg frequencies, diode areas and spacings become impractically small and parasitic effects can dominate the cell. Dissipation is also an issue for very high Bragg frequency lines since waveguide dimensions must become very small.

3.4.1 Material Properties at THz Frequencies

Semiconductor materials have much different properties at THz frequencies than at DC. Dielectric relaxation and electron scattering effects, though very fast in their responses, must be considered as time scales are reduced [12]. The skin effect can also reduce the cutoff frequency. But at what frequency should one consider modifying the DC models? The combination of dielectric relaxation

$$\omega_d = \sigma/\varepsilon \quad (3.23)$$

(σ is the conductivity and ε is the dielectric constant) and electron scattering

$$\omega_s = q/(m^*\mu_n) \quad (3.24)$$

(m^* is the electron effective mass and μ_n is the electron mobility) causes a classical plasma resonance from the “inertial inductance” (scattering) and “displacement capacitance” (relaxation). The plasma resonance frequency is the geometric mean of the scattering and dielectric relaxation frequencies $\omega_p = \sqrt{\omega_d \cdot \omega_s}$ and it has a quality factor $Q = \sqrt{\omega_d/\omega_s}$.

This implies that each resistor in figure 3.4 must be replaced with a resonant “tank” (*RLC*) circuit at sufficiently high frequencies. For my standard diode, the plasma resonance occurs at 24 THz with a Q of 12 in the N+ layer, but in the diode layer (assuming 10^{17} cm^{-3} doping) it occurs at 2.4 THz with a Q of 3. The DC model predicts a 2.8 THz cutoff, so is not accurate. If a diode were designed with a much higher DC cutoff (e.g. heavy uniform doping), plasma resonance would be a much more severe limitation. Diodes can operate above the plasma resonance frequency, but the NLTL is a broadband device and any null in the response above the excitation frequency will inhibit operation. In order for the NLTL to produce THz signals, an alternative material system and/or very heavy doping may be required.

Another issue is the skin effect occurring in the semiconductor itself. This effect causes the current to flow in a frequency dependent thickness $\delta = \sqrt{2/(\omega\mu_0\sigma)}$ of the material. For my standard diode, $\delta = 1.4 \mu\text{m}$ at 1 THz. This is larger than the thickness of the $N+$ layer, so again in my diode is not a limiting issue since total loss is very large by 500 GHz. As diode cutoff frequencies increase, the skin effect will become a greater problem.

3.4.2 Limits

Given the flexibility of design parameters, what will set the limit to step function or impulse speed? One can design a diode with at least a 10 THz resistive cutoff that has reasonable breakdown, a high slew rate limit, and moderate nonlinearity. Plasma resonance will change the THz response, reducing cutoff (3–5 THz). The more limiting NLTL component is the CPW itself. On GaAs, $v_{CPW} = 113 \mu\text{m}/\text{ps}$ and for a typical set of parameters $\ell \approx 240 \mu\text{m} \cdot 100 \text{ GHz}/f_B$. The diode itself typically has an area $A \approx 70 \mu\text{m}^2 \cdot 100 \text{ GHz}/f_B$. Ignoring parasitics, a 1 THz Bragg cell is $24 \mu\text{m}$ long and the diode area is $7 \mu\text{m}^2$. This presents some problems with the layout. A 4 THz diode requires $\leq 1 \mu\text{m}$ design rules hence approaches the size of the cell itself. Ohmic contacts and ion implantation require some overlap and increase the physical size of the diode further. For such a cell, the layout parasitics alone will greatly influence the cell's dispersion and limit waveform response.

As the NLTL cell size becomes smaller, so must the dimensions of the CPW in order to minimize the layout parasitics. This increases the CPW loss which decreases the waveform amplitude and reduces the compression along the length of the NLTL. As frequencies increase, the NLTL losses increase greatly (figure 3.14). This effect is difficult to characterize, but can be simulated given software capable of modeling all the properties of the NLTL. At this time, there is no such simulator available and one must try to compensate for these effects in the cell design.

There is a possible solution to both the diode to transmission line length ratio and layout parasitics problems. If one could use an air bridge as a CPW center conductor, the velocity would approach that of free space and line lengths could be increased by a factor of three for the same f_B . This possible solution also has the advantage of wider center conductors for similar CPW impedances. Of course, this novel CPW geometry would require extensive electromagnetic modeling to get adequate design parameters. Extensive process development would also be required to minimize the air bridge post size and a multiple air

bridge process may be required to suppress parasitic modes.

This leaves the limitations of the material itself. ω_d can be increased by increasing the doping (σ), but ω_s is fixed by the effective mass and mobility which decreases slowly with increasing doping. An alternative material system would be required to exceed these limits since the plasma resonance depends on the geometric mean of the dielectric relaxation and scattering frequencies. What one would desire is a small effective mass (larger ω_p) with a wide bandgap (low loss lines, good Schottky contacts). Unfortunately, the bandgap generally decreases along with the effective mass. At this point, the material limits have not been reached; layout issues have been dominant. Although the plasma resonance occurs below the resistive cutoff for the uniform diodes, loss on the NLTL is very large well below this frequency. As work on these devices progresses, the material itself will be the ultimate limitation.

Chapter 4

Simulation and Fabrication

A sufficient set of models has been established for the NLTL components and overall device operation has been described. All one need do is specify the desired output vs. input characteristics and the NLTL's parameters are essentially specified. One should use a simulation tool to verify the circuit's operation. Unfortunately, approximations and assumptions that facilitate theoretical understanding tend to diverge from simulated results due to inadequate models; and simulations tend to diverge from measurements due to inadequate modeling. Results from the simulator should be closer to measurements so long as the models used are a more accurate representation of the device than the approximations used in calculations.

4.1 Design by Simulation

The shock NLTL is both the easiest to understand and the most reliable to build. Since the waveform harmonics are well below the Bragg edge, the LC model is sufficient. It is also very convenient to express the general NLTL (shock, DHG, or impulse) in terms of its shock line parameters, T_{comp} , Z_0 , and Z_{LS} . If one assumes the geometric tapering rule ($f_{B,n} = f_{B,in}/k^n$) and provides the input ($f_{B,in}$) and output ($f_{B,out}$) Bragg frequencies, the line is completely specified: the tapering rule

$$k = \frac{f_{B,out}}{f_{B,in}} \left(\frac{\pi Z_0 T_{comp} f_{B,in} - \kappa Z_{LS}}{\pi Z_0 T_{comp} f_{B,out} - \kappa Z_{LS}} \right) \quad (4.1)$$

and

$$N = \frac{\ln(f_{B,in}/f_{B,out})}{\ln k} \quad (4.2)$$

is the number of sections. So, for a given diode (which provides κ), a mathematically concise way of generating tapered lines is given.

Assuming one can design the diode to have a very high cutoff frequency (> 10 times f_B) and an NLTL cell with low skin loss, the output Bragg frequency will set either the pulse transition time, peak conversion frequency, or impulse width. As will be seen later, loss plays a significant role in NLTL design. The input f_B depends on the type of NLTL and the desired sinusoidal drive frequency (f_{drive}). $f_{B,in}/f_{drive}$ is either > 10 for a shock, 2 to 4 for a DHG, or 1 to 2 for an impulse line. This narrows the parameter search space for the “ideal” line, but leaves the compression time uncertain except for a shock where $T_{comp} > 0.295/f_{drive}$, the 10%–90% rise/fall time of a sine wave. Since both DHG and impulse devices rely on the interaction between two or more solitons, even the minimum compression time for the desired result is uncertain. Design by simulation is required.

The intent of this section is to provide a complete set of simulation results that cover the evolution of the NLTLs. The first generation of devices used $90\ \Omega$ interconnects and 1.7 THz hyperabrupt diodes and suffered from a large amount of skin loss. The second generation of devices used $75\ \Omega$ interconnects with the same diodes as the first generation, greatly reducing skin loss. The third generation of NLTLs used $75\ \Omega$ interconnects and both hyperabrupt and uniform series diodes to achieve 1.5 and 2.8 THz cutoff respectively. Tradeoffs in device performance are not obvious in simulations, but offer a good starting point; device measurements demonstrate inadequacies in simulation.

4.1.1 Shock Lines

Shock lines are tapered to reduce skin loss and ringing. Lower Bragg frequencies allow wider center conductors with relatively small parasitics. As the Bragg frequency increases, the CPW must become smaller to keep the parasitic effects small. Since the simulation tool (mwSPICE [40]) does not allow skin loss, the simulations shown demonstrate the effects of varying NLTL (T_{comp} and f_B), and diode ($f_{C,LS}$) parameters for a given input (0 to -6 V step with 20 ps fall time) on a homogeneous line. A step function is used for illustrative purposes; sinusoidal drive is more readily produced and generally a more stable source.

The response of a line where the diode cutoff frequency limits the shock speed ($f_{C,LS} = f_B$) is shown in figure 4.1. The waveform is very clean (no over/under shoot) and shows uniform shock formation over the pulse’s leading edge. The cutoff frequency is 500 GHz and by the 148th diode ($T_{comp} = 41$ ps), the shock is fully formed and has reached its asymptotic limit of 2.9 ps ($\approx 1.5/f_{C,LS}$).

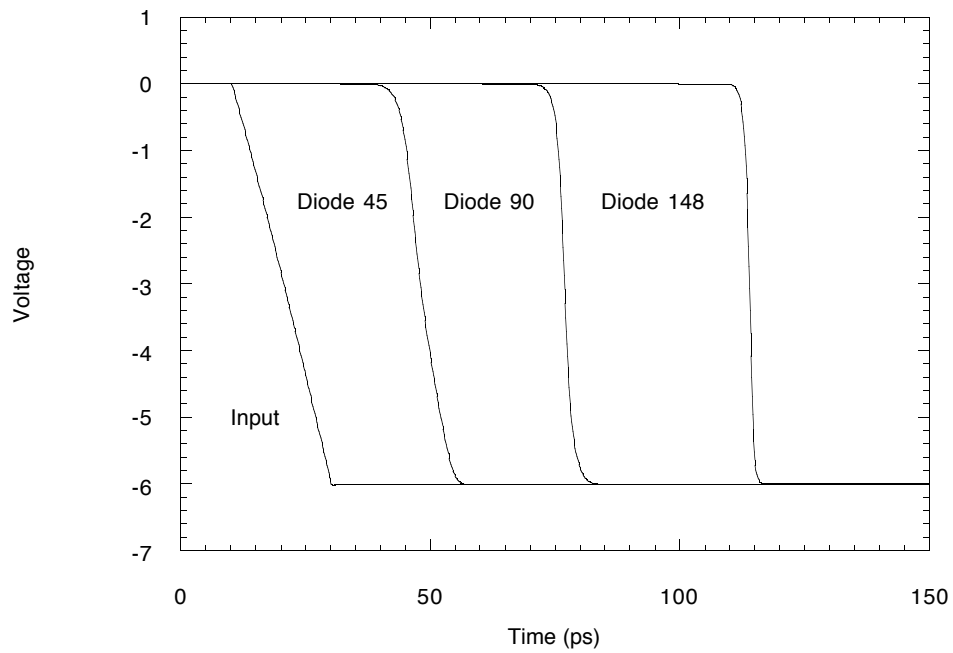


Figure 4.1: Simulation of a shock NLTL with $f_{C,LS} = f_B = 500$ GHz. Asymptotic shock formation is achieved by the 148th diode ($T_{comp} = 41$ ps) giving a 2.9 ps edge. Note the complete absence of ringing in the waveform.

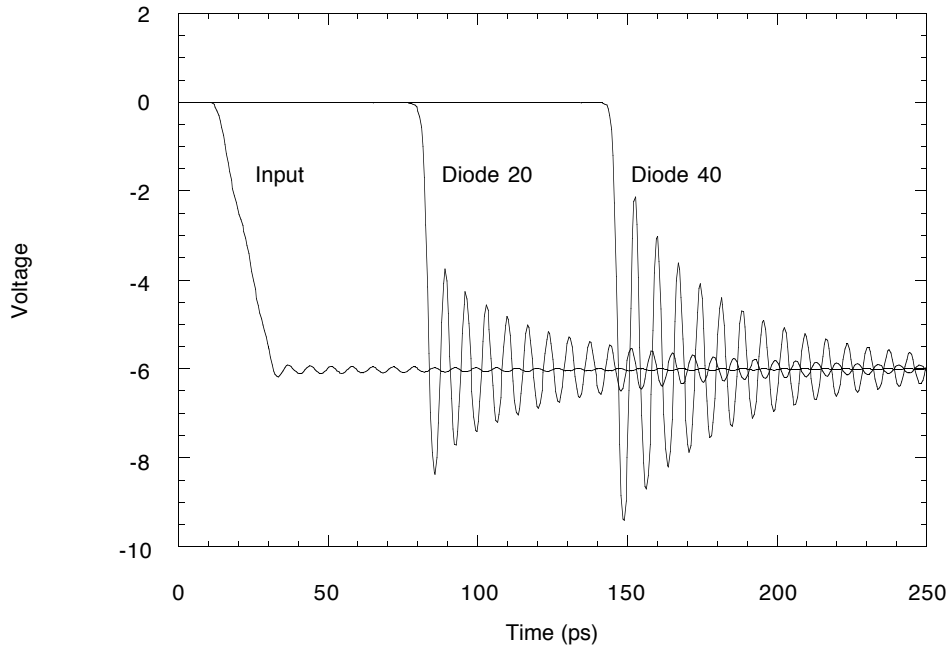


Figure 4.2: Simulation of a shock NLTL with $f_{C,LS} = 2$ THz and $f_B = 100$ GHz. Asymptotic shock formation is achieved by the 20th diode ($T_{comp} = 23$ ps) giving a 2.4 ps edge. Note the large amount of ringing in the waveform.

Figure 4.2 shows the response of a line where the diode has a very high cutoff frequency ($f_{C,LS} = 20f_B$). Here, there is a great deal of ringing causing overshoot, and shock formation is uniform over the leading edge. The ringing is nearly the same frequency as f_B , 100 GHz, and the diode has a 2 THz cutoff. The asymptotic shock speed is 2.4 ps ($\approx 1/4f_B$) by the 20th diode ($T_{comp} = 23$ ps), and by the 40th diode, ringing is nearly the same amplitude as the shock front. For the Bragg limited line, sinusoidal drive can be a problem since the ringing extends over a very long duration, interfering with subsequent cycles.

Figure 4.3 shows the response of a line where the effects of diode and Bragg frequency are nearly the same. Here, $f_{C,LS} = 2$ THz and $f_B = 500$ GHz ($f_{C,LS} = 4f_B$). The asymptotic shock speed is 0.9 ps ($\approx 1/2f_B$) by the 120th diode ($T_{comp} = 32$ ps). Ringing is not pronounced on this NLTL but shock formation

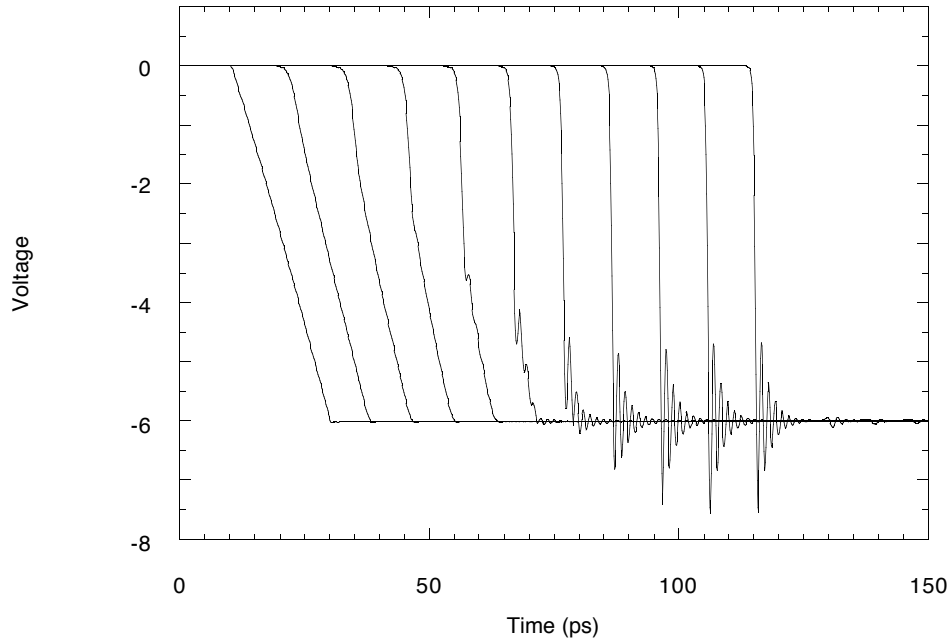


Figure 4.3: Simulation of a shock NLTL with $f_{C,LS} = 4f_B = 2$ THz. Waveforms are shown every 15^{th} diode. Asymptotic shock formation is achieved by the 120^{th} diode ($T_{comp} = 32$ ps) giving a 0.9 ps edge. There is some ringing in the waveform, but much less than the Bragg limited line.

is not uniform. The shock first appears by the 15^{th} diode and gradually grows over the entire leading edge. This partial shock formation occurs in all NLTLs where the propagation delay $T_D(V) = \sqrt{LC(V)}$ has a different time variation than the input pulse. In this case, $T_D(V)$ is not linear with voltage, but the input pulse varies linearly with time. It is not as obvious in the other simulations due to different dominant effects.

For shock NLTLs, a good balance between the limiting effects of the diode and Bragg frequencies is to keep $f_{C,LS}$ 4–6 times f_B . This provides a waveform with slightly underdamped shape but require less physical length to reach the asymptote than diode limited lines. If one increases f_B towards the end of the line to become diode limited, the waveform has less ringing at the output and

rapid compression near the input. This is done in the geometrically tapered lines and has the added benefit of reducing skin loss near the input by allowing wider center conductors. The simulated response of a geometrically tapered shock NLTL is shown in figure 4.4. By grading f_B from 125 to 900 GHz over the 51 ps of compression ($k = 0.977$, $N = 85$) and employing $f_{C,LS} = 1.7$ THz diodes and $90\ \Omega$ interconnects, ringing is greatly reduced by the 0.7 ps output edge. This line was fabricated and measured; see chapter five for details.

The effect of varying T_{comp} can be seen by examining the waveforms at different diodes. The shock builds up (edge becomes faster) until the minimum fall time is attained then maintains that edge speed. One would want to find the length required for this limit (typically $1.5 \times T_{fall,in}$) then truncate the NLTL to reduce the effects of skin (and diode) loss. These guidelines demonstrate the considerations in shock line design and provide a method for determining the line's parameters.

4.1.2 DHG Lines

Distributed harmonic generation relies on the propagation properties of solitons. An input waveform having width greater than given in equation 2.28 for its amplitude will separate into two or more solitons on propagation through the NLTL. Separation occurs because the input waveform corresponds to a superposition of solitons having different amplitudes which propagate at different rates. The DHG is driven by a sinusoidal source which can be viewed as an impulse train repeating at f_{drive} with $1/2f_{drive}$ FWHM duration. The number of solitons, hence the order of harmonic conversion is very roughly $N_h \approx f_B/f_{drive}$.

Efficient conversion requires low loss. This means that $f_{C,LS} \gg f_B$ and line length must be minimized. In the case of the DHG, a frequency-domain nonlinear simulator is the best choice since the number of harmonics and nonlinear elements is small and skin loss can be accounted for. LIBRA [40] was used for the simulations shown. It provides both time- and frequency-domain results. For the simulations shown, two different types of NLTL were used: those using $90\ \Omega$ interconnects and diodes with 1.7 THz cutoff and $\kappa = 0.973$ (first generation), and those with $75\ \Omega$ interconnects and standard (2.0 THz, $\kappa = 0.745$) diodes (second generation). $f_{B,in}/f_{drive}$ can be varied to achieve different orders of multiplication, but DHG length plays a critical role. If the line is too long, the second (or third) solitons will be overtaken by larger amplitude ones since the drive is repetitive. If the line is too short, solitons will not fully separate. This implies a ‘‘coherence length’’ for the DHG line, but design by simulation

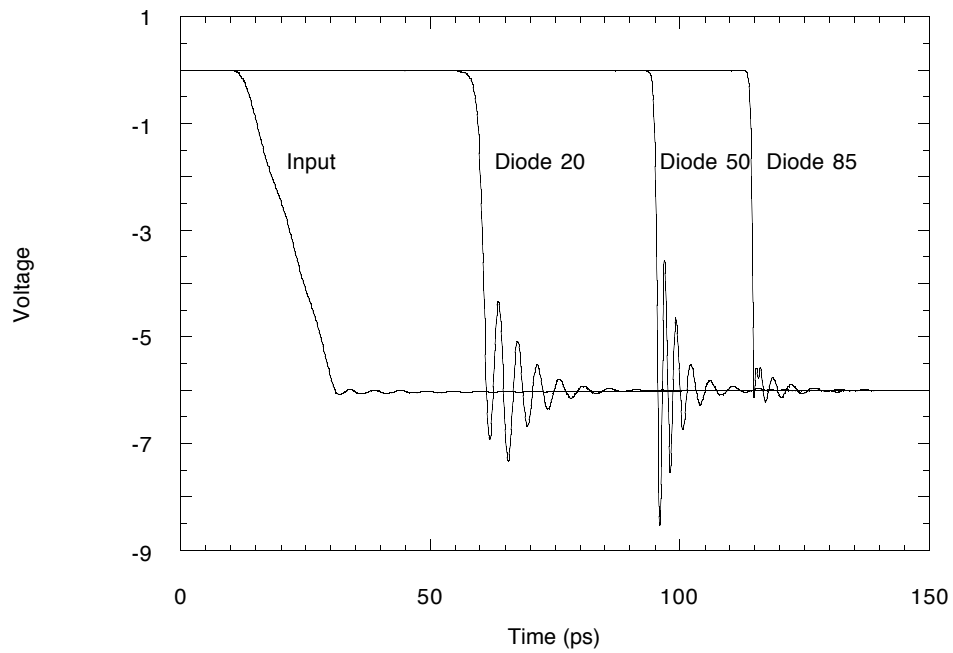


Figure 4.4: Simulation of a tapered shock NLTL with $f_{C,LS} = 1.7$ THz and Bragg frequency grading from 125–900 GHz. Asymptotic shock formation is achieved and ringing is early eliminated by the end of the line, the 85th diode ($T_{comp} = 51$ ps) giving a 0.7 ps edge.

is required due to nonlinear soliton interaction. If one simulates a long line, the optimum length for a given type of conversion can be determined, but resimulation with a termination is required since the large-signal impedance of the soliton line is not exactly the same as that of the shock (Z_{LS}) and reflections can occur. Generally, for higher orders of conversion, longer lines are required.

The first generation of DHGs consisted of two devices: 10 and 20 diode lines, both using 44 GHz Bragg frequency. The second generation of devices also consisted of two DHGs: a 15 diode, $f_B = 69$ GHz and a 20 diode, $f_B = 99$ GHz line. The Bragg frequencies were determined by the LC method (c.f. shock lines), so the actual Bragg cutoff is up to 20% higher in frequency (see equation 2.4). The lengths of the first generation of devices were determined to give peak conversion efficiencies for doubling over the Ka- band. Lengths for the second generation were determined for doubling over the V-band (69 GHz line) and tripling over the W-band (99 GHz line).

Figure 4.5 and 4.6 show the simulated harmonic output power of the first generation of devices. The shorter line has a peak conversion efficiency of -5.6 dB at 38 GHz and has a fairly narrow -3 dB bandwidth from 32–42 GHz. The longer line has a lower peak conversion efficiency of -6.4 dB at 34 GHz but a wider -3 dB bandwidth from 27–42 GHz, covering the entire Ka-band. Clearly, the line length plays an important role in device characteristics. Both lines used a 20 dBm sine wave with -2.5 V DC bias as a source.

Figure 4.7 shows the simulated harmonic output power of the V-band doubler and figure 4.8 shows the simulated harmonic output power of the W-band tripler. For both circuits, a 24 dBm sine wave with a -4.6 V DC bias was used. Line lengths were adjusted to get the best conversion efficiency in standard waveguide (V- and W-) bands assuming Ka-band drive.

Figure 4.7 shows the simulated harmonic output power of the V-band doubler which has a peak conversion efficiency of -5 dB at 70 GHz with a -3 dB bandwidth from 58–75 GHz. Figure 4.8 shows the simulated harmonic output power of the W- band tripler which has a peak conversion efficiency of -8.5 dB at 102 GHz with a -3 dB bandwidth from 90–175 GHz. Although the order of harmonic conversion is related to f_B/f_{drive} , the line length plays an important role in which order of harmonic is emphasized. The 69 GHz line can act as a doubler, tripler, quadrupler, etc., but the best efficiency is achieved for doubling, determined by the line length. Similarly, the 99 GHz line could be used as any order converter, but the third harmonic has the best conversion efficiency for the intended Ka-band drive.

Diode loss does not become a limiting issue until $f_{C,LS} \leq 20f_B$. Skin loss

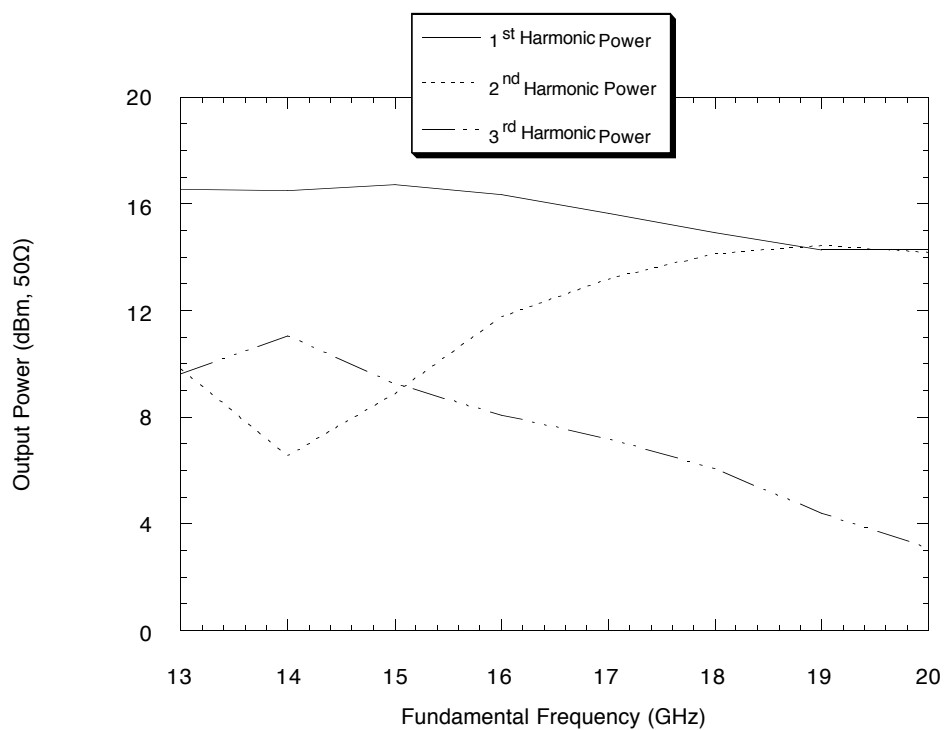


Figure 4.5: Simulated harmonic conversion using a 10 diode, $f_B = 44$ GHz NLTL. The input is a 20 dBm sine wave with a -2.5 V DC bias. The peak conversion efficiency of -5.6 dB occurs at 38 GHz and covers a small portion of the Ka-band: -3 dB bandwidth is between 32 and 42 GHz.

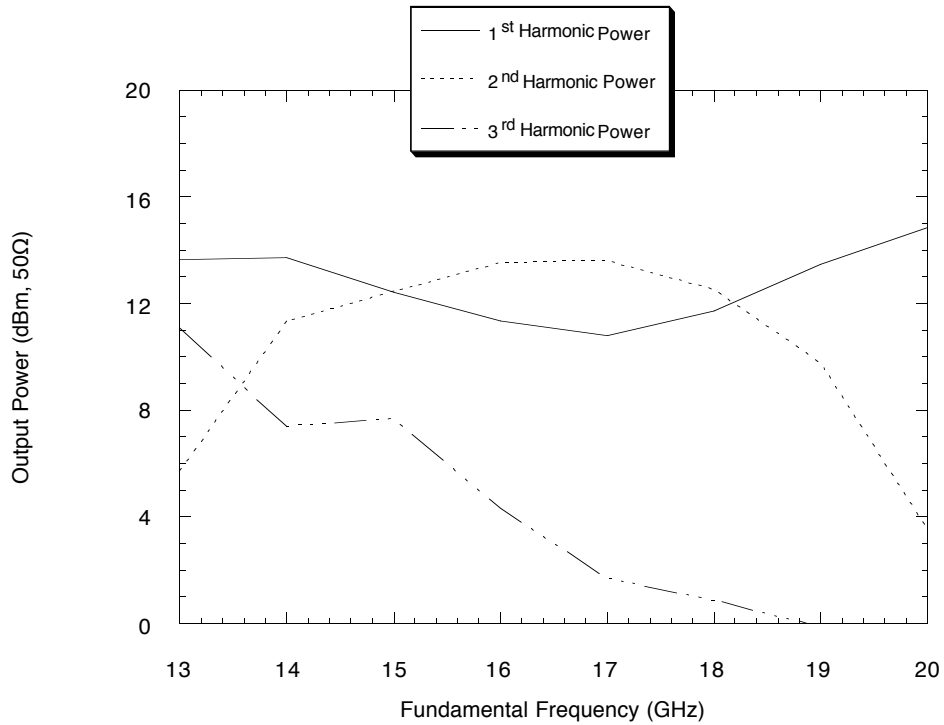


Figure 4.6: Simulated harmonic conversion using a 20 diode, $f_B = 44$ GHz NLTL. The input is a 20 dBm sine wave with a -2.5 V DC bias. The peak conversion efficiency of -6.4 dB occurs at 34 GHz and covers most of the Ka-band: -3 dB bandwidth is between 27 and 42 GHz.

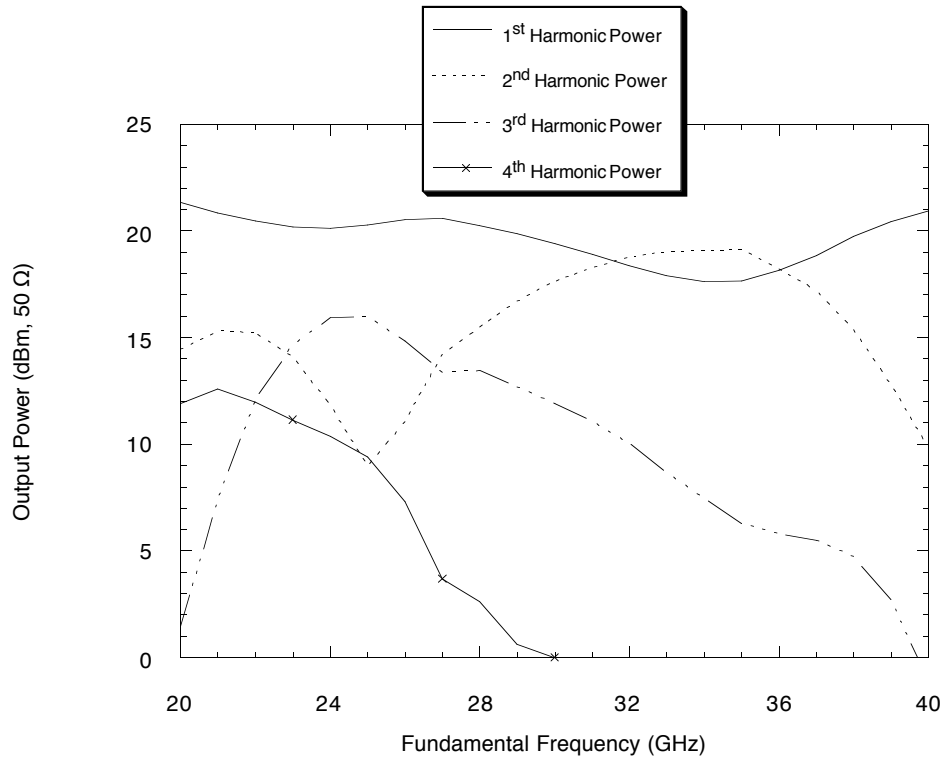


Figure 4.7: Simulated harmonic conversion using a 15 diode, $f_B = 69$ GHz NLTL. The input is a 24 dBm sine wave with a -4.6 V DC bias. The peak conversion efficiency of -5 dB occurs at 70 GHz and covers most of the V-band: -3 dB bandwidth is between 58 and 75 GHz.

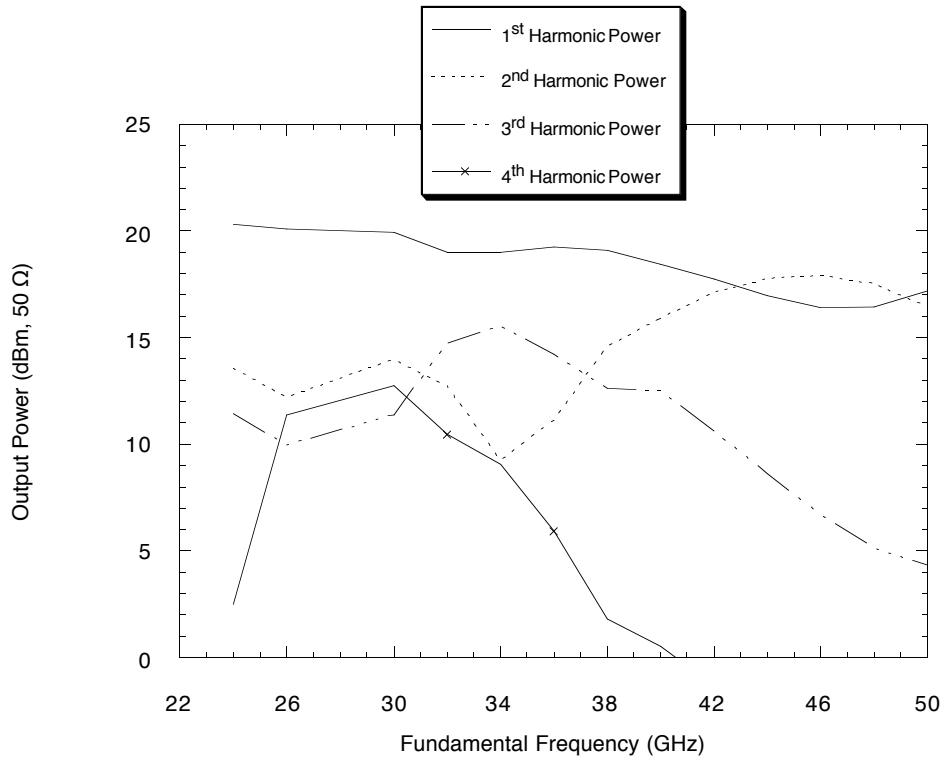


Figure 4.8: Simulated harmonic conversion using a 20 diode, $f_B = 99$ GHz NLTL. The input is a 24 dBm sine wave with a -4.6 V DC bias. The peak conversion efficiency of -8.5 dB occurs at 102 GHz and covers most of the W-band: -3 dB bandwidth is between 90 and 120 GHz.

dominates for lower Bragg frequencies. For the 99 GHz line, the diodes are just beginning to have a detrimental effect on conversion efficiency. Other issues affecting conversion efficiency are impedance matching and drive amplitude. Having a good impedance match at the NLTL input allows most of the drive power to enter the line. Impedance matching at the output prevents standing waves on the line and allows power to be transferred to the load. Using LIBRA [40] one can insert a directional coupler in the simulation to determine the time average incident and reflected powers, adjusting NLTL parameters to minimize reflections.

The NLTL is a nonlinear device, so the conversion efficiency will change (along with many other parameters) with changing drive amplitude. One could vary the drive power along with the frequency to find the truly optimal conditions, but this leads to much greater simulation time and convergence problems. A general trend is for the efficiency to start out very low then increase with added power. If one includes diode breakdown effects, there will be a maximum to this efficiency curve. Including a large number of variations in the simulation is superfluous since the fabricated device will undoubtedly have unmodeled effects and the drive frequency and power can easily be varied in testing where guaranteed convergence occurs in nanoseconds.

Higher orders of harmonic generation can be achieved, but efficiencies drop as harmonics increase. The reason for this is that each soliton separated from the input “impulse” (sine lobe) is progressively smaller. Slightly better efficiencies for higher orders of multiplication can be obtained by using cascaded as compared to uniform NLTLs. The first generation of devices suffered from additional skin loss due to $90\ \Omega$ interconnects. Impedance optimization occurred shortly after this wafer was measured. All of the DHGs discussed above were fabricated, and measurements are shown in chapter five.

4.1.3 Impulse Lines

Impulse compression lines are very much like tapered shock lines. The main differences are lower f_B/f_{drive} ratios and larger $T_{comp} \cdot f_{drive}$ products. Ikezi [18] describes impulse compression as “adiabatic” squeezing of the input waveform while Hirota [15] describes it as soliton decomposition. The latter description is more generalized (applicable to DHG, impulse, and even shock NLTLs) and will be adopted.

The output impulse width is roughly $T_{FWHM,out} \approx 1/2f_{B,out}$ for a fully compressed impulse (small tail) in the absence of loss. The input Bragg frequency

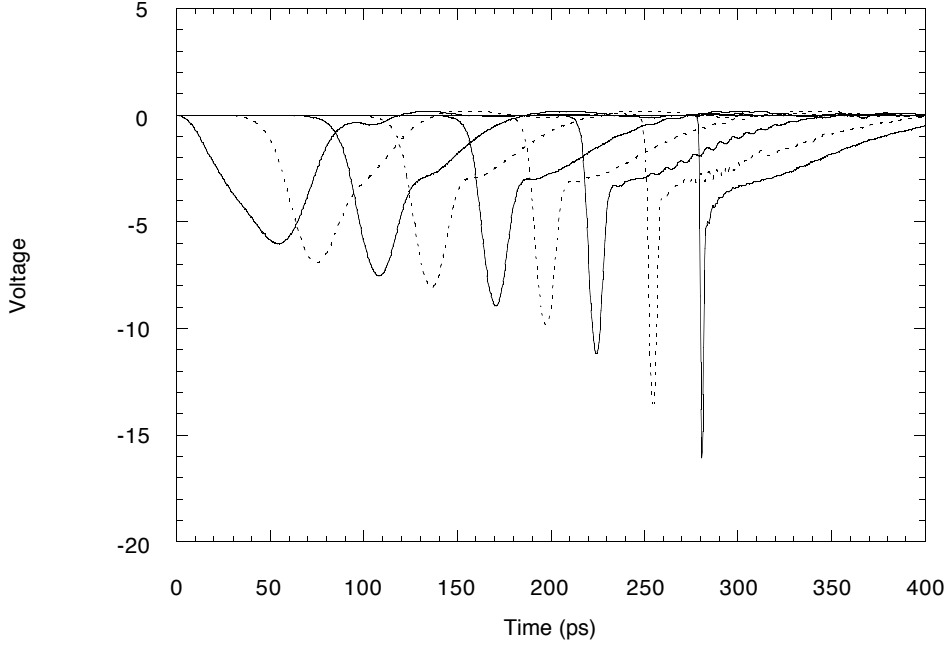


Figure 4.9: Simulation of an NLTL with $f_{B,in} = 16$ GHz, $T_{comp} = 120$ ps, and $f_{B,out} = 250$ GHz. Waveforms are shown at the input, output, and equal distances ($2360 \mu\text{m}$ spacings) along the length of the line (19 mm). The input is a 6 V amplitude raised cosine impulse.

$f_{B,in} = 1$ to $2 \times f_{drive}$. Larger input Bragg to drive ratios generate a large secondary soliton over the first sections of the NLTL and are usually undesirable. So, for a given input frequency (assuming sinusoidal drive) and desired output impulse width, one can vary $f_{B,in}$ and T_{comp} to explore the variety of possible outcomes in simulation. LIBRA would be very desirable for this, but the number of harmonics required ($N_h > 2f_{B,out}/f_{input}$) and the number of nonlinear elements prohibits its use. SPICE is the only practical program available to simulate the structure.

Five simulations are used to illustrate the effects of varying line length and input Bragg frequency. They all use $Z_0 = 75 \Omega$ and $f_{B,out} = 250$ GHz. Figure 4.9 shows the evolution of a single impulse on propagation through an NLTL

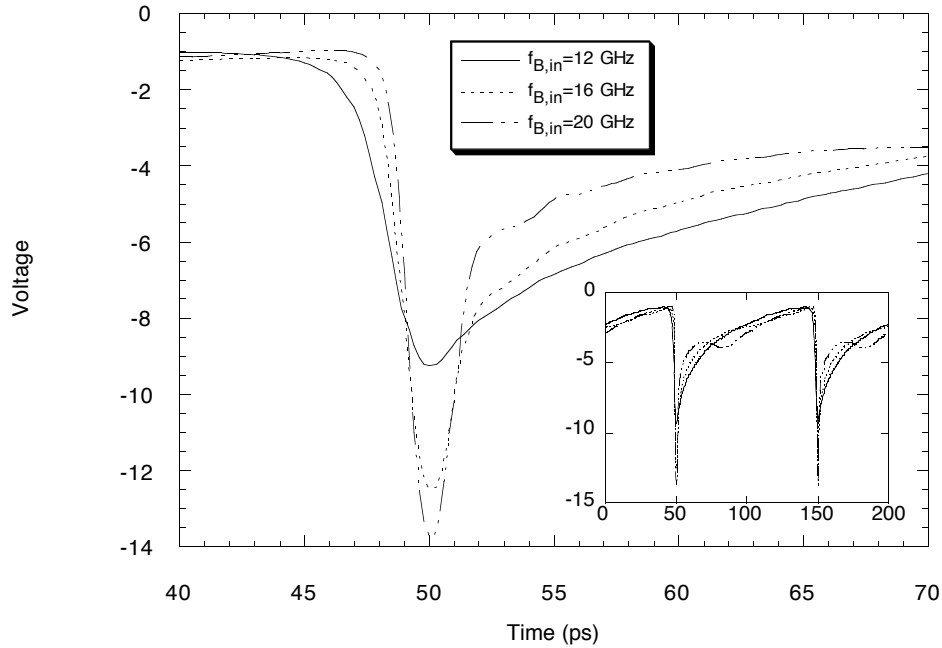


Figure 4.10: Simulation of three impulse NLTLs having $T_{comp} = 120$ ps and $f_{B,in} = 12, 16,$ and 20 GHz. A low $f_{B,in}$ prevents much of the signal from entering the line while a high one creates a noticeable secondary impulse.

with 16 GHz input Bragg frequency and 120 ps compression. Figure 4.10 shows simulated output waveforms for three different $f_{B,in}$ values on a $T_{comp} = 120$ ps line. Figure 4.11 shows simulated output waveforms for three different T_{comp} values on an $f_{B,in} = 16$ GHz line. A higher input Bragg frequency improves impulse shape, but generates an undesired secondary impulse. This may or may not be acceptable. Increasing NLTL length improves impulse shape, but there is a point of “diminishing returns” where there is no marked improvement in impulse shape. Also, larger values for T_{comp} and $f_{B,in}$ will increase the loss on the line. The tail extending from the impulse on each waveform has not dissipated to zero volts by the time the next cycle of drive arrives. This causes the baseline to drop from zero (as at the input) to about -1 volt in the large-signal steady state, reducing effective nonlinearity.

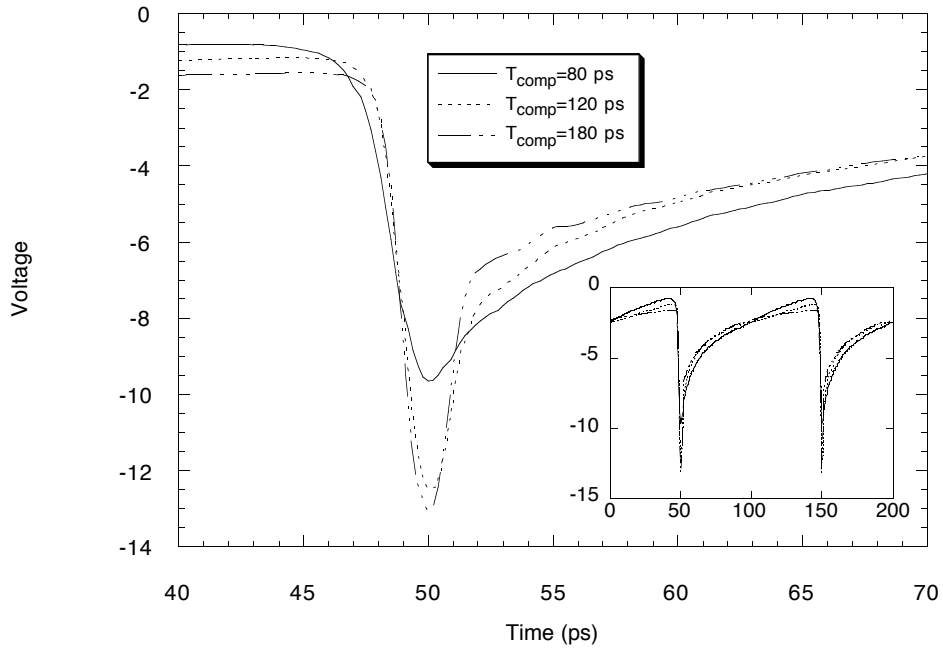


Figure 4.11: Simulation of three impulse NLTLs having $f_{B,in} = 16$ GHz and $T_{comp} = 80, 120,$ and 180 ps. A short line prevents impulse formation (solitons cannot separate) while a long line does not greatly improve impulse shape. If loss were included, the longest line would have a much smaller amplitude.

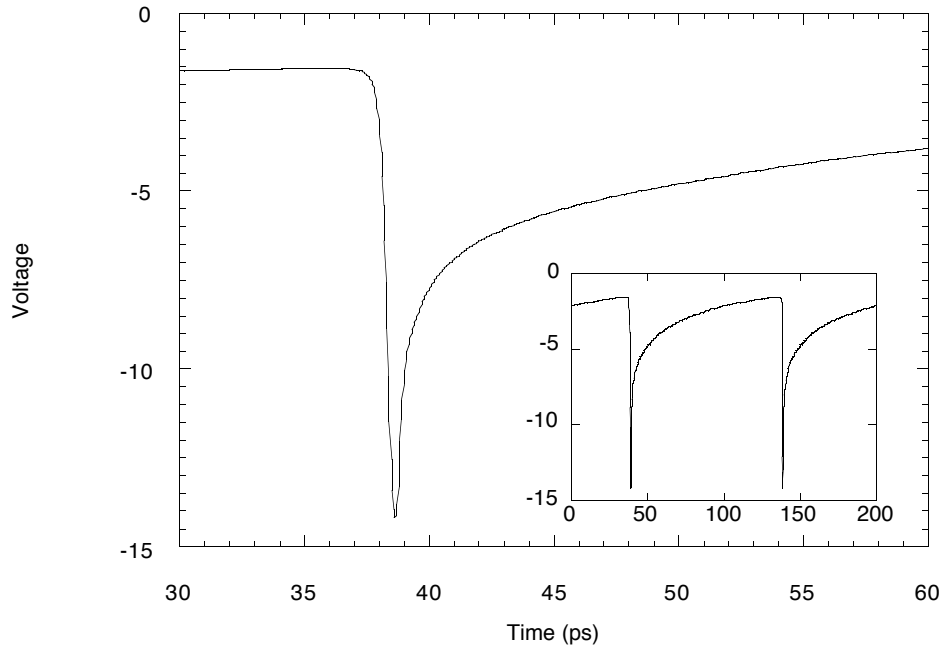


Figure 4.12: Simulation of the first generation impulse NLTL. It has $f_{B,in} = 16$ GHz, $f_{B,out} = 890$ GHz, and $T_{comp} = 188$ ps. Measurements on these devices demonstrated the need for impedance optimization since skin loss dominated all parasitic effects.

As with the DHGs, the first generation of impulse compression lines shown were designed using 1.7 THz, $\kappa = 0.973$ diodes and $90\ \Omega$ interconnects. The first impulse compression line was designed assuming a 10 GHz, 6 V_{p-p}, -3 V DC bias drive. The line had a 16 GHz input and 890 GHz output Bragg frequency with 188 ps of compression. A simulation of this line is shown in figure 4.12 and predicts subpicosecond impulse width. Since impedance optimization occurred after this design (indeed due to this design), the large number of squares of metal in the center conductor (2251) greatly attenuated the impulse and dominated other parasitic effects. Measurements on this device are shown in chapter five.

The second generation of devices used “standard” diodes (2.0 THz, $\kappa = 0.745$) and $75\ \Omega$ interconnects and were designed for $T_{FWHM,out} \approx 2$ ps ($f_{B,out} =$

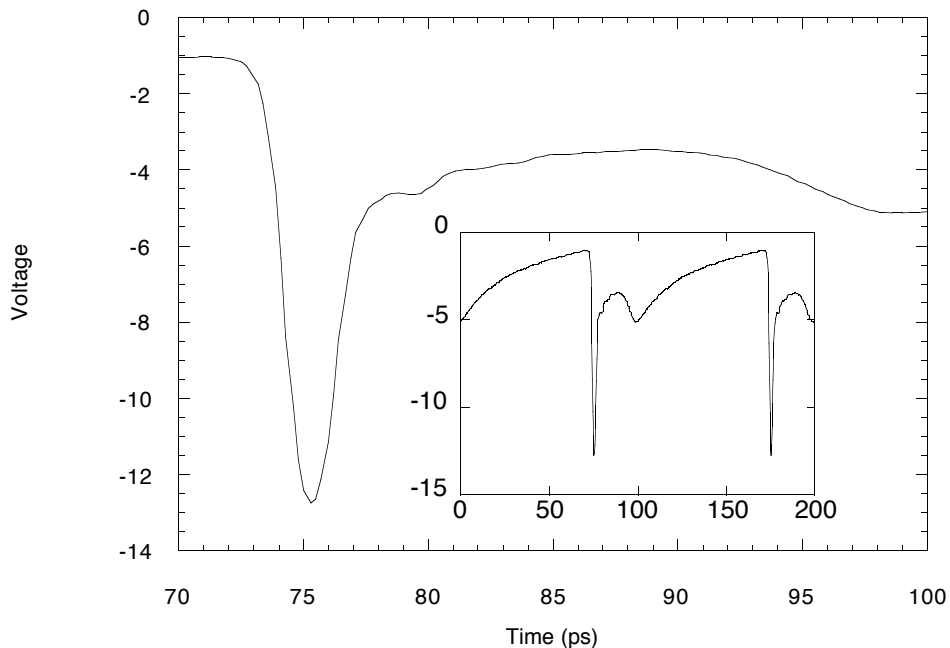


Figure 4.13: Simulation of the second generation impulse NLTL. It has $f_{B,in} = 24$ GHz, $f_{B,out} = 225$ GHz, and $T_{comp} = 120$ ps. This line was designed to operate at 15 GHz, but the best impulses were measured at 9 GHz drive.

225 GHz) using a 6 V_{p-p}, -3 V DC bias drive, either at 10 or 15 GHz. Interestingly, the lines designed to be driven at 15 GHz produced the best impulses when driven at 9 GHz, better than those designed for 10 GHz drive. Since they were designed for 120 ps compression (as opposed to the 180 ps for the 10 GHz drive circuits), the shorter length reduced overall loss. A simulation of this line having $f_{B,in} = 24$ GHz ($15/10 \times 16$ GHz), $T_{comp} = 120$ ps, and $f_{B,out} = 225$ GHz is shown in figure 4.13. As expected, a secondary impulse appears since $f_{B,in}/f_{drive} \geq 2$. These lines were fabricated and measurements shown in chapter five, but the indicated secondary impulse is not present. This may be due to layout parasitics reducing the Bragg frequency.

By using series diodes, both κ and C_{LS} are reduced by a factor of ≈ 1.5 while $\partial V/\partial t|_{\max}$ and V_{BR} are doubled. The penalty here is increased line length

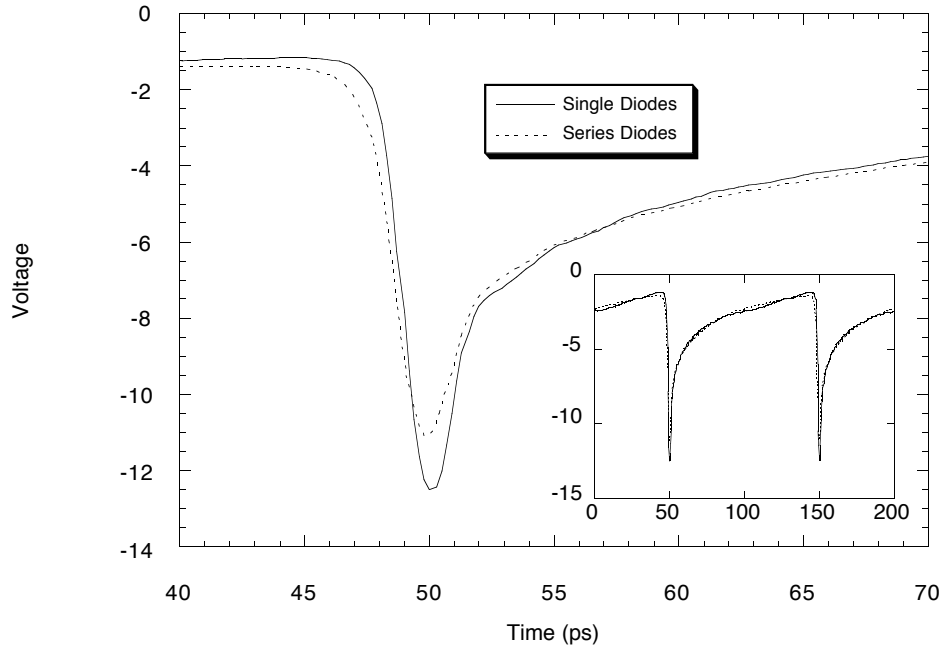


Figure 4.14: Simulated comparison between two NLTLs having $T_{comp} = 120$ ps, $f_{B,in} = 16$ GHz, and $F_{B,out} = 250$ GHz; one using single diodes, the other using series diodes. Since the series diodes reduce compression, the line is $\approx 1.5\times$ longer, and more loss (both diode and skin) is experienced, hence the peak amplitude is smaller using series diodes.

hence increased loss. Figure 4.14 shows the difference between single and series diodes for the same impulse line design parameters. The increased length causes increased loss and decreased peak amplitudes even without including skin loss. Although the series diode waveform has a poorer impulse shape (large tail), one can drive it with much more power than the single diode line.

Since series diodes increase the line length to T_{comp} ratio, the relative loss is greater (figure 4.14). If one were to use a shorter duration input impulse (higher f_{drive}), the overall line length is reduced and the breakdown and slew rate limits are increased. Both $f_{B,in}$ and T_{comp} should scale linearly by the same ratio as the increased drive frequency. For example, going from 9 to 30 GHz drive, the

line should be about 1/3 as long and the input Bragg roughly 3 times as large.

Series standard diodes have $\kappa = 0.479$, $f_{C,LS} = 1.47$ THz, and 28 V breakdown while uniformly doped ($N = 10^{17}\text{cm}^{-3}$) series diodes have $\kappa = 0.379$, $f_{C,LS} = 2.80$ THz, and 22 V breakdown. Uniform diodes look promising since the cutoff frequency is nearly twice that of the standard diode, but length increases by 26%.

Scaling the $T_{comp} = 120$ ps, $f_{B,in} = 24$ GHz line from 9 to 30 GHz drive suggests the new line will require only 36 ps of compression and have a 80 GHz input Bragg frequency. In order to cover a wide base of possible modeling insufficiencies, several variations of this device were simulated: $T_{comp} = 35$ and 25 ps, and $f_{B,in} = 67, 80, \text{ and } 93$ GHz, (six NLTLs). $f_{B,out} = 450$ GHz was used, taking advantage of the higher diode cutoff frequency to achieve shorter impulses. These simulations are shown using a 30 GHz, 27 dBm -3 V DC input in figure 4.15 and 4.16 showing the 25 and 35 ps compression lines respectively. Output impulses with ≈ 1.2 ps duration and 8–16 V_{p-p} amplitude are predicted. Larger input amplitudes resulting in large output amplitudes are possible with series diodes. A longer compression time results in more total loss, but better impulse shape (smaller tail). Although secondary impulse formation is evident, measurements on the second generation device suggests this secondary impulse will be less noticeable in testing. A photomicrograph of the series diodes cell layout is shown in figure 4.17. All six of these lines were fabricated and measured in this third generation of devices; see chapter five.

4.2 Device Fabrication

Nonlinear transmission lines can be fabricated using relatively coarse design rules and as few as three masks [37]. Finer design rules allow higher cutoff frequency diodes and adding two mask levels provides parasitic mode suppression through air bridges. The NLTLs are fabricated on semi-insulating GaAs epitaxial wafers. The crystal orientation is not critical since isotropic etches are used, but [100] cut crystals allow electrooptic sampling [36], if such a measurement technique is desired. Each processing step will be discussed in turn. A detailed process flow sheet (used in the clean room) is included in appendix two.

Our GaAs wafers are purchased through a vendor [44]. Specifications for the epitaxial structure are based on the diode design, trading off nonlinearity, breakdown, and cutoff frequency (chapter three). The material must be very uniform in its characteristics over the wafer surface since devices can be very large, and must follow the designed doping profile closely. Since this vendor

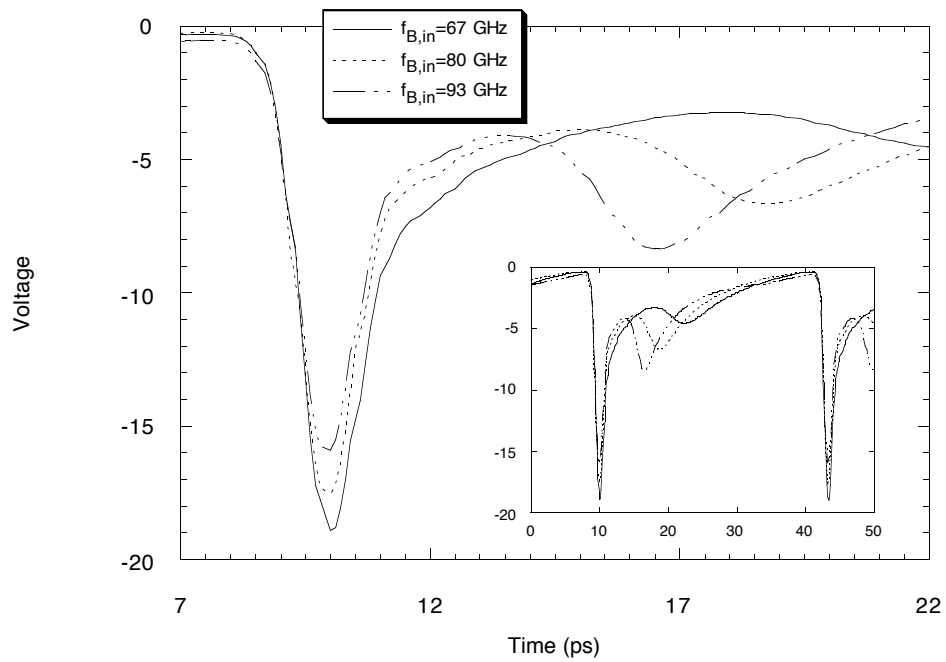


Figure 4.15: Impulse NLTLs with 25 ps compression and three different input Bragg frequencies. A lower $f_{B,in}/f_{drive}$ ratio provides a larger primary and smaller secondary impulse, but a poorer impulse shape.

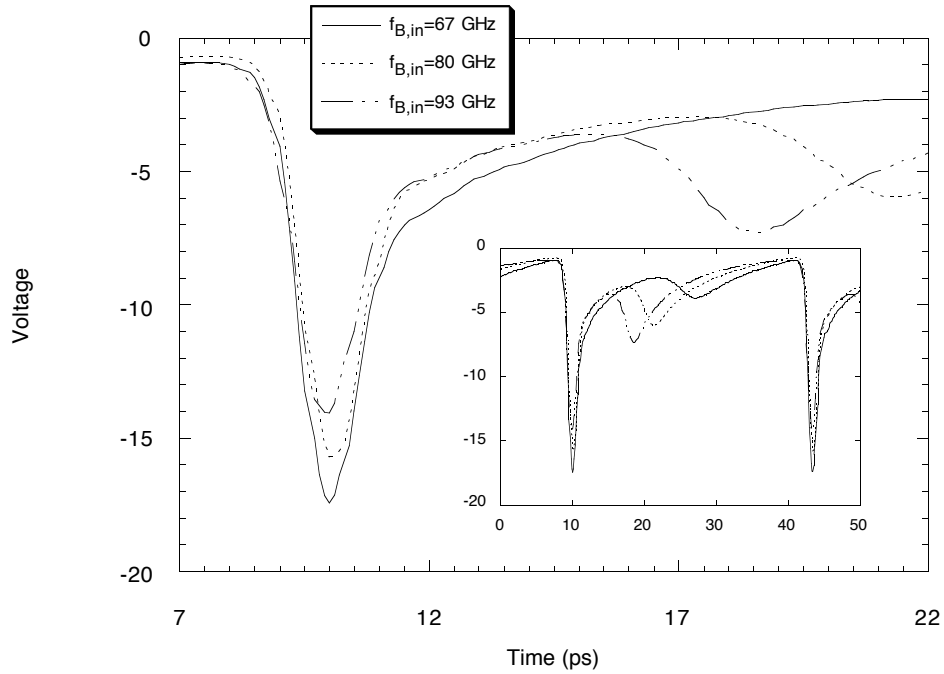


Figure 4.16: Impulse NLTLs with 35 ps compression and three different input Bragg frequencies. A lower $f_{B,in}/f_{drive}$ ratio provides a larger primary and smaller secondary impulse, but a poorer impulse shape.

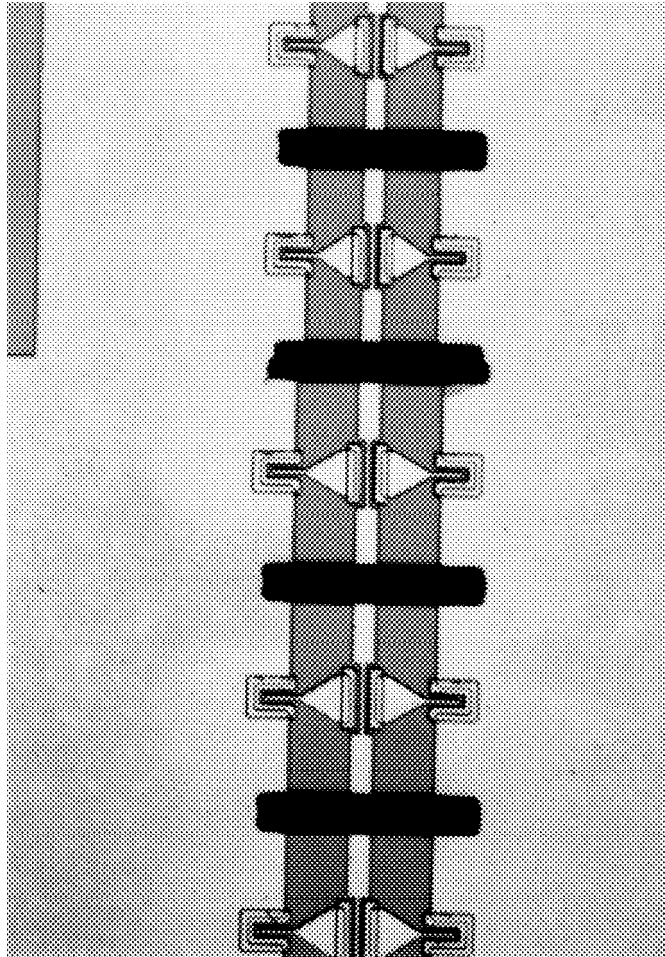


Figure 4.17: Photomicrograph of a series diode NLTL. It is a combination of the signal diode and ground diode cells discussed in chapter three.

provides polaron (doping concentration vs. depth) and sheet resistivity data for each wafer, the material can be relied upon. A specification of a $\pm 10\%$ tolerance on the doping parameters is given, which results in $< 10\%$ accurate values of capacitance and resistance.

4.2.1 Ohmic Contacts

By making ohmic contacts the first step, one can use standard Schottky contact metalization. Refractory metals are required for the Schottky if ohmics are done after the Schottky. Ohmics require high temperature annealing and under these conditions, nonrefractory Schottky metal can diffuse into the surface of the GaAs, introducing undesired doping. Figure 4.18 shows a cross section of a wafer undergoing the ohmic process. The contacts are patterned with photoresist treated with toluene to form a “liftoff” profile. This profile prevents metal from contacting coated areas and causes a physical separation in the metal layer. By rinsing the wafer in acetone, the photoresist is stripped along with the undesired metal. The toluene treatment (liftoff profile) is used in all but the air bridge step

In order to contact the highly doped N+ collector layer, one must etch through the diode layer. A hydrogen peroxide and ammonia etch ($H_2O_2 : NH_4OH : H_2O :: 21 ml : 3.6 ml : 300 ml$) is used which usually etches at 7 nm/s and is very isotropic. This rate varies due to temperature fluctuations and evolution of O_2 from the H_2O_2 . A eutectic mixture of Au and Ge is then deposited by evaporation. Since Au and Ge have different vapor pressures, they evaporate at different rates. If one uses a crucible containing the eutectic mixture, the Ge will evaporate more rapidly than the Au, and the mixture will no longer be eutectic after one or two evaporations. The method used is to evaporate pure Ge, then pure Au, then Ge and Au again in the eutectic proportion. This method results in *very* reproducible contact resistances. 100 Å of Ni is deposited on top of the AuGe eutectic and plays an important role in the contact metallurgy [7]. Finally, 3000 Å of pure Au is evaporated to insure good electrical contact.

Rapid thermal annealing (RTA) is the last part of the ohmic contact step. This procedure consists of rapidly raising the wafer temperature to 400°C, holding there for 60 seconds, then reducing it back to room temperature. The Ge and Au then combine to form the eutectic, and then diffuses into the upper part of the N+ layer, forming the ohmic contact. One should be careful, in this procedure, since very toxic As can be liberated from the wafer. The wafer and RTA

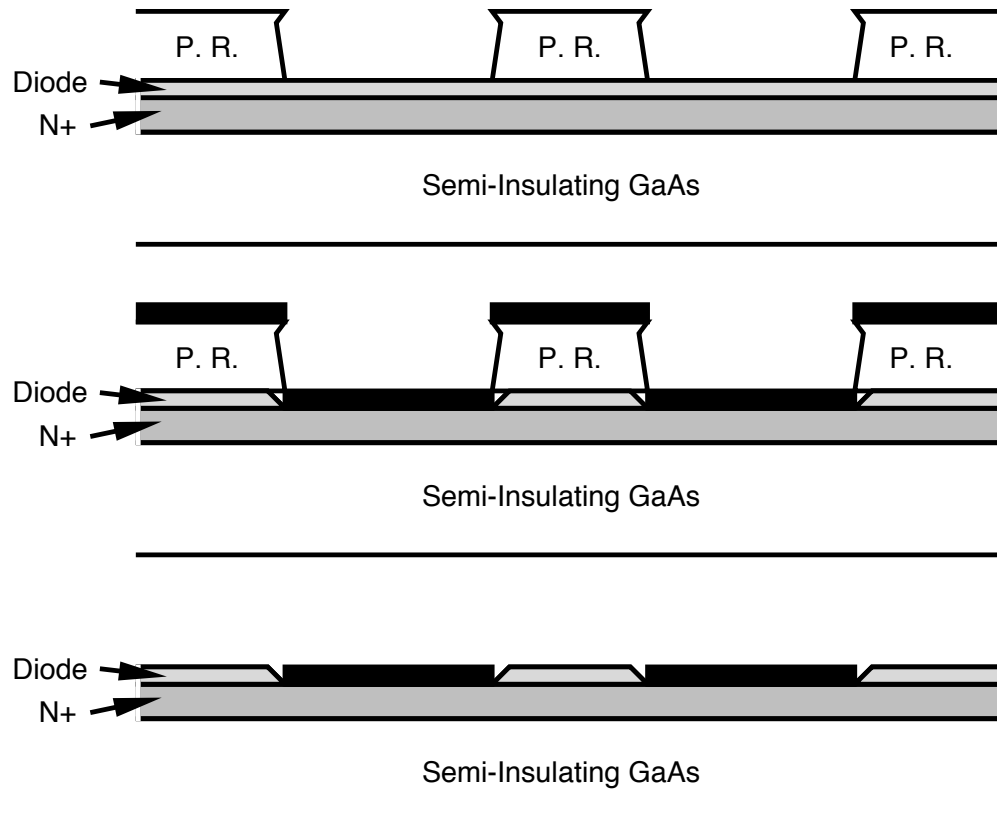


Figure 4.18: Cross sectional view of the ohmic process. Liftoff profile photoresist (P. R.) is used, and outlines the ohmic pads. After lithography, a wet etch exposes the N+ layer, and AuGe/Ni/Au can be evaporated and lifted off. After liftoff, rapid thermal annealing provides typically $20 \Omega \cdot \mu\text{m}$ contact resistance.

platen should be cleaned after this step. One should then measure the resistance of the ohmics to determine if sufficient annealing has occurred. If one does not measure typical values for contact and sheet resistance, realloying at a higher temperature is indicated.

4.2.2 Proton Implantation

In order to separate one diode from another and render most of the wafer semi-insulating, proton implantation (as opposed to a mesa process) is used. Hydrogen ions (protons) have the greatest penetration depth of any atomic species, and deep penetration allows thicker N+ layers, increasing diode cutoff frequencies. Isolation is due to the dislocation defects caused by collisions between energetic protons and the crystal lattice. The defects create energy states within the bandgap of the material, and if the defect density is large in comparison to the doping level, the Fermi level is pinned near mid band, causing the mobile electron density in the conduction band to be low.

In order to protect diode active areas (and resistors through the N+ collector) from implantation, a removable Au mask is used. A 1000 Å thick layer of SiO_2 is deposited on the wafer after cleaning. This prevents damage to the critical metal- semiconductor interface. Polyimide, which can be removed easily, is spun on top of the SiO_2 to a 1.2 μm thickness then thinned to 1.0 μm by oxygen plasma. A thick (1.6 μm) thick gold layer is patterned by liftoff to protect areas from the implant. Before sending the wafer to the ion implantation vendor [43], one must remove the exposed polyimide (using oxygen plasma etching). This prevents burning of the polyimide which would prevent its removal, the final step in this procedure. Figure 4.19 shows a cross section of a wafer undergoing the ion implant process.

In order to determine the energy and dose of protons for implantation, two sources of information were used: *Projected Range Statistics* [2] and “Proton Isolation for GaAs Integrated Circuits” [13]. Ion implantation is a statistical process, where the damage density increases with increasing depth to a peak (μ), then tapers off over some standard deviation of distance (σ). One can approximate the damage vs. depth characteristic as a triangle: no damage at $x = 0$ depth, linear increase to the peak damage at $x = \mu$, and no damage at $x = \mu + 2\sigma$. The peak damage depends on the dose: $Damage = 6Dose/(\mu + 2\sigma)$ and the projected range in GaAs depends on the energy: $\mu = 6.5 \text{ nm/keV}$ [13]. The deviation in the range was determined from Gibbons’ statistics on hydrogen in germanium, since there was no data on H^+ in GaAs.

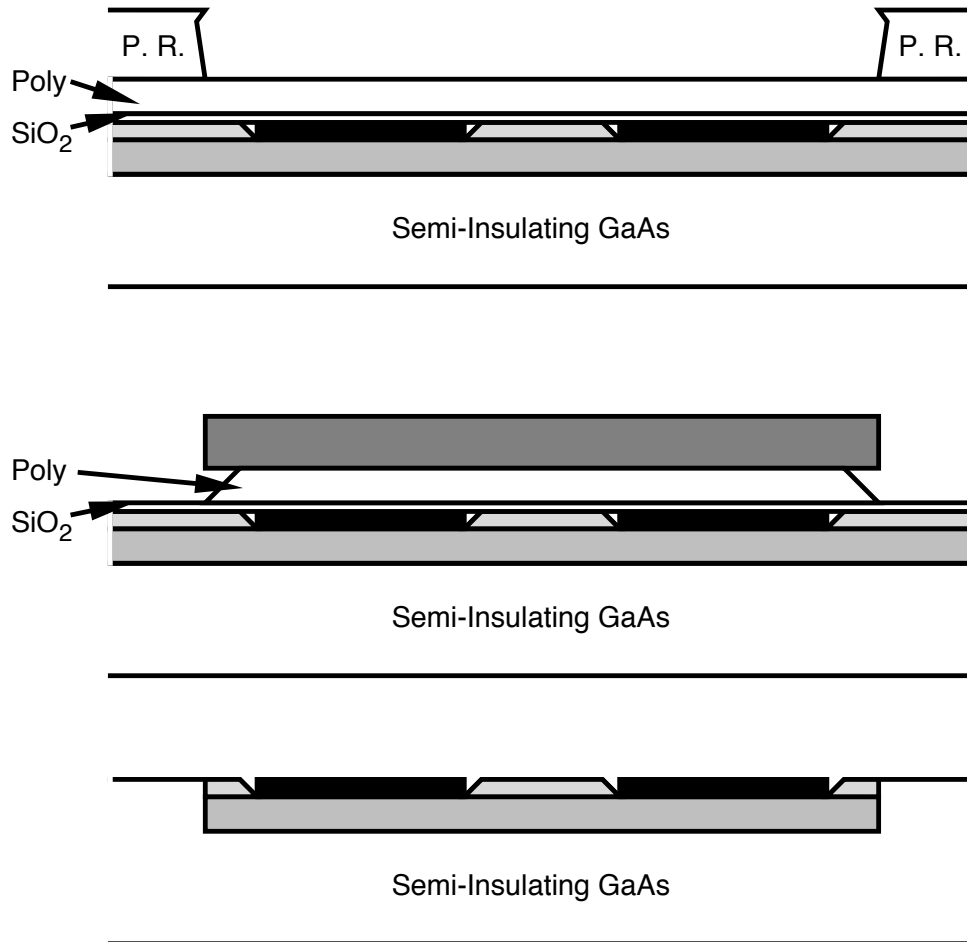


Figure 4.19: Cross sectional view of the ion implant process. The 1000\AA of SiO_2 acting as a surface protection layer is deposited by plasma enhanced chemical vapor deposition. $1.2\ \mu\text{m}$ of polyimide is then spun on and etched back to $1.0\ \mu\text{m}$, preparing the surface for liftoff lithography. $1.6\ \mu\text{m}$ of Au is then lifted off to protect the desired areas from the implant. Before implantation, the exposed areas of polyimide are removed with oxygen plasma to prevent burning. The wafer is then stripped of this mask.

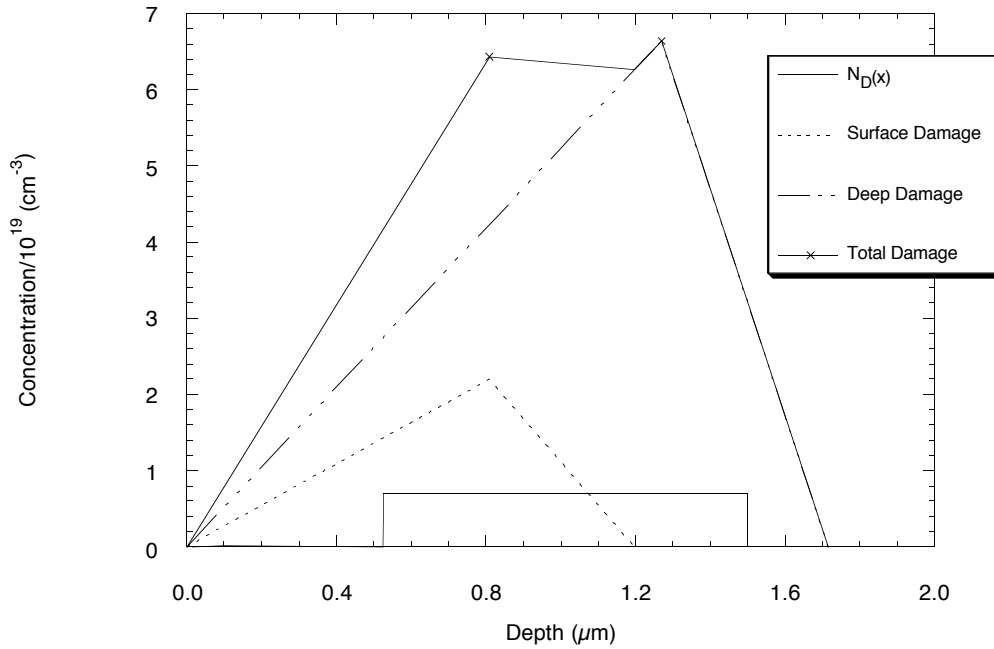


Figure 4.20: Proton implant damage and doping profile vs. depth in the hyperabrupt wafer. A surface implant at 125 keV with a $4.4 \cdot 10^{14} \text{ cm}^{-2}$ dose and a deep implant at 195 keV with a $1.9 \cdot 10^{15} \text{ cm}^{-2}$ dose were used. This causes crystal damage in excess of $3\times$ the doping concentration, insuring good isolation.

In order to insure good isolation, the crystal damage is maintained $\geq 3\times$ the doping density. Since the doping is fairly constant over the epi and the damage is triangular, two implants are used: a low energy, surface damage implant, and a high energy, deep implant. The resulting curve is shown in figure 4.20. This curve is for the hyperabrupt wafer and uses a 125 keV, $4.4 \cdot 10^{14} \text{ cm}^{-2}$ surface implant and a 195 keV, $1.9 \cdot 10^{15} \text{ cm}^{-2}$ deep implant. In order for the implant mask to function, the projected range must be at least $\mu + 4\sigma$. Assuming that the range statistics of polyimide are like photoresist, an effective loss of about 40 keV can be expected, requiring the Au to be $\geq 1.5 \mu\text{m}$ thick. $1.6 \mu\text{m}$ of gold is used, so protection of the diodes is insured. The 10^{17} cm^{-3} doped uniform wafer uses the same deep level implant, but reduces the surface implant to 110 keV at a $4.0 \cdot 10^{14} \text{ cm}^{-2}$ dose.

4.2.3 Schottky and Interconnects

Schottky contacts and interconnections are made in a single step. Ti/Pt/Au metal is patterned by liftoff to make Schottky contacts, connections to ohmic metal, and other required connections. 200 \AA of titanium is used for good adhesion, 500 \AA of platinum is used as a diffusion barrier, preventing the $1 \mu\text{m}$ thick gold from penetrating the surface of the diode. The total metal thickness need be no thicker than the skin depth at the drive frequency, about $1 \mu\text{m}$ at 10 GHz in Au. Thicker metal will not reduce loss on the structure. Figure 4.21 shows a cross section of a wafer undergoing the schottky process.

After the Schottky contacts have been made, the diodes can be fully tested: sheet and contact resistivity along with $I(V)$ and $C(V)$ curves can be measured at a DC probe station. Microwave measurements are reserved for trouble shooting and gaining additional information if devices fail to operate. Functional testing may be possible at this stage, depending on NLTL cell design and measurement technique.

4.2.4 Air Bridges

Air bridges reduce parasitic mode propagation, and may be required for other circuits on the wafer (e.g. sampling circuit). Figures 4.22 and 4.23 show cross sections of a wafer undergoing the air bridge process. The first step is to pattern the posts which are the terminal points of the air bridge. $3 \mu\text{m}$ thick photoresist that has been post baked to smooth the edges is used for this mask. It is very important to have very clean Au in these post holes to insure good electrical

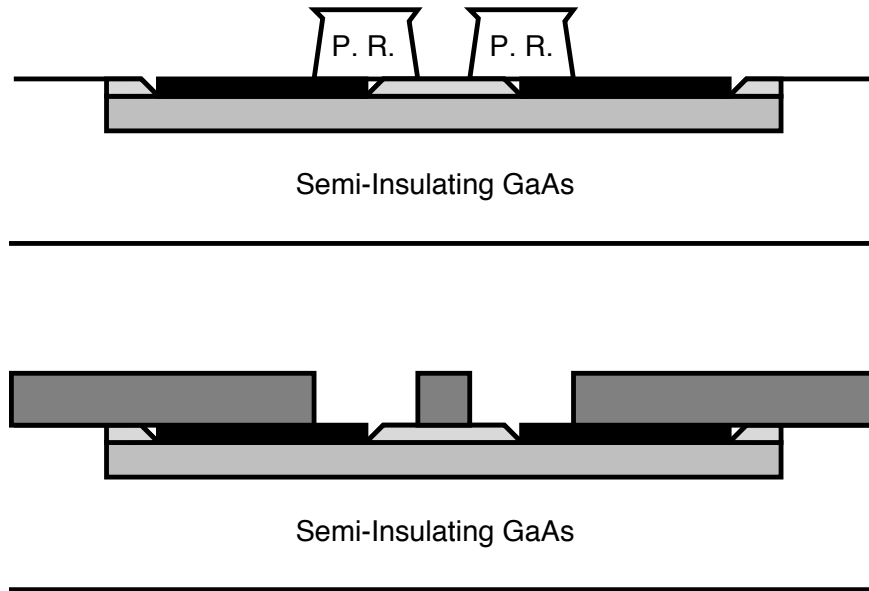


Figure 4.21: Cross sectional view of the schottky process. Liftoff profile photoresist (P. R.) is used, and outlines the areas to be metalized. After liftoff, diodes are completed and can be fully characterized.

continuity. After the post lithography, a very thin layer of Au (using Ti as sticking material on both sides of the Au) is sputtered to coat exposed surfaces at all angles. This is called the “flash” layer, and allows electrical contact to all areas of the wafer for electroplating.

A second coating of $3\ \mu\text{m}$ thick post baked photoresist is used to define the spans of the bridges. A small section of this top layer is then exposed to allow a clip lead to be attached for electroplating. Au is plated at a rate of $1\ \mu\text{m}/\text{hour}$ to a thickness of $3\ \mu\text{m}$. At this point, the air bridges are complete, and the photoresist and flash layer must be removed. The top photoresist layer is removed by flood exposure and development, preventing premature removal of the lower photoresist. A gold etchant removes the flash layer (HF is used to remove the Ti on both sides of the Au flash layer), slightly decreasing the thickness of the air bridge. Finally, acetone is used to remove the bottom photoresist, and the wafer is ready for functional testing. A view from the top of the wafer is shown in figure 4.24.

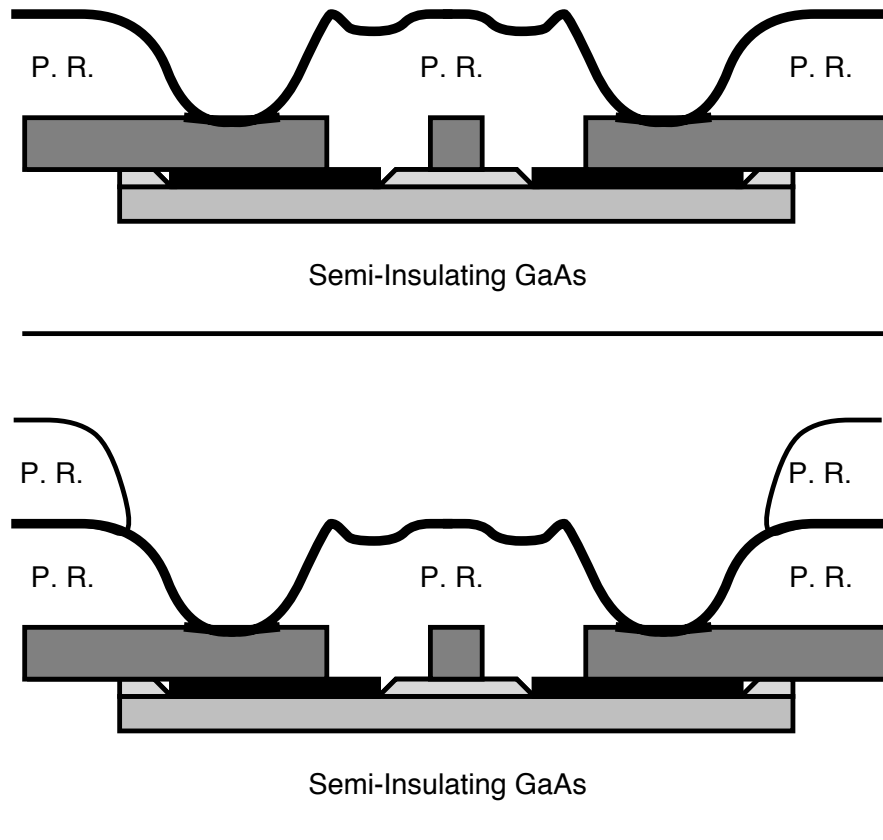


Figure 4.22: Cross sectional view of the air bridge process. Post baked photoresist (P. R.) is used to smooth edges. Air bridge terminals (posts) are first patterned, then the thin flash layer is sputtered, allowing electrical contact. A second layer of post baked photoresist is used to pattern the spans of the bridges.

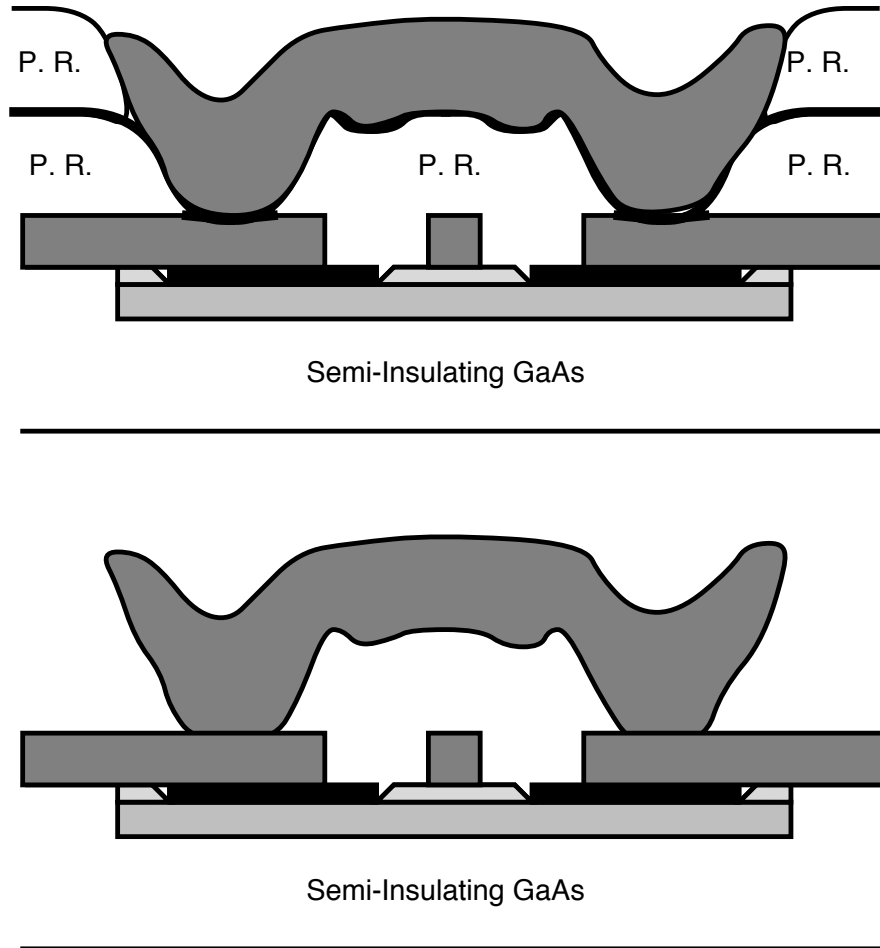


Figure 4.23: After patterning posts and spans, the air bridges are formed by electroplating $3\ \mu\text{m}$ of Au in these exposed areas. Very durable air bridges result. Photoresist and the remaining flash layer are then removed.

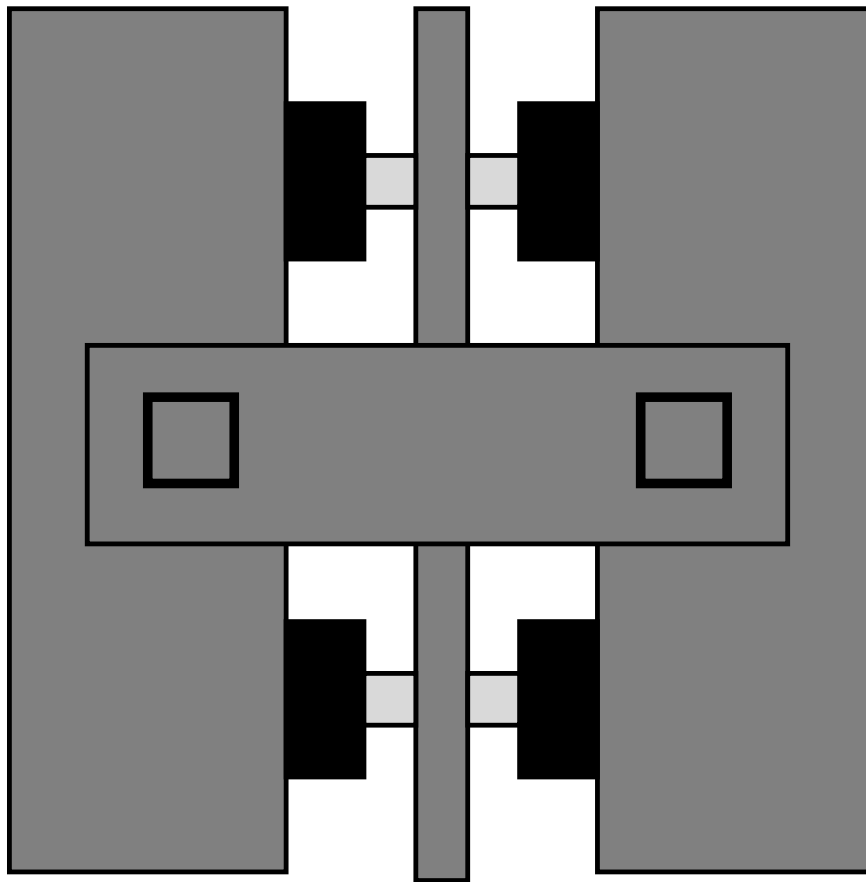


Figure 4.24: Top view of the completed process showing CPW, diode, and air bridge.

Chapter 5

Device Measurements

After defining NLTL operation, modeling the components, simulating the structure and fabricating the devices, they must be measured. Since the waveforms are very fast (ps transition times) and can be very large in amplitude (up to 20 V in simulation), making measurements can be difficult. It is nearly impossible to electrically couple broadband (DC to 400 GHz) signals from a wafer to a measurement device. Although very fine, high cutoff frequency coaxial cable exists [41], connectors are unavailable. Furthermore, there is no commercially available waveform measurement device covering the desired band. There are two possible solutions to these problems: use noninvasive electrooptic (EO) sampling techniques, or design and build a monolithic sampling circuit.

EO sampling relies on the electrooptic effect of (in this case) GaAs where the polarization dependent dielectric constant also depends on the electric field intensity in the material. The electrooptic effect causes a modulation in polarization of an incident laser impulse in proportion to the electric field in the GaAs. By detecting the polarization modulation, one can determine the electric field and hence the voltage on a GaAs circuit without interfering with device operation.

The temporal resolution of the EO system is generally limited by the laser impulse duration, timing jitter, and interaction time between the electrical and optical signals. The dynamic range of the system depends on the received optical power, laser noise, and the design of the polarization demodulator. The EO system at UCSB can either use a Nd:YAG laser which is limited to 5 ps resolution, or a Ti:Sapphire laser which has sub-ps impulse duration, but is a free-running laser. If the timing jitter of the Ti:Sapphire laser could be reduced through timing stabilization or some other technique, sub-ps resolution could be

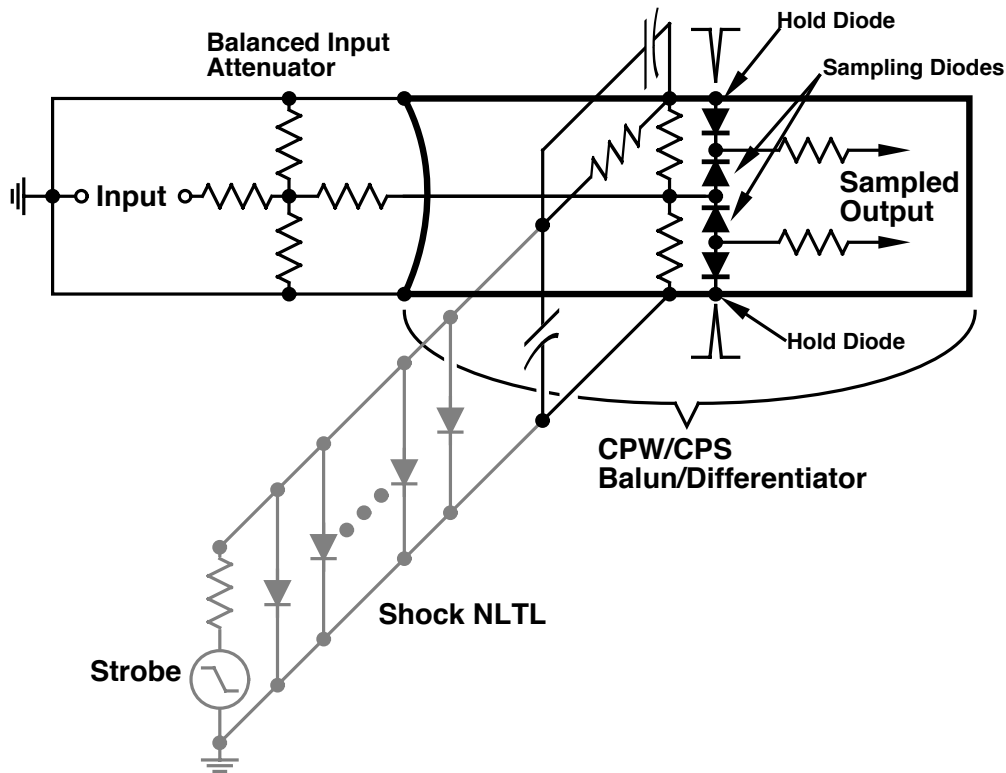


Figure 5.1: Schematic diagram of the high-speed sampling circuit used to measure NLTL output. The strobe NLTL generates a 1–2 ps 10%–90%, 5 V amplitude shock which in turn generates a symmetric pair of impulses which drive the sampling diodes.

attained. Currently, there is no timing stabilizer on the Ti:Sapphire laser system prohibiting its use. With these considerations in mind, a monolithic sampling circuit appears more promising, assuming better performance than laser-based systems can be achieved.

Ruai Yu designed a very high speed monolithic sampling circuit using a shock NLTL to gate switching diodes [37]. These samplers have demonstrated 1.8 ps 10%–90%, 5.3 V_{p-p} pulse measurements. These measurements are the convolution of the sampler's impulse response and the shock line's output, hence both sampler and shock have somewhat faster responses; the deconvolution of the two responses is not possible. By modifying his design, one is able to attain at least the same speed and increase the dynamic range by including a larger attenuator at the input. Figure 5.1 shows a schematic diagram of the shock NLTL

gated monolithic sampling circuit. A CPW shock NLTL is coupled through a two capacitor matching network to a pair of short-circuited CPS transmission lines. These lines act as a differentiator, creating a pair of symmetric impulses from the input pulse. These symmetric impulses are then coupled to the sampling diodes through reverse-biased diodes acting as hold capacitors. For the very short time the diodes are on, charge is coupled from the input to the hold “capacitors.” The voltage on these hold capacitors will be linearly related to the voltage at the input.

A large attenuator is used in the sampling circuit since the diode bridge has a dynamic range of 200–500 mV_{p-p}. A small difference in frequency (typically 100 Hz) between the input signal and sampling circuit gate signal allows convenient signal processing and measurement on low frequency oscilloscopes. The intermediate frequency (IF) bandwidth is limited by the signal acquisition hardware, and is normally in excess of 10 kHz, allowing rich harmonic content in the observed waveform. Voltage calibration is done by sweeping a DC current at the input, measuring the IF voltages, then computing the linear relationship between the input voltage ($V_{in} = I_{in}R_{in}$) and the two IF outputs. The input resistance can be measured on a test structure having no NLTL attached. This calibration routine assures the DC linearity of the sampler and allows accurate voltage measurements referenced to the sampler input (NLTL output).

5.1 First Generation Devices

The first generation of NLTL devices was completed in early June of 1990. This hyperabrupt wafer ($V_H = 14.1$ V, $N_0 = 2 \cdot 10^{17}$ cm⁻³, 425 nm thick diode layer) contained a shock line, two DHGs, and an impulse line. All the lines used 90 Ω interconnects and 50 Ω large-signal impedance. Mask layout was done using 3 μm design rules (i.e. Schottky contact width and spacing). Interconnect impedance optimization occurred at a later date. All NLTL cells used the “signal diode” configuration (figure 3.11).

The shock line had $f_{B,in} = 125$ GHz, $f_{B,out} = 900$ GHz, and $T_{comp} = 51$ ps. It was driven by a 22 dBm, 10 GHz sine wave with -2.5 V DC bias. The output was measured by a monolithic sampling circuit [37]. The measured step function has a 1.8 ps 10%–90% fall time and is 5.3 V_{p-p} (figure 5.2). An identical line was used to generate the sampling circuit gate impulses (strobe signal). This shock line has been the basis for most high speed systems developed in Dr. Rodwell’s research group. Subsequent generations of devices relied on this shock-strobed sampler for most measurements.

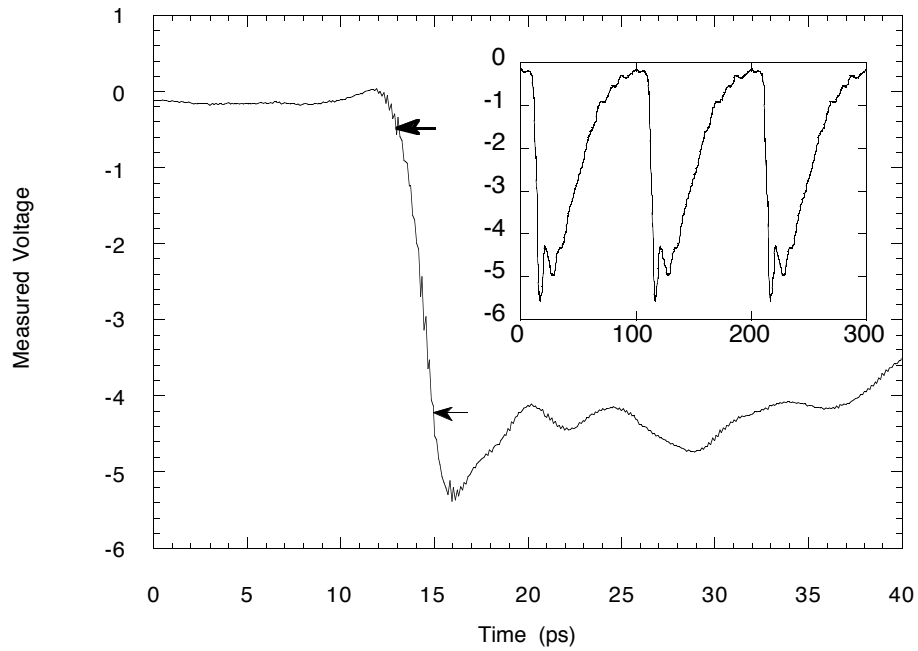


Figure 5.2: The NLTL has $f_{B,in} = 125$ GHz, $f_{B,out} = 900$ GHz, and $T_{comp} = 51$. The measured waveform is 1.8 ps 10%-90% fall time and 5.3 V_{p-p}. The line was driven by a 22 dBm, 10 GHz sine wave with -2.5 V DC bias.

There were two DHGs on the first generation wafer: 10 and 20 diode NLTLs with 44 GHz Bragg frequency. Both of these lines were designed as frequency doublers to the Ka-band. Output power vs. frequency measurements are shown in figure 5.3 and 5.4 for the 10 and 20 diode lines respectively. Measurements were made using a calibrated spectrum analyser. Simulation results are shown for comparison. The 10 diode line had a peak conversion efficiency of -7.4 dB at 34 GHz with a -3 dB bandwidth from 29–38 GHz. The 20 diode line had a peak conversion efficiency of -9.3 dB at 31 GHz with a -3 dB bandwidth from 26.5–36 GHz. The longer line had more loss, but a similar bandwidth to the shorter line. Simulations indicated more loss, but wider bandwidth for the 20 diode line. This is evidence of unmodeled effects, particularly due to the reduction in peak conversion frequency, possibly due to unmodeled layout parasitics. $75\ \Omega$ interconnects would greatly reduce loss in these structures and were implemented in the second generation.

The first generation of impulse lines had $f_{B,in} = 16$ GHz, $f_{B,out} = 890$ GHz, and $T_{comp} = 188$ ps. Since $90\ \Omega$ interconnects were used (along with a very high $f_{B,out}$), skin loss dominated the response (2251 squares of metal along the center conductor, $\approx 71\ \Omega$ at DC). The impulse of the waveform shown in figure 5.5 is 2.9 V_{p-p} and has a duration of 5.8 ps FWHM. The NLTL was driven by a 27 dBm sine wave with -3.0 V DC bias. The huge amount of attenuation necessitated the impedance optimization method discussed in chapter three. The impulses shown in figure 5.5 demonstrate impulse compression principles, but the output of the NLTL has about the same amplitude as a shock line.

This first generation of NLTLs demonstrated large discrepancies between simulation and measurements. Two significant problems were observed. Layout parasitics (shunt capacitance, series inductance) can reduce the Bragg frequency, particularly for cells designed for very high f_B . This may have caused slower shocks than simulated. Skin loss, unmodeled in time-domain simulations, can dominate an NLTL's response. These effects must either be modeled or their effects reduced in order for simulations to match measurements more closely.

5.2 Second Generation Devices

The second generation of NLTL devices was completed in late June of 1991. This hyperabrupt wafer ($V_H = 14.1$ V, $N_0 = 2 \cdot 10^{17}$ cm⁻³, 425 nm thick diode layer) was the same as used in the first generation. The significant difference was using $75\ \Omega$ interconnects, greatly reducing loss. Shock lines using $90\ \Omega$ interconnects were used to strobe the sampling circuits, minimizing variability in measurement.

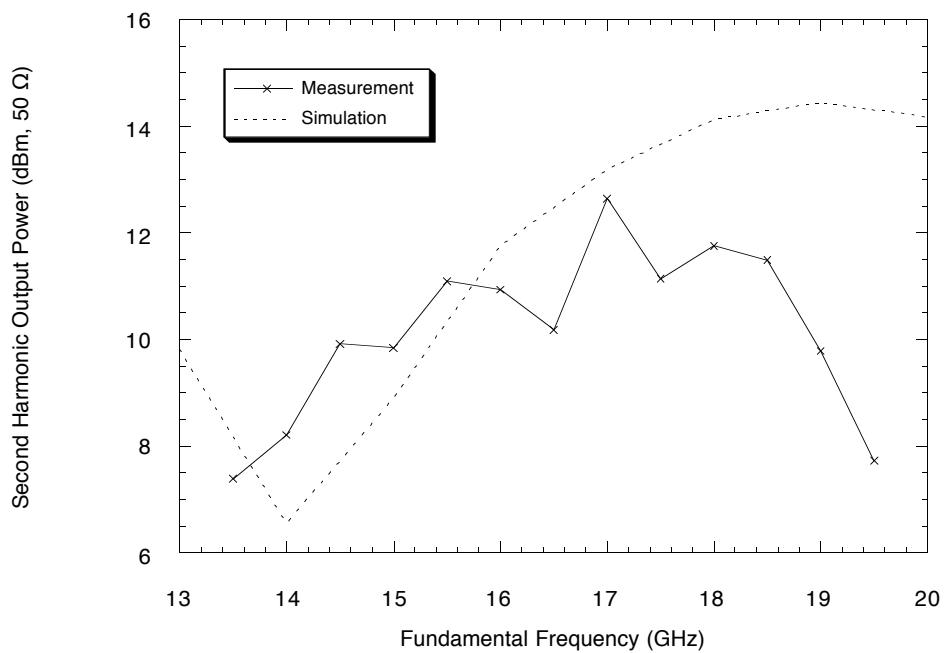


Figure 5.3: Measurement of the 10 diode Ka-band DHG. It has a peak conversion efficiency of -7.4 dB at 34 GHz with a -3 dB bandwidth from 29– 38 GHz. The line was driven by a 20 dBm sine wave with -2.4 V DC bias. The simulation is shown for comparison

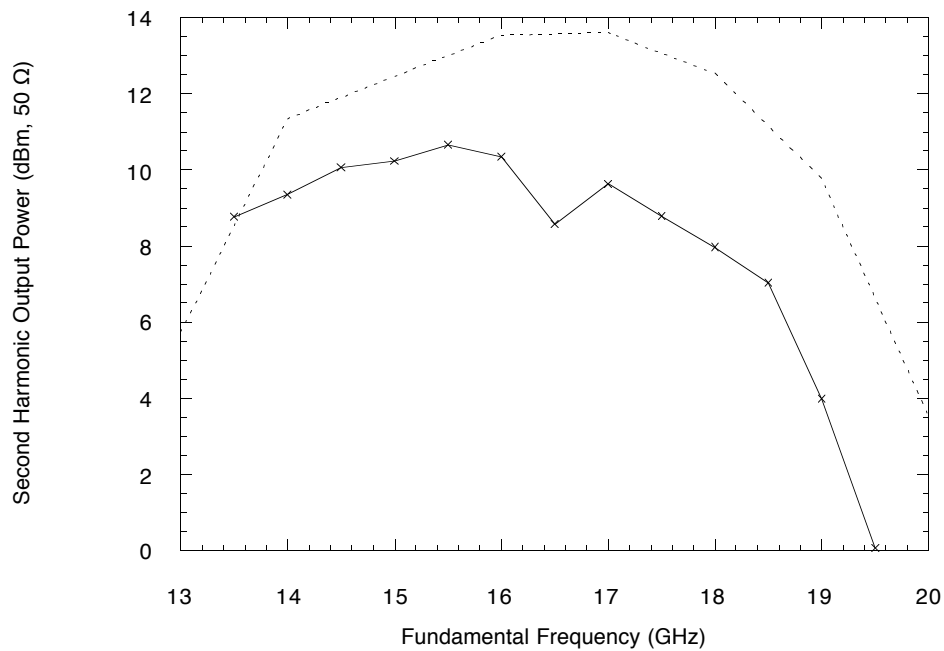


Figure 5.4: Measurement of the 20 diode Ka-band DHG. It has a peak conversion efficiency of -9.3 dB at 31 GHz with a -3 dB bandwidth from 26.5– 36 GHz. The line was driven by a 20 dBm sine wave with -2.6 V DC bias. The simulation is shown for comparison

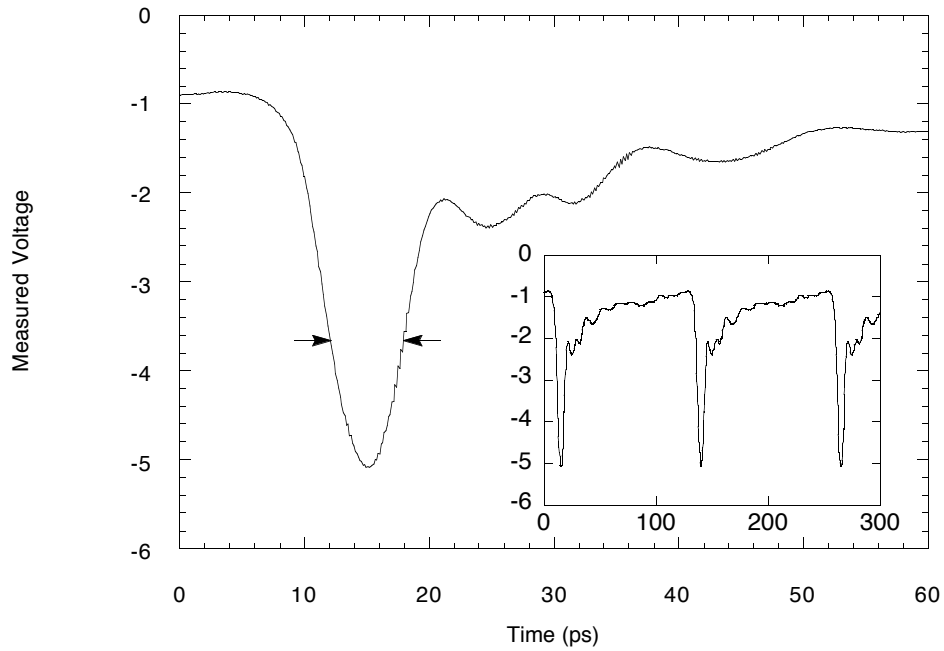


Figure 5.5: The impulse of the waveform is $2.9 V_{p-p}$ and has a duration of 5.8 ps FWHM. The NLTL was driven by a 27 dBm sine wave with -3.0 V DC bias. Metallic loss dominated the device's response.

Mask layout was again done using $3\ \mu\text{m}$ design rules (i.e. Schottky contact width and spacing).

Another difference between the first and second generation of devices was the implementation of the “ground diode” NLTL cell (figure 3.12). This allowed wider center conductors necessary for lower impedance CPW. It also introduced the problem of parasitic CPS modes which are not suppressed in this layout. Waveforms with large amounts of ringing were observed in initial measurements. After adding air bridges to the circuits, ringing due to CPS modes was nearly eliminated. Better efficiencies in harmonic conversion and larger impulses were measured.

There were two DHGs on the second generation wafer: a V-band doubler and a W-band tripler. Measurements were made using a calibrated shock line strobed sampling circuit rather than the Ka-band spectrum analyser used before. Simulation results are shown for comparison and include diode breakdown effects not modeled in chapter four. The V-band doubler (figure 5.6) had a peak conversion efficiency of -6.6 dB at 56 GHz with a -3 dB bandwidth from < 52 –63 GHz. The W-band tripler (figure 5.7) had a peak conversion efficiency of -10.5 dB at 78 GHz with a -3 dB bandwidth from < 78 –108 GHz. The source was limited to the Ka-band (26.5–40 GHz), limiting the low end of frequency drive.

Due to limitations in our sources, the complete frequency response of the DHGs could not be measured. Other sources were available from 6–18 GHz, but there is a critical gap between 18–26.5 GHz. The peak conversion efficiency was lower than simulation for the V-band doubler. This is most likely due to unmodeled layout parasitics which lower Bragg frequency. The W-band tripler shows substantial differences in response characteristics. Although not observed with the tripler, the parasitic effects become more noticeable as Bragg frequencies increase.

An attempt at a harmonic quadrupler consisting of two cascaded doublers was made. The two NLTLs had 67 and 136 GHz Bragg frequencies and were 15 and 13 diodes in length respectively. Although the fourth harmonic output power was small, the waveform consisted of high repetition rate compressed impulses. The cascaded set of NLTLs was driven with a 31.5 GHz, 24 dBm sine wave with a -3.7 V bias (figure 5.8) and produced $8.1\ \text{V}_{\text{p-p}}$, 4.5 ps FWHM impulses. A high repetition rate, large amplitude impulse train is useful diode switching and multiplexing circuits while a lower rate impulse train is better suited to samplers.

The second generation of impulse lines were designed to be driven at 15 GHz with $f_{B,in} = 24\ \text{GHz}$, $f_{B,out} = 225\ \text{GHz}$, and $T_{comp} = 120\ \text{ps}$, simply scaling the first generation lines. On measuring the devices, the best impulse shape

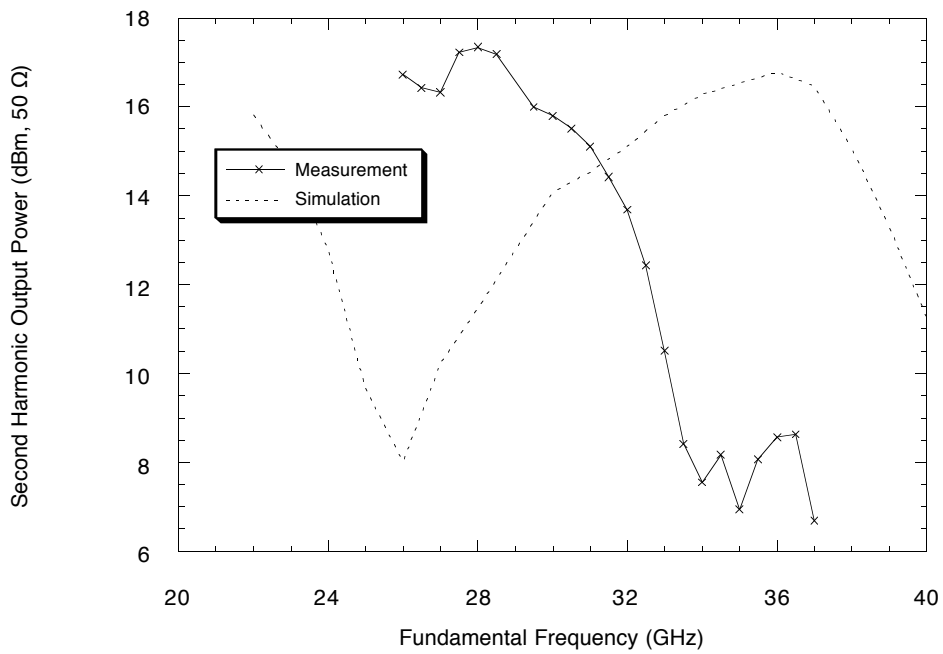


Figure 5.6: Measurement of the V-band doubler. This 15 diode, nominal 69 GHz NLTL has a peak conversion efficiency of -6.6 dB at 56 GHz with a -3 dB bandwidth from < 52–63 GHz. The line was driven by a 24 dBm sine wave with -4.6 V DC bias. The simulation including breakdown effects is shown for comparison

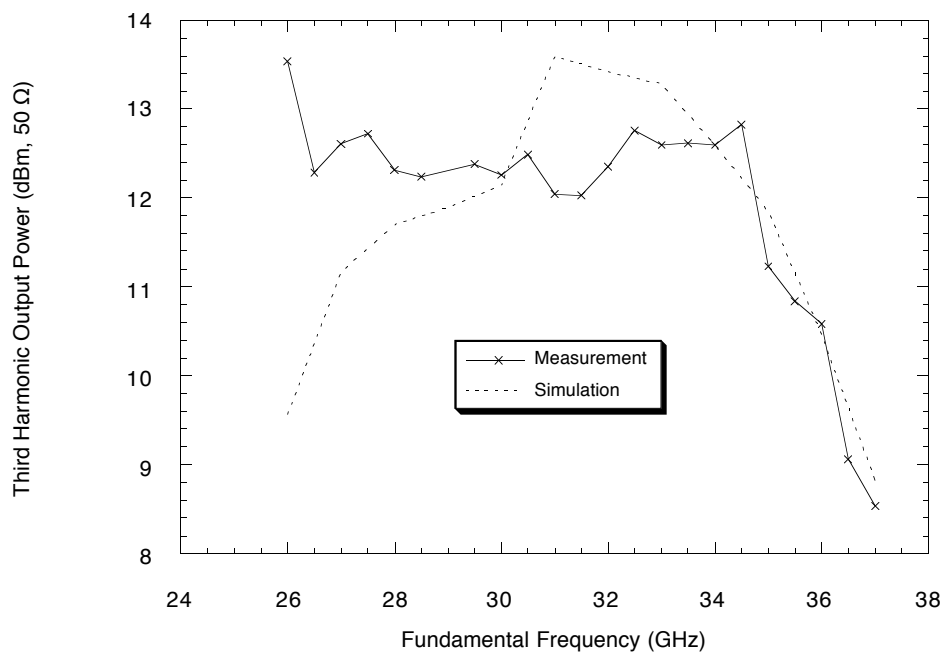


Figure 5.7: Measurement of the W-band tripler. This 20 diode, nominal 99 GHz NLTL has a peak conversion efficiency of -10.5 dB at 78 GHz with a -3 dB bandwidth from < 78–108 GHz. The line was driven by a 24 dBm sine wave with -4.6 V DC bias. The simulation including breakdown effects is shown for comparison

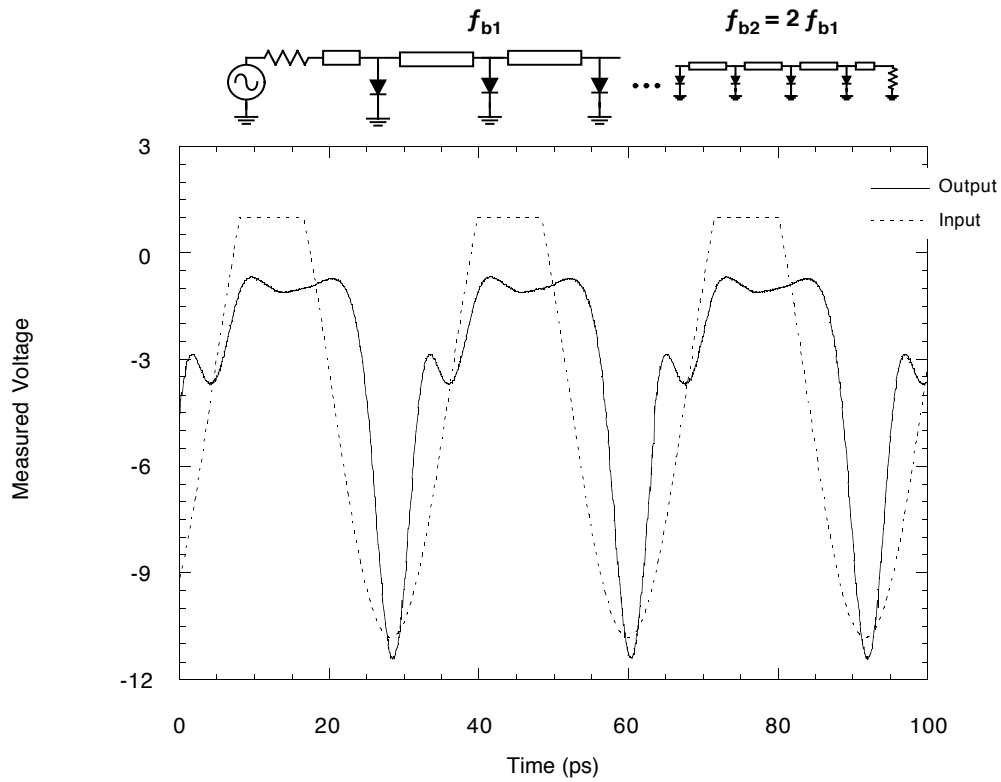


Figure 5.8: A high repetition rate impulse compressor was measured which consisted of two NLTLs having 67 and 136 GHz Bragg frequencies that were 15 and 13 diodes in length respectively. The cascaded set of NLTLs was driven with a 31.5 GHz, 24 dBm sine wave with a -3.7 V bias and produced 8.1 V_{p-p}, 4.5 ps FWHM impulses.

occurred using 9 GHz drive. The impulse of the waveform shown in figure 5.9 is $11.4 V_{p-p}$ and has a duration of 5.1 ps FWHM. The NLTL was driven by a 27 dBm sine wave with -3.0 V DC bias. This NLTL was also driven by a 3.22 GHz step recovery diode (SRD) impulse train generator to demonstrate lower repetition rate impulse compression. The SRD produced an impulse train of $9.1 V_{p-p}$, 27.9 ps FWHM impulses, and the NLTL impulse compressor's output (figure 5.10) was $12.8 V_{p-p}$, 5.1 ps FWHM. Both measured waveforms have a secondary impulse following the main impulse by 10 ps; this is most likely a reflection of the main impulse. A secondary soliton in the waveform would occur at a much later time (see simulation in figure 4.13). The impulse width is still nearly twice the predicted duration. Again, layout parasitics may have reduced the output Bragg frequency to cause this.

Note that the impulse duration for the first and second generation of impulse NLTLs is nearly the same even though $f_{B,out}$ differs by $4\times$. One explanation for this is that the waveform on the first generation impulse line was smaller at the output and its baseline dropped from 0 to about -1 V. Both of these effects tend to reduce the nonlinearity of the diodes, and reduced nonlinearity in the presence of loss greatly inhibits soliton interactions. The second generation device had one third the number of squares of metal in the center conductor. This, in addition to the ground plane diodes, reduced discrepancies between simulation and measurement that were so great in the first impulse line.

The second generation of devices demonstrated a very important design issue. Too many design changes causes confusion regarding which change produced which effect. Preliminary measurements showed very strong ringing which changed with different drive frequencies. Since the attenuator, sampler, and cell layouts were all changed, it was unclear exactly which change caused this excessive ringing. Undesired CPS modes from the new cell design caused this ringing which was greatly reduced after adding air bridges.

5.3 Third Generation Devices

The third generation of NLTL devices was completed in early December of 1992. Two wafers were fabricated: a hyperabrupt wafer ($V_H = 14.1$ V, $N_0 = 2 \cdot 10^{17} \text{ cm}^{-3}$, 425 nm thick diode layer), the same as used in the first generation, and a uniform wafer (10^{17} cm^{-3} , 350 nm thick diode layer). 75Ω interconnects and series diodes were used. On the hyperabrupt wafer, samplers using first generation shock lines were used, but longer lines were required on the uniform wafer to accommodate the lower compression. Mask layout was done using $2 \mu\text{m}$

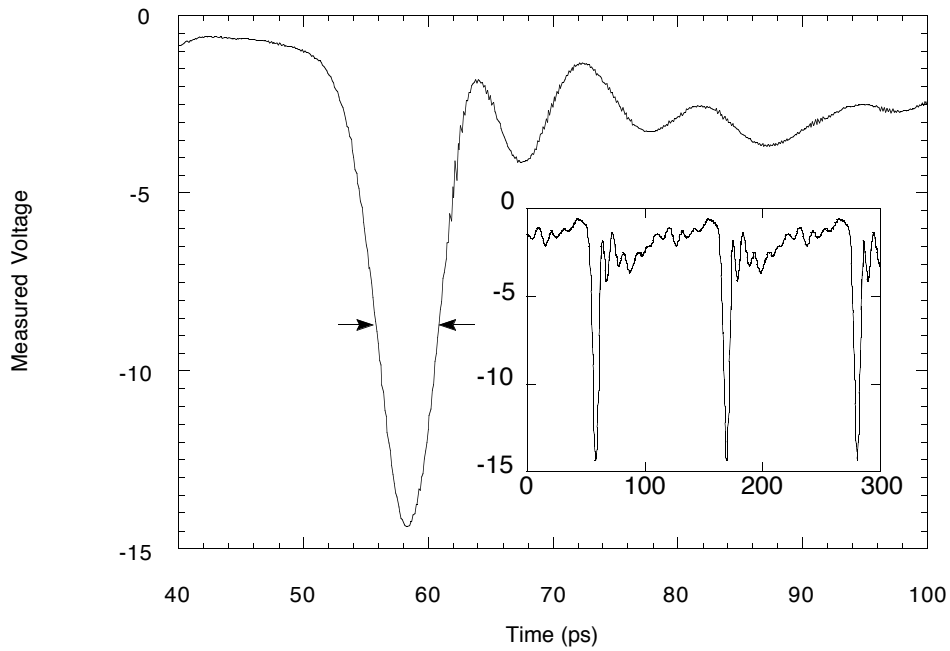


Figure 5.9: The second generation impulse compression NLTL was driven by a 27 dBm sine wave with -3.0 V DC bias. The impulse of the waveform is 11.4 V_{p-p} and has a duration of 5.1 ps FWHM. Large amplitude, short duration impulses were produced, but nearly twice the duration as expected.

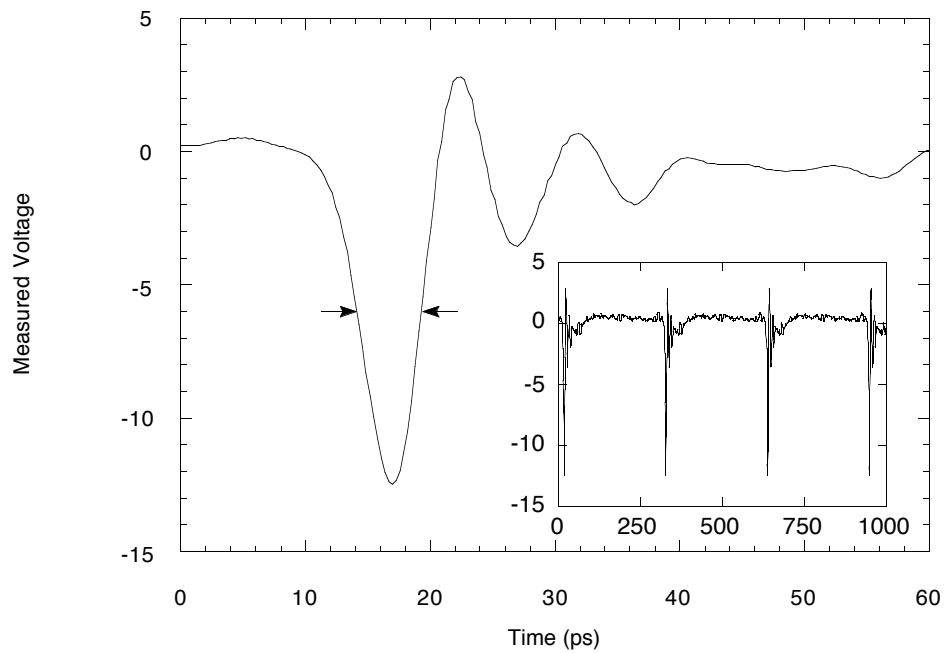


Figure 5.10: In order to demonstrate low repetition rate impulse compression, the second generation NLTL was driven by a 3.22 GHz step recovery diode. The impulse of the output waveform is $12.8 V_{p-p}$ and has a duration of 5.1 ps FWHM.

Schottky contact width and $3\ \mu\text{m}$ Schottky to ohmic spacing.

Two sets of lines were designed, one intended for the hyperabrupt wafer and one for the uniform. The single impulse compression line for the hyperabrupt doping used the same parameters as the second generation impulse line, but implemented series diodes which reduced normalized compression and increased length. Six lines were designed for the uniform doping as described in chapter four, consisting of three different input Bragg frequencies ($f_{B,in} = 67, 80, \text{ and } 93\ \text{GHz}$), two compression times ($T_{comp} = 25\ \text{ and } 35\ \text{ps}$), and all having a 450 GHz output Bragg frequency.

The impulse compression line designed for the hyperabrupt wafer was intended to test the effect of diode breakdown and slew rate limitations. As described in chapter three, the diodes have a breakdown voltage in the vicinity of peak voltage measurements shown in figure 5.9. Also, the slope of that curve showed a slew rate near the limit predicted in chapter three. By using series diodes, the breakdown and slew limits should double. The penalty is increased loss due to a smaller normalized compression and increased diode loss (lower $f_{C,LS}$).

The impulse compression lines designed for the uniform wafer were attempts to double the speed of previous measurements. By scaling the second generation impulse line's parameters from 9 GHz drive to 30 GHz and nearly doubling the cutoff frequency of the diodes, $\approx 2\times$ faster impulses should result. Several different line parameters bracketing the scaled line's were used to accommodate possible nonlinear scaling laws.

The first generation sampling circuit was used to measure both first and second generation NLTLs. The response of this circuit showed $\leq 1.8\ \text{ps}$ rise time. Since the speed of the new lines should approach this, increasing the sampler's bandwidth by decreasing the differentiator round trip time by 20%, reducing the sampling diode areas by 56%, and increasing the input attenuation was attempted. Unfortunately, these modifications, instead of increasing the sampler's speed, caused it to cease functioning properly.

Since a copy of the first generation shock line existed on the mask, a method of testing the sampling circuit's operation was provided. This measurement is shown in figure 5.11. Although measuring an identical circuit, the new sampling circuit shows a much different waveform than figure 5.2: it has a different shape, smaller amplitude ($2.5\ V_{p-p}$), and a slower fall time (2.3 ps). These symptoms were confusing. The $C(V)$ and $I(V)$ measurements indicated the correct doping profile and overall good diode performance. Network analysis indicated similar RF performance to earlier devices. The discrepancy in measured waveforms had

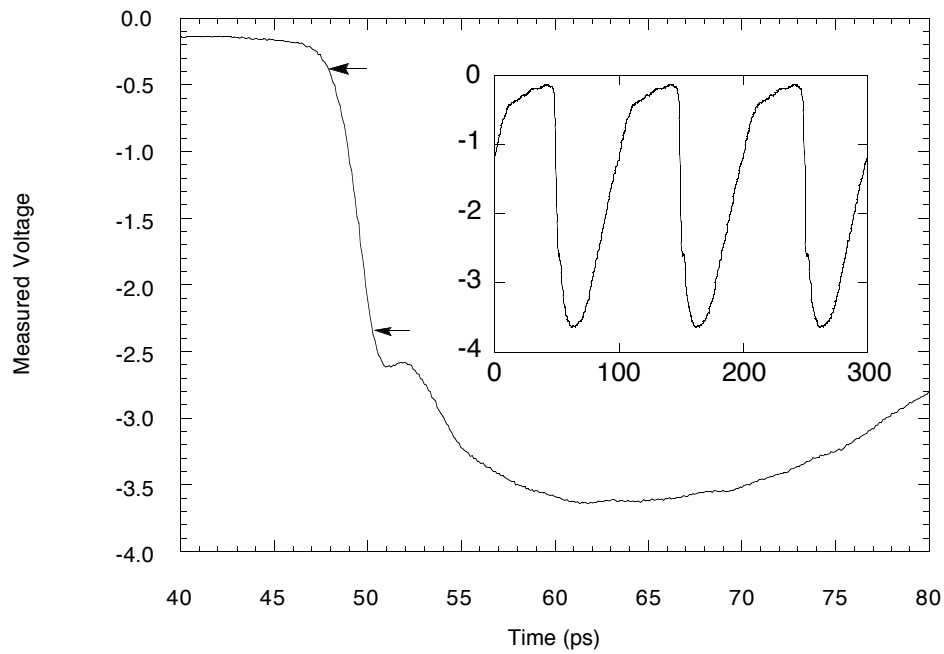


Figure 5.11: Response of the first generation shock line as measured by the modified sampling circuit. Although the design parameters and drive conditions were the same as the first generation line, the measured response shows a much different waveform than figure 5.2: it has a different shape, smaller amplitude ($2.5 V_{p-p}$), and a slower fall time (2.3 ps).

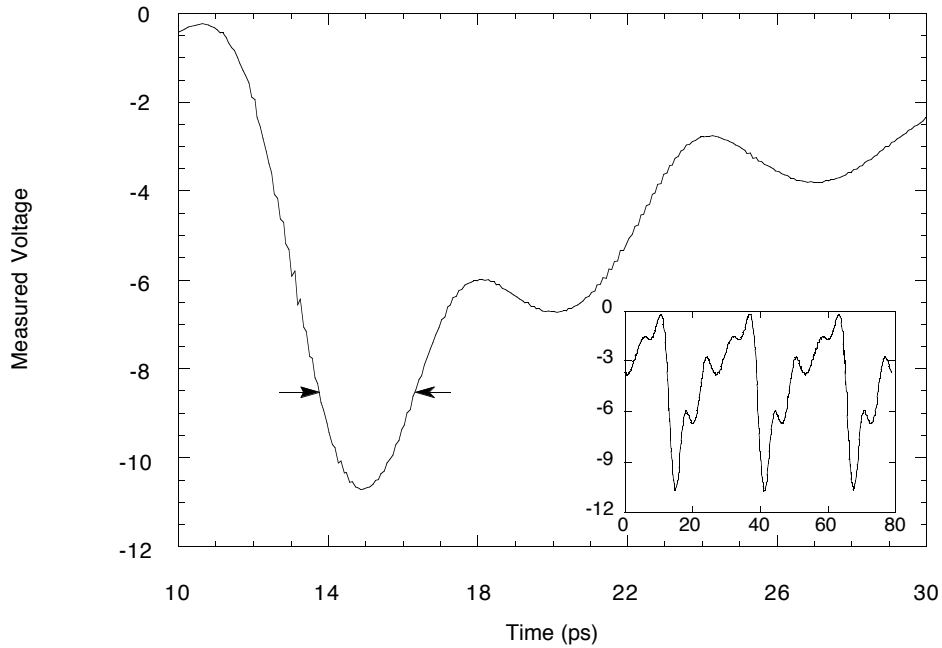


Figure 5.12: Output of an NLTL with $f_{B,in} = 67$ GHz and $T_{comp} = 25$ ps as measured by the modified sampling circuit. A 34 dBm, 38 GHz sine wave drove the circuit. The DC voltage at the output of the line was measured with a fine needle probe to be -8 V, clearly indicating inaccurate sampler response.

to be due to sampling circuit itself, a result of my over-ambitious modifications.

A further proof of the sampling circuits inaccuracy was found by measuring the DC voltage with a fine needle probe at the NLTL's output and comparing that to the calibrated sampling circuit's response. The measured waveform of an impulse compression NLTL with $f_{B,in} = 67$ GHz and $T_{comp} = 25$ ps is shown in figure 5.12 being driven with a 38 GHz, 34 dBm sine wave. The calibrated sampler response shows a waveform with 4.4 V_{p-p} and 2.6 ps FWHM duration impulses with a -4.1 V DC level. The DC voltage measured by the probe was -8 V. This is nearly the *peak* voltage of the waveform shown. Clearly, the sampling circuit was not providing an accurate representation of the NLTL's output. The sampler may be compressing the waveform or slowing its response.

Since the monolithic sampling circuit failed to accurately measure the waveforms, several measurement alternatives were attempted. One attempt was to bring a high speed sampling circuit with a known response in close proximity to the NLTL's output. By capacitively coupling the impulse compression line's output to the coupled sampling circuit's input, a waveform proportional to the derivative of the output waveform is sampled. Unfortunately, the sampling circuit used for this capacitively coupled measurement had a 4 ps rise time (limited by bond wires and a transmission line attached to the sampler's input), too slow to make an accurate measurement of the third generation impulse compression lines.

In order to get a faster response, bonding an operational sampling circuit directly to the impulse compressor's output attenuator was done. By sawing between the defective sampling circuit and the impulse compression line, access to its output was achieved. Unfortunately, the dimensions were too small (23 μm center conductor, 16 μm gaps) for successful bonding and the result was a short circuit.

There are two possible solutions to this measurement problem. One is to return to the first generation sampling circuit design and refabricate the two wafers. This would require a larger attenuator, but the rest of the circuit could remain unchanged. This would involve generating a new mask set, obtaining more epitaxial wafers and processing them. These materials would cost approximately \$10,000 with at least a four week lead time. Processing could take from four to eight weeks and incur additional cost. This is an expensive and time consuming solution, but should prove successful.

A more rapid and inexpensive solution to measurement difficulties is to modify the EO sampling system. The main problem of this system is the jitter of the free running laser which causes phase noise. Kirk Giboney, the main researcher involved with the EO system, is attempting to circumvent this jitter problem by using a very high IF frequency. The intent is to use a modulation frequency in excess of the phase noise corner of the laser's spectral content. Unfortunately, the laser system is heavily used. Even preliminary testing has not been done due to an indefinite queue. If these measurements prove successful, a report on the third generation of impulse compression devices will be forthcoming.

Chapter 6

NLTL Arrays

The motivation for developing NLTL based impulse compressors is the generation of large amplitude, short duration waveforms for a variety of applications. A limitation of the CPW NLTL is that only two diodes can be placed in series (even this causes significant layout difficulties) and skin loss is substantial. As seen in chapter four, there is a tradeoff between diode cutoff frequency, depletion edge velocity, and breakdown voltage. Higher cutoff frequency diodes allow faster transitions but have lower breakdown voltages. By using several diodes in series, heavier doping can be used to increase cutoff frequencies and maintain both a high breakdown and slew limit.

If more than two diodes are to be placed in series, the CPW lateral dimensions become large in comparison to a wavelength. A large CPW structure with several diodes in series loading it is similar to two planes of diodes in the gaps between center conductor and ground planes. It will be shown later that for typical diode loading in a plane, the wave guiding structure mainly influences input and output coupling and has little bearing on propagation within the plane. A plane of diodes confines the propagating wave near the surface.

Skin loss can greatly reduce wave amplitude in CPW NLTLs. It dominated the first impulse NLTL's response and degrades the performance all the lines discussed so far. By using some wave guiding medium that does not require current flow in the direction of propagation, metallic loss can be virtually eliminated. It may be possible to eliminate such conductors in self-guiding planar diode arrays. One can extend the planar diode array to three dimensions by stacking planes. NLTL arrays would be capable of much greater waveform amplitudes than the CPW structures.

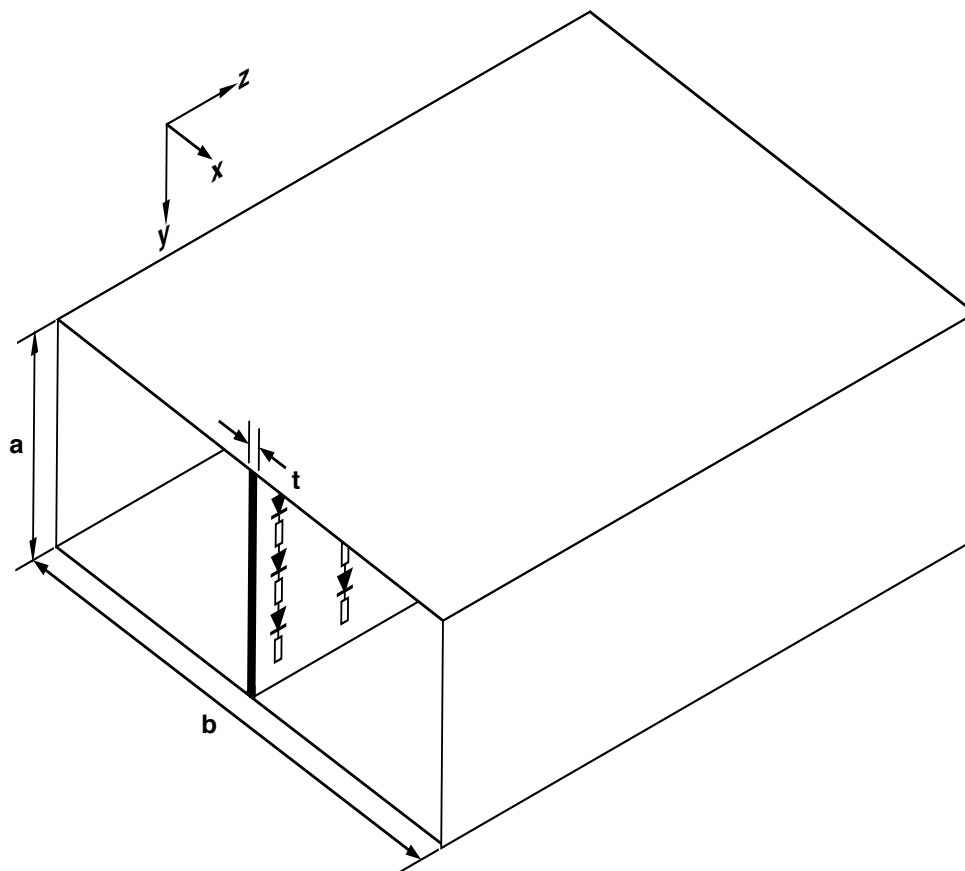


Figure 6.1: A Plane of diodes on its supporting substrate placed within a rectangular waveguide. This structure has propagation characteristics that are very different from unloaded waveguide.

6.1 Plane Arrays

Consider several series connected diodes periodically spaced in a plane, supported in a rectangular waveguide (RWG) (figure 6.1). This arrangement is termed finline [3]. By adding this plane of capacitance to the structure (both diode and substrate), the RWG will have very different propagation characteristics.

Approximating the effect of the diode plane and its supporting substrate as a simple capacitance per unit length of RWG (\bar{C}), one can use the transverse resonance method to determine the propagation constants. For the arrangement shown in figure 6.1, only odd TE modes will be effected by the diode plane.

This discussion will concentrate only on the TE_{01} mode. In order to achieve transverse resonance, the transverse input admittance at the plane of symmetry must be zero. By examining a section of the transverse (x-y) plane, an equivalent circuit can be constructed (figure 6.2). Assuming there is no variation in the y direction, the input admittance is

$$Y_{in} = j\omega \frac{\bar{C}}{2} - jY_0 \cot\left(\frac{k_x b}{2}\right) = 0 \quad (6.1)$$

where $Y_0 = k_x/(ka\eta_0)$ is the characteristic admittance of the RWG in the x direction and k_x is the propagation constant in the x direction. This reduces to

$$k^2 = \frac{2k_x}{\bar{C}c_0\eta_0 a} \cot\left(\frac{k_x b}{2}\right) = \frac{2\alpha_x}{\bar{C}c_0\eta_0 a} \coth\left(\frac{\alpha_x b}{2}\right) \quad (6.2)$$

where c_0 is the free-space velocity, η_0 is the impedance of free space (377Ω), k is the wave number, and α_x is the attenuation constant in the x direction ($\alpha_x = jk_x$). Combining equation 6.2 with the dispersion relation ($k^2 = k_z^2 + k_x^2 = k_z^2 - \alpha_x^2$) provides the propagation constant in the desired direction of propagation (z). The propagation constant in the x direction (k_x) becomes imaginary for frequencies above

$$\omega_x = \sqrt{\frac{4c_0}{\bar{C}\eta_0 ab}}. \quad (6.3)$$

For these frequencies, the wave is evanescent in the x direction and becomes guided by the plane of capacitance.

Consider a standard WR-28 waveguide ($a = 3.56$ mm, $b = 7.11$ mm) with a plane of capacitance centered (figure 6.2). The unloaded RWG has a cutoff frequency of 21 GHz, below which waves do not propagate. The capacitance per unit length of a wafer is $\bar{C} = \epsilon t/a$, 16 pF/m for a 0.5 mm thick GaAs wafer. Waves become surface guided above 14 GHz according to equation 6.3. Figure 6.3 shows the propagation relationships for this structure where the cutoff frequency has been reduced to 12 GHz for 16 pF/m loading. Larger capacitive loading reduces cutoff frequency further. For very small loading, a perturbational analysis is valid; this is often the case with narrow band finline circuits using very low dielectric constant material.

This plane of capacitance model is valid only if the wafer is much thinner than the field decay constant ($1/\alpha_x$). At 15 GHz the decay constant is 5 mm, $10\times$ the wafer thickness, so this approximation is invalid except for a narrow (12–15 GHz) range of frequencies; and these frequencies cannot even be launched into

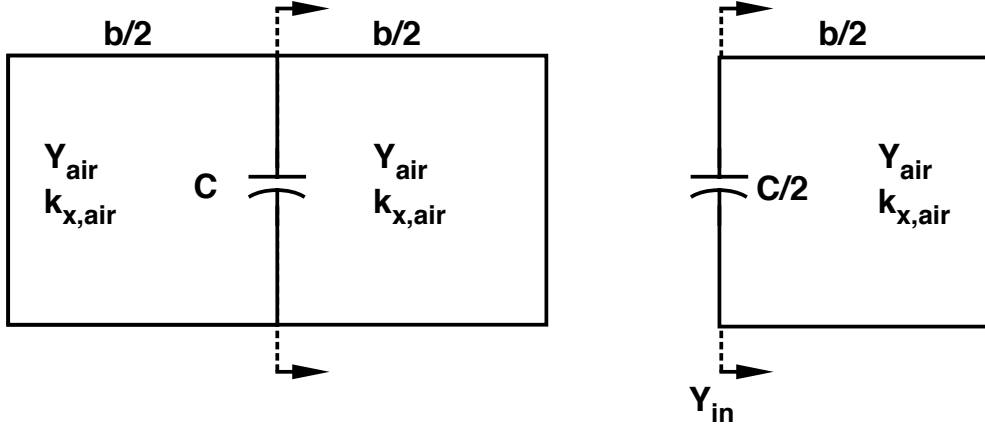


Figure 6.2: Equivalent circuit for the transverse resonance method. This approximation applies only if the lateral decay constant ($1/\alpha_x$) is much larger than the substrate thickness.

the unloaded structure. A plot of the decay constant vs. frequency is shown in figure 6.4. A better approximation for higher frequencies is to assume a uniform dielectric (GaAs) on one side of the capacitive plane (now the diodes alone), air on the other. Since the field decay lengths are very small at high frequencies, the actual size and boundary conditions at the edges have reduced importance. The transverse resonance method can be used again, but with a new circuit, figure 6.5.

Assuming high frequencies (evanescence in the x direction), the admittance for the GaAs side in the x direction is

$$Y_{GaAs} = -j \frac{\alpha_{x,GaAs}}{k\eta_0 a} \coth \left(\frac{\alpha_{x,GaAs} b}{2} \right), \quad (6.4)$$

for the air side is

$$Y_{air} = -j \frac{\alpha_{x,air}}{k\eta_0 a} \coth \left(\frac{\alpha_{x,air} b}{2} \right), \quad (6.5)$$

and for the capacitor is $Y_C = j\omega C$. By approximating the structure as infinitely wide ($b \rightarrow \infty$), the boundaries become absorbing, and the hyperbolic cotangents approach unity. This approximation is valid if the lateral decay constant is much *smaller* than the substrate thickness, the opposite condition to the first analysis. For a propagating mode, the total x direction admittance at the symmetry plane

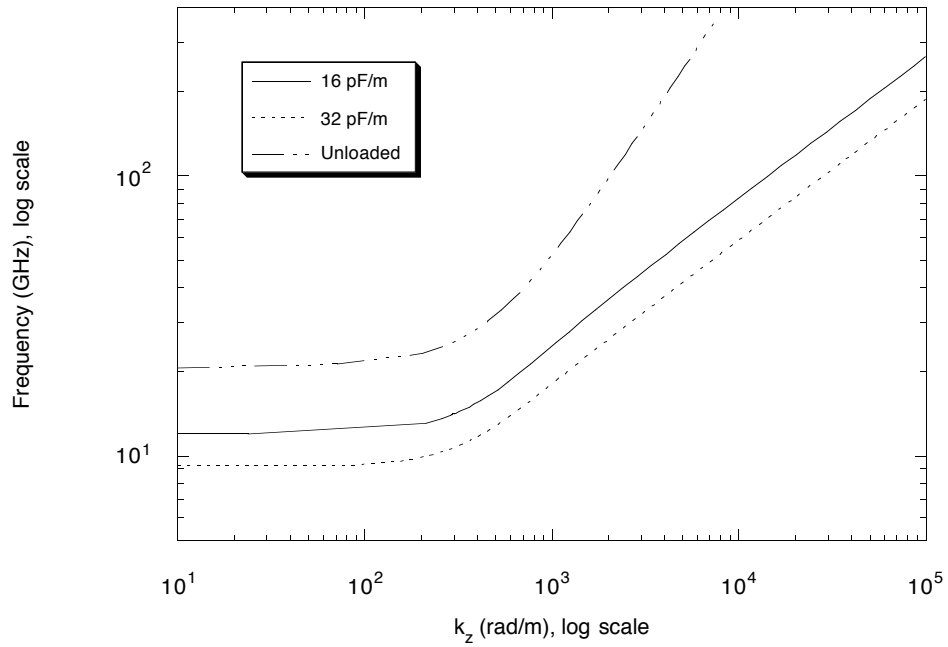


Figure 6.3: Dispersion relationship for the capacitively loaded RWG. An unloaded RWG has a 21 GHz cutoff, a 16 pF/m (0.5 mm thick GaAs wafer) loading reduces it to 12 GHz, and a 32 pF/m loading reduces it to 9 GHz. Note the slope of the curves. Capacitive loading causes stronger dispersion due to surface guiding effects.

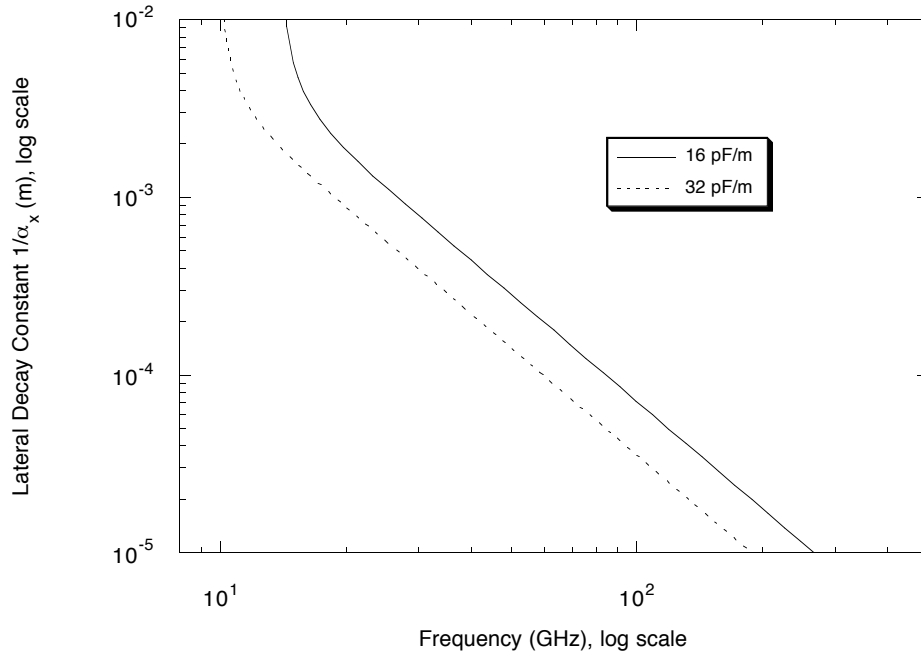


Figure 6.4: Lateral decay constant ($1/\alpha_x$) of the capacitively loaded RWG. The decay constant decreases as ω^2 for high frequencies. As the decay constant decreases to a value near the substrate thickness, the model is no longer valid.

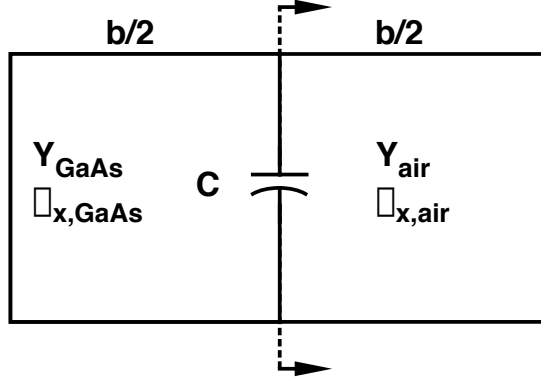


Figure 6.5: A new model for transverse resonance analysis. By taking the limit as $b \rightarrow \infty$ and assuming evanescence, absorbing boundaries replace the RWG.

must be zero: $Y_{GaAs} + Y_{air} + Y_C = 0$. This reduces to

$$k^2 c_0 \eta_0 a C = \alpha_{x,GaAs} + \alpha_{x,air} \quad (6.6)$$

and a new dispersion relation

$$k^2 = k_z^2 / \varepsilon_R - \alpha_{x,GaAs}^2 / \varepsilon_R = k_z^2 - \alpha_{x,air}^2 \quad (6.7)$$

is required (ε_R is the relative dielectric constant for the GaAs substrate). The revised propagation relation is shown in figure 6.6 assuming diode loading equal to the dielectric loading (16 pF/m). The lateral decay constant in GaAs ($1/\alpha_{x,GaAs}$) is shown in figure 6.7. In both figures, the curve corresponding to the original model (capacitive plane in RWG) with 32 pF/m loading (16 pF/m for the substrate, 16 pF/m for the diodes) is shown for comparison.

The above analyses approximated the propagation characteristics of a plane of closely spaced diodes on a substrate. With this information, the guided wavelength and degree of field confinement were determined. Unfortunately, the analysis did not consider wave impedance which is very important for NLTL design. In order to determine the wave impedance, the fields must be calculated everywhere in the structure. This degree of sophistication is not within the scope of this discussion. Also, in view of the design by simulation technique required for the CPW NLTL, a simulation tool capable of modeling both the array and the diode would be required; such a tool should allow impedance calculations and more.

One can transform the diode loaded RWG into an equivalent circuit by dividing it up into circuit equivalents in the x and z directions. Forcing uniformity

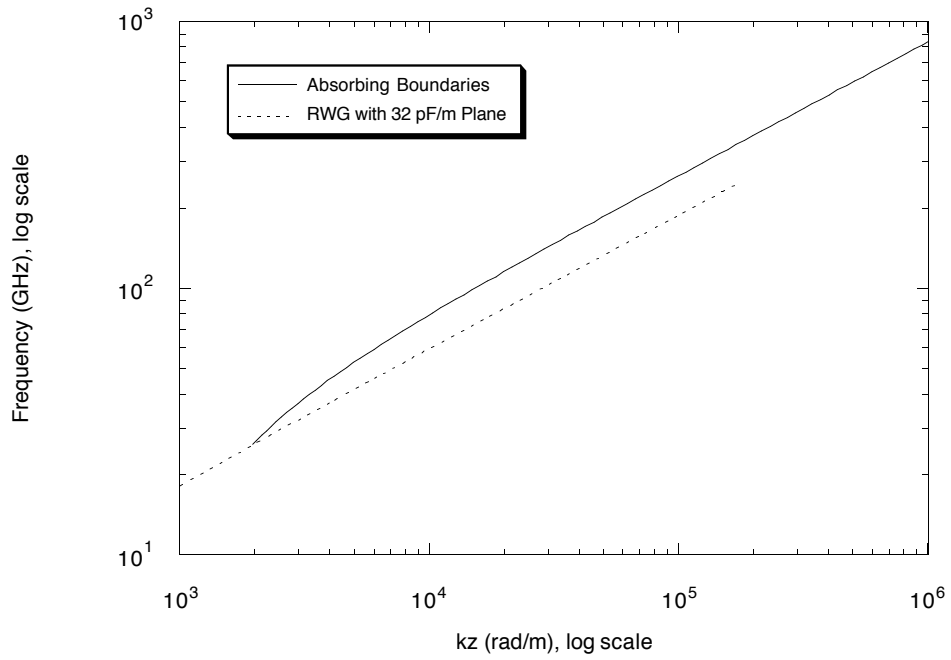


Figure 6.6: Dispersion relationship for the capacitively loaded RWG with absorbing boundaries and 16 pF/m diode loading. A curve is shown for the capacitive plane loaded RWG model with 32 pF/m (substrate + diodes) for comparison.

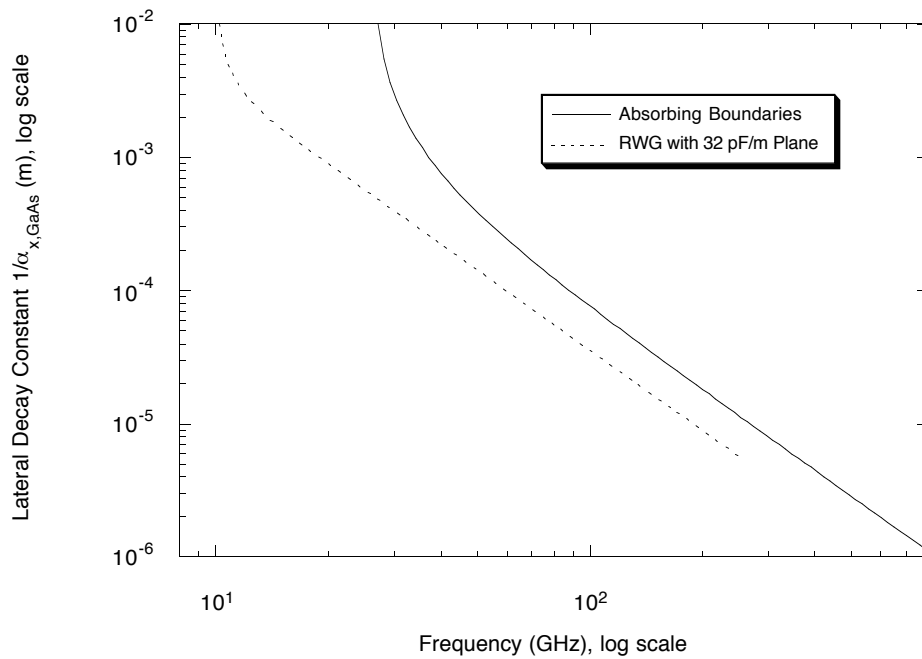


Figure 6.7: Lateral decay constant ($1/\alpha_{x, GaAs}$) of the capacitively loaded RWG with absorbing boundaries and 16 pF/m diode loading. A curve is shown for the capacitive plane loaded RWG model with 32 pF/m (substrate + diodes) for comparison.

in the y direction ($\partial/\partial y = 0$), the resulting circuit is a two dimensional grid of inductors with capacitors loading each node. This circuit can be derived from Maxwell's equations and the boundary conditions. Assuming the time-varying electric field is polarized in the y direction, Faraday's law provides the two relationships

$$\frac{\partial E_y}{\partial z} = \mu_0 \frac{\partial H_x}{\partial t} \text{ and } \frac{\partial E_y}{\partial x} = \mu_0 \frac{\partial H_z}{\partial t}; \quad (6.8)$$

and Ampere's law provides

$$\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} = \varepsilon \frac{\partial E_y}{\partial t}. \quad (6.9)$$

Now, applying the boundary conditions for the surface currents of the RWG, the magnetic intensity can be related to the surface current

$$\vec{J}_s = \hat{n} \times \vec{H} \quad (H_x = J_{s,z} \text{ and } H_z = -J_{s,x}). \quad (6.10)$$

where \hat{n} is the unit normal vector to the conductor's wall. One can then divide the RWG into small divisions (Δx and Δz) in the x and z directions. By taking the line integral of the electric field in the y direction, and surface currents in the transverse directions, one can relate the field intensities to voltage and current:

$$V = aE_y, \quad I_z = \Delta x J_{s,z}, \quad \text{and } I_x = \Delta z J_{s,x}. \quad (6.11)$$

Combining equations 6.8, 6.10, and 6.11, and quantizing spatial derivatives, equivalent series inductors can be determined with

$$\Delta V = \frac{a\Delta z\mu_0}{\Delta x} \frac{\partial I_z}{\partial t} \quad (6.12)$$

where ΔV is the change in voltage due to current in the z direction and the equivalent inductor in the z direction is $L_z = a\Delta z\mu_0/\Delta x$. Similarly for the x direction,

$$\Delta V = \frac{a\Delta x\mu_0}{\Delta z} \frac{\partial I_x}{\partial t} \quad (6.13)$$

and $L_x = a\Delta x\mu_0/\Delta z$. Shunt capacitances can be determined by combining equations 6.9, 6.10, and 6.11, and quantizing spatial derivatives, resulting in

$$\Delta I_z + \Delta I_x = \frac{\varepsilon\Delta x\Delta z}{a} \frac{\partial V}{\partial t} \quad (6.14)$$

where $\Delta I_z + \Delta I_x$ is the total change in current at a node and the equivalent capacitance is $C = \varepsilon\Delta x\Delta z/a$.

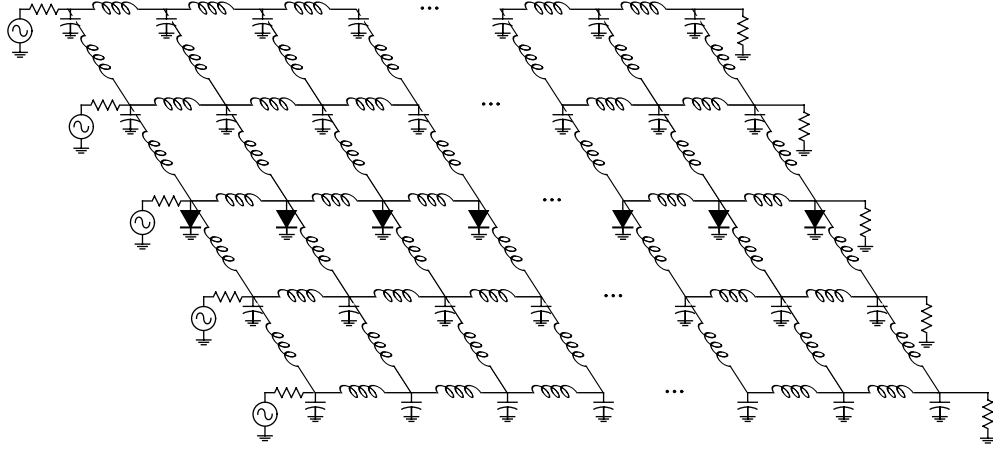


Figure 6.8: LC approximation of the RWG with a plane of diodes. Both generators and impedances must have correct magnitude and phase for rapid convergence. Limitations built in to SPICE prevented a sufficient number of elements to verify field confinement.

An analysis of the resulting LC mesh was attempted using SPICE. A circuit diagram is shown in figure 6.8. All generators and impedances must have the correct magnitudes and phases for rapid convergence; lacking this, the correct equivalent field distribution will evolve on propagation (escaping the near-field), but many more elements are required. By examining the voltage magnitude vs. frequency, one should be able to observe field confinement as reduced voltage away from the center of the structure, and measure impedance as a ratio of voltage to current. Unfortunately, a sufficient number of circuit elements to observe even the TE_{01} mode of the unloaded RWG could not be simulated due to the program's built in limitations. A 3-dimensional field modeling program or finite element analysis may be required, but these tend to expend vast amounts of computer resources and rarely treat nonlinearity.

Even with the limited characterization of the planar diode array, an NLTL design was attempted, in order to gain knowledge about the structure by measurement. This presented some problems. First, the loaded phase velocity (ω/k_z , neglecting periodicity) is inversely proportional to frequency at high frequencies. The Bragg frequency for this structure can be determined as

$$f_B = \frac{v_{phase,z} Z_{LS}}{\pi l Z_0} \quad (6.15)$$

where $v_{phase,z}$ is the phase velocity (ω/k_z) for the array without diode loading.

This forces diodes to be much more closely spaced than the CPW NLTL where $v_{phase,z}$ is constant. In fact, there is no circuit element available which approximates this strong dispersion. Another problem is coupling power into and out of the array.

The analysis showed that for sufficiently high frequencies, the metallic boundaries of the supporting RWG are not needed, indeed do not matter. In light of this, the array was placed on a dielectric lens to couple the output of the array to an antenna-based measurement system. This measurement system consists a bow tie antenna connected to a high speed sampling circuit which is strobed by an NLTL [23]. The simplest way to couple power into the array is to embed it in a coplanar strip (CPS) environment. This has a field pattern similar to the TE_{01} mode of the RWG, but requires a balanced signal. Since the input is a sine wave at a fixed amplitude, one can either use a simple matching network, or accept some power reflection due to mismatch.

In order for the array to radiate, an antenna is needed. As shown in chapter four, radiation can occur only if the guided wave velocity is larger than the wave velocity in the dielectric. The surface guided wave has a very slow velocity and will not radiate. Since the array is imbedded in CPS, an antenna consisting of a flared CPS is the best choice. By calculating the radiation loss of the flared CPS [5], one can determine the antenna's size based on the minimum frequency of radiation. By gradually reducing the diode loading towards the end of the array where the antenna begins, the wave should be coupled back into a CPS mode after being surface guided in the fully loaded array. The design parameters that were used follow:

1. Input: Ka-band traveling wave tube amplifier, assume 30 GHz at ≤ 10 watts. This provides $\leq 9 V_{p-p}$ on each diode in a 100Ω CPS system assuming 10 diodes in series.
2. Diode spacing: minimum diode spacing to achieve maximum Bragg frequency. This is limited by layout to $66 \mu\text{m}$, providing $f_B \approx 150$ GHz.
3. Diode area: designed to provide 16 pF/m as discussed, this requires $200 \mu\text{m}^2$ diodes with $50 \mu\text{m}$ spacing in the x direction assuming 10 diodes in series.
4. Array length: Assuming that the array will operate in a similar fashion to CPW NLTLs (except for velocity), one can determine the normalized compression ratio and large-signal parameters: $T_{comp} \approx \ell \cdot 6.5$ ps/mm. 3 mm of array were used.

5. Array to antenna transition: The diode area is continually reduced along a 1 mm length of CPS to couple from the surface guided mode into the unloaded CPS of the antenna.
6. Antenna: designed to radiate ≥ 30 GHz signals with ≥ 20 dB of return loss. This antenna has a 20° flare angle and is 8 mm in length.

Photomicrographs of the input to the array, a close-up, and transition section with the antenna are shown in figures 6.9, 6.10, and 6.11 respectively. Measurements have not been made on these arrays due to the difficulty of launching a balanced mode on the CPS at high power levels in the Ka-band. A report on these devices will be forthcoming.

6.2 Volume Arrays

Consider an NLTL constructed using parallel plate waveguide (figure 6.12) as a unit NLTL cell. Neglecting fringing fields and non TEM modes, the electric field is parallel to the diode direction. All NLTL parameters can be determined for this structure. Now, consider an $M \times N$ array of these parallel plate NLTLs (figure 6.13). Again, ignoring fringing fields, the electric field is parallel to the diodes. The field pattern resembles that of a plane wave in the limit of an infinite array. Horizontally adjacent cells will have equal electric fields (voltages), and currents flowing in vertically adjacent parallel plates will cancel.

If one were to remove the metallic boundaries of the parallel plates, the field pattern will remain the same due to the symmetry of the structure. Of course, at the edges of the structure these assumptions break down because the fields will fringe and currents will not cancel. The boundary conditions are important and will be discussed later. The resulting array of diodes would appear as figure 6.14, an array of planes of series connected diodes. The electric field must be parallel to the diodes and the Poynting vector must be in the plane of the diodes. This is a valid extension of the planar diode array discussed above.

The propagation characteristics of the volume array are similar to the planar arrays. At sufficiently low frequencies, the structure would appear as a homogeneous nonlinear dielectric built of parallel plate waveguides (c.f. RWG). As frequencies increase, waves will be confined to the planes of diodes and fields will decay between the planes; the parallel plate model breaks down. Since there is a large number of NLTLs in the array, very large amplitude signals should be possible.

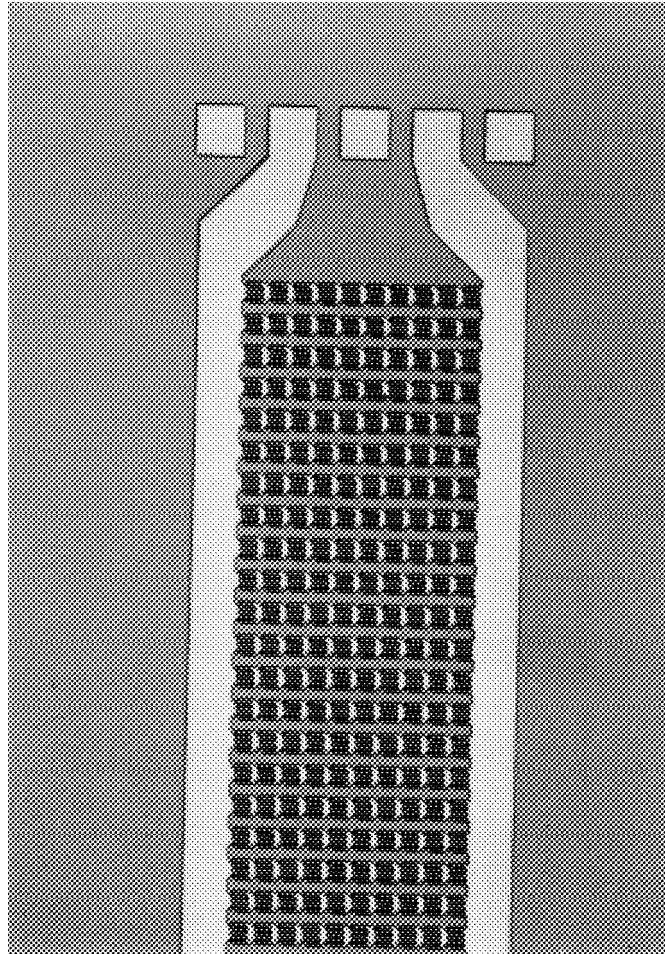


Figure 6.9: Photomicrograph of the input to the planar array. The contact pads are $100\ \mu\text{m}$ square and are designed to couple a balanced mode to the CPS of the array.

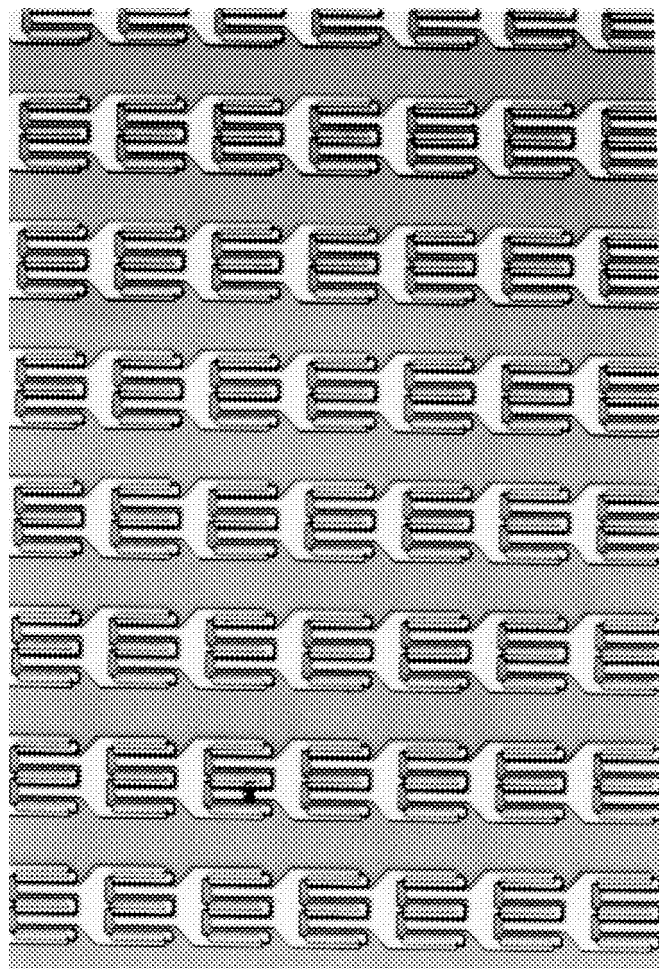


Figure 6.10: Photomicrograph of the planar array diodes. Even with this close spacing, the Bragg frequency is ≈ 150 GHz.

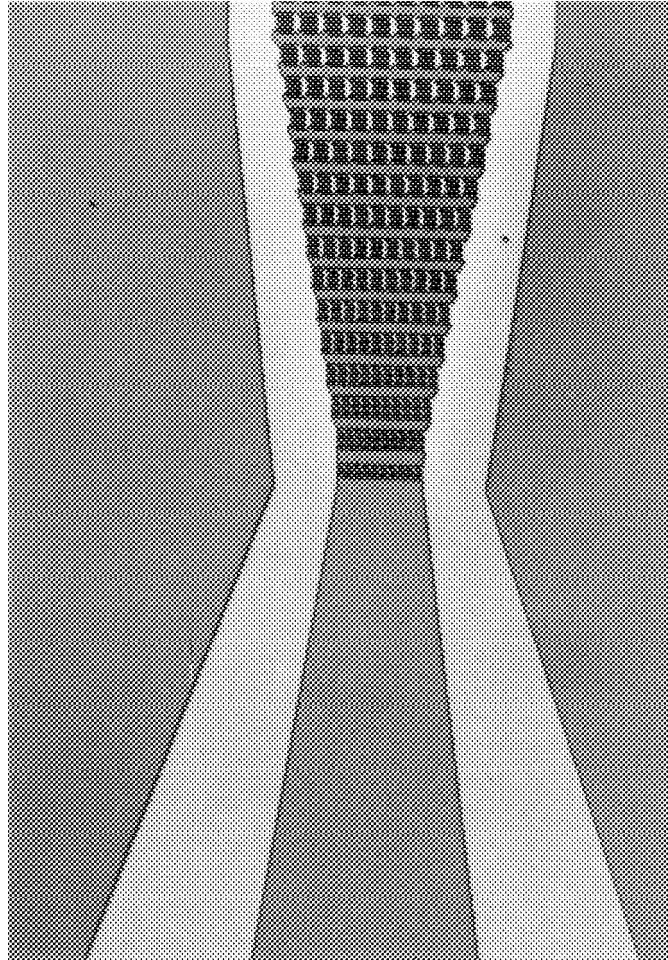


Figure 6.11: At the output of the array, diode areas are reduced in order to couple the surface guided mode back into the CPS mode. After this, a flared CPS is used to radiate the signals.

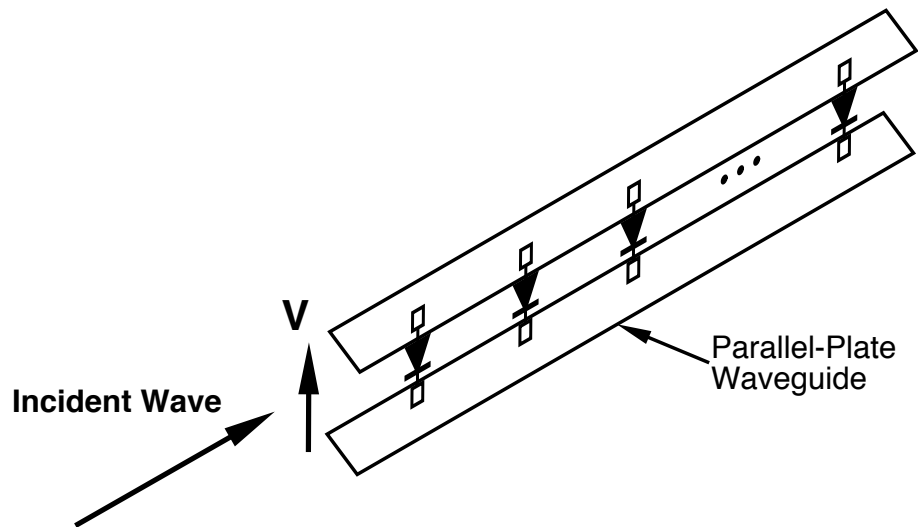


Figure 6.12: Unit cell for the volume array. It consists of a parallel plate waveguide operating in the TEM mode periodically loaded with diodes. This is an NLTL.

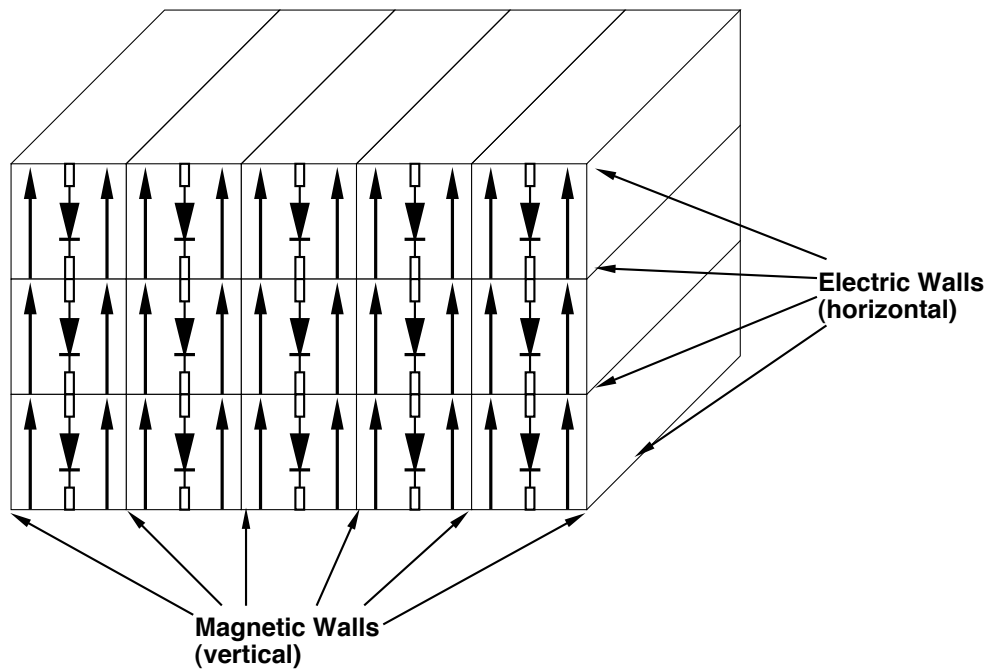


Figure 6.13: An $M \times N$ array of unit cells. Due to the symmetry of the structure, metallic boundaries can be removed.

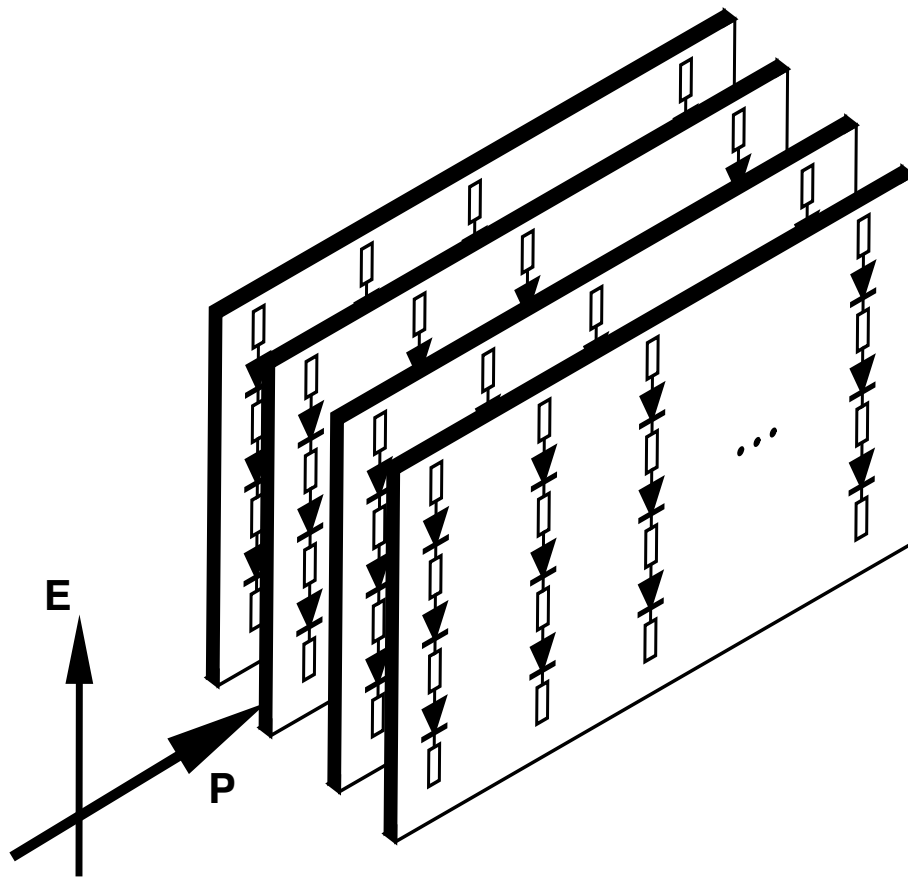


Figure 6.14: The $M \times N$ array of NLTLs can be thought of as (and fabricated as) a stack of planar diode arrays.

A stack of diode planes in free space would require a very intense, well confined beam of mm-wave radiation in order for the NLTL cells to develop a sufficient voltage swing to experience the nonlinearity of the diodes. Launching a plane wave into the structure presents some problems. The practical lower limit electromagnetic beam size is typically a circular spot with a half power diameter of one wavelength. At 30 GHz this is 1 cm, and assuming Ka-band drive the array need be no larger. Since the launched wave will not have uniform intensity, the wave will propagate at different speeds across the wave front, eliminating symmetry. Another problem is input and output matching to the array which will have a very low impedance (dielectric loaded with diodes).

The cutoff frequency of the arrays will either depend on the periodicity in the direction of wave propagation (Bragg frequency) or be limited by wave diffraction caused by periodicity in the transverse directions. Assuming diffraction is a limit, the arrays will not confine a beam for frequencies above $f_C = c/d\sqrt{\varepsilon_{R,eff}}$ where d is the spacing in the direction of consideration and $\varepsilon_{R,eff}$ is the effective relative dielectric constant including effects of diode loading. Assuming a square unit cell, the limit is set by the diode plane spacing. If one uses stacks of 0.5 mm thick GaAs wafers and assumes diodes double the effective dielectric constant, the limit is 120 GHz. Thinner substrates with lower dielectric constants would increase this limit. If one bonds GaAs diodes to quartz substrates and thins them to 50 μm , the limit is approximately 2 THz.

As the array becomes finer to allow higher frequency propagation, the power intensity required increases. Assuming a 2 V_{p-p} swing on each diode, the power intensity required is $\sqrt{\varepsilon_{R,eff}}/(2\eta_0 d^2)$ (watts per unit area). For the 0.5 mm GaAs wafers, this is 3 W/cm^2 , but for the quartz substrates, this increases to 150 W/cm^2 . The former power level is practical, but diffraction limits the bandwidth; the latter power level is difficult to attain, but the frequency range is very interesting. A supporting structure (e.g. waveguide) could reduce the incident beam size hence the minimum array size, but have minimal effect on propagation characteristics.

Consider a K-band ridged waveguide (figure 6.15). Filled with air, it can propagate waves from 12–40 GHz. The ridge area is 1.90×0.64 mm, much smaller than the 1 cm diameter free space beam. If one could place the volume array in this structure, many problems could be solved at once: boundary conditions are met (currents can flow in top and bottom part of waveguide), total power requirements are reduced (1.2 instead of 100 mm^2), and power coupling is facilitated (waveguide tuners can be used). Using low dielectric constant, very thin substrate arrays would allow wide bandwidth, high power waveforms to be

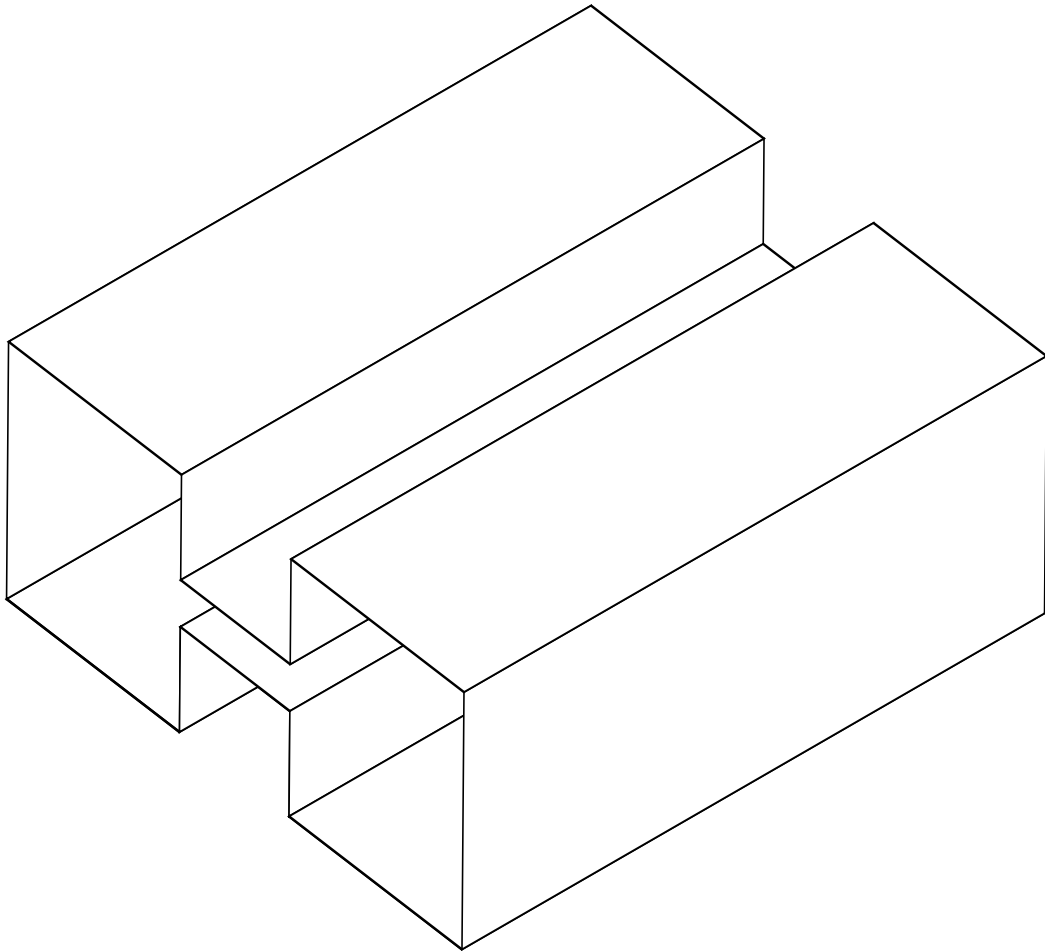


Figure 6.15: A K-band ridged waveguide. Overall dimensions are 7.7×3.3 mm, the ridge is 1.90×0.64 mm. Waves can propagate from 12–40 GHz in the unloaded structure without overmoding.

generated.

Since volume arrays draw on plane array analysis, the propagation characteristics discussed rely on many assumptions. If the characteristics of the plane arrays can be determined and assumptions revisited, the volume arrays would allow even greater power outputs. Imbedding the volume arrays in waveguide would greatly enhance their practicality. Much more intensive analyses must be done if these structures are to be realized, but the generation of very large power at near THz frequencies may be possible.

Chapter 7

Summary and Future Directions

The work presented here described the evolution of NLTLs through three generations. Shock lines capable of less than 1.8 ps transition times had sufficient amplitude to drive a sampling bridge. This large amplitude pulse generator is roughly $10\times$ faster than an SRD pulse generator with comparable amplitude and $10\times$ larger amplitude than an RTD pulse generator with comparable speed. Both second and third order broad band harmonic generators were shown with conversion loss as low as 6.6 dB covering the Ka-, V-, and W-bands. These harmonic generators have wider bandwidth than the classical resonant designs and higher efficiencies than conductive nonlinearity converters. Impulse compression lines were shown that produced $13 V_{p-p}$, 5 ps duration impulses, roughly $4\times$ faster and larger amplitude than comparable SRD impulse generators.

The first generation of devices suffered from excessive skin loss. This was corrected with great success in the second generation by reducing interconnect impedance. The third generation of devices could only be measured by the inaccurate monolithic sampler. My attempt to increase the sampler's speed resulted in their failure. Recent evidence has shown that the ion implantation encroaches nearly $1 \mu\text{m}$ laterally beyond the thick gold mask. Since the sampling diodes were reduced from 3×3 to $2 \times 2 \mu\text{m}$, the diodes were very poor. Electrooptic sampling techniques are being pursued to determine the performance of the third generation devices which implemented series diodes to increase breakdown and slew rate limitations.

Both first and second generation devices showed an increasing discrepancy between designed and realized Bragg frequency as f_B increased. This was most likely due to unmodeled parasitics resulting from diode to transmission line connections. Although not a limitation in itself, the NLTL cell layout plays a critical

role in realizing higher f_{BS} . A discussion of limits to NLTL performance was presented in chapter three. The fundamental limits are the diode and cell layout. Since one can design a diode with a very high DC cutoff frequency with reasonable nonlinearity and breakdown, other effects dominate. Other effects include the material properties at THz frequencies and physical (lithographic) limits in NLTL cell layouts.

As doping levels increase, the plasma resonance increases faster than the DC cutoff frequency. For heavily doped diodes, breakdown is the fundamental material limitation. Using series diodes should allow higher breakdown and cutoff frequency than single diodes. For the NLTLs presented here, the dominant effect was cell layout parasitics reducing designed Bragg frequencies.

Although the parasitics cannot be eliminated completely, their effects can be modeled by electromagnetic simulation. Including the parasitic layout effects and minimum geometries, the maximum Bragg frequency is limited by diode spacing in the slow ($113 \mu\text{m}/\text{ps}$) CPW environment. A faster phase velocity would allow higher Bragg frequencies with similar design rules. One possible way to achieve this is to use an air bridge for the CPW center conductor, touching down for Schottky contacts. An added advantage is the ability to use wider center conductors, reducing skin loss. Scott Allen is pursuing this technology development which may allow up to $3\times$ higher realized Bragg frequencies.

Nonlinear transmission line arrays were discussed in chapter six. These devices are promising for high power applications. From my preliminary analysis, the phase velocity can be very slow, limiting the maximum Bragg frequency hence pulse speed or harmonic content, but skin loss can be greatly reduced. If one could exchange the GaAs substrate for quartz, higher cutoff frequencies should be possible. The volume array can be considered as an array of plane arrays, and to fully understand the planar structure, a simulation tool combining finite element analysis with nonlinear simulation is required. Uddalak Bhattacharya is currently working on improving the understanding of these devices.

Sampling circuits driven by NLTL pulse generators with rise times $< 1.8 \text{ ps}$ were shown. These circuits have been used for a variety of system applications including optoelectronic samplers, time-domain reflectometers/spectrum analyzers, and spectroscopy systems [20, 38, 23]. So far, only sampling circuits have been monolithically integrated with the NLTLs; but they can also be integrated with HEMTs, HBTs, and other switching diode circuits.

Since very large amplitude impulses can be generated, they could be divided to drive several sets of switching devices (diodes or transistors). This would allow very high speed multiplexing and demultiplexing of digital signals. The output

of such a multiplexer could then be amplified (monolithically) to modulate a laser diode for optical communications. A demultiplexer driven by an NLTL could couple the output lines to high speed line driver amplifiers. One could also connect the IF output lines of a monolithic sampler to an on-wafer amplifier, greatly increasing the IF bandwidth and signal processing speed.

With the push for ever higher data rates, measurement bandwidths, communication carrier frequencies, and shorter gate delays and test signal responses, the need for low cost, high speed pulses and harmonic generators will continue. The existing NLTL technology presents such a low cost, efficient alternative to conventional techniques. By improving NLTL performance with better diodes, cell layouts, arrays, and possibly integrating the lines with transistor circuitry, future needs can also be met.

Appendix A

Automated NLTTL Layout Resources

The continuously tapered NLTTLs used throughout this work would have taken a very long time to lay out by manual drawing. The layout program ACADEMY [40] has a feature that eases this difficulty. It allows one to write a *macro* which can transform parametric data (eg. diode area, interconnect transmission line length, etc.) into layout information (polygon vertices, layer level, etc.). To further automate the process, I have written a C [46] program which takes the NLTTL parameters (compression time, large-signal impedance, etc.) and transforms them into a circuit file containing macro specifications which ACADEMY can read and transform into a layout. Depending on the specific NLTTL design, either the C program or the macro may have to be changed (perhaps both). Below are file listing of a typical C program and macro, in this case the ones used to lay out the shock NLTTLs.

A.1 C Program for Macro Implementation

```
#include <stdio.h>
#include <ctype.h>
#include <string.h>
#include <math.h>

#define PI 3.141592654 /* pi */
#define V 113.3893419 /* Velocity in GaAs um/ps */
```

```

main() {
int n,i,w,l;
float fb0,fbx,zls,zl,tcomp,rs,cjo,phi,m,iss,in,floss;
float vmax,vmin,cmax,cmin,qmax,qmin,cls,t0,tx,a0,cr;
float tline,k,lline,x,y,z,lng,area,sq,fb,lngb,atten;
char a[128],b[128],fsim[64],flay[64],t[1];
FILE *fs,*fl;

/*****
/* Introduction */
*****/
printf("This programme will generate NLTLs for you.\n");
printf("You can either do a homogeneous line, or an\n");
printf("inhomogeneous line. The difference is that\n");
printf("you enter either starting and ending bragg\n");
printf("frequencies (which determine the number of\n");
printf("sections and the tapering rule), or define\n");
printf("the number of sections and the tapering rule\n");
printf("(tapering rule = 1 for homogeneous line).\n");
printf("This programme uses a 6th order polynomial cap.\n\n");
printf("Please enter starting Bragg frequency (GHz) : ");
scanf("%s",a);
fb0=atof(a);
printf("Please enter ending Bragg frequency (GHz) : ");
scanf("%s",a);
fbx=atof(a);
printf("Please enter line compression (ps) : ");
scanf("%s",a);
tcomp=atof(a);
printf("Please enter large signal impedance (ohms) : ");
scanf("%s",a);
zls=atof(a);
printf("Please enter line impedance (ohms) : ");
scanf("%s",a);
zl=atof(a);

*****/

```

```

/* Get the diode data */
/*****/

/* Diode Parameters (1X1 diode) (ff, ohms) */
printf("\nDefault Diode Parameters: (1 um X 1 um)\n");
rs=171.9;
cjo=1.32767;
phi=1.27517;
m=0.810205;
iss=2.24;
in=1.82;
printf("Series resistance:      RS = %f ohm X um^2\n",rs);
printf("Zero-bias capacitance: CJO = %f fF / um^2\n",cjo);
printf("Barrier potential:      PHI = %f V\n",phi);
printf("Grading constant:       M = %f\n",m);
printf("Saturation current:     ISS = %f pA / um^2\n",iss);
printf("Ideality factor:        N = %f\n",in);

printf("\nDo you want to change them?");
scanf("%s",a);
if (a[0] == 'y') {
printf("Please enter RS = ");
scanf("%s",a);
rs=atof(a);
printf("Please enter CJO = ");
scanf("%s",a);
cjo=atof(a);
printf("Please enter PHI = ");
scanf("%s",a);
phi=atof(a);
printf("Please enter M = ");
scanf("%s",a);
m=atof(a);
printf("Please enter ISS = ");
scanf("%s",a);
iss=atof(a);
printf("Please enter N = ");
scanf("%s",a);

```

```

in=atof(a);
}

printf("\nPlease enter maximum then minimum voltage:\n");
printf("(reverse bias max then min e.g. 6 then 0.\n");
scanf("%s",a);
vmax=atof(a);
scanf("%s",a);
vmin=atof(a);

cmin=cjo/exp(m*log(1+vmax/phi));
cmax=cjo/exp(m*log(1+vmin/phi));

qmin=phi*cjo*exp((1-m)*log(1+vmin/phi))/(1-m);
qmax=phi*cjo*exp((1-m)*log(1+vmax/phi))/(1-m);

cls=(qmax-qmin)/(vmax-vmin);
t0=(1000*zls)/(PI*fb0*zl);
tx=(1000*zls)/(PI*fbx*zl);
a0=(zl/zls)*(zl/zls)-1;
cr=sqrt(a0)*(sqrt(1/a0+cmax/cls)-sqrt(1/a0+cmin/cls));
tline=tcomp/cr;

if(fbx != fb0) {
k=(tline-t0)/(tline-tx);
n=(0.5+log(tx/t0)/log(k));
lline=V*((t0-k*tx)/(1-k));
}
else {
k=1;
n=0.5+tline/t0;
lline=V*n*t0;
}

printf("\nThe line has the following parameters:\n\n");
printf("Large Signal Capacitance      : %f ff/um^2\n",cls);
printf("Compression ratio              : %f\n",cr);
printf("Tapering factor                  : %f\n",k);

```

```

printf("Number of sections          : %d\n",n);
printf("Total line length           : %f um\n\n",lline);

printf("Please enter circuit file name: ");
scanf("%s",fsim);
strcpy(fl原因,fsim);
strcat(fsim,"_sim.ckt");
strcat(fl原因,"_lay.ckt");
printf("\nThere will be two files: *_sim.ckt and *_lay.ckt\n");
fs=fopen(fsim,"w");
fl=fopen(fl原因,"w");
printf("\nDo you want to include transmission line loss?");
scanf("%s",a);
floss=10;
if (a[0] == 'y') {
printf("\nEnter skin loss frequency (GHz) : ");
scanf("%s",b);
floss=atof(b);
}

/* Write the files */

fprintf(fs,"! SPICE file for NLTL with %.2f
GHz initial Bragg frequency,\n",fb0);
fprintf(fs,"! %.2f GHz final Bragg frequency
and %f tapering rule,\n",fbx,k);
fprintf(fs,"! and %.2f ps total compression.\n",tcomp);
fprintf(fs,"DIM\n");
fprintf(fs,"  LNG UM\n");
fprintf(fs,"CKT\n");

fprintf(fl,"! Academy file for NLTL with %.2f GHz
initial Bragg frequency,\n",fb0);
fprintf(fl,"! %.2f GHz final Bragg frequency and
%f tapering rule,\n",fbx,k);
fprintf(fl,"! and %.2f ps total compression.\n",tcomp);
fprintf(fl,"DIM\n");
fprintf(fl,"  LNG UM\n");

```

```

fprintf(fl,"CKT\n");

x=((0.5*exp(zl/11.33893419)-1)/
(0.5*exp(zl/11.33893419)+1));
y=x*x*x*x;
z=(1-sqrt(1-y))/(2*sqrt(1-y));
for(i=1;i<n+2;i++) {
lng=V*t0*exp((i-1)*log(k));
lngb=lng*(1+k)/2;
area=1e6*((1-(zls/zl)*(zls/zl))/(PI*fb0*zls))*
exp((i-1)*log(k))/cls;
w=1+200/(1+2*z);

/* Determine aspect ratio, type and design rule */

while (lng < w*(1.5*(1+z*2))) {
w--;
}
if (w < 3) {
w=3;
}
if (area > 60) {
strcpy(t,"A");
l=4;
}
else if (area > 30) {
strcpy(t,"B");
l=4;
}
else {
strcpy(t,"B");
l=3;
}
sq += lng/w;
fb=fb0*exp((1-i)*log(k));
if (a[0] == 'n') {
atten=0;
}
}

```

```

else {
  atten=8.685889638*sqrt(floss*PI*1e9*
2.44e-8*4*PI*1e-7)/(2*zl*w);
}

fprintf(fl,"  NLTL%s_U%d  %d  %d
Z=%.2f W=%d ADI=%.2f LLI=%.2f LAM=%d !
fb=%.2f\n",t,i,i,i+1,zl,w,area,lng,l,fb);
if(i==1) {
  fprintf(fs,"  TLINP_TO 201 1 Z=%.2f L=%.2f
K=7 A=%e F=%f\n",zl,lng/2,atten,floss);
}
fprintf(fs,"  S1PA_D%d  %d  0  [MODEL=
MIKE AREA=%.2f] ! fb=%.2f\n",i,i,area,fb);
if(i==n+1) {
  fprintf(fs,"  TLINP_T%d  %d  %d  Z=%.2f
L=%.2f K=7 A=%e F=%f\n",i,i,i+1,zl,
lng/2,atten,floss);
}
else {
  fprintf(fs,"  TLINP_T%d  %d  %d  Z=%.2f
L=%.2f K=7 A=%e F=%f\n",i,i,i+1,zl,
lngb,atten,floss);
}
}
fprintf(fl,"  DEF2P 1 %d NLTL%d\n",i,i-1);
fprintf(fl,"! Total number of squares is %.2f\n",sq);

fprintf(fs,"  DEF2P 201 %d NLTL\n",i);
fprintf(fs,"! Total number of squares is %.2f\n",sq);
fprintf(fs,"MODEL\n");
fprintf(fs,"  MIKE D RS=%f CJO=%fE-15 VJ=%f &\n",rs,cjo,phi);
fprintf(fs,"          M=%f IS=%fE-12 N=%f\n",m,iss,in);
fprintf(fs,"SOURCE\n");
fprintf(fs,"  NLTL RES_RIN 201 202 R=50\n");
fprintf(fs,"  NLTL IVS_VIN 202 0
TRAN=SIN(-6 14 9E9 0 0 90)\n");
fprintf(fs,"  NLTL RES_RL %d 0 R=50\n",i);

```

```

fprintf(fs,"CONTROL\n");
fprintf(fs,"  NLTL TRAN 10E-12 2E-9\n");
fprintf(fs,"SPICEOUT\n");
fprintf(fs,"  NLTL TRAN V(ALL)\n");

fclose(fs);
fclose(fl);
exit(0);
}

```

A.2 Typical Circuit File Output from C program

A.2.1 SPICE Simulation File

```

! SPICE file for NLTL with 125.00 GHz initial Bragg frequency,
! 800.00 GHz final Bragg frequency and 0.982776 tapering rule,
! and 51.00 ps total compression.

```

```
DIM
```

```
  LNG UM
```

```
CKT
```

```

TLINP_T0 201 1 Z=90.00 L=80.21 K=7 A=0.0e+00 F=10.0
S1PA_D1  1  0 [MODEL=MIKE AREA=64.17] ! fb=125.00
TLINP_T1  1  2 Z=90.00 L=159.03 K=7 A=0.0e+00 F=10.0
S1PA_D2  2  0 [MODEL=MIKE AREA=63.07] ! fb=127.19
TLINP_T2  2  3 Z=90.00 L=156.29 K=7 A=0.0e+00 F=10.0
S1PA_D3  3  0 [MODEL=MIKE AREA=61.98] ! fb=129.42
TLINP_T3  3  4 Z=90.00 L=153.60 K=7 A=0.0e+00 F=10.0
S1PA_D4  4  0 [MODEL=MIKE AREA=60.91] ! fb=131.69
TLINP_T4  4  5 Z=90.00 L=150.96 K=7 A=0.0e+00 F=10.0
S1PA_D5  5  0 [MODEL=MIKE AREA=59.87] ! fb=134.00
TLINP_T5  5  6 Z=90.00 L=148.36 K=7 A=0.0e+00 F=10.0
S1PA_D6  6  0 [MODEL=MIKE AREA=58.83] ! fb=136.34
TLINP_T6  6  7 Z=90.00 L=145.80 K=7 A=0.0e+00 F=10.0
S1PA_D7  7  0 [MODEL=MIKE AREA=57.82] ! fb=138.73

```



```
TLINP_T7  7  8  Z=90.00 L=143.29 K=7 A=0.0e+00 F=10.0
S1PA_D8  8  0  [MODEL=MIKE AREA=56.82] ! fb=141.16
TLINP_T8  8  9  Z=90.00 L=140.82 K=7 A=0.0e+00 F=10.0
S1PA_D9  9  0  [MODEL=MIKE AREA=55.85] ! fb=143.64
TLINP_T9  9 10  Z=90.00 L=138.40 K=7 A=0.0e+00 F=10.0
S1PA_D10 10  0  [MODEL=MIKE AREA=54.88] ! fb=146.16
TLINP_T10 10 11  Z=90.00 L=136.01 K=7 A=0.0e+00 F=10.0
S1PA_D11 11  0  [MODEL=MIKE AREA=53.94] ! fb=148.72
TLINP_T11 11 12  Z=90.00 L=133.67 K=7 A=0.0e+00 F=10.0
S1PA_D12 12  0  [MODEL=MIKE AREA=53.01] ! fb=151.32
TLINP_T12 12 13  Z=90.00 L=131.37 K=7 A=0.0e+00 F=10.0
S1PA_D13 13  0  [MODEL=MIKE AREA=52.10] ! fb=153.98
TLINP_T13 13 14  Z=90.00 L=129.10 K=7 A=0.0e+00 F=10.0
S1PA_D14 14  0  [MODEL=MIKE AREA=51.20] ! fb=156.67
TLINP_T14 14 15  Z=90.00 L=126.88 K=7 A=0.0e+00 F=10.0
S1PA_D15 15  0  [MODEL=MIKE AREA=50.32] ! fb=159.42
TLINP_T15 15 16  Z=90.00 L=124.70 K=7 A=0.0e+00 F=10.0
S1PA_D16 16  0  [MODEL=MIKE AREA=49.45] ! fb=162.21
TLINP_T16 16 17  Z=90.00 L=122.55 K=7 A=0.0e+00 F=10.0
S1PA_D17 17  0  [MODEL=MIKE AREA=48.60] ! fb=165.06
TLINP_T17 17 18  Z=90.00 L=120.44 K=7 A=0.0e+00 F=10.0
S1PA_D18 18  0  [MODEL=MIKE AREA=47.76] ! fb=167.95
TLINP_T18 18 19  Z=90.00 L=118.36 K=7 A=0.0e+00 F=10.0
S1PA_D19 19  0  [MODEL=MIKE AREA=46.94] ! fb=170.89
TLINP_T19 19 20  Z=90.00 L=116.32 K=7 A=0.0e+00 F=10.0
S1PA_D20 20  0  [MODEL=MIKE AREA=46.13] ! fb=173.89
TLINP_T20 20 21  Z=90.00 L=114.32 K=7 A=0.0e+00 F=10.0
S1PA_D21 21  0  [MODEL=MIKE AREA=45.34] ! fb=176.94
TLINP_T21 21 22  Z=90.00 L=112.35 K=7 A=0.0e+00 F=10.0
S1PA_D22 22  0  [MODEL=MIKE AREA=44.56] ! fb=180.04
TLINP_T22 22 23  Z=90.00 L=110.42 K=7 A=0.0e+00 F=10.0
S1PA_D23 23  0  [MODEL=MIKE AREA=43.79] ! fb=183.19
TLINP_T23 23 24  Z=90.00 L=108.51 K=7 A=0.0e+00 F=10.0
S1PA_D24 24  0  [MODEL=MIKE AREA=43.03] ! fb=186.40
TLINP_T24 24 25  Z=90.00 L=106.65 K=7 A=0.0e+00 F=10.0
S1PA_D25 25  0  [MODEL=MIKE AREA=42.29] ! fb=189.67
TLINP_T25 25 26  Z=90.00 L=104.81 K=7 A=0.0e+00 F=10.0
S1PA_D26 26  0  [MODEL=MIKE AREA=41.56] ! fb=192.99
```

```
TLINP_T26 26 27 Z=90.00 L=103.00 K=7 A=0.0e+00 F=10.0
S1PA_D27 27 0 [MODEL=MIKE AREA=40.85] ! fb=196.38
TLINP_T27 27 28 Z=90.00 L=101.23 K=7 A=0.0e+00 F=10.0
S1PA_D28 28 0 [MODEL=MIKE AREA=40.15] ! fb=199.82
TLINP_T28 28 29 Z=90.00 L=99.49 K=7 A=0.0e+00 F=10.0
S1PA_D29 29 0 [MODEL=MIKE AREA=39.45] ! fb=203.32
TLINP_T29 29 30 Z=90.00 L=97.77 K=7 A=0.0e+00 F=10.0
S1PA_D30 30 0 [MODEL=MIKE AREA=38.77] ! fb=206.88
TLINP_T30 30 31 Z=90.00 L=96.09 K=7 A=0.0e+00 F=10.0
S1PA_D31 31 0 [MODEL=MIKE AREA=38.11] ! fb=210.51
TLINP_T31 31 32 Z=90.00 L=94.43 K=7 A=0.0e+00 F=10.0
S1PA_D32 32 0 [MODEL=MIKE AREA=37.45] ! fb=214.20
TLINP_T32 32 33 Z=90.00 L=92.81 K=7 A=0.0e+00 F=10.0
S1PA_D33 33 0 [MODEL=MIKE AREA=36.81] ! fb=217.95
TLINP_T33 33 34 Z=90.00 L=91.21 K=7 A=0.0e+00 F=10.0
S1PA_D34 34 0 [MODEL=MIKE AREA=36.17] ! fb=221.77
TLINP_T34 34 35 Z=90.00 L=89.64 K=7 A=0.0e+00 F=10.0
S1PA_D35 35 0 [MODEL=MIKE AREA=35.55] ! fb=225.66
TLINP_T35 35 36 Z=90.00 L=88.09 K=7 A=0.0e+00 F=10.0
S1PA_D36 36 0 [MODEL=MIKE AREA=34.94] ! fb=229.61
TLINP_T36 36 37 Z=90.00 L=86.58 K=7 A=0.0e+00 F=10.0
S1PA_D37 37 0 [MODEL=MIKE AREA=34.33] ! fb=233.64
TLINP_T37 37 38 Z=90.00 L=85.09 K=7 A=0.0e+00 F=10.0
S1PA_D38 38 0 [MODEL=MIKE AREA=33.74] ! fb=237.73
TLINP_T38 38 39 Z=90.00 L=83.62 K=7 A=0.0e+00 F=10.0
S1PA_D39 39 0 [MODEL=MIKE AREA=33.16] ! fb=241.90
TLINP_T39 39 40 Z=90.00 L=82.18 K=7 A=0.0e+00 F=10.0
S1PA_D40 40 0 [MODEL=MIKE AREA=32.59] ! fb=246.14
TLINP_T40 40 41 Z=90.00 L=80.76 K=7 A=0.0e+00 F=10.0
S1PA_D41 41 0 [MODEL=MIKE AREA=32.03] ! fb=250.45
TLINP_T41 41 42 Z=90.00 L=79.37 K=7 A=0.0e+00 F=10.0
S1PA_D42 42 0 [MODEL=MIKE AREA=31.48] ! fb=254.84
TLINP_T42 42 43 Z=90.00 L=78.01 K=7 A=0.0e+00 F=10.0
S1PA_D43 43 0 [MODEL=MIKE AREA=30.94] ! fb=259.30
TLINP_T43 43 44 Z=90.00 L=76.66 K=7 A=0.0e+00 F=10.0
S1PA_D44 44 0 [MODEL=MIKE AREA=30.40] ! fb=263.85
TLINP_T44 44 45 Z=90.00 L=75.34 K=7 A=0.0e+00 F=10.0
S1PA_D45 45 0 [MODEL=MIKE AREA=29.88] ! fb=268.47
```

```
TLINP_T45 45 46 Z=90.00 L=74.04 K=7 A=0.0e+00 F=10.0
S1PA_D46 46 0 [MODEL=MIKE AREA=29.36] ! fb=273.18
TLINP_T46 46 47 Z=90.00 L=72.77 K=7 A=0.0e+00 F=10.0
S1PA_D47 47 0 [MODEL=MIKE AREA=28.86] ! fb=277.97
TLINP_T47 47 48 Z=90.00 L=71.52 K=7 A=0.0e+00 F=10.0
S1PA_D48 48 0 [MODEL=MIKE AREA=28.36] ! fb=282.84
TLINP_T48 48 49 Z=90.00 L=70.28 K=7 A=0.0e+00 F=10.0
S1PA_D49 49 0 [MODEL=MIKE AREA=27.87] ! fb=287.79
TLINP_T49 49 50 Z=90.00 L=69.07 K=7 A=0.0e+00 F=10.0
S1PA_D50 50 0 [MODEL=MIKE AREA=27.39] ! fb=292.84
TLINP_T50 50 51 Z=90.00 L=67.88 K=7 A=0.0e+00 F=10.0
S1PA_D51 51 0 [MODEL=MIKE AREA=26.92] ! fb=297.97
TLINP_T51 51 52 Z=90.00 L=66.71 K=7 A=0.0e+00 F=10.0
S1PA_D52 52 0 [MODEL=MIKE AREA=26.46] ! fb=303.19
TLINP_T52 52 53 Z=90.00 L=65.57 K=7 A=0.0e+00 F=10.0
S1PA_D53 53 0 [MODEL=MIKE AREA=26.00] ! fb=308.51
TLINP_T53 53 54 Z=90.00 L=64.44 K=7 A=0.0e+00 F=10.0
S1PA_D54 54 0 [MODEL=MIKE AREA=25.55] ! fb=313.91
TLINP_T54 54 55 Z=90.00 L=63.33 K=7 A=0.0e+00 F=10.0
S1PA_D55 55 0 [MODEL=MIKE AREA=25.11] ! fb=319.41
TLINP_T55 55 56 Z=90.00 L=62.24 K=7 A=0.0e+00 F=10.0
S1PA_D56 56 0 [MODEL=MIKE AREA=24.68] ! fb=325.01
TLINP_T56 56 57 Z=90.00 L=61.16 K=7 A=0.0e+00 F=10.0
S1PA_D57 57 0 [MODEL=MIKE AREA=24.26] ! fb=330.71
TLINP_T57 57 58 Z=90.00 L=60.11 K=7 A=0.0e+00 F=10.0
S1PA_D58 58 0 [MODEL=MIKE AREA=23.84] ! fb=336.50
TLINP_T58 58 59 Z=90.00 L=59.08 K=7 A=0.0e+00 F=10.0
S1PA_D59 59 0 [MODEL=MIKE AREA=23.43] ! fb=342.40
TLINP_T59 59 60 Z=90.00 L=58.06 K=7 A=0.0e+00 F=10.0
S1PA_D60 60 0 [MODEL=MIKE AREA=23.02] ! fb=348.40
TLINP_T60 60 61 Z=90.00 L=57.06 K=7 A=0.0e+00 F=10.0
S1PA_D61 61 0 [MODEL=MIKE AREA=22.63] ! fb=354.51
TLINP_T61 61 62 Z=90.00 L=56.07 K=7 A=0.0e+00 F=10.0
S1PA_D62 62 0 [MODEL=MIKE AREA=22.24] ! fb=360.72
TLINP_T62 62 63 Z=90.00 L=55.11 K=7 A=0.0e+00 F=10.0
S1PA_D63 63 0 [MODEL=MIKE AREA=21.85] ! fb=367.04
TLINP_T63 63 64 Z=90.00 L=54.16 K=7 A=0.0e+00 F=10.0
S1PA_D64 64 0 [MODEL=MIKE AREA=21.48] ! fb=373.47
```

```
TLINP_T64 64 65 Z=90.00 L=53.23 K=7 A=0.0e+00 F=10.0
S1PA_D65 65 0 [MODEL=MIKE AREA=21.11] ! fb=380.02
TLINP_T65 65 66 Z=90.00 L=52.31 K=7 A=0.0e+00 F=10.0
S1PA_D66 66 0 [MODEL=MIKE AREA=20.75] ! fb=386.68
TLINP_T66 66 67 Z=90.00 L=51.41 K=7 A=0.0e+00 F=10.0
S1PA_D67 67 0 [MODEL=MIKE AREA=20.39] ! fb=393.46
TLINP_T67 67 68 Z=90.00 L=50.52 K=7 A=0.0e+00 F=10.0
S1PA_D68 68 0 [MODEL=MIKE AREA=20.04] ! fb=400.35
TLINP_T68 68 69 Z=90.00 L=49.65 K=7 A=0.0e+00 F=10.0
S1PA_D69 69 0 [MODEL=MIKE AREA=19.69] ! fb=407.37
TLINP_T69 69 70 Z=90.00 L=48.80 K=7 A=0.0e+00 F=10.0
S1PA_D70 70 0 [MODEL=MIKE AREA=19.35] ! fb=414.51
TLINP_T70 70 71 Z=90.00 L=47.96 K=7 A=0.0e+00 F=10.0
S1PA_D71 71 0 [MODEL=MIKE AREA=19.02] ! fb=421.77
TLINP_T71 71 72 Z=90.00 L=47.13 K=7 A=0.0e+00 F=10.0
S1PA_D72 72 0 [MODEL=MIKE AREA=18.69] ! fb=429.16
TLINP_T72 72 73 Z=90.00 L=46.32 K=7 A=0.0e+00 F=10.0
S1PA_D73 73 0 [MODEL=MIKE AREA=18.37] ! fb=436.68
TLINP_T73 73 74 Z=90.00 L=45.52 K=7 A=0.0e+00 F=10.0
S1PA_D74 74 0 [MODEL=MIKE AREA=18.05] ! fb=444.34
TLINP_T74 74 75 Z=90.00 L=44.74 K=7 A=0.0e+00 F=10.0
S1PA_D75 75 0 [MODEL=MIKE AREA=17.74] ! fb=452.13
TLINP_T75 75 76 Z=90.00 L=43.97 K=7 A=0.0e+00 F=10.0
S1PA_D76 76 0 [MODEL=MIKE AREA=17.44] ! fb=460.05
TLINP_T76 76 77 Z=90.00 L=43.21 K=7 A=0.0e+00 F=10.0
S1PA_D77 77 0 [MODEL=MIKE AREA=17.14] ! fb=468.11
TLINP_T77 77 78 Z=90.00 L=42.47 K=7 A=0.0e+00 F=10.0
S1PA_D78 78 0 [MODEL=MIKE AREA=16.84] ! fb=476.32
TLINP_T78 78 79 Z=90.00 L=41.73 K=7 A=0.0e+00 F=10.0
S1PA_D79 79 0 [MODEL=MIKE AREA=16.55] ! fb=484.66
TLINP_T79 79 80 Z=90.00 L=41.02 K=7 A=0.0e+00 F=10.0
S1PA_D80 80 0 [MODEL=MIKE AREA=16.27] ! fb=493.16
TLINP_T80 80 81 Z=90.00 L=40.31 K=7 A=0.0e+00 F=10.0
S1PA_D81 81 0 [MODEL=MIKE AREA=15.99] ! fb=501.80
TLINP_T81 81 82 Z=90.00 L=39.62 K=7 A=0.0e+00 F=10.0
S1PA_D82 82 0 [MODEL=MIKE AREA=15.71] ! fb=510.59
TLINP_T82 82 83 Z=90.00 L=38.93 K=7 A=0.0e+00 F=10.0
S1PA_D83 83 0 [MODEL=MIKE AREA=15.44] ! fb=519.54
```

```
TLINP_T83  83  84  Z=90.00 L=38.26 K=7 A=0.0e+00 F=10.0
S1PA_D84  84  0  [MODEL=MIKE AREA=15.17] ! fb=528.65
TLINP_T84  84  85  Z=90.00 L=37.60 K=7 A=0.0e+00 F=10.0
S1PA_D85  85  0  [MODEL=MIKE AREA=14.91] ! fb=537.91
TLINP_T85  85  86  Z=90.00 L=36.96 K=7 A=0.0e+00 F=10.0
S1PA_D86  86  0  [MODEL=MIKE AREA=14.66] ! fb=547.34
TLINP_T86  86  87  Z=90.00 L=36.32 K=7 A=0.0e+00 F=10.0
S1PA_D87  87  0  [MODEL=MIKE AREA=14.40] ! fb=556.93
TLINP_T87  87  88  Z=90.00 L=35.69 K=7 A=0.0e+00 F=10.0
S1PA_D88  88  0  [MODEL=MIKE AREA=14.16] ! fb=566.69
TLINP_T88  88  89  Z=90.00 L=35.08 K=7 A=0.0e+00 F=10.0
S1PA_D89  89  0  [MODEL=MIKE AREA=13.91] ! fb=576.62
TLINP_T89  89  90  Z=90.00 L=34.47 K=7 A=0.0e+00 F=10.0
S1PA_D90  90  0  [MODEL=MIKE AREA=13.67] ! fb=586.73
TLINP_T90  90  91  Z=90.00 L=33.88 K=7 A=0.0e+00 F=10.0
S1PA_D91  91  0  [MODEL=MIKE AREA=13.44] ! fb=597.01
TLINP_T91  91  92  Z=90.00 L=33.30 K=7 A=0.0e+00 F=10.0
S1PA_D92  92  0  [MODEL=MIKE AREA=13.20] ! fb=607.47
TLINP_T92  92  93  Z=90.00 L=32.72 K=7 A=0.0e+00 F=10.0
S1PA_D93  93  0  [MODEL=MIKE AREA=12.98] ! fb=618.12
TLINP_T93  93  94  Z=90.00 L=32.16 K=7 A=0.0e+00 F=10.0
S1PA_D94  94  0  [MODEL=MIKE AREA=12.75] ! fb=628.95
TLINP_T94  94  95  Z=90.00 L=31.61 K=7 A=0.0e+00 F=10.0
S1PA_D95  95  0  [MODEL=MIKE AREA=12.53] ! fb=639.98
TLINP_T95  95  96  Z=90.00 L=31.06 K=7 A=0.0e+00 F=10.0
S1PA_D96  96  0  [MODEL=MIKE AREA=12.32] ! fb=651.19
TLINP_T96  96  97  Z=90.00 L=30.53 K=7 A=0.0e+00 F=10.0
S1PA_D97  97  0  [MODEL=MIKE AREA=12.11] ! fb=662.60
TLINP_T97  97  98  Z=90.00 L=30.00 K=7 A=0.0e+00 F=10.0
S1PA_D98  98  0  [MODEL=MIKE AREA=11.90] ! fb=674.22
TLINP_T98  98  99  Z=90.00 L=29.48 K=7 A=0.0e+00 F=10.0
S1PA_D99  99  0  [MODEL=MIKE AREA=11.69] ! fb=686.03
TLINP_T99  99  100 Z=90.00 L=28.98 K=7 A=0.0e+00 F=10.0
S1PA_D100 100  0  [MODEL=MIKE AREA=11.49] ! fb=698.06
TLINP_T100 100  101 Z=90.00 L=28.48 K=7 A=0.0e+00 F=10.0
S1PA_D101 101  0  [MODEL=MIKE AREA=11.29] ! fb=710.29
TLINP_T101 101  102 Z=90.00 L=27.99 K=7 A=0.0e+00 F=10.0
S1PA_D102 102  0  [MODEL=MIKE AREA=11.10] ! fb=722.74
```

```

TLINP_T102  102  103  Z=90.00 L=27.51 K=7 A=0.0e+00 F=10.0
S1PA_D103   103  0    [MODEL=MIKE AREA=10.91] ! fb=735.40
TLINP_T103  103  104  Z=90.00 L=27.03 K=7 A=0.0e+00 F=10.0
S1PA_D104   104  0    [MODEL=MIKE AREA=10.72] ! fb=748.29
TLINP_T104  104  105  Z=90.00 L=26.57 K=7 A=0.0e+00 F=10.0
S1PA_D105   105  0    [MODEL=MIKE AREA=10.54] ! fb=761.41
TLINP_T105  105  106  Z=90.00 L=26.11 K=7 A=0.0e+00 F=10.0
S1PA_D106   106  0    [MODEL=MIKE AREA=10.35] ! fb=774.75
TLINP_T106  106  107  Z=90.00 L=25.66 K=7 A=0.0e+00 F=10.0
S1PA_D107   107  0    [MODEL=MIKE AREA=10.18] ! fb=788.33
TLINP_T107  107  108  Z=90.00 L=25.22 K=7 A=0.0e+00 F=10.0
S1PA_D108   108  0    [MODEL=MIKE AREA=10.00] ! fb=802.14
TLINP_T108  108  109  Z=90.00 L=12.50 K=7 A=0.0e+00 F=10.0
DEF2P  201  109  NLTL
! Total number of squares is 1935.93
MODEL
  MIKE D RS=81.222000 CJO=1.080399E-15 VJ=0.643663 &
      M=0.451841 IS=1.000000E-12 N=1.500000
SOURCE
  NLTL RES_RIN  201 202 R=50
  NLTL IVS_VIN  202 0  TRAN=SIN(-6 6 10E9 0 0 90)
  NLTL RES_RL   109 0  R=50
CONTROL
  NLTL TRAN 10E-12 2E-9 1.8e-9
SPICEOUT
  NLTL TRAN V(109) v(202) v(201) v(1)

```

A.2.2 Academy Layout File

```

! Academy file for NLTL with 125.00 GHz initial Bragg frequency,
! 800.00 GHz final Bragg frequency and 0.982776 tapering rule,
! and 51.00 ps total compression.

```

```

DIM
  LNG UM
CKT

```

```
nltla_u1 1 2 z=90 W=8 adi=64.17 lli=160.41 lam=4 ! fb=125.00
nltla_u2 2 3 z=90 W=7 adi=63.07 lli=157.65 lam=4 ! fb=127.19
nltla_u3 3 4 z=90 W=7 adi=61.98 lli=154.93 lam=4 ! fb=129.42
nltla_u4 4 5 z=90 W=7 adi=60.91 lli=152.27 lam=4 ! fb=131.69
nltlb_u5 5 6 z=90 W=7 adi=59.87 lli=149.64 lam=4 ! fb=134.00
nltlb_u6 6 7 z=90 W=7 adi=58.83 lli=147.07 lam=4 ! fb=136.34
nltlb_u7 7 8 z=90 W=7 adi=57.82 lli=144.53 lam=4 ! fb=138.73
nltlb_u8 8 9 z=90 W=7 adi=56.82 lli=142.04 lam=4 ! fb=141.16
nltlb_u9 9 10 z=90 W=7 adi=55.85 lli=139.60 lam=4 ! fb=143.64
nltlb_u10 10 11 z=90 W=6 adi=54.88 lli=137.19 lam=4 ! fb=146.16
nltlb_u11 11 12 z=90 W=6 adi=53.94 lli=134.83 lam=4 ! fb=148.72
nltlb_u12 12 13 z=90 W=6 adi=53.01 lli=132.51 lam=4 ! fb=151.32
nltlb_u13 13 14 z=90 W=6 adi=52.10 lli=130.23 lam=4 ! fb=153.98
nltlb_u14 14 15 z=90 W=6 adi=51.20 lli=127.98 lam=4 ! fb=156.67
nltlb_u15 15 16 z=90 W=6 adi=50.32 lli=125.78 lam=4 ! fb=159.42
nltlb_u16 16 17 z=90 W=6 adi=49.45 lli=123.61 lam=4 ! fb=162.21
nltlb_u17 17 18 z=90 W=6 adi=48.60 lli=121.48 lam=4 ! fb=165.06
nltlb_u18 18 19 z=90 W=6 adi=47.76 lli=119.39 lam=4 ! fb=167.95
nltlb_u19 19 20 z=90 W=5 adi=46.94 lli=117.33 lam=4 ! fb=170.89
nltlb_u20 20 21 z=90 W=5 adi=46.13 lli=115.31 lam=4 ! fb=173.89
nltlb_u21 21 22 z=90 W=5 adi=45.34 lli=113.33 lam=4 ! fb=176.94
nltlb_u22 22 23 z=90 W=5 adi=44.56 lli=111.38 lam=4 ! fb=180.04
nltlb_u23 23 24 z=90 W=5 adi=43.79 lli=109.46 lam=4 ! fb=183.19
nltlb_u24 24 25 z=90 W=5 adi=43.03 lli=107.57 lam=4 ! fb=186.40
nltlb_u25 25 26 z=90 W=5 adi=42.29 lli=105.72 lam=4 ! fb=189.67
nltlb_u26 26 27 z=90 W=5 adi=41.56 lli=103.90 lam=4 ! fb=192.99
nltlb_u27 27 28 z=90 W=5 adi=40.85 lli=102.11 lam=4 ! fb=196.38
nltlb_u28 28 29 z=90 W=5 adi=40.15 lli=100.35 lam=4 ! fb=199.82
nltlb_u29 29 30 z=90 W=4 adi=39.45 lli=98.62 lam=4 ! fb=203.32
nltlb_u30 30 31 z=90 W=4 adi=38.77 lli=96.92 lam=4 ! fb=206.88
nltlb_u31 31 32 z=90 W=4 adi=38.11 lli=95.25 lam=4 ! fb=210.51
nltlb_u32 32 33 z=90 W=4 adi=37.45 lli=93.61 lam=4 ! fb=214.20
nltlb_u33 33 34 z=90 W=4 adi=36.81 lli=92.00 lam=4 ! fb=217.95
nltlb_u34 34 35 z=90 W=4 adi=36.17 lli=90.42 lam=4 ! fb=221.77
nltlb_u35 35 36 z=90 W=4 adi=35.55 lli=88.86 lam=4 ! fb=225.66
nltlb_u36 36 37 z=90 W=4 adi=34.94 lli=87.33 lam=4 ! fb=229.61
nltlb_u37 37 38 z=90 W=4 adi=34.33 lli=85.82 lam=4 ! fb=233.64
nltlb_u38 38 39 z=90 W=4 adi=33.74 lli=84.35 lam=4 ! fb=237.73
```

| | | | | | | | | | |
|-----------|----|----|------|-----|-----------|-----------|-------|---|-----------|
| nltlb_u39 | 39 | 40 | z=90 | W=4 | adi=33.16 | lli=82.89 | lam=4 | ! | fb=241.90 |
| nltlb_u40 | 40 | 41 | z=90 | W=4 | adi=32.59 | lli=81.47 | lam=4 | ! | fb=246.14 |
| nltlb_u41 | 41 | 42 | z=90 | W=4 | adi=32.03 | lli=80.06 | lam=4 | ! | fb=250.45 |
| nltlb_u42 | 42 | 43 | z=90 | W=3 | adi=31.48 | lli=78.68 | lam=4 | ! | fb=254.84 |
| nltlb_u43 | 43 | 44 | z=90 | W=3 | adi=30.94 | lli=77.33 | lam=4 | ! | fb=259.30 |
| nltlb_u44 | 44 | 45 | z=90 | W=3 | adi=30.40 | lli=76.00 | lam=4 | ! | fb=263.85 |
| nltlb_u45 | 45 | 46 | z=90 | W=3 | adi=29.88 | lli=74.69 | lam=3 | ! | fb=268.47 |
| nltlb_u46 | 46 | 47 | z=90 | W=3 | adi=29.36 | lli=73.40 | lam=3 | ! | fb=273.18 |
| nltlb_u47 | 47 | 48 | z=90 | W=3 | adi=28.86 | lli=72.14 | lam=3 | ! | fb=277.97 |
| nltlb_u48 | 48 | 49 | z=90 | W=3 | adi=28.36 | lli=70.89 | lam=3 | ! | fb=282.84 |
| nltlb_u49 | 49 | 50 | z=90 | W=3 | adi=27.87 | lli=69.67 | lam=3 | ! | fb=287.79 |
| nltlb_u50 | 50 | 51 | z=90 | W=3 | adi=27.39 | lli=68.47 | lam=3 | ! | fb=292.84 |
| nltlb_u51 | 51 | 52 | z=90 | W=3 | adi=26.92 | lli=67.29 | lam=3 | ! | fb=297.97 |
| nltlb_u52 | 52 | 53 | z=90 | W=3 | adi=26.46 | lli=66.14 | lam=3 | ! | fb=303.19 |
| nltlb_u53 | 53 | 54 | z=90 | W=3 | adi=26.00 | lli=65.00 | lam=3 | ! | fb=308.51 |
| nltlb_u54 | 54 | 55 | z=90 | W=3 | adi=25.55 | lli=63.88 | lam=3 | ! | fb=313.91 |
| nltlb_u55 | 55 | 56 | z=90 | W=3 | adi=25.11 | lli=62.78 | lam=3 | ! | fb=319.41 |
| nltlb_u56 | 56 | 57 | z=90 | W=3 | adi=24.68 | lli=61.70 | lam=3 | ! | fb=325.01 |
| nltlb_u57 | 57 | 58 | z=90 | W=3 | adi=24.26 | lli=60.63 | lam=3 | ! | fb=330.71 |
| nltlb_u58 | 58 | 59 | z=90 | W=3 | adi=23.84 | lli=59.59 | lam=3 | ! | fb=336.50 |
| nltlb_u59 | 59 | 60 | z=90 | W=3 | adi=23.43 | lli=58.56 | lam=3 | ! | fb=342.40 |
| nltlb_u60 | 60 | 61 | z=90 | W=3 | adi=23.02 | lli=57.55 | lam=3 | ! | fb=348.40 |
| nltlb_u61 | 61 | 62 | z=90 | W=3 | adi=22.63 | lli=56.56 | lam=3 | ! | fb=354.51 |
| nltlb_u62 | 62 | 63 | z=90 | W=3 | adi=22.24 | lli=55.59 | lam=3 | ! | fb=360.72 |
| nltlb_u63 | 63 | 64 | z=90 | W=3 | adi=21.85 | lli=54.63 | lam=3 | ! | fb=367.04 |
| nltlb_u64 | 64 | 65 | z=90 | W=3 | adi=21.48 | lli=53.69 | lam=3 | ! | fb=373.47 |
| nltlb_u65 | 65 | 66 | z=90 | W=3 | adi=21.11 | lli=52.76 | lam=3 | ! | fb=380.02 |
| nltlb_u66 | 66 | 67 | z=90 | W=3 | adi=20.75 | lli=51.86 | lam=3 | ! | fb=386.68 |
| nltlb_u67 | 67 | 68 | z=90 | W=3 | adi=20.39 | lli=50.96 | lam=3 | ! | fb=393.46 |
| nltlb_u68 | 68 | 69 | z=90 | W=3 | adi=20.04 | lli=50.09 | lam=3 | ! | fb=400.35 |
| nltlb_u69 | 69 | 70 | z=90 | W=3 | adi=19.69 | lli=49.22 | lam=3 | ! | fb=407.37 |
| nltlb_u70 | 70 | 71 | z=90 | W=3 | adi=19.35 | lli=48.37 | lam=3 | ! | fb=414.51 |
| nltlb_u71 | 71 | 72 | z=90 | W=3 | adi=19.02 | lli=47.54 | lam=3 | ! | fb=421.77 |
| nltlb_u72 | 72 | 73 | z=90 | W=3 | adi=18.69 | lli=46.72 | lam=3 | ! | fb=429.16 |
| nltlb_u73 | 73 | 74 | z=90 | W=3 | adi=18.37 | lli=45.92 | lam=3 | ! | fb=436.68 |
| nltlb_u74 | 74 | 75 | z=90 | W=3 | adi=18.05 | lli=45.13 | lam=3 | ! | fb=444.34 |
| nltlb_u75 | 75 | 76 | z=90 | W=3 | adi=17.74 | lli=44.35 | lam=3 | ! | fb=452.13 |
| nltlb_u76 | 76 | 77 | z=90 | W=3 | adi=17.44 | lli=43.59 | lam=3 | ! | fb=460.05 |


```
nltlb_u77 77 78 z=90 W=3 adi=17.14 lli=42.84 lam=3 ! fb=468.11
nltlb_u78 78 79 z=90 W=3 adi=16.84 lli=42.10 lam=3 ! fb=476.32
nltlb_u79 79 80 z=90 W=3 adi=16.55 lli=41.37 lam=3 ! fb=484.66
nltlb_u80 80 81 z=90 W=3 adi=16.27 lli=40.66 lam=3 ! fb=493.16
nltlb_u81 81 82 z=90 W=3 adi=15.99 lli=39.96 lam=3 ! fb=501.80
nltlb_u82 82 83 z=90 W=3 adi=15.71 lli=39.27 lam=3 ! fb=510.59
nltlb_u83 83 84 z=90 W=3 adi=15.44 lli=38.59 lam=3 ! fb=519.54
nltlb_u84 84 85 z=90 W=3 adi=15.17 lli=37.93 lam=3 ! fb=528.65
nltlb_u85 85 86 z=90 W=3 adi=14.91 lli=37.28 lam=3 ! fb=537.91
nltlb_u86 86 87 z=90 W=3 adi=14.66 lli=36.63 lam=3 ! fb=547.34
nltlb_u87 87 88 z=90 W=3 adi=14.40 lli=36.00 lam=3 ! fb=556.93
nltlb_u88 88 89 z=90 W=3 adi=14.16 lli=35.38 lam=3 ! fb=566.69
nltlb_u89 89 90 z=90 W=3 adi=13.91 lli=34.77 lam=3 ! fb=576.62
nltlb_u90 90 91 z=90 W=3 adi=13.67 lli=34.18 lam=3 ! fb=586.73
nltlb_u91 91 92 z=90 W=3 adi=13.44 lli=33.59 lam=3 ! fb=597.01
nltlb_u92 92 93 z=90 W=3 adi=13.20 lli=33.01 lam=3 ! fb=607.47
nltlb_u93 93 94 z=90 W=3 adi=12.98 lli=32.44 lam=3 ! fb=618.12
nltlb_u94 94 95 z=90 W=3 adi=12.75 lli=31.88 lam=3 ! fb=628.95
nltlb_u95 95 96 z=90 W=3 adi=12.53 lli=31.33 lam=3 ! fb=639.98
nltlb_u96 96 97 z=90 W=3 adi=12.32 lli=30.79 lam=3 ! fb=651.19
nltlb_u97 97 98 z=90 W=3 adi=12.11 lli=30.26 lam=3 ! fb=662.60
nltlb_u98 98 99 z=90 W=3 adi=11.90 lli=29.74 lam=3 ! fb=674.22
nltlb_u99 99 100 z=90 W=3 adi=11.69 lli=29.23 lam=3 ! fb=686.03
nltlb_u100 100 101 z=90 W=3 adi=11.49 lli=28.72 lam=3 ! fb=698.06
nltlb_u101 101 102 z=90 W=3 adi=11.29 lli=28.23 lam=3 ! fb=710.29
nltlb_u102 102 103 z=90 W=3 adi=11.10 lli=27.74 lam=3 ! fb=722.74
nltlb_u103 103 104 z=90 W=3 adi=10.91 lli=27.27 lam=3 ! fb=735.40
nltlb_u104 104 105 z=90 W=3 adi=10.72 lli=26.80 lam=3 ! fb=748.29
nltlb_u105 105 106 z=90 W=3 adi=10.54 lli=26.34 lam=3 ! fb=761.41
nltlb_u106 106 107 z=90 W=3 adi=10.35 lli=25.88 lam=3 ! fb=774.75
nltlb_u107 107 108 z=90 W=3 adi=10.18 lli=25.44 lam=3 ! fb=788.33
nltlb_u108 108 109 z=90 W=3 adi=10.00 lli=25.00 lam=3 ! fb=802.14
DEF2P 1 109 NLTL108
! Total number of squares is 1935.93
```

A.3 Macro Used in Academy

```

! Academy macro file
iboc = 3 ! point type for begin open contour
ibccf= 4 ! point type for begin closed contour, filled
ibcce= 5 ! point type for begin closed contour, empty
ibcir= 6 ! point type for begin circle (give center)
ibhol= 7 ! point type for begin hole (give center x,y)
icon = 8 ! point type for connecting point
iarc = 9 ! point type for begin arc (give radius,
sweep angle in degrees)
icen = 10 ! point type for end arc (give center x,y)
ieoc = 11 ! point type for end open contour
iecc = 12 ! point type for end closed contour
iecir= 13 ! point type for end circle (give radius, 2nd
value ignored)
iiso = 14 ! point type for isolated point
! text font codes
istick=3 ! stick font
iblock=4 ! block font
! Below are the original layers:
schint    = 0      ! schottky contacts and interconnect
ohmic     = 1      ! ohmic metal
isolation = 2      ! ion implant isolation
nitride   = 3      ! silicon nitride mask
post      = 4      ! air bridge post & capacitor contact
ab        = 5      ! air bridge
hr        = 6      ! high-res mask, 1 um features
! angunit - predefined to convert from circuit angle
unit to radians
!-----
!! New Arbitrary Impedance NLT L suited for 50 ohm
large-signal impedance lines
!
defelem "NLT LA",2,"z","w","adi","lli","lam"
real z,x,y,w,adi,lli,ctr,dpth,lambda,b,g,s,lam,wab
lli=0.5*int(0.5+2*lli)

```

```

w=int(0.5+w)
lambda=int(0.5+lam)
! Check it out!
if w < lambda then
    w=lambda
end if
! Find center of the line section:
ctr=0.5*int(0.5+lli)
! Find depth of slot:
dpth=0.5*int(0.5+adi/lambda)+2*lambda
! Find gap width
x=sqr(1-((0.5*exp(z/11.33893419)-1)/]
(0.5*exp(z/11.33893419)+1))^4)
! X=w/(w+2b)
y=(1-x)/(2*x)
b=0.5*int(0.5+2*y*w)
! Find ground width
g=10*int(0.5+0.5*b)
! Find diode tail for 14 degree slope
! s=tan(angle)*(b-2*lambda)
s=0.5*int(0.5+0.5*(b-2*lambda))
! Draw the CPW with slots
level schint
! Center conductor
point ibccf,0,w/2
node n1,0,0
point icon,0,w/-2
point icon,lli,w/-2
node n2,lli,0
point iecc,lli,w/2
! Upper ground
point ibccf,0,b+w/2
point icon,0,g
point icon,lli,g
point icon,lli,b+w/2
point icon,ctr+2.5*lambda,b+w/2
point icon,ctr+2.5*lambda,b+w/2+dpth
point icon,ctr-2.5*lambda,b+w/2+dpth

```

```

point iecc,ctr-2.5*lambda,b+w/2
! Lower ground
point ibccf,0,-1*(b+w/2)
point icon,0,-1*g
point icon,lli,-1*g
point icon,lli,-1*(b+w/2)
point icon,ctr+2.5*lambda,-1*(b+w/2)
point icon,ctr+2.5*lambda,-1*(b+w/2+dpth)
point icon,ctr-2.5*lambda,-1*(b+w/2+dpth)
point iecc,ctr-2.5*lambda,-1*(b+w/2)
! Upper diode
point ibccf,ctr-lambda/2-s,w/2
point icon,ctr-lambda/2,b+w/2-2*lambda
point icon,ctr-lambda/2,b+w/2+dpth-2*lambda
point icon,ctr+lambda/2,b+w/2+dpth-2*lambda
point icon,ctr+lambda/2,b+w/2-2*lambda
point iecc,ctr+lambda/2+s,w/2
! Lower diode
point ibccf,ctr-lambda/2-s,w/-2
point icon,ctr-lambda/2,-1*(b+w/2-2*lambda)
point icon,ctr-lambda/2,-1*(b+w/2+dpth-2*lambda)
point icon,ctr+lambda/2,-1*(b+w/2+dpth-2*lambda)
point icon,ctr+lambda/2,-1*(b+w/2-2*lambda)
point iecc,ctr+lambda/2+s,w/-2
! Now, do the Ohmics
level ohmic
! Upper ohmic
point ibccf,ctr-1.5*lambda-10,b+w/2-lambda
point icon,ctr-1.5*lambda-10,b+w/2+dpth+10-lambda
point icon,ctr+1.5*lambda+10,b+w/2+dpth+10-lambda
point icon,ctr+1.5*lambda+10,b+w/2-lambda
point icon,ctr+1.5*lambda,b+w/2-lambda
point icon,ctr+1.5*lambda,b+w/2+dpth-lambda
point icon,ctr-1.5*lambda,b+w/2+dpth-lambda
point iecc,ctr-1.5*lambda,b+w/2-lambda
! Lower diode
point ibccf,ctr-1.5*lambda-10,-1*(b+w/2-lambda)
point icon,ctr-1.5*lambda-10,-1*(b+w/2+dpth+10-lambda)

```

```

point icon,ctr+1.5*lambda+10,-1*(b+w/2+dpth+10-lambda)
point icon,ctr+1.5*lambda+10,-1*(b+w/2-lambda)
point icon,ctr+1.5*lambda,-1*(b+w/2-lambda)
point icon,ctr+1.5*lambda,-1*(b+w/2+dpth-lambda)
point icon,ctr-1.5*lambda,-1*(b+w/2+dpth-lambda)
point iecc,ctr-1.5*lambda,-1*(b+w/2-lambda)
! Finally, the ion implant
level isolation
! Upper
point ibccf,ctr-2.5*lambda-10,b+w/2
point icon,ctr-2.5*lambda-10,b+w/2+dpth+10
point icon,ctr+2.5*lambda+10,b+w/2+dpth+10
point iecc,ctr+2.5*lambda+10,b+w/2
! Lower
point ibccf,ctr-2.5*lambda-10,-1*(b+w/2)
point icon,ctr-2.5*lambda-10,-1*(b+w/2+dpth+10)
point icon,ctr+2.5*lambda+10,-1*(b+w/2+dpth+10)
point iecc,ctr+2.5*lambda+10,-1*(b+w/2)
! Now, add some air bridges:
level post
if (2*b+w) >= 200 then
    wab=30
else
    wab=20
end if
point ibccf,0,b+w/2+5
point icon,0,b+w/2+5+wab
point icon,wab/2,b+w/2+5+wab
point iecc,wab/2,b+w/2+5

point ibccf,0,-1*(b+w/2+5)
point icon,0,-1*(b+w/2+5+wab)
point icon,wab/2,-1*(b+w/2+5+wab)
point iecc,wab/2,-1*(b+w/2+5)

point ibccf,lli-wab/2,-1*(b+w/2+5)
point icon,lli-wab/2,-1*(b+w/2+5+wab)
point icon,lli,-1*(b+w/2+5+wab)

```

```

point iecc,lli,-1*(b+w/2+5)

point ibccf,lli-wab/2,b+w/2+5
point icon,lli-wab/2,b+w/2+5+wab
point icon,lli,b+w/2+5+wab
point iecc,lli,b+w/2+5

level ab
point ibccf,0,b+w/2+5+wab+lambda
point icon,wab/2+lambda,b+w/2+5+wab+lambda
point icon,wab/2+lambda,-1*(b+w/2+5+wab+lambda)
point iecc,0,-1*(b+w/2+5+wab+lambda)

point ibccf,lli-wab/2-lambda,b+w/2+5+wab+lambda
point icon,lli,b+w/2+5+wab+lambda
point icon,lli,-1*(b+w/2+5+wab+lambda)
point iecc,lli-wab/2-lambda,-1*(b+w/2+5+wab+lambda)

end define
!-----
! Another new NLTL suited for 50 ohm
large-signal impedance lines
!
defelem "NLTLB",2,"z","w","adi","lli","lam"
real z,x,y,w,adi,lli,lambda,b,g,ldi,left,
right,delta,lam,lohms
lli=0.5*int(0.5+2*lli)
w=int(0.5+w)
lambda=int(0.5+lams)
! Check it out
if w < lambda then
    w=lambda
end if
! Find gap
x=sqr(1-((0.5*exp(z/11.33893419)-1)/
(0.5*exp(z/11.33893419)+1))^4)
! X=w/(w+2b)
y=(1-x)/(2*x)

```

```

b=0.5*int(0.5+2*y*w)
! Find ground width
g=10*int(0.5+0.5*b)
! Find diode length
ldi=0.5*int(0.5+2*(adi/lambda))
! Find left and right sides of diode
left=0.5*int(0.5+lli-ldi)
right=left+ldi
! Draw CPW with center conductor diodes
level schint
! Upper ground
point ibccf,0,w/2+b
point icon,0,g
point icon,lli,g
point iecc,lli,w/2+b
! Lower
point ibccf,0,-1*(w/2+b)
point icon,0,-1*g
point icon,lli,-1*g
point iecc,lli,-1*(w/2+b)
! Center
if w = lambda then
    point ibccf,0,w/2
    node n1,0,0
    point icon,0,w/-2
    point icon,lli,w/-2
    node n2,lli,0
    point iecc,lli,w/2
else
    delta=(w-lambda)/2
    point ibccf,0,w/2
    node n1,0,0
    point icon,0,w/-2
    point icon,left-1.5*lambda-delta,w/-2
    point icon,left-1.5*lambda,lambda/-2
    point icon,right+1.5*lambda,lambda/-2
    point icon,right+1.5*lambda+delta,w/-2
    point icon,lli,w/-2

```

```

node n2,lli,0
point icon,lli,w/2
point icon,right+1.5*lambda+delta,w/2
point icon,right+1.5*lambda,lambda/2
point icon,left-1.5*lambda,lambda/2
point iecc,left-1.5*lambda-delta,w/2
end if
! Ground extensions
point ibccf,left,2.5*lambda
point icon,left,w/2+b
point icon,right,w/2+b
point iecc,right,2.5*lambda
! lower
point ibccf,left,-2.5*lambda
point icon,left,-1*(w/2+b)
point icon,right,-1*(w/2+b)
point iecc,right,-2.5*lambda
! Now ohmics
level ohmic
lohm=b+w/2-0.5*lambda
if lohm < 10 then
    lohm=10
end if
! Upper
point ibccf,left-lambda,1.5*lambda
point icon,left-lambda,1.5*lambda+lohm
point icon,right+lambda,1.5*lambda+lohm
point iecc,right+lambda,1.5*lambda
! Lower
point ibccf,left-lambda,-1.5*lambda
point icon,left-lambda,-1.5*lambda-lohm
point icon,right+lambda,-1.5*lambda-lohm
point iecc,right+lambda,-1.5*lambda
! finally, the ion implant
level isolation
if ldi < 10 then
    point ibccf,0.5*int(lli-9.5),lohm+2.5*lambda
    point icon,0.5*int(lli-9.5),lohm+2.5*lambda+10

```



```

    point icon,0.5*int(lli+10.5),lohms+2.5*lambda+10
    point icon,0.5*int(lli+10.5),lohms+2.5*lambda
    point icon,right,lohms+2.5*lambda
    point icon,right,-1*(lohms+2.5*lambda)
    point icon,0.5*int(lli+10.5),-1*(lohms+2.5*lambda)
    point icon,0.5*int(lli+10.5),-1*(lohms+2.5*lambda+10)
    point icon,0.5*int(lli-9.5),-1*(lohms+2.5*lambda+10)
    point icon,0.5*int(lli-9.5),-1*(lohms+2.5*lambda)
    point icon,left,-1*(lohms+2.5*lambda)
    point iecc,left,lohms+2.5*lambda
else
    point ibccf,left,lohms+2.5*lambda
    point icon,right,lohms+2.5*lambda
    point icon,right,-1*(lohms+2.5*lambda)
    point iecc,left,-1*(lohms+2.5*lambda)
end if
!
end define
!-----
! Another new NLTL suited for 20 ohm
large-signal impedance lines
!
defelem "NLTL",2,"z","w","adi","lli","lam","wdi"
real z,x,y,w,adi,lli,lambda,wdi,b,g,ldi,lam,ctr,wab
lli=0.5*int(0.5+2*lli)
w=int(0.5+w)
lambda=int(0.5+lam)
wdi=int(0.5+wdi)
! Check it out
if w < lambda then
    w=lambda
end if
if wdi < lambda then
    wdi=lambda
end if
! Find gap
x=sqr(1-((0.5*exp(z/11.33893419)-1)/
(0.5*exp(z/11.33893419)+1))^4)

```

```

! X=w/(w+2b)
y=(1-x)/(2*x)
b=0.5*int(0.5+2*y*w)
! Find ground width
g=10*int(0.5+0.5*(2*b+w))
! Find each diode's length
ldi=0.5*int(0.5+adi/wdi)
! Find center of line
ctr=0.5*int(0.5+lli)
! Draw CPW with notched gground planes
level schint
! Upper ground
point ibccf,0,w/2+b
point icon,ctr-wdi/2-2*lambda,w/2+b
point icon,ctr-wdi/2-2*lambda,w/2+b+ldi+3*lambda
point icon,ctr+wdi/2+2*lambda,w/2+b+ldi+3*lambda
point icon,ctr+wdi/2+2*lambda,w/2+b
point icon,lli,w/2+b
point icon,lli,g
point iecc,0,g
!Center conductor
point ibccf,0,w/2
node n1,0,0
point icon,0,-1*(w/2)
point icon,ctr-wdi/2,-1*(w/2)
point icon,ctr-wdi/2,-1*(w/2+b+ldi+lambda)
point icon,ctr+wdi/2,-1*(w/2+b+ldi+lambda)
point icon,ctr+wdi/2,-1*(w/2)
point icon,lli,-1*(w/2)
node n2,lli,0
point icon,lli,w/2
point icon,ctr+wdi/2,w/2
point icon,ctr+wdi/2,w/2+b+ldi+lambda
point icon,ctr-wdi/2,w/2+b+ldi+lambda
point iecc,ctr-wdi/2,w/2
! Bottom ground
point ibccf,0,-1*(w/2+b)
point icon,ctr-wdi/2-2*lambda,-1*(w/2+b)

```

```

point icon,ctr-wdi/2-2*lambda,-1*(w/2+b+ldi+3*lambda)
point icon,ctr+wdi/2+2*lambda,-1*(w/2+b+ldi+3*lambda)
point icon,ctr+wdi/2+2*lambda,-1*(w/2+b)
point icon,lli,-1*(w/2+b)
point icon,lli,-1*g
point iecc,0,-1*g
! Draw Ohmic contacts
level ohmic
! Upper contact
point ibccf,ctr-wdi/2-3*lambda,w/2+b-lambda
point icon,ctr-wdi/2-3*lambda,w/2+b+ldi+4*lambda
point icon,ctr+wdi/2+3*lambda,w/2+b+ldi+4*lambda
point icon,ctr+wdi/2+3*lambda,w/2+b-lambda
point icon,ctr+wdi/2+lambda,w/2+b-lambda
point icon,ctr+wdi/2+lambda,w/2+b+ldi+2*lambda
point icon,ctr-wdi/2-lambda,w/2+b+ldi+2*lambda
point iecc,ctr-wdi/2-lambda,w/2+b-lambda
! Lower Contact
point ibccf,ctr-wdi/2-3*lambda,-1*(w/2+b-lambda)
point icon,ctr-wdi/2-3*lambda,-1*(w/2+b+ldi+4*lambda)
point icon,ctr+wdi/2+3*lambda,-1*(w/2+b+ldi+4*lambda)
point icon,ctr+wdi/2+3*lambda,-1*(w/2+b-lambda)
point icon,ctr+wdi/2+lambda,-1*(w/2+b-lambda)
point icon,ctr+wdi/2+lambda,-1*(w/2+b+ldi+2*lambda)
point icon,ctr-wdi/2-lambda,-1*(w/2+b+ldi+2*lambda)
point iecc,ctr-wdi/2-lambda,-1*(w/2+b-lambda)
! Now, the ion implant
level isolation
! Upper ion
point ibccf,ctr-wdi/2-4*lambda,w/2+b+lambda
point icon,ctr-wdi/2-4*lambda,w/2+b+ldi+5*lambda
point icon,ctr+wdi/2+4*lambda,w/2+b+ldi+5*lambda
point iecc,ctr+wdi/2+4*lambda,w/2+b+lambda
! Lower Ion
point ibccf,ctr-wdi/2-4*lambda,-1*(w/2+b+lambda)
point icon,ctr-wdi/2-4*lambda,-1*(w/2+b+ldi+5*lambda)
point icon,ctr+wdi/2+4*lambda,-1*(w/2+b+ldi+5*lambda)
point iecc,ctr+wdi/2+4*lambda,-1*(w/2+b+lambda)

```

```

! Now, add some air bridges:
level post
if (2*b+w) >= 200 then
    wab=30
else
    wab=20
end if
point ibccf,0,b+w/2+5
point icon,0,b+w/2+5+wab
point icon,wab/2,b+w/2+5+wab
point iecc,wab/2,b+w/2+5

point ibccf,0,-1*(b+w/2+5)
point icon,0,-1*(b+w/2+5+wab)
point icon,wab/2,-1*(b+w/2+5+wab)
point iecc,wab/2,-1*(b+w/2+5)

point ibccf,lli-wab/2,-1*(b+w/2+5)
point icon,lli-wab/2,-1*(b+w/2+5+wab)
point icon,lli,-1*(b+w/2+5+wab)
point iecc,lli,-1*(b+w/2+5)

point ibccf,lli-wab/2,b+w/2+5
point icon,lli-wab/2,b+w/2+5+wab
point icon,lli,b+w/2+5+wab
point iecc,lli,b+w/2+5

level ab

point ibccf,0,b+w/2+5+wab+lambda
point icon,0,-1*(b+w/2+5+wab+lambda)
point icon,lli,-1*(b+w/2+5+wab+lambda)
point icon,lli,b+w/2+5+wab+lambda
point icon,0,b+w/2+5+wab+lambda
point icon,wab/2+lambda,b+w/2+lambda
point icon,lli-wab/2-lambda,b+w/2+lambda
point icon,lli-wab/2-lambda,-1*(b+w/2+lambda)

```

```
point icon,wab/2+lambda,-1*(b+w/2+lambda)
point iecc,wab/2+lambda,b+w/2+lambda

end define
```


Appendix B

Detailed Processing Information

Over the three years that this project has been under way, several different wafer vendors and process improvements have been tried. The greatest consistency and reliability in molecular beam epitaxial wafers occurred with Quantum Epitaxial Designs, Inc., Ben Franklin Technology Center, 115 Research Drive, Bethlehem, Pennsylvania 18015. What follows is a detailed description of the processing procedure followed by Dr. Mark Rodwell's research group. It represents the latest refinements implemented in the latest process run. Earlier process runs were similar.

I. Standard Processing Steps.

A. Solvent Cleaning

1. Check the resistivity of the DI water. It should be $> 17M\Omega$
2. Hot TCA 5 min.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 3 min.
7. Blow dry with N_2
8. Dehydration bake, 120°C , 30 min. in petri dish without cover

B. AZ P 4210 Photoresist Application

1. Cool down after dehydration, 10 min.
2. Use our own spinner bowl and our chuck without the O-ring
3. Wafer on spinner chuck with vacuum, blow with N_2
4. Apply AZ P 4210 with syringe and filter to cover wafer
5. Spin at 5.5 krpm for 30 sec.
6. Soft Bake, 90°C , 30 min. in petri dish without cover

7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
- C. AZ P 4330-RS Photoresist Application
1. Cool down after dehydration, 10 min.
 2. Use our own bowl and chuck without O-ring
 2. Wafer on spinner chuck with vacuum, blow with N_2
 3. Apply AZ P4330-RS with syringe and filter to cover wafer
 4. Spin at 6 krpm for 30 sec.
 5. Soft Bake, 90°C , 30 min. in petri dish without cover
 7. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
- D. AZ P 4210 Exposure
1. Cool down after soft bake, 10 min.
 2. Use exposure of 7.5 mW for 10.5 sec. (79 mJ)
 3. Use hard-contact (HP mode) and use our own O-ring
- E. AZ Liftoff Development
1. 2 beakers of AZ 400K : H_2O :: 1:4 in temperature control bath (20°C)
 2. 1 beaker of toluene in temp. control bath (can be recycled) with cover
 3. 10 min. toluene soak
 4. Blow off toluene with N_2
 5. Develop in first beaker for 60 sec.
 6. Develop in second beaker for 30 sec.
 7. Rinse in running DI water for 3 min.
 8. Blow dry with N_2
- F. AZ Post-Baked Development
1. Mix AZ 400K : H_2O :: 1 : 4
 2. 2 beakers of diluted developer in temperature control bath (20°C)
 3. Develop in first beaker for 45 sec.
 4. Develop in second beaker for 15 sec.
 5. Rinse in running DI water for 3 min.
 6. Blow dry with N_2
 7. Oxygen plasma descum
 - a. 300mT of O_2
 - b. power = 100W at high frequency (13.56 MHz)
 - c. run for 15 seconds
 8. Post Bake in 120°C oven for 30 min. in petri dish without cover
- G. Oxygen Plasma Descum of Photoresist
1. 300mT of O_2
 2. power = 100W at high frequency (13.56 MHz)
 3. run for 15 seconds

H. Liftoff (in order of severity)

1. Beaker of ACE with magnetic stirrer bar at setting of 3-4 (usually takes ~ 20 min.)
2. ACE squirt bottle
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight.
4. Only as a last resort: Beaker of ACE in ultrasonic
5. Rinse in METH then ISO with squirt bottle
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2

II. Self-Aligned Ohmic Contacts (Dark-Field)

- A. Solvent Cleaning (standard)
- B. AZ P 4210 Photoresist Application (standard)
- C. AZ P 4210 Exposure (standard)
- D. AZ Liftoff Development (standard)
- E. Oxygen Plasma Descum of Photoresist (standard)
- F. Recess Etch
 1. Mix etchant
 - a. $NH_4OH : H_2O_2 : H_2O :: 21 \text{ ml} : 3.6 \text{ ml} : 300 \text{ ml}$
 - b. Use magnetic stirrer bar to agitate solution 30 min. before etch
 2. Mix a dilute slution of $NH_4OH : H_2O :: 1 : 10$
 3. Dektak wafer, measure photoresist thickness
 4. Dip in dilute NH_4OH for 20 sec.
 5. Rinse in DI for 3 min.
 6. Etch in $NH_4OH : H_2O_2 : H_2O$ solution for 20 or 30 seconds
 - a. Etch rate: $\sim 70\text{\AA}/\text{sec}$.
 7. Rinse in running DI for 3 min.
 8. Blow dry with N_2
 9. Use Dektak to determine etch depth and rate
 10. Etch to get through N+ region, repeating steps 6 to 9, rotating wafer 180°
- G. Evaporation
 1. Place wafer in E-Beam mount
 2. Use aluminum ring to mask wafer edges
 3. Make sure the crystal monitor reads < 18 ; change if necessary
 4. Pump down to at least $2 \cdot 10^{-6}$ torr
 5. Deposit material:
 - a. Ge 108\AA , $2 - 3\text{\AA}/\text{sec}$.
 - b. Au 102\AA , $2 - 3\text{\AA}/\text{sec}$.

- c. Ge 63\AA , $2 - 3\text{\AA}/\text{sec}$.
- d. Au 236\AA , $2 - 3\text{\AA}/\text{sec}$.
- e. Ni 100\AA , $2 - 3\text{\AA}/\text{sec}$.
- f. Au 1500\AA , $5\text{\AA}/\text{sec}$. (5 min. cooldown)
- g. Au 1500\AA , $5\text{\AA}/\text{sec}$.

H. Liftoff (standard)

I. Rapid Thermal Anneal

1. Program RTA for the following:
 - a. delay 20 sec.
 - b. ramp $30^\circ\text{C}/\text{sec}$. to 400°C
 - c. sustain 60 sec. 400°C
 - d. delay 150 sec. to cool
2. Place wafer in center of Si holder
3. Run Program
4. Rinse wafer in DI for 2 min.
5. Inspect under microscope to verify proper annealing
6. Measure TLM pattern, should get $R_C \sim 20\Omega \cdot \mu\text{m}$, $R_{SH} \sim 4\Omega/\text{sq}$.
7. If you don't get typical values $\pm 50\%$, consider changing program

III. Ion Implantation Mask (Dark-Field)

A. Solvent Cleaning (standard)

B. Silicon Dioxide Application

1. Thickness should be $\sim 1000\text{\AA}$
2. Index should be ~ 1.49
3. Proceed with polyimide application immediately

C. Polyimide Application

1. Mix adhesion promoter in a dropper bottle
 - a. One part QZ 3289 concentrate
 - b. Nine parts QZ 3290 dilutant
2. Use our own bowl and chuck without O-ring
3. Wafer on spinner chuck with vacuum
4. Blow off with N_2
5. Apply adhesion promoter to cover wafer
6. Spin at 5 krpm for 30 sec.
7. Let evaporate for 2 min. on chuck then blow off with N_2
8. Apply Probromide 284 to cover wafer with syringe and filter
9. Spin at 6 krpm for 30 sec. (gives $\sim 1.4\mu\text{m}$ film)
10. Clean the bowl and chuck with ACE (wear a Silver Shield glove)
11. Hard bake polyimide in petri dish without cover

- a. 90°C for 30 min.
 - b. ramp to 170°C at 5°C per min.
 - c. hold at 170°C for 40 min.
 - d. ramp to 240°C at 2°C per min.
 - e. hold at 240°C for 20 min.
 - f. ramp to 170°C at 2°C per min.
- D. Oxygen Plasma
1. Set for 100 W, 300 mTorr of O_2
 2. Run for 1 min. (etches $\sim 0.4\mu\text{m}$ of polyimide)
- E. AZ P 4210 Photoresist Application (standard)
- F. AZ P 4210 Exposure (standard)
- G. AZ Liftoff Development (standard)
- H. Evaporation
1. Place wafer in E-Beam mount
 2. Use aluminum ring to mask wafer edges.
 3. Use boom to lower sample, increasing deposition rate by a factor of ~ 3.1
 4. Make sure the crystal monitor reads < 18 ; change if necessary
 5. Pump down to at least $2 \cdot 10^{-6}$ torr
 6. Deposit material:
 - a. $\text{Ti } 200 \div 3.1 = 65\text{\AA}, 2 - 3\text{\AA}/\text{sec}.$
 - b. $\text{Au } 8,000 \div 3.1 = 2580\text{\AA}, 5 - 7\text{\AA}/\text{sec}.$ (8 min. cooldown)
 - c. $\text{Au } 8,000 \div 3.1 = 2580\text{\AA}, 5 - 7\text{\AA}/\text{sec}.$
- I. Liftoff (standard)
- J. Polyimide Post Bake (in petri dish without cover)
1. 170°C for 15 min.
 2. ramp to 240°C at 2°C per min.
 3. hold at 240°C for 30 min.
 4. ramp to 170°C at 2°C per min.
- K. Polyimide Etch
1. 10 min. cool down
 2. Set for 200 W, 300 mTorr of O_2
 3. Run for ~ 8 min. to remove all polyimide from exposed areas
 4. Inspect under microscope
 4. Run longer if necessary in 30 or 60 sec. steps
- L. Ion Implantation
1. First call, then send via Federal Express to:
IICO Corp.

3050 Oakmead Village Drive
Santa Clara, Ca 95051
(408) 727-2547

2. Typical implant (Change implant profile to fit your epi structure)
 - a. Proton (H⁺), $1.7 \cdot 10^{15} \text{cm}^{-2}$, 180keV , 7° off angle
 - b. Proton (H⁺), $4 \cdot 10^{14} \text{cm}^{-2}$, 110keV , 7° off angle
 - c. keep beam current $\sim 100 \mu\text{A}$ to minimize heating

M. Strip Polyimide

1. Put wafer in suspended holder and heat polyimide thinner $\sim 90^\circ\text{C}$
2. Allow wafer to soak in hot thinner for ~ 60 min. with stirrer bar.
3. Put wafer in room temperature polyimide stripper for 10 min.
4. If some Au remains, put back in hot thinner for 60 min. as in steps 1 & 2
5. Put hot thinner into ultrasonic bath and run for 1 min.
 - a. By this time, all pieces of gold should be gone; goto 6.
 - b. If some gold pads remain, goto step 3
6. Put in room temperature stripper for 10 min.
7. Put back in hot thinner with stirrer bar for 10 min.
8. Follow with ACE, METH, ISO in squirt bottles
9. Rinse in running DI for 3 min.
10. Inspect under microscope
11. If more gold remains, repeat entire process, steps 1 to 9

N. Oxygen Plasma Clean

1. Set O_2 plasma for 300 mTorr and 300 W
2. Run for 10 minutes
3. Inspect under microscope
4. If any scum remains, run in plasma for longer

O. Silicon Dioxide Removal

1. Put wafer in straight Buffered HF for 2 min.
2. Rinse in running DI for 3 min.
3. Inspect under microscope
4. Etch again in 30 sec. intervals as necessary

IV. Schottky Contacts and Interconnect Metal (Dark-Field)

- A. Solvent Cleaning (standard)
- B. AZ P 4210 Photoresist Application (standard)
- C. AZ P 4210 Exposure (standard)
- D. AZ Liftoff Development (standard)
- E. Oxygen Plasma Descum of Photoresist (standard)

F. Evaporation

1. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$
2. Dip in dilute NH_4OH for 20 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N_2
5. Place wafer in E-Beam mount
6. Use aluminum ring to mask wafer edges.
7. Use boom to lower sample, increasing deposition rate by a factor of ~ 3.1
8. Make sure the crystal monitor reads < 18 ; change if necessary
9. Pump down to about $7 \cdot 10^{-7}$ torr
10. Deposit material:
 - a. Ti $200 \div 3.1 = 65\text{\AA}$, $2 - 3\text{\AA}/\text{sec}$.
 - b. Pt $500 \div 3.1 = 165\text{\AA}$, $2 - 3\text{\AA}/\text{sec}$.
 - c. Au $5,000 \div 3.1 = 1615\text{\AA}$, $4 - 6\text{\AA}/\text{sec}$. (5 min. cooldown)
 - d. Au $5,000 \div 3.1 = 1615\text{\AA}$, $4 - 6\text{\AA}/\text{sec}$.

G. Liftoff (standard)

V. Air Bridges and Posts (both Dark-Field)

NOTE: You must proceed from steps A. to I. without stopping!

- A. Solvent Cleaning (standard)
- B. AZ P 4330-RS Photoresist Application (standard)
- C. AZ P 4330-RS Exposure # 1 : Post Mask
 1. Cool down after soft bake, 10 min.
 2. Set exposure of 7.5 mW for 12.5 sec. (94 mJ)
 3. Use hard-contact (HP mode) and use our own O-ring
- D. AZ Post-Baked Development (standard)
- E. Gold Etch
 1. Mix new etchant every time: Gold Etch : $H_2O :: 1 : 5$
 2. Etch for 5 sec.
 3. Rinse in running DI for 3 min.
- F. Sputter Flash Layer
 1. Load Sample
 2. Pump down to less than $5 \cdot 10^{-6}$
 3. Set Ar pressure to 20 mTorr
 4. Ti Layer
 - a. Adjust power level to 0.1 kW
 - b. sputter 100\AA Ti (deposition rate is $\sim 70\text{\AA}/\text{min}$.)
 5. Au Layer

- a. Adjust power level to 0.2 kW
- b. Sputter 2000Å Au (deposition rate is $\sim 643\text{\AA}/\text{min.}$)
6. Ti Layer
 - a. Adjust power level to 0.1 kW
 - b. sputter 300Å Ti (deposition rate is $\sim 70\text{\AA}/\text{min.}$)
- G. AZ P 4330-RS Photoresist Application (standard)
- H. AZ P 4330-RS Exposure # 2 : Air Bridge Mask
 1. Cool down after soft bake, 10 min.
 2. Use exposure of 7.5 mW for 14 sec. (105 mJ)
 3. Use hard-contact (HP mode) and use our own O-ring
- I. AZ Post-Baked Development (standard)
- J. Plating Preparation
 1. Clean tweezers, anode, thermometer and magnet with ISO and DI water
 2. Rinse wafer in running DI for 3 min.
 3. Heat 800 ml of plating solution in beaker with short stirrer bar to 45°C
- K. Titanium Etch
 1. Dektak photoresist and record initial thickness
 2. Use a swab with ACE to remove small area of photoresist for electrical contact
 3. Mix $HF : H_2O :: 1 : 20$
 4. Etch top layer of Ti ~ 30 sec. (10 sec. after surface appears gold)
 5. Rinse in running DI for 3 min.
- L. Gold Plating
 1. Plate for 15 minutes at $50\mu\text{A}$ with stirrer bar at 45°C
 2. Rinse in running DI for 3 minutes
 3. Blow dry with N_2
 4. Dektak the photoresist and calculate how much the depth has changed
 5. Adjust the current to get a plating rate of $\sim 1.8\mu\text{m}/\text{hr.}$
 6. Repeat steps 2 to 6 to keep close track of the plating rate
 7. Plate until the top of the air bridges are even with the photoresist $\sim 3\mu\text{m}$
- M. First Photoresist Layer Removal
 1. Flood expose top layer for 60 sec. at 7.5 mW
 2. 2 beakers of AZ 400K : DI :: 1 : 1
 3. Develop in first beaker for 60 sec.

4. Develop in second beaker for 30 sec.
 5. Rinse in running DI water for 3 min.
 6. Blow dry with N_2
- N. Etch First Titanium Layer
1. Use $HF : H_2O :: 1 : 20$ from before
 2. Etch for $\sim 30sec.$ with moderate agitation
 3. This should be 10 seconds after gold appears
 4. Rinse in running DI water for 3 min.
 5. Blow dry with N_2
- O. Etch Gold Layer
1. Mix new etchant: Gold Etch : $H_2O :: 1 : 1$
 2. Etch initially for 5 sec., using stirrer bar
 3. Rinse in running DI for 3 min.
 4. Blow dry with N_2
 5. Inspect under microscope
 6. If some Au is still left, etch for another 3 sec.
 7. Repeat steps 2 through 6 as necessary, rotating the wafer each time
- P. Etch Bottom Titanium Layer
1. use $HF : H_2O :: 1 : 20$ from before
 2. Etch for ~ 30 sec. with moderate agitation
 3. Etch for 10 seconds after gold appears
 4. Rinse in running DI water for 3 min.
 5. Blow dry with N_2
- Q. Remove Bottom Photoresist Layer
1. Use ACE in beaker with stirrer bar for 3 min.
 2. Follow with ACE, METH, ISO in squirt bottles
 3. Rinse in running DI for 3 min.
 4. Blow dry with N_2

At various times between processing steps, measurements are made on the wafer to determine important device characteristics. Contact and sheet resistances are measured with a TLM pattern. This pattern consists of seven 100 by 100 μm by square ohmic metal pads that have 5, 10, 15, 20, 25, and 30 μm separations. By plotting the measured resistance between adjacent pads, one can determine the sheet resistivity (R_{SH}), specific contact resistance (R_C), and the contact transfer length (L_C). Measurements of the TLM pattern are made both before and after ion implantation. Figure B.1 is a typical plot of the TLM

pattern resistances before ion implantation. Since rapid thermal annealing cannot be done after ion implantation, the TLM measurement before the implant verifies the anneal. The TLM measurement after ion implantation and Schottky metalization characterizes the material. Figure B.2 is a typical plot of the TLM pattern resistances after ion implantation.

There are two other important test structures, large area diodes and interdigitated finger diodes. The large area diodes are 100 by 100 μm areas of Schottky metal ($10000\mu\text{m}^2$). With this test structure, $I(V)$ and $C(V)$ characteristics can be determined. Figure B.3 is a typical plot of the large area diode's $I(V)$ curve and figure B.4 shows the same diode's $C(V)$ curve. The interdigitated diodes are arrays of 20 100 by 2 μm Schottky contacts ($4000\mu\text{m}^2$). The $I(V)$ curves (figure B.5) should be similar, but differences in the $C(V)$ characteristics between large area and interdigitated diodes indicates the edge effect caused by lateral depletion. The edge effect tends to flatten out the $C(V)$ curve, reducing NLTL compression (figure B.6). Data from these test structures allows characterization of most NLTL modeling parameters.

Another test structure often included is a complete NLTL with microwave probeable pads at both ends. By performing network analysis on this test structure at different bias voltages, one can determine the change in *small-signal* propagation delay (figure B.7) and insertion gain as a function of voltage (figure B.8). This indicates the device performance inclusive of all parasitics associated with the NLTL itself. Insertion gain varies with bias voltage since the diode's loss cutoff frequency ($1/2\pi R_{series}C_{diode}(V)$) increases with increasing reverse bias. A shock line is best suited to these measurements since it has a high Bragg frequency (transmission measurements are not strongly attenuated) and is fairly small.

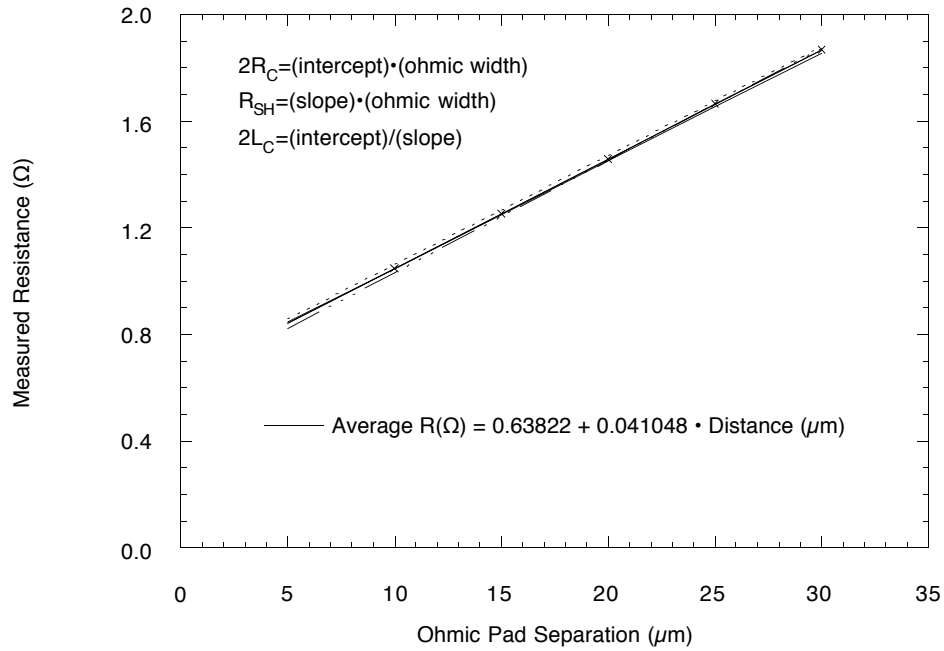


Figure B.1: TLM pattern measurement before ion implantation. Three measurements were made at different locations on QED wafer #4885 and shows $R_C = 31.9\Omega \cdot \mu\text{m}$, $R_{SH} = 4.10\Omega/\text{sq.}$, and $L_C = 7.77\mu\text{m}$.

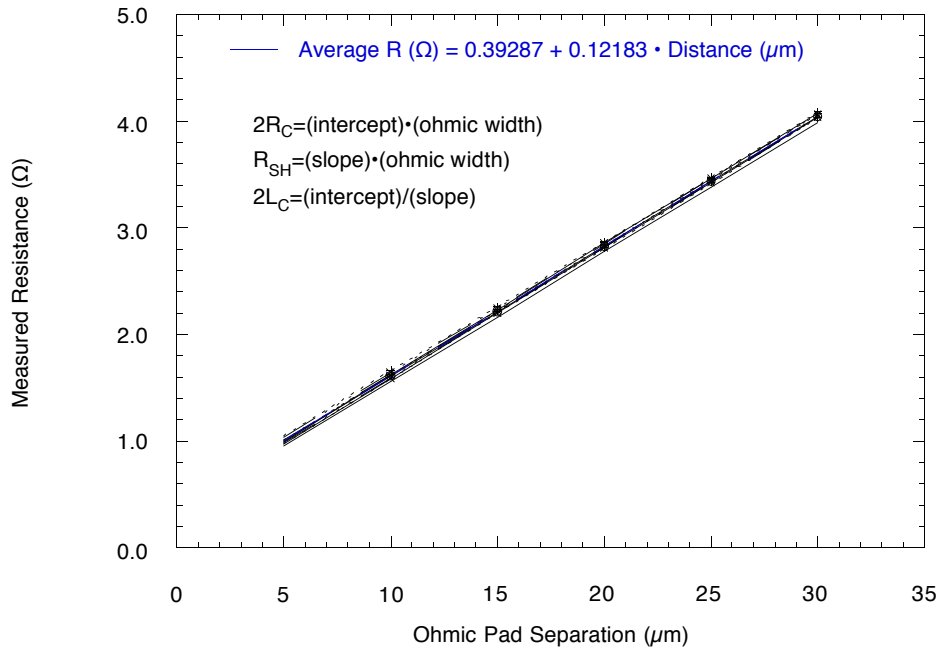


Figure B.2: TLM pattern measurement after ion implantation. Nine measurements were made at different locations on QED wafer #4885 and shows $R_C = 19.6 \Omega \cdot \mu\text{m}$, $R_{SH} = 12.1 \Omega/\text{sq.}$, and $L_C = 1.61 \mu\text{m}$.

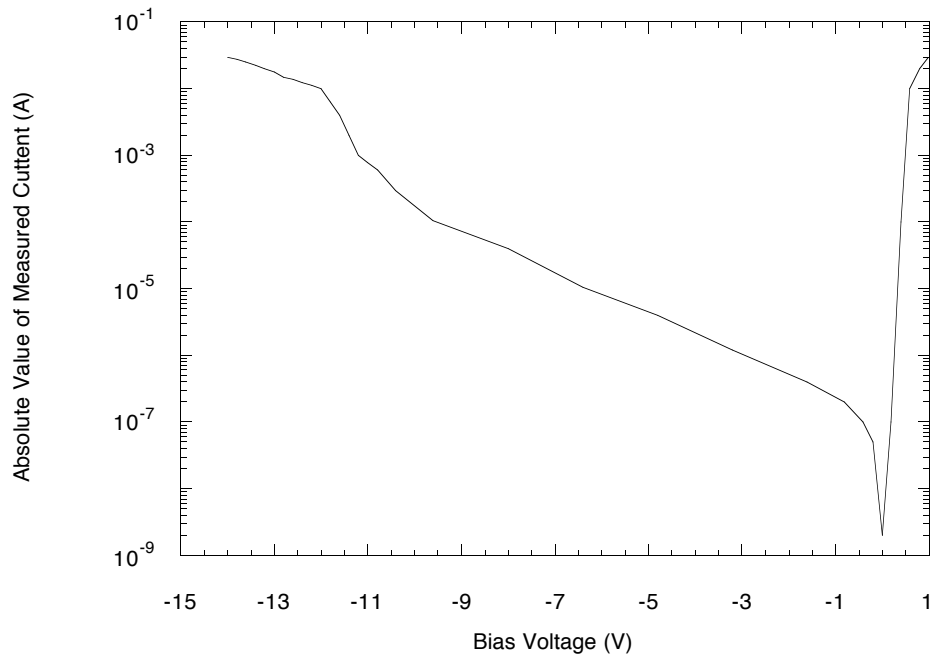


Figure B.3: 100 by 100 μm large area diode $I(V)$ characteristic from QED wafer #4885. This diode has an 11.5 V breakdown, 1.36 ideality factor, and 313 pA saturation current.

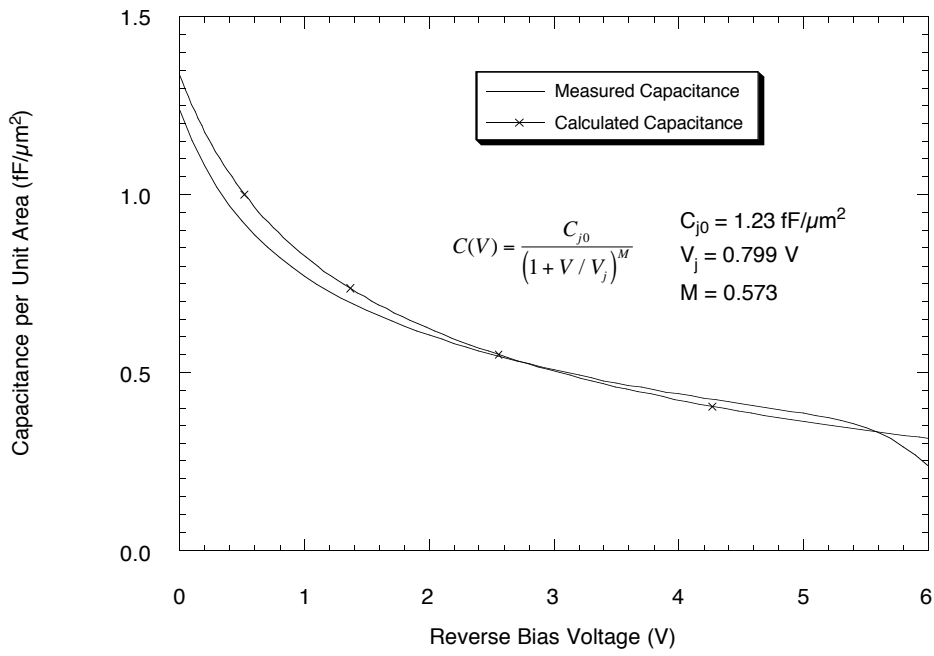


Figure B.4: 100 by 100 μm large area diode $C(V)$ characteristic from QED wafer #4885. A numerical least square error fit provides the SPICE model parameters.

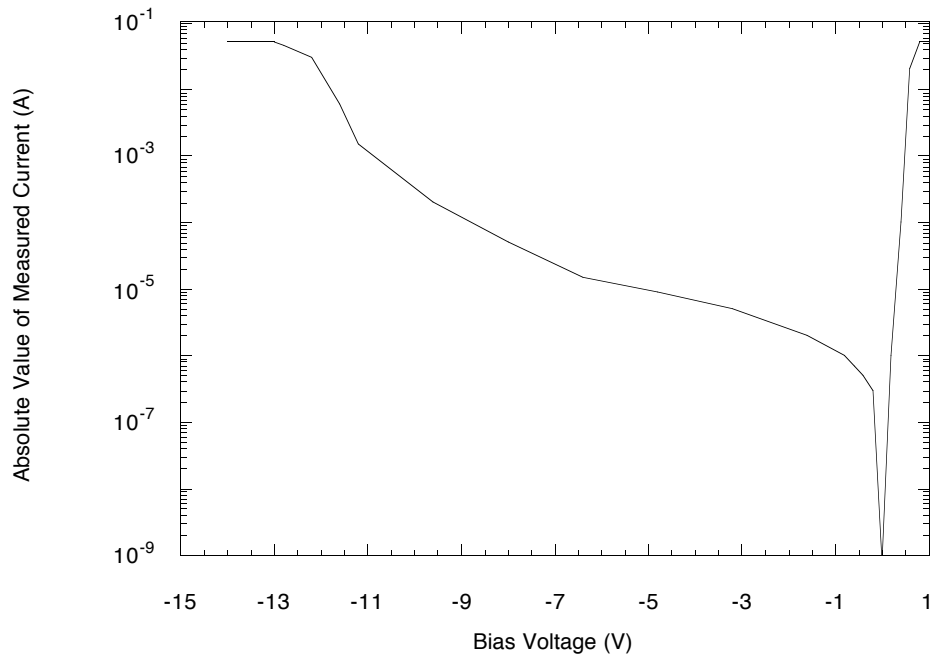


Figure B.5: Interdigitated finger diode $I(V)$ characteristic from QED wafer #4885. This diode has an 11.6 V breakdown, 1.59 ideality factor, and 1.40 nA saturation current.

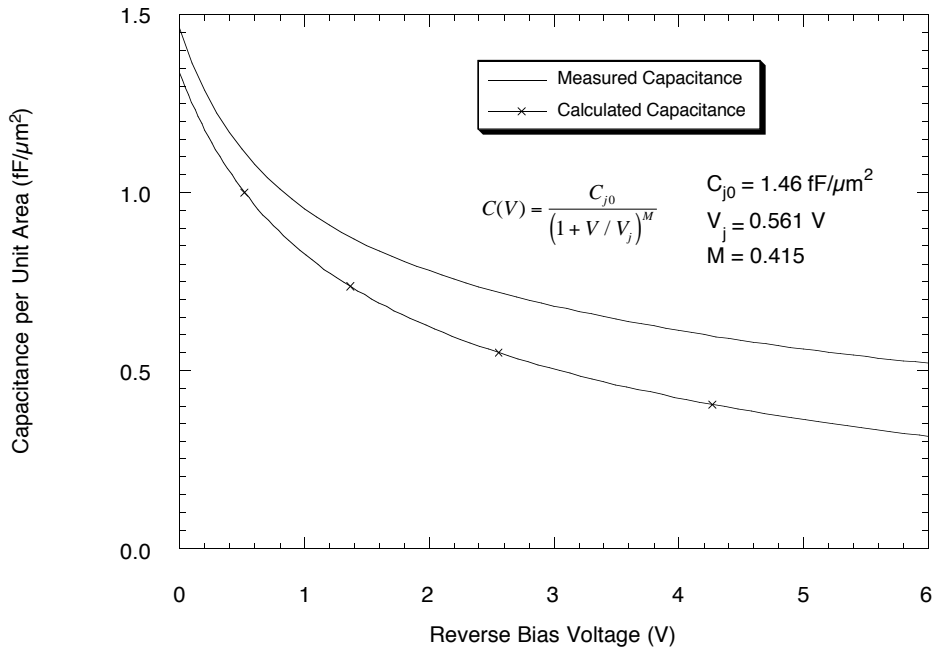


Figure B.6: Interdigitated finger diode $C(V)$ characteristic from QED wafer #4885. A numerical least square error fit provides the SPICE model parameters. The larger discrepancy between calculated and measured capacitance may be due to overexposed Schottky contacts (larger area than expected).

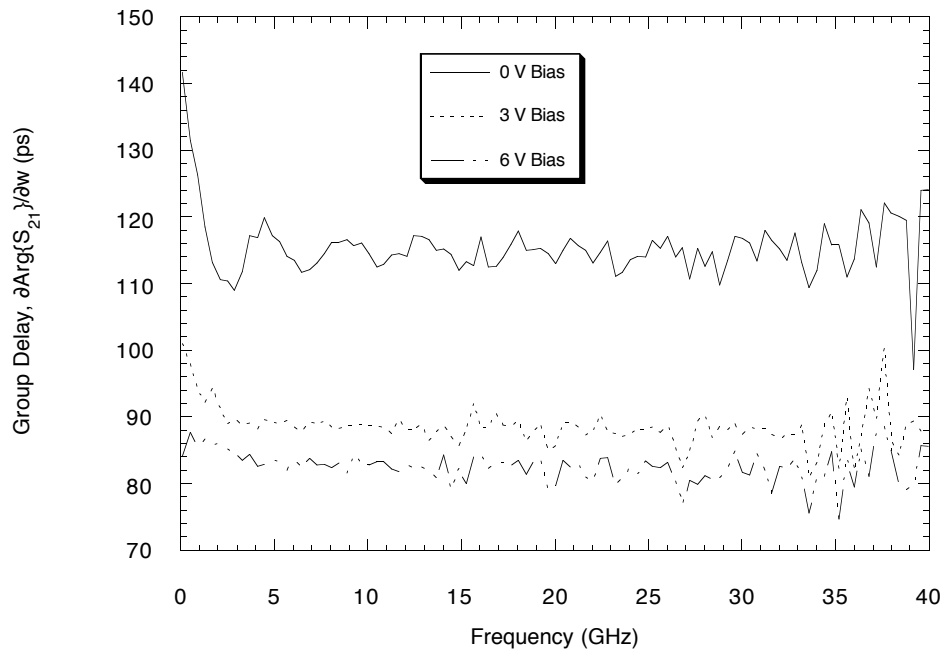


Figure B.7: Group delay measurement of the shock line on QED wafer #4885 using 90Ω interconnect CPW. The delay changes by 33.5 ps over a 6 volt swing.

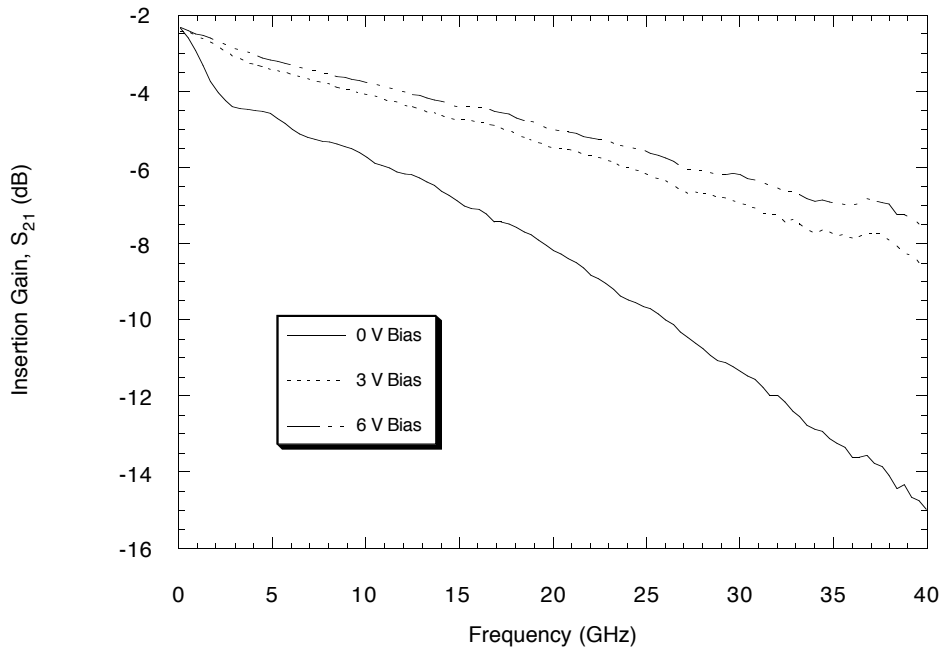


Figure B.8: Insertion gain measurement of the shock line on QED wafer #4885 using 90Ω interconnect CPW. Low frequency loss is nearly invariant with changing bias, while high frequency loss varies greatly.

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