UNIVERSITY of CALIFORNIA
Santa Barbara

# III-V Ultra-Thin-Body InGaAs/InAs MOSFETs for Low Standby Power Logic Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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Applications

# Acknowledgements

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## First Author Publications

[1] **C. Y. Huang**, P. Choudhary, S. Lee, S. Kraemer, V. Chobpattana, B. Thibeault, W. Mitchell, S. Stemmer, A. Gossard, and M. Rodwell, "*12 nm-Gate-Length Ultrathin-Body InGaAs/InAs MOSFETs with $8.3 \cdot 10^5{:}1$ $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$*," 73rd IEEE Device Research Conference(DRC), pp. 260-261, 2015. (Conference oral presentation and proceeding)

[2] **C. Y. Huang**, S. Lee, E. Wilson, P. Long, M. Povolotskyi, V. Chobpattana, S. Stemmer, A. C. Gossard, G. Klimeck, and M. J. W. Rodwell, "*Comparison of ultra-thin InAs and InGaAs quantum wells and ultra-thin-body surface-channel MOSFETs*," International Conference on Indium Phosphide and Related Materials (IPRM), 2015. (Conference oral presentation and abstract)

[3] **C. Y. Huang**, X. Bao, Z. Ye, S. Lee, H. Chiang, H. Li, V. Chobpattana, B. Thibeault, W. Mitchell, S. Stemmer, A. Gossard, E. Sanchez, and M. Rodwell, "*Ultrathin InAs-Channel MOSFETs on Si substrates,*" International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), pp. 1-2, 2015. (Conference oral presentation and proceeding)

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[8] **C. Y. Huang**, S. Lee, D. C. Elias, J. J. M. Law, A. D. Carter, V. Chobpattana, S. Stemmer, A. C. Gossard, M. J. W. Rodwell, "*Reduction of leakage current in $In_{0.53}Ga_{0.47}As$ channel metal-oxide-semiconductor field-effect-transistors using $AlAs_{0.56}Sb_{0.44}$ confinement layers,*" Applied Physics Letters, v. 103, p. 203502, 2013. (Journal paper)

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*Metal-Oxide-Semiconductor Field-Effect Transistors with AlAs$_{0.56}$Sb$_{0.44}$ Barrier Layers and InAs MBE Source/Drain Regrowth*," 30th North American Molecular Beam Epitaxy Conference (NAMBE), 2013. (Conference oral presentation and abstract)

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[14] D. C. Elias, J. J. M. Law, H. W. Chiang, A. Sivananthan, C. Zhang, B. J. Thibeault, W. J. Mitchell, S. Lee, A. D. Carter, **C.-Y. Huang**, V. Chobpattana, S. Stemmer, S. Keller, and M. J. W. Rodwell, "*Formation of Sub-10 nm width InGaAs finFETs of 200 nm Height by Atomic Layer Epitaxy,*" 71st Device Research Conference (DRC), pp. 1-2, 2013.

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## Abstract

III-V Ultra-Thin-Body InGaAs/InAs MOSFETs for Low Standby Power Logic
Applications

by

Cheng-Ying Huang

As device scaling continues to sub-10-nm regime, III-V InGaAs/InAs metal-
oxide-semiconductor field-effect transistors (MOSFETs) are promising candidates
for replacing Si-based MOSFETs for future very-large-scale integration (VLSI)
logic applications. III-V InGaAs materials have low electron effective mass and
high electron velocity, allowing higher on-state current at lower $V_{\mathrm{DD}}$ and reducing
the switching power consumption. However, III-V InGaAs materials have a nar-
rower band gap and higher permittivity, leading to large band-to-band tunneling
(BTBT) leakage or gate-induced drain leakage (GIDL) at the drain end of the
channel, and large subthreshold leakage due to worse electrostatic integrity. To
utilize III-V MOSFETs in future logic circuits, III-V MOSFETs must have high
on-state performance over Si MOSFETs as well as very low leakage current and
low standby power consumption. In this dissertation, we will report InGaAs/InAs
ultra-thin-body MOSFETs. Three techniques for reducing the leakage currents in
InGaAs/InAs MOSFETs are reported as described below.

1) Wide band-gap barriers: We developed $AlAs_{0.44}Sb_{0.56}$ barriers lattice-match
to InP by molecular beam epitaxy (MBE), and studied the electron transport
in $In_{0.53}Ga_{0.47}As/AlAs_{0.44}Sb_{0.56}$ heterostructures. The InGaAs channel MOS-

FETs using $AlAs_{0.44}Sb_{0.56}$ bottom barriers or p-doped $In_{0.52}Al_{0.48}As$ barriers were demonstrated, showing significant suppression on the back barrier leakage.

2) Ultra-thin channels: We investigated the electron transport in InGaAs and InAs ultra-thin quantum wells and ultra-thin body MOSFETs ($t_{ch} \sim$ 2-4 nm). For high performance logic, InAs channels enable higher on-state current, while for low power logic, InGaAs channels allow lower BTBT leakage current.

3) Source/Drain engineering: We developed raised InGaAs and recessed InP source/drain spacers. The raised InGaAs source/drain spacers improve electro-statics, reducing subthreshold leakage, and smooth the electric field near drain, reducing BTBT leakage. With further replacement of raised InGaAs spacers by recessed, doping-graded InP spacers at high field regions, BTBT leakage can be reduced $\sim$100:1.

Using the above-mentioned techniques, record high performance InAs MOS-FETs with a 2.7 nm InAs channel and a $ZrO_2$ gate dielectric were demonstrated with $I_{on} =$ 500 $\mu A/\mu m$ at $I_{off} =$ 100 $nA/\mu m$ and $V_{DS} =$0.5 V, showing the highest on-state performance among all the III-V MOSFETs and comparable performance to 22 nm Si FinFETs. Record low leakage InGaAs MOSFETs with recessed InP source/drain spacers were also demonstrated with minimum $I_{off} =$ 60 $pA/\mu m$ at 30 nm-$L_g$, and $I_{on} =$ 150 $\mu A/\mu m$ at $I_{off} =$ 1 $nA/\mu m$ and $V_{DS} =$0.5 V. This re-cessed InP source/drain spacer technique improves device scalability and enables III-V MOSFETs for low standby power logic applications. Furthermore, ultra-thin InAs channel MOSFETs were fabricated on Si substrates, exhibiting high yield and high transconductance $g_m \sim$2.0 $mS/\mu m$ at 20 nm-$L_g$ and $V_{DS}=$0.5 V. With further scaling of gate lengths, a 12 nm-$L_g$ III-V MOSFET has shown max-

imum $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio $\sim$8.3$\times$10$^5$, confirming that III-V MOSFETs are scalable to sub-10-nm technology nodes.

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# Chapter 1

# Introduction

## 1.1   Introduction

In 1965, a paper entitled, "Cramming More Components onto Integrated Circuits," published by Gordon Moore predicted that the number of components in integrated circuits will double roughly every two years [1]. This prediction afterwards became widely known as "Moore's law" in technology history, driving the success of computer industries for more than four decades and the fast-growing mobile computing electronics. Miniaturization of metal-oxide-semiconductor field effect transistor (MOSFET) has led to higher transistor density, higher computational capability, and simultaneously lower production cost. However, as Si complementary metal-oxide-semiconductor (CMOS) technology approaches sub-10-nm generations, increasing leakage current (standby power consumption) and increasing switching power (active power) consumption become the fundamental limits for continuous MOSFET scaling and slow down the progress of Moore's law.

Conventional MOSFET scaling not only involves the reduction of device size but also requires the reduction in the transistor supply voltage ($V_{\mathrm{DD}}$). The active power consumption decreases proportionately to the square of supply voltage ($P_{\mathrm{active}} \sim fCV_{\mathrm{DD}}^2$). Fig. 1.1(a) shows the $V_{\mathrm{DD}}$ scaling for the successive CMOS logic generations [2]. To keep constant electric field in the channel and reduce the switching power consumption, $V_{\mathrm{DD}}$ must be reduced, while low $V_{\mathrm{DD}}$ results in low on-state current and increases the switching delay ($CV_{\mathrm{DD}}/I_{\mathrm{on}}$). To attain reasonable on-state current and reduce delay, the threshold voltage $V_{\mathrm{th}}$ must be scaled down simultaneously with $V_{\mathrm{DD}}$ to maintain sufficient gate overdrive voltage ($V_{\mathrm{GS}} - V_{\mathrm{th}}$). However, low $V_{\mathrm{th}}$ causes a dramatic increase on subthreshold leak-
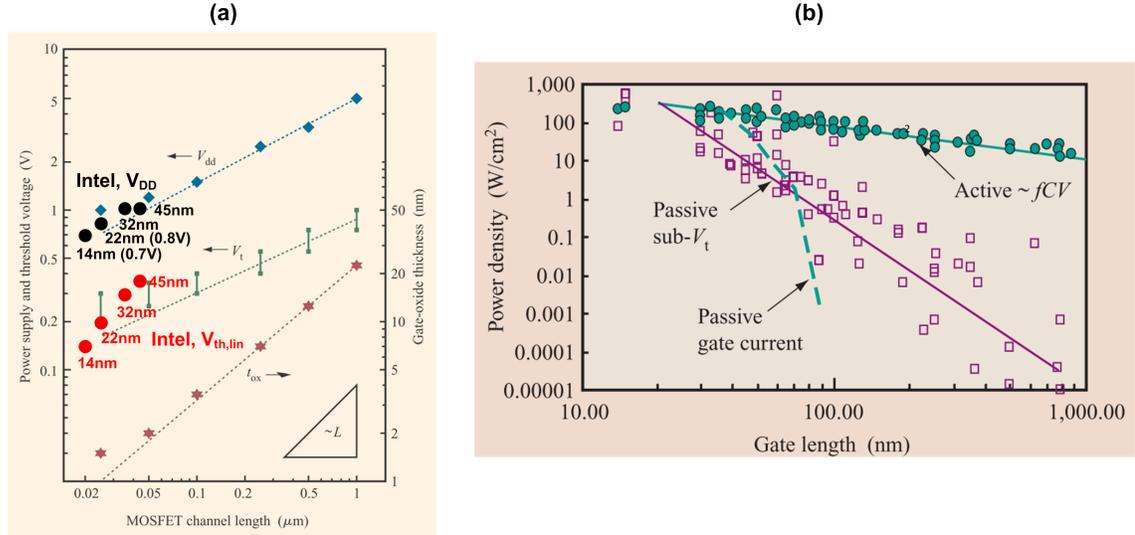
Figure 1.1: (a) $V_{\text{DD}}$ scaling, $V_{\text{th}}$ scaling, and the oxide thickness scaling for the previous CMOS generations (Modified figure from [2]). (b) Active power consumption and standby power consumption as a function of gate lengths [3].

age, and increases standby power ($P_{\text{standby}} \sim I_{\text{leakage}} V_{\text{DD}}$). Given that there is a lower limit for $V_{\text{th}}$ ($\sim$0.1 V), $V_{\text{DD}}$ scaling also slows down around $\sim$0.7-0.8 V to avoid unacceptable performance loss. Therefore, the incapable of continued $V_{\text{DD}}$ scaling gives rise to high active power consumption and is the main roadblock for continuous CMOS scaling.

The other limitation of MOSFET scaling is excess off-state leakage. High off-state leakage current can arise from large subthreshold leakage due to worse electrostatics, or from the tunneling leakage caused by large electric field in the oxides and the channels. Fig. 1.1(b) shows the active power and standby power consumption as a function of gate lengths [3]. As device scaling continues, the standby power consumption ($P_{\text{standby}} \sim I_{\text{leakage}} V_{\text{DD}}$) increases with the increment of leakage current and might approach the active power consumption if the leakage current can not be properly controlled (e.g. gate leakage in Fig. 1.1(b)). Normally

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the MOSFET off-state leakage is limited by thermionic current and the minimum off-state leakage can be set by adjusting the threshold voltage. However, with the aggressive gate length scaling and oxide thickness scaling, the other leakage components such as gate leakage, junction leakage, and band-to-band tunneling leakage now become significant as compared to thermionic leakage. Reducing these leakage currents in nanoscale MOSFETs are of the utmost importance for continuous device scaling, in particular for low standby power logic applications and the battery-driven mobile electronics.

A successful extension of Moore's law to next technology nodes requires a solution to alleviate the above-mentioned power constraint and leakage constraint. In the past decade, new materials and new device architecture have been successfully implemented in modern CMOS technology to enable continued MOSFET scaling, for examples, SiGe source/drain stressor at 90 nm node [4], high-k/metal gate process at 45 nm node [5], and tri-gate transistor at 22 nm node [6]. To extend Moore's law to sub-10-nm generations, more innovations are indispensable and will definitely come in the foreseeable future.

Recently, new channel materials such as III-V compound semiconductors and Ge have drawn great attention because of their superior transport properties. III-V InGaAs/InAs materials are considered as promising candidates to replace Si n-channel MOSFETs. InGaAs channels have higher electron mobility and electron velocity than that of Si MOSFETs, which could deliver higher $I_{\mathrm{on}}$ at lower supply voltage. On the counterpart of p-channel, Ge is a very attractive replacement of Si p-channel MOSFETs because Ge has higher hole mobility and hole velocity. By introducing these heterogeneous channels (III-V and Ge) on the ex-

isting Si CMOS process platform, higher $I_{\text{on}}$ could be achieved at an aggressively scaled $V_{\text{DD}}$ around $\sim$0.5 V. Therefore, these high mobility channels could alleviate the limitations of $V_{\text{DD}}$ scaling and enable lower active power consumption.

## 1.2   Why III-V MOSFETs?

III-V InGaAs/InAs materials have smaller electron effective mass ($m^* \sim 0.041$ for $In_{0.53}Ga_{0.47}As$) than Si channels ($m_{\text{t}}^* \sim 0.19$). Smaller electron effective mass provides the excellent transport properties, as evidenced by high electron mobility ($\mu \sim 1/m^*$) and high injection velocity ($v_{\text{inj}} \sim \sqrt{1/m^*}$). Table 1.1 compares the material properties of Si, Ge, and III-V materials. Fig. 1.2 shows the injection velocity of III-V channels and Si channels [7]. Even at lower $V_{\text{DD}}$ at 0.5 V, the injection velocity of III-V channels is about $3 \times 10^7$ (cm/s), at least two times higher than strained-Si channels. Besides the superior transport properties, III-V materials also have relatively mature manufacturing experiences from the radio-frequency (RF), microwave and millimeter wave analog industries. A wide variety of compound semiconductors provides an immense playground (e.g. band-gap, band alignment, effective mass, and strain etc.) to engineer the device structure and improve transistor performance. Because of smaller effective mass and higher tunneling probability, lower contact resistance (n-type) on III-V materials can also be obtained, which is pivotal for the on-state performance of nanoscale transistors [8].

Introducing III-V channels for VLSI logic applications has encountered tremendous challenges that still have not been resolved yet [9]. A suitable gate di-

| 300K | Si | Ge | GaAs | InAs | $In_{0.53}Ga_{0.47}As$ |
|---|---|---|---|---|---|
| Electron effective mass, $m_e^*$ | 0.19 | 0.08 | 0.063 | 0.023 | 0.041 |
| Electron mobility, $\mu_e(cm^2/Vs)$ | 1450 | 3900 | 9200 | 33000 | 12000 |
| Hole mobility, $\mu_h(cm^2/Vs)$ | 370 | 1800 | 400 | 450 | 300 |
| Band gap, $E_g(eV)$ | 1.12 | 0.66 | 1.42 | 0.35 | 0.74 |
| Relative permittivity, $\epsilon_r$ | 11.7 | 16.2 | 12.9 | 15.2 | 13.9 |
| Lattice constant($\mathring{A}$) | 5.43 | 5.66 | 5.65 | 6.06 | 5.87 |
| Thermal expansion coefficient $(10^{-6}\ ^\circ C^{-1})$ | 2.6 | 5.9 | 5.73 | 4.52 | 5.66 |

Table 1.1: Material properties for Si, Ge and III-V compound semiconductors.
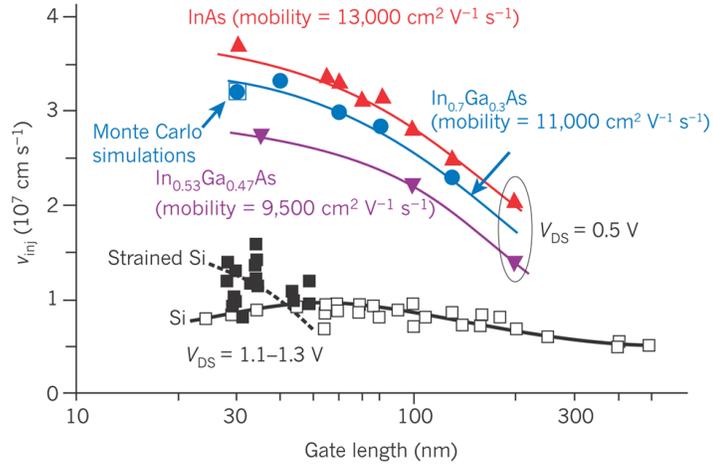


Figure 1.2: Comparison of electron injection velocity of III-V HEMT and Si MOSFETs [7].

electric with high permittivity and lower interface trap density is crucial for MOS-FET operations. Unlike $Si/SiO_2$ interfaces, to achieve high quality gate dielectrics on III-V channels poses the first formidable challenge. The widely-held belief is the exposure of III-V channels to the air must be prevented so that the in-situ oxide deposition immediately after channel growth is necessary [10,11]. Recently, the development of self-cleaning process in atomic layer deposition (ALD) has significantly improved high-k/III-V interfaces [12–14] and allowed a more flexible gate-last integration solution. The other major challenge is a suitable and manu-facturable scheme to integrate III-V materials on Si wafers. The very dissimilar material properties between III-V and Si give rise to a high density of defects such as threading dislocations, anti-phase boundaries, and stacking faults/twins. These defects might imperil the device operations, so an effective method to pre-vent defect formation or to divert defects away from the device active area must be established [9, 15, 16]. On the other hand, for VLSI CMOS, n-/p- channels must coexist on the Si wafers. This greatly increases the process/integration com-plexity, and the solution must be found and validated.

In terms of device performance, high off-state leakage currents render III-V MOSFETs unsuitable for VLSI logic circuits. Since III-V channels have smaller band-gap, as shown in Table 1.1, large band-to-band tunneling occurs at the re-gions of crowded electric field, leading to excess off state leakage and limiting the device scalability. Higher relative permittivity of III-V channel also results in worse electrostatics and the increased subthreshold leakage. The band-to-band tunneling leakage and high subthreshold leakage strongly jeopardize the applica-tion of III-V MOSFETs at sub-10-nm technology nodes. To meet the requirements

for wide-span logic products from high performance (HP) servers to low-power (LP) mobile computing electronics, the leakage current must be sufficiently low ($I_{off}$ $\sim$100 nA/$\mu$m for HP, and 30 pA/$\mu$m for LP). Therefore, toward the ultimate success, III-V MOSFETs must be demonstrated on Si, with substantial higher performance than Si MOSFETs as well as very low leakage currents for different types of logic products.

## 1.3    Outline

In this dissertation, we are focused on III-V InGaAs/InAs ultra-thin body MOSFETs as illustrated in Fig. 1.3. The final goal is to achieve high performance and very low leakage III-V MOSFETs for both high performance and low standby power logic applications. Several leakage reduction methods—including barrier engineering, channel engineering, and source/drain engineering—are proposed during the progress toward this goal. The outline of this dissertation is described below.

Chapter 2 briefly introduces the ballistic MOSFET theory and the practical design considerations for nanoscale MOSFETs, including parasitic resistance, interface traps, MOSFET electrostatics, and off-state leakage currents. The MOSFET on-state performance, subthreshold characteristics, and the band-to-band tunneling leakage will be discussed in detail.

Chapter 3 discusses the back barrier design of planar III-V MOSFETs. To reduce the back barrier leakage, two approaches have been proposed. The first
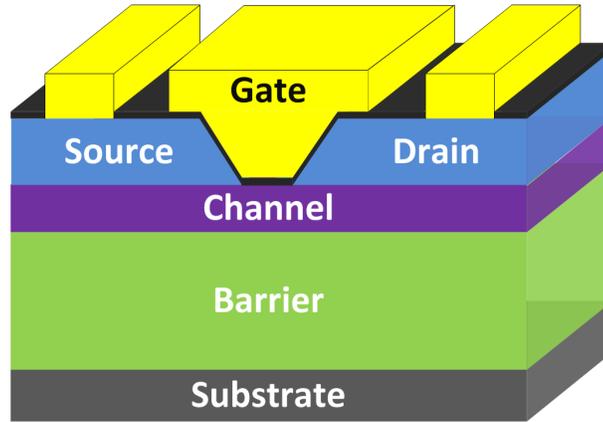
Figure 1.3: UCSB ultra-thin channel planar MOSFETs.

approach is the implementation of wide band-gap AlAsSb barriers. The MBE growth of AlAsSb, the electron transport in InGaAs/AlAsSb heterostructures, and the MOSFET results for comparing InAlAs barriers and AlAsSb barriers are investigated in detail. The second approach is using P-type doped InAlAs barriers, which is also capable of reducing the buffer leakage.

Chapter 4 considers the ultimate channel design for ultra-thin body III-V MOSFETs. We first investigate the electron transport properties in InAs and InGaAs quantum wells. We then compare the ultra-thin surface channel InGaAs and InAs MOSFETs. As the channel thickness decreases, strong quantum confinement effects and non-parabolic band effects significantly influence the electron transport properties. In addition, we observe that the oxide traps above the conduction band edge of the channels greatly reduce the channel mobility and reduce on-state current. We conclude this chapter with a demonstration of record high performance InAs MOSFETs, showing comparable on-state performance to 22 nm Si FinFETs.

Chapter 5 reports the source/drain engineering for III-V MOSFETs. The

source/drain vertical spacers are proposed to improve transistor electrostatics and suppress the leakage currents. Using a recessed InP source/drain spacer, band-to-band tunneling leakage can be significantly reduced. We demonstrate the record low leakage III-V MOSFETs with minimum $I_{\text{off}} \sim 60$ pA/$\mu$m at $L_{\text{g}} = 30$ nm. This recessed InP spacer greatly improves the device scalability and enables III-V MOS-FETs for low power logic applications.

Chapter 6 demonstrates a 12 nm $L_{\text{g}}$ III-V ultra-thin channel MOSFET. A 2.5 nm InGaAs/InAs composite channel MOSFET with doping-graded, recessed InP source/drain spacers shows well-balanced on/off DC performance, featuring maximum $I_{\text{on}}/I_{\text{off}}$ ratio larger than $8.3 \times 10^5$, minimum leakage current around 1.3 nA/$\mu$m, and the subthreshold swing around 107 mV/dec. at $V_{DS} = 0.5V$. The FET result confirms that III-V MOSFETs are scalable to sub-10-nm technology nodes.

Chapter 7 demonstrates high performance and high yield ultra-thin InAs channel MOSFETs on Si substrates. A 20 nm gate length MOSFET exhibits high on-state current and high extrinsic transconductances ($\sim 2$ mS/$\mu$m). The III-V MOSFETs on Si substrates show negligible buffer leakage. The device results will be compared in detail with InAs MOSFETs on InP substrates.

Chapter 8 concludes this dissertation and summarizes the key experimental results. The directions for further improvements on transistor performance will be discussed.

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# Chapter 2

# MOSFET Theory and Design

In this chapter, we briefly review the ballistic MOSFETs theory and compare the ballistic currents for III-V MOSFETs and Si MOSFETs. We also introduce the practical design considerations for nanoscale MOSFETs, including on-state performance, subthreshold characteristics and off-state leakage. Several important device parameters are defined in this chapter, and will be widely used for the analysis of experimental data.

## 2.1   Ideal MOSFETs theory

### 2.1.1   Ballistic MOSFET model

As transistor gate lengths decrease, the operation of transistor approaches ballistic limits [1, 2]. The ballistic electrons travel from the source to the drain without losing their energy through scattering events, and the electrons only relax the energy when arriving at heavily-doped drain. For ballistic MOSFETs, the on-state current can be described by,

$$\frac{I_{\mathrm{D}}}{W_{\mathrm{g}}} = q v_{\mathrm{inj}} C_{\mathrm{g-ch}} (V_{\mathrm{GS}} - V_{\mathrm{th}}) \tag{2.1}$$

where the $v_{\mathrm{inj}}$ is the injection velocity, $C_{\mathrm{g-ch}}$ is the total gate-to-channel capacitance, and $V_{\mathrm{GS}} - V_{\mathrm{th}}$ is gate overdrive voltage. The current is determined by the gate-to-channel capacitance and the injection velocity at the top of the barrier, as seen in Fig. 2.1(a).

The total gate-to-channel capacitance, $C_{\mathrm{g-ch}}$, consists of three series capac-
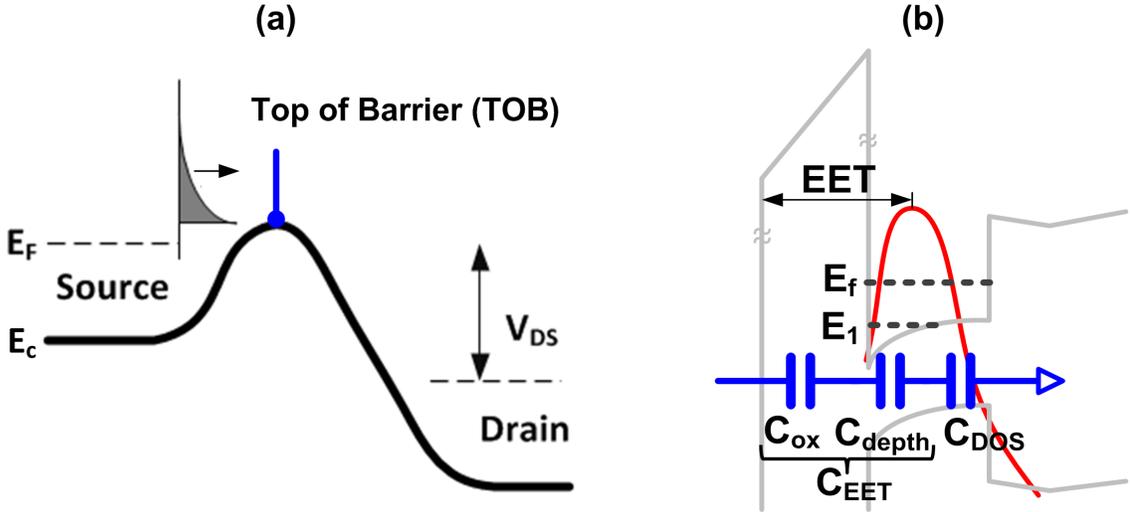
Figure 2.1: (a) The band diagram of MOSFETs along the channels, showing that the position of top-of-barrier determines the amount of current flow from the source to the drain. (b) The gate-to-channel capacitance consists three series capacitances, including oxide capacitance, wave-function depth capacitance, and density-of-state capacitance (Courtesy of Sanghoon Lee).

itances shown in Fig. 2.1(b); $C_{\text{ox}}$, the gate oxide capacitance, and $C_{\text{depth}}$, the capacitance term from semiconductors due to the offset of the centroid of electron wave-function from the oxide/channel interface, and $C_{\text{DOS}}$, the density of state capacitance associated with the Fermi level ($E_{\text{F}}$) position relative to the first sub-band ($E_1$) in the quantum wells. These three capacitances can be described as the following equations [3].

$$C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} \tag{2.2}$$

$$C_{\text{depth}} \simeq \frac{\epsilon_{\text{channel}}}{\frac{t_{\text{ch}}}{2}} \tag{2.3}$$

$$C_{\text{DOS}} = \frac{d(-qN_{\text{s}})}{d(\frac{E_{\text{f}}-E_1}{q})} = \frac{g_{\text{v}}\frac{q^2 m*^2}{\pi\hbar^2}}{1 + \exp(-\frac{E_{\text{f}}-E_1}{kT})} \tag{2.4}$$

where $\epsilon_{\text{ox}}$ and $\epsilon_{\text{channel}}$ are the permittivity of the gate oxide and the semiconductor channel, respectively. $t_{\text{ox}}$ and $t_{\text{ch}}$ are the oxide thickness and the channel thickness, respectively. $g_{\text{v}}$ is band degeneracy and is equal to 1 for III-V InGaAs/InAs at $\Gamma$ valley, and 6 for Si at $\Delta$ valley. For $C_{\text{depth}}$, the electron wave-function depth is roughly located at the middle of the quantum well channel. Unlike $C_{\text{ox}}$ and $C_{\text{depth}}$ of which the physical meanings are straightforward, $C_{\text{DOS}}$ is only significant for III-V channels because III-V materials have smaller electron effective mass, lower density of states, and lower band degeneracy. The density-of-state capacitance depends on the relative position of Fermi level ($E_{\text{f}}$) and the first sub-band energy ($E_1$). At a non-degenerate case ($E_1 - E_{\text{f}} > 3kT$), $C_{DOS}$ is $\frac{q^2 m^*}{2\pi\hbar^2} \exp(\frac{E_{\text{f}} - E_1}{kT})$. At a degenerate case ($E_{\text{f}} - E_1 > 3kT$), $C_{DOS}$ is equal to $\frac{q^2 m^*}{2\pi\hbar^2}$.

On the other hand, the injection velocity is determined by the thermal velocity times a correcting factor from Fermi-Dirac integral as shown in Eq. 2.5.

$$v_{\text{inj}} = \sqrt{\frac{2kT}{\pi m^*}} \frac{F_{1/2}(\frac{E_{\text{f}} - E_1}{kT})}{F_0(\frac{E_{\text{f}} - E_1}{kT})} \tag{2.5}$$

where $F_{1/2}$ and $F_0$ are Fermi-Dirac integral of 1/2 order and zero order, respectively. The injection velocity is independent of lateral electric field and the scattering parameters, and only determined by the effective mass and Fermi level position. At a non-degenerate case, the injection velocity is the same as thermal velocity $\sqrt{\frac{2kT}{\pi m^*}}$. At a degenerate case, the injection velocity is $\frac{4}{3\pi}\sqrt{\frac{2q(E_{\text{f}} - E_1)}{m^*}}$.

Given that $E_{\text{f}} - E_1$ can be expressed in terms of ($V_{\text{GS}} - V_{\text{th}}$),

$$\frac{E_{\text{f}} - E_1}{q} = \frac{C_{\text{EET}}}{C_{\text{EET}} + C_{\text{DOS}}}(V_{\text{GS}} - V_{\text{th}}) \tag{2.6}$$

where $C_{\text{EET}} = \frac{C_{\text{ox}} C_{\text{depth}}}{C_{\text{ox}} + C_{\text{depth}}}$ is the equivalent electrostatic capacitance. Then in combination of all the equations from 2.1 to 2.6, the ballistic current can be derived as below.

$$J_{\text{ballistic}} = q \frac{C_{\text{EET}} \cdot C_{\text{DOS}}}{C_{\text{EET}} + C_{\text{DOS}}} (V_{\text{GS}} - V_{\text{th}}) v_{\text{inj}} \tag{2.7}$$

At a degenerate case, $J_{\text{ballistic}} \backsim K(V_{\text{GS}} - V_{\text{th}})^{1.5}$, where K is a function of $C_{\text{EET}}$ and $m^*$. Unlike long channel MOSFETs where the transistors operate under drift-diffusion limits, the saturation current is proportional to $J \backsim (V_{\text{GS}} - V_{\text{th}})^2$.

### 2.1.2 Ballistic Si and III-V MOSFETs

Given Eq. 2.7, the ballistic current is determined by electron effetive mass, the total gate-to-channel capacitance, and the relative position of $E_{\text{f}} - E_1$ (or $V_{\text{GS}} - V_{\text{th}}$). Using this equation, we can calculate the ballistic current as a function of effective electrostatic thickness (EET) and electron effective mass as shown in Fig. 2.2 [4]. In Fig. 2.2, there is an optimal channel effective mass for a given EET. The electron effective mass less than the optimal effective mass suffers from density of state bottleneck, while the effective mass larger than the optimal effective mass decreases the injection velocity. Given that $g_{\text{v}}$ is 1 for III-V and 2 for ultra-thin Si channel (only $\triangle_2$ is occupied while $\triangle_4$ is emptied because of quantum confinement in thin channels), if EET is smaller than 0.5 nm (100) Si MOSFETs will outperform (100) III-V InGaAs MOSFETs [4]. However, such highly scaled EET is extremely challenging because thin gate dielectrics cause large gate leakage and reliability issues. Ultra-thin channels also result in large
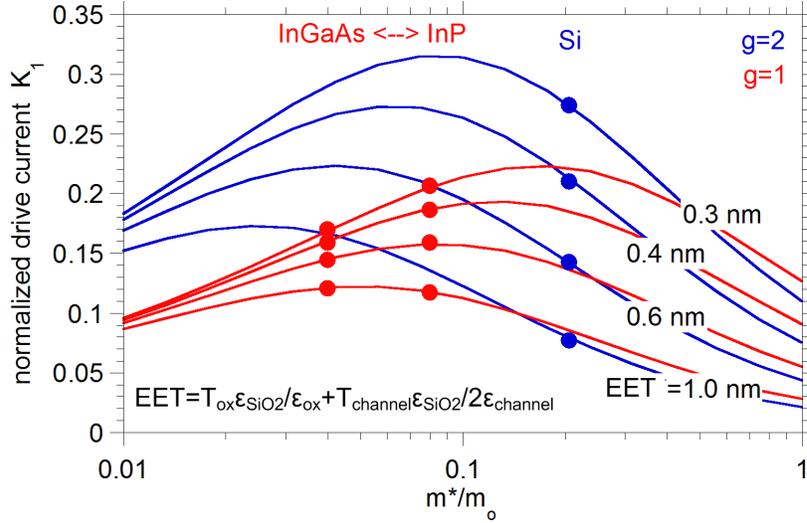
Figure 2.2: MOSFET normalized drive current for ballistic III-V and Si MOS-FETs [4].

threshold voltage variation because of quantum confinement. If EET is unscalable and larger than 0.5 nm, theoretically III-V InGaAs MOSFETs have the capability to exceed Si MOSFETs and achieve higher ballistic current.

## 2.2   Practical MOSFETs design considerations

In this section, we will discuss the practical MOSFET design. The previous section have shown the ideal ballistic current for III-V MOSFETs. However, in reality the MOSFET performance is strongly affected by the parasitic resistance and parasitic capacitance. As gate lengths decrease, deleterious short channel effects caused by degraded 2-D electrostatics significantly affect the MOSFET characteristics. For example, a typical MOSFET transfer characteristic is shown
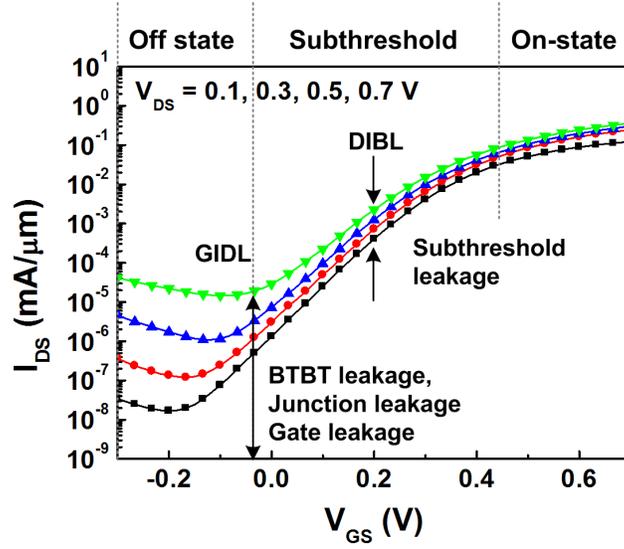
Figure 2.3: A typical MOSFET transfer characteristic, showing on-state region, subthreshold region, and off-state region.

in Fig. 2.3. The $I_{\text{DS}}$-$V_{\text{GS}}$ curves can be divided into three regions, including on-state current, subthreshold leakage, and off-state leakage floor. We will define the key figures of merit for MOSFET operations in these three regions, and discuss the practical design considerations to improve MOSFET performance in many important aspects for logic applications.

## 2.2.1 On-state performance

In section 2.1, it was assumed that the source/drain regions are perfectly conductive with zero resistance ($R_{\text{S}} = R_{\text{D}} = 0$) for a MOSFET. However, in reality, the source/drain regions have finite series resistance from the source/drain layers ($R_{\text{access}}$) and the source/drain metal contact ($R_{\text{contact}}$), as shown Fig. 2.4. At long gate lengths, this parasitic source/drain resistance ($R_{\text{SD}} = R_{\text{S}} + R_{\text{D}}$) is
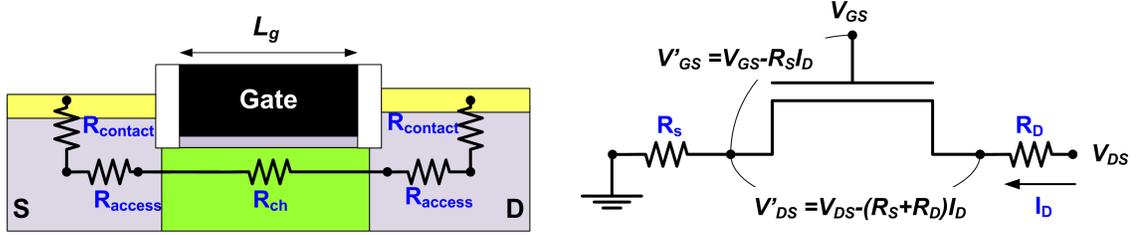
Figure 2.4: (a) The series resistance in MOSFETs. (b) The circuit diagram of MOSFETs with series resistance.

much smaller than channel resistance ($R_{ch}$), and thus negligible. But at small gate lengths where the channel resistance is small, the source/drain parasitic resistance becomes dominant in total resistance of MOSFETs, and significantly degrades the on-state performance if $R_{SD}$ is too high. Fig. 2.4 shows the parasitic source/drain resistance in MOSFETs, and the corresponding circuit diagram.

The on-state resistance ($R_{on}$) of a MOSFET can be extracted at the linear region of the MOSFET output characteristic. $R_{on}$ is defined as Eq. 2.8 and consists of $R_S$, $R_D$ and $R_{ch}$.

$$R_{on} = \frac{V_{DS}}{I_{DS}}|_{V_{DS}\rightarrow 0} = R_S + R_D + R_{ch} \tag{2.8}$$

The voltage drops across $R_S$ reduces effective $V_{GS}$ by $I_D R_S$, thereby reducing charge density in the channel and degrading the extrinsic transconductance.

$$g_m = \frac{dI_{DS}}{dV_{GS}}|_{V_{DS}=constant} = \frac{g_{m,i}}{1 + g_{m,i}R_S} \tag{2.9}$$

where $g_m$ and $g_{m,i}$ are extrinsic and intrinsic transconductance.

As the gate lengths scale beyond sub-10-nm nodes, the source/drain contact pitch must be scaled down simultaneously to continue area scaling and enable

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higher transistor density. However, the source-drain pitch does not scale proportionately to the gate length because a smaller contact area dramatically increases the contact/resistance ($R_{\text{contact}}$). High contact resistance makes it difficult to further scale the transistor while still maintain high on-state performance. From International Technology Roadmap for Semiconductor (ITRS), the specific contact resistivity at source/drain must be smaller than $5 \times 10^{-9}$ $\Omega \cdot cm^2$ at 10 nm technology node [5]. High contact resistance from scaled ohmic contact is therefore the most critical issue that limits the device performance of nanoscale transistors.

In addition to parasitic source/drain resistance, the oxide/semiconductor interface traps have the considerable influence on MOSFET operations. The interface traps could be filled by channel electrons when the Fermi level is raised across the trap energy levels with increasing $V_{\text{G}}$ . The charges filled in the interface traps ($Q_{\text{it}}$) behave like an interface-trap capacitance ($C_{\text{it}}$) in parallel to the semiconductor capacitance. Thus, $C_{\text{it}}$ can be defined as Eq. 2.10.

$$C_{\text{it}}(\psi_{\text{s}}) = \frac{dQ_{\text{it}}}{d\psi_{\text{s}}} = q^2 D_{\text{it}} \tag{2.10}$$

where $\psi_{\text{s}}$ is the channel surface potential, and $D_{\text{it}}$ is the interface trap density.

The charges filled in the interface traps can not contribute to the source-drain current. If the trap density is too high, the Fermi level can be pinned at the energy level of interface traps, reducing the gate control on the channel potential. On the other hand, the interface charges give rise to large Coulomb scattering with channel electrons, thus reducing effective channel mobility and degrading on-state current and transconductance. As a consequence, to deliver high drive current, a high quality gate dielectric with low interface trap density on the semiconductor

channel is indispensable for any kind of MOSFETs.

## 2.2.2  Electrostatics and subthreshold characteristics

The current of an ideal MOSFET is controlled by the position of top-of-barrier in the channel. The top-of-barrier is only modulated by the gate bias, as described in Fig. 2.1(a). However, this is only true when the gate length is sufficiently long as compared to the depletion width of drain-channel junctions (The depletion of drain-channel junction is larger than source-channel junction due to large reverse bias). As gate lengths decrease, short channel effects (SCE) exacerbate and the depletion region of drain-channel junction encroaches into the channel region. The lateral electric field penetration into the channel reduces the height of the top-of-barrier and lowers the MOSFET threshold voltage. Therefore, the threshold voltage decreases with increasing drain bias and decreasing gate lengths. This phenomenon is called drain-induced barrier lowering (DIBL) and $V_t$ roll-off. The effect of DIBL can be seen as a capacitance coupling ($C_{\mathrm{gd}}$) between the drain terminal and the channel surface potential, as illustrated in Fig. 2.5. To characterize DIBL, it is usually defined as Eq. 2.11.

$$DIBL = \frac{V_{\mathrm{t,sat}} - V_{\mathrm{t,lin}}}{V_{\mathrm{D,sat}} - V_{\mathrm{D,lin}}} \tag{2.11}$$

In addition to DIBL, the other signature of short channel effects is the increased subthreshold swing. The subthreshold swing is defined as the following equation.

$$SS = \frac{dV_{\mathrm{GS}}}{d \log I_{\mathrm{D}}} \Big|_{\mathrm{V_{DS}=constant}} = \left(\frac{dV_{\mathrm{GS}}}{d\psi_{\mathrm{s}}}\right)\left(\frac{d\psi_{\mathrm{s}}}{d \log I_{\mathrm{D}}}\right) = m * n \tag{2.12}$$
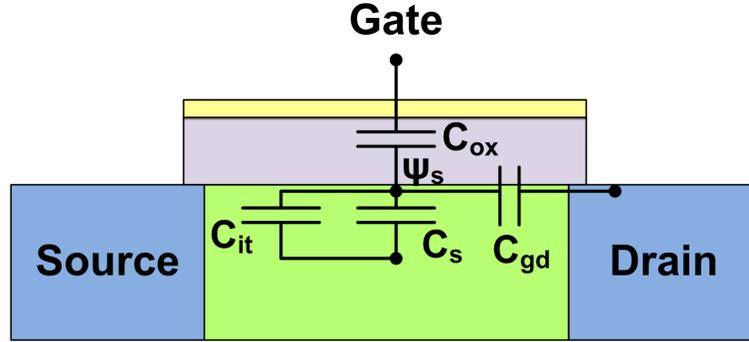
Figure 2.5: The equivalent circuit diagram for the capacitances that are connected to the channel surface potential.

where $\psi_s$ is the channel surface potential. $m = \frac{dV_{GS}}{d\psi_s}$ is the corresponding change of surface potential with the change of the gate bias. Given that the transport of MOSFET current is controlled by a thermionic current and $I_D \propto \exp\frac{q\psi_s}{kT}$, $n = \frac{d\psi_s}{d\log I_D} = (\ln 10)(\frac{kT}{q})$. Therefore, assume that at subthreshold region the gate voltage drop entirely falls on the semiconductor channels, then $m = 1$ and the ideal subthreshold swing $SS = (\ln 10)(\frac{kT}{q}) = 60$ mV/dec. at 300 K. In practice, the subthreshold swing is affected by the presence of interface traps ($C_{it}$) and two dimensional (2-D) electrostatics ($C_{gd}$). With the presence of oxide/semiconductor interface traps, the subthreshold swing is degraded. When the Fermi level (or surface potential) is modulated by the gate bias in the subthreshold region, the interface traps having trap energy in the channel band-gap could be occupied or emptied, depending on the relative position of the Fermi level and the trap energy level. These interface traps act as a parallel capacitance ($C_{it}$) with the semiconductor capacitance ($C_s$). Therefore, the subthreshold swing with the consideration for the interface traps is described as,

$$SS = \frac{dV_{\text{GS}}}{d \log I_{\text{D}}} = (60 \frac{mV}{dec.})(\frac{C_{\text{ox}} + C_{\text{s}} + C_{\text{it}}}{C_{\text{ox}}}) \qquad (2.13)$$

For a fully depleted ultra-thin-body MOSFET, $C_{\text{s}}$ is negligible at subthreshold region, so $SS = (60 \frac{mV}{dec.})(\frac{C_{\text{ox}} + C_{\text{it}}}{C_{\text{ox}}})$. For long gate length devices, the subthreshold swing reflects the interface trap density between gate dielectrics and semiconductor channels, thereby being an important indicator to evaluate the dielectric quality. As gate lengths become smaller, the subthreshold swing is not only affected by the interface trap density ($C_{\text{it}}$) but also altered by 2-D electrostatics ($C_{\text{gd}}$). The $C_{\text{gd}}$ increases with the decrement of gate lengths so that the channel surface potential is also modulated by the drain bias through $C_{\text{gd}}$, as illustrated in Fig. 2.5. Therefore, the subthreshold swing deteriorates as the gate length is made smaller.

One simple device parameter to analyze the 2-D electrostatics in MOSFETs is the natural length ($\lambda$), as shown in Eq. 2.14 [6].

$$\lambda = \sqrt{\frac{\epsilon_{\text{ch}}}{N \epsilon_{\text{ox}}} t_{\text{ox}} t_{\text{ch}}} \qquad (2.14)$$

where N is the number of the gate. The natural length depends on the device structure, and is smaller for FinFETs or double gate devices. In general, the physical gate length ($L_g$) should be larger than $6\lambda$ to mitigate short channel effects [7]. Note that because III-V channels have larger permittivity with the resultant larger natural length, III-V MOSFETs have worse electrostatics as compared to Si MOSFETs at the same channel thickness, oxide thickness, and oxide materials.

### 2.2.3   Off-state leakage: band-to-band tunneling

For VLSI logic circuits, MOSFETs must deliver high on-state current as well as low leakage, particularly for low standby power mobile electronics. Unfortunately, the off-state leakage increases quickly as gate lengths reduced and becomes the main battlefield for continuous device scaling. Fig. 2.6 shows the leakage paths in a MOSFET, including (1) subthreshold leakage ($I_{sub}$), (2) gate leakage ($I_G$), (3) drain-channel junction leakage ($I_{junc}$), (4) gate-induced drain leakage ($I_{GIDL}$), (5) punch-though leakage ($I_{punch-through}$) and (6) direct source-drain tunneling leakage ($I_{S-Dtunneling}$) [8,9]. For an ideal MOSFET, the off-state leakage is limited by subthreshold leakage (1) and can be made smaller by simply adjusting the threshold voltage. However, in practice, at zero or negative gate bias the off-state leakage might begin to saturate at a certain level, as shown in Fig. 2.3. This saturated off-state leakage floor could arise from the gate leakage or the band-to-band tunneling leakage such as $I_{junc}$ and $I_{GIDL}$. To remedy the gate leakage, the high-k dielectric layers have been implemented to mitigate the gate leakage ($I_G$) instead of aggressive scaling of oxide physical thickness [10]. The junction leakage ($I_{junc}$) and GIDL ($I_{GIDL}$) can be optimized by careful junction engineering in the source/drain region using ion implantation technique, e.g. lightly-doped drain (LDD) [11, 12]. The punch-through leakage ($I_{punch-through}$) can be mitigated by super steep retrograde wells, halo implantation, or using ultra-thin body SOI or FinFETs [8,13]. For devices with extremely short gate lengths, the direct source-drain tunneling leakage ($I_{S-Dtunneling}$) might occur and could be more serious for III-V MOSFETs due to smaller tunneling effective mass [14,15]. Detailed mechanisms for each leakage path and the possible solutions can be found in [8,9].
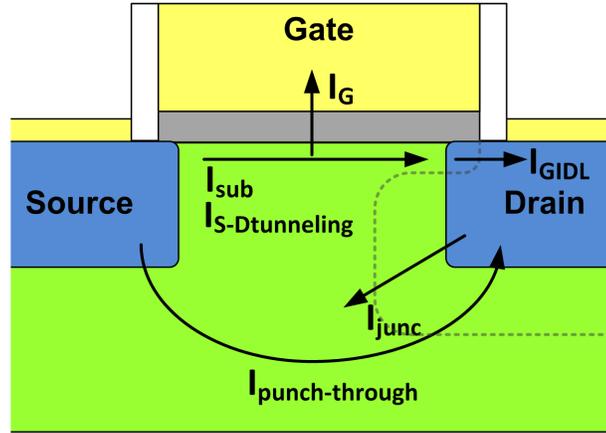
Figure 2.6: The possible leakage paths in nanoscale MOSFETs.

In this subsection, we will concentrate on the band-to-band tunneling (BTBT) related leakage.

Since high mobility channels have smaller band-gap energy, off-state leakage currents related to band-to-band tunneling are dominant for III-V and Ge channel MOSFETs [16]. BTBT occurs at the concentrated electric filed region such as drain-channel junction ($I_{junc}$), or the gate-drain overlap region ($I_{GIDL}$). In a typical MOSFET operation, the drain (N-type doped) and the channel (P-type doped well) junction is under large reverse-bias. The junction leakage could arise from the minority carrier injection from the depletion edges, or the carrier generation in the depletion region, or the avalanche current near drain. Besides the above-mentioned mechanisms, if the drain and channel are heavily doped, the depletion width of the drain/channel junction becomes very narrow, leading to electron tunneling from the valence band of the p-doped channel to the conduction band of the n-doped drain. Given that III-V materials have a smaller tunneling mass and a smaller band-gap with a resultant narrower tunneling width, the strong voltage
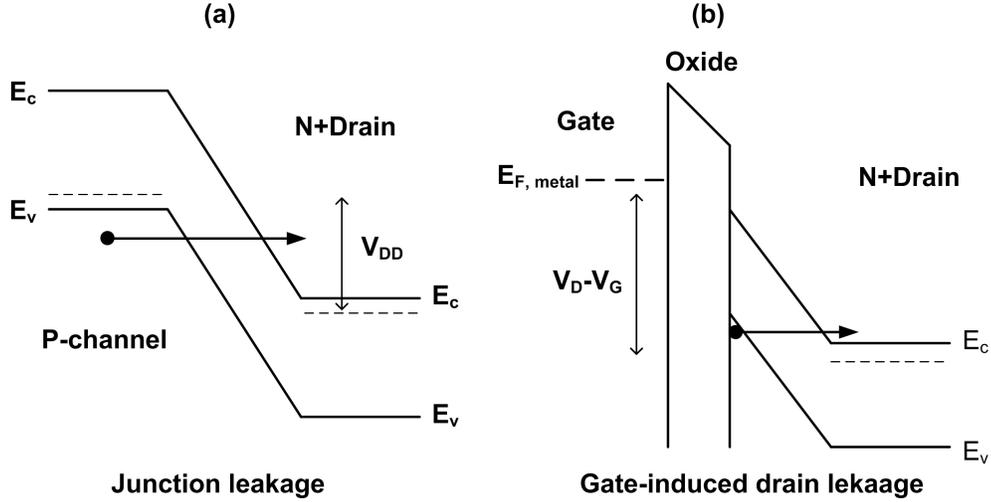
Figure 2.7: (a) The band profile of drain-to-channel junction under reverse bias. (b) The band profile at the gate-drain overlap region at large negative $V_G$ and positive $V_D$.

drop in drain-channel junction could potentially give rise to large band-to-band tunneling, as illustrated in Fig. 2.7(a). The tunneling rate (direct tunneling without a phonon) can be expressed by Eq. 2.15 [17].

$$G_{\mathrm{BTBT}} = AE \exp(-\frac{B}{E}) \tag{2.15}$$

where $E$ represents the electric field, $A \propto \sqrt{\frac{m^*}{E_{\mathrm{G}}}}$ and $B \propto (m^*)^{1/2} E_{\mathrm{G}}^{3/2}$ are the coefficients and depend on the effective mass and the band-gap. Obviously, band-to-band tunneling is highly dependent on material band-gap, and small band-gap channels are more vulnerable to large tunneling leakage.

On the other hand, gate-induce-drain leakage (GIDL) is the other type of band-to-band tunneling leakage. Unlike junction leakage where BTBT occurs at the large drain-channel junction, GIDL occurs at the local area of the gate-drain overlap (surface band-to-band tunneling), as shown in Fig. 2.6. Because at

negative $V_G$ and positive $V_D$ the electric field is crowded at the gate-drain overlap region, the field crowding can cause large surface band bending, leading to large band-to-band tunneling or trap-assisted tunneling (TAT) [18] as shown in Fig. 2.7(b).

There are two important comments for these two BTBT related leakage. First, because the junction leakage path is away from the gate terminal, the BTBT leakage from the drain-channel junction is less sensitive to $V_G$. However, for GIDL where BTBT occurs at the surface of gate-drain overlap region, the GIDL increases as applying larger negative gate bias. Therefore, examining the behavior of BTBT leakage floor with respect to $V_{GS}$ might help differentiate the location of the BTBT leakage path.

Second, it was noticed that the BTBT leakage current increases with the decrement of the gate length because of lateral bipolar effects [19, 20]. When BTBT occurs near drain, the generated holes will either flow to the source side or to the substrates. Because the quantum well MOSFETs have the hole confinement from the semiconductor back barriers which prevent the hole extraction to the substrates, a large amount of holes could stay in the quantum wells and reduce the channel potential. The decrease on channel potential acts as a forward-bias on the source-channel junction, thus reducing the source-to-channel barrier and increasing the leakage current. In consequence, the BTBT leakage $I_{BTBT}$ can be amplified by a current gain ($\beta$) so that the total leakage is $(\beta + 1)I_{BTBT}$, as illustrated in Fig. 2.8. This phenomenon is called lateral bipolar effects in MOSFETs.
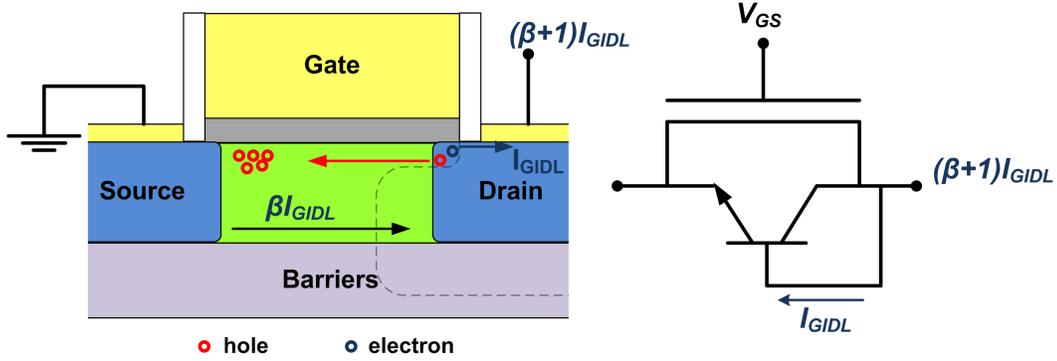
Figure 2.8: A lateral bipolar effect in quantum well MOSFETs. The accumulation of holes in quantum well channels decreases the channel potential, forward-biasing the source-channel barriers and increasing leakage.

## 2.3    Summary

In this chapter, we reviewed the design considerations for ideal ballistic MOS-FETs and the practical MOSFETs. To attain high on-state performance of ballistic MOSFETs, the channel effective mass must be carefully selected according to the given effective electrostatics thickness. Optimized channel effective mass could deliver the highest ballistic current with the best balance between density of state and the injection velocity.

In practice, MOSFETs performance is significantly affected by the parasitic resistance, parasitic capacitance, 2-D electrostatics, and the off-state leakage. The parasitic source/drain resistance must be minimized to improve on-current and extrinsic transconductance. The oxide/semiconductor interface traps must be minimized to improve on-state performance as well as subthreshold swing. The transistor must have good 2-D electrostatics in that the natural length is sufficiently small as compared to the gate length. The minimum off-state leakage current in MOSFETs is usually limited by band-to-band tunneling leakage (junc-

tion leakage or gate-induced drain leakage) as well as the gate leakage if the oxide is too thin. Especially for III-V high mobility channels, lower band-gap energy gives rise to larger band-to-band tunneling leakage. As the device gate length now approaches sub-10-nm, how to suppress the off-state leakage current for a highly scaled III-V MOSFET to a sufficiently low level is the most critical challenge. This would eventually determine if III-V MOSFETs are suitable for VLSI CMOS logic applications.

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# Chapter 3

# Barrier Engineering: Wide Band-gap AlAsSb Barriers

Since 22 nm technology node, Si industries have introduced the new device architecture such as ultra-thin body (UTB) silicon-on-insulator (SOI) [1] or Fin-FETs [2] into CMOS logic technology. The UTB-SOI or FinFETs improve gate control on the channel, mitigate short channel effects, and reduce the leakage currents [3]. Because the leakage currents of MOSFETs not only flow at the oxide/channel interface but also occur in the deeper semiconductor regions, the deep leakage current can not be properly turned off because the leakage path is far below the channel and has inferior gate control. By introducing a buried oxide (BOX) beneath the Si channel, the buried oxide blocks the deep leakage path. In contrast, FinFETs or trigate MOSFETs suppress the deep leakage current by making a thin Si fin channel wrapped around by the gate terminal. Both UTB-SOI and FinFETs eliminate the deep leakage path by only allowing the current to flow in the semiconductor channels very close to the gate. Making thinner body or shrinking the fin width allows better gate control and reduces the leakage currents.

For III-V MOSFETs, III-V-on-insulator (III-V-O-I) or III-V FinFETs can also be adopted to reduce the leakage currents. However, III-V heterojunctions provide a powerful design knob of III-V MOSFETs. For III-V planar quantum well MOSFETs, the channel can be either bounded by semiconductor barriers on the both sides (buried-channel MOSFETs) or bounded by the top dielectric layer and the bottom semiconductor barrier (surface-channel MOSFETs). Both structures are similar to III-V-O-I devices, while the buried oxide is now replaced by the wide band-gap semiconductor bottom barrier. The wide band-gap barriers have higher conduction band energy than III-V channels, which effectively

confines the electrons in the channel and blocks the deep leakage path in the buffer layers. Unlike III-V-O-I devices that require a complicated wafer bonding process, the wide-gap semiconductor barriers can be easily grown by epitaxial growth techniques, offering smooth interfaces, a low trap density and superior crystalline quality. Conventionally, for InGaAs material system, $In_{0.53}Ga_{0.47}As/InP$ and $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ are two typical lattice-matched heterojunctions. InP barriers and InAlAs barriers provide 0.2 eV and 0.5 eV conduction band offset (CBO) to $In_{0.53}Ga_{0.47}As$ channels, respectively [4]. However, for highly scaled III-V MOSFETs, the channel thickness must be scaled down in proportional to gate lengths in order to maintain strong gate control on channel electrostatic. Reducing the channel thickness increases the sub-band energy, leading to larger electron wave-function penetration into the barrier layers and creating a parallel conduction path. The increased sub-band energy also reduces the maximum allowable sheet charge density in the channel. As gate voltage increases, the Fermi level could reach the conduction band energy of the barrier layer, and begin to modulate the parasitic charges. This reduces carrier mobility and modulation efficiency [5]. Therefore, to mitigate these problems, a wider band-gap barrier material with higher conduction band offset to InGaAs channels is important for realizing ultra-thin-body InGaAs MOSFETs at sub-10-nm nodes.

$AlAs_{0.56}Sb_{0.44}$, lattice-matched to InP, is therefore proposed here as a novel barrier material for $In_{0.53}Ga_{0.47}As$ channel MOSFETs. $AlAs_{0.56}Sb_{0.44}$ provides higher conduction band offset to $In_{0.53}Ga_{0.47}As$ than that of $In_{0.52}Al_{0.48}As$ ($X_{AlAsSb} - \Gamma_{InGaAs} \sim 1.0$ eV and $\Gamma_{AlAsSb} - \Gamma_{InGaAs} \sim 1.6$ eV) [6, 7]. In this chapter, we start from the development of AlAsSb layers using MBE growth, and then inves-

tigate the electron transport in InGaAs/AlAsSb ultra-thin quantum wells [8]. We also compare the electron mobility in InGaAs/AlAsSb heterostructure to InGaAs/InAlAs heterostructure [9]. Last, InGaAs channel MOSFETs with an AlAsSb bottom confinement layer were demonstrated, and compared with In- AlAs barriers [10]. Two approaches to reduce barrier leakage are proposed here, including AlAsSb wide band-gap barriers and p-doped InAlAs barriers.

## 3.1    MBE growth of AlAsSb barriers

### 3.1.1    AlAsSb lattice-matched to InP

$AlAs_{0.56}Sb_{0.44}$ materials lattice-matched to InP were developed on Veeco Gen II solid source molecular beam epitaxy using $As_2$ and $Sb_2$ from valved crackers. The substrates were epi-ready, semi-insulating InP (001) substrates. To grow the mixed group-V $AlAs_{0.56}Sb_{0.44}$ material, $As_2$ and $Sb_2$ flux must be carefully cali- brated in order to control the composition of AlAsSb layer. Two growth conditions were developed with different V/III ratio. For $AlAs_{0.56}Sb_{0.44}$ lattice matched to InP, the beam equivalent pressure (BEP) ratio of $As_2$ to $Sb_2$ is around 5.1 for the total $(As_2+Sb_2)$/Al ratio~22 and $As_2$/$Sb_2$~1.8 for total $(As_2+Sb_2)$/Al~42. All the AlAsSb epitaxial layers were grown at 490 °C measured by infrared pyrometer and the growth rate was 0.24 $\mu$m/hr. During the growth of AlAsSb, the reflection high energy electron diffraction (RHEED) shows a $(1 \times 3)$ surface reconstruction, indicating a Sb-rich growth condition. Fig. 3.1 shows the X-ray diffraction mea- surements of $AlAs_{0.56}Sb_{0.44}$ epitaxial layers grown at two different conditions. It
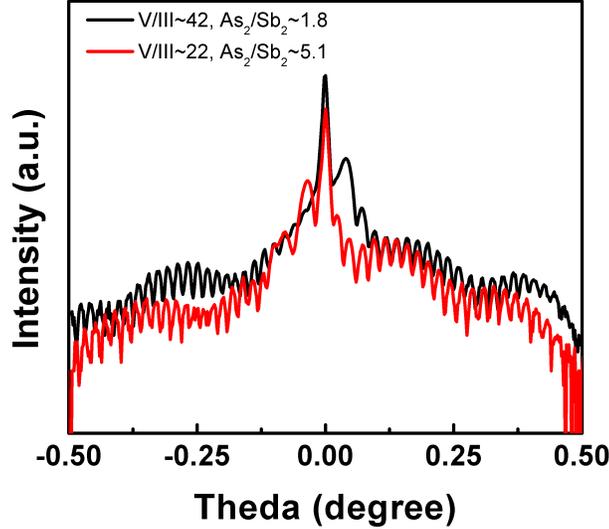
Figure 3.1: X-ray diffraction of n-doped $AlAs_{0.56}Sb_{0.44}$ layers grown at different V/III ratio. The beam equivalent pressure ratio of $As_2$ to $Sb_2$ is around 5.1 for the total $(As_2+Sb_2)/Al$ ratio~22 and $As_2/Sb_2$~1.8 for total $(As_2+Sb_2)/Al$~42.

could be observed that increasing V/III ratio broadens the diffraction peak, indicating the degradation of crystalline quality.

## 3.1.2    N-type doping in AlAsSb layers

Silicon (sample A series) and tellurium (sample B series) were also investigated as n-type dopant sources for $AlAs_{0.56}Sb_{0.44}$ layers. Table 3.1 summarizes the growth conditions and Hall measurements for all the n-doped AlAsSb samples. From X-ray diffraction measurements, the lattice mismatch between AlAsSb layers and InP substrates is less than $4\times10^{-3}$ for all the n-doped samples.

Table 3.1 shows the electrical properties of Si-doped (Sample A series) and Te-doped (Sample B series) $AlAs_{0.56}Sb_{0.44}$ layers. Te acts as an effective dopant for

39

| Sample | Total V/III ratio | As$_2$/Sb$_2$ ratio | Si or Te cell temperature (°C) | Type | Active carrier concentration ($10^{17}$ cm$^{-3}$) | Hall mobility (cm$^2$/V· s ) |
|--------|-------------------|---------------------|-------------------------------|------|---------------------------------------------------|------------------------------|
| A1     | 22                | 5.1                 | 1300                          | n    | 4.27                                              | 702                          |
| A2     | 22                | 5.1                 | 1360                          | n    | 2.95                                              | 951                          |
| A3     | 42                | 1.8                 | 1360                          | n    | 4.89                                              | 756                          |
| B1     | 22                | 5.1                 | 550                           | n    | 0.66                                              | 252                          |
| B2     | 22                | 5.1                 | 600                           | n    | 5.30                                              | 211                          |
| B3     | 22                | 5.1                 | 625                           | n    | 8.59                                              | 142                          |
| B4     | 22                | 5.1                 | 650                           | n    | 15.6                                              | 338                          |
| B5     | 22                | 5.1                 | 675                           | n    | 20.3                                              | 270                          |

Table 3.1: The growth conditions and Hall measurements for Si-doped (sample A series) and Te-doped (sample B series) AlAs$_{0.56}$Sb$_{0.44}$ layers.

AlAsSb layers, while Si is not a robust n-type dopant. Similar to most Sb-based materials, the Te-doped AlAsSb samples show a limited electron concentration of about $2 \times 10^{18}$ cm$^{-3}$ under current growth conditions. In comparison, the active carrier concentration of Si-doped AlAsSb samples is around low-$10^{17}$ cm$^{-3}$, one order lower than that of Te-doped AlAsSb. Si is known to exhibit amphoteric doping behavior in III-V semiconductors, being a donor in AlAs while being an acceptor in AlSb [11,12]. This amphoteric nature of Si might cause dopant instability in AlAsSb layers, rendering it unsuitable for practical device applications.

## 3.2   Electron transport in InGaAs/AlAsSb and InGaAs/InAlAs heterostructures

The potential for increased on-state current using InGaAs channels relies on the superior transport properties of two dimensional electron gas (2DEG), which is manifested by large carrier density and high carrier velocity. AlAsSb barri-

ers offer larger conduction band offset to InGaAs channels, allowing higher carrier density in quantum wells without loss of quantum confinement. However, although the electron transport properties of lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ 2DEGs have been reported extensively in the literature [13–15], there are only a few reports of electron transport in the lattice-matched $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ material system [16]. Detailed investigation of this system is necessary if AlAsSb barriers are to be used in highly scaled InGaAs-channel MOSFETs. In this section, we investigate electron transport in $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ ultra-thin quantum well 2DEGs. InGaAs/AlAsSb 2DEGs with varying InGaAs quantum well thickness were grown and their properties were compared with that of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ 2DEGs [9].

### 3.2.1  InGaAs quantum well 2DEG structure

The lattice-matched $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ 2DEG is shown in Fig. 3.2 The InGaAs/AlAsSb 2DEG structures consist of a semi-insulating InP substrate, a 270 nm unintentionally doped (U.I.D.) InAlAs buffer layer, a 30 nm U.I.D. AlAsSb bottom barrier, a U.I.D. InGaAs channel (3, 5, 7.5, or 10 nm thickness), a 3 nm U.I.D. AlAsSb spacer layer, a 3 nm $1.3 \times 10^{19}$ cm$^{-3}$ Si-doped InAlAs modulation-doped layer, a 15 nm U.I.D. AlAsSb top barrier and a 5 nm U.I.D. InGaAs capping layer. For comparison, similar $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ 2DEGs were also grown as shown in Fig. 3.2; in these the AlAsSb bottom barrier, the spacer layer, and the top barrier are replaced with U.I.D. InAlAs layers. The unintentionally doped impurity concentrations of InAlAs layers and AlAsSb layers

were estimated to be around $10^{15}$ cm$^{-3}$ and below $10^{15}$ cm$^{-3}$ respectively. All layers were grown at 490 °C, as measured by an infrared pyrometer. The group-V species, As$_2$ and Sb$_2$, provided from As and Sb valved crackers respectively, were used to grow AlAs$_{0.56}$Sb$_{0.44}$ layers with a As/Sb beam equivalent pressure ratio of around 5.1 and a total (As+Sb)/III ratio of around 22. After growing the AlAsSb bottom barrier, the group-III shutters were closed, interrupting growth for 30 seconds. During this interruption, the wafer was exposed to either an As or Sb column-V flux, with the As and Sb beam flux pressure (BEP) around $5.0 \times 10^{-6}$ torr and $1.0 \times 10^{-7}$ torr respectively. After growing the InGaAs channel, the group-III shutters were closed, interrupting growth for 120 seconds. For some samples, during this interruption, the wafer was exposed to an As flux for 90 seconds and subsequently exposed to an Sb flux for 30 seconds. For other samples, the wafer was exposed to an As flux for 120 seconds. During this interruption, the As and Sb BEP were about $5.1 \times 10^{-7}$ torr and $1.0 \times 10^{-7}$ torr respectively.

Fig. 3.2(b) shows the conduction band profile of a 5 nm InGaAs/AlAsSb 2DEG structure simulated by a 1-D self-consistent Schrödinger-Poisson simulation program (BandProfiler provided by Professor William Frensley). The conduction band energy of the AlAsSb barrier is linearly interpolated from the unstrained AlAs and AlSb materials, neglecting the bowing parameter. To measure the carrier concentration and carrier mobility of InGaAs/InAlAs and InGaAs/AlAsSb 2DEGs, the room temperature Hall effect measurements were carried out using van der Pauw technique with DC current at various magnetic field of 0.2, 0.4, 0.6 Tesla. The variations of 2DEG mobility across the wafer were less than 10 percents for all the samples. The temperature-dependent Hall-effect measurements

**(a)**

| 5 nm InGaAs cap | 5 nm InGaAs cap |
| --- | --- |
| 15 nm AlAsSb N.I.D top barrier | 15 nm InAlAs N.I.D top barrier |
| 3 nm Si-doped InAlAs | 3 nm Si-doped InAlAs |
| 3 nm AlAsSb N.I.D spacer | 3 nm InAlAs N.I.D spacer |
| 3,5,7.5,10 nm InGaAs N.I.D well | 3,5,7.5,10 nm InGaAs N.I.D well |
| 30 nm AlAsSb N.I.D bottom barrier | |
| 270 nm InAlAs N.I.D buffer | 300 nm InAlAs N.I.D buffer |
| Semi-insulating InP substrate | Semi-insulating InP substrate |

**(b)**
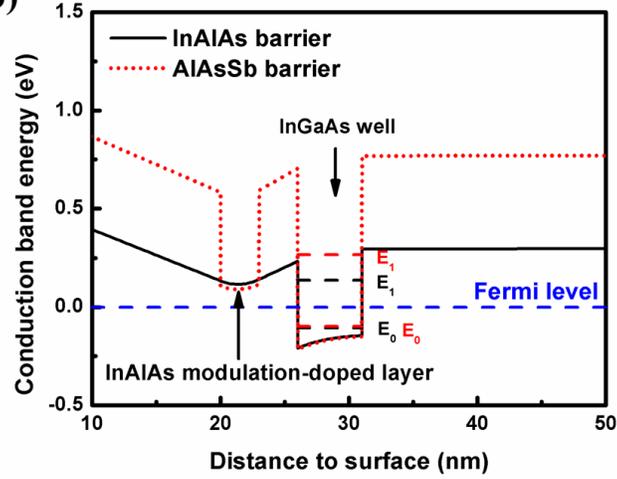


Figure 3.2: (a) The InGaAs/AlAsSb and InGaAs/InAlAs 2DEG quantum well layer structures using modulation-doped InAlAs layers above the well. (b) Simulated conduction band profile for a 5 nm InGaAs well. The dashed lines indicate the Fermi level and the first two bound states band minima within the well.

were measured from 45 K to room temperature in a magnetic field of 0.6 Tesla.

## 3.2.2   Transport scattering model

In this subsection, we describe the electron transport models used to calculate electron mobility in the InGaAs quantum well. At low electric fields, the elec-

tron velocity is proportional to the electron mobility, which is associated with the electron effective mass and the electron scattering time. Scattering mechanisms including acoustic phonon scattering [17], polar optical phonon scattering [18, 19], remote impurity scattering [20], interface roughness scattering [20], and alloy scattering [21] were considered in the calculations. The InGaAs quantum well was modeled with infinite barriers. This approximation is satisfactory because the AlAsSb barriers have a high conduction band offset to InGaAs wells. Further, only intra-valley scattering in the lowest sub-band was included. The inter-subband scattering is negligible since electrons mainly populate the first lowest subband, as seen in Fig. 3.2(b). Electron-electron interaction and nonparabolic conduction band dispersion were not considered in the calculations.

### A. Acoustic phonon scattering

Assuming no intersubband scattering in the quantum well, the scattering time for the acoustic phonon depends on the deformation-potential of the acoustic phonon in the crystal. The scattering time can be expressed as, [17]

$$\frac{1}{\tau_{\mathrm{AC}}} = \frac{3m_{\mathrm{n}}k_{\mathrm{B}}T}{2\hbar^3 L}\frac{D^2}{\rho\mu_{\mathrm{L}}^2} \tag{3.1}$$

where $D$ is the acoustic phonon deformation potential, $\rho$ the InGaAs mass density, $\mu_{\mathrm{L}}$ the longitudinal acoustic phonon velocity, $m_{\mathrm{n}}$ the electron effective mass, $T$ the temperature and $D$ the well thickness.

### B. Polar optical phonon scattering

Considering the electron scattering by the absorption of polar optical phonons in a narrow quantum well, the scattering time is approximated by Price and Ridley [18] [19] as,

$$\frac{1}{\tau_{\mathrm{PO}}} = \frac{e^2 k_0}{8\hbar\kappa^*} \frac{1}{\exp(\frac{\hbar\omega_0}{k_{\mathrm{B}}T}) - 1} \tag{3.2}$$

where $\omega_0$ is the optical phonon frequency, $k_0 = \sqrt{2m_{\mathrm{n}}\omega_0/\hbar}$ the change of electron wave vector by phonon scattering, $(\kappa^*)^{-1} = (\kappa_\infty)^{-1} + (\kappa_0)^{-1}$, and $\kappa_\infty$ and $\kappa_0$ are the high-frequency and low-frequency dielectric constants.

## C. Remote impurity scattering

Following the treatment by A. Gold, [20] considering two dimensional sheet charges from modulation-doped impurities $N_i$ at locations $z_i$ from the bottom boundary of the InGaAs well, the scattering time for remote impurity scattering can be expressed as,

$$\frac{1}{\tau_{\mathrm{IM}}} = \frac{1}{2\pi\hbar E_{\mathrm{f}}} \int\limits_0^{2k_{\mathrm{f}}} \frac{\langle|U_{\mathrm{IM}}|^2\rangle}{\varepsilon(q)^2} \frac{q^2}{(4k_{\mathrm{f}}^2 - q^2)^{1/2}} dq \tag{3.3}$$

where $E_{\mathrm{f}}$ is the Fermi energy, $k_{\mathrm{f}}$ the Fermi wave vector, $N_{\mathrm{s}}$ the 2DEG sheet carrier density, $\varepsilon(q)$ the static dielectric function including screening effect by the two dimensional electron gas, and $\langle|U_{\mathrm{IM}}|^2\rangle$ is the Coulomb scattering potential,

$$\langle|U_{\mathrm{IM}}(q)|^2\rangle = N_{\mathrm{i}}(\frac{e^2}{2\kappa_0 q})^2 F(q, z_{\mathrm{i}})^2 \tag{3.4}$$

$\kappa_0$ is the dielectric constant of the InGaAs well, and the form factor $F(q, z_{\mathrm{i}})$

can be expressed as [20],

$$F(q, z_{\mathrm{i}}) = \frac{8\pi^2}{Lq} \frac{1}{4\pi^2 + L^2 q^2} \frac{1}{2} \exp(-q(z_{\mathrm{i}} - L))[1 - \exp(-qL)] \qquad (3.5)$$

In this calculation, the Thomas-Fermi approximation for two dimensional electron gas was used, and the static dielectric function was approximated as $\varepsilon(q) = 1 + q_{\mathrm{TF}}/q$, where $q_{\mathrm{TF}} = 2/a_{\mathrm{B}}$ and $a_{\mathrm{B}}$ is the Bohr radius.

### D. Interface roughness scattering

Interface roughness scattering is well-known to be the dominant scattering event in thin quantum wells. [22, 23] The interface roughness can be considered as the variation in the well thickness, leading to a broadening subband energy in the quantum well. Again, following the treatment of A. Gold, [20] the interface topology is assumed as a Gaussian fluctuation with the average height $\Delta$ and the correlation length $\Lambda$ expressed as,

$$\langle \Delta(\vec{r}) \Delta(\vec{r'}) \rangle = \Delta^2 \exp(-\frac{|\vec{r} - \vec{r'}|^2}{\Lambda^2}) \qquad (3.6)$$

where we assume that the top and bottom interfaces are described by the same parameters. The scattering potential $\langle |U_{\mathrm{IF}}(q)|^2 \rangle$ of the interface roughness scattering is,

$$\langle |U_{\mathrm{IF}}(q)|^2 \rangle = 2(\frac{4\pi}{L^2})(\frac{\pi}{k_{\mathrm{F}} L})^4 (E_{\mathrm{f}} \Delta \Lambda)^2 \exp(\frac{-q^2 \Lambda^2}{4}) \qquad (3.7)$$

while the momentum relaxation time is,

$$\frac{1}{\tau_{\text{IF}}} = \frac{1}{2\pi\hbar E_{\text{f}}} \int\limits_{0}^{2k_{\text{f}}} \frac{\langle |U_{\text{IF}}|^2 \rangle}{\varepsilon(q)^2} \frac{q^2}{(4k_{\text{f}}^2 - q^2)^{1/2}} dq \qquad (3.8)$$

**E. Alloy scattering**

Given that $\text{In}_x\text{Ga}_{1-x}\text{As}$ is a ternary alloy, alloy scattering caused by the random distribution of group-III elements also significantly affects mobility. [21] For an infinite quantum well, the electron mobility limited by alloy scattering is [21],

$$\mu_{\text{Alloy}} = \frac{128 L e \hbar^3}{27\pi^2 m_{\text{n}}^2 \Omega (1-x) |\Delta U|^2} \qquad (3.9)$$

where $\Omega$ is the volume of the primitive cell, $x$ the alloy composition and $\Delta U$ the alloy scattering potential. It is worth noting that the electron mobility limited by alloy scattering decreases as the well thickness $L$ decreases, and is independent of temperature.

**F. Total mobility**

The total electron mobility contributed by each individual scattering mechanism is determined by Matthiessens rule,

$$\frac{1}{\tau_{\text{total}}} = \frac{1}{\tau_{\text{AC}}} + \frac{1}{\tau_{\text{PO}}} + \frac{1}{\tau_{\text{IM}}} + \frac{1}{\tau_{\text{IF}}} + \frac{1}{\tau_{\text{Alloy}}} \qquad (3.10)$$

with $\mu_{\text{j}} = e\tau_{\text{j}}/m_{\text{n}}$ and $\tau_{\text{j}}$ is the scattering time defined by each scattering mechanism. Table 3.2 summarizes the material parameters used in the calculations. Since we have no experimental measurement of the interface roughness parameters of these 2DEGs samples, we assumed the average height $\Delta$ is 2.93 $\mathring{A}$ (1

| | | |
|---|---|---|
| Electron effective mass density | $m_n$ | $0.041\ m_0$ |
| 2DEG carrier concentration | $N_s$ | $2.4 \times 10^{12}$ cm$^{-2}$ |
| Impurity concentration | $N_i$ | $3.9 \times 10^{12}$ cm$^{-2}$ |
| Deformation potential | D | 9.4 eV |
| Alloy scattering potential | $\Delta U$ | 0.7 eV |
| InGaAs DC dielectric constant | $\kappa_0$ | $13.9\ \varepsilon_0$ |
| InGaAs high frequency dielectric constant | $\kappa_\infty$ | $11.5\ \varepsilon_0$ |
| LO phonon energy of InGaAs | $\omega_0$ | 34.5 eV |
| LA phonon velocity | $\mu_L$ | $4253$ ms$^{(-1)}$ |
| Mass density of InGaAs | $\rho$ | 5690 kg/m$^3$ |
| Interface average height | $\Delta$ | 2.93 Å |
| Interface correlation length | $\Lambda$ | 210 Å |

Table 3.2: Material parameters used in the calculations of the InGaAs/AlAsSb 2DEG mobility.

monolayer) and adjusted the correlation length $\sim 210$ Å to obtain the best fit between calculated and measured mobility of a narrow (3 nm) quantum well. In addition, an alloy scattering potential of 0.7 eV, was determined by a best fit between theory and experiment of the 7.5 nm and 10 nm thick quantum well samples. This value is comparable to that of previously reported InGaAs/InAlAs heterostructures [21, 24, 25].

### 3.2.3   2DEG results and simulation

Fig. 3.3 shows a comparison between calculated and measured temperature-dependent Hall mobility for InGaAs/AlAsSb 2DEGs with 3 nm, 5 nm, 7.5 nm and 10 nm well thickness. The 2DEG carrier concentration for all the samples in Fig. 3.3 is c.a. $2.0 \sim 2.5 \times 10^{12}$ cm$^{-2}$, and is insensitive to temperature, varying by less than $\pm 5$ % between 45 K and 300 K. Noting again that the correlation length has been adjusted to obtain best fit, the theoretical calculations show good agreement

with the experimental data. For thick quantum wells (10 nm and 7.5 nm), the room temperature mobility is dominated by polar optical phonon scattering while the low temperature mobility is primarily dominated by alloy scattering in the channel. In contrast, for a 5 nm thick well, the low temperature mobility is dominated by the combination of interface roughness and alloy scattering, with polar optical phonons also significantly contributing to the net scattering rate at 300 K. Further shrinking the well thickness to 3 nm, the interface roughness scattering becomes dominant at all temperatures.

Fig. 3.4 compares simulation and measurements of 2DEG electron mobility versus InGaAs well thickness at 45 K and 300 K. For thicker wells (L>10 nm), the 2DEG mobility is limited primarily by alloy scattering at 45 K and by polar optical phonon scattering at 300 K. For thinner wells, interface roughness scattering increases and becomes the limiting scattering mechanism for wells thinner than 4 nm. Since the interface roughness scattering is independent of temperature, the room temperature 2DEG mobility for thin wells is also degraded by the strong interface roughness scattering. As seen in Eq. 7, the scattering potential of interface roughness scattering is proportional to the inverse sixth power of the well thickness ($L^{-6}$). Hence, for the thinner wells, the electron mobility decreases dramatically as the well is made thinner.

Fig. 3.5 compares the measured room temperature and low temperature Hall mobility of InGaAs/InAlAs and InGaAs/AlAsSb 2DEGs as a function of well thickness. The 2DEG mobility is found to be comparable for both InAlAs and AlAsSb barriers for thick (10 nm) InGaAs quantum wells. However, upon reducing the quantum well thickness, the 2DEG mobility for both InGaAs/InAlAs

49
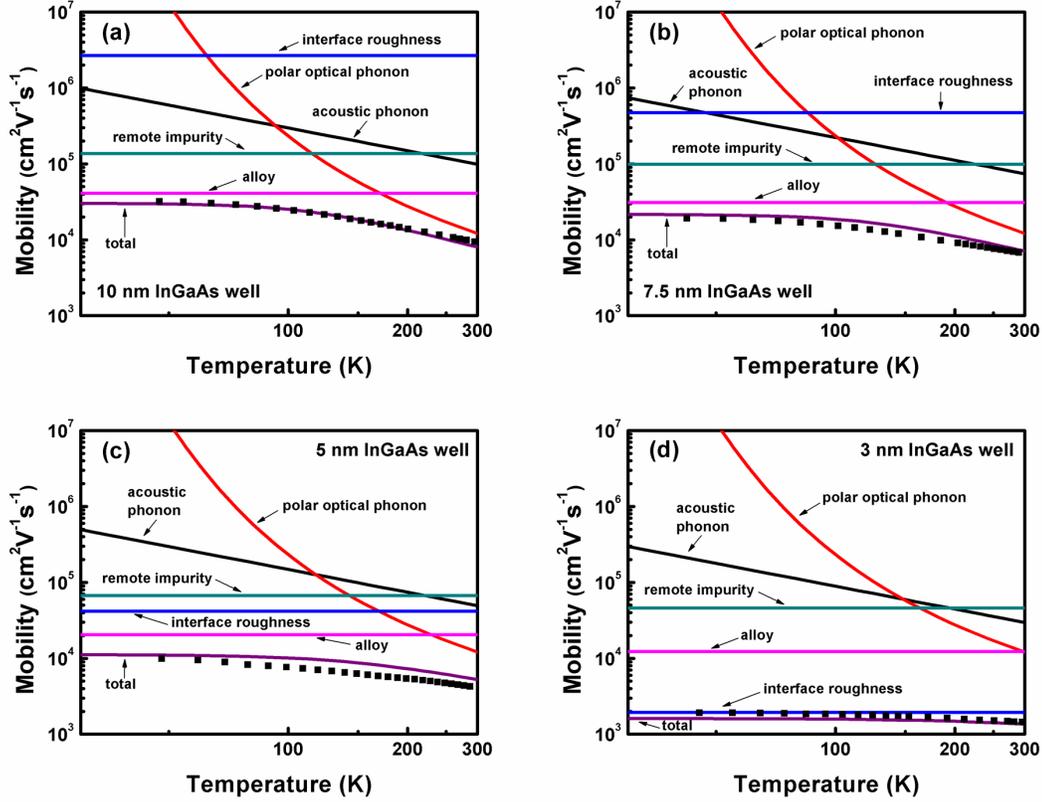
Figure 3.3: Measured temperature-dependent Hall mobilities and the corresponding numerical calculations of mobilities for 10 nm, 7.5 nm, 5 nm, and 3 nm thick InGaAs/AlAsSb 2DEGs. The material parameters used in the calculations are shown in Table 3.2.

and InGaAs/AlAsSb heterostructures decreases significantly, with a particularly strong degradation for the InGaAs/AlAsSb 2DEGs. This result indicates that interface roughness scattering is stronger for InGaAs/AlAsSb interfaces than for InGaAs/InAlAs interfaces. The larger interface roughness scattering of the InGaAs/AlAsSb interfaces could be attributed to two mechanisms: First, the larger conduction band offset at the InGaAs/AlAsSb heterojunction results in a large fluctuation of the bound state energy in the InGaAs well for a given fluctuation in well thickness, leading to stronger intrasubband scattering than for a In-
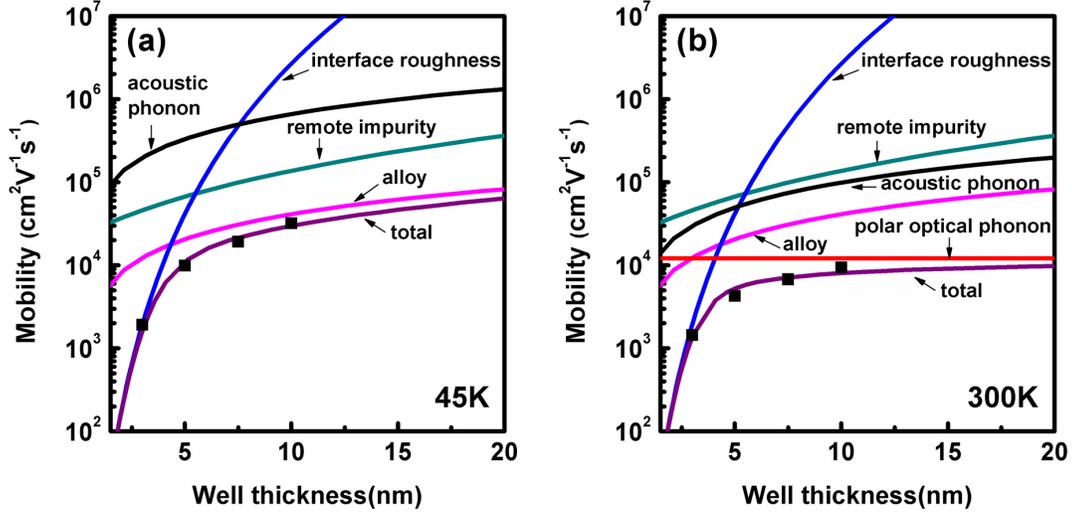
Figure 3.4: Measured and calculated (a) low temperature (45 K) and (b) room temperature (300 K) Hall mobilities of InGaAs/AlAsSb 2DEGs as a function of InGaAs quantum well thickness.

GaAs/InAlAs heterojunction [26]. Second, as reported in Ref. [23,27,28] given the higher aluminum content of an AlAsSb bottom barrier than of an InAlAs bottom barrier, greater surface roughness may arise at this interface either due to the proclivity of high aluminum content surfaces to oxidize [29], or due to impurities in the MBE system's aluminum source [30].

The dependence of mobility on carrier concentration was also investigated. A series of 10 nm thick InGaAs/AlAsSb quantum wells with varying modulation-doped 2D carrier concentrations were grown and characterized. Fig. 3.6 compares measured and calculated room temperature mobility as a function of 2DEG carrier concentration. The 2DEG carrier concentration in the 10 nm InGaAs quantum well is well-controlled by varying the modulation-doped concentration in the barrier (Fig. 3.6), which indicates that the density of defects either in the AlAsSb
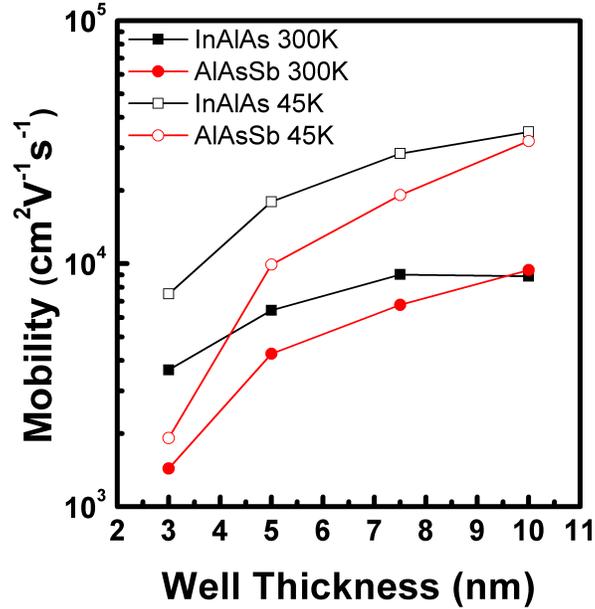
Figure 3.5: Measured low temperature (45 K) and room temperature (300 K) mobilities of InGaAs/InAlAs and InGaAs/AlAsSb 2DEGs as a function of the InGaAs well thickness.

barriers or at the InGaAs/AlAsSb interfaces is negligible compared to the 2DEG carrier concentrations typical of field-effect transistors. Furthermore (Fig. 3.6), alloy scattering, acoustic phonon scattering, and polar optical phonon scattering are independent of 2DEG carrier concentration. The room temperature mobility in the 10 nm well is primarily limited by polar optical phonon scattering. For 2DEG carrier concentrations less than $3 \times 10^{11}$ cm$^{-2}$, remote impurity scattering from the modulation-doped layer becomes the dominant scattering mechanism. Remote impurity scattering can be reduced by increasing the distance between the modulation doping and the quantum well.
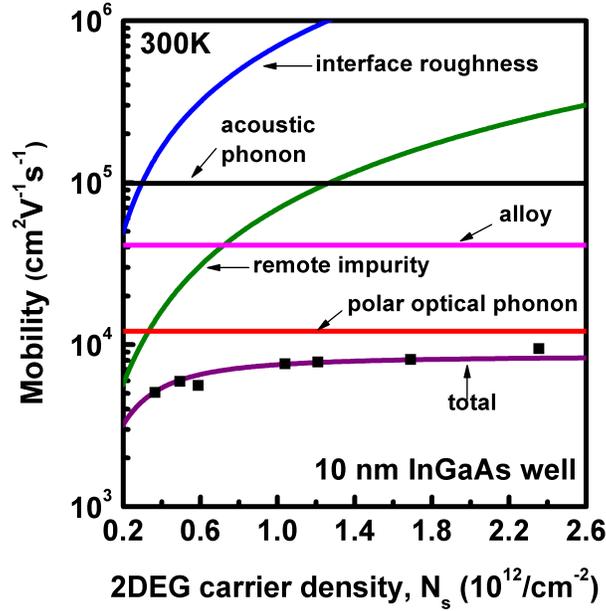
Figure 3.6: The measured and the calculated room temperature mobilities of InGaAs/AlAsSb 2DEGs as a function of 2DEG carrier concentration ($N_s$). The modulation-doped impurity concentration was varied from $1.0 \times 10^{12}$ to $3.9 \times 10^{12}$ cm$^{-2}$ by controlling the Si shutter opening time or the Si cell temperature. The calculation assumes the modulation-doped impurity concentration, Ni, is $2 \times 10^{12}$ cm$^{-2}$.

## 3.2.4   As and Sb interface soaking

Given the evidence presented above that interface roughness scattering is responsible for the observed degradation of 2DEG mobility in thin quantum wells, treatment of the interfaces is critical for further improvement on 2DEG mobility in 3-5 nm quantum wells. For this purpose, different interface treatments including As exposure and Sb exposure at the InGaAs/AlAsSb interfaces were investigated. G. Tuttle et al. [31] reported that the 2DEG mobility in InAs/AlSb quantum wells was strongly dependent on the growth of the InAs/AlSb interfaces, with InSb-like interfaces providing significantly higher 2DEG mobility than AlAs-like interfaces.

| Well thickness | Colume-V exposure during interuption | | $N_s$, 300K | Hall mobility, 300K |
|---|---|---|---|---|
| (nm) | Top interface | Bottom interface | $(10^{12}$ cm$^{-2})$ | $(10^3$ cm$^2$/V·s$)$ |
| 5 | As | As | 2.30 | 4.95 |
| 5 | As | Sb | 2.36 | 4.90 |
| 5 | Sb | As | 2.30 | 4.88 |
| 5 | Sb | Sb | 2.23 | 4.87 |

Table 3.3: InGaAs/AlAsSb 2DEG Hall mobility as a function of column-V exposure during growth interruptions at the InGaAs/AlAsSb interfaces.

The difference was attributed to the scattering between transport electrons and antisite defects created at the AlAs-like interfaces. Following the similar concept, we therefore treated the InGaAs/AlAsSb interfaces with different group-V species. Since the complexity of InGaAs/AlAsSb interfaces leads to six combinations of interface (InAs, InSb, GaAs, GaSb, AlAs, and AlSb), instead of intentionally growing a certain type of interface by the shutter sequences during MBE growth, as described earlier, we interrupted the growth and exposed the surface to As or Sb for at least 30 seconds. Table 3.3 summarizes the Hall results of various 2DEG samples. It could be found that for narrow wells (5 nm) under this investigation, the room temperature 2DEG mobility is insensitive to which group-V species (As or Sb) the wafer was exposed to during the growth interruptions at the InGaAs/AlAsSb interfaces. Another sample with 2 minutes Sb interruption at both the top interface and the bottom interface, and the other sample with an intentionally-grown 1.25 monolayer InSb-like interface (with the similar shutter sequences described in [31]), both showed similar carrier concentration and room temperature 2DEG mobility as the samples in Table 3.3.

| Well thick-ness (nm) | Top interface | Bottom interface | $N_s$, 300K ($10^{12}$ cm$^{-2}$) | Hall mobility, 300K ($10^3$ cm$^2$/V·s) |
|---|---|---|---|---|
| 5 | As interruption | As interruption | 2.13 | 4.78 |
| 5 | 2ML InAlAs | 2ML InAlAs | 1.94 | 5.69 |
| 3 | As interruption | As interruption | 1.89 | 1.63 |
| 3 | 2ML InAlAs | 2ML InAlAs | 1.84 | 2.71 |

Table 3.4: Comparison of InGaAs/AlAsSb 2DEG Hall mobility with As interruption and with an insertion of two monolayer InAlAs at the InGaAs/AlAsSb heterointerfaces.

## 3.2.5   Mobility enhanced layers

Given that InGaAs/InAlAs heterointerfaces provide lower interface roughness scattering than InGaAs/AlAsSb heterointerfaces, we then grew InGaAs/AlAsSb quantum wells with a 5 (∼2ML) InAlAs layer inserted at the InGaAs/AlAsSb interfaces. Table 3.4 summarizes the room temperature mobility of 3 nm and 5 nm thick quantum wells with and without the InAlAs interfacial layer. With a 2ML InAlAs interfacial layer, the 2DEG mobility for the 3 nm thick InGaAs well increases from $1.63 \times 10^3$ cm$^2$/V·s to $2.71 \times 10^3$ cm$^2$/V·s, while the mobility for the 5 nm thick InGaAs well increases from $4.78 \times 10^3$ cm$^2$/V·s to $5.69 \times 10^3$ cm$^2$/V·s.

Note that the Hall mobility of InGaAs/AlAsSb 2DEGs with the 2ML InAlAs interfacial layers is still inferior to that of InGaAs/InAlAs 2DEGs ($\mu \sim 3.65 \times 10^3$ cm$^2$/V·s for a 3 nm well and $\mu \sim 6.43 \times 10^3$ cm$^2$/V·s for a 5 nm well). Further, Ref. [32] reports a 2DEG mobility of ∼4200 cm$^2$/V·s at 4 K in a 2.3 nm thick InGaAs quantum well with InP barriers. Given the smaller barrier energies associated with the InGaAs/InAlAs (∼0.5 eV) and InGaAs/InP interfaces (∼0.2 eV), these high mobilities may in part result from the reduced interface roughness scattering associated with the weaker quantum confinement in these materials systems.

## 3.3    Leakage reduction I: III-V FETs with wide band-gap barriers

In this section, we compare DC characteristics of InGaAs MOSFETs using AlAsSb and InAlAs barriers. The AlAsSb barriers and P-type doped InAlAs barriers can effectively reduce the buffer leakage current as compared with un-doped InAlAs barriers [10].

### 3.3.1    InGaAs FETs with AlAsSb barriers

Fig. 3.7 shows the device structure of sample A (InAlAs barriers) and sample B (AlAsSb barriers). Sample A consists of a 400 nm unintentionally doped (U.I.D.) $In_{0.52}Al_{0.48}As$ buffer layer, a 3 nm Si-doped ($1.3\times10^{19}$ cm$^{-3}$) $In_{0.52}Al_{0.48}As$ pulse doping layer, a 3 nm U.I.D. $In_{0.52}Al_{0.48}As$ spacer layer and a 10 nm InGaAs channel. Sample B consists of a 375 nm U.I.D. InAlAs buffer layer, a 25 nm U.I.D. AlAsSb bottom barrier layer, a 3 nm Si-doped ($1.3\times10^{19}$ cm$^{-3}$) InAlAs pulse doping layer, a 3 nm U.I.D. $AlAs_{0.56}Sb_{0.44}$ spacer layer, and a 10 nm $In_{0.53}Ga_{0.47}As$ channel. To fabricate MOSFETs, hydrogen silsesquioxane (HSQ) dummy gates were patterned by e-beam lithography, and ∼50 nm thick, n-type $In_{0.53}Ga_{0.47}As$ (Si: $4\times10^{19}$ cm$^{-3}$) source-drain layers were regrown by metal organic chemical vapor deposition (MOCVD). After MOCVD regrowth, the dummy gates were removed in buffered HF. Channel surface damage caused by regrowth was then removed by two cycles of digital etching [33]. The final $In_{0.53}Ga_{0.47}As$ channel thickness is ∼7.5 nm for both samples. Transistors were then mesa-isolated, were
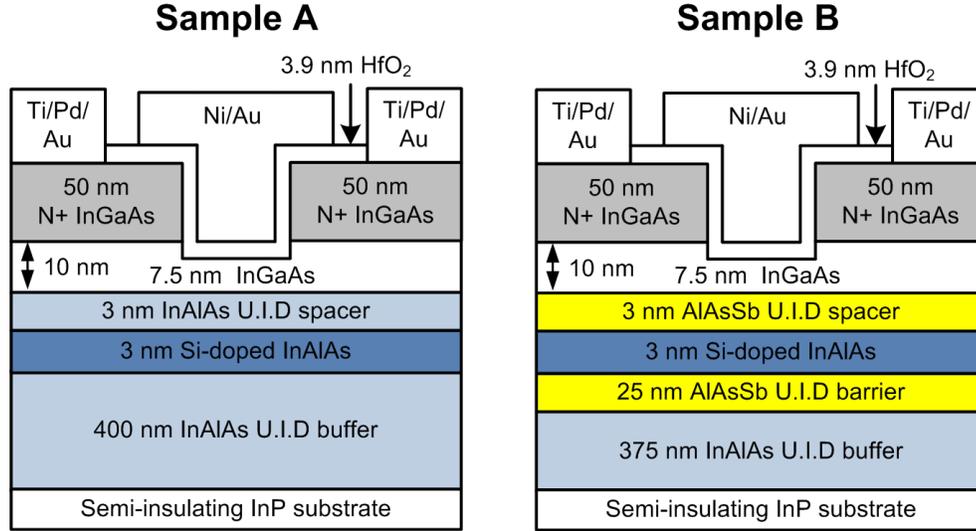
**Sample A**



**Sample B**

Figure 3.7: Device structure of sample A(In$_{0.52}$Al$_{0.48}$As barrier) and sample B (AlAs$_{0.56}$Sb$_{0.44}$ barrier). The pulse doping layer is 3 nm, $1.3\times10^{19}$ cm$^{-3}$ Si-doped In$_{0.52}$Al$_{0.48}$As. The InGaAs channel thickness is 7.5 nm. (U.I.D. = un-intentionally doped)

cleaned in buffered HF for 2 min and then in-situ cleaned in an atomic layer deposition (ALD) reactor using alternating cycles of nitrogen plasma and trimethylaluminum pretreatment. Approximately 3.9 nm HfO$_2$ gate dielectric was then blanket-deposited. Samples were then annealed in forming gas (5% H$_2$/95% N$_2$) at 400 °C for 15 min. 35 nm/120nm thermally-evaporated Ni/Au gate metal and 20 nm/50 nm/100 nm Ti/Pd/Au source/drain metal were then deposited and patterned by liftoff. Because AlAs$_{0.56}$Sb$_{0.44}$ is readily oxidized by air exposure and is etched during the mesa isolation, 0.75 $\mu$m mesa etch undercut is observed at the edge of the bottom barrier in the final devices. The final gate width determined by scanning electron microscope is $\sim$23.5 $\mu$m (25 $\mu$m as drawn) for sample B.

Fig. 3.8 shows the transfer characteristics of sample A and sample B, at 56 nm and 58 nm gate lengths ($L_\text{g}$) respectively. At $V_\text{DS}$=0.5 V, sample A shows
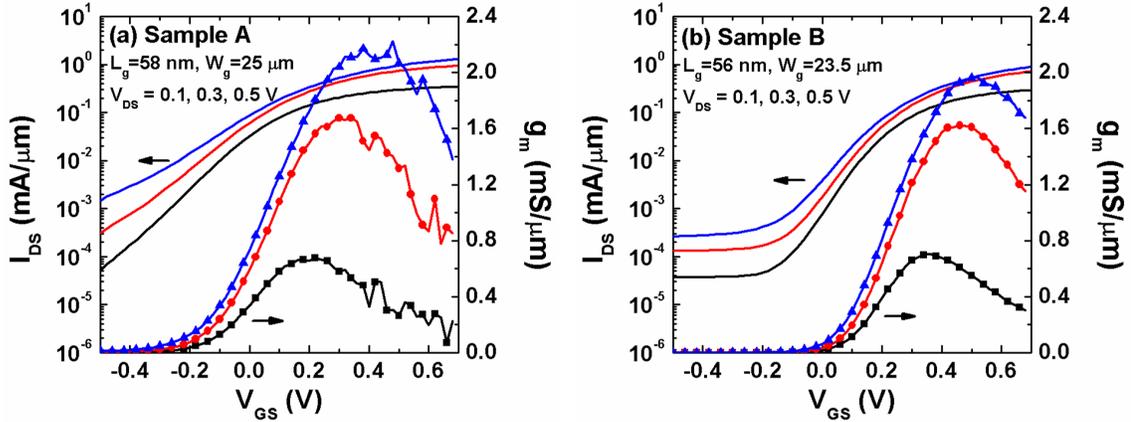
Figure 3.8: Transfer characteristics of (a) sample A with $L_g$=56 nm and (b) sample B with $L_g$=58 nm at $V_{DS}$ of 0.1, 0.3, and 0.5 V.

2.2 mS/$\mu$m peak transconductance and 242 mV/dec. subthreshold swing ($SS$), while sample B shows 1.96 mS/$\mu$m peak transconductance and 134 mV/dec. $SS$. The drain-source leakage current ($I_{DS}$ at e.g. $V_{GS}$= -0.2 to 0.4 V) is significantly reduced in sample B. The slightly reduced transconductance of sample B may be due to reduced mobility arising from stronger interface roughness scattering of InGaAs/AlAsSb heterojunction as discussed in the section 3.2. As a function of gate lengths, threshold voltages are 0.1-0.15 V more positive for sample B, possibly a result of the increased eigenstate energy in the InGaAs channel, also due to stronger quantum confinement.

Fig. 3.9(a) and 3.9(b) compares the subthreshold characteristics of samples A and B as a function of gate lengths. With sample A (InAlAs barrier), the off-state drain leakage current ($I_D$ at e.g. $V_{GS}$=0.2 to 0.4 V) increases rapidly as $L_g$ is reduced from 558 nm to 131 nm and 56 nm, particularly for $V_{DS}$=0.5 V. At short gate lengths, 130 nm and 58 nm $L_g$, sample B (AlAsSb barrier), exhibits much smaller off-state leakage than sample A. For $L_g$ <200 nm, sample
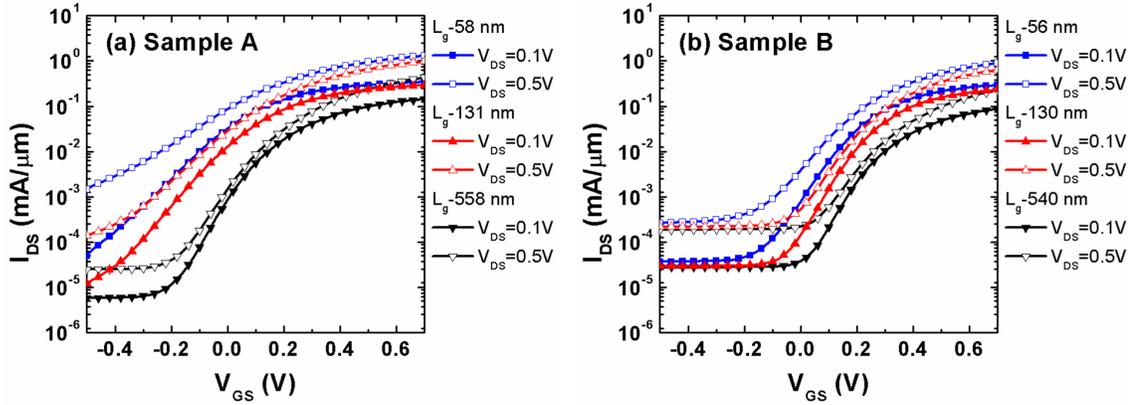
Figure 3.9: Subthreshold characteristics (a) of sample A with $L_g$=56, 131, and 558 nm and (b) of sample B with $L_g$=58, 130, and 540 nm.

B shows considerably smaller subthreshold swing as shown in Fig. 3.10. Sample B shows a residual off-state leakage of $3 - 4 \times 10^{-5}$ mA/$\mu$m at $V_{DS}$=0.1 V and $2 - 3 \times 10^{-4}$ mA/$\mu$m at $V_{DS}$=0.5 V. This background leakage has an approximately linear (Ohmic) variation with $V_{DS}$, and is only weakly dependent upon the gate length; on other experimental samples, we have observed similar background leakage when the isolation mesa etch depth is insufficient.

Off-state drain leakage current arising from simple electrostatics (excessive channel or gate dielectric thickness) or from source-drain or band-band tunneling would not show the strong observed dependence upon the energy offset of the lower barrier. Leakage by thermal emission from the N+ source over the channel-barrier interface should however show a strong dependence upon the barrier energy, consistent with Fig. 3.8 and Fig. 3.9. Fig. 3.11 shows a computed energy band diagram drawn vertically through the MOSFET regrown N+ $In_{0.53}Ga_{0.47}As$ source (Si-doped: $4 \times 10^{19}$ cm$^{-3}$), through the un-doped $In_{0.53}Ga_{0.47}As$ channel, and into $In_{0.52}Al_{0.48}As$ or $AlAs_{0.56}Sb_{0.44}$ bottom barrier layer. The band diagram
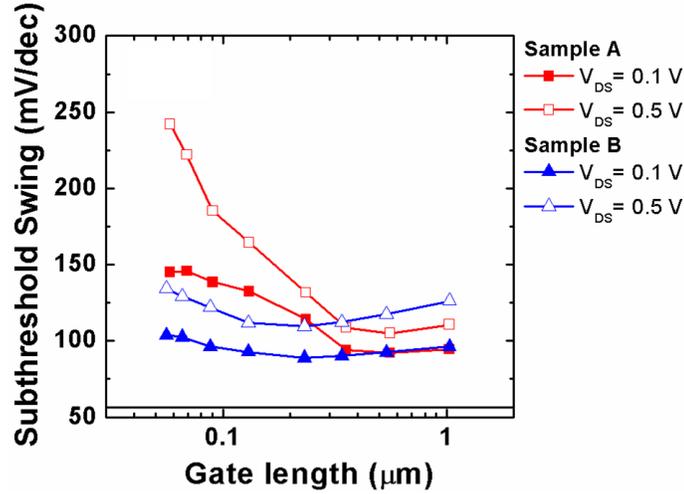
Figure 3.10: Subthreshold swing vs. $L_g$ for sample A and sample B at $V_{DS}$=0.1 V and $V_{DS}$ =0.5 V.

is calculated by self-consistent 1-D Schrödinger and Poisson equation using Band-Profiler (provided by Professor William Frensley). The conduction band energy and valence band energy of $AlAs_{0.56}Sb_{0.44}$ barrier is linearly interpolated from un-strained AlAs and AlSb layers without considering bowing parameter. As shown in Fig. 3.11, the electron Fermi level lies $\sim$0.4 eV above the conduction band of the N+ source and $\sim$0.2 eV above that of the un-doped InGaAs channel. The $In_{0.52}Al_{0.48}As$ layer provides only $\sim$0.1-0.2 eV barrier above the electron Fermi level, insufficient to strongly suppress thermal emission from the N+ source. Using an oxide barrier [34], or a wide band-gap semiconductor barrier will potentially reduce this barrier leakage current. Replacement of the $In_{0.52}Al_{0.48}As$ barrier with $AlAs_{0.56}Sb_{0.44}$ increases the barrier energy by $\sim$0.5 eV, and should suppress this thermal emission by ca. $10^8$:1.
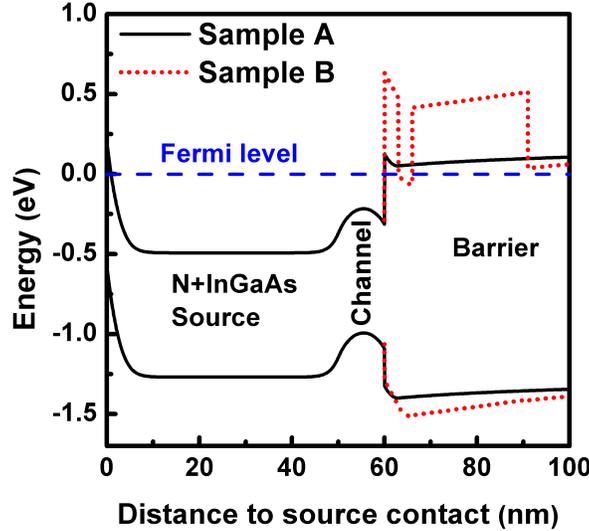
Figure 3.11: Energy band diagram of sample A ($In_{0.52}Al_{0.48}As$ barrier) and sample B ($AlAs_{0.56}Sb_{0.44}$ barrier) with raised N+ InGaAs source/drain (Si–doped: $4 \times 10^{19}$ cm$^{-3}$), drawn on a vertical line passing through the N+ source, the InGaAs channel, and the InAlAs or AlAsSb bottom barrier. Given the high source doping, the InAlAs barrier energy lies only $\sim$ 0.1-0.2 eV above the Fermi energy, while the AlAsSb barrier provides $\sim$ 0.6-0.7 eV carrier confinement.

## 3.3.2   InGaAs FETs with P-type doped InAlAs barriers

In previous subsection, we found that un-doped InAlAs barriers showed high buffer leakage as compared to un-doped AlAsSb barriers. If the conduction band edge of the barrier is not sufficiently high, electron injection from heavily-doped source into back barrier layers can cause high off-state leakage at large $V_{DS}$. Another approach to increase conduction band edge and reduce barrier leakage is doping engineering of barrier layers instead of band-gap engineering. Fig. 3.12 shows the device comparisons between un-doped InAlAs barriers and P-doped InAlAs barriers. The conduction band energy of InAlAs barriers increases about half band-gap energy ($\sim$0.7 eV) by inserting a Be-doped ($1 \times 10^{17}$ cm$^{-3}$) InAlAs layer,

which intentionally forms a P-i-N dipole with the Si-doped InAlAs modulation-doped layer. The P-doped InAlAs layer depletes the electrons in the barrier layer, and removes the barrier leakage path. In Fig. 3.12(c), the off state leakage is largely reduced to two orders of magnitude from 1 $\mu$A/$\mu$m (limited by barrier leakage) to 10 nA/$\mu$m (limited by band-to-band tunneling) for 50 nm-$L_{\mathrm{g}}$ devices. A significant reduction in subthreshold swing from 221 mV/dec. to 105 mV/dec. at $V_{\mathrm{DS}}$=0.5 V indicates the improvement on transistor electrostatics after adding a p-doped InAlAs barrier.

Last but not least, note that the leakage in un-doped InAlAs barriers behaves like an InAlAs barrier MOSFET in parallel with the InGaAs channel MOSFET. Since the InAlAs barrier is distant from the gate metal, this barrier MOSFET is difficult to turn off and the barrier leakage could increase rapidly as the gate length decreases because of serious short channel effects. We found that the barrier leakage in un-doped InAlAs barriers is not linearly proportional to $1/L_{\mathrm{g}}$, and can increase more than $\sim$2-3 orders of magnitude when $L_{\mathrm{g}}$ decreases from 1 $\mu$m to 50 nm. Once a p-doped InAlAs barrier is incorporated, the barrier leakage is sufficiently low ($<$100 pA/$\mu$m), and band-to-band tunneling leakage (BTBT) becomes dominant on the minimum $I_{\mathrm{off}}$. The detail of band-to-band tunneling leakage and the remedies of BTBT leakage will be discussed in the next two chapters.

(a)



(b)



(c)
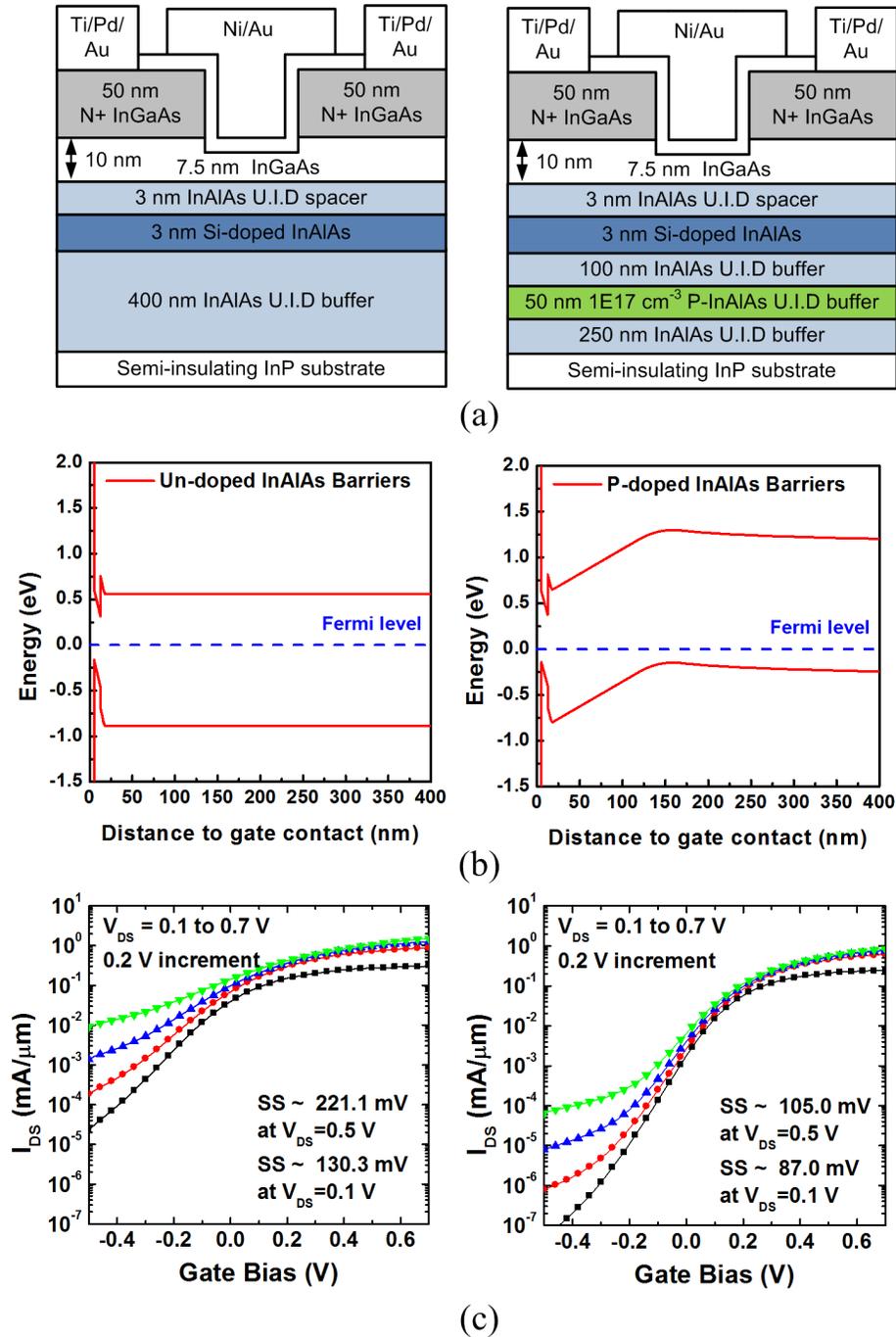
Figure 3.12: (a) The device structures with un-doped InAlAs barriers (left) and P-doped InAlAs barriers (right). (b) The corresponding band energy diagrams. (c) The corresponding $I_{\text{DS}}$-$V_{\text{GS}}$ curves of 50 nm-$L_{\text{g}}$ devices.

## 3.4   Summary

In this chapter, we have developed $AlAs_{0.56}Sb_{0.44}$ barrier layers lattice- matched to InP and demonstrated a high mobility $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ two dimensional electron gas (2DEG) with room temperature mobility up to $9\times10^3$ cm$^2$/V·s. We have also investigated the electron transport in $In_{0.53}Ga_{0.47}As/AlAs_{0.56}Sb_{0.44}$ two dimensional electron gases and compared their properties with $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ 2DEGs. Stronger interface roughness scattering is observed for In-GaAs/AlAsSb heterointerfaces than for InGaAs/InAlAs heterointerfaces. For the well thickness below 4 nm, interface roughness scattering becomes the dominant scattering mechanism, limiting the 2DEG mobility at low temperature as well as room temperature. Changing the group-V exposure between As and Sb during growth interruptions at the InGaAs/AlAsSb interfaces does not significantly change the 2DEG mobility. With the insertion of a two monolayer InAlAs at the InGaAs/AlAsSb interfaces, the interface roughness scattering is reduced and the mobility greatly increased. The room temperature 2DEG mobility shows 66 % improvement from $1.63\times10^3$ cm$^2$/V·s to $2.71\times10^3$ cm$^2$/V·s for a 3 nm InGaAs well.

We have also compared the DC characteristics of planar $In_{0.53}Ga_{0.47}As$ channel MOSFETs using $AlAs_{0.56}Sb_{0.44}$ barriers to similar MOSFETs using $In_{0.52}Al_{0.48}As$ barriers. $AlAs_{0.56}Sb_{0.44}$, with $\sim$1.0 eV conduction-band offset to $In_{0.53}Ga_{0.47}As$, improves electron confinement within the channel. A 56 nm gate length device with the $AlAs_{0.56}Sb_{0.44}$ barrier exhibits 1.96 mS/$\mu$m peak transconductance and $SS$=134 mV/dec. at $V_{DS}$=0.5 V. At gate lengths below 100 nm and $V_{DS}$=0.5 V, the MOSFETs with $AlAs_{0.56}Sb_{0.44}$ barriers show steeper subthreshold swing and

reduced drain-source leakage current. We attribute the greater leakage observed with the $In_{0.52}Al_{0.48}As$ barrier to thermionic emission from the N+ $In_{0.53}Ga_{0.47}As$ source over the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterointerface. In addition to AlAsSb barriers, P-doped InAlAs barriers were also developed and confirmed as an effective remedy to reduce barrier leakage.

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# Chapter 4

# Channel Engineering: Ultra-thin InGaAs and InAs Channels

When transistor gate lengths ($L_\mathrm{g}$) are scaled down to below 10 nm, channel thickness must be reduced simultaneously to maintain good electrostatic integrity and reduce the subthreshold leakage [1]. Channel thickness scaling is evident from shrinking the fin width of FinFETs or thinning the Si body of silicon-on-insulator (SOI) MOSFETs. Nowadays the state-of-art 14 nm Si FinFETs have fin width about ~8 nm and the advanced ultra-thin body (UTB) fully depleted SOI (FDSOI) MOSFETs have Si body thickness about ~5 nm, as illustrated in Fig. 4.1 [2, 3]. With the continuous scaling of physical gate length, at 7 nm technology node, III-V channels must be stringently evaluated at 2~4 nm channel thickness. Therefore, electron transport in ultra-thin channels must be carefully scrutinized, and III-V channels must be carefully designed with the considerations for transistor electrostatics, on-state performance, and off-state leakage.

In this chapter, we report MBE growth optimization of InAs channels, and then compare the electron transport properties of InGaAs and InAs in ultra-thin quantum wells two dimensional electron gas (2DEG). Ultra-thin channel III-V MOSFETs with respective 3 nm InGaAs and 3 nm InAs channels are compared thoroughly. In addition to engineer the channel band-gap using different channel materials, we also investigate the impact of channel thickness scaling on the DC performance of InGaAs MOSFETs. Finally, we conclude this chapter with a record high performance InAs channel MOSFET, featuring the highest on-state performance among all the reported III-V MOSFETs and comparable performance to 22 nm Si FinFET technology [4].
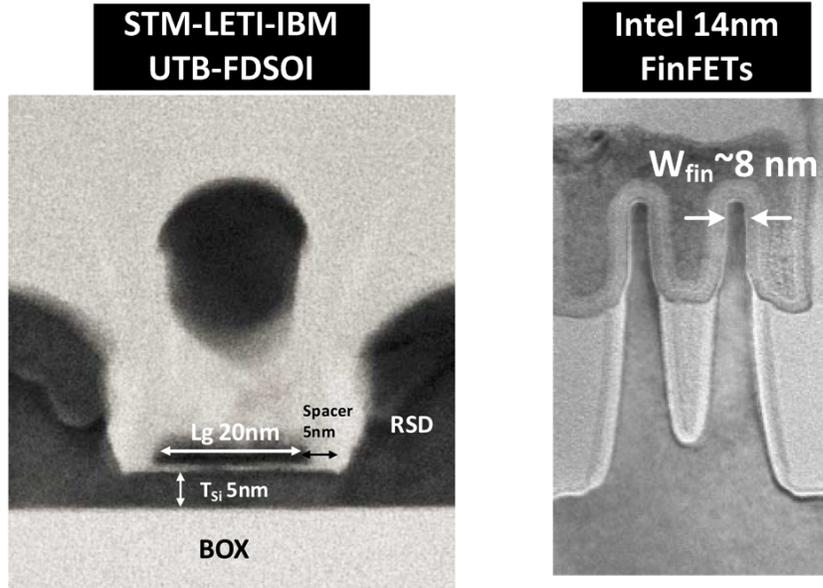
Figure 4.1: A TEM image of ultra-thin-body (UTB) fully depleted silicon on insulator (FDSOI), featuring a 5 nm thick Si channel [2]. A TEM image of Intel 14 nm FinFETs, featuring a 8 nm narrow fin [3].

## 4.1 MBE growth of composite channel 2DEGs

In this section, we report the optimized MBE growth of composite channel 2DEGs. Fig. 4.2(a) shows the 2DEG structure of InGaAs/InAs/InGaAs composite channels. The composite channels have symmetric sandwich structures with an inserted InAs channel clad in the InGaAs top and bottom channels. The total quantum well is 10 nm thick, and is bounded by either InAlAs or AlAsSb barriers. Since InAs has –3.1% lattice-mismatched with InP substrates, the InAs layer has a critical thickness at which the strain energy of pseudomorphic InAs layer surpasses the critical energy, and starts to relax by forming misfit and threading dislocations. To maintain superior transport properties and achieve high performance III-V MOSFETs, defect-free InAs layers are desirable because the crystalline de-

fects could be a potential leakage current source [5] and degrade the electron transport properties.

The growth of a strained InAs layer is highly dependent on the growth temperature, growth rate, and V/III ratio [6]. In this study, the InAs layer was grown at 375~400 °C, lower than the growth temperature of InAlAs or AlAsSb barriers (490 °C). Lowering the growth temperature of InAs increases the InAs critical thickness and avoids strain relaxation [6]. The growth rate of InAs layer is ~0.69 $\mathring{A}$/s, which is about half of the $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ growth rate. Fig. 4.2(b) shows the impact of As/In beam equivalent pressure (BEP) ratio on the 2DEG mobility of composite channels. The optimal As/In ratio is about 5.5, showing electron mobility >12000 $cm^2$/V·s. The As/In BEP ratio higher or lower than 5.5 causes the degradation of 2DEG mobility. Fig. 4.2(c) shows the Hall mobility of composite channel 2DEGs as a function of the inserted InAs well thickness. Note that the total well thickness is 10 nm. After lowering As/In BEP ratio from 10 to 5.5, the 2DEG mobility increases as InAs thickness increases. The growth reproducibility for composite channel 2DEGs with thick InAs layers is greatly improved as lowering As/In BEP ratio to 5.5, as an indicative of improved mechanical stability and an increase on the InAs critical thickness. The highest mobility of composite channel 2DEGs achieves ~13000 $cm^2$/V·s at room temperature.
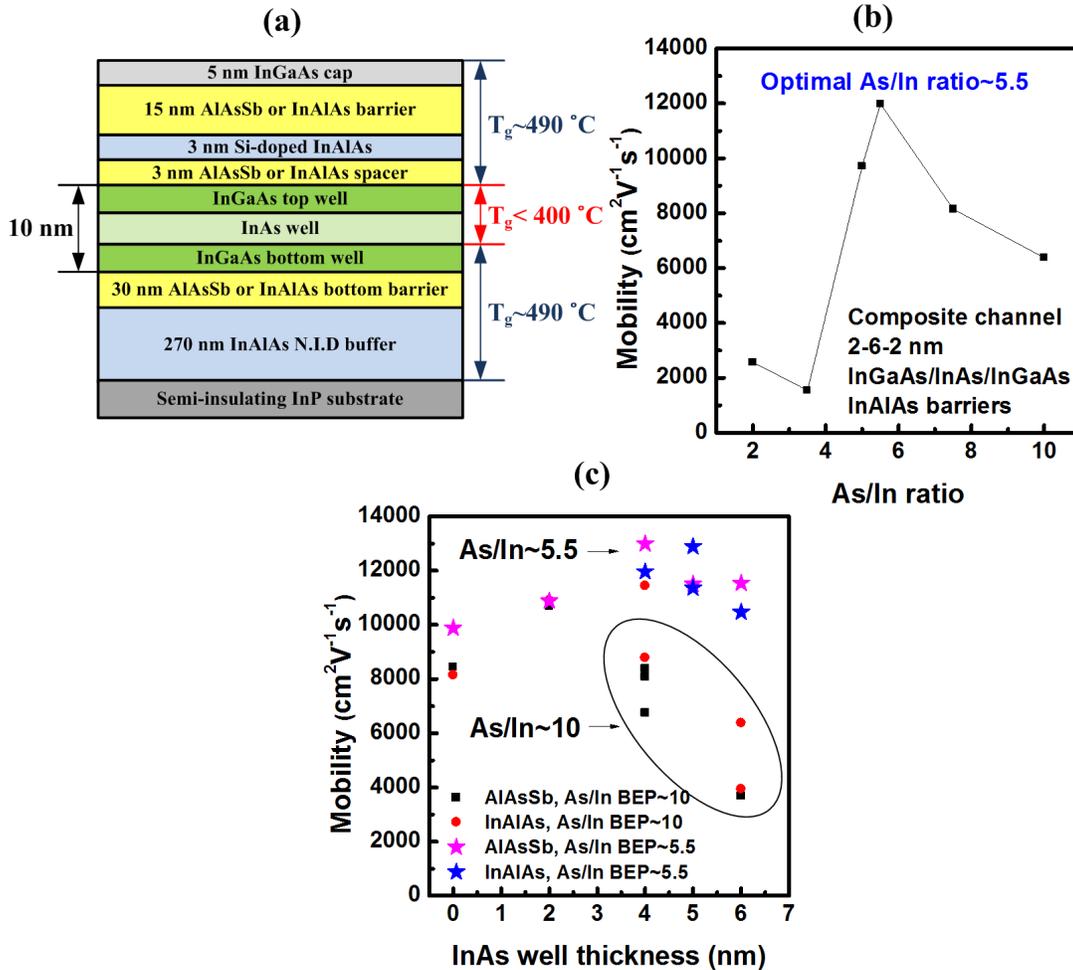
Figure 4.2: (a) The composite channel 2DEG structures and the respective growth temperature for each layer. (b)The dependency of 2DEG mobility for 2-6-2 nm InGaAs-InAs-InGaAs composite channels on the As/In BEP ratio during the 6 nm InAs growth. (c) Composite channel 2DEG mobility as a function of the InAs well thickness.(The channels are 10 nm InGaAs, 4-2-4 nm, 3-4-3 nm, 2.5-5-2.5 nm, and 2-6-2 nm InGaAs-InAs-InGaAs composite channels.)

## 4.2    Electron transport in InGaAs and InAs ultra-thin quantum wells

With the optimized InAs growth condition, we can compare the electron transport in strained InAs wells with lattice-matched InGaAs wells. Fig. 4.3 shows the 2DEG structure and the corresponding band diagram calculated by 1-D self-consistent Schrödinger-Poisson simulation (BandProfiler provided by Professor William Frensley). The measured 2DEG mobility and carrier concentrations as a function of InGaAs and InAs well thickness are shown in Fig. 4.4. The 2DEG mobility is found higher in the thick InAs wells than in the thick InGaAs wells, but 2DEG mobility converges as the well is thinned to 2 nm. The electron concentration in the quantum well also decreases with reduced well thickness because of increasing sub-band energy ($E_0$) and hence reduced $E_{\mathrm{F}}$-$E_0$.

As wells are thinned, the electron scattering time becomes dominated by interface roughness scattering as discussed in the last chapter. The rapid mobility degradation of InAs wells could be attributed to larger interface roughness of InAs wells due to the proclivity of island growth of strained InAs layers (Stranski-Krastanov growth). On the other hand, the electron effective mass also increases because of the quantized sub-band energy and the non-parabolic conduction band. Due to strong quantum confinement effects in ultra-thin wells, the quantized sub-band energy raises with the decrement of well thickness, leading to the penetration of electron wave-function into barrier layers where the electron effective mass is higher and therefore reduce electron transport mass. Also, due to non-parabolic conduction band, the electrons populated in high energy quantized sub-band have
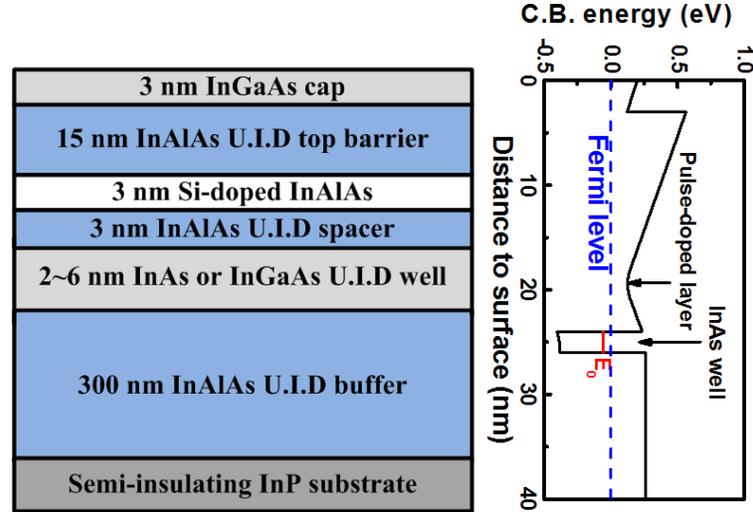
Figure 4.3: Double heterostuctures for the study of electron transport in quantum wells and the associated band diagram calculated by 1-D self-consistent Schrödinger-Poisson simulation.

larger effective mass than that at the band minimum of $\Gamma$ valley. Given that InAs has larger non-parabolic coefficient of conduction band than InGaAs ($\alpha \sim 2.6$ eV$^{-1}$ versus $\alpha \sim 1.3$ eV$^{-1}$), the electron effective mass of InAs increases more rapidly, and could be similar to that of InGaAs at 2∼3 nm channel thickness. Fig. 4.5 summarizes the effective mass values from experimental measurements and theoretical calculations for InGaAs and InAs wells in the literatures [7–12]. The in-plane effective mass shows little difference in extremely thin (2∼3 nm) InAs and InGaAs wells. This might explain the similar mobility observed for 2 nm InGaAs and InAs wells.
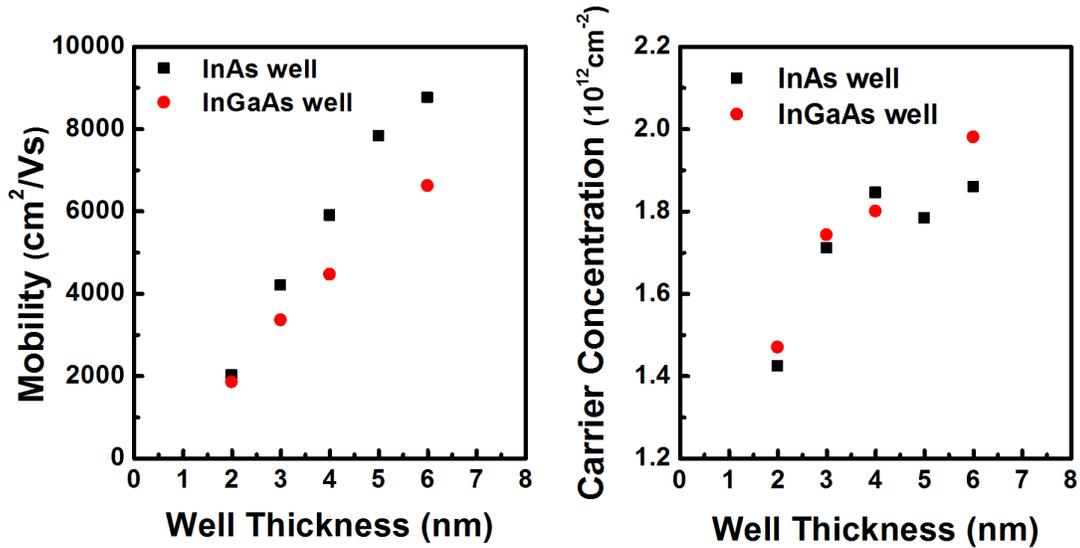
Figure 4.4: Comparison of electron mobility and the carrier concentration in InAs and InGaAs quantum wells as a function of well thickness.
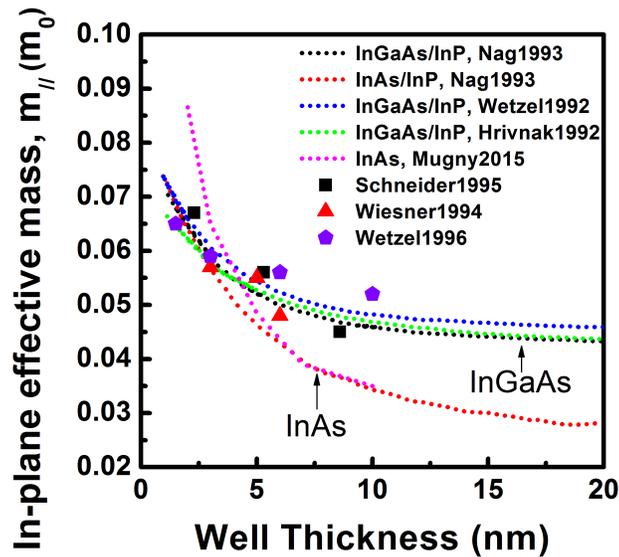


Figure 4.5: Summary of in-plane electron effective mass reported in the literature [7–12].(Dot line: theoretical calculations, solid dot: experimental data from InGaAs channels)

The following text appears to the right of the device structure diagram:

□ **MBE growth:**
  - **3 nm InGaAs cap + 3 nm InGaAs or InAs channel**
□ **HSQ dummy gate patterning**
□ **MOCVD S/D regrowth**
  - **10 nm U.I.D. InGaAs spacer**
  - **50 nm N+ InGaAs contact layer**
□ **Isolation and dummy gate removal**
□ **Digital etch: 2 cycles**
  **(removing 3 nm InGaAs cap)**
□ **High-k dielectric: 29Å HfO$_2$**
□ **Gate metal liftoff process**
  - **Ni/Au thermal evaporation**
□ **S/D metal liftoff process**
  - **Ti/Pd/Au E-beam evaporation**

Figure 4.6: The device structure and the detailed process flow of ultra-thin–body MOSFETs with a 3 nm InGaAs or a 3 nm InAs channel.

## 4.3 Leakage reduction II: ultra-thin channels

### 4.3.1 Channel materials: InAs versus InGaAs

Here we fabricated 3 nm InAs and 3 nm InGaAs ultra-thin-body (UTB) MOSFET and compared their DC characteristics. Fig. 4.6 shows the structure of surface channel MOSFETs with respective 3 nm InAs or InGaAs channels, and the detailed process flow. Both samples have a 3 nm InGaAs cap layer above the 3 nm InAs or InGaAs bottom channels. After HSQ dummy gate process and the subsequent MOCVD source/drain regrowth, the 3 nm InGaAs cap layer was removed by two cycles of digital etch, leaving a 3 nm bottom channel. Two samples were processed in parallel to reduce process variations and ensure accurate control of channel thickness. The samples have 10 nm unintentionally-doped (U.I.D.) InGaAs source/drain spacers and a 2.9 nm HfO$_2$ gate dielectric. The design of InGaAs source/drain spacers will be discussed in detail in chapter 5.

Fig. 4.7 shows I$_D$-V$_{GS}$ and I$_D$-V$_{DS}$ curves of 40 nm-$L_g$ FETs. Unlike the
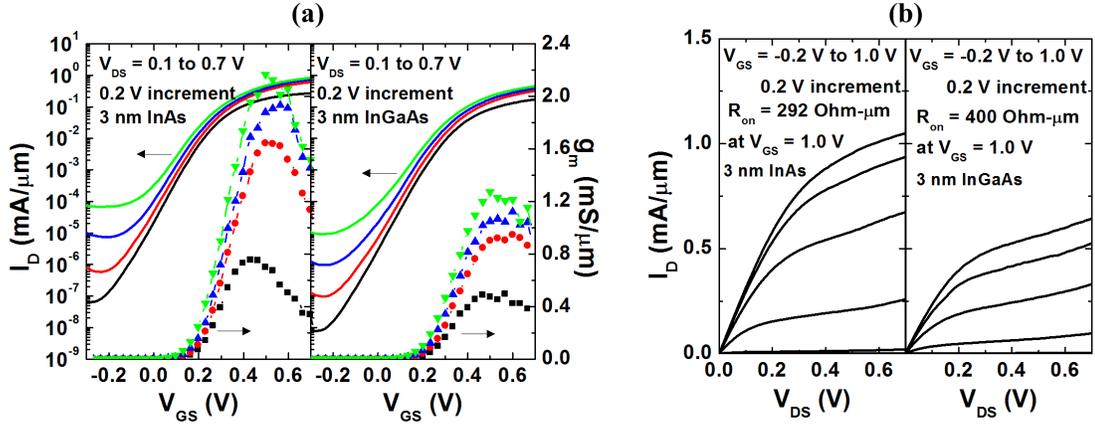
Figure 4.7: (a) The transfer characteristics and (b) the output characteristics of $L_g$-40 nm devices.

2DEG quantum well where the mobility are similar for InGaAs and InAs, InAs UTB MOSFETs show ~1.6:1 higher on-state current and transconductance than InGaAs UTB MOSFETs, but InGaAs channels show one order lower minimum $I_{off}$ than InAs channels. Fig. 4.8 compares the on-state performance, showing $I_{on}$ at $I_{off}$=100 nA/$\mu$m, transconductance, and $R_{on}$ as a function of $L_g$. InAs channels show maximum $I_{on}$~400 $\mu$A/$\mu$m at 100 nA/$\mu$m fixed $I_{off}$ and V$_{DS}$=0.5 V. At all gate lengths between 40 nm and 1 $\mu$m, $I_{on}$ and $g_m$ are much higher for InAs FETs than for InGaAs FETs, indicating not only higher injection velocity but also higher electron mobility in the InAs channel than in the InGaAs channel. Fig. 4.8(c) compares the on-resistance for InAs and InGaAs FETs, both showing parasitic source/drain resistance around 190±20 $\Omega \cdot \mu$m. This confirms that the inferior on-state performance of InGaAs channels is not caused by parasitic source/drain resistance, but from the InGaAs channel itself.

Fig. 4.9(a) and 4.9(b) show subthreshold swing ($SS$) and drain-induced barrier lowering ($DIBL$) as a function of $L_g$, respectively. Thanks to thin chan-

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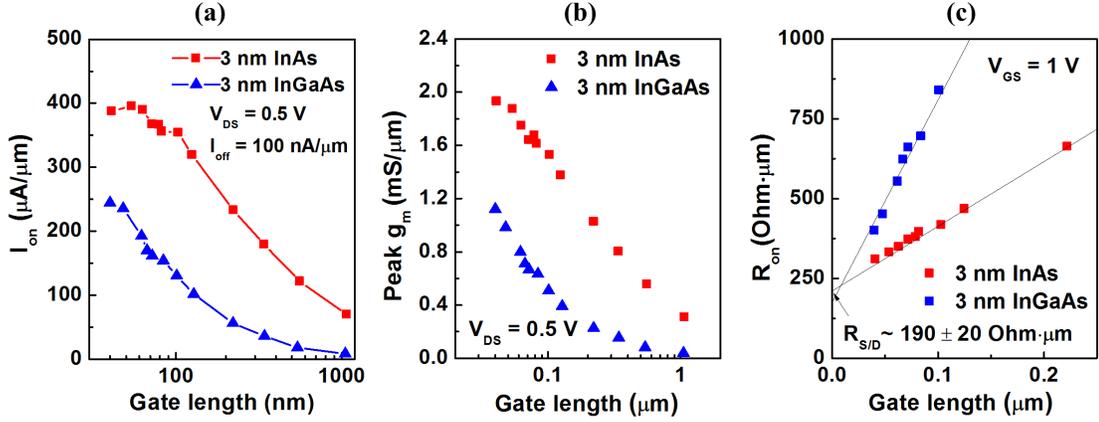
Figure 4.8: (a) $I_{\text{on}}$ vs. $L_{\text{g}}$ at 100 nA/$\mu$m $I_{\text{off}}$ and V$_{DS}$=0.5 V. (b) Peak $g_{\text{m}}$ vs. $L_{\text{g}}$ at V$_{DS}$=0.5 V. (c) $R_{\text{on}}$ vs. $L_{\text{g}}$ at V$_{GS}$=1 V.

nels and improved electrostatic integrity, both devices exhibit excellent $SS\sim 83$ mV/dec at $V_{\text{DS}}$= 0.5 V and low $DIBL\sim$110 mV/V for 40 nm-$L_{\text{g}}$ devices. Fig. 4.9(c) compares the minimum $I_{\text{off}}$ of the two devices. Due to its larger channel band gap, at short $L_{\text{g}}$ InGaAs FETs show one order lower off-state leakage current than InAs FETs, where $I_{\text{off}}$ is dominated by band-to-band tunneling (BTBT) leakage. This band-to-band tunneling leakage is evident, as shown in Fig. 4.7(a), from the signature that BTBT leakage increases as lowering the gate voltage and larger $V_{\text{D}}$-$V_{\text{G}}$. For long $L_{\text{g}}$ devices ($\sim$1 $\mu$m), the $I_{\text{off}}$ of InAs FETs are still limited by BTBT, while the $I_{\text{off}}$ of InGaAs FETs limited by gate leakage.

High indium content in thin surface-channel MOSFETs improves on-current despite having little effect on mobility in similarly thick wells bounded by semiconductor barriers. There are several possible explanations. Due to thin channels, the strong quantum confinement reduces the energy splitting between $\Gamma$ valley and L valley. As gate voltage increases, the electrons could populate in the L valleys, leading to mobility degradation in (100) InGaAs MOSFETs [13–16]. To clar-
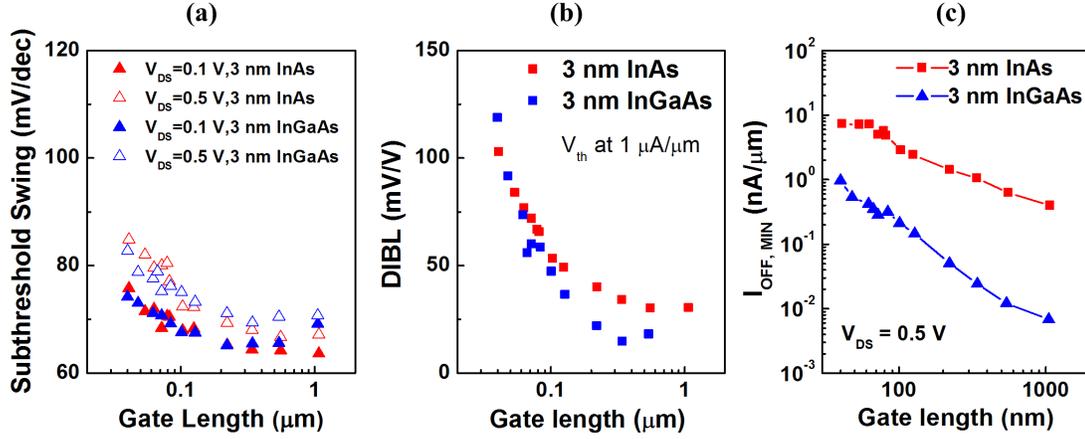
Figure 4.9: (a) Subthreshold swing vs. $L_{\mathrm{g}}$. (b) $DIBL$ vs. $L_{\mathrm{g}}$. (c) $I_{\mathrm{off,min}}$ vs. $L_{\mathrm{g}}$ at $\mathrm{V}_{DS}$=0.5 V.

ify the different valley population, Evan Wilson and Pengyu Long in Network for Computational Nanotechnology at Purdue University calculated the tight-binding band structures of 3 nm InAs and InGaAs channels as shown Fig. 4.10. In the calculation, the channels are bounded by 2 nm InAlAs bottom barriers, and the hydrogen-terminated top surface. The result shows ∼0.6 eV Γ-L bound state energy separation in a 3 nm InGaAs well, and ∼0.9 eV splitting in a 3 nm InAs well. Therefore, at the $\mathrm{V}_{GS}$-$\mathrm{V}_{th}$ corresponding to peak $g_{\mathrm{m}}$, the L valley is unlikely to be populated with either material.

Unlike quantum well 2DEGs where the well is bounded by semiconductor barriers, in FET channels there may be severe electron interactions between oxide traps and channel electrons. The traps with energy levels within the conduction band such as As-As anti-bonding or Ga dangling bonds could affect the transistor on-state performance. The low $g_{\mathrm{m}}$ of thin InGaAs channels may be due to Fermi level pinning, at positive gate bias, from interface traps at energies within the

| | In$_{0.53}$Ga$_{0.47}$As | InAs |
|---|---|---|
| m$_e$* at Γ [m$_0$] | 0.080 | 0.063 |
| Γ − L separation [eV] | 0.596 | 0.905 |
| E$_g$ at Γ [eV] | 1.06 | 0.639 |
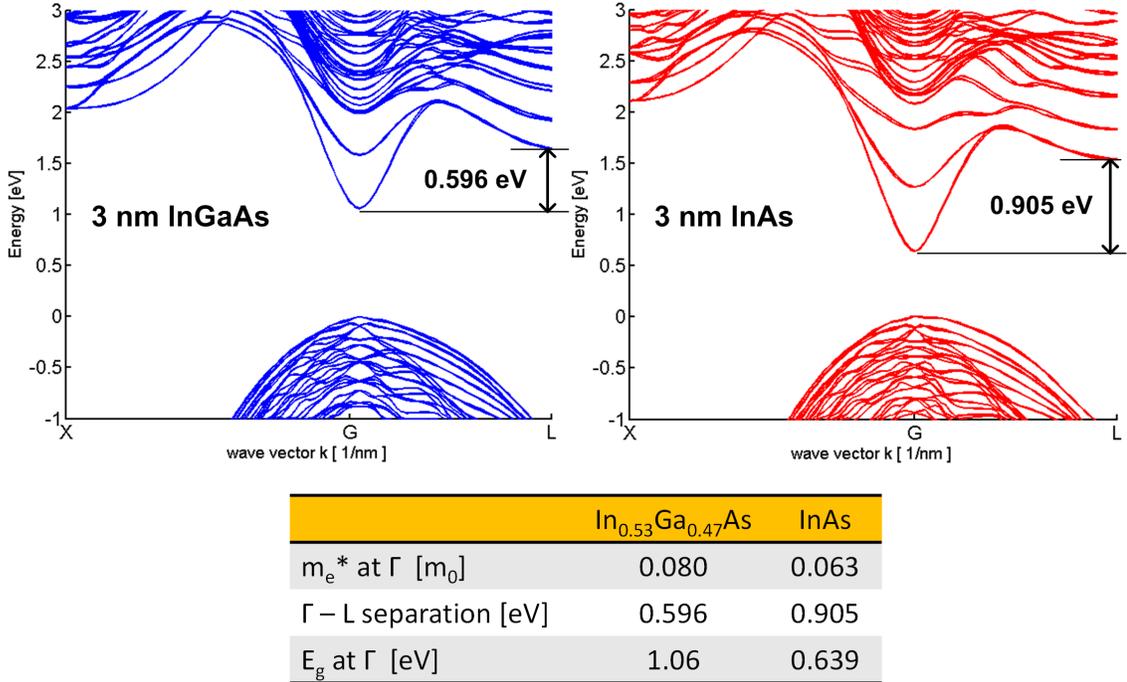
Figure 4.10: Tight binding band structures of 3 nm InGaAs and 3nm InAs wells with a hydrogen-terminated top surface and 2 nm InAlAs bottom barriers. No strain effect on InAs channel is considered in the calculations.

conduction band, again from As-As anti-bonding [17]; On the contrary, InAs has lower conduction band minimum, a larger energy separation between Fermi level and these trap states, and has no deleterious Ga dangling bonds. Therefore, electrons in InAs channels have less scattering with these oxide traps and are unlikely to be trapped in these interface states. Furthermore, it is observed that at long gate length the InAs channels usually show lower subthreshold swing than InGaAs channels, as an example shown in Fig. 4.9(a). This indicates that lower interface trap density with high-k dielectrics on InAs channels. More experimental results will be shown in the next subsection.

### 4.3.2   Channel thickness scaling

In this subsection, we compare a 4.5 nm InGaAs channel MOSFET with a 3 nm InGaAs channel MOSFET with a $ZrO_2$ gate dielectric layer, and investigate the electron transport properties in MOSFETs. The detailed device structure, process flow and the computed energy band diagrams are shown in Fig. 4.11. Fig. 4.12 shows the transfer and output characteristics of 4.5 nm and 3 nm InGaAs MOSFETs. Thinning the channel from 4.5 nm to 3 nm reduces the minimum $I_{off}$ from 30 nA/$\mu$m to 3.5 nA/$\mu$m but degrades $I_{on}$ and the transconductance. Thinning the channel increases the quantized band gap, thus reducing band-to-band tunneling (BTBT) leakage. Comparing the gate $I_G$ and drain $I_D$ leakage for 3 nm InGaAs FET in Fig. 4.12, it is observed that the minimum off-state leakage is still dominated by BTBT leakage rather than by gate leakage. Unfortunately, continuous scaling of channel thickness results in an unacceptable loss of on-state performance. For lower standby power logic applications, we seek to further reduce BTBT leakage while maintaining high on-state performance.

Fig. 4.13 shows transconductance, on-state current and on-resistance as a function of gate lengths. Similar to the results in last subsection, 3 nm InGaAs channels, regardless of using $ZrO_2$ or $HfO_2$ gate dielectrics, result in low on-state current and transconductance as compared to 4.5 nm InGaAs channels and 3 nm InAs channels. Unlike InGaAs, 3 nm thin InAs channels show lower channel resistance, while InGaAs channels thinner than 3.5 nm show degraded on-state performance and large channel resistance. Note that for 4.5 nm InGaAs channels, the $I_{on}$ at fixed $I_{off}$ drops as $L_g$ below 40 nm due to worse electrostatics and large $SS$, as shown in Fig. 4.13(b). Larger band-to-band tunneling leakage at negative

- **MBE growth: 6 nm InGaAs channel**
- **HSQ dummy gate patterning**
- **MOCVD S/D regrowth**
  - **10 nm UID InGaAs spacer**
  - **50 nm N+ InGaAs contact layer**
- **Isolation and dummy gate removal**
- **Digital etch**
  - **Sample A: 1 cycle (4.5 nm InGaAs)**
  - **Sample B: 2 cycle (3 nm InGaAs)**
- **High-k dielectric: 30Å ZrO₂**
- **Gate metal liftoff process**
  - **Ni/Au thermal evaporation**
- **S/D metal liftoff process**
  - **Ti/Pd/Au E-beam evaporation**

| Sample | A | B |
|--------|-----|-----|
| Channel (nm) | 4.5 | 3 |
| InGaAs spacer (nm) | 11.5 | 13 |

Figure 4.11: The process flow, detailed device structure and the corresponding energy band diagrams for 4.5 nm and 3 nm InGaAs channel MOSFETs.
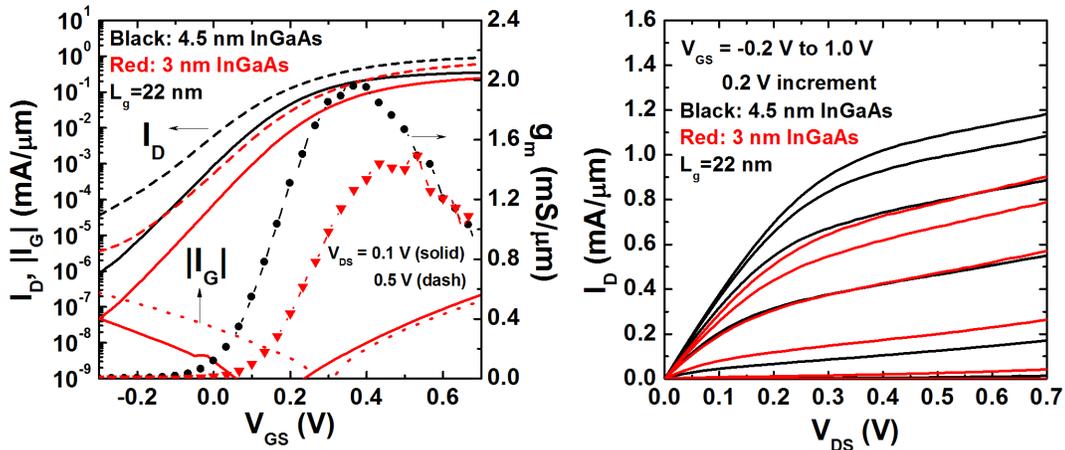
Figure 4.12: The transfer and output characteristics for 4.5 nm and 3 nm InGaAs channel MOSFETs.

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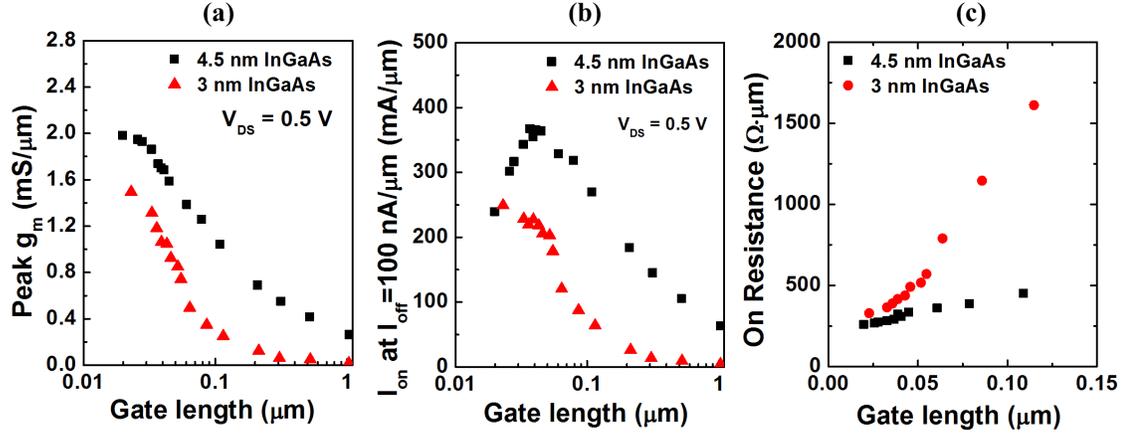
Figure 4.13: (a) The transconductance, (b) on-state current at 100 nA/$\mu$m $I_{\text{off}}$, and (c) on-resistance as a function of gate length for 4.5 nm InGaAs and 3 nm InGaAs MOSFETs.

gate bias also causes the degradation of $SS$ and reduces $I_{\text{on}}$ at the fixed $I_{\text{off}}$. For the figure of merit of $I_{\text{on}}$ at fixed $I_{\text{off}}$ and $V_{\text{DD}}$, $SS$ is the most important device parameter that must be optimized to increase on-state current. Therefore, thinner channels with resultant better gate control are highly demanded. Given that thin InAs channels still maintain good transport properties, thin InAs channels are clearly superior to InGaAs channels for high performance logic if the minimum off-state leakage is still acceptable.

To clarify the different transport properties of ultra-thin channels, we measured the capacitance-voltage (C-V) curves of InGaAs channel MOSFETs at 25 $\mu$m-$L_{\text{g}}$. Fig. 4.14 shows the C-V measurements of 4.5 nm and 3 nm InGaAs channels respectively. The C-V curve of 4.5 nm InGaAs channels shows high gate-to-channel capacitance ($C_{\text{g}-\text{ch}}{\sim}2.5\ \mu\text{F/cm}^2$) and small frequency dispersions, while large frequency dispersions are observed for 3 nm InGaAs channels. This might be an evidence of strong interactions between channel electrons and oxide
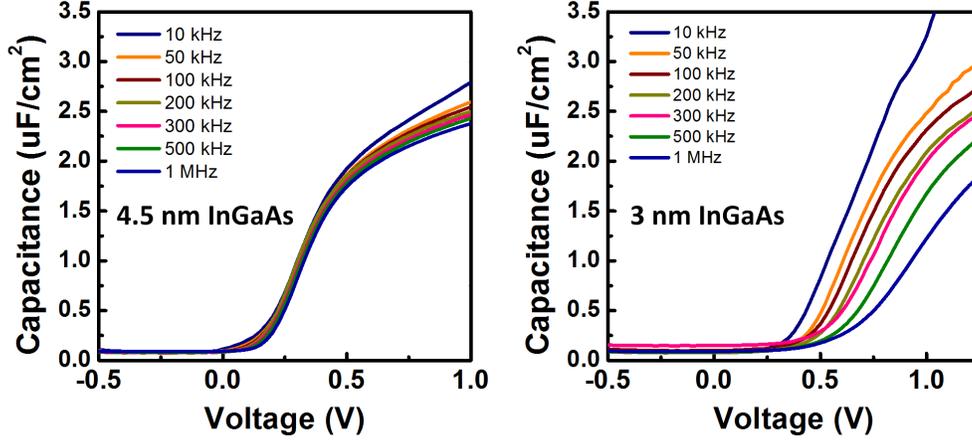
Figure 4.14: The capacitance-voltage measurements of $L_{\mathrm{g}}$-25 $\mu$m MOSFETs for 4.5 nm and 3 nm InGaAs channels and $ZrO_2$ gate dielectrics. The source and drain are grounded and the measured frequency varies from 10 kHz to 1 MHz.

traps. Note that the MOSFET C-V curves were measured with source and drain grounded together. When applying positive gate bias, the accumulated electrons in the channel are supplied by the source and drain. If the channel is thin and highly resistive, the series resistance in the InGaAs channel can also cause frequency dispersions. Further development of a equivalent circuit model would be helpful to separate the individual contributions from interface traps and channel series resistance to the C-V frequency dispersions.

For the interface traps above the conduction band edge of the III-V channel, J. Robertson used density-functional theory (DFT) and calculated the energy distribution of interface traps in different channel materials, as shown in Fig 4.15(a) [18, 19]. The As-As anti-bonding and Ga dangling bonds have energy levels above conduction band edge, which could potentially pin the Fermi level and reduce the effective channel mobility. These interface trap states have

little energy dependance with respect to channel In/Ga alloy compositions. By increasing In content of the channel, the conduction band edge is lower so that the electron has less interactions with these interface traps. In Fig. 4.15(b), N. Taoka et al. reported that As-As anti-bonding causes Fermi level pinning at the energy level ~0.21-0.35 eV above the conduction band minimum of InGaAs channels [17, 20]. An increase on channel indium content lowers conduction band minimum, and increases the effective channel mobility. Due to strong quantum confinement and the increased sub-band energy, we believe that the 3 nm In-GaAs channel MOSFETs also suffer from strong electron interactions with these interface traps. Strong electron scattering or electron capture by these interface traps can significantly reduce $I_{on}$. The As-As anti-bonding state is the most likely culprit which is responsible for Fermi level pinning and the poor on-state performance of 3 nm InGaAs channels.

### 4.3.3    Effective channel mobility of ultra-thin channels

In Fig. 4.16, we compare the C-V curves and the effective channel mobility for a 4.5 nm InGaAs channel, a 2.5 nm InAs channel, and a 5 nm InAs channel. The channel effective mobility ($\mu_{eff}$) can be calculated by the following equations [21].

$$\mu_{eff} = \frac{L_g}{W_g} \frac{1}{Q_s(V_g)} \frac{I_D(V_g)}{V_D} \tag{4.1}$$

$$Q_s(V_g) = \int C_{g-ch} dV_g \tag{4.2}$$
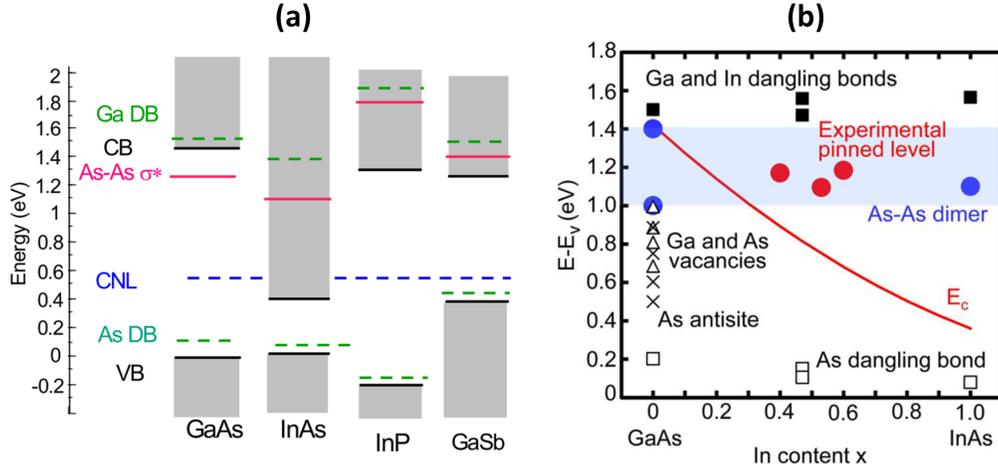
Figure 4.15: (a) The interface trap energy calculated by density-functional theory by J. Robertson [18]. (Note: CB=conduction band, VB=valence band, CNL=charge neutrality level, DB=dangling bond, and $\sigma^*$=anti-bonding) (b) High indium content channels lower minimum conduction band edge and reduce the interactions between channel electrons and the traps above conduction band [20].

Clearly, in Fig 4.16(a), when thinning the InAs channel from 5 nm to 2.5 nm, the effective gate capacitance increases. Using 4.5 nm InGaAs channels also increases effective gate-to-channel capacitance as compared to 5 nm InAs channels because of larger effective mass with resultant larger density of state capacitance, and slightly thin channels. Also, the threshold voltage shifts to positive when the channel is made thinner or the channel band-gap increases from InAs to InGaAs. Fig. 4.16(b) shows the effective channel mobility for 25 $\mu$m $L_g$ devices. The 5 nm InAs channels show the effective mobility near 1100 cm$^2$/V·s, while 2.5 nm InAs channels only show the effective mobility $\sim$250 cm$^2$/V·s. In contrast, 4.5 nm InGaAs channels only maintain the effective mobility$\sim$300 cm$^2$/V·s. Because of large C-V dispersions and low drain current $I_D$ as compared to $I_G$, the mobility of 3 nm InGaAs channel can not be extracted.
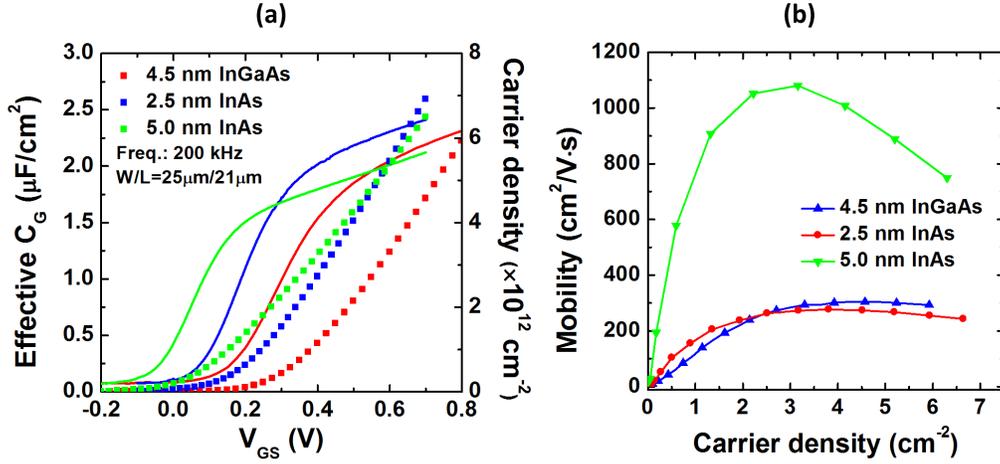
Figure 4.16: (a) Comparison of capacitance-voltage measurements for 4.5 nm InGaAs, 2.5 nm InAs, and 5 nm InAs channels. (b) The extracted effective channel mobility using split C-V measurements for different channel designs.(The results of InAs channels provided from Sanghoon Lee)

When transistors operate on drift-diffusion limits (long $L_g$ devices), the effective channel mobility is an important parameter for on-state performance. High channel mobility enables higher on-state current and transconductance. However, when transistors approach ballistic limits, mobility becomes less important. Instead, the channel effective mass, the effective gate capacitance, and the parasitic source/drain resistance become increasingly important for shorter $L_g$ devices. The effective mass determines the carrier injection velocity. Careful selection of channel effective mass which mitigate the density-of-state bottleneck and maintain high injection velocity allows high on-state performance of the ballistic MOSFETs. On the other hand, the effective gate capacitance is determined by oxide capacitance and semiconductor capacitance, as discussed in chapter 2.1. Higher gate capacitance not only requires extremely thin gate dielectrics, but also extremely thin channels because in thin channels the centroid of electron wave-function is closer

to the oxide/semiconductor interface. Therefore, for ballistic III-V MOSFETs at sub-10-nm nodes, $m^*$ and $C_{g-ch}$ should be optimized more carefully rather than channel mobility for the design of ballistic MOSFETs.

## 4.4    Record high performance III-V FET: 2.7 nm InAs channel and $ZrO_2$

Given the aforementioned knowledge of channel design, we fabricated a 2.7 nm InAs channel MOSFET with a $ZrO_2$ gate dielectric and a 12 nm InGaAs source/drain spacer. The source/drain spacers design will be discussed in detail in chapter 5. The sample was fabricated and reported in VLSI 2014 by Sanghoon Lee [4]. This device shows the record on-state performance among all the III-V MOSFETs and is comparable to 22 nm Si FinFET.

Fig. 4.17 shows the cross-sectional scanning transmission electron microscopy (STEM) image of a 25 nm-$L_g$ InAs MOSFET. The FET has a 2.7 nm InAs channel, and a 1 nm $AlO_xN_{1-x}$ interfacial layer and a 2.5 nm $ZrO_2$ gate dielectric layer. The source/drain region has a 12 nm unintentionally-doped InGaAs vertical spacer, followed by a N+ InGaAs source/drain contact layer. The device structure is shown in Fig. 4.18(a). Fig. 4.18(b) shows the transfer characteristic, and Fig. 4.18(c) shows subthreshold characteristic, and Fig. 4.18(d) shows the output characteristic of a 25 nm-$L_g$ FET. Despite the extremely thin channel, high extrinsic transconductance $\sim$2.4 mS/$\mu$m, and high $I_{on}\sim$500 $\mu$A/$\mu$m at $I_{off}$=100 nA/$\mu$m and $V_{DS}$=0.5 V can still be obtained. The $SS$ is 77 mV/dec for 25 nm-

$L_g$, showing excellent short channel control for a planar MOSFET. The on-state resistance ($R_{on}$) of 25 nm-$L_g$ FETs is about $\sim$300 $\Omega\cdot\mu$m, consisting 25 $\Omega\cdot\mu$m from source/drain ohmic contact, 60 $\Omega\cdot\mu$m from source/drain sheet resistance, 75 $\Omega\cdot\mu$m from the InGaAs source/drain spacer, and 60 $\Omega\cdot\mu$m from the ballistic resistance and the rest of 80 $\Omega\cdot\mu$m from 25 nm InAs channel resistance. Fig. 4.18(e) compares the $I_{on}$ at fixed $I_{off}$=100 nA/$\mu$m with the recently published III-V FETs. The devices show the highest $I_{on}$ among all the III-V MOSFETs and have similar performance to the state of art 22 nm Si FinFET [22]. Fig. 4.18(f) shows subthreshold characteristic of a 1 $\mu$m-$L_g$ FET. Nearly ideal subthreshold swing $SS\sim$61 mV/dec. and negligible hysteresis when alternating bias directions were observed, indicating that the superior oxide/smiconductor interface and very low interface trap density. More details regarding to this device and the high-k gate dielectric can be found in [4] and [23].

## 4.5    Summary

InGaAs and InAs channels in quantum well 2DEGs show different transport properties from surface channel MOSFETs. Low field mobility of InGaAs and InAs quantum well 2DEGSs converge at 2 nm well thickness, while thin InAs channels show significant higher on-state current than InGaAs channels. We attribute the performance improvement of InAs channels to less channel electron interaction with the interface traps, having energy levels above conduction band edge. Because of non-parabolic conduction band and strong quantum confine-
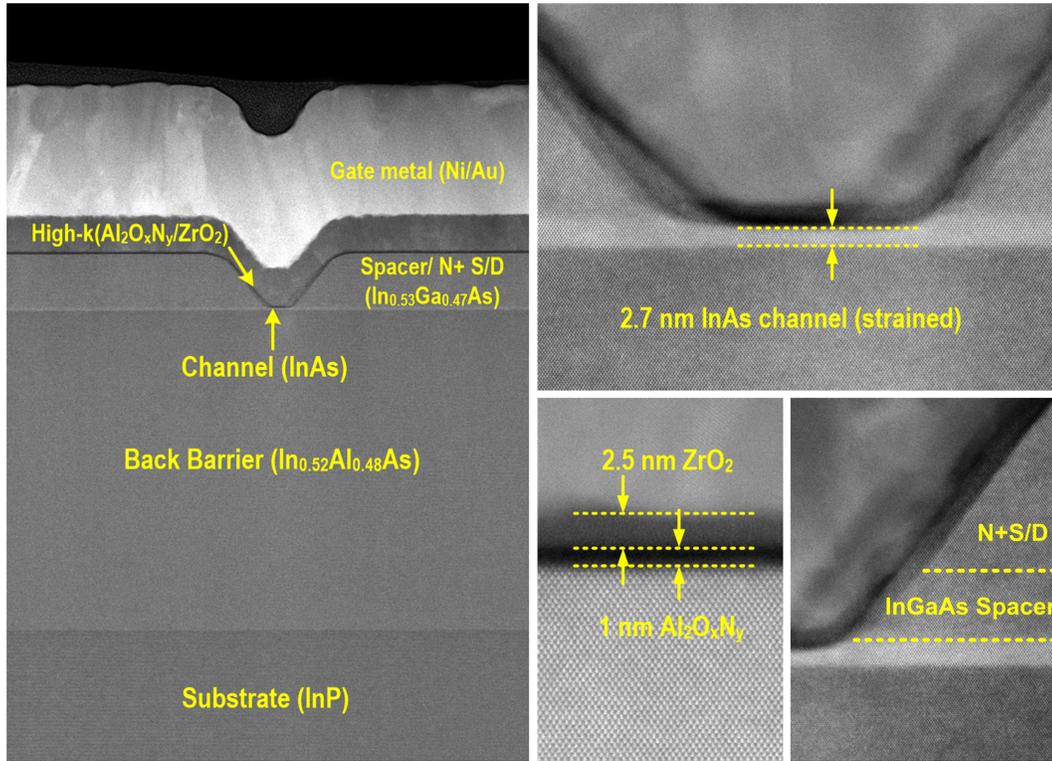
Figure 4.17: The cross-sectional STEM images of 25 nm-$L_\text{g}$ InAs MOSFETs, showing $\sim$2.7 nm InAs channel, $\sim$1 nm AlO$_x$N$_{1-x}$ interfacial layer and $\sim$2.5 nm ZrO$_2$ gate dielectric. The source/drain has $\sim$12 nm un-doped InGaAs vertical spacer and the N+InGaAs contact layers.(Courtesy of Sanghoon Lee)

ment effects, InGaAs and InAs might have similar effective mass (same curvature of E-k diagram) at channel thickness about 2$\sim$3 nm. However, the conduction band minimum is lower for InAs than InGaAs, thus reducing the electron interactions with the oxide traps; the traps believed from the As-As anti-bonding. With respect to off-state leakage, InGaAs channels have lower band-to-band tunneling leakage because of larger band-gap, making InGaAs channels more suitable for low standby power logic applications.

Using a 2.7 nm InAs channel with a highly scaled ZrO$_2$ gate dielectric, the 25 nm-$L_\text{g}$ FET shows transconductance 2.4 mS/$\mu$m, $SS\sim$77 mV/dec., minimum
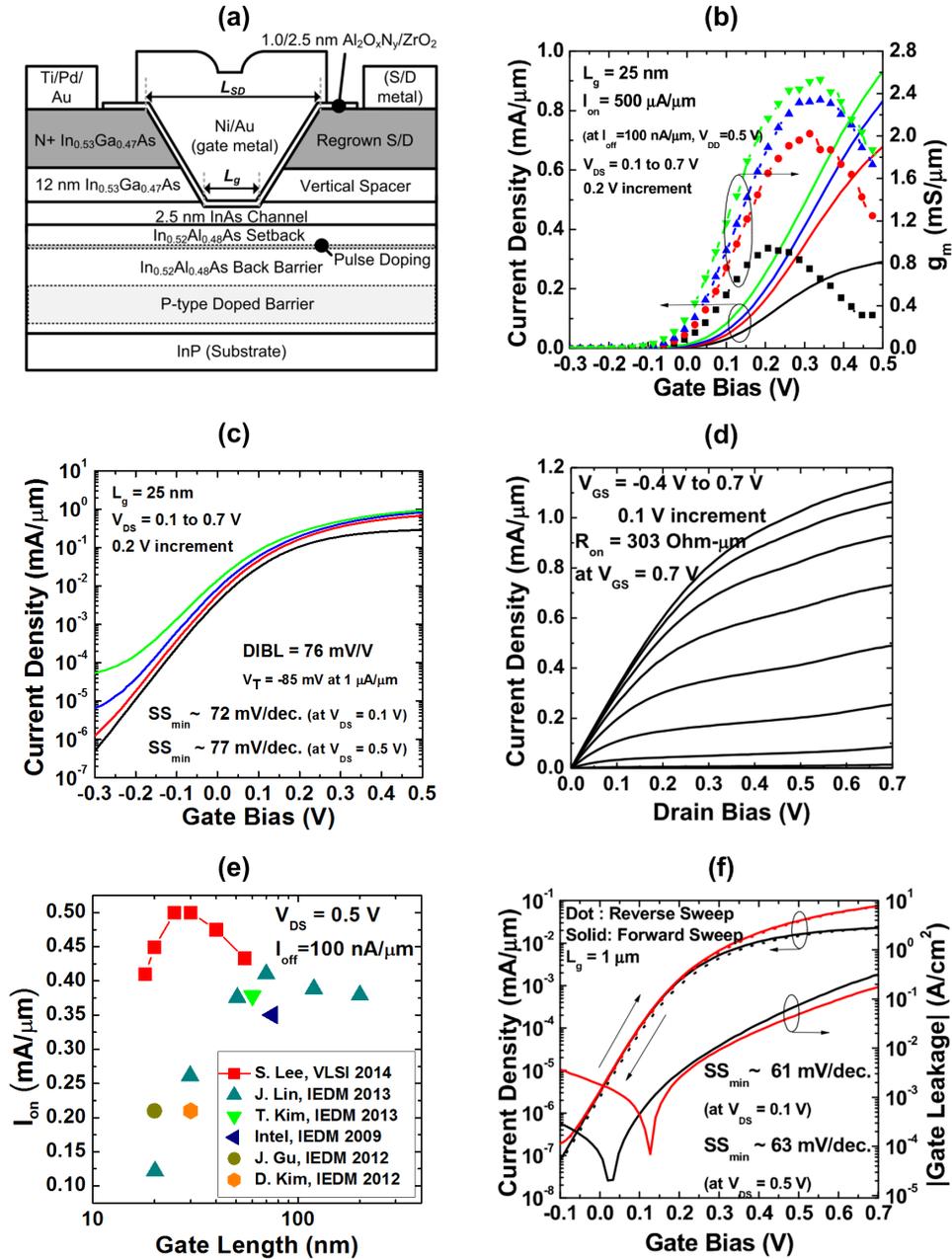
Figure 4.18: (a) Device schematics, (b) the transfer characteristic, (c) the subthreshold characteristic, and (d) the output characteristic of a 25 nm-$L_g$ InAs MOSFET. (e) Benchmark of $I_{on}$ at fixed $I_{off}$=100 nA/$\mu$m to recent published III-V MOSFETs. (f) The subthreshold characteristics of $L_g$-1 $\mu$m device, showing $SS$=61 mV/dec.(Courtesy of Sanghoon Lee)

$I_{\mathrm{off}}{\sim}10$ nA/$\mu$m, and $I_{\mathrm{on}}{=}500$ $\mu$A/$\mu$m at $I_{\mathrm{off}}{=}100$ nA/$\mu$m and $V_{\mathrm{DS}}{=}0.5$ V. This InAs FET shows the highest on-state performance among all the III-V MOSFETs, and has comparable performance to advanced 22 nm Si FinFETs.

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# Chapter 5

# Source-Drain Engineering: InGaAs and InP Source/Drain Spacers

III-V InGaAs/InAs MOSFETs, despite showing high on-state current, suffer from high off-state leakage and cannot be properly turned off. Off-state leakage current ($I_{\text{off}}$) increases as gate lengths decrease and high $I_{\text{off}}$ might eventually limit the device scalability, rendering III-V MOSFETs unsuitable for VLSI logic applications. Due to small band-gap energy of III-V materials, III-V channels are vulnerable to high band-to-band tunneling (BTBT) and impact ionization at the high field regions near the drain end of the channel. On the other hand, III-V materials have larger permittivity, resulting in deteriorated MOSFET electrostatics due to stronger drain-to-channel capacitance coupling (i.e. drain-induced barrier lowering). High off-state leakage currents also degrade subthreshold swing and reduce the on-state current at fixed $I_{\text{off}}$ and $V_{\text{DD}}$. In chapter 4.4, we have demonstrated a 2.7 nm InAs channel MOSFET, showing minimum $I_{\text{off}}$ $\sim$10 nA/$\mu$m and simultaneously achieving record on-state current ($I_{\text{on}}$=500 $\mu$A/$\mu$m at 100 nA/$\mu$m $I_{\text{off}}$ and $V_{\text{DS}}$=0.5 V). However, 10 nA/$\mu$m $I_{\text{off}}$ is still too large to utilize III-V MOSFETs for standard performance (SP, $I_{\text{off}} = 1$ nA/$\mu$m) and low power (LP, $I_{\text{off}} = 30$ pA/$\mu$m) logic applications. Therefore, off-state leakage current must be further reduced if III-V MOSFETs are targeted at low standby power mobile computing. New leakage reduction techniques other than channel thickness scaling are highly desirable because continuous thinning the channel causes severe performance degradation.

In the past two decades, source-drain stress engineering has become the powerful engine to drive higher on-state current in Si MOSFETs. For example, SiGe as a source-drain stressor for p-channel MOSFETs (PMOS) was implemented since 90 nm logic node [1]. SiGe source/drain stressor induces the uniaxial compres-

sive strain in Si channels, increasing hole mobility and PMOS on-state current. On the counterpart, carbon and phosphorous doped Si (Si:CP) source/drain [2] and stress memorization technology (SMT) [3] were recently introduced in Si n-channel MOSFETs (NMOS) to induce tensile strain in Si channels, enhancing electron mobility and NMOS on-state current. In addition to stress engineering, the doping profile of source/drain junctions have significant impacts on the leakage current of Si MOSFETs [4–6]. Lightly-doped drain (LDD) structure was widely used in Si MOSFETs to reduce series resistance beneath the gate sidewall spacers. It was also observed that the doping profile of channel/LDD junction significantly affected the gate-induced drain leakage (GIDL) [4,5]. However, as to III-V MOSFETs, the knowledge of source-drain engineering is still very limited, and is waiting for extensive explorations.

In this chapter, we start to engineer the source/drain regrowth in the ultra-thin-body III-V MOSFETs. It was found that the source-drain design has profound impact on the off-state leakage and the subthreshold characteristics of ultra-thin-body III-V MOSFETs. We begin with a review on molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) source/drain regrowth in UC Santa Barbara. Subsequently, we investigate the raised source/drain spacers (InGaAs or InP) [7, 8] and recessed InP source/drain spacers on III-V MOSFETs [9]. Moreover, we optimize the doping profile at the source/drian vertical spacer to improve the on-state performance and off-state leakage currents. Finally, we conclude this chapter by demonstrating a record low leakage III-V MOSFET with minimum $I_{\text{off}} \sim 60$ pA/$\mu$m at 30 nm $L_{\text{g}}$ [10]. With the invention of recessed doping graded InP source/drain spacers, III-V MOSFETs, for the first

time, are eligible for low standby power logic applications.

## 5.1  MBE and MOCVD source/drain regrowth

In this section, we briefly review MBE and MOCVD source-drain regrowth. Table 5.1 summarizes the doping concentration of InGaAs and InAs grown by MBE and MOCVD in UC Santa Barbara. Although MBE regrowth can achieve higher doping concentration, MBE regrowth is difficult to achieve high selectivity, leaving unwanted polycrystalline materials grown on the oxide mask. The non-selective regrowth causes large process variations and more complicate planarization process is required to remove the unwanted materials. To achieve higher selectivity of MBE growth, metal-enhanced epitaxy (MME), with As shutter always open but group-III shutter open intermittently, is implemented [11, 12]. The MME InGaAs achieves $4 \times 10^{19}$ cm$^{-3}$ and MME InAs achieves $7 \times 10^{19}$ cm$^{-3}$ doping concentrations at 450 °C growth temperature. Higher growth temperature improves selectivity, but reduces the doping concentration. The detailed growth behavior can be found in [11, 12].

In contrast, MOCVD regrowth has higher selectivity and higher throughput as compared to MBE regrowth. The selectivity of MOCVD growth depends on several growth parameters, including growth temperature, reactor pressure, carrier gas, precursor species and precursor partial pressure. Because MOCVD regrowth temperature is usually much higher than MBE regrowth, higher selectivity of MOCVD regrowth can be obtained. The MOCVD regrowth also has the advan-

tage of growth uniformity because the laminar carrier flow (hydrogen) distributes the precursor uniformly across the wafers, and the growth rate is typically limited by the precursor diffusion through the boundary layer (mass transfer limited) under current growth conditions. For the mass transfer limited growth, the growth rate is insensitive to the growth temperature, and well-controlled by the precursor concentration. In UCSB III-V MOCVD system, a high concentration disilane $(Si_2H_6$, 400 pm) bottle was installed as a n-type dopant source, enabling higher doping concentration of InGaAs than that using silane $(SiH_4)$ source. MOCVD grown Si-doped InGaAs can reach $4 \times 10^{19}$ cm$^{-3}$ active carrier concentration obtained from Hall measurement. In addition to InGaAs source/drain layers, InP and InAs source/drain regrowth have been developed, allowing us to do the band-gap engineering in the source/drain regions. We found that heavily doped InP layers grown at 600 °C gave rise to rough and hazy surface because the Si precipitate could disrupt the epitaxial layer growth [13]. By lowering the growth temperature of N-doped InP from 600 °C to 550 °C, the surface of heavily doped InP layers is greatly improved. Since an active Si dopant must occupy the group III sites of the lattice, the group III precursors (TMI) are competing with Si dopant during the growth. By lowering TMI flow and the growth rate from 3.9 Å/s to 1.95 Å/s, more Si dopant can be incorporated into group III sites, providing a higher doping concentration in InP layers. The highest doping concentration of Si-doped InP is about $5.5 \times 10^{19}$ cm$^{-3}$, obtained from Hall measurements.

Heavily doped InAs growth, unfortunately, is relatively difficult in UCSB MOCVD as compared to MBE growth. The large lattice mismatch between InAs and InP causes a high density of defects in the epitaxial layer. Lowering the growth

| Technique | Materials | Growth temperature (°C) | Growth rate (Å/s) | Sheet resistance ($\Omega/\square$) | Active carrier density ($10^{19}$ cm$^{-3}$) | Hall mobility (cm$^2$/V·s) |
|---|---|---|---|---|---|---|
| MBE-MME | InAs | 450 | 0.7 | 18.1 | 7.05 | 980 |
| MBE-MME | InAs | 500 | 0.7 | 19.4 | 5.98 | 1070 |
| MBE-MME | InGaAs | 450 | 1.33 | 31.5 | 4.01 | 990 |
| MOCVD | InGaAs | 600 | 1.75 | 22.9 | 4.00 | 1360 |
| MOCVD | InP | 550 | 3.9 | 95.5 | 1.98 | 660 |
| MOCVD | InP | 550 | 1.95 | 56.1 | 5.50 | 400 |
| MOCVD | InAs | 520 | 4.2 | 213.1 | 1.05 | 380 |

Table 5.1: The doping concentration of source/drain layers grown by MBE and MOCVD. In MBE system, MME represents metal-modulation epitaxy [11, 12]. Si and Te co-doping were used with Si cell at 1395 °C and Te cell at 635 °C. In MOCVD, 400 ppm disilane was used with disilane flow 40/45/10 (out/in/dilution).

temperature can improve the crystalline quality and reduce sheet resistance, but the decomposition efficiency of disilane might decrease quickly at lower growth temperature [14]. Therefore, to simultaneously achieve high crystalline quality as well as high doping concentration might be challenging for InAs because of very narrow growth windows. Further study on MOCVD InAs growth is highly desirable because InAs material has electron Fermi level naturally pinned above the conduction band edge, thereby being the best candidate for n-type contact layers among all the III-As/P materials [15].

## 5.2 Raised InGaAs and InP source/drain spacers

Fig. 5.1 shows device structures of InAs/InGaAs channel MOSFETs with N+InGaAs source/drain (sample 5.2A), N+InP source/drain (sample 5.2B), and unintentionally-doped InP source/drain spacers (sample 5.2C). The epitaxial structures consist of a semi-insulating InP substrate, a 50 nm unintentionally-doped (U.I.D.) InAlAs layer, a 250 nm $1 \times 10^{17}$ cm$^{-3}$ Be-doped InAlAs layer, a 100 nm U.I.D. InAlAs layer, a 2 nm $1 \times 10^{19}$ cm$^{-3}$ Si-doped InAlAs modulation-doped layer, a 5 nm U.I.D. InAlAs setback layer, a 3 nm InGaAs sub-channel, a 6 nm InAs channel, and a 4 nm InGaAs cap. HSQ dummy gates were patterned by e-beam lithography. Before source/drain (S/D) regrowth, $\sim$2 nm of the InGaAs cap at the S/D region was digitally etched using UV ozone and dilute HCl. The samples were then transferred to an MOCVD reactor for S/D regrowth. Sample 5.2A has a 50 nm N+InGaAs regrowth. Sample 5.2B and sample 5.2C incorporate a 10 nm N+InP ($2 \times 10^{19}$ cm$^{-3}$) S/D and a 10 nm U.I.D. InP spacer between the channel and the N+InGaAs S/D, respectively. The devices were then isolated and three cycles of digital etch removed the 4 nm InGaAs cap in the channel region. After transferring to atomic layer deposition (ALD) reactor, the surface was prepared by TMA/nitrogen plasma cycles, and 2.9 nm HfO$_2$ was deposited. Ni gates and Ti/Pd/Au S/D contacts were defined using liftoff.

Fig. 5.2 shows the transfer characteristics and output characteristics of $L_\mathrm{g}$-65 nm devices for sample 5.2A, 5.2B and 5.2C. Sample 5.2A shows very high transconductance about 3.0 mS/$\mu$m at $V_\mathrm{DS}$=0.5 V. Sample 5.2B with a N+InP source

**Sample 5.2A**

| Ti/Pd/Au | Ni/Au | Ti/Pd/Au |
|---|---|---|
| 50 nm N+ InGaAs | | 50 nm N+ InGaAs |

2 nm InGaAs

| 6 nm InAs |
| 3 nm InGaAs |
| 5 nm InAlAs U.I.D. spacer |
| 2 nm 1E19 cm$^{-3}$ Si-doped InAlAs |
| 100 nm InAlAs U.I.D. buffer |
| 250 nm 1E17 cm$^{-3}$ p-InAlAs buffer |
| 50 nm InAlAs U.I.D buffer |
| Semi-insulating InP substrate |

**Sample 5.2B**

| Ti/Pd/Au | Ni/Au | Ti/Pd/Au |
|---|---|---|
| 50 nm N+ InGaAs | | 50 nm N+ InGaAs |
| 10 nm N+ InP | | 10 nm N+ InP |

2 nm InGaAs

| 6 nm InAs |
| 3 nm InGaAs |
| 5 nm InAlAs U.I.D. spacer |
| 2 nm 1E19 cm$^{-3}$ Si-doped InAlAs |
| 100 nm InAlAs U.I.D. buffer |
| 250 nm 1E17 cm$^{-3}$ p-InAlAs buffer |
| 50 nm InAlAs U.I.D buffer |
| Semi-insulating InP substrate |

**Sample 5.2C**

| Ti/Pd/Au | Ni/Au | Ti/Pd/Au |
|---|---|---|
| 50 nm N+ InGaAs | | 50 nm N+ InGaAs |
| 10 nm U.I.D InP | | 10 nm U.I.D InP |

2 nm InGaAs

| 6 nm InAs |
| 3 nm InGaAs |
| 5 nm InAlAs U.I.D. spacer |
| 2 nm 1E19 cm$^{-3}$ Si-doped InAlAs |
| 100 nm InAlAs U.I.D. buffer |
| 250 nm 1E17 cm$^{-3}$ p-InAlAs buffer |
| 50 nm InAlAs U.I.D buffer |
| Semi-insulating InP substrate |

Figure 5.1: Device structures of sample 5.2A with N+InGaAs source/drain, sample 5.2B with N+InP source/drain, and sample 5.2C with 10 nm undoped InP source/drain spacers.

shows comparable on-state and off-state performance to Sample 5.2A, showing a transconductance of 2.95 mS/$\mu$m at $V_{DS}$=0.5 V. The subthreshold swing ($SS$) of $L_g$=65 nm devices for both sample 5.2A and 5.2B is ~150 mV/dec at $V_{DS}$=0.5 V. It is noted that Yonai et al. report that the N+InP source can mitigate the source starvation and increase on-state current because the InP/InGaAs heterojunction has 0.2 eV conduction band offset and improves the charge supply from InP source to InGaAs channel [16]. Our result, in contrast to [16], shows no significant improvement on on-state current and transconductance after incorporating the N+InP source. However, note that even sample 5.2A has a conduction-band offset between the N+InGaAs source and the InAs channel. Moreover, the different source/drain parasitic resistance from N+InGaAs ($4 \times 10^{19}$ cm$^{-3}$) and N+InP ($2 \times 10^{19}$ cm$^{-3}$) might make it difficult to differentiate the impacts of parasitic source/drain resistance and the source-to-channel heterojunctions.

Adding a 10 nm U.I.D. InP spacer (sample 5.2C), significantly improves the subthreshold swing ($SS$=114 mV/dec. at $V_{DS}$=0.5 V) and reduces $I_{off}$ of a $L_g$=65 nm device, as shown Fig. 5.2(c). Transconductance remains high ($g_m$~2.6 mS/$\mu$m

105

**(a)**



**(b)**



**(c)**
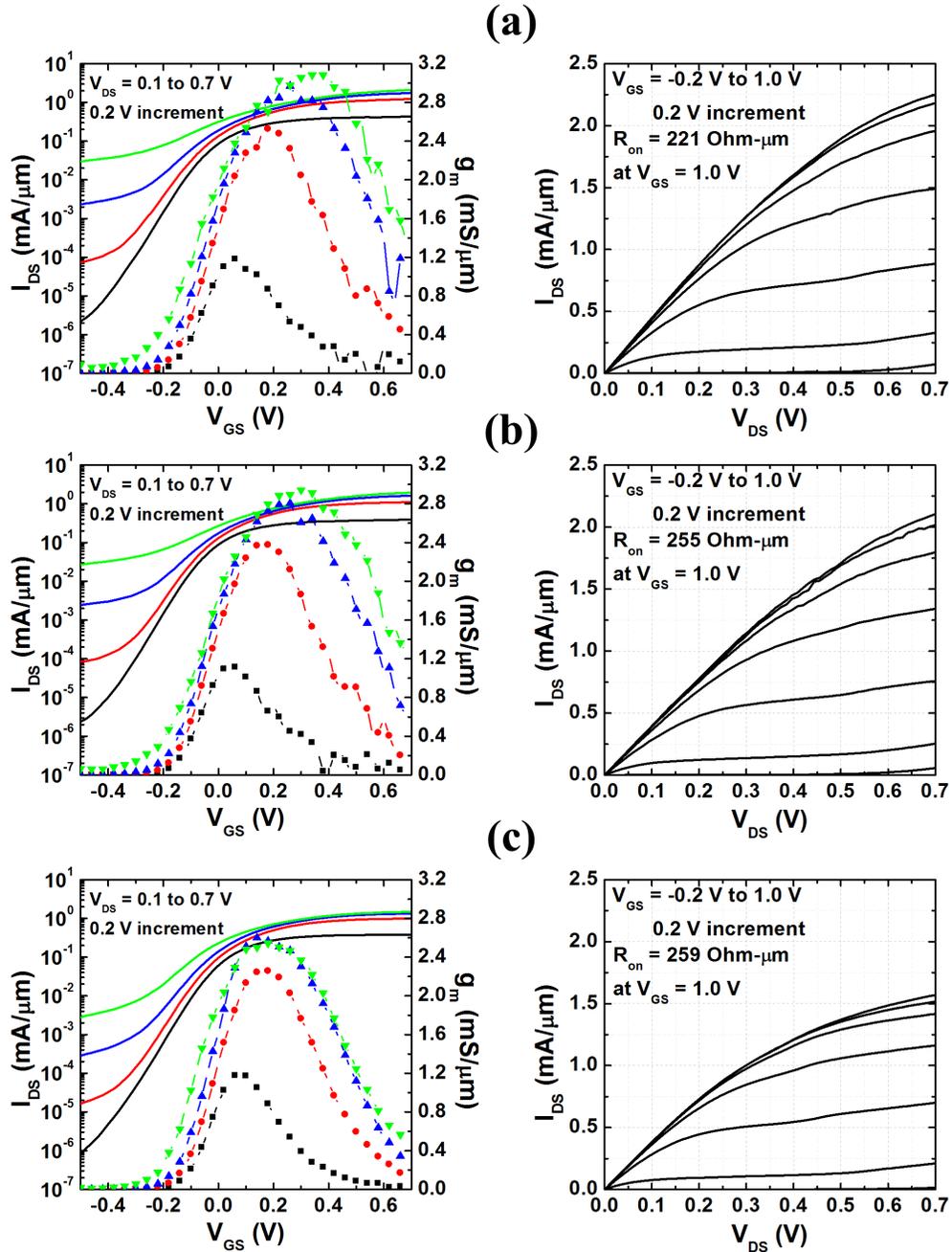
Figure 5.2: Transfer and output characteristics of $L_g$=65 nm devices for (a) sample 5.2A, (b) sample 5.2B, and (c) sample 5.2C.

at $V_{\mathrm{DS}}$=0.5 V). The minimum off-state leakage of sample 5.2C (10 nm U.I.D. InP spacer) is 250 nA/$\mu$m, one order smaller than that of sample 5.2A and 5.2B. High off-state leakage with resultant high subthreshold swing in samples 5.2A and 5.2B is caused by band-to-band tunneling leakage. Fig. 5.3 compares sample 5.2C to the FETs with similar channel design but InGaAs raised source/drain spacers [7]. The leakage current of sample 5.2C is similar to FETs with an 8 nm InGaAs spacer. It is evident that increasing spacer thickness reduces $SS$ and minimum $I_{\mathrm{off}}$, but the raised InP spacers show minimum off state leakage no lower than InGaAs spacers. Therefore, we conclude that it is the spacer thickness, and not its band-gap, which determines the minimum $I_{\mathrm{off}}$. This implied that the raised source/drain spacers reduce $I_{\mathrm{off}}$ mainly through decreased electric field at the drain end of the channel, and most band-to-band tunneling leakage currents occur at or closer to the channel, not in the raised source/drain region. Since reducing the off-state leakage current is not a credit to the spacer band-gap, InGaAs source/drain spacers is more preferred than InP spacers because N+InGaAs source to InGaAs spacers and channels has less junction resistance. Examining the output characteristics of sample 5.2C (Fig. 5.2(c)), under large positive gate bias ($V_{\mathrm{GS}}$ >0.5 V) $I_{\mathrm{on}}$ is reduced; the energy barrier at the interface of the N+InGaAs and the U.I.D. InP spacer limits the source electron supply to the InAs/InGaAs channel, thereby reducing the maximum $I_{\mathrm{on}}$.

Fig. 5.4(a) shows transconductance $g_{\mathrm{m}}$ versus $L_{\mathrm{g}}$ for samples 5.2A, 5.2B, and 5.2C. All the samples show high $g_{\mathrm{m}}$, with a slight degradation ($\sim$10%) for sub-100 nm-$L_{\mathrm{g}}$ devices on Sample 5.2C. Fig. 5.4(b) shows $SS$ versus $L_{\mathrm{g}}$. The insertion of the U.I.D. InP spacer significantly improves $SS$ at short gate lengths. Fig.
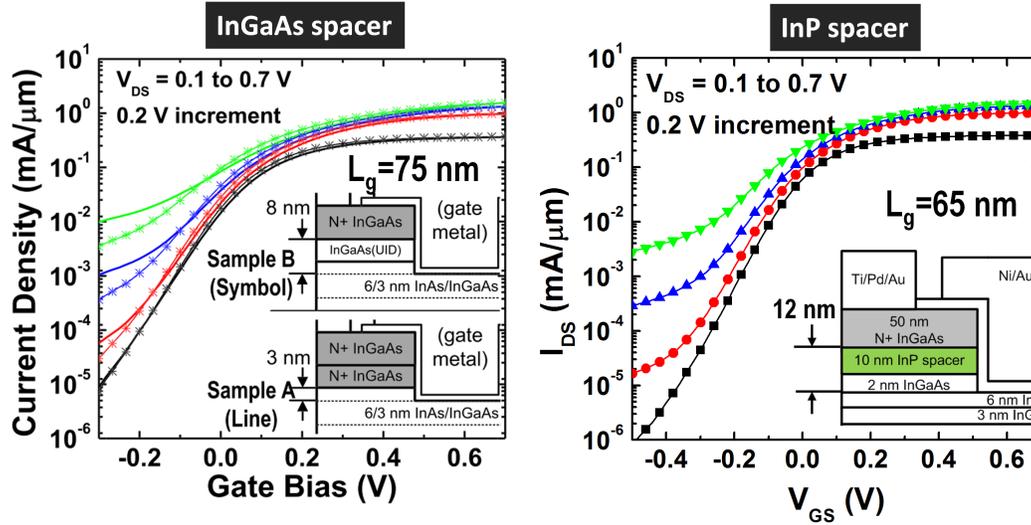
Figure 5.3: Comparison of raised InGaAs spacers and raised InP spacers for FETs with the similar channel design. The result of raised InGaAs spacers were reported by Sanghoon Lee [7].

5.5 compares the $g_m$ and $SS$ of this work to recently reported III-V MOSFETs. The U.I.D. InP vertical spacer shows performance similar to the U.I.D. InGaAs vertical spacer [7]. In contrast to FETs using lateral gate-drain spacing to control $SS$ and $I_{off}$ [17,18], the source/drain vertical spacer allows continuous scaling of the S/D contact pitch, as is necessary in VLSI.

In summary, the un-doped raised source/drain spacers, either InGaAs or InP, slightly increase the effective gate length (i.e. electron transport length), smooth the electric field near the drain side, improve devices electrostatics (lower $DIBL$ and $SS$), and reduce band-to-band tunneling current. The source/drain spacers thickness must be optimized separately with respective channel designs and gate lengths. With the optimized InGaAs spacer thickness, the subthreshold characteristic can be greatly improved while FETs still maintaining high on-state performance. Most importantly, note that in this section the InP wide band-gap

**(a)**



**(b)**
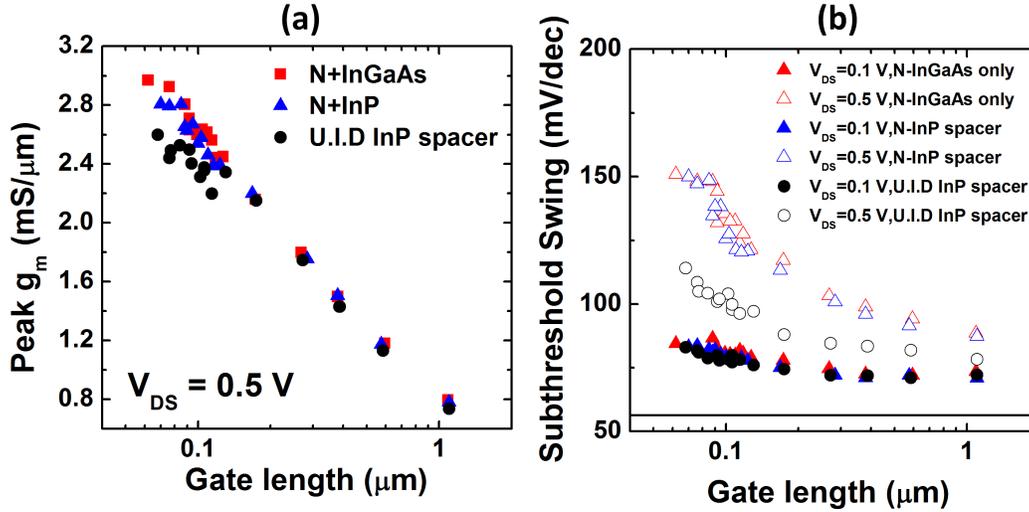


Figure 5.4: (a) Comparison of $g_m$ versus $L_g$ for samples 5.2A, 5.2B, and 5.2C. (b) Comparison of $SS$ versus $L_g$ for samples 5.2A, 5.2B, and 5.2C.
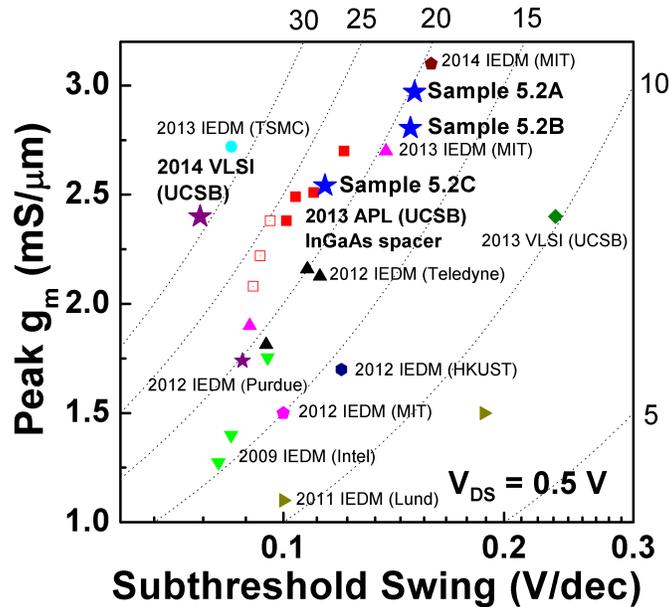


Figure 5.5: Benchmark of $g_m$ and $SS$ for the three samples in this section to recently reported III-V MOSFETs.

spacers are placed in the raised source/drain region. In the next section, we will regrow InP spacers in the recessed source/drian regions. Afterward, this recessed InP source/drain spacer becomes a disruptive innovation that, for the first time, enables III-V MOSFETs viable for low power logic applications.

## 5.3   Recessed InP source/drain spacer and InP channel cap

As gate lengths decrease, the electric field becomes extremely strong near the drain region. The concentrated electric field near the drain side results in non-local band-to-band-tunneling (BTBT) leakage in the devices. This BTBT leakage can be further amplified by lateral bipolar effects, in which the holes generated by BTBT accumulate at the source side of the channel, forward-biasing the source-to-channel junction and leading to excess off-state leakage (see section 2.2.3 and [19]). In section 5-2, replacing a raised InGaAs source/drain spacer with a raised InP spacer does not further reduce the minimum off-state leakage. Strong electric field at the drain side of the channel still results in large BTBT leakage. Chu et al. simulated the electric field distribution for the V-gate GaN high electron mobility transistor (HEMT), indicating that the electric field is crowed at the gate edge near the drain-side [20]. Recently, Lin et al. simulated the BTBT contour in the quantum well III-V MOSFETs, also showing large BTBT generation at the gate edge near the drain-side [19]. These simulation results indicate that the band-to-band tunneling is likely to occur around the gate edge at the drain side

**Sample 5.3A**   **Sample 5.3B**   **Sample 5.3C**
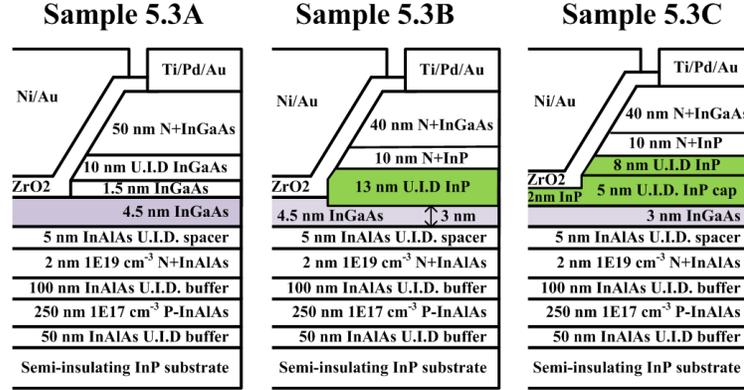


Figure 5.6: Devices structures of sample 5.3A (raised InGaAs spacer), 5.3B (recessed InP spacer), and 5.3C (InP cap layer). The devices have symmetric source/drain and only the drain side of the devices is shown here.

of the channel, not at the raised source/drain region. Therefore, we suspect that replacing the narrow band-gap InGaAs with wide band-gap InP at the gate edge where the electric field is crowded should help reduce band-to-band tunneling [9].

To examine this idea, three samples were fabricated with the detailed structures shown in Fig. 5.6. All samples have the same back barrier design, and a 6 nm thick $In_{0.53}Ga_{0.47}As$ channel grown by MBE. The final channel thickness is controlled by digital etch before oxide deposition. Sample 5.3A has a 4.5 nm InGaAs channel and a InGaAs source/drain spacer. Sample 5.3B has a 4.5 nm InGaAs channel and a partially recessed InP spacer. Sample 5.3C has a MOCVD grown InP cap layer atop a 3 nm InGaAs channel and the subsequent MOCVD grown an 8 nm InP spacer above the InP cap layer. Note that in sample 5.3C, the high field region at the corner of the gate edge is completely surrounded by wide band-gap InP spacers. To control the similar electrostatics, three samples have similar spacer thickness to ensure fair comparisons.

Fig. 5.7 shows the transfer and output characteristics of $L_g$~22 nm devices

for samples 5.3A, 5.3B and 5.3C. Sample 5.3A shows large off-state leakage current and large subthreshold swing. The $SS$ of sample 5.3A increases as $V_{\text{GS}}$ is made more negative. The off-state leakage decreases only slowly as the gate bias is decreased, especially at higher drain bias (ca, $V_{\text{DS}}$=0.7 V). This saturated leakage floor, dominated by band-to-band tunneling, limits the device scalability and makes III-V MOSFETs unsuitable for low power logic ($I_{\text{off}}$~1 nA/$\mu$m for SP and $I_{\text{off}}$~30 pA/$\mu$m for LP). In contrast, with replacement of InGaAs by wide band-gap InP at high field region, samples 5.3B and 5.3C show significantly improved sub-threshold swing ($SS$) and much lower minimum off-state leakage, with $I_{\text{D}}$ reduced dramatically, 1-2 orders of magnitude as compared to sample 5.3A.

Fig. 5.7 also shows the gate leakage current. For sample 5.3A, drain leakage exceeds gate leakage by 1 to 2 orders of magnitude, being dominated by BTBT. For samples 5.3B and 5.3C, at large negative $V_{\text{GS}}$, gate and drain leakage are equal, indicating that gate-drain leakage dominates the observed off-state drain current, with negligible BTBT. For samples 5.3B and 5.3C, the off-state leakage at large negative $V_{\text{GS}}$ is smaller than 1 nA/$\mu$m, which meets the specification of standard performance logic applications. Note that, for the devices reported here, the gate electrode overlaps both the N+source and the N+drain by more than 500 nm. This results, at 25 nm gate length, in gate-source and gate-drain overlap areas both approximately 20:1 larger than the overlap area between the gate and the channel. Eliminating these large excess areas would reduce the gate leakage current by at least 20:1.

Figs. 5.8(a) and 5.8(b) show the transconductance and on-resistance as a function of gate lengths. At gate lengths smaller than 100 nm, the transconduc-

**(a)**

**(b)**

**(c)**
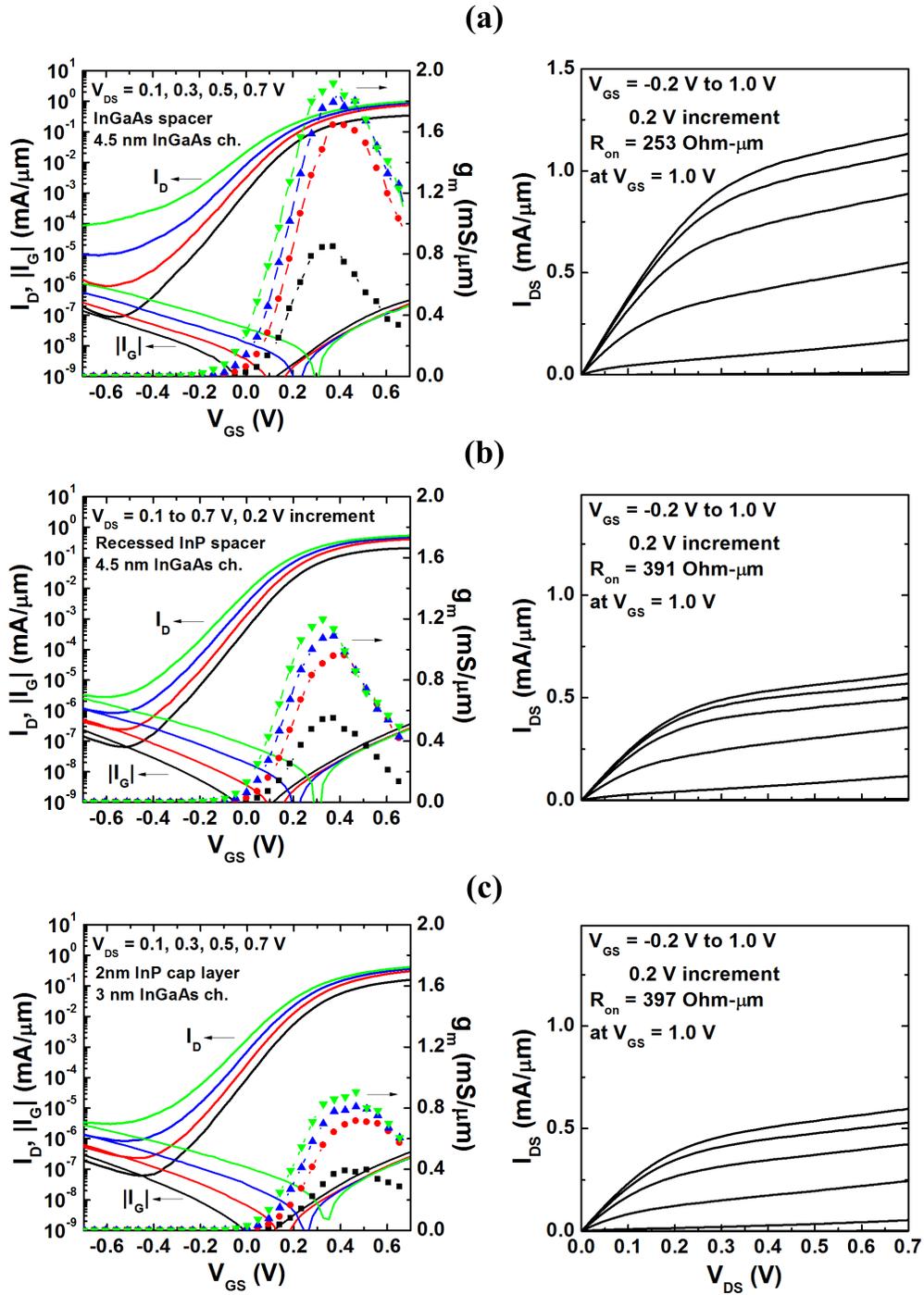
Figure 5.7: Transfer and output characteristics for (a) sample 5.3A, (b) sample 5.3B, and (c) sample 5.3C.

**(a)**

**(b)**
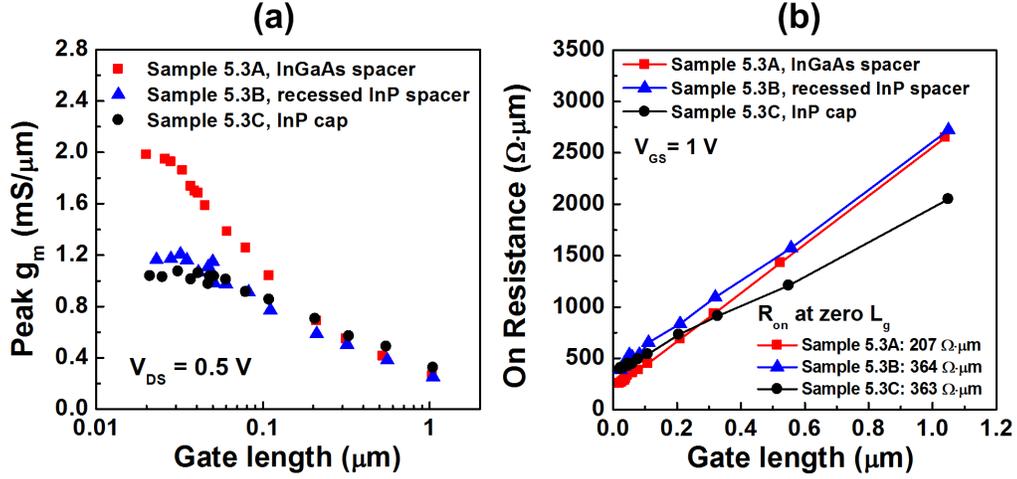
Figure 5.8: Comparison of (a) $g_{\mathrm{m}}$ versus $L_{\mathrm{g}}$ and (b) $R_{\mathrm{on}}$ versus $L_{\mathrm{g}}$ for sample 5.3A, 5.3B, and 5.3C.

tance of samples 5.3B and 5.3C is far below that of sample 5.3A, showing 40~50% smaller transconductance than sample 5.3A at $L_{\mathrm{g}}{\sim}22$ nm. In Fig. 5.8(b), at gate lengths below 100 nm, the drain-source on-resistance $R_{\mathrm{on}}$ of samples 5.3B and 5.3C is substantially larger than that of sample 5.3A, with $R_{\mathrm{on}}$ extrapolated to zero gate length of 207, 364, and 363 $\Omega \cdot \mu$m for samples 5.3A, 5.3B, and 5.3C, respectively. It is evident that the InP spacer greatly increases the parasitic source/drain resistance in the devices. As a result, the on-state performance deteriorates significantly at shorter gate lengths.

In the present designs, the InP S/D spacers (samples 5.3B and 5.3C) suppress BTBT leakage but increase parasitic source/drain resistance. To aid in understanding this trade-off, Fig. 5.9 shows the energy band diagram drawn on a path passing through the N+source and into the channel and the back barrier. Although the reduced current, and increased resistance, might be attributed to conduction-band barriers at InP-InGaAs heterointerfaces, heavy doping at inter-
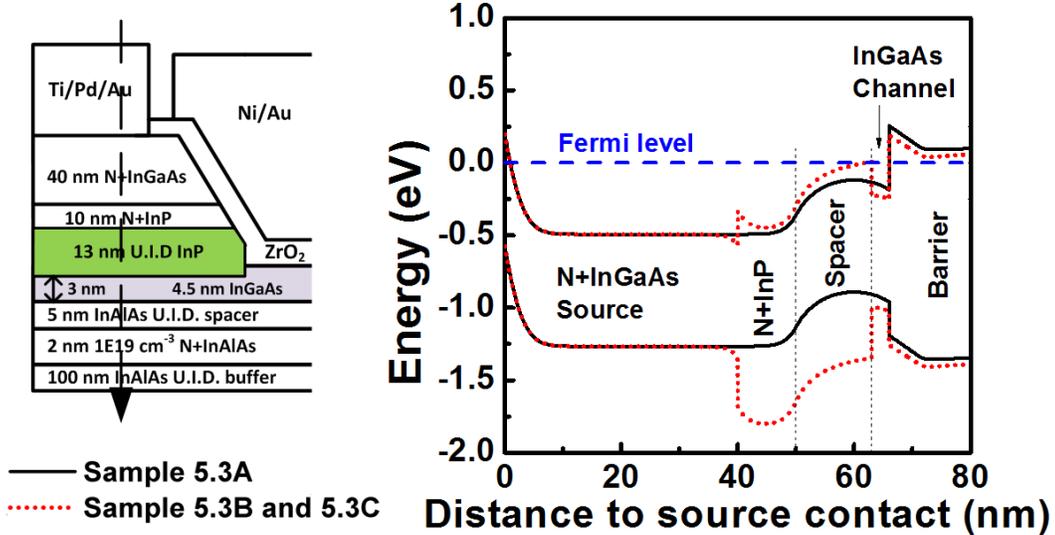
Figure 5.9: Energy band diagrams of the three samples, drawn on a path passing through the N+source and into the channel and the barrier.

faces between the N+InGaAs S/D ($4\times10^{19}$ cm$^{-3}$) and the N+InP ($5\times10^{19}$ cm$^{-3}$) regrowth ensures that conduction-band energy spikes at these interfaces remain well below the Fermi energy, while, because of quantization in the thin channel, the channel bound state is only ~0.1 eV below the InP S/D conduction band edge in sample 5.3B, and only ~0.07 eV below the S/D conduction band edge in sample 5.3C. Instead, we suspect that the reduce $I_{on}$ results from increased access resistance from the thick InP spacer layers.

Electron transport through the source spacer is aided by conduction through a surface electron accumulation layer induced by the gate. Given that the electron affinity in the InP spacer is smaller than that of InGaAs, there is a smaller accumulation electron density at surfaces of the InP spacers than with InGaAs spacers. This increases the on-resistance contribution of InP spacers. By using a

composite graded InP/InGaAs spacer or a doping-graded InP spacer, access resistance may be reduced and on-state current improved, while FETs still maintain low off-state leakage.

## 5.4  Optimization of InP source/drain spacer

In section 5.3, we have reported two techniques—a recessed InP spacer and an InP cap layer—both reduce the off-state leakage to below 1 nA/$\mu$m for $L_g \sim 22$ nm devices. In this section, we will focus on the optimization of recessed InP spacers and the reduction of the parasitic source/drain resistance [10].

### 5.4.1  InP source/drain spacer thickness

The large parasitic resistance caused by InP spacers can be easily reduced by shrinking InP spacer thickness. Here we reduce spacer thickness from 13 nm (sample 5.3B) to 5 nm (sample 5.4A). Fig. 5.10 compares the transfer characteristics of sample 5.3A (11.5 nm InGaAs spacers) and sample 5.4A (5 nm recessed InP spacers) at $L_g$=60 nm. Clearly, the minimum $I_{off}$ is limited by BTBT in sample 5.3A, while $I_{off}$ is limited by gate leakage $I_G$ in sample 5.4A. This result indicates that a 5 nm InP recessed spacer is sufficient to reduce the BTBT. As a result of thinner InP spacers, on-state performance is greatly improved, showing similar transconductance and $I_{on}$ to InGaAs FETs with 11.5 nm InGaAs spacers (sample 5.3A).
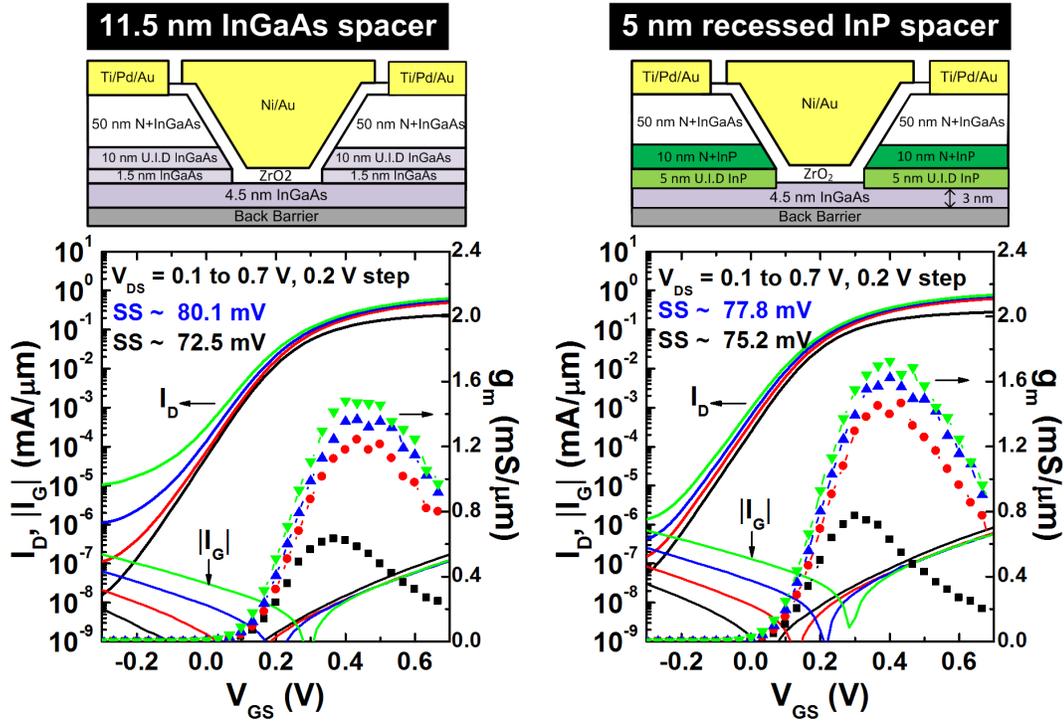
Figure 5.10: Transfer characteristics of FETs with 11.5 nm InGaAs spacers (sample 5.3A) and 5 nm recessed InP spacers (sample 5.4A) at 60 nm $L_g$.

Although thinner InP spacers reduce $R_{on}$ and increase $I_{on}$, InGaAs FETs with thinner InP spacers have poorer electrostatics. Fig. 5.11 shows the transfer characteristics of sample 5.4A at different gate lengths. The subthreshold swing, and drain-induced barrier lowering ($DIBL$) increase dramatically with a decrease on the gate lengths. Fig. 5.12 compare the $g_m$, $R_{on}$, $SS$, $DIBL$ as a function of gate lengths for different spacer design, including 5 nm recessed InP spacers, 13 nm recessed InP spacers, and 11.5 nm InGaAs spacers. It is clearly shown that reducing InP spacer thickness improves $g_m$ and $R_{on}$ at the cost of worse electrostatics, and increased $SS$ and $DIBL$. To maintain good electrostatics, hence low $SS$, the spacer must have some minimum thickness, yet for low BTBT leakage
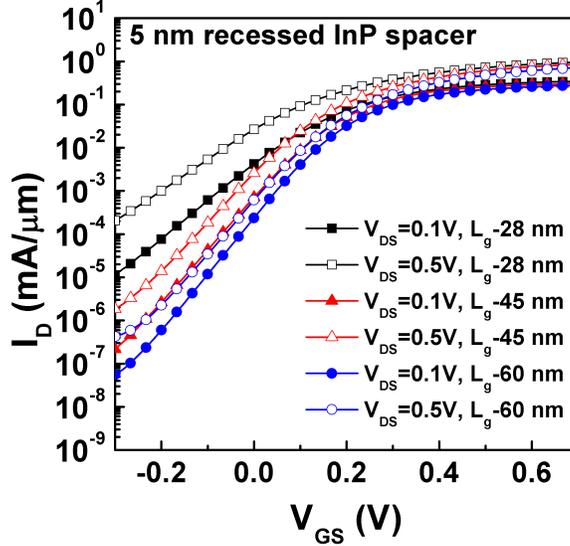
Figure 5.11: $I_D$-$V_{GS}$ characteristics vs. $L_g$ for InGaAs FETs with 5 nm recessed InP spacers.

only a fraction of this at the high-field region need be InP.

## 5.4.2   Doping-graded InP source/drain spacers

Thick, fully-depleted InP spacers reduce the on-state performance while thin InP spacers suffer from the worse electrostatics. For simultaneous high $I_{on}$ and low $I_{off}$, this suggests the use of spacers alloy-graded from InP to InGaAs. Alternatively, a doping-graded InP spacer would be lightly depleted in the source, minimizing access resistance, yet heavily depleted in the drain, minimizing BTBT and $SS$. Fig. 5.13(a) shows the device structure of Sample 5.4B, having a 5 nm undoped, recessed InP spacer, and above it an 8 nm linearly doping-graded InP spacer and 30 $\mathring{A}$ $ZrO_2$ gate dielectric. Fig. 5.13(b) shows the transfer characteristic
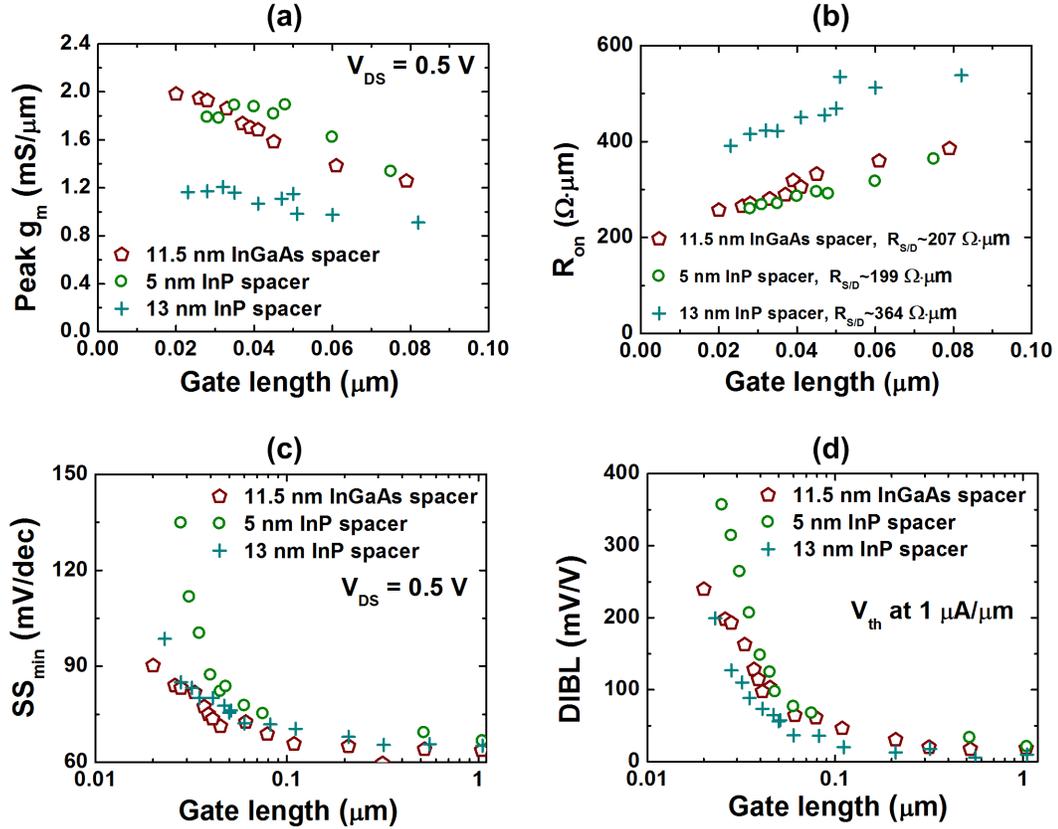
Figure 5.12: Comparisons of (a) $g_m$ vs. $L_g$, (b) $R_{on}$ vs. $L_g$, (c) $SS$ vs. $L_g$, (d) $DIBL$ vs. $L_g$ for 4.5 nm InGaAs channel MOSFETs with a 5 nm recessed InP spacer (sample 5.4A), a 13 nm recessed InP spacer (sample 5.3B), and a 11.5 nm InGaAs spacer (sample 5.3A).

of sample 5.4B at $L_g$-30 nm. The $L_g$-30 nm device shows ∼300 pA/$\mu$m minimum off-state leakage at $V_{DS}$=0.5 V, again being limited by gate leakage. The peak transconductance is 1.6 mS/$\mu$m at $V_{DS}$=0.5 V, greatly improved as compared to thick InP spacers (see Fig. 5.12(a)).

To evaluate the impacts of different source/drain designs, we extrapolate the $R_{on}$ to zero gate length to attain parasitic source/drain resistance ($R_{S/D}$). Fig. 5.14 summarizes the parasitic source/drain resistance for different spacer designs
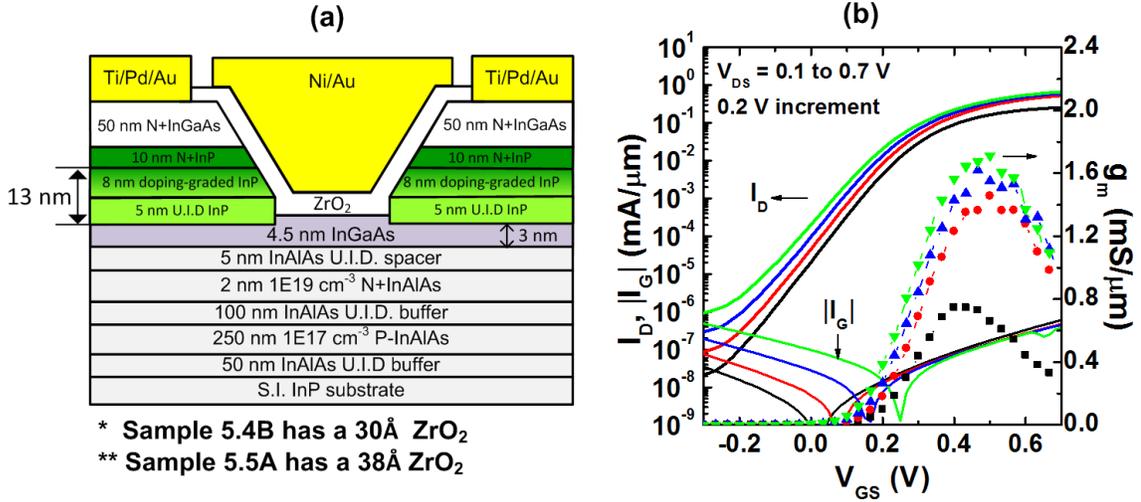
Figure 5.13: (a) The device schematic diagram of the InGaAs MOSFET with a recessed, doping graded InP spacer. (b) The transfer characteristic of sample 5.4B at $L_g$-30 nm, having a 30 Å $ZrO_2$.

and the inset in Fig. 5.14 shows the simple equivalent circuit diagram. The $R_{S/D}$ consists of four resistances; (1) $R_{contact} \sim 25$ $\Omega \cdot \mu$m from the source/drain ohmic contacts on N+InGaAs layers. (2) $R_{N+S/D} \sim 60$ $\Omega \cdot \mu$m from the sheet resistance of N+InGaAs source/drain layers. (3) $R_{ballistic} \sim 60$ $\Omega \cdot \mu$m from the ballistic resistance [21, 22]. (4) $R_{spacer}$ contributes to the rest of $R_{S/D}$.

In Fig. 5.14, the doping-graded InP spacers shows parasitic source/drain resistance $(R_{S/D})$ around $\sim 260$ $\Omega \cdot \mu$m, a significant improvement on $R_{on}$ as compared to 13 nm un-doped InP spacers, while still slightly inferior to InGaAs spacers. It is noted that $R_{S/D}$ only increases slowly with InGaAs spacer thickness, but $R_{S/D}$ increases dramatically as the InP spacer thickness increases. Further optimization of source/drain spacer design is required, especially for the short $L_g$ devices.
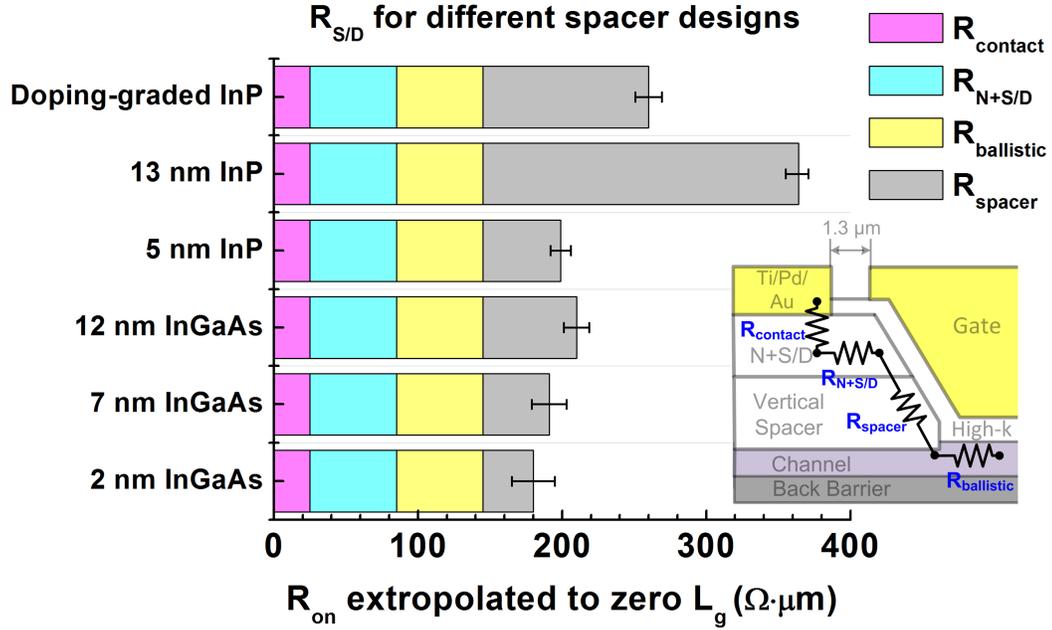
Figure 5.14: Comparison of the parasitic source/drain resistance with respect to different spacer designs.

## 5.5  Record low leakage III-V MOSFETs

### 5.5.1  Minimum $I_{\text{off}} \sim 60$ pA/$\mu$m: III-V FETs for low power logic

In section 5.4.2, with a doping-graded InP spacer, band-to-band-tunneling leakage can be diminished in InGaAs MOSFETs to the level below gate leakage ($\sim$300 pA/$\mu$m), while the FETs still maintain good on-state performance. Given that the minimum off-state leakage is dominated by gate leakage in sample 5.4B, we fabricated a similar device (see Fig. 5.13), but intentionally increased the gate oxide thickness from 30 $\mathring{A}$ (sample 5.4B) to 38 $\mathring{A}$ (sample 5.5A) to fathom the lowest achievable leakage level. Fig. 5.15 shows the transfer characteristic of

sample 5.5A. At $L_g$-30 nm, the minimum $I_{off}$ after increasing oxide thickness is further reduced to 60 pA/$\mu$m, showing a 100:1 smaller BTBT leakage floor than obtained using InGaAs source/drain spacers (sample 5.3A). To our knowledge, this is the record lowest leakage current observed in an InGaAs MOSFET at a VLSI-relevant gate length. For the first time, III-V MOSFETs show sufficiently low leakage current, being feasible for low standby power logic circuits and mobile computing electronics.

Fig. 5.16(a) and 5.16(b) compare the transconductance and subthreshold swing as a function of $L_g$ for different InP spacer designs. Because the doping-graded InP spacers improve $R_{S/D}$, the transconductance is improved, in particular for short $L_g$ devices. Moreover, the subthreshold swing for FETs with the doping-graded InP spacers is similar to that with 13 nm thick un-doped InP spacers, indicating that good electrostatics is still maintained. The doping-graded InP spacers exhibit good compromise between on- and off- state performance.

## 5.5.2   Benchmark of $I_{on}$-$I_{off}$ for III-V MOSFETs

Fig. 5.17(a) shows $I_{on}$ as a function of $L_g$ at $I_{off}$=1 nA/$\mu$m and $V_{DS}$=0.5 V. The threshold voltage is defined at $I_{off}$=1 nA/$\mu$m using constant current method, and the $I_{on}$ is obtained at $V_{GS}$-$V_{th}$=0.5 V and $V_D$=0.5 V. Most reported III-V MOSFETs in the literature have high $I_{off}$ (>10 nA/$\mu$m) for $L_g$ smaller than 100 nm, and hence there are no available data for cross comparison if $I_{off}$ is set at 1 nA/$\mu$m. We compare the key MOSFETs fabricated in UC Santa Barbara at $I_{off} =$ 1 nA/$\mu$m. The FETs with InGaAs spacers show low $I_{on}$ at smaller $L_g$ because high
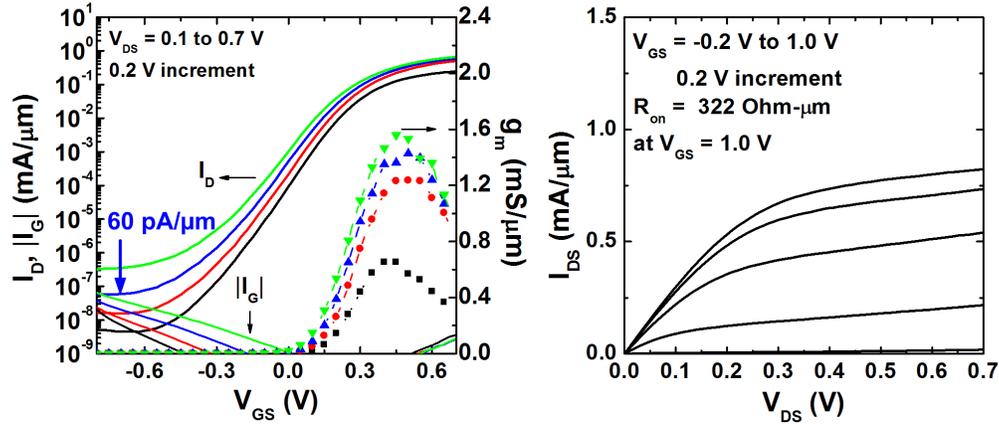
Figure 5.15: The transfer and output characteristics of 4.5 nm InGaAs FETs with a 3.8 nm $ZrO_2$ and a recessed, doping graded InP spacers at $L_g$-30 nm.
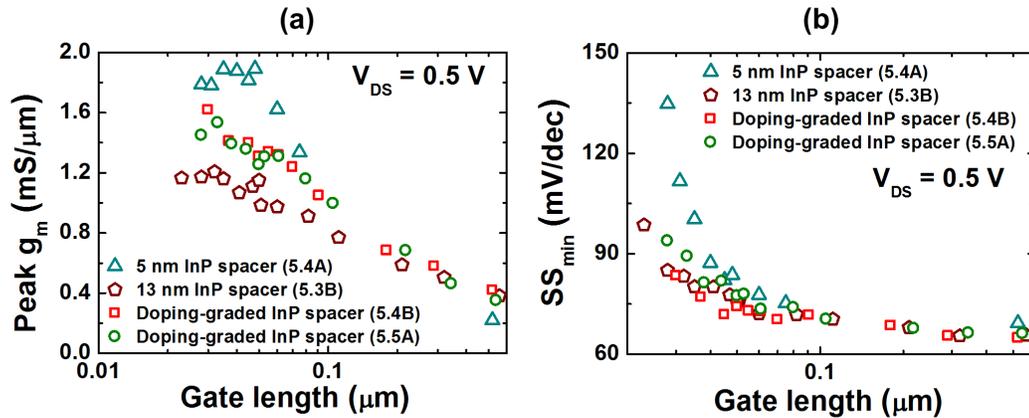


Figure 5.16: Comparisons of (a) $g_m$ vs. $L_g$ and (b) $SS$ vs. $L_g$ for a doping–graded InP spacer, a 5 nm undoped InP spacer, and a 13 nm undoped InP spacer.

BTBT leakage not only degrades the $SS$, but also increases $I_{\text{off}}$ above 1 nA/$\mu$m at small $L_{\text{g}}$. Although shrinking the InGaAs channel thickness from 4.5 nm to 3 nm improves device scalability, the peak $I_{\text{on}}$ is also reduced from 80 $\mu$A/$\mu$m to 50 $\mu$A/$\mu$m. Instead of further thinning the channel, the FETs with recessed InP spacers show significantly improved $I_{\text{on}}$ at small $L_{\text{g}}$ due to reduced BTBT leakage. Sample 5.4B shows the maximum peak $I_{\text{on}}$=150 $\mu$A/$\mu$m at $L_{\text{g}}$= 45 nm. Sample 5.5A shows slightly reduced $I_{\text{on}}$= 120 $\mu$A/$\mu$m due to the thicker gate dielectric, which decreases $g_{\text{m}}$ and increases $SS$. Last, for samples 5.3B (13 nm un-doped InP spacers), and 5.4B (doping-graded InP spacers) and 5.5A (doping-graded InP spacers), $I_{\text{on}}$ decreases rapidly as $L_{\text{g}}$ is reduced below 40 nm. This is a consequence of poor electrostatics, hence large $SS$, at these gate lengths.

Fig. 5.17(b) shows $I_{\text{on}}$ vs. $L_{\text{g}}$ at $V_{\text{DS}}$=0.5 V, but at a larger $I_{\text{off}}$=100 nA/$\mu$m, benchmarking against recent III-V MOSFETs and 22 nm Si FinFETs. The FETs with 4.5 nm In$_{0.53}$Ga$_{0.47}$As channels show performance comparable to leading III-V FETs. As reported in chapter 4.4, given an $I_{\text{off}}$=100 nA/$\mu$m metric, the 2.7-nm-thick InAs channel MOSFETs show the highest $I_{\text{on}}$ and performance comparable to 22 nm Si FinFETs, as a consequence of larger gate capacitance and good electrostatics. In contrast, for low-power applications, a wider band-gap In$_{0.53}$Ga$_{0.47}$As channel more readily provides low leakage current. Further improvements on the InP spacer design would reduce $R_{\text{S/D}}$ and increase $I_{\text{on}}$ at short $L_{\text{g}}$.

To further improve $I_{\text{on}}$ at small $L_{\text{g}}$, a tri-gate or nanowire structure would provide improved electrostatics and hence improved $SS$. For low power (LP) and ultra-low-power (ULP) logic where the requirement of leakage current is set at 30 pA/$\mu$m and 15 pA/$\mu$m, the gate overdrive voltage is mainly on the subthreshold
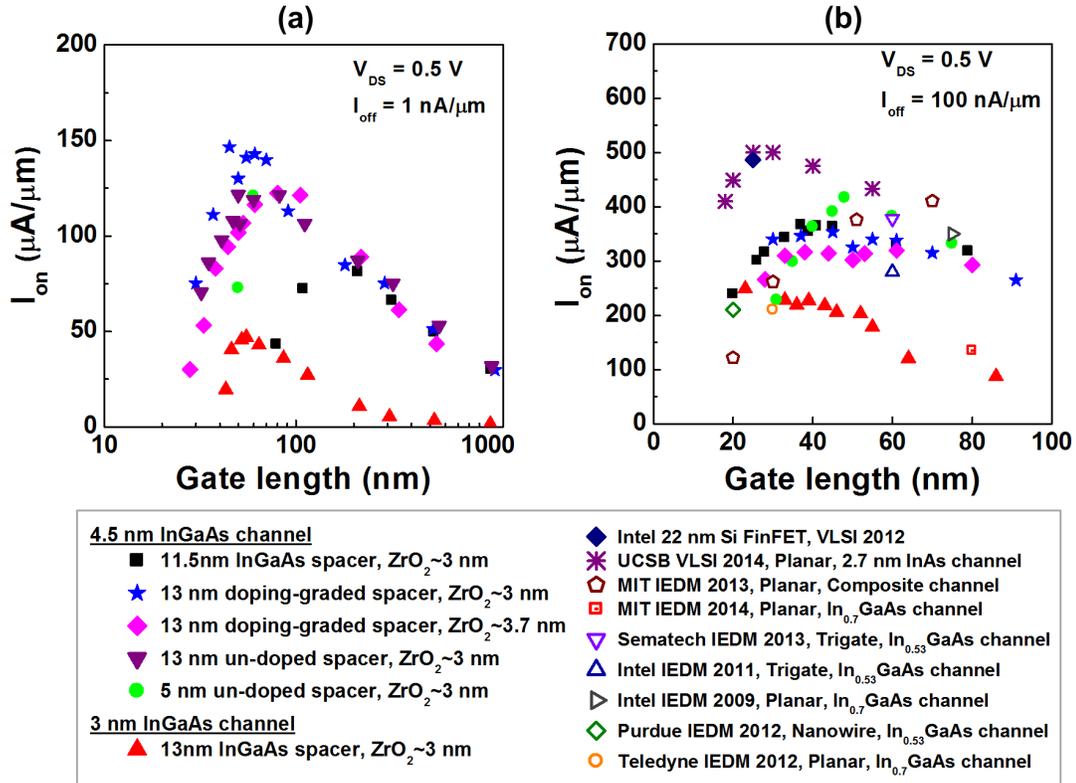
Figure 5.17: (a) $I_{\mathrm{on}}$ vs. $L_{\mathrm{g}}$ at $I_{\mathrm{off}}$=1 nA/$\mu$m and $V_{\mathrm{DS}}$=0.5 V. (b) $I_{\mathrm{on}}$ vs. $L_{\mathrm{g}}$ at $I_{\mathrm{off}}$=100 nA/$\mu$m and $V_{\mathrm{DS}}$=0.5 V and the benchmark with recently published III-V MOSFETs.

region. Therefore, subthreshold swing is the most important device parameter of MOSFET to gain high $I_{\mathrm{on}}$ at fixed $I_{\mathrm{off}}$. Instead of using thick source/drain spacers to control electrostatics, improving electrostatics using FINFET or nanowire will improve subthreshold swing without an increase on series resistance. With the combination of a thin recessed InP spacers for low BTBT leakage, InGaAs MOSFETs would then be suitable for low power logic.

### 5.5.3    Residual leakage: sidewall passivation

We have already demonstrated the lowest $I_{\text{off}}$ ~60 pA/$\mu$m at the $L_{\text{g}}$-30 nm InGaAs MOSFET in section 5.5.1. However, we seek to further reduce leakage current to meet the low power logic specification ($I_{\text{off}}$~30 pA/$\mu$m) and ultra-low power logic specification ($I_{\text{off}}$~15 pA/$\mu$m). Unfortunately, once the BTBT leakage is removed by recessed InP spacers, the minimum $I_{\text{off}}$ is then limited by mesa sidewall leakage. Fig. 5.18(a) shows the minimum $I_{\text{off}}$ as a function of gate lengths and gate widths for InGaAs MOSFETs with recessed InP spacers. Fig. 5.18(b) shows the top view of MOSFET mask layout. Clearly, the minimum $I_{\text{off}}$ is now independent of gate length, and, unlike BTBT leakage, has no lateral bipolar current gain at smaller gate length (see section 2.2.3). Furthermore, it is observed that the absolute $I_{\text{off}}$ current level is no longer proportional to gate width. Hence, $I_{\text{off}}/W_{\text{g}}$ increases proportionally as the gate width decreases. This result indicates that the residual leakage path might be located at the device mesa sidewalls, not within the channels or the back barriers. Therefore, further improvements on the mesa sidewall passivation could lower the minimum $I_{\text{off}}$, making III-V MOSFETs viable for ultra-low power logic applications.

## 5.6    Summary

In this chapter, we have developed raised InGaAs source/drain spacers and recessed InP spacers. The raised source/drain spacers improve transistor electrostatics, reducing subthreshold leakage, and smooth the electric field, reducing
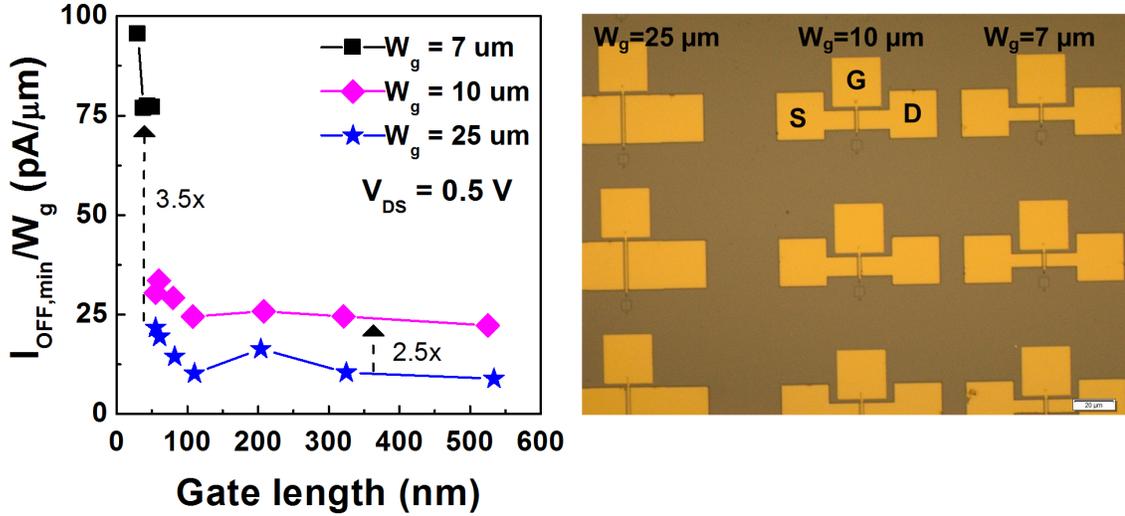
Figure 5.18: (a) The dependence of $I_{\text{off}}$ as a function of gate lengths and gate widths. (b) The top view of MOSFET mask layout in this study.

BTBT leakage near the drain end of the channel. A certain amount of spacer thickness is required to maintain electrostatics, in which InGaAs spacers are preferred because InGaAs has larger electron affinity and less parasitic source/drain resistance. Only at the high field regions in FETs where BTBT occurs require wide band-gap InP spacers. It is found that a partially recessed InP spacer is sufficient to remove BTBT leakage for a 4.5 nm InGaAs channel MOSFET. However, InP spacers, in contrast, largely increase parasitic source/drain resistance and cause $I_{\text{on}}$ and $g_{\text{m}}$ degradation. The doping-graded InP spacers reduce the parasitic source/drain resistance, improve $I_{\text{on}}$, and still maintain good electrostatics and low $I_{\text{off}}$.

With the recessed InP source/drain spacers, we have demonstrated a record low leakage InGaAs MOSFET with minimum $I_{\text{off}} \sim 60$ pA/$\mu$m at $V_{\text{DS}} = 0.5$ V. The residual off-state leakage current comes from imperfect sidewall passivation.

The recessed InP spacer technique, for the first time, enables III-V MOSFETs feasible for low power logic applications. With further improvement of sidewall passivation, III-V MOSFETs will be suitable for ultra-low power logic ($I_{\mathrm{off}}$~15 pA/$\mu$m) and mobile computing electronics.

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# Chapter 6

# 12 nm-$L_\mathrm{g}$ III-V MOSFETs with High $I_\mathrm{on}/I_\mathrm{off}$ Ratio

III-V InGaAs/InAs MOSFETs are being considered to replace Si channels at future 7 or 5 nm technology nodes according to International Technology Roadmap for Semiconductors (ITRS). At the 5 nm node, the ITRS targets 12 nm physical gate length [1]. At such small dimensions, few III-V MOSFETs have been reported, and the observed off-state leakage currents have been high [2–10]. High off-state leakage current arising from band-to-band tunneling (BTBT) near the drain end of channel makes it difficult to scale III-V MOSFETs to sub-10-nm generations. In chapter 4.4, we have reported a FET using a 2.7 nm thick InAs channel to reduce $I_\mathrm{off}$ to 10 nA/$\mu$m for 25 nm $L_\mathrm{g}$, simultaneously achieving record $I_\mathrm{on}$ (500 $\mu$A/$\mu$m at 100 nA/$\mu$m $I_\mathrm{off}$ and $V_\mathrm{DD}$=0.5 V) (see chapter 4.4 and [10]). To further reduce BTBT leakage current, we have also developed InGaAs-channel MOSFETs with 4.5 nm thick channels and graded-doping recessed InP source/drain spacer layers; these showed a minimum 60 pA/$\mu$m $I_\mathrm{off}$ at 30 nm $L_\mathrm{g}$ (see Chapter 5.5 and [11]). However, the physical gate length is still longer than the targeted gate length ($L_\mathrm{g}$~12 nm) for the interested technology nodes.

In this chapter, we further reduce the physical gate length by optimizing the dummy gate process, and report 12 nm-$L_\mathrm{g}$ FETs with 1.5/1 nm InGaAs/InAs composite channels, and recessed doping-graded InP source/drain spacers. The FETs demonstrate high ~1.8 mS/$\mu$m transconductance ($g_\mathrm{m}$), low ~107 mV/dec. subthreshold swing ($SS$), and low ~1.3 nA/$\mu$m minimum $I_\mathrm{off}$ at $V_\mathrm{DS}$=0.5 V. For the first time, III-V InGaAs/InAs MOSFETs at 12 nm gate length were demonstrated with well-balanced on-off DC performance. The maximum $I_\mathrm{on}/I_\mathrm{off}$ ratio at $V_\mathrm{DS}$=0.5 V is more than 8.3×$10^5$, confirming that III-V MOSFETs are scalable to sub-10-nm technology nodes.

# 6.1    A 12 nm-$L_\text{g}$ ultra-thin-body III-V MOSFET: device performance

## 6.1.1    Device fabrication and performance

Fig. 6.1(a) shows the device structure, and 6.1(b) shows the top-view SEM image on the $L_\text{g}$-12 nm devices (defined by the edges of regrown layers). Fig. 6.1(c) shows the detailed process flow. The final device consists of a 1 nm InAs bottom channel and a 1.5 nm In$_{0.53}$Ga$_{0.47}$As top channel. The devices have 12 to 1000 nm physical gate lengths. The InGaAs layer in the source/drain (S/D) region was partially removed by a digital etch, leaving ∼0.5 nm InGaAs and 1 nm InAs to prevent the oxidation of the InAlAs barriers and ensure high crystalline quality of MOCVD regrowth. The S/D layers grown by MOCVD have an un-doped InP spacer, a linearly doping-graded InP spacer, a Si-doped InP (∼5×10$^{19}$ cm$^{-3}$) layer and a Si-doped (∼4.0×10$^{19}$ cm$^{-3}$) In$_{0.53}$Ga$_{0.47}$As contact layer. The FETs have a ∼3.4 nm ZrO$_2$ gate dielectric, including the AlO$_x$N$_{1-x}$ interfacial layer formed by the ALD cyclic TMA/nitrogen plasma pre-treatment. Ni/Au gate and Ti/Pd/Au S/D metal contacts were defined using liftoff.

Fig. 6.2 shows the cross-sectional TEM image of a 12 nm-$L_\text{g}$ FET. The metal gate width is ∼8 nm. The FET has a 2.5 nm thin channel. The InP spacers were partially recessed with the regrowth interface ∼1.5 nm above In-AlAs barriers. There are two important findings from the regrowth. First, the source/drain spacers have (011) facet next to the gate edge as compared to the (111)B facet shown in Fig. 4.17. In this device, the regrowth has crystal facet at (011) plane because the (111)A plane has the growth rate faster than (011) plane,

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**(a)**

$L_g$~12 nm

Ti/Pd/Au

Ni/Au

Ti/Pd/Au

N+InGaAs                                           50 nm
N+InP                                              10 nm
Doping-graded InP                                   8 nm
U.I.D. InP spacer          ZrO$_2$    0.5 nm        5 nm
                        1.5 nm InGaAs
1 nm InAs
5 nm InAlAs U.I.D. spacer
2 nm 1E19 cm$^{-3}$ N+InAlAs
100 nm InAlAs U.I.D. buffer
250 nm 1E17 cm$^{-3}$ P-InAlAs
50 nm InAlAs U.I.D buffer
S.I. InP substrate

**(b)**

$L_g$~12 nm

X 650,000    10.0kV SEI    10nm   UCSB      3/25/2015
                           SEM    WD 4.2mm  12:54:45

**(c)**

Channel
Barrier
Substrate

**MBE grown
device epilayer**

HSQ
Ch.
Barrier
Substrate

**Pattern dummy gate
Source/drain recess etch**

HSQ
N+ S/D          Ch.
Barrier
Substrate

**MOCVD source/drain
regrowth**

ZrO$_2$
N+ S/D    Ch.
Barrier
Substrate

**Isolation
Strip dummy gate
Digital etch
Deposit ALD dielectric
FGA anneal**

Ni
N+ S/D    Ch.
Barrier
Substrate

**Lift-off gate metal**

Ti/Pd/Au
Ni
N+ S/D    Ch.
Barrier
Substrate

**Deposit
S/D contacts**

Figure 6.1: (a) The device structure. (b) The top-view of SEM images. (c) The schematic diagram of process flow.

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thereby leaving (011) facet adjacent to the dummy gate after regrowth. In the other case in Fig. 4.17 where the dummy gate orientation rotates 90 degree, the regrowth facet is (111)B plane instead of (0$\bar{1}$1) plane because (111)B is the slowest growth plane, thereby forming an inclined (111)B facet after regrowth. The vertical (011) facet is more preferred because it could allow a tighter source/drain pitch without making a self-aligned contact on the (111) surface. Second, it is observed that the spacer thickness next to the gate edge is very different from the nominal spacer thickness ($t_\mathrm{spacer}$) far from the gate. This indicates that the effective vertical spacers are thinner than the nominal spacer thickness. Therefore, the effective gate length does not increase as much as the added spacer thickness ($L_\mathrm{eff} < L_\mathrm{g} + 2t_\mathrm{spacer}$).

Fig. 6.3(a) shows the transfer characteristic of a 12 nm-$L_\mathrm{g}$ FET, achieving 1.8 mS/$\mu$m peak $g_\mathrm{m}$ at $V_\mathrm{DS}$=0.5 V. The subthreshold swing, Fig. 6.3(b), is 98.6 mV/dec. at $V_\mathrm{DS}$=0.1 V and 107.5 mV/dec. at $V_\mathrm{DS}$=0.5 V. The minimum leakage current is as low as 1.3 nA/$\mu$m at $V_\mathrm{DS}$=0.5 V, where $I_\mathrm{off}$ is limited by BTBT. This leakage current is sufficiently low to meet the requirement of high performance (HP, 100 nA/$\mu$m) logic applications, and close to the specification of standard performance (SP, 1 nA/$\mu$m) applications. Fig. 6.3(c) shows the output characteristic of a 12 nm-$L_\mathrm{g}$ FET. The maximum $I_\mathrm{D}$ exceeds 1.25 mA/$\mu$m at $V_\mathrm{GS}$=1.2 V and $V_\mathrm{DS}$=0.7 V, and the on-resistance ($R_\mathrm{on}$) at $V_\mathrm{GS}$=1 V is 302 $\Omega \cdot \mu m$. The $I_\mathrm{D}$ at $V_\mathrm{GS}$=1.2 V and $V_\mathrm{DS}$=0.5 V is 1.1 mA/$\mu$m, showing maximum $I_\mathrm{on}/I_\mathrm{off}\sim$8.3$\times$10$^5$. This result demonstrated a well-balance on/off DC performance, confirming that III-V MOSFETs are scalable to sub-10-nm technology nodes.
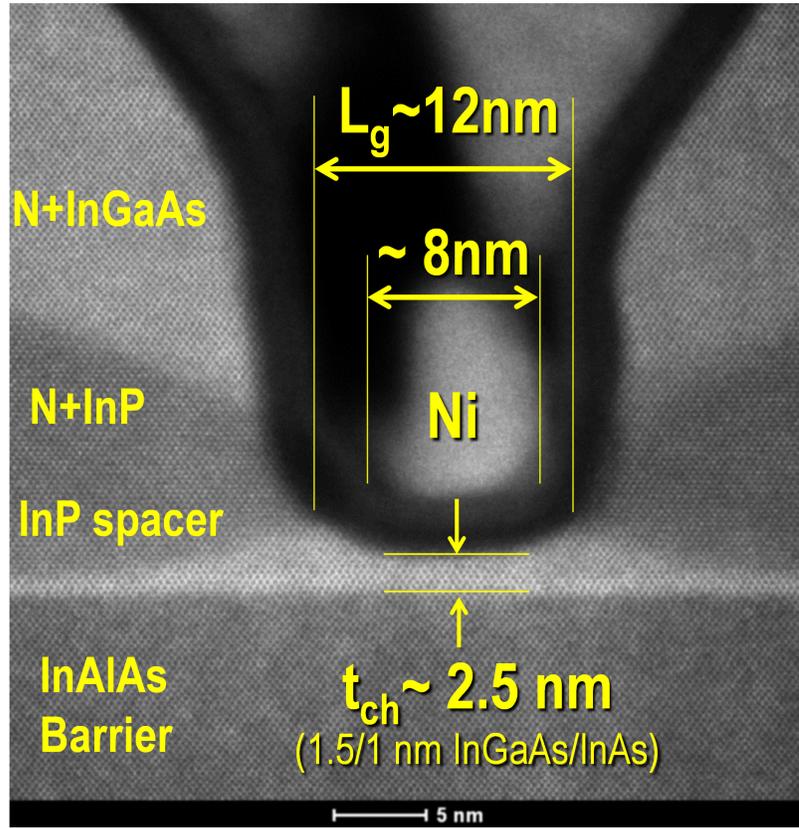
Figure 6.2: The scanning TEM image for a 12nm-$L_\text{g}$ FET. (Image courtesy of Stephan Kraemer.)

## 6.1.2   Comparison with record high performance and low leakage III-V FETs

In this subsection, we compare the ultra-thin-body composite channel MOS-FETs to the previously reported high performance InAs MOSFETs (see chapter 4.4 and [10]) and low leakage InGaAs MOSFETs with recessed InP spacers (see chapter 5.5 and [11]). Fig. 6.4(a) and 6.4(b) show $g_\text{m}$ and $R_\text{on}$ as a function of $L_\text{g}$, respectively. Examining $g_\text{m}$ vs. $L_\text{g}$, the present InGaAs/InAs composite channel devices show $g_\text{m}$ slightly superior to 4.5 nm InGaAs MOSFETs using InP
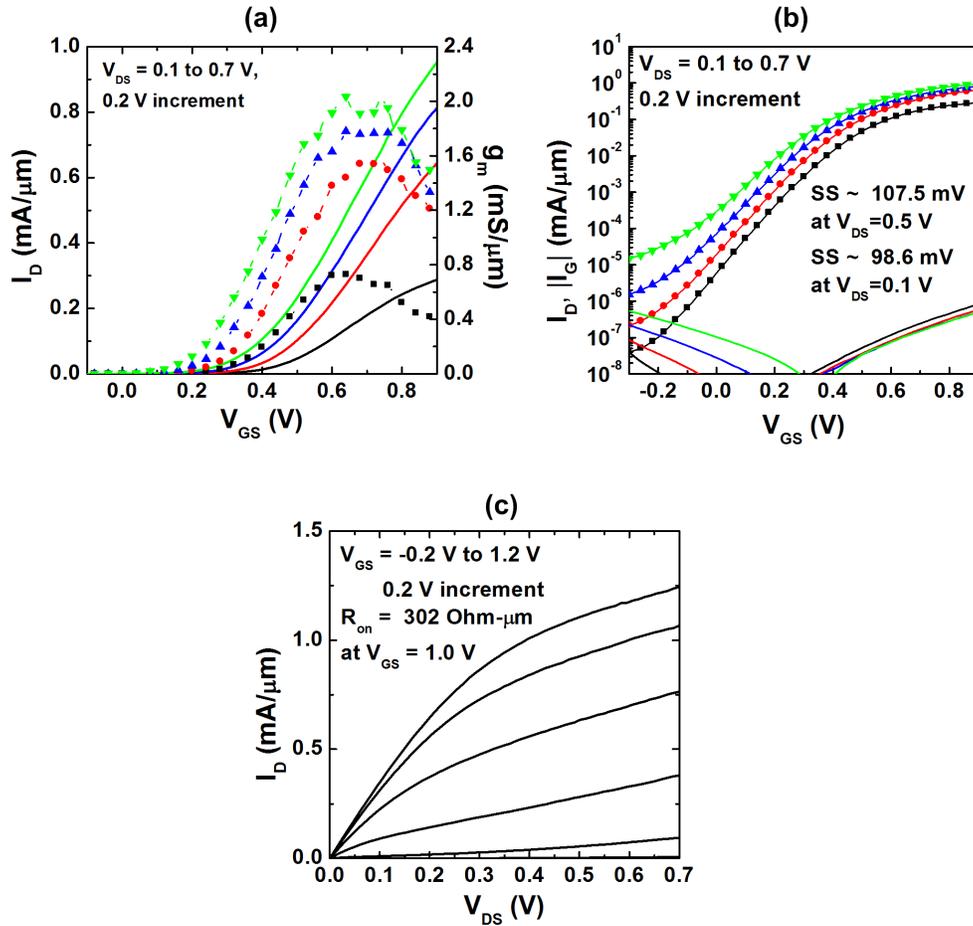
Figure 6.3: (a) $I_{\mathrm{D}}$ and transconductance $g_{\mathrm{m}}$ versus $V_{\mathrm{GS}}$, (b) subthreshold characteristics, and (c) output characteristics for a 12 nm-$L_{\mathrm{g}}$ FET.

spacers, but lower $g_{\mathrm{m}}$ than 2.7 nm InAs channels with 12 nm InGaAs spacers. On-resistance, Fig. 6.4(b), $\sim$262 $\Omega \cdot \mu m$ when extrapolated to zero $L_{\mathrm{g}}$, is also consistent with earlier results using similar InP spacers, as shown in Fig. 5.14. Clearly, as the gate length deceases, the parasitic source/drain resistance ($R_{\mathrm{S/D}}$) becomes dominant for $R_{\mathrm{on}}$, and lower $R_{\mathrm{S/D}}$ of InGaAs source/drian spacers would enable higher transconductance and higher $I_{\mathrm{on}}$.

Fig. 6.5(a) shows $SS$ vs. $L_{\mathrm{g}}$ and Fig. 6.5(b) shows $DIBL$ vs. $L_{\mathrm{g}}$. As the
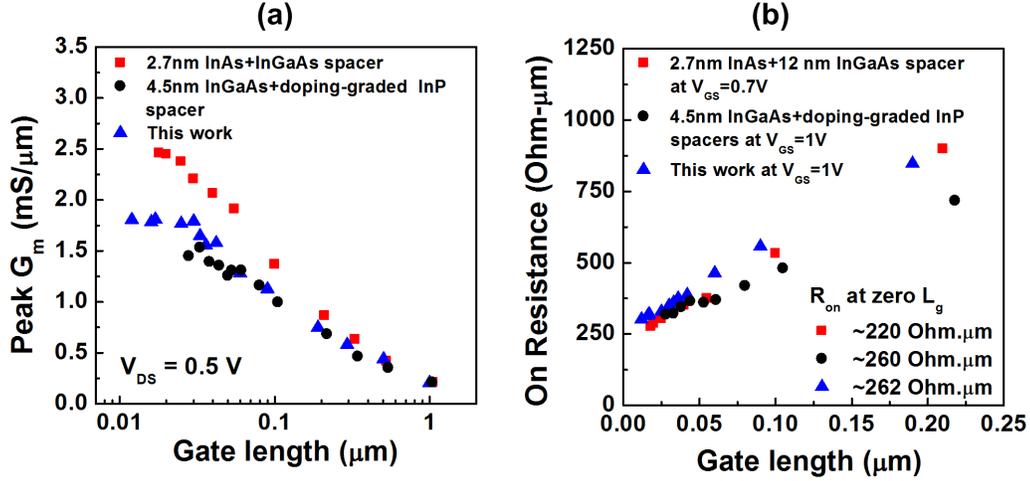
Figure 6.4: (a) Comparison of $g_m$ and (b) $R_{on}$ as a function of $L_g$ for 2.5 nm composite channels MOSFETs to previously reported high performance InAs MOSFETs (chapter 4.4 and [10]) and low leakage InGaAs MOSFETs with recessed InP spacers (chapter 5.5 and [11])

gate length decreases, $SS$ and $DIBL$ increase due to deteriorating electrostatics. Because the effective gate length is slightly larger for 12 nm thick InGaAs spacers than doping-graded InP spacers (5 nm un-doped spacer + 8 nm linearly doping-graded spacers), the 2.7 nm InAs channel FETs have better short channel control. Further thinning the channel or increasing spacer thickness would mitigate such short channel effects, but unfortunately both increase on resistance because of higher channel resistance and higher parasitic source/drain resistance. On the other hand, in chapter 4, we have reported that InGaAs channels thinner than ~3.5 nm show poor $g_m$. InAs channels, in contrast, though showing high $g_m$ even at 2.7 nm thick, show high BTBT leakage. Therefore, a FinFET or nanowire structure would improve electrostatics, allowing use of thicker channels and thinner source/drain spacers. Because only a thin InP drain spacer at the high field region would be required to suppress BTBT, on-state performance ($g_m$) would be
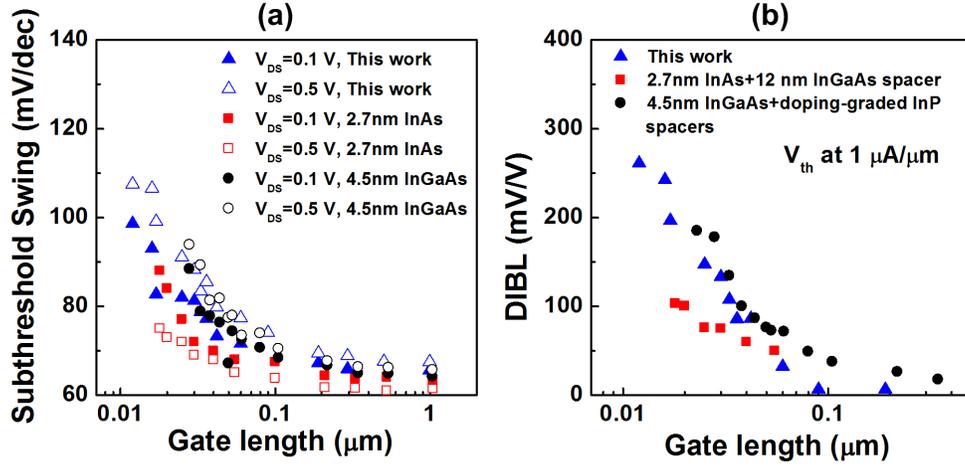
Figure 6.5: (a) Comparison of $SS$ and (b) $DIBL$ as a function of $L_\mathrm{g}$ for 2.5 nm composite channels MOSFETs to previously reported high performance InAs MOSFETs (chapter 4.4 and [10]) and low leakage InGaAs MOSFETs with recessed InP spacers (chapter 5.5 and [11])

improved.

Fig. 6.6(a) shows minimum $I_\mathrm{off}$ vs. $L_\mathrm{g}$. The FETs reported here, having a 1.5/1 nm InGaAs/InAs composite channel and recessed InP spacers, show lower leakage current than FETs using 2.7 nm InAs channels and InGaAs S/D spacers (see chapter 4.4 and [10]), but larger leakage than FETs using 4.5 nm InGaAs channels and recessed InP spacers (see chapter 5.5 and [11]). A clear tradeoff between $I_\mathrm{on}$ and $I_\mathrm{off}$ is observed in Fig. 6.6. Fig. 6.6(b) benchmarks $I_\mathrm{on}$ as a function of $L_\mathrm{g}$ at $I_\mathrm{off}$=100 nA/$\mu$m and $V_\mathrm{DS}$=$V_\mathrm{GS}$-$V_{TH}$=0.5 V. The FETs reported here show $I_\mathrm{on}\sim$311 A/$\mu$m at $L_\mathrm{g}$=42 nm, similar to the low leakage devices reported in chapter 5.5.
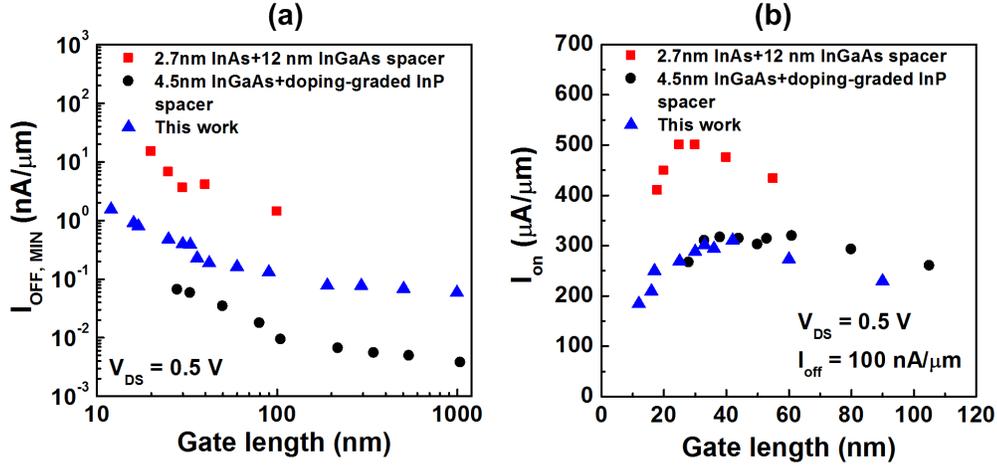
Figure 6.6: (a) Comparison of minimum $I_\text{off}$ at $V_\text{DS}$=0.5 V and (b) $I_\text{on}$ at fixed $I_\text{off}$=100 nA/$\mu$m and $V_\text{DS}$=0.5 V as a function of $L_\text{g}$ for 2.5 nm composite channels MOSFETs to previously reported high performance InAs MOSFETs (chapter 4.4 and [10]) and low leakage InGaAs MOSFETs with recessed InP spacers (chapter 5.5 and [11])

### 6.1.3 Effective channel mobility of 2.5 nm composite channels

Fig. 6.7 shows the C-V measurements and effective channel mobility in 25 $\mu$m MOSFETs. The gate capacitance is about 2.4 $\mu$F/cm$^2$ at $V_\text{GS}$=1 V. Unlike 3 nm InGaAs channel shown in Fig. 4.14, 2.5 nm composite channels show less frequency dispersions as seen in the inset of Fig. 6.7(a). In Fig. 6.7(b), the mobility for composite channel MOSFETs is about 250 cm$^2$/V·s, slightly lower than a 2.7 nm InAs channel (280 cm$^2$/V·s) and 4.5 nm InGaAs channels (300 cm$^2$/V·s). Note that at the extremely short gate length where the transistor is working near the ballistic limit, higher long channel mobility does not ensure higher on-state performance. It is clearly shown in Fig. 6.4 that the on-state performance of short $L_\text{g}$ MOSFETs has strong correlation to the parasitic source/drain resis-
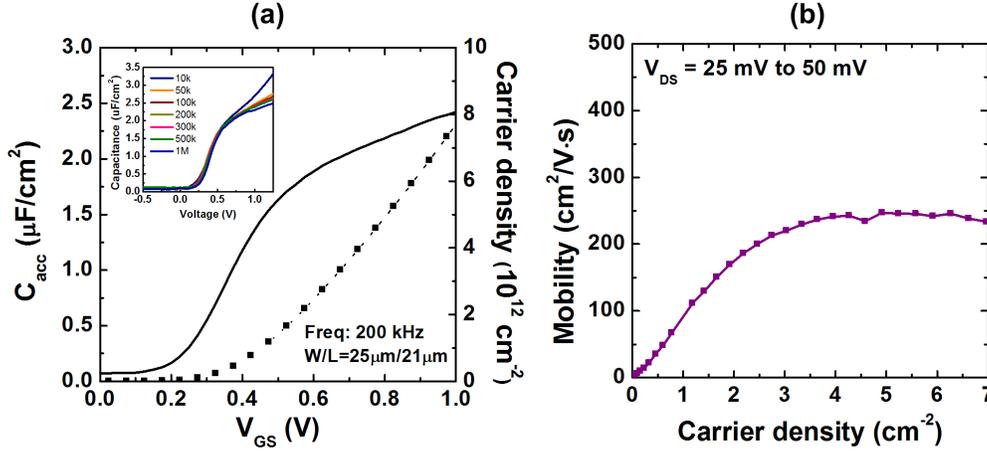
Figure 6.7: (a) Capacitance-voltage measurements for 2.5 nm composite channel MOSFETs. The inset shows C-V frequency dispersion. (b) The extracted effective channel mobility using split C-V measurements for 25 $\mu$m-$L_\text{g}$ devices.

tance rather than the long channel mobility. For a ballistic MOSFET, an optimal channel effective mass, higher gate-to channel capacitance (i.e. thin channel and thin oxide), and low parasitic source/drain resistance would be the most critical parameters for device design.

## 6.2   Summary

In this chapter, we have reported a III-V MOSFET with a 12 nm physical gate length, an ultra-thin 1.5/1 nm InGaAs/InAs composite channel, and a recessed doping-graded InP S/D vertical spacer. The FET demonstrates $g_\text{m}\sim$1.8 mS/$\mu$m transconductance, $SS\sim$107 mV/dec., minimum $I_\text{off}\sim$1.3 nA/$\mu$m at $V_\text{DS}$=0.5 V, and well-balanced on-off DC performance with maximum $I_\text{on}/I_\text{off}\sim$8.3$\times$10$^5$. Band-to-band tunneling leakage current is well-controlled through the thin composite

InGaAs/InAs channel, and by the recessed InP source/drain spacers. This work demonstrates that III-V MOSFETs can scale to the sub-10-nm technology nodes.

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# Chapter 7

# Ultrathin InAs Channel MOSFETs on Si substrates

Si complementary-metal-oxide-semiconductor (CMOS) logic technology is continuously driven by scaling transistor dimensions, increasing transistor density and, more importantly, decreasing the cost per transistor. Aiming at future logic technology and continuous cost reductions, III-V MOSFETs must be fabricated on Si substrates, and must be compatible with the existing Si process platform. As discussed in chapter 1.2, the heterogeneous integration of III-V semiconductors on Si is extremely difficult because of very dissimilar material properties. The large lattice mismatch, different crystal polarity, and large mismatch of thermal expansion coefficient cause a high density of defects in the III-V layers on Si. Although several integration schemes have been proposed over the past three decades, e.g. blanket epitaxy [1–3], wafer bonding [4–6], epitaxial lateral overgrowth (ELO) [7], and aspect ratio trapping (ART) [8–10], the best integration approach has still not been established yet. In consequence, to attain a device-quality III-V layer on Si substrates is still the greatest barricade to realize III-V MOSFETs for future CMOS logic technology.

To date, only few results have been reported for III-V MOSFETs on Si substrates [1, 2, 4, 5], and the demonstrations of high performance III-V MOSFETs on Si are still limited. If III-V InGaAs/InAs channels are to be viable as a replacement for Si channels, it must be established that high performance and high yield can be obtained. In this chapter, we cooperated with Applied Materials and have fabricated an ultra-thin InAs channel MOSFET on Si substrates [11], and compared to our record high performance InAs FETs on InP substrates [12].

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## 7.1   Device epitaxial layers growth

Fig. 7.1(a) shows the device structure of ultra-thin InAs channel MOSFETs on Si substrates. The III-V buffer layers on Si were grown by Applied Materials 300 mm III-V MOCVD system. The buffer layers grown over the entire on-axis (100) Si substrates, a 400 nm unintentionally doped (U.I.D.) GaAs, a 300 nm U.I.D. InP, a 20 nm p-doped InGaAs, a 50 nm U.I.D. InAlAs and a 10 nm U.I.D. InP cap. The samples were then shipped to UC Santa Barbara, cleaved, cleaned by dilute HCl, and immediately loaded into a Veeco GENII solid source MBE system. The 2 nm InGaAs cap, 3.5 nm InAs channel and the InAlAs barrier layers were then grown on top of the III-V-buffers on Si.

Fig. 7.1(b) shows the surface roughness of the III-V buffer layers on Si substrates grown by Applied Materials 300 mm III-V MOCVD system. Fig. 7.1(c) shows the surface roughness of MBE-grown channel layers on Applied Materials III-V-on-Si buffer. From the images of atomic force microscope (AFM), the root-mean-square roughness ($R_q$) is degraded from $\sim$3.1 nm for the III-V buffer to $\sim$6.9 nm after MBE growth. No obvious anisotropic growth was observed on the surface. Note that the same epitaxial structure when grown on InP substrates has typically $R_q \sim$0.2 nm. The samples grown on the Si substrates have $\sim$35:1 larger surface roughness than the control samples grown on InP. Such large surface roughness is worrisome in particular for ultra-thin channel MOSFETs with a targeted 2$\sim$4 nm channel thickness. Therefore, a thicker channel ($\sim$3.5 nm InAs + $\sim$0.5 nm InGaAs) as compared to the 2.7 nm InAs (see chapter 4.4) was fabricated to avoid severe mobility degradation in the thin channels caused by interface roughness scattering.

**(a)**
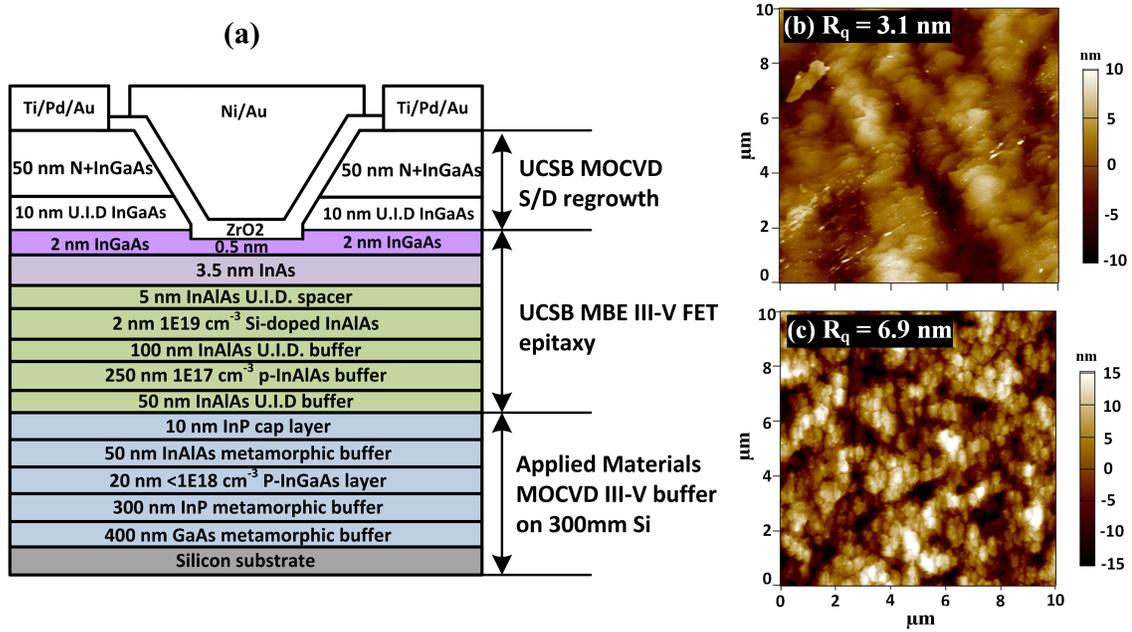


Figure 7.1: (a) Device structure of ultra-thin InAs channel MOSFETs on Si substrates. (b) The AFM image of Applied Materials III-V buffer on Si. (c) The AFM image of the channel surface after MBE III-V FET epitaxy.

Fig. 7.2(a) shows the transmission electron microscope (TEM) image of the whole device. A large amount of threading dislocations in the epitaxial layers and misfit dislocations at the hetero-interface can be observed. The (111) planar defects such as stacking faults or microtwins are also present in the epitaxial layers. Fig. 7.2(b) shows the magnified TEM image on the channel regions, revealing a $\sim$20 nm gate length and $\sim$3.5-4 nm channel thickness. Note that the channel consists of 3.5 nm InAs bottom channel and 0.5 nm InGaAs top channel. Although large long-range surface roughness is observed in the AFM measurements, as the gate lengths become smaller, the long range surface roughness becomes less significant. In fact, the channel surface is smooth locally for a 20 nm-$L_g$ device, as shown in Fig. 7.2(b).
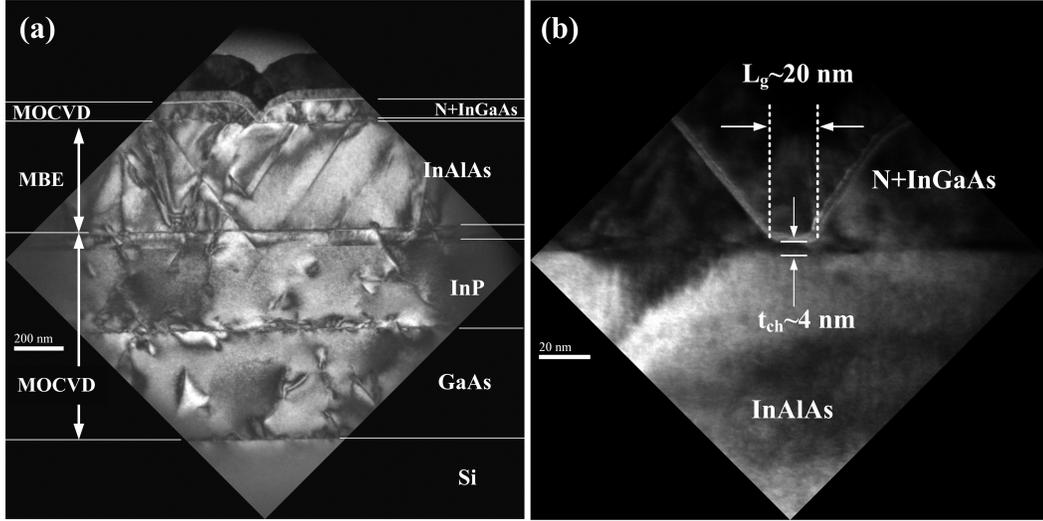
Figure 7.2: (a) A TEM image of the whole device structure, showing Applied Material III-V buffers on Si, UCSB MBE grown back barriers and the InAs/InGaAs channels with $ZrO_2$ high-k/Ni metal gate, and UCSB MOCVD InGaAs source/drain regrowth. (b) The magnified TEM image on the channel regions of a 20 nm-$L_g$ device.

## 7.2 Device performance and comparisons

Fig. 7.3(a) and Fig. 7.3(b) show the $I_D$-$V_{GS}$ and $I_D$-$V_{DS}$ characteristics of 20 nm-$L_g$ devices on Si substrates. The device shows 2.0 mS/$\mu$m extrinsic transconductance ($g_m$) and 142 mV/dec. subthreshold swing ($SS$). The maximum on-state saturation current (Fig. 7.3(b)) is 1.4 mA/$\mu$m. The devices on Si substrates still exhibit high on-state current and transcoductance. The minimum leakage current is closed to 100 nA/$\mu$m for $L_g$-20 nm devices, limited by band-to-band tunneling (BTBT). The off-state leakage for a 1 $\mu$m-$L_g$ device, as shown in Fig. 7.4(a), is about 500 pA/$\mu$m and again dominated by BTBT, indicating that the buffer
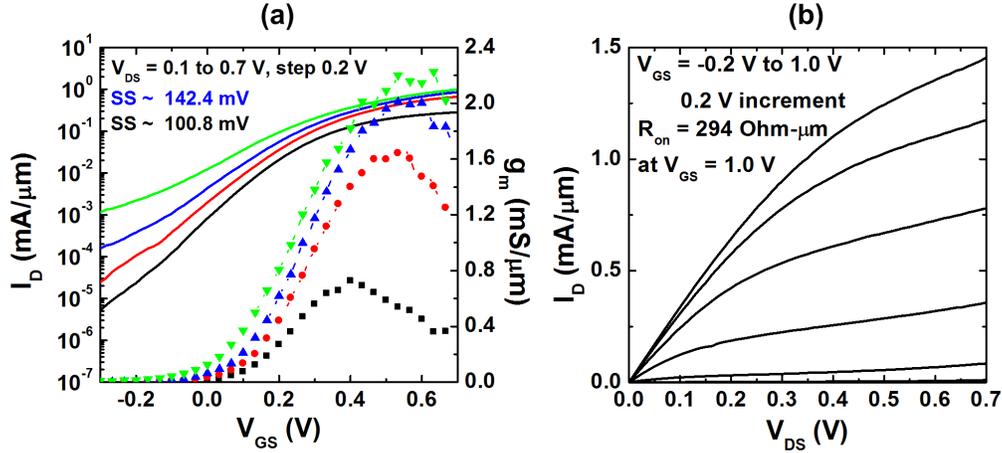
Figure 7.3: (a) $I_\text{D}$-$V_\text{GS}$ of a 20 nm-$L_\text{g}$ device. (b) $I_\text{D}$-$V_\text{DS}$ of a 20 nm-$L_\text{g}$ device.
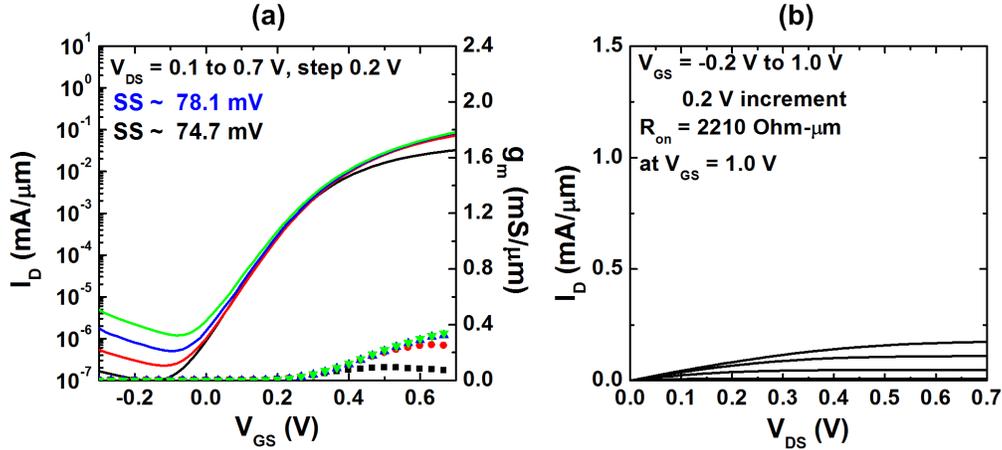


Figure 7.4: (a) $I_\text{D}$-$V_\text{GS}$ of a 1 $\mu$m-$L_\text{g}$ device. (b) $I_\text{D}$-$V_\text{DS}$ of a 1 $\mu$m-$L_\text{g}$ device.

leakage is sufficiently low and negligible. The subthreshold swing for 1 $\mu$m-$L_\text{g}$ device is 78 mV/dec. at $V_\text{DS} = 0.5$ V, higher than the values of III-V FETs on InP ($SS<70$ mV/dec.). The larger $SS$ could be attributed to a slightly thicker channel, inferior semiconductor quality [13], and large surface roughness [14].

Fig. 7.5(a) compares $g_\text{m}$ vs. $L_\text{g}$ for devices on Si and 2.7 nm InAs FETs on InP (see chapter 4.4). The long-channel devices on Si show slightly higher $g_\text{m}$

than in 2.7 nm InAs channel MOSFETs, implying that the mobility of the 3.5 nm InAs channel on Si is higher than that of 2.7 nm InAs channel on InP. Note that thin channel mobility is limited by the interface roughness scattering and drops quickly with the sixth power of channel thickness ($\mu_e \sim T_{\mathrm{ch}}^{-6}$) [15]. Although the channel grown on Si is $\sim$35:1 rougher than that on InP, high electron mobility is still maintained by using a slightly thicker channel.

At small gate lengths, the transconductance of the MOSFETs on Si is inferior to that of 2.7 nm InAs FETs on InP. Fig. 7.5(b) shows $R_{\mathrm{on}}$ vs. $L_{\mathrm{g}}$. The $R_{\mathrm{on}}$ extrapolated to zero $L_{\mathrm{g}}$ is $\sim$247 $\Omega \cdot \mu m$, higher than $\sim$210 $\Omega \cdot \mu m$ reported for 2.7 nm InAs FETs. Further, from transmission line measurement (TLM) measurements (the inset of Fig. 7.5(b) on the samples grown on Si, the regrown S/D shows 20-25% larger sheet resistance and specific contact resistivity than samples grown on InP. We therefore ascribe the poorer of $g_{\mathrm{m}}$ at short $L_{\mathrm{g}}$ for the devices fabricated on Si to both increased parasitic S/D resistance ($R_{\mathrm{SD}}$) and reduced gate-channel capacitance. Because of lattice mismatch and anti-phase domains, III-V heteroepitaxial layers grown on Si contain a high density of dislocations and planar defects, as shown in Fig. 7.2(a). These defects easily propagate to the surface through the MBE channel growth and the MOCVD source/drain regrowth. These defects may cause the increased sheet resistance of the regrown source/drain layers, and consequently reduce the MOSFET $g_{\mathrm{m}}$.

Fig. 7.6(a) and Fig. 7.6(b) show $SS$ and $DIBL$ as a function of $L_{\mathrm{g}}$. Higher $SS$ and $DIBL$ for the 3.5 nm InAs channel devices may be ascribed to the thicker channel; this reducing the electrostatic control of the channel by the gate. The degraded $SS$ may also arise from higher interface trap density because of the
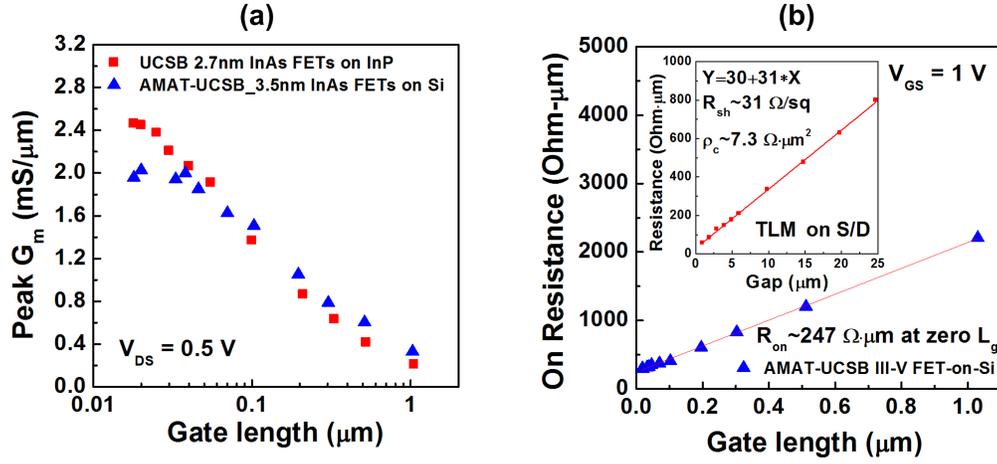
Figure 7.5: (a) Comparison of $g_m$ and (b) $R_{on}$ as a function of $L_g$ for this work on Si substrates and 2.7 nm InAs MOSFETs on InP.
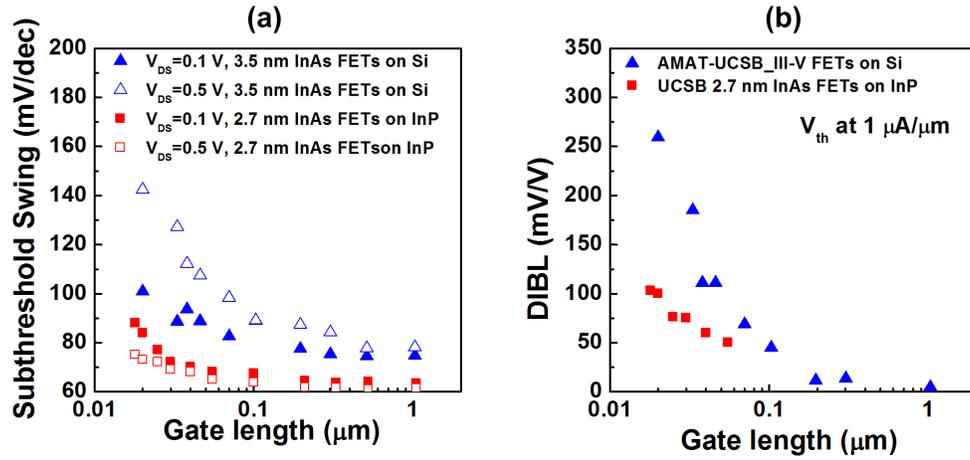


Figure 7.6: (a) Comparison of $SS$ and (b) $DIBL$ as a function of $L_g$ for this work on Si substrates and 2.7 nm InAs MOSFETs on InP.

rough channel surface [14] or poor semiconductor crystalline quality [13]. Further improving the surface roughness would allow further shrinking the channel, and improve $SS$ and $DIBL$.

Fig. 7.7 shows $I_{on}$ at fixed $I_{off}$=100 nA/$\mu$m for recent III-V FETs on Si [1, 3–5, 11]. The devices in this work show peak $I_{on}$=235 $\mu$A/$\mu$m at 100 nm
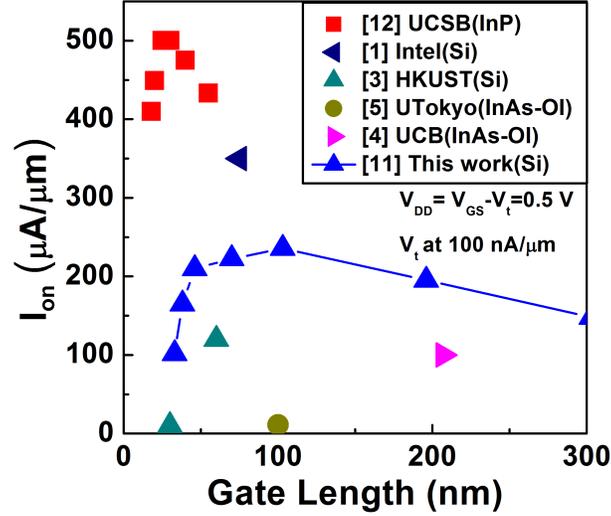
Figure 7.7: $I_{on}$ at fixed $I_{off}$=100 nA/$\mu$m for recently reported planar III-V FETs on Si [1,3–5,11], and compared to results on InP [12].

$L_g$. All the devices on Si show smaller $I_{on}$ than 2.7 nm InAs FETs on InP due to larger $SS$ and smaller $g_m$. Fig. 7.8 shows $g_m$, $SS$, $V_{t,lin}$, $V_{t,sat}$ maps of 45 nm-$L_g$ devices. All devices show the average $g_m$=1.82$\pm$0.10 mS/$\mu$m, while 14 of 15 devices show $g_m$>1.7 mS/$\mu$m. The average $SS$ is 123$\pm$11 mV/dec. The $V_{th}$ at $V_{DS}$=0.1 V is 0.059 V and the $\sigma_{V_{t,lin}}$ $\sim$19 mV. The $V_{th}$ at $V_{DS}$=0.5 V is –0.009 V and the $\sigma_{V_{t,sat}}$ $\sim$28 mV. The $V_{th}$ variation may arise from either variations in channel surface roughness or the gate length. Note that for III-V ultra-thin channels MOSFET, strong quantum confinement effects might increase the threshold voltage variation. Further improved surface roughness might reduce the $V_{th}$ variation within the wafer.

| $G_m$ map (mS/µm) @ $V_{DS}$=0.5V | | | | | |
|---|---|---|---|---|---|
| | | 20 mm | | | |
| | **1** | **2** | **3** | **4** | **5** |
| **A** | 1.90 | 1.73 | 1.74 | 1.90 | 1.93 |
| **B** | 1.85 | 1.88 | 1.81 | 1.76 | 1.88 |
| **C** | 1.80 | 1.55 | 1.86 | 1.86 | 1.91 |

12 mm

**$G_m$~ 1.82 mS/µm, $\sigma_{Gm}$ ~ 0.10 mS/µm**

| Vt, lin (V) @ 1 µA/µm, $V_{DS}$=0.1V | | | | | |
|---|---|---|---|---|---|
| | | 20 mm | | | |
| | **1** | **2** | **3** | **4** | **5** |
| **A** | 0.070 | 0.045 | 0.074 | 0.043 | 0.020 |
| **B** | 0.085 | 0.054 | 0.063 | 0.044 | 0.054 |
| **C** | 0.041 | 0.102 | 0.047 | 0.056 | 0.055 |

12 mm

**$V_{t,lin}$~ 0.056 V, $\sigma_{Vt,lin}$ ~ 19 mV**

| SS map (mV/dec) @ $V_{DS}$=0.5V | | | | | |
|---|---|---|---|---|---|
| | | 20 mm | | | |
| | **1** | **2** | **3** | **4** | **5** |
| **A** | 115.7 | 128.3 | 106.9 | 130.6 | 140.2 |
| **B** | 107.4 | 117.5 | 107.5 | 141.6 | 120.9 |
| **C** | 132.1 | 116.4 | 135.2 | 124.4 | 127.4 |

12 mm

**SS~ 123 mV/dec, $\sigma_{SS}$ ~ 12 mV/dec**

| Vt,sat (V) @ 1 µA/µm, $V_{DS}$=0.5V | | | | | |
|---|---|---|---|---|---|
| | | 20 mm | | | |
| | **1** | **2** | **3** | **4** | **5** |
| **A** | -0.003 | -0.041 | 0.022 | -0.020 | -0.049 |
| **B** | 0.036 | -0.006 | 0.008 | -0.042 | -0.006 |
| **C** | -0.032 | 0.042 | -0.026 | 0.003 | -0.020 |

12 mm

**$V_{t,sat}$~ -0.009 V, $\sigma_{Vt,sat}$ ~ 28 mV**

Figure 7.8: The maps of $g_m$, $SS$, $V_{t,lin}$, $V_{t,sat}$ for 45 nm-$L_g$ devices on the 2 mm×1.2 mm samples.

## 7.3    Summary

In this chapter, we have demonstrated ultra-thin InAs channel MOSFETs on Si with high performance and high yield. The FET delivers high $I_{on}$ and high extrinsic transconductance ∼2.0 mS/$\mu$m at $V_{DS}$=0.5 V. Increasing the channel thickness reduces scattering in the rough channel, but degrades $SS$ and $I_{on}$ at short $L_g$. Further improved channel growth and surface roughness might improve threshold voltage variations, and allow a thinner channel, thus improving $SS$ as well as $I_{on}$ at fixed $I_{off}$. Improved source/drain regrowth could reduce source/drain parasitic resistance and increase transconductance for short $L_g$ devices.

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# Chapter 8

# Conclusion

## 8.1   Summary

Toward the ultimate goal of replacing Si channels, III-V MOSFETs must have higher performance than Si MOSFETs as well as very low leakage currents with low standby power consumption. Unfortunately, III-V MOSFETs are vulnerable to high subthreshold leakage and high band-to-band tunneling leakage because of larger material permittivity and smaller band-gap. Fig. 8.1 shows the progressive III-V MOSFET designs for reducing the leakage currents. Early UCSB III-V MOSFETs suffer from large channel leakage as well as back barrier leakage. Therefore, AlAsSb wide-band gap barriers with larger conduction band offset to InGaAs were developed to reduce such barrier leakage. The electron transport in InGaAs/AlAsSb heterostructure shows larger interface roughness scattering than that in InGaAs/InAlAs heterojunctions. The InGaAs MOSFETs with AlAsSb barriers effectively reduce the buffer leakage, in particular for short gate length devices. However, because of process difficulties of AlAsSb barriers, p-type doped InAlAs barriers were also developed to diminish barrier leakage.

With the optimized bottom barrier designs, the main leakage component is now located at the channels. High channel leakage current is caused by subthreshold leakage and band-to-band tunneling leakage at the drain end of the channels. To control the subthreshold leakage, thinner channels were implemented to enhance the gate control on channel potential and the raised InGaAs source/drain vertical spacers were developed to improve electrostatics. The band-to-band tunneling leakage is highly dependent on the channel band-gap, so reducing the channel thickness with resultant increased confinement band-gap or increasing Ga/In alloy composition ratio greatly reduces the band-to-band tunneling leakage. The
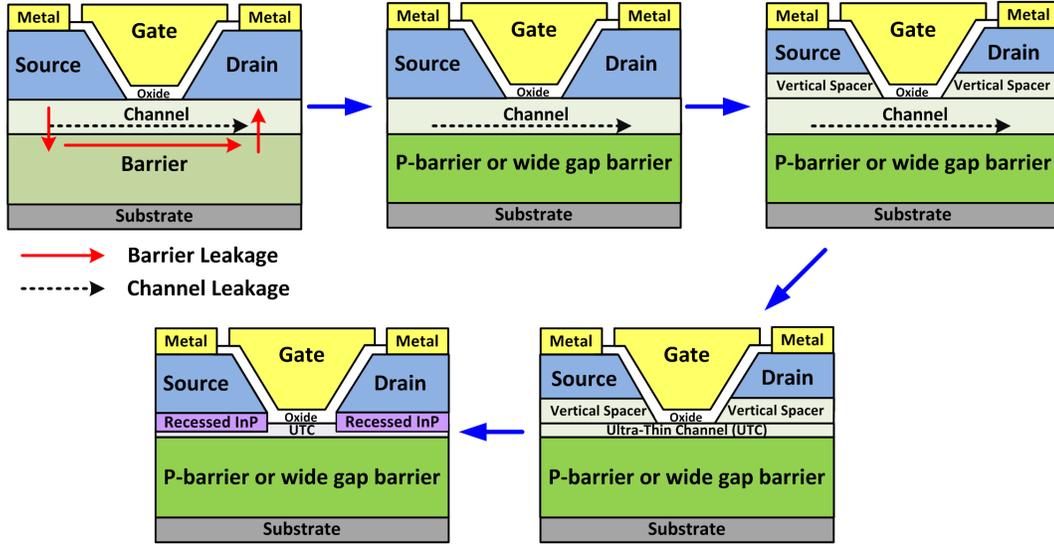
Figure 8.1: Progression of III-V MOSFET designs for reduced off-state leakage.

raised InGaAs source/drain vertical spacers not only improve channel electrostatics, reducing the subthreshold leakage, but also smooth the electric field near the drain, reducing the BTBT leakage. We noticed that the thin InAs channels still show superior on-state performance, while thin InGaAs channels show large performance loss. This could arise from the electron interaction with the oxide traps, having trap energy level above the conduction band-edge of the III-V channels; the As-As anti-bonding is the main culprit for this trap. Because of strong quantum confinement in thin channels, InGaAs channels have first sub-band energy very close to the trap energy of As-As anti-bonding, thereby having the stronger electron interaction with the oxide trap and degrading the on-state performance.

With an ultra-thin 2.7 nm InAs channel and 12 nm InGaAs raised source/drain spacers, we were able to demonstrate a high performance InAs MOSFET, with on-state performance comparable to 22 nm Si FinFETs. The $I_{\mathrm{on}}$ is 500 $\mu$A/$\mu$m at $V_{\mathrm{DS}}$=0.5V and $I_{\mathrm{off}}$=100 nA/$\mu$m. Although this device shows promising on-

state performance, the minimum off-state leakage is saturated at 10 nA/$\mu$m at $V_{DS}$=0.5V. For low standby power logic applications, the leakage current must be reduced to the level below 100 pA/um. In consequence, we developed recessed InP source/drain spacers. By replacing the small band-gap InGaAs materials with the wide band-gap InP spacers at the concentrated electric field regions, the band-to-band tunneling leakage is dramatically reduced about two orders of magnitude as compared to FETs with InGaAs spacers. A low leakage III-V MOSFET was demonstrated with minimum $I_{off}$ ~60 pA/$\mu$m at $V_{DS}$=0.5 V and $L_g$ = 30 nm. This recessed InP spacer technique enhances device scalability and enables III-V MOSFETs for low standby power logic applications.

Furthermore, with an extremely thin 2.5 nm InGaAs/InAs composite channel and a doping-graded recessed InP source/drain spacer, we demonstrated a 12 nm III-V MOSFET with maximum on-off ratio over $8.3 \times 10^5$, the extrinsic tansconductance 1.8 mS/$\mu$m, the subthreshold swing around 107 mV/dec., and the minimum $I_{off}$ as low as 1.3 nA/$\mu$m. This device has leakage current sufficiently low for standard performance logic applications. This result confirms that III-V MOSFETs can scale to sub-10-nm technology nodes.

Last, we demonstrated the ultra-thin InAs MOSFETs on Si substrates. Despite having large long range surface roughness, a 20 nm-$L_g$ FET still shows large on-state current and high extrinsic transconductance. High yield and low device variations were obtained. These results demonstrate the promising potential for using III-V channels on Si for future VLSI CMOS logic technology.

## 8.2    Future work

MOSFETs at sub-10-nm nodes face enormous challenges, including electro-statics, leakage currents, contact resistivity, and insufficient on-state current at lower $V_{DD}$. From Fig. 5.17, we clearly observe the degradation of $I_{on}$ at smaller gate lengths. This indicates that the electrostatics in UCSB planar MOSFETs are insufficient for scaling down to the sub-10-nm technology nodes. Thinner chan-nels and thicker spacers improve electrostatics, while losing on-state performance. Therefore, new device architecture such as III-V FinFETs or nanowire MOSFETs are required for continuous scaling. On the other hand, with the help of FinFETs and nanowire MOSFETs on electrostatics, only a small amount of recessed InP spacer is needed to reduce band-to-band tunneling leakage. Hence, the on-state resistance ($R_{on}$) can be reduced and the on-state performance can be improved. Further improvement on InP spacers is highly desirable to reduce the parasitic source/drain resistance.

Future transistors will also require extremely low contact resistivity because the contact resistance is much larger than the channel resistance at small gate lengths. The lowest contact resistivity obtained by A. Baraskar in UCSB is $5 \times 10^{-9}$ $\Omega \cdot cm^{-2}$ for heavily doped N+InAs [1], which is slightly higher than the state-of-art Si MOSFETs. The lowest contact resistivity of Si MOSFETs is $2 \times 10^{-9}$ $\Omega \cdot cm^{-2}$ for N-contact on heavily phosphorous-doped Si [2], and $1.5 \times 10^{-9}$ $\Omega \cdot cm^2$ for p-contact on heavily Boron-doped $Si_{0.7}Ge_{0.3}$ [3]. At the end of scaling roadmap, if III-V MOSFETs are about to replace Si MOSFETs, a very low contact resistivity at a highly scaled contact is the must-have for nanoscale MOSFETs. New inno-vations and experimental breakthroughs on III-V contacts are highly demanding.

Last, although UCSB InAs ultra-thin-body MOSFETs show the record performance of III-V MOSFETs at a VLSI relevant gate length (25 nm-$L_\mathrm{g}$) and perhaps performance comparable to 22 nm Si FinFETs, the results are still inferior to the most advanced 14 nm Si FinFETs [4]. To achieve the final goal, III-V MOSEFTs must have substantial performance improvements over Si MOSFETs to justify the cost for developing a production III-V MOSFET technology.

In fact, there is still a long way to go.

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# Appendix A

# MOSFET Process Flow

Figure A.1: UCSB Gate Last Process Flow.

| Loop | Stop No | Process step | Equipment | Process |
|------|---------|--------------|-----------|---------|
| MBE | 1.1 | Wafer clean (Optional) | MBE lab bench | Dilute HCl ($H_2O$:HCl=10:1) dip 1 min.<br>*Skipped for epi-ready InP subtrates. |
| | 1.2 | MBE growth | System C | 1. InP oxide desorbs (spike anneal) at 550 °C under As-BEP~$1E10^{-5}$ torr<br>2. InAlAs buffer growth: 490°C, G.R.: 1.331 Å/s, As/III BEP~33.<br>3. InGaAs channel growth: 460 °C, G.R.: 1.329 Å/s, As/III BEP~28.<br>4. InAs channel growth: <400 °C, As/In BEP~5.8, G.R.:0.7 Å/s |
| Dummy Gate | 10.1 | Solvent Clean | Solvent Bench | Aceton/IPA/DI clean |
| | 10.2 | $Al_2O_3$ adhesion layer | Oxford-FlexAL ALD | 300°C $Al_2O_3$ (TMA+$H_2O$)1 nm |
| | 10.3 | Solvent Clean | Solvent Bench | Aceton/IPA/DI clean |
| | 10.4 | Dehydration | PR Bench | 110°C 5 min |
| | 10.5 | HSQ Spin coating | PR Bench | 1. Warming up 2%HSQ at room temperature for 15 mins<br>2. Spin coating 2%HSQ at 5000 rpm/min for 30 sec (Recipe 9) |
| | 10.6 | Solvent Removal | PEII | 2 mins to remove HSQ solvent, and vent EB/LL simultaneously |
| | 10.7 | E-Beam lithograhy | JEOL 6500 | 1. 500 pA, dose:2000, Aperture3<br>2. Recipe: yymmdd_NEWHSQV10.jdf and *.sdf, and *.mgn |
| | 10.8 | EB Developer | Develop bench | 1. NaOH:NaCl:H2O = 2g: 8g:200mL<br>2. 50 sec develop (note: Unexposed HSQ and $Al_2O_3$ are removed) |
| S/D Regrowth | 20.1 | Dummy gate bake | Hotplate | 150°C, 30 mins: avoid HSQ outgas at MOCVD |
| | 20.2 | Digital etch | UV ozone | One cycle digital etch before regrowth (15min UV ozone+dilute HCl dip 1min)<br>*Several cycles for recessed spacers |
| | 20.3 | HCl dip | Acid bench | 10:1 $H_2O$:HCl dip (30 sec to 1 min) |
| | 20.4 | MOCVD Source/Drain Regrowth | Thomas Swan MOCVD | 1. n+InGaAs (~4E19 cm$^{-3}$): 350 torr, 600 °C, GR:1.77 Å/s, $Si_2H_6$: 40sccm<br>2. n+InP (~5E19 cm$^{-3}$): 350 torr, 550 °C, GR:1.95 Å/s, $Si_2H_6$: 40sccm |
| | 20.5 | Inspection: Sheet resistance | Four point probe | Sheet resistance~25 Ohm/□ for 50 nm n+InGaAs |
| | 20.6 | Inspection: SEM & OM | SEM & OM | Regrowth check |
| Mesa Isolation | 30.1 | Solvent Clean | Solvent Bench | Aceton/IPA/DI clean |
| | 30.2 | Dehydration | PR bench | 110°C 5min |
| | 30.3 | SPR 955 PR coating | Spin Coater | 1. HMDS 20s soaking<br>2. HMDS Spin (Recipe 7: 4000 rpm/min)<br>3. Wait 1min<br>4. SPR 955 (Recipe: : 4000 rpm/min) |
| | 30.4 | PreExposure Bake | PR Bench | 90°C, 1min |
| | 30.5 | Exposure | GCA200 | Mask: B1_ISO (MOSGATELASTV6), Exposure time 0.27s, JOB name: SLINSHOT/INSHOT |
| | 30.6 | PostExposure Bake | PR Bench | 110°C, 1min |
| | 30.7 | Develop | PR Bench | AZ MIF 300 develop 1 min |
| | 30.8 | Mesa Isolaiton etch | Acid Bench | 1. Citric Acid:$H_2O_2$:$H_2O$=50g:75ml:50ml, 90sec: remove 60nm InGaAs (10 nm channel + 50 nm regrowth)<br>2. $H_3PO_4$:$H_2O_2$:$H_2O$=10ml:10ml:250ml, 15 sec: remove 80nm InAlAs<br>3. HCl:$H_3PO_4$=40ml:160ml, 13 sec: remove 23 nm InP |
| | 30.9 | Etch depth control | DETAK | Etch stops at undoped InAlAs buffer |
| | 32.0 | PR Strip | Isothermal tank | 1165 overnight |
| | | | | Process continues in next page. |

| Loop | Stop No | Process step | Equipment | Process |
|---|---|---|---|---|
| **HK/MG** | 40.1 | Solvent Clean | Solvent Bench | Aceton/IPA/DI clean |
| | 40.2 | Dummy gate removal | HF Bench | BOE etch 90 sec |
| | 40.3 | Digital etching | UV Ozone/Acid bench | 15 min UV ozone and 30 sec BOE/dilute HCl dip (at least 1 cycle, etch rate:1.5nm/cycle) |
| | 40.4 | BOE etch | HF Bench | 2 min to remove native oxide |
| | 40.5 | High-k deposition | Oxford-FlexAL ALD | TMA-N* plasma clean + $HfO_2$ or $ZrO_2$ |
| | 40.6 | Solvent Clean (Optional) | Solvent Bench | Aceton/IPA/DI clean |
| | 40.7 | FGA anneal | Rodwell Furnace | 1. 400°C forming gas (5%/95% $H_2/N_2$), 15 min anneal, ramp: 10°C/min 2. Natually cooling down with furnance power off (~1hr) 3. Take out sample when T<150°C |
| | 40.8 | Solvent Clean | Solvent Bench | Aceton/IPA/DI clean |
| | 40.9 | Dehydration | Hotplate | 110°C 5min |
| | 42.0 | nLOF 5510 PR coating | Spin Coater | 1. HMDS 20s soaking 2. HMDS Spin (Recipe 7: 4000 rpm/min) 3. Wait 1min 4. nLOF5510 (Recipe 7: 4000 rpm/min) |
| | 42.1 | PreExposure Bake | PR Bench | 90°C, 1min |
| | 42.2 | Exposure | GCA200 | Mask: LIFT2 (SLEE), Exposure time 0.27s, JOB name:SLINSHOT\INSHOT |
| | 42.3 | PostExposure Bake | PR Bench | 110°C, 1min |
| | 42.4 | Develop | PR Bench | AZ MIF 300 develop 1 min |
| | 42.5 | Metal gate Evaporation | Thernal Evaporator | Ni 35-50 nm (1Å/sec), Au 120-160 nm (2~3Å/sec) |
| | 42.6 | PR Strip | Isothermal tank | 1165 overnight |
| **S/D Contact** | 50.1 | Solvent Clean | Solvent Bench | Aceton/IPA/DI clean |
| | 50.2 | Dehydration | PR Bench | 110°C, 5min |
| | 50.3 | nLOF 5510 PR coating | Spin Coater | 1. HMDS 20s soaking 2. HMDS Spin (Recipe 7: 4000 rpm/min) 3. Wait 1min 4. nLOF5510 (Recipe 7: 4000 rpm/min) |
| | 50.4 | PreExposure Bake | PR Bench | 90°C, 1min |
| | 50.5 | Exposure | GCA200 | Mask: BL_SD, Exposure time 0.27s, JOB name: SLINSHOT/INSHOT |
| | 50.6 | PostExposure Bake | PR Bench | 110°C, 1min |
| | 50.7 | Develop | PR Bench | AZ MIF 300 develop 1 min |
| | 50.8 | Oxide removal | HF Bench | BOE 90 sec |
| | 50.9 | S/D Metal | EB1 | Ti 20nm: 0.7Å/sec Pd 20nm:1.2Å/sec Au 120nm: 2.5Å/sec |
| | 52.0 | PR Strip | Isothermal tank | 1165 overnight |
| **Device measurement** | | | | |