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Indium Phosphide Heterojunction Bipolar Transistors with Emitter Regrowth by Molecular Beam Epitaxy

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical Engineering

by

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June 2013

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D.W. Scott, C. Kadow, Y. Dong, Y. Wei, A.C. Gossard, and M.J.W. Rodwell "Low-resistance n-type polycrystalline InAs grown by molecular beam epitaxy," *Journal of Crystal Growth*, vol. 267, no. 1-2, June 2004, pp. 35-41.

D. Scott, Y. Wei, M. Urteaga, and M.J.W. Rodwell, "RF performance and process development of InP DHBTs using non-selective emitter regrowth," IEEE International Conference on Indium Phosphide and Related Materials, Kagoshima, Japan, May 31-June 4, 2004.

D.W. Scott, Y. Wei, Y. Dong; A.C. Gossard, and M.J.W. Rodwell, "A 183 GHz and 165 GHz regrown-emitter DHBT with abrupt InP emitter," *IEEE Electron Device Letters*, vol. 25 , no. 6, June 2004, pp. 360-2.

ABSTRACT

Indium Phosphide Heterojunction Bipolar Transistors with Emitter Regrowth by Molecular Beam Epitaxy

by

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A novel InP-based heterojunction bipolar transistor (HBT) technology using molecular beam epitaxy (MBE) regrowth to form the emitter-base heterojunction and emitter capping layers is presented in this dissertation. The motivation for this work is to combining the positive attributes of the SiGe HBT device structure and fabrication technology with the superior attributes of III-V material systems. The intention of this work is to provide initial investigations into the required material properties as well as initial demonstrations of devices with regrown emitters.

Low-resistance polycrystalline InAs (poly-InAs) deposited onto silicon nitride (SiN_x) dielectric is demonstrated, and an investigation into material property dependencies on deposition conditions is presented. Low-resistance poly-InAs may be used as an emitter capping material in an InP HBT with regrown emitter where the emitter contact material is wider than the base-emitter junction area. An emitter contact area larger than the emitter junction allows scaling of the device to reduce parasitic capacitances without introducing detrimental parasitics to the emitter contact resistance. Such an HBT could be produced using a patterned base-collector template covered in SiN_x with openings in the dielectric in areas where emitter junctions are

desired. Areas where the base semiconductor is exposed to emitter regrowth would produce a monocrystalline emitter, and areas where deposition occurs onto SiN_x would produce polycrystalline material.

A graded InAlAs emitter with InAs emitter cap was used in the initial demonstrations of the regrown emitter HBT. Large-area devices were used to successfully demonstrate proof-of-concept devices and to make the first-order improvements required for a small-area RF device demonstration. The first small-area regrown emitter InP HBT with emitter contact area wider than the $0.7 \times 8\ \mu m^2$ base-emitter junction demonstrated 160 GHz peak f_τ and simultaneous 140 GHz f_{max}. Further studies into the base-collector template surface preparation process produced an improved regrowth surface with near-epitaxial smoothness. A simplified, abrupt InP emitter regrowth onto this surface produces regrowth similar to what is observed for growth onto epi-ready InP substrates. The improved regrown emitter HBT with $0.7 \times 8\ \mu m^2$ InP emitter area is used to demonstrate a simultaneous 183 GHz f_τ and 165 GHz f_{max}.

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Chapter 1

Introduction

This work presents a summary of a novel InP-based heterojunction bipolar transistor (HBT) technology that employs molecular beam epitaxy (MBE) regrowth to form the emitter-base heterojunction and emitter capping layers. This work is intended as a first step in combining the positive attributes of the SiGe HBT structure and fabrication technology with the positive attributes of III-V material systems. A simple understanding of the recent trends in III-V and SiGe-based HBT technology is helpful to understand the factors that motivate this work. A brief review of HBT technology, device parameters, and current trends in HBT performance will be presented in this chapter.

Research in wide bandwidth HBTs is driven by applications in radar, high-speed communication such as microwave and millimeter-wave wireless, and large capacity optical fiber communications systems. Wireless receivers and transmitters require low-noise RF preamplifiers, multiple stages of amplification, and frequency conversion, which are typically implemented as small-scale monolithic millimeter integrated circuits (MMICs). Although the operating frequency of these circuits is set by the application, advancements in transistor performance allows for the evolution of

the applications to progressively higher frequencies. III-V HBT technology offers advantages in higher transconductance, better threshold voltage control, higher output resistance, and higher current driving capability than its III-V counterparts in metal semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs) which currently dominate the MMIC applications.

InP-based HEMTs are prevalent in MMIC applications because the technology has established a lead in high frequency performance. InGaAs/InAlAs HEMTs with 45 nm gate lengths were reported with maximum current gain cutoff frequencies ($f\tau$) over 400 GHz as early as 2001.[1] Separately, transistors with 100 nm gate lengths and maximum oscillation frequencies (f_{max}) of 600 GHz were reported in 1995.[2] These performance demonstrations were achieved through the use of aggressive lithographic scaling in the III-V material system. In contrast, aggressive lithographic scaling of III-V HBTs has not been prevalent. Commercial InP and GaAs-based HBTs are typically fabricated with emitter widths of 1 to 2 μm and collector junction widths of 3 to 5 μm.

By comparison, state-of-the-art SiGe-based HBTs are fabricated with < 0.2 μm emitter-base junction widths, and have obtained simultaneous f_τ and f_{max} results of 270 and 260 GHz and a record f_τ of 350 GHz.[3] SiGe-based HBTs employ superior fabrication techniques to obtain deep submicron features in a planar, Si-compatible fabrication process. The silicon fabrication technology and the silicon bipolar device structure allows for extreme levels of parasitic reduction in SiGe HBTs relative to III-V HBTs. These features allow SiGe to remain competitive in the high-speed digital and mixed-signal applications. III-V HBTs maintain a superior bandwidth advantage

despite larger device parasitics, a relatively immature fabrication technology, and consequently, higher costs and lower scales of integration. The lead in device bandwidth is maintained by the intrinsic properties of the III-V material system. GaAs and InP lattice-matched materials allow for bandgap energy variations so the emitter bandgap may be much larger than that of the base material. This allows the base region to be very heavily doped, ~10^{20} cm^{-3}, to reduce base sheet resistance while minority carrier injection into the emitter region remains low. In contrast, the lattice mismatch constraints in Si/SiGe HBTs limit the allowable Ge to Si alloy ratio and a weaker heterojunction is formed. The emitter-base bandgap energy difference is much less than that in III-V materials and lower base doping must be used. Higher electron velocities are also a significant advantage in III-V materials. In InAlAs/InGaAs HBTs with 0.2 to 0.3 μm collector thickness, the effective electron velocity is approximately four times higher than that observed in Si. The higher electron velocity results in higher current-gain cutoff frequencies.

1.1 Brief history of the heterojunction bipolar transistor

W. H. Brattain and J. Bardeen demonstrated power amplification in a three-terminal point-contact semiconductor device on December 16, 1947 at Bell Telephone Laboratories.[4,5] Shortly afterwards, group leader W. B. Shockley presented the theory of p-n junctions and of bipolar junction transistors.[6] In June 1948, Shockley filed a U.S. patent describing the idea of a wide bandgap semiconductive emitter material to achieve a bipolar transistor with high carrier injection efficiency into a

narrower bandgap base.[7] Independently, Kroemer theoretically described the same principle in a 1957 paper published in *Proceedings of the IRE*.[8]

It was at about this time that the first experimental demonstrations of heterojunctions began to appear. Jenny of RCA Laboratories attempted to form a GaAsP/GaAs heterojunction by diffusing phosphorous into GaAs[9], but the technique was never successful because the diffused junctions were not very abrupt. This work emphasized the need to create abrupt junctions by epitaxial growth. Researchers at IBM were the first to report grown heterojunctions of Ge on GaAs in 1958.[10] The experimental behavior of the Ge/GaAs junction was verified by the theory of heterojunction operation developed by Anderson in 1962[11], and the success of this initial work motivated continued efforts on the growth of heterojunctions.

It was not until 1969 that Jadus and Feucht demonstrated the first functional HBT with a heterojunction formed by growing Ge on GaAs.[12] This transistor structure achieved a common-emitter current gain of ~10 with a base doping level four orders of magnitude higher than that of the emitter. This confirmed the theoretical proposals set forth by Shockley and Kroemer years earlier. It was generally realized, though, that defect currents caused by poor interfacial properties limited the gain of these devices. Further research, therefore, began to focus on the employment of new material systems and epitaxial growth methods to realize heterojunction interfaces with relatively low defect levels.

By the early 1970s it was shown that the AlGaAs/GaAs material system could be used to produce a heterointerface with low defect density. This low defect density

is attributed to the small lattice mismatch over the full range of the $Al_xGa_{1-x}As$ alloy composition. Dumke, Woodall, and Rideout at IBM grew the first AlGaAs/GaAs HBT in 1972 using liquid phase epitaxy (LPE).[13] Work on the HBT continued throughout the 1970s and 1980s with emphasis still being placed on the development of growth techniques and material systems. The emergence of MBE and metal-organic chemical vapor deposition (MOCVD) as viable methods for growing high-quality epitaxial structures helped to accelerate HBT research and lead to high-performance HBTs.

1.2 Scaling in III-V HBTs

Despite the evolution of III-V material epitaxy, less attention has been focused on improving the device structure until the last decade. For instance, in 1995 the fastest InP-based HBTs[14] were still formed using a triple-mesa structure as shown in Figure 1.1. Moderate scaling of the epitaxy (vertical scaling) and device dimensions (lateral scaling) allowed for progress up to this point, but the triple-mesa device structure eventually impeded further progress. Improvements to the device by scaling suggest that the reduction in device dimensions, either lateral or vertical, will result in an improved frequency response. Transistor bandwidths are generally determined by carrier transit times and RC charging time constants. HBT transit times are reduced by decreasing the thickness of the base and collector epitaxial layers. Reducing the epitaxial thicknesses, however, will lead to an increase in base resistance and collector capacitance unless accompanied by lateral scaling of the base and collector junction

widths. This example suggests that the full benefits of scaling III-V HBTs are only realized if all transistor parasitics are simultaneously reduced.

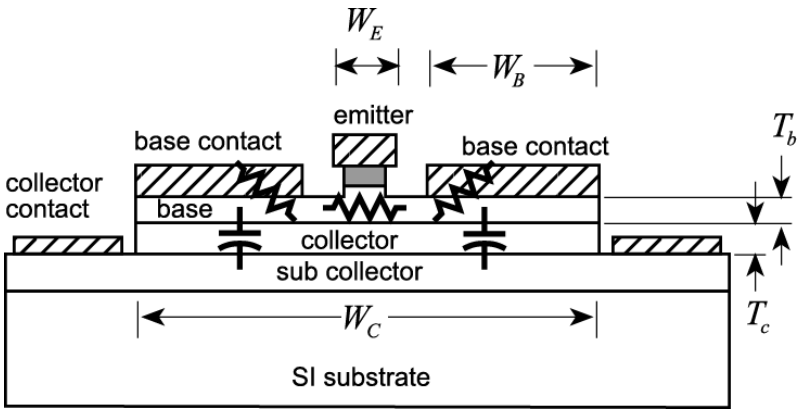


Figure 1.1 Cross-section of a mesa HBT. The emitter-base junction has width W_e, length L_e, and area $A_e = L_e W_e$. The collector-base junction has width W_c, length L_c, and area $A_c = L_c W_c$.

The simplified cross-section of a mesa HBT shown in Figure 1.1 illustrates the difficulty in scaling the transistor's collector-base junction. The patterned etches and metal depositions that form the HBT junctions result in a device structure where the collector-base junction must lie beneath the full area of the base ohmic contacts. To obtain low base contact resistance, the base ohmic contact must be at least one contact transfer length, $L_{contact}$, wide at the sides of the emitter stripe. For an HBT with a 400 Å thick InGaAs base and 5×10^{19} cm^{-3} doping, $L_{contact} \cong 0.4$ μm. Process tolerances for lithographic alignment may further limit the minimum collector-base junction dimensions.

In literature, transistor bandwidth is often described by the figures-of-merit current gain cutoff frequency f_τ and the power gain cutoff frequency f_{max}. The current

gain cutoff frequency is the maximum frequency at which the magnitude of AC current gain (h_{21}) decreases to unity. Beyond f_τ the device will have current gain less than unity. The maximum oscillation frequency f_{max} is the frequency at which the unilateral power gain of the transistor tends to unity. The unilateral power gain effectively represents the maximum power gain that is achievable by the transistor, and transistors cannot provide power gain at frequencies above f_{max}. In more general analog and digital circuits, these figures-of-merit may not accurately predict the circuit performance. For instance, f_τ is commonly used to evaluate a transistor's potential in digital logic applications. However, a detailed charge analysis of switching times reveals that device current density, collector-base junction capacitance, and emitter resistance make much larger fractional contributions to logic gate delay than they contribute to the emitter-collector forward delay $\tau_{ec}=1/2\pi f_\tau$.[15] In analog and digital circuits, f_τ and f_{max} are used to provide a first order estimate of device transit delays and of the magnitude of the dominant transistor parasitics.

The cutoff frequencies can be estimated from HBT parameters calculated from the physical device properties and fit to a lumped-element device model. Experience shows that the simple hybrid-π small-circuit equivalent model shown in Figure 1.2 is sufficient to describe all but the most highly scaled devices up to a frequency of 110 GHz. Although some concerns exist regarding the accuracy of the model at higher frequencies and in describing highly scaled devices[16], this first-order model is excellent for determining the terms that limit transistor bandwidth.

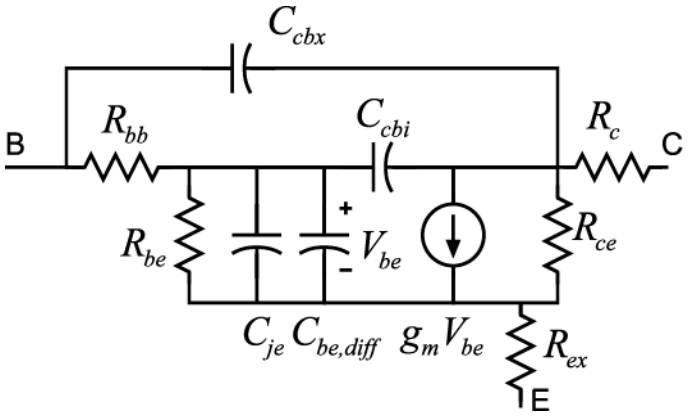


Figure 1.2 Hybrid- π small-signal HBT equivalent circuit. $C_{cbe,diff} = g_m(\tau_b + \tau_c)$.

The scaling analysis that follows has been presented elsewhere in greater detail. It is repeated here for completeness as the benefits of device scaling motivate the approach of using the regrown emitter structure presented in this thesis.

1.2.1 Factors determining f_τ

This approach to HBT scaling is derived from the parameters that limit device bandwidth. The current-gain cutoff frequency is given by a sum of transit times and charging delays:

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}\left(C_{je} + C_{cb}\right) + \left(R_{ex} + R_c\right)C_{cb} \qquad (1.1)$$

where τ_b and τ_c are the base and collector transit times, R_{ex} and R_c are the parasitic emitter and collector resistances, C_{je} and C_{cb} are the emitter-base and base-collector junction capacitances, and I_c is the collector current.

Examining each component separately, τ_b is the base transit time which depends on the base thickness, bandgap energy grading variation in the base layer, and upon the carrier properties such as mobility and diffusion in the base region. If a linear grading of the base semiconductor bandgap energy with position is used to reduce τ_b, then [17]

$$\tau_b = \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right) - \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right)^2\left(1 - e^{-\Delta E/kT}\right) + \frac{T_b}{\upsilon_{exit}}\left(\frac{kT}{\Delta E}\right)\left(1 - e^{-\Delta E/kT}\right) \qquad (1.2)$$

where ΔE is the grading in the base bandgap energy, T_b the base thickness, and D_n is the base minority carrier diffusivity. The base exit velocity υ_{exit} is of the order $(kT/m^*)^{1/2}$ for a non-graded base[18], and is somewhat larger with base bandgap grading. In this relation, m^* is the effective mass of the electron. For a typical InGaAs base at 5×10^{19} cm^{-3} doping, 52 meV bandgap grading is sufficient to reduce τ_b by ~2:1.[15] For a thick base layer or a large υ_{exit}, $\tau_b \propto T_b^2$; with InGaAs base layers below ~400 Å thickness, the exit velocity term in Eqn. 1.2 adds a significant correction.

The collector transit time τ_c is the mean delay of the collector displacement current which is a ratio of the collector thickness T_c and the effective carrier velocity given by [19,20]

$$\tau_c = \int_0^{T_c} \frac{(1 - x/T_c)}{\upsilon(x)}\,dx \equiv \frac{T_c}{2\upsilon_{eff}}, \qquad (1.3)$$

where $\upsilon(x)$ is the position-dependent electron velocity in the collector drift region and υ_{eff} is an effective electron velocity. τ_c is most strongly dependent upon the electron

velocity in the proximity of the base, and becomes progressively less sensitive to the electron velocity as the electron passes through the collector.[20] In HBTs with thin epitaxial layers, nonequilibrium electron transport is observed in the collector drift region.[21] At low collector-base bias voltages, electrons may travel through a significant fraction of the collector drift region in the high velocity Γ-valley before acquiring sufficient kinetic energy (0.55 eV for InGaAs [22], 0.6 eV for InP [23]) to scatter to the lower velocity L-valley. The result is that $\upsilon(x)$ is highest near the base. This velocity overshoot effect significantly reduces collector transit time and in structures with thin InGaAs or InP collector regions (< 3000 Å), υ_{eff} = 3-5 × 10^7 cm/s. By contrast, measured saturation velocities in thick InGaAs drift layers are in the range of υ_{sat} = 6 to 9 × 10^7 cm/s.[22]

The RC charging terms in Eqn. 1.1 contribute a significant fraction of the total forward delay in submicron HBTs, and these terms must be considered in detail. In the term $[kT/qI_c]C_{cb}$ the collector current density is limited by the onset of base push-out (the Kirk effect[24]). At high collector current densities, electron space charge screening at the edge of the base-collector junction eventually leads to a collapse of the electric field. Holes may then diffuse into the collector and effectively extend the base region, leading to an increase in base transit time and collector-base capacitance. It has been demonstrated that GaAs HBTs may exhibit improved f_τ when biased close to the Kirk threshold[21], as the reduced electric field at the collector-base junction edge increases velocity overshoot and reduces the collector transit time. We will ignore this possibility while considering the contribution of $(kT/qI_c)C_{cb}$ to f_τ.

From electrostatic considerations, the maximum collector current before base push-out is

$$I_{c,\max} = A_e(V_{cb} + \phi)3\varepsilon\upsilon_{sat} / T_c^2 \propto A_e / T_c^2 \qquad (1.4)$$

where υ_{sat} is an assumed uniform electron velocity within the collector, and the collector doping N_d is chosen to obtain a fully-depleted collector at zero bias current and the applied V_{cb}. The collector capacitance is $C_{cb}=\varepsilon A_c/T_c$. With the HBT biased at $I_{c,max}\propto 1/T_c^2$, $(kT/qI_c)C_{cb}= T_c(A_c/A_e)$. This delay term is thus minimized by scaling (reducing T_c), but bias current densities must increase in proportion to the square of the desired fractional improvement in f_τ.

The emitter charging time $(kT/qI_c)C_{je}$ in Eqn. 1.1 plays a significant role in determining f_τ. If C_{je} is assumed to be a simple depletion capacitance, it would be reasonable to expect that the charging time could be minimized by making the emitter-base depletion region very thick with use of very low emitter doping combined with a thick bandgap grading region in the base-emitter heterojunction. The tradeoffs between the depletion capacitance and excessive charge storage in the depletion layer are described in detail elsewhere and the results are repeated here.[15] Using methods similar to those used to derive the collector transit time [19,20]

$$C_{je} / A_e = \varepsilon / T_{eb} + \frac{\partial}{\partial V_{be}}\left[\int_0^{T_{eb}} (x / T_{eb}) qn(x) dx\right] \qquad (1.5)$$

where T_{eb} is depletion layer thickness and $n(x)$ is the electron density in the depletion region. The term in $(kT/qI_c)C_{je}$ Eqn. 1.1 can then be written as

$$(kT/qI_c)C_{je} = \left(\frac{\varepsilon A_e}{T_{eb}}\right)\left(\frac{kT}{qI_c}\right) + \frac{\Gamma T_{eb} T_b}{D_n}\int_0^1 \frac{n(\zeta T_{eb})}{n(T_{eb})}\zeta^2 d\zeta \qquad (1.6)$$

where $\Gamma = kT/\Delta E - (kT/\Delta E - D_n/v_{exit}\ T_b)e^{-\Delta E/kT}$ is a factor involving the base bandgap grading ($\Gamma \approx 1$ for a non-graded base) and $\zeta = x/T_{eb}$ is a normalized position variable.

The first term in Eqn. 1.6 describes the depletion-layer capacitance, and is minimized by using high bias current densities $J_e = I_e = A_e$. The second term describes storage of mobile electron charge within the depletion layer, and is minimized by reducing $T_{eb}T_b$. This analysis shows that the depletion region thickness cannot be indefinitely extended to reduce base-emitter junction capacitance, as charge storage in the region also contributes to the transistor's forward delay. The $R_{ex}C_{cb}$ delay term in Eqn. 1.1 is thus a significant limitation when scaling for high f_τ. The relative sizes of the emitter and collector contacts in a well-designed submicron HBT allow R_c to be four to ten times smaller than R_{ex}, and R_cC_{cb} can be neglected in a first order analysis. To calculate R_{ex}, we must consider the geometry of the emitter epitaxial structure.

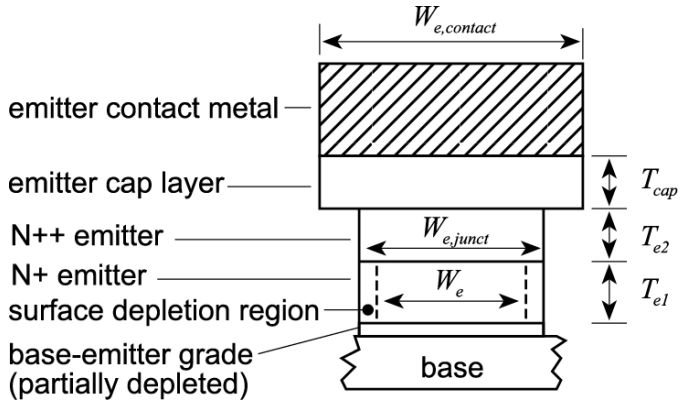


Figure 1.3 Cross-section of a base-emitter structure including epitaxial layers and emitter contact metal. For submicron emitters, the lateral depletion of the N+ emitter can comprise a significant portion of the emitter width.

The emitter layer structure shown in Figure 1.3 is composed of a heavily-doped narrow-bandgap contacting "cap" layer, an *N*++ heavily-doped wide-bandgap emitter layer, and a more lightly-doped (*N*+) emitter layer near the base interface to avoid dopant diffusion from the N++ layers into the emitter-base junction. If the heterojunction is properly graded to avoid conduction band barriers, the parasitic emitter resistance may be expressed as

$$R_{ex} = \frac{\rho_{c,e}}{L_e W_{e,contact}} + \frac{\rho_{cap} T_{cap}}{L_e W_{e,contact}} + \frac{\rho_{e2} T_{e2}}{L_e W_{e,\,junct}} + \frac{\rho_{e1} T_{e1}}{L_e W_e} \qquad (1.7)$$

where $\rho_{c,e}$ is the emitter specific ohmic contact resistivity, and ρ_{cap}, ρ_{e2}, and ρ_{e1} are the bulk resistivities of the cap, *N*++, and *N*+ emitter layers. For submicron emitters in a mesa HBT, the junction width $W_{e,junct}$ is significantly smaller than the contact width $W_{e,contact}$ due to lateral undercutting of the emitter material by the etch process used to form the emitter-base junction, and the electrically active junction width W_e can be

significantly smaller than $W_{e,junct}$ because of the surface (edge) depletion regions of width $\left(2\varepsilon\phi / qN_{e1}\right)^{1/2}$, where N_{e1} is the $N+$ layer doping and ϕ is the band bending due to pinning of the Fermi energy at the surface. For simplicity in the scaling analysis, we will approximate

$$R_{ex} \cong \rho_e / A_e \tag{1.8}$$

where ρ_e is a fitted parameter, approximately 50 Ω-μm^2 for submicron HBTs fabricated at UCSB using a graded InAlAs/InGaAs emitter-base structure [25] and 25 Ω-μm^2 for abrupt InP/InGaAs junctions.[26]

From these values of R_{ex} the $R_{ex}C_{cb}$ charging time can then be examined. Since $C_{cb} = \varepsilon A/T_c$,

$$R_{ex}C_{cb} = \left(\frac{\varepsilon\rho_c}{T_c}\right)\left(\frac{A_c}{A_e}\right). \tag{1.9}$$

This term can contribute a significant delay to f_τ. An f_τ of 295 GHz has been obtained in HBTs fabricated at UCSB using the substrate transfer process.[27] Although the substrate transfer process allows A_c/A_e to be small at 2.3:1, the $R_{ex}C_{cb}$ still constitutes 11% of the total $1/2\pi f_\tau$ forward delay. In mesa HBTs (Figure 1.1) A_c/A_e is often larger than 2.3:1 and hence, $R_{ex}C_{cb}$ contributes an even larger delay. Because $R_{ex}C_{cb} \propto 1/T_c$, thinning the collector to reduce τ_c also increases $R_{ex}C_{cb}$.

To increase HBT current gain cutoff frequencies, the base and collector layers must be thinned and the bias current density increased. Thinning the collector increases $R_{ex}C_{cb}$, imposing a limit to epitaxial scaling. Limits to bias current density

imposed by device reliability, and loss in breakdown voltage with reduced collector thickness, are two further potential limits to scaling. Finally, unless the device structure of Figure 1.1 is laterally scaled, vertical HBT scaling for increased f_τ will result in reduced power-gain cutoff frequencies f_{max}.

1.2.2 Factors determining f_{max}

In an HBT with base resistance R_{bb} and collector capacitance C_{cb}, the power gain cutoff frequency is approximately $f_{\max} \cong (f_\tau / 8\pi\tau_{cb})^{1/2}$. The base-collector junction is a distributed network, and the τ_{cb} term represents an effective, weighted time constant. The distributed network arises because the current distribution in the base-collector mesa is non-homogeneous, e.g. current density is greatest directly beneath the emitter. Because the base-collector junction parasitics are distributed, calculation of τ_{cb} is of complex. To simplify the analysis, f_{max} is first approximated as $f_{\max} \cong (f_\tau / 8\pi R_{bb} C_{cb})^{1/2}$, where $R_{bb}C_{cb}$ is the product of the base resistance and the full capacitance $C_{cb} = \varepsilon A/T_c$ of the base-collector junction.

The base resistance R_{bb} represents the sum of contact resistance $R_{b,cont}$, base-emitter gap resistance R_{gap}, and spreading resistance under the emitter R_{spread}. With base sheet resistance ρ_s, and specific contact resistance ρ_υ, we have

$$\begin{aligned} R_{bb} &= R_{b,cont} + R_{gap} + R_{spread} \\ R_{b,cont} &= \sqrt{\rho_s \rho_\upsilon} / 2L_e \\ R_{gap} &= \rho_s W_{cb} / 2L_e \\ R_{spread} &= \rho_s W_c / 12L_e \end{aligned} \qquad (1.10)$$

The base-collector time constant is then

$$R_{bb}C_{cb} = \left[\left(\sqrt{\rho_s \rho_\upsilon} + \rho_s W_{eb}\right)\left(\frac{\varepsilon}{2}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_c}{T_c}\right] + \left[\left(\frac{\rho_s \varepsilon}{12}\right)\left(\frac{L_c}{L_e}\right)\right]\left[\frac{W_c W_e}{T_c}\right] \tag{1.11}$$

Equation 1.11 shows the influence of device scaling on the time constant $R_{bb}C_{cb}$. Decreasing the base thickness to reduce τ_b increases the base sheet resistivity ρ_s, increasing $R_{bb}C_{cb}$. Decreasing the collector thickness T_c to reduce τ_c directly increases $R_{bb}C_{cb}$, as is shown explicitly in Eqn. 1.11.

Low $R_{bb}C_{cb}$, and consequently high f_{max} may be obtained by scaling the emitter and collector junction widths W_e and W_c to submicron dimensions. Reducing the emitter width W_e alone reduces towards zero the component of $R_{bb}C_{cb}$ associated with the base spreading resistance (the second term in Eqn. 1.11). In the mesa HBT (Figure 1.1), the minimum collector junction width W_c is set by the width of the base ohmic contacts which must be at least one contact transfer length ($L_{contact} = (\rho_\upsilon/\rho_s)^{1/2}$). As a result, the component of $R_{bb}C_{cb}$ associated with the base contact resistance (the first term in Eqn. 1.11) has a minimum value, independent of lithographic limits, and consequently, f_{max} does not increase rapidly with scaling. Given this minimum $R_{bb}C_{cb}$, attempts to obtain high f_τ by thinning the collector results in decreased f_{max}, frustrating efforts to improve HBT bandwidths.

If the parasitic portion of the collector-base junction could be eliminated, f_{max} would increase rapidly with scaling. The collector-base junction need only be present

where current flows, e.g. under the emitter. An example of one such effort is UCSB's substrate transferred HBT. Various research groups have also demonstrated removal of the parasitic base-collector junction by laterally etching the extrinsic region of the collector. In both methods, the goal is to form emitter and collector junctions of near equal width, hence $W_c = W_e$. With submicron scaling of the emitter and collector junction widths, the first term in Eqn. 1.11 dominates becomes scalable to W_e. By this approximate analysis, f_{max} then increases as the inverse square root of the minimum feature size.

1.3 Highly scaled III-V HBTs

To obtain simultaneously high values of f_τ and f_{max}, the emitter and collector widths must both be scaled. To date, several methods have been successfully applied to reduce or eliminate the parasitic collector-base capacitance and, thus, improve f_{max}. The transferred substrate process is an extremely aggressive method of reducing the parasitic collector-base junction capacitance, and the method requires substantial departures from the typical mesa HBT fabrication process. Alternative processes requiring less radical alterations have been also demonstrated. In AlGaAs/GaAs HBTs it has been demonstrated that deep proton implantation through the base layer and into the collector region can be used to reduce the extrinsic collector capacitance.[28] Wet chemical etchants can be used to remove the extrinsic collector junction by laterally undercutting beneath the base layer,[29] and the collector capacitance under the base contact pad can be reduced using dielectric spacer layers.[30] Alternatively, R_{bb} can be reduced by regrowing, prior to base contact

deposition, thick extrinsic P+ contact regions on the exposed base surface.[31,32] Low $R_{bb}C_{cbi}$ can also be obtained in the typical mesa structure by reducing the lateral width of the base ohmic contacts. InGaAs base layers grown by MBE can be produced with $> 10^{20}$ cm^{-3} doping. At such doping levels, the transfer length $L_{contact} = (\rho_c/\rho_s)^{1/2}$ can be greatly reduced as long as the correct (low ρ_c) base contact is used. The width of the base ohmic contacts can then be accordingly reduced to eliminate excess collector-base junction area. The transferred substrate HBT will be briefly discussed in the following subsection followed by a discussion on recent results of highly-scaled mesa HBTs.

1.3.1 Transferred-substrate HBTs

The transferred-substrate process is a means of realizing a highly scalable HBT. In scaling for high f_τ, limitations include high power and current density, demand for low emitter resistance, and the collapse of f_{max} due to extrinsic collector-base junction. The substrate transfer process allows the extrinsic collector-base junction to be reduced or eliminated by providing lithographic access to both the emitter and collector material. This access allows for narrow definition of both the emitter and collector stripes and the formation of an HBT structure similar to that shown in Figure 1.4. With the extrinsic collector-base capacitance greatly reduced, aggressive lithographic scaling without epitaxial scaling greatly increases f_{max} at constant f_τ. If high values of both f_τ and f_{max} are sought, simultaneous lithographic and epitaxial scaling is required. Further improvements in device bandwidth beyond what

is reported here would require operation at higher current densities and reduction of parasitic base and emitter resistances.

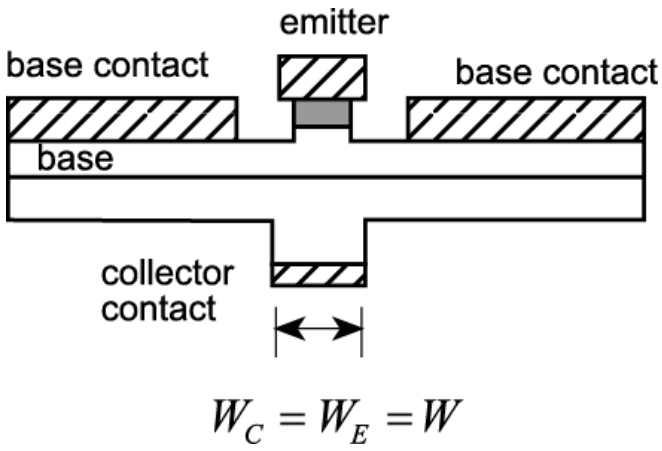


Figure 1.4 Cross-section of an HBT with the collector-base junction lying only under the emitter. Such a device structure can be formed using substrate transfer processes.

The transferred substrate epitaxial structure has been grown by MBE on semi-insulating InP substrates, and both single and double heterojunction transistors have been fabricated in the transferred-substrate technology. The single heterojunction transistors have an InAlAs/InGaAs emitter-base junction with an InGaAs collector region. The double heterojunction devices have an InP collector for increased breakdown, and an InP emitter may be used in place of the InAlAs ternary for improved heat flow from the emitter.[33] Chirped superlattice grades are used to smooth conduction band discontinuities at the base heterojunctions. The InGaAs base is typically 300 to 400 Å thick, has *2kT* bandgap grading, and is Be-doped at 5×10^{19} cm^{-3}. The collector thickness is typically 2000 to 3000 Å thick, and an N+ pulse-doped layer placed 400 Å from the base-collector metallurgical junction delays the

onset of base push-out at high collector current densities. High f_{max} devices are typically fabricated with Schottky collector contacts that provide zero collector series resistance.[34]

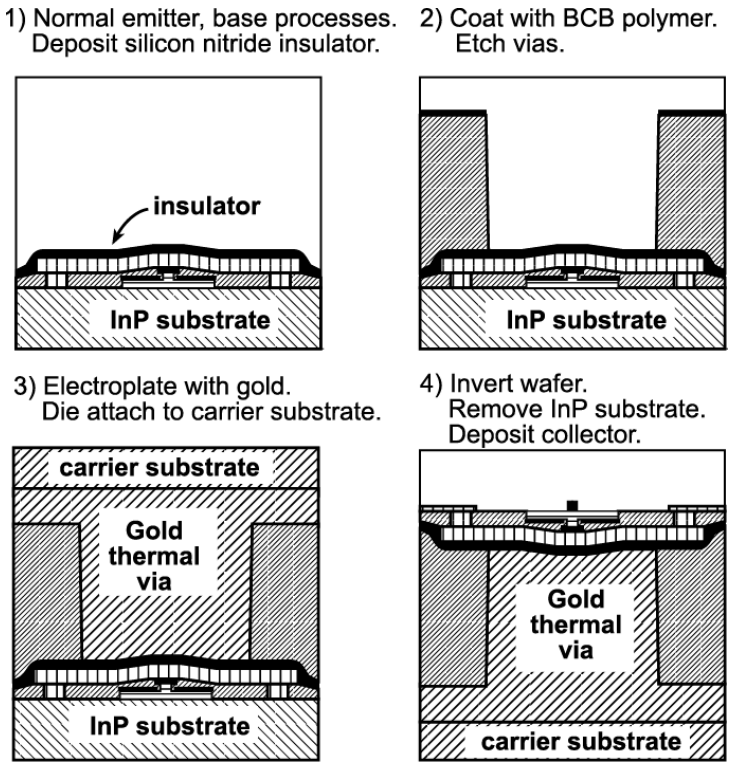


Figure 1.5 Transferred substrate HBT fabrication process flow.

Figure 1.5 shows the transferred substrate process flow. Standard fabrication processes[35] are used to define the emitter-base junction, the base mesa, polyimide planarization, and the emitter contacts. The substrate transfer process commences with the deposition of a 5 μm thickness Benzocyclobutene (BCB) transmission-line dielectric. Thermal and electrical vias are etched in the BCB, and electroplating is used to deposit metal vias and to form the wafer's ground plane. The wafer is then

solder-bonded to a GaAs or AlN carrier substrate. The InP substrate is removed in a selective HCl etch to expose the collector epitaxial layer, and collector contacts are patterned onto the exposed collector. Shown in Figure 1.6 is a detailed cross section of the completed transferred substrate device.

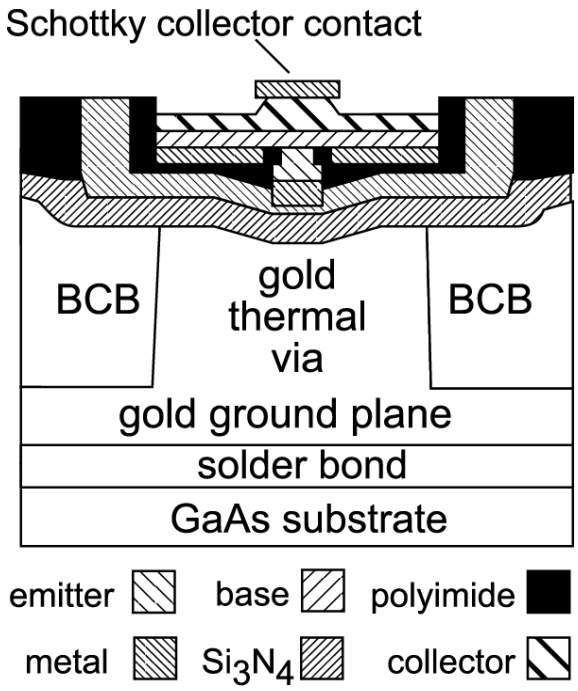


Figure 1.6 Schematic cross-section of a transferred substrate HBT.

For the emitter-base junction, deep submicron scaling requires tight control of lateral undercutting during the base contact recess etch. The undercut both narrows the emitter and defines the liftoff edge in self-aligned base contact deposition. For InAlAs emitters, the transferred substrate process uses a combination of dry and wet etch mechanisms. A CH_4/H_2/Ar reactive ion etch (RIE) is used to remove the N+ InGaAs emitter contact layer and to partially etch into the InAlAs emitter. A

HCl/HBr/acetic acid selective wet etch is then used to remove the InAlAs emitter and to etch partially into the emitter-base grade. The selective nature of this etch allows it to stop at a consistent depth in the InAlAs/InGaAs grade. A timed, nonselective citric acid-based wet etchant is then used to remove the remaining base-emitter grade. The etch is allowed to penetrate approximately 100 Å into the base layer to ensure that the contacts lay on base material. An all wet etch process is used for transferred substrate devices using an InP emitter. A selective H_2O_2/H_3PO_4 etchant is used to remove the N+ InGaAs emitter contact layer, and the etch stops at the InP emitter layer. A selective HCl/H_3PO_4 etch is then used to remove the emitter semiconductor, and this etch stops at the InGaAs base. For emitter etch processes, an undercut of ~0.1 μm is desirable to minimize base gap resistance between the emitter and the base metal, and the etch processes must be well controlled to maintain as little undercut as possible.

In defining the collector-base junction, the use of a Schottky-collector contact eliminates the need for an etch of similar precision as when an N+ ohmic collector contact layer is used. The collector junction is defined by the stripe width of the collector metal. After collector deposition, a self-aligned wet etch of ~1000 Å depth removes the collector junction sidewalls to eliminate fringing fields. This etch also reduces the collector junction width by ~2000 Å. The step, intended to reduce C_{cb}, is observed to provide a greater increase in f_{max} than would be expected from the physical reduction in collector junction width.

Extrapolated f_{max} up to 820 GHz and f_τ up to 300 GHz have been obtained with transferred-substrate HBTs.[36,37] Both of these results were obtained using single

heterojunction transistors with a wide-bandgap InAlAs emitter and InGaAs base and collector. The high f_{max} result was obtained using a 400 Å base layer and 3000 Å collector while the high f_τ result was achieved using a 300 Å base and 2000 Å collector structure. At the time of each publication, the results were the highest ever reported in a bipolar transistor technology in any material system.

A number of integrated circuit results have been reported in the transferred substrate process. Master-slave latches configured as 2:1 static frequency dividers were fabricated which correctly function at all frequencies in the 5-75 GHz range.[38] This static frequency divider was the fastest ever reported until that time. High-speed analog ICs accomplishments in the transferred substrate technology include 80 GHz distributed amplifiers,[39] 50 GHz broadband differential amplifiers,[40] and broadband Darlington and f_τ-doubler resistive feedback amplifiers.[41,42] Tuned mm-wave amplifiers have been demonstrated using transferred substrate HBTs, including a 75 GHz amplifier and 180 GHz tuned amplifier.[43,44]

The circuits described above contain as few as two and as many as seventy transistors, as well as passive components and interconnects. Larger digital and mixed-signal ICs have been fabricated in the transferred substrate process. For instance, Δ-Σ modulators composed of 150 HBTs and operating at up to 18 GHz clock rate have been demonstrated,[45] and larger digital circuits (~250 HBTs) were developed to include sum and carry generation circuits for pipeline adder-accumulators.[46]

Despite record results for discrete transferred-substrate HBTs and the success of circuits constructed using the device technology; there have been only a few duplications of the transferred substrate work outside of UCSB. InP DHBTs have been produced at the Ferdinand-Braun-Institut für Höchstfrequenztechnik.[47,48] Along with improvements to the epitaxial stack (InP emitter and collector), changes were made to improve the thermal characteristics of the device after the transferred substrate process. The UCSB transferred substrate process leaves the remaining HBT epi "floating" in low thermoconductivity dielectric; allowing heat leave the device mostly through the emitter and collector contacts. As current density increases, the device will heat. This heat will eventually lead to device failure if the current density is taken too high. The effort at Ferdinand-Braun attempts to resolve the heating issue by sinking heat out of the emitter, through a thick lateral metal layer, and into a high thermoconductivity AlN substrate. This device has produced an f_τ of 410 GHz and f_{max} of 480 GHz at current density J_c = 6.5 mA/μm^2 for a 0.8 × 5 μm^2 emitter with 300 Å carbon-doped base and 1250 Å total collector thickness.

A transferred substrate HBT demonstration at Northrop Grumman Corporation also attempts to resolve the heating issue by transferring the device to a higher thermal conductivity SiC substrate after patterning the narrow backside collector.[49] The Northrop Grumman device produces an f_τ of 397 GHz and f_{max} > 400 GHz at current density J_c = 10.5 mA/μm^2 for a 0.2 × 3 μm^2 emitter with 280 Å beryllium-doped base and 1500 Å total collector thickness.

The transferred substrate effort at UCSB has had its greatest affect by altering the perception of scaling potential in III-V HBTs. New focus has since been given to the original mesa HBT structure utilizing very aggressive scaling in the device layout and epitaxial structure to minimize device parasitics. This effort is responsible for a new generation of highly-scaled III-V mesa HBTs.

1.3.2 Trends in highly scaled mesa HBTs

Aggressive scaling in III-V HBTs using the original mesa structure has lead to new record results. Ida, *et al.* reported an InP/InGaAs mesa DHBT in late 2002 with aggressive epitaxial and layout scaling.[50] The emitter dimension was $0.8 \times 3\ \mu m^2$ and the paper compares devices with 20 and 30 nm thick base layers and 150 nm collectors. The device incorporated heavy carbon base doping at $6 \times 10^{19}\ cm^{-3}$ for lattice-matched InGaAs and compositional grading of the GaAs in the InGaAs base. The GaAs mole fraction in the 30 nm base device was linearly increased from 0.47 (lattice matched to InP) to 0.56 towards the base-emitter heterojunction. In the 20 nm base device a larger mole fraction was used to achieve a higher base doping concentration. The composition was 0.56 at the base-collector interface and increased to 0.60 towards the base-emitter junction. The device also incorporated an isolated base pad layout.[51] The base pad isolation structure was used to eliminate the extrinsic collector capacitance at the large area where the base is connected to the pad structure. The 20 nm device achieved a record 351 GHz f_τ and 288 GHz f_{max} at a current density of $J_c = 667\ kA/cm^2$ while simultaneously high values of 329 GHz was obtained for both f_τ and f_{max} in the 30 nm device.

Dahlström, *et al.* later reported an InP/InGaAs/InP mesa DHBT with 282 GHz f_τ and 400 GHz f_{max} using a 25 nm doping-graded InGaAs base and 214 nm collector depletion layer.[52] The high f_{max} result is attributed to the minimization of base resistance R_{bb} and collector-base capacitance C_{cb}. The R_{bb} parasitic is composed of base current spreading under the emitter stripe, the emitter-base gap resistance, and the contact resistance of the base metal. The first two components are reduced by high base doping to obtain low base resistance, narrow emitter junctions, and minimal spacing between the emitter junction and base contact. The third component—the base contact resistance—is minimized by very high base doping and by the Pd/Ti/Pt/Au ohmic base metal.[53] The base doping in this device is graded from a degenerate 8×10^{19} cm^{-3} at the emitter interface to 5×10^{19} cm^{-3} at the collector side producing a 49 meV potential drop and a 16.5 kV/cm drift field in the base assuming Fermi-Dirac statistics and accounting for bandgap narrowing. Assuming $D_{n,b}$ = 43 cm^2/sec average diffusivity and 4×10^7 cm/s exit velocity into the collector, the calculated base transit time is reduced from 0.18 to 0.10 ps contributing to a lower f_τ. The emitter metal for this device is 0.7 μm wide with a junction undercut by 80 nm on each side producing an emitter junction width of 0.54 μm. The base metal is self-aligned to the emitter metal and extends 1 μm on each side of the 8 μm emitter length producing a total base-collector junction width of 2.7 μm. The aggressive lateral scaling and the high base doping allow for an InP mesa HBT with high f_τ and record f_{max}.

The same team later produced a device with the same epitaxial structure, layer thicknesses, and device dimensions but improved RF performance.[54] This device demonstrated a 370 GHz f_τ and 459 GHz f_{max} by decreasing base and emitter contact resistances, increasing current density through the device, and undercutting the extrinsic collector region under the base by 200 nm to reduce C_{cb}. The f_τ demonstrated in this device was the highest reported for a InP-based mesa HBT at the time. These results were some of the highest simultaneous numbers ever reported at the time, and the C_{cb}/I_c ratio = 0.28 ps/V at V_{cb} = 0.5 V was the lowest ever reported for an InP mesa DHBT.

The Ida, *et al.* group from above also reported simultaneously high f_τ and f_{max} results for an InP/InGaAs mesa DHBT in late 2003.[55] The paper presented at the GaAs IC Symposium reported the first sub-4 ps delay in an ECL circuit. As an addendum to the circuit results which used non self-aligned base to emitter electrodes, the group fabricated devices with self-aligned base contacts to demonstrate the capability of the device technology. The circuit results utilized the earlier reported device with the 30 nm compositionally graded base, 150 nm collector, and 0.8 × 3 μm^2 emitter which produce simultaneous f_τ and f_{max} over 300 GHz. The group reports that the dominant part of their non self-aligned base resistance is access resistance between the emitter mesa and base electrode. In their lateral scaling experiment, they used the same epitaxial layer structure as for the non self-aligned device and fabricated devices with 0.6, 0.8, and 1.0 μm widths and 5 μm lengths. They found that f_{max} increases with decreased emitter width which they attribute to reduced intrinsic base resistance

and reduced intrinsic base-collector capacitance. The 0.6 × 5 μm^2 self-aligned device achieved a maximum simultaneous f_τ and f_{max} of 347 and 492 GHz, respectively.

In 2006, Lind, *et al.* reported a record InP/InGaAs/InP DHBT with 650 GHz f_{max} and simultaneous 420 GHz f_τ.[56] In this work, the emitter width was scaled to 250 nm and substantial improvements had been made to the base and emitter Ohmic contacts. The HBTs were formed using an all wet etch triple mesa fabrication process where undercut determined the 250 nm emitter width. The InGaAs base is 30 nm thick and carbon doped from 7 to 4 × 10^{19} cm^{-3} to create a 50 meV conduction band grade. The total collector thickness including base-collector grade is 150 nm. TLM measurements showed a base contact resistance ρ_c < 5 Ω·μm^2 and base sheet resistance ρ_s = 630 Ω. The emitter ρ_c = 5.3 Ω·μm^2 was extracted from RF-parameter fitting. These contact resistance numbers represent a 50% improvement compared to previous work from the same group. The 0.25 × 3.1 μm^2 emitter area device demonstrated a 650 GHz f_{max} and 420 GHz f_τ at I_C = 9 mA and V_{ce} = 1.58 V.

Using epitaxial material and fabrication process identical to Lind, Griffith *et al.* reported a record InP/InGaAs/InP DHBT with 755 GHz f_{max} and simultaneous 416 GHz f_τ in 2007.[57] In this work, the base contact resistance ρ_c = 6.3 Ω·μm^2, base sheet resistance was measured slightly lower at ρ_s = 603 Ω, and the emitter ρ_c = 5.1 Ω·μm^2. Despite the similarities, Griffith's 0.30 × 2.0 μm^2 emitter area device was able to demonstrate a record 755 GHz f_{max} and 416 GHz f_τ at I_C = 6.98 mA and V_{ce} = 1.74 V.

1.4 Highly scaled SiGe HBTs

SiGe HBTs emerged in the early 2000s as strong RF performance contenders to InP HBTs. In addition to the newly improved performance, SiGe HBTs had the additional promise of process maturity, higher levels of integration and yield, and the ability to monolithically integrated CMOS devices into the SiGe fabrication process (BiCMOS).

In 2002, Hitachi reported an NPN SiGe HBT with heavily-doped and narrow intrinsic base layer and emitter area of 0.15 × 1.0 μm^2 demonstrating 227 GHz f_{max} and 201 GHz f_τ at I_C = 1.2 mA and V_{ce} = 1.5 V.[58] The record RF performance is attributed to optimization of the thickness and profile of the carbon doping in the SiGe base layer to reduce both intrinsic base resistance and contact resistance to the external base elements. The work also indicates emitter width dependence where narrow emitter (and proportionally narrow base) widths of 0.15 μm demonstrate higher peak f_{max} compared to emitter widths up to 0.3 μm.

IHP Microelectronics reported an NPN SiGe:C HBT in 2003 with elevated extrinsic base contacts rather than the more conventional implanted extrinsic base. Peak f_{max} was observed to increase from 186 GHz to 225 GHz when elevated base contacts were used in lieu of the implanted extrinsic base. The improvement is attributed to reduced R_{bb} and C_{cb} when using the elevated base structure. A further reduction was obtained in base resistance by shrinking the drawn emitter width from 0.21 μm to 0.175 μm; increasing the peak f_{max} to 243 GHz. The 0.175 × 0.84 μm^2 emitter area HBT with selectively grown elevated extrinsic base has 243 GHz f_{max} and

190 GHz f_τ at I_C = 1.5 mA and V_{ce} = 1.5 V.[59] The same group later reported a SiGe HBT with aggressive vertical scaling and a selectively undercut collector to reduce base-collector capacitance. The device improvements produce a 0.175 × 0.84 μm^2 NPN HBT with 300 GHz f_τ and 250 GHz f_{max} at I_C = 1.5 mA and V_{ce} = 1.5 V where the total C_{cb} at V_{cb} = 0 V is reduced from 3fF to 2.5fF when comparing a conventionally fabricated device to the device with undercut collector.[60]

Infineon Technologies also reported SiGe HBTs with impressive results using a thinned base region with increased doping levels; allowing for reduced base transit time without increasing the intrinsic base sheet resistance. The Infineon HBTs also utilize a mono-crystalline emitter contact for reduced total emitter resistance.[61] The 0.14 × 2.6 μm^2 NPN HBT demonstrates a 300 GHz f_{max} and simultaneous 215 GHz f_τ at I_C = 3.5 mA and V_{cb} = 1 V.[62] A higher maximum f_τ of 225 GHz is also reported for V_{cb} = 0 V, but f_{max} drops to ~260 GHz at this bias condition.

In 2002, IBM reported SiGe HBTs with 70% improvement in f_τ and f_{max} compared with their 120 GHz f_τ production device.[63] To achieve simultaneously high f_τ and f_{max}, the NPN vertical and lateral dimensions were reduced compared to the 120 GHz generation. The emitter n-epitaxial layer thickness, collector, and base doping concentrations were scaled to achieve a target f_τ of 200 GHz. A self-aligned, raised extrinsic base is employed, the emitter dimension is narrowed, and the emitter to extrinsic base spacer is reduced to lower the total base resistance R_{bb}. The resulting device has a pinched base resistance of 2.5 kΩ/sq, a peak dc current gain of 400, BV_{CEO} of 1.7 V, and BV_{CBO} of 5.5 V. For a 0.12 × 2.5 μm^2 emitter area device at V_{cb}

of 1 V, f_τ is over 200 GHz for a current density range of 8.3-16.5 mA/ μm^2, peaking at 207 GHz; the f_{max} peaks at 285 GHz. In 2004, further improvement in f_τ was achieved by vertical profile scaling [3], and reduction of base resistance was achieved by reducing the polysilicon parasitic resistance component of the raised extrinsic base to obtain a 0.12 × 2.5 μm^2 emitter area device with 350 GHz f_{max} and 300 GHz f_τ at I_C = 5.7 mA and V_{cb} = 0.5 V.[64]

[1] K. Shinohara, Y. Yamashita, A. Endoh, K. Hikosaka, T. Matsui, T. Mimura, and S. Hiyamizu, "Ultrahigh-speed pseudomorphic InGaAs/InAlAs HEMTs with 400-GHz cutoff frequency," *IEEE Electron Device Letters*, vol. 22, no. 11, November 2001, pp 507-9.

[2] P.M Smith, S.-M.J Liu, M.-Y Kao, P. Ho, S.C. Wang, K.H.G. Duh, S.T. Fu, P.C. Chao, "W-band high efficiency InP-based power HEMT with 600 GHz $f_{max,}$" *IEEE Microwave and Guided Wave Letters*, vol.5, no.7, July 1995, pp.230-2.

[3] J-S. Rieh, B. Jagannathan, H. Chen, KT. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S-J. Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker, K. Vaed, R. Volant, D. Ahlgren, G. Freeman, K. Stein K, S. Subbanna, "SiGe HBTs with cut-off frequency of 350 GHz," *International Electron Devices Meeting. Technical Digest.* IEEE. 2002, pp.771-4.

[4] J. Bardeen and W. H. Brattain, "The transistor, a semi-conductor triode," *Phys. Rev.* **74**, 230 (1948).

[5] W. H. Brattain and J. Bardeen, "Nature of the forward current in germanium point contacts," *Phys. Rev.* **74**, 231 (1948).

[6] W. Shockley, "The theory of p-n junctions in semiconductors and p-n junction transistors," *Bell System Technology Journal* **28**, 435 (1949).

[7] W. Shockley, "Circuit element utilizing semiconductive materials," U.S. Patent No. 2 569 347 September 25, 1951.

[8] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proc. IRE* **45**, 1535 (1957).

[9] D. A. Jenny, "The status of transistor research in compound semiconductors," *Proc. Inst. Radio Engrs.* **46**, 959 (1958).

[10] R. Ruth, J. C. Marinace and W. C. Dunlap, Jr., "Vapor deposited single-crystal germanium," *J. Appl. Phys.* **31**, 995 (1960).

[11] R. L. Anderson, "Experiments on Ge-GaAs heterojunction," *Solid-State Electron.* **5**, 341 (1962).

[12] D. K. Jadus and D. L. Feucht, "The realization of a wide band gap emitter transistor," *IEEE Trans. Electron Devices* **16**, 102 (1969).

[13] W. P. Dumke, J. M. Woodall, and V. L. Rideout, "GaAs-GaAlAs heterojunction transistor for high-frequency operation," *Solid-State Electron.* **15**, 12 (1972).

[14] S. Yamahata, K. Kurishima, H. Ito, Y. Matsuka, "Over-22-GHz-fT-and-fmax InP/InGaAs double-heterojunction bipolar transistors with a new hexagonal-shaped emitter," *IEEE GaAs IC Symposium Technical Journal*, 1995, pp. 163-6.

[15] M.J.W. Rodwell, M. Urteaga, Y. Betser, T. Mathew, S. Krishnan, D. Scott, S. Jaganathan, D. Mensa, R. Pullela, Q. Lee, B. Agarwal, U. Bhattacharya, S. Long, "Scaling of InGaAs/InAlAs HBTs for high speed mixed-signal and mm-Wave ICs," *International Journal of High Speed Electronics and Systems*, vol. 11, no. 1, World Scientific Publishing Company, 2001.

[16] M. Urteaga, S. Krishnan, D. Scott, Y. Wei, M. Dahlstrom, S. Lee, M.J.W. Rodwell, "Submicron InP-based HBTs for ultra-high frequency amplifiers," *International Journal of High Speed Electronics and Systems*, vol. 13, no. 2, World Scientific Publishing Company, 2003.

[17] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid State Electronics*, vol. 28, 1985, pp. 1101-3.

[18] B. G. Streetman, *Solid State Electronic Devices*, third ed., Prentice-Hall, 1990.

[19] S. Laux, W. Lee, "Collector signal delay in the presence of velocity overshoot," IEEE Electron Device Letters, vol. 11, no. 4, 1990, pp. 174-6.

[20] T. Ishibashi, "Influence of electron velocity overshoot on collector transit times of HBTs," IEEE Transactions on Electron Devices, vol. 37, no. 9, September 1990, pp 2103-5

[21] T. Ishibashi, "Nonequilibrium electron transport in HBTs," IEEE Transactions on Electron Devices, vol. 48, no. 11, November 2001, pp. 2595-605.

[22] M. Littlejohn, K.W. Kim, H. Tian, "High-field transport in InGaAs and related heterostructures," in *Properties of lattice-matched and strained Indium Gallium Arsenide*, P. Bhattacharya, ed., INSPEC, 1993, London.

[23] E. P. O'Reilly, "Band structure of InP: Overview," in *Properties of Indium Phosphide*, INSPEC, 1991, London.

[24] C.T. Kirk, "A theory of transistor cutoff frequency (f_τ) fall-off at high current density," IEEE *Transactions on Electron Devices*, ED-9, 1962, p. 164.

[25] D. Mensa, *Improved current-gain cutoff frequency and high gain-bandwidth amplifiers in transferred substrate HBT technology*, University of California, Santa Barbara Ph.D. Thesis, September, 1999.

[26] M. Dahlström, *Ultra high speed InP heterojunction bipolar transistors*, Royal Institute of Technology, Stockholm Ph.D. Thesis, 2003.

[27] M. Urteaga, D. Scott, M. Dahlström, Y. Betser, S. Lee, S. Krishnan, T. Mathew. S. Jaganathan. Y. Wei, M.J.W. Rodwell, "Ultra High Speed Heterojunction Bipolar Transistor Technology," *2001 GOMAC Conference Technical Digest*, March 2001.

[28] M.-C. Ho, R.A. Johnson, W.J. Ho, M.F. Chang, P.M. Asbeck, "High-performance low-base-collector capacitance AlGaAs/GaAs heterojunction bipolar transistors fabricated by deep ion implantation," *IEEE Electron Device Letters*, vol. 16, no. 11, November 1995, pp. 512-4.

[29] W. Liu, D. Hill, H.F. Chau, J. Sweder, T. Nagle and J. Delany, "Laterally etched undercut (LEU) technique to reduce base-collector capacitance in heterojunction bipolar transistors," *Technical Digest , IEEE GaAs IC Symposium*, 1995, pp. 167-170.

[30] T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, K. Mochizuki, T. Nakamura, "Small-scaled InGaP/GaAs HBTs with WSi/Ti base electrode and buried SiO_2," *IEEE Transactions on Electron Devices*, vol.45, no.11, November 1998, pp.2276-82.

[31] H. Shimawaki, Y. Amamiya, N. Furuhata, K. Honjo, "High f_{max} AlGaAs/InGaAs and AlGaAs/GaAs HBT's with p+/p regrown base contacts," *IEEE Transactions on Electron Devices*, vol. 42, no. 10, October 1995, pp. 1735-44.

[32] Y. Matsuoka, S. Yamahata, K. kurishima and H. Ito, "Ultrahigh-speed InP/InGaAs double-heterostructure bipolar transistors and analysis of their operation," *Japanese Journal of Applied Physics*, vol. 35, 1996, pp.5646-54.

[33] I. Harrison, M. Dahlström, S. Krishnan, Z. Griffith, Y.M. Kim, M.J.W. Rodwell, "Thermal limitations of InP HBTs in 80 and 160Gbit integrated circuits," *Conference Proceedings, IEEE International Conference on Indium Phosphide and Related Materials*, 2003, pp.160-3.

[34] R. P. Smith, S.T. Allen, M. Reddy, S.C. Martin, J. Liu, R. E. Muller, M.J.W. Rodwell, "0.1 μm Schottky-collector AlAs/GaAs resonant tunneling diodes," *IEEE Electron Device Letters*, vol. 15, no. 8, August 1994, pp. 295-7.

[35] W. E. Stanchina, R.H. Walden, M. Hafizi, H.-C. Sun, T. Liu, C. Raghavan, K.E. Elliott, M. Kardos, A.E. Schmitz, Y.K. Brown, M.E. Montes, M. Yung, "An InP-based HBT fab for high-speed digital, analog, mixed-signal, and optoelectronic ICs, " *Technical Digest, IEEE GaAs IC Symposium*, 1995, pp. 31-4.

[36] Q. Lee, S. C. Martin, D. Mensa, R.P. Smith, J. Guthrie, and M.J.W. Rodwell, "Submicron transferred-substrate heterojunction bipolar transistors," *IEEE Electron Device Letters*, vol. 20, no. 8, August 1999, pp. 396-8.

[37] Y. Betser, D. Scott, D. Mensa, S. Jaganathan. T. Mathew and Mark Rodwell, "InAIAs/InGaAs HBTs with simultaneously high values of f_τ and f_{max} for mixed analog/digital applications," *IEEE Electron Device Letters*, vol. 22, no. 2, February 2001, pp. 56-8.

[38] T. Mathew, H.J. Kim, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M.J.W. Rodwell, S. Long, "75 GHz ECL Static Frequency Divider Using InAIAs/InGaAs HBTs," *IEE Electronic Letters*, vol. 37, no. 11, May 2001, pp. 667-8.

[39] S. Krishnan, S. Jaganathan, T. Mathew, Y. Wei, M. J. W. Rodwell, "Broadband HBT amplifiers," *2000 IEEE Cornell Conf. High Speed Electronics.* Ithaca, NY.

[40] B. Agarwal, Q. Lee, R. Pullela, D. Mensa, J. Guthrie, and M. J.W. Rodwell, "A transferred-substrate HBT wideband differential amplifier to 50 GHz," *IEEE Microwave Guided Wave Lett*., vol. 8, July 1998, pp. 263–265.

[41] D. Mensa, R. Pullela, Q. Lee, B. Agarwal, J. Guthrie, S. Jaganathan, M. J.W. Rodwell, "Baseband amplifiers in the transferred-substrate HBT technology," *Technical Digest, IEEE GaAs IC Symposium*, 1998, pp. 33-6.

[42] S. Krishnan, D. Mensa, J. Guthrie, S. Jaganathan, T. Mathew, R. Girish, Y. Wei and M.J.W. Rodwell, "Broadband lumped HBT amplifiers," *IEE Electronics Letters*, vol. 36, no. 5, March 2000, pp.466-7.

[43] J.R. Guthrie, M. Urteaga, D. Scott, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan, Y. Betser and M.J.W. Rodwell, "HBT MMIC 75GHz Power Amplifiers," *Conference Proceedings, IEEE International Conference on Indium Phosphide and Related Materials*, 2000, pp.246-9.

[44] M. Urteaga, D. Scott, T. Mathew, S. Krishnan, Y. Wei and M.J.W. Rodwell, "185 GHz Monolithic amplifier in InGaAs/InA1As transferred-substrate HBT technology," *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, 2001, pp. 1713-1716.

[45] S. Jaganathan, D. Mensa, T. Mathew, Y. Betser, S. Krishnan. Y. Wei. D. Scott, M. Urteaga, M. Rodwell, "A 18 GHz continuous time $\sum$-Δ modulator implemented in InP transferred substrate HBT technology," *Technical Digest, IEEE GaAs IC Symposium*, 2000, pp. 251-4.

[46] T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M.J.W. Rodwell, S. Long, "2 Bit Adder: Carry and Sum Logic Circuits at 19 Ghz Clock Frequency in InA1As/InGaAs HBT Technology," *IEE Electronics Letters*, vol. 37, no. 19, September 2001, pp. 1156-7.

[47] Kraemer, T.; Lenk, F.; Maassdorf, A.; Wuerfl, H.J.; Traenkle, G., "High yield transferred substrate InP DHBT," *Indium Phosphide & Related Materials, 2007. IPRM '07. IEEE 19th International Conference on*, vol., no., pp.407-408, 14-18 May 2007.

[48] Kraemer, T.; Rudolph, M.; Schmueckle, F.J.; Wuerfl, J.; Traenkle, G., "InP DHBT process in transferred-substrate technology with f_τ and f_{max} over 400 GHz," *Electron Devices, IEEE Transactions on*, vol.56, no.9, pp.1897-1903, Sept. 2009.

[49] Scott, D.W.; Monier, C.; Wang, S.; Radisic, V.; Phuong Nguyen; Cavus, A.; Deal, W.R.; Gutierrez-Aitken, A., "InP HBT transferred to higher thermal conductivity substrate," *IEEE Electron Device Letters*, vol. 33, no. 4, 2012, pp. 507-509.

[50] M. Ida, K. Kurishima, N. Wantannabe, "Over 300 GHz f_τ and f_{max} double heterojunction bipolar transistors with a thin pseudomorphic base," *IEEE Electron Device Letters*, vol. 23, no. 12, December 2002, pp. 694-6.

[51] M. Ida, S. Yamahata, H. Nakajima, N. Wantannabe, "High-performance small InP/InGaAs HBTs with reduced parasitic base-collector capacitance fabricated using novel base-metal design," *Proceedings of the International Symposium on Compound Semiconductors*, 1999, pp. 293-6.

[52] M. Dahlstrom, X.M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y.M. Kim, Y. Wu, J.M. Fastenau, W.K. Liu, M.J.W. Rodwell, "Wideband DHBTs using a graded carbon-doped InGaAs base," *IEEE Electron Device Letters*, vol. 24, no. 7, July 2003, pp. 433-5.

[53] E.F. Chor, R.J. Malik, R.A. Hamm, R. Ryan, "Metallurgical stability of ohmic contacts on thin base InP/InGaAs/ InP HBTs," *IEEE Electron Device Letters*, vol. 17, February 1996, pp. 62-4.

[54] Z. Griffith, M. Dahlstrom, M. Urteaga, M.J.W. Rodwell, X.M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, W.K. Liu, "InGaAs-InP mesa DHBTs with simultaneously high f_τ and f_{max} and low C_{cb}/I_c ratio," *IEEE Electron Device Letters*, vol. 25, no. 5, May 2004, pp. 250-3.

[55] M. Ida, K. Kurishima, K. Ishii, N. Wantannabe, "High-speed InP/InGaAs DHBTs with a thin pseudomorphic base," *IEEE GaAs IC Symposium Technical Digest*, 2003, pp. 211-4.

[56] Lind, E.; Griffith, Z.; Rodwell, M.J.W.; Xiao-Ming Fang; Loubychev, D.; Yu Wu; Fastenau, J.M.; Liu, A.W.K. , "250 nm InGaAs/InP DHBTs w/650 GHz f_{max} and 420 GHz f_τ, operating above 30 mW/μm^2," *Device Research Conference Digest*, 64th, June 2006, pp. 26-28.

[57] Griffith, Z.; Lind, E.; Rodwell, M.J.W.; Xiao-Ming Fang; Loubychev, D.; Ying Wu; Fastenau, J.M.; Liu, A.W.K., "Sub-300 nm InGaAs/InP Type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz f_{max} and 416 GHz f_T," *IEEE 19th International Conference on Indium Phosphide & Related Materials Technical Digest*, 14-18 May 2007, pp.403-406.

[58] T. Hashimoto, Y. Nonaka, T. Tominari, H. Fujiwara, K. Tokunaga, M. Arai, S. Wada, T. Udo, M. Seto, M. Miura, H. Shimamoto, K. Washio, H. Tomioka, "Direction to improve SiGe BiCMOS technology featuring 200-GHz SiGe HBT and 80-nm gate CMOS," *IEDM Technical Digest*, 2003, pp. 129-132.

[59] H. Rücker, B. Heinemann, R. Barth, D. Bolze, J. Drews, U. Haak, W. Höppner, D. Knoll, K. Köpke, S. Marschmeyer, H.H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, H.E. Wulf, Y. Yamamoto, "SiGe:C BiCMOS technology with 3.6 ps gate delay," *IEDM Technical Digest*, 2003, pp. 121-124.

[60] B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, T. Grabolla, U. Haak, W. Höppner, D.K. Köpke, B. Kuck, R. Kurps, S. Marschmeyer, H.H. Richter, H. Rücker, P. Schley, D. Schmidt, W. Winkler, D.Wolansky, H.E. Wulf, Y. Yamamoto, "A low-parasitic collector construction for high-speed SiGe:C HBTs," *IEDM Technical Digest*, 2004, pp. 251-254.

[61] T.F. Meister, H. Schifer, K. Aufinger, R. Stengl, S. Boguth, R. Schreiter, M. Rest, H. Knapp, M. Wurzer, A. Mitchell, T. Bottner, J. Bock, "SiGe bipolar technology with 3.9 ps gate delay," *IEEE Bipolar BiCMOS Circuits and Technology Meeting Technical Digest*, 2003, pp. 103-106.

[62] J. Böck, H. Schäfer, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, T. Böttner, R. Stengl, W. Perndl, and T. F. Meister, "3.3 ps SiGe bipolar technology," *IEDM Technical Digest*, 2004, pp. 255-258.

[63] B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. R. Greenberg, R. Groves, S. J. Jeng, J. Johnson, E. Mengistu, K. T. Schonenberg, C. M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{max} and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Letters*, vol. 23, no. 5, May 2002, pp. 258-260.

[64] M. Khater, J.S. Rieh, T. Adam, A. Chinthakindi, J. Johnson, R. Krishnasamy, M. Meghelli, F. Pagette, D. Sanderson, C. Schnabel, K. T. Schonenberg, P. Smith, K. Stein, A. Strieker, S.J. Jeng, D. Ahlgren, G. Freeman, "SiGe HBT technology with f_{max} / f_T = 350/300 GHz and gate delay below 3.3 ps," *IEDM Technical Digest*, 2004, pp. 247-250.

Chapter 2

MBE Growth of InP HBTs

2.1 Introduction to HBT Growth

The material growth for HBTs and the regrown emitter HBT work was performed in Varian Gen II MBE systems at UCSB. The MBE systems are typically used for the growth of optoelectronic devices, such as surface and vertical cavity lasers and detectors. In recent years, the growth of electron devices, such as HEMTs and HBTs, has become more common in the epitaxial systems. Two systems, referred to as System A and System B, were used for this work. Both systems contain the group III elemental solid sources gallium, aluminum, and indium. Valved cracker sources provide the group V elements in each system. System A has an arsenic source installed, and System B has arsenic, phosphorous, and antimony sources available. Both systems have beryllium and carbon as p-type dopant sources, and silicon is available as an n-type dopant.

The Gen II MBE systems are designed to accommodate a single 3-inch, round substrate. However, material growth at UCSB is typically performed on full 2-inch substrates, quarters of 2-inch substrates, or even smaller samples. Molybdenum face-

plates and silicon backing wafer mounting blocks are available and typically used to convert the 3-inch growth stage for full 2-inch wafers and quarters of 2-inch wafers. Indium bonding may also be used to attach smaller samples or quarter wafers to solid molybdenum blocks for growth. Indium bonded samples allow multiple small and non-standard shaped samples to be mounted for growth. The indium mounting technique also provides strong, uniform thermal contact between the growth sample and the mounting block. The mounting, however, requires additional effort, it may be difficult to remove the indium from the sample backside, and there is potential for contamination or oxidation buildup as the sample is being handled and heated during the mounting process. The use of molybdenum adapter plates and silicon backing wafers is therefore generally preferred over indium mounting.

HBT growths, emitter regrowths, and the growth of base-collector templates are generally performed on full 2-inch Fe-doped semi-insulating InP substrates using the molybdenum adapter plates and backing wafer mountings. Epi-ready substrates were purchased from Sumitomo Electric Semiconductor Materials, Inc. and Wafer Technology, Ltd. Both vendors provide substrates that are identical in specification, and no significant difference is observed in the growth conditions or epitaxial quality when switching between the substrate vendors.

The epitaxial growth rates and ternary compositions used during this work were determined using either reflected high energy electron diffraction (RHEED) oscillations or beam equivalent flux. When using RHEED calibrations, the binary growth rates for InAs on InAs, GaAs on GaAs, and for AlAs on GaAs were

determined on each growth day. The growth rate at a fixed substrate temperature is determined for at least three temperatures for the indium, aluminum, and gallium cells. The binary growth rates were then used to calculate the growth rates and cell temperatures required to obtain ternary InAlAs and InGaAs material lattice matched to the InP substrate. Source temperatures are typically chosen to maintain a growth rate of 1μm/hour. Calibration by RHEED on each growth day is a very manual and time-consuming process. Dedicated RHEED blocks (samples that are left in vacuum and used especially for RHEED calibrations) must be maintained for the InAs and GaAs/AlAs measurements, time is often required to obtain and potentially develop the RHEED signal on each growth day, and the quality of the RHEED signal often requires the grower to make subjective interpretations of the oscillation patterns.

Calibration by beam equivalent flux measurements may be done more quickly and with greater convenience. Beam flux measurements are obtained by exposing a bare ion gauge to the flux of a group III or group V source at varying cell temperatures. The bare ion gauge is located inside the vacuum of the growth chamber on the back side of the growth substrate heater. It may be utilized when the substrate is in the load position (substrate facing away from the sources) so deposition of material does not occur on the wafer or bare substrate heater. At the beginning of a growth campaign, it may be required to initially calibrate the binary growth rates by RHEED. These cell temperature versus growth rate calibrations can then be translated to cell temperature versus beam flux, and RHEED calibration is no longer necessary after this point. This is because beam flux correlates well with the amount of source

material arriving at the substrate's position. As long as the beam flux can be maintained (by altering the cell temperatures on a daily basis), the growth rates determined by RHEED are presumed to be remain constant and RHEED calibration is not necessary until the state of the ion gauge is changed or there is major alteration to the MBE system. X-ray measurements may be used to confirm that the InP substrate and the ternary materials are lattice-matched. Fine adjustments can then be made to the calibrated beam flux values to compensate for any possible drift in the ion gauge.

Calibration of the source cell temperatures using beam equivalent flux is preferred because the process is less time-consuming. Furthermore, the UCSB MBE systems have been set up with control computers that are able to automatically heat and dump the sources, open the source shutters, and sample the beam flux according to a user-defined control program. A complete array of temperature versus beam flux measurements can be obtained before the grower arrives for the day's growths. Our experience suggests that beam flux calibration is a very robust method. Early in the project, all growths in System A were calibrated by RHEED. Later growths requiring the phosphorous source in System B used beam flux calibrations exclusively.

The epi-ready substrates are mounted to molybdenum conversion blocks and loaded into the MBE system through a load-lock system and allowed to pump down overnight. The load-lock chamber is heated for several hours during the initial pump down to aid in degassing the chamber walls and the trolley system that carries the molybdenum blocks and wafers. Before entering the MBE growth chamber, each substrate is heated to 300ºC in the high vacuum buffer chamber for approximately one

hour. The substrate and block assembly is further baked in the growth chamber at 400ºC for ten minutes before being turned to face the source cells (growth position). As the substrate is being baked in the growth chamber, the beam flux of the group V sources is determined and the initial group V beam is set. The group V source will be left on until the end of growth. Although the buffer chamber and growth chamber bakes are set to 300ºC and 400ºC, respectively, these temperature settings are determined and fed back to the controller via a thermocouple positioned on the radiant heater element behind the wafer. The temperature at the surface of the wafer through the silicon backing wafer and molybdenum block elements is expected to be lower.

The substrate block rotation rate is set at 10 to 20 rpm during the initial heating and during growth to help obtain uniform deposition from the fixed epi sources across the wafer. When in the growth position, the substrate's surface temperature can be measured by pyrometer. The pyrometer used on the UCSB MBE systems has a lower limit of 450ºC. The substrate is heated over a period of 20 minutes to a temperature of 520ºC to 530ºC as determined by pyrometer. Desorption of the InP surface oxide typically occurs at 530ºC to 535ºC and is complete in less than 60 seconds suggesting that the surface oxide on epi-ready InP substrates is thin. The desorption process is apparent as the RHEED pattern changes from a spotty, incomplete signal to a more streaky, complete 2×4 reconstruction. At the same time, a drop of 10ºC to 15ºC is observed in the pyrometer temperature. It is believed that the surface temperature of the wafer is not actually changing, but that the emissivity of the surface is changed as the oxide is removed. The wafer is brought back to the oxide removal temperature

and allowed to remain at that temperature for about 60 seconds. The temperature is then lowered to 475ºC in preparation for growth with the expectation that the temperature at the wafer's surface will rise when the source shutters are opened. Growth is generally initiated at 480ºC to 510ºC for InP lattice matched materials. Pyrometer readings are viewed during 10 second growth pauses throughout the growth. The readings are taken only when the source shutters are closed to prevent deposition onto the pyrometer window but also because the emissivity at the wafer surface during growth leads to inaccurate readings.

2.2 HBT Epitaxial Structure

The evolution of the regrown emitter epitaxial structure began during a period of transition in the research group as we were moving away from the transferred substrate HBT and toward what would become the narrow mesa HBT. The regrown emitter HBT evolution also occurred after the installation of CBr_4 carbon dopant sources on Systems A and B and after the installation of the group V phosphorous source on System B. The carbon doping source allows for higher p-type doping of the InGaAs base region while maintaining bulk mobility comparable to that of beryllium doping. The availability of the phosphorous source was significant as it allows for the development of HBT epitaxial stacks containing wide bandgap InP layers as the collector and emitter regions.

The baseline transferred substrate HBT structure is shown in Figure 2.1. The HBT structure used in the transferred substrate work employed an InAlAs emitter as the single heterojunction and an InGaAs collector beneath the beryllium-doped

InGaAs base. The device structure of the transferred substrate HBT does not require a heavily-doped subcollector region, and one was not included in the typical epitaxial stack.

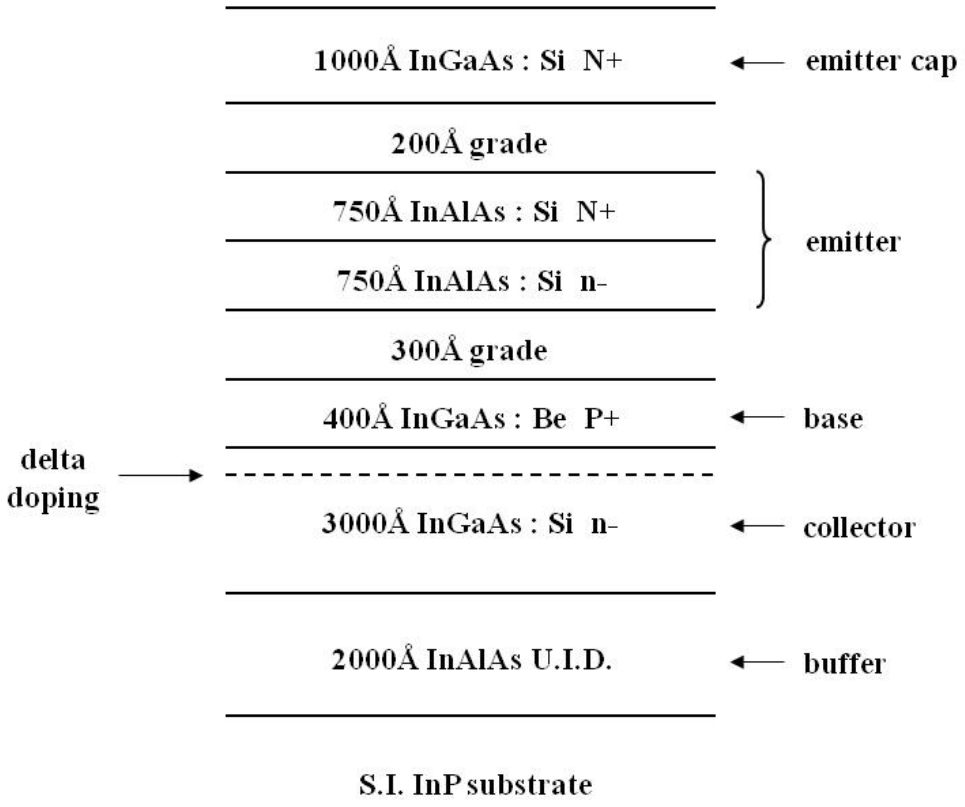


Figure 2.1 Baseline structure for transferred substrate SHBT with InAlAs emitter.

SHBTs have achieved impressive device performance[1] and are more simple to design and grow compared to DHBTs. The SHBT InGaAs collector requires only a change in doping as the HBT growth transitions from the collector to the base. A collector region composed of InGaAs, however, will have a lower breakdown tolerance than one composed of a wide bandgap semiconductor such as InP. For instance, the bias across a 2000 Å thick InGaAs collector requires only about 2.2V

before current avalanche sets in. A composite InP collector of the same thickness can take up to 7.5V before breakdown.[2] Low avalanche breakdown prevents the use of the thinner collector regions that would allow for higher current densities. In addition to the low breakdown problem, the thermal conductivity of InGaAs is 1/15th that of InP. When HBTs are run at high current densities, heat management becomes a critical issue and an InP collector would be preferred to InGaAs for its superior ability to dissipate heat.

An epitaxial stack that could be used for a conventional mesa structure DHBT is shown in Figure 2.2. This structure incorporates an InP collector for higher breakdown and better heat dissipation. It also includes a carbon-doped base region to obtain a higher doping-mobility product. A thin, heavily-doped InGaAs layer is included as a narrow bandgap contact layer to the subcollector while the bulk of the subcollector is composed of heavily-doped InP. The ternary InGaAs layer thickness is minimized relative to the InP layers to improve the thermoconductivity of the epitaxial stack. The InAlAs emitter and chirped superlattice grade that are used in the transferred substrate HBT have been carried over to this proposed mesa structure DHBT. It would also be possible, however, to use an InP layer as the wide-bandgap emitter material. The InP emitter details will be discussed later in this chapter.

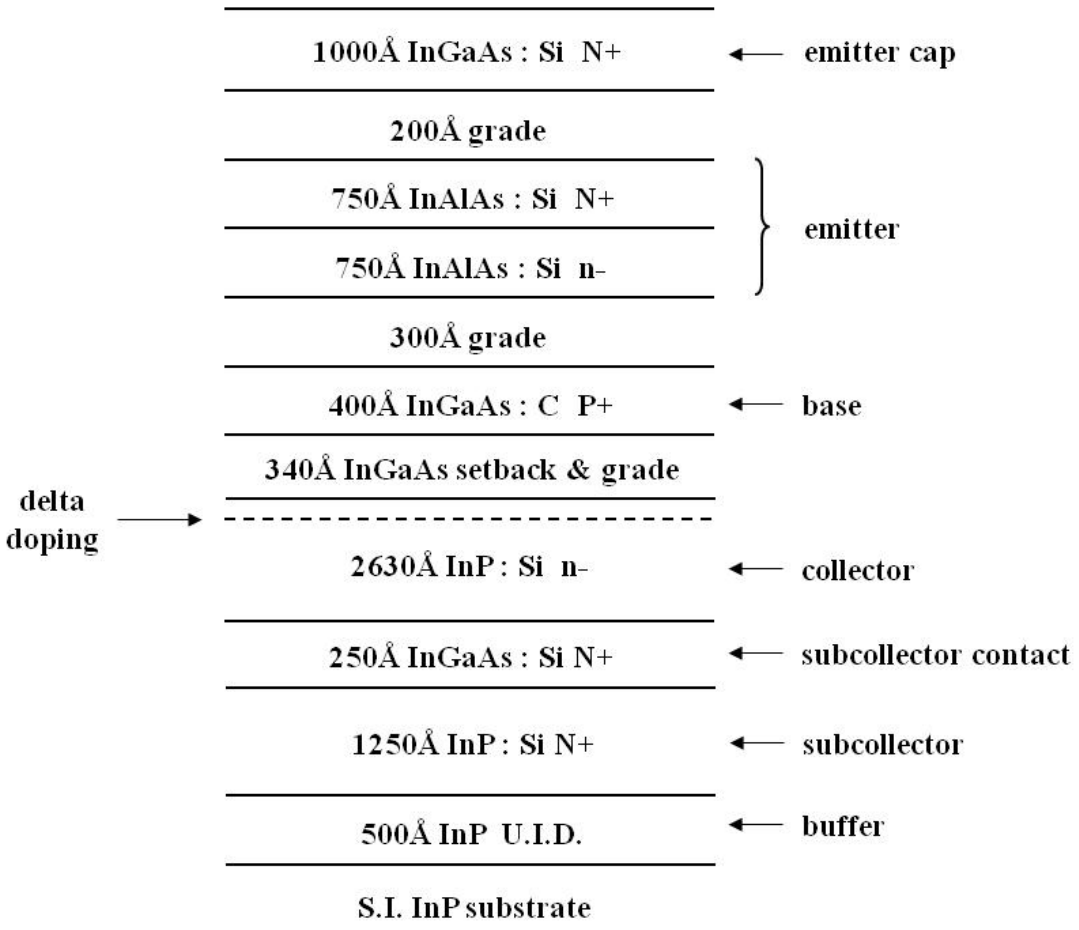


Figure 2.2 Epitaxial stack for a mesa structure DHBT with graded InAlAs emitter, carbon-doped base, and InP collector.

2.3 Base Layer Growth – InGaAs:Be

A report from the early 1980s showed that InGaAs could be doped into the low 10^{19} cm^{-3} range with nearly complete activation using beryllium by solid-source MBE.[3] Beryllium was widely adopted as the p-type dopant for MBE of III-V compounds. Following this, many papers relating to the diffusion of beryllium and the growth conditions to minimize this diffusion began to appear. It has been experimentally determined that the diffusion coefficient of beryllium acceptors

depends on the concentration of beryllium as well as the growth temperature of beryllium-doped layers and the layers grown after the beryllium-containing layers.[4] Dopants may also diffuse due to electric fields formed in the material during the growth process. Controlling the diffusion of beryllium and the growth conditions that favor high activation efficiency of beryllium in InGaAs is discussed in this section.

Low sheet resistance and minimal transit time requires the base layer to be thin (hundreds of angstroms) and heavily doped with *active* carriers. Beryllium diffusion into the lightly-doped collector can render regions of the collector p-type. This would affect the Kirk effect threshold and the overall transit time of carriers through the HBT. Beryllium diffusion into the emitter affects the turn-on voltage V_{be}, the DC current gain, the ideality factor, and the base transit time. These types of problems make beryllium diffusion a sinificant concern when designing and growing HBT structures. It is a problem, however, that may be addressed in several ways: steps may be taken to minimize the diffusion itself, the existing diffusion may be accepted and the effects may be minimized, or beryllium doping may be avoided altogether. The process where beryllium diffusion is minimized will be discussed here, and the replacement of beryllium as a p-type dopant in InGaAs will be addressed in a later section.

The most common remedy for beryllium diffusion is to grow the beryllium containing layers at lower temperatures. Aiding in this solution is that beryllium is less mobile at lower temperatures and diffuses less. Note that it is not enough to grow only the beryllium-doped layers at lower temperature; the subsequent layers also need

to be grown at lower temperatures to maintain the minimal diffusion. Enhanced activation at high doping concentrations may also occur at lower growth temperatures due to inhibited formation of electrically inactive beryllium precipitates.[5] That is, the lower surface mobility of adatoms at the lower growth temperatures makes it more difficult for the beryllium atoms to find one another and form clusters on the growth surface. The growth temperature used in this work for the beryllium-doped base growth is estimated to be 380ºC. This temperature is estimated because the infrared pyrometer used to measure the substrate surface temperature during growth has a lower measurement limit of 450ºC. The 380ºC growth temperature is estimated by lowering the substrate temperature from 480ºC to 455ºC at the beginning of the base growth. The thermocouple setpoint is then lowered an additional 75ºC to achieve the estimated 380ºC substrate temperature.

Increasing the group V As_2 flux during the beryllium-doped InGaAs growth may also allow for higher doping concentration. In order to form electrically active p-type carriers, the beryllium dopant needs to incorporate into the group III sites. The concentration of group III vacancies increases relative to the group V vacancies as arsenic flux is increased. It should follow that the group III vacancies will then be the preferred incorporation sites and higher beryllium doping will be obtained.[4] Further details on the development of growth conditions for beryllium-doped InGaAs for use in HBT base layers are detailed in Dr. Dino Mensa's thesis.[6]

The hole concentration in InGaAs as a function of the beryllium cell temperature on each MBE system is determined using Hall measurements of doping

calibration samples. These samples are composed of unintentionally-doped InAlAs buffer layers grown on semi-insulating InP substrates with the doped material of interest grown on top. The InAlAs buffer layer is a high-resistance layer used to initiate arsenide growth on InP and to provide a smooth growth surface prior to deposition of the doped InGaAs. Table 2.1 shows a four year summary of beryllium-doped InGaAs doping calibration results for MBE growth System A. The beryllium cell temperature and the resulting hole concentration and mobility are indicated. Note the increasing beryllium cell temperature required to obtain doping concentrations in the low-$10^{19}cm^{-3}$ range between 1998 and 2000. Beryllium was added to the doping cell in the spring of 2001. After this time, it was observed that higher doping could be obtained at lower cell temperatures.

Table 2.1 InGaAs:Be Hall measurements results from System A.

Date	**Cell Temp. (ºC)**	**Doping ($\times 10^{19}$ cm^{-3})**	**Mobility (cm^2/V-s)**
1/1998	980	4.2	50.5
3/1999	985	2.8	57.2
6/2000	1000	2.5	41.8
6/2000	1000	2.4	64.9
7/2000	1020	3.3	57.5
8/2000	1020	3.1	53.4
9/2001	950	1.2	58.2
9/2001	975	2.5	51.8
9/2001	990	3.6	52.0

2.4 Base Layer Growth – InGaAs:C

The problems with beryllium diffusion and the growth conditions that minimize diffusion may be simply avoided by using an alternate p-type doping source in the base layer. Carbon is known to have a diffusion coefficient roughly three orders of magnitude lower than that of beryllium at similar temperatures and concentrations. In this work, a carbon tetrabromide source (CBr_4) has been used. The source and controller unit used on System A was fabricated and installed by Dr. Ryan Naone and MBE lab supervisor John English when Dr. Naone was a graduate student at UCSB. The UCSB CBr_4 source design was modeled after a CBr_4 source built at Penn State University.[7] After successful demonstration and minor modifications were made to the CBr_4 source on System A, a second source and controller were built and installed on the System B MBE.

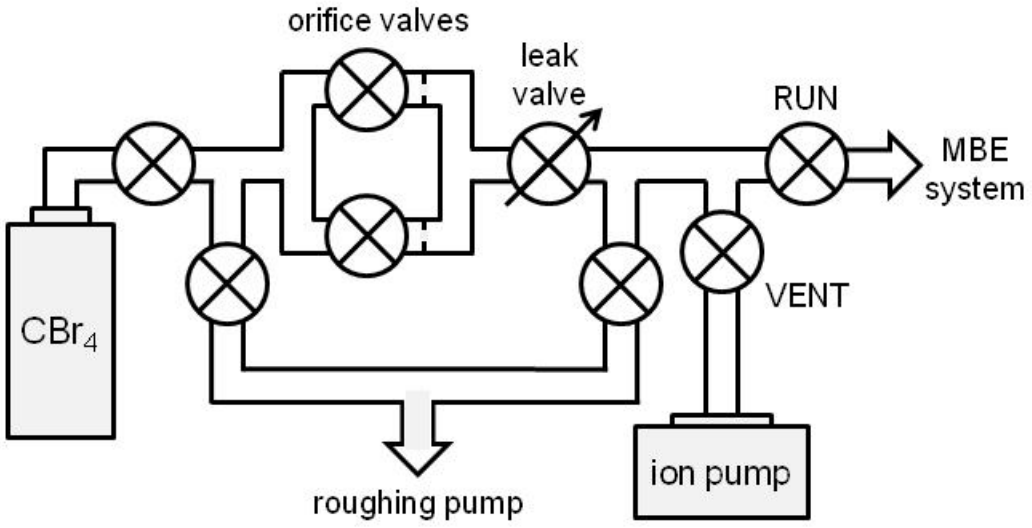


Figure 2.3 Schematic of the CBr_4 carbon source gas manifold.

A schematic of the carbon source is shown in Figure 2.3. The CBr_4 material has been vacuum deposited into a small stainless steel cylinder by the vendor, and is maintained at a low temperature (usually -5ºC) in our system to reduce the sublimation rate. The CBr_4 vapor is passed through one of two fixed-size orifices before arriving at an adjustable leak valve. These orifices are additions to the original design and are intended to limit the amount of vapor arriving at the leak valve. The adjustable leak valve is controlled by the user to ultimately limit the amount of CBr_4 flowing from the source. The vapor is directed from the leak valve to either an ion pump where the flux of the CBr_4 can be measured or into the MBE system for doping of materials. This is the so-called RUN/VENT method where RUN corresponds to the dopant entering the MBE system and VENT represents diversion of the CBr_4 to the ion pump. The purpose of the RUN/VENT system is to set up a steady state of CBr_4 flux as the vapor is flowing into the ion pump during VENT mode. The ion pump current and pressure can be monitored during this steady state of flow and these parameters can help to determine and reproduce the carbon doping level when the CBr_4 is directed to the growth chamber. The CBr_4 flows into the ion pump until carbon doping is desired. At that point, the system is set to RUN mode, and the dopant is routed to the growth chamber instead of the ion pump.

In order to take full advantage of carbon's reduced diffusion coefficient relative to beryllium, the dopant should be deliverable to the growth sample on a scale that is short relative to the growth of a few monolayers. This is a concern for the CBr_4 system because the RUN valve is physically located outside of the MBE system and is

connected through about 50 cm of stainless steel tubing. Furthermore, the carbon source has no shutter mechanism inside of the MBE so the RUN valve is the final point of control for the system. By monitoring the beam flux gauge, it has been determined that the doping source requires 10 seconds to achieve 90% rise and fall times. The 10 second rise time is attributed to the time required to fill the 50 cm of line with CBr_4 when the valve is switched from VENT to RUN mode. The fall time corresponds to the time required to empty the line of CBr_4 after the valve has been switched to VENT. At a typical growth rate of 1μm/hour, 10 seconds corresponds to about 28 Å of growth. A method to circumvent (or to at least reduce) the lag when turning on the carbon source is to switch the valve to the RUN position up to 10 seconds prior to the anticipated growth of the carbon-doped layers. Circumventing the lag time when turning the source off can be handled by a 10 second growth interruption where growth is resumed after the CBr_4 has been removed from the RUN line. The installation of a shutter for the carbon source would probably be the most complete solution to the lag time issue.

The growth conditions for carbon-doped layers are slightly modified from those used to grow beryllium-doped layers. It is known that the group IV carbon dopant can demonstrate amphoteric behavior in III-V compounds. For instance, while carbon acts as an efficient p-type dopant in GaAs, it is an inefficient n-type dopant in InAs and InP. As a deterrent to n-type compensation, the V/III ratio is decreased during carbon-doped growth to encourage incorporation of the carbon dopant onto the group V vacancies. Also, with diffusion being less of a concern, carbon-doped

samples are typically grown at a temperature of at least 420ºC compared to the estimated growth temperature of 380ºC when beryllium is used. Doping calibrations were grown to characterize carbon doping and mobility in InGaAs using the CBr_4 source. The data was also intended to provide a reference for doping level versus the ion pump parameters used to monitor the CBr_4 flux. A summary of the results is shown in Table 2.2.

As shown in the table, only the ion pump current was initially recorded in an attempt to establish its relationship to the doping concentration or the doping-mobility product. The ion pump pressure is a more sensitive indicator of the carbon flux into the pump, and it has also been recorded for more of the growths listed in Table 2.2. However, the ion pump parameters do not appear to be well-controlled predictors of the doping or doping-mobility product in InGaAs as shown in Figure 2.4. Also shown in the table are the results of growth temperatures up to 480ºC. Raising the growth temperature did not improve the predictability of the carbon doping versus the ion pump parameters. However, the data does reveal that the carbon-doped InGaAs can be grown over a wide range of temperatures without altering the doping concentration and mobility results. The data shown in Table 2.2 suggests that the control of doping concentration is limited by some variable that has not yet been determined.

Table 2.2 Carbon doping source parameters and Hall measurement results from System A.

Date	Substrate Temp. (°C)	Ion Pump Current (μA)	Ion Pump Pressure (10^{-7} torr)	Doping ($\times 10^{19}$ cm^{-3})	Mobility (cm^2/V-s)
7/2000	420	230	--	4.1	45.8
7/2000	420	310	--	5.6	47.4
7/2000	420	370	--	5.5	52.3
7/2000	420	310	--	6	53.5
7/2000	420	310	--	6.3	40.7
1/2001	420	350	7.9	8	47.5
1/2001	420	410	9.2	9.2	30.4
2/2001	420	650	15	9.3	43.3
2/2001	420	570	13	8.8	45.9
2/2001	420	480	11	8.8	44.2
2/2001	420	400	8.9	7.3	50.5
4/2001	420	465	11	15	30.3
4/2001	420	420	9.4	14.6	30.2
4/2001	420	360	7.9	13	31.7
6/2001	420	410	9.2	12	12.5
6/2001	420	380	8.5	12	27.4
6/2001	420	340	7.6	12	37.2
6/2001	420	300	6.7	11	37.7
7/2001	420	265	5.8	9.6	40.3
7/2001	420	240	5.4	9.8	38.3
7/2001	420	250	5.6	8.4	32.9
9/2001	470	420	9.3	8.8	41.3
9/2001	470	370	8.3	9.5	39.6
9/2001	470	320	7.2	8	5.4
11/2001	480	320	7.2	7.4	39.5
11/2001	480	380	8.6	6.6	36.4
11/2001	480	320	7.2	7.9	39.3

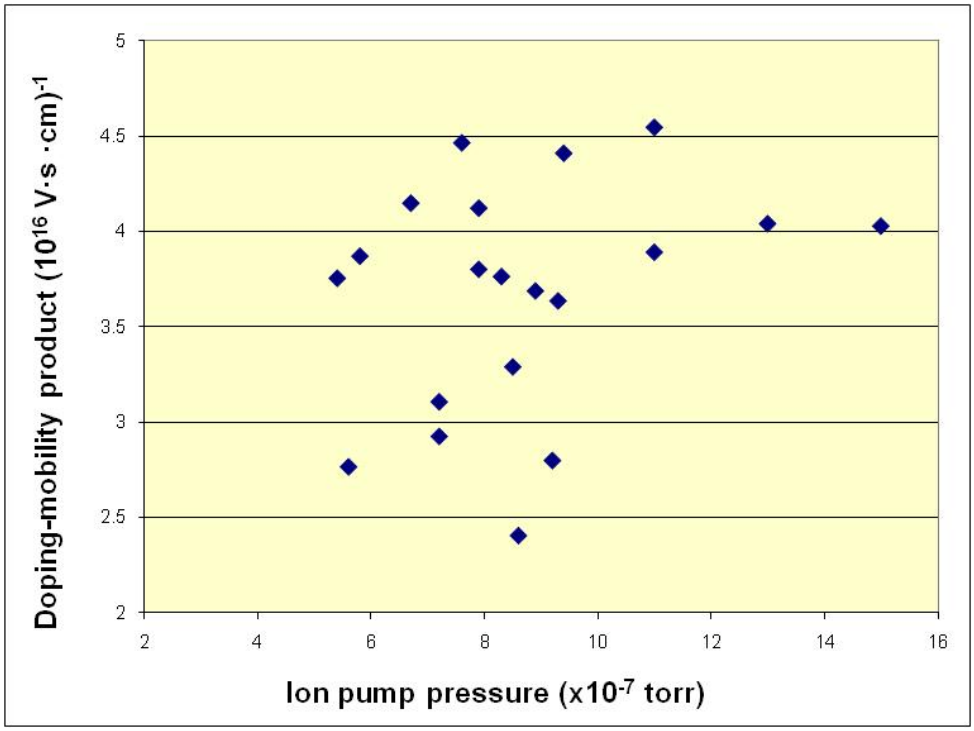


Figure 2.4 Carbon doping-mobility product instability suggests that ion pump pressure is not a well-controlled predictor of InGaAs doping and mobility from the CBr4 source.

Despite the lag issues with the RUN/VENT system and the lack of predictable doping control, carbon doping from the CBr_4 source is able to produce higher doping concentrations compared to beryllium doping. The higher carbon doping can also be obtained while maintaining comparable mobilities to those of beryllium-doped InGaAs. Hole mobility for carbon-doped InGaAs is plotted as a function of hole concentration in Figure 2.5. Also shown are similar data points obtained from beryllium-doped InGaAs. Hole concentrations may be obtained in beryllium-doped InGaAs in the 1×10^{19} cm^{-3} to 4×10^{19} cm^{-3} range with mobilities in the 50 to 60 cm^2/V-s range. Carbon-doped InGaAs has typical hole concentrations in the 4×10^{19} cm^{-3} to 15×10^{19} cm^{-3} range with mobilities in the 40-50 cm^2/V-s range. While the overall

mobility data for the carbon-doped samples is lower than in the beryllium-doped samples, it should be noted that the doping-mobility *product* is most meaningful when heavily doping the base layer for low sheet resistance. The higher doping-mobility product for carbon-doped InGaAs along with the much lower tendency to diffuse into neighboring epi regions puts carbon ahead of beryllium as a base dopant.

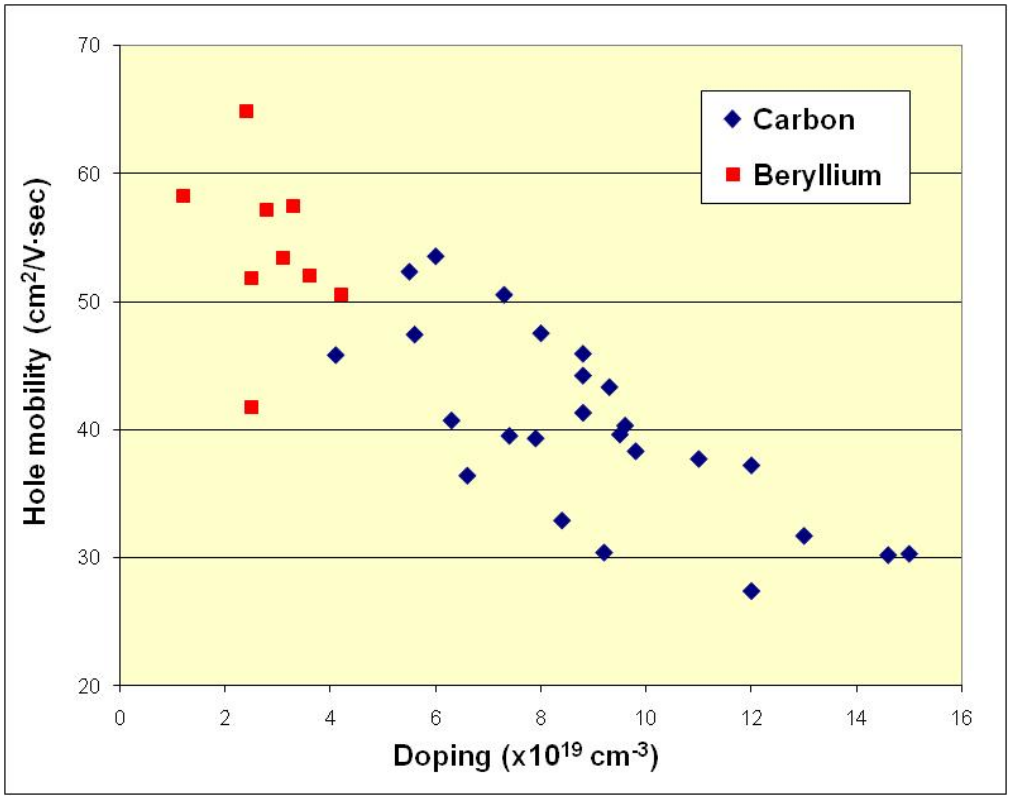


Figure 2.5 Hole mobility for carbon and beryllium-doped InGaAs as a function of hole concentration.

2.5 Growth of the Collector Layers

The growth conditions for a lightly, Si-doped InGaAs collector region in a SHBT are optimized to reduce the possibility of scattering as electrons pass through it. Growth

temperatures between 480ºC and 510ºC are high enough to produce good crystal quality in an InGaAs collector region. The As_2 flux should also be just sufficient to keep the growth surface As_2 rich. It has been observed that a minimal background pressure produces material with higher mobility; suggesting decreased impurity incorporation during the growth. The subcollector contact layer shown in Figure 2.1 typically requires heavy silicon doping at or above 1×10^{19} cm^{-3} and is grown with a high As_2 flux to improve the activation efficiency of silicon.

Hall measurements for light and heavy Si doping of InGaAs are generally performed every four to six months and after all major MBE system maintenance openings. The doping calibrations versus temperature generally do not change in a significant manner over these time intervals. The monitoring practice, however, is maintained as a verification. InGaAs samples are grown for at least three Si doping cell temperatures in narrow temperature ranges; one range for lightly-doped InGaAs and one for heavily-doped InGaAs. An exponential curve fit is established based on the Hall data and the temperature required to obtain specific doping levels can be extrapolated in these ranges. A sample of these plots are shown in Figure 2.6 and Figure 2.7. It has been found that the Si doping behavior in InAlAs is similar to that in InGaAs when grown in the 480ºC to 510ºC temperature range, and it is assumed that the doping concentration is similar for both materials during collector growth.

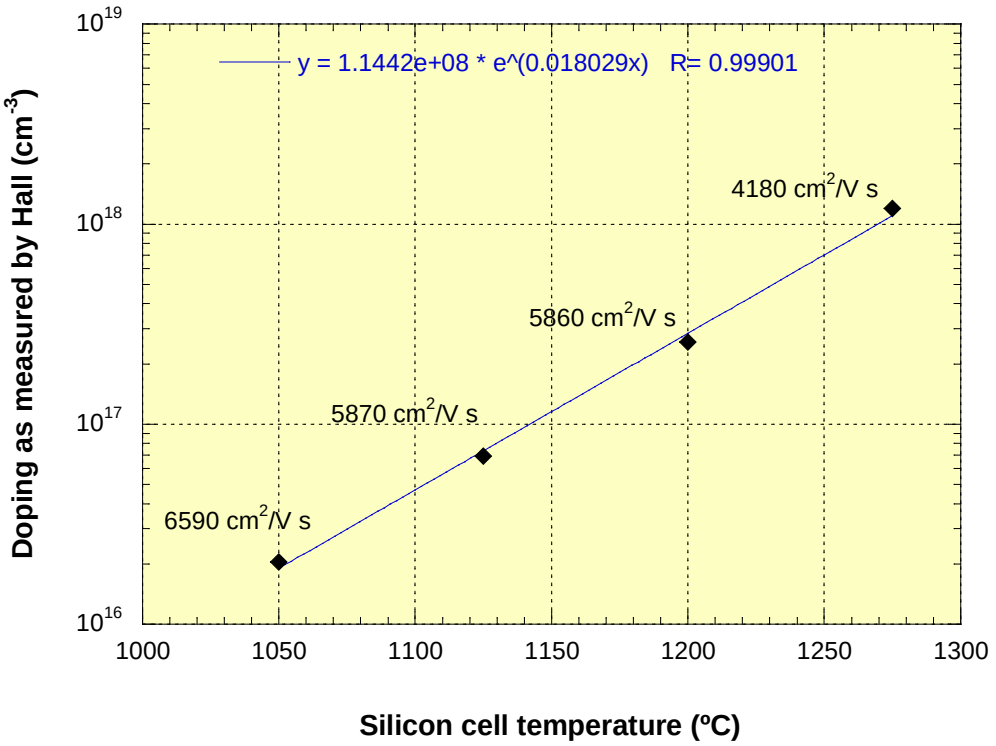


Figure 2.6 Silicon doping and mobility data versus temperature for lightly-doped InGaAs.

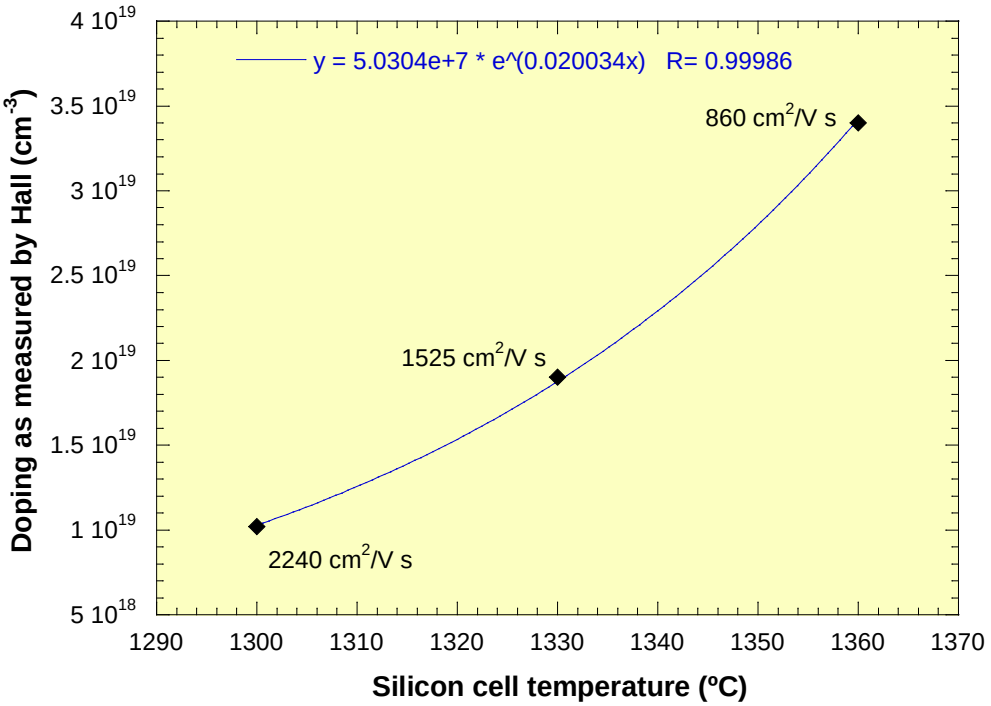


Figure 2.7 Silicon doping and mobility data versus temperature for heavily-doped InGaAs.

As mentioned earlier, InP can also be used as the collector material to form a DHBT with an InGaAs base. The InP collector allows for a higher breakdown and better heat dissipation when compared to a SHBT with an InGaAs collector. The use of a thick, heavily-doped InP region as a subcollector also has better heat dissipation than an InGaAs subcollector. However, using an abrupt InP collector with an InGaAs base in a DHBT creates a conduction band discontinuity that would severely degrade device performance. The discontinuity will increase the base electron storage time and electron-hole recombination due to electron trapping in the base. A grading layer is therefore used in the DHBTs of this work to suppress the base-collector conduction band discontinuity. The base-collector grade is most often composed of a 200 Å unintentionally-doped setback layer and an InAlAs/InGaAs chirped superlattice grade from InGaAs to $In_{0.26}Ga_{0.26}Al_{0.48}$. This produces zero conduction band offset at the interface to the InP collector region. The superlattice period is as small as 15 Å to suppress miniband effects and the associated transit time degradation. A 30 Å pulse-doped Si layer ($N_{d,pulse} = 3\times10^{18}$ cm^{-3}) is also inserted at the InP interface to suppress the change in conduction band quasi-field.

The growth of InP material for the collector and subcollector is typically carried out at temperatures between 480ºC and 500ºC. The phosphorous beam flux is moderately high (beam equivalent pressure of 6 to 7×10^{-6} torr). Doping calibration for the InP layers are conducted in a manner similar to that described above for silicon in InGaAs. The doping calibrations for InP layers is used for the subcollector, collector,

and for InP emitter layers. A sample of the Hall doping and mobility data for silicon in InP versus doping cell temperature is shown in Figure 2.8.

The heavily-doped InP subcollector growth typically follows an unintentionally-doped InP buffer layer. The buffer is grown on the InP substrate after oxide desorption, and the buffer acts as a smoothing layer between the substrate and active epitaxial layers.

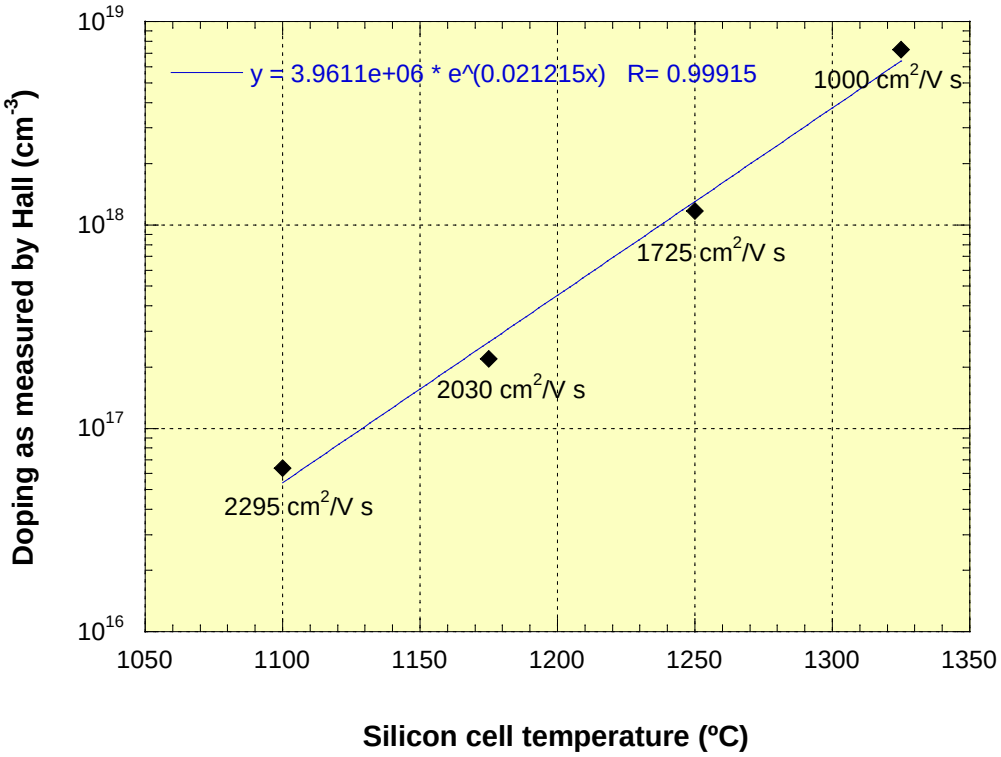


Figure 2.8 Typical doping and mobility data versus temperature for silicon-doped InP.

2.6 Growth of the Emitter Layers

InAlAs or InP can be used as the emitter regions for an InP HBTs. InAlAs offers certain advantages, including reduced base-emitter surface leakage and good passivation with SiN. Also, because the InAlAs bandgap is larger than InP (1.48 eV

compared to 1.35 eV), a larger valence band discontinuity is possible for InAlAs especially when the base-emitter junction is graded. The choice of base dopant also helps to determine the choice of emitter material as the diffusion of dopant from a beryllium-doped base into the emitter can be better controlled by inserting a graded region at the base-emitter junction as described later. The use of carbon doping in the base region may require that an all wet etch emitter process be used. The wet etch process used for InAlAs and InGaAs laterally undercuts a significant amount of the emitter material even under carefully controlled etch conditions. This process is unsuitable when forming sub-micron scale HBTs. The wet etch process for an InP emitter, in contrast, offers a smaller etch undercut that terminates even if excessive wet etching is required.

The base-emitter heterojunction for both InAlAs and InP can be either graded or abrupt, and there are several factors when deciding between a graded and abrupt junction. Normally a graded base-emitter junction has a lower turn-on voltage, a higher threshold for hole reverse-injection from the base, and a lower junction ideality factor. A ledge structure can also be incorporated into the base-emitter grade to reduce base-emitter leakage current; increasing DC current gain. An abrupt base-emitter junction, requires a simpler epitaxial design and simpler growth, higher turn-on voltage, lower threshold for hole-back injection, and higher ideality factor. An abrupt base-emitter junction can also provide higher DC current gain (without a ledge) and may reduce base transit time as electrons are injected into the base with minimum barrier energy.

The choice of base dopant may also influence the decision between using a graded or abrupt emitter. Carbon doping in InP creates an n-type semiconductor. In this case, using an abrupt InP emitter may be advantageous when using a carbon-doped base. The use of heavily-diffusive beryllium in the base layer does not work as well with an abrupt base-emitter junction. In an abrupt junction, beryllium diffusion of only a few tens of angstroms has been shown to significantly degrade f_τ and current gain. Accepting that the beryllium will diffuse, a base-emitter grading structure can be designed to reduce the sensitivity of device parameters to the diffusion. Base-emitter junctions that are graded over a few hundred angstroms exhibit f_τ and current gain that vary more slowly as a function of beryllium diffusion distance.[8]

A graded superlattice junction that could be used between an InGaAs base and InAlAs emitter is shown in Figure 2.9. In this structure, alternating layers of InGaAs and InAlAs are used to approximate a liner grade from the base to emitter. During the growth the wafer rotation is increased to 20 rpm to ensure good uniformity of the thin layers across the wafer. An analog, linear grade where the aluminum and gallium compositions are uniformly graded across the entire thickness of the junction is not easy to accomplish using MBE and requires precise control of the thermal response from the aluminum and gallium cells as the heater powers are adjusted. The thermal response of each cell changes as the cells become depleted through use, and the reproducibility of the base-emitter grading is made even more difficult. The graded superlattice structure may also provide an advantage over the analog grade; the

multiple interface grade may suppress beryllium diffusion as the dopant may preferentially incorporate into only one of the superlattice layers.[9]

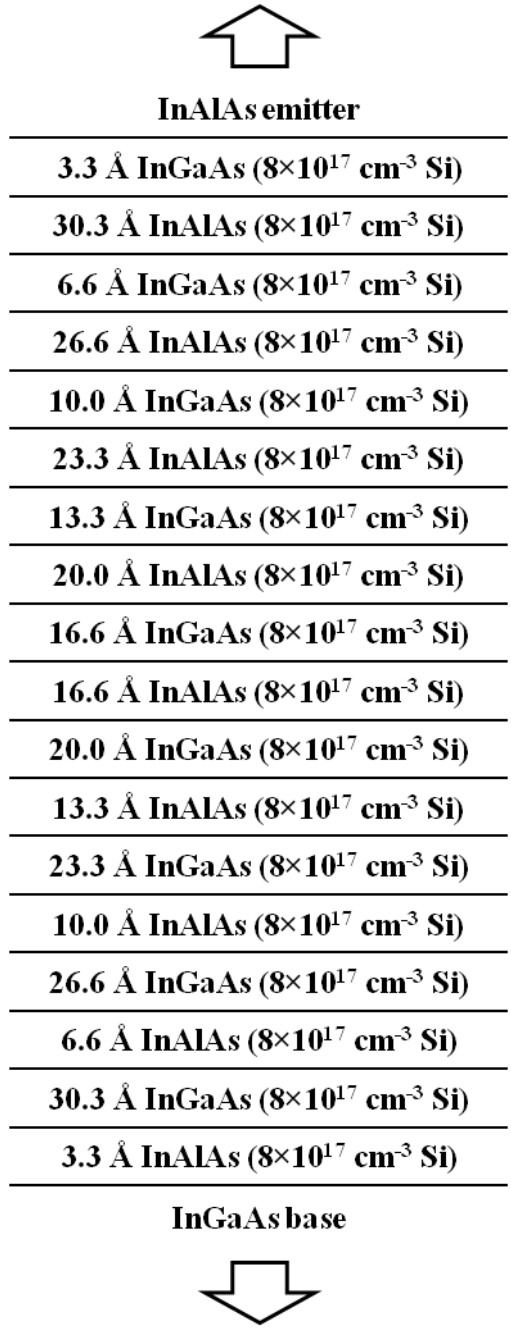


Figure 2.9 Epitaxial graded superlattice structure between an InGaAs base and InAlAs emitter.

The emitter growth follows the growth of the base layer and requires about 30 additional minutes for typical emitter designs. If beryllium is used as the base dopant, the emitter growth cannot be conducted at the same temperatures as used for the collector layer growth because of the beryllium diffusion. The emitter layers for a beryllium-doped base are generally grown at an estimated 380ºC. The emitter and cap layers have a surface morphology that is rough compared to typical epitaxial layers, and this is attributed to the low growth temperatures. Doping calibrations for the low-temperature growth of InAlAs and InGaAs show that electron concentrations in InAlAs are about 20% lower than in InGaAs. A theory proposed in literature suggests that higher growth temperatures may be required for InAlAs to obtain the highest electron concentration using silicon dopant.[10]

[1] Lee, Q.; Martin, S.C.; Mensa, D.; Smith, R.P.; Guthrie, J.; Rodwell, M.J.W., "Submicron transferred-substrate heterojunction bipolar transistors," *Electron Device Letters, IEEE*, vol.20, no.8, pp.396-398, Aug 1999.

[2] Dahlstrom, M.; Fang, X.-M.; Lubyshev, D.; Urteaga, M.; Krishnan, S.; Parthasarathy, N.; Kim, Y.M.; Wu, Y.; Fastenau, J.M.; Liu, W.K.; Rodwell, M.J.W. , "Wideband DHBTs using a graded carbon-doped InGaAs base," *Electron Device Letters, IEEE*, vol.24, no.7, pp. 433- 435, July 2003.

[3] Cheng, K. Y.; Cho, A. Y.; Bonner, W. A., "Beryllium doping in Ga0.47In0.53As and Al0.48In0.52As grown by molecular-beam epitaxy," *Journal of Applied Physics*, vol.52, no.7, pp.4672-4675, Jul 1981

[4] Miller, Jeffrey N.; Collins, Douglas M.; Moll, Nicolas J., "Control of Be diffusion in molecular beam epitaxy GaAs," *Applied Physics Letters*, vol.46, no.10, pp.960-962, May 1985.

[5] R. A. Hamm, M. B. Panish, R. N. Nottenburg, Y. K. Chen, and D. A. Humphrey, "Ultrahigh Be doping of $Ga_{0.47}In_{0.53}As$ by low-temperature molecular beam epitaxy," *Applied Physics Letters*, vol.54, no.25, pp.2586-2588, June 1989.

[6] Mensa, Dino. "Improved Current-Gain Cutoff Frequency and High Gain-Bandwidth Amplifiers in Transferred Substrate HBT Technology." Diss. U of California, Santa Barbara, 1999. Print.

[7] Miller, D. L.; Micovic, M.; Lubyshev, D. I.; Cai, Weizhong; Hwang, Wen-Yen; Zhang, Kai, "Iodine and carbon tetrabromide use in solid source molecular beam epitaxy," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol.16, no.3, pp.1361-1366, May 1998.

[8] Metzger, R. A.; Hafizi, M.; Wilson, R. G.; Stanchina, W. E.; Jensen, J. F.; McCray, L. G., "Be diffusion at the emitter-base junction of graded AlInAs/GaInAs heterojunction bipolar transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol.10, no.6, pp.2347-2350, Nov 1992.

[9] Hafizi, Madjid; Metzger, Robert A.; Stanchina, William E., "Stability of beryllium-doped compositionally graded and abrupt AlInAs/GaInAs heterojunction bipolar transistors," *Applied Physics Letters*, vol.63, no.1, pp.93-95, Jul 1993.

[10] Higuchi, M.; Ishikawa, T.; Imanishi, K.; Kondo, K., "Doping characteristics of Si into molecular-beam epitaxially grown InAlAs layers," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol.9, no.6, pp.2802-2804, Nov 1991.

Chapter 3

MBE Growth of Polycrystalline Semiconductors

3.1 Motivation for Polycrystalline Material

Ion implanted polycrystalline silicon (polysilicon) is an important material for silicon BJTs and SiGe HBTs as polysilicon is used to form extrinsic contact layers to the base and emitter regions. Extrinsic polysilicon emitter contacts are used as both the contact and diffusion source in self-aligned bipolar transistors.[1,2] The extrinsic emitter region produces a low-resistance emitter contact that is much larger than the base-emitter junction. This feature permits silicon bipolar transistors to operate at very high current densities. The heavily-doped polysilicon is also used to define the very narrow base-emitter junction. Operation at high current densities provides a decisive advantage in fast digital and mixed-signal ICs. In addition, SiGe HBTs use buried dielectric layers in combination with the regrown polysilicon base contact layers to achieve narrow base-collector junctions while maintaining large base contact areas.[3] The minimal base-collector overlap reduces the $R_{bb}C_{cb}$ product, partially compensating for the poor mobility and low collector electron velocity in silicon bipolar materials.

In contrast, mesa structure InP HBTs have large base-collector junction areas that are defined by the base width. A compromise must be made in the base contact width to reduce base contact resistance while also minimizing base-collector capacitance. The InP HBT fabrication processes used to produce sub-micron emitter devices may also be limited by yield and scales of integration. It has been found that the conventional InP emitter-base junction fabrication process has lower yield as emitter dimensions are scaled to submicron dimensions. Potential yield-limiters are the self-aligned base metal lift-off process used to form base contacts close to emitter and the emitter etch process used to form narrow base-emitter junctions. Silicon bipolar fabrication processes are able to produce superior yield and scales of integration using alternate fabrication methods. The self-aligned base contacts are formed prior to the emitter deposition, and the sub-micron base-emitter junctions are formed by a combination of crystalline growth and polycrystalline deposition rather than by mesa etching.

An SEM cross-section of a 0.2 μm self-aligned selective epitaxial growth (SEG) HBT is shown in Figure 3.1 along with the process steps used to fabricated the HBT.[2] An n^+ buried layer (BL) is formed by ion implantation followed by annealing. A 0.3 μm-thick Si epitaxial layer is then deposited, and the trench grooves for isolation are formed and filled with SiO_2 by planarization with CMP. Next, the intrinsic region is covered by Si_3N_4, poly-Si, and SiO_2. This multilayer is used to form the self-aligned SEG structure. An amorphous Si film for the base poly-Si and a thick SiO_2 layer are then deposited, and a window to the intrinsic region is opened in these

films by etching. The first selectively implanted collector (SIC1) region is then formed by phosphorus-ion implantation through the multilayer and into the Si epitaxial layer, and a SiO_2 sidewall is formed in the opening. The Si_3N_4, poly-Si, and SiO_2 are then selectively dry etched in the opening and the Si_3N_4 is laterally enlarged by wet etch.

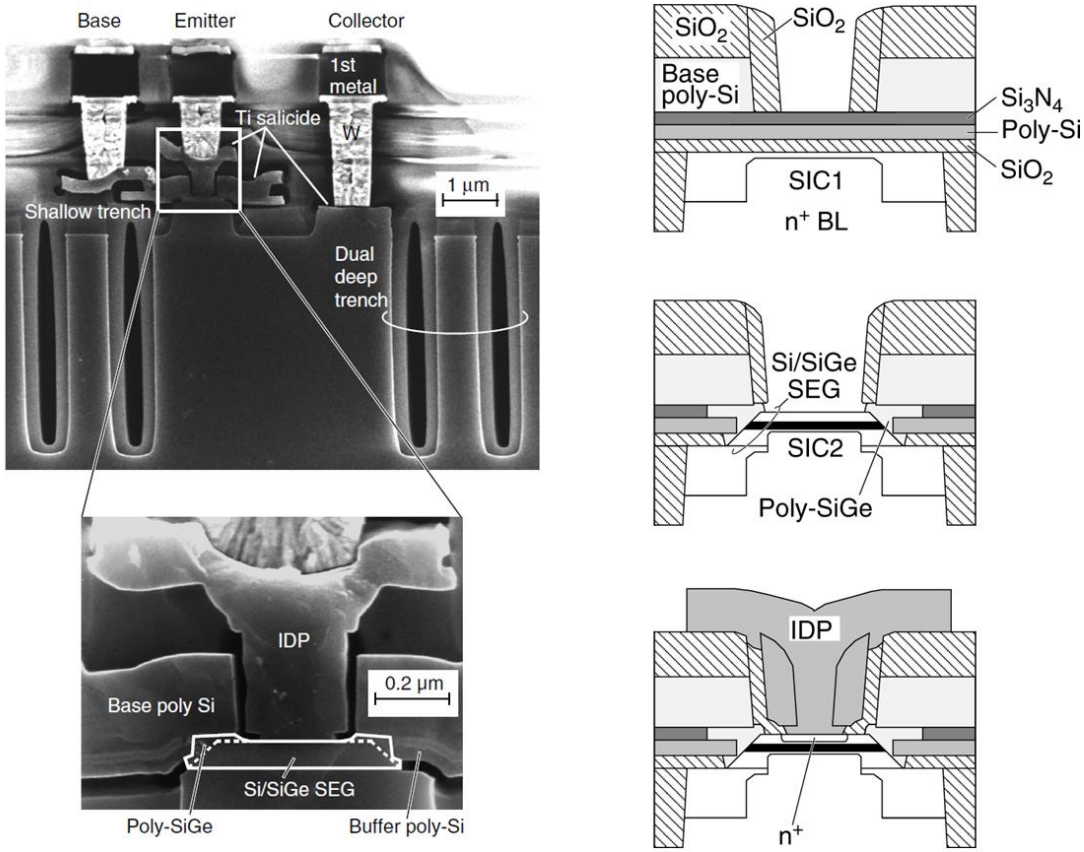


Figure 3.1 SEM cross-section of SiGe HBT with enlargement of the active device region (left), and fabrication process details used to produce a self-aligned SiGe HBT.[2]

The Si-cap and SiGe-base multilayer is selectively grown by UHV/CVD. Poly-SiGe base contacts are formed during the intrinsic SEG. The poly-SiGe forms

connections between the epitaxial base poly-Si contact layers. Phosphorus ions are then implanted in the lower part of the SEG layer to form the second SIC region (SIC2). Two selective implantations of phosphorous are applied to increase the collector-doping level.

Thin SiO_2 and in-situ phosphorus-doped poly-Si (IDP) layers are deposited, and the IDP film remains on the sidewall of the window. After an emitter area is opened by wet etching of the thin SiO_2, a second IDP layer is deposited. A shallow emitter with a junction depth of about 20nm is formed by thermal diffusion from the IDP layers into the Si-cap layer. Contacts to the emitter, base, and collector are then formed simultaneously in a self-aligned manner.

A potential path to high performance mixed-signal ICs is to combine the best features of SiGe and InP HBT technologies. We propose an HBT technology that uses InP-based semiconductor materials while also taking advantage of the structural features and fabrication processes similar to those used for SiGe HBTs. A proposed double-regrowth InP HBT fabrication process is summarized in Figure 3.2. The process begins with the formation of a collector pedestal in a previously growth collector and subcollector template. The pedestal can be formed by etching mesas into the N- collector until the N+ subcollector is reached. The semiconductor surface is then planarized with SiN_x so the N- collector pedestals are planar to the new surface. The planarization is accomplished by depositing a thick, conformal SiN_x film by PECVD and then etching back until the top surface of the collector is exposed. The collector pedestal may also be formed by coating the wafer with SiN_x, pattering and

etching openings into the SiN_x, and using MOCVD regrowth to form the N- and N+ layers into the openings. The MOCVD version of the collector pedestal process flow is more similar to the process used in SiGe HBT technology but requires MOCVD regrowth which is not a trivial process for III-V semiconductors.

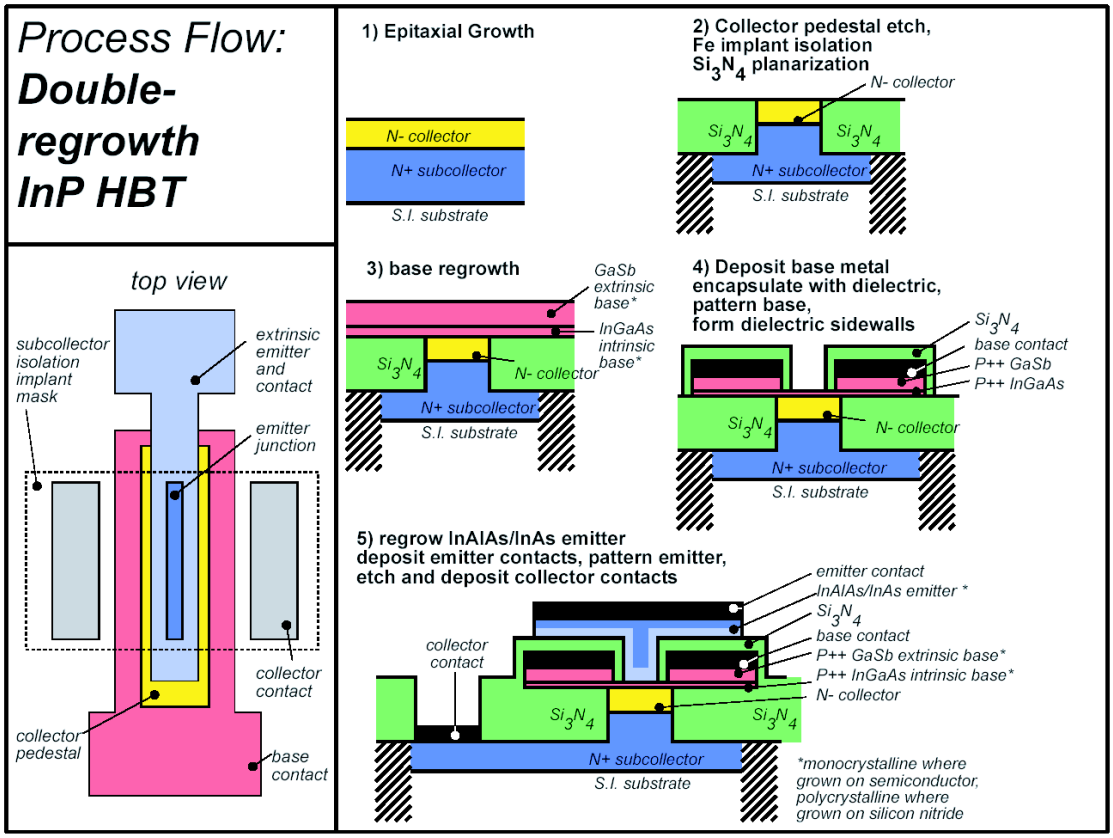


Figure 3.2 Process flow summary to form a double-regrowth InP HBT with structural features and fabrication processes similar to those used for SiGe HBTs.

Subsequent to forming the collector pedestal, the intrinsic base and extrinsic base layers are regrown by non-selective-area MBE. The non-selective growth forms monocrystalline layers where growth occurs on semiconductor and polycrystalline layers where grown on SiN_x. The base growth blankets the entire surface of the wafer

and a refractory metal is used to define base contact areas around each of the collector pedestals. The emitters are aligned to the collector pedestals and patterned in the middle of the base contacts. Emitter growth windows are etched into the extrinsic base contact layer, and the base contacts are encapsulated on the top and sidewall surfaces by SiN_x. The wafer is then returned to the MBE system for emitter regrowth. InAlAs or InP is deposited as the emitter material and a low-resistance material is deposited as the cap and emitter contact. Similar to the base regrowth, growth of the emitter is monocrystalline in the emitter window (on semiconductor) and polycrystalline over the SiN_x surface. Emitter metal is then deposited and serves as a mask during the emitter etch. A collector contact is formed by etching through the SiN_x to contact the buried subcollector region.

Using emitter regrowth, a deep submicron base-emitter junction can be formed without the base-emitter etch step that is used when fabricating mesa HBTs. As stated earlier, avoiding this step is important as it has been found to be a yield limiter with progressively increased impact as emitter dimensions are reduced. Additionally, the extrinsic emitter contact region can be defined with a width much greater than the base-emitter junction. This allows for a large emitter contact and lower emitter resistance even for deep submicron base-emitter junctions. The buried refractory contact and extrinsic base regrowth are buried underneath the emitter material prior to deposition of the emitter, and the emitter growth window is etched through the refractory metal to form self-aligned base contacts that are separated from the base-emitter junction by the width of the sidewall SiN_x. The base regrowth produces a

thick extrinsic base contact to reduce base contact resistance while allowing for a thin intrinsic base layer. The collector pedestal and buried dielectric layer under the extrinsic base region helps to minimize base-collector capacitance. This proposed process flow is intended to strongly resemble that of Si/SiGe technology.

For this double regrowth InP HBT, the extrinsic emitter layer is made of polycrystalline III-V material. To minimize the emitter access resistance, it is of key importance to have low resistivity polycrystalline material in the extrinsic emitter region. In this chapter, we discuss efforts to produce low resistivity polycrystalline material. The following section reports the details of a study where n-type InAs has been chosen as a potential candidate for the polycrystalline extrinsic emitter material.

3.2 Low-resistance Polycrystalline InAs

Ion implanted polycrystalline silicon (polysilicon) is an important material in the fabrication of silicon BJTs and SiGe HBTs. Polysilicon contacts to the extrinsic base placed over dielectric spacer layers have been successfully employed to reduce base-collector capacitance[3] while polysilicon emitter contacts are used as both the contact and diffusion source in self-aligned bipolar transistors.[1,2] There has been a trend in SiGe HBTs towards 100 nm emitter widths.[4,5,6] As emitter widths move towards 100 nm, attention has been given to the optimization of the extrinsic polycrystalline electrode to reduce resistance in the narrow emitter contact.[7]

As the emitter dimensions of III-V HBTs also scale towards deep sub-micron dimensions, a similar emitter contact method may be applied to create an extrinsic emitter contact wider than the base-emitter junction width, thereby reducing emitter

access resistance.[8,9] As shown in Figure 3.3, a low-resistance polycrystalline material may be employed as an extrinsic emitter contact layer over a buried dielectric in a regrown emitter InP HBT. Using this structure, the emitter contact area and resistance may be preserved as emitter junctions are scaled towards deep sub-micron dimensions. Although papers have also been presented using selective emitter regrowth [10,11] where minimal extrinsic emitter area is formed, a wide extrinsic emitter contact formed by non-selective emitter regrowth may prove beneficial as base-emitter junction areas are further scaled.

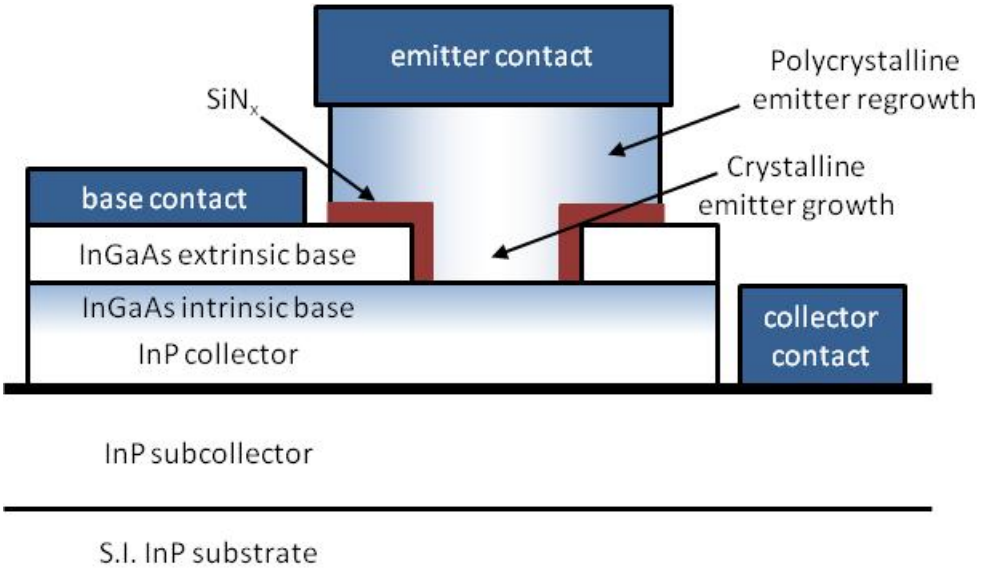


Figure 3.3 III-V HBT with extrinsic emitter contact layer over a buried dielectric.

Details of a study where n-type InAs has been chosen as a potential candidate for the polycrystalline extrinsic emitter material are presented here. InAs was chosen because of its narrow bandgap and the high carrier mobility of monocrystalline InAs bulk material. InAs also has a favorable Fermi-level pinning in the conduction

band.[12,13] This avoids carrier depletion through Fermi level pinning at grain boundaries, an effect that would increase resistivity. In this work, we study the electrical characteristics of low-resistance, silicon-doped polycrystalline InAs (poly-InAs) deposited by non-selective MBE. We examine several aspects of the growth conditions and the effects of those conditions on the conductive properties of the film.

3.2.1 Polycrystalline InAs: Experimental Procedures

Poly-InAs samples were deposited in a solid-source Varian Gen II MBE system equipped with a valved arsenic source. The n-type dopant was silicon, and the poly-InAs samples were grown on 2-inch, semi-insulating (100) GaAs substrates coated with SiN_x. Prior to SiN_x deposition, the GaAs wafers were cleaned with solvent and thoroughly rinsed in deionized water. The native oxide was removed using dilute HF solution followed by a thorough rinse in deionized water. A 1500 Å SiN_x film was deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the GaAs wafers at a temperature of 300ºC. The SiN_x was then lithographically patterned, and a 1 cm^2 area of dielectric was removed from the center of each wafer using HF etchant. This area of exposed GaAs allows for consistent temperature monitoring by pyrometer and as well as observation of the RHEED signal while the wafer is inside the MBE growth chamber.

The SiN_x coated GaAs wafers were heated in the MBE growth chamber under an arsenic overpressure to a substrate temperature of over 600ºC, and oxide desorption was confirmed by RHEED in the exposed GaAs regions. The substrate temperature was lowered prior to InAs deposition, and InAs growths were performed at various

temperatures in the 430ºC to 490ºC range. The arsenic to indium (V-III) ratios were also varied from 10 to 40 according to beam equivalent pressure (BEP) measurements, and deposition thicknesses were varied from about 750 Å to 3200 Å. These thicknesses were estimated during growth using the growth rates of monocrystalline InAs as determined by RHEED. Measurements of the actual maximum thickness for each of the poly-InAs samples were then more accurately determined by ex-situ height profilometry. The maximum thickness measurements were also confirmed by SEM cross-section on the samples of varied thickness. Growth rates for the poly-InAs depositions were maintained at 0.36 μm/hour. This growth rate was initially estimated from monocrystalline InAs RHEED and then corrected by ex-situ maximum height measurements. A fixed silicon doping cell temperature was used for all of the poly-InAs growths. The silicon doping cell temperature used in these experiments corresponds to a doping cell temperature that produces a 1×10^{19} cm^{-3} doping level in InP lattice-matched InGaAs grown at a rate of 1.0 μm/hour. No attempts were made during this study to optimize the doping level for maximum conductivity in poly-InAs.

Indium contacts were formed on each of the samples and annealed for 3 minutes at a temperature of 150ºC. Room temperature Hall measurements were then used to determine carrier concentration and mobility for each of the growths. Each sample was also patterned and etched to determine the maximum poly-InAs thicknesses by height profilometry. Plan-view SEM images were used to determine the grain size variation in all samples, and TLM patterns with Ti/Pt/Au contacts were fabricated for most samples to confirm the Hall measurement data. The TLM

measurements were also used to demonstrate that the low contact resistivity of poly-InAs is preserved. Contact resistivity in these samples range from 0.5 $\Omega \cdot \mu m^2$ to 80 $\Omega \cdot \mu m^2$.[9,14]

3.2.2 Polycrystalline InAs: Results and discussion

Four approximately 1300 Å thick poly-InAs samples were grown at different temperatures while maintaining a fixed V-III ratio of 20. The growth temperatures were varied from 430ºC to 490ºC in 20ºC increments. Figure 3.4(a) shows the dependence of each sample's electron concentration and mobility on growth temperature. A highly non-uniform surface morphology is observed by macroscopic inspection of the 490ºC growth sample. After several attempts to improve the growth at 490ºC, it was concluded that the growth temperature is too high to maintain uniform deposition onto the SiN_x templates. The non-uniformity may be due to poor nucleation and/or adhesion onto SiN_x at this temperature. It is noted, however, that the deposition of InAs in the exposed GaAs window is uniform at all growth temperatures including the 490ºC sample.

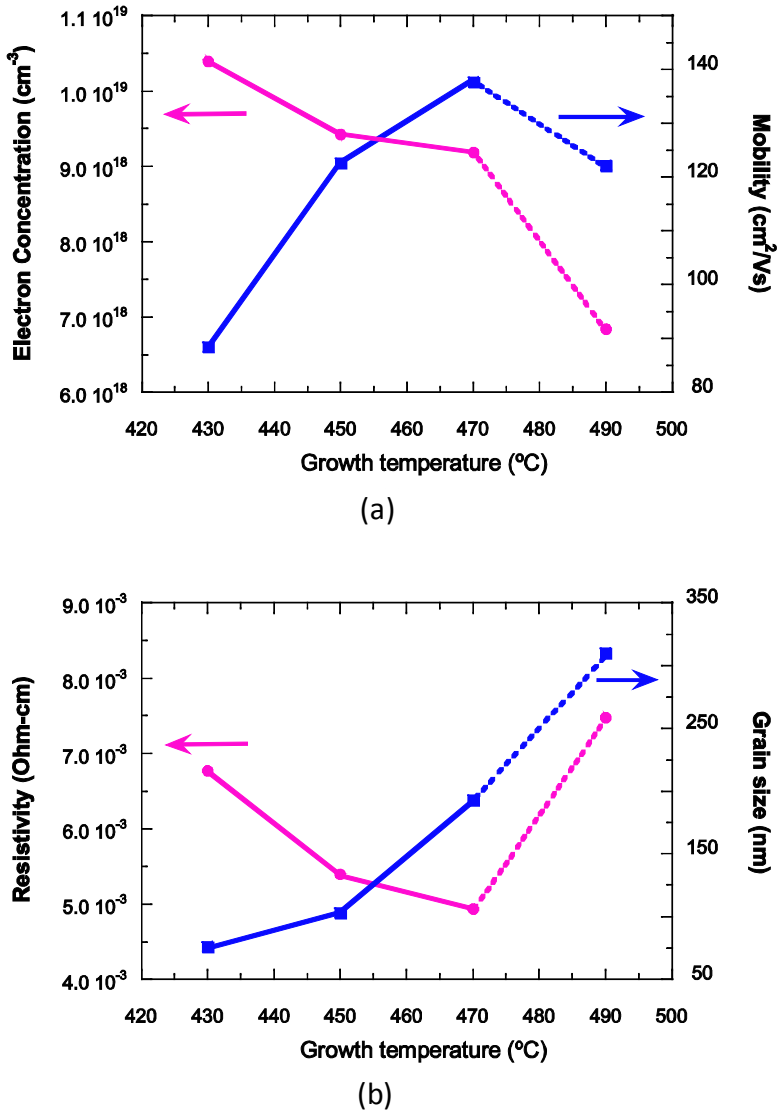


Figure 3.4 Dependence of poly-InAs sample (a) electron concentration and mobility, and (b) resistivity and grain size on growth temperature.

The degradation of growth at 490ºC is also evident in the electrical properties for that sample. For growths between 430ºC and 470ºC we observe a strong dependence of the electron mobility on growth temperature and a weaker effect on the electron concentration. The increased mobility may be attributed to grain size

dependence at the various growth temperatures. Figure 3.5 shows plan-view SEM images for each of the growth temperatures. There is a clear trend toward larger grain size with higher growth temperature. However, there also appears to be a reduction in the density of the crystallites at higher temperatures. The grain density for the 490ºC growth is especially degraded, and we believe this may account for the degradation in mobility despite the large grain size. Shown in Figure 3.4(b) is the grain size and resistivity for all samples versus growth temperature. Grain size is larger when grown

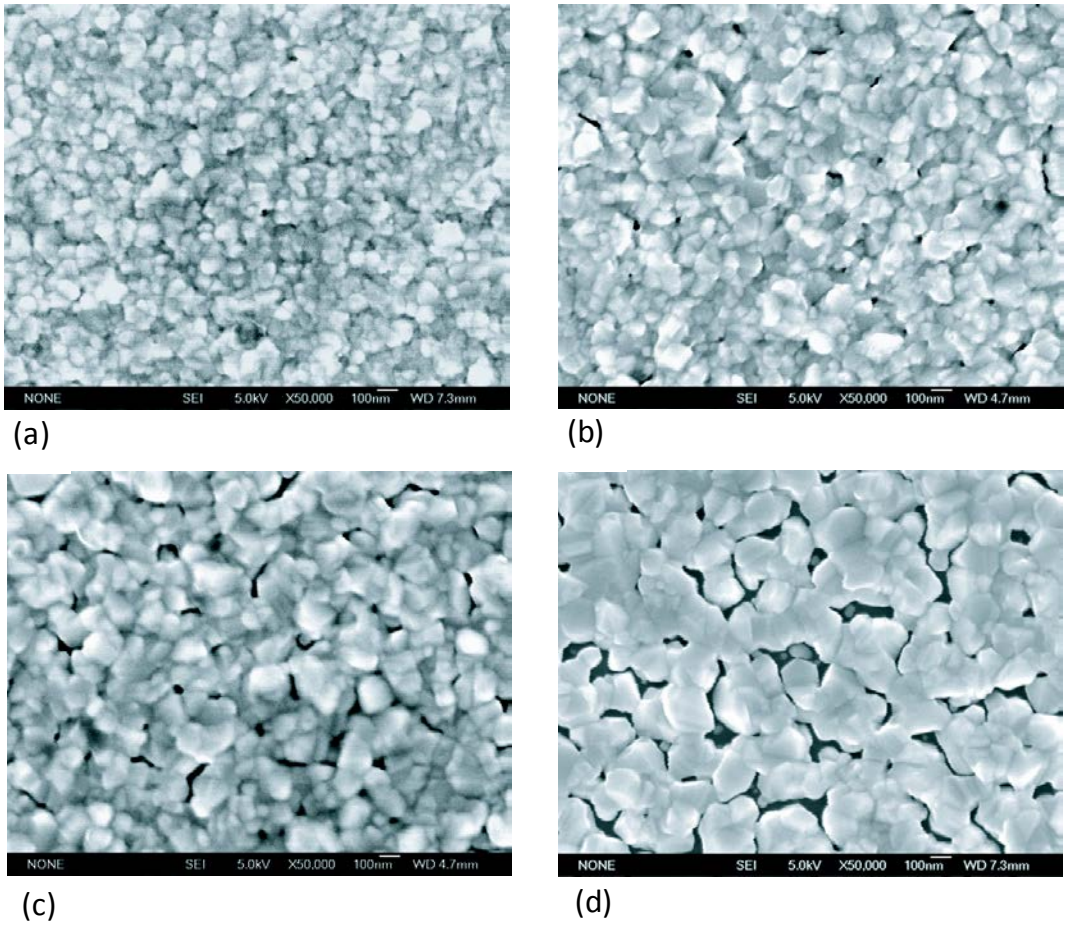


Figure 3.5 Plan-view SEM images of poly-InAs samples grown at temperatures (a) 430ºC, (b) 450ºC, (c) 470ºC, and (d) 490ºC

at higher temperature; ranging from an average of about 75 nm at 430ºC to an average of about 310 nm for the growths at 490ºC. For samples grown at temperatures less than 490ºC, there is a clear trend of resistivity decreasing with increased grain size.

A second set of poly-InAs samples was grown at varying arsenic to indium beam flux ratios ranging from 10 to 40 while maintaining a fixed growth temperature of 470ºC. Figure 3.6 shows the electron concentration and mobility of these samples as a function of V-III ratio. An arsenic to indium ratio of 10 gives poor carrier characteristics that do not follow the trends of the higher V-III ratios. We believe this poor response to be indicative of an As-poor growth region for deposition onto SiN_x. In the remaining samples the electron mobility shows a strong decreasing trend with increased V-III ratio. A study of InAs growth on GaAs by MBE has shown that growth carried out under conditions leading to In-stable reconstruction results in higher quality bulk InAs material.[15,16] This finding suggests that lower arsenic to indium ratio will produce InAs crystallites that are closer to stoichiometric, and this accounts for the higher mobility at lower V-III ratios. In this set of samples it is found that the change in V-III ratio does not significantly affect the electron concentration. The dependence of grain size on V-III ratio is also weak.

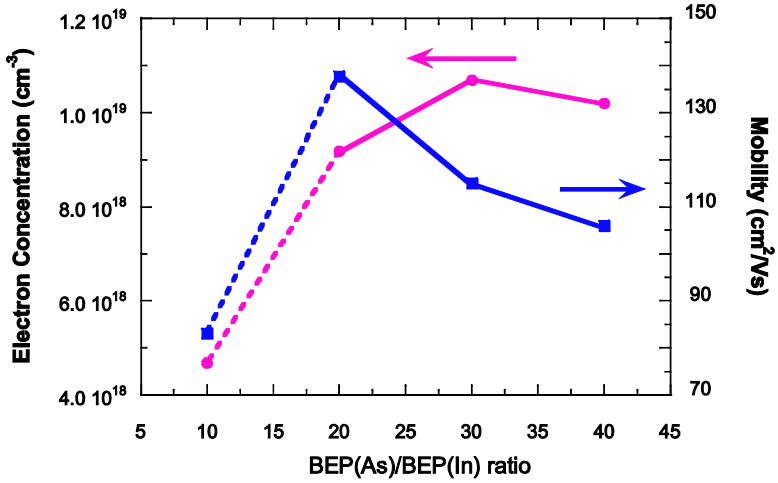


Figure 3.6 Dependence of electron concentration and mobility of poly-InAs on V-III ratio.

A third set of poly-InAs samples was grown with maximum film thickness varying from 750 Å to 3200 Å at a growth temperature of 470ºC. Figure 3.7(a) shows the variation in resistivity and grain size as a function of film thickness. The resistivity of the poly-InAs has a strong dependence on the maximum film thickness with lower resistivity at higher thicknesses. Consequently, the sheet resistivity is not proportional to the reciprocal of film thickness as in monocrystalline material. Instead, the resistivity decreases rapidly as the thickness approaches 1300 Å. It then follows a strong, but less aggressive dependence as thickness increases. Figure 3.7(b) shows that the electron concentration is also not weakly dependent on the film thickness. However, the shape of the resistivity versus thickness curve can be attributed mostly to the increase in mobility. This is an interesting observation as the polycrystalline grain size is shown to be somewhat linear in Figure 3.7(a). The effect of both the crystallite size and the density may contribute to the nonlinear mobility at

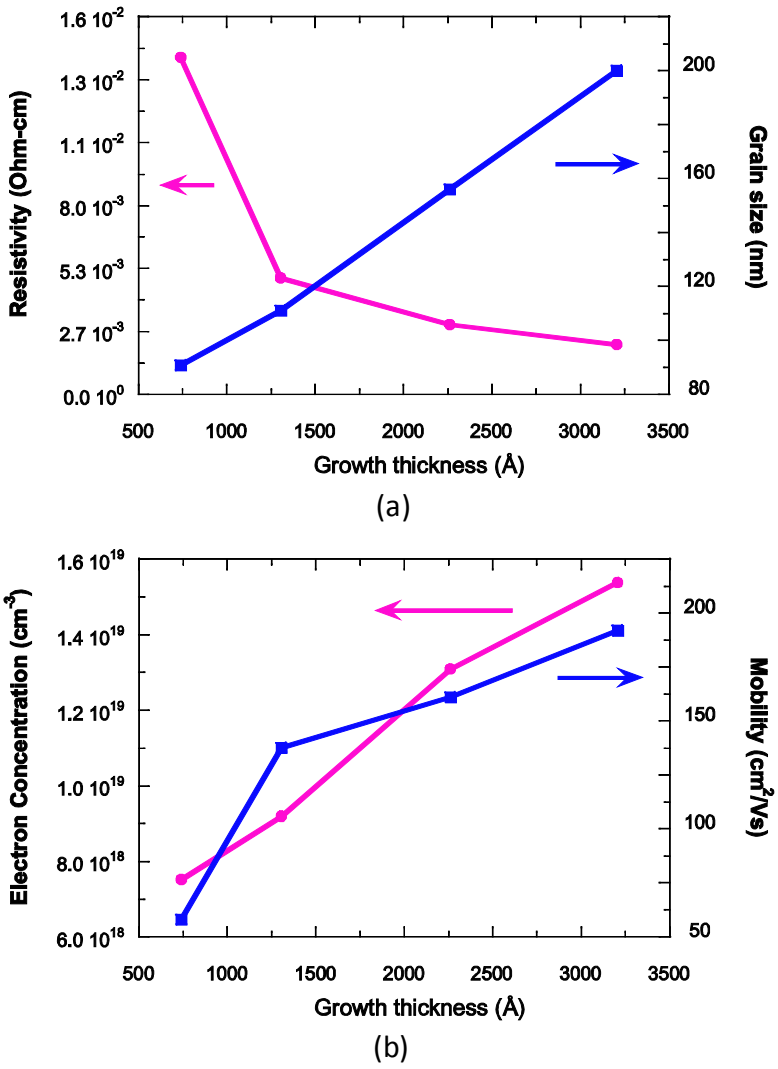


Figure 3.7 Dependence of poly-InAs sample (a) resistivity and grain size, and (b) electron concentration and mobility on thickness.

lower film thickness. Although the grain size follows a nearly linear relation to growth thickness, it can be seen in Figure 3.8 that the density of the crystallites is also increasing. The density increases until the grain size is comparable to the thickness of the growth. With increased thickness the mobility follows a somewhat linear relationship to maximum growth thickness. Based on the plan view SEM images, we

suspect that the thinner depositions, especially the 730 Å film, may be non-continuous films. Hall mobility and carrier density measurements cannot be well applied to a non-continuous film, and a non-continuous film would account for the observed variations at lower film thickness.

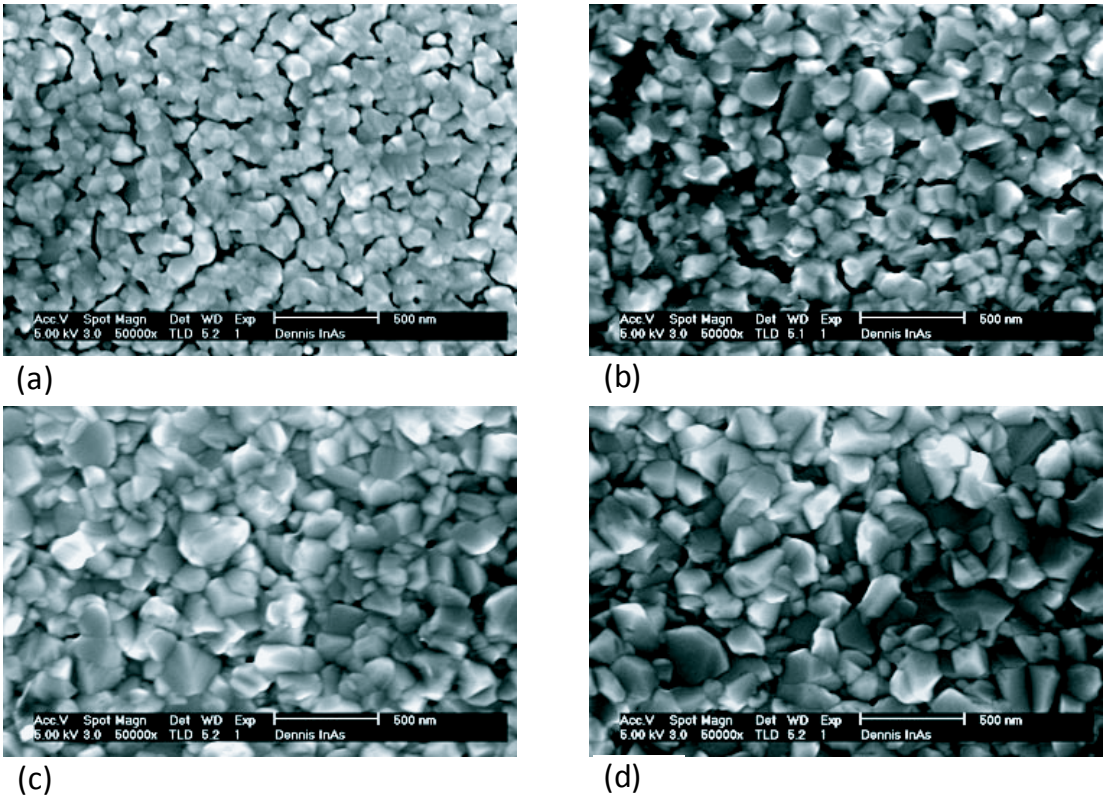


Figure 3.8 Plan-view SEM images of poly-InAs samples thicknesses of (a) 730 Å, (b) 1300 Å, (c) 2250 Å, and (d) 3200 Å.

Cross-sectional SEM images were used to examine the continuity of the poly-InAs at the various growth thicknesses. It was observed that the thickness measurements determined by step profilometry are representative only of the maximum film thickness. The difference between the minimum and maximum

thickness is at least 500 Å in all of the samples. A cross-section of the 3200 Å film is shown in Figure 3.9. Measurements show the highest and lowest points of the film as well as the thickness of the underlying SiN_x layer. The 500 Å deviation from maximum film thickness is most apparent in the Hall data for the 730 Å sample, and the effect of the variation becomes less significant as the thickness increases.

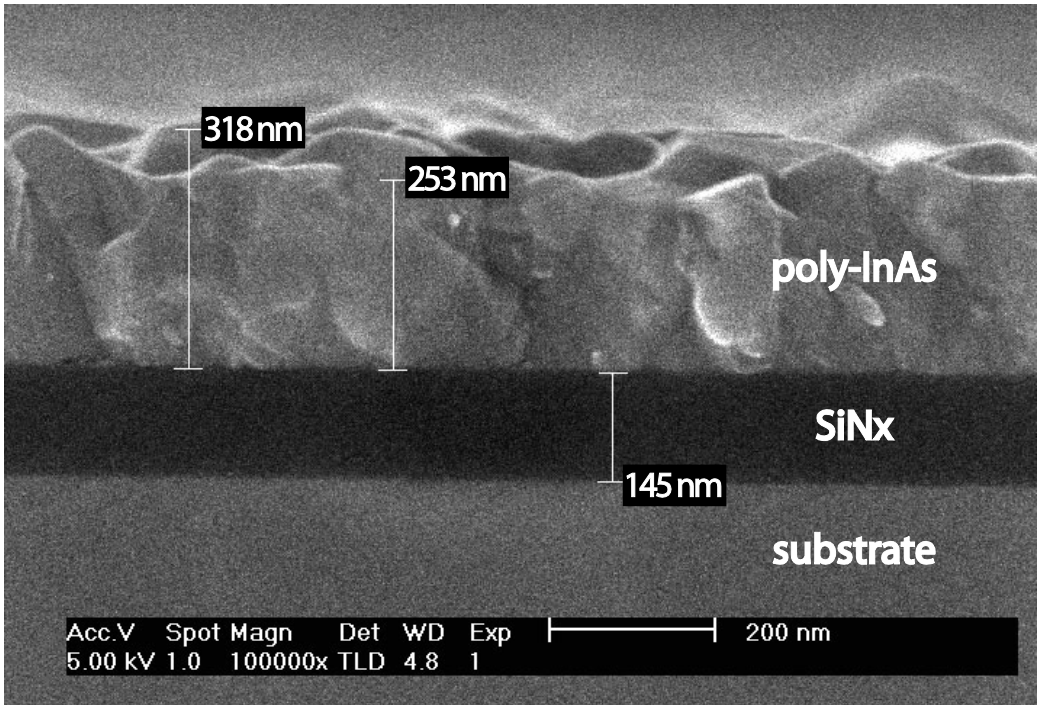


Figure 3.9 Cross-section SEM of 3200 Å poly-InAs sample showing variation in thickness.

[1] M. Takagi, K. Nakayama, C. Terada, and H. Kamioka, "Improvement of Shallow Base Transistor Technology by Using a Doped Poly-Silicon Diffusion Source," *J. Jpn. Soc. Appl. Phys. (Suppl.)* vol.42, pp. 101-109, 1973.

[2] Washio, K.; Kondo, M.; Ohue, E.; Oda, K.; Hayami, R.; Tanabe, M.; Shimamto, H.; Harada, T.; , "A 0.2-μm self-aligned selective-epitaxial-growth SiGe HBT featuring 107-GHz f_{max} and 6.7-ps ECL," *Electron Devices, IEEE Transactions on* , vol.48, no.9, pp. 1989-1994, Sep 2001.

[3] Nakamura, T.; Miyazaki, T.; Takahashi, S.; Kure, T.; Okabe, T.; Nagata, M., "Self-aligned transistor with sidewall base electrode," *Electron Devices, IEEE Transactions on* , vol.29, no.4, pp. 596- 600, Apr 1982.

[4] Jeng, S.J.; Jagannathan, B.; Rieh, J.-S.; Johnson, J.; Schonenberg, K.T.; Greenberg, D.; Stricker, A.; Chen, H.; Khater, M.; Ahlgren, D.; Freeman, G.; Stein, K.; Subbanna, S. , "A 210-GHz f_T SiGe HBT with a non-self-aligned structure ," *Electron Device Letters, IEEE*, vol.22, no.11, pp.542-544, Nov 2001.

[5] Jagannathan, B.; Khater, M.; Pagette, F.; Rieh, J.-S.; Angell, D.; Chen, H.; Florkey, J.; Golan, F.; Greenberg, D.R.; Groves, R.; Jeng, S.J.; Johnson, J.; Mengistu, E.; Schonenberg, K.T.; Schnabel, C.M.; Smith, P.; Stricker, A.; Ahlgren, D.; Freeman, G.; Stein, K.; Subbanna, S. , "Self-aligned SiGe NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," *Electron Device Letters, IEEE*, vol.23, no.5, pp.258-260, May 2002.

[6] Rieh, J.-S.; Jagannathan, B.; Chen, H.; Schonenberg, K.T.; Angell, D.; Chinthakindi, A.; Florkey, J.; Golan, F.; Greenberg, D.; Jeng, S.-J.; Khater, M.; Pagette, F.; Schnabel, C.; Smith, P.; Stricker, A.; Vaed, K.; Volant, R.; Ahlgren, D.; Freeman, G.; Stein, K.; Subbanna, S. , "SiGe HBTs with cut-off frequency of 350 GHz," *Electron Devices Meeting, 2002. IEDM '02. Digest. International*, pp. 771-774, 2002.

[7] Washio, K.; Ohue, E.; Hayami, R.; Kodama, A.; Shimamoto, H.; Miura, M.; Oda, K.; Suzumura, I.; Tominari, T.; Hashimoto, T.;, "Ultra-high-speed scaled-down self-aligned SEG SiGe HBTs," *Electron Devices Meeting, 2002. IEDM '02. Digest. International*, pp. 767- 770, 2002.

[8] Scott, D.; Xing, H.; Krishnan, S.; Urteaga, M.; Parthasarathy, N.; Rodwell, M., "InAlAs/InGaAs/InP DHBTs with polycrystalline InAs extrinsic emitter regrowth," *Device Research Conference, 2002. 60th DRC. Conference Digest*, pp. 171- 172, 2002.

[9] Wei, Y.; Scott, D.W.; Yingda Dong; Gossard, A.C.; Rodwell, M.J., "A 160-GHz f_T and 140-GHz f_{MAX} submicrometer InP DHBT in MBE regrown-emitter technology," *Electron Device Letters, IEEE*, vol.25, no.5, pp. 232- 234, May 2004.

[10] Fu, S.L.; Park, S.; Hsin, Y.M.; Ho, M.C.; Chin, T.P.; Yu, P.L.; Tu, C.W.; Asbeck, P.M., "GaInP/GaAs HBTs with selectively regrown emitter and wide bandgap extrinsic base," *Device Research Conference, 1994. 52nd Annual*, pp.91-92, 1994

[11] Park, S.H.; Chin, T.P.; Liu, Q.Z.; Fu, S.L.; Nakamura, T.; Yu, P.K.L.; Asbeck, P.M., "Submicron self-aligned HBT's by selective emitter regrowth," *Electron Device Letters, IEEE*, vol.19, no.4, pp.118-120, Apr 1998.

[12] Spitzer, W. G.; Mead, C. A., "Barrier Height Studies on Metal-Semiconductor Systems,"*Journal of Applied Physics*, vol.34, no.10, pp.3061-3069, Oct 1963.

[13] Mead, C. A.; Spitzer, W. G., "Fermi Level Position at Metal-Semiconductor Interfaces," *Phys. Rev.*, vol.134, A713, 1964.

[14] Scott, D.; Urteaga, M.; Parthasarathy, N.; English, J.H.; Rodwell, M.J.W., "Molecular beam deposition of low-resistance polycrystalline InAs," *High Performance Devices, 2002. Proceedings. IEEE Lester Eastman Conference on*, pp. 207- 212, 6-8 Aug. 2002.

[15] Schaffer, W. J.; Lind, M. D.; Kowalczyk, S. P.; Grant, R. W., "Nucleation and strain relaxation at the InAs/GaAs(100) heterojunction," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol.1, no.3, pp.688-695, Jul 1983.

[16] Hancock, Bruce R.; Kroemer, Herbert, "Relation between growth conditions and reconstruction on InAs during molecular beam epitaxy using an As_2 source," *Journal of Applied Physics*, vol.55, no.12, pp.4239-4243, Jun 1984.

Chapter 4

Regrown Emitter HBTs

4.1 Motivation for Regrown Emitter HBTs

The development and evolution of HBTs with MBE regrown base-emitter junctions is described in this chapter. These HBTs are the first demonstrations of an HBT utilizing non-selective regrowth to form the active base-emitter heterojunction. The regrown emitter HBT utilizes the low-resistivity polycrystalline InAs described in the previous chapter as an extrinsic emitter with very low-resistivity contact. The emitter contact area is also much wider than the base-emitter junction, facilitating low emitter resistance. The emitter regrowth eliminates the need to form the base-emitter junction by etching and self-aligned metal liftoff, processes that may reduce yield at deep submicron dimensions. This work was intended as a first step to parallel the highly scaled, high integration, low parasitic, and high-yield aspects of Si/SiGe bipolar transistors.

Details and performance results for III-V HBTs and Si/SiGe transistors have been covered in previous chapters. The main advantages of III-V HBTs over Si/SiGe transistors are in the material properties. The primary disadvantage is the immaturity

of III-V fabrication technology and device structure relative to the silicon counterparts. Despite the superior material properties of III-V HBTs, Si/SiGe HBT RF performance remains highly competitive. Silicon is able to remain competitive due to the aggressive device scaling and parasitic reduction allowed by the fabrication technology and device structure. The low-resistance polysilicon emitter contact used in SiGe is much wider than the active emitter junction allowing the emitter resistance to remain low while shrinking the active junction area. Emitter regrowth in Si/SiGe HBTs also allows for deep submicron emitter widths while maintaining high yield. Conventional III-V mesa HBTs would suffer from emitter contact resistance if the emitter metal were scaled to dimensions as small as those used in Si/SiGe HBTs. It may also be difficult to reliably produce base-emitter junctions using the etching processes conventional to III-V HBTs if dimensions similar to those used in Si/SiGe HBTs were attempted. By following the method of emitter regrowth used in Si/SiGe HBTs, we hope to circumvent potential fabrication issues and device parasitic degradation without compromising the superior materials aspects found in III-V HBTs.

4.2 Initial Development of Regrown Emitter HBTs

The initial work on regrown emitter HBTs began with the development of low-resistance poly-InAs as detailed in the previous chapter. As shown in Figure 4.1, the n-type doping levels attainable in poly-InAs are comparable to those attainable in crystalline InGaAs lattice matched to InP as described in Chapter 2. The doping and mobility for Si-doped bulk InAs grown on a SiN_x substrate are 1.3×10^{19} cm^{-3} and 620

$cm^2/V•s$, respectively. The mobility for crystalline InGaAs Si-doped at 1.0×10^{19} cm^{-3} is 2200 $cm^2/V•s$. Although the doping-mobility product of this initial poly-InAs on SiN is still three times lower than that of crystalline InGaAs, the ability to create a device with a regrown emitter area much larger than the base-emitter junction presents potential opportunities for lowering emitter resistance.

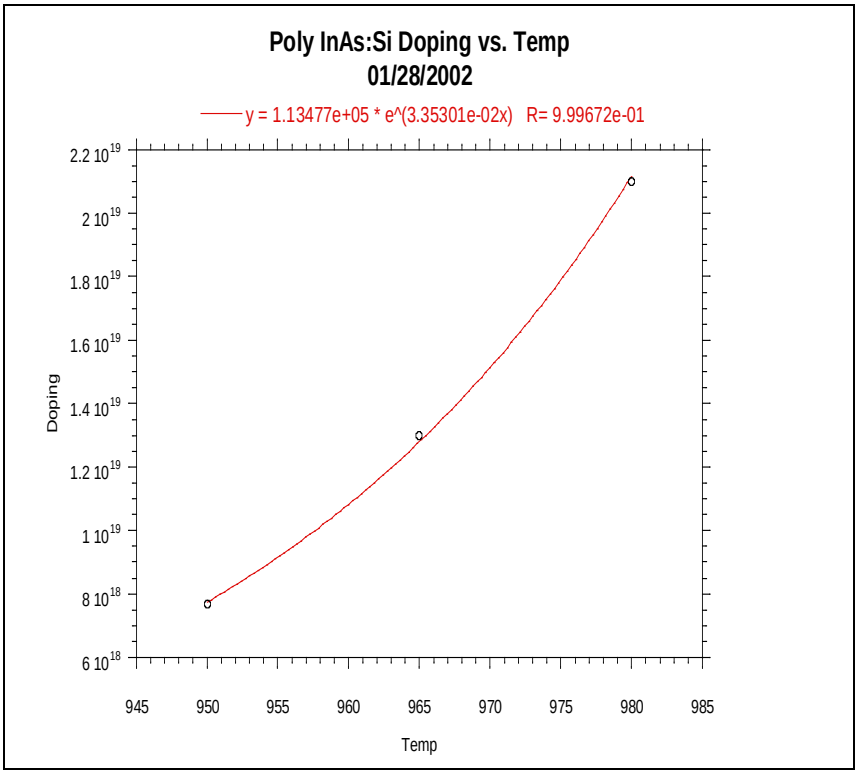


Figure 4.1 Low resistance poly-InAs doping vs. temperature

A simple HBT mask layout and fabrication process was developed to demonstrate the DC characteristics of an HBT with regrown emitter. This simplified process flow and mask set is referred to as the RGQAD (regrown quick and dirty) HBT. The HBT structure and fabrication begins with a patterned base-collector

template onto which the emitter will be grown. The base-collector template is grown by MBE on a 2-inch semi-insulating InP substrate. The template consists of a 2500Å InGaAs n+ subcollector, 1200Å n- InP collector, 300Å n- base-collector grade and undoped setback, 400Å p+ InGaAs base, 80Å InP p+ etch stop, and 520Å p+ InGaAs cap. Silicon is the n-type dopant, carbon is the p-type dopant for InGaAs, and beryllium is the p-type dopant for InP. The 520Å InGaAs cap is intended as an extrinsic base contact layer to help reduce base access resistance along the length of the HBT. A cross-section schematic of the base-collector template as-grown and after fabrication is shown in Figure 4.2.

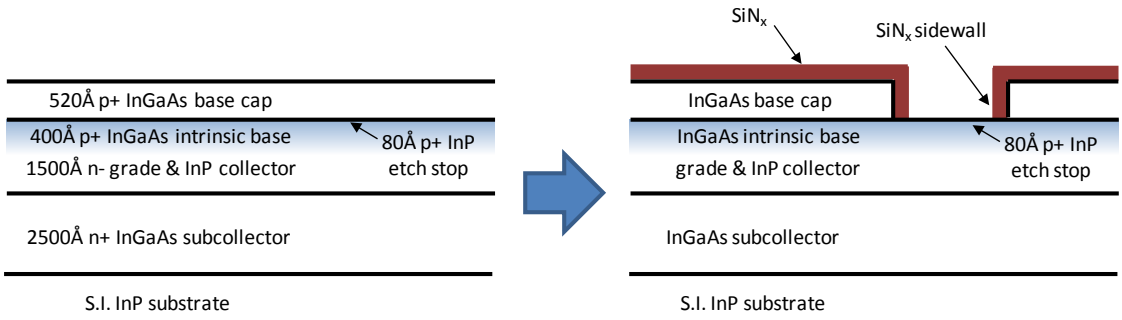


Figure 4.2 Cross-section schematic of the base-collector template as-grown (left), and after fabrication in preparation for emitter regrowth (right).

The fabrication process begins with the deposition of PECVD SiN_x onto the template wafer. The SiN_x deposition temperature is typically less than 300ºC. Regrowth areas with emitters on the RGQAD mask as small as $1 \times 15\ \mu m^2$ are defined by optical lithography, and the SiN_x is removed from the emitter regrowth areas by reactive ion etch (RIE) dry plasma etching. The 520Å InGaAs base cap layer in the regrowth area is removed using a dilute citric acid and peroxide wet etchant that

selectively stops at the 80Å InP etch stop. SiN_x sidewalls are then formed on the InGaAs sidewalls in the etched openings, and the InP etch stop layer is removed using HCl-based wet etchant before emitter regrowth.

MBE is used to grow the emitter layers onto the patterned base-collector template. As stated, the 80Å InP etch stop is removed immediately prior to loading the fabricated base-collector template wafers into the MBE loading chamber using a selective HCl-based wet etchant that stops on the 400Å InGaAs base layer. The intention is to maintain the InGaAs base regrowth surface in a pristine condition until the template is ready for introduction into the MBE vacuum. Once loaded into the growth chamber, the SiN_x coated base-collector template is heated to a temperature setting of 400ºC for a minimum of 10 minutes. An increase in the growth chamber's background pressure is typically observed due to heating and out-gassing from the wafer block and CAR. The pressure increase for a base-collector template is greater than what is normally observed, and this is attributed to hydrogen escaping from the PECVD-deposited SiN_x. The growth chamber's background pressure is allowed to stabilize before turning the wafer to the growth position, applying an As overpressure, and slowly heating the wafers to a 530ºC pyrometer reading on the wafer's surface. The wafer temperature is then lowered to 480ºC for the emitter growth, and the emitter deposition commences. The emitter epitaxial stack consists of a 200Å InGaAs/InAlAs n- grade, 600Å InAlAs n- emitter, 500Å InAlAs n+ emitter, and 1000Å heavily doped InAs cap. Regrowth of the emitter material in the semiconductor areas is intended to be mono crystalline. Regrowth on the SiN_x surface is expected to be polycrystalline.

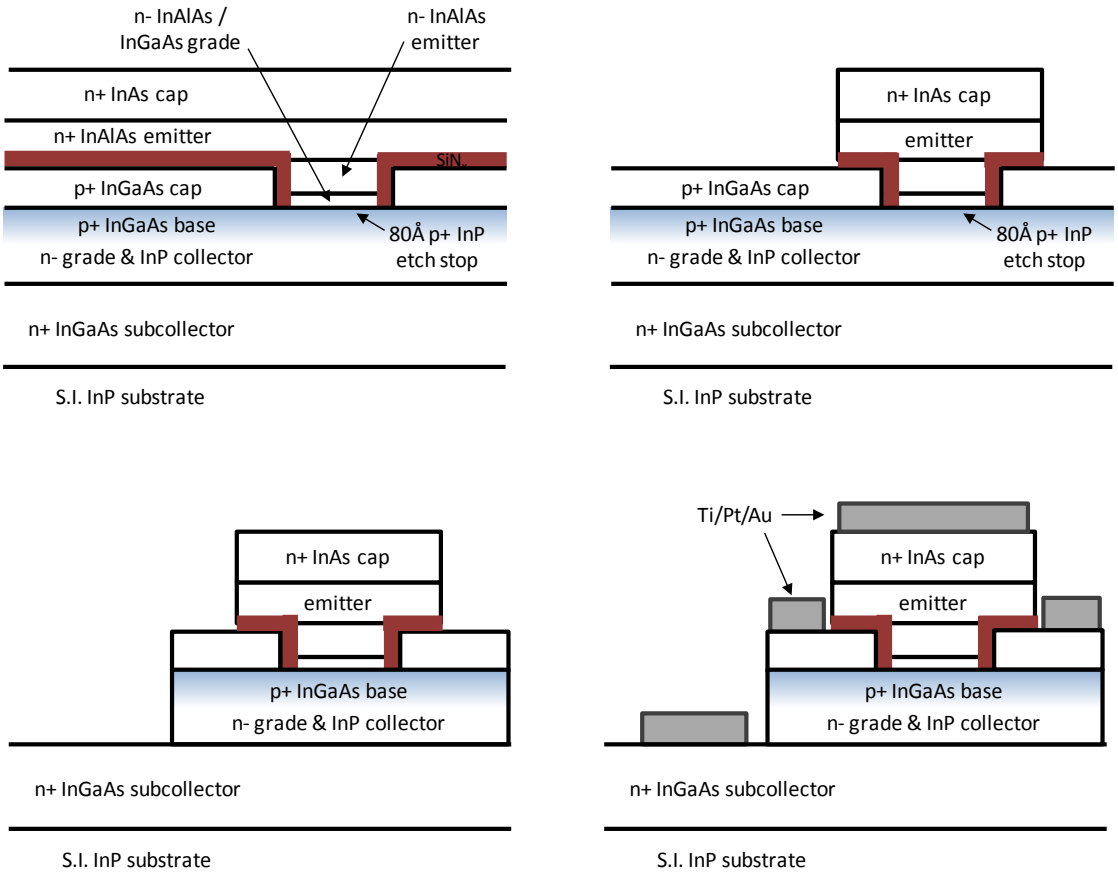


Figure 4.3 RGQAD large-area regrown emitter HBT fabrication process summary.

A summary of the simplified RGQAD fabrication process is shown in Figure 4.3. After emitter growth, large-area contacts are patterned and wet etched from the regrowth stack stopping on the SiN_x. The SiN_x that is not underneath the patterned areas is then removed by HF-based etchant, and a majority of the wafer's exposed surface is now the base cap material. The base stack and collector are then patterned and selectively wet etched to the subcollector surface, and a metal layer is patterned and evaporated onto the HBT mesas. In the RGQAD process, a Ti/Pt/Au metal stack is simultaneously deposited on the emitter, base, and subcollector followed by metal

lift-off and photoresist strip. A top-down microscope image of the RGQAD device array and regrown emitter HBT is shown in Figure 4.4 below.

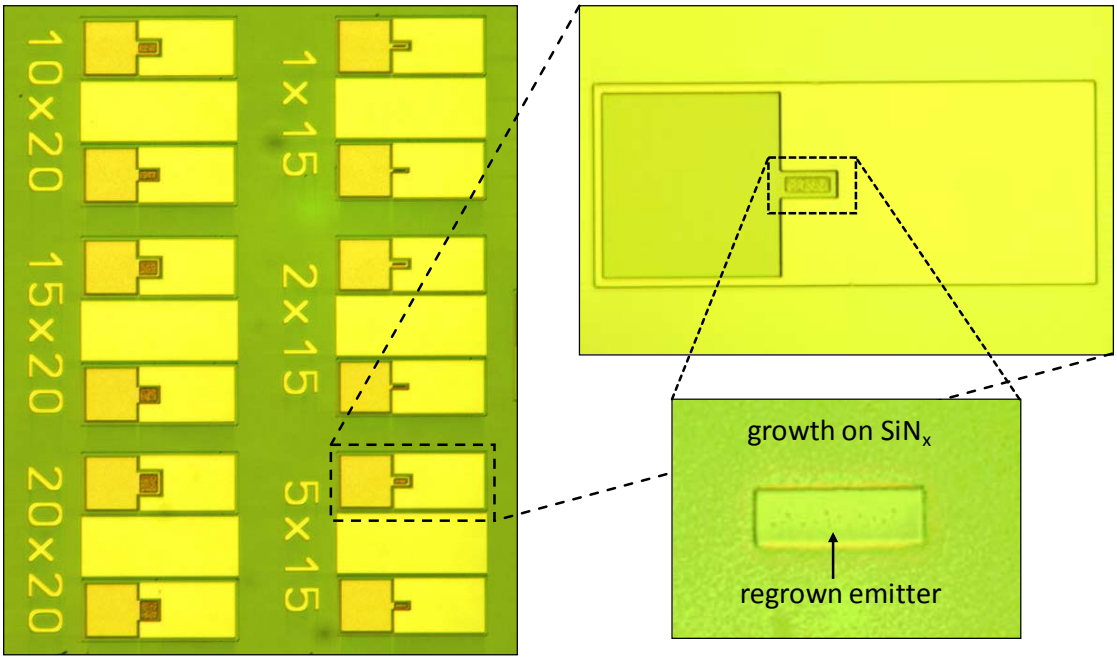


Figure 4.4 Top-down miscroscope image of a 5 × 15 μm^2 regrown emitter HBT in the RGQAD device array (left) and details of the device and regrowth area (right).

In the first emitter regrowth attempt, the emitter areas were patterned and etched onto the base-collector template wafer and the emitter regrowth was performed with the remaining wafer surface covered in SiN_x. During MBE regrowth, the SiN_x-covered surface presents an emissivity offset in the pyrometer temperature reading that is not consistent with the actual temperature of the wafer's semiconductor surface. Therefore, the first regrown emitter HBT was grown under non-optimal temperature conditions. This problem was remedied in subsequent growths by removing a 1 cm^2 area of the SiN_x from the 2-inch base-collector template wafer prior to regrowth.

Removing the SiN_x near the center of the wafer exposes the underlying semiconductor surface allowing for verification of RHEED patterns and accurate readings of wafer temperature from the pyrometer. Shown in Figure 4.5 are emitter regrowth areas from the first growth without accurate pyrometer readings and the second growth where the semiconductor at the center of the template wafer was exposed allowing for accurate pyrometer feedback.

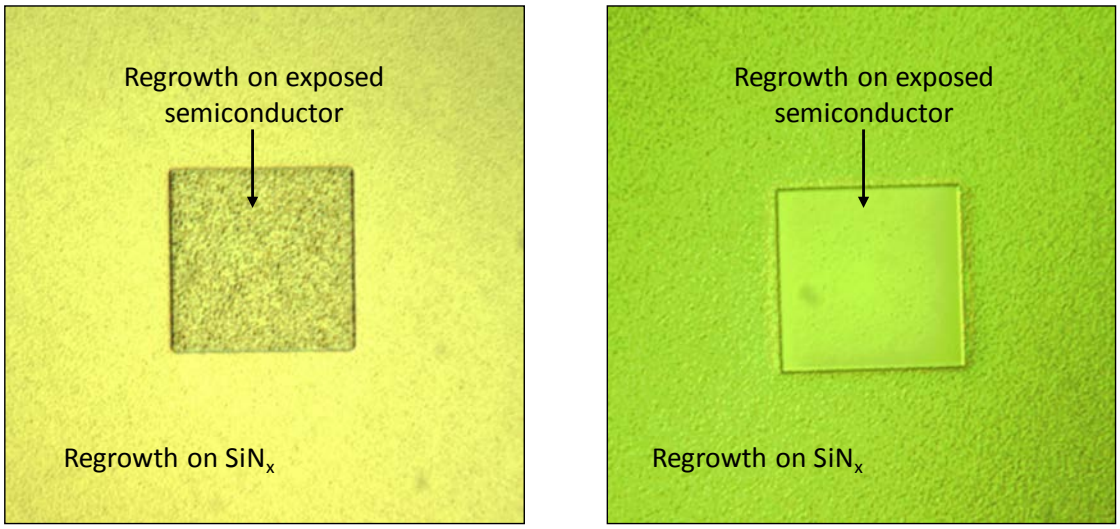


Figure 4.5 Microscope image from (left) emitter regrowth without accurate pyrometer readings during MBE growth, and (right) regrowth with proper pyrometer feedback.

The improvement in crystal regrowth quality between the first and second attempts is also observed in the SEM cross-sections shown in Figure 4.6. The cross-section images each show regrowth on SiN_x and on bare semiconductor areas. The image on the left shows the first growth attempt where SiN_x covered most of the wafer and the emitter was grown under non-optimal temperature conditions. The image on

the right shows the regrowth where the SiN_x was removed from the center of the wafer to allow for RHEED verification prior to growth and accurate pyrometer readings.

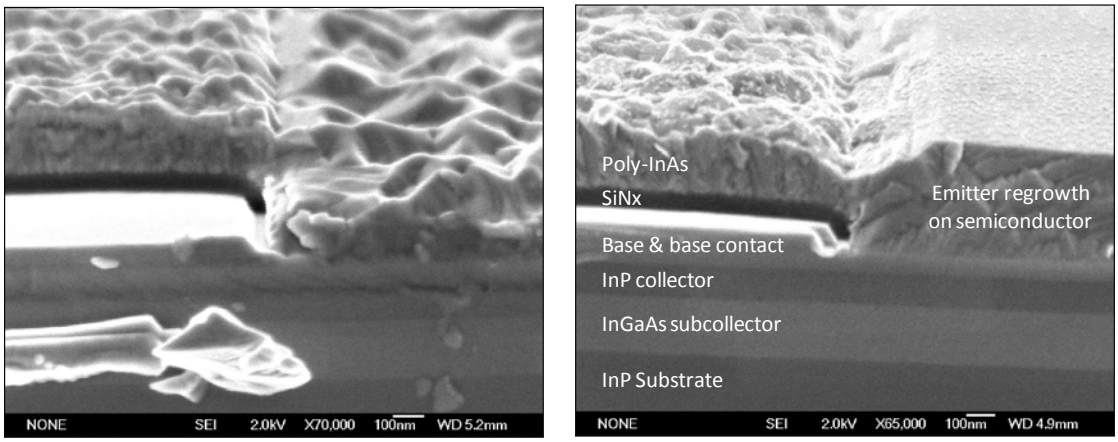


Figure 4.6 SEM cross-section images from (left) emitter regrowth without accurate pyrometer readings during MBE growth, and (right) regrowth with proper pyrometer feedback.

4.2.1 Initial DC results

Figure 4.7 shows the common-emitter I.V. and Gummel characteristics for one of the first regrown emitter HBTs with 0.8 × 15 μm^2 emitter area. This HBT had the etched RHEED verification window on the base-collector template, and was grown at the proper temperature. Although the as-drawn emitter width on the mask is 1 μm, the fabricated emitter growth area after is found to be narrower. The common-emitter current gain β is greater than 20, the collector-emitter breakdown voltage BV_{CEO} is above 3.5V, and the offset voltage is about 0.15V. The dip in the common-emitter I.V. collector current is attributed to a growth error in the base-collector template. As shown in Figure 4.8, the delta doping layer in the digital base-collector grade was insufficient to prevent current blocking at a moderate current density. By increasing

the doping of the delta-doped layer between the base-collector grade and the lightly-doped InP collector, the conduction band is pulled down at the grade-collector junction and the onset of current blocking is delayed. Also noted in the Gummel characteristic of Figure 4.7 is the high crossover between the base and collector currents. The high crossover generally indicates a poor quality base-emitter junction. The result is not surprising in this initial attempt at a regrown base-emitter junction, and further effort is required to to improve the quality of the junction.

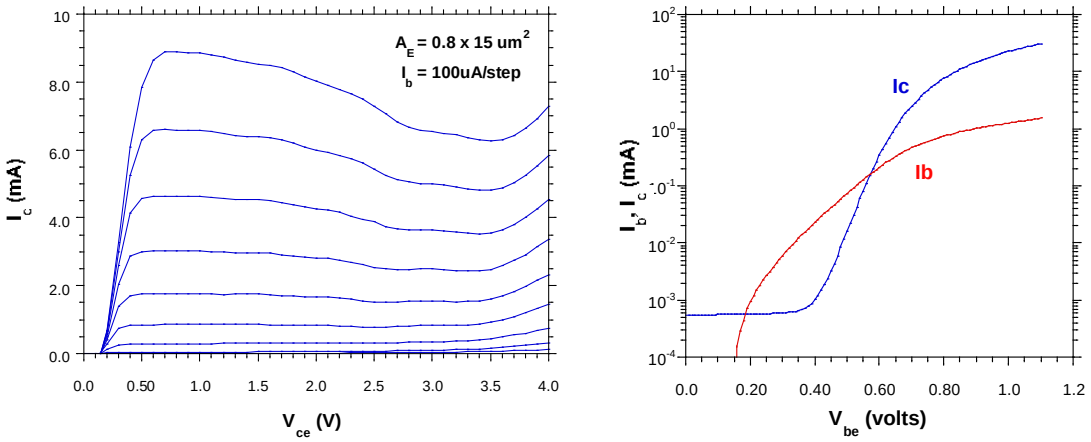


Figure 4.7 Common-emitter I.V. and Gummel characteristics for first generation 0.8 × 15 μm^2 regrown emitter HBT with β > 20.

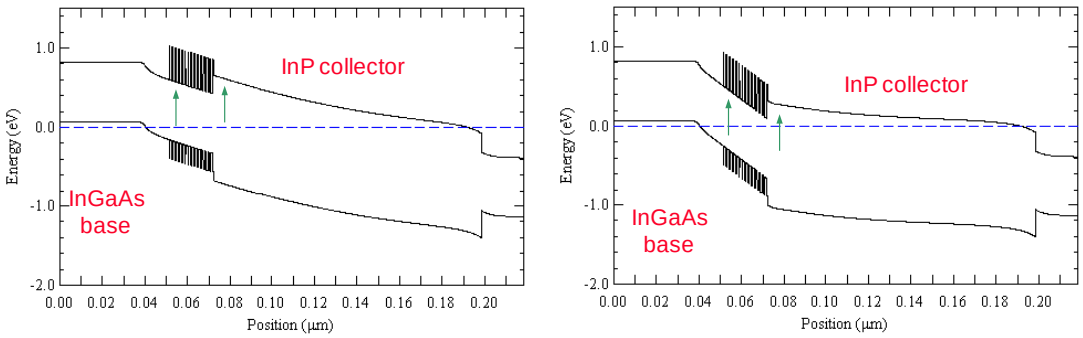


Figure 4.8 (left) Band diagram showing incorrect base-collector grade that accounts for current blocking seen in the common-emitter curve above. (right) Band diagram showing corrected base-collector grade. A thin, heavily-doped layer was inserted between the base-collector grade and collector to pull the conduction band down at the grade-collector junction.

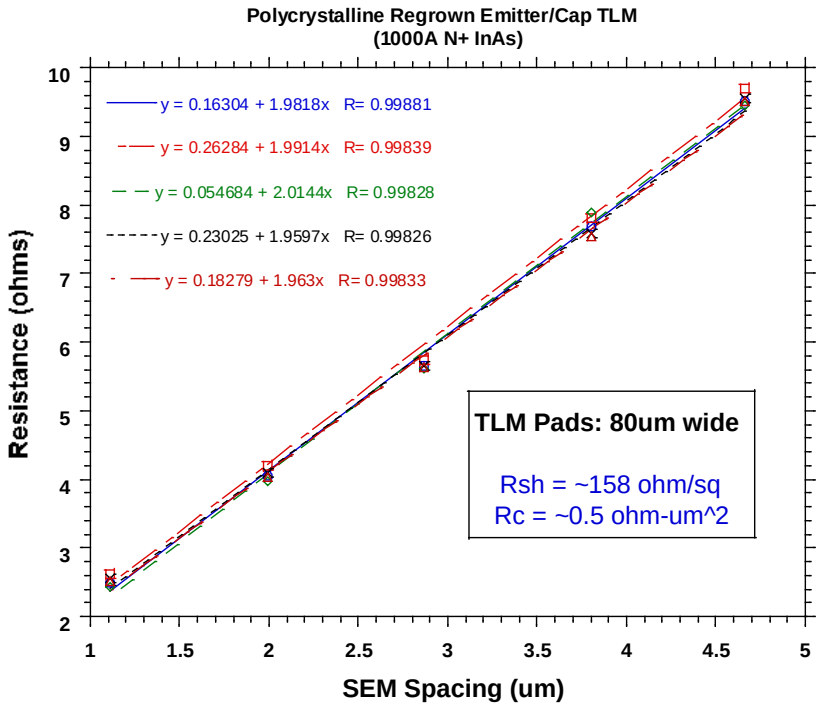


Figure 4.9 RGQAD polycrystalline emitter cap TLM measurements

Included on the RGQAD mask set are TLM patterns for the polycrystalline emitter material and the base cap/InP etch stop/base layers of the template. The TLM pads are 80 µm wide, and the 1.1 µm to 4.6 µm spacings have been measured by SEM. Shown in Figure 4.9 are the TLM measurements for the poly-InAs and emitter growth on SiN_x. As expected, the poly-InAs contact resistance is very low and the emitter cap sheet resistance is 158 Ω/sq. Additionally, it is observed that poly-InAs grown on poly-InAlAs emitter material has lower resistivity than poly-InAs grown directly on SiN_x. As shown in Table 4.1, the resistivity of poly-InAs grown directly on SiN_x is higher than poly-InAs grown on a 1000 Å thick layer of poly-InAlAs. Attempts to measure doping and mobility of Si-doped poly-InAlAs indicate that the

poly-InAlAs is highly resistive (unmeasurable on our equipment). The poly-InAlAs, therefore, does not contribute to the lower sheet resistance of the poly-InAs. It is assumed that the poly-InAlAs improves surface nucleation for the poly-InAs compared to the conditions seen when poly-InAs is grown directly on SiN_x.

Table 4.1 Variation of doping, mobility and resistivity for 1000 Å poly-InAs versus (a) SiN_x and poly-InAlAs growth surfaces and (b) Si dopant cell temperature are varied

Growth Surface	**Si Dopant Cell Temp (°C)**	**Doping ($\times 10^{19}$ cm^{-3})**	**Mobility (cm^2/V-s)**	**Resistivity (Ohm·cm)**
SiN_x	1250	2.03	66.4	4.6×10^{-3}
1000Å poly-InAlAs	1250	2.43	84.5	3.0×10^{-3}
SiN_x	1275	2.92	38.2	5.6×10^{-3}
1000Å poly-InAlAs	1275	3.80	58.6	2.8×10^{-3}

The RGQAD base TLM is patterned onto the 520 Å p+ InGaAs cap layer of the base-collector template. Underneath the InGaAs cap layer is 80 Å of p+ InP and 400 Å p+ InGaAs base layer; the crystalline emitter is grown on the 400 Å InGaAs layer after patterning and etching the base-collector template. TLM data for the base contact stack is shown in Figure 4.10. The addition of a p+ InGaAs cap layer on top of the base layer does not reduce the base resistance. Additionally, the contact resistance is at least an order of magnitude higher than expected. It is believed that the 80 Å InP etch stop layer prevents conduction of both InGaAs layers in the TLM pattern as well as skewing the contact resistance measurement.

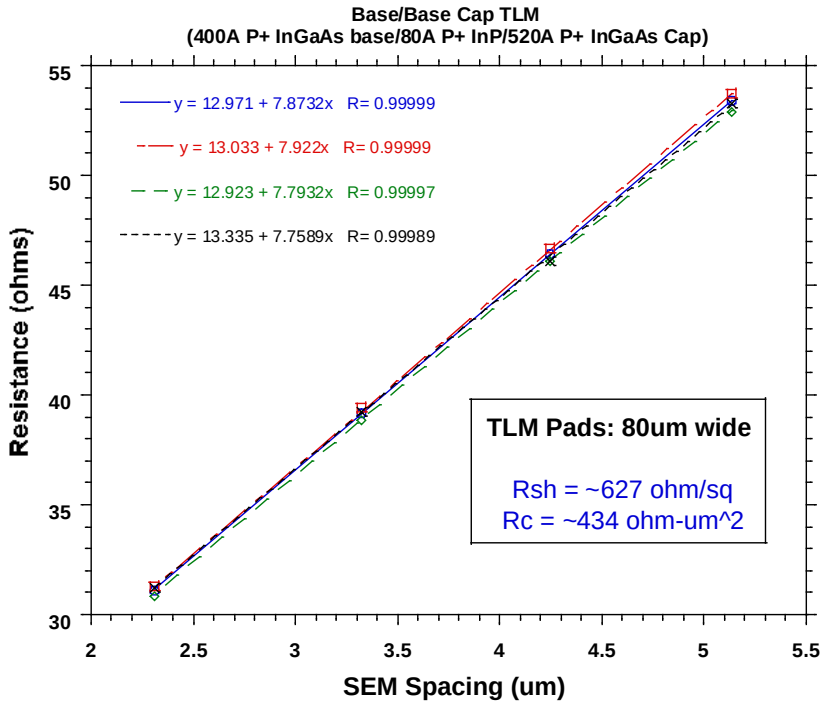


Figure 4.10 RGQAD base and base cap TLM measurements

The 80 Å InP etch stop thickness was arbitrarily chosen during the base-collector template design. This thickness was conservatively chosen to survive the selective citric-based wet etch of the 520 Å InGaAs base cap. After observing the contact resistance data shown above, a small study was conducted to determine the minimum InP thickness required to stop the citric-based wet etch. Three template samples were grown with 60 Å, 40 Å and 20 Å InP layers and the 520 Å InGaAs cap. The samples were patterned with photoresist and then etched with standard citric:H_2O_2:H_3PO_4:DI (50:5:1:200) InGaAs etchant for 90 seconds (standard etch time is 75 seconds). All InP etch stop thicknesses survive the wet etch process, so 20 Å InP etch stops have been used in subsequent base-collector templates.

4.2.2 Initial RF results

The first RF result for a regrown emitter HBT were demonstrated using the non-selective MBE base-emitter junctions described in previous sections. The InAlAs emitter and InAs emitter cap were grown on a base-collector template with a refractory base metal buried beneath the SiN sidewall layer as shown in Figure 4.11. The intention of the buried refractory metal is to reduce base contact resistance by extending the base contact metal underneath the regrown emitter area while allowing for a wide emitter contact to the emitter cap.

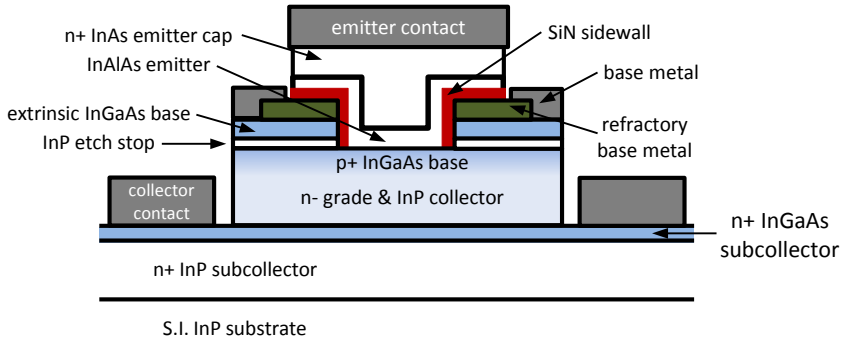


Figure 4.11 Cross-section schematic of regrown emitter HBT with base refractory metal

The base-collector template is grown on an semi-insulating InP substrate. The epitaxial structure consists of 3100 Å InGaAs/InP n+ subcollector, 1100 Å n- InP collector, 400 Å n- grade and undoped setback, 400 Å p+ InGaAs base, 20 Å InP p+ etch stop, and 500 Å InGaAs base contact layer. The InGaAs base and base contact layers are carbon doped while the p-type InP etch stop is beryllium doped.

A 1000 Å Ti/W metal stack is sputtered on the base-collector template, patterned, and dry etched to form the refractory base contact. A 1000 Å layer of

PECVD SiN_x is then deposited onto the wafer, and the emitter-etch windows are lithographically defined in the centers of the refractory base contacts. The emitter etch windows are 0.5, 0.7 and 0.9 μm wide, and lengths of 4 and 8 μm are available. The SiN_x and Ti/W metal stack are RIE etched from the emitter regrowth areas using a single lithography step. After stripping the photoresist, the exposed extrinsic base cap in the emitter regrowth window is selectively etched using citric-based etchant. A second 1000 Å PECVD SiN_x is deposited over the entire wafer to create an insulating layer in the emitter regrowth window that will be used to form the emitter sidewall. Directional RIE etch-back is used to form vertical SiN_x sidewalls in the emitter window. A SiN_x spacer less than 0.1 μm wide is thus formed between the intrinsic emitter and the extrinsic base contact region. After removing the 20 Å InP etch stop using HCl-based etchant, non-selective MBE regrowth is used to deposit a 275 Å base-emitter grade, 600 Å n- InAlAs emitter, 500 Å n+ InAlAs, 500 Å InGaAs and 1500 Å heavily doped InAs. The regrown epitaxy in the exposed intrinsic base region is monocrystalline while deposition on SiN_x is polycrystalline. A Ti/Pt/Au/Pt metal stack is deposited on the emitter regrowth windows using lift-off processes to form the emitter contacts. The excess regrown-emitter material covering the entire wafer with SiN_x underneath is dry-etched by inductively coupled plasma (ICP) and RIE, respectively. The emitter metal acts as an etch mask during this process. To reduce resistance along the length of the device, a self-aligned Ti/Pd/Au metal is evaporated over the exposed portion of the refractory Ti/W contacts. The remaining device fabrication includes device isolation and collector contact deposition. Polyimide is

used as an insulating material, and Au metallization forms the coplanar waveguide wiring. Although polyimide is used in the fabrication process, it is important to note that the base-emitter junction is not defined by an etch process and polyimide is not required for passivation of this junction; passivation is maintained by the SiN_x deposited onto the emitter sidewalls. A focused ion beam (FIB) cross-section of the small-area regrown emitter HBT is shown in Figure 4.12.

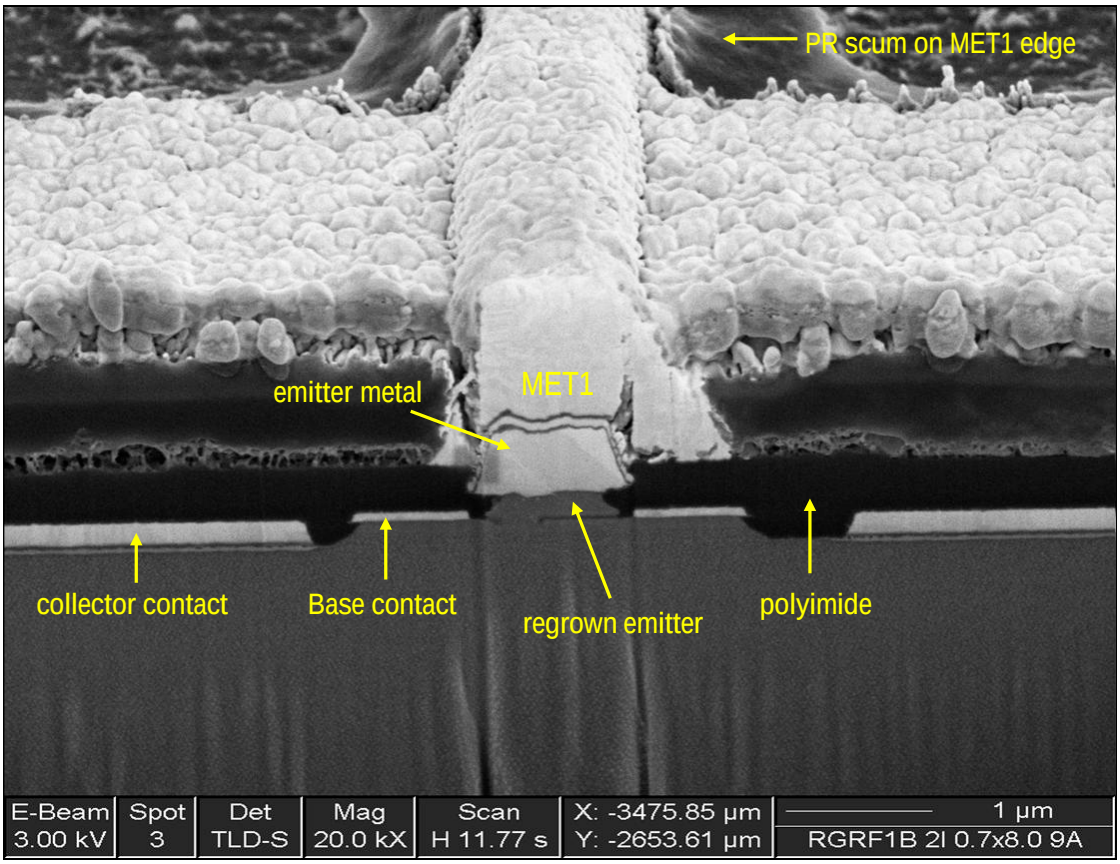


Figure 4.12 FIB cross-section of the small-area regrown emitter HBT

The common-emitter I-V curves for devices with regrown base-emitter junction areas of $0.7 \times 8\ \mu m^2$ and $0.3 \times 4\ \mu m^2$ are shown in Figure 4.13. The emitter

cap contact extends an additional 0.3 μm to each side of the junction and the refractory base has a width of 0.6 μm on each side of the emitter. Collector contacts with 2.7 μm width are spaced 0.5 μm from each side of the base mesa. The base-collector layer structure is designed similar to previous work[1] enabling a maximum emitter current density of 8×10^5 A/cm^2 and a collector breakdown voltage (V_{CEO}) of 6 volts.

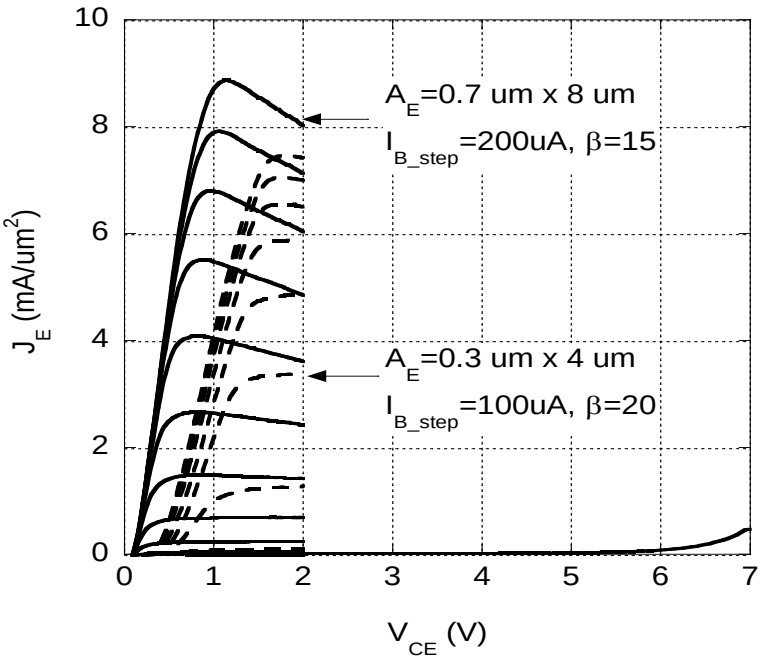


Figure 4.13 Common-emitter I-V curves for regrown-emitter HBTs with $A_E = 0.7 \times 8$ μm^2 and $A_E = 0.3 \times 4$ μm^2

The microwave performance of the 0.7×8 μm^2 device was characterized by on-wafer s-parameter measurements from 5 GHz to 40 GHz using a HP8510C network analyzer. The peak f_τ of 160 GHz and a simultaneous f_{max} of 140 GHz are extracted using 20-dB/decade extrapolation from the plots of h_{21} and Mason's Gain as shown in Figure 4.14. The RF measurement in Figure 4.14 was obtained at a current

density of 4×10^5 A/cm^2 and collector voltage of 1.3 V. Figure 4.14 also shows the maximum stable/available power gain (*MSG/MAG*) and the stability factor (*K*).

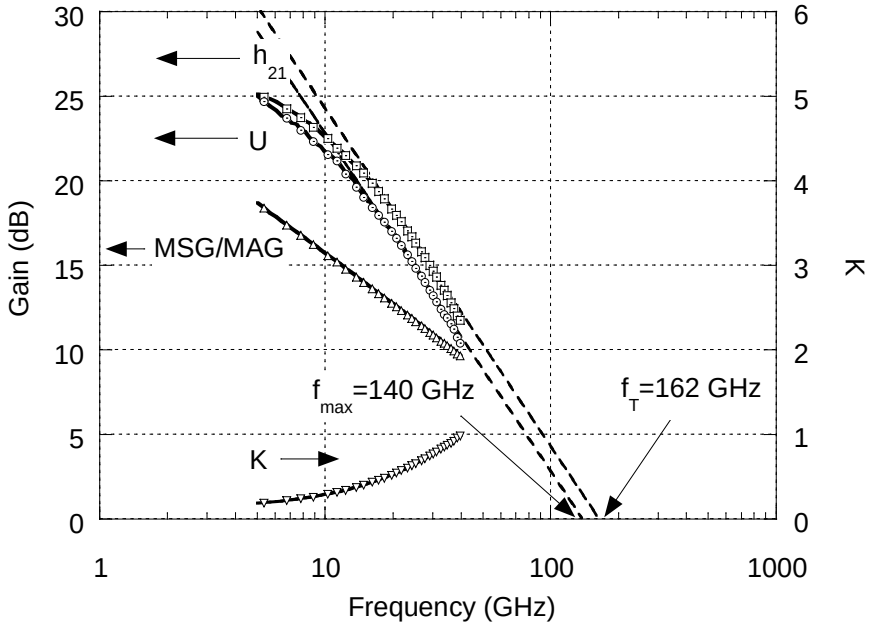


Figure 4.14 First RF gains and stability factor for 0.7×8 μm^2 regrown emitter HBT

Both the DC fly-back measurement and a hybrid-π model extraction demonstrate an emitter contact resistance of 80 Ω-μm^2. This excess emitter resistance substantially degrades the device bandwidth, and is beyond the expected value calculated from the polycrystalline InAs TLM measurements.[2] The excess emitter resistance is attributed to surface states on the intrinsic base caused by the pre-regrowth processing. This hypothesis was tested by a series of emitter regrowth experiments on large-area DC transistors. Improvements to pre-regrowth surface treatments and processing will need to be developed to improve the emitter resistance numbers.

On-wafer TLM measurements from this first RF fabrication also shows high base sheet resistance of 1200 Ω/sq. It is believed that this high resistance is caused by passivation of carbon doping in the base layers. The carbon passivation would be caused by hydrogen desorbing from the hydrogen-rich PECVD SiN_x layers on the surface of the template wafer and on the emitter regrowth sidewalls. Although passivation is not observed in the carbon-doped layers after SiN_x PECVD deposition, high background pressures are observed in the MBE system as the template wafers are being heated for surface oxide desorption prior to emitter regrowth. Large quantities of hydrogen are being released from the PECVD SiN_x during the regrowth processes, and it is not unlikely that this hydrogen might be passivating the carbon-doped layers of the HBT. Further process development is required to remove PECVD SiN_x from the regrown-emitter HBT fabrication process.

4.3 Improvements to the Regrown Emitter HBT

As described in the previous sections, the non-selective regrown emitter process was initially demonstrated on InAlAs/InGaAs/InP DHBTs using a chirped superlattice (CSL) grade at the emitter-base interface.[3,4] In the initial work, citric acid-based etchant was used during base-collector template preparation to remove the base cap layer prior to the SiN_x sidewall deposition, and the thin InP etch stop was removed using HCl-based etchant immediately prior to emitter regrowth. Subsequent investigations of the regrowth surface after these etch steps and an investigation into CSL regrowth onto the process-exposed surface reveal major deficiencies with the original fabrication process and epitaxial design choice.

4.3.1 Improvements to emitter regrowth surface preparation

Shown in Figure 4.15 is an atomic force microscopy (AFM) scan of the base-collector template surface immediately after template growth. This scan of a newly-grown epitaxial surface is used here as a standard for the best expected surface roughness and morphology. The scan shows typical variations in the epitaxial surface roughness less than the 10nm scale included with the scan image. The surfaces shown in Figure 4.16 are obtained after the selective, citric acid-based etchant is used to remove the 500 Å InGaAs base cap layer from the template wafer. The citric acid etchant is composed of citric acid and H_2O_2 diluted in de-ionized water (DI) to obtain an InGaAs etch rate of 9 Å/sec. As shown in Figure 4.16(a), the template surface roughness degrades during the 60 sec etch. Extending the etch to 90 sec further degrades the surface roughness as shown in Figure 4.16(b).

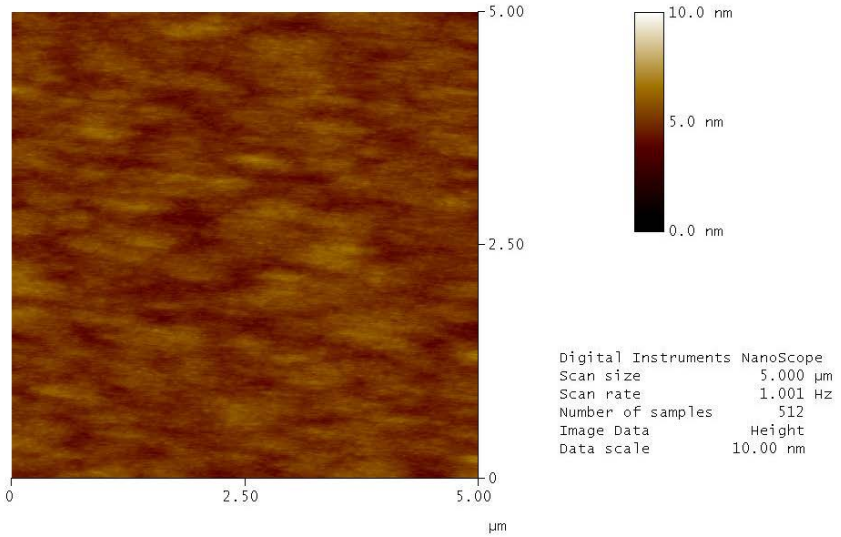


Figure 4.15 AFM image of the as-grown base-collector template InGaAs surface showing <10nm roughness

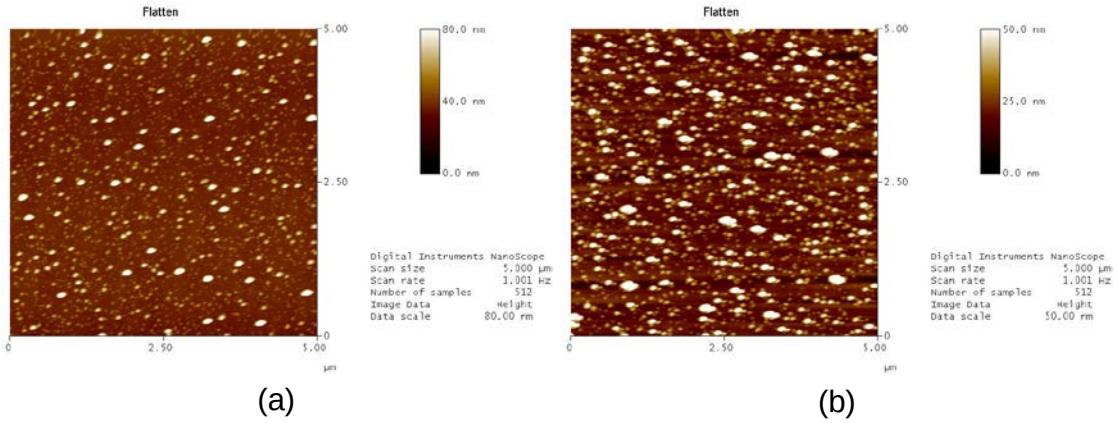
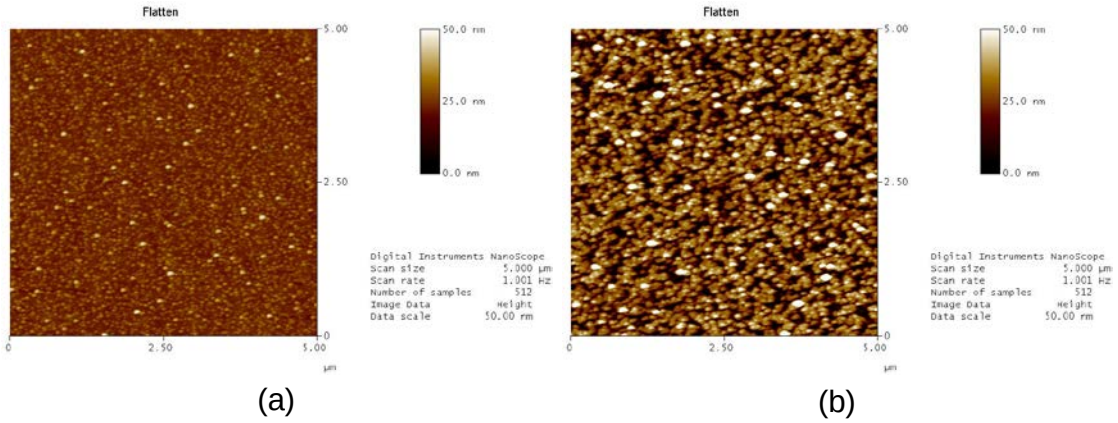


Figure 4.16 AFM images of template surfaces after (a) 60 sec and (b) 90 sec citric:H_2O_2:DI to remove the 500Å InGaAs layer

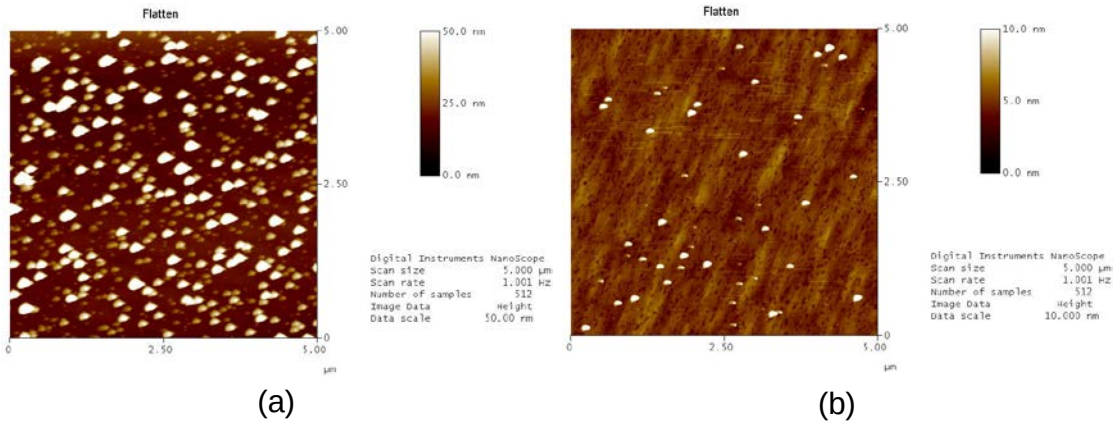
After observing the rough surface produced by the citric-based etch, various selective InGaAs etchants were tested to find an alternative that might produce a smoother surface after removal of the 500 Å InGaAs layer. The best results were obtained using a H_2SO_4:H_2O_2 etch diluted with DI to obtain an etch rate of 30 Å/sec. Shown in Figure 4.17(a) is an AFM image of the base-collector template surface after a 20 sec etch in the H_2SO_4-based etch. Although the surface is still rough according to the included 50 nm scale, the topographic features are much smaller than those of the original citric-based etch process. Extending the H_2SO_4-based etch time to 35 sec further increases the surface roughness as shown in Figure 4.17(b).



(a) (b)

Figure 4.17 AFM images of template surfaces after (a) 20 sec and (b) 35 sec H_2SO_4:H_2O_2:DI to remove the 500Å InGaAs layer

After removing the InGaAs base capping layer, PECVD SiN_x is deposited and removed from the regrowth surface as the dielectric sidewalls are formed. The 20 Å InP etch stop layer is then removed immediately prior to regrowth. In the original fabrication process, a strong HCl-based etch was used to remove the InP layer. Figure 4.18 shows AFM scans of the citric and H_2SO_4-etched surfaces from Figure 4.16(a) and Figure 4.17(a), respectively, after InP etch in strong HCl etchant. The citric-etched surface in Figure 4.18(a) shows increased roughness after the HCl etch. The H_2SO_4 etched surface in Figure 4.18(b), however, is less rough after the HCl etch. In fact, most of the sampled surface is as smooth as the as-grown base-collector template shown in Figure 4.15. Although large topographic feature are present, the overall smoothness of the H_2SO_4etched surface suggests that the H_2SO_4-based InGaAs etchant is superior to the citric-based etchant when used with the strong HCl InP etch.

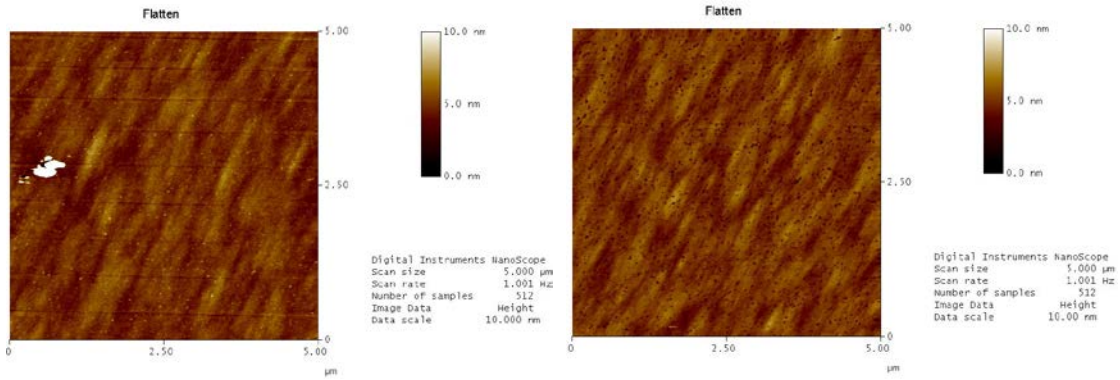


(a) (b)

Figure 4.18 AFM images of template regrowth surface after strong HCl etch on (a) 60 sec citric:H_2O_2:DI etched surface and (b) 20 sec H_2SO_4:H_2O_2:DI etched surface.

Experiments were also conducted to determine if an alternative to the strong HCl-based etchant might improve the regrowth surface after the InP etch. The etch process most successful in producing a smooth surface is based on techniques developed for MBE regrowth of InP onto InP and InGaAsP surfaces.[5] The process utilizes UV light-ozone oxidation followed by a weak (1:10) HF:DI oxide removal. Although it is estimated that the process removes only 20-40 Å of material, the InP etch stop layer is only 20 Å thick so the etch depth is sufficient. AFM scans of the surfaces after the ozone and weak oxide etch process are shown with a 10nm roughness scale in Figure 4.19. The citric-based etched surface from Figure 4.16(a) is shown in Figure 4.19(a) after exposure to the ozone and HF etch. The surface is considerably improved compared to the surfaces shown in either Figure 4.16(a) or Figure 4.18(a). The H_2SO_4 etched surfaces from Figure 4.17(a) is shown in Figure 4.19(b). The large topographic features that appear in HCl-etched surface Figure 4.18(b) are no longer present. The ozone and weak HF etch appears to leave a

smoother surface compared to the strong HCl-based InP etch. After the ozone and HF-based etch, the etched base-collector template has surface roughness comparable to the as-grown template for both the citric- and H_2SO_4-etched surfaces.



(a) (b)

Figure 4.19 AFM images of template regrowth surface after UV-ozone oxidation and HF:DI (1:10) oxide removal on surface etched by (a) 60 sec citric:H_2O_2:DI and (b) 20 sec H_2SO_4:H_2O_2:DI.

The original fabrication process used to expose and prepare the emitter regrown surface included a selective citric-based InGaAs etch followed by a strong HCl-based to remove the InP etch stop. This process produces a surface with relatively rough 50 nm RMS roughness. An AFM image of this original surface is shown in Figure 4.20. Included in this figure is the non-rectifying I-V characteristic produced by a large-area (60×60 µm^2) emitter regrowth onto this surface. In contrast, the surface preparation process using H_2SO_4-based InGaAs etch followed by UV-ozone and weak HF etchant to remove the InP produces a surface with less than 10nm RMS roughness. An AFM surface scan and improved large-area rectifying characteristic for an emitter regrowth onto this surface is shown in Figure 4.21.

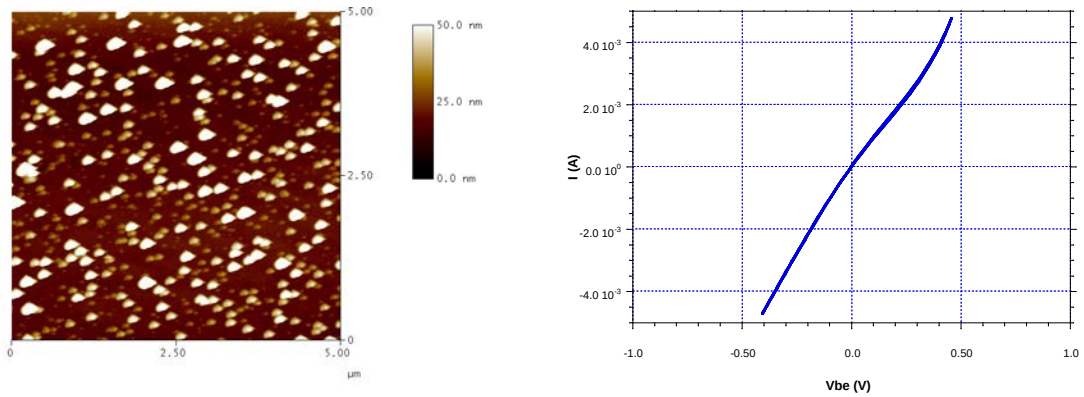


Figure 4.20 AFM image and IV characteristic for base-emitter junction formed on template prepared with the original citric- and strong HCl-based etchants

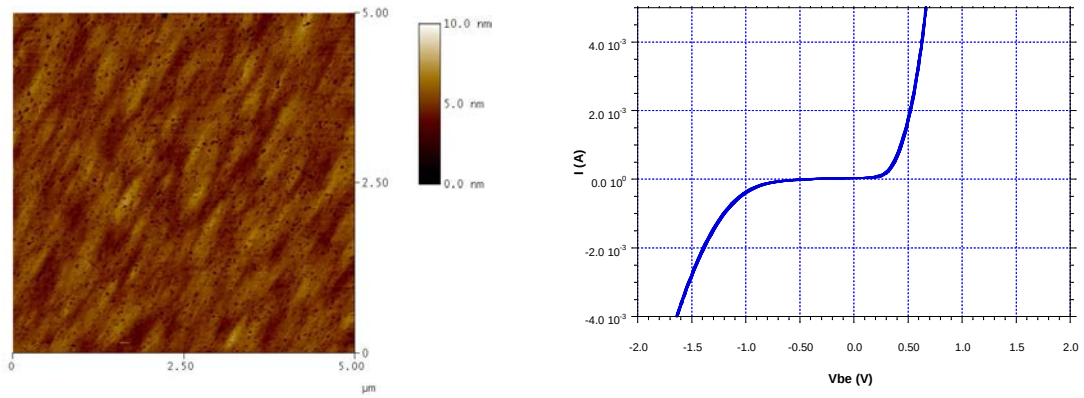


Figure 4.21 AFM image and IV characteristic for base-emitter junction formed on template prepared with improved H_2SO_4-based InGaAs etch and UV-ozone/weak HF etchants

4.3.2 Simplified epitaxial structure for emitter regrowth

The emitter structure used in the initial regrown emitter work included the 300Å, 18-layer CSL grade from the InGaAs base to the InAlAs emitter shown in Figure 2.9. Initiating MBE regrowth using a ternary superlattice is difficult. During initiation and regrowth of the CSL, strong three-dimensional growth is observed in the MBE system's RHEED signal as shown in Figure 4.22. Weak two-dimensional

reconstructions are eventually observed during the InAlAs emitter growth, but the two-dimensional growth occurs only after about 800 Å of deposition. Initiation of strong island growth in the superlattice structure raises concern over the actual alloy compositions formed at the regrowth interface and over potential non-planar deposition of the layers in the critical graded portion of the emitter.

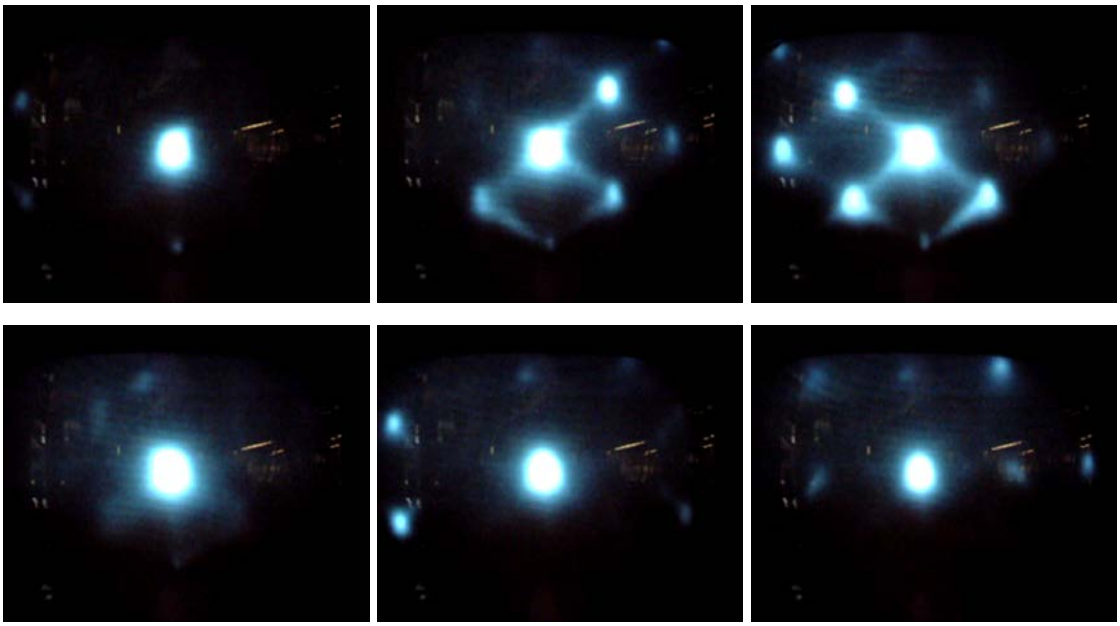


Figure 4.22 Spotty RHEED signal progression showing the strong three-dimensional growth observed during the first 800Å of ternary emitter regrowth

A simplified, abrupt InP emitter structure with no base-emitter grade resolves these concerns by eliminating both the CSL and the use of ternaries near the regrown heterojunction. InP regrowth is less prone to three-dimensional reconstruction, and elimination of the ternary superlattice makes the regrowth less sensitive to composition and planarity effects. Two-dimensional reconstructions are observed by RHEED after less than 100 Å of growth as shown in Figure 4.23. The appearance of

two-dimensional reconstructions in the RHEED signal in the first 100Å of growth is similar to what is observed for growth on epi-ready InP substrates. The combination of simplified growth structure and the improved regrowth surface show dramatic improvements in large-area diode characteristics and in the RHEED signal during emitter regrowth.

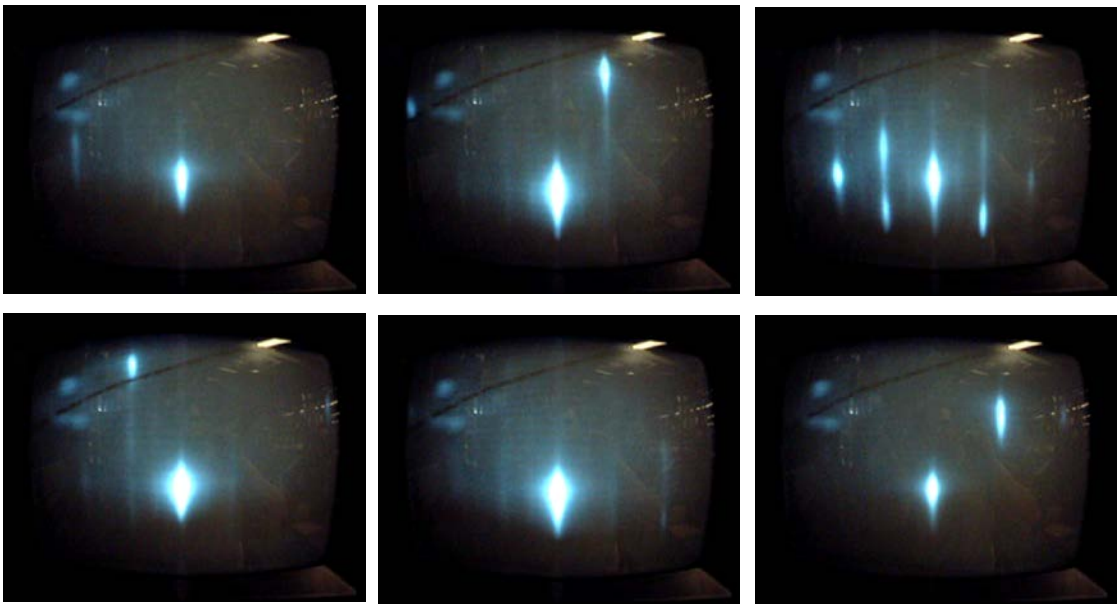


Figure 4.23 Streaky RHEED signal progression observed within the first 100Å of InP emitter regrowth indicates two-dimensional growth and improvement compared to Figure 4.22

4.3.3 Regrown emitter HBT RF results after improvements

Small-area RF devices using emitter regrowth were fabricated while implementing the improvements discussed in the previous sections. As usual, the device is fabricated using a patterned base-collector template onto which the emitter and cap layers are regrown. The template is grown on a semi-insulating (100) InP substrate. The template is composed of a 3000/100 Å InP/InGaAs n+ subcollector,

1100 Å n- InP collector, 400 Å n- grade and undoped setback layer, 400 Å p+ InGaAs base, a 20 Å InP p-type etch stop, and a 500 Å p+ InGaAs base contact layer. The n-type layers are silicon doped, the InGaAs base layers are carbon doped, and the p-type InP is beryllium doped.

A refractory metal stack was sputtered onto the base-collector template, patterned, and dry etched to form what will be a self-aligned base metal buried under the emitter regrowth. Sputtered SiN_x is deposited over the entire wafer, and emitter-etch windows are lithographically defined in the centers of the refractory base contacts. Sputtered SiN_x deposition was developed for this emitter regrowth work in an attempt to remove hydrogen-rich PECVD SiN_x from the carbon doped surface of the wafer. Various submicron emitter widths are included on the regrown emitter fabrication mask, and the emitter lengths are oriented perpendicular to the [011] direction. Using a single photoresist lithography as an etch mask, RIE is used to remove the sputtered SiN_x and refractory metal layers from the emitter regrowth areas. After stripping the photoresist and cleaning the wafer of organic contaminates, the base cap layer in the emitter regrowth window is selectively removed using H_2SO_4-based etchant as described in the previous section.

A 1000 Å layer of PECVD SiN_x is then deposited over the wafer and strongly biased, low pressure RIE is used to form a 0.1 μm vertical SiN_x spacer in the emitter growth windows. During this etch process, all of the PECVD SiN_x is removed from the wafer surface while a thin layer of the PECVD SiN_x is left in the emitter regrowth window to act as an insulating sidewall between the InGaAs base contact layer and

emitter regrowth. Although hydrogen-free, sputtered SiN_x is used for most of the template fabrication, the emitter growth window still contains the hydrogen-abundant PECVD SiN_x sidewall layer. To completely eliminate PECVD SiN_x from the template fabrication process, conformal sputtered SiN_x or some other hydrogen-free SiN_x must be developed to act as the SiN_x sidewall.

After sidewall deposition, the 20Å InP etch stop is removed by a series of ozone treatments and dilute HF-based etchants to expose the intrinsic base regrowth surface. A schematic of the base-collector template before MBE regrowth is shown in Figure 4.24(a). The abrupt, InP emitter described in the previous section has been used for this small-area device demonstration. The emitter is composed of lightly-doped InP followed by heavily-doped InP and InGaAs. The emitter cap is graded in four steps from the InP lattice-matched InGaAs to a 1500Å layer of low-resistance InAs contact material. The regrowth on the exposed base material is monocrystalline while the material deposited on SiN_x is polycrystalline. Emitter contact metal composed of a Ti/Pt/Au/Pt stack is deposited over the emitter regrowth windows, and the excess regrown material with SiN_x underneath is dry-etched by ICP and RIE, respectively, using the emitter metal as an etch mask. The regrown and patterned emitter on the base-collector template is shown in Figure 4.24(b). Because the base refractory metal has low electrical conductivity, self-aligned Ti/Pd/Au metal is deposited onto the exposed portions of the refractory contacts to reduce feed resistance. The remaining fabrication processes include device isolation and collector

contact deposition as shown in Figure 4.24(c). Polyimide is used as an insulating material and Au metallization forms the coplanar waveguide wiring.

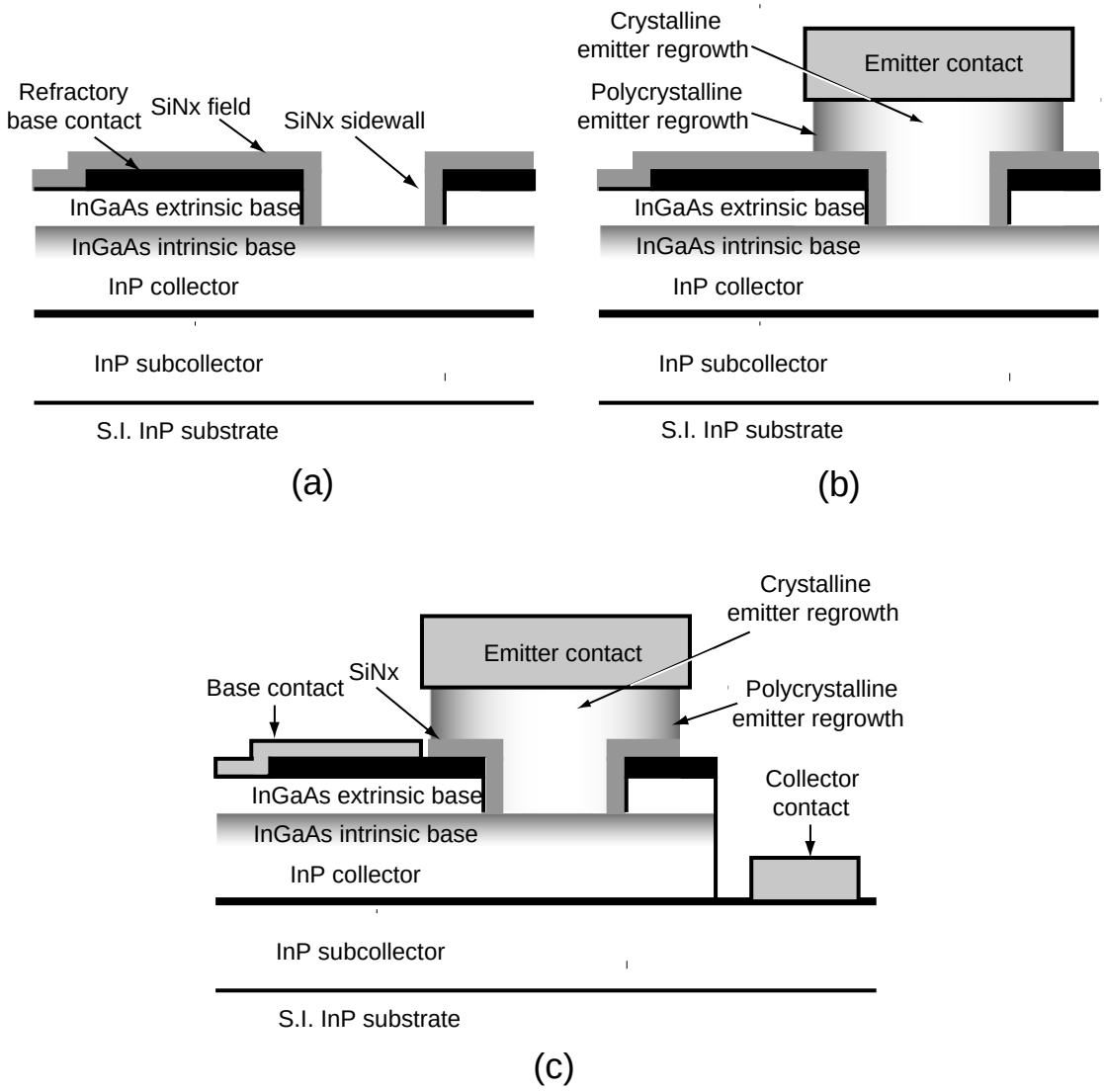


Figure 4.24 Cross-section schematic of regrown-emitter DHBT fabrication process at (a) template fabrication, (b) emitter formation, and (c) completion of HBT mesa

The common-emitter I-V curves for a $0.7 \times 8\ \mu m^2$ regrown emitter device are shown in Figure 4.25. The device geometry is identical to the device described in Section 4.2.2, and the base-collector layer structure is similar to previous work that

enabled a maximum emitter current density of 6×10^5 A/cm^2 at an associated at $V_{CE,sat}$ of 1.5 V and V_{CEO} of 6 V.[6] The common-emitter current gain for this device is 17.

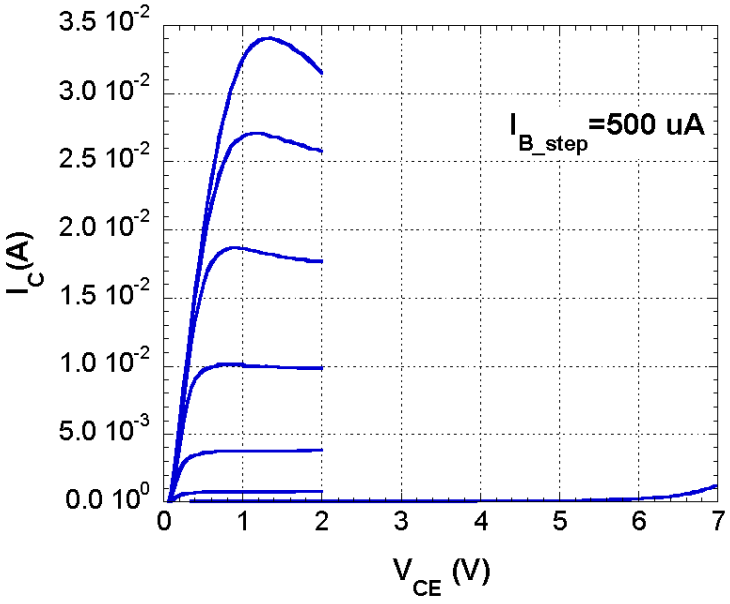


Figure 4.25 Common-emitter I-V curves for regrown emitter HBT with improved fabrication and regrowth processes

The microwave performance of the device was characterized by s-parameter measurements from 5 to 40 GHz. Simultaneous maximum 183 GHz f_τ and 165 GHz f_{max} are extracted using -20 dB/decade extrapolations from h_{21} and Mason's Gain as shown in Figure 4.26. The RF measurements shown in the figure are obtained at bias current density of 3×10^5 A/cm^2 and V_{CE} of 1.5 V. Also shown are maximum stable/available power gain (MSG/MAG) and stability factor (K). Despite improvements to the device fabrication and regrowth, the observed f_τ and f_{max} are lower than expected. The PECVD SiN_x that remains as the insulating sidewall between the emitter regrowth and base contact layer may be releasing enough

hydrogen during the emitter regrowth process to passivate the carbon doping in the nearby base layer. Also suspect are potential voids in the insulating SiN_x sidewall and breaks and voids observed in the regrown emitter layers. The growth artifacts may arise from defects in the SiN_x sidewall or from facet-dependent emitter growth. Further investigations would be required to better understand the deficiencies of the regrown emitter HBT. Despite the shortcoming of this device's RF performance, a great deal has been learned through this initial work and the potential for a high performance InP HBT with emitter regrowth is likely attainable.

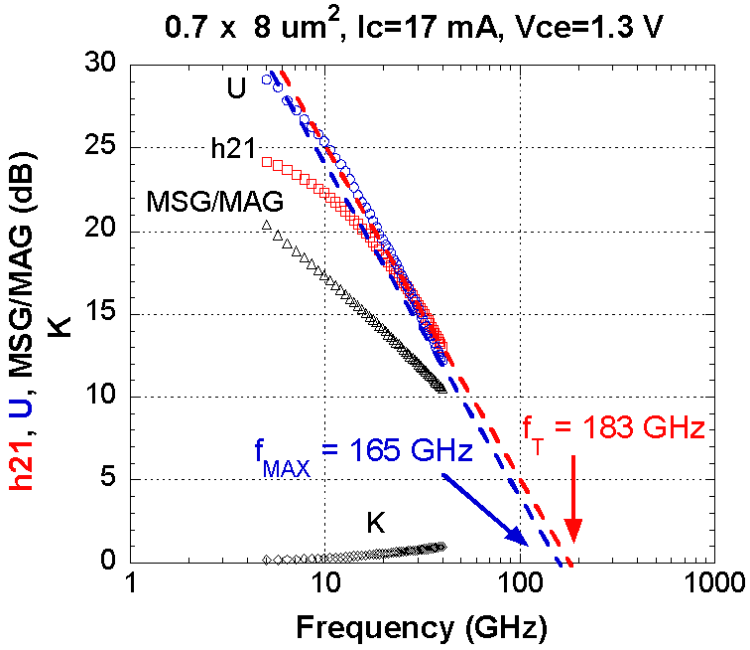


Figure 4.26 RF gains and stability factor for 0.7 × 8 μm^2 regrown abrupt InP emitter HBT with improved fabrication and regrowth

[1] Z. Griffith, M. Dahlstrom, M. Urteaga, M.J.W. Rodwell, X.M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, W.K. Liu, "InGaAs-InP mesa DHBTs with simultaneously high f_τ and f_{max} and low C_{cb}/I_c ratio," *IEEE Electron Device Letters*, vol. 25, no. 5, May 2004, pp. 250-3.

[2] Scott, D.; Urteaga, M.; Parthasarathy, N.; English, J.H.; Rodwell, M.J.W., "Molecular beam deposition of low-resistance polycrystalline InAs," High Performance Devices, 2002. Proceedings. *IEEE Lester Eastman Conference* on, pp. 207- 212, 6-8 Aug. 2002.

[3] Scott, D.; Xing, H.; Krishnan, S.; Urteaga, M.; Parthasarathy, N.; Rodwell, M., "InAlAs/InGaAs/InP DHBTs with polycrystalline InAs extrinsic emitter regrowth," *Device Research Conference*, 2002. 60th DRC. Conference Digest, pp. 171- 172, 2002.

[4] Wei, Y.; Scott, D.W.; Yingda Dong; Gossard, A.C.; Rodwell, M.J., "A 160-GHz f_T and 140-GHz f_{MAX} submicrometer InP DHBT in MBE regrown-emitter technology," *Electron Device Letters*, IEEE, vol.25, no.5, pp. 232- 234, May 2004.

[5] W. Passenberg, W. Schlaak, "Surface preparation for molecular beam epitaxy-regrowth on metalorganic vapour phase epitaxy growth InP and InGaAsP layers," *Journal of Crystal Growth*, 1997, vol. 173, pp. 266-70.

[6] Z. Griffith, M. Dahlstrom, M. Urteaga, M.J.W. Rodwell, X.M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, W.K. Liu, "InGaAs-InP mesa DHBTs with simultaneously high fτ and fmax and low Ccb/Ic ratio," IEEE Electron Device Letters, vol. 25, no. 5, May 2004, pp. 250-3.

Chapter 5

Conclusion

The work described in this written dissertation was performed during the time period between fall 1999 and spring 2004, and most references in the dissertation are consequently from that time period or earlier. The oral defense of the work did not occur until spring 2013, and in the time between the work and the oral defense there has been continued development in InP HBT technology. This allows for a conclusion chapter that acts less as a prediction of what might be, but more as an epilogue of what has happened during the nine years following the regrown emitter HBT work.

5.1 Advancement in InP HBTs

During the nine years after the regrown emitter HBT work, advanced InP HBTs did not become more structurally similar to SiGe HBTs, and regrowth of InP HBT layers has not become commonplace. The InP HBT, however, has continued to find performance advancements through a path that is more evolutionary rather than revolutionary. Advancements in InP HBTs have come through scaling and parasitic reductions, and the resulting RF performance has essentially doubled during this time period.

As reported in Chapter 1, emitter widths in high-performance InP HBTs prior to 2004 were not generally scaled below 0.5 μm. It was not until 2006 that high-performance devices with emitter widths of 0.25 μm were reported.[1,2] Advancements at that time were strongly motivated by the DARPA Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST) program which specifically required 0.25 μm emitter width HBTs with cutoff frequencies of at least 450 GHz as a program goal. Evolutionary performance advancements were obtained by scaling of the device epi for reduced transit time through the device as well as potentially reduced emitter resistance, narrowing of the mesa HBT features for reduced capacitance, increasing the current density through the device, and improving the ohmic contact technology not only to have lower contact resistance but also to survive the increased current densities and to behave appropriately when combined with the reduced epitaxial thicknesses.

Incorporating the advancements listed above in the correct combination can be challenging. One successful combination of these advancements was demonstrated in the form of an InP HBT with dry-etched refractory emitter metal and simultaneous f_τ of 430 GHz and f_{max} of 800 GHz.[3] This 0.27 × 3.5 μm^2 device utilizes a 30 nm InP emitter and 100 nm collector drift region. Peak RF performance was obtained with a bias of I_C = 17.4 mA (J_C = 18.4 mA/μm^2) and V_{ce} = 1.64 V. The molybdenum emitter contacts were formed by blanket evaporation, electron beam lithography (EBL), and dry etch. The emitter mesa was formed by a sequence of wet etch and SiN sidewall depositions to help minimize emitter undercut during wet etch and provide minimal

gap resistance for the self-aligned base metal evaporation. The refractory emitter metal provides both a thermally stable ohmic contact at high emitter current density and a low emitter contact resistance.

A further scaled 0.15 × 3 μm^2 InP DHBT with both the emitter and base mesas defined by EBL was reported with simultaneous f_τ = 530 GHz and f_{max} = 750 GHz in 2012.[4] In this device, the emitter and the base contacts on each side of the emitter were lithographically defined with 150 nm widths; producing a total base mesa width of just 450 nm, the narrowest reported HBT to date. The RF results were measured at a bias of I_C = 12.4 mA (J_C = 27.6 mA/ μm^2) and V_{ce} = 1.5 V. Current gain cutoff frequency f_τ is higher than the previous devices with record f_{max} due to the thinning of the drift collector from 100 nm to 70 nm. Narrowing the base mesa via EBL to reduce C_{cb} allows for the 750 GHz f_{max} despite the C_{cb} increase penalty from thinning the collector to 70 nm thickness.

The InP HBT with highest RF performance currently in literature is a 0.13 × 2 μm^2 emitter area device with f_τ > 520 GHz and f_{max} > 1.1 THz.[5] This device uses EBL to define the emitter and aggressively scaled epitaxy with a 25 nm thickness base and 100 nm thickness collector. The peak RF performance is obtained at an I_C = 6.9 mA (J_C = 26.5 mA/ μm^2) with V_{ce} = 1.6 V. Although an electroplated emitter post process with dielectric sidewall spacers is reported, no details about the ohmic contact fabrication processes are given.

The InP HBT performance advancements seen in recent years are demonstrated through straight-forward implementations of lateral and epitaxial

scaling, aggressive increase in current density through the device, and good epitaxial design. Less straight-forward is the extensive work that has been done to improve the ohmic contacts in InP HBTs. Included in this work are examples of low resistance contacts to heavily-doped n-type InGaAs appropriate for emitter contacts and contacts to heavily-doped p-type InGaAs as would be used to contact the base region.

Ohmic contacts to n-type InGaAs are referred to as being *in-situ* when deposited after epitaxial growth and before removal from the high vacuum system, or *ex-situ* when the wafer is exposed to the atmosphere after epitaxial growth; suggesting that some type of surface preparation must be applied prior to deposition of emitter ohmic metal. An example of low resistance *in-situ* ohmic contact to n-type InGaAs is molybdenum (Mo) deposited after the InGaAs emitter MBE growth before breaking vacuum demonstrating TLM contact resistivity as low as $(1.1 \pm 0.6) \times 10^{-8}\ \Omega\ cm^2$.[6] Surface preparation for *ex-situ* contacts on n-type InGaAs has also been successfully demonstrated. Recent studies have favored UV-ozone oxidation of photoresist patterned surfaces followed by oxide removal by either dilute HCl or dilute HF.[7,8]

Ohmic contact to heavily-doped, p-type InGaAs have also been reported for the *in-situ* case using Mo and iridium (Ir) as metal contact layers.[9,10] If used to contact the base region in an InP HBT, *in-situ* deposition would likely require emitter regrowth. Fortunately, low contact resistance *ex-situ* ohmic contacts to p-type InGaAs have been reported using UV-ozone oxidation and dilute acid oxide removal as surface treatment prior to metal deposition.[11,12] The *ex-situ* demonstrations show thermally-stable tungsten TLM contact resistance as low as $0.55\ (+/-\ 0.69/0.41) \times 10^{-8}$

Ω cm^2 as deposited onto p = 1.6 × 10^{20} cm^{-3} InGaAs. The contact resistance increases to 1.90 (+/- 1.19/0.88) × 10^{-8} Ω cm^2 after annealing at 250ºC for 60 minutes in a nitrogen environment, but this contact resistance is still considered exceptionally low.

While InP HBTs have made consistent progress in RF performance since 2004, SiGe HBTs have reported little performance advancement beyond what was covered in Chapter 1 of this dissertation. IBM did release their high-performance SiGe BiCMOS 8HP process targeting RF applications as a foundry offering in 2005. The 8HP device is at the 130 nm technology node and offers 200 GHz f_τ and 270 GHz f_{max} at V_{cb} = 0.5 V with a breakdown BV_{CEO} of 1.77 V.[13] While the RF performance of SiGe HBTs has not maintained the rapid progress demonstrated in the early 2000s, the achievement in offering high-performance devices on 200 mm diameter wafers as a foundry service should not be disregarded. Alternatively, advanced InP HBTs have not proven themselves to be high-yielding or highly adaptable even to medium-scale integration. Examples of large circuits in advanced InP HBT technologies are rare, and transistor counts top out near 5000 in large circuit demonstrations.[14,15] In recent years, DARPA has altered its strategy to obtain high-performance HBTs in high-yield circuits with high levels of integration by funding programs such as Compound Semiconductor Materials on Silicon (COSMOS). Rather than forcing higher performance from Si-based devices or higher yield and integration from III-V technologies, DAPRA proposes integration of high-performance III-V electronics with Si CMOS and SiGe technologies; attempting to demonstrate improved circuit performance by utilizing the strengths of each technology.[16,17]

5.2 Retrospects and Future Work on Regrown Emitter HBTs

The work present in this dissertation provides a demonstration of the emitter regrowth portion of a conceptual device. It lays the groundwork for a more rigorous implementation of the regrown emitter in a base-collector template with extrinsic base contact regions thicker than the intrinsic base. There is a great deal of work that can still be done, and the potential for performance benefits are still available.

In light of the improvements in InP HBT performance and the improvements in ohmic contacts since the emitter regrowth work, it is likely that the regrown emitter contact wider than the base-emitter junction may not be necessary. In that case, the method by which the emitter regrowth is performed is not be limited to MBE deposition; CVD methods may be better suited for providing high-yielding, high-quality InP emitter regrowth similar to what is used for SiGe HBTs. A more in-depth and rigorous analysis of the emitter regrowth surface, regrowth methodology, and resulting base-emitter junction is certainly in order if emitter regrowth work is to proceed.

If a base-collector template with InP etch stop is used for future regrown emitter work, a greater investigation might be put into the surface preparation steps detailed in Section 4.3.1 where the 20 Å etch stop is removed by UV-ozone oxidation and dilute HF etchant. Although there is an undeniable improvement of the regrowth surface during that step of the process and also in the regrowth onto that surface, it is not completely clear that the 20 Å InP layer is actually removed by the oxidation and etch process. However, as Professor Chris Palmstrøm pointed out during the oral

defense of this work, there may be advantage to intentionally leaving behind some or all of that InP etch stop layer. An InP surface will have less native oxide compared to an InGaAs surface, and it would thus be easier to desorb oxide from InP than from InGaAs prior to regrowth. Also, the desorption of oxide from the regrowth surface in this work has generally been done in an arsenic background assuming an exposed InGaAs base surface. The beam flux was then switched to phosphorous to begin the InP emitter. In either the case where the InP etch stop is left behind or if the exposed regrowth surface truly is InGaAs, removing the switch from arsenic to phosphorous at the critical base-emitter regrowth interface presents an advantage. The final argument to leave the InP etch stop layer intact might be the most important. In this work, the metallurgical regrowth junction is also assumed to be the electrical base-emitter junction. This is very much different from the case of the SiGe HBT where the heavily-doped n-type poly is deposited onto an unintentionally doped Si layer and the electrical base-emitter junction is formed by diffusion of dopant from the n-type poly into the undoped Si. By including the actual base-emitter electrical junction on the base-collector template during initial growth of the base-collector template and using the regrowth only to complete and connect to the base-emitter junction, the metallurgical regrowth junction can be dissociated from the electrical base-emitter junction.

As stated at the end of Chapter 4, further work on the regrown emitter InP HBT will require further work and investigation into the PECVD SiN used to form the sidewalls in the emitter regrowth window. Although the deposition and dry etch of

SiN was not found to be a first-order contributor to the regrowth surface damage described in Section 4.3, it should not be assumed that the deposition and removal of SiN has no effect on the regrowth surface. Potential damage from these steps may have been simply overshadowed by the other surface preparation steps of the original process. Once those process steps were improved, no effort was made to investigate if the SiN deposition and dry etch then showed up as a significant factor in damaging the regrowth surface. Additionally, there are outstanding issues with potential voids in the SiN sidewalls that may contribute to the high base-emitter leakage current observed throughout this work, and there are outstanding suspicions that the sidewall SiN releases hydrogen (inherent in PECVD dielectrics) during the high-temperature regrowth process and that the hydrogen is passivating the carbon doping in the base near the emitter regrowth windows.

It turns out that the emitter regrowth work presented in this dissertation was not necessary to advance InP HBT performance during the decade that followed. However, emitter regrowth may eventually find a place in the future of high-performance InP HBTs. If so, a great deal of work still needs to be done to implement it. It is my hope that the work presented in this dissertation will lessen that burden in some small part.

[1] Lind, E.; Griffith, Z.; Rodwell, M.J.W.; Xiao-Ming Fang; Loubychev, D.; Yu Wu; Fastenau, J.M.; Liu, A.W.K. , "250 nm InGaAs/InP DHBTs w/650 GHz f_{max} and 420 GHz f_{τ}, operating above 30 mW/μm^2," *Device Research Conference Digest*, 64th, June 2006, pp. 26-8.

[2] Griffith, Z.; Lind, E.; Rodwell, M.J.W.; Xiao-Ming Fang; Loubychev, D.; Ying Wu; Fastenau, J.M.; Liu, A.W.K., "Sub-300 nm InGaAs/InP Type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz f_{max} and 416 GHz f_T," *International Conference on Indium Phosphide & Related Materials Technical Digest*, 14-18 May 2007, pp. 403-6.

[3] V. Jain, E. Lobisser, A. Baraskar, B. J. Thibeault, M. J. W. Rodwell, Z. Griffith, M. Urteaga, D. Loubychev, A. Snyder, Y. Wu, J. M. Fastenau, W. K. Liu, "InGaAs/InP DHBTs in a dry-etched refractory metal emitter process demonstrating simultaneous f_{τ} / f_{max} ~ 430/800 GHz," *IEEE Electron Device Letters*, vol. 32 , no. 1, January 2011, pp. 24-6.

[4] E. Lobisser, J. C. Rode, V. Jain, H.-W. Chiang, A. Baraskar, W. J. Mitchell, B. J. Thibeault, M. J. W. Rodwell, "InGaAs/InP DHBTs with emitter and base defined through electron-beam lithography for reduced Ccb and increased RF cut-off frequency," *39th International Symposium on Compound Semiconductors Digest*, 27-30 August 2012.

[5] M. Urteaga, R. Pierson, P. Rowell, V. Jain, E. Lobisser, M. J. W. Rodwell, "130 nm InP DHBTs with f_{τ} > 0.52 THz and f_{max} >1.1 THz," *69th IEEE Device Research Conference Digest*, June 20-22, 2011.

[6] A. K. Baraskar, M. A. Wistey, V. Jain, U. Singisetti, G. Burek, B. J.Thibeault, Y. J. Lee, A. C. Gossard, M. J. W. Rodwell, "Ultra low resistance, non-alloyed ohmic contacts to n-InGaAs," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 27, no. 4, Jul/Aug 2009, pp. 2036-9.

[7] V. Jain, A.K. Baraskar, M.A. Wistey, U. Singisetti, Z. Griffith, E. Lobisser, B. J. Thibeault, A.C. Gossard, M. J. W. Rodwell, "Effect of surface preparations on contact resistivity of TiW to highly doped n-InGaAs," *International Conference on Indium Phosphide & Related Materials Technical Digest*, 10-14 May 2009, pp. 358-61.

[8] R. Dormaier, S. E. Mohney, "Factors controlling the resistance of ohmic contacts to n-InGaAs," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 30, no. 3, May/Jun 2012, pp. 1209-18.

[9] A. Baraskar, V. Jain, M. Wistey, E. Lobisser, B. Thibeault, Y. J. Lee, A. Gossard, M. Rodwell, " *In-situ* ohmic contacts to p-InGaAs," *Electronics Materials Conference Digest*, 23-25 June 2010.

[10] A K. Baraskar, V. Jain, M. A. Wistey, E. Lobisser, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, "*In-situ* iridium refractory ohmic contacts to p-InGaAs," *27th North American Molecular Beam Epitaxy Conference Digest*, 26-29 September 2010.

[11] A. Baraskar, V. Jain, M. A. Wistey, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, "*In-situ* and e*x-situ* ohmic contacts to heavily doped p-InGaAs," *16th International Conference on Molecular Beam Epitaxy Digest*, 22-27 Aug 2010.

[12] E. Lobisser, A. Baraskar, V. Jain, B. Thibeault, A. Gossard, M. J W Rodwell, "*Ex-situ* tungsten refractory ohmic contacts to p-InGaAs," *38th International Symposium on Compound Semiconductors Digest*, 22-26 May 2011.

[13] IBM Systems and Technology, "IBM SiGe BiCMOS 8HP," IBM. November 2012. Web. 9 June 2013. < http://public.dhe.ibm.com/common/ssi/ecm/en/tgd03022usen/TGD03022USEN.PDF>.

[14] Monier, C.; Scott, D.; D'Amore, M.; Chan, B.; Dang, L.; Cavus, A.; Kaneshiro, E.; Nam, P.; Sato, K.; Cohen, N.; Lin, S.; Luo, K.; Wang, J.; Oyama, B.; Gutierrez, A., "High-speed InP HBT technology for advanced mixed-signal and digital applications," *Electron Devices Meeting Digest*, 10-12 Dec. 2007, pp.671-4.

[15] Chan, B.; Oyama, B.; Monier, C.; Gutierrez, A., "An ultra-wideband 7-Bit 5 Gsps ADC implemented in submicron InP HBT technology," *Compound Semiconductor Integrated Circuit Symposium Digest*, 14-17 October, 2007.

[16] Gutierrez-Aitken, A.; Chang-Chien, P.; Scott, D.; Hennig, K.; Kaneshiro, E.; Nam, P.; Cohen, N.; Ching, D.; Khanh Thai; Oyama, B.; Zhou, J.; Geiger, C.; Poust, B.; Parlee, M.; Sandhu, R.; Wen Phan; Oki, A.; Kagiwada, R., "Advanced Heterogeneous Integration of InP HBT and CMOS Si Technologies," *Compound Semiconductor Integrated Circuit Symposium Digest*, 3-6 October, 2010.

[17] Oyama, B.; Ching, D.; Thai, K.; Gutierrez-Aitken, A.; Cohen, N.; Scott, D.; Hennig, K.; Kaneshiro, E.; Nam, P.; Chen, J.; Chang-Chien, P.; Patel, V. J., "InP HBT/Si CMOS-Based 13-Bit 1.33Gsps Digital-to-Analog Converter with >70 dB SFDR," *Compound Semiconductor Integrated Circuit Symposium*, 14-17 October 2012.