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Fabrication Processes and Epitaxial Growth Technologies for Base-Collector Parasitics Reduction in Indium Phosphide HBT

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4. **Y. Dong**, Y. Wei, Z. Griffith, M. Urteaga, M. Dolstrom, A. Gossard, and M. Rodwell, 'InP Heterojunction Bipolar Transistor with Selectively Implanted Collector', *2003 International Semiconductor Device Research Symposium, Washington, DC, (ISDRS 2003).*

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8. **Y. Dong**, D. Scott, Y. Wei, A. Gossard, and M. Rodwell, 'Low Resistance P-type Polycrystalline GaSb grown by Molecular Beam Epitaxy', *Journal of Crystal Growth,* 256 (2003) 223-229.

9. **Y. Dong**, D. Scott, A. Gossard, and M. Rodwell, 'Characterization of Contact Resistivity on InAs/GaSb Interface', *Electronic Materials Conference, Salt Lake City, UT, 2003.*

10. **Y. Dong**, Y. Okuno, and U. Mishra, 'Selective Area Growth of InP through Narrow Openings by MOCVD and its Application to InP HBT', *15th International Conference on Indium Phosphide and Related Materials, Santa Barbara, CA, 2003 (IPRM 2003)*.

11. **Y. Dong**, D. Scott, A. Gossard, and M. Rodwell, 'Molecular Beam Epitaxy of Low-Resistance Polycrystalline P-type GaSb', *15th International Conference on Indium Phosphide and Related Materials, Santa Barbara, CA, 2003, (IPRM 2003)*.

12. N. Parthasarathy, **Y. Dong**, D. Scott, M. Urteaga and M.J.W. Rodwell, 'Planar Device Isolation for InP Based DHBTs', *62nd Device Research Conference, Notre Dame, IN, 2004*.

13. D. Scott, C. Kadow, **Y. Dong**, Y. Wei, A. C. Gossard, and M.J.W. Rodwell, 'Low Resistance n-type Polycrystalline InAs grown by Molecular Beam Epitaxy', accepted by *Journal of Crystal Growth.*

14. Y. Wei, D. Scott, **Y. Dong,** A.C. Gossard, and M.J.W. Rodwell, ' A 160-GHz f_T and 140-GHz f_{MAX}, Submicronmeter InP DHBT in MBE Regrown-Emitter Technology', IEEE Electron Dev. Lett., 25 (2004) 232-234.

15. D. Scott, Y. Wei, **Y. Dong,** A.C. Gossard, and M.J.W. Rodwell, ' A 183GHz f_T and 165GHz f_{MAX} Regrown-Emitter DHBT with Abrupt InP Emitter', IEEE Electron Dev. Lett., 25 (2004) 360-362.

16. Y. Wei, D. Scott, **Y. Dong,** A.C. Gossard, and M.J.W. Rodwell, '280GHz f_T InP DHBT with 1.2μm^2 Base-Emitter Junction Area in MBE Regrown Emitter Technology', *62nd Device Research Conference, Notre Dame, IN, 2004*.

Abstract

Fabrication Processes and Epitaxial Technologies For Base-Collector Paracitics Reduction in Indium Phosphide HBT

by

Yingda Dong

The increasing demand in communication and radar technology for higher bit-rates and increased frequency resolution is eventually reflected in the requirement of devices capable of operating at very high frequencies. Currently the great limitations on heterojunction bipolar transistor (HBT) speed are the parasitic components of the device, most notably the extrinsic base-collector capacitance (C_{BC}) and base resistance (R_B).

This dissertation is focused on efforts to develop novel regrowth and fabrication process technologies toward reducing InP HBT's base-collector parasitic capacitance and base resistance. Although ultra wide-bandwidth InP HBTs were the end goal, the majority of the efforts were focused on growth and process technologies.

InP HBT with extrinsic base laterally overgrown on buried SiO_2 has been proposed and developed for simultaneous reduction of C_{BC} and R_B. To obtain

maximum lateral overgrowth length, the MOCVD selective growth of InP through narrow mask openings has been carefully examined. Both DC and RF characteristics of the base-regrown HBTs are demonstrated.

InP HBT with a collector pedestal has also been developed for base-collector capacitance reduction. The collector pedestal is formed by using selective ion implantation and regrowth by molecular beam epitaxy. Many aspects of Si implantation in InP have been examined. Concerns relating to HBT layer structure design, epitaxial growth, and device fabrication have been addressed. N-type sheet charge accumulation is discovered on the InP regrowth interface and P-type counter-doping layer is successfully introduced to compensate the interfacial charge. Both DC and RF performances of pedestal HBTs are demonstrated with 40% base-collector capacitance reduction achieved.

Finally to combine the best features of SiGe and InP HBT technology, double-poly regrowth InP HBT is proposed with structural features and process flow close to that of a Si/SiGe HBT. In our efforts to find a low resistivity material for the extrinsic base, the MBE growth and electrical properties of carbon-doped polycrystalline GaSb, as well as the interfacial contact resistivity of N-InAs/P-GaSb heterostructure are thoroughly investigated.

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Chapter 1
Introduction

1.1 Overview

Heterojunction bipolar transistors (HBTs) have high transconductance, extremely reproducible parameters and wide bandwidth. These attributes make HBTs the device of choice for many precision high-speed circuits. In recent years, research in wide bandwidth HBTs[1],[2] have been driven fast by applications in high-frequency communications and radar. First, in optical fiber communications, the emergence of 160Gb/s transmission equipment in the near future must rely on a timely and substantial improvement in the bandwidth of semiconductor electronics. Amplifiers with flat gain and linear phase over a ~DC-110GHz bandwidth and master-slave latches[3] operable at 80GHz or 160GHz clock frequency will be required. A second set of driving applications are wideband, high resolution and analog-digital converters (ADCs). Digital-analog converters (DACs), and direct digital frequency synthesizers[4]. Increased bandwidths of these mixed-signal ICs will increase the bandwidth and frequency agility of military radar and communication systems. High resolution ADCs and

DACs require transistor bandwidths 10^2:1 to 10^4:1 larger than the signal frequencies involved. Transistors with several hundred GHz f_T and f_{max} would enable high-resolution microwave mixed-signal ICs. A third driving application is in monolithic millimeter-wave integrated circuits (MIMICs). Progressive improvements in transistor bandwidths permit the evolution of radar and communications ICs to higher frequencies. A transistor with 1THz power gain cut-off frequency would provide useful gain over the full 30GHz-300GHz millimeter-wave band. This would permit e.g. digital radio links with millimeter-wave carrier frequencies and 1-10Gb/s channel capacities.

These ever-growing demands in communications and radar technologies for increased bit-rates and frequency resolution all require system capable of providing increased bandwidth and clock rates, which is eventually reflected in the requirement that the HBTs, which are the building blocks of these systems, must be capable of operating at higher and higher frequencies.[5],[6]

1.2 Motivations of InP HBT's Base-collector Parasitic Reduction

Two measures or figure-of-merit useful in evaluating the high-frequency performance of a transistor are the current-gain cutoff frequency f_T, and maximum frequency of oscillation f_{max}. f_T is defined as the frequency at which

the short-circuit current gain decreases to unity. f_{max} is defined as the frequency at which the maximum available power gain decreases to unity. Though finally dependent on the application, transistors with increased f_T and f_{max} are desirable in order to meet the demands in bandwidth of the next generation of systems.

To a first approximation, f_T corresponds to the transit time of carriers through the device. For an HBT, f_T is written as:

$$f_T = \frac{1}{2\pi(\tau_E + \tau_B + \tau_C + \tau_{CC})} \ , \qquad (1.1)$$

where τ_E and τ_{CC} are time constants related to the charging and discharging of the device capacitance and τ_B and τ_C are transit times through the device. In order to increase f_T in bipolar transistors, the relative time constants and transit times must be reduced. This entails scaling the device vertically to decrease the distances across which the carriers transit. With the advent of precise growth techniques, like molecular beam epitaxy (MBE), which allow for the control of device layer thickness at the atomic scale, vertical or epitaxial scaling is easily achieved, and transistors with f_T on the order of several hundred GHz are possible.[7],[8]

On the other hand, f_{max}, which is related to f_T, is strongly dependent on the magnitude of the base resistance (R_B) and base-collector capacitance (C_{BC}) time constant:

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{BCi}}} \;, \tag{1.2}$$

C_{Bci} is the intrinsic part of C_{BC} in series with the base resistance. f_{max} is increased by reducing R_B and C_{BCi} chiefly through increased doping in the base and horizontal scaling. State-of-the-art conventional emitter-up transistors with ~0.4μm wide emitters demonstrate f_{max} of up to ~500GHz.[7],[9] But commonly, conventional mesa-structured HBTs are still limited by the extrinsic base-collector capacitance underneath the base contacts.

At a given HBT scaling generation, defined by the minimum emitter feature size, different transistors layer structures are preferred so as to obtain a differing balance of device parasitics that are more sited for the particular application – i.e. mm-wave tuned amplifiers benefit from high f_{max} and tolerate appreciably lower f_T. The minimum gate delay of a digital IC in contrast is not determined by an algebraic function of f_T and f_{max}, but instead by a set of time constants of which $C_{BC}\Delta V_{logic}/I_C$ is a major contributor.

Since base-collector capacitance (C_{BC}) is a critical factor limiting the device and IC's high-frequency performance, various technologies and techniques that directly address the reduction of C_{BC} have been examined: HBT with a buried subcollector by selective epitaxy[10] and selective implantation[11], sidewall contacted bases[12], undercut collectors[13], collector-up transistors with regrown

base-collector junction or implanted extrinsic emitters[14],[15], and the transferred substrate HBT[16].

1.3 Synopsis of the Dissertation

This dissertation covers several novel regrowth technologies and process techniques toward reducing base-collector parasitic capacitance and base resistance. Although ultra wide-bandwidth InP HBTs were the end goal, the majority of this thesis is focused on process technologies.

Chapter 2 discusses the design, epitaxial growth and fabrication process of InP HBT with extrinsic base laterally overgrown on buried SiO_2 for simultaneous reduction of C_{BC} and R_B. The MOCVD selective growth behaviors of InP through narrow openings have been carefully examined. It is found that the lateral overgrowth of InP on SiO_2 is strongly dependent on both the opening width and orientation. Based on these experimental results, HBTs with extrinsic base laterally overgrown on buried SiO_2 were fabricated. Emitters were aligned 60° off [011] direction to obtain the maximum lateral overgrowth length for the extrinsic base. Both DC and RF characteristics of the base-regrown HBTs are demonstrated.

Chapter 3 presents the design and fabrication of an InP HBT with a collector pedestal. The pedestal, formed by selective ion implantation and

regrowth by molecular beam epitaxy, permits a larger collector depletion thickness under the base contacts than the collector depletion thickness directly under the emitter. The extrinsic C_{cb} can then be reduced without increasing the collector transit time or decreasing the Kirk-effect-limited current density. Many aspects of silicon selective implantation in InP are examined, including implant energy and fluence, annealing conditions, dopant activation efficiency, as well as the implanted dopants' lateral distribution. MBE regrowth on implanted and subsequently processed templates is investigated. N-type sheet charge accumulation was discovered on the InP regrowth interface and the possible origins of the N-type sheet charges have been investigated. P-type counter-doping layer is introduced and successfully compensates the regrowth interfacial charges. Both DC and RF performance of pedestal HBTs are demonstrated and analyzed.

To combine the best features of SiGe and InP HBT technology, double-poly regrowth InP HBT is proposed. This HBT has structural features and process flow close to that of a Si/SiGe HBT, but uses InP-based materials. In Chapter 4, work on the development of double-poly HBT process, with a focus on the development of low resistance polycrystalline extrinsic base, are examined. In our efforts to find a low resistivity p-type polycrystalline material, the MBE growth and electrical properties of carbon-doped GaSb are thoroughly investigated. It has been found that with the same doping level, grain size and

similar film thickness, the resistivity of poly-GaSb is more than one order of magnitude lower than that of poly-GaAs. This strongly suggests that poly-GaSb is an excellent candidate for the use as an extrinsic base material in InP HBTs. To further lower the resistivity of the polycrystalline extrinsic base layer, N-InAs/P-GaSb composite extrinsic base structure is proposed to exploit the very low bulk and metal contact resistivity of n-type polycrystalline InAs. The interfacial contact resistivity between n-type InAs and p-type GaSb layers, and its dependence on the doping densities on both sides of the heterostructure are also investigated.

Conclusions and suggested future work are presented in Chapter 5.

References

[1] H. Kroemer, 'Heterostructure bipolar transistors and integrated circuits', Proc. IEEE, Vol. 70, pp. 13-25, 1982

[2] P. Asbeck, F. Chang, K.-C. Wang, G. Sullivan, and D. Cheung, 'GaAs-based heterojunction bipolar transistors for very high performance electronic circuits', Proc. IEEE, Vol. 81, pp. 1709-1726, 1993

[3] M. Sokolich, D. P. Docter, Y. K. Brown, A. R. Kamer, J. F. Jensen,W. E. Stanchina, S. Thomas, III, C. H. Fields, D. A. Ahmari, M. Lui, R. Martinez, and J. Duvall, "A low power 52.9 GHz static frequency divider in a manufacturable 180 GHz AlInAs/InGaAs HBT IC technology," in Tech.Dig., IEEE GaAs IC Symp., Atlanta, GA, Nov. 1–4, pp. 117–120, 1998

[4] D. C. Larson, "High speed direct digital synthesis techniques and applications," Tech. Dig., IEEE GaAs IC Symp., pp. 209–212, 1998

[5] B. Agarwal, Q. Lee, R. Pullela, D. Mensa, J. Guthrie, and M.J.W. Rodwell, 'A transferred-substrate HBT wide-band differential amplifier to 50GHz', IEEE Microwave and Guided Wave Lett., Vol. 8, pp. 253-265, 1998

[6] T. Mathew, H.-J. Kim, D. Scott, S. Jaganathan, S. Krishnan, Y. Wei, M. Urteaga, S. Long, and M.J.W. Rodwell, '75GHz ECL static frequency divider using InAlAs/InGaAs HBTs', Electronic Lett., Vol. 37, pp. 667-668, 2001

[7] M. Dahlström, X.-M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y.M. Kim, Y. Wu, J.M. Fastenau, W.K. Liu, and M.J.W. Rodwell,

‘Widebandgap DHBTs using a graded Carbon-Doped InGaAS Base’, IEEE Electron Device Lett., Vol. 25, pp. 433-435, 2003

[8] W. Hafez, J.-W. Lai, M. Feng, ‘InP/InGaAs SHBTs with 75 nm collector and f/sub T/>500 GHz’, Electronics Lett., Vol. 39, No. 20, pp.1475-6, 2003

[9] Z. Griffith, M. Dahlström, M. Urteaga, M.J.W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, and W.K. Liu, ‘InGaAs/InP mesa DHBTs with simultaneously high ft and fmax, and low Ccb/Ic ratio’, submmited to IEEE Electron Dev. Lett.

[10] J. Song, M.R. Frei, J.R. Hayes, R. Bhat, and H.M. Cox, ‘Self-aligned InAlAs/InGaAs heterojunction bipolar transistor with a buried subcollector grown by selective epitaxy’, IEEE Electron Device Lett., Vol. 15, No. 4, pp. 123-125, 1994

[11] M. Sokolich, M.Y. Chen, D.H. Chow, Y. Royter, S. Thomas III, C.H. Fields, D.A. Hitko, B. Shi, M. Montes, S.S. Bui, Y.K. Boegeman, A. Arthur, J. Duvall, R. Martinez, T. Hussain, R.D. Rajavel, K. Elliot, and J.D. Thompson, InP HBT integrated circuit technology with selectively implanted subcollector and regrown device layers, 25th IEEE GaAs IC Symposium, San Diego, CA, USA, Nov. 2003

[12] K. Mochizuki, T. Tanoue, T. Oka, K. Ouchi, K. Hirata, and T. Nakamura, ‘High-speed InGaP/GaAs transistors with sidewall base contact structure’, IEEE Electron Device Lett., Vol. 18, pp. 562-564, 1997

[13] Y. Miyamoto, J.M.M. Rios, A.G. Dentai, S. Chandrasekhar, ‘Reduction of base-collector capacitance by undercutting the collector in GaInAs/InP DHBTs’, IEEE Electron Device Lett., Vol. 17, pp. 97-99, 1996

[14] H.C. Tseng and Y.Z. Ye, 'High performance, graded-base AlGaAs/InGaAs collector-up heterojunction bipolar transistors using a novel selective area regrowth process', IEEE Electron Device Lett., Vol. 20, pp. 271-273, 1999

[15] S. Yamahata, Y. Matsuoka, and T. Ishibashi, ' High fmax collector-up AlGaAs/GaAs heterojunction bipolar transistors with a heavily carbon-doped base fabricated using oxygen ion implantation', IEEE Electron Device Lett., Vol. 14, pp. 173-175, 1993

[16] Q. Lee, B. Agarwal, R. Pullela, D. Mensa, J. Guthrie, L. Samoska, and M.J.W. Rodwell, 'A > 400 GHz fmax Transferred-Substrate Heterojunction Bipolar Transistor IC Technology', IEEE Electron Device Lett., Vol. 19 No. 3, pp. 77-79, 1997

Chapter 2

InP HBT with Extrinsic Base Laterally Overgrown on SiO_2

2.1 Introduction

In InP heterojunction bipolar transistors (HBTs), the vertical layer optimization has led to very small intrinsic transit time. This has come about through the base and collector thinning as well as exploiting non-equilibrium carrier transport in the base and collector layers[1],[2],[3],[4]. It has hence become more important to reduce the parasitic elements such as series resistances and parasitic capacitances, which can limit the overall speed performance of HBTs. Among these parasitic elements, the base resistance (R_B) and base-collector capacitance (C_{BC}) are the most critical.

Heavy doping in the base layer is an effective way to lower the base resistance. However, many related problems exist, such as reduced current gain

due to decreased emitter injection efficiency and higher base recombination[5], lower device reliability, as well as dopant redistribution during epitaxial growth.[6] One promising way to avoid these difficulties is using heavily doped layer only in the extrinsic base region, since the extrinsic base resistance, including the base contact resistance, is usually the dominant part of the total base resistance. A selectively regrown extrinsic base structure is therefore effective in reducing the base resistance[7],[8]. In these regrown-base HBT structures, the extrinsic bases were heavily doped and were substantially thicker than the intrinsic base layer (Fig.2.1), and thus the extrinsic base resistance could be significantly reduced.

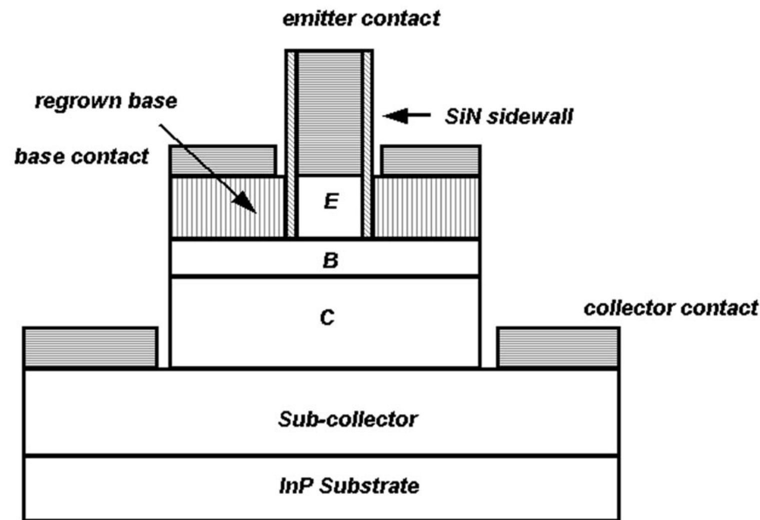


Fig.2.1 The schematic cross-section of the HBT with regrown-extrinsic base.

Although extrinsic base regrowth can effectively lower the base resistance, it cannot directly reduce the base-collector capacitance. It is therefore desirable to overgrow the heavily doped extrinsic base on buried SiO_2 surrounding the collector pedestal due to the low dielectric constant of SiO_2, as illustrated in Fig.2.2. By doing this, simultaneous reduction of R_B and C_{BC} will become possible.

Polycrystalline extrinsic base regrown on buried SiO_2 have been applied to AlGaAs/GaAs HBTs by Mochizuki *et al.*[9] Polycrystalline materials, however, have much higher resistivity than single crystal materials[10],[11],[12], since the carrier mobility in polycrystalline materials is usually one order of magnitude lower than that in crystalline materials with similar doping density. It is hence difficult to achieve low base resistance with polycrystalline materials. Single crystal extrinsic base overgrowth, on the other hand, can give much lower base sheet resistance and will be more effective in reducing the total base resistance.

The regrowth of single crystal extrinsic base on SiO_2 will be possible if large lateral overgrowth of InP/InGaAs materials can be realized. In this chapter, first selective growth of InP through SiO_2 openings by metal-organic chemical vapor deposition (MOCVD) is discussed and the dependence of lateral overgrowth on the opening width and orientation is presented and qualitatively explained. The lateral overgrowth technique is then applied to the fabrication of

regrown-base InP HBTs. Both DC and RF characteristics of the prototype devices are demonstrated.

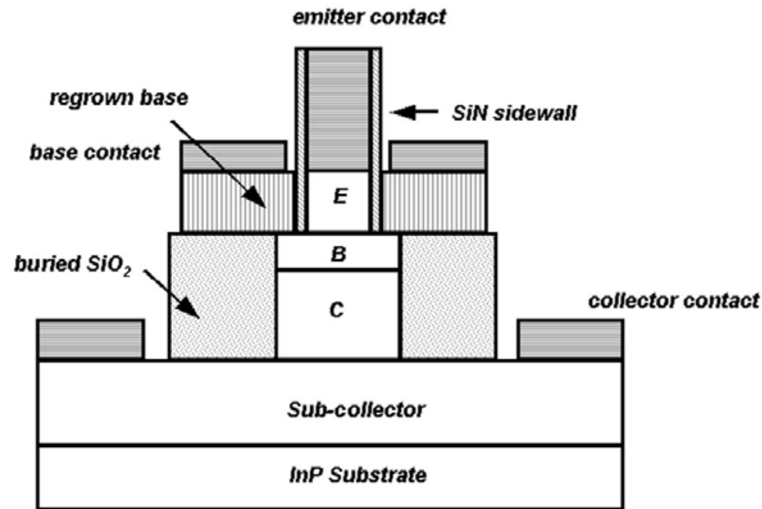


Fig.2.2 The schematic cross-section of the HBT with extrinsic base overgrown on buried SiO_2.

2.2 Epitaxial Techniques

2.2.1 Molecular Beam Epitaxy

Two growth techniques are pertinent to HBTs in this work. They are molecular beam epitaxy (MBE), the subject of this section, and metal-organic chemical vapor deposition (MOCVD), the subject of the next section.

MBE is a growth technique by which a specific number of atomic layers can be precisely grown. It allows the growth of abrupt interfaces, both in material composition and in intentional impurity doping profiles. The epitaxial growth takes place in an ultra vacuum chamber whose base pressure is maintained at ~10^{-8} to 10^{-10} torr. Fig.2.3 illustrates a schematic diagram of a high-vacuum MBE chamber.

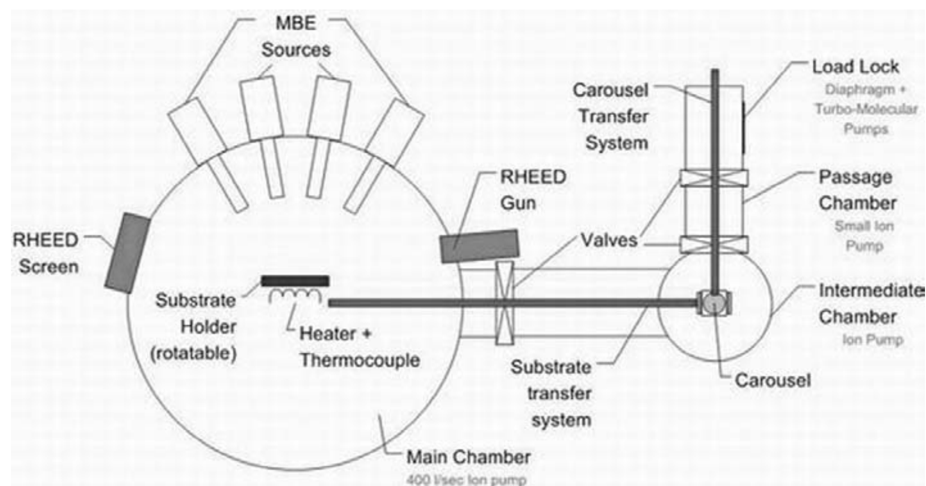


Fig.2.3 Schematic diagram of a typical high-vacuum MBE chamber.

A total of typically eight effusion cells (also known as furnaces) containing different solid sources materials face the target substrate. A shutter is equipped on each diffusion cell. After the source material is heated to its melting temperature, it is emitted out of the effusion cell once the shutter is opened. Because the chamber is maintained at ultrahigh vacuum, the evaporated source molecules do not collide with each other but form a molecular beam that

impinges directly on the semiconductor substrate mounted on the heater. The high temperature promotes the movement (through diffusion) of the impinging molecules around the substrate surface, allowing them to arrange themselves into proper crystalline sites. Since the shutter's switching time is short compared to the growth time for a single atomic layer, the exact number of atomic layers to be grown is accurately controlled.

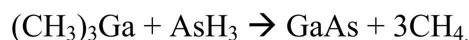
MBE growth takes advantage of the fact that Group V atoms impinging on the substrate surface immediately stick to the Group III atoms already present at the surface, until an atomic layer of Group V atoms is formed. Any additional Group V atoms that arrive after the formation of this atomic layer will not stick on the surface. This is not true for Group III atoms. If there are excess Group III atoms such as In atoms, the excess In atoms remain on the surface and eventually form an "In-rich" surface. The crystalline structure of InP is then lost. Therefore, a phosphorus overpressure is intentionally used during the growth of InP wherein both indium and phosphorus shutters are open. Since the adsorption of P atoms on a fresh In surface takes negligible time, the In flux determines the growth rate. The growth of InP results in successive completion of a layer of In, then a layer of P, as so on. The substrate for growth is normally in [100] orientation. In this direction, any particular single layer contains only either In or P atoms, consistent with the natural growth mechanism just described.

A calibration of growth rate can be done with a reflection-high-energy-diffraction (RHEED) assembly, which consists of an electron gun on one side of the chamber and a phosphorus screen on the opposite side. The RHEED intensity oscillates as monolayers of materials are grown. Each oscillation period indicates a completion of monolayer.

MBE growth at UCSB is done with computer-controlled furnace temperatures and shutter switching. The computer control allows reproducible growth of precise layer structures. Before each growth the flux of each source is measured with a beam flux monitor, which is located behind the substrate, as shown in Fig.2.3. The desired furnace temperatures are set in order to achieve the desired fluxes. This reduces the layer thickness error since as the source material is being consumed with time, the flux of a given source material changes for a specific furnace temperature.

2.2.2 Metal-Organic Chemical Vapor Deposition

The operation of MOCVD is more complicated than that of MBE, involving several complex chemical reactions. A basic chemical reaction in MOCVD is that between a metal-organic compound and a hydride. For example, when trimethyligallium vapor is mixed with arsine over a high-temperature substrate, GaAs is formed along with a gaseous by-product (methane)



$$(CH_3)_3Ga + AsH_3 \rightarrow GaAs + 3CH_4.$$

The substrate temperature in MOCVD is in the range of 550°C to 650°C. All constituents inside the growth chamber are in the vapor phase. A mass flow controller is used to regulate the gas slow and thereby control the growth rate. A horizontal MOCVD reactor is schematically shown in Fig.2.4.

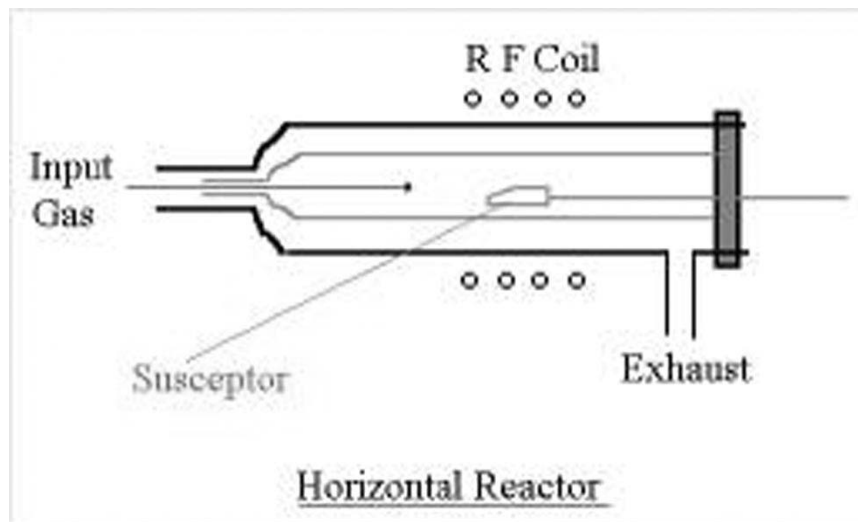


Fig.2.4 Schematic diagram of a horizontal MOCVD reactor.

It is mentioned previously that in MBE growth, the P atoms impinging on the InP surface immediately stick to the InP atoms already there, until an atomic layer of P is formed. Having excess P fluxes ensures that MBE growth is determined solely by the In atom flux and prevents the growth surface from entering the In-enriched condition. Similarly, in MOCVD growth. The growth proceeds in an environment with excess PH_3. The growth rate of InP within a

specified temperature range is limited by the diffusion of TMIn to the wafer surface and becomes linearly dependent on the TMIn concentration.

The usual p-type dopants include diethylzinc (DEZn), trimethylaresine (TMAs), and tetrachloride (CCl_4). DEZn is the only p-type dopant available in the InP MOCVD system at UCSB. The zinc in DEZn is the element that actually dopes the semiconductor. Zinc, unlike carbon, has a relatively high diffusion coefficient, similar to Be used in MBE.

Just as in MBE, the preferred wafer orientation for MOCVD growth is along the [100] direction. In-situ growth monitors such as RHEED are not available in MOCVD. Calibration of the epitaxy growth rate in a MOCVD run typically requires wet etching of the calibration samples.

Many efforts have been made to investigate the feasibility to use MOCVD do selective growth in mask areas on GaAs or InP substrate. Compared with MOCVD, the selective growth by conventional MBE is very difficult due to the high sticking coefficient of Group III materials on the mask. Nevertheless, selectivity in MBE has been achieved by periodic supply molecular beam epitaxy (PSE/MBE)[13] and the lateral overgrowth has also been realized by using the low angle incidence microchannel epitaxy (LAIMCE) in MBE system.[14]

2.3 Epitaxial Lateral Overgrowth of InP on SiO_2

2.3.1 Overview

Almost all compound semiconductor devices consist of two or more of the suitable semiconductor layers grown on a substrate. A grown layer is refered to as an epitaxial layer if it has the same crystallographic lattice dimensions as the substrate. Usually the epitaxial layer is exactly lattice matched to the substrate, although layers with the deviation of their lattice parameters as large as 0.05% are generally refered to as lattice matched. A large lattice mismatch induces stress, which in turn causes strain especially in the grown layers. This leads to the generation of defects at the interface that can be mobile enough to reach the surface.

In standard definition, heteroepitaxy denotes the epitaxial growth of a material that is different from the substrate on which it is grown. E.g., epitaxy of $In_{0.53}Ga_{0.47}As$ on InP is considered as heteroepitaxy since they are lattice matched but chemically different. Today the term heteroepitaxy is often instead employed to denote the growth of a material whose lattice parameter differs from that of the substrate, e.g. GaN on sapphire, InP on GaAs, InP on SiO_2 etc.

In heteroepitaxy one would expect material growth with high defect density. However, several defect-engineering approaches have been taken to suppress those defects. These include: 1) Growth of very thick layers – in this case the grown layer is sufficiently thick that the defects generated at the interface do not

propagate up to the surface and hence a part of the layer at the top is free of defects. 2) Epitaxial lateral overgrowth – in this case, the growth starts on the open surface, and when the layer reaches a particular thickness, the layer starts to grow laterally from the opening on the masked region. 3) Compliant substrate – compliant substrates offer a new approach to strain management in lattice-mismatched structures. The role of the compliant substrate is to reduce the strain in a mismatched overlayer by sharing the strain via deformation of the substrate, or by nucleating and confining defects in the substrate. This is done either by direct bonding or twist bonding of an appropriate layer on a substrate. In our work, the epitaxial lateral overgrowth approach has been adopted to grow InP on SiO_2. The lattice mismatching in this system is ~8%.

Epitaxial lateral overgrowth has been studied and applied to various devices[15],[16],[17],[18],[19],[20],[21]. Selective area growth of InP and related materials is gaining importance in the fabrication of several advanced optoelectronic devices. However, few attempts have been made to investigate the selective growth of InP with a focus on fabricating electronic devices.

In our efforts to laterally overgrow an InP HBT's extrinsic base on buried SiO_2 layer, the seed area for the base lateral overgrowth is limited by the HBT's scaling requirements: the extrinsic base regrowth seed area needs to be narrower than normal base metal contact width for effective base-collector capacitance

reduction. For this reason, our studies on the InP lateral overgrowth are focused on the growth through very narrow seed area (less than 1μm wide).

Since the UCSB InP MOCVD system's susceptor rotational speed was only 200 rpm, the selective area growth of InGaAs is difficult. With low susceptor rotational speed, the gas-flow speed just above the susceptor is slow due to the smaller centrifugal force generated by the low-speed rotation. Therefore, the residence time of the material molecules adjacent to the susceptor is longer. This position also has the highest temperature in the gas phase. As a result, the pyrolysis of the source molecules in the gas phase is less restrained, which leads to low growth selectivity. Initial tests showed that many polycrystalline InGaAs particles were deposited on the SiO_2 regrowth mask even when high growth temperature was used. Selective growth tests of InP were much more successful. With InP growth, very few polycrystalline particles were found on the SiO_2 mask after the regrowth. This clean regrowth was mainly due to the higher mobility of In atoms than Ga atoms. To obtain better regrowth selectivity, InP was therefore selected to be the majority of the laterally regrown base. For the same reason, most of the selective growth experiments in this thesis use InP.

2.3.2 Crystallographic Structures of Zinc Blende

Knowledge of the crystallographic structure of semiconductor is essential for understanding the process of epitaxy during the lateral overgrowth. InP

crystallizes in a zinc blende (sphalerite) lattice. The zinc blende structure consists of two interpenetrating, face centered cubic (fcc) sublattices consisting of only indium and phosphorous atoms in each sublattice. Each sublattice is shifted by a/4 [111] relative to the other fcc sublattice, where a is the length of the fcc lattice constant. The zinc blende structure of InP is shown in Fig.2.5, where open circles are indium atoms and solid circles are the phosphorus atoms.

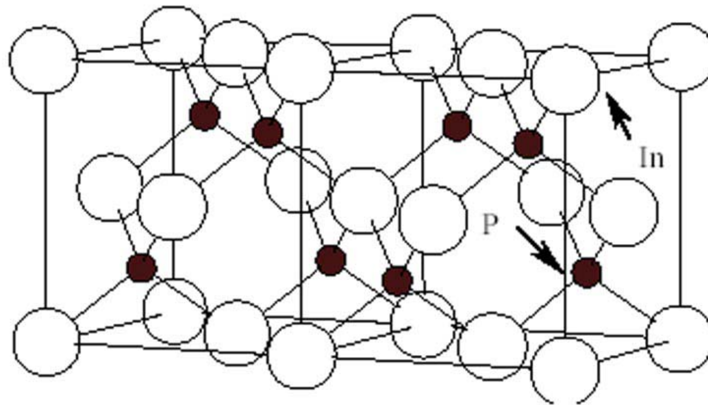


Fig.2.5 Schematics of InP lattice structure.

The most common surface used for the growth of III-V's on InP and GaAs is (100). The {100}, {011}, and {111} basic planes in III-V compounds are of particular interest. The properties of these surfaces strongly influence III-V semiconductor growth. Other surfaces with higher Miller indices can be resolved on an atomic scale into stepped structures built up from combinations

of these three basic set of planes. Knowledge on the properties of these basic planes will facilitate the understanding of InP's lateral overgrowth behavior.

An ideal {100} plane is shown in Fig.2.6. It consists of alternating planes of indium and phosphorus atoms. The indium and phosphorus planes are geometrically equivalent and are equally spaced. Each In (P) atom in In (P) plane is bonded downward into the crystal to two P (In) atoms. Under typical growth conditions in MOCVD system, where V/III ratio is larger than unity, the growth can be treated as indium incorporation limited, since under the condition of excess PH_3, total adsorption of phosphorus atoms takes place readily. The growth on {100} plane can be seen as layer-by-layer growth, and there is no substantial nucleation barrier for crystal growth on {100} planes.

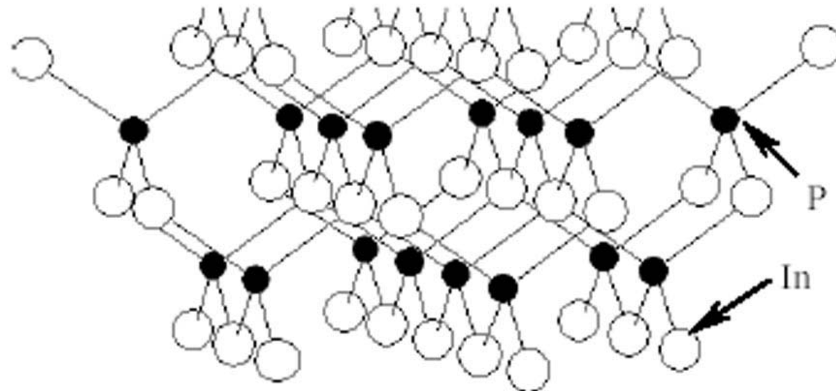


Fig.2.6 Atomic structure of {100} planes in InP crystal.

The atomic structure of the {011} planes is shown in Fig.2.7. The {011} planes contain equal number of In and P atoms. The atoms in {011} planes form zigzag chains, each atom being bonded to two adjacent atoms in the chain, with its other two bonds extending out on each side to the remaining tetragonal position. It can be difficult to nucleate growth of new atomic planes on {011} facets because incorporating each new indium atom can add two dangling bonds. Here the addition of indium atoms can be considered to control the growth, since under the conditions of excess PH_3, total adsorption of phosphorous atoms takes place readily. Once the first atom is in place, atoms of the opposite type can be deposited adjacent to it without adding the dangling bonds.

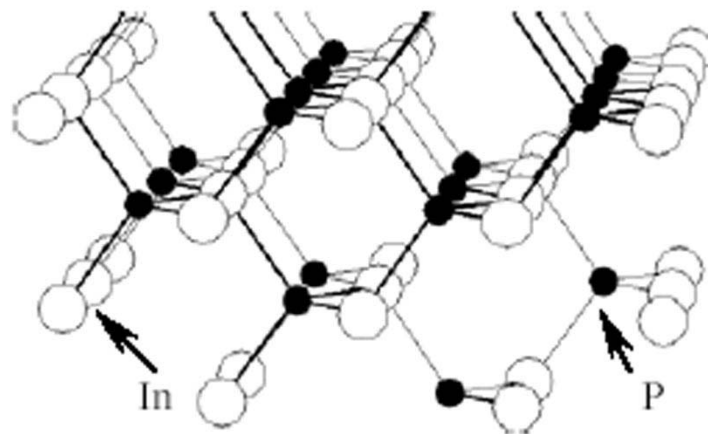


Fig.2.7 Atomic structure of {011} planes in InP crystal.

The structure of {111} planes is shown in Fig.2.8. This family of planes is significant for understanding the growth profile in the epitaxial lateral overgrowth of InP. The {111} double layer contains two closely spaced planes of In and P atoms which are denoted as {111}A and B planes, respectively. Each atom in a given plane has three bonds to atoms in the other plane. The fourth bond extends normal to the plane of the double layer to connect to an atom in the next such double layer. Since the two sides of the {111} layer are not chemically equivalent, a crystal bounded by such facets would be expected to show phosphorus polarization effects during the selective growth. Growth on {111}B planes is lethargic in a phosphorus rich vapor ambient, because further attachment of In atoms at {111}B planes will add two dangling bonds. It means that In atoms have to overcome high energy barrier in order to deposit on {111}B planes.

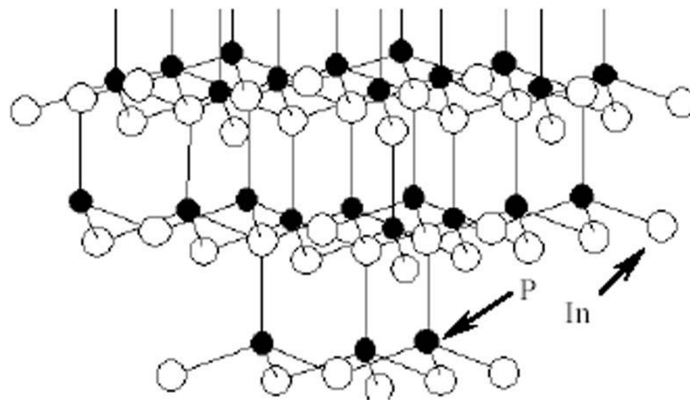


Fig.2.8 Atomic structure of {111} planes in InP crystal.

2.3.3 InP Lateral Overgrowth Experiments and Results

In our initial regrowth experiments, the regrown material showed strong faceting when the openings were aligned to the [011] direction, the direction along which the InP HBT emitters are usually aligned. It was observed that the growth facets were bounded by (1-11)B and (11-1)B planes and formed a pyramidal shape without any lateral overgrowth on SiO_2. These behaviors strongly suggested that the lateral overgrowth had significant orientation dependence.

To investigate the lateral overgrowth's orientation dependence, test patterns of SiO_2 opening stripes at various rotations were used, as illustrated in Fig.2.9.

Fig.2.9 Schematic of growth angle patterns of SiO_2 stripes.

Growth experiments were performed using this pattern. First, radial stripes of SiO_2 mesa stripes were formed on (100) InP substrate by plasma-enhanced chemical vapor deposition (PECVD) and subsequent reactive ion etching (RIE) with SF_6/Ar gases. The central mesa stripe in the test pattern was aligned perpendicular to the major flat. The mesas were 0.8 µm tall, 2 µm wide and were indexed at 5° intervals. A thin layer of SiO_2 regrowth mask (1000Å) was then deposited and lifted-off on both sides of the tall SiO_2 mesa. The opening width between the central mesa and regrowth mask was varied from 0.5 to 4 µm. The central SiO_2 mesa is designed to emulate the tall emitter mesa of an InP HBT, while the thin SiO_2 regrowth mask emulates the buried SiO_2 layer which would surround the collector pedestal. Projection lithography patterned the radiant stripes and the alignment accuracy between the tall SiO_2 mesa and thin SiO_2 regrowth mask was within ±0.1µm.

The selective growth of InP was performed in a horizontal MOCVD reactor at 350 torr using trimethylindium and tertiarybutylphosphine as source materials. First 250 Å InP was grown at 550ºC with V/III ratio of 100, then 2250Å InP was grown at 615ºC with V/III ratio of 50. The first 250 Å InP layer was grown at a low temperature with high V/III ratio to help initiate the growth in the openings. It was found that the growth of this thin layer under such conditions helped improve the quality of the subsequent selective growth. Since our MOCVD system's susceptor rotational speed was only 200 rpm, relatively high growth

temperature (> 600ºC) was chosen for the rest of the selective growth to suppress the generation of polycrystalline particles on the mask. Fig.2.10 shows the top view of the sample after growth.

The sample was cleaved along [01-1] direction after growth. The scanning electron micrograph (SEM) image in Fig.2.11(a) shows the cross-section of the InP deposits grown through stripe openings aligned to [011] direction. As illustrated in Fig.2.11(b), the growth facets in Fig.2.11(a) are bounded by the low index planes: (100), (1-11)B and (11-1)B without any obvious overgrowth of InP on the SiO2 mask.

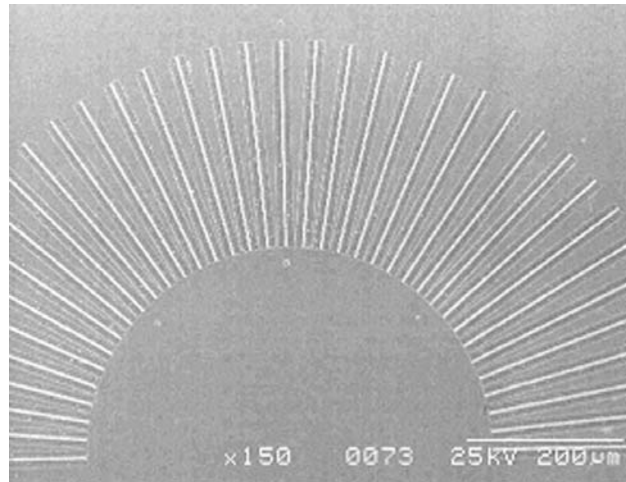


Fig.2.10 SEM image of the selective growth through the radial line openings on an InP substrate.

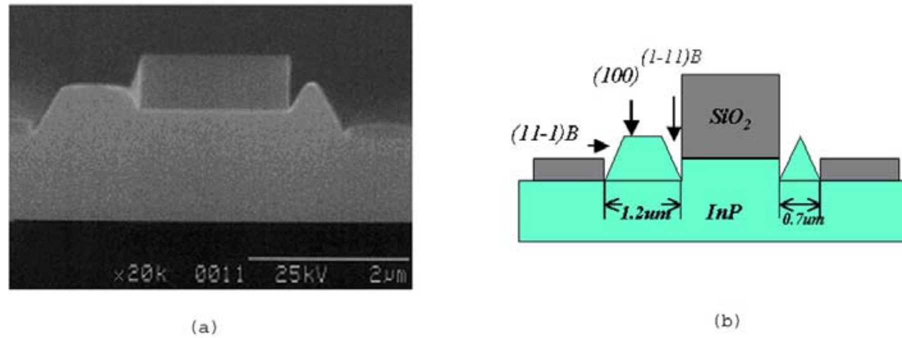


Fig.2.11 (a) SEM cross-section image the selective growth through opening along [011] direction. (b) Schematic of growth through [011] oriented opening.

Fig.2.12 shows the SEM cross-section image of the deposit through an opening aligned 30º from the [011] direction. Although the thin SiO_2 mask cannot be seen clearly, the width of the InP deposit through the opening is clearly larger than the opening width (0.5μm). This shows that there is lateral growth of InP over the SiO_2 mask even though no nucleation site exists on SiO_2. From Fig.2.12 it is also clear that the boundary planes of the regrown InP are no longer {111}B planes.

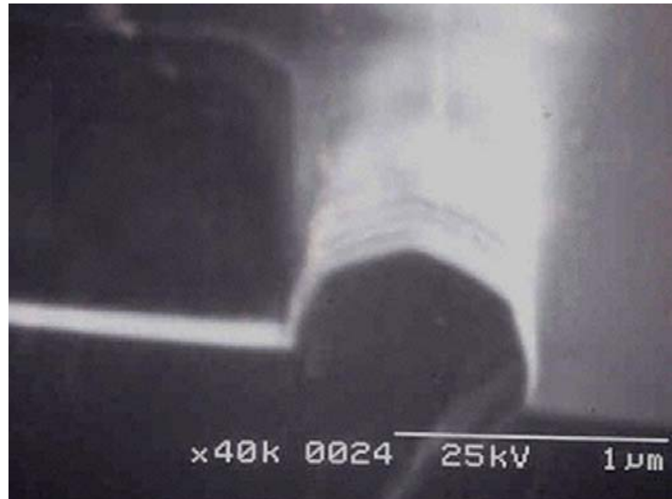


Fig.2.12 SEM cross-section image of the selective growth through a 0.5μm opening 30° off [011] direction.

In order to systematically investigate the lateral overgrowth's orientation dependence, the lateral overgrowth length was measured at 5° intervals using SEM. The data, plotted as a function of the opening's orientation and width, is shown in Fig.2.13. The lateral overgrowth length, as expected, has strong dependence on opening orientation, with minima occurring at the major low-index directions: [001], [011] and [01-1]. This growth behavior agrees well with that reported for selective growth of thick InP through wide openings by HVPE[22].

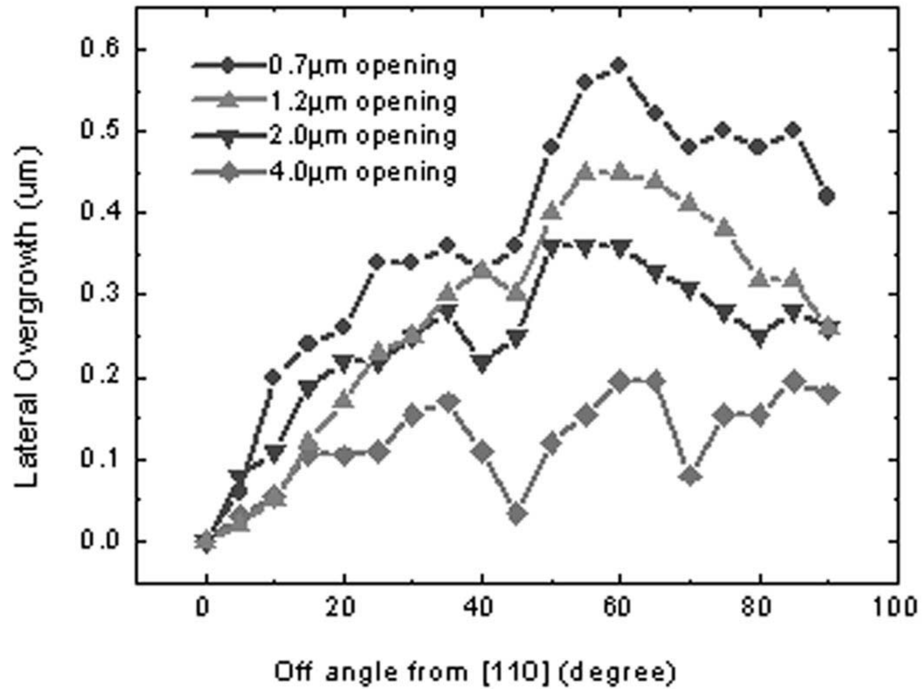


Fig.2.13 Dependence of lateral overgrowth length on opening orientation and width.

From Fig.2.13 it is also seen that the lateral overgrowth length increases with decreasing opening width. At 60° orientation of [110], the lateral overgrowth length through the 0.7 μm wide opening is almost 0.6 μm, while the lateral overgrowth length through the 4μm wide opening is less than 0.2 μm. Similar lateral overgrowth experiments were also performed on InGaAs surfaces. Very similar behaviors have been observed.

2.3.4 Qualitative Explanations for Lateral Overgrowth Behaviors

The dependence of lateral growth on mask opening width and orientation can be qualitatively explained by the Burton-Cabrera-Frank (BCF) growth model[23]. When the stripe opening is rotated away from the low index directions, as illustrated in Fig.2.14, the growth boundaries become high-index vicinal planes, which have high density of steps at the growth front over the SiO_2 mask. These crystallographic steps on boundary plane can supply the seed for continuous lateral growth over the SiO_2 mask, although there is no nucleation site on the mask. The high step density on the vicinal sidewall surface therefore increases the lateral growth rate if the mass transport rate from the gas phase is fast enough to support it.

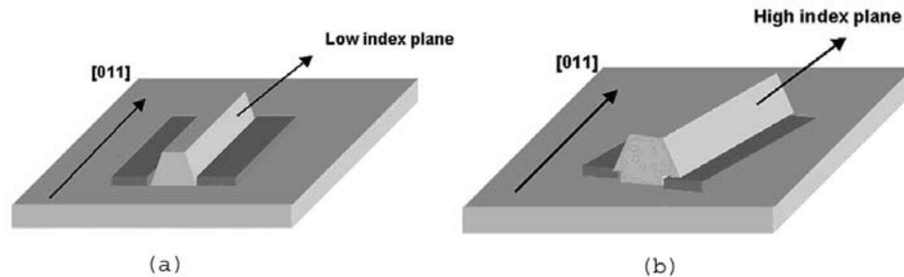


Fig.2.14 Schematics of regrowth when the opening is (a) along [011] direction and (b) away from [011] direction.

The dependence of lateral overgrowth on mask opening width can be similarly explained. Through narrow openings, the vertical growth requires less mass transport. As a result, this allows more of the material arriving on the top surface and the mask area to migrate to the sidewall and be incorporated in the sidewall growth. As illustrated in Fig.2.15, this can result in increased lateral overgrowth on the SiO_2 mask.

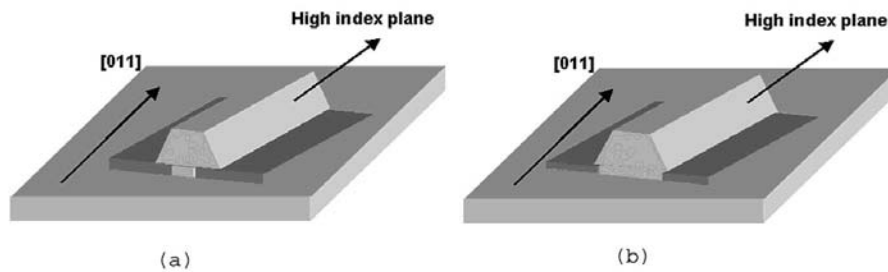


Fig.2.15 Schematics of regrowth with (a) narrow and (b) wide opening aligned away from [011] direction.

2.4 InP HBT with Laterally Overgrown Base on Buried SiO_2

As discussed earlier, for HBTs with a laterally overgrown extrinsic base it is desirable to keep the regrowth window between the emitter mesa and the buried SiO_2 as narrow as possible to reduce the base collector capacitance. Considering

this, the following device structure for extrinsic base regrowth was proposed. As shown in Fig.2.2, the base mesa can be etched down to the subcollector, leaving a narrow base shoulder. SiO_2 can then be deposited to surround the collector pedestal. This defines an intrinsic base-collector junction area only slightly larger than the emitter-base junction area, this bringing a significantly reduced C_{BC}. The base shoulder also provides a narrow opening for the subsequent selective growth to facilitate the lateral overgrowth of the extrinsic base. To obtain the largest lateral overgrowth length for the extrinsic base, the emitter stripes can be aligned 60° off [011] direction.

The following sections discuss the growth and process steps used to realize this device structure.

2.4.1 Intrinsic HBT Material Structure and Growth

The intrinsic HBT structure was grown on a Fe-doped semi-insulating (100) InP substrate using solid-source MBE. The layer structure is listed in Table 2.1.

Since the base lateral regrowth process was still under heavy investigation and far from mature, a relatively simple HBT layer structure was adopted to avoid complicating the device fabrication to facilitate problem shooting.

The InGaAs base used in this structure was 550 Å thick , and was Be-doped at $4x10^{19}$ cm^{-3}. The top 50 Å InGaAs was undoped to alleviate the diffusion of

Be dopants into the emitter. From the hall measurements on the doping calibration samples, the hole mobility in the base layer was 55 cm^2/VS.

Layer	Material	Thickness (Å)	Doping (cm^{-3})
Cap	n+ InGaAs	600	Si: $2x10^{19}$
Emitter	n+ InP	300	Si: $2x10^{19}$
	n InP	700	Si: $2x10^{17}$
Base	InGaAs	50	Undoped
	p+ InGaAs	500	Be: $4x10^{19}$
Collector	n- InGaAs	3000	Si: $1x10^{16}$
Subcollector	n+ InGaAs	4000	Si: $2x10^{19}$

Table 2.1 Epitaxial layer parameters of the intrinsic HBT region.

The InGaAs emitter cap was N+ doped with Si at $2x10^{19}cm^{-3}$, and 600 Å thick. The InP emitter was 1000 Å thick with the first 700 Å Si-doped at $3x10^{17}cm^{-3}$ and the remainder doped at $1x10^{19}$ cm^{-3}. The InGaAs collector was 3000Å thick and doped with Si at $1x10^{16}$ cm^{-3}. The N+ InGaAs subcollector was heavily doped at $2x10^{19}$ cm^{-3} to achieve low collector access resistance. Fig.2.16 shows the band diagram associated with the HBT layer structure under forward

bias. The bias conditions are: emitter-base voltage $V_{BE} = 0.7$ V, emitter-collector voltage $V_{CE} = 1.5$ V.

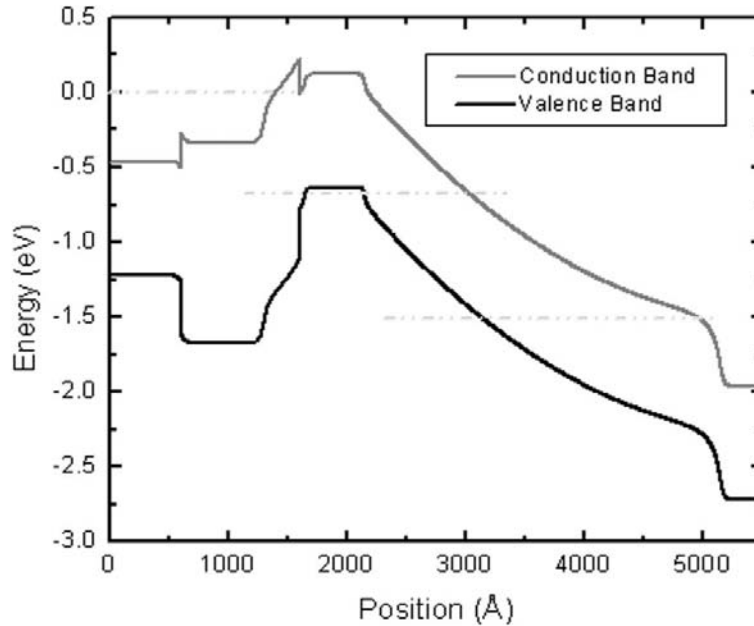


Fig.2.16 The band diagram of the HBT's layer structure under forward bias.

2.4.2 HBT Fabrication Process

After the MBE epitaxial growth, tungsten was used as refractory emitter electrode by RF sputtering and subsequent reactive ion etching (RIE) with SF_6:Ar gases. The tungsten thickness was 1.0 μm. A 400 Å Ni layer was deposited and lifted-off on the tungsten layer to be used as the etching mask.

Relatively low gas pressure (10mτ) and high bias voltage (300V) were used during the tungsten RIE to reduce the etch undercut. From Fig.2.17 it can be seen that the tungsten emitter metal undercut was controlled within 0.1μm.

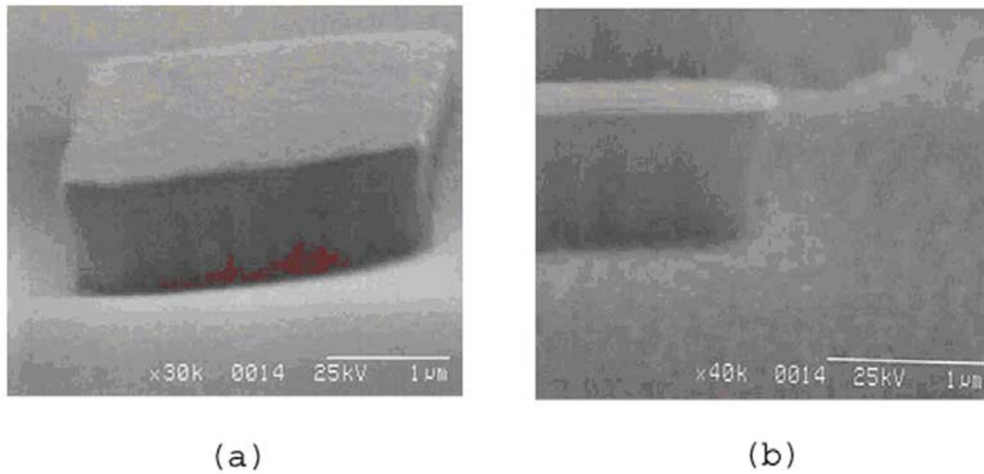


Fig.2.17 SEM pictures of the emitter lateral profiles after tungsten dry etch.

After the tungsten dry etch, the InGaAs emitter cap and InP emitter layers were wet etched and a SiN sidewall was formed around the emitter electrode and emitter layers to prevent short between regrown extrinsic base and emitter. The sidewall was formed by SiN PECVD deposition and subsequent reactive ion etching. Fig.2.18 shows the SEM picture of an emitter mesa covered by SiN sidewall.

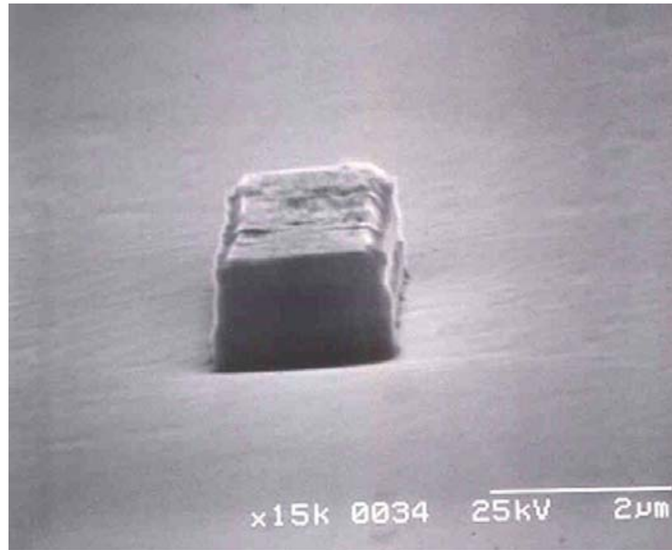


Fig.2.18 SEM picture of an emitter mesa after SiN sidewall formation.

After the emitter sidewall formation, lithography was performed and the emitter was covered by photoresist 0.6 μm wider than the emitter mesa on both sides. The base mesa was then reactive-ion etched down to the subcollector. Following this 3500 Å SiO_2 regrowth mask was deposited by electron beam deposition and then lifted-off. A narrow base opening (the extrinsic base regrowth seed area) between the emitter mesa and the SiO_2 mask was therefore formed. The edge profile around the base opening was measured and the refilled SiO_2 surface was found to be smooth and aligned with the base opening surface very well. The height difference between the SiO_2 surface and the base opening

surface was within 200 Å. Fig.2.19 shows the SEM top view of a device after buried SiO_2 was deposited and lifted-off.

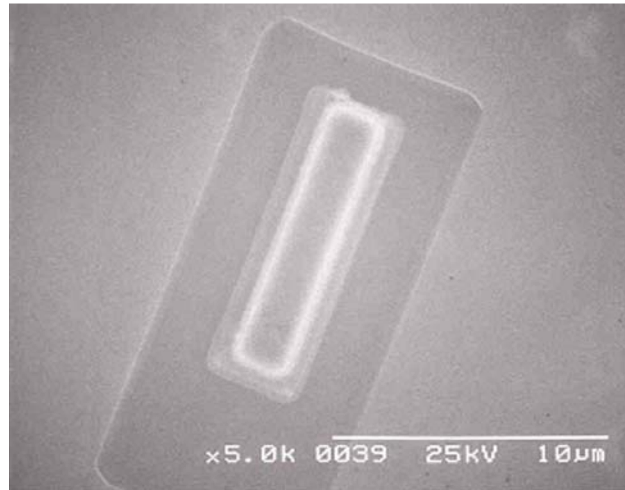


Fig.2.19 SEM top view picture of a device after buried SiO_2 deposition and liftoff.

The base selective regrowth was subsequently performed and the regrown layers consisted of a 250 Å InP layer grown at 550ºC with a V/III ratio of 100, a 1500 Å InP layer grown at 615ºC with a V/III ratio of 50 and a 250 Å InGaAs layer grown at 615ºC. This extrinsic base was heavily doped with Zn to achieve low extrinsic base resistance. The extrinsic base's lateral overgrowth length was found to be ~0.5µm, which was comparable to the result of a lateral overgrowth experiment using a 0.7µm mask opening oriented 60° from the [011] direction (Fig.2.13).

After forming Pd/Ti/Pd/Au base electrodes using the liftoff technique, the base collector mesa was formed by wet etching. The collector electrode of Ti/Pt/Au was then deposited, and finally the HBTs were isolated by wet etching down to the semi-insulating substrate. After passivating the device with polyimide and making contact holes through it, pad metals (Ti/Au) were fabricated by liftoff. The transmission line was aligned along the major flat direction, while the emitters were rotated 60º away from [011] direction. Fig.2.20 shows a SEM picture of the finished device.

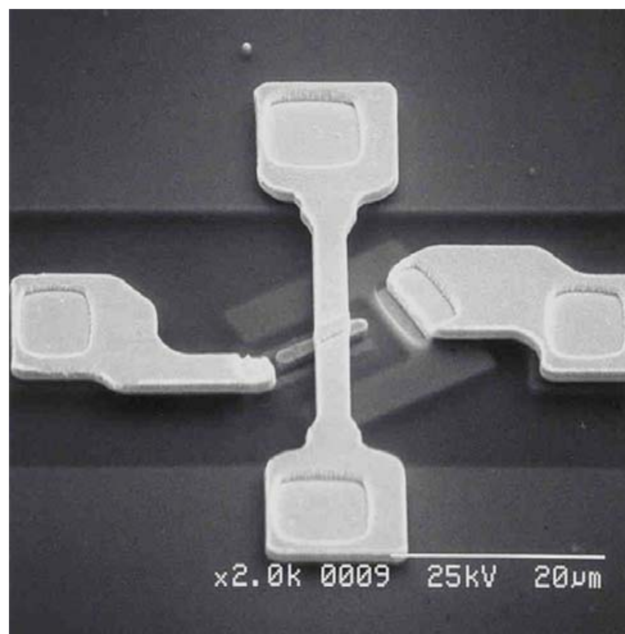


Fig.2.20 SEM picture of the finished HBT with lateral base regrowth.

2.4.3 DC Measurements of the Regrown Base HBTs

DC characterization includes Gummel plots and DC common-emitter characteristics. These were measured by a semiconductor parameter analyzer using microwave probes, bias-T, and 50Ω transmission lines to prevent microwave device oscillation during DC measurements.

Shown in Fig.2.21 are the Gummel plots of a regrown-base HBT and a conventional HBT with the same layer structure and junction dimensions. Both HBTs have 1x10 μm^2 emitter area. The base and collector current ideality factors of the regrown-base HBT are 1.93 and 1.33, while the ideality factors of the conventional HBT are 1.45 and 1.28. When V_{CE} is 1.5V, the DC current gain is 15 for the regrown-base HBT and 48 for the conventional HBT

The large recombination current resulted in the low current gain and high base-current ideality factor for the regrown-base HBT. The origin of this excess base current at low current density could be attributed to the process-induced surface damages of the p-InGaAs prior to the regrowth, particularly the damages caused by the RIE etch during the SiN sidewall formation, and the interface degradation during the regrowth.

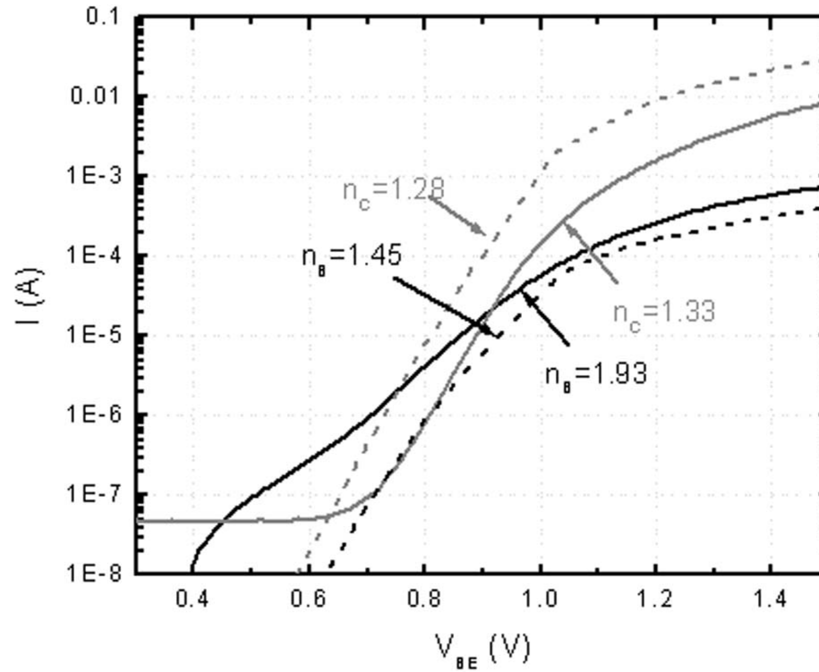


Fig.2.21 Gummel plots of the regrown-base HBT (solid line) and the conventional HBT (dashed line) with the emitter size of 1x10 μm^2.

From the Gummel plots it was also found that V_{be} at a given I_C is ~100mV larger for the regrown-base HBT. This larger turn-on voltage could be attributed to the Be and Zn out-diffusing into the emitter-base setback layer during the selective regrowth. To qualitatively estimate the influence of the Zn diffusion on the turn-on voltage, we numerically calculated the band diagrams using the simulation tool Bandprof. The results are shown in Fig.2.22. Our band diagram simulation was based on the assumption that Be and Zn atoms diffused into InP emitter layer and caused the 50 Å emitter layer immediately above the

emitter-base junction to become p-doped at $1x10^{17}cm^{-3}$. It is clear from Fig.2.22 that p-type dopant diffusion can induce an increase in the emitter-base conduction band potential barrier, which can explain the regrown base HBT 's increased V_{be}. To suppress this p-type dopant out-diffusion, the use less diffusive dopants for the intrinsic base layer, such as carbon, would be effective. More importantly, the setback layer could be eliminated if diffusive dopants are avoided.

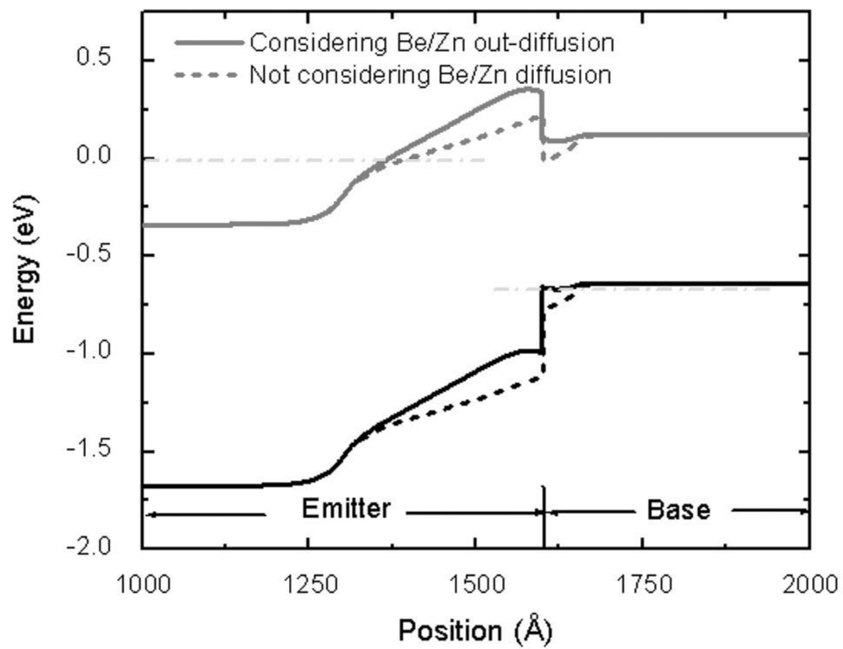


Fig.2.22 Band diagram of emitter-base junction with and without considering the p-type dopant diffusion during the base regrowth.

The common-emitter characteristics of the same regrown-base HBT are shown in Fig.2.23. It can be seen that the V_{CE} offset voltage is relatively high. This could be attributed to the device's single-heterojunction structure, abrupt emitter-base junction, as well as the larger base-emitter turn-on voltage caused by the p-type dopant out-diffusion.

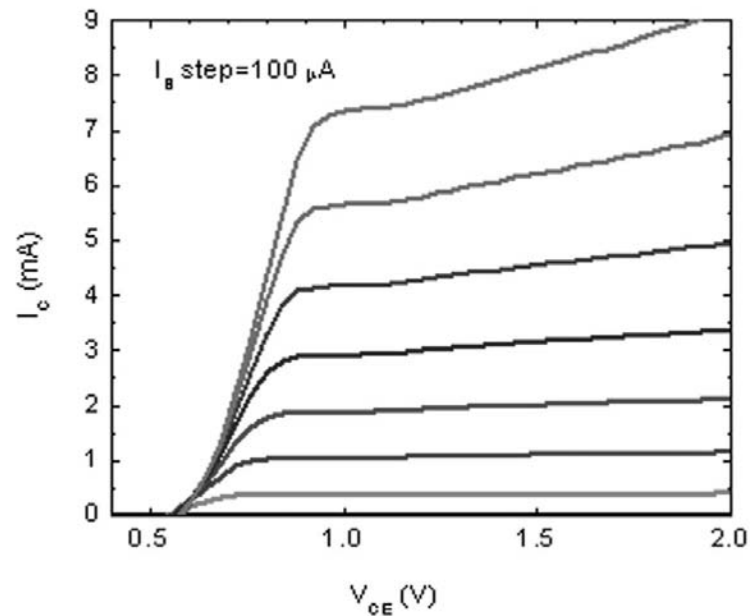


Fig.2.23 Common-emitter characteristics for 1x10 μm^2 device.

2.4.4 RF Measurements of the Regrown Base HBTs

The microwave performance of the HBT was characterized by measuring S-parameters with on-wafer probing from 0.5 to 40 GHz. The total base-collector

capacitance (C_{BC}) was calculated from the imaginary part of the 2 port parameter Y_{12}. Fig.2.24 shows the measured C_{BC} as a function of V_{CE} at I_C=10mA. For the regrown-base HBT with 1x10 μm^2 emitter size and 130 μm^2 base-collector junction area, the value of C_{BC} saturated at the high voltage is 25fF. For conventional HBTs, C_{BC} was found to saturate at 60fF at the same current. Clearly a 60% reduction of C_{BC} has been achieved by reducing the base-collector junction width and overgrowing the extrinsic base on buried SiO_2.

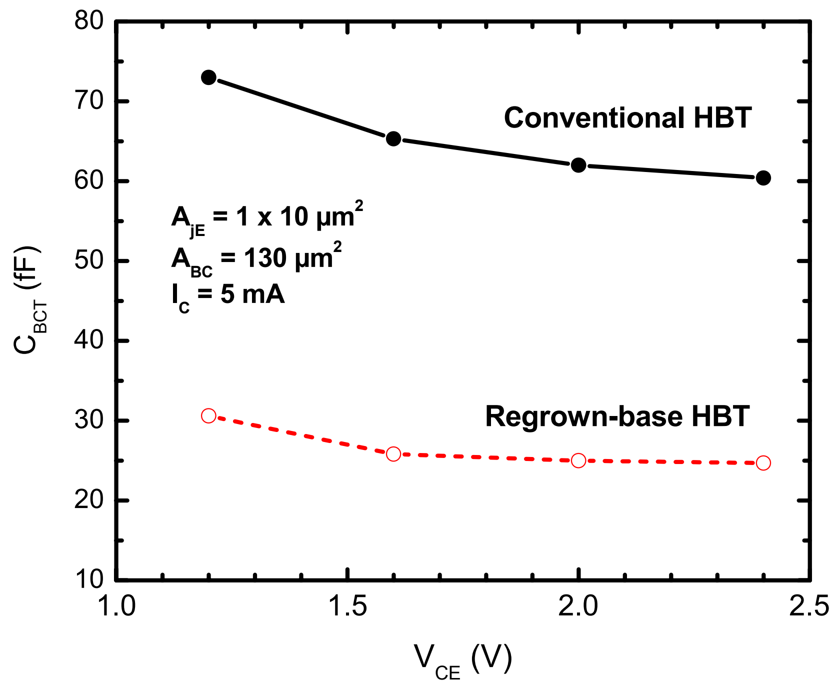


Fig.2.24 Bias dependence of the total base-collector capacitance of conventional and regrown-base HBTs.

Fig.2.25 shows the frequency-dependence of the current gain and Mason's unilateral gain for a 1x10 μm^2 HBT with regrown base at I_C = 10mA and V_{CE} = 1.5V. The cutoff frequencies f_T = 113GHz and f_{max} = 84GHz were obtained through assuming a -20 dB/decade frequency-dependence of current gain and unilateral gain. At the same current and collector bias, f_T = 115GHz and f_{max} = 95GHz were measured for the conventional HBT without base regrowth. It can be seen that the f_T values for conventional and regrown-base HBTs are very close, while regrown-base HBT's f_{max} is ~10% lower than conventional HBT's in spite of regrown-base HBT's significantly reduced base-collector capacitance. The f_{max} value of the regrown-base HBT is mainly limited by its large base contact resistance. Table 2.2 lists the base sheet and contact resistivity values of both regrown and conventional HBTs from the transmission line model (TLM) analysis. As expected, the base regrowth significantly reduces the extrinsic base's sheet resistance. However, the contact resistivity on the regrown extrinsic base is much higher than that on the intrinsic base. This was caused by the low maximum p-level attainable with MOCVD when using Zn as acceptor dopant at relatively high growth temperature. In our regrown extrinsic base the p-type doping density was only $1x10^{19}cm^{-3}$, which was obviously not high enough to achieve low base contact resistance. Due to the susceptor rotational speed limit of our MOCVD system, the growth temperature cannot be further lowered. Otherwise the selectivity of the base regrowth would be significantly reduced.

Under this circumstance, to obtain higher p-doping in the extrinsic base, especially near the extrinsic base surface, post-growth Zn diffusion can be a very effective and controllable technique[24]. Improved microwave performance is expected if post-growth Zn diffusion can be successfully applied to our base regrowth process.

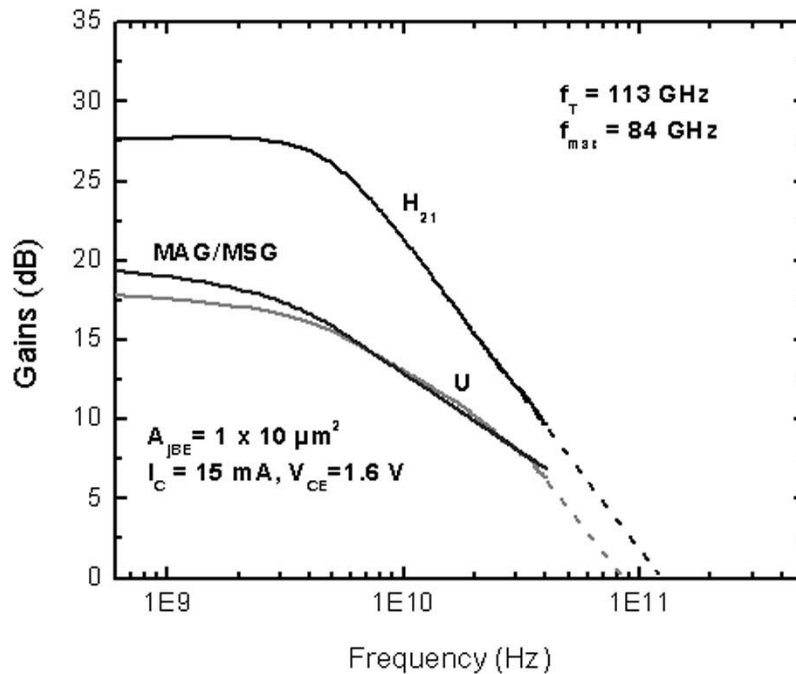


Fig.2.25 Frequency dependence of current gain(H_{21}), Mason's unilateral gain(U) and maximum stable gain/maximum available gain (MSG/MAG) at Ic=10mA, V_{CE}=1.6V.

	Sheet Resistance (Ω/□)	Contact Resistivity (Ω-cm^2)
Conventional HBT	550	9.0×10^{-7}
Regrown-base HBT	340	1.5×10^{-5}

Table 2.2TLM measurement results from the base layers of conventional and regrown-base HBTs.

2.5 Summary

To realize the InP HBT with extrinsic base laterally overgrown on buried SiO_2 for the simultaneous reduction of base-collector capacitance and base resistance, we have investigated the selective growth of InP by MOCVD through narrow mask openings by MOCVD. It is found that the lateral overgrowth of InP on SiO_2 is strongly dependent on both the opening width and orientation. The lateral overgrowth length reached the maximum at 60° off [011] direction and the minima along the major low index directions. The lateral

overgrowth also showed a increasing overgrowth length increasing with decreasing mask opening width.

Based on these results, HBTs employing extrinsic base laterally overgrown on buried SiO_2 were fabricated. Emitters were aligned 60° off [011] direction to obtain the maximum lateral overgrowth length for the extrinsic base. The regrown-base HBTs exhibit acceptable DC performances with current gain ~15. Lower base recombination current and higher current gain can be expected after further efforts are made to improve the selective growth quality as to minimize e process related damage and contamination.

RF measurements demonstrate ~60% base-collector capacitance reduction compared with conventional HBTs with the same layer structure and device layout. f_{max} of regrown base HBTs is lower than expected due to the high base contact resistance caused by the low Zn doping density in the extrinsic base, even though the extrinsic base sheet resistance is reduced through regrowth.

To substantially improve regrown-base HBT's bandwidth, a more advanced MOCVD system is necessary. If susceptor's rotational speed can be mechanically controlled and reach 1000 rpm, we will be able to use much lower temperature for the base regrowth. Significantly higher Zn doping density can then be obtained in the extrinsic base without compromising the regrowth selectivity. In addition, with higher susceptor rotational speed and better regrowth selectivity, InGaAs can be used as the extrinsic base material with

carbon doping. This can ultimately avoid the Zn doping limit problem in InP and provide much lower base resistance.

In our proto-type device demonstrations simple device layout and lay structure designs were adopted to minimize the device processing and fabrication difficulties, and they were far from mature. Significant improvements in regrown-base HBTs' performance can also be expected after further optimizing the device designs

References

[1] H. Nakajima, 'Design and fabrication of high-speed InP-based heterojunction bipolar transistors', IEEE Proc. of the 5th International InP and Related Materials Conf., pp. 13-16, 1993

[2] M. Ida, K. Kurishma, and N. Watanabe, 'Over 300GHz fT and fMAX InP/InGaAs double heterojunction bipolar transistors with a thin pseudomorphic base', IEEE Electron Device Lett., Vol. 23, pp. 694-696, 2002

[3] M. Dahlström, X.-M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y.M. Kim, Y. Wu, J.M. Fastenau, W.K. Liu, and M.J.W. Rodwell, 'Widebandgap DHBTs using a graded Carbon-Doped InGaAS Base', IEEE Electron Device Lett., Vol. 25, pp. 433-435, 2003

[4] Z. Griffith, M. Dahlström, M. Urteaga, M.J.W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, and W.K. Liu, 'InGaAs/InP mesa DHBTs with simultaneously high fT and fmax, and low Ccb/IC ratio', submmited to IEEE Electron Dev. Lett.

[5] O. Nakajima, H. Ito, T. Nittono, and K. Nagata, 'Current induced degradation of Be-doped AlGaAs/GaAs HBT's and its suppression by Zn diffusion into extrinsic base', Tech Dig. IEEE IEDM, pp. 673-676, 1990

[6] D.L. Miller and P.M. Asbeck, 'Be redistribution during growth of GaAs and AlGaAs by molecular beam epitaxy', J. Appl. Phys., Vol.57, No.6, pp.1816-1822, 1985

[7] H. Shimawaki, Y. Amamiya, N. Furuhata, and K. Honjo, 'High-fmax AlGaAs/InGaAs and AlGaAs/GaAs HBT's with p+/p Regrown base contacts', IEEE Trans. Electron Devices, Vol. 42, pp.1735-1744, 1985

[8] M. Ida, S. Yamahata, K. Kurishima, H. Ita, T. Kobayashi, and Y. Matsuoka, 'Enhancement of fmax in InP/InGaAs HBT's by Selective MOCVD Growth of Heavily-doped Extrinsic Base Regions, IEEE Trans. Electron Devices', Vol. 43, No. 11, pp.1812-1818, 1996

[9] K. Mochizuki, T. Nakamura, T. Tanoue and H. Masuda, 'AlGaAs/GaAs HBTs with buried SiO2 in the Extrinsic Collector, Solid State Electronics', Vol. 38, pp1619-1622, 1995

[10] K. Mochizuki, T. Nakamura, T. Mishima, H. Masuda and T. Tanoue T, 'Molecular beam deposition of low-resistance polycrystalline GaAs', Journal of Electronic Materials, Vol 23, pp. 577-580, 1994

[11] N.Y. Li, C.W. Tu, Journal of Crystal Growth, 'Low-resistance polycrystalline GaAs grown by gas-source molecular beam epitaxy using CBr4', Vol 188, pp. 45-49, 1998

[12] Y. Dong, D.W. Scott, Y. Wei, A.C. Gossard and M.J.W. Rodwell, 'Low-resistance p-type polycrystalline GaSb grown by molecular beam epitaxy', Journal of Crystal Growth, Vol. 256, pp.223-229, 2003

[13] G. Bacchin and T. Nishinaga, 'Fabrication of submicrometer structures by PSE/MBE', J. Crystal Growth, Vol. 211, pp. 389-394, 2000

[14] G. Bacchin, A. Umeno and T. Nishinaga, ' Lateral growth in molecular beam epitaxy by low angle incidence microchannel epitaxy', Appl. Surf. Sci., Vol. 159, pp. 270-276, 2000

[15] L. Jastrzebski, 'SOI by CVD: epitaxial lateral overgrowth (ELO) process-review', J. of Crystal Growth, Vol. 63, No. 3, pp. 493-526, 1983

[16] C. Bozler, G. Alley, 'Fabrication and numerical simulation of the permeable base transistor', IEEE Trans. Electron Devices, ED-27, No. 6, pp. 1128-41, 1980

[17] S. Naritsuka, T. Nishinaga, 'Spatially resolved photoluminescence of laterally overgrown InP on InP-coated Si substrates', J. Crystal Growth, Vol. 174, No.1-4, pp. 622-9, 1997

[18] O. Parillaud, E. Gil-Lafon, B. Gerald, P. Etienne, D. Pribat, 'High quality InP on Si by conformal growth', Appl. Phys. Lett., Vol. 68, No.19, pp. 2654-6, 1996

[19] T. Arai, Y. Harada, S. Yamagami, Y. Miyamoto and K. Furuka, 'CBC reduction in GaInAs/InP buried metal heterojunction bipolar transistor', Conference Proceedings, 2000 International Conference on Indium Phosphide and Related Materials, IEEE., pp. 254-257, 2000

[20] J. Park, P. Barnes, C. Tin, and A. Allerman, 'Lateral overgrowth and epitaxial lift-off of InP by halide vapor-phase epitaxy', J. Crystal Growth, Vol.187, No.2, pp.185-193, 1998

[21] L. Wernersson, M. Borgström, B. Gustafson, A. Gustafsson, J. Jarlskog, J. Malm, A. Litwin, L. Samuelson, W. Seifert, 'MOVPE overgrowth of metallic features for realisation of 3D metal-semiconductor quantum devices', J. Crystal Growth, Vol. 221, pp. 704-712, 2000

[22] Y.T. Sun, E. Rodriguez Messmer, D. Soderstrom, D. Jajan, S. Lourdudoss, 'Temporally resolved selective area growth of InP in the openings off-oriented from 110 direction', J. Crystal Growth, Vol. 225, pp. 9-15, 2001

[23] W. Burton, N. Cabrera, F. Frank, Phil. Trans. Roy. Soc. A 243, pp.299, 1951

[24] D. Franke, F.W. Reier and N. Grote, 'Post-growth Zn diffusion into InGaAs/InP in a LP MOVPE, Journal of Crystal Growth', Vol.195, pp.112-116, 1998

Chapter 3

InP HBT with Selectively Implanted Collector

3.1 Introduction

To increase the logic speed of heterojunction bipolar transistors, as discussed in the last chapter, the base–collector junction capacitance (C_{BC}) should be reduced as much as possible. In a mesa structured HBT, a large portion of C_{BC} originates from the extrinsic base-collector region under the base contact. In this chapter, we propose and investigate another approach to reduce the base-collector capacitance. This new HBT structure has a collector pedestal under HBT's intrinsic region by using selective ion implantation and MBE regrowth, as illustrated in Fig.3.1. This structure parallels the widely used selectively implanted collector (SIC) structure in Si/SiGe HBT fabrication process, and is the first such reported structure in III-V HBT technology.

Compared to SiGe HBTs, InP HBTs with InP collectors have 20 times better intrinsic base sheet resistance, 4 times better collector electron velocity, and 6 times better breakdown x f_T product. However, today InP HBT technology employs relatively crude fabrication processes which severely limit both its performance and integration scale. In contrast, the advanced fabrication processes of SiGe HBT technology bring superior yield and scales of integration, which overcomes the weakness in Si material properties. It is clear that one path to high performance InP HBT devices is to combine best features SiGe and InP HBT technologies. InP HBT with selectively implanted collector is part of our efforts in this direction.

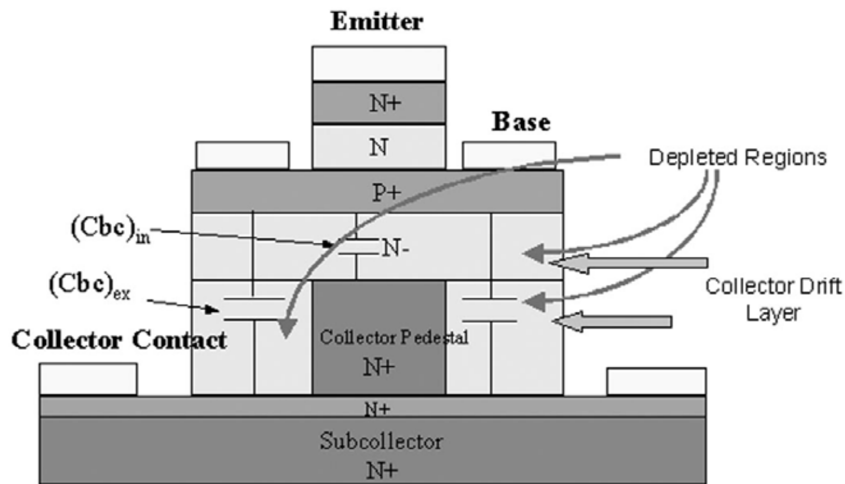


Fig.3.1 Schematic cross-section of the HBT with selectively implanted collector pedestal.

As shown in Fig.3.1, the HBT structure is designed so that the depleted collector thickness in HBT's intrinsic region is much larger than the depleted collector thickness in HBT's intrinsic region, and therefore the extrinsic base-collector capacitance can be significantly reduced. Although C_{BC} can also be reduced by forming a narrow N+ subcollector stripe lying under the emitter[1], such structures can have large collector access resistance Rc arising from long, narrow N+ layer. For emitter lengths greater than ~2μm, the resulting collector resistance then limits the maximum HBT current density under low-voltage (logic) operation. The collector pedestal structure, however, does not significantly increase collector access resistance relative to a standard mesa structure, and is consequently the approach most widely employed in Si/SiGe technology.

In this chapter, we describe the design, material epitaxy and process techniques to realize this pedestal HBT structure. We also demonstrate and analyze the DC and RF characteristics of our fabricated devices.

3.2 Si Ion Implantation in InP

3.2.1 Overview

InP is one of the popular materials for microwave, millemeter wave, high power, and high speed device applications because of its higher peak electron drift velocity, lower carrier ionization coefficient, etc. Some of these applications require buried or very thick n-type or p-type layers. Ion implantation is an attractive choice for obtaining these layers when compared to growth techniques because it is more economical and offers other advantages like selective area doping, planarity, and higher yield. In this section, we will discuss the details of the selective silicon ion implantation used in our device fabrication process, including the choice of implant energy and fluence, annealing conditions for dopant activation, and crystal quality of overgrown material on implanted substrates.

3.2.2 Implantation Energy and Fluence

In the HBT structure shown in Fig.3.1, the collector pedestal layer is designed to be 2000 Å. During HBT fabrication process, this layer is selectively implanted and the collector pedestal region becomes n-type. To lower the total collector access resistance, it is desirable to implant this region with a large fluence and make it heavily doped. Nevertheless, heavy dose implantation can

cause much damage to the material and even amorphisize it, significantly reducing the crystal quality of the overgrowth material on the implanted substrate. Once the material becomes amorphous, it is very difficult to remove the implant damage effectively even by using high-temperature annealing. As a result, a tradeoff between implant doping density and material lattice damage is unavoidable.

After a series of implant simulations and experiments, we chose to implant ^{28}Si at 110KeV with a dose of $8x10^{13}cm^{-2}$. Fig.3.2 shows the TRIM simulated implanted Si profile.

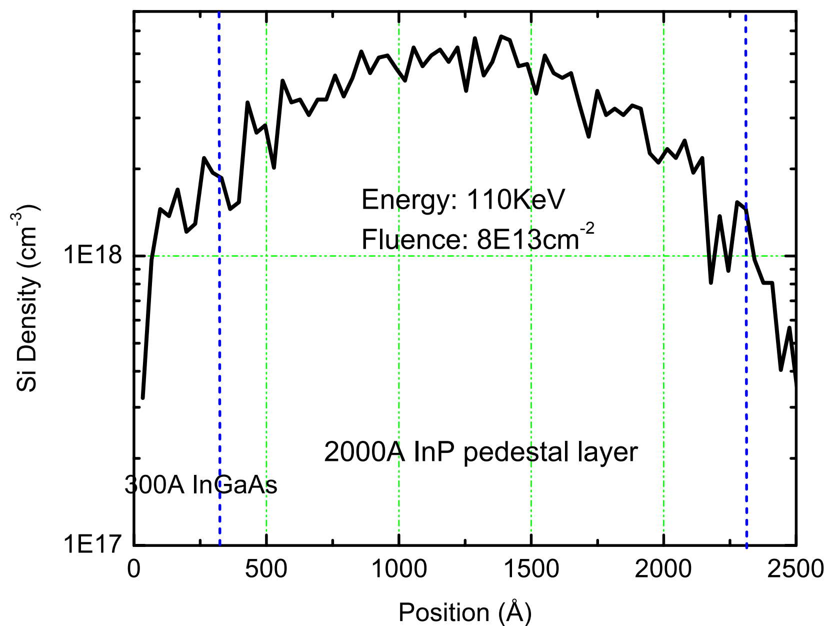


Fig.3.2 TRIM simulated Si implantation doping profile.

It can be seen that the average doping density in the 2000Å InP collector pedestal region is $3x10^{18}cm^{-3}$. Hall measurements were performed on test samples implanted with silicon ions using this energy and fluence, and the measured electron mobility was 1300 cm^2/VS. Combining the average doping density and electron mobility values, the resistance per unit area of the implanted collector pedestal region is estimated to be $3x10^{-8}$ Ω-cm^2. With this resistivity, the collector pedestal region only adds an extra 0.5Ω to the total collector resistance even if the HBT's implanted area is as small as 0.7x8 μm^2. This corresponds to a collector x collector area product of 2.8 Ω-μm^2, which would only induce a 28mV voltage drop for an HBT operating at 10^6 A/cm^2. This pedestal resistance is therefore sufficiently low and will not significantly affect device performance. The implant fluence ($8x10^{13}cm^{-2}$) is also acceptable for the subsequent MBE regrowth since several groups have found that InP only started to amorphosize when the implant fluence approached $5x10^{14}$ cm^{-2}.[2]

3.2.3 Implant Lateral Distribution

The lateral distribution of the implanted dopants close to the edge of the implant window is critical to our device performance. Ideally the ions are vertically implanted through the mask window and no ions exist beneath the implant mask. The lateral motion of the ions caused by lateral collisions and

scattering always leads to a lateral Gaussian distribution. The ions reaching beyond the implant window edge can increase the effective width of collector pedestal region and therefore reduce the area of the region with thick depleted layers. As a result, pedestal HBT's effectiveness of base-collector capacitance reduction closely depends on the implanted dopants' lateral distribution close to the window edges.

The two-dimensional implanted ion distribution can be written as the product of vertical and lateral distributions

$$n(x,y) = \frac{n_{vert}(x)}{\sqrt{2\pi}\sigma_{\perp}} \exp(-y^2 / 2\sigma_{\perp}^2) , \tag{3.1}$$

where $\sigma_{\perp}$ is the lateral Gaussian distribution standard deviation.

This equation describes the result of implanting at a single point on the surface. To find the result of implanting through a mask window, we must integrate Eq. 3.1 over the open areas where the ion beam can enter. For a mask with an opening from y=-a to y=a, this gives a density d(x,y) of

$$d(x,y) = \int_{-a}^{a} n(x, y-y')dy' = \frac{n(x)}{2}\left[erfc(\frac{y-a}{\sqrt{2}\sigma_{\perp}}) - erfc(\frac{y+a}{\sqrt{2}\sigma_{\perp}}) \right] \tag{3.2}$$

For our collector pedestal Si implantation, as illustrated in Fig.3.2, the Si doping density in the pedestal region n(x) can be approximately regarded as constant, close to $3\text{x}10^{18}\text{cm}^{-3}$. TRIM simulation indicates that $\sigma_{\perp}$, the lateral Gaussian distribution standard deviation, is 500 Å for a 110 KeV Si

implantation. Fig.3.3 shows the calculated Si doping density profile for an implantation through a 0.8μm wide slit.

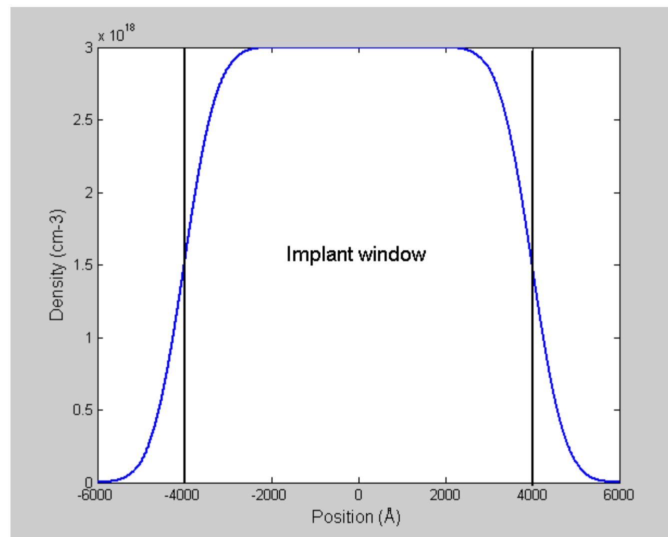


Fig.3.3 Si implantation profile through a 0.8 μm slit with 110KeV energy.

From the lateral doping profile the depletion thickness in the area close to the implant window edges can be calculated, assuming that the collector is 1000Å thick with $6x10^{16}cm^{-3}$ doping density, that the pedestal layer is 2000Å thick and undoped, and that the base-collector reverse bias is 0V. The calculation results are plotted in Fig.3.4. Clearly at a position 0.13μm away from the implant window edge, the silicon ion density is already very low and the collector pedestal layers are fully depleted. Within this 0.13μm non-fully-depleted region, the collector and pedestal layers still have a combined depletion thickness larger than the collector depletion thickness directly under the emitter. Further

calculation indicates that even though in this non-fully-depleted region C_{BC} is not reduced by a factor of three, it is nevertheless still reduced by 30%.

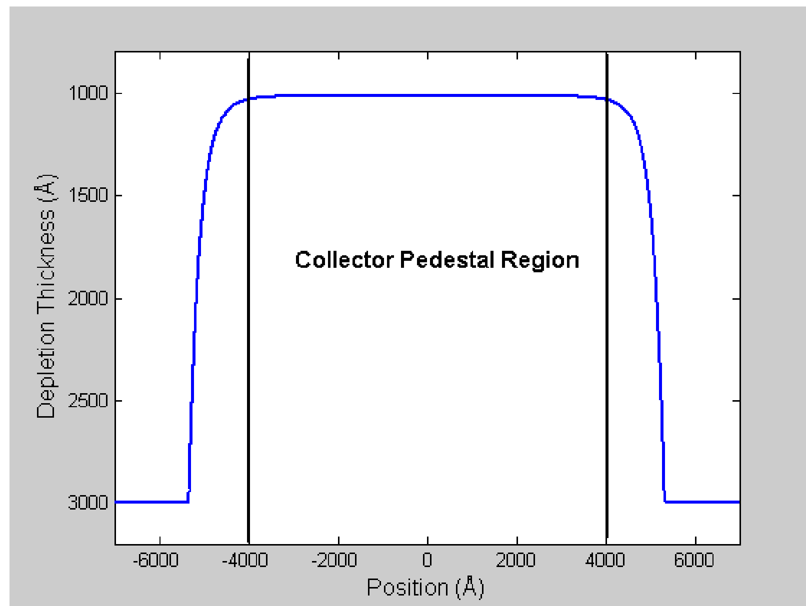


Fig.3.4 Calculated collector and pedestal layers depletion thickness close to the collector pedestal region at $V_{CB} = 0V$.

3.2.4 Annealing of Implanted Si Dopants

After Si ion implantation, high temperature annealing is required to activate the implanted Si dopants. To protect the sample surface morphology during annealing, a 500 Å PECVD deposited Si_3N_4 layer along with an InP proximity cover wafer are used, as illustrated in Fig.3.5.

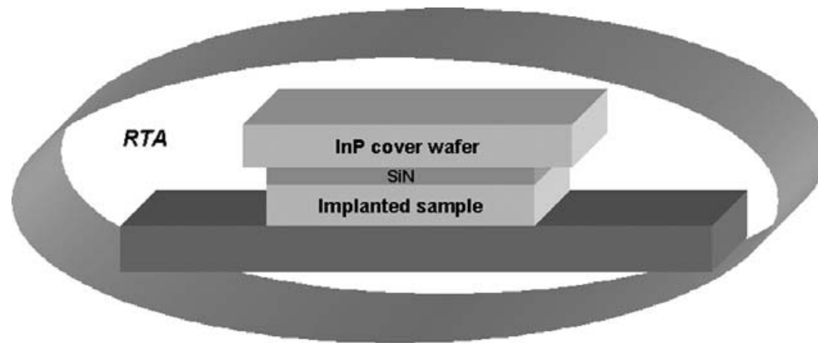
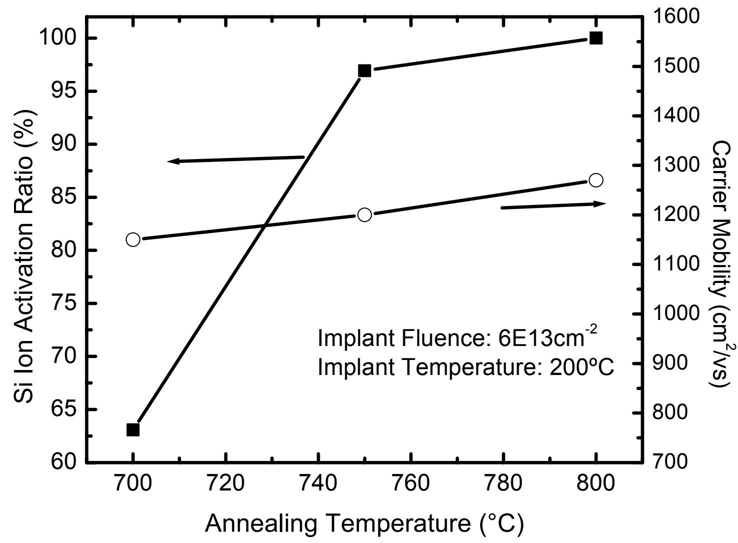


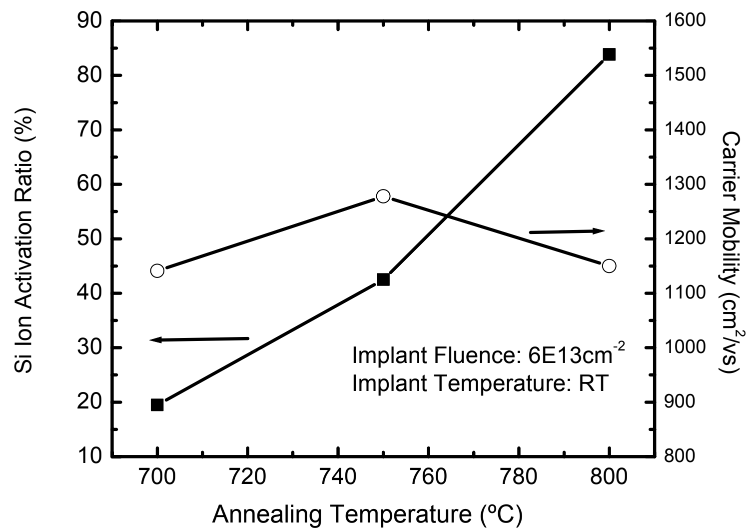
Fig.3.5 Schematics of the implanted sample's annealing condition.

To study the relationship between the annealing temperature and the Si dopant activation efficiency, variable temperature halogen lamp rapid thermal annealing (RTA) was performed for 10 sec. After the annealing, the Si_3N_4 cap was removed by buffered HF and the samples were characterized by van der Pauw Hall measurements.

Fig.3.6 displays the Si dopant activation efficiency and electron mobility of two samples implanted at 200°C and room temperature, both with an implant fluence of $6x10^{13}$ cm^{-2}.



(a)



(b)

Fig.3.6 Si activation efficiency and electron mobility as a function of annealing temperature for samples implanted at (a) 200°C and (b) room temperature.

From Fig.3.6(a) it can be seen that almost 100% of the implanted silicon dopants can be activated with annealing temperature above 750°C. It is also clear that samples implanted at elevated temperature (200°C) have better dopant activation efficiency than samples implanted at room temperature. This can be attributed to elevated temperature's minimization of the material lattice damage during implantation.[3]

3.2.5 Regrowth Crystalline Quality on Implanted Substrate

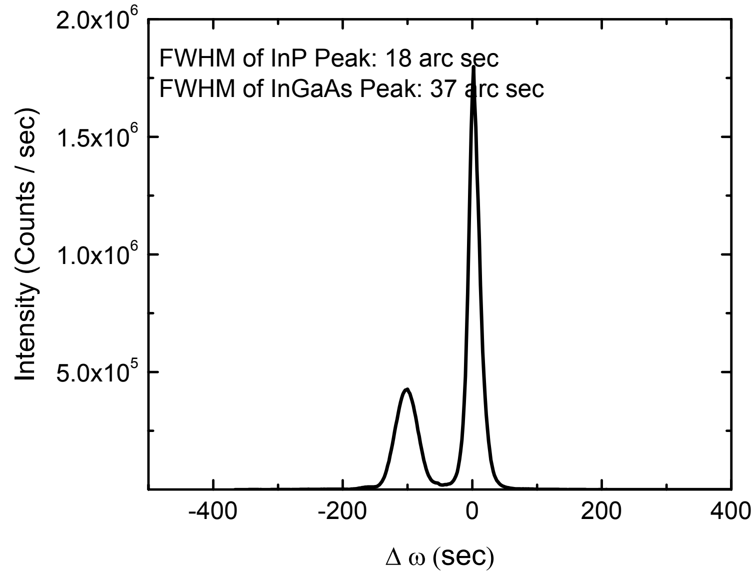
Ion implantation results in damages to the InP crystal, most of which can be removed by a high temperature annealing step for activating the implanted dopants. However, some damage is known to exist even after anneals of long duration. The anneal step itself can cause etch pits and other defects on InP surface, particularly if the sample surface is not properly protected during anneal. It is therefore important to investigate whether high quality HBT structures, which are sensitive to the minority-carrier lifetime, can be grown on implanted and annealed InP substrates.

To study regrown material quality on implanted InP substrates, a 0.5 µm $In_{0.53}Ga_{0.47}As$ layer was grown by MBE on a wafer implanted with a relatively

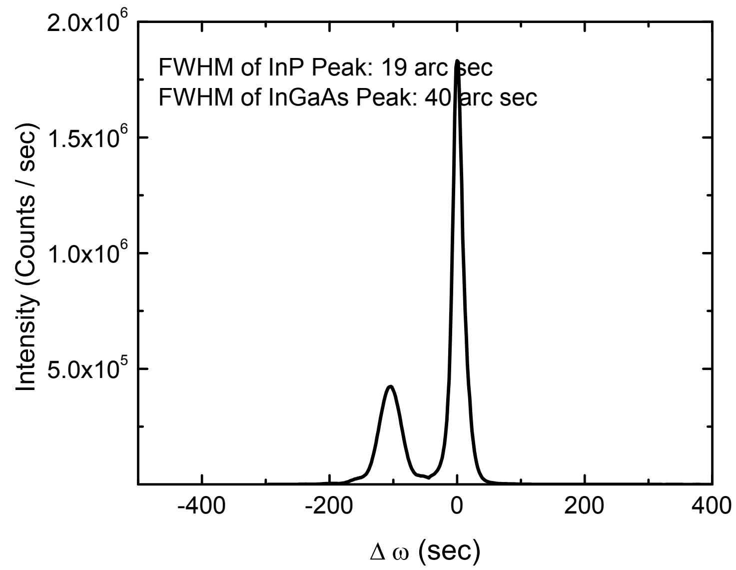
heavy fluence of $1.4x10^{14}cm^{-2}$ and annealed at 750°C. For comparison, the same growth was done on an unimplanted InP substrate.

The crystalline quality of these two InGaAs layers was assessed using X-ray diffratometry. Diffraction patterns were recorded in the vicinity of the symmetric (004) reflection using CuKα radiation (Fig.3.7). The X-ray diffraction spectrum of the two samples are very similar. They are both composed of two closely neighboring peaks with FWHM value amounting to ~40 arc sec for the 0.5 μm InGaAs layer and ~18 arc sec for the InP substrate. These numbers are in agreement with data given in the literature for high quality MBE growth.[4]

Regrowth experiments have also been carried out on InP substrates implanted with even higher fluence ($\sim 4x10^{14}$ cm^{-2}). The DC characteristics of the regrown InP/InGaAs/InP DHBT structure with high base doping ($\sim 6x10^{19}cm^{-3}$) exhibited current gain of 12 and very low base-collector leakage current (~ 0.7 $nA/\mu m^2$ at $V_{CB} = 2V$). These results further prove that the growth of high-performance HBTs and other minority-carrier lifetime sensitive devices on implanted and annealed InP substrates is possible.



(a)



(b)

Fig.3.7 X-ray diffraction spectrums of InGaAs layers grown on (a) unimplanted InP substrate and (b) InP substrate implanted with Si.

3.3 HBT Layer Structure Design

3.3.1 Emitter Design

For an InP DHBT, the emitter can be either InAlAs or InP. InAlAs offers certain advantages, including reduced emitter-base surface leakage and good passivation with SiN. Also, because the InAlAs bandgap is larger than InP (1.48eV compared to 1.35eV), a larger valence band discontinuity is possible when the emitter-base junction is graded. One of the factors determining the choice of emitter material, however, is that the carbon doped base necessitates wet etching of the HBT, and the InAlAs/InGaAs wet etch always creates a large undercut, unsuitable for high performance devices. An InP emitter, in contrast, offers smaller etch undercut, and also better electrical resisitivity and better heat transfer. For these reasons, InP was chosen as the emitter material for our devices.

The emitter-base heterojunction can be either graded or abrupt. There are several implications of the choice between a graded and abrupt junction. Normally a graded emitter-base junction has a lower turn-on voltage, a higher threshold for hole-back injection, and a low junction ideality factor. The base-emitter grade can be incorporated into a ledge to reduce emitter-base leakage current. An abrupt emitter-base junction, on the other hand, is usually associated with simpler layer design, higher turn-on voltage, lower threshold for hole-back injection, and higher ideality factor. An abrupt emitter-base junction can also

provide higher DC current gain and reduce base transit time since electrons are injected into the base with a minimum energy $\Delta E_{barrier}$.

In our HBT design, abrupt InP-InGaAs emitter-base junction was adopted for its simplicity with material epitaxy and its potential ability to reduce the base transit time.

3.3.2 Base Design

To reduce the base transit time, the base can be graded as proposed by Kroemer.[5] The grading creates a quasi-electric field that sweeps electrons across the base. This can be achieved through either bandgap grading or doping grading. In bandgap grading the material composition is changed throughout the base, as in InGaAs where the In composition is changed from 53% at the base-collector interface to 44% at the emitter-base interface.[6] Modern SiGe HBTs have an increasing Ge content in the base at about 5-10%.

The other approach to create a base grade is to change the base doping level through the base, heavy doping at the emitter-base interface and low doping at the base-collector interface.[7] At degenerate doping levels ($\sim 3\times10^{19}$ cm^{-3}), a small (~30%) linear change in doping level is able to create a strong electric field.

Our HBT design uses a 300 Å InGaAs base with linear carbon doping grading from $8x10^{19}$ cm^{-3} to $5x10^{19}$ cm^{-3}. At $8x10^{19}$ cm^{-3}, the variation in Fermi energy with doping is strong and large drift fields are introduced with moderate change in doping. Assuming Fermi-Dirac statistics and including bandgap narrowing, the linear grading from $8x10^{19}$ cm^{-3} to $5x10^{19}$ cm^{-3} produces a 49 meV potential drop and 16.5 KV/cm drift field. Assuming 43 cm^2/s average electron diffusivity and a $4x10^7$ cm/s base exit velocity, the calculated base transit time is reduced by the grading from 0.18 ps to 0.10 ps.[8],[9] This calculation neglects the initial injecting electron velocity from the emitter.

3.3.3 Collector Design

SHBTs with InGaAs collector have achieved impressive device performance and are comparatively easy to design and grow. The main problem of InGaAs collector is its low breakdown. A 2000 Å thick InGaAs collector can only take around 2.2 V before the avalanche breakdown, whereas the same thickness for a composite InP collector breaks down at 7.5V. A second problem is the low thermal conductivity of InGaAs, which is less than 1/5 of InP's thermal conductivity. At high current densities, heat management becomes a critical issue.

To use an InP collector and InGaAs base, the conduction band discontinuity between InGaAs and InP must be removed; otherwise the device performance will be severely degraded. The discontinuity will increase base electron storage time and electron-hole recombination due to electron trapping in the base. In our HBT design, this base-collector conduction band discontinuity is suppressed by grading. The base-collector grade employs a 200 Å InGaAs setback layer and a 240Å InAlAs/InGaAs chirped superlattice grading from InGaAs to $In_{0.26}Ga_{0.26}Al_{0.48}As$, producing zero conduction band offset at the interface. The superlattice period is as small as 15 Å, reducing miniband effects and the associated degradation in transit time. The Si pulse-doped layer (30 Å, $N_{d,pulse}$ = $3x10^{18}$ cm^{-3}) has sheet doping $T_{pulse}N_{d,pulse} = \varepsilon_r \Delta E_c / q^2 T_{grade}$, selected to suppress the change in the conduction band quasi-field at the interface with the InP collector.

C_{cb}/I_C is a key parameter determining logic speed. To ensure full collector depletion, hence low C_{cb} at a minimum voltage $V_{cb,min}$, the maximum collector doping must satisfy

$$V_{cb,\min} + \phi = qN_d T_c^2 / 2\varepsilon_r \, , \qquad (3.1)$$

In our HBT designs, a 1000 Å thick collector was used. Targeting nearly complete depletion at $V_{cb,min}$ = 0 V, a collector doping density of $7x10^{16}$ cm^{-3} was chosen.

3.4 MBE Growth

3.4.1 Oxide Desorption

All HBT pedestal template growths were done on Fe-doped semi-insulating InP substrates. These wafers are purchased ‘epi-ready’ and the native oxide present on the wafer before the growth is quite thin. RHEED streaks are usually visible on these wafers before oxide desorption has begun. To desorb the oxide, the wafer is gradually heated to ~525°C as indicated by the pyrometer. This temperature is normally maintained for ~3 min until a complete 2x4 reconstruction pattern begins to appear.

The HBT structure is regrown on the pedestal template after the selective implantation and subsequent high temperature annealing. Before loading the sample into the MBE chamber, the InGaAs sacrificial layer on the top of the pedestal template is wet etched using a 1:1:25 H_3PO_4:H_2O_2:H_2O solution. The template is then rinsed under running DI water for extended time. It has been found that oxide on the pedestal template after the wet etching and water rinse process is thicker than that on the ‘epi-ready’ wafers. Usually the pedestal template needs to be heated and maintained at 525°C for 5~6 min before clear 2x4 reconstruction patters appear. It was reported that extended desorption (~20min) cleaning under high As overpressure (2×10^{-5} Torr) could improve surface morphology and increase regrowth quality.[10] We however could not reproduce these findings in our experiments. The HBTs regrown on templates

with extended oxide desorption had poor material quality and very leaky junctions.

3.4.2 Lattice Matching

To ensure the epitaxial layers are lattice matched to InP substrate, growth must be carefully calibrated either by proper matching of the binaries using RHEED oscillation rates or through beam flux calibrations. When combining rates from binary RHEED oscillations, the different lattice constant must be considered. The gallium growth rate on InP substrate, for example, is faster than that on GaAs substrate since the unit cell is smaller and few atoms are needed to complete a monolayer. By considering the geometry of the situation, it is seen that growth rate on InP is

$$GR_{GaonInP}(\text{Å}/s) = \left(\frac{a_{InP}}{a_{GaAs}}\right)^3 GR_{GaonGaAs}(\text{Å}/s)\,, \qquad (3.2)$$

where a_{GaAs} and a_{InP} are the lattice constants of GaAs and InP respectively.

For accurate lattice matching, therefore, the correct proportional growth rate of a component such as Ga must be converted to the rate on the InP substrate for RHEED calibrations. A slightly less than unity sticking coefficient for indium in the ternary requires that an empirical correction factor must be used.

The flux calibration method has been used more often for MBE growth in this work. With this calibration method, the cell temperature is varied until a

desired flux is measured. This calibration does not allow for arbitrary growth rates, but is considerably less time consuming than RHEED oscillation. However, in either method, x-ray calibration samples should be grown to ensure complete lattice matching.

3.4.3 Interfaces

The details of interfaces are often neglected in MBE, since a majority of devices are based on a single group-V species. Changes of group-III species, such as a GaAs-AlAs interface, are handled easily by the shutters of a MBE system. Since an overpressure of the group-V species is always present, growth including changes of group-V species are much more difficult.

The treatment of the surface can strongly affect the types of atomic bonds that form at the interface. This in turn affects the properties of the structure. A good example of this is seen in InAs quantum wells with AlSb barriers. Two possible interfaces could be formed: AlAs-like and InSb like, since both anion and cation are changed in this situation. By using shutter sequencing to force certain interfaces, work at UCSB found devices with interfaces formed by these two alternatives had substantially different properties.[11]

In our HBT growth, the As-P interface must be carefully treated for optimal material quality and device performance. The effect of arsenic exposure on an InP substrate is best understood from the experience of desorbing the native

oxide on an InP substrate with only arsenic overpressure. Substrates prepared in this manner often suffer from high surface defect density that could be attributed to the arsenic exposure. For this consideration, the As exposure time for the InP surface during the InP-InGaAs growth transition is kept less than 15sec.

The phosphorous flux seems to have less impact on arsenic compounds. During the growth that contained such interfaces, little change in the RHEED pattern was observed during the transition. In our growth, the phosphorous exposure time for the InGaAs surface is chosen to be ~25 sec.

3.4.4 Carbon Doping

Beryllium used to be widely employed as the p-type dopant for the growth of III-V compounds by MBE. It was found that InGaAs could be doped into $10^{19}cm^{-3}$ range with beryllium with nearly complete activation. However, it was also found that beryllium dopants had a strong tendency to diffuse, with the diffusion coefficient strongly dependent on the beryllium concentration, the growth temperature, and the III/V flux ratio. In n-p-n HBT structures, beryllium diffusion from the base into the lightly doped collector can render large regions of the collector p-type, affecting the Kirk threshold and the overall transit time. Beryllium diffusion into the emitter can affect the base-emitter turn-on voltage, the DC current gain, and the junction ideality factor.

Carbon is known to have a diffusion coefficient roughly three orders of magnitude less than the beryllium at similar concentrations and growth temperatures. Carbon doping therefore promises significant benefits for HBT technology.

In our HBT growth, a carbon tetrabromide (CBr_4) source is used. The CBr_4 itself is vacuum sublimed into a stainless steel cylinder. CBr_4 vapour passes through a leak valve, which is set by the user to deliver the required flux of CBr_4. Caron doping calibration samples were grown in order to characterize carbon doping in InGaAs. The thickness of the InGaAs layer was normally 3000Å. The results of hole concentration (determined by Hall measurement) vs. hole mobility are plotted in Fig.3.8. A hole concentration of $8.5x10^{19}$ cm^{-3} was obtained with a hole mobility of 40 cm^2/Vs. This hole concentration is high enough for our HBT base growth.

If even higher carbon concentration ($>10^{20}cm^{-3}$) is needed, the V/III ratio can be decreased to facilitate carbon incorporation on the group-V site. Lowering the substrate temperature to ~430°C is another effective way to obtain higher carbon concentration.

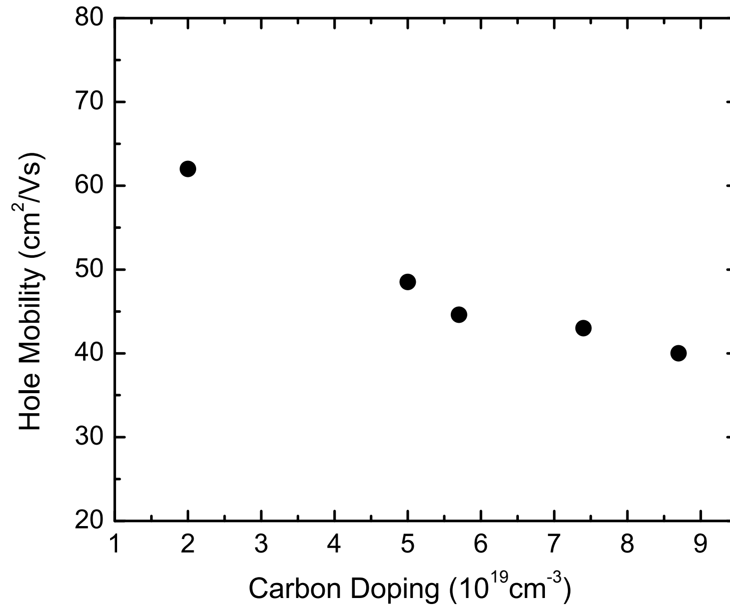


Fig.3.8 Hole mobility as a function of carbon doping density for $In_{0.53}Ga_{0..47}As$ grown by MBE at UCSB.

3.5 Device Fabrication

3.5.1 Overview

Fig.3.9 illustrates the schematics of the device fabrication process. The subcollector template was grown by MBE and consisted of a 2000 Å n+ InP subcollector layer, a 50 Å InGaAs n+ subcollector contact layer, a 2000 Å

undoped InP collector pedestal layer, and a 500Å undoped InGaAs sacrificial cap layer.

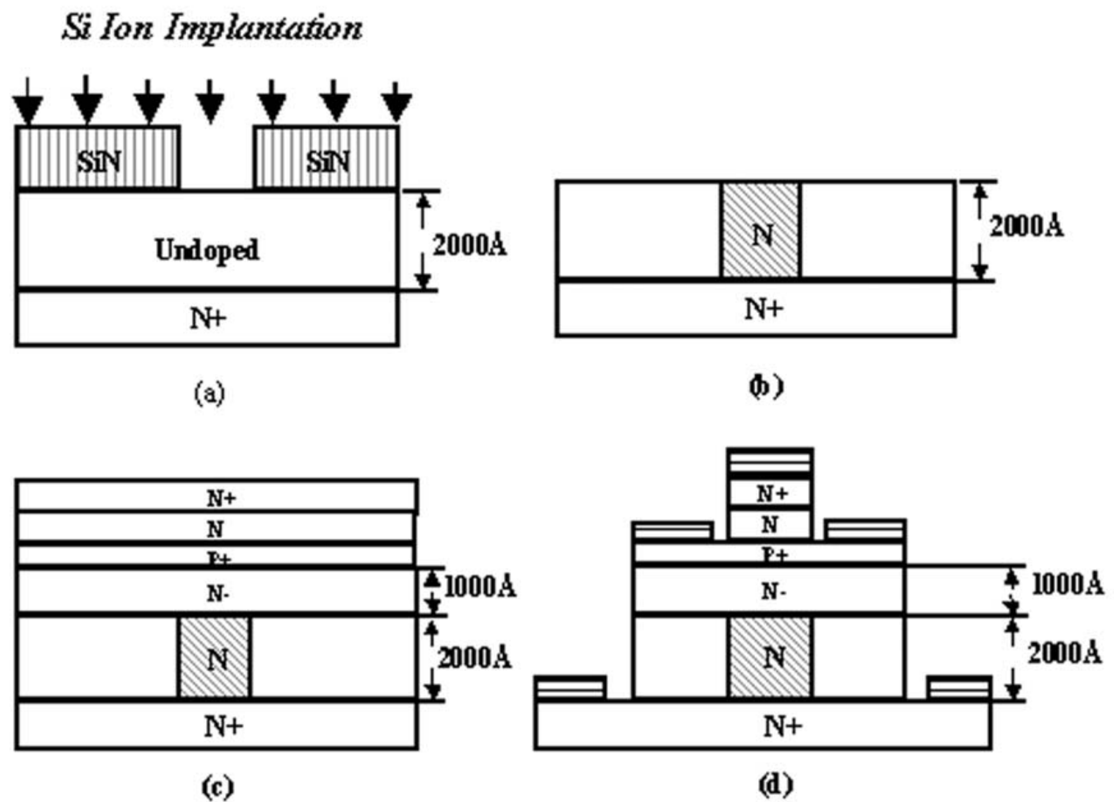


Fig.3.9 Collector pedestal HBT fabrication steps: (a) implant window definition and Si ion implant, (b) implant mask removal and high temperature annealing, (c) HBT structure regrowth, (d) triple-mesa HBT fabrication.

After the subcollector and pedestal template growth, tungsten alignment marks were formed by blank sputtering and subsequent reactive ion etching (RIE). 0.8 μm SiN was then deposited by PECVD as the implant mask.

The implant window was defined by optical lithography and the implant window width was varied in a series of devices to study the effectiveness of the selectively implanted collector pedestal for base-collector capacitance reduction. The SiN was then removed from the implant window by RIE. ^{28}Si was implanted at 110KeV with a dose of 8×10^{13} cm^{-2} at 200 °C. After the implant, the SiN mask was removed and rapid thermal annealing (RTA) at 750 °C was performed for 10 for dopant activation. During the annealing a 500Å PECVD deposited SiN cap and an InP proximity wafer were used to protect the sample surface morphology.

After the annealing, the SiN cap and InGaAs sacrificial layer were removed by wet etching with buffered HF. The sample was then loaded into the MBE system for regrowth. An InP DHBT structure including the collector drift layer, base, and emitter were grown subsequently. Triple-mesa HBTs were then fabricated using optical lithography and wet etching. The base contact was PdTiPdAu while emitter and collector contacts were TiPdAu. The HBTs were passivated and planarized with polyimide or benzocyclobutene (BCB).

The following sections cover several aspects of the process that are unique compared with normal InP DHBT fabrication process.

3.5.2 Alignment Mark

In the pedestal-implantation HBT fabrication process, it is crucial to align the implanted pedestal region with the HBT's intrinsic area accurately, otherwise the collector transit time will increase and the Kirk threshold current density will decrease, reducing the device's high-frequency performance. It is therefore very important to have clear and distinct alignment marks after the MBE regrowth. For this reason, metal alignment masks are preferable to etched alignment marks, because the regrown material deposited on the alignment mark can be etched away, while it is very difficult to do the same on etched alignment marks. As discussed earlier, the pedestal template needs to be annealed at a high temperature (~800°C) to activate the implanted dopants after the selective implantation. The metal alignment mark is therefore required to withstand this high temperature annealing. For this consideration, a number of refractory metals with high melting temperatures, including Ni, Ti, Pt, Pd and W were tested. Their melting temperatures are listed in Table 3.1.

The Ti, Ni, Pd and Pt test alignment marks were deposited on InP wafers by E-beam deposition and consequently lifted off. Tungsten alignment marks were formed by blank sputtering and RIE dry etching. All the test samples were covered by 500Å SiN cap layer and an InP proximity wafer and annealed at 800˚C for 10 sec, the same condition used to activate the implanted Si dopants.

Fig.3.10 shows that microscope images of the alignment marks made of Ti, Ni, Pd and Pt after annealing.

Clearly, these alignment marks all changed shape significantly after annealing. It is believed that high temperature annealing, even though below the metal's melting point, resulted in an interfacial intermixing as well as mutual migration and reaction between the metal and the InP. Obviously more thermally stable alignment marks are required.

Metal	Melting Temperature (°C)
Ti	1668
Ni	1455
Pt	1768
Pd	1554
W	3422

Table 3.1 Melting temperature of metals considered for using as alignment marks.

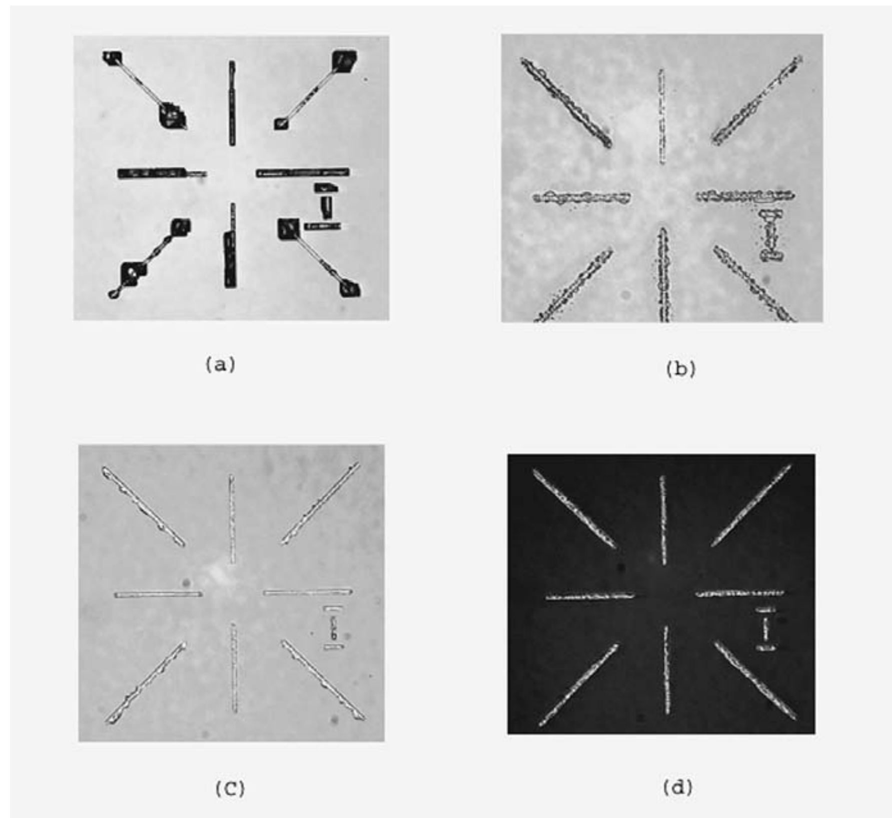


Fig.3.10 Microscope images of alignment marks formed by (a) Ti (b) Ni (c) Pt and (d) Pd.

Optical microscope images of tungsten alignment marks after high temperature annealing and MBE regrowth are displayed in Fig.3.11. The shape of the alignment mark did not change slightly as a result of superior thermal stability of tungsten. Therefore, although the tungsten alignment mark formation involves sputtering and dry etch, which both cause a certain amount of damage to the epitaxial surface before regrowth, it is still the best choice for the alignment marks.

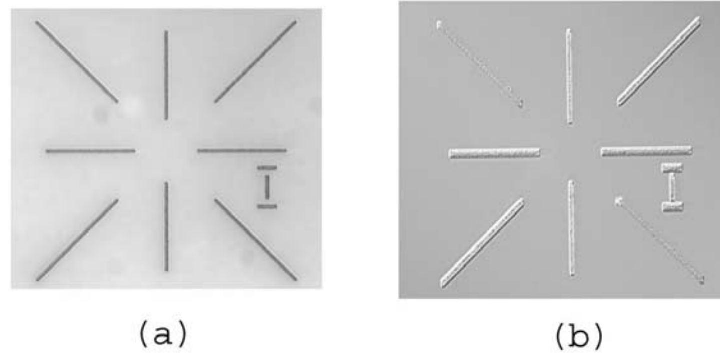


Fig.3.11 Microscope images of tungsten alignment mark after (a) high temperature annealing and (b) HBT structure regrowth.

3.5.3 SiN Implant Mask

For the collector pedestal formation, high energy (>100 KeV) silicon implantation will be used. As a result, a thick SiN (>5000 Å) implant mask is needed to prevent the silicon ions' penetration into the non-pedestal region. If a significant portion of Si ions reach the non-pedestal region, it will be converted to n-type doping, and hence will not fully deplete under low reverse base-collector bias.

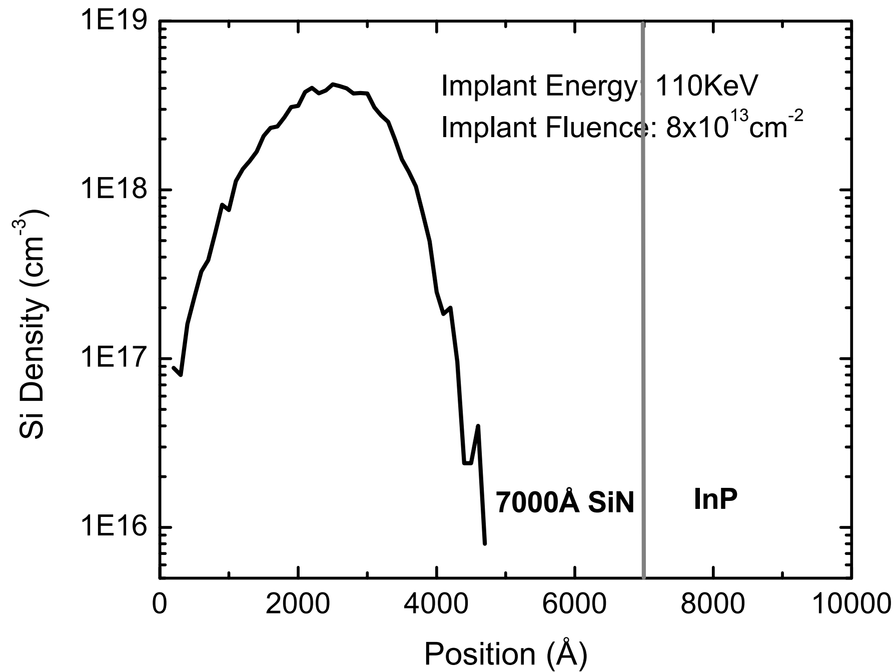


Fig.3.12 Simulated Si implantation profile in the SiN implant mask.

Fig.3.12 displays the TRIM simulated Si implantation profile in SiN layer. Clearly a 7000Å SiN is sufficiently thick for effective masking. To verify this, Si was implanted with 110KeV energy and $8x10^{13}cm^{-3}$ fluence into a test sample with a thick undoped InP layer covered by 7000Å PECVD deposited SiN layer. Before the SiN deposition a Hall measurement was performed on the test sample. The resistance was found to exceed the Hall measurement limit, indicating extremely low background carrier density in the undoped InP layer. After the implantation the thick SiN layer was removed and the sample was annealed. A Hall measurement was again performed to determine the carrier

density brought by the small fraction of Si dopants implanted through the SiN mask. The measured sheet carrier density was $2.2 \times 10^{11} cm^{-2}$. It is clear that less than 0.3% of the total implanted Si ions penetrated the SiN implant mask. Although this ratio was higher than TRIM simulation predicted, the penetrated silicon ion density was low and would not affect the pedestal layer's proper depletion. Further, the residual Si concentration will decrease exponentially if we increase the implant mask thickness.

3.5.4 Implant Window Etch

As discussed in the last section, a thick SiN (~7000 Å) implantation mask is needed to prevent the silicon ions' penetration into the non-pedestal region. Since the collector pedestal implant window is slightly wider than the emitter (<1μm), the SiN implant window width is comparable to its depth. The successful definition and etch of this SiN implant opening is therefore crucial to the device fabrication.

Photoresist is used as the etching mask for SiN etch. Since the implantation opening width is less than 1μm, the photoresist must be thin to avoid losing lithography resolution. The etching selectivity between SiN and photoresist needs must then be carefully considered. To reduce excess damage induced by

the dry etch process to the semiconductor surface, a low power dry etch is preferred.

To find a good etching condition to achieve small sidewall undercuts, relatively high etching rate for SiN and low etching rate for photoresist, and low etching power and self-bias voltage for low surface damage, a series of experiments were performed using different gas mixtures and etch conditions. Fig.3.13(a) shows the cross section of a 0.4 μm SiN opening formed by CF_4:O_2 RIE etch with pressure of 40 mτ and bias voltage of 100 V. The SiN mask was 5000Å thick. The photoresist was found to be etched slowly under this condition, with only ~2000 Å removed after the etch. However, due to the relatively high gas pressure and low bias voltage, the SiN etch undercut was large, estimated ~0.1 μm from Fig.3.13(a). To increase the dry etch anisotropy, lower gas pressure and higher bias voltage are desirable. However, such changes will decrease the etch selectivity between SiN and the photoresist layers as well as result in more etch damage to the exposed pedestal window surface. A well balanced etch condition therefore needs to be found.

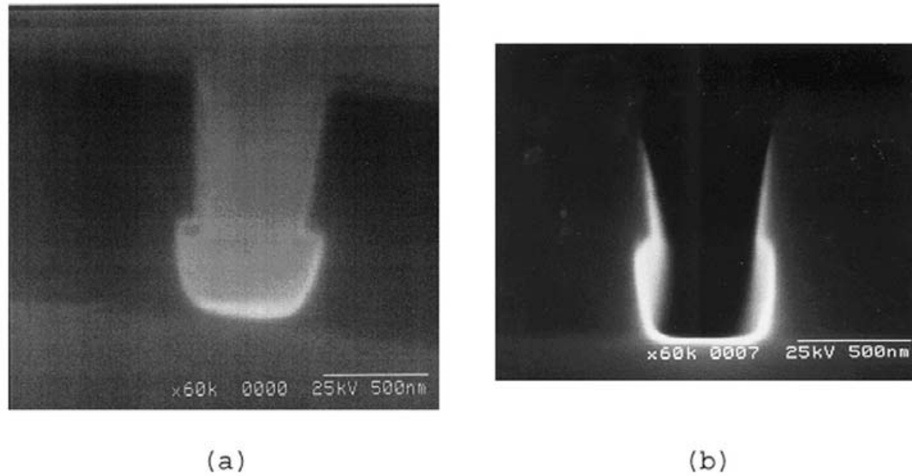


Fig.3.13 SEM images of a 0.4 μm SiN implant window etch profile using CF_4:O_2 (20:2 sccm) under etch conditions of (a) 100mτ pressure, 100V bias voltage, and (b) 200mτ pressure, 200V bias voltage.

After a series of experiments, the best result was obtained by using 20 mτ gas pressure and 200 V bias voltage. Fig.3.13(b) shows the cross section of a 0.4 μm implant window etched under this condition. The etch undercut was reduced to ~50 nm, and only 4000 Å photoresist was removed.

A mixture of SF_6, Ar, and O_2 gases can also be used to etch the SiN implant mask. Fig.3.14 shows an implant window profile by etching with 15mτ gas pressure and 200 V bias voltage. Clearly the etch undercut was even smaller than that obtained using the CF_4 gas mixture. However, SF_6:Ar:O_2 mixture etched photoresist much faster than CF_4:O_2 mixture, and therefore was not

suitable for the process. For a SiN implant mask of less than 5000 Å thickness, a SF_6:Ar:O_2 etch is preferred for its high etching rate and small etch undercut.

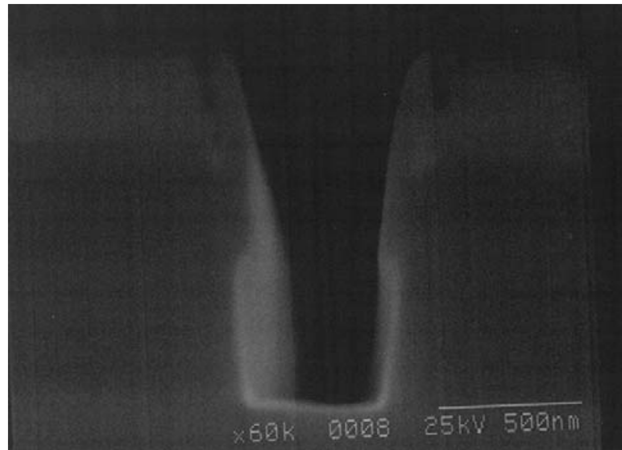


Fig.3.14 SEM images of a 0.4μm SiN implant window etch profile using SF_6:Ar:O_2 (5:10:3 sccm) etched at 15 mτ with 250 V bias voltage.

3.5.5 Metal Contact on n-type InP

In our current pedestal HBT process, the base mesa is etched down to the subcollector where the collector metal is deposited. Alternatively, the collector N+ contact region can be implanted simultaneously with the collector pedestal region. In this way, as illustrated in Fig.3.15, the base mesa must only be etched to the level of pedestal layer. This produces a nearly planar structure.

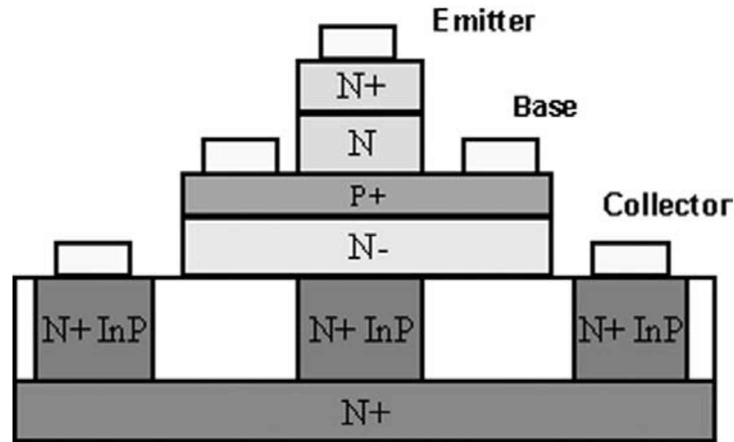


Fig.3.15 Schematic cross-section of the HBT with selectively implanted collector pedestal and collector contact regions.

From Fig.3.15 it is also seen that the collector metal will directly contact the implanted N+ InP region instead of the epitaxially grown N+ InGaAs layer. Although the metal-semiconductor barrier height is similar for InP and InGaAs, the larger electron effective mass in InP results in higher contact resistivity for a given doping density.

Recently there have been attempts to reduce the parasitic base-collector capacitance by forming an implanted N+ subcollector directly on InP substrate,[1] as we mentioned at the beginning of this chapter. In this kind of HBT structure, the collector metal also needs to directly contact N+ InP surface. We have future plans to combine this HBT structure with our collector pedestal

structure to further reduce the parasitic base-collector capacitance, and this therefore gives us another reason to investigate the possibility of achieving low metal contact resistance on N+ InP.

Non-alloy contacts of Ti(500Å)/Pt(750Å)/Au(2000Å) were first studied. The contacts were made to an n-type InP layer epitaxially grown on semi-insulating InP substrate by MBE. The thickness of this epitaxial InP layer was 0.3 µm, and silicon was the n-type dopant at a concentration of 1×10^{19} cm^{-3}. After the E-beam contact metal deposition and lift-off, the conductive mesa was defined and etched in $HCl:H_3PO_4$ solution. Rapid thermal annealing was then applied to anneal the samples at three different temperatures (300°C, 350°C, and 400°C) for 1 minute. From measurements using the transmission line method (TLM), the contact resistivity (R_c) of the metal contact was calculated and listed in Table 3.2.

Clearly the contact resistivity values changed little with the annealing temperature, and they were almost one order of magnitude higher than the contact resistivity of the same metal structure on N+ InGaAs layer. Annealing temperatures above 400°C might be able to produce lower contact resistance, but it can easily damage the base metal contact and therefore not usable for normal InP HBT process. Higher doping density in n-InP layer can also help reduce the contact resistivity. Nevertheless, a very large implant fluence must be used and the implanted InP could be severely damaged or even amorphousized,

which is hardly desirable for the subsequent regrowth process. As a result, it is difficult to produce low collector access resistance on implanted subcollector layer by using non-alloy metal contact.

Annealing Temperature (°C)	Contact Resistivity (Ωcm^2)
350	$1.4x10^{-6}$
400	$1.7x10^{-6}$
450	$1.7x10^{-6}$

Table 3.2 Contact resistivity of Ti/Pt/Au on n-InP annealed at three different annealing temperatures.

The alloy metal contact structure Ni/Ge/Au was then investigated. Table 3.3 lists the contact resistivity values after annealing the Ni (200 Å) / Ge (500 Å) / Au (500 Å) / Ni(200 Å) / Au(2000 Å) contacts at three different temperatures. Clearly the contact resistivity is significantly lower than non-alloy metal contact resistivity and strongly depends on the annealing temperature. It is believed that the decomposition of a ternary Ni-In-P layer at the InP surface at high temperature (~300 °C) and the subsequent formation of Ni_2P plus $AuIn_3$ produce

a low barrier height at the InP interface. This reaction is further driven by the inward diffusion of Au and outward diffusion of In.

Although the Ni/Ge/Au alloy shows very low contact resistance, the metal morphology is a major concern because of the low eutectic temperature for Ge and Au. A rough metal contact can cause problems in later processing steps. Contact spiking and poor edge definition can also seriously reduce the device fabrication yield. Fig.3.16 shows microscopic images of the Ni/Ge/Au/NiAu metal surface morphology after annealing at 300°C, 350°C and 400°C. It can be seen that the samples annealed at 300°C and 350°C both had uniform surface morphology. However, as the annealing temperature reached 400°C, the alloy reaction between Au and Ge occurred and the InP surface was deteriorated by alloying. During annealing, In and P out-diffuse and Au spiked into the InP substrate, making voids on the contact surface, as is readily observed in Fig.3.16(c). In summary, high annealing temperature can considerably lower the contact resistivity of Ni/Ge/Au alloy contacts to N+ InP, but unfortunately also causes poor contact morphology. Within an annealing temperature range (300°C - 350°C) associated with good contact morphology, the contact resistivity is close to $4x10^{-7}$ Ωcm^2. Although such a contact resistivity is still higher than normal contacts to n+ InGaAs (~$2x10^{-7}$ Ωcm^2), it is generally acceptable for HBT fabrication.

Annealing Temperature (°C)	Contact Resistivity (Ωcm^2)
300	4.3×10^{-7}
350	5.1×10^{-7}
400	2.2×10^{-7}

Table 3.3 Contact resistivity of Ni/Ge/Au/Ni/Au on n-InP annealed at three different annealing temperatures.

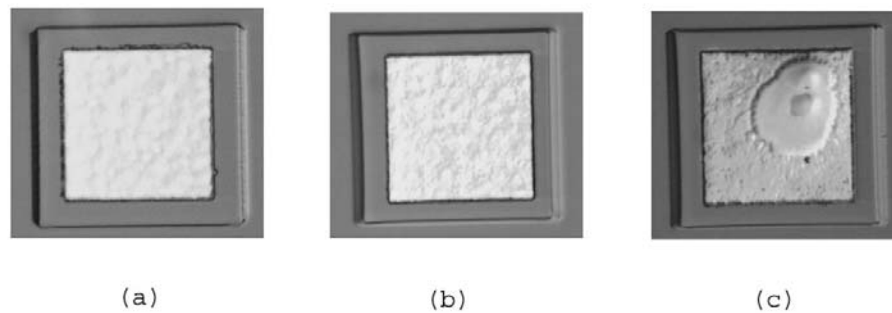


Fig.3.16 Microscope images of Ni/Ge/Au/Ni/Au contact metal morphology after annealing at (a) 300°C, (b) 350°C and (c) 400°C.

3.5.6 Regrowth Interface Treatment

As discussed earlier, before the MBE regrowth the pedestal template surface undergoes a series of processing steps, including tungsten sputtering,

tungsten RIE etch, SiN PECVD deposition, implant window RIE etch, and high temperature annealing. It is well-known that MBE regrowth quality strongly depends on the material surface condition. Therefore, the impact of these processing steps to the subsequent MBE regrowth must be carefully investigated.

To identify the potential problems, HBT structures were regrown on templates subjected to different processing steps. Large area HBTs were then fabricated and the device characteristics, particularly the base-collector reverse-bias leakage current were measured to evaluate the regrown material quality.

One problem was spotted even before the HBT fabrication and characterization. Fig.3.17(a) displays the microscope image of the material surface regrown on a template which has undergone SiN deposition and RIE etch. After the SiN dry etch, the top 300Å InGaAs sacrificial layer was etched by H_3PO_4:H_2O_2:H_2O solution without any further surface treatment. As Fig.3.17(a) shows, this process creates a large density of defects on the regrown material surface. After large HBTs were fabricated and characterized, most tested p-n junctions exhibited either high leakage currents or outright short circuits. This was likely caused by the high defect density.

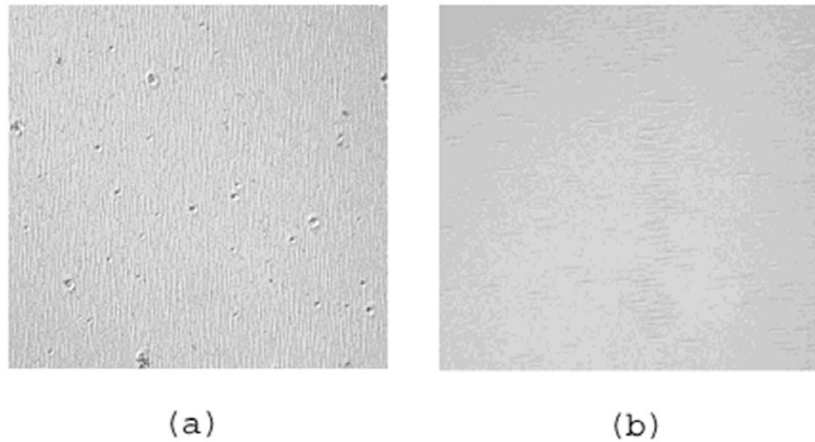


Fig.3.17 Microscope images of the material surface regrown on template (a) directly after SiN RIE etch and (b) with BHF cleaning after SiN RIE etch.

It was believed that the defects were caused by the residuals left on the template surface by the SiN RIE etch, and that the wet etch of the top InGaAs sacrificial layer was not sufficient to completely remove these contaminants. To thoroughly remove the dry etch residuals, the template was cleaned in buffered HF for 2 min after the SiN RIE etch. The regrown material quality was greatly improved by adding this extra surface-cleaning step, as Fig.3.17(b) shows. A large reduction in defect density is apparent. As expected, the large area HBTs fabricated on this wafer demonstrated good DC characteristics, and yield close 100%.

Similar regrowth tests were performed on a series of templates. Fig.3.18 shows the base-collector diode IV characteristics of five test samples. The base-collector junction area of the large area HBTs is 80 x 140μm^2, and the highest observed base-collector leakage current density at V_{CB} = 3V is ~1 $\mu A/\mu m^2$. For normal RF devices with ~20 μm^2 base-collector junction area, the leakage current will be ~20 μA. This is acceptably low for most circuit applications. This result clearly indicates that MBE regrowth of high quality junctions on implanted and processed templates is possible.

From Fig.3.18 it can be found that the largest base-collector leakage current was observed for the sample regrown after tungsten sputtering and RIE etching. The tungsten dry etch may have left metallic contaminants on the surface, at a density insufficient to cause growth defects, but still sufficient for degraded junction quality and increased junction reverse leakage. To improve junction quality, metallic contaminants were removed by treating the sample with UV ozone for 10 min and cleaning in buffered HF for 1min after the tungsten dry etch. The BHF cleaning time was short to avoid the lateral etch of the tungsten alignment marks. The large area device characterization showed that this UV ozone combined with HF surface treatment was very effective in removing the metallic contaminants and reduced the base-collector leakage current by almost two orders of magnitude.

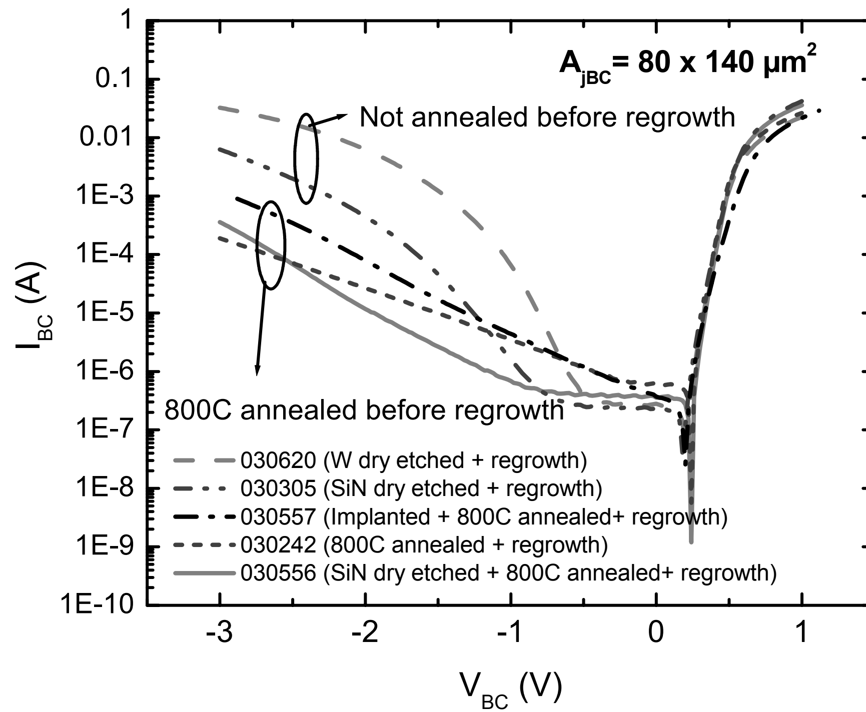


Fig.3.18 Base-collector diode IV characteristics of large area HBTs regrown on templates undergone different processing steps.

Fig.3.18 also shows that devices regrown on annealed templates have base-collector leakage currents almost two orders of magnitude lower than those regrown on templates with the same processing steps but without being annealed at high temperature. The improved material quality and junction leakage can be attributed to damage removal by the high temperature annealing. The annealing is therefore not only required to activate the implanted dopants, but also to greatly improved the regrowth material quality.

3.6 Regrowth Interface Charge Accumulation

3.6.1 First Generation Pedestal HBT

The first generation HBT with selectively implanted collector pedestal was fabricated as described in last section. The subcollector template was grown by MBE and consisted of a 2000 Å n+ InP subcollector layer, a 50 Å InGaAs n+ subcollector contact layer, a 2000 Å undoped InP collector pedestal layer, and a 300 Å undoped InGaAs sacrificial cap layer. After the alignment mark formation and selective implantation, the sample was loaded into the MBE system for regrowth. An InP DHBT structure including the collector drift layer, base, and emitter were grown subsequently. Table 3.4 lists the parameters of the layer structure. As can be seen, the collector depletion region above the collector pedestal was designed to be 1000Å thick, while outside the pedestal region the depletion thickness was designed to be 3000 Å. Triple-mesa HBTs were then fabricated using optical lithography and wet etching. The base contact was PdTiPdAu while emitter and collector contacts were TiPdAu. The HBTs were passivated and planarized with polyimide. Fig.3.19 shows the SEM image of a device after mesa isolation.

To simply the fabrication process, the base pad was designed to be relatively large and the total base-collector junction area was 65 μm^2.

Layer	Material	Thickness (Å)	Doping (cm^{-3})
Cap	InGaAs	400	Si:$2x10^{19}$
Emitter	InP	800	Si: $2x10^{19}$
	InP	100	Si: $8x10^{17}$
	InP	300	Si: $3x10^{17}$
Base	InGaAs	400	C: $6x10^{19}$
Collector	InGaAs	200	Si: $3.6x10^{16}$
	InGaAs/InAlAs	240	Si: $3.6x10^{16}$
	InP	30	Si: $3x10^{18}$
	InP	530	Si: $3.6x10^{16}$

Table 3.4 Parameters of the HBT epitaxial layers grown above the collector pedestal layer (first generation).

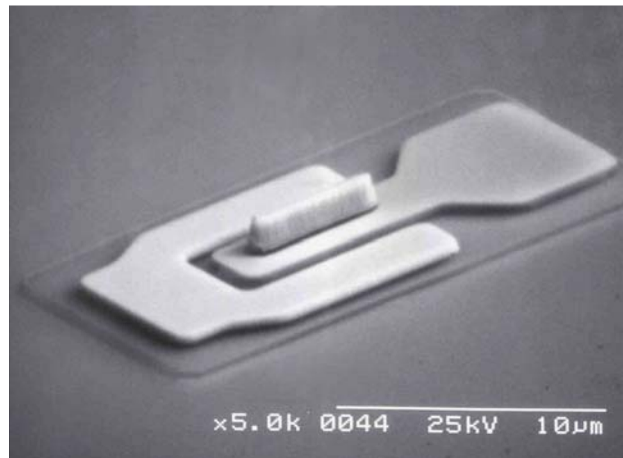


Fig.3.19 SEM image of a fabricated 0. 5× 6 μm^2 HBT before planarization.

Fig.3.20 shows the Gummel characteristics of a 0.5 × 6 μm^2 device. The base and collector ideality factors are 1.55 and 1.28 respectively, which are very similar to HBTs having a similar same structure but without implantation and regrowth. The Gummel characteristics were measured with 0.3 V collector-base reverse bias, so that the base-collector junction leakage I_{cbo} could be observed. Fig.3.20 indicates I_{cbo}~200 nA and this leakage current is acceptably low for most circuit applications. Fig.3.21 shows the common emitter DC characteristics of the same device, measured from 0 - 500 kA/cm^2 current density. The current gain is close to 25 and $V_{CE,SAT}$ is less than 0.8V at 500kA/cm^2 current density, which indicates good regrown HBT material quality and low collector access resistance.

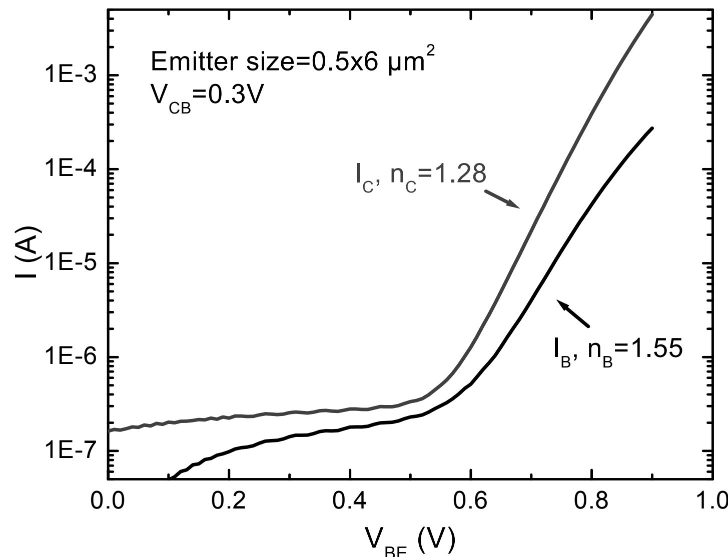


Fig.3.20 Gummel plots of an HBT with 0.5×6 μm^2 emitter size.

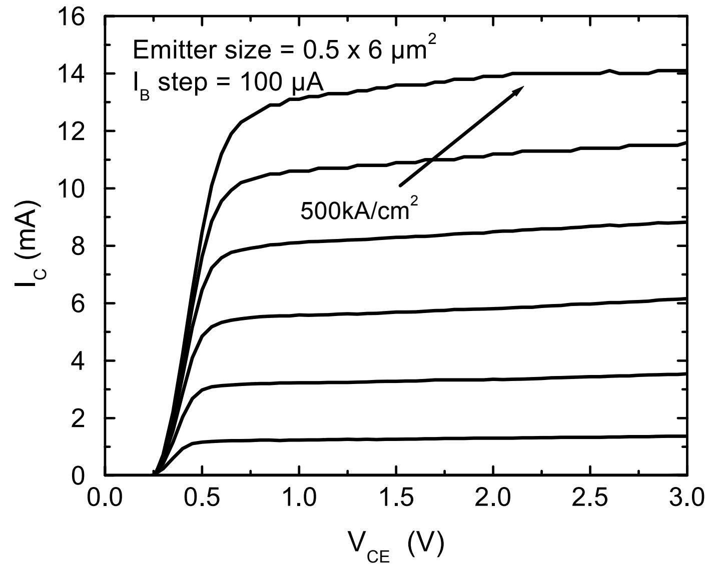


Fig.3.21 Common Emitter characteristics of an HBT with 0.5×6 μm^2 emitter size.

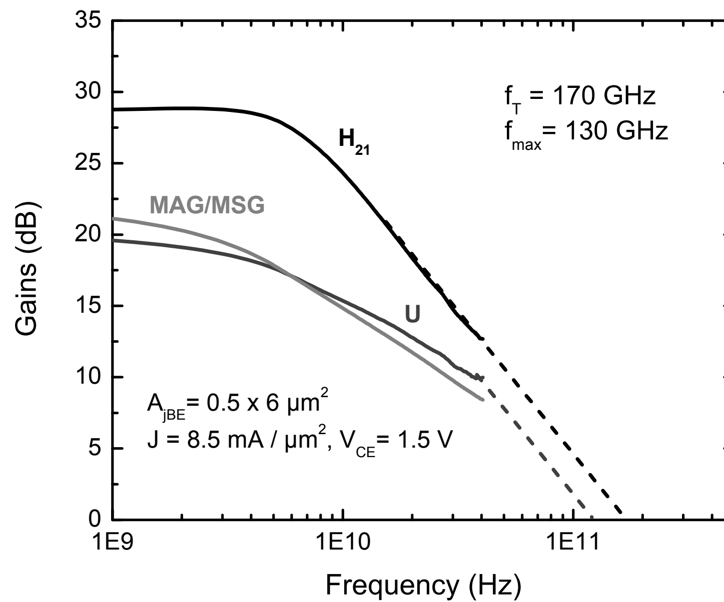


Fig.3.22 Frequency dependence of current gain(H_{21}), Mason's unilateral gain(U) and maximum stable gain/maximum available gain (MSG/MAG) at J = 850 kA/cm^2 and V_{CE} = 1.5V.

RF measurements were performed and on-wafer line-reflect-line calibration standards were employed. The cut-off frequencies f_T = 170 GHz and f_{max} = 127 GHz were measured at J = 850 kA/cm^2 and V_{CE} = 1.5 V, as shown in Fig.3.22. The measured f_T and f_{max} values were lower than expected. The discrepancy was due to an unexpectedly large base-collector capacitance. The total base-collector capacitance C_{BC} was determined from the imaginary part of Y_{12}. Fig.3.23 shows the measured C_{BC} as a function of V_{CE} at J_E = 0.5mA/μm^2.

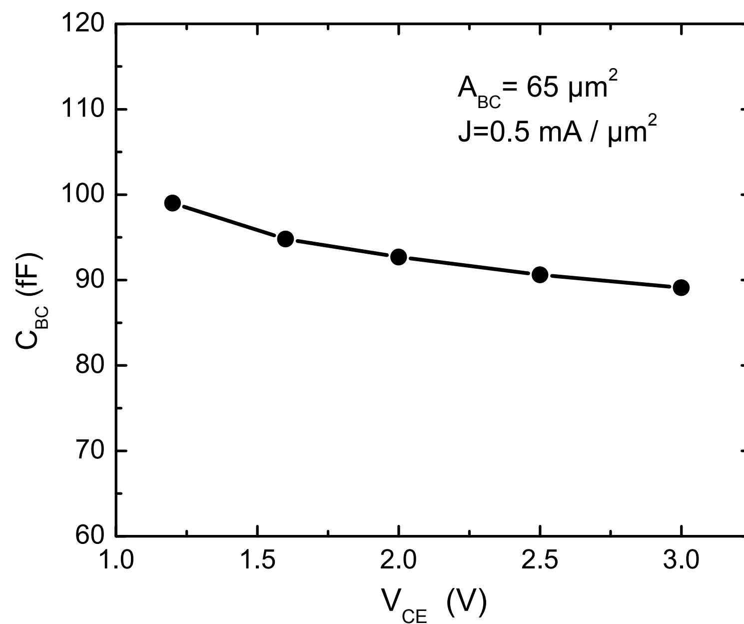


Fig.3.23 The dependence of total base-collector capacitance on V_{CE}.

The measured base-collector capacitance per unit area is ~1.3 fF/μm^2, which corresponds to ~800Å collector depletion thickness. As Fig.3.23 shows, C_{BC} only changes slightly with increases in base-collector reverse bias voltage. This indicates that the pedestal layer in the extrinsic base-collector area and the base-pad region is not depleted.

3.6.2 Regrowth Interface Charge Accumulation

To further investigate the depletion of the collector and pedestal layers, C-V measurements were performed on the base-collector junction of large-area HBTs fabricated on the same wafer. The layer structure of these test HBTs was exactly the same as the small area devices except that there was no Si implantation into the collector pedestal layer. As seen from the measured C-V curve (Fig.3.24), the base-collector capacitance corresponds to ~1000Å collector depletion thickness, and the collector pedestal layer is only depleted when a large reverse bias voltage (~2V) is applied.

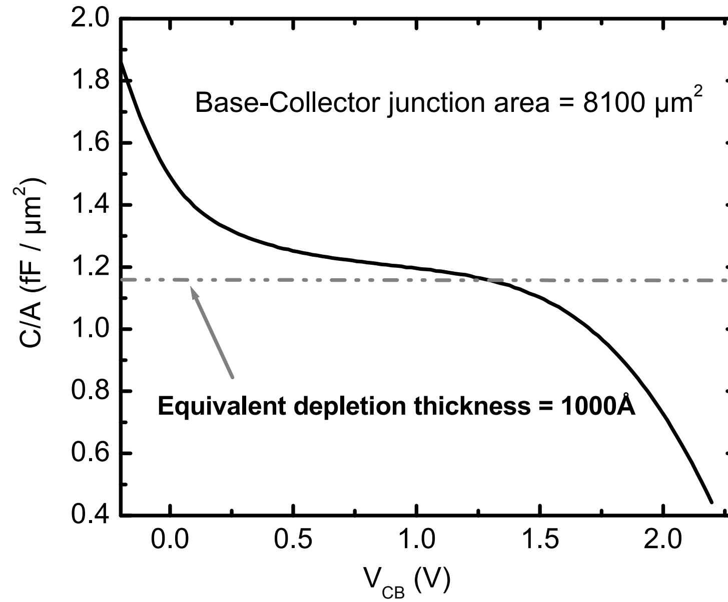


Fig.3.24 C-V measurements across the base-collector junction of large-area test device.

The carrier concentration in the collector layers can be calculated from the CV curve from:

$$N_D = -\frac{2}{q\varepsilon_S}\left[\frac{1}{\frac{d(1/C^2)}{dV}}\right], \tag{3.3}$$

Fig.3.25 displays the calculated profile of carrier concentration versus depth in the collector and pedestal layers. The x-axis is the position measured from the base-collector interface towards the collector and pedestal layers.

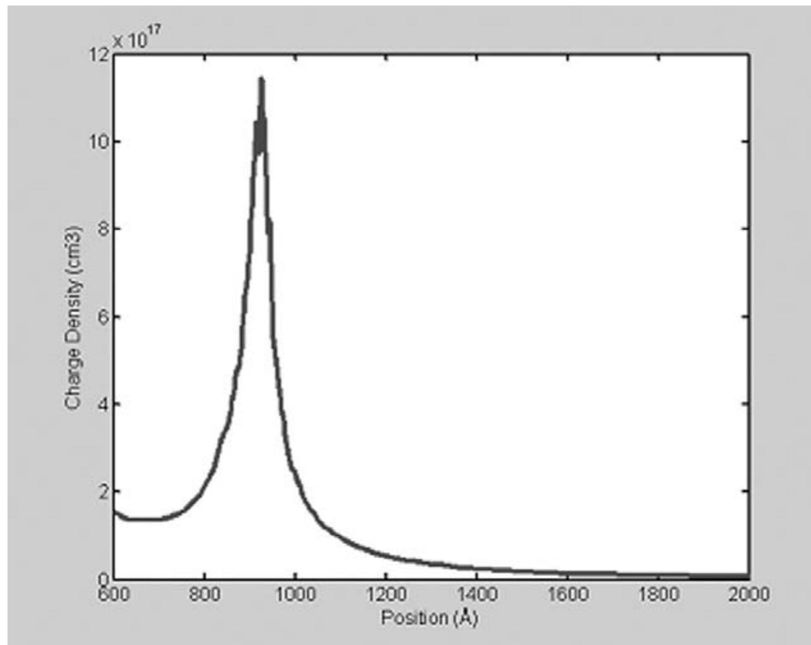


Fig.3.25 Carrier concentration versus depth profile in the collector layers.

It is clearly seen that at x=1000 Å, the location of the regrowth interface between the collector layer and the pedestal layer, there is a strong n-type charge accumulation. By integrating the this peak charge concentration at the regrowth interface, an interfacial sheet charge density of $1.8\mathrm{x}10^{12}$ cm^{-2} was obtained.

To better understand the influence of this charge accumulation on the device characteristics, device simulation was performed using Bandprof [12]. In the simulation an n-type delta-doping layer with $1.8\mathrm{x}10^{11}cm^{-2}$ carrier density is placed on the regrowth interface to emulate the interfacial charge accumulation. Fig.3.26 shows the simulated electron density in the collector region when base-collector reverse bias voltage is either 1.0 V or 2.2 V.

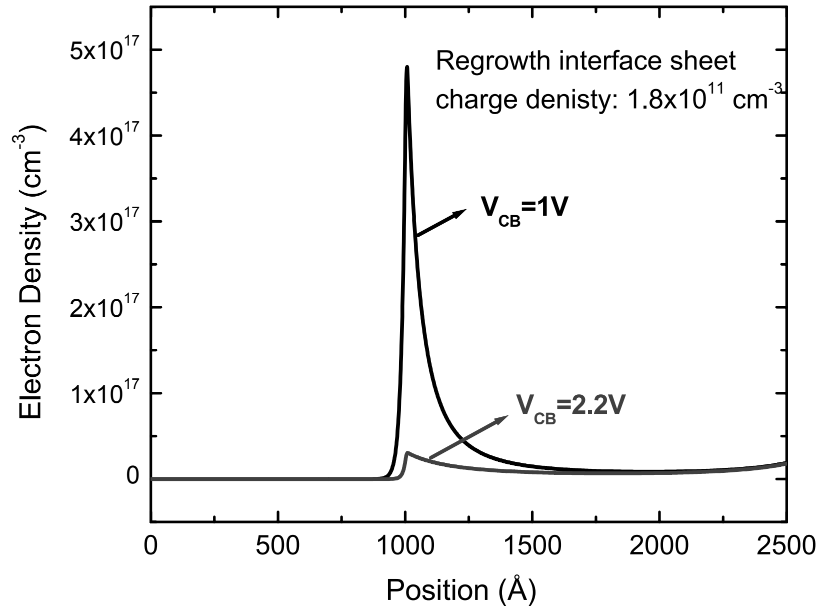
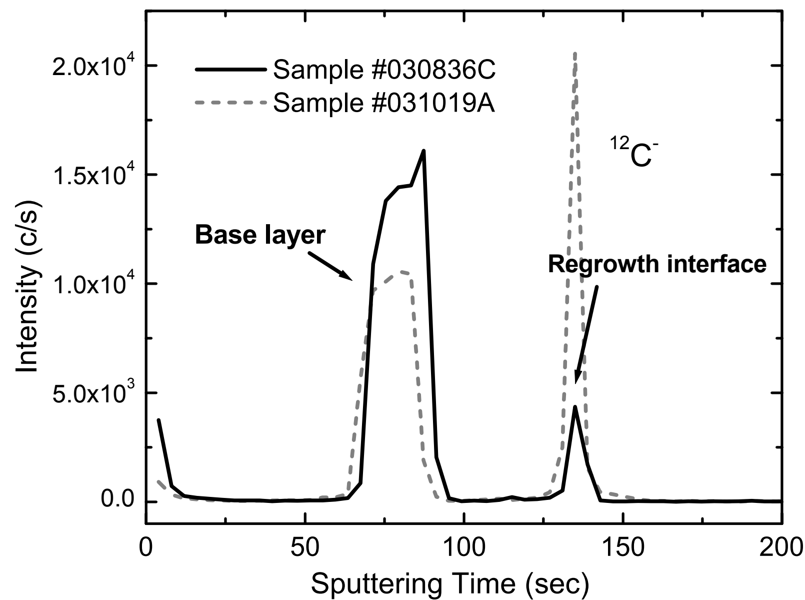


Fig.3.26 Simulated electron density in the collector region with interfacial charge accumulation at two different collector-base bias voltages.

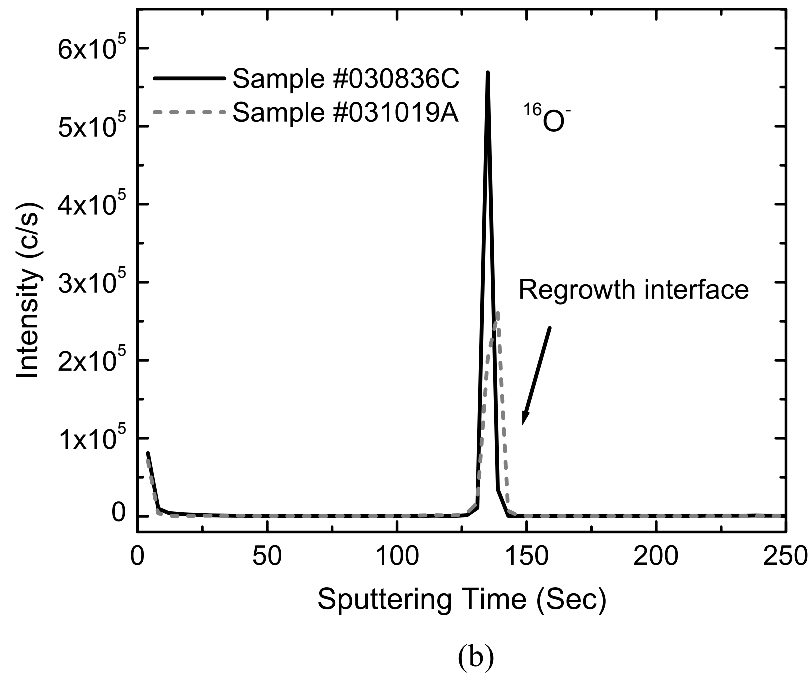
At low base-collector reverse bias, the accumulated charge at the regrowth interface cannot be depleted and the electron concentration at the regrowth interface remains high. Only when a high reverse bias (~2V) is applied, is the surface accumulation charge depleted. This simulation result agrees very well with the C-V measurement result displayed in Fig.3.24.

To study the origin of this n-type sheet charge accumulation, a series of samples were subjected to different processes, including UV ozone treatment, SiN depostion and dry etch, tungsten sputtering and dry etch, HF cleaning, high temperature annealing, as well as a modestly extended phosphorous annealing in

the MBE chamber. The impurities at the regrowth interface were subsequently analyzed by secondary ion mass spectrometry (SIMS). As expected, among these samples significant but highly variable carbon and oxygen concentrations were found at the regrowth interface. Fig.3.27 shows the carbon and oxygen SIMS profiles of two samples, #030836C and #031019A. For #030836C, there were no processing steps before the HBT regrowth except for the wet etch of the InGaAs protecting layer. For #031019A, a series of processing steps were applied to simulate the pedestal HBT fabrication process, including tungsten sputtering and dry etch, SiN deposition and dry etch, high temperature annealing and HF cleaning.



(a)



(b)

Fig.3.27 Intensity of SIMS signal of two samples subjected two different processes before regrowth, (a) shows the $^{12}C^{-}$ concentration, while (b) shows the $^{16}O^{-}$ concentration.

As can be seen from Fig.3.27, These two samples' carbon and oxygen concentrations were very different on the regrowth interface, most likely due to the different processing steps applied. Also notice that the base carbon doping densities in #030836C and #031019A were $5.0x10^{19}cm^{-3}$ and $7.5x10^{19}cm^{-3}$ respectively, and this difference is reflected in the SIMS carbon profile. This verifies the accuracy of the SIMS data.

Large junction area HBTs were fabricated on all these test samples. CV measurements were performed on the reverse-biased base-collector junctions and regrowth interfacial charge accumulation was observed on all these samples. The interfacial charge density values were calculated and are listed in Table 3.5.

For all tested samples, experiencing a variety of surface treatments, the interfacial accumulation charge densities nevertheless were relatively constant, varying only between 1.6×10^{12} cm^{-2} and 1.9×10^{12} cm^{-2}. The interfacial carbon and oxygen concentration, as analyzed by the SIMS and clearly displayed in Fig.3.27, were highly variable from sample to sample. These results suggested that absorption of carbon or oxygen was not likely to be the origin of the observed interfacial charge accumulation.

Silicon atoms were also suspected of being a possible donor source on the regrowth interface, since the wet etch of the protecting InGaAs layer was performed in glass vessels and Si ions could be produced and adsorb to the regrowth surface. However, in the SIMS analysis, only very weak silicon signal was detected on the regrowth interface (Fig.3.28), and its concentration was much lower than the interfacial accumulation charge density.

Sample#	Process steps before regrowth	Regrowth interfacial charge density N_S (cm^{-2})
#030836C	No processing steps	$1.61x10^{12}$
#030242	800 °C annealing	$1.82x10^{12}$
#030305	SiN deposition + dry etch + HF cleaning	$1.67x10^{12}$
#030556	SiN deposition + dry etch + HF cleaning + 800 °C annealing	$1.73x10^{12}$
#030620	Tungsten sputtering + dry etch	$1.72x10^{12}$
#030646D	Tungsten sputtering + dry etch + SiN deposition + dry etch + HF cleaning + 800 °C annealing	$1.80x10^{12}$
#031125	No processing steps before regrowth, oxide desorption time prolonged for 5 min	$1.65x10^{12}$

Table 3.5 Regrowth interfacial charge densities of test samples subjected to different processing steps before MBE regrowth.

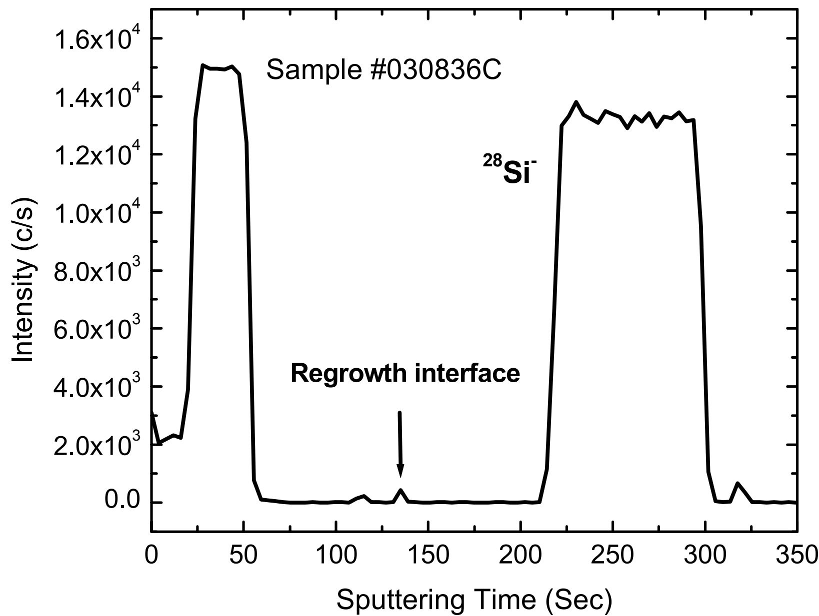


Fig.3.28 Intensity of silicon SIMS signal of Samples #030836C.

Since our SIMS analysis suggest that the adsorption of impurities like carbon, oxygen and silicon adsorption at the interface is not the origin of the surface charge, a stronger hypothesis is that the n-type charge accumulation arises from states associated with disorder at the regrowth interface. It is well known that InP surface states usually pin the Fermi-level ~0.3 eV below the conduction band, independent of the InP bulk doping level and the type of metal contact used. This indicates the presence of surface donor-like states and is also very similar to the stability of the regrowth interfacial charge density observed in our experiments.

3.6.3 Interfacial Charge Compensation

Although we are still investigating the origin and mechanism of surface charge accumulation with the objective of fundamentally eliminate it, there is another short-term approach to allow fabrication of functioning HBTs. If the accumulated n-type charges are compensated by the addition of p-type doping, then the pedestal layer will be fully depleted at low base-collector bias. However, to correctly compensate the interfacial charges, several issues need to be addressed.

First, we need to know how much p-type counter doping we should apply. Because the interfacial charge density proved stable, the required amount of counter doping is easy to determine. However, small variation between samples in the interfacial charge density still exists. Further, the amount of p-type dopant in the compensation layer grown above the regrowth interface will vary from designed values, since small doping calibration error is unavoidable. Therefore, it is not possible to apply an exact compensation of the n-type charge density by p-type counter-doping. Hence, it is important to know how much error margin in dopingwe have without compromising the device performance.

At 0.3 V base-collector reverse bias, Bandprof simulations show that when the p-type compensating dopant density is higher than the n-type surface charge density by $1.2\text{x}10^{12}$ cm^{-2}, holes start to accumulate on the regrowth interface. On the other hand, when the p-type compensating dopant density is lower than n-

type surface charge by $4.0\text{x}10^{11}$ cm^{-2}, electrons will accumulate at the interface. From these simulation results it can be estimated that the acceptable error margin for the compensating doping density is $1.6\text{x}10^{12}$ cm^{-2}. This value far exceeds the normal variations of interfacial charge density and MBE doping calibration error, and thus indicates that successful interfacial charge compensation is possible.

Secondly, the position of the compensating doping layer needs to be considered as well. The compensating doping layer can be grown immediately above the regrowth interface during the HBT regrowth. It can also be grown immediately above the pedestal layer during the first expitaxial growth and hence be placed immediately below the regrowth interface. After several experiments we chose to locate the compensating layer above the regrowth interface. There are two reasons. First, as discussed earlier, the carrier accumulation could be related to the band bending near the interface caused by the ionized donor levels associated with surface states. These charged centers are concentrated at the interface and could diffuse into the overlayer during the regrowth. By counter doping above the regrowth interface, the additional dopant can reduce the charge center diffusion characteristic Debye length and thus effectively alleviate the charge center diffusion. Secondly, if the counter doping layer is included in the pedestal template, this thin p-type InP or InGaAs layer will be partially etched during the wet etching of the top sacrificial layer before the regrowth. The real

thickness of the compensating layer therefore becomes difficult to control. This problem will disappear if the compensating layer is grown during second epitaxial growth.

3.6.4 Be-InP and C-InGaAs charge compensation layers

It has been reported that carbon behaves as a donor in InP.[13] For this reason, if a p-type InP delta-doping layer is to be used to compensate the n-type interfacial charges, we must use beryllium since it is the only other p-type dopant source available in our MBE system. Also for MBE growth of InP, beryllium is preferred to the other usual acceptor impurities (Zn, Mg, Cd) because Be exhibits a sticking coefficient close to unity and provides for a fairly shallow acceptor level.

Beryllium-doped thin InP layer was therefore used for carrier compensation at the regrowth interface and a series of test samples were regrown with different Be sheet density. The results of these experiments, however, were not consistent. For most test samples, the C-V results exhibited a lower voltage required for pedestal layer depletion compared with previous results observed from samples with direct HBT regrowth and no compensating layer. Nevertheless, the carrier compensation effect was much weaker than expected. Fig.3.29 shows the C-V profile of a test sample with a 30 Å Be-InP layer. The total Be sheet density on the regrowth interface was $1.9\text{x}10^{12}$ cm^{-2} according to

the Be:InP doping calibration results. It is seen that although C_{BC} starts to decrease at $V_{CB} = 0.5$ V, the pedestal layer did not become fully depleted until $V_{CB} = 2$ V. From these data, the net carrier concentration at the regrowth interface was calculated to be 1.4×10^{12} cm^{-2}. Clearly only a fraction of the accumulation charges were compensated by the Be:InP layer.

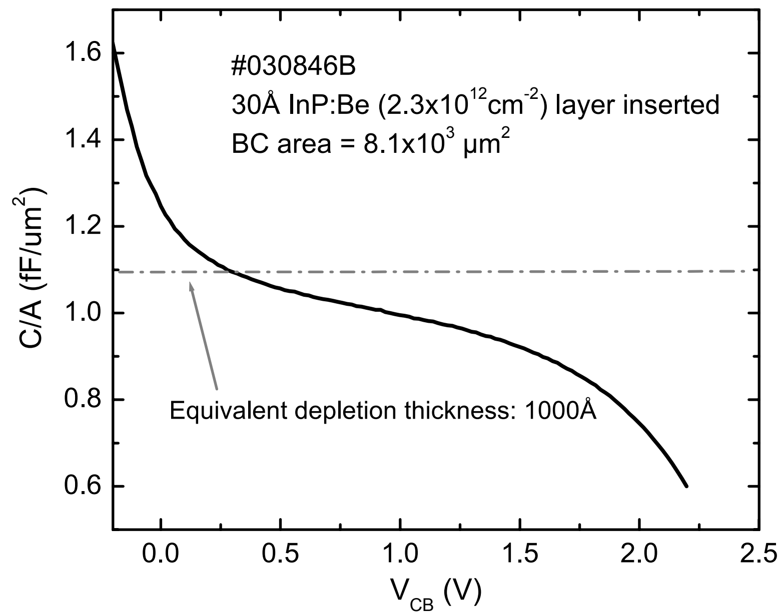


Fig.3.29 C-V measurement profile across the base-collector junction of a large-area HBT grown with a Be-InP compensating layer on the regrowth interface.

This ineffectiveness of the Be-InP compensating layer was attributed to the existence of oxygen at the regrowth interface. It has been reported that oxygen tends to compensate the Be doping efficiency in GaAs, InGaAs and InP.[14], [15]

With high oxygen impurity concentration, Be-InP was even found to be n-type in Hall measurements. Since Be is very reactive, it is likely that the oxygen compensation in Be-doped InP is chemical effect, due to the formation of electrically inactive Be-O complexes.

Carbon-doped InGaAs layer was then instead used. Carbon is not as active as Beryllium and therefore much less susceptible to the influence of oxygen on the regrowth interface. To investigate carbon-doped InGaAs compensating layer's effectiveness, samples with different amount of carbon dapants were grown and tested. Fig.3.30 exhibits the base-collector junction C-V profiles of five samples with 0 Å, 10 Å, 20 Å, 30 Å, and 40 Å C-InGaAs layers inserted immediately above the regrowth surface. The carbon doping density in the InGaAs layers was $5.0\times10^{18}cm^{-3}$, according to doping calibrations. It is clear that the pedestal layer becomes progressively easier to deplete with increasing carbon doping on the regrowth surface. When the C-InGaAs thickness reaches 40 Å, the compensating InGaAs layer's carbon sheet density is 2.0×10^{12} cm^{-2}, approximately equal to the n-type interfacial charge density. For this sample, the collector and pedestal layers become fully depleted when V_{CB} = 0.3V. It is evident that with this compensating layer present, full depletion of the collector regions outside the pedestal will be obtained at low V_{CB} and thus the base-collector capacitance in that region can truly be reduced.

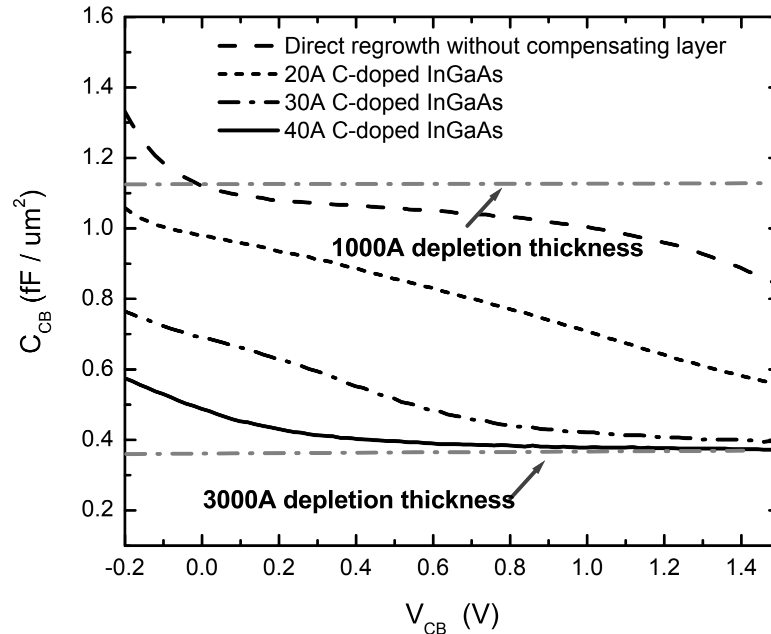


Fig.3.30 C-V profiles across the base-collector junctions of large-area test device with C-InP compensating layers of different thickness.

3.7 Device Results

After successfully compensating the negative sheet charge on the regrowth interface, second generation small-area HBTs were fabricated. Compared with the first generation pedestal HBTs, the device layout was changed and the base contact pad area was significantly reduced to further decrease the base-collector parasitic capacitance. The plane view and schematic cross-section of the HBT are illustrated in Fig.3.31. In the device fabrication process, various pedestal

implant mask widths (W_P) were used to systematically investigate of the pedestal structure's effectiveness in base-collector capacitance reduction.

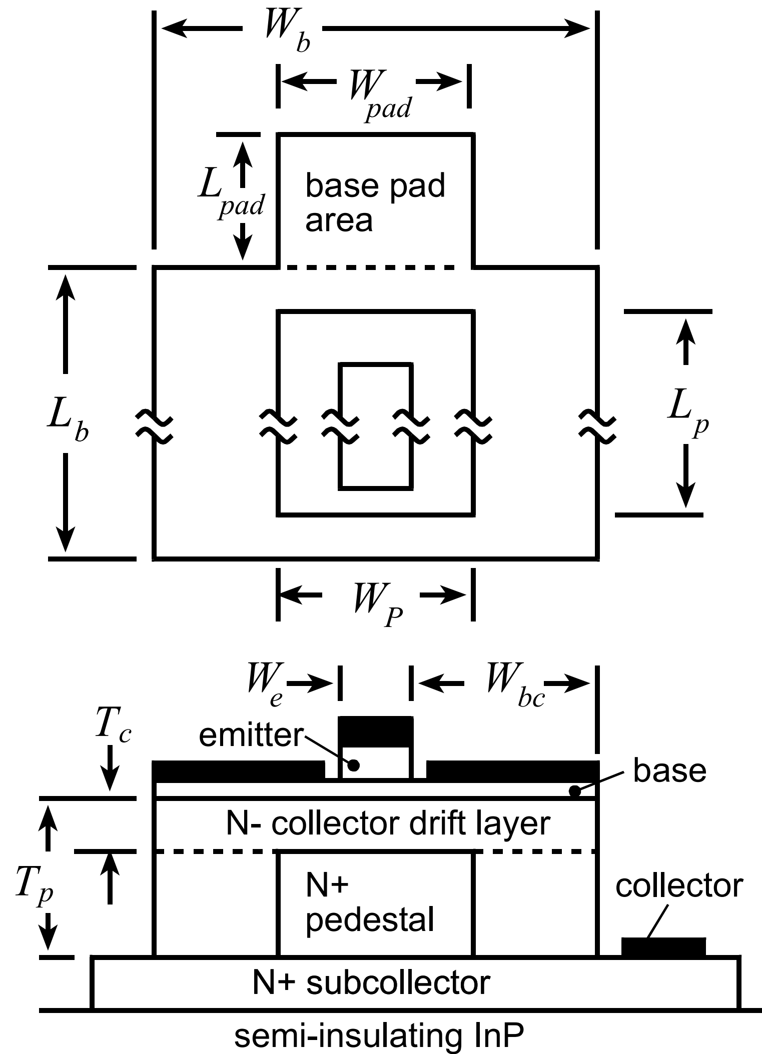


Fig.3.31 Plane view and schematic cross-section of the HBT with selectively implanted collector pedestal.

There were also some changes to the device layer structure compared to the first process run of small area pedestal HBTs. The base layer thickness was thinned from 400 Å to 300 Å and carbon base doping grade from $8x10^{19}$ cm^{-3} to $5x10^{19}$ cm^{-3} was used to reduce the base transit time. The collector thickness was reduced to 900 Å and the collector doping density was increased to $6x10^{16}$ cm^{-3} to enhance the Kirk threshold current. Also as described in the previous section, a 40 Å $2.0x10^{12}$ cm^{-2} p-type carbon-doped InGaAs charge compensating layer was grown immediately above the regrown interface, so that full depletion of the collector regions outside the pedestal could be obtained.

The fabrication process was similar to that described in 3.6.1 except that BCB was used to planarize and passivate the HBTs instead of polyimide. It has been reported that BCB passivation was better than polyimide massivation in terms of reducing InP and InGaAs p-n junction surface leakage current,[16] and this is consistent with observations at UCSB. Fig.3.32 displays a SEM image of a device with 0.5x7 μm^2 emitter junction area and 0.7 µm base contact width on either side of the emitter. It can be seen that a base plug was placed at the end of the base, and the thickness of the base plug is such that it becomes level with the emitter metal. In this way, after the BCB planarization and etch back processes, the emitter metal and base plug metal can be exposed simultaneously and no extra step is needed to etch through BCB to contact the base metal.

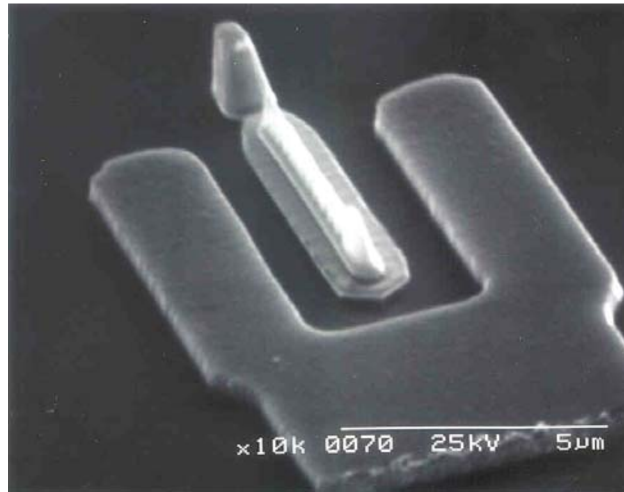


Fig.3.32 SEM image of a device with 0.5x7µm² emitter junction area and small base contact pad area.

3.7.1 DC Characteristics

Fig. 3.33 shows the Gummel characteristics of an HBT with W_E=0.4 μm and emitter length L_e=7 μm. The base n_b and collector n_c current ideality factors are both low, and I_{cbo} is also low, 320 pA at V_{cb}=0.3 V. The observed n_b, n_c, and I_{cbo} are similar to that we observe with HBTs fabricated without junction regrowth, indicating high regrown HBT material quality. The common-emitter characteristics, as shown in Fig.3.34 indicate a DC current gain $\beta \cong 10$, again typical of non-regrown DHBTs grown in our laboratory with high (8×10^{19} cm^{-3}) base doping. For the pedestal HBTs, the observed $V_{br,ceo}$= 5.3 V is significantly

higher ($V_{br,ceo}$ =4.1 V) than that of reference devices having the same T_c = 90 nm depletion thickness over the full width of the base-collector mesa ($W_p = W_b$). The reference devices are similar in structure to conventional mesa HBTs; we attribute their reduced $V_{br,ceo}$ to premature surface breakdown due to surface state charge density.[17], [18] In the pedestal HBTs, the thin 900 Å collector depletion region is not exposed to the surface. The pedestal HBT's collector breakdown field is $E_{\max} = 5.9 \cdot 10^5$ V/cm. Given that collector electron velocity $v_{eff} \cong 3.2 \cdot 10^7$ cm/s [19], the associated Johnson figure-of-merit is very high: $E_{\max} v_{sat} \cong 1.9 \cdot 10^{13}$ V/s.

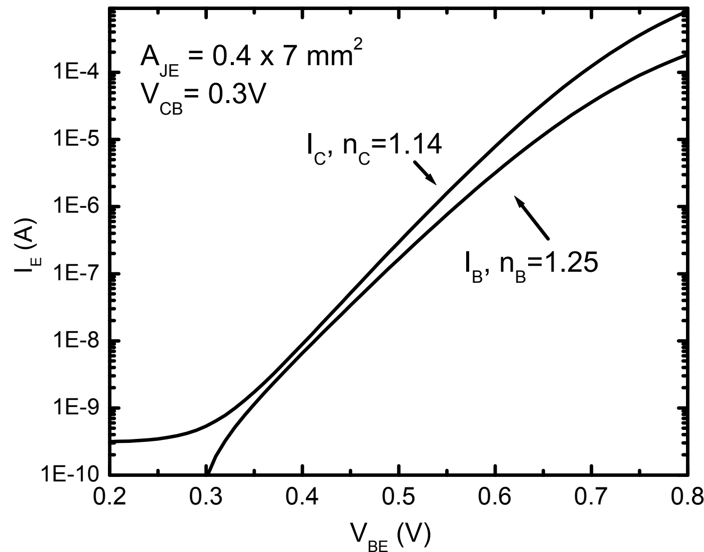


Fig. 3.33 Gummel ($\log(I_b, I_c)$ vs. V_{be}) characteristics of an HBT with a 0.4 μm × 7 μm emitter and a 0.8 μm × 8.5 μm collector pedestal.

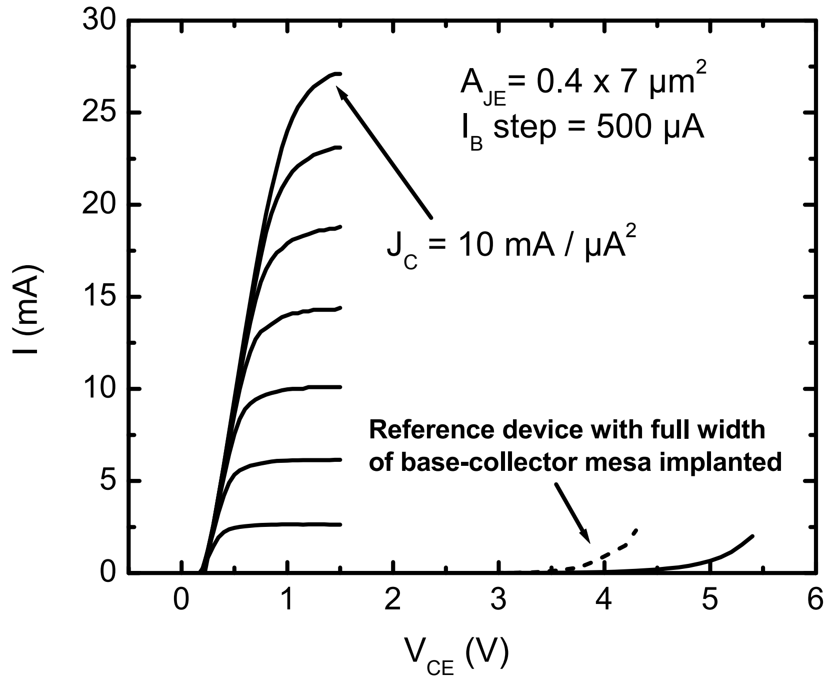


Fig.3.34 Common Emitter characteristics of an HBT with a 0.4 μm × 7 μm emitter and a 0.8 μm × 8.5 μm collector pedestal. Common-emitter breakdown $V_{br,ceo}$ is 5.3 V. Also shown is the common-emitter characteristics at I_b = 0 mA, for a reference device having no pedestal ($W_p = W_b$ and T_c =90 nm), showing $V_{br,ceo}$ = 4.1 V.

The DC safe operating area (SOA) is shown in Fig.3.35. Bias points for device failure (shown) are at ~ 20 mW/μm^2 dissipation. It is therefore demonstrated

that the device can be biased well above the conditions required for high transistor bandwidth.

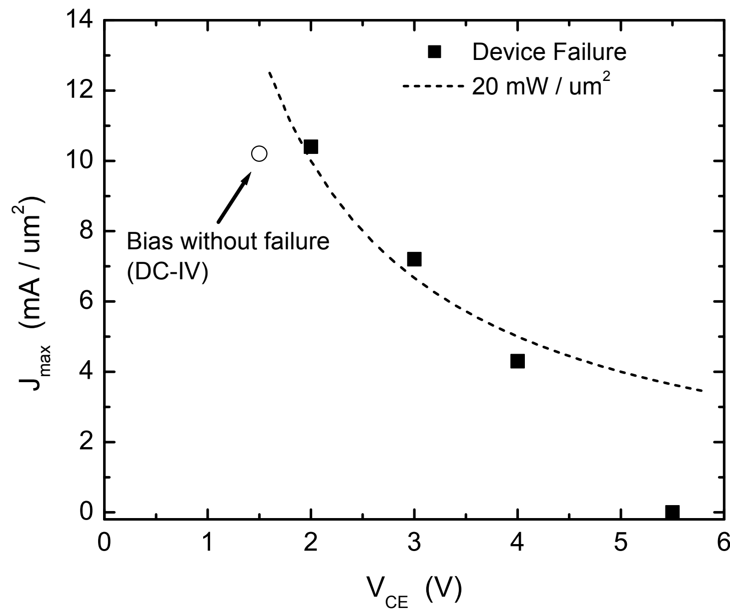


Fig.3.35 Measured safe operating area of HBTs with 0.4x7 μm^2 emitter size.

3.7.2 RF Characteristics

The microwave 2-port parameters were characterized by s-parameter measurement from 5-40 GHz. The total base-collector capacitance C_{BC} was calculated from the imaginary part of Y_{12}. Fig.3.36 shows the variation C_{BC} as a function of J_C at V_{CB}=0.3V for devices with different collector pedestal width W_P. As illustrated in Fig.3.31, the base-collector capacitance is equal to

$$C_{BC} = \frac{\varepsilon_r W_b L_p}{T_p} + \varepsilon_r L_p (\frac{1}{T_c} - \frac{1}{T_p})(W_p + \Delta W_p) + C_{Bpad}, \qquad (3.4)$$

where T_c and T_p are the depleted collector thicknesses above and outside the pedestal region, L_P is the impanted pedestal length, W_b is the base mesa width, W_p is the collector pedestal mask width, ΔW_p is the extra collector pedestal width caused by implant mask dimensional variation in processing and implant straggle, and C_{Bpad} is the base-collector capacitabce associated with the base-pad region.

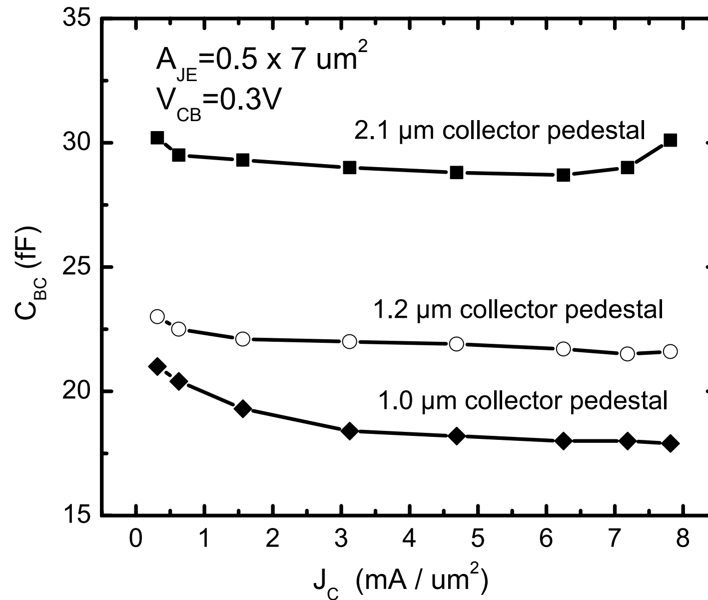


Fig.3.36 Variation of C_{cb} dependence with current density J_e for devices with different collector pedestal width W_p.

As shown in Fig.3.36, at J_e = 6 mA/μm^2 and V_{cb} =0.3 V, HBTs with W_p =1.0 μm showed C_{cb} = 18 fF, as compared to C_{cb} = 29 fF for devices with the 90 nm depletion thickness over the full collector-base mesa area, a 1.6:1 reduction in C_{cb}. All HBTs of Fig.3.36 have T_c =900 Å, T_p =2700 Å, L_E = 7.0 μm, L_b = 8.5 μm, W_E = 0.5 μm, and W_b = 2.1 μm, and have a base contact pad area of dimensions L_{pad} =3.0 μm and W_{pad} = 1.2 μm.

To further investigate the effective collector pedestal width, we plot C'_{BC} against the collector pedestal mask width W_p to determine the value of ΔW_P, as shown in Fig.3.37. C'_{BC} is the base-collector capacitance without including C_{Bplug}. From the intercept in Fig.3.37, we find that ΔW_P= 0.30µm, which indicates that the implant straggle and the SiN mask dry etch undercut widen the collector pedestal by 0.15 µm on each side of the implant window. With improved implant window dry etch process, this value can be reduced.

From h_{21} and Mason's Gain, F_t=170GHz and F_{max}=150GHz were extracted. Both cutoff frequencies were low due to very high emitter and base resistances caused by an error in etchback process which left a thin layer of polymer on the emitter and base metal before deposition of the interconnect metals.

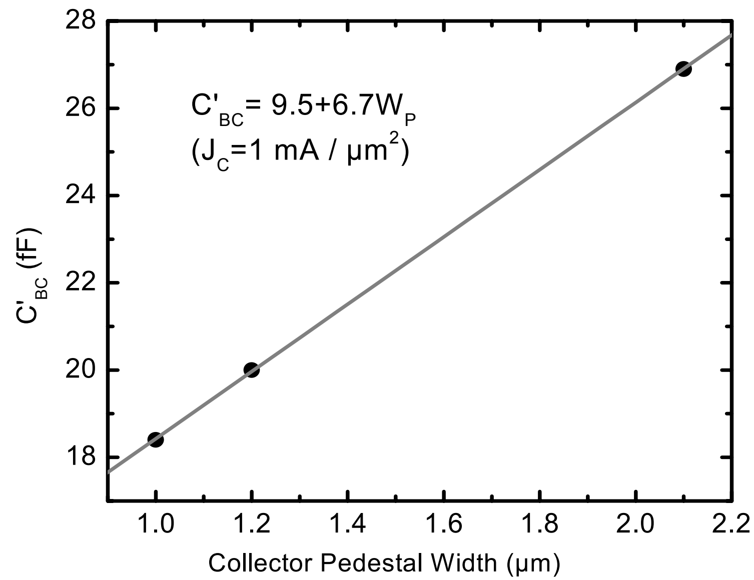


Fig.3.37 C_{BC} dependence on collector pedestal width at $J_C = 1\ mA/\mu m^2$.

The emitter resistance fly-back measurement result is shown in Fig.3.38. For a device with a 0.5 x 7 μm^2 emitter junction area, the measured emitter resistance is 26 Ω, which exhibits an emitter contact resistivity as high as 90 $\Omega\cdot\mu m^2$. Better mesa HBTs fabricated at UCSB show emitter contact of 15 $\Omega\cdot\mu m^2$.

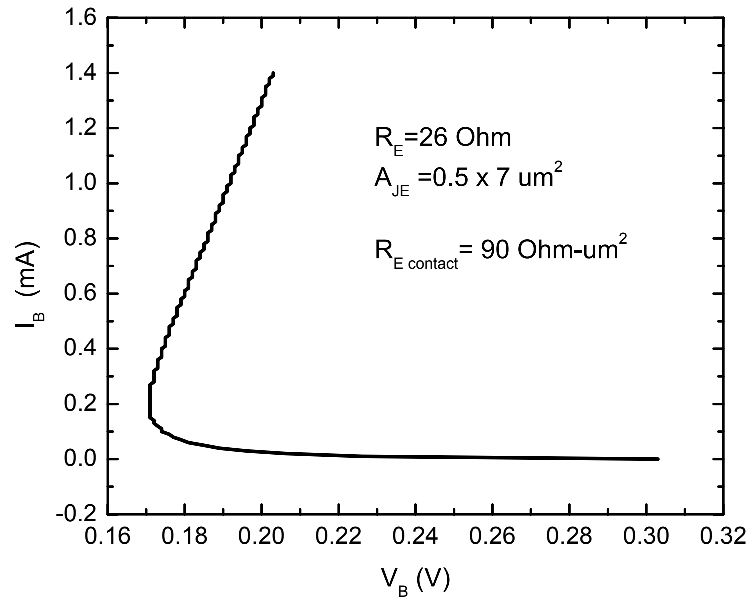


Fig.3.38 Emitter resistance fly-back measurement result for a device with a 0.5 x 7 μm² emitter junction area.

3.8 Summary

In InP HBTs, the collector-base capacitance (C_{cb}) strongly limits mm-wave power gain and digital switching speed and should be minimized. In mesa HBTs, a large portion of C_{cb} originates from the extrinsic base-collector region under the base contact. In this case, reducing the emitter width significantly increases HBT bandwidth only if the base contact width is proportionally reduced; reduction of base contact width is constrained by nonzero Ohmic

contact resistivity, nonzero base metal sheet resistance, and process dimensional tolerances. To reduce this excess C_{cb} we propose and fabricate an InP HBT with a collector pedestal. The pedestal, formed using selective ion implantation and regrowth by molecular beam epitaxy, permits a larger collector depletion thickness under the base contacts than the collector depletion thickness directly under the emitter. The extrinsic C_{cb} can then be reduced without increasing the collector transit time $\tau_c = T_c / 2v_{eff}$ or decreasing the Kirk-effect-limited current density $J_{Kirk} \propto v_{eff} / T_c^2$.

Silicon implantation in InP has been carefully investigated, including the implant energy and fluence necessary to form a low resistance as well low damage collector pedestal region, optimum implant temperature, proper annealing temperature and condition, and dopant activation efficiency. Implant lateral distribution and its influence to pedestal device performance was simulated and later proved consistent with the experimentally measured results.

To improve the regrowth material quality, a series of growth experiments were performed to systematically study the impacts of the processing steps, including sputtering, dry etch, implantation and annealing, to the subsequent MBE regrowth. A number of contamination sources leading to growth defects and high junction leakage current were discovered and several surface cleaning methods were adopted and proved effective. High temperature annealing was

also found to be able to substantially remove the surface damages and help improve the regrowth quality.

The RF characteritics of the first generation pedestal HBTs exhibited high base-collector capacitance caused by incomplete collector depletion outside the pedestal region. The capacitance-voltage measurements indicated a large negative sheet charge density $N_s \cong -1.8 \cdot 10^{12} / \text{cm}^2$ at the regrowth interface. Experiments performed on a range of samples with various surface cleaning procedures prior to MBE regrowth exhibited $N_s \cong -(1.8 \pm 0.2) \cdot 10^{12} / \text{cm}^2$. [20]Because N_s proved stable with variations in processing, it was compensated through introduction of a 40 Å, $2 \cdot 10^{12} / \text{cm}^2$ P-type carbon-doped $In_{0.53}Ga_{0.47}As$ charge compensation layer grown immediately above the regrowth interface. With this compensation layer present, full depletion of the collector regions outside the pedestal was obtained at low V_{cb}.

The pedestal HBTs showed excellent DC characteristics including extremely low I_{cbo}, and low junction ideality factors, indicating that high junction quality could be obtained in a collector pedestal process incorporating MBE regrowth. The HBTs exhibited a 1.6:1 reduction in C_{cb} and a 1.3:1 increase in common-emitter breakdown voltage $V_{br,ceo}$ over devices of the same T_c but without the pedestal.

The measured peak f_τ and $f_{\max}$ are low due to very high emitter and base resistances caused by an error in processing which left a thin layer of polymer on the emitter and base metal before deposition of the interconnect metals. The present samples nevertheless show clearly key expected pedestal HBT characteristics, including reduced C_{cb}, increased $V_{br,ceo}$, and low I_{cbo}. With emitter and base contacts of normal quality and with further scaling, it is feasible to realize transistors with f_τ and $f_{\max}$ exceeding 500 GHz, and $V_{br,ceo}$ exceeding 5 Volts.

References

[1] M. Sokolich, M.Y. Chen, D.H. Chow, Y. Royter, S. Thomas III, C.H. Fields, D.A. Hitko, B. Shi, M. Montes, S.S. Bui, Y.K. Boegeman, A. Arthur, J. Duvall, R. Martinez, T. Hussain, R.D. Rajavel, K. Elliot, and J.D. Thompson, 'InP HBT integrated circuit technology with selectively implanted subcollector and regrown device layers', 25th IEEE GaAsIC Symposium, San Diego, CA, USA, Nov. 2003

[2] R. Cusco, J. Ibanez, N. Blanco, G. Gonzalez-Diaz, and L. Artus, 'Study of Si implanted and annealed InP by means of Raman spectroscopy', Nuclear Instruments & Methods in Physics Research Section, B-Beam Interactions with Materials & Atoms, Vol.132, No.4, pp.627-32, 1997

[3] M.V. Rao, R.K. Nadella, and O.W. Holland, 'Elevated-temperature 3-MeV Si and 150-keV Ge implants in InP:Fe', J. Appl. Phys., Vol.71, No.1, pp. 126-132, 1992

[4] C. Ferrari, P. Franzosi, L. Gastaldi and F. Taiariol, 'Crystal quality investigation of InGaAs/InP and InGaAlAs/InP single heterostructures grown by molecular-beam epitaxy', J. Appl. Phys. Vol. 63, No. 8, pp. 1228-32, 1988

[5] H. Kroemer, 'Two integral relations pertaining to the electron transportthrough a bipolar transistor with a nonuniform energy gap in the base region', Solid State Electronics, Vol. 28, No. 11, pp.1101-1103, 1985

[6] M.J.W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthroe, Y. Bester, S.C. Martin, R.P. Smith, S. Jaganathan, S. Krishnan, S. Long, R. Pullela, B.

Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlstrom, 'Submicron Scaling of HBTs', IEEE Tran. Electron Devices, Vol. 48, No. 11, pp.2606-2624, 2001

[7] D. Streit, M. Hazafi, D. Umemoto, J.R. Velebeir, L. Tran, A. Oki, M. Kim, S. Wang, C. Kim, L. Sadwick, and R.J. Hwu, 'Effect of exponentially graged base doping on the performance of GaAs/AlGaAs heterojunctionbipolar transistirs', IEEE Electron Device Letters, Vol. 12, No. 5, 1991

[8] M. Dahlstrom, X.M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y.M. Kim, Y. Wu, J.M. Fastenau, W.K. Liu, and M.J.W. Rodwell, 'Wideband DHBTs using a graded carbon-doped InGaAs base', III Electron Device Letters, Vol. 24, No. 7, pp. 433-5, 2003

[9] Z. Griffith, M. Dahlström, M. Urteaga, M.J.W. Rodwell, X.-M. Fang, D. Lubyshev, Y. Wu, J.M. Fastenau, and W.K. Liu, 'InGaAs/InP mesa DHBTs with simultaneously high ft and fmax, and low Ccb/IC ratio', submmited to IEEE Electron Dev. Lett.

[10] A. Dodabalapur, T.Y. Chang, B. Tell, and K.F. Brown-Goebeler, 'Growth of InAlAs/InGaAs and InGaAlAs/InGaAs heterojunction bipolar transistors on Si-implnated InP substrates by molecular beam epitaxy', J. Appl. Phys., Vol. 71, No. 5, pp.2449-51, 1992.

[11] G. Tuttle, H. Kroemer, and J.H, English, 'Effects of interface layer sequencing on the transport properties of InAs/GaSb quantum wells: evidence for antisite donars at the InAs/AlSb interface', Journal of Appl. Phys., Vol. 67, No. 6, pp. 3032-7, 1990

[12] Bandprof was the band structure simulation software kindly provided by Prof. William R. Frensley at Electrical Engineeing Department, University of Texas, Dallas.

[13] M. Weyers and K. Shiraishi, 'Carbon in III-V compounds: a theoretical approach', Jpn. J. Appl. Phys., Vol. 31, No. 8. pp. 2483-7, 1992

[14] T. Humer-Hager and P. Zwicknagl, 'Influence of oxygen implantation on the carrier concentration profile in p-GaAs', Appl. Phys. Lett., Vol. 52, No. 1, pp.63-64, 1986

[15] E. Von Neida, S.T. Pearton, W.S. Hobson, and C.R. Abernathy, 'Interaction of Be and O in GaAs', Appl. Phys. Lett., Vol. 54, No.16, pp.1540-1542, 1989

[16] H.S. Kim, J.H. Shi, H.M. Bang, Y. Jee, S.W. Yun, J. Burm, M.D. Kim, and A.G. Choo, 'Dark current reduction in APD with BCB passivation', Electronic Lett., Vol. 37, No. 7, pp. 455-457, 2001

[17] L.S. How Kee Chun, J.L. Courant, P. Ossart, G. Post, "In-situ surface preparation of InP-based semiconductors prior to direct UVCVD silicon nitride deposition for passivation purposes". 1996 IEEE Conference on Indium Phosphide and Related Materials Schwabisch-Gmund, Germany, 21-25 April 1996

[18] L.S. How Kee Chun, J.L. Courant, A. Falcou, P. Ossart, G. Post, "UV-deposited silicon nitride coupled with XeF2 surface cleaning for III-V optoelectronic device passivation", Microelectronic Engineering, Vol.36, No.1-4, Elsevier, pp. 69-72, June 1997

[19] Mattias Dahlström , Mark J.W. Rodwell: "Current Density Limits In InP DHBT: Collector Current Spreading And Effective Electron Velocity", Proceedings, 2004 IEEE

Indium Phosphide and Related Materials Conference, May 31-June 4, Kagoshima, Japan

Chapter 4

InP HBT with Polycrystalline Extrinsic Base — Material Aspects

4.1 Introduction

As discussed in Chapter 3, despite superior electron transport and breakdown characteristics, InP HBTs have thus far failed to provide decisive advantages in mixed-signal ICs, due to rudimentary, low performance, and low-yield fabrication processes. It is believed that with the adoption of advanced SiGe-like fabrication processes, large potential improvements in speed and yield are possible, which will enable a new generation of mixed-signal applications.

SiGe technology uses a regrown (polysilicon) extrinsic emitter, which allows for an emitter contact much larger than the emitter junction. This produces a low-resistance emitter contact and permits SiGe HBTs to operate at very high current densities, a decisive advantage in fast digital and mixed-signal

ICs. In addition, an SiGe HBT uses buried oxide layers in combination with the regrown polysilicon base contact layers, allowing a narrow collector junction and large base ohmic contacts. This reduces the $R_{bb}C_{cb}$ product, partially offsetting the poor resistance and low collector electron velocity. In marked contrast, present InP HBTs with their triple mesa processes have large base-collector junction areas, as stipulated by the need for base contacts of non-zero size and the unfortunate presence of a parasitic collector junction under the base contacts.

Present InP HBT fabrication processes also result in limited yield and scales of integration. It has been found that the standard InP emitter-base junction fabrication process has increasingly low yield as the emitter dimensions are scaled below 1μm. The low yield is a consequence both of the self-aligned liftoff used to form base contacts close to emitter, and to the formation of the emitter-base junction through etch processes, which necessarily include both wet-chemical etch and dry reactive-ion procedures.

The superior yield and scales of integration of Si/SiGe HBTs result from its unique fabrication processes (Fig.4.1). Submicron emitter-base junctions are formed by a combination of crystalline and polycrystalline regrowths, not by mesa etching.

One clear path to high performance mixed-signal ICs is to combine the best features of SiGe and InP HBT technology. We investigate an HBT technology,

whose structural features and process flow are as close as possible to that of a Si/SiGe HBT, but using InP-based semiconductor materials. The double-regrowth InP HBT is proposed accordingly, and the fabrication processes are illustrated in Fig.4.2.

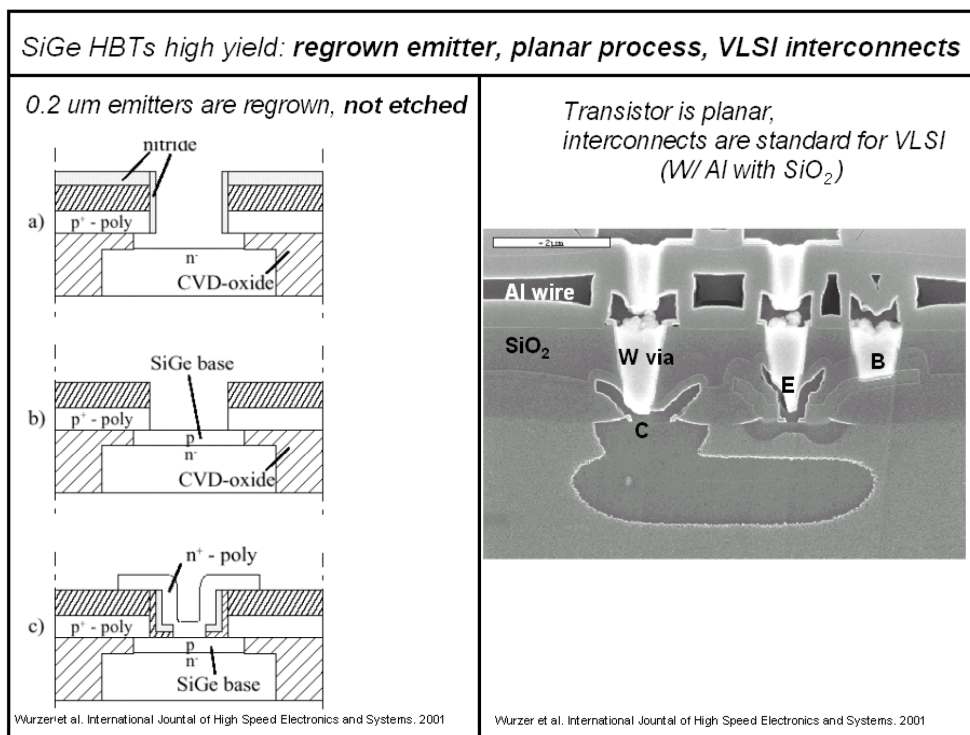


Fig.4.1 Factors responsible for high yield in Si/SiGe HBT processes.

The process starts with formation of a collector pedestal. As shown in Fig.4.2, the pedestal is formed by etching through the N- collector and into the N+ subcollector, with a subsequent Si_3N_4 replanization step. This replanization

will be performed by depositing a very thick Si_3N_4 film by PECVD, and subsequently etching it back until the collector top surface is reached.

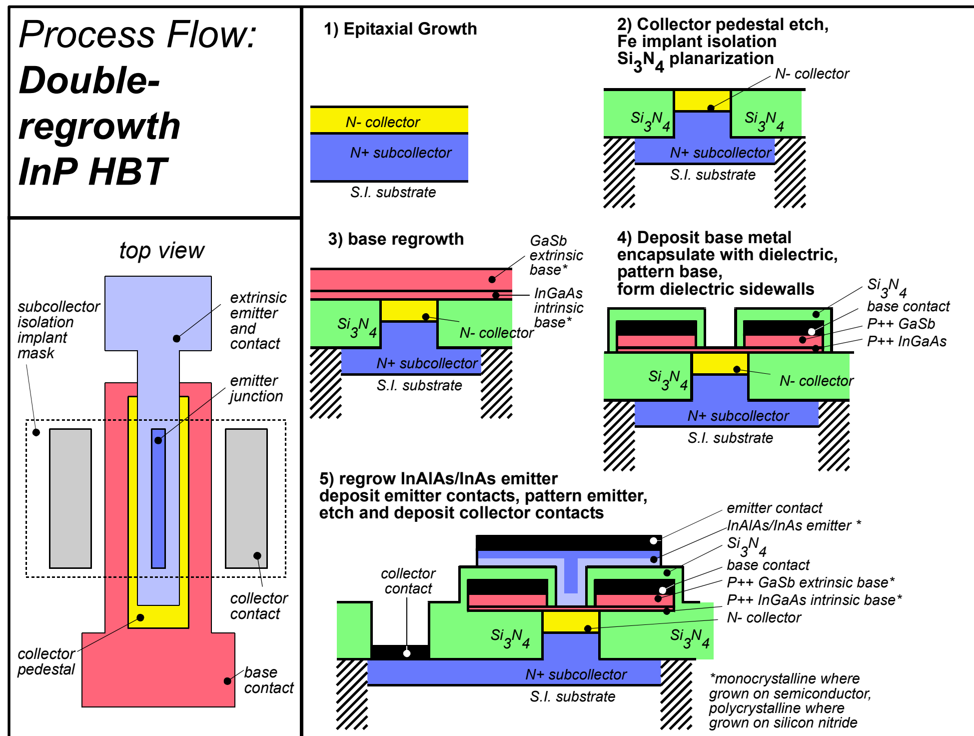


Fig.4.2 Double-regrowth InP HBT process flow.

The collector pedestal can also be formed by coating the wafer with Si_3N_4, pattering and etching openings into the Si_3N_4, and regrowing by MOCVD the N- and N+ layers in the openings. The MOCVD version of the collector pedestal process flow is similar to that used in SiGe technology, as shown in Fig.4.1.

Subsequent to collector pedestal formation, the base layers are regrown by non-selective-area epitaxy (MBE), forming monocrystalline layers where grown on semiconductor and polycrystalline layers where grown on Si_3N_4. After this extrinsic base regrowth, a refractory base contact is deposited by blanket sputtering, patterned by etching, and encapsulated on both top surface and sidewalls by Si_3N_4 dielectric. The wafer is then placed in an MBE system again and an intrinsic InAlAs or InP and extrinsic InAs emitter layers are grown. Similar to the extrinsic base regrowth, growth is in the normal monocrystalline mode in the emitter window, while the growth is polycrystalline over the Si_3N_4 surface. Emitter metal is then deposited by blanket sputtering and etching, and the emitter metal serves as the etch mask for the emitter semiconductor. The final process step is a recess etch, followed by collector contact deposition.

Through the emitter regrowth, a deep submicron base-emitter junction is formed by regrowth, avoiding the emitter-base etch step of mesa HBTs, a step which has progressively larger impact upon yield as emitter dimensions are reduced. Secondly, the N-type emitter contact layer can be defined with a width much greater than the emitter-base junction, allowing for a large emitter contact and thereby a low emitter resistance. Through the extrinsic base regrowth, a small excess collector-base capacitance can be obtained, resulting form the collector pedestal and the buried dielectric layer in the collector-base junction. This proposed process flow strongly resembles that of Si/SiGe technology.

For this double regrowth InP HBT, the extrinsic base layer is made of polycrystalline III-V material. To minimize the total base resistance, it is of key importance to have low resistivity polycrystalline extrinsic base layer. In this chapter, we discuss our efforts to achieve low resistivity polycrystalline extrinsic base through two approaches. First, p-type polycrystalline GaSb is chosen as a strong candidate to be used as extrinsic base material for GaSb's low energy bandgap, high carrier mobility, and p-type GaSb's favorable surface Fermi level pinning position. We study the growth and electrical properties of low resistance carbon-doped polycrystalline GaSb (poly-GaSb) by molecular beam epitaxy using CBr_4. Several aspects of growth conditions and film properties that significantly affect poly-GaSb film's resistivity are carefully examined. Secondly, we propose to use p-type GaSb capped with n-type InAs as the extrinsic base layer. It has been widely known that InAs-GaSb heterostructure forms a broken-gap band lineup and it is possible for the p-type GaSb's valence band electrons to transfer into the conduction band of the neighboring n-type InAs, giving rise to an ohmic p-n junction. In our work, we examine the contact resistivity across the InAs(n)/GaSb(p) interface at relatively low current density ($< 10^4$ A/cm^2) and its dependence on the doping densities on both sides of the junction.

4.2 Low-Resistance P-type Polycrystalline GaSb

4.2.1 Overview

Polycrystalline GaAs (poly-GaAs) has been applied to the extrinsic base regrowth in GaAs-based HBTs.[1] However, it was not nearly as successful as those of polycryslline silicon in the SiGe BJT technology. One reason could be ascribed to the difficulty of achieving low resistance poly-GaAs. Some efforts have been made to investigate the electric properties of poly-GaAs grown by different methods and a considerably wide range of resistivity values have been reported.[1],[2],[3] The lowest resistivity reported for poly-GaAs is ~$3x10^{-3}$ Ω-cm [3], far too high to achieve low sheet resistance for a thin extrinsic base layer, such as required in the sub-micron double–poly regrowth HBT fabrication process.

A polycrystalline material is composed of small crystallites joined together by grain boundaries. The angle between orientations of the adjoining crystallites is often large. Inside each crystallite the atoms are arranged in a periodic manner so that it can be considered as a small single crystal. Fig.4.3 show the SEM pictures of polycrystalline InAs and GaSb, two examples of polycrystalline materials. It is believed that since the atoms at the grain boundary are disordered, there are a large number of defects due to incomplete atomic bonding. These trapping states at the grain boundaries can pin the surface Fermi

level and significantly influence the bulk conductivity [2], [4]. The trapping states are capable of trapping carriers and thereby immobilizing them. This reduces the number of free carriers available for electrical conduction. After trapping the mobile carriers the traps become electrically charged, creating a potential energy barrier, which impedes the motion of carriers from one crystallite to another, thereby reducing their mobility.

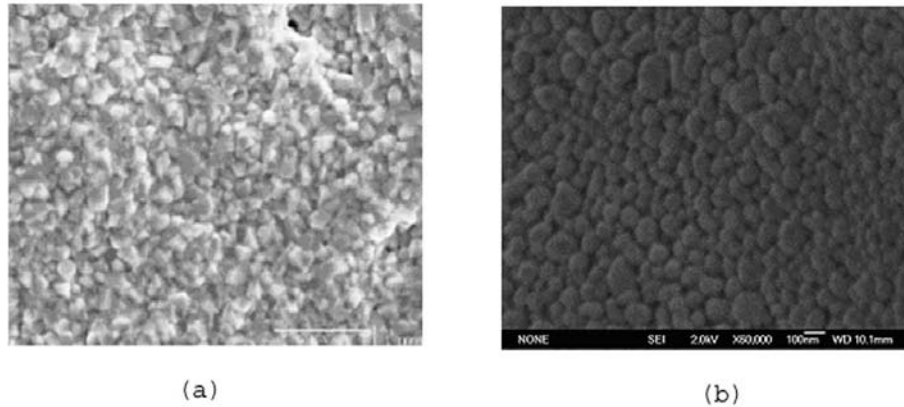


Fig.4.3 SEM picture of (a) polycrystalline InAs and (b) polycrystalline GaSb.

In our study, p-type GaSb has been chosen as a potential candidate for the polycrystalline extrinsic base material for InP-based HBT. Besides GaSb's low energy bandgap and therefore high carrier mobility, another advantage is attributed to p-type GaSb's favorable surface Fermi level pinning position.

It has been found that p-type GaSb's surface Fermi-level is pinned in the valence band[5]. As Fig.4.4 shows, this Fermi level pinning at the grain boundaries partially depletes the carrier concentration. If the effect is strong, as in GaAs, barriers are critical to carrier flow between grain boundaries. The surface pinning of GaSb results in minimal carrier depletion, hence high conductivity is expected.

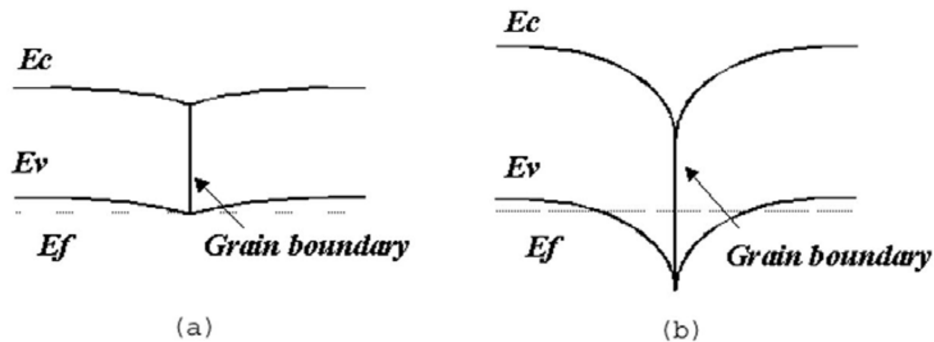


Fig.4.4 Schematic diagrams of the energy band structure near grain boundaries in p-type of (a) GaSb and (b) GaAs.

In this work, we study the growth and electrical properties of low resistance carbon-doped polycrystalline GaSb (poly-GaSb) by molecular beam epitaxy using CBr_4. We examine several aspects of growth conditions and film properties that significantly affect poly-GaSb film's resistivity. It is found that

the resistivity of poly-GaSb film depends strongly on film's thickness and grain size, particularly when the film thickness is comparable with the grain size. We demonstrate that with similar doping level, grain size, and film thickness, the resistivity of poly-GaSb is more than one order of magnitude lower than that of poly-GaAs.

4.2.2 Experimental Procedures

Poly-GaSb samples were grown in a Varian Gen II system equipped with a valved and cracked Sb source. High purity carbon tetrabromide (CBr_4) was delivered into the growth chamber through an ultra-high vacuum leak valve. A 0.3μm thick SiO_2 film was deposited on a semi-insulating (100) GaAs substrate by plasma-enhanced chemical vapor deposition (PECVD) and the sample was then cleaned prior to being loaded into the MBE chamber. The growth rate was 0.2 μm/hr and the CBr_4 flux was fixed with the same leak valve setting.

Hall measurements were performed at 295 K using the van der Pauw geometry at a magnetic field of 4000 G. Indium metal contacts were formed at 200-250°C. Hall measurements were performed on as-grown samples without any additional annealing.

4.2.3 Results and Discussions

Three 1000Å poly-GaSb samples were grown at different substrate temperatures with a fixed antimony to gallium beam flux ratio of 5. Fig.4.5 shows the dependence of the poly-GaSb samples' hole concentration and mobility on the growth temperature.

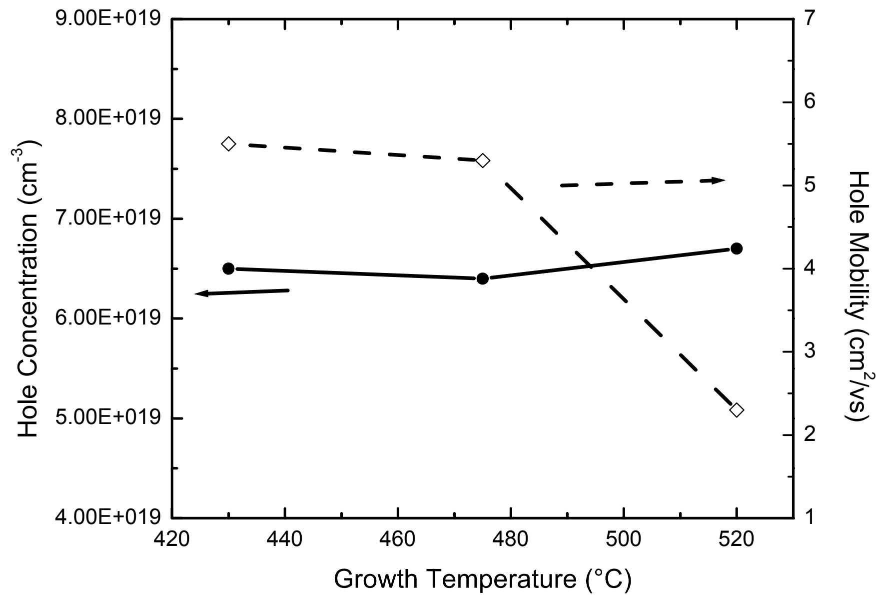


Fig.4.5 The dependence of hole concentration and mobility of poly-GaSb samples on growth temperature

It is clear that the growth temperature strongly influenced the hole mobility, but only weakly affected the hole concentration. This behavior could be related

to the grain size's growth temperature dependence, which is shown in Fig.4.6 together with the resistivity of the same poly-GaSb films.

Fig.4.7 displays the SEM images of poly-GaSb grown at (a) 520ºC and (b) 475ºC at a magnification of 35,000. Clearly the grain size becomes much smaller at a lower growth temperature, decreasing from 250nm to 80 nm. If the potential energy barrier on the grain boundaries impedes the motion of carriers from one crystallite to another and thereby decreases the bulk conductivity hence the apparent bulk hole mobility, it is surprising to find that the hole mobility increases as the grain size decreases, and the number of associated grain boundaries increases. Note, however, that with smaller grain sizes, the total boundary area connecting the crystallites may become larger, which can significantly improve the carrier conduction. This may explain the increasing trend of hole mobility with the decrease of grain size.

From Fig.4.6 it can be found that the resistivity decreases rapidly with the substrate temperature, dropping from 520ºC to 475ºC but remains relatively constant at lower growth temperature even though the grain size drops further. Also from Fig.4.6, it can be seen that for the poly-GaSb film grown at 520ºC, the film thickness is smaller than the average grain size, while for the films grown at 475ºC and 430ºC, the film thicknesses are larger than the average grain size.

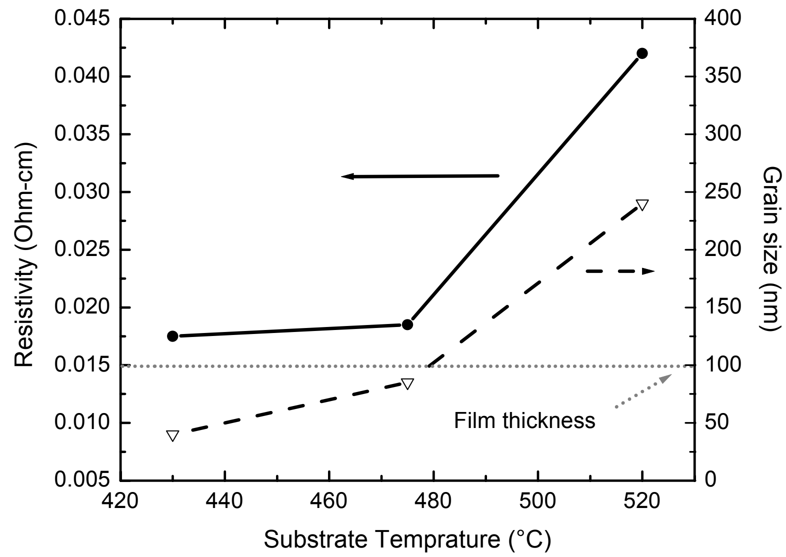


Fig.4.6 The dependence of resistivity and grain size of poly-GaSb samples on substrate temperature.

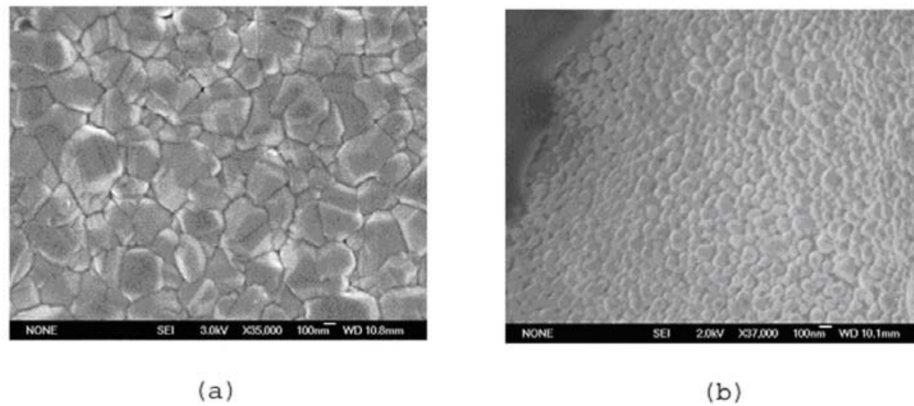


Fig.4.7 SEM images of poly-GaSb samples grown at (a) 520ºC and (b) 475ºC.

It is reasonable to assume that when the film thickness is smaller than the grain size, the grain contact areas are substantially reduced, severely limiting the conduction between polycrystalline crystallites. Under this circumstance, the resistivity of the polycrstallline film could become very sensitive to the grain size. This may explain the rapid decrease of resistivity when the growth temperature was reduced from 520 ºC to 475 ºC and the relatively constant resistivity observed at lower growth temperature.

The second set of poly-GaSb samples were grown with varying antimony to gallium beam flux ratios at a constant growth temperature of 440 ºC. Fig.4.8 shows the hole concentration and mobility of these samples as a function of the V/III ratio. The hole concentration shows a clear increasing trend for decreasing V/III ratio. This behavior can be explained by considering that carbon must displace Sb from its lattice site in order to act as an effective p-type dopant. With lower Sb beam pressure, the chance of carbon being incorporated into the Sb sublattice will be larger and the hole concentration will therefore be increased. In this set of samples it was found that the change of V/III flux ratio did not significantly affect the hole mobility. The dependence of the grain size on the V/III ratio was also weak.

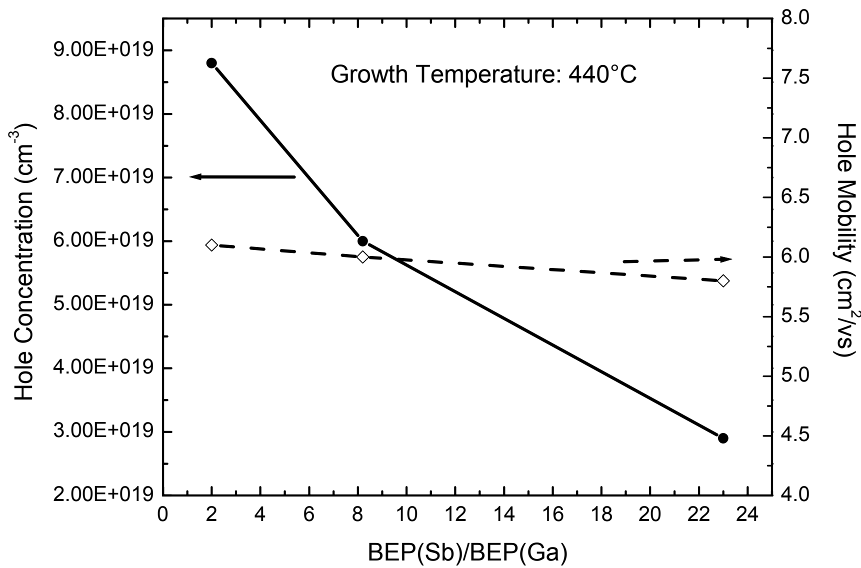


Fig.4.8 Polycrystalline GaSb hole concentration and mobility as a function of V/III beam flux ratio.

The third set of poly-GaSb samples were grown with 1000Å, 1500Å, 2000Å and 3000 Å film thicknesses, all at 440ºC growth temperature. Fig.4.9 shows the resistivity of these four samples as a function of film thickness. The hole concentration, mobility, and sheet resistivity are listed in Table 4.1. It is clear that unlike monocrystalline material, the resistivity of poly-GaSb has a strong dependence on film thickness, with thicker films having lower resistivity. Consequently, the sheet resistivity is no longer proportional to the reciprocal of the film thickness; instead it increases very rapidly with decreasing film

thickness. These results suggest that resistivity should be compared only between polycrystalline films of similar thickness.

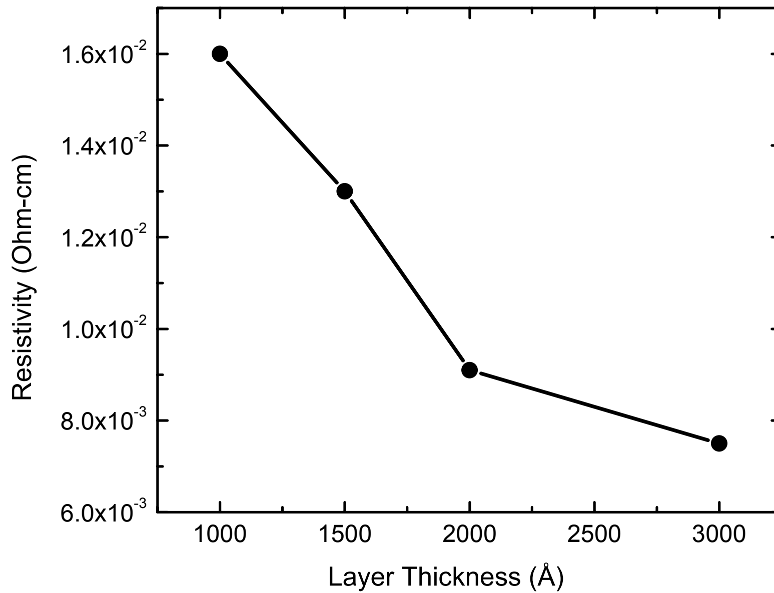


Fig.4.9 The dependence of poly-GaSb resistivity on film thickness.

Since these samples were all grown at 440 ºC and had very similar average grain sizes, it is clear from the data in Table 4.1 that the hole mobility decreases as the ratio of film thickness to grain size is decreased. This is obviously consistent with the results obtained from Fig.4.6.

Poly GaSb Thickness (Å)	Hole Density N_s (cm^{-3})	Mobility μ (cm^2/Vs)	Bulk Resistivity ρ (Ωcm)	Sheet resistivity ρ_s ($\Omega/\square$)
3000	8.2e19	10.2	7.5e-3	240
2000	8.0e19	8.6	9.1e-3	450
1500	8.1e19	5.8	1.3e-2	900
1000	7.8e19	5.1	1.6e-2	1550

Table 4.1 Electrical properties of poly-GaSb samples with different film thicknesses.

The resistivity of the 3000Å poly-GaSb film is 7.5×10^{-3} Ω-cm, over one order of magnitude lower than that of polycrystalline GaAs with the same carbon doping level in a thicker 4000Å film[3]. The properties of polycrystalline GaSb and GaAs films are listed in Table 4.2 for comparison.

	Poly-GaSb by MBE (Our work)	Poly-GaAs by GSMBE (N.Y. Li *et al*, 1998)
Carbon doping density (cm^{-3})	$8x10^{19}$	$8x10^{19}$
Grain Size (Å)	~700	400~2000
Film Thickness (Å)	3000	4000
Bulk Resistivity (Ω-cm)	$7.5x10^{-3}$	$\sim1x10^{-1}$

Table 4.2 Comparison between polycrystalline GaSb of our work and polycrystalline GaAs in reference [3].

The resistivity of poly-GaSb is expected to decrease further by using higher CBr_4 flux during growth to achieve carbon doping density above $8x10^{19}cm^{-3}$.

4.2.4 Summary

Low resistance poly-GaSb films can be achieved by MBE growth using CBr_4 doping. The resistivity of poly-GaSb has strong dependence on film's thickness and grain size, particularly when the film thickness is comparable with the grain size. It has been found that growth temperature strongly influence the

grain size, but has little effect on hole concentration. The hole concentration, on the other hand, is significantly affected by the antimony to gallium beam flux ratio, with low V/III ratios increasing the carbon incorporation. Therefore, low growth temperature and low V/III beam flux ratio are desirable to achieve low resistivity poly-GaSb films. With the same doping level ($8x10^{19}cm^{-3}$), grain size (~100nm) and similar film thickness, the resistivity of poly-GaSb is found to be more than one order of magnitude lower than that of poly-GaAs. This low resistivity is attributed to GaSb's favorable surface Fermi-level pinning position and higher hole mobility. These results suggest that poly-GaSb is a good candidate for the use as an extrinsic base material in InP HBTs.

4.3 Contact Resistivity on InAs/GaSb Interface

4.3.1 Overview

In our proposed double-poly regrowth HBTs, p-type GaSb is potentially a good candidate to be used as extrinsic base material, as previously discussed in this chapter. However, p-type polycrystalline GaSb's resistivity is still relatively high compared with n-type polycrystalline InAs, which has demonstrated a bulk resistivity of $1.4x10^{-3}\Omega$-cm for 1000 Å film and metal contact resistivity of

$1.6x10^{-7}\Omega$-cm^2.[6] These low resistivities are due to InAs's very high electron mobility and favorable surface Fermi level pinning close to the conduction band.[7] The extrinsic base's sheet resistance is therefore expected to be reduced if the majority of the extrinsic base is made of n-type polycrystalline InAs. The base contact resistance will also significantly decrease if the base contact is made on n-type polycrystalline material instead of p-type material because of electron's much smaller effective mass compared to hole's. To utilize this, however, a p-n junction will exist in the extrinsic base. It is therefore requisite to study whether an ohmic p-n interface can be formed between the n-type extrinsic and the p-type intrinsic base layers.

At the interface of semiconductor heterostructures, the energy gaps of the two constituent materials usually overlap, resulting in relatively minor band-edge discontinuities. It has been recognized that there exists systems where the conduction band edge of the former, primarily because of its unusually large electron affinity, lies below the valence band edge of the latter. The lack of overlap in this case is expected to lead to entirely different behaviors heterojunctions.

In this work, we propose to use p-type GaSb capped with n-type InAs as the extrinsic base layer. It has been widely known that InAs-GaSb heterostructure forms a broken-gap band lineup, as shown in Fig.4.10, and it is possible for the p-type GaSb's valence band electrons to transfer into the conduction band of the

neighboring n-type InAs, giving rise to a low-resistance ohmic p-n junction. The electronic properties of InAs(n)/GaSb(p) heterostructure have been studied extensively, but most studies have been focused on the negative differential resistance in this material system.[8] In this section, we examine the contact resistivity across the InAs(n)/GaSb(p) interface at relatively low current density ($<10^4$ A/cm^2) and its dependence on the doping densities on both sides of the junction. Results from n+/p+ InAs tunneling junction structure and InAs/GaSb/AlSb/GaSb tunneling heterostructure were also obtained for comparison.

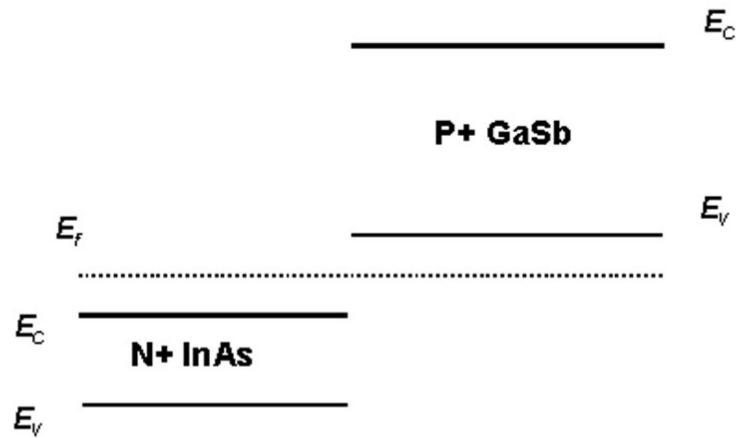


Fig.4.10 Band diagram of N-InAs/P-GaSb heterojunction.

4.3.2 Experimental Procedures

A series of test samples were grown on semi-insulating InP wafers in a Varian Gen II MBE system. The test structures consisted of a 500 Å GaAsSb layer (lattice matched to InP), a 400 Å layer grading from GaAsSb to GaSb, and a 100 Å GaSb layer. These three layers were doped with carbon. A top 1000 Å Si-doped InAs layer was then grown. This layer structure was designed for the extrinsic base of an InP HBT, therefore the total layer thickness was constrained by process design considerations. The doping densities in both the GaSb and the neighboring InAs layer were varied to investigate the dependence of the contact resistivity on the doping densities across the GaSb-InAs junction.

After growth, transmission line patterns were defined by using standard photolithography. Ti/Pt/Au contact metals were electron beam evaporated onto the samples and lifted-off. The TLM patterns had a width of 100 μm, a length of 50 μm, and gap spacings which varied from 2 to 30 μm. The spacings of the terminals were determined to an accuracy of 0.1 μm by scanning electron microscope (SEM). Mesas were defined to limit the current flow while a four-point probe arrangement was used to eliminate the effects of probe contact resistance. Mesas were chemically etched in a H_3PO_4:H_2O_2:H_20 (4:1:50) solution, which etches InAs, GaSb, and GaAsSb. Measurement of the resistance across the gaps was determined by taking the average resistance measured from two nearby devices with identical spacings. The measurements were performed

for three sets of TLM patterns across the wafer to check the sample uniformity. The specific contact resistivity between metal and n-type InAs was derived from a plot of the measured resistance versus gap spacing. After this, the top InAs cap layer was selectively chemically etched in acetic acid:H_2O:H_2O_2 (5:5:1) solution. The wet etch undercut beneath the TLM terminals was determined to be less than 0.1 μm by SEM. The resistance between each spacings was measured again and plotted against the gap spacing. This time from the least-squares straight line fit to the data, the y-axis intercept corresponds to the contact resistance between the metal and n-type InAs plus the resistance between n-type InAs and p-type GaSb. By subtracting the metal-InAs contact resistance from the total resistance, the contact resistivity between n-type InAs and p-type GaAs could be obtained. Fig.4.11 shows the schematics of the TLM measurements before and after the InAs cap layer etching.

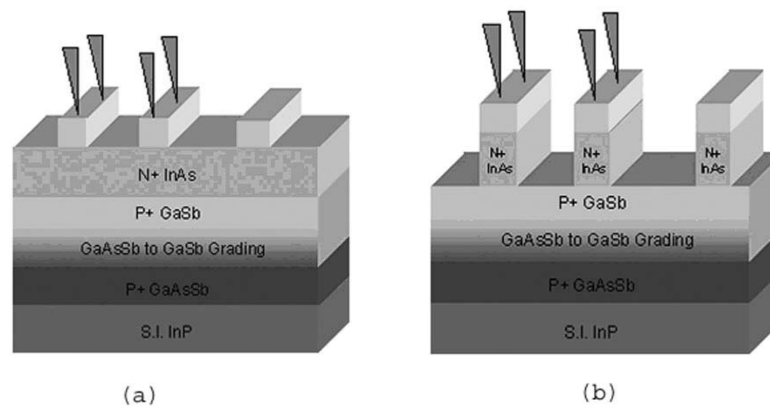


Fig.4.11 Schematics of TLM measurements (a) before and (b) after the InAs cap layer etching.

4.3.3 Results and Discussions

As expected, the contact resistivity between metal and n-type InAs was found to be extremely low and the resistance between metal and InAs is over one order of magnitude lower than the resistance between InAs and GaSb. As a result, the value of metal-InAs resistivity does not significantly affect the measurement accuracy of the contact resistivity between the InAs and GaSb layers.

A series of samples with varied n-type and p-type doping densities across the InAs-GaSb junction were tested. Fig.4.12 shows the contact resistivity at the InAs-GaSb interface as a function of the carbon-doping density in the GaSb layer, with the silicon doping density in the InAs cap layer fixed at $1x10^{17}$ cm^{-3}. The contact resistivity shows a clear decreasing trend with increasing carbon-doping density. A detailed analysis of the variation of the interfacial conducting characteristics against the carbon doping density in GaSb requires a theoretical modeling for this structure. Here, in this work, we will not attempt to analyze their interfacial conducting characteristics in detail. We only speculate that higher hole concentration in GaSb would increase the electron's probability of transmission from the conduction band of InAs to the valence band of GaSb. Fig.4.13 shows the dependence of the InAs(n)/GaSb(p) interfacial contact resistivity on the silicon doping level in the InAs layer. Two sets of samples were tested, with fixed carbon doping densities of $4x10^{19}$ cm^{-3} and $7x10^{19}$ cm^{-3}

respectively. It can be seen that the interface contact resistivity only changes by a factor of 2 when the Si doping density is varied by more than two orders of magnitude. Compared to the results shown in Fig.4.12, it is clear that the interfacial contact resistivity has a much weaker dependence on the doping density in n-type InAs than that in p-type GaSb layer. It can also be seen that the interfacial contact resistivity does not decrease monotonically with the increase of the Si doping density in the InAs layer, and this trend is very similar in both sets of samples. It is possible that when the electron density in InAs layer is near $1.0 \times 10^{19} cm^{-3}$, the Fermi level is close to a position where the maximum electron reflection coefficient for InAs(n)/GaSb(p) interface structure is reached.

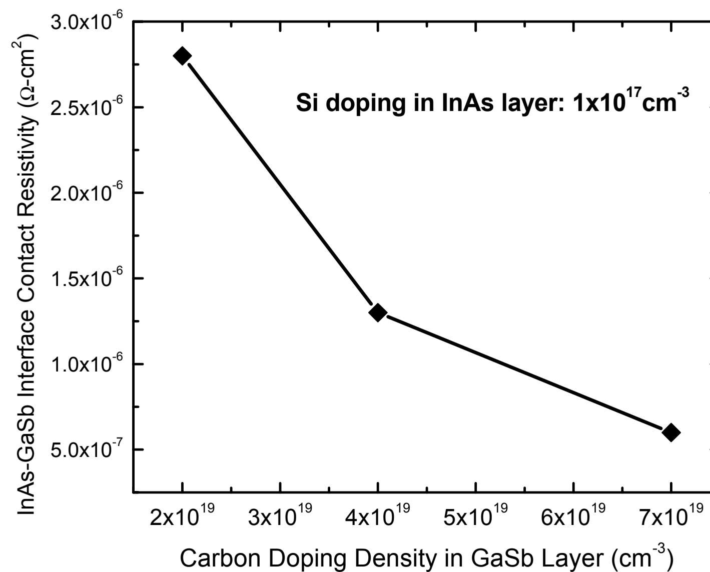


Fig.4.12 Dependence of InAs(n)/GaSb(p) interfacial contact resistivity on carbon doping density in the GaSb layer.

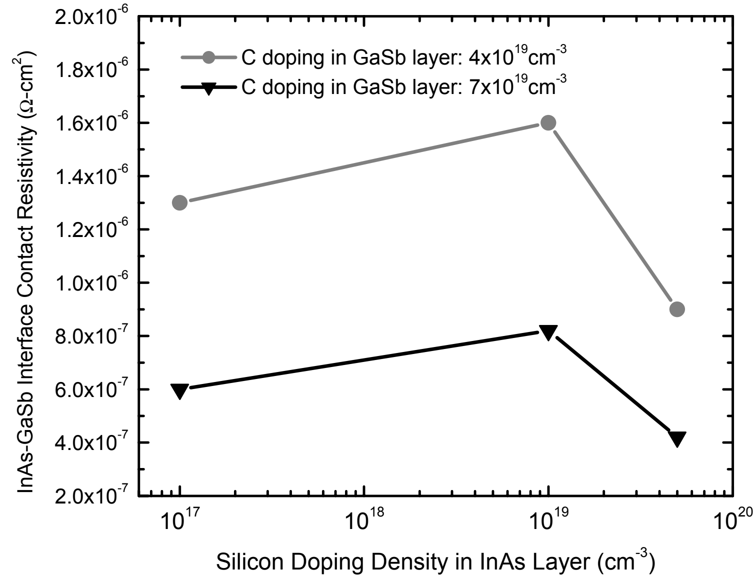


Fig.4.13 Dependence of InAs(n)/GaSb(p) interfacial contact resistivity on silicon doping density in InAs layer.

The interfacial contact resistivity values obtained in this work are listed in Table 4.3. Among these samples, the lowest InAs(n)/GaSb(p) interface contact resistivity value is $4.2x10^{-7}$ Ω-cm^2, obtained from the sample with the highest doping densities on both sides of the junction.

Doping Density of p-GaSb (cm-3)	Doping Density of n-InAs (cm-3)	Contact Resistivity (Ω-cm2)
$2x10^{19}$	$1x10^{17}$	$2.8x10^{-6}$
$2x10^{19}$	$6x10^{17}$	$3.0x10^{-6}$
$4x10^{19}$	$1x10^{17}$	$1.3x10^{-6}$
$4x10^{19}$	$1x10^{19}$	$1.6x10^{-6}$
$4x10^{19}$	$5x10^{19}$	$9.0x10^{-7}$
$7x10^{19}$	$1x10^{17}$	$6.0x10^{-7}$
$7x10^{19}$	$1x10^{19}$	$8.2x10^{-7}$
$7x10^{19}$	$5x10^{19}$	$4.2x10^{-7}$

Table 4.3 InAs(n)/GaSb(p) interfacial contact resistivities with different doping densities in the InAs and GaSb layers.

For comparison to these values, two reference samples were grown and tested. The first reference sample with a p+ (C: $7x10^{19}cm^{-3}$) InAs and n+ (Si: $1x10^{19}cm^{-3}$) InAs tunneling junction showed an interfacial contact resistivity of $1.3x10^{-5}$ Ω-cm^2 across the p-n interface, more than one order of magnitude higher than those of InAs(n)/GaSb(p) samples.

The second reference sample consisted of a thin AlSb barrier layer displaced from an InAs(n)/GaSb(p) interface. Fig.4.14 shows the band diagram of this material system. It has been reported[9] that the insertion of a AlSb layer would form a quasi-bound state in the region between the InAs-GaSb interface and the AlSb barrier, leading to resonant tunneling of carriers across the structure and therefore enhance the conduction. In our test sample the interfacial contact resistivity obtained was 5.4×10^{-7} Ω-cm^2, slightly lower than the interfacial resistivity obtained from the structure without the AlSb layer inserted (6.0×10^{-7} Ω-cm^2).

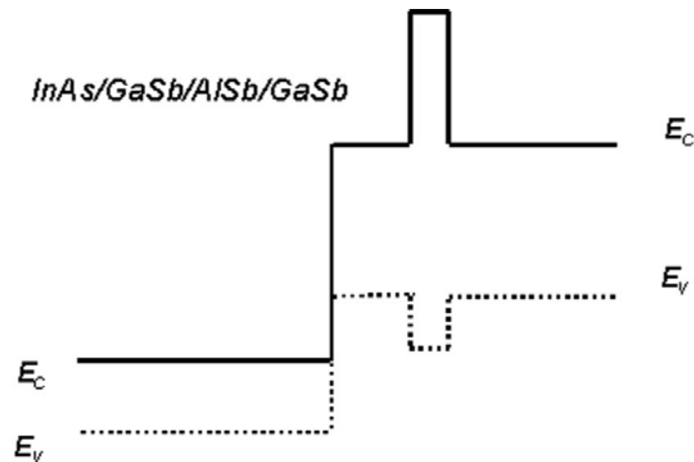


Fig.4.14 Band diagram of InAs/GaAs/AlSb/GaSb tunneling junction.

The lowest contact resistivity obtained at the InAs(n)/GaSb(p) interface, 4.2×10^{-7} Ω-cm^2, can be compared to that between metal and highly p-doped

InGaAs, where values of $1\times10^{-7}\ \Omega\text{-cm}^2$ to $1\times10^{-6}\ \Omega\text{-cm}^2$ have been obtained[10]. This suggests that with moderate reduction in the interfacial resistance and substantial reduction in sheet resistance, p-type GaSb capped with n-type InAs can be employed as extrinsic base material in InP HBTs, or in other device structures where low access resistance is required.

4.4 Summary

To combine the best features of SiGe and InP HBT technology, double-poly regrowth InP HBT is proposed with structural features and process flow as close as is possible to that of a Si/SiGe HBT, but using InP-based materials. For double-poly InP HBTs, low resistivity polycrystalline material is employed as the extrinsic base layer on buried SiO_2/Si_3N_4 surrounding a collector pedestal. To lower the total base access resistance, the choice of low resistivity III-V polycrystalline material for the extrinsic base layer is of key importance.

To find a low resistivity p-type polycrystalline material, we first investigate a promising candidate, carbon-doped GaSb, for its high carrier mobility and favorable Fermi-level pinning position on the grain surface. Our experiments show that low resistance poly-GaSb films can be achieved by MBE growth using CBr_4 doping. It is also found that the resistivity of poly-GaSb has strong dependence on film's thickness and grain size, particularly when the film

thickness is comparable with the grain size. Growth temperature strongly influence the grain size, but has little effect on hole concentration. The hole concentration, on the other hand, is significantly affected by the antimony to gallium beam flux ratio, with low V/III ratios increasing the carbon incorporation. Therefore, low growth temperature and low V/III beam flux ratio are desirable to achieve low resistivity poly-GaSb films. With the same doping level ($8 \times 10^{19} cm^{-3}$), grain size (~100nm) and similar film thickness, the resistivity of poly-GaSb is found to be more than one order of magnitude lower than that of poly-GaAs. These results suggest that poly-GaSb is an excellent candidate for the use as an extrinsic base material in InP HBTs.

In our efforts to further lower the resistivity of the polycrystalline extrinsic base layer, N-InAs/P-GaSb composite extrinsic base structure is also proposed to exploit the very low bulk and metal contact resistivity of n-type polycrystalline InAs. N-InAs/P-GaSb structure is chosen because InAs-GaSb heterostructure forms a broken-gap band lineup giving rise to an ohmic p-n junction.

We have carefully investigated the interfacial contact resistivity between n-type InAs and p-type GaSb layers, and its dependence on the doping densities on both sides of the heterostructure. An n+/p+ InAs tunneling junction structure and an InAs/GaSb/AlSb/GaSb tunneling heterostructure were also grown and tested for comparison. The lowest contact resistivity obtained at the the

InAs(n)/GaSb(p) interface is comparable to that between metal and highly p-doped InGaAs. It is therefore clear that by using N-InAs/P-GaSb composite polycrystalline extrinsic base, the extrinsic base sheet resistance can be significantly reduced, while the total base contact resistance will basically remain unchanged. Based on these results, N-InAs/P-GaSb is proposed as another strong candidate to be used as the extrinsic base in the double-poly regrowth InP HBTs.

References

[1] K. Mochizuki, T. Nakamura, T. Tanoue and H. Masuda, 'AlGaAs/GaAs HBTs with buried SiO2 in the Extrinsic Collector', Solid State Electronics, Vol. 38, pp. 1619-1622, 1995

[2] J.J.J. Yang, P.D. Dapkus, R.D. Dupuis, and R.D. Yingling, 'Electrical properties of polycrystalline GaAs films', J. of Appl. Phys., Vol. 51, No. 7, pp. 3794-3800, 1980

[3] N.Y. Li, C.W. Tu, 'Low-resistance polycrystalline GaAs grown by gas-source molecular beam epitaxy using CBr4', Journal of Crystal Growth, Vol. 188, No.1-4, pp. 45-49, 1998

[4] J.Y.W. Seto, 'The electrical properties of polycrystalline silicon films', Journal of Appl. Phys., Vol. 12, No.12, pp. 5247-54

[5] W.E. Spicer, P.W. Chye, P.R. Skeath, C.Y. Su, I. Lindau, 'New and unified model for Schottky barrier and III-V insulator interface states formation', J. Vac. Sci. and Technol, Vol. 16, No. 5, 1422-1433, 1979

[6] D. Scott, M. Urteaga, N. Parthasarathy, and M.J.W. Rodwell, "Molecular Beam Deposition of Low-Resistance Polycrystalline InAs." Lester Eastman Conference, University of Delaware, August 6-8, 2002

[7] C. Nguyen, B. Brar, H. Kroemer, 'Surface-layer modulation of electron concentrations in InAs-AlSb quantum wells', J. Vac. Sci. and Technol., Vol.11, No. 4, pp.1706-1709, 1993

[8] D.A. Collins, E.T. Yu, Y. Rajakarunanayake, J.R. Soderstrom, D.Z.-Y. Ting, D.H. Chow, and T.C. McGill, 'Experimental observation of negative differential resistance from an InAs/GaSb interface', Aool. Phys. Lett, Vol. 57, No. 7, pp. 683-685, 1990

[9] D.Z.-Y. Ting, D.A. Collins, E.Y. Tu, D.H. Chow, and T.C. McGill, 'Large peak current densities in novel resonant interband tunneling heterostructures', Appl. Phys. Lett. Vol. 57, No. 12, pp.1257-1259, 1990

[10] J.S. Yu, S.H. Kim, T.I. Kim, 'PtTiPtAu and PdTiPtAu Ohmic Contacts to p-InGaAs', Proceedings of the IEEE Twenty-Fourth International Symposium on Compound Semiconductors. IEEE. pp.175-178, 1998

Chapter 5
Conclusion

5.1 Achievements

This dissertation presents several novel regrowth technologies and process techniques toward reducing base-collector parasitic capacitance and base resistance.

To realize the InP HBT with extrinsic base laterally overgrown on buried SiO_2 for the simultaneous reduction of base-collector capacitance and base resistance, we have investigated the selective growth of InP through narrow mask openings by MOCVD. The lateral overgrowth of InP on SiO_2 is found to be strongly dependent on both the opening width and orientation. The lateral overgrowth length reached its maximum at 60° off the [011] direction, and reached minima along the major low index directions. The lateral overgrowth also showed increasing overgrowth length for decreasing opening width. Based on these results, HBTs employing extrinsic base laterally overgrown on buried SiO_2 were fabricated. Emitters were aligned 60° off the [011] direction to obtain the maximum lateral overgrowth length for the extrinsic base. The regrown-base HBTs exhibit acceptable DC performance with current gain of approximately15.

Lower base recombination current and higher current gain can be expected after additional efforts are made to improve the selective growth quality as well as minimize the process related damage and contamination. RF measurements demonstrate ~60% base-collector capacitance reduction compared with conventional HBTs with the same layer structure and device layout. F_{max} of regrown base HBTs is lower than expected due to the high base contact resistance caused by the low Zn doping density in the extrinsic base, even though the extrinsic base sheet resistance is indeed reduced through regrowth.

To reduce excess base-collector capacitance, we also propose and fabricate an InP HBT with a collector pedestal. The pedestal, formed by using selective ion implantation and regrowth by molecular beam epitaxy, permits a larger collector depletion thickness under the base contacts than the collector depletion thickness directly under the emitter. Various issues associated with fabrication of the collector pedestal HBT, such as silicon implantation, MBE regrowth quality, regrowth interfacial charge accumulation, and device design as related to high frequency performance, have been investigated. The pedestal HBTs showed excellent DC characteristics including extremely low I_{cbo}, and low junction ideality factors, indicating that high junction quality could be obtained in a collector pedestal process incorporating MBE regrowth. The HBTs exhibited a 1.6:1 reduction in C_{cb} and a 1.3:1 increase in common-emitter breakdown voltage $V_{br,ceo}$ over devices of the same T_c but without the pedestal. The

measured peak f_τ and $f_{\max}$ are low due to very high emitter and base resistances caused by an error in processing which left a thin layer of polymer on the emitter and base metal before deposition of the interconnect metals. The present samples nevertheless show clearly key expected pedestal HBT characteristics, including reduced C_{cb}, increased $V_{br,ceo}$, and low I_{cbo}. With emitter and base contacts of normal quality and with further scaling, it is feasible to realize transistors with f_τ and $f_{\max}$ exceeding 500 GHz, and $V_{br,ceo}$ exceeding 5 Volts.

To combine the best features of SiGe and InP HBT technology, double-poly regrowth InP HBT is proposed with structural features and process flow as close as is possible to that of a Si/SiGe HBT, but using InP-based materials. To find a low resistivity p-type polycrystalline material for the regrown extrinsic base, a promising candidate, carbon-doped GaSb, is studied for its high carrier mobility and favorable Fermi-level pinning position on the grain surface. MBE growth conditions and electrical properties of carbon-doped polycrystalline GaSb are thoroughly investigated. With the same doping level (8×10^{19} cm^{-3}), grain size (~100 nm) and similar film thickness, the resistivity of poly-GaSb is found to be more than one order of magnitude lower than that of poly-GaAs. These results suggest that poly-GaSb is an excellent candidate for the use as an extrinsic base material in InP HBTs. In our efforts to further lower the resistivity of the polycrystalline extrinsic base layer, an N-InAs/P-GaSb composite extrinsic base structure is proposed to exploit the very low bulk and metal contact resistivity of

n-type polycrystalline InAs. The interfacial contact resistivity between n-type InAs and p-type GaSb layers has been carefully investigated and many interesting results are obtained.

5.2 Future Work

5.2.1 Lateral Overgrowth of Extrinsic Base

Though a great deal of work has gone into the fabrication of the InP HBT with laterally overgrown extrinsic base, this work simply represents a foundation for future work oriented towards optimization of the transistors for high frequency operation.

As discussed in Chapter 2, the relatively low p-type doping level in the extrinsic base, caused by the low maximum p-level attainable with MOCVD when using Zn as acceptor dopant, induces the high base contact resistivity and significantly limits the HBT's high frequency performance, especially f_{max}. To obtain higher p-doping in the extrinsic base near the surface, post-growth Zn diffusion has been proposed and more experiments are needed. This difficulty could also be alleviated in a MOCVD system with higher susceptor rotational speed and carbon doping source. In that case, carbon doped InGaAs could be used as the

extrinsic base material while good growth selectivity could still be obtained. Much lower extrinsic base sheet and contact resistances could be expected if this could be realized.

Although MOCVD is a feasible and powerful growth technique to selectively grow heterostructure in masked areas on GaAs and InP substrates, it still has significant limitations. MOCVD generally operates with gas phase supersaturation far from equilibrium, which leads to the ready nucleation of materials on both the masked and unmasked regions, diminishing the selectivity of this process when using the commonly used growth precursors. Compared with MOCVD selective growth, better results could be obtained by using low pressure hydride vapor phase epitaxy (LP-HVPE) to conduct extrinsic base lateral overgrowth.

To improve the device's high frequency performance, further scaling of the transistor is necessary. Although yield could still be a problem, traditional mesa-structured HBTs can have base contact width less than 0.5μm by using self-aligned lift-off process. With the adoption of recently introduced self-aligned sidewall spacer process[1], the base contact width could be further reduced. To compete with these HBT fabrication techniques, our extrinsic base's regrowth window width needs to be reduced accordingly. Experiments on the lateral overgrowth behaviors through ultra-narrow mask openings (<0.5μm) are

necessary. More accurate and reliable fabrication techniques also need to be developed for this ultra-narrow base regrowth process.

5.2.2 Collector Pedestal HBTs

In collector pedestal HBT fabrication process, the regrowth interfacial charge accumulation still requires further investigation. Successful charge compensation has been achieved by using compensating p-type δ-doping on the regrowth interface. However, the amount of interfacial charge may change in a different MBE growth system, which could make it difficult to have fast technology transfer to a new fabrication environment for wider application.

The origin of this regrowth interfacial charge is still not completely clear. More regrowth experiments and SIMS analysis need to be conducted to study how much of this charge accumulation is caused by dangling bonds on the regrowth surface, and how much is caused by the surface contaminants. It would also be necessary to investigate the possibility of passivating the dangling bonds before conducting the MBE regrowth.

In Si/SiGe bipolar transistor fabrication process, the pedestal collector is formed by implanting through the base layer to the collector layer and using the base contact as the self-aligned implant mask. In our HBT fabrication process, this technique is not readily applied because the implant profiles' negative skewness

would cause a high doping density in the collector layer, which would prevent the collector layer's full depletion. Fig.5.1 shows the simulation results of the implant through the base layer. It can be found that when the density of the Si dopants in the pedestal layer is $1x10^{18}cm^{-3}$, the collector doping density will reach ~$3x10^{17}cm^{-3}$. This is too high for a 1000 Å InP collector layer.

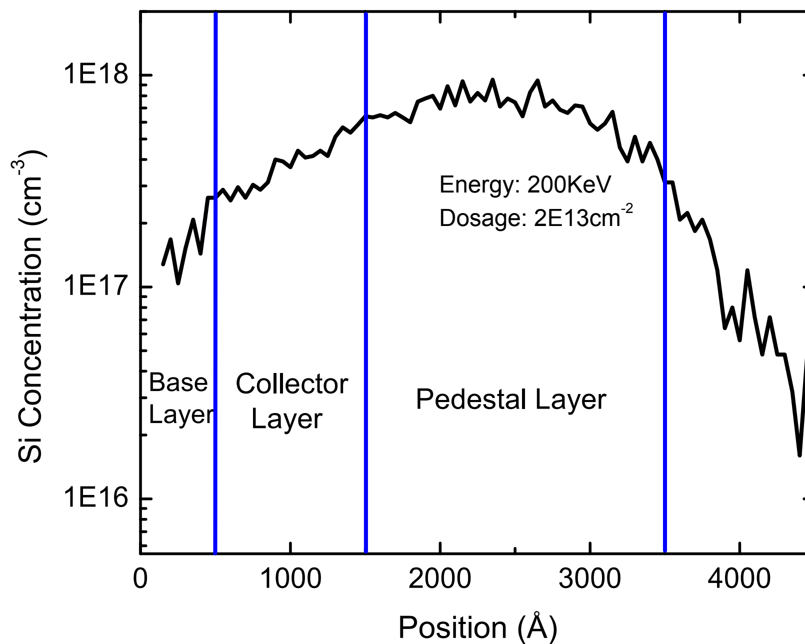


Fig.5.1 TRIM simulation of an N+ implant pedestal through base layer.

However, with further scaling of the device, the required collector doping density will increase rapidly with reduced collector thickness. When the collector thickness is 750Å, the desired collector doping density will be as high

as $\sim 3x10^{17}$ cm^{-3}. Clearly with this collector thickness, it is feasible to implant through the base to form the collector pedestal. In this case, the pedestal template will contain pedestal, collector, as well as base layer, and only emitter layer needs to be regrown after the selective implantation. As a result there would be no regrowth interface in the base-collector junction and this avoids accumulated sheet charge between the collector and pedestal layers.

Further, if the collector pedestal is implanted through the base, the fabrication and regrowth processes will be easy to integrate with the double-poly regrowth process for the realization of SiGe-like InP HBTs, as illustrated in Fig.5.2.

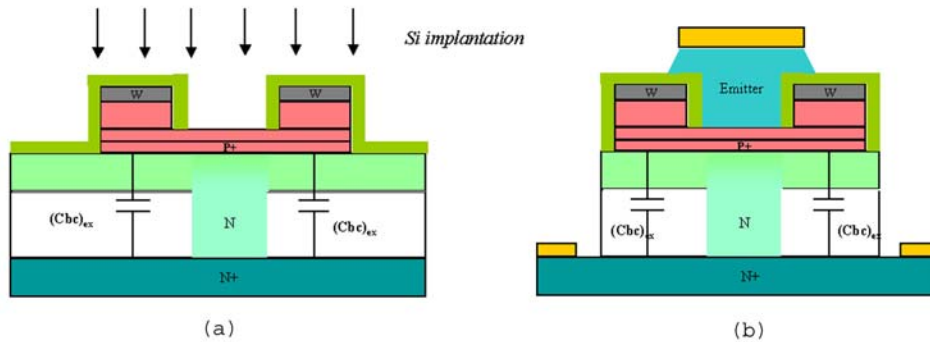


Fig.5.2 Schematics of (a) selective implantation through base layer, and (b) HBT structure after emitter regrowth.

5.2.3 Double-Poly Regrowth Process

The double-poly regrowth process is still far from mature. Although polycrystalline GaSb has shown great potential as low resistivity extrinsic base

material, its sheet resistivity is relatively high if a thin extrinsic base layer is used. More experiments are necessary to investigate the possibility of further increasing the carbon doping level in poly-GaSb.

InSb has similar surface Fermi-level pinning position and even narrower band gap than GaSb. In theory poly-InSb can provide lower resistivity than poly-GaSb. One important factor potentially prohibiting the use of poly-InSb is its low melting temperature (~520°). During the emitter regrowth the temperature is likely to exceed 520°C and this could cause serious problem if poly-InSb is used as the extrinsic base material. However, the melting temperature of polycrystalline material could be different from the single crystal material, and also the emitter regrowth temperature could be decreased and carefully monitored to alleviate this problem. For these two reasons, the possibility of using poly-InSb and poly-InGaSb should still be carefully examined.

The emitter regrowth process has not been covered by this work. During the process development, it has been found that one major difficulty for the emitter regrowth is caused by strongly facet-dependent growth. As shown in

Fig.5.3, the regrown deposit inside the emitter regrowth window is bounded by {111}B planes and it is difficult to connect it with the polycrystalline emitter material deposited on the SiN mask. This broken link very likely is the cause of the high observed emitter resistance.

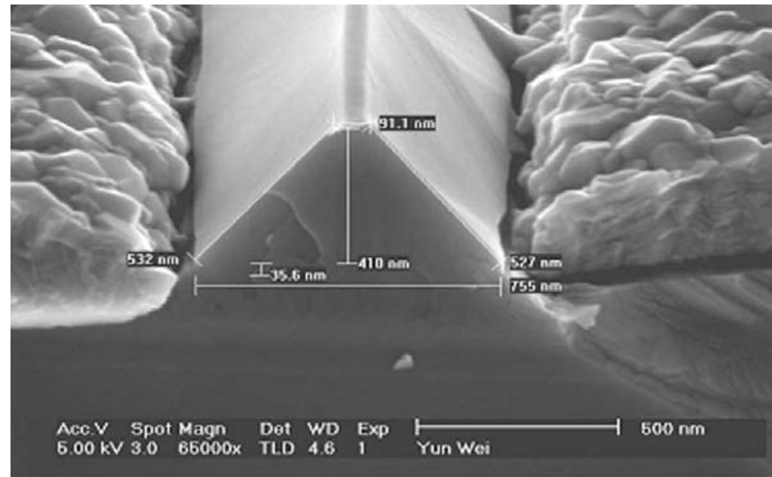


Fig.5.3 SEM cross-section image of the emitter regrowth through opening along [011] direction.

This growth phenomenon is very similar to that observed in the InP overgrowth experiments by MOCVD, which has been described in Chapter 2. There we have found that the lateral overgrowth length and growth boundary planes are strongly dependent on the opening orientation. Based on these results, initial experiments have been carried out by Dennis Scott and Yun Wei to study the emitter regrowth behaviors through openings 30° and 60° away from the [011] direction.

Fig.5.4 shows the top view of the sample after emitter regrowth with opening aligned 60° off [011] direction. Compared with the regrowth through emitter

openings along the traditional [011] direction, the connection between the deposit inside the opening and the polycrystalline emitter on the SiN mask has been significantly improved. Encouraging emitter resistance results have been obtained, and more systematic investigations are underway.

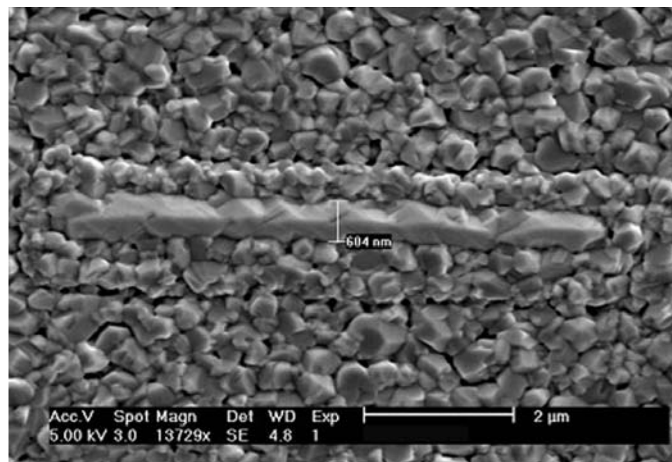


Fig.5.4 SEM top view of the sample after emitter regrowth with opening aligned 60° off [011] direction.

References

[1] M. Urteaga, P. Rowell, R. Pierson, B. Bra, M. Dahlstrom, Z. Griffith, M.J.W. Rodwell, S. Lee, N. Nguyen, and C. Nguyen, 'Deep Submicron InP DHBT Technology with Electroplated Emitter and Base Contacts', 62nd Device Research Conference, Notre Dame, IN, 2004.