Millimeter-wave CMOS and InP front-end ICs for optical and wireless high data-rate communication

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Research Thesis

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Abstract

In the past decades the world network traffic has grown exponentially with a rate of 60%/year. As a result, an extensive research has been devoted to the improvement of the efficiency and the capacity of both optical and wireless communication channels.

Since 2008, optical coherent detection has started to gain a renewed interest mainly due to its potential to boost the spectral-efficiency when a full vector optical filed is detected. A significant progress in photonic integration, together with a constant growth in speed of integrated electronics have managed to decrease the loop delay of optical phase-lock-loops, resulting in sufficient phase-locking bandwidth relative to the local oscillator laser linewidth. Such optical phase-locked-loops based homodyne receivers pave the way to a coherent, high-speed, digital-signal-processing free short distance communication. The effort of this research is targeted to develop and design fast InP integrated circuits for optical phase locking. A Costas phase frequency detector featuring lasers detuning pull-in range of $\pm 50\,GHz$ was designed, manufactured and successfully tested. A work on homodyne BPSK and $100\,GBaud/s$ QPSK receivers based on such Costas phase frequency detectors with two and four stable states, accordingly is also reported. A novel, fully digital, single-sideband mixer for offset locking is also introduced.

In the field of wireless communication, data rates of $10-20\,Gb/s$ can potentially be transmitted using $120\,GHz$ band wireless links; a frequency region currently not used by industrial, scientific and medical applications, with a relatively small atmospheric absorption of about $1\,dB/km$. While most of the reported $120\,GHz$ TX's employ ASK modulations, in order to increase the data-

rate and spectrum efficiency, quadrature coherent modulations must be used. The TX reported in this research utilizes a two mixing-steps scheme. The first stage is a high gain $40\,GHz$ I/Q mixer based on a Weaver topology, while the second mixing stage upconverts to $120\,GHz$ using a $80\,GHz$ LO, using the more available power levels at $80\,GHz$, compared with $120\,GHz$. The quadrature phases are generated using injection-locked frequency dividers at $40\,GHz$ that use the same $80\,GHz$ LO. This way, the design achieves a record data rate of $20.6\,Gb/s$, wide frequency tuning range of $101-118\,GHz$ and compact area of just $0.21\,mm^2$.

List of Abbreviations

AGC	Automatic Gain Control
AOM	Acousto-Optic Modulator
ASK	Amplitude Shift Keying
BER	Bit Error Rate
BERT	Bit Error Rate Test
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CAD	Computer Aided Design
CCO	Current Controlled Oscillator
CHA	Cherry-Hooper Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DBR	Distributed Bragg Reflector
DC	Direct Current
DSP	Digital Signal Processing
ECL	Emitter Coupled Logic
ECL	External Cavity Laser
EDFA	Erbium Doped Fiber Amplifier
EIC	Electrical Integrated Circuit
EM	Electromagnetic
ESA	Electrical Spectrum Analyer

EVM	Error Vector Magnitude
FD	Frequency Detection
GCM	Gilbert Cell Mixer
GSG	Ground Signal Ground
GSSG	Ground Signal Signal Ground
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
IL	Insertion Loss
ILFD	Injection Locked Frequency Divider
IM-DD	Intensity Modulation Direct Detection
InP	Induim Phosphide
LF	Loop Filter
LIDAR	Light Radar
LO	Local Oscillator
MZM	Mach-Zehnder Modulater
OPLL	Optical Phase Locked Loop
OSNR	Optical Signal to Noise Ratio
PA	Power Amplifier
PC	Polarization Controller
PD	Phase Detection
PFD	Phase Frequency Detector

PIC	Photonic Integrated Circuit
PLL	Phase Locked Loop
PM	Phase Margins
PRBS	Pseudo Random Bit Sequence
QPSK	Quadrature Phase Shift Keying
RBW	Resolution Bandwidth
RF	Radio Frequency
RFA	Resistive Feedback Amplifier
RFIC	Radio Frequency Integrated Circuit
SG-DBR	Sample Grating Distributed Bragg Reflector
SiGe	Silicon Germanium
SRF	Self Resonance Frequency
SSB	Single Side-Band
TIA	Transimpedance Amplifier
TX	Transmitter
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VOA	Variable Optical Attenuator
VSA	Vector Signal Analysis
WDM	Wavelength Division Multiplexing
XOR	Exclusive OR

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1. Introduction

1.1 Optical Coherent Communication

The ever growing data volumes transmitted through the optical fiber communication systems demand more and more efficient transmission techniques. The $20\ dB$ sensitivity improvement at the $1.5 - 1.6\ \mu m$ wavelength region and the ability to work near the shot-noise limit [1] makes the coherent optical communication preferable over the IM-DD systems. Comparing to heterodyne methods, where the signal is optically down-converted to an intermediate frequency and further processed by electrical phase-locked loops or by digital signal processors for phase and frequency estimation and recovery, with homodyne receivers the information is down-converted directly to the baseband by optical means alone, thus can support at least twice higher data-rates for the same receiver bandwidth while greatly improve the receiver sensitivity. Similar to a microwave communication, optical homodyne detection requires optical phase-locked loops (OPLL) to control over the local-oscillator laser phase.

The advantages of coherent optical signaling are increasingly being recognized for a range of applications. Wavelength Division Multiplexing (WDM) fiber communications benefits from improved spectral density, leading to higher transmission capacity in existing wavelength channels. To date, these benefits

are only partially realized, mainly through the development of coherent systems accommodating incoherent sources, e.g. using DSP to compensate for laser incoherence. The importance of optical coherent communication and optical frequency synthesis can be fully grasped when compared to the impact of the radio frequency synthesis and RF coherent communication on today's world as we know it. Since the first demonstration of OPLL [2], this technique was used for a wide range of application such as LIDAR [3, 4], laser linewidth narrowing and cloning [5], coherent receivers [6] and millimeter wave generation [4].

OPLLs presented in this study are based on the ability of the integrated photonic circuits to recover both the in-phase and the quadrature-phase components of the reference and local oscillator lasers beat-note. Using this information, the phase-frequency detector can recover both the frequency offset magnitude and sign, which makes it possible to lock two lasers having initial frequency offset as large as fast electronics can detect ($\sim 100\ GHz$), much higher than a typical loop bandwidth. In addition, using highly integrated photonic and electronic circuits loop delays as low as $\sim 100 - 200\ ps$ are feasible. Due to such short loop-delays it is possible to reach loop bandwidth large enough ($100\ MHz$ - $1\ GHz$) for locking high linewidth semiconductor lasers.

The main effort of this research was targeted to develop and design fast ICs for optical phase-locking for communication and wavelength synthesis applications. Three main IC topologies were designed and tested:

1. A $40\ Gbps$ coherent homodyne BPSK receiver based on Costas phase-frequency detector featuring lasers detuning pull-in range of $\pm\ 50\ GHz$ and two stable phase detection states. The fully digital design makes the system insensitive to the input photocurrents. A complete front-end BPSK receiver system was successfully assembled and tested.

2. A novel, fully digital single side-band mixer for offset locking. Such single side band mixer can be used for WDM dense comb generation, mm-wave synthesis, LIDARs and similar application. The digital single side-band mixer was also tested as a part of an OPLL system.
3. A $100\,GBps$ QPSK linear receiver based Costas phase-frequency detectors with lasers detuning pull-in range of $\pm 50\,GHz$ and four phase-detection stable states.

1.2 CMOS F-Band Wireless Communication

The use of wireless communication systems has significantly grown in the last decades. Most of today wireless standards operate at carrier frequencies of a few GHz, limiting the maximum data bandwidths to several tens of megahertz. The ever-growing demand for data bandwidth constantly leads to higher frequency carrier utilization. Some of the novel $60\,GHz$ wireless standards with $3.5 - 4\,Gb/s$ bandwidth (e.g. IEEE802.15.c) have been already embedded into commercial systems.

Data rates of $10 - 20\,Gb/s$ can potentially be transmitted using $120\,GHz$ band wireless links; a frequency region currently used by industrial, scientific and medical applications, with a relatively small atmospheric absorption of about $1\,dB/km$ [7]. Link implementations using a SiGe and an InP HEMT technologies have been reported [7, 8]. With CMOS technologies demonstrating device cut-off frequencies of $200 - 300\,GHz$, $120\,GHz$ CMOS links seem feasible [9, 10]. Additionally, the possibility to integrate the RF circuits with digital

signal processors on a single chip greatly reduces the system cost, making CMOS a natural choice for this application.

While most of the reported $120\,GHz$ TX's employ ASK modulations (Table 1), in order to increase the data-rate and spectrum efficiency, quadrature coherent modulations must be used. One of the main challenges in designing a quadrature modulation transmitter at $120\,GHz$ is achieving accurate quadrature phase generation and a wide tuning range. Recently reported quadrature transmitters, [7, 10], perform a one-step upconversion while the quadrature phases are generated using $90°$ hybrids or transmission line couplers.

	[11]	[9]	[10]	Current Work
Technology	130 nm	40 nm	65 nm LP	65 nm
Carrier Frequency (GHz)	135	135	116	100-118
Data Rate (Gb/s)	10	10	10	20.6
Modulation	ASK	ASK	BPSK/ QPSK/ 8QAM	BPSK/ QPSK
Output Power (dBm)	-5	-9	-5	-3
Chip Area (mm^2)	0.21	0.35	1.5	0.21*
DC Power (mW)	N/A	17.9	200	280

* IC core area.

Table 1: Comparison with State-of-the-art F-band/D-band CMOS TX

Upconversion CMOS mixers at range of $120\,GHz$ typically suffer from high conversion loss while $120\,GHz$ quadrature generation using transmission lines methods is sensitive to length mismatches, has high loss, high area consumption and practically no frequency tuning range. To overcome the lines loss and mixer conversion-loss, additional buffers and power amplifiers must be introduced, resulting in additional area and power consumption. In addition, multi-stage amplifier chains will narrow the bandwidth, leading to a potential

decrease in the maximum supported data-rate.

The proposed research tackles this obstacle by using two mixing steps. The first stage is a high gain $40\,GHz$ I/Q mixer based on a Weaver topology, while the second mixing stage upconverts to $120\,GHz$ using a $80\,GHz$ LO, using the more available power levels on $80\,GHz$ compared with $120\,GHz$. The quadrature phases are generated using injection locked frequency dividers (ILFD) at $40\,GHz$ that use the same $80\,GHz$ LO. The design achieves a record data rate of $20.6\,Gb/s$, wide frequency range of $101-118\,GHz$ and compact area of just $0.21\,mm^2$.

2. Optical Phase-Locked Loops

2.1 Challenges

Unlike RF Phase-Locked Loops (PLL), where the reference oscillator is spectrally pure and the reference frequency is comparable with the loop bandwidth, in an OPLL, the tunable laser linewidth is in the tens or hundreds of MHz range while the input signal frequency is about six orders of magnitude larger than the loop bandwidth (about $193\,THz$ for $1550\,nm$ wavelength).

This vast ratio of oscillator frequency to loop bandwidth has profound impact upon the range of wavelengths over which OPLL will acquire lock, and impairs greatly the rate both at which the OPLL can scan its frequency and its absolute frequency tuning range. The wide ($\sim 200\,GHz$) frequency tuning range of semiconductor lasers, of great value in tunable sources, imposes the demand for very wide bandwidth electronics. The initial frequency offset between reference and controlled lasers may exceed $200\,GHz$, approaching the range of operation of electronic amplifiers and far beyond the control bandwidth of feedback loops. Given normal laser wavelength tolerances, it will take milliseconds for an OPLL to acquire lock. Moreover, to acquire lock, the beat note between lasers must fall within the PLL loop bandwidth, f_{PLL}. PLLs thus have a maximum locking range of $\Delta f_{lock} \sim 3 f_{PLL}$, [12], and further take a time $T_{lock} \sim 1/2\pi f_{PLL}$ to lock once the reference and controlled laser are brought

within range. Hunt-and-search locking methods are further slowed by the response time of control electronics, and can take 100's of ms. This limits useful OPLL applications. Attempts to increase the locking range by dividing the beat note frequency using a frequency divider have two main drawbacks: an increase in a loop delay due to an introduction of a divider into a loop, and a disability of the divider to operate in an absence of a beat note, when the loop is locked.

Without photonic integration, the situation is far worse. A bulk, or fiber, optic OPLL would increase the system complexity by introducing far larger loop delay, τ. For an absolute loop stability of an OPLL, the loop natural frequency ω_n and the loop delay τ must satisfy the relation of $\omega_n \cdot \tau < 0.736$ [13]. Recent state-of-art OPLLs typically need sufficiently low linewidth lasers (KHz range) to accommodate a slow phase-locked loop [14]. Such low linewidth lasers are typically expensive and unsuited for volume production or optical integration. Early works have tried to use wide linewidth semiconductor lasers with very compact bulk optics to achieve small loop latencies [15, 16]. To achieve $> 100\,MHz$ loop bandwidth, a loop delay of $\tau < 1.2\,ns$ is required. By using bulk optics and discrete components electronics such performance is nearly impossible [17].

2.2 Basic Structure

In its most simple form, the OPLL can be represented by the schematic in Fig. 1. The operation is similar to any PLL, the input optical reference is photo-mixed with the local oscillator (LO) laser output and the resulting

photocurrent produces an error signal to be filtered and fed-back to frequency-tune the LO-laser. An efficient LO laser can have $\sim 10\, GHz/mA$ frequency tuning sensitivity at low frequencies, dropping down to $< 1\, GHz/mA$ at $1\, GHz$ [18].

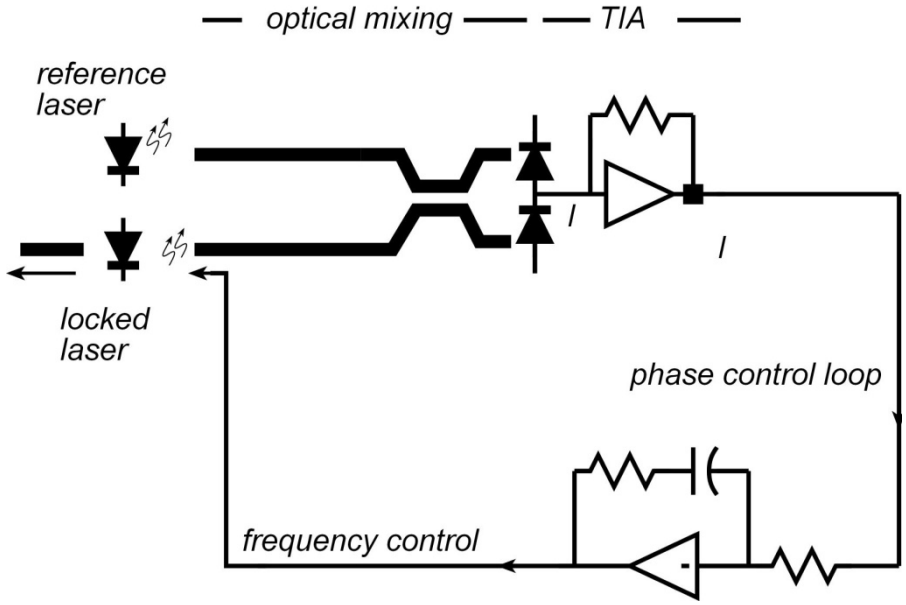


Fig. 1: Basic OPLL configurations as might be used to lock transmitter or receiver LO lasers.

For a reference laser frequency f_R and a slave laser frequency f_L, the photodiodes output current, given by Eq. 1, is proportional to $\cos(\Delta\theta(t))$. Here E_R, θ_R, and f_R are the electric field amplitude, phase, and frequency of the reference laser, while E_L, θ_L, and f_L are those of the locked laser, and $\Delta\theta(t) = 2\pi\Delta f t + \Delta\theta_0$ where $\Delta f = f_R - f_L$ and $\Delta\theta_0 = \theta_R - \theta_L$.

$$I_{PD} \propto \left|E_R e^{j(2\pi f_R t + \theta_R)} + E_L e^{j(2\pi f_L t + \theta_L)}\right|^2 = |E_R|^2 + |E_L|^2 + 2|E_R||E_L|\cos(\Delta\theta(t)) \quad \textit{Eq. 1}$$

$$K_{PD} = I_{PD} = 2|E_R||E_L|\cos(\Delta\theta(t)) \xrightarrow{\Delta\theta \ll 1} 2|E_R||E_L| \quad \textit{Eq. 2}$$

Since $\cos(\Delta\theta(t)) = \cos(-\Delta\theta(t))$ the frequency offset sign cannot be extracted unambiguously, hence measurement or control of the sign of the frequency offset is not possible. In addition, such loop topology imposes phase detection gain, K_{PD}, directly proportional to the product of reference and LO laser field intensities (Eq. 2). This makes the PLL open loop gain and hence bandwidth dependent upon optical intensity, potentially subjecting the loop to instability for varying component parameters or operating conditions.

2.3 Innovation

A PLL will not by itself acquire lock if the initial reference-slave lasers offset frequency exceeds the required final offset frequency by ~3 times the PLL loop bandwidth f_{PLL} [12]. At $\lambda = 1550\,nm$, $\pm 0.02\%$ wavelength detuning corresponds to a $\pm 39\,GHz$ offset frequency, much larger than the $\sim 1\,GHz$ f_{PLL}, feasible given typical laser tuning characteristic [19] and minimum delays, achievable by a discrete loop. Hence, in order to obtain initial lock the lasers should be manually brought into the locking range, and if the lock is lost it will not be automatically obtained again.

If OPLLs are to be scanned in frequency, both the magnitude and sign of an optical frequency difference must be measured. Normal optical interferometry cannot do this. Hence, innovations in loop design, supporting Photonic Integrated Circuit (PIC) and electronics are required.

The novel technique (Fig. 2) dramatically improves PLL lock times and scan rates. By using an optical 90-hybrid [20], both the in-phase and quadrature-phase components of the optical field are measured. Loop can be designed to

measure the initial loop frequency detuning using a phase-frequency difference detector [21, 22], and the initial lasers detuning then can be made as large as that of available photodetectors and ICs, about $\pm\,100\,GHz$. The time to acquire frequency lock is set by the loop bandwidth operating in frequency-control mode; this is $f_{loop,FLL} = \pi f_{PLL}^2/\Delta f_{lock}$ [21], about $100\,MHz$ for a $2\,GHz$ OPLL loop bandwidth and a $\pm 100\,GHz$ frequency acquisition range; the loop will then acquire lock in $1/2\pi f_{loop,FLL} = 1.3\,ns$.

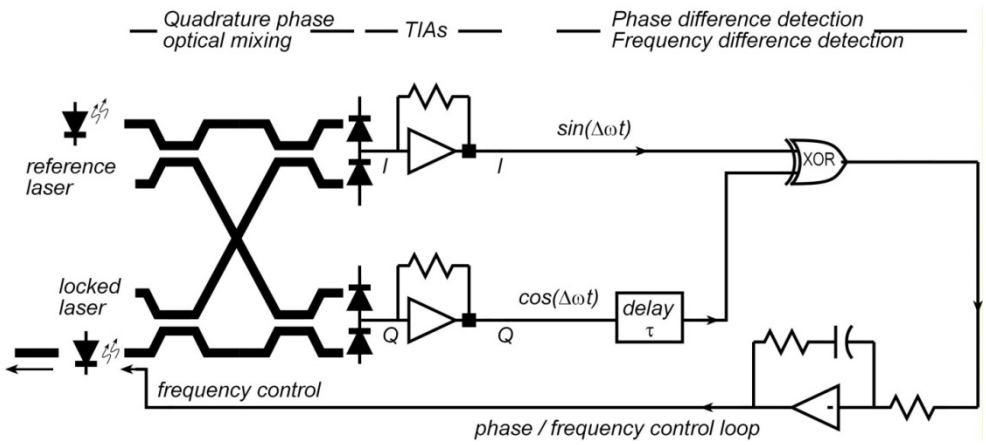


Fig. 2: OPLL with quadrature optical mixing.

Measurement of both in-phase and quadrature-phase components of the optical field is also necessary for optical frequency synthesis and for single side-band locking. With I/Q detection, an optical/electrical Weaver single-sideband frequency converter is realized [23], and the OPLL will uniquely force the slave laser to a frequency offset $\Delta\omega$; if only one of the two optical heterodyne components is measured, the OPLL mixing is double-sideband, and the loop will lock at offsets of $+\Delta\omega$ or $-\Delta\omega$.

When measuring both of the quadrature phases of the lasers offset beat-note, the phase detection characteristics yields two stable states, enabling to lock on a BPSK modulated reference laser and recover the data, as will explained in

section 4 and 6.

Most of the ICs presented in this study operate in digital mode. By digitizing the input I/Q photocurrents, one removes the dependency on the local and reference lasers optical signal power, thus not only making the design simpler and more robust, but also keeping the loop gain constants (K_{PD}, etc.) constant, thus maintaining the same loop dynamics and preserving the loop stability.

3. High Frequency InP Mixed Signal Design

3.1 InP Heterojunction Bipolar Transistor Technology

To design large scale integrated high speed ICs, indium phosphide/ indium gallium arsenide (InP/InGaAs) material system was used. The HBT (Heterojunction Bipolar Transistor) devices, available on this technology, demonstrate cut-off frequencies of $f_t = 300\,GHz$ and $f_{\max} = 300\,GHz$ with $0.5\,\mu m$ emitter width [24, 25] enabling up to $100\,GHz$ mixed signal design.

A 4-metal interconnect stack was used with MIM capacitors of $0.3\,fF/\mu m^2$ implemented between the first and the second metal layers. Signal lines were implemented using metal 1 and metal 2 as inversed microstrips with metal 4 serving as a ground plane. Some of the designed used a ground-plane implemented on metal 3 while the power lines on metal 4. The advantages and disadvantages of this option are farther described. The resistors were implemented by a $50\,\Omega/\mathrm{sq}$ thin film deposition.

3.2 High Frequency Digital Design

Some of the ICs described in this work are complex digital IC operating with digital signals over a $DC - 100\,GHz$ range. Such ICs design and layout required a combination of digital and controlled-impedance millimeter-wave techniques.

The limiting amplifiers and buffers were implemented using differential emitter-coupled logic (ECL) (Fig. 3). To avoid reduced circuit bandwidth from interconnect capacitance, all digital interconnects between gate were implemented as double-terminated transmission lines [26]. This introduces a resistive $25\,\Omega$ load to the driving stage. By working in such a $50\,\Omega$ environment, the degradation increase in gate delay caused by driving a long line is simply $\tau = l/v$, where l is the length and v is the propagation velocity. In contrast, if the gate were instead loaded with resistance $R_L \gg Z_0$, the additional delay would be $R_L C_{wire} = (l/v)(R_L/Z_0)$ [27].

The ECL emitter followers are placed at gate inputs, rather than gate outputs. If emitter followers are instead placed at gate outputs, their inductive output impedance can interact with any load .capacitance to cause ringing or instability.

The linear operation of a bipolar ECL stage is limited to input voltages of $\Delta V_{linear} \approx \frac{2kT}{q} + 2I_0 R_{EE}$, with I_0 is the differential tail current and R_{EE} the emitter contact resistance. To fully switch a bipolar differential pair with large noise margin, a logic voltage swing of $\Delta V_{logic} = 3\Delta V_{linear} \approx \frac{6kT}{q} + 6I_0 R_{EE} \approx 300\,mV$ for $I_0 = 12\,mA$, based on an equivalent collector load resistor of 25 Ω. According to this tail current, transistors are sized to operate at current densities approaching the Kirk-effect limit [28]. For the given ECL stage

parameters, the small signal gain is $A_V = g_m R_L = \frac{I_0 q}{2kT} R_L = \frac{\Delta V_{logic}}{2q/kT} = 6$.

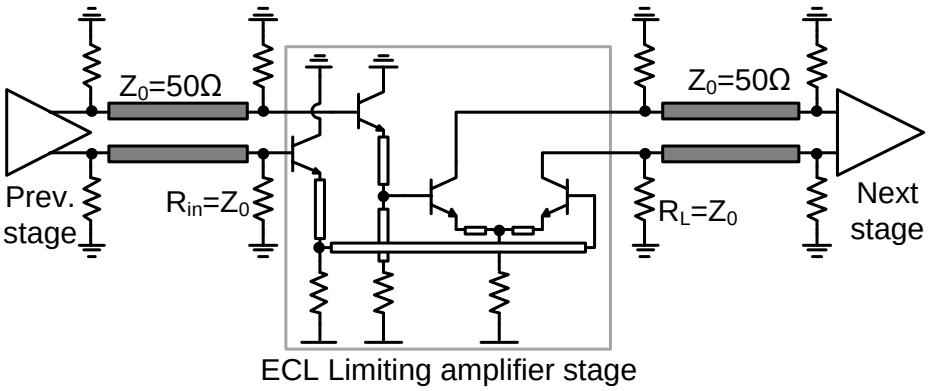


Fig. 3: ECL two-level logic with double terminated line interconnects.

Boolean logic, such as the 180° and 90° rotation blocks, XOR gate, and frequency divider are implemented in 2-level differential ECL logic, i.e. Gilbert cells (Section 5.3). To maintain a $50\ \Omega$ interconnect environment, these cells were placed along a $50\ \Omega$ double-terminated bus, Fig. 4. Interconnects from the gate to the bus present wiring parasitics and are kept short. The typical length of such vertical stubs is $30\ \mu m$, much shorter than a typical wavelength of $2.5\ mm$ at $40\ GHz$.

The two-level ECL cells (Fig. 4a) have three inputs: two on the upper level (A,B) and one on the lower level (C). The lower level inputs have longer delay, so when balanced delays are required, two parallel gates are used, with interchanged inputs and parallel outputs. Such realization was used with the XOR gate of the single side-band mixer IC.

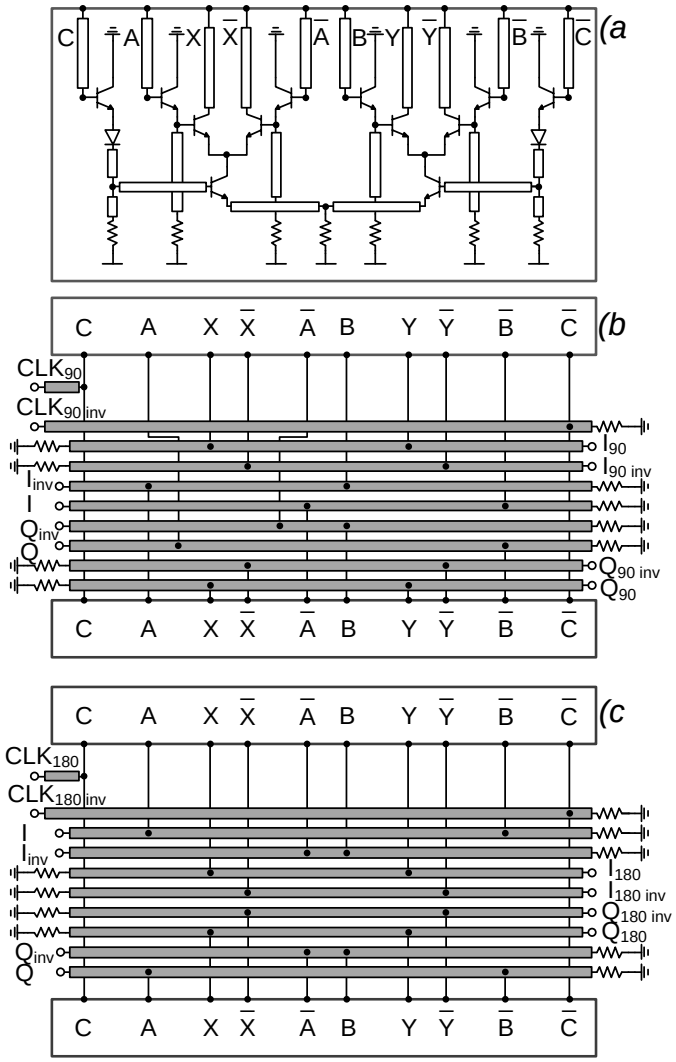


Fig. 4: a) Gilbert cell as a building block for Boolean logic, b) 90° rotation, and c) 180° rotation blocks schematics.

High frequency digital signal distribution (fan-out) was implemented by using three different techniques (Fig. 5). In the first method (a), the fan-out is implemented by simply splitting the $50\,\Omega$ line into two high impedance $100\,\Omega$ lines. The long line is correctly terminated in $50\,\Omega$, while the driving buffer sees a total load of $25\,\Omega$. The RC charging time is $\tau = 2C_L \cdot 25\Omega$. The second technique (b) uses a pair of $50\,\Omega$ lines, driven from a second gate. Each line, in the absence of the next stage capacitive loading, C_L (Fig. 5), is correctly

terminated. The RC charging time is $\tau = 2C_L \cdot 25\Omega$. Because the sending end of the transmission line is not correctly terminated, topologies (a) and (c) suffer from round-trip pulse reflections if C_L is significant. This is eliminated in the final topology (c) signals are split 2:1 locally and buffered with gates before distribution on $50\,\Omega$ doubly-terminated interconnects. In this technique the reflections are well controlled and the RC charging time is: $\tau = C_L \cdot 25\Omega$. Technique (c) introduces additional power consumption and layout complexity.

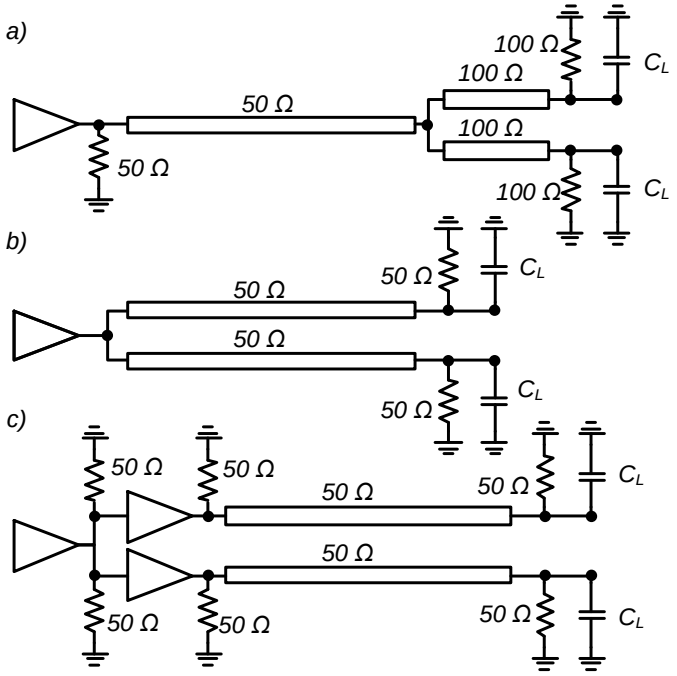


Fig. 5: Digital fan-out techniques. a) single line fan-out, b) double line fan-out, c) isolated double line fan-out.

The design of a $40\,GHz$ digital logic with a synchronized clock network requires precise electromagnetic (EM) modeling and verification, performed by the Agilent Momentum CAD tool. The top metal (M4) was assigned as a ground-plane while the majority of interconnects were implemented on M1 and M2 in a form of inverted thin-film microstrip lines Fig. 6a. M3 was primarily

used for local routing solutions and local interconnects within gates. The use of inverted microstrip allows narrow line spacing (approximately two times the line-to-ground distance: $8{\sim}10\,\mu m$), and continuous ground plane without breaks, maintaining ground integrity and avoiding ground-bounce. The use of a bottom ground plane within a complex IC environment would eventually lead to a highly fragmented ground (Fig. 7), unable to provide parasitics free current return paths. Due to the thin dielectric, the top ground plane makes the ground vias inductance negligible and allows dense ground vias spacing, as requires in complex IC. The drawbacks, however, of the thin dielectrics is the reduced line inductance, demanding thinner lines for high characteristics impedances. Thin lines also demonstrate increased skin loss and limit the maximum possible DC current [29].

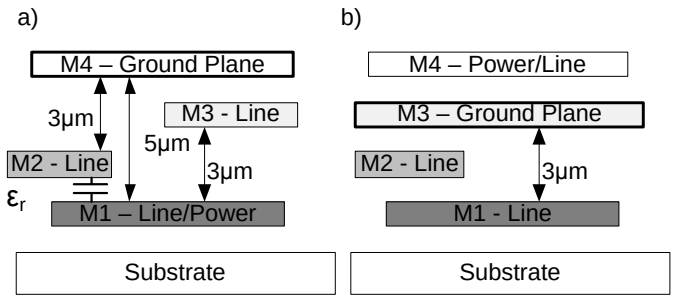


Fig. 6: Metal stack cross-section: a) M4 as a ground-plane, b) M3 as a ground-plane.

Compared to M1, the dielectric thickness between M2 and the ground-plane is smaller, creating difficulty in implementing high impedance lines and leading to increased resistive losses. The power grid was routed on M1, crossing M1 lines with M3 bridges, and M2 from beneath. The crossovers of M1–M2 lines and M2 – power lines introduce additional capacitance of $C_{cross} \approx 2\,fF$ for typical $5x8\,\mu m^2$ overlaps (Fig. 6a). This capacitance creates signal crosstalk.

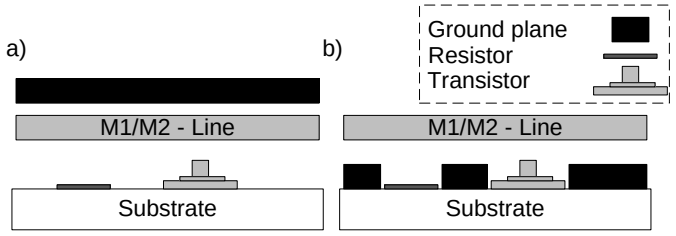


Fig. 7: a) Top ground plane, vs b) Bottom ground plane layout.

The other possible wiring strategy is to assign M3 as a ground plane (Fig. 6b) and to use M4 mainly as a power grid or for sensitive lines requiring complete crosstalk isolation. This approach completely eliminates the parasitic capacitance formed between the power and signal lines and greatly simplifies the design by separating the routing of power grids from signal lines. However, this methodology also has limitations. Due to a thinner dielectric, M2 lines are made narrower ($3\,\mu m$ wide for $50\,\Omega$ impedance), presenting even higher losses and unsuitable for long connections. Even with M1, the implementation of high impedance lines becomes impossible. To provide a power path to active devices, M3 needs to be perforated to allow vias to pass through, consequently violating the unity of the ground plane. However, the impact of these openings on M3 can be neglected if they are local and small in size. Eventually, both of the M3 and M4 ground-plane approaches allow a full EM simulation to be performed on the entire interconnects, rather than separately modeling individual segments.

The main advantage, however, of both ground-planes approaches is the constant and well defined cross-section of each interconnection, regardless to the interconnections nearby. This way a simulation transmission line model can be defined, and used for various lengths lines, yielding accurate results and reducing the need of EM simulations for every new line, of for every line modification.

4. InP HBT Optical Coherent BPSK Receiver

4.1 BPSK Receiver Electrical IC

The BPSK receiver IC is designed to work with PIC with 4-phases (0°, 90°, 180°, 270°) optical interferometer [9]. By measuring both in-phase and the quadrature-phase components of the local and the reference lasers beat-note, the phase-offset and the single side-band frequency offset information can be extracted. Under zero frequency offset, the Electrical Integrated Circuit (EIC) output is proportional to the optical phase difference; in the presence of an optical frequency difference, the IC output is proportional to this frequency difference. The ability to detect both phase and frequency difference enabling the OPLL to lock even with initial frequency offsets as large as $\pm 50\,GHz$. In addition, the phase offset characteristic demonstrates two stable states to lock on BPSK modulated signal.

4.2 Theory and Design

The full BPSK receiver system block diagram is presented on Fig. 8 where

the EIC diagram is marked in a grey dashed frame. The receiver receives the in-phase (0°, 180°) and the quadrature-phase (90° and 270°) components of the reference and local lasers beat-note, provided by the PIC optical interferometer and photodiodes. Assuming the LO laser electrical field is $E_{LO} = A \cdot \cos(\omega_{LO} + \theta_{LO})$ and the reference laser electrical field is $E_{REF} = A \cdot \cos(\omega_{REF} t + \theta_{REF})$, the in-phase and the quadrature-phase photocurrents provided to the EIC are $I = B \cdot \cos(\Delta\omega t + \Delta\theta)$, Eq. 1, and $Q = B \cdot \sin(\Delta\omega t + \Delta\theta)$, Eq. 3.

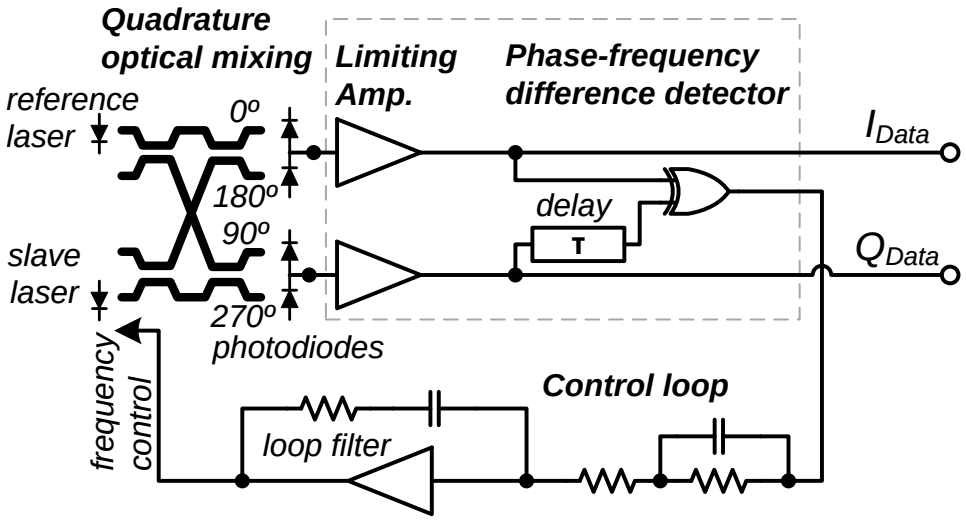


Fig. 8: A complete phase-locked coherent receiver. The block diagram of the BPSK phase-frequency detector IC is marked by a grey dashed frame.

$$Q_{PD} \propto \left| E_R e^{j(2\pi f_R t + \theta_R)} + E_L e^{j\left(2\pi f_L t + \theta_L + \frac{\pi}{2}\right)} \right|^2 = |E_R|^2 + |E_L|^2 + 2|E_R||E_L| \sin\left(\Delta\theta(t)\right) \quad \text{Eq. 3}$$

Both I and Q signals carry information on both phase and frequency offset magnitude and sign. The core of the phase-frequency detector (PFD) consists of a delay line in the Q arm and a XOR gate, which is based on a Gilbert

multiplier topology (Fig. 9), designed according to the design and layout methodology described at 3.2.

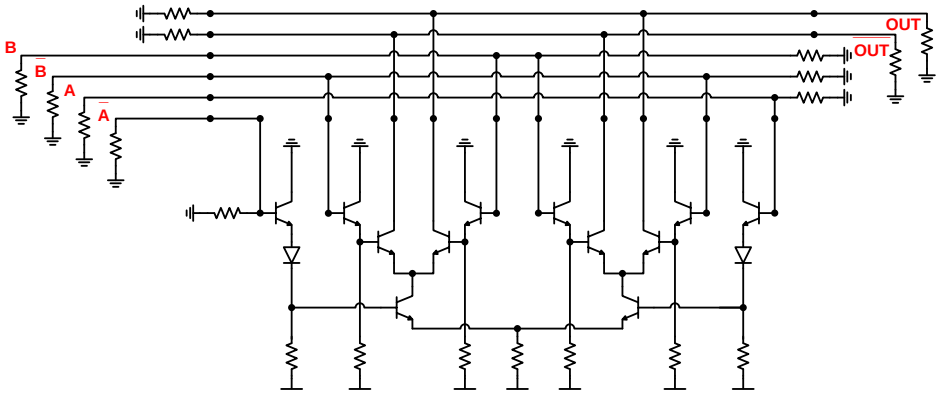


Fig. 9: XOR gate topology.

To reduce the dependency on the local and reference lasers photocurrent, the PFD is preceded by a chain of four high gain ECL limiting amplifiers that convert the signals into a rail to rail square wave - Fig. 10.

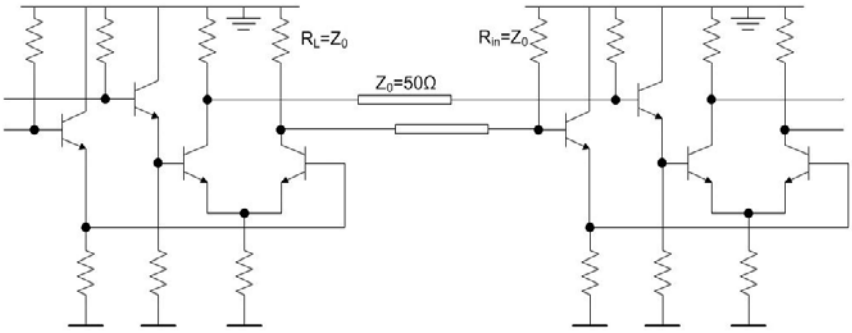


Fig. 10: Schematics of the limiting ECL gates merged in a 50 Ω transmission lines environment.

The input differential limiting amplifiers are designed to operate with unbalanced photodiodes PIC [19]; hence a new biasing topology was proposed (Fig. 11). The purpose of this topology is to present separate differential-mode

and common-mode input impedance. The DC current provided by the photodiodes is drawn by Q_1 and Q_2, biasing the photodiodes at $V_X \approx -V_{EE} + 2V_{BE} \approx -2\,V$, a DC voltage, enabling direct PIC – EIC connection without the use of DC blocks. In the differential operation mode the node V_X becomes a virtual ground, providing a differential input impedance of $R_D = 50\,\Omega$. A common mode signal will alter the V_X voltage, activating the $Q_3 - Q_{1,2}$ negative feedback loop, which results in the common mode current drawn by $Q_{1,2}$. Small signal analysis shows a common mode input impedance of $R_C/2$. This way the common and the differential input impedances can be controlled separately.

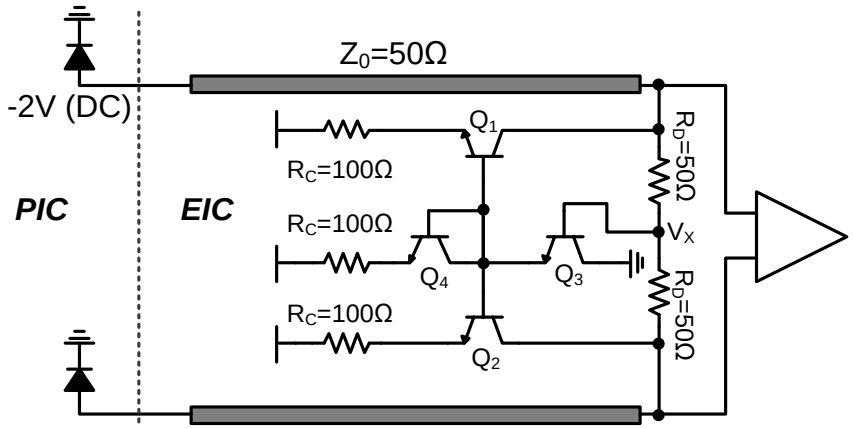


Fig. 11: Input biasing circuit.

For electromagnetic considerations, the IC is biased by a negative $V_{EE} = -3.8\,V$ and ground as a positive supply as the signal high frequency reference is the positive supply lines and it is better to drive the signal relative to the ground plane reference, rather than to a supply source. All the ECL gates are biased by a tail current of $12\,mA$, hence providing a differential signal of $600\,mV$ at a full swing mode, as fully explained at 3.2.

In case of frequency detection, the Q signal is delayed by τ and then mixed with I. A linear, small signal analysis of the PFD, Eq. 4, suggests that the

output signal consists of two components: a high frequency component with a double frequency but zero average and a DC component with magnitude proportional to the offset frequency Δf. Since the PFD output is integrated by a low frequency hybrid loop filter, the low frequency component is the one to consider.

$$I(t)\oplus Q'(t-\tau) = cos(\Delta\omega t + \Delta\theta)\sin(\Delta\omega(t-\tau) + \Delta\theta) \\ = 0.5sin(2\Delta\omega t - \Delta\omega\tau + 2\Delta\theta) + 0.5sin(\Delta\omega\tau) \qquad \textit{Eq. 4}$$

By setting $\tau = 10\,ps$, the DC term of Eq. 4, provides an unambiguous frequency detection characteristics of $\Delta f = \pm 50\,GHz$(equivalent to $\pm\pi$). Due to the limiting amplifiers the I/Q signals result in hard limited square waves. In this case, the PFD output will provide a double frequency square wave with varying duty-cycle that depends on the frequency offset, resulting in the same frequency detection characteristics (as seen on Fig. 12). This behavior can be understood when applying hard limiting function on Eq. 4. The DC component of the equation, i.e. $0.5sin(\Delta\omega\tau)$, shifts the double frequency sinusoid up or down, thus changing the mid-level crossing points. When clipped it results in varying duty-cycle. The simulated PFD output in a frequency detection mode for various offset frequencies is shown on Fig. 12. The double-frequency waveform has a varying duty cycle that is translated to an equivalent average value when integrated.

In phase detection mode, i.e. $\Delta\omega = 0$, the PFD output is $\sin(2\Delta\theta)$. The periodic phase detection characteristic, with a factor of 2 in the sin argument makes the loop stable for both $0°$ and $180°$ degrees offset. This particular property allows the loop to lock on a BPSK modulated carrier - Fig. 13. In BPSK modulation the carrier phase toggles between $0°$ and $180°$. Both of the

phases yield the same phase detection sign and value, thus maintaining the same loop behavior. When the loop is locked, the down-converted I/Q signals can be directly delivered to the signal processing block.

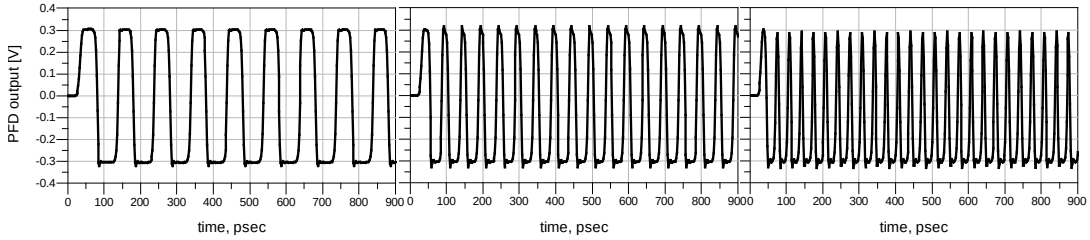


Fig. 12: PFD output waveform for frequency detection. From left to right: $\Delta f = 5\ GHz, \Delta f = 10\ GHz, \Delta f = 15\ GHz$

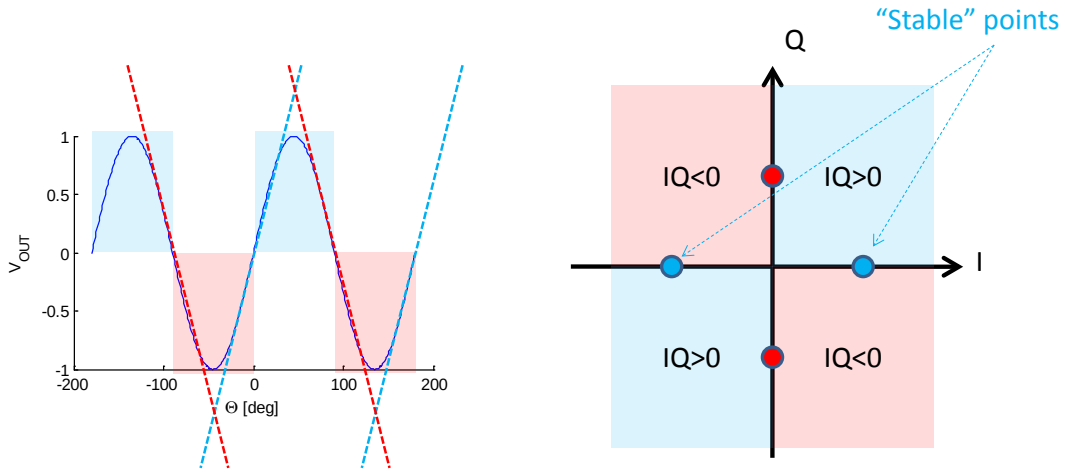
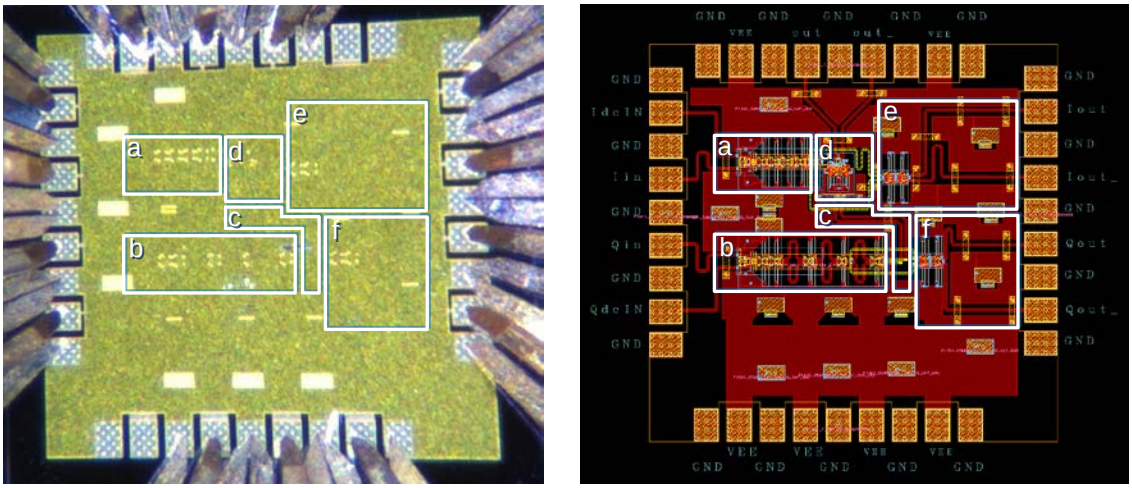


Fig. 13: PFD phase detection mode.

Fig. 14 displays the BPSK receiver EIC layout and chip photo. The I/Q beat-note photocurrents are applied on the left side of the chip, while the I/Q data is received on the right. The PFD output is delivered on the top side. As can be seen, the I/Q photocurrents are digitized by a four-limiting-amplifiers chain (frames a and b), and the Q signal is delayed by $\tau = 10\,ps$ (frame c) and mixed

with I (frame d). The downconverted data, after additional amplification, is then delivered (frame e and f). To overcome losses on the long delay line, it was partially implemented between the Q arm limiting-amplifiers chain (frame b). This way, amplifiers provide additional gain to mitigate the losses.



a) 'I' beat-note input path, b) 'Q' beat-note input path, c) 10ps delay line, d) XOR gate, e) 'I' data output, f) 'Q' data output

Fig. 14: BPSK receiver EIC chip photo and layout

4.3 Experimental and results

To fully characterize the phase frequency detector two typed of measurements should be performed: frequency detection mode and phase detection mode. In frequency detection mode (Fig. 15a) the $I \sim cos(\Delta\omega t)$ and $Q \sim sin(\Delta\omega t)$ signals were emulated by a single $40\ GHz$ RF signal generator (Agilent N5183A) with a power splitter and a ± 90 degrees relative phase shifter to emulate the actual photocurrents for positive and negative frequency offsets. In electrical characterization a single ended input version of a chip was used. The PFD output was inspected for the high frequency and DC components (Eq. 4),

separated using a Bias-T. The high frequency component was delivered to an Agilent 86100A sampling oscilloscope, with $50\,GHz$ HP 54751A sampling module; while the signal of interest, the DC component, was measured using the real time sampling oscilloscope (Agilent DSO6012A). The DC component of the measured output waveform (vs. simulated) in frequency detection mode is presented on Fig. 16. The DC component, $\sin(\Delta\omega\tau)$ (Eq. 4) for a delay line of $\tau = 10\,ps$ demonstrates a span of $\pm 50\,GHz$, indicating the frequency detection range.

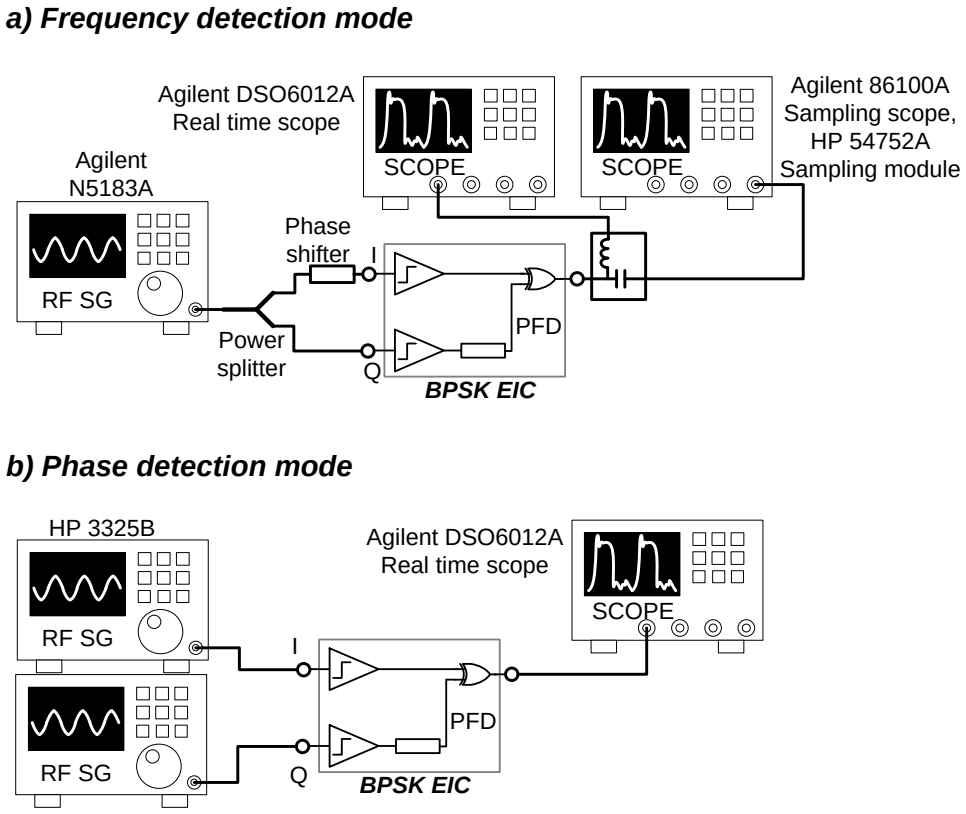


Fig. 15: Measurement setup for the BPSK EIC PFD. a) frequency detection mode, b) phase detection mode

In phase detection mode, activated when $\Delta\omega = 0$, the input photocurrents are $I \sim cos(\Delta\theta)$ and $Q \sim sin(\Delta\theta)$. In this case Eq. 4 is reduced to $sin(2\Delta\theta)$. Instead

of applying two DC inputs, emulating I and Q for different values of $\Delta\theta$, and then sweeping, the measurement was performed with two extremely low frequency ($10\,Hz$) sinusoidal inputs: $I \sim cos(2\pi \cdot 10Hz \cdot t)$ and $Q \sim sin(2\pi \cdot 10Hz \cdot t)$ provided by two HP 3325B signal generators (Fig. 15b). The PFD output was inspected using a real time sampling oscilloscope (Agilent DSO6012A). The measured waveform at the output of the PFD (Fig. 16 bottom) indicates a double frequency phase detection behavior as a function of $\Delta\theta$. Here, the time axis represents $\Delta\theta$, with period of $50\,ms$ (while the input period is $100\,ms$), proving the two-stable-stated concept.

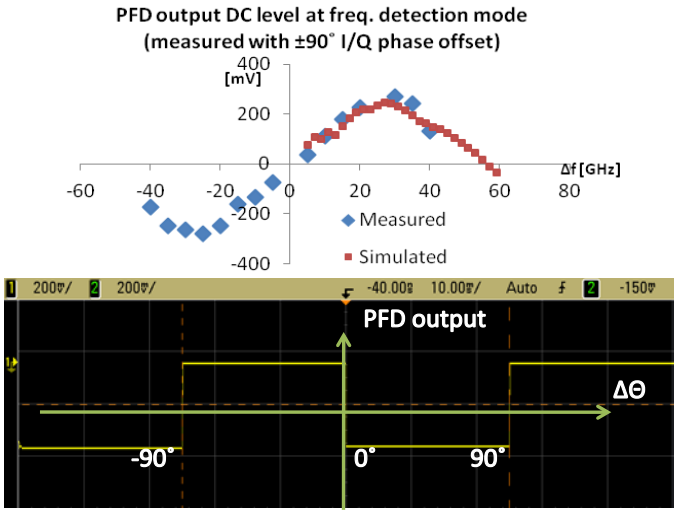


Fig. 16: Top – PFD frequency detection (measured vs. simulated). Bottom – PFD phase detection – measured.

The limiting amplifiers form a square-wave phase detection behavior. As the bang-bang type PLL loop is not usable (the bang-bang PLL is never actually locked so it cannot be used to recover data), a triangle-wave-approximation slope will be considered for loop design. This way, also, any dependency on the input photocurrents is eliminated.

4.4 BPSK Receiver – System

The full integration and characterization of the BPSK receiver is described in detail in [30-32]. Here we shortly bring the main system assembly considerations and parameters, and results overview.

4.4.1 BPSK Receiver Topology

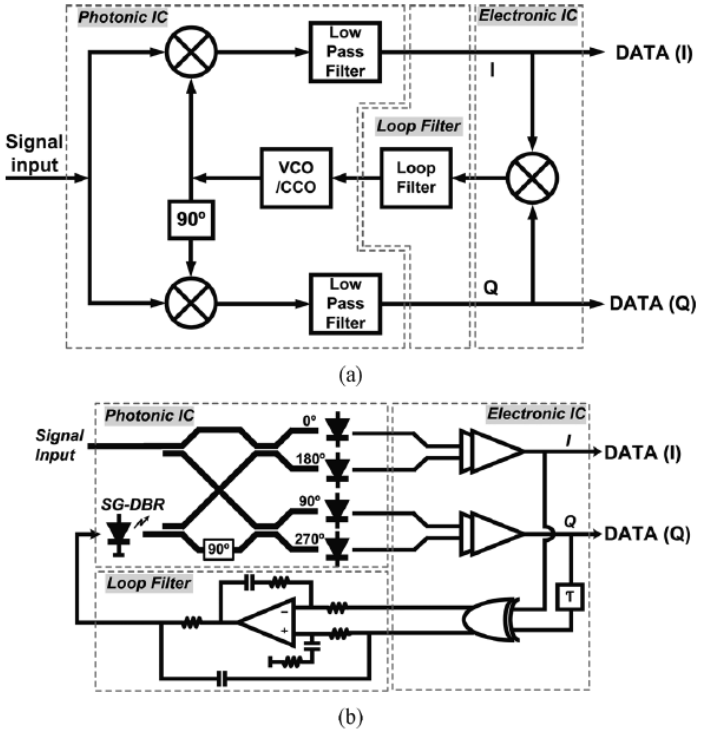


Fig. 17: (a) The classic model of a Costas loop, (b) Detailed representation of a Costas loop based OPLL, [32]

The OPLL based BPSK receiver Fig. 17 was design according to the Costal loop architecture [33]. Throughout the history of optical communication, Costas loop, as a homodyne OPLL, has been regarded challenging because of long

delay in the feedback loop due to the bulk size of photonic, electrical, and loop filter components [34, 35]. Such long loop delay limits the loop bandwidth, affecting the phase-noise suppression and track/hold ranges. In these cases, the OPLL requires stable and narrow linewidth reference sources for both the LO and transmitting lasers to maintain a proper operation under a stable phase-lock [13, 33, 36, 37].

Recently, number of works has reported a relatively stable OPLL feedback loop using integration technology. A homodyne OPLL using a high speed HEMT for a small delay loop filter with a loop bandwidth of $300\ MHz$ [38], a heterodyne OPLL using an RF XOR as a phase detector with loop delay of $1.8\ ns$ [39], and a highly integrated heterodyne OPLL using an integrated single side band mixer and a PFD with delay of $0.2\ ns$ and closed loop bandwidth of $550\ MHz$ [19] were published. OPLL based coherent optical receivers have been also demonstrated. Costas receivers using homodyne OPLLs with below $10\ Gbit/s$ [40, 41], decision-driven loops including sub-carrier modulation scheme [42, 43], and a digital OPLL using a sampled I-Q signals with slow DSP for homodyne reception of PSK $40\ Gb/s$ [35] have been published. However, the receivers still require a narrow linewidth of the LO and transmitting lasers due to a narrow loop bandwidth, and they may need additional blocks such as voltage controlled oscillators, a Mach–Zehnder modulator, and even digital processing blocks to recover the carrier signal.

System	
Carrier	AlN
Area	$10 \times 10\ mm^2$
Power	$3\ W$
$f_{closed\ loop}$ (PD)	$1.1\ GHz$
$f_{closed\ loop}$ (FD)	$178\ KHz$
Frequency pull-in	$17.5\ GHz$
Loop delay	$120\ ps$

LF	
Type	II
$f_{open\ loop}$	$700\ MHz$
$P.M.$	$60°$
Propagation delay	$30\ ps$
Op-Amp.	TI LMH6609

EIC	
Area	$1.3 \times 1.2\ mm^2$
Propagation delay	$50\ ps$
Power	$2\ W$
Output voltage levels	$600\ mV_{p-p}$
Frequency detection	$K_{FD} = 12\ mV/GHz$
Phase detection	$K_{PD} = 0.2 \sim 0.4\ V/rad$

PIC	
Area	$4.3 \times 0.54\ mm^2$
Propagation delay	$40\ ps$
Power	$0.5\ W$

SG-DBR Laser	
Tuning range	$1541 - 1583\ nm$
Tuning response	$K_{CCO} = 8\ GHz/mA$
Small signal resistance	$R_d = 100\ \Omega$
P_{out}	$20\ mW$
Time constant	$\tau_{laser} = 1.6\ ns$

Photodetectors	
Quantum eff.	$> 95\%$
Contact resistance	$R_{cont} = 100\ \Omega$
Cut-off frequency	$35\ GHz\ @\ 50\ \Omega load$

Table 2: BPSK receiver – OPLL loop parameters

According to the electrical Costas loop architecture (Fig. 17a), the input signal is downconverted using an I/Q quadrature phases of a local voltage controlled oscillator (VCO). The downconverted signal is then mixed again to form a feedback-signal to control the frequency of the local VCO. The loop filter determines the loop dynamics, such as loop bandwidth, loop order,

stability, etc. The optical Costas loop shares the same architecture. As shown on Fig. 17b, the InGaAsP/InP based PIC includes a widely-tunable sampled-grating DBR (SG-DBR) laser, operating as the current-controlled oscillator (CCO), while the quadrature signals are generated in an optical 90-degree hybrid, [44], where the 90° phase shift is introduced by an optical phase shifter, based on current injection. The I/Q signals are detected by four high speed photodetectors, which convert the optical signal to electrical one and act as low pass filters. The EIC block is described in 4.1. The error signal from the PFD feeds back to the laser – a CCO, through the loop filter (LF). An active LF with a novel two-path loop structure was developed [30], including an active slow path and a passive feed-forward fast path. The feed-forward path includes no active components and provides the shortest delay possible for high frequency signals, while the active path is composed of an operational amplifier (Op-amp) based active filter, which serves as an integrator on frequency, forming a type II loop, [21]. The structure of this loop filter is also shown in Fig. 17b.

A full listing of the parameters of loop components is brought in Table 2. The system was integrated on an AlN $10 \times 10\, mm^2$ carrier with a total loop delay of $120\, ps$ allowing closed-loop bandwidths of up to $1\, GHz$.

4.4.2 FEEDBACK LOOP ANALYSIS

The LF is comprised of two parallel paths: The active integration path dominant at low frequencies, while a high-frequency feed-forward path reduces the loop delay, thus increases the closed loop bandwidth.

Eq. 5 describes the loop transfer function written as a sum of two parallel paths. $\tau_{OP} = 1/2\pi \cdot 100MHz$ and $\tau_{d\_op} = 200\, ps$ are the pole and the delay of

the operational amplifier, respectively. $C_{FF} = 1\,pF$ is the feed forward capacitor (Fig. 17b) and $R = 500\,\Omega$ is the resistor at the output of the op-amp that translates the output voltage to a laser tuning current. $\tau_{laser} = 1/2\pi \cdot 100MHz$ is the laser's response pole. τ_1 and τ_2 were determined at $17\,MHz$ and $2.2\,MHz$, respectively, according to the values of the op-amp feedback network components. Eventually, $\tau_d = 120\,ps$ is the loop delay.

Besides the design effort to achieve high phase margins and high closed loop BW, additional effort was made to avoid a $180°$ phase difference between the two paths at their crossover frequency, what could cause a closed loop gain notch [30].

$$T(s) = K_{PD}K_{CCO} \cdot \frac{1}{\tau_{laser}s + 1} \cdot \left(\frac{\tau_2 s + 1}{\tau_1 s^2} \cdot \frac{1}{\tau_{OP}s + 1} \cdot \frac{1}{R} \cdot e^{-\tau_{d\_op}s} + \frac{C_{FF}}{2}\right) \cdot e^{-\tau_d s} \qquad \textit{Eq. 5}$$

The loop response shows a natural frequency of $\omega_n = 4.4 \times 10^9 \frac{rad}{s} = 700\,MHz$ and $65°$ phase margin.

4.4.3 System Integration and Experimental Results

The system was realized on a single AlN substrate ($\varepsilon_r = 9$) of a $10 \times 10\,mm^2$ size, Fig. 18. The components are connected using wirebonds or on-board transmission lines. The red arrow indicates the feed-forward path that was minimized for shortest delay. The active loop filter is comprised of a commercial voltage feedback op-amp, TI LMH6609 with $70\,dB$ open loop gain and $200\,MHz$ gain-bandwidth-product.

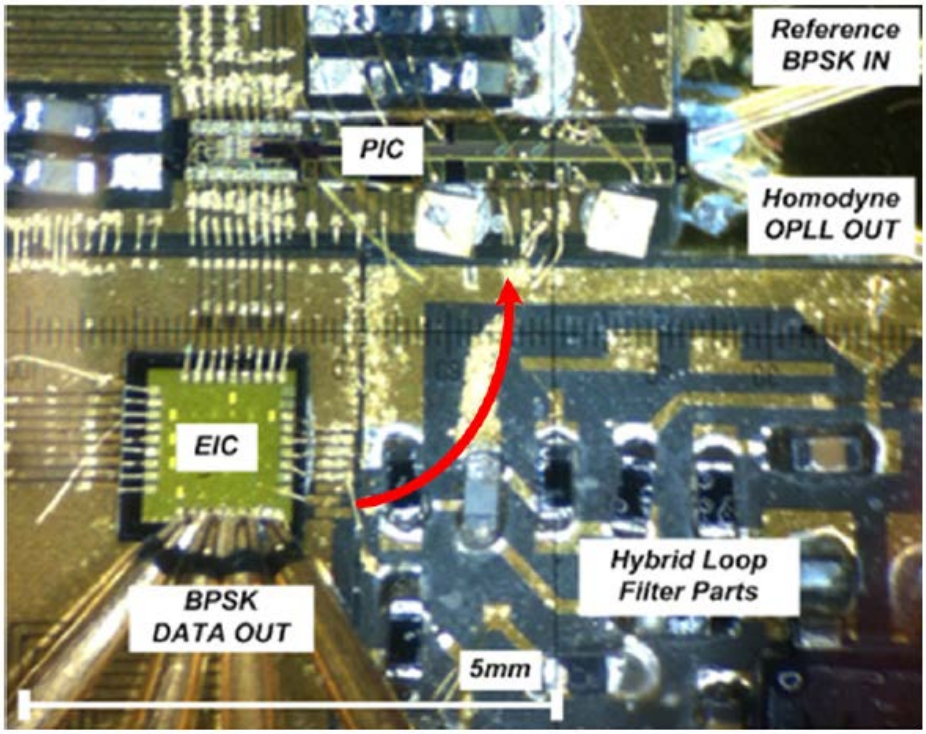


Fig. 18: Costal-loop OPLL system photograph (Red arrow: feed-forward path) [30].

A Koshin Kogaku tunable laser, with $100\,KHz$ linewidth, was used for a 1550nm external reference laser. The SG-DBR laser was locked to the reference laser and beat with the modulated reference laser using a $100\,MHz$ acousto-optic modulator (AOM). The spectrum of the beat signals was examined using an electrical spectrum analyzer (ESA), Fig. 19 – peak tone at $100\,MHz$, right side peak at $1.2\,GHz$, and left side peak at $1.0\,GHz$ as an image frequency. From the spectral results, a closed loop bandwidth of $1.1\,GHz$ is observed.

To prove the BPSK coherent optical receiver performance, BER vs. OSNR has been measured using a test setup as shown in Fig. 20. A PRBS $(2^{31}-1)$ pulse pattern generator and Mach-Zehnder Modulator (MZM) have been used for BPSK optical data modulations up to $40\,Gbit/s$, and OSNR has been

controlled by a variable optical attenuator (VOA) prior to the Erbium doped fiber amplifier (EDFA) and $0.95\,nm$ optical band pass filter (BPF). Only I-differential outputs from the EIC are connected to $50\,Gbit/s$ BERT measurement through an external differential decoder using a $50\,Gbit/s$ XOR and 1 bit-delay by phase shifters to solve the phase ambiguity of the Costas loop. At the same time, lock status of the SG-DBR has been monitored with an ESA. A BER vs. OSNR has been measured for $25\,Gbit/s$ to $40\,Gbit/s$ as shown in Fig. 21, and the BPSK receiver exhibits error-free ($BER < 10^{-12}$) up to $35\,Gbit/s$ and $BER < 10^{-7}$ for $40\,Gbit/s$. Open received eye outputs for $25\,Gbit/s$ and $40\,Gbit/s$ are measured using a $70\,GHz$ sampled oscilloscope without the differential decoder. In addition, the linewidths of the locked SG-DBR laser with $25\,Gbit/s$ BPSK data and without the data are measured as shown in Fig. 22 using a self-heterodyne technique with a $25\,km$ fiber, and all locked SG-DBR lasers show the same linewidth of $100\,kHz$ as the reference laser. This result suggests that the Costas loop with a $25\,Gbit/s$ BPSK data modulation can restore the carrier laser without degrading the linewidth and data reception performances.

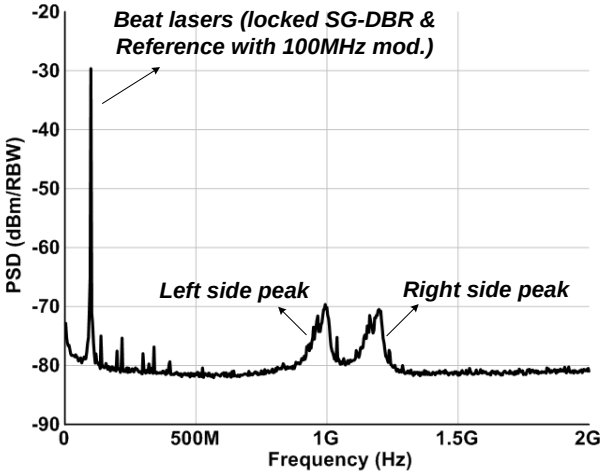


Fig. 19: A beat spectrum between a homodyne OPLL and a reference laser with $100\,MHz$ *modulator (RBW:* $100\,KHz$*),* [31]

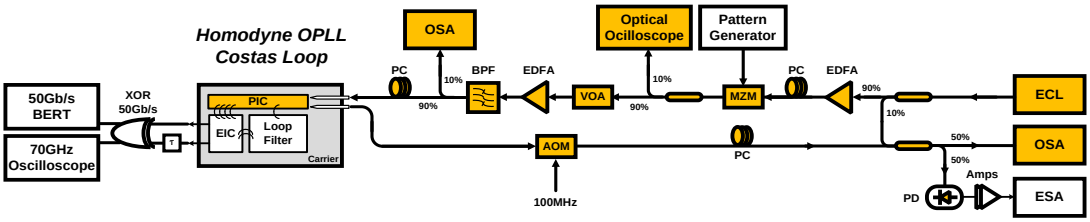


Fig. 20: A test setup of BER vs. OSNR for a Costas BPSK homodyne receiver (ECL: external cavity laser, PC: polarization controller), [31]

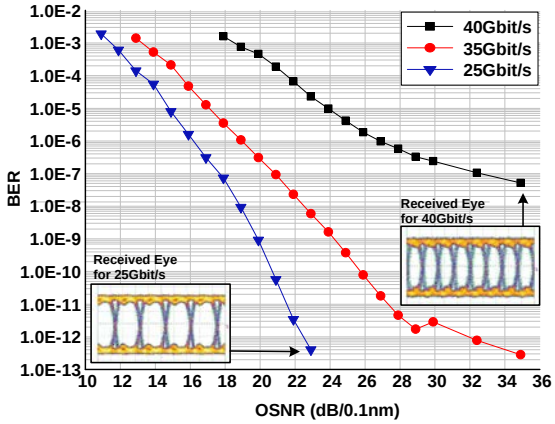


Fig. 21: BER vs. OSNR for $25\sim40\ Gbit/s$ *and the received eye outputs for* $25-40\ Gbit/s$, [31]

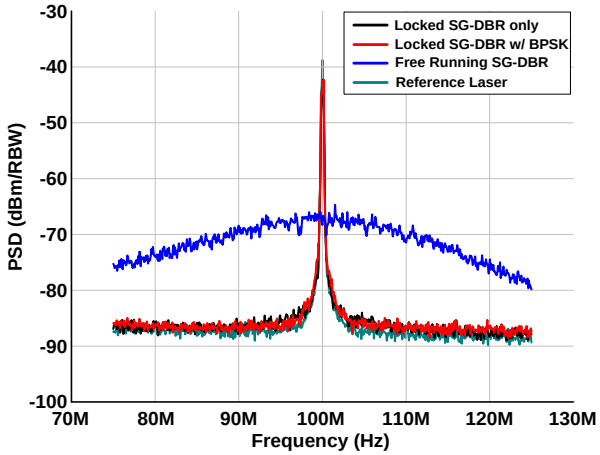


Fig. 22: Self-heterodyne linewidth measurements for locked SG-DBR without and with $25\ Gbit/s$ *PBSK, free-running SG-DBR, and a ref. laser (RBW:* $50\ KHz$*),* [31]

5. A 1-20 GHz All-Digital InP HBT Optical Wavelength Synthesis IC

5.1 Background

Coherent communication methods have been of a great interest due to their superior noise performance comparing to the direct-detection ones. However, coherent communication is mainly based on a free running optical local-oscillator (LO) and digital processing after detection for data and clock recovery. WDM optical communications systems use diode lasers coupled to optical resonators to produce optical channel spacing, typically $\sim 50\,GHz$. The WDM receiver, in turn, is implemented by optical filters to separate the channels. In marked contrast, in microwave systems, frequencies are precisely determined by PLL/synthesis techniques, allowing close frequency spacing of communications channels and efficient use of the spectrum. Using OPLLs [45]-[39], pairs of lasers can be locked in both optical phase and frequency. By introducing frequency offsets within the OPLL, the frequency difference between a pair of lasers can be set to this injected frequency, allowing wavelength spacing within WDM, LIDAR, and other optical systems to be set

precisely and under digital control. This is optical wavelength synthesis.

Due to the large optical frequency (e.g. $193\,THz$ for a $1550\,nm$ laser), frequency division techniques cannot be used for frequency synthesis. Because of the large ratio of optical oscillator frequency to the typical loop bandwidth in OPLLs ($\sim 200\,MHz$ - $1\,GHz$), it is also much more difficult to force the loop to lock. The large initial frequency offset between lasers forces development of frequency difference detectors operating over a $100\,GHz$ bandwidth. To get a large loop bandwidth, yet preserving stability, the loop delay must be minimized [13]. One factor determining loop delays is the speed-of-light propagation delay on both optical waveguides and electrical interconnects. To minimize this delay, the loop must be physically small. This goal is best achieved by monolithic integration. Previously reported OPLLs [15, 17, 38, 39, 45] have used an optical interferometer, which measures the sign of the phase offset between the two lasers. This is insufficient to extract the sign of the laser frequency offset, information required for either frequency offset detection or for frequency offset-locking with an unambiguous sign to the frequency offset. By measuring both the sine and cosine of the laser phase offset in a quadrature-phase (I/Q) interferometer, both in-phase and quadrature-phase components of the offset signal are measured. This allows both measurement of frequency offset and use of a single side band mixer to perform offset locking with controlled frequency offset magnitude and sign.

Table 3 summaries important milestones in optical offset phase locking. An OPLL for frequency-offset locking contains a PIC, a microwave EIC containing frequency offset control and phase-frequency detectors, and a high-frequency ($500\,MHz$), low-delay feed-forward-compensated op-amp loop-filter [30]. This work mainly focused on the design methodology and performance of the EIC – an InP HBT optical wavelength synthesis IC comprising of a $1-20\,GHz$ *digital*

single-sideband (SSB) mixer and a $\pm 40\,GHz$ phase-frequency difference detector. The digital design eliminates the dependence of loop bandwidth on optical signal levels (i.e. input photocurrent magnitudes) and enables wide frequency locking range.

Work (year)	Loop Delay	Frequency detection	Single side-band locking	Comments
[45] (2011)	1 ns	No	No	Hybrid XOR gate
[15] (1999)	380 ps	No	No	Hybrid mixer and PD
[17] (1992)	400 ps	No	No	
[19] (2012) using the reported IC	200 ps	Yes	Yes	Fully integrated SSB Mixer and PFD

Table 3: Heterodyne Optical Phase Locking – Parallel works

5.2 Optical Synthesizer Design

A simplified offset locked OPLL block diagram is presented in Fig. 23. The loop is comprised of an optical interferometer acting as a phase detector, a microwave mixer to apply frequency offset (Δf_{ext}), and a loop-filter to control the loop bandwidth and dynamics. For a reference laser frequency f_R and a slave laser frequency f_L, the photodiodes output current, given by Eq. 1, while the phase detection gain, K_{PD} is given by Eq. 2. As was mentioned previously, by using this topology, the frequency offset sign cannot be determined and the

phase detection gain, K_{PD}, dependency on the input photocurrent potentially compromises the loop stability.

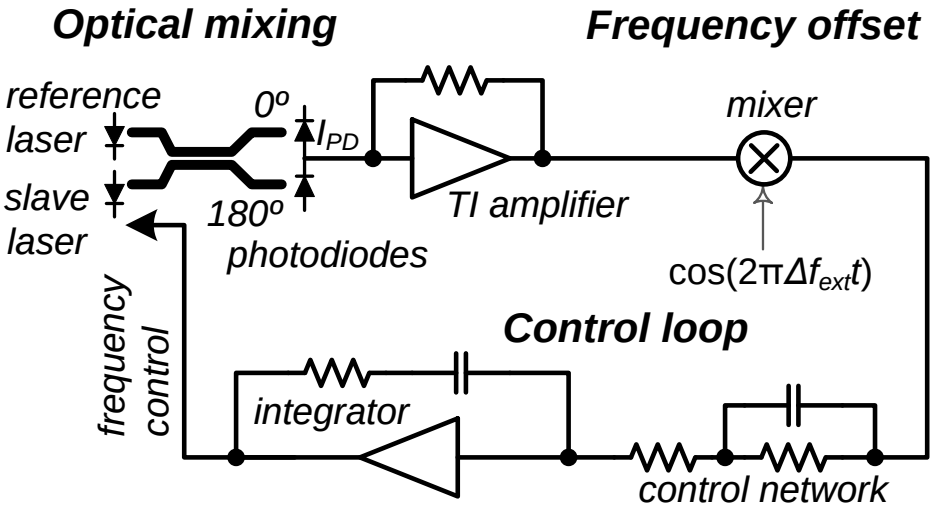


Fig. 23: Simplified OPLL block diagram.

A microwave mixer downconverts the beat note to $\cos(2\pi(\Delta f - \Delta f_{ext})t + \Delta\theta_0)$. Since the downconverted signal frequency falls within the loop bandwidth range, the loop locks the lasers with Δf_{ext} offset.

In a type II PLL, which has a zero steady state error in response to a ramp input, the loop-filter includes an integrator with a compensating zero, with loop filter current gain transfer function of $(1 + \tau_1 s)/\tau_2 s$, where τ_1 and τ_2 are integration and zero time constants. Given this filter transfer function, the overall PLL loop transmission is as in Eq. 6. A laser operates as a CCO whose tuning coefficient is defined as $K_{CCO} = df_L/dI$. As with a VCO, the CCO provides additional integration in the loop transmission.

The loop bandwidth, f_{PLL}, is the frequency for which $\|T(2\pi j f_{PLL})\| = 1$ approximated by Eq. 7 and determined by the loop-filter time constants, phase-detection gain, and the laser's current-to-frequency conversion gain.

$$T(s) = K_{PD}\frac{K_{CCO}}{s}\cdot\frac{1+\tau_1 s}{\tau_2 s} \qquad \textit{Eq. 6}$$

$$f_{PLL} \approx \frac{\tau_1}{2\pi\tau_2}K_{PD}K_{CCO} \qquad \textit{Eq. 7}$$

To measure the sign of the frequency offset, both the in-phase (I) and quadrature-phase (Q) (Eq. 1 and Eq. 3 respectively) components of lasers offset beat-note are required. Since a simple optical interferometer provides only the in-phase component, I_{PD}, a 90 degree optical hybrid [20] should be used.

Fig. 24 suggests a block diagram of an analog OPLL loop with a single side-band mixer for offset sign control, and a phase-frequency detection mechanism to extend the frequency locking acquisition range. In this OPLL, the reference and slave laser are mixed at $(0°, 90°, 180°, 270°)$ phase offsets and detected by photodiodes, producing photocurrents proportional to the cosine (I) and sine (Q) of the optical phase difference. The coupler and photodiodes thus form an I/Q mixer.

To control optical frequency offset spacing, the slave laser must be locked to a controlled positive or negative frequency offset from that of the reference laser. The offset is introduced by shifting the I/Q photodetector signal frequencies using a two-stage (Weaver) single-sideband mixer implemented using quadrature optical and microwave mixers. The microwave offset reference LO, provided by a microwave synthesizer, thus controls the optical frequency spacing.

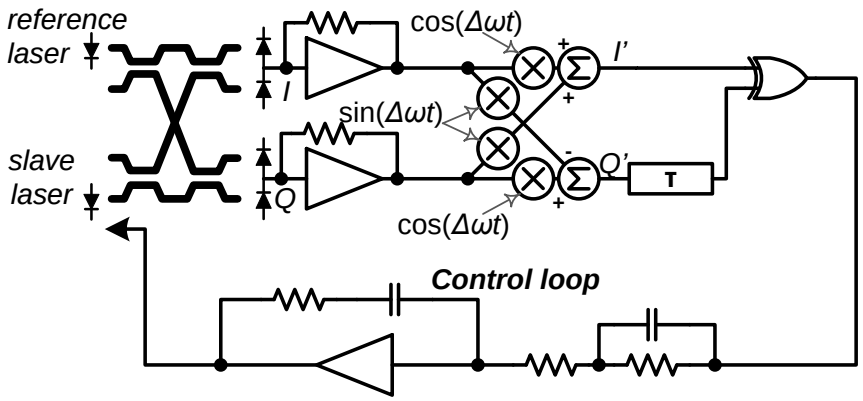


Fig. 24: A generic diagram of an OPLL consisting of reference and locked lasers, 4-phase optical mixing, offset frequency injection with a single-sideband mixer, phase-frequency difference detector, and loop filter

The I/Q photocurrents provided by the photodiodes (given by Eq. 3) are $I \sim \cos(\omega_d t + \theta_d)$, $Q \sim \sin(\omega_d t + \theta_d)$, where ω_d is the frequency difference between the reference and the slave laser and θ_d is the phase offset. Propagating the I/Q signals through the single sideband mixer yields the following – on the I arm:

$$\begin{aligned} I' \sim I \cdot \cos(\Delta\omega t) + Q \cdot \sin(\Delta\omega t) &\sim \cos(\omega_d t + \theta_d + \Delta\omega t) \\ &+ \cos(\omega_d t + \theta_d - \Delta\omega t) - \cos(\omega_d t + \theta_d + \Delta\omega t) \\ &+ \cos(\omega_d t + \theta_d - \Delta\omega t) \sim \cos((\omega_d - \Delta\omega)t + \theta_d) \end{aligned} \qquad \textit{Eq. 8}$$

While on the Q arm:

$$\begin{aligned} Q' \sim -I \cdot \sin(\Delta\omega t) + Q \cdot \cos(\Delta\omega t) &\sim -\sin(\omega_d t + \theta_d + \Delta\omega t) \\ &+ \sin(\omega_d t + \theta_d - \Delta\omega t) - \sin(\omega_d t + \theta_d + \Delta\omega t) \\ &+ \sin(\omega_d t + \theta_d - \Delta\omega t) \sim \sin((\omega_d - \Delta\omega)t + \theta_d) \end{aligned} \qquad \textit{Eq. 9}$$

Eq. 8 and Eq. 9 suggest that when looking in the I'/Q' signals (the I/Q signals

after the single sideband mixer), the loop becomes similar to the BPSK receiver (Eq. 4), only now the loop tends lock the lasers on $\omega_d - \Delta\omega = 0$, i.e. $\omega_d = \Delta\omega$. In other words, the loop will lock when the frequency offset between the two lasers is equal to the external RF signal, rather than to zero.

A Quadricorrelator PFD [22] provides an error signal proportional to the offset frequency – Eq. 4. The first term of Eq. 4 is responsible for the phase detection, when $\omega_d - \Delta\omega = 0$, and provides a $180°$ period characteristic as a function of θ_d. In case of $\omega_d - \Delta\omega \neq 0$, the second term of the equation provides a frequency detection indication with detection range set by the τ delay.

The analog OPLL loop will only operate well for I/Q signals within the linear range of the mixers and any amplifiers between them and the photodetectors. Given variable photocurrents, this will require automatic gain control (AGC). Even with such AGC, the phase detection gain, K_{PD}, will still depend upon the reference and slave lasers optical intensity. It is also difficult to design a wideband single-sideband mixer using standard analog topologies, since these require cosine and sine components of the RF signals [23] and hence $90°$ phase shifters, injection-locked frequency dividers or hybrid $90°$. Such phase-generation techniques are essentially narrow-banded. To obtain a wide offset locking frequency range, a digital frequency translation technique was developed.

5.3 Theory and Design

To enable tuning of a frequency offset over a wide ± 1 to $\pm 20\,GHz$

bandwidth, and to reduce the dependency on the photocurrents from the PIC, an all-digital SSB mixer is proposed - Fig. 25. The I/Q photocurrents generated by the PIC detectors are converted to digital levels using a chain of limiting amplifiers, Fig. 3. Because the mixer and phase/frequency detector are entirely digital, the phase-detector and frequency-detector gains are independent of IC process parameters (transistor and passive element parameter values). In marked contrast, had a linear analog mixer and phase detector been designed, the loop bandwidth would have varied with variations of optical component parameters (hence photocurrent amplitudes), and mixer and preamplifier gains. In this circumstance, precise control of the OPLL bandwidth would have been difficult to obtain.

Subsequent to digital limiting, frequency shifts are introduced with a digital SSB mixer (Fig. 25). Given a positive laser frequency offset Δf, the I/Q photocurrents rotate counterclockwise through the points (1,1), (-1,1), (-1,-1), (1,-1) in the (I,Q) plane (Fig. 26). For a negative frequency offset, $-\Delta f$, this rotation reverses. For zero frequency offset the constellation remains static at one of the four points as determined by the relative laser phases.

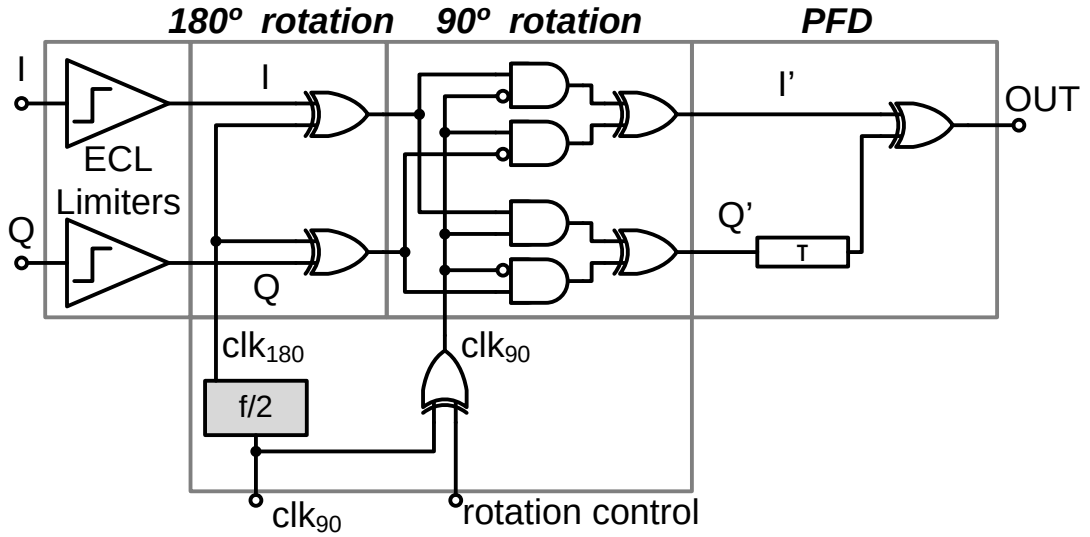


Fig. 25: Digital block diagram of the OPLL IC, consisting of input limiter amplifiers, a digital SSB mixer implemented with 180° *and* 90° *rotation blocks, and an phase-frequency difference detector.*

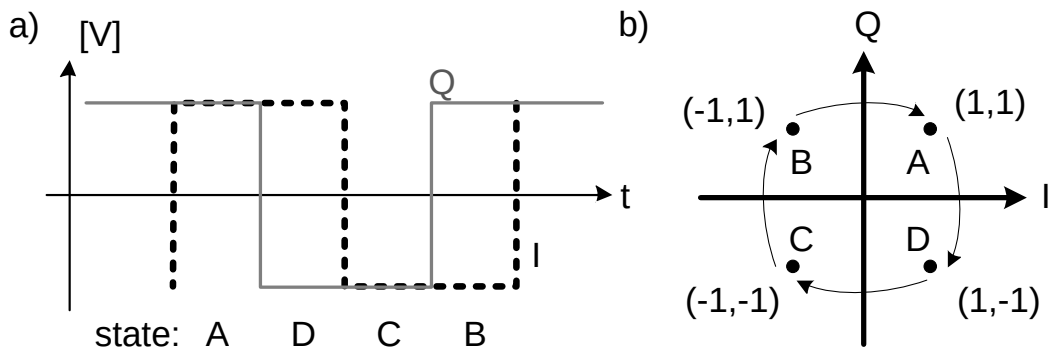


Fig. 26: Digitally limited I/Q signals for optical frequency offset. a) Time domain square wave. b) Rotating constellation in the (I,Q) plane.

The digital SSB mixer provides a frequency offset by rotating this constellation in the opposing direction, producing a static output pair (I',Q'). The mixer is formed of cascaded 180° and 90° rotation blocks. The 180° block rotates the (I,Q) state by 180° (i.e. A→C, B→D, etc.) when its input clock is 1 but provides no rotation when its input clock is 0. The 90° block rotates the (I,Q) state by 90° (i.e. A→B, B→C, etc.) when its input clock is 1, but provides no rotation when its input clock is 0. Applying high clock signals to both blocks rotates the state by 270° (Fig. 27). Applying periodically clock signals f_{clk90}, f_{clk180} at a 2:1 frequency ratio to the 180° and 90° rotation blocks rotates the I'/Q' constellation and provides a frequency shifts Δf; these signals are derived from a static frequency divider [46], (Fig. 25). Inverting the sign of f_{clk90}, by changing the rotation control signal, inverts the rotation direction, therefore the sign of the frequency offset.

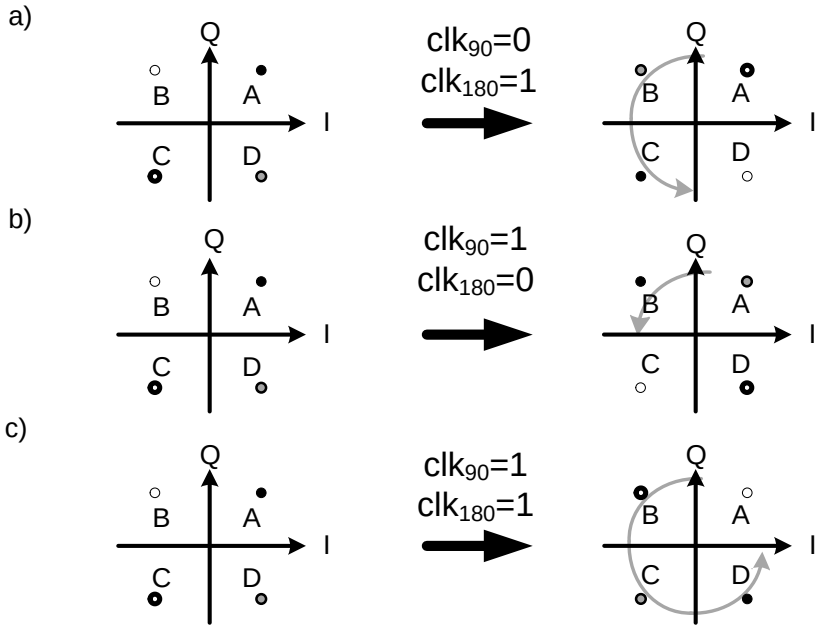


Fig. 27: Digital state rotation. a) 180° *rotation, b)* 90° *rotation and c)* 270° *rotation.*

The PFD is an ECL XOR gate with a delay line of $10\,ps$ in the Q arm. This frequency detector permits automatic loop acquisition for offset frequencies below $\pm 50\,GHz$. To force equal transistor delays on both inputs, the gate uses two parallel multipliers with crossed inputs and shunt outputs. The small signal analysis of the PFD is developed in Eq. 4.

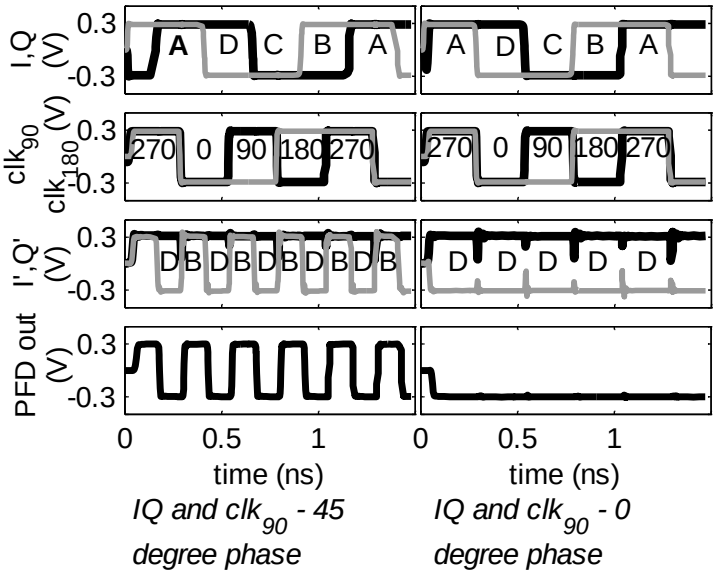


Fig. 28: SSB mixer in phase detection mode. Signal propagation as a function of various I/Q phases relative to clk_{90}*. For* $45°$ *phase a* 50% *duty cycle output signal with zero average DC.*

In phase-locked mode, i.e. when the laser offset, Δf, matches the clk_{90} frequency (i.e. $f_{clk90} = 2\Delta f$) under a suitable rotation control sign, the relative phase between the lasers will change the I/Q signals phase relative to clk_{90} and clk_{180}. This will eventually result in (I',Q') state oscillating at a frequency $2f_{clk90}$ between two adjacent states (A and B, B and C, etc.) with a duty cycle determined by the phase offset (Fig. 28). In this operation mode, either I' or Q' is constant while the other signal oscillates between 1 and 0 at a frequency of f_{clk90} with a duty cycle varying linearly with the phase offset. In this mode, the output of the XOR gate is a similar oscillating digital signal. For a $45°$ (I,Q) phase relative to clk_{90}, the oscillation has 50% duty cycle, hence the PFD provides zero DC (average) output. This brings the system into lock. Because the PFD output is digital with only its pulse duty cycle varying as a function of loop phase offset, there is no dependence on the photocurrent magnitudes of circuit's parameters.

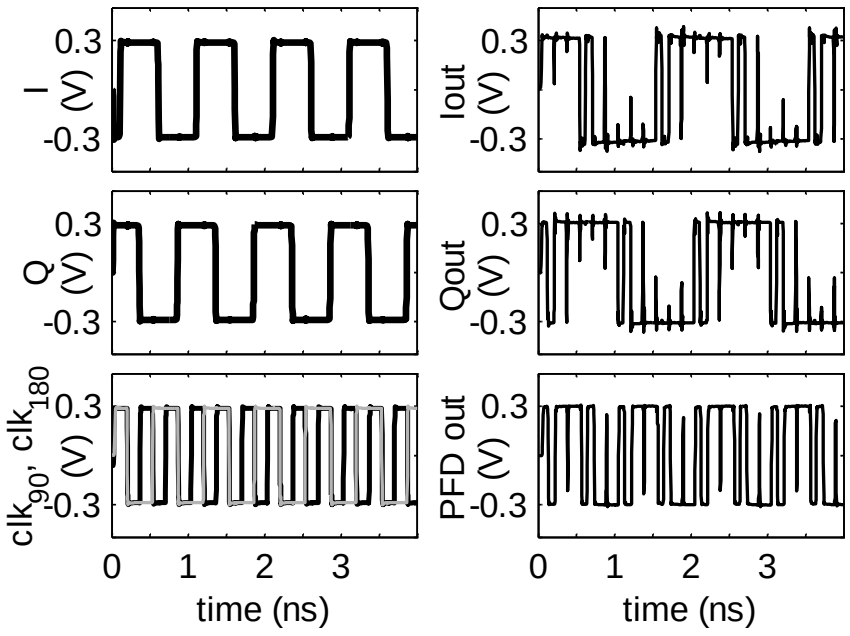


Fig. 29: SSB mixer at frequency locking mode. $\Delta f = 1\ GHz$ *and* $f_{clk90} = 3\ GHz$*. Since frequency lock occurs only for* $\Delta f = 1.5\ GHz$*, the (I',Q') state will rotate at the error frequency of* $0.5\ GHz$*.*

In PLL frequency acquisition mode, which occurs when the frequency offset between the reference and the offset laser, Δf, does not match the clk_{90} frequency (i.e. $f_{clk90} \neq 2\Delta f$), the I' and Q' outputs are quadrature square waves whose frequency is error frequency (Fig. 29) . Because the PFD output is formed by forming the XOR product of these signals after introducing a relative delay tau, the PFD output has a DC component varying as $\sin(2\pi\Delta f\tau)$ (Eq. 4). This DC signal forces the RF and LO lasers into frequency synchronization at the offset frequency f_{clk90}, i.e. forces the loop into lock. The digital frequency-detector gain is independent of all optical or electronic IC parameters, except that of the delay line τ, and hence is well controlled in the presence of normal optical and IC process parameter variations.

All of the in-cell and external transmission lines were individually EM

modeled. Fig. 4a shows the in-cell lines which are not terminated due to their lumped behavior ($\sim 30\,\mu m$). However, both of them introduce capacitive and inductive parasitic loading with a delay and these effects must be taken into account for a precise simulation of the entire system.

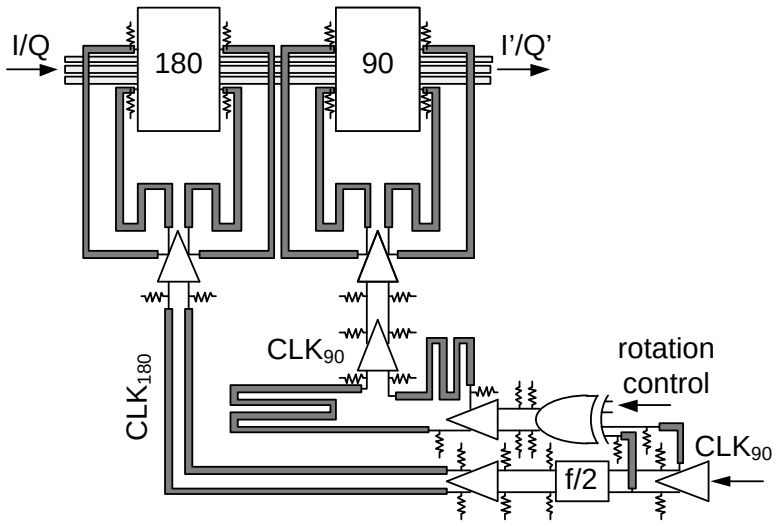


Fig. 30: Clock distribution diagram.

The clock distribution network (Fig. 30) is the most critical part in terms of speed and timing precision. After the microwave offset reference has been split into $180°$ and $90°$ clocks, it must arrive in a synchronized fashion to both of the $180°$ and $90°$ rotation blocks. Each clock signal and its corresponding complementary must arrive simultaneously to all of the four ports at each rotation block (Fig. 30). In addition, clk_{90} must be delayed behind clk_{180} exactly the amount of time takes for the I/Q signal to pass the $180°$ rotation block and reach the $90°$ rotation block. This ensures synchronized operation of both of the rotation blocks on the same I/Q state. The delay was tuned by adjusting the line lengths as well as using buffer stacking. The clock network was implemented on M2, while the signal lines are mainly on M1. To maintain a symmetrical wiring structure and minimize the crossovers, the methodology

shown in Fig. 5b was used for the final clock splitting. The IC demonstrates a total delay of $100\,ps$, reducing the limitation on wideband loops design. Delays achieved by hybrid mixers and phase detectors are typically longer [45].

5.4 Measurement and Characterization

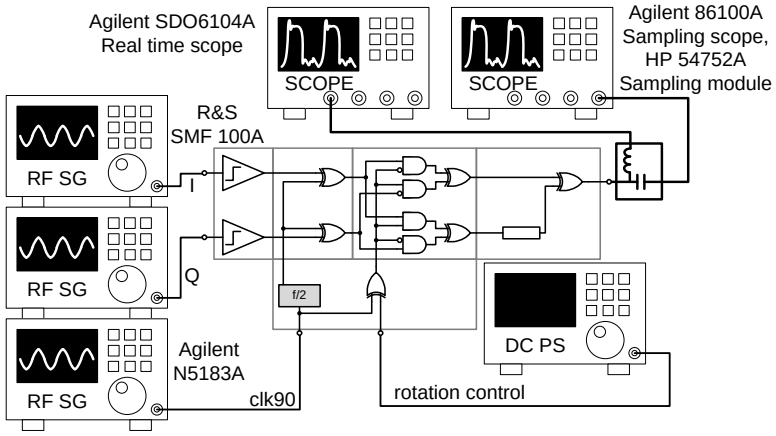


Fig. 31: SSB mixer measurement setup.

The integrated SSB mixer chip was measured for phase and frequency detection. To separate the output's average component from the time varying component a bias-tee was used (Fig. 31). The average component was inspected using an Agilent SDO6104A real time oscilloscope with a sampling rate of $4\,GSa/s$, while the time varying component using an Agilent 86100A sampling oscilloscope with a $50\,GHz$ HP 54752A sampling module. The optical I/Q signals were emulated by two R&S SMF 100A synchronized microwave synthesizers and the clk_{90} signal was supplied by a third, Agilent N5183A synthesizer. The input power was set to $-4\,dBm$ for both the I/Q input and clk_{90}. Signals were delivered on-wafer using microwave wafer probes. The IC

was biased by a negative power supply of $-3.8\,V$ and the overall DC power was $5.3\,W$. The IC photo is shown in Fig. 32 and the total area is $1.8\,mm^2$.

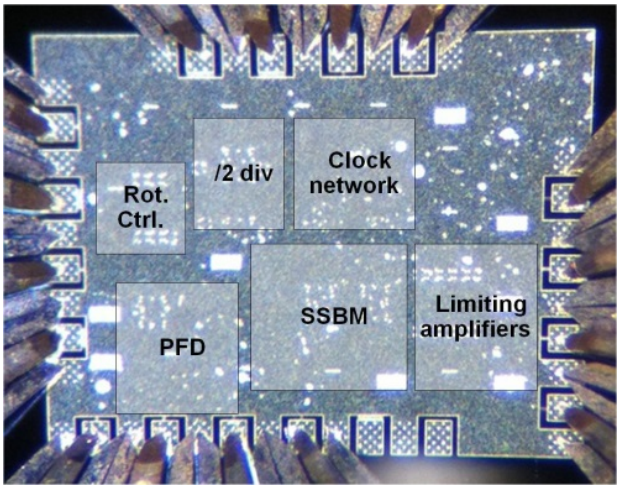


Fig. 32: IC chip image.

The experimental and simulation results are shown in Fig. 33. In Fig. 33a, the phase-frequency difference detector output is plotted as a function of phase difference with the emulated I/Q photocurrent signals set at $15\ (20)\,GHz$ and with f_{clk90} set at $30\ (40)\,GHz$, i.e. with the system operating in phase-detection mode. The phase error signal varies $\pm 300\,mV$ at $15\,GHz$ offset and $\pm 120\,mV$ at $20\,GHz$ offset as the phase is varied through $360°$. This indicates proper operation of the phase detector for frequency offsets as large as $\pm 20\,GHz$. The phase detection characteristic demonstrates periodicity of $180°$, forming two stable points for the loop to lock; a property enables the system to lock on a BPSK modulated signal, thus potentially turning the system into a WDM selectable channel receiver. A phase-detection characteristic forms a triangle wave with K_{PD} independent on inputs photocurrents. Such phase-detection behavior results from a phase error measure between the I/Q signal and the offset signal, rather than the actual phase between the two lasers; a phase error

changing the SSB mixer output duty-cycle only.

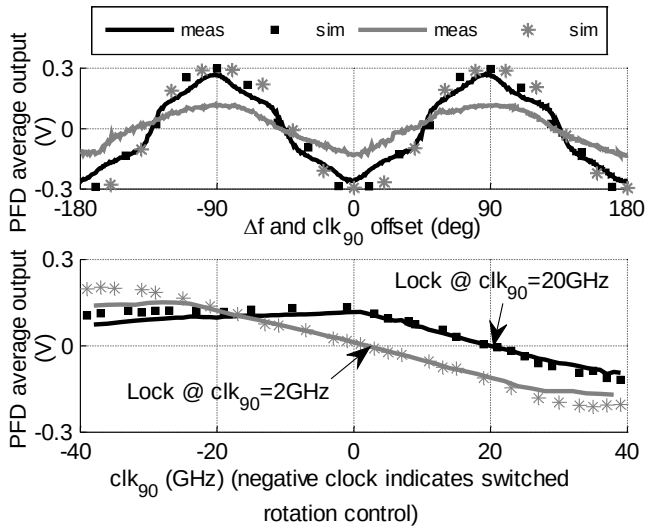


Fig. 33: PFD phase, frequency detection measurements. a) phase detection characteristic, measurement vs. simulation for $\Delta f = 20\ GHz$, $f_{clk90} = 40\ GHz$ *(grey) and for* $\Delta f = 15\ GHz$, $f_{clk90} = 30\ GHz$ *(black). b) frequency detection characteristic, measurement vs. simulation for* $\Delta f = 10\ GHz$ *and* $\Delta f = 1\ GHz$.

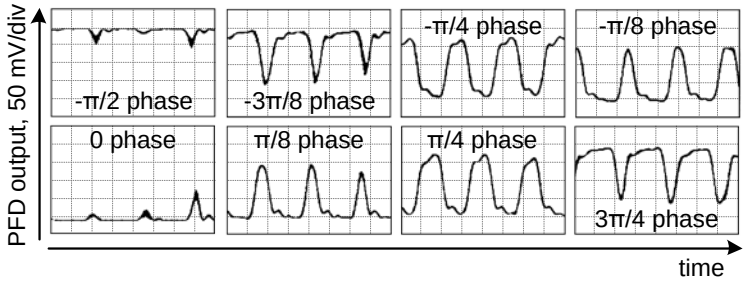


Fig. 34: PFD OUT measured waveforms in phase detection mode for $\Delta f = 2\ GHz$ *and* $f_{clk90} = 4\ GHz$.

In Fig. 33b, the PFD output is measured at laser offset frequencies of $\Delta f = 1$ and $10\ GHz$, by adjusting the SSB mixer LO frequency f_{clk90}. This measured the PFD characteristic in frequency detection mode. The frequency detection characteristic shows frequency error detection over a $\pm 40\ GHz$ range, with zero

frequency detector output when, as designed, the laser offset frequency is equal to $f_{clk90}/2$.

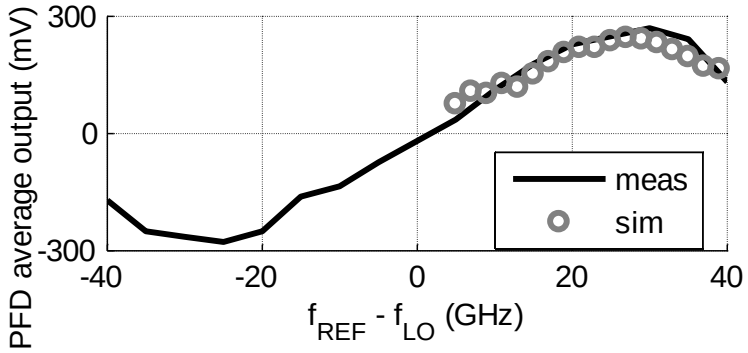


Fig. 35: PFD stand-alone frequency detection response, measurements vs. simulation.

The PFD output time waveforms in phase detection mode, as a function of phase offset, for $\Delta f = 2\,GHz$ and $f_{clk90} = 4\,GHz$ are presented in Fig. 34. The output waveform duty-cycle varies in a linear fashion as a function of phase offset, forming a triangle characteristic shown in Fig. 33. The $\pm 20\,GHz$ offset limit for phase detection operation might be explained by the quadrupled frequency beat note, produced at the output of the PFD at a phase detection mode (Fig. 34), pushing the gates to their speed limit (i.e. $80\,GHz$).

Stand-alone PFD measurements in frequency detection mode were also performed for $\pm 40\,GHz$ offset I/Q inputs. Fig. 35 demonstrates the measured triangular wave behavior, with a $\pm 50\,GHz$ period when extrapolated. Due to the symmetry of the circuit, the simulation data covers only the half of the region whether the measurements cover the entire region to verify the proper functionality. The $\pm 50\,GHz$ period is achieved by the $10\,ps$ delay line: $\sin(2\pi\Delta f\tau)$, Eq. 4. Modifying the delay line length will result in a trade-off between the K_{FD} magnitude in the linear mode and the frequency acquisition

range. The K_{FD} value and the triangular wave behavior are similar to Fig. 33b, only that the zero crossing point is shifted to the origin as expected for a PFD stand alone.

The next, $250\,nm$, InP HBT technology node allows design of frequency dividers up to $204\,GHz$ [46] and faster digital logic [27, 47, 48]. In complex ICs, however, the maximum clock rate might also be limited by fan-in, fan-out, gates delay or complex interconnects. By implementing the SSB mixer using the suggested technology it is possible to achieve clock rates of around $80\sim100\,GHz$ for $40\sim50\,GHz$ offset locking to meet the modern WDM standards.

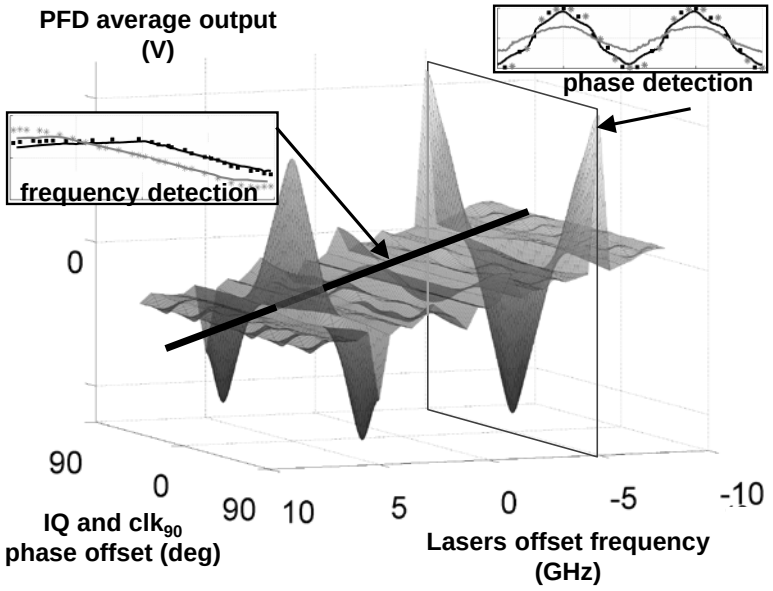


Fig. 36: Numerical PFD simulation for simultaneous phase and frequency detection modes. The offset clock, f_{clk90}, was set to $-10\,GHz$ *while the laser offset was swept over various phases and frequencies.*

A combined phase-frequency characteristic was also numerically generated using a behavioral model, with $f_{clk90} = -10\,GHz$ (the negative sign denotes a

rotation control bit 'zero' value) - Fig. 36. The linear frequency detection characteristic crosses zero at $\Delta f = -5\,GHz$, where the frequency locking occurs. At this point the loop switches to a phase detection mode characterized by a triangle function. Yet the plot suggests another phase detection mode for $\Delta f = +5\,GHz$ as well. This parasitic phenomenon occurs due to the digital (vs. linear) nature of the mixer; however since the frequency detection curve does not cross zero at this offset frequency a lock cannot occur, as was also shown experimentally [19].

As in the phase-lock state the IC output produces an output beat-note with f_{clk90} frequency (Fig. 28), any attempts to perform lock on frequency offsets lower than the loop bandwidth (f_{PLL}) will bring the loop to track the output beat-note, driving the system into a direct laser modulation rather than locking. This behavior imposes a limitation on the lower limit of the frequency offsets range to be $\sim 2f_{PLL}$.

5.5 System experiment

A system experiment comprising the reported SSB mixer IC was carried out by M.Lu et al. and was reported in [19].

The OPLL was integrated on a $10x10\,mm^2$ AlN carrier substrate. The system, Fig. 37, includes an InP photonic IC [20], the SSB mixer PFD IC described in this work and an external, $500\,MHz$ loop bandwidth, feed-forward-compensated op-amp loop filter [30]. The photonic IC contains a tunable SG-DBR laser, an optical 90 degree hybrid and four photodiodes for delivering a differential I/Q components of the lasers beat note.

The reference laser was provided to the photonic IC by an Agilent 8164B Lightwave Measurement System featuring a $100\,kHz$ linewidth, while the offset frequency, clk_{90}, was set by an Agilent E8257D microwave signal generator. The local SG-DBR laser was coupled out and externally mixed with the reference laser for monitoring purposes. The linewidth of an unlocked SG-DBR laser was above $100\,MHz$. The overall optical spectrum was inspected by an HP 70004A optical spectrum analyzer to verify a single side-band locking nature, while the locked laser linewidth was measured by inspecting the mixed beat note using the R&S FSU spectrum analyzer.

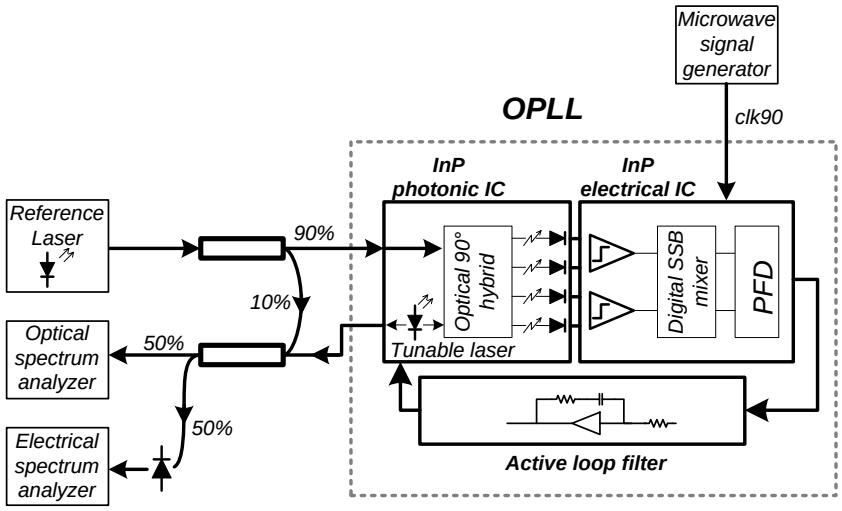


Fig. 37: Simplified offset locking experiment setup. (M.Lu et al. [19]*).*

The integrated SG-DBR laser was successfully phase locked to the reference with offsets ranging from $-9\,GHz$ to $+7.5\,GHz$ (Fig. 38). The offset locking sign was set by applying proper rotation control signal and the system kept lock while the RF offset frequency (clk_{90}) was gradually swept both in the negative and positive ranges. To confirm the single side-band fashion of locking, the optical spectrum was measured to compare the reference and the local laser wavelengths (Fig. 39). It was impossible to lock with frequency offsets as low as the loop bandwidth since the low frequency beat note provided by the PFD

cannot be integrated.

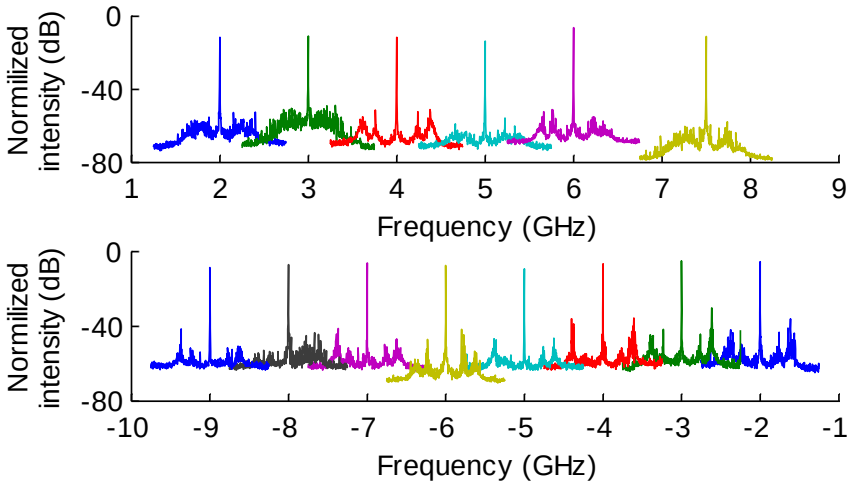


Fig. 38: ESA image of the two lasers beat note when phase locked with various frequency offsets (M.Lu et al. [19]*).*

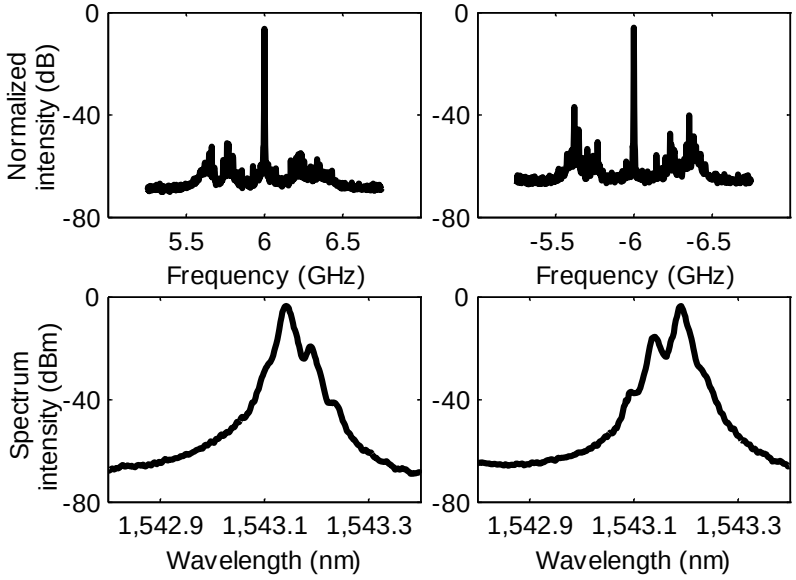


Fig. 39: Left: Beat note spectrum of two lasers (top) and optical spectrum (bottom) when phase locked with $+6\ GHz$ *offset. Right: Beat note spectrum of two lasers (top) and optical spectrum (bottom) when phase locked with* $-6\ GHz$ *offset. The reference laser has the higher power. Measured with* $5\ kHz$ *resolution bandwidth (M.Lu et al.* [19]*).*

The phase noise of the OPLL includes contributions from the RF source, the EIC, and the optical system (laser open loop noise divided by the loop transmission). Recent system demonstrations exhibit $\pm 25\,GHz$ record offset locking [49].

6. InP HBT Optical Coherent QPSK Receiver

The $100\,GBaud/s$ QPSK receiver is based on the BPSK receiver concept of using multi stable-states PFD (Fig. 40). In case of a phase detection mode, the product of $I \cdot Q \cdot (I+Q) \cdot (I-Q)$, implemented in the circuit, provides a $90°$ period phase detection characteristics to guarantee four stable points (blue points, Fig. 41) thus making the loop insensitive to a modulated data. The τ delay line provides a frequency detection characteristic similar to the BPSK receiver PFD. The linear front end receiver features an AGC loop to avoid signal distortion for $0.2{\sim}1\,mA$ input photocurrents.

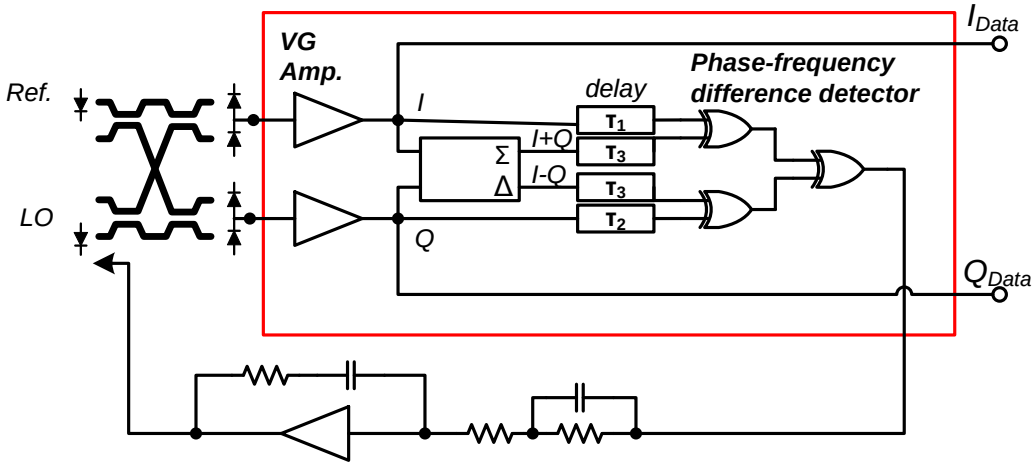


Fig. 40: QPSK receiver block diagram (red frame)

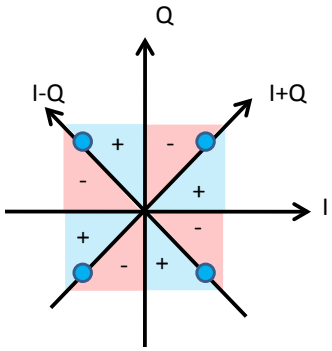


Fig. 41: Phase detection operation diagram.

6.1 Theory and Design

Similar to the BPSK receiver concept, the QPSK receiver comprises two front ends (for both I and Q arms) and a PFD (Fig. 40). However, additional conceptual differences must be considered.

In order to phase lock on a QPSK modulated data, the phase detection characteristics requires four stable states. This property is achieved by multiplying $I \cdot Q \cdot (I+Q) \cdot (I-Q)$. However, in order to implement the functionality of recovering the frequency detuning as well, four delay lines are required: τ_1 for I, τ_2 for Q, τ_3 for I+Q and τ_4 for I-Q (four lines in the most general form) Fig. 40, compared to a single delay line in the BPSK PFD. Developing the expression for $PFD_{out} = I(t-\tau_1) \cdot Q(t-\tau_2) \cdot [I+Q](t-\tau_3) \cdot [I-Q](t-\tau_4)$ one obtains two main components: a quadrature and double frequency ($4\Delta\omega$ and $2\Delta\omega$, where $\Delta\omega$ is the frequency difference between the local and the reference lasers) components (with zero average) and a DC component. Since the loop filter averages the output of the PFD, only the non-zero average level, i.e. the DC, contributes to the frequency detection response -

Eq. 10.

$$\overline{PFD_{out}} = \overline{I(t-\tau_1)\cdot Q(t-\tau_2)\cdot [I+Q](t-\tau_3)\cdot [I-Q](t-\tau_4)} = \sin(\Delta\omega[-(\tau_1+\tau_2)+(\tau_3+\tau_4)]) + \cos(\Delta\omega[-(\tau_1-\tau_2)-(\tau_3-\tau_4)]) - \cos(\Delta\omega[-(\tau_1-\tau_2)+(\tau_3-\tau_4)]) \quad \textit{Eq. 10}$$

The frequency response, as presented in Eq. 10, is not symmetrical in respect to the origin ($\Delta\omega = 0$), thus cannot be used for locking. By setting $\tau_3 = \tau_4 \triangleq \tau$ the frequency response collapses to $\overline{PFD_{out}} = \sin(\Delta\omega[-(\tau_1+\tau_2)+(\tau_3+\tau_4)])$ – an odd function that crosses the origin. In the next step we rewrite the expression for $\overline{PFD_{out}}$ in terms of the relative delay of I and Q in respect to (I+Q) and (I-Q),i.e. $\Delta\tau_1 = \tau_1 - \tau$ and $\Delta\tau_2 = \tau_2 - \tau$ respectively, as suggested by Eq. 11:

$$\overline{PFD_{out}} = \sin(\Delta\omega[-(\tau_1+\tau_2)+(\tau_3+\tau_4)]) = \sin(\Delta\omega[-(\tau_1-\tau_3)-(\tau_2-\tau_4)]) \overset{\tau_3=\tau_4\triangleq\tau}{\cong} -\sin(\Delta\omega[\Delta\tau_1+\Delta\tau_2]) \quad \textit{Eq. 11}$$

The immediate conclusion from Eq. 11 is that the detection range in frequency detection mode is a function of $\Delta\tau_1 + \Delta\tau_2$, similar to the delay line τ in BPSK receiver. By setting $\Delta\tau_1 + \Delta\tau_2 = 10\,ps$ a detection range of $\pm 50\,GHz$ is obtained. It is now left to determine the sign of $\Delta\tau_1 + \Delta\tau_2$ and the optimal ratio between $\Delta\tau_1$ and $\Delta\tau_2$. To complete this task, one compare the PFD functionality in the phase detection mode to the frequency detection one. When operating in phase detection ($\Delta\omega = 0$), the input I and Q photocurrents are DC signals with values of $\cos(\Delta\theta)$ and $\sin(\Delta\theta)$, respectively. The PFD response to DC inputs is independent on the delay lines and yields $PFD_{out} \sim \sin(4\Delta\theta)$, with

four stable states – Fig. 42.

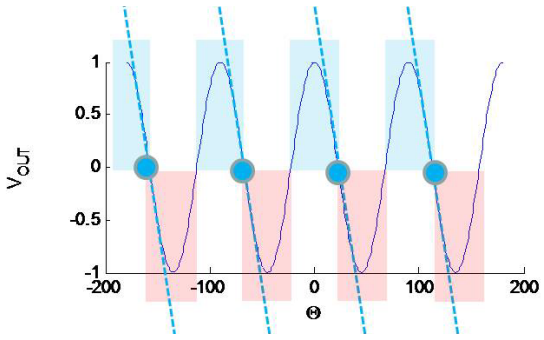


Fig. 42: A normalized PFD response in phase detection mode.

Nevertheless, in case of modulated data, given the delays are longer than a bit period T_{bit}, i.e. $T_{bit} < \Delta\tau_1, \Delta\tau_2$, the multiplication of $I \cdot Q$ by $(I+Q)\cdot(I-Q)$ will result in a multiplication of the current bit a previous bit value (which is random), resulting in a zero average. To avoid it, the bit period must be longer that the maximal delay line: $T_{bit} > \max(\Delta\tau_1, \Delta\tau_2)$. The effect of the delays on phase detection is visualized on Fig. 43. Only a product of I by Q by (I+Q) by (I-Q) of the same bit (blue zone) contributes to the phase-detection characteristics: $\sin(4\Delta\theta)$. When multiplying the values of different bits (red zone) – the result is a zero average.

Since the receiver targets a data-rate of $100\ GBaud/s$, the minimal bit period is $T_{bit} = 10\ ps$. To set $\Delta\tau_1 + \Delta\tau_2 = 10\ ps$ (for $\pm 50\ GHz$ frequency detection range), while minimizing the red zone (Fig. 43), equal delay lines of $\Delta\tau_1 = \Delta\tau_2 = 5\ ps$ are obtained.

It is now left to find the sign of $\Delta\tau_1 + \Delta\tau_2$. According to Eq. 11, the sign of $\Delta\tau_1 + \Delta\tau_2$ is responsible for the sign of K_{FD}. The control loop, eventually, is designed to provide a negative feedback for both phase and frequency detection modes. Hence, given the loop is negative in frequency-detection, the phase-detection loop will lock on phase-offsets providing K_{PD} sign equal to K_{FD}.

Sequentially, the sign of K_{FD} will determine whether the loop locks on either of the 0,90,270,360 phases or 45,135,225,315 phases. Locking on 45,135,225,315 phases will result in a constellation points of (1,1), (1,-1), (-1,1), (1,1), i.e. two levels of I and two levels of Q. This is the solution of interest (Fig. 44). On contrary, if the phase is to lock on one of the 0,90,270,360 phases, three-level eye diagram will be received. Analysis shows that $\Delta\tau_1 + \Delta\tau_2 > 0$ yields the K_{FD} with the same sign as K_{PD} at one of the 45,135,225,315 phases, Fig. 45.

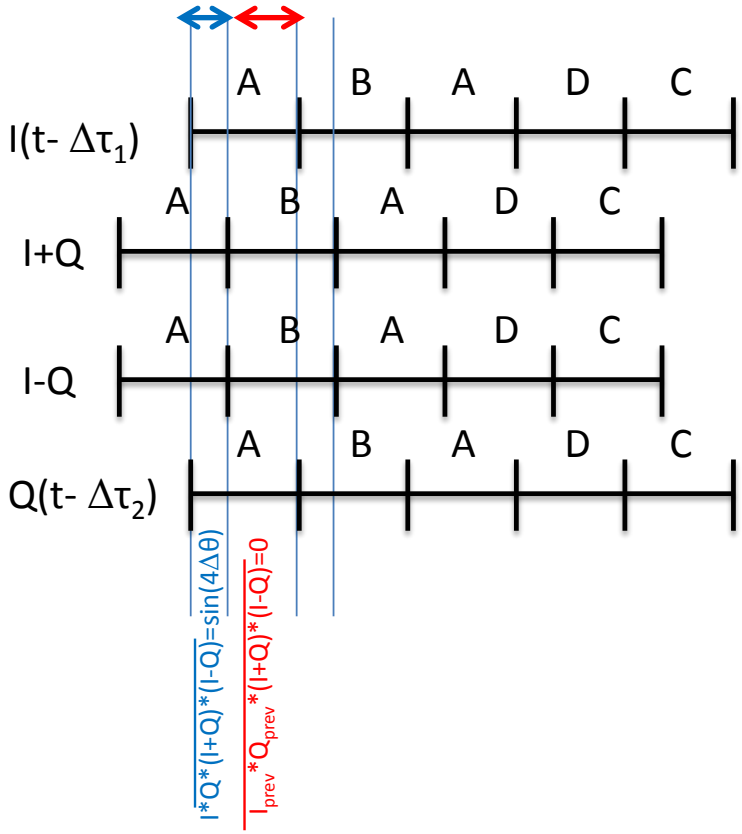


Fig. 43: Effect of the QPSK PFD delay line on phase-detection under modulated data.

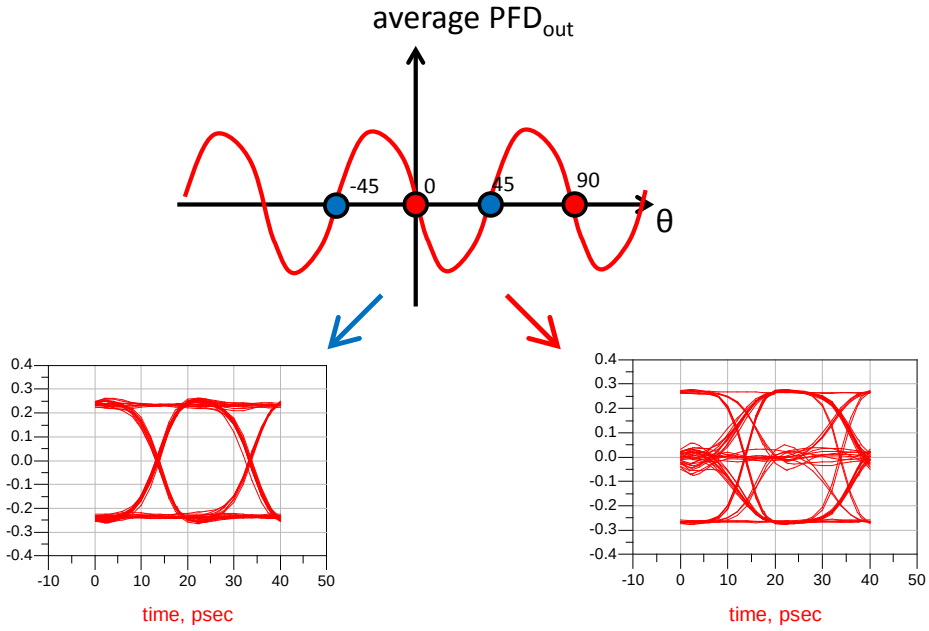


Fig. 44: (Right) Three-levels eye diagram as a result of a phase-locking on 0,90,270,360 *phases, (Left) Two-levels eye diagram as a result of a phase-locking on* 45,135,225,315 *phases.*

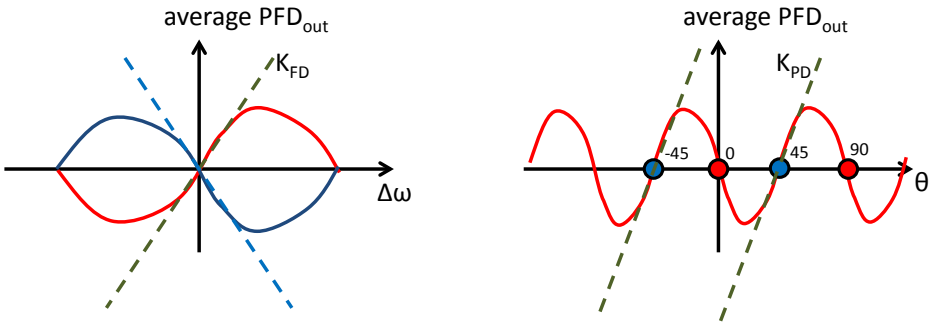


Fig. 45: Positive sign of $\Delta\tau_1 + \Delta\tau_2$ *yields the same sign for* K_{FD} *and for* K_{PD} *at* 45,135,225,315 *phases.*

6.2 Linear Front-End

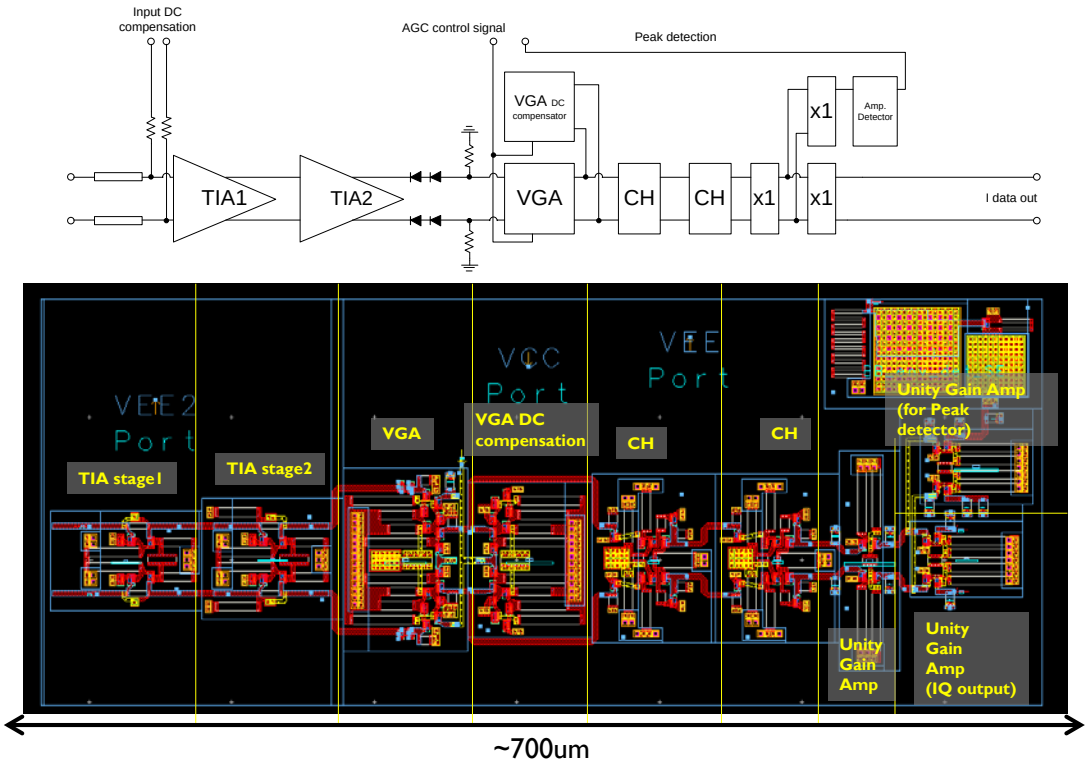


Fig. 46: Front end block diagram and layout.

For a successful phase-frequency offset recovery the I, Q, (I+Q) and (I-Q) signals must preserve their linear nature (otherwise the I+Q and I-Q information vanishes). Hence, no limiting ECL stages were used. Instead, the linear front end comprised of two stage linear resistive feedback amplifier (TIA1 and TIA2) (Fig. 46) with a total differential gain of 16 dB each and BW of $107\,GHz$, variable gain amplifier (VGA) to control the liniarity for a wide range of input photocurrent, and two high bandwidth Cherry-Hooper amplifiers (CHA). Next, the signal is split using ultra-high bandwidth unity-gain degenerated ECL cells to provide the output signal to both the peak-detector (for locking an external AGC loop to ensure linear operation), the PFD and the

data output port.

The TIAs require a separate bias voltage of -5.2 V (V_{EE2}), next, the signal is shifted to a standard ECL voltage levels ($0\sim-300\,mV$) where the blocks are fed by a $-3.8\,V$ supply. The input DC level is $-2\,V$ in order to bias the photodiodes. All the interconnections are implemented by a $50\,\Omega$ inverse microstrips on M1 level and EM modeled together with other passive components. M3 was used as a ground plane.

The maximal transimpedance gain of the each front end is $70\,dB\Omega$ with $70\,GHz$ bandwidth, suitable for $100\,GBaud/s$ data rates. Next sections will describe each block individually.

6.2.1 A 107 GHz 55 dBΩ InP Broadband Transimpedance Amplifier

6.2.1.1 Background

To support coherent optical communication while supporting complex modulation formats and/or multiple subcarriers, a wideband *linear* electrical front-end must be introduced. Linearity, high input dynamic range, wideband matching, low noise and a good interface with the optical IC are the key properties of such a front-end.

Recently reported broadband front-ends can be divided into two main groups: limiting and non-limiting (linear). The limiting front ends usually employ the $g_m - Z_t$ (Cherry-Hooper) topology [50]. The g_m stage limits the signal while keeping the transimpedance stage in linear operation, thus maintaining the values of the input/output impedances. Gain-bandwidth products of $g_m - Z_t$

amplifiers are poorer than those of linear differential amplifiers. Limiting amplifiers serve as combined gain blocks and decision circuits in BPSK and QPSK receivers.

In a given technology, non-limiting, linear amplifiers can deliver a higher bandwidth than limiting amplifiers. Linear amplifiers are necessary given more complex modulation formats (multiple RF subcarriers, 16QAM, etc.). A $3\,dB$ bandwidth of $102\,GHz$ is reported in [51].

The linear transimpedance amplifier (TIA) reported in this work comprises two-stage linear differential resistive-feedback amplifier (RFA) biased by a negative, $-5.2\,V$, source. Due to a self-biased $-2\,V$ input voltage, the TIA directly interfaces to a PIC [44], reverse-biasing the photodiodes by $-2\,V$. Diodes level-shift the output to $-450\,mV$, permitting $50\,\Omega$ terminated connections to other linear circuits, such as Gilbert-cell mixers (GCM) for frequency conversion. The output interface is also compatible with ECL. The TIA demonstrates $107\,GHz$ $3\,dB$ bandwidth, $16\,dB$ differential gain, $-1\,dBm$ output at $1\,dB$ gain compression, $30\,ps$ group delay, and $675\,GHz$ gain-bandwidth product with a power consumption of $365\,mW$. The gain-bandwidth is particularly high given the mature status of the $0.5\,\mu m$ InP HBT IC technology employed.

6.2.1.2 Resistive-Feedback amplifier

In RFA (Fig. 47), emitter/source degeneration is added to a single-ended or differential stage, producing a stage having transconductance $g_m = (kT/qI + R_E/2)^{-1}$ (Fig. 48a). The transconductance stage has high input and output impedances; adding a feedback resistor of value $R_f = (1 - A_v)Z_0$ and selecting the stage transconductance according to $g_m = (1 - A_v)Z_0^{-1}$ results in a

gain block of the desired gain $A_v = V_{out}/V_{in}$ and having input and output impedances $R_{in} = R_{out} = Z_0$. Both gain-bandwidth and noise are better than that of simple resistively-loaded amplifiers.

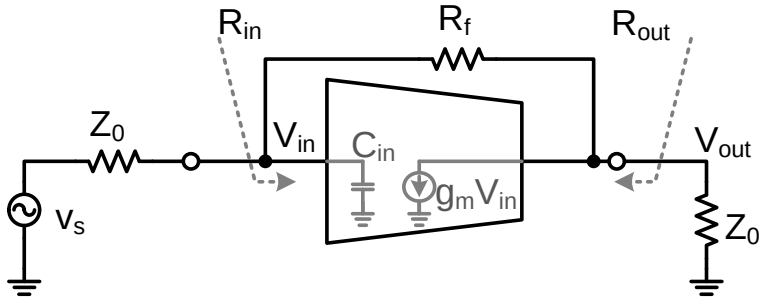


Fig. 47: Resistive feedback g_m stage driven loaded by a Z_0 impedance and driven by a Z_0 source.

6.2.1.3 Circuit Design

The g_m stage is a differential pair having emitter-followers which both buffer the stage input capacitance and increase the V_{CE} of the common-emitter transistors [52], *both effects* benefiting bandwidth. With extrinsic transconductance constrained to $g_m = (1 - A_v)Z_0^{-1}$ and with emitter current density selected for peak f_t and f_{max}, the emitter junction areas of Q_1 and Q_3 are the only free design variables and are set to $2.5\ \mu m^2$ each. Increasing Q_1 and Q_3 junction areas increases capacitances and g_m but reduces parasitic resistances. Optimization by hand calculation minimizes the total $\sum R_i C_j$ first-order time constant. C_f adjusts damping.

Fig. 48 shows a full schematic and Fig. 48a a single stage in floor-plan orientation. The IC draws $70\ mA$ from a $-5.2V$ supply. All transistors are biased at the optimum f_t, f_{max} current density of $3{\sim}4\ mA/\mu m^2$. Transistors Q_{1-2} form the emitter follower stage of the Darlington with $R_1 = 300\ \Omega$. Transistors Q_3

are part of the differential degenerated common emitter stage with $R_E = 10\ \Omega$. The differential pair current tail was implemented using resistors ($R_2 = 165\ \Omega$), instead of current mirrors as this gives lower noise and less capacitance. The feedback resistor R_f is $150\ \Omega$.

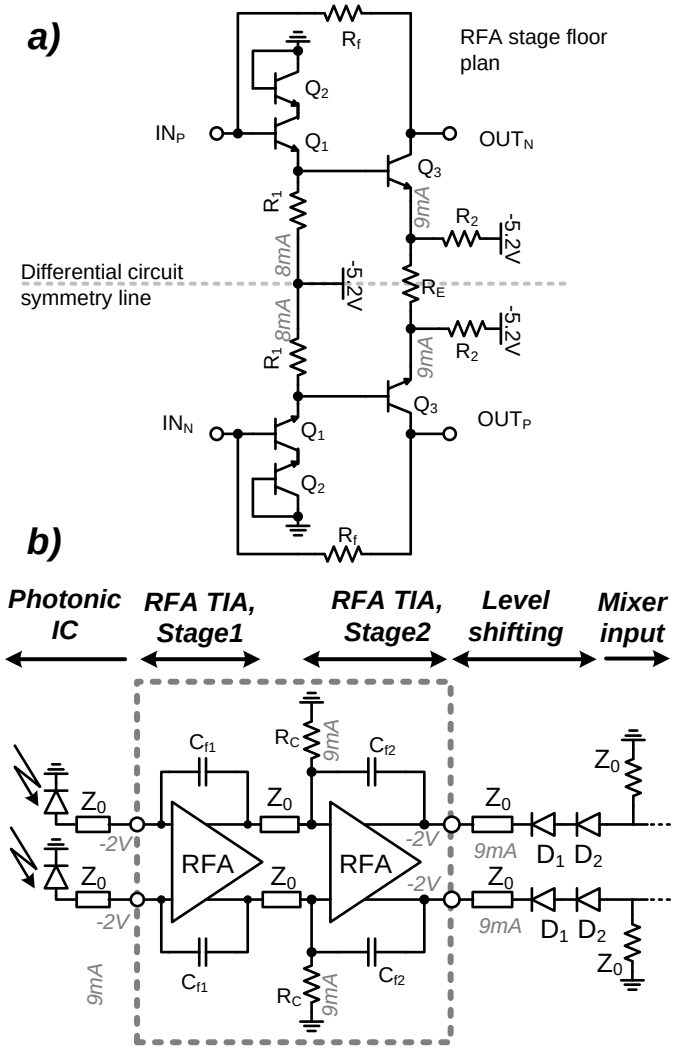


Fig. 48: RFA full schematics. a) single stage RFA floor plan schematic, b) full two stage RFA TIA block diagram (dashed frame) and its integration into a receiver front-end.

The grey frame on Fig. 48b presents the two-stage full RFA within a receiver front end. The stages are directly cascaded. Via DC negative feedback through the resistances R_f of stage-1, the voltage drop across $R_C = 230\ \Omega$, establishes a -

$2\,V$ DC input bias voltage which biases the input photodiodes. The large DC drop also permits R_C to be large, minimizing its loading of stage 1. The stage-2 DC output current, together with the level-shift diodes and the $50\,\Omega$ loads, establishes the stage-2 collector DC bias at $-2\,V$ and the amplifier DC output at $-450\,mV$.

6.2.1.4 Layout

The IC layout was designed according to the layout methodology presented on Fig. 6b. Signal lines are metal 1 and metal 2 inverted microstrip interconnects with a metal 3 ground plane. This allows controlled impedances on *all* IC interconnects. Metal 4 is the power grid. This avoids cross-over capacitances between signal lines and power conductors, improving signal integrity and simplifying layout. Inverted microstrip allows narrow line spacing (approximately two times the line-to-ground distance, i.e. $6\text{-}10\,\mu m$), and a continuous unbroken ground-plane, maintaining ground integrity and avoiding ground-bounce.

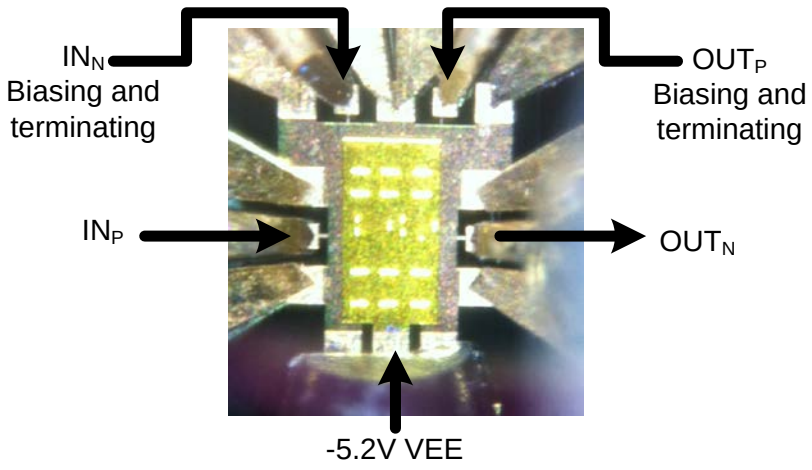


Fig. 49: RFA die photo.

A small overlap capacitance arises wherever M1 and M2 transmission-lines (with an M3 ground plane) cross. At the expense of added via inductance, this crossover capacitance can be avoided by transitioning one line in the crossover region to an M4 microstrip line with an M3 ground-plane. Though used in the larger (WDM) receiver ICs, this technique was not necessary in the amplifier itself.

All transmission-lines and passive components were individually EM-modeled by Agilent Momentum. The RFA test layout, Fig. 49, was designed in a single-ended fashion to permit measurements beyond $67\,GHz$. The remaining two ports are connected to bias-Tees and RF terminations. The differential layout is fully symmetric, following the floor plan of Fig. 48a, and interconnects are kept short. The active IC area is $220 \times 80\,\mu m^2$.

6.2.1.5 Measurement Results

Measurements include small-signal S-parameters, gain compression, and $30 - 44\,Gb/s$ eye patterns.

Small-signal S-parameters

The S-parameter measurements were performed using an Agilent PNA-X N5257A for the $1\text{-}50\,GHz$ band and OML millimeter wave extenders, controlled by an Agilent N5257A PNA-X $50\text{-}110\,GHz$, for the $50\text{-}75\,GHz$ and $75\text{-}110\,GHz$ bands. The input power was $-24\,dBm$. Given the extended frequency range, only single-ended measurements were feasible. The remaining two ports were terminated in $50\,\Omega$ connected through $65\,GHz$ bias tees. Reflections from these bias tees and terminations are not corrected for in the two-port calibration, and produce ripple in the S-parameter data.

The low frequency single-ended gain is $9.8\,dB$ with $2\,dB$ gain ripple (Fig. 50). Adding $6\,dB$ for a differential operation results in a $16\,dB$ differential gain – a $55\,dB\Omega$ equivalent, with $107\,GHz$ bandwidth. The gain-bandwidth product of the IC is $675\,GHz$. The measured group delay is $30\,ps$. A $-10\,dB$ input/output return loss was measured up to $80\,GHz$, increasing to $-5\,dB$ at higher frequencies. In a fully differential operation the return losses are expected to improve due to balanced operation. S-parameters were measured for $1-3\,mA$ input DC currents (to emulate photodiode DC bias currents) with less than $0.3\,dB$ observed variation in the amplifier gain.

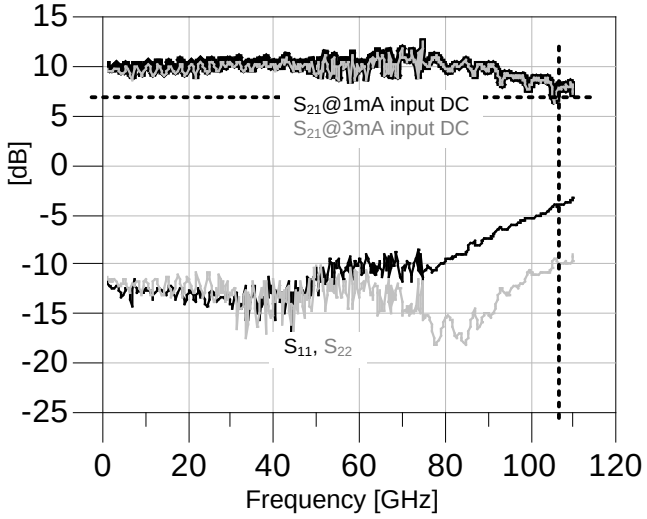


Fig. 50: Measured single-ended S_{21} and input/output insertion losses for the two-stage amplifier. Given two outputs, the differential gain should exceed the single-ended S_{21} by $6\,dB$.

Power compression and linearity

The gain compression measurements were performed using an R&S 100A $22\,GHz$ signal generator to provide the input power and R&S FSU46 spectrum analyzer for output spectral measurement. The $1\,dB$ compression was measured up to $20\,GHz$. According to Fig. 51, the maximum input power for linear

operation is -9 dBm (equivalent to 2.25 mA-amplitude input current), resulting in an output 1 dB gain compression point of -1 dBm. With a simulated input referred current noise of 44 $pA/\sqrt{Hz}$, the estimated input dynamic range, for $SNR > 10\ dB$, is 33 dB.

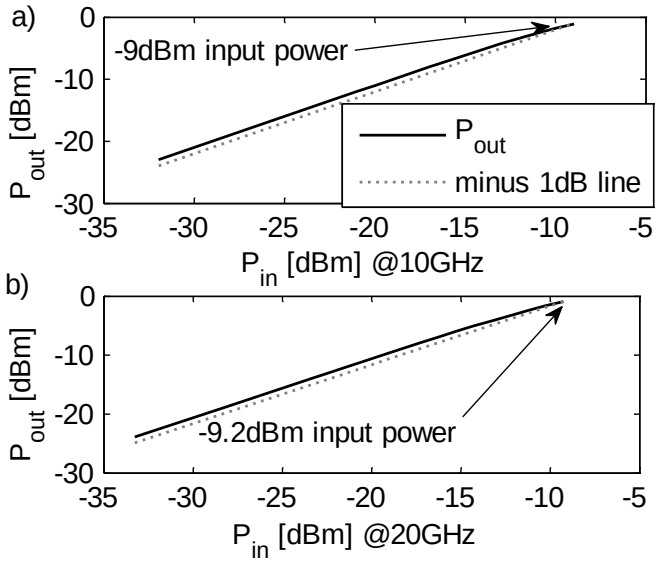


Fig. 51: P1dB measurement at a) 10 GHz input signal, b) 20 GHz input signal

Time domain measurements

While the amplifier's bandwidth should be sufficient to support even 160 Gb/s operation, equipment was available for testing only to 44 Gb/s. The data was generated by a Centellax TG1P4A $2^{31}-1$ PRBS generator with 430 mV output amplitude. This was reduced 10 dB using coaxial attenuators. The IC output signal was sampled using an Agilent DCA-X 86100D oscilloscope with an Agilent 86118A 70 GHz remote sampling head.

The measurement results, Fig. 52, demonstrate a gain of 10 dB, with peak-peak jitter addition of 2.5 ps at 44 GHz. The lack of ringing proves robust

phase margin and stable design. The displayed rise/fall times are limited by the instrumentation.

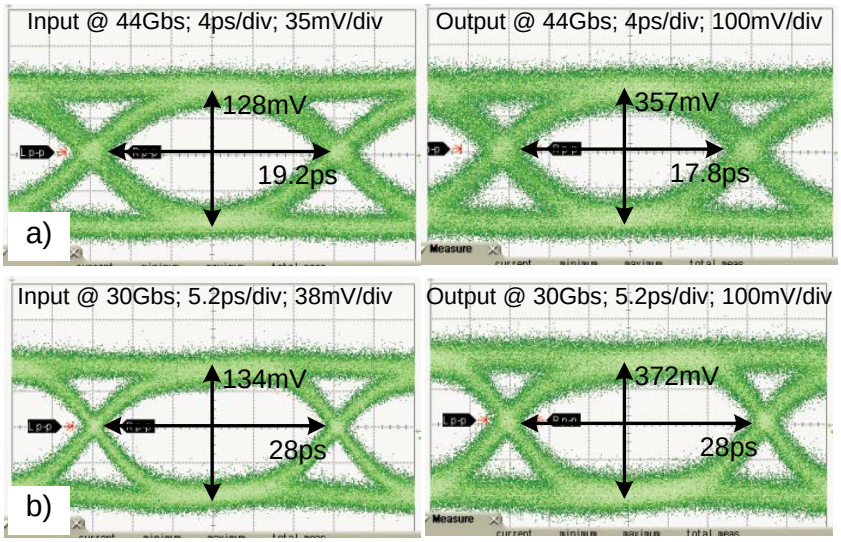


Fig. 52: Input/output eye diagram. a) $44\ Gb/s$*, input amplitude of* $128\ mV$*, b)* $30\ Gb/s$*, input amplitude of* $134\ mV$

6.2.2 VARIABLE GAIN AMPLIFIER

The VGA consists of two Gilbert cells with one operate as a variable gain amplifier while the other compensates the DC bias. As shown on Fig. 53, the top cell acts as an amplifier, with differential inputs provided to the G_m core. The control signal, V_{agc}, is provided in a single ended fashion to both of the blocks, while $V_{agc,bar}$ is an average DC value of V_{agc}. This way the opposite operation of the DC-compensation Gilbert cell corrects the skewed bias point of the gain cell. To boost the stage bandwidth, a degeneration resister in parallel to a peaking capacitor was added to the G_m stage.

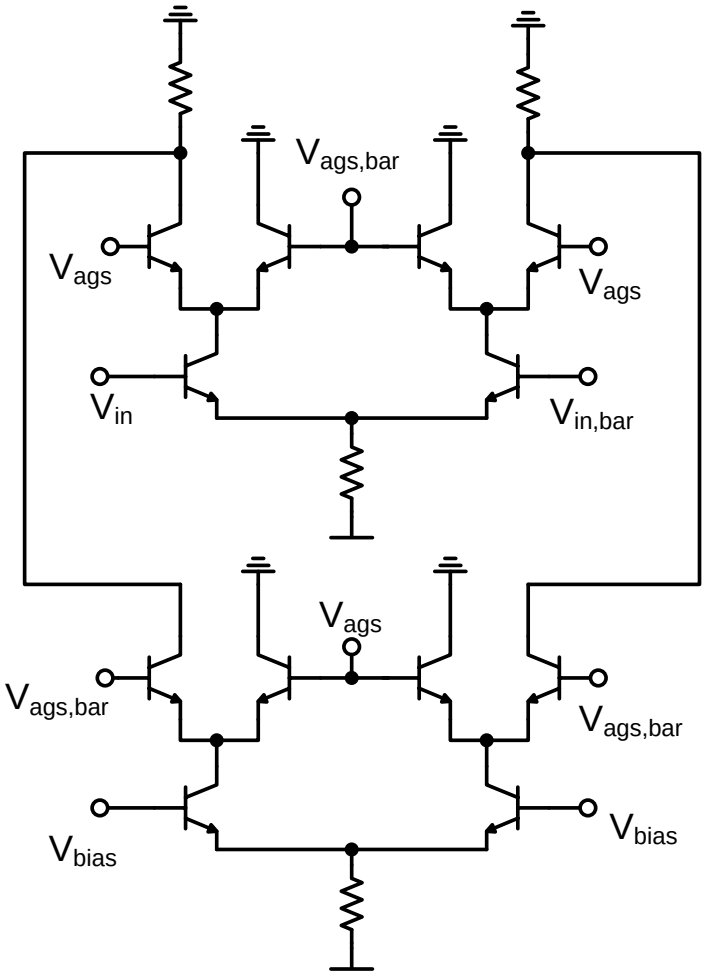


Fig. 53: Variable gain amplifier schematics

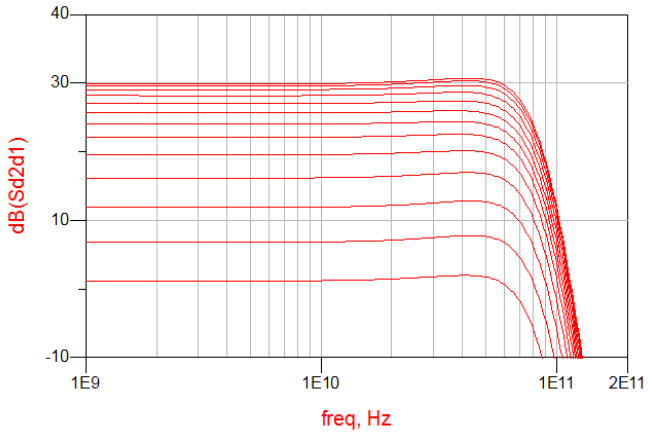


Fig. 54: Simulated front-end differential gain

Fig. 53 presents the small signal gain of the complete front-end as with the

VGA control voltage varies between $-120\sim+120\,mV$.

6.2.3 PEAK DETECTION

The heart of the peak detector is the capacitor C, charged by the transistor and discharged by the DC current source I_0. At the steady state, When the emitter current of the transistor is I_0 as well, V_{out} is proportional to the input amplitude. The right hand of the schematics (Fig. 55) provides only the DC level compensation, $V_{out,0}$.

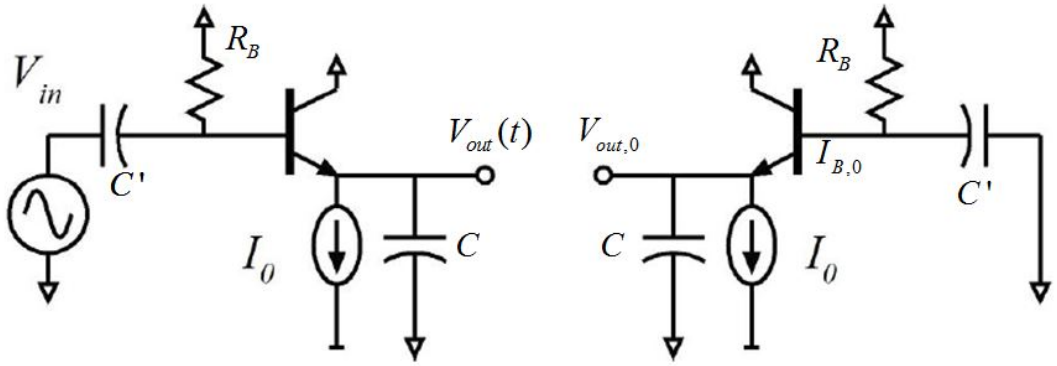


Fig. 55: Peak detector schematics.

To fully analyze the circuit operation, $V_{out,0}$ should be first calculated. The reader can easily see that $V_{out,0} = -I_{B,0} \cdot R_B - V_{BE} = -\frac{I_0 R_B}{\beta+1} - \frac{kT}{q}\ln\left(\frac{I_0}{I_S}\right) \approx -\frac{kT}{q}\ln\left(\frac{I_0}{I_S}\right)$ for low voltage drops over R_B. Here, $I_{B,0}$ is the base DC current and I_S is the reverse saturation current of the base-emitter diode. To analyze the dynamic behavior of the left half of the circuit it is assumed that the input signal, $V_{in}(t)$ is a symmetrical square wave with peak values of $\pm V_h$ and a half-period of T_B for $t > 0$, and zero for $t < 0$ (Fig. 56).

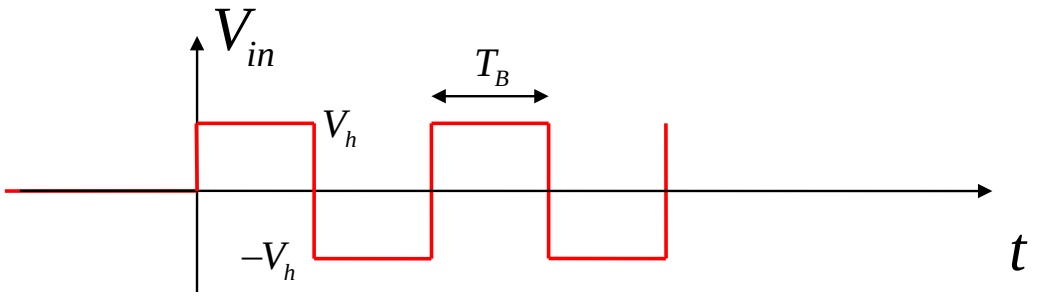


Fig. 56: An input waveform to the peak detector.

Under the assumption that the voltage drop across R_B is low enough, i.e. $V_h > I_{B,0}R_B$ and the the pole of the HPF formed by C' is lower than the square wave frequency, i.e. $2\pi C'R_B \gg T_B$, it is possible to state that the base voltage is $V_B(t) \approx V_{in}(t)$.

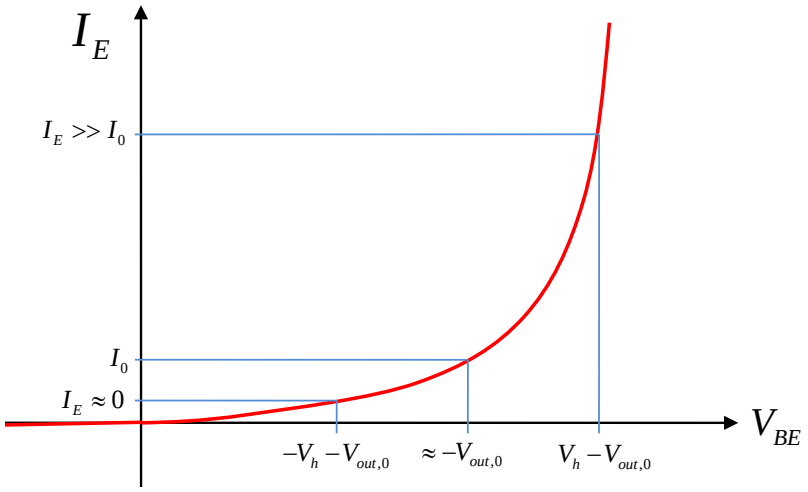


Fig. 57: The transistor emitter current for various input voltages.

Prior to the steady state mode, the circuit operates at a transient mode until stabilization, with capacitor C charging as the dominant process. At the first half of a cycle, where $V_B \approx V_{in} = V_h$, the transistor emitter current is much higher than I_0, i.e $I_E \gg I_0$, so the capacitor C is being charged by the difference current $I_{charge} = I_E - I_0 \gg I_0$. (Fig. 57). However, at the second half, with $V_B \approx V_{in} = -V_h$, the transistor is can be considered as cut-off so the capacitor is

discharged by I_0 alone: $I_{discharge} = -(I_E - I_0) \approx I_0$.

Since $I_{charge} > I_{discharge}$, the voltage drop across the capacitor C raises with each cycle. As the voltage across the capacitor C gets higher, the charging current I_E gets smaller and the process exhaust itself when $I_E|_{V_{BE}=V_h-V_{out}} = 2I_0$. At this point the capacitor C is charged by a current I_0 during the first half of period and discharged by the same current at the second half, making V_{out} to fluctuate around a constant value $V_{out,mean}$ (Fig. 59).

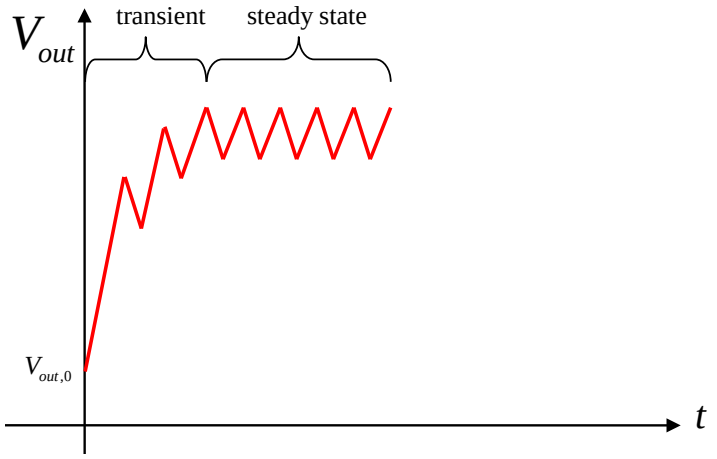


Fig. 58: Two operation modes of the peak detector – a transient mode and a steady-state mode.

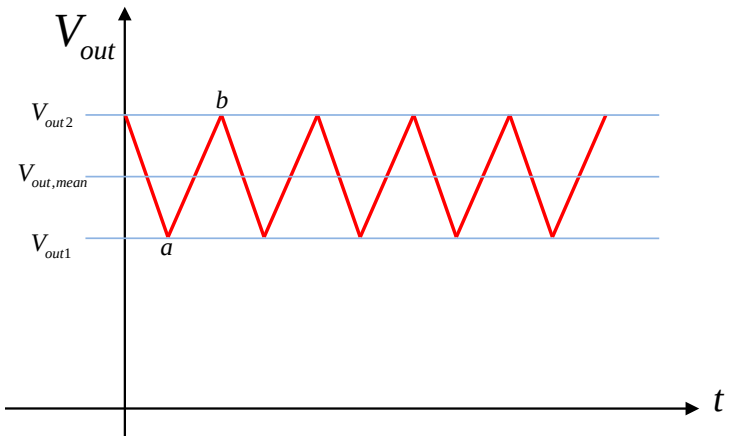


Fig. 59: Steady state

To analyze the steady-state mode one assumes that during each half cycle the capacitor C voltage experiences only slight fluctuations, not enough to impact the transistor current I_E. In this case, the capacitor C charges and discharges in a linear fashion, by current I_0. Hence, the voltage fluctuation is $V_{out2} - V_{out1} = \frac{I_0 T_B}{C}$ (Fig. 59). The assumption on constant transistor current requires $\frac{I_0 T_B}{C} \ll \frac{kT}{q}$. At point 'a', $V_{in} = V_h$ and $I_E = 2I_0$, hence $V_{BE1} = \frac{kT}{q}\ln\left(\frac{2I_0}{I_S}\right)$ and $V_{out1} = V_h - V_{BE1} = V_h - \frac{kT}{q}\ln\left(\frac{2I_0}{I_S}\right)$. On the other hand, $V_{out2} = V_{out1} + \frac{I_0 T_B}{C} = V_h - \frac{kT}{q}\ln\left(\frac{2I_0}{I_S}\right) + \frac{I_0 T_B}{C}$. Calculating $V_{out,mean}$ one obtains $V_{out,mean} = \frac{V_{out1}+V_{out2}}{2} = V_h - \frac{kT}{q}\ln\left(\frac{2I_0}{I_S}\right) + \frac{I_0 T_B}{2C} = \frac{V_{peak}}{2} - \frac{kT}{q}\ln\left(\frac{2I_0}{I_S}\right) + \frac{I_0 T_B}{2C}$.

$$
\begin{aligned}
V_{out,total} &= V_{out,mean} - V_{out,0} \\
&= \frac{V_{peak}}{2} - \frac{kT}{q}\ln\left(\frac{2I_0}{I_S}\right) + \frac{I_0 T_B}{2C} - \left(-\frac{kT}{q}\ln\left(\frac{I_0}{I_S}\right)\right) \\
&= \frac{V_{peak}}{2} + \frac{I_0 T_B}{2C} - \frac{kT}{q}\ln 2
\end{aligned}
\qquad \textit{Eq. 12}
$$

The total output voltage, including the DC compensation is given by Eq. 12 and depends on V_peak, transistor DC current I_0, capacitor C and the data frequency. The peak detection IC was designed with $C' = 500\,fF, C = 1\,pF, R_B = 1\,k\Omega$ and $I_0 = 600\,\mu A$. The IC response to various amplitude square waveforms and various frequencies is presented on Fig. 60. To design a control loop, an average value can be used around a typical point.

Simulated gain-control loop are presented on Fig. 61. For input photocurrent varies from $0.2{\sim}1.5\,mA$ peak-to-peak, the output signal envelope remains constant between $\pm 250\,mV$ – voltage levels necessary to ensure linear operation of the ECL cells. The bottom plot shows the variation of the control signal vs. input amplitude.

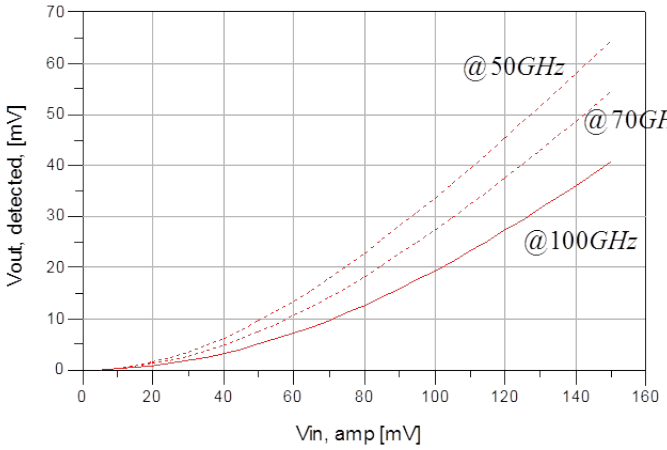
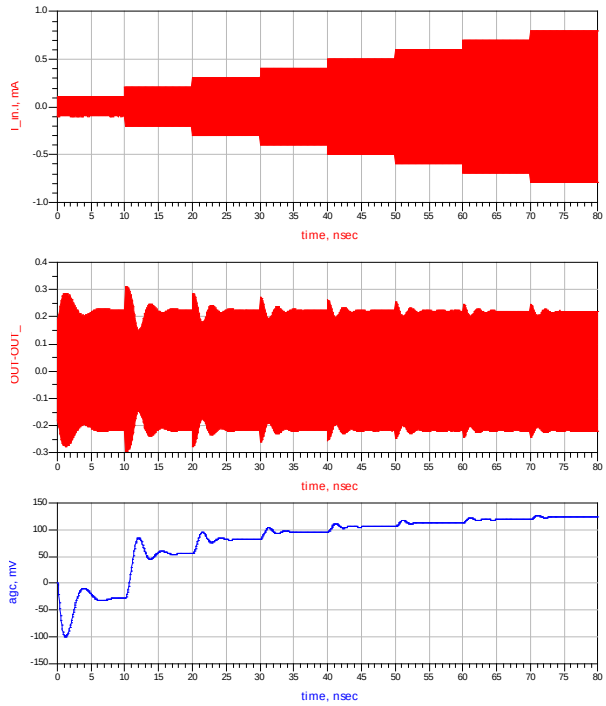


Fig. 60: Peak detector IC response to input square waveform vs. the waveform amplitude and frequency.



•Input current [mA]

•Output Voltage [V]

•AGC control signal[mV]

Fig. 61: Simulated gain-control loop response to various input current amplitudes.

6.2.4 CHERRY-HOOPER AMPLIFIER

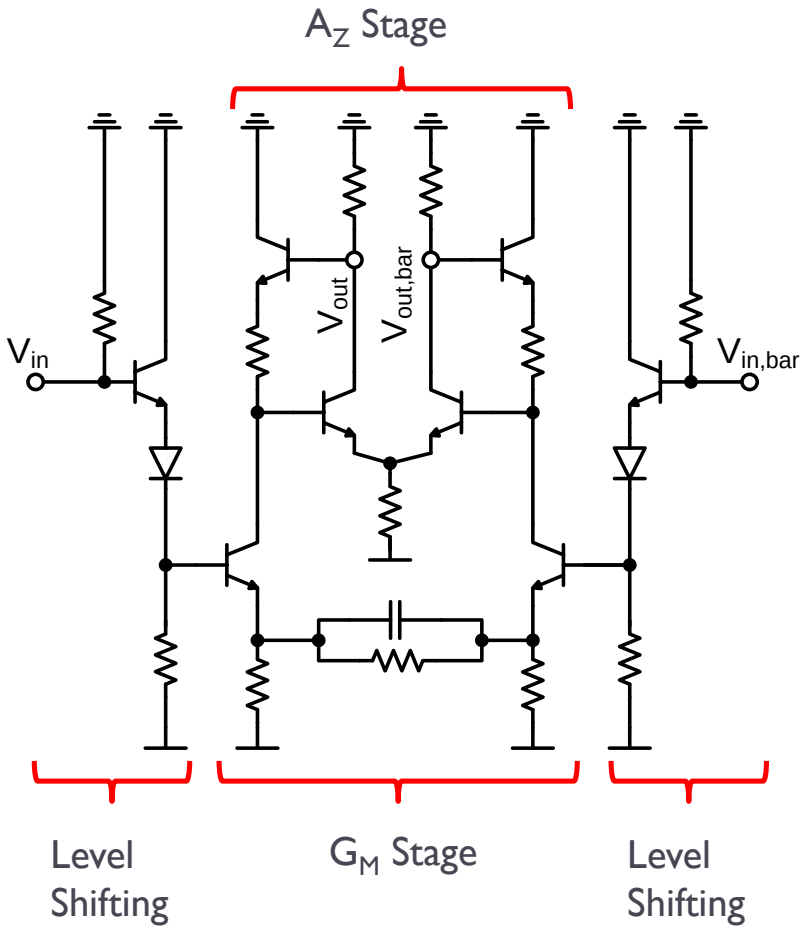


Fig. 62: Cherry-Hooper amplifier schematics.

To maximize the bandwidth while maintaining the ECL voltage levels, CHA [50, 53, 54] were used. CHA are designed by cascading G_m and Z_t cells (Fig. 62) and as the limiting behavior takes place in the G_m stage, the amplifier operates in a saturated mode over a high range of input dynamic range. Even though the CHA are targeted to operate linearly, they exhibit much higher bandwidth compared to the standard ECL cell, also due to the low input impedance and high bandwidth of the Z_t cell. To boost even more the bandwidth and the linearity of the G_m cell, a degeneration resistor in parallel to a peaking

capacitor were used.

Fig. 63 displays simulation results of the CHA cell. A linearity to almost $0.1\,V$ input voltage, with bandwidth of $87\,GHz$ is achieved. The slight peaking in the frequency response in high frequency compensates the relatively low bandwidth of the VGA.

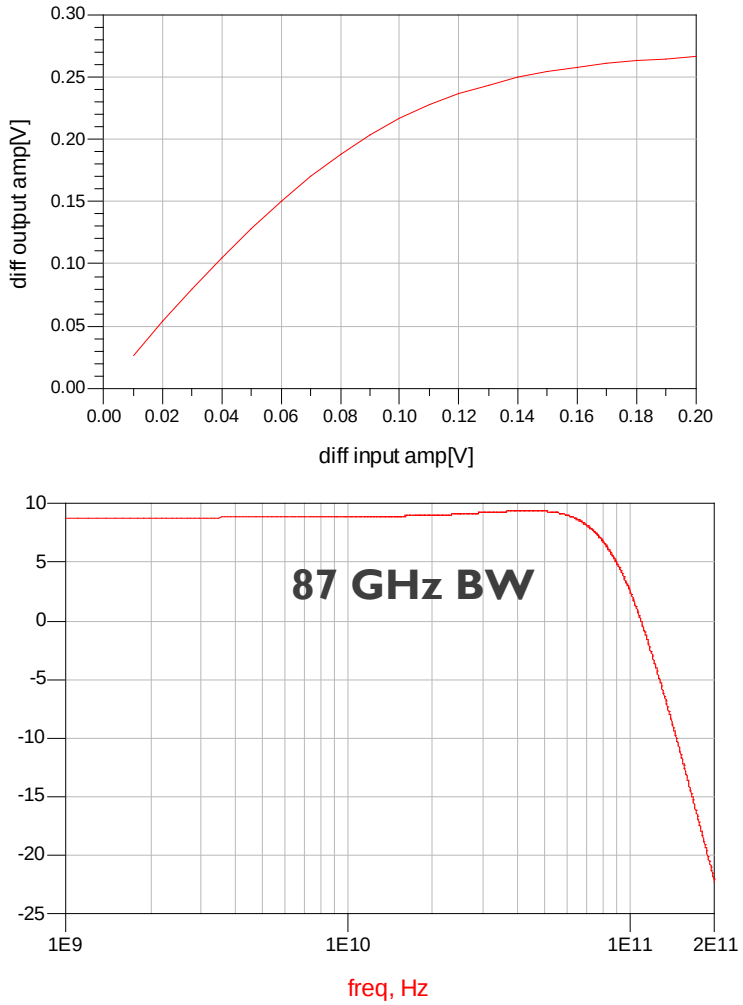


Fig. 63: Cherry-Hooper amplifier simulation results: (top) large signal linearity, (bottom) small signal frequency response.

6.3 Phase-Frequency Detector

The I+Q and I-Q signals are delivered by a fully passive addition-subtraction resistive network [55]. Setting the resistors values as shown on Fig. 64, both input and output matching to a $50\,\Omega$ differential impedance is achieved. Assuming differential signals, it can be shown that $A - C \propto I + Q$ and $D - B \propto I - Q$.

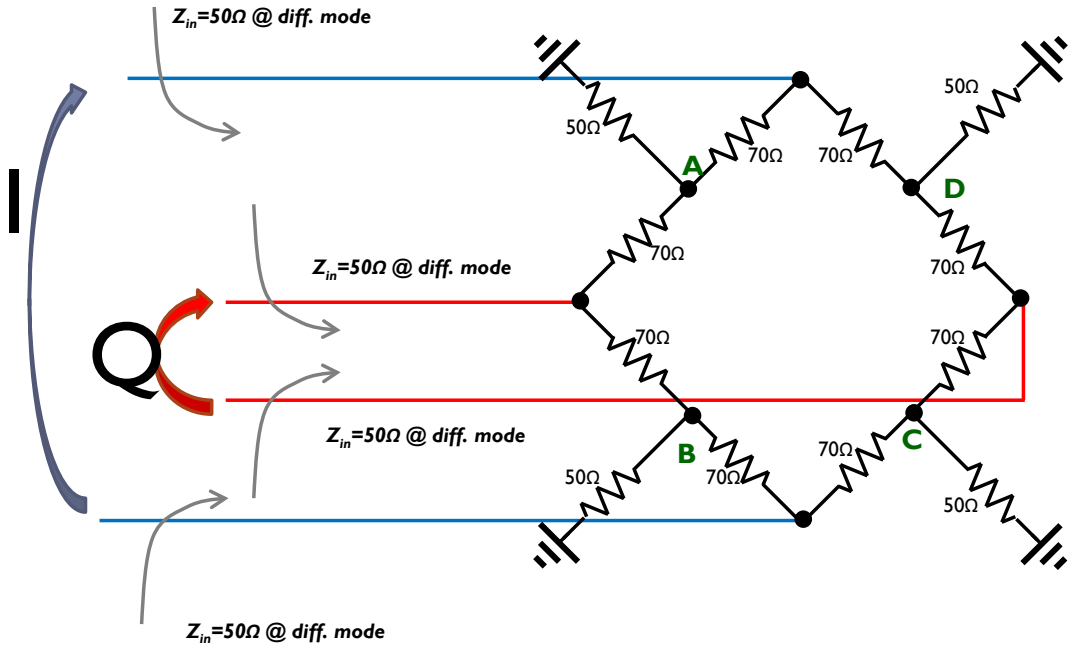


Fig. 64: Passive network for I and Q summation and subtraction.

To ensure proper operation, the summation and subtraction paths delays must be made equals, i.e. $\tau_3 = \tau_4$. The network layout, hence, was design in a very symmetric fashion, taking into account the entire path, up to the XOR gate multiplier (Fig. 65). Crossovers are minimized and kept the same for all of the paths. The layout was fully EM simulated.

To complete the multiplication process of $I \cdot Q \cdot (I + Q) \cdot (I - Q)$, two more

XOR gates are required. The order of multiplication plays a critical role on the choice of proper delays. As multiplying $I \cdot Q$ at the second stage in inconvenient layout-wise, a further multiplication of $I \cdot (I+Q) \cdot (I-Q)$ takes place and a multiplication by Q occurs last.

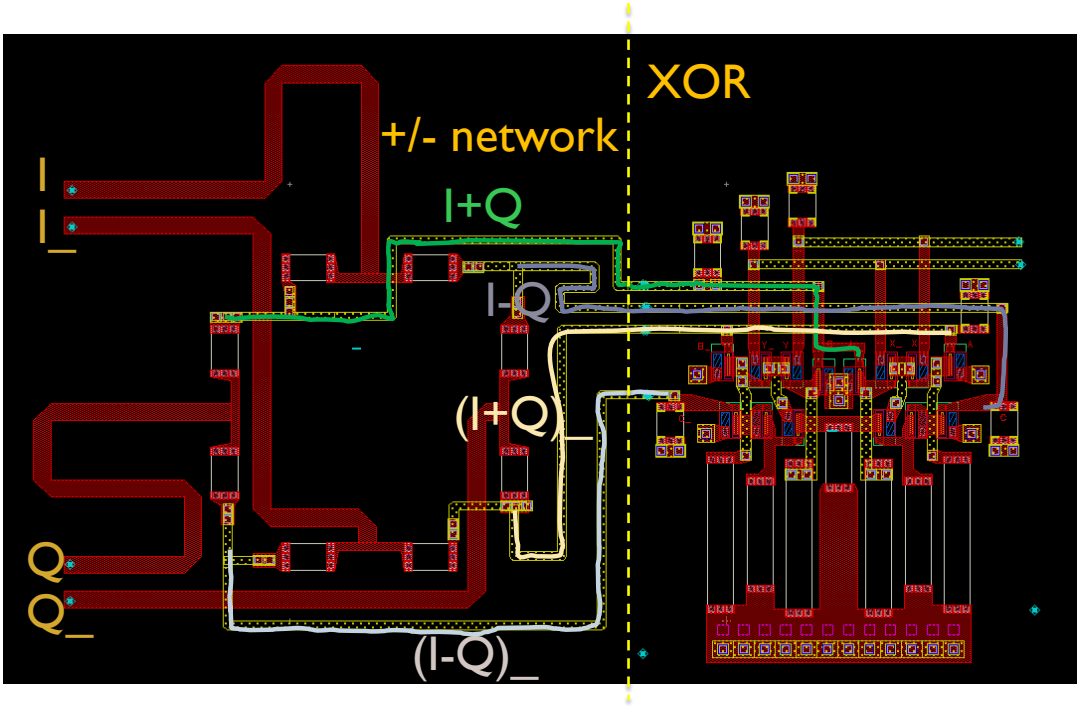


Fig. 65: Layout of the (I+Q) and (I-Q) paths

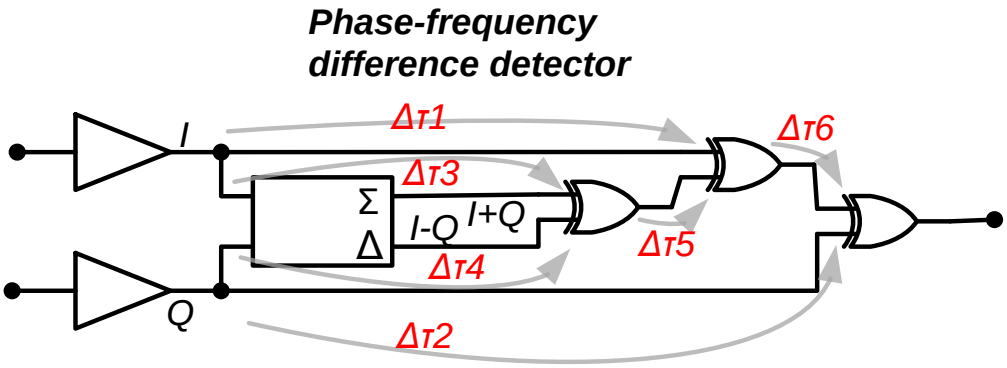


Fig. 66: QPSK PFD multiplication order and relative delays.

Fig. 66 presents the block diagram of the PFD. First, $(I+Q)$ is multiplied by $(I-Q)$, then the result is multiplied by I and finally by Q. Given the notated

relative delays, one can write: $\tau_1 = \Delta\tau_1 + \Delta\tau_6$; $\tau_2 = \Delta\tau_2$; $\tau_3 = \Delta\tau_3 + \Delta\tau_5 + \Delta\tau_6$ and $\tau_4 = \Delta\tau_4 + \Delta\tau_5 + \Delta\tau_6$. Demanding $\tau_3 = \tau_4$ results in $\Delta\tau_3 = \Delta\tau_4$. In addition, $\tau_3 - \tau_1 = \Delta\tau_3 + \Delta\tau_5 - \Delta\tau_1 = 5\,ps$ and $\tau_4 - \tau_2 = \Delta\tau_4 + \Delta\tau_5 + \Delta\tau_6 - \Delta\tau_2 = 5\,ps$. Equating $\tau_3 - \tau_1 = \tau_4 - \tau_2$ while substituting $\Delta\tau_3 = \Delta\tau_4$ yields $\Delta\tau_2 = \Delta\tau_6 + \Delta\tau_1$.

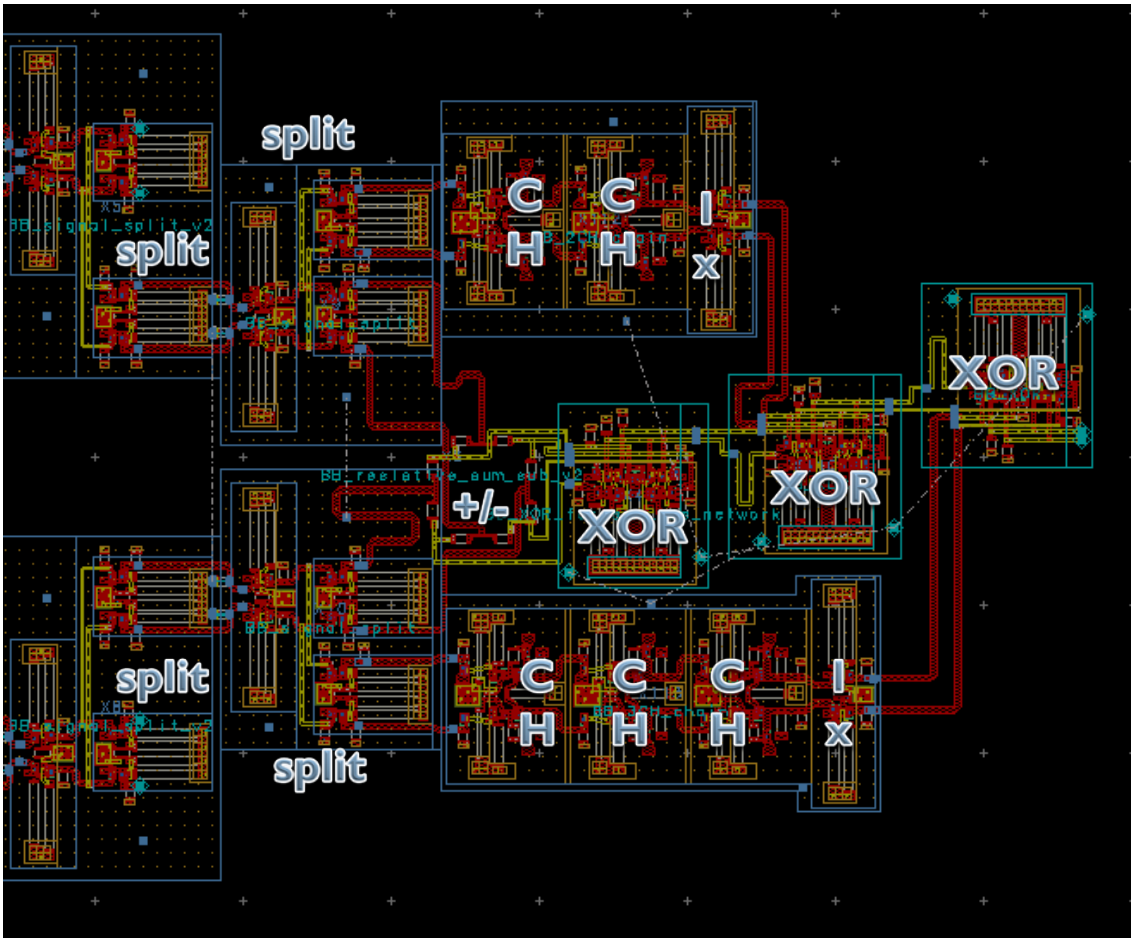


Fig. 67: QPSK PFD full layout.

The I/Q signals delivered by the front end are split and supplies to the PFD (left hand of Fig. 67). Then they are split again and delivered to the summation-subtraction network to form I+Q and I-Q. In parallel, I and Q are delayed and later multiplied by I+Q and I-Q. Due to the large delay required to satisfy the delays relations, active cells such as CHA and unity-gain cells

were used to introduce delay, rather than just long lossy lines. In addition, after each multiplication the beat-note frequency is doubled and eventually exceeds the cells bandwidth so very high bandwidth cells must be used. For these reasons, the last XOR gate does no longer operate in limiting mode.

6.4 QPSK Integration and Simulation Results

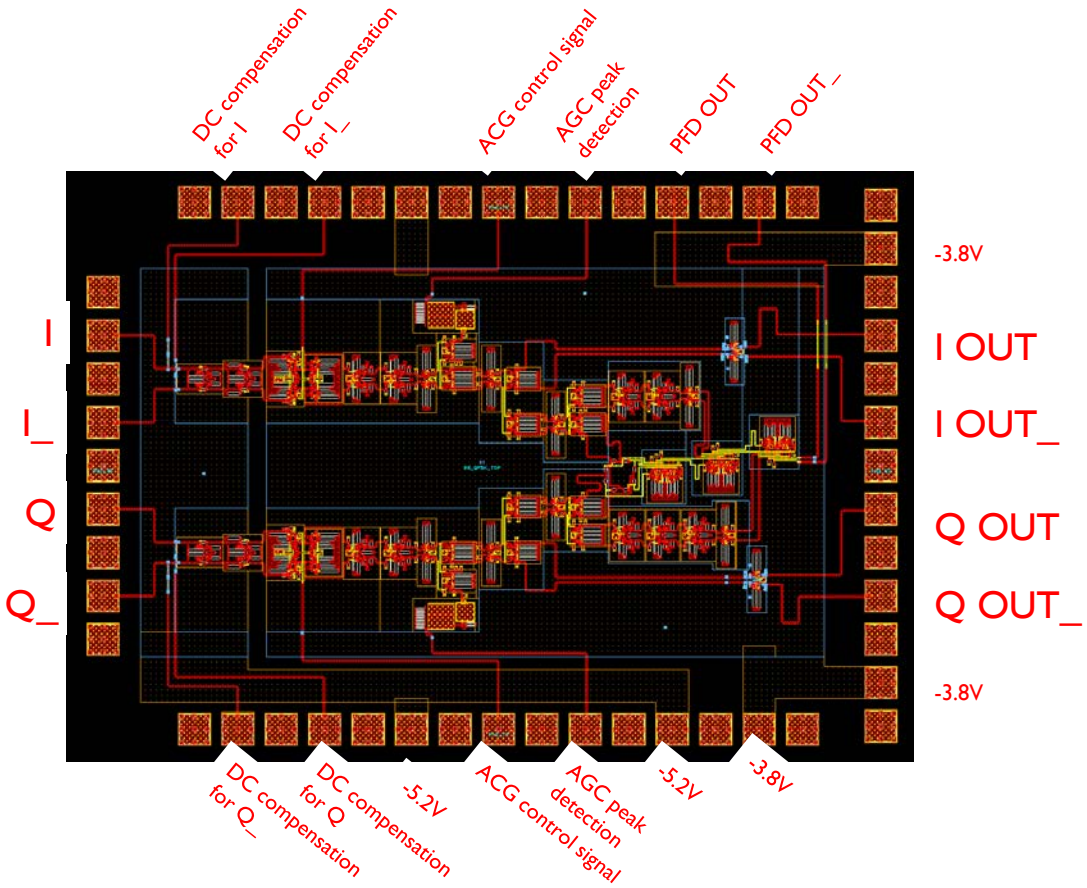


Fig. 68: QPSK top level layout.

The top level of the QPSK receiver consists of two (I and Q) linear front-ends and a PFD. Fig. 68. The I and Q photocurrents are provided on the left. The demodulated data is delivered on the right and the PFD output is on top. Most of the IC is powered by a $-3.8\,V$ supply while the resistive feedback amplifier is powered by $-5.2\,V$, hence two separate power planes are used (on M4) with a single ground plane on M3. Input DC compensation pads are also available for use in case of photodiodes imbalance. Each front-end includes its own peak detector and VGA. The total chip size is $1.8 \times 1.3\,mm^2$.

To characterize the QPSK receiver, the front ends and the PFD were both simulated. Fig. 69 shows I and Q output data eye diagram at locked state, for a $0.2\,mA$ input photocurrent at $100\,GBaud/s$ data rate. The inputs contain the local oscillator shot-noise (which is assumed to be the main noise source of the incoming signal) to emulate a practical operation mode.

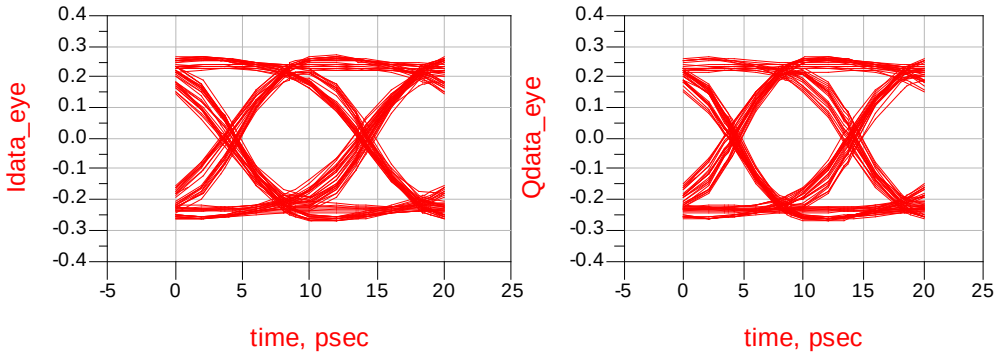


Fig. 69: I and Q output data eye diagram for locked state. The input photocurrent is 0.2mA, at $100\,GBaud/s$ *data-rate.*

Simulation of the PFD operation was carried out under QPSK modulated input at $100\,GBaud/s$ data rate. To emulate LO and reference lasers phase and frequency offsets, skewed and rotating constellation sources were constructed on

ADS. Frequency detection range was originally design to operate within a $\pm 50\,GHz$ range. As can be observed on Fig. 70, the frequency detection characteristics reaches a peak on $30\,GHz$, what can be extrapolated to a $\pm 60\,GHz$ range. The phase detection demonstrates a 90° periodicity, required for four stable states. It can also be seen that K_{FD} and K_{PD} at 45° acquire a same sign, necessary for correct demodulation. The lack of symmetry of the phase detection characteristics is caused by different paths for I+Q, I-Q and for I, Q. At 0° phases, I+Q and I-Q signals are the two leveled ones, while at 45° phase offset the I and Q are two leveled.

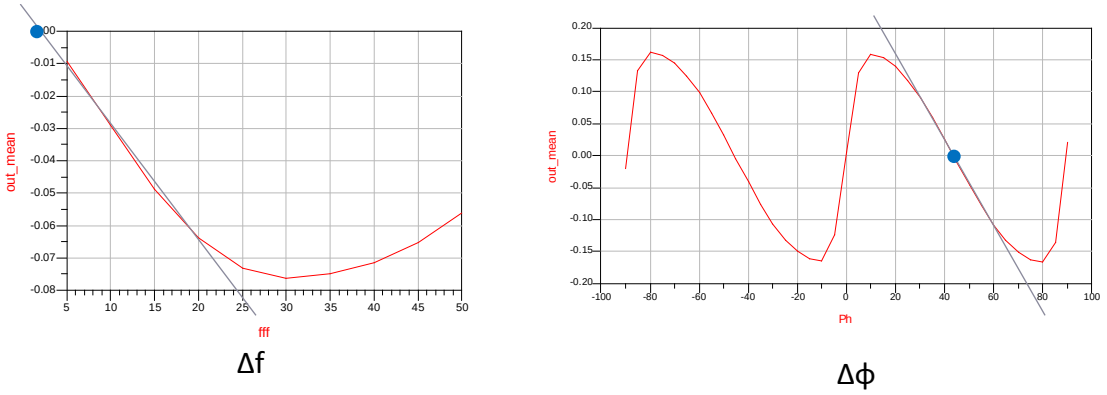


Fig. 70: QPSK PFD characterization under $100\,GB/s$ *modulation: (left) frequency detection, (right) phase detection.*

6.5 QPSK System Measurements

A $800\,MHz$ closed loop BW (Fig. 71), type II loop filter was designed to operate homodyne QPSK receiver at phase-locked mode. The loop filter architecture is similar to the BPSK one in having both active and feed-forward

path to minimize loop delay.

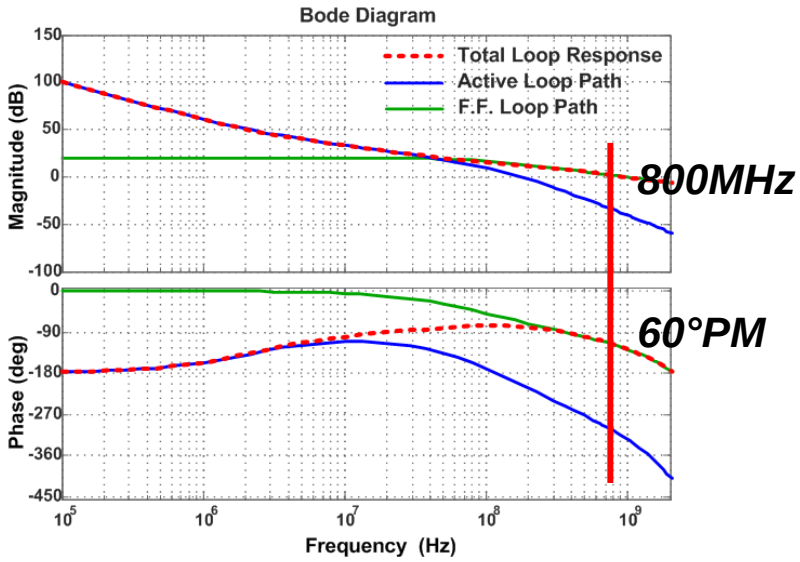


Fig. 71: QPSK loop filter design – open loop gain

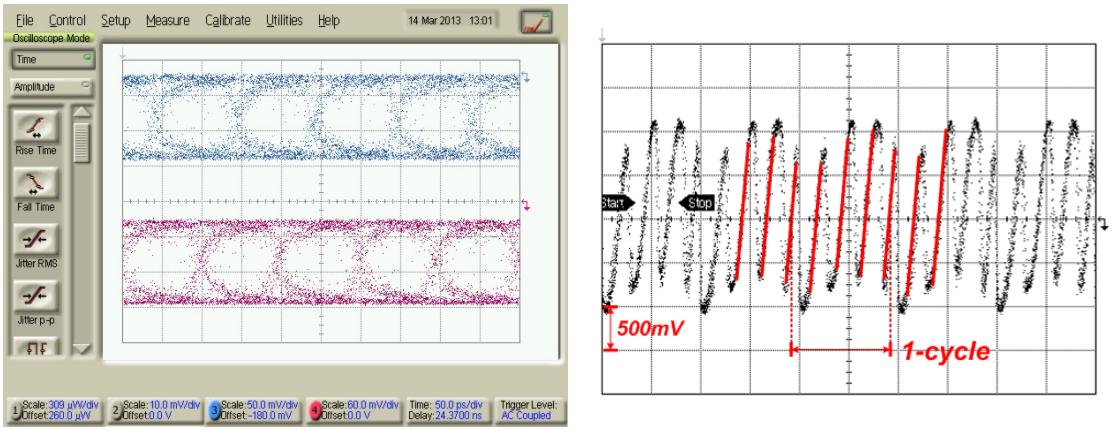


Fig. 72: QPSK receiver measurement – (left) $10\ GBaud/s$ *data demodulation, (right) PFD measurement in phase detection mode.*

A measured phase detection behavior exhibits four stable states (Fig. 72-right) and the full receiver was operated with $10\ GBaud/s$ QPSK data. The demodulated eye diagram is shown on Fig. 72-left.

Due to cycle slips the system was not characterized for higher bit-rates.

7. An F-Band 20.6 Gb/s QPSK Transmitter in 65nm CMOS

7.1 IC design and topology

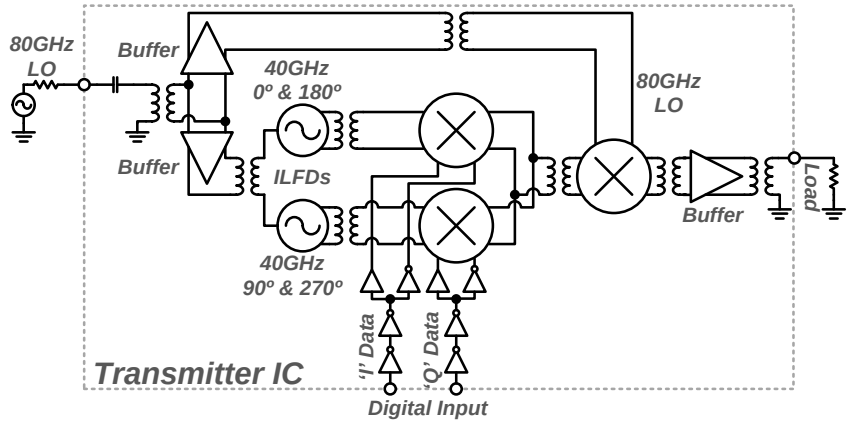


Fig. 73: Transmitter block diagram and layout floor plan.

The transmitter was designed using a TSMC CMOS $65\,nm$ process with devices feature cut-off frequencies of about $180\,GHz$. A heterodyne quadrature topology was chosen to upconvert the data to a $120\,GHz$ carrier (Fig. 73). The IC is driven by an external $80\,GHz$ LO. The LO signal is split and divided by a pair of injection locked frequency dividers for $0°, 180°, 90°, 270°$ phases formation at $40\,GHz$. ILFDs require small area and low power consumption and offers a frequency tuning range, while benefiting from low sensitivity to layout

line length mismatch. The $40\,GHz$ modulated data is upconverted to $120\,GHz$ using a second mixing stage while the output of the second mixing stage is driven by a one stage output buffer (PA) to a $50\,\Omega$ load (can be an antenna or on chip probing). An inverters chain delivers the I and Q data channels to the quadrature mixer, while operating as an active balun and digitizing the waveforms.

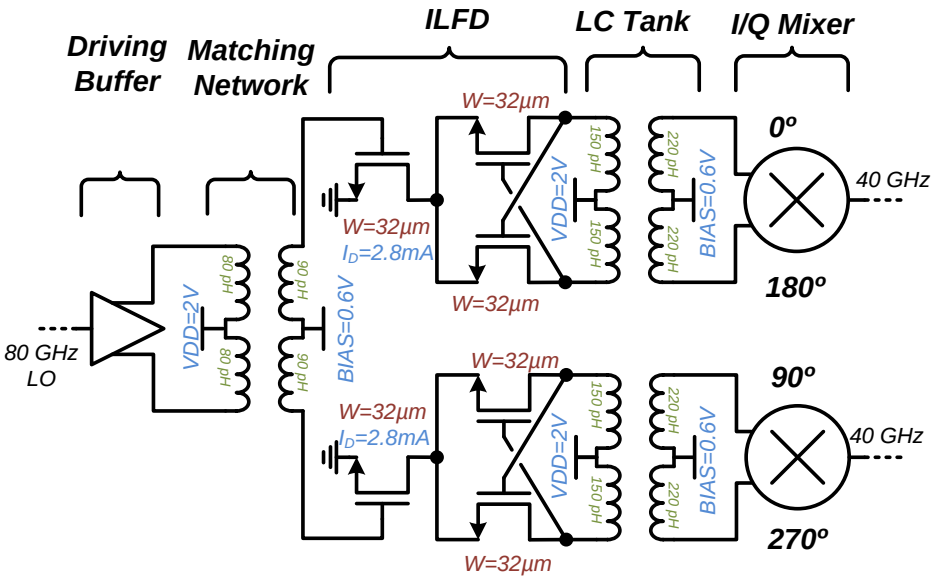


Fig. 74: ILFD schematic.

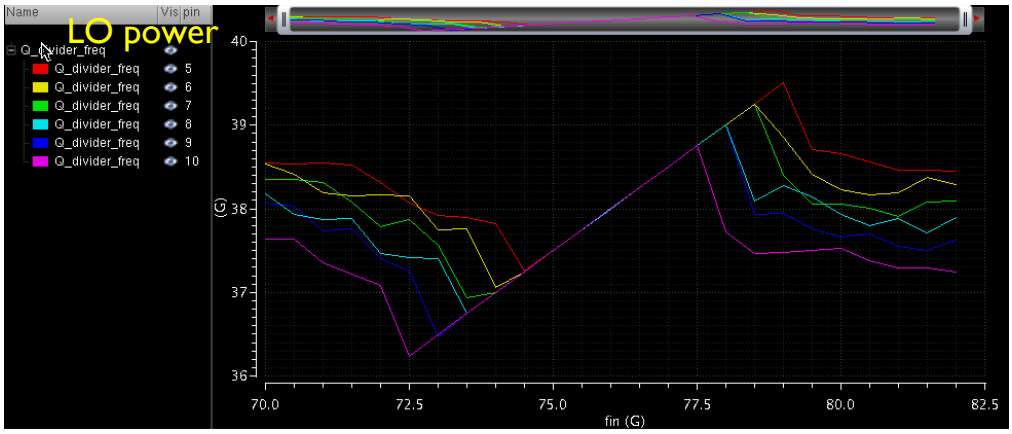


Fig. 75: ILFD oscillating frequency vs external LO frequency.

The quadrature LO is generated using ILFDs, implemented cross-coupled

VCOs. The choice of ILFD for quadrature generation aims to achieve high phase accuracy and low phase noise across the entire frequency-locking range [56]. The driven stage input capacitance is utilized to form the LC tank (by impedance transformation); a tank tuned for locking at the $40\,GHz$ range. Simulation results suggest a locking range of $72\sim80\,GHz$ external LO frequency, for various LO power levels, Fig. 75. For a driving LO of $8\,dBm$ the ILFD deliver about $-3\,dBm$ LO to the quadrature mixer.

The quadrature upconversion core is comprised of two pseudo-differential double-balanced Gilbert cells to reduce the odd-order mixing products. The switching core of the mixer is fully switched by the rail-to-rail digital data while the quadrature LO from the ILFDs is delivered to the Gm core (Fig. 76).

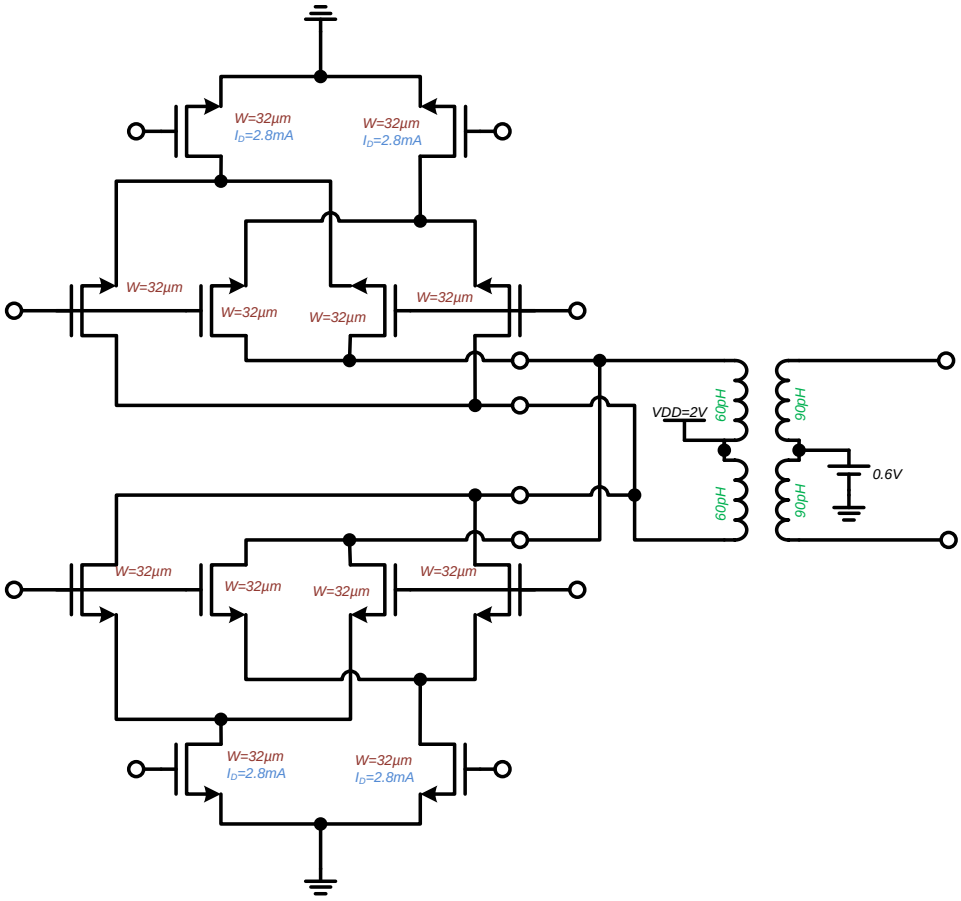


Fig. 76: Quadrature mixer schematics.

The second mixing stage is also implemented, similar to the I/Q mixers, using a pseudo-differential double-balanced Gilbert cell (Fig. 77). The transistor sizing was optimized for linearity rather than conversion gain. The mixer's $80\,GHz$ LO is provided externally, by the same source that drives the ILFDs.

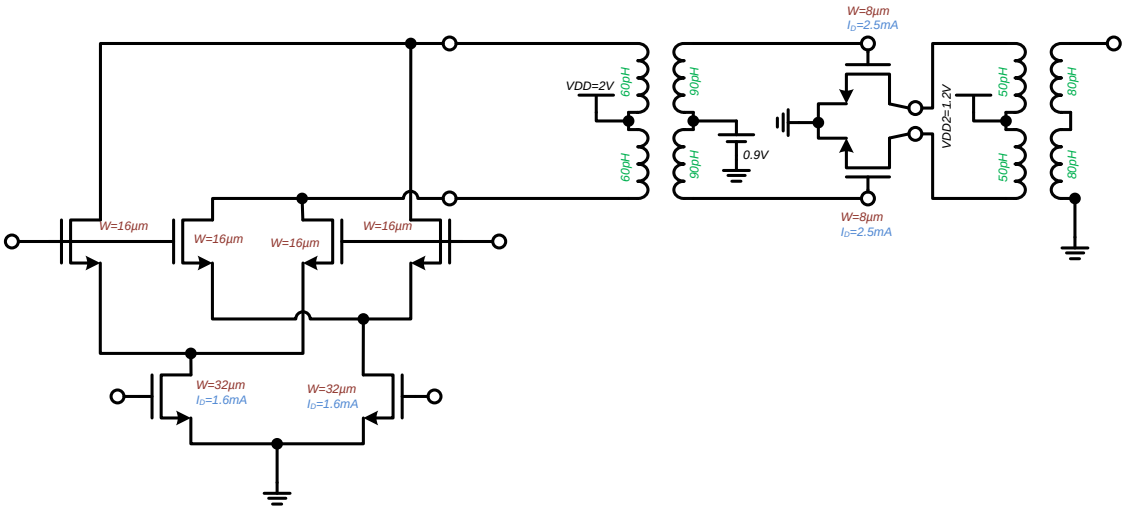


Fig. 77: Second (RF) mixer and output buffer schematics.

As the output buffer operates at frequencies higher than half f_t and f_{max}, it is hard to achieve maximum available gain higher than $3-4\,dB$. A simple pseudo-differential common source stage was used, with an output P1dB of $-1\,dBm$. Though QPSK is considered to be a constant envelope modulation, practical I and Q data transitions are not perfectly square, resulting in varying modulated-signal envelope. In such case, a highly non-linear output buffer (PA) will cause spectral regrowth. For this reason an effort was made to maximize the data path linearity.

The input LO splitter buffers are pseudo-differential cascode stages. As the buffers operate at $80\,GHz$ (hence the maximum available gain is higher), the cascode topology partially trades-off the gain with better linearity, stability and isolation (Fig. 78).

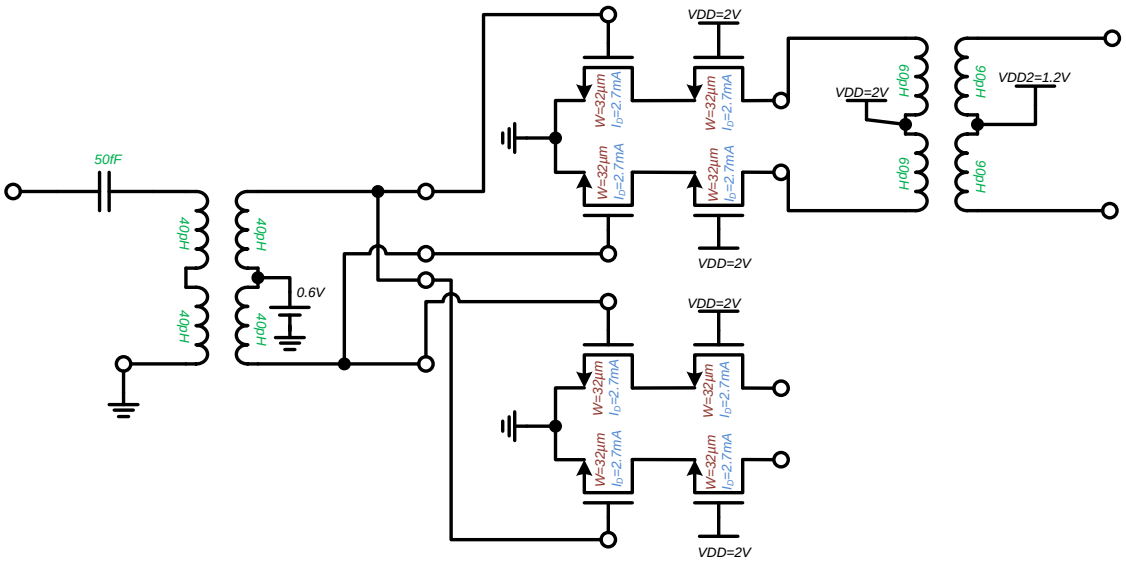


Fig. 78: LO splitting network schematics.

7.2 Layout and EM Considerations

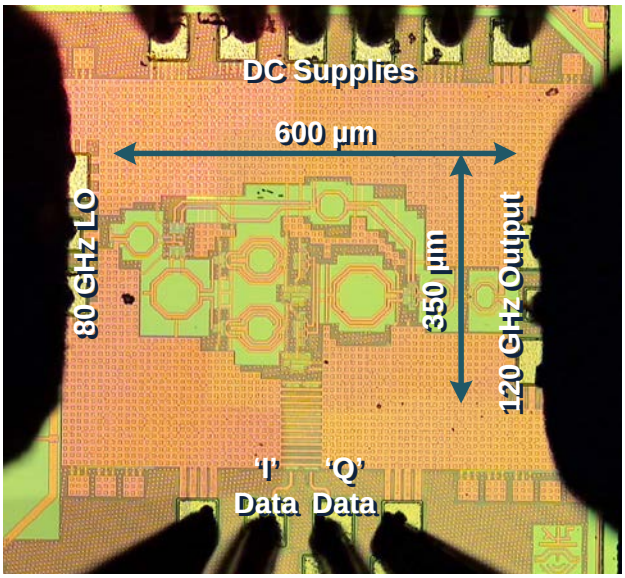


Fig. 79: Chip photograph. The core area is $0.21\,mm^2$.

The transmitter layout floor-plan preserve symmetry for the high frequency

LO path while the data is delivered from below (Fig. 79). As the data bandwidth is about $10\,GHz$ for each channel, the difference in the signal paths to the I/Q mixer is negligible. All transformers, pads and interconnects were electromagnetically modeled using an Agilent Momentum EM simulator.

The DC is provided through a dense power grid, separated by ground layers. This way the entire grid operates as a large capacitor, while power supplies cross-talk is minimized. Two DC power supplies are used: $2\,V$ supplies for the Gilbert cells, ILFDs and the splitters, while the output buffer was biased by a $1.2V$ supply. The designed frequencies were targeting the $110-120\,GHz$ range to use the more available W-band measurement equipment.

7.3 Measurements and Characterization

The transmitter IC was measured using on-chip probing. The input LO was delivered using $100\,\mu m$ pitch, $110\,GHz$ GSG probes (Fig. 79 on the left) while a similar probe was used to sample the output signal (Fig. 79 on the right). To apply the data, a $100\,\mu m$ pitch, $67\,GHz$ GSSG probe was utilized.

Fig. 80 describes the transmitter IC measurement setup. The input LO is driven by a frequency x4 multiplier (AMC-15-RFH00) while the output was downconverted using an external $75-110\,GHz$ mixer (QMB-9393WS) driven by a x6 frequency multiplier (AMC-15-RFHB0). Three types of measurements were performed: a carrier power and ILFDs locking range characterization, time domain full data recovery, and constellation EVM measurements.

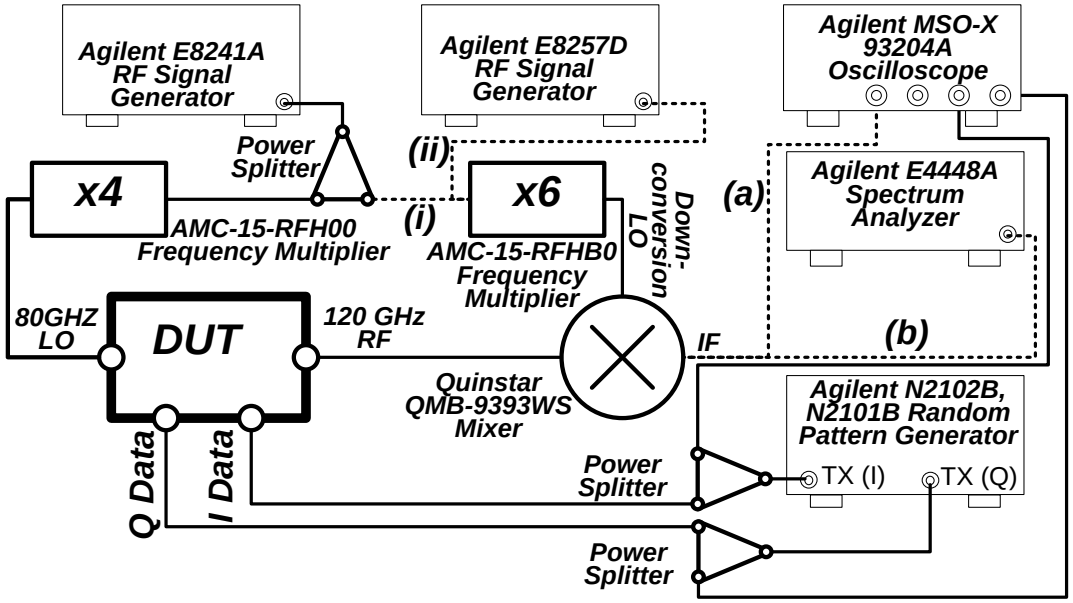


Fig. 80: Transmitter measurement setup.

7.3.1.1 Carrier Characterization

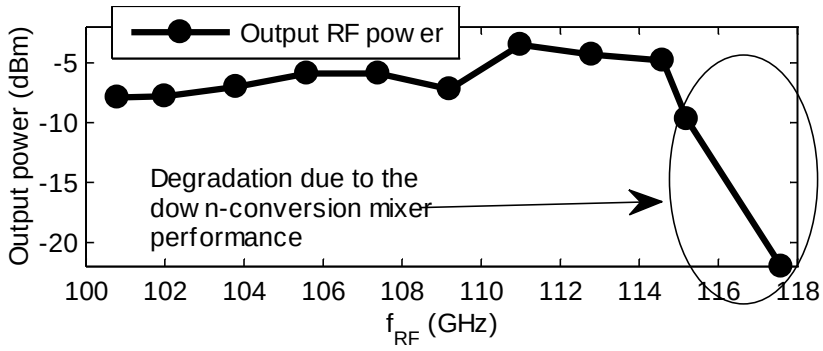


Fig. 81: Output RF power vs. RF frequency (for LO frequency varied between 67.2 *GHz and* 78.4 *GHz).*

To inspect the output carrier power both frequency multipliers were driven by separate signal generators and the external downconversion mixer IF power was measured using a spectrum analyzer (Agilent E4448A) (Fig. 80. configuration (ii) and (b)). The maximum carrier frequency was limited by the measurement setup. As the x4 frequency multipliers is designed for a 50-75 *GHz*

band and the downconversion mixer for $75\text{-}110\ GHz$, the IC could be measured only for sub – $120\ GHz$ frequencies. The output RF power is presented on Fig. 81.

The output RF power is about -5 to $-3\ dBm$ for a constant $8\ dBm$ input LO power. The drastic drop in the output power at $\sim 118\ GHz$ is a result of the external x4 multiplier output power drop by $5\ dB$ at frequencies above $78\ GHz$. The data on Fig. 81 is used to calculate the ILFDs locking range. An output RF carrier locking range of $\Delta f_{RF} = 18\ GHz$ is a consequence of a $\Delta f_{ILFD} = 6\ GHz$ locking range around a free-running frequency of $37 GHz$. Simulations suggest that the locking range limit can be extended to $40\ GHz$ by increasing the input LO power.

7.3.2 Data Recovery and Eye diagram

In data recovery mode the measurement setup was connected according to configuration (i) and (a). Both the LO multiplier and the downconversion mixer were driven by the same signal generator to synchronize the phase between the upconversion and the downconversion LOs. As the external mixer is limited by a maximum LO frequency, the transmission was performed using a carrier of $107\ GHz$.

The data was supplied by a random pattern generator (Agilent N2102B and N2101B) and the output baseband was delivered to a scope (Agilent, MSO-X 9.204A). Fig. 82 displays the original vs. the recovered data. A full, dual channel (QPSK) operation mode at $8.5 \times 2 = 17\ Gbps$ data recovery is presented on subplot (a). The channels selection was controlled by varying the downconversion LO phase relative to the upconversion LO. The $100\ mV_{p-p}$ output is translated to $-16\ dBm$ power, matching the power levels on Fig. 81.

Subplot (b) presents the eye diagram of each channel. The relatively closed eye in the dual channel operation (QPSK) can be as well caused by the use of a single downconversion mixer. When operating in a single channel mode (subplot (c) and (d) – one channel at a time) the eye is wide open for up to $10\ Gb/s$ data rate. It is expected that for a dedicated receiver architecture a transmission at $10\ Gb/s$ and above at each channel can be obtained, as shown for the constellations below.

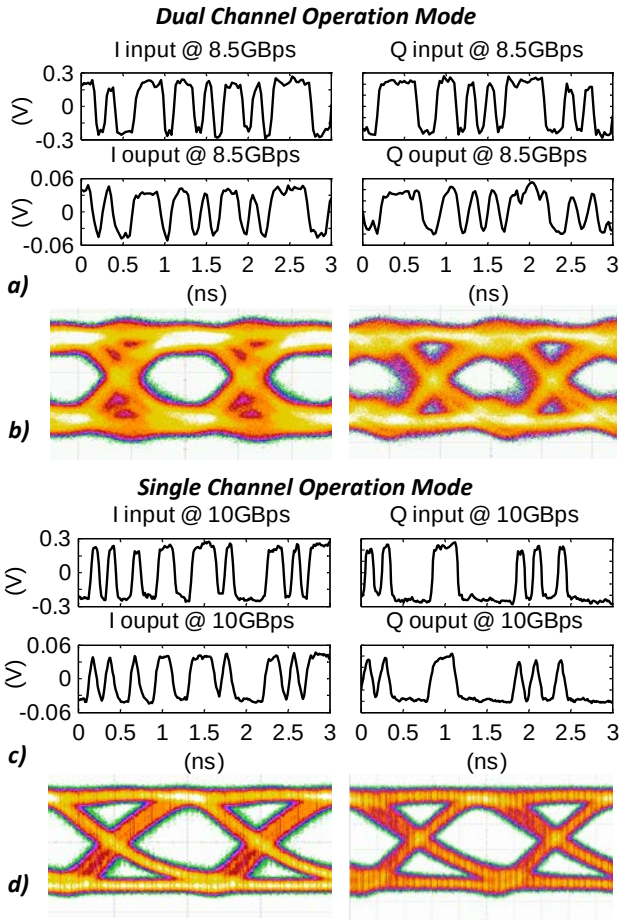


Fig. 82: Data recovery experiment. a) Original and recovered data waveforms with $8.5\ Gb/s$ *each channel data rate at dual channel operation (QPSK). b) Eye diagrams for* $8.5\ Gb/s$ *dual channel operation. c) Waveforms of the original and recovered I or Q for* $10\ Gb/s$ *data rate, single channel (BPSK). c) Eye diagrams for* $10\ Gb/s$*, single channel operation.*

7.3.3 CONSTELLATION AND EVM

The I/Q constellation was measured using the oscilloscope VSA software. The setup was connected in configuration (ii) and (a). The external mixer has downconverted the signal to an IF to be sampled by a scope. The limited downconversion-mixer IF range of $10\,GHz$ applies an additional limitation on the measurements setup and might have impaired the received EVM.

As shown in Fig. 83, constellations for both 20.6 and $10\,Gb/s$ data-rates were measured. The IF frequency was chosen accordingly, to achieve the best performance of the downconversion link.

The constellation map indicates a good I/Q phase matching. For a $30\,dB$ downconversion-link conversion-loss the measured EVM with is $24.8\,dB$ ($BER = 6.4 \cdot 10^{-9}$ equivalent [57]) at $20.6\,Gb/s$ data-rate (limited by the PRBS generator, and $21\,dB$ ($BER = 8.4 \cdot 10^{-12}$ equivalent) at $10\,Gb/s$.

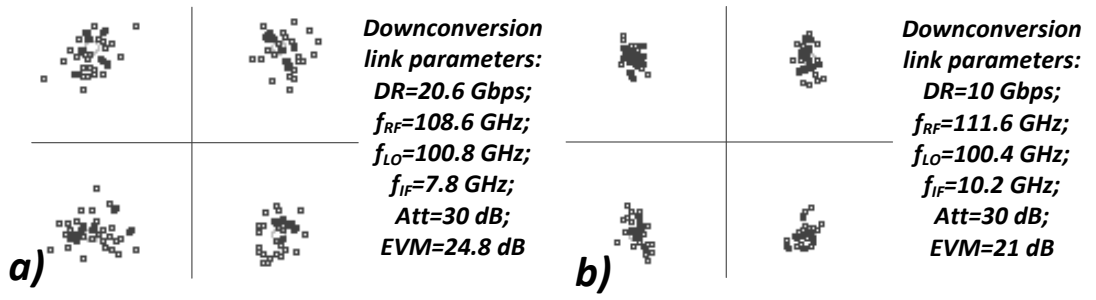


Fig. 83. QPSK constellation and IF spectrum at a) $20.6\,Gb/s$*, b)* $10\,Gb/s$*.*

8. Appendix

8.1 Impedance Matching Using Transformers

The topic of impedance transformation and matching is one of the well-established and essential aspects of microwave engineering. A few decades ago, when discrete RF design was dominant, impedance matching was mainly performed using transmission-lines techniques that were practical due to the relatively large design size. As microwave design became possible using integrated on-chip components, area constraints made $L-C$ section matching (using lumped passive elements) more practical than transmission line matching. Both techniques are conveniently visualized and accomplished using the well-known graphical tool – the Smith chart.

Since CMOS technology was primarily and initially developed for digital purposes, the lack of high quality passive components made it practically useless for RF design. The device speed was also far inferior to established III-V technologies such as GaAs HBTs and HEMTs. The first RF CMOS receiver was constructed in 1989 [58] but it would take another several years for a fully integrated CMOS RF receiver to be presented. The scaling trend of CMOS in the past two decades improved the transistors speed exponentially, which

provided more gain at RF frequencies and also enabled operation at millimeter-wave frequencies. The use of copper metallization and the increased number of metal layers (~ 10 at present) also improved the integrated passive devices in CMOS for RF circuits. The ability to integrate RF circuits with mixed signal and digital circuits on the same chip generated the motivation to use CMOS for RF applications. By 2005 CMOS was already the dominant technology in most RF applications below $10\,GHz$ [59].

Monolithic inductors play a critical role in RF components, but in marked contrast to capacitors, they exhibit much lower quality factors, particularly at low frequencies and on silicon conductive substrates. The evolution of on-chip inductors has also come a long way since the 60s and 70s when it was widely claimed that integrated inductors with reasonable Q were practically unrealizable and should be placed externally. As a result, inductors were implemented using bondwires and package pins. Only with the appearance of an accurate analytical model have integrated spiral inductors become popular. With the increasing operating frequency of narrowband integrated circuits, monolithic inductors and transformers became more popular. In current millimeter-wave integrated circuits their physical dimensions become comparable to the size of active blocks. As passive components have a significant impact on the system performance, extensive work on silicon integrated inductors and transformers modeling has been performed, offering an extensive analysis of various transformer topologies, layout geometries, substrate impact and layout parasitics [60-63].

In contrast with non-integrated RF circuits, transformers (made of coupled inductors) play a key role in CMOS based RFICs [64, 65] and became the obvious choice when it comes to impedance matching and cascaded blocks in CMOS RF and mm-wave ICs. Transformers enable symmetric differential

operation, with a virtual ground along the symmetry line. They provide DC separation between the stages and easy biasing through the center tap. In addition, transformers enable high voltage swings with low voltage headroom and are used in implementations of power combining [66, 67], resonance loading [68-70], bandwidth peaking, low-noise feedback [71], baluns, and serve as a key component in active building blocks such as power amplifiers [72-74] and low noise amplifiers [71, 75, 76].

In contrast to the more traditional $L-C$ impedance matching (L-sections, π-sections, etc.) performed using a Smith chart, no similar method exists to perform exact conjugate impedance matching using transformers. The method usually used for matching is adding additional parallel and series capacitors to resonate the transformer's residual inductances [66]. To the best of the our knowledge, no straight-forward tool has been developed to determine the required transformer sizing and winding ratio for exact conjugate matching given a load and source impedance in the manner used in the case of lumped inductors and capacitors or transmission lines.

This section is focused on proposing and demonstrating a universal graphical tool (a nomogram) for conjugate impedance matching using transformers. The tool not only offers direct determination of transformer parameters, but also provides the designer with insight into design trade-offs and alternatives such as transformer sizing, matching bandwidth, and various winding ratios, thus easily enabling a design starting point and leading to an optimized solution.

The graphical tool developed in this work is based on a first order transformer approximation of a non-ideal transformer (Fig. 84.a) represented by two ideal inductors (the ideality assumption will be reviewed and justified later on) L_1, L_2 coupled with a mutual magnetic coupling coefficient k. To use

this representation for circuit analysis purposes, an equivalent scheme (Fig. 84.b) is presented by [77], comprised of two ideal leakage inductors $(1-k^2)L_1$, k^2L_1 and an ideal $N:1$ transformer, with $N = k\sqrt{L_1/L_2}$.

In cases when the transformer is used as a matching network between two stages, the values of L_1 and L_2 should be determined to produce a conjugate match between a source and a load.

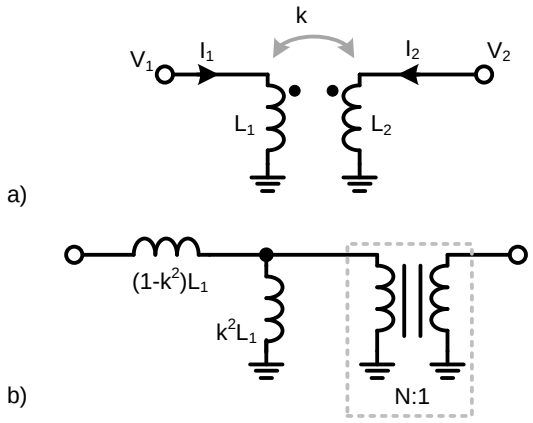


Fig. 84: a) A first order transformer model, with $-1 < k < 1$ as the magnetic coupling coefficient. b) Equivalent circuit with an ideal $N:1$ transformer.

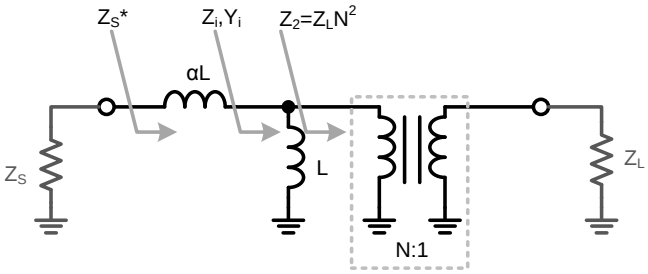


Fig. 85: A modified representation of the transformer, including nodes impedances notations.

For the convenience of the derivation process, the following notations are used:

$$\alpha \equiv \frac{1-k^2}{k^2} \qquad \textit{Eq. 13}$$

$$L \equiv k^2 L_1 \qquad \textit{Eq. 14}$$

Using Eq. 13 and Eq. 14 with the equivalent scheme yields the scheme shown in Fig. 85, with inductor values replaced by αL and L. As the typical value of k for monolithic transformers is usually in a range of $0.7-0.8$, α will be consequently equal to $1-0.5$. Without a loss of generality, it is assumed that both the source impedance, Z_S, and the load impedance, Z_L, are capacitive. This is a practical assumption when active stages are involved. To define an unambiguous quality factor for both capacitive and inductive impedances, the definition $Q=-Im\{Z\}/Re\{Z\}$ is used. Using this definition, $Q>0$ for capacitive impedances and $Q<0$ for inductive ones. One can also express both the load and the source impedances in terms of its quality factor, i.e. $Z_L = R_L - jQ_L R_L$, and $Z_S = R_S - jQ_S R_S$ with $R_L, R_S > 0$.

The purpose of using the transformer is to conjugate match the impedance so that the transformer would show an impedance of Z_S^* to the source impedance Z_S. Alternatively, the same condition holds at other points along the connection between the source and the load; for example. at the intermediate impedance point of Z_i. Expressing Z_i in terms of Z_S^*, Y_i in terms of Z_L and equating $Z_i = 1/Y_i$, yields a quadratic equation in L or in its normalized value of $\tilde{Z} = \omega\alpha L/R_S$ (detailed derivation in the Appendix):

$$\frac{Q_L}{1+\left(Q_S-\tilde{Z}\right)^2}-\frac{\alpha}{\tilde{Z}}=\frac{-\left(Q_S-\tilde{Z}\right)}{1+\left(Q_S-\tilde{Z}\right)^2} \qquad \textit{Eq. 15}$$

It now means that for each set of source and load impedances (defined by their quality factors) we can solve equation Eq. 15 and find the required transformer definable by its L (normalized by the source resistance and the frequency of operation for an assumed coupling factor k). The problem of finding the transformer to match Z_S to Z_L is then solved. However, we would like to provide a graphical tool that solves this matching problem that is general enough to provide solution independent of parameters such as the frequency and source or load resistances. In order to do that, instead of solving directly for the primary and secondary inductor coils L_1 and L_2, we define normalized parameters that allow a general graphical representation of the solution. We found that defining cross quality factors for the two coils does just that: $Q_{XL1}=\frac{\omega L_1}{Re\{Z_S\}}$ and $Q_{XL2}=\frac{\omega L_2}{Re\{Z_L\}}$. These cross quality factors can be calculated from the solution of $\tilde{Z}$ using Eq. 15 with:

$$Q_{XL1}=\frac{\tilde{Z}}{1-k^2} \qquad \textit{Eq. 16}$$

$$Q_{XL2}=\frac{\tilde{Z}}{\alpha}\cdot\frac{1+Q_L^2}{1+\left(Q_S-\tilde{Z}\right)^2} \qquad \textit{Eq. 17}$$

The result is that it is possible now to find normalized solutions (Q_{XL1} and Q_{XL2}) for the inductance of both coils assuming a desired transformer coupling factor k and depends only on the source and load impedance quality factors Q_S and Q_L. The details of these calculations are shown in the appendix.

8.2 Graphical Tool

Equations Eq. 16 and Eq. 17 for Q_{XL1} and Q_{XL2} form the foundations of the matching chart proposed in this study. As shown by Eq. 15, $\tilde{Z}$ has no direct dependence on the frequency of interest, and on the actual source and load impedance values. Since the cross quality-factors Q_{XL1} and Q_{XL2} are functions of $\tilde{Z}$, Q_S, Q_L and k (as shown at Eq. 16 and Eq. 17), they also have normalized values, and it is possible to plot the Q_{XL1} and the Q_{XL2} contours as a function of Q_L and Q_S for a given (or assumed) value of k (Fig. 86). The inductor values L_1 and L_2 derived from the chosen Q_{XL1} and the Q_{XL2} would of course be frequency dependent, according to $R_S Q_{XL1}/\omega$ and $R_L Q_{XL2}/\omega$, respectively.

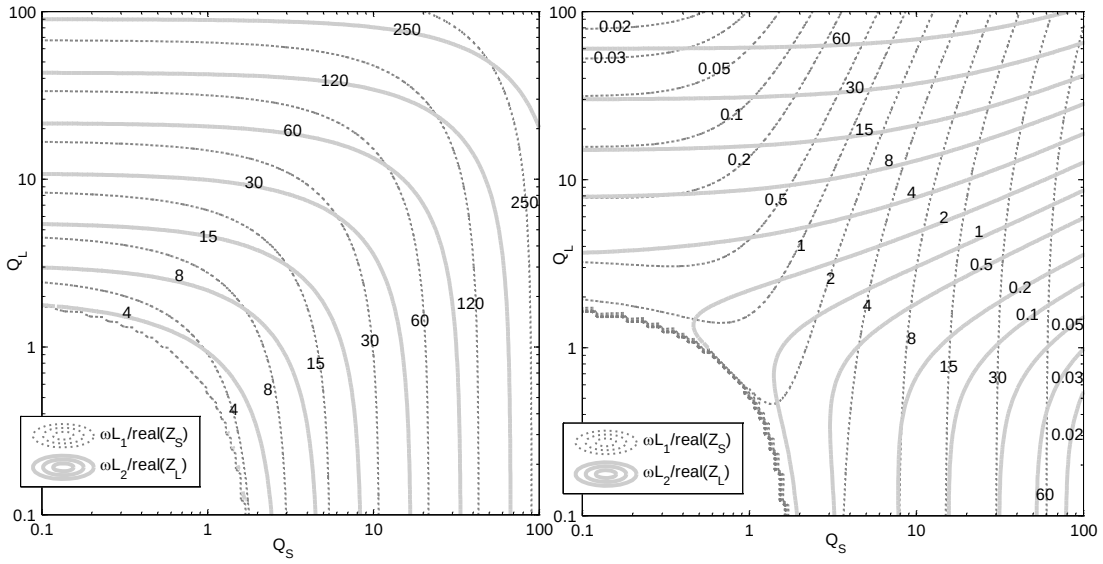


Fig. 86: Matching chart: $\omega L_1/Re\{Z_S\}$ and $\omega L_2/Re\{Z_L\}$ contours vs. Q_L and Q_S for $k = 0.8$. Right: solution #1 of Eq. 15. Left: solution #2 of Eq. 15.

The matching chart on Fig. 86 is a contour plot of $Q_{XL1}(Q_S, Q_L)$ and $Q_{XL2}(Q_S, Q_L)$ values based on the substitution of solution of Equations Eq. 15, into Eq. 16 and Eq. 17 (for a typical coupling value of $k = 0.8$), suitable for any

capacitive source and load impedances (as plotted for $Q_S, Q_L > 0$). As a result of the Q_{XL1} and Q_{XL2} independency on the actual source and load impedances and on the frequency of operation, the chart is universal and is suitable for any matching application. It is also valid in case when a capacitive impedance is to be matched to a pure real impedance such as $50\ \Omega$, regardless of the value of R_L and R_S (no solution is available if both of the impedances are inductive). Given only the quality factors Q_S and Q_L of the source and load impedances (at the frequency interest) one can graphically find the required values of Q_{XL1} and Q_{XL2}. Then, given the actual $Re\{Z_L\} = R_L$ and $Re\{Z_S\} = R_S$, the actual values of L_1 and L_2 can be determined which eventually forms the transformer at the frequency of interest.

8.2.1 MATCHING EXAMPLE

The general algorithm for using the charts in Fig. 3 is as follows:

- For a given Z_S and Z_L calculate Q_S and Q_L at the frequency of interest.
- Find the crossing point of Q_S and Q_L on the matching chart.
- Extract the values of Q_{XL1} and Q_{XL2} curves meeting at the crossing point.
- Finally, obtain the required $L_1$and L_2 that form the transformer using the frequency of interest ω and the source and load resistances R_S and R_L: $L_1 = \frac{Q_{XL1}R_S}{\omega}, L_2 = \frac{Q_{XL2}R_L}{\omega}$

In order to demonstrate the practical applicability of the matching chart, a numerical matching example is given. In the example, a source impedance of

$Z_S = 100 - 300j$ is to be matched to a load impedance of $Z_L = 50 - 100j$ at $f = 60\,GHz$. The quality factors calculated from the source and load impedances are $Q_S = 3$ and $Q_L = 2$, respectively.

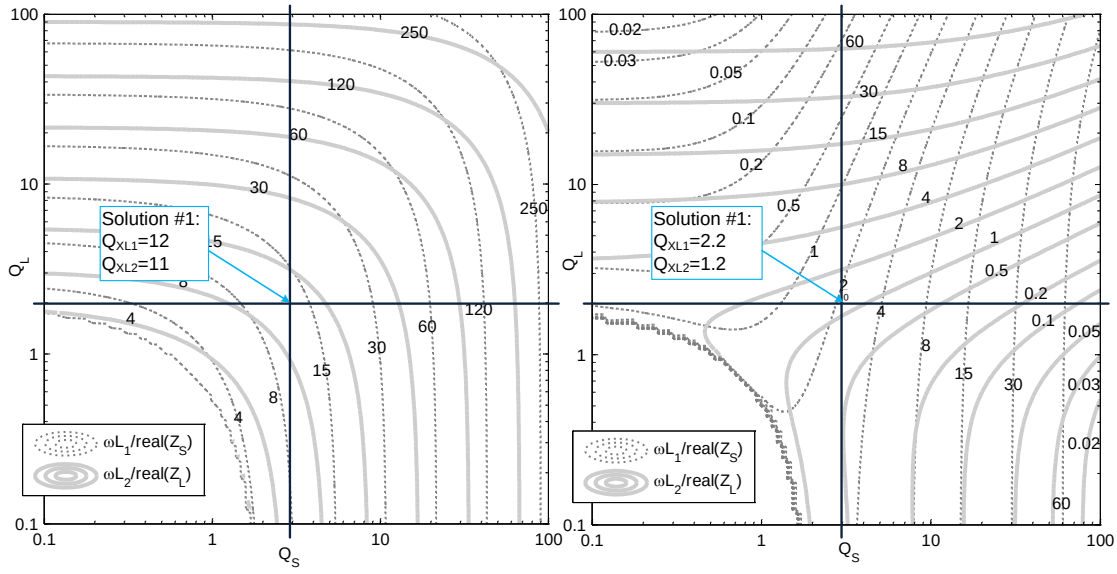


Fig. 87: An example of the matching procedure for $Z_S = 100 - 300j$ *and* $Z_L = 50 - 100j$.

By finding the intersection of $Q_S = 3$ and $Q_L = 2$ lines on the chart of Fig. 87, values of $Q_{XL1} = 2.2$ and $Q_{XL2} = 1.2$ are extracted (solution #1). Based on these values, the source and load resistances, together with the operating frequency, the magnitudes of the transformer inductors, $L_1 = 580\,pH$ and $L_2 = 160\,pH$ are found. In the same manner, using solution #2, values of $L_1 = 3.5\,nH$ and $L_2 = 1.6\,nH$ are obtained; values much larger than those obtained by solution #1 and not very practical in an integrated circuit at $60\,GHz$ and so solution #1 will be used.

These results are verified using a CAD simulation tool. The transformer was modeled by ideal coupled inductors, with a coupling coefficient k, loaded by Z_L and driven by a source Z_S (Fig. 88.a). The return loss is plotted for both

solutions #1 and #2 (Fig. 88.b and Fig. 88.c). It can be seen that for $k = 0.8$ (the value of k used for the matching chart on Fig. 86) an exact matching is achieved at $60\ GHz$. However, since prior to the actual transformer design the exact value of k cannot be accurately predicted, it is valuable to see the sensitivity of the solution to variations in the magnetic coupling coefficient.

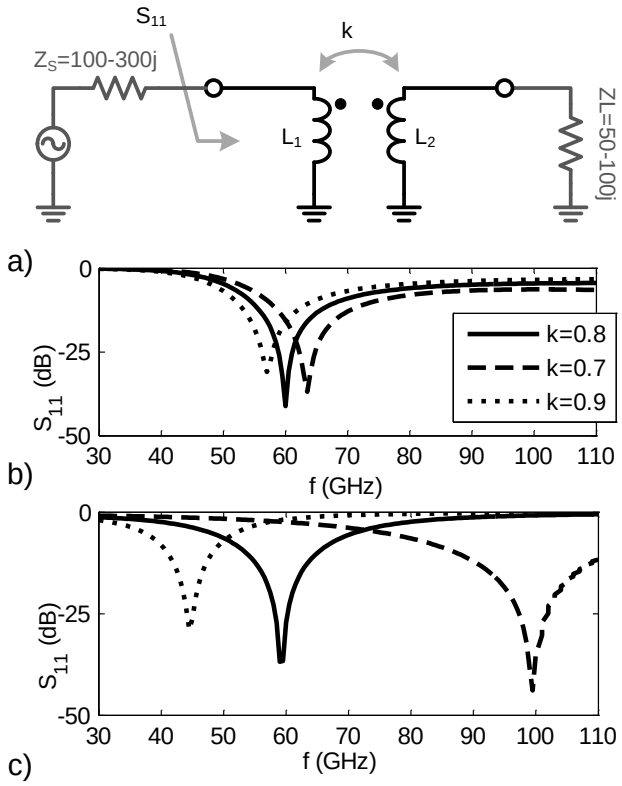


Fig. 88: a) A transformer test bench schematics. b) S_{11} *for solution #1.* $L_1 = 580\ pH, L_2 = 160\ pH$ *with different values of* k*. c)* S_{11} *for solution #2.* $L_1 = 3.5\ nH, L_2 = 1.6\ nH$ *with different values of* k*.*

The return loss for both of the solutions was also simulated under slight deviations of k. Plots for $k = 0.7, k = 0.9$, in addition to $k = 0.8$, while using the original inductor values are presented on Fig. 88. It can be seen that with the transformer designed by solution #1, the resonance frequency shifts by only 5% from its original value, while with solution #2 it shifts by more than 50%.

Since the proposed method aims to supply a starting point for the design flow, solution #2 again proves to be less practical. For these reasons, only solution #1 only will be used.

8.2.2 EQUALIZATION OF INDUCTORS

Implementation of integrated transformers requires exact tuning of the inductors to achieve the correct winding ratio, quality factor, magnetic coupling, high SRF and inductors sizing. All this is done under a limitation of finite metal layers, via parasitics and by inherited physical asymmetry resulted by large winding ratios and the use of underpasses with lower metal layers. Large inductors, with large winding ratio, N, result in additional design difficulties such as degradation of the transformer quality factor [66] and the self-resonance frequency (SRF) [68]. In order to simplify the design flow and increase the accuracy of the transformer, it is often desirable to use small inductors with low winding ratio. The proposed matching chart can be used to easily review the design possibilities, and the modifications required to balance (or equalize) the transformer (i.e.. $L_1 = L_2$). For $L_1 = L_2$:

$$\frac{Q_{XL1}}{Q_{XL2}} \equiv \frac{\omega L_1 / Re\{Z_S\}}{\omega L_2 / Re\{Z_L\}} = \frac{Re\{Z_L\}}{Re\{Z_S\}} \qquad \textit{Eq. 18}$$

According to Eq. 18, and based on the values of the previous example: $Re\{Z_L\}/Re\{Z_S\} = 0.5$. This ratio will be used in the following discussion.

The set of points with $Q_{XL1}/Q_{XL2} = 0.5$ is marked on the matching chart (Fig. 89) by a grey line. To equalize the inductors, the original point must be shifted toward any location on the grey line by means of alternating Q_S and/or

Q_L without changing the real part of the source/load impedances. Two cases are demonstrated: option A – increasing Q_L to the value of ~ 4.6, and option B – decreasing Q_S to the value of ~ 1.2. To increase Q_L from 2 to 4.6 (Fig. 89 option A) at $60\,GHz$ without changing the real part of Z_L, an additional capacitor of $21\,fF$ is added in a series to the load. Having done that, the new values of the cross quality-factor of L_1 and L_2 are $Q_{XL1} = 1.55$ and $Q_{XL2} = 3.1$, leading to $L_1 = L_2 = 410\,pH$. Decreasing Q_S without changing the real part is possible only by adding a series inductor or an inductive transmission line. To reduce Q_S to the value of 1.2 (Fig. 89 option B) a series inductor of $480\,pH$ is required. Based on option B, the new values of cross quality-factors are $Q_{XL1} = 0.9$ and $Q_{XL2} = 1.8$, leading to $L_1 = L_2 = 240\,pH$.

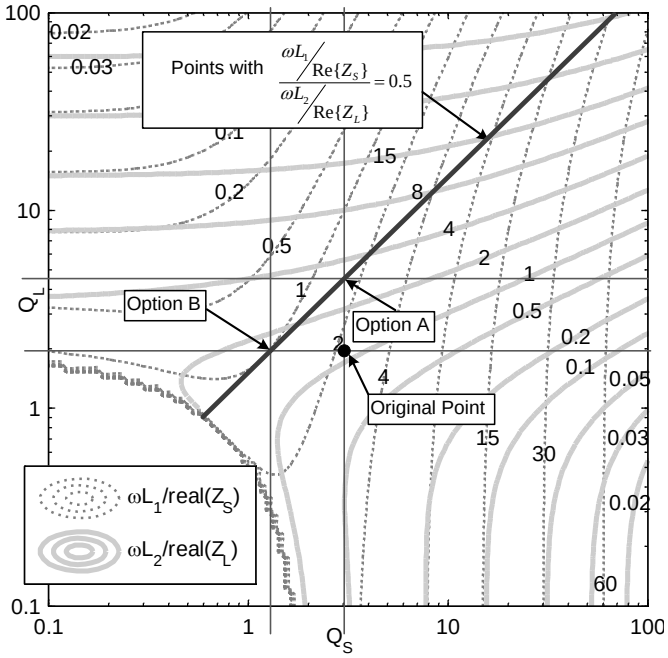


Fig. 89: Inductors equalization process.

The plot of the return loss of the equalized transformer is presented on Fig. 90. Both options yield matching at $60\,GHz$. Option B requires a smaller

transformer at the expense of an additional inductor, while option A required only a small additional capacitor. It is interesting to note that the matching bandwidth of option B is larger due to the smaller quality factors involved. This technique allows the designer to control not only the transformer sizing and the winding ratio but also the desired matching bandwidth.

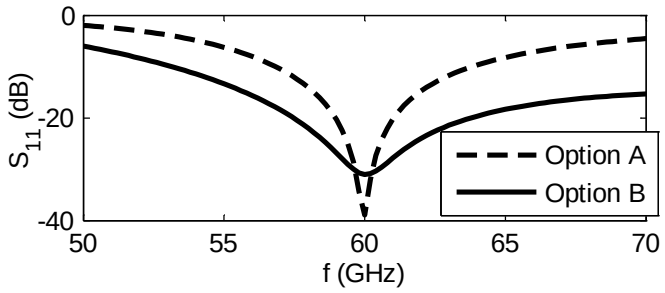


Fig. 90: Return loss for matching with option A and option B inductors equalization.

8.2.3 TRANSFORMER PARASITICS

Since the proposed method was based on ideal inductors, it is important to review the impact of a finite inductor quality factor Q_{L1} and Q_{L2}. For example, an L_1 inductor with a finite Q_{L1} contributes a series resistance R_{L1} connected in series to R_S. In order to neglect this resistance, R_S should be much greater than R_{L1}, or $Q_{L1} \gg Q_{XL1}$.

Silicon spiral inductors have two main loss mechanisms – resistive loss in the inductor trace metal and conductive loss in the silicon substrate. At low GHz frequencies the substrate loss is significant and may even dominate the achievable quality factor [64, 78]. As frequencies increase into the mm-wave region and typical inductors are smaller in value and area, substrate loss

becomes less compared with metal resistive loss, especially when including the skin effect. Extensive work has been done on the optimization of the quality factor and the SRF, [65, 79, 80], offering methods such as decreasing the turns number [66, 81], differential topologies [82, 83], thicker metals [68, 84] and substrate shielding [75] to prevent the inductor quality factor degradation. Typical values of inductor quality factors feasible using a silicon process are about $10-15$ in the lower GHz range [85], maintaining similar order of magnitude up to $110\,GHz$ [70]. A quality factor above 30 at $60\,GHz$ has been also reported [75]. Although the quality factor and the SRF of a transformer are higher than stand-alone inductors [76], low Q values can degrade the insertion loss, approximated by the expression $IL \approx 1-2/\sqrt{kQ_{L1}Q_{L2}}$, [85]. Typical inductor parameters of $k=0.8$ and $Q_{L1}=Q_{L2}=10$ would yield a $1\,dB$ insertion loss.

The demand that $Q_{L1} \gg Q_{XL1}$ can be relaxed at the mm-wave regime as the quality factor of a capacitive impedance decreases with frequency. At lower frequencies, where the assumption of $Q_{L1} \gg Q_{XL1}$ is not necessarily valid, a two-step iteration process can be used. The first iteration step is performed assuming ideal inductors. Q_S and Q_L are calculated based on the original source and load impedance values, and Q_{XL1} and Q_{XL2} are extracted from the matching chart. The values of L_1 and L_2 are then calculated. The values of $L_{1,2}$ together with the typical $Q_{L1,2}$ is used to estimate the inductor series resistance $R_{L1,2}$, which in turn, will be added in series to the source and the load resistance, changing $Q_{S,L}$ to $Q'_{S,L}=Q_{S,L}R_{S,L}/\left(R_{S,L}+R_{L1,2}\right)=Q_{S,L}R_{S,L}/R'_{S,L}$. The new values of $Q_{S,L}$, i.e. $Q'_{S,L}$, are now used to find the updated values of $Q_{XL1,2}$, i.e. $Q'_{XL1,2}$, and consequently the updated inductors $L'_{1,2}$.

The convergence process can be demonstrated by a numerical example. In

this example, the two iteration method is used to match a $Q_S = 60$ source impedance to $Q_L = 60$ load impedance by a transformer designed using a process with a typical inductor quality factor of $Q_{L1,2} \approx 10$. In the first iteration, ideal inductors are assumed. $Q_{S,L} = 60$ yields $Q_{XL1,2} = 40$ (Fig. 86). Consequently, $\omega L_{1,2} = Q_{XL1,2} \cdot R_{S,L}$. Based on the inductor quality factor, the parasitic resistance $R_{L1,2}$ is calculated: $R_{L1,2} = \omega L_{1,2}/Q_{L1,2} = Q_{XL1,2} \cdot R_{S,L}/Q_{L1,2} = 4R_{S,L}$. This resistance is assumed to be absorbed into the source and the load to maintain the ideal inductors regime, yielding the new $Q_{S,L}$, i.e. $Q'_{S,L} = Q_{S,L}R_{S,L}/(R_{S,L} + R_{L1,2}) = Q_{S,L} \cdot R_{S,L}/R'_{S,L} = 0.2Q_{S,L} = 12$. Using $Q'_{S,L}$ with the matching chart produces $Q'_{XL1,2} = 7$ and consequently $\omega L'_{1,2} = Q'_{XL1,2}R'_{S,L} = \frac{7}{40}Q_{XL1,2} \cdot 5R_{S,L} = \frac{7}{8}\omega L_{1,2}$.

The example suggests an error of just 12.5% in the inductors values between the first iteration, based on infinite $Q_{L1,2}$, and the second iteration. The reader is encouraged to perform a third iteration to verify that a convergence has been achieved.

8.2.4 ADMITTANCE NOTATION

In addition to the impedance matching functionality, a transformer is often used to provide DC bias to the stage. In such cases a series capacitor cannot be used to increase the port quality factor as it acts as a DC block (though in principle a series capacitance can be implemented as a series inductor above its SRF [86]). A parallel reactive element can also be used to change the port quality factor, but it does not naturally fit into our impedance-based matching methodology. To extend the chart to handle parallel elements, an admittance-based representation could also be developed.

For a given source impedance $Z_S = R_S - jQ_sR_S$, the real part of its admittance is $Re\{Y_S\} = 1/(R_S(1+Q_S^2))$. Hence:

$$\omega L_1 \cdot Re\{Y_S\} = Q_{XL1} \cdot \frac{1}{1+Q_S^2} \qquad \textit{Eq. 19}$$

And similarly:

$$\omega L_2 \cdot Re\{Y_L\} = Q_{XL2} \cdot \frac{1}{1+Q_L^2} \qquad \textit{Eq. 20}$$

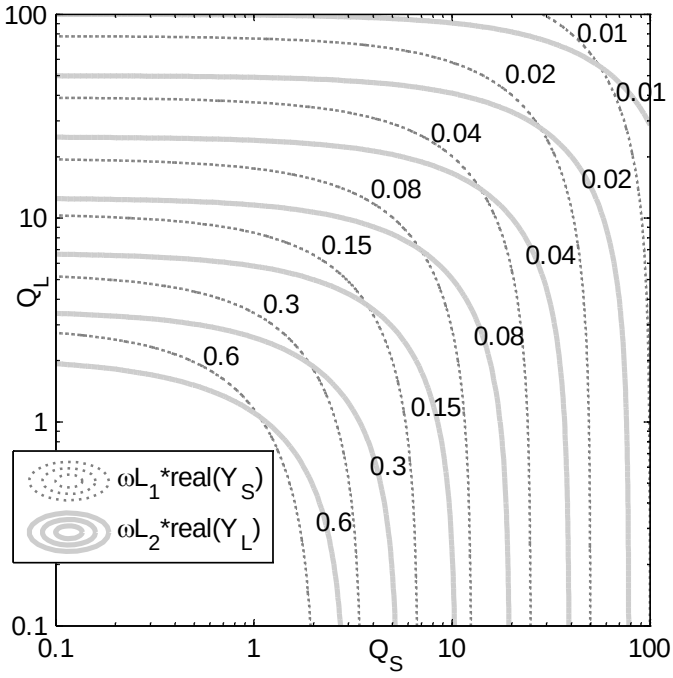


Fig. 91: Admittance matching chart: $\omega L_1 \cdot Re\{Y_S\}$ *and* $\omega L_2 \cdot Re\{Y_L\}$ *contours vs.* Q_L *and* Q_S *for* $k = 0.8$*. (solution #1 of Eq. 15).*

Equations Eq. 19 and Eq. 20 are used to plot an equivalent admittance notation matching chart as shown in Fig. 91. The contour values suggest that large ratios of $\omega L_1 Re\{Y_S\}$ to $\omega L_2 Re\{Y_L\}$ cannot be achieved. This means that additional series components cannot be used to equalize the transformer, but they can be used to modify the Q_S and Q_L and thus modify the matching

bandwidth and the transformer sizing.

The quality factor of the load and source stay the same whether they are treated as impedance or admittances. As a result, the matching charts for impedance (Fig. 86a) and admittance (Fig. 91) have the same axis and are easily interchangeable and easy to use when adding both parallel and serial elements to control the transformer sizing and matching bandwidth.

8.3 View of Matching on a Smith Chart

For a community which is very familiar with the Smith chart as a tool for impedance matching, it is interesting to visualize the impedance matching process with a transformer on a Smith chart and understand its limitations.

The operation of the coupled inductors transformer can be viewed according to the block representation of Fig. 85. First, the load impedance is transformed using an ideal $N{:}1$ transformer. This transformation does not change the quality factor of the reflected Z_L, so N simply moves the load impedance along the corresponding equi-Q curve. Inductors αL and L are set to bring Y_2 (Z_L after $N{:}1$ transformation) from the quality-factor line Q_L (in the bottom half of the Smith chart, i.e. $+Q_L$) to the quality factor line $-Q_S$ (i.e. Q_S at the upper half, corresponding to Z_S^*). As shown in 8.5, the value of the normalized inductor impedances $\tilde{Z} = \omega\alpha L/R_S$ and $\tilde{Z}/\alpha = \omega L/R_S$ are determined solely by Q_L, Q_S (for a given k). Based on that, the proposed matching process can be also viewed on a Smith chart. Using the Smith chart for transformer impedance matching purposes, however, is not a one-step solution, as with the proposed graphical tool, and requires a more iterative approach.

Choosing $Z_0 = R_S$, the normalized conjugate of the source impedance is located at $\tilde{Z}_S^* = 1 + jQ_S$ (Fig. 92). The algorithm states the following: First, $\tilde{Z}_S^*$ is marked on a unity resistance circle with imaginary value of Q_S. For an arbitrary point $\tilde{Z}_i = Z_i/R_S$ on a unity impedance circle, the distance between $\tilde{Z}_S^*$ and $\tilde{Z}_i$ equals $Q_s - Q_i = {}^{\omega\alpha L}/_{R_S} = \tilde{Z}$ (red arrows path), while the distance between $\tilde{Z}_i$ and the crossing point of the constant $Re\{\tilde{Y}_i\}$ circle with the Q_L line (green arrows path), namely $\tilde{Y}_2$, equals ${}^{R_S}/_{\omega L} = {}^{\alpha}/_{\tilde{Z}}$ (Fig. 92). Since $\tilde{Z} \cdot {}^{\alpha}/_{\tilde{Z}} = \alpha$, and for $k = 0.8$, $\alpha = 0.5$, a point $\tilde{Z}_i$ must be found in a way to satisfy the requirement on the two paths product (the black and the grey one - Fig. 92) to be equal 0.5.

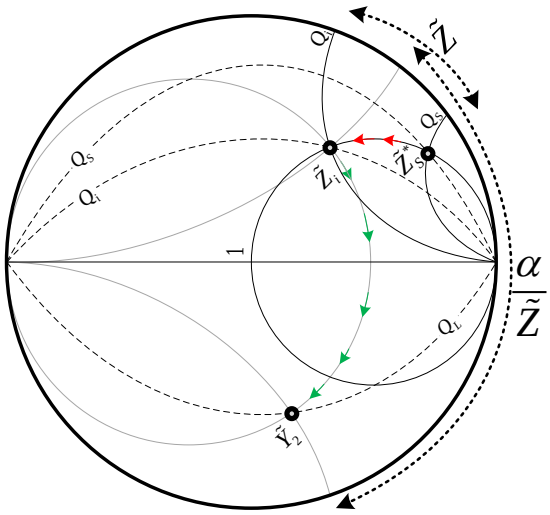


Fig. 92: Transformer matching process using a Smith Chart.

To find $\tilde{Z}_i$ an initial guess is required, followed by several correction steps until final convergence. Once completed, the value of $\tilde{Z}$ is extracted and the

value of L_1 is calculated using $L_1 = {\tilde{Z}R_S}/{\omega(1-k^2)}$.

To find L_2 one must first find $N^2 = Re\{Z_2\}/Re\{Z_L\}$ ($Z_2 = 1/Y_2$ is graphically obtained from the Smith chart after successfully finding $\tilde{Z}_i$). Finally, $L_2 = k^2 L_1 / N^2$ completes the process. It is therefore clear that matching using the Smith chart is potentially possible but not very easy or intuitive, which really motivated this work.

8.4 Practical Transformer Verification

In this section, a practical case-study is examined. Two CMOS 65nm differential buffers are matched using a transformer at a $120\,GHz$ frequency. The transformer was designed based on the inductor parameters extracted from the matching chart and verified using an Agilent Momentum electromagnetic simulator. Later, the matching was validated again using the transformer full electromagnetic model to assess the accuracy of the design.

At this current example, a source of $Z_{out1} = Z_S = 10 - 55j$ is matched to a $Z_{in2} = Z_L = 20 - 104j$ at a frequency of $120\,GHz$ (Fig. 93.a). Those values represent the single ended impedance (half of the differential one), leading to quality factors of $Q_S = 5.5$ and $Q_L = 5.2$. Using the matching chart of Fig. 86 (solution #1), one can obtain the normalized inductor impedances of $Q_{XL1} = 3.3$ and $Q_{XL2} = 3$. Extracting the inductor values leads to $L_1 = 43.7pH$ and $L_2 = 79.6\,pH$ – single ended values (half of the transformer) and a coupling factor $k = 0.725$.

A monolithic transformer was designed using a CMOS 65nm process and verified using Agilent Momentum simulator (Fig. 93.b). The top thick metal

(ME9) was used to implement L_1 in a single symmetrical loop and ME8 was used to implement L_2 with an additional smaller loop to achieve the larger inductance. The transformer parameters, extracted from the transformer Z-matrix, were compared with the target values for validation. The final design demonstrate the desired inductors values with a magnetic coupling of $k = 0.725$ (Fig. 93.b), slightly lower then $k = 0.8$ used for the matching chart. Finally, the matching was verified by measuring the return loss as seen by the output of Buffer 1 (Fig. 93.c). The return loss plot demonstrates about $-17\,dB$ matching at $123\,GHz$, a 2.5% deviation from the target frequency, mostly attributed to the different than assumed coupling factor, which could also be refined by designing more symmetrical transformer with lower winding ratios.

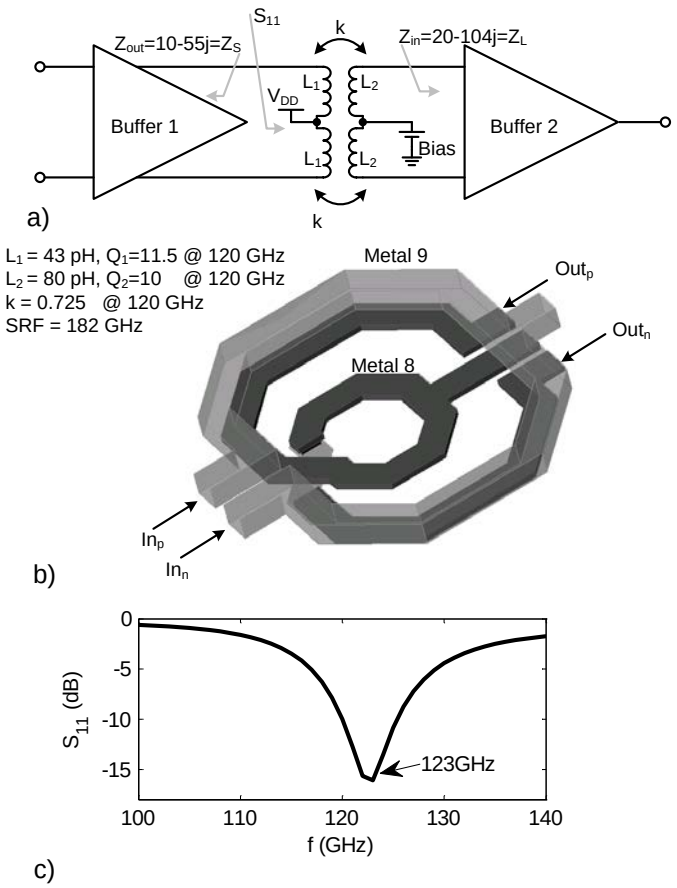


Fig. 93: Amplifier interstage impedance matching using a practical

transformer. a) System blocks schematics, b) Transformer layout and parameters, c) Return loss after matching.

8.5 Matching Chart Derivation

The ideal $N{:}1$ transformer reflects the load impedance multiplied by N^2, preserving its quality factor, as described by Eq. 21. Shifting to an admittance notation leads to Eq. 22.

$$Z_2 = N^2 Z_L = N^2 R_L - jN^2 Q_L R_L \equiv R_2 - jQ_L R_2 \qquad \textit{Eq. 21}$$

$$Y_2 = \frac{1}{Z_2} = \frac{1}{R_2} \cdot \frac{1 + jQ_L}{1 + Q_L^2} \equiv G_2 + jQ_L G_2; \;\; G_2 > 0 \qquad \textit{Eq. 22}$$

To satisfy impedance matching one shall equate $Z_i = 1/Y_i$ (Fig. 85) while expressing Z_i in terms of Z_S^* to Y_i in terms of Y_2:

$$Z_i = Z_S^* - j\omega\alpha L = R_S + j(Q_S R_S - \omega\alpha L) = \frac{1}{Y_2 + \frac{1}{j\omega L}} = \frac{1}{Y_i} \qquad \textit{Eq. 23}$$

Substituting Y_2 Eq. 22 into Eq. 23 and equating the real and the imaginary parts yields:

$$\begin{cases} G_2 = \dfrac{R_S}{R_S^2 + (Q_S R_S - \omega\alpha L)^2} & \textit{Eq. 24} \\ Q_L G_2 - \dfrac{1}{\omega L} = \dfrac{-Q_S R_S + \omega\alpha L}{R_S^2 + (Q_S R_S - \omega\alpha L)^2} & \textit{Eq. 25} \end{cases}$$

Substituting G_2 from Eq. 24 into Eq. 25 and multiplying both hands of the equation by R_S yields a quadratic equation in terms of L,Eq. 26. It is interesting to note that the expression $\tilde{Z} \equiv \omega\alpha L/R_S$ is the normalized impedance of the inductor αL on a Smith chart with $Z_0 = R_S$, where the normalized Z_S^* is located on the $Re\{\tilde{Z}_S^*\} = 1$ circle, and $Im\{\tilde{Z}_S^*\} = Q_S$.

$$\frac{Q_L}{1 + \left(Q_S - \dfrac{\omega\alpha L}{R_S}\right)^2} - \alpha\frac{R_S}{\omega\alpha L} = \frac{-\left(Q_S - \dfrac{\omega\alpha L}{R_S}\right)}{1 + \left(Q_S - \dfrac{\omega\alpha L}{R_S}\right)^2} \qquad \textit{Eq. 26}$$

The expression $Q_s - \tilde{Z}$ is Q_i, the quality factor of Z_i. Modifying Eq. 26 by replacing $\omega\alpha L/R_S = \tilde{Z}$ and solving it in respect to $\tilde{Z}$, one obtains two solutions:

$$\tilde{Z}_{1,2} = \frac{2\alpha Q_S + Q_S + Q_L}{2(\alpha + 1)} \mp \frac{\sqrt{(2\alpha Q_S + Q_S + Q_L)^2 - 4(\alpha^2 + \alpha)(1 + Q_S^2)}}{2(\alpha + 1)} \qquad \textit{Eq. 27}$$

Equation Eq. 27 suggests that the value of $\tilde{Z}$ depends solely on the quality factors of the source and load impedances: Q_S and Q_L, and on the magnetic coupling factor, k. The actual values of the source and the load impedance does not play any role. Moreover, for a given $\tilde{Z}$, the value of L_1 can be extracted relying on the value of R_S, and is independent of R_L. Recalling that $\tilde{Z} = \omega\alpha L/R_S = \omega(1 - k^2)L_1/R_S$ yields Eq. 28.

$$\frac{\omega L_1}{R_S} = \frac{\tilde{Z}}{1-k^2} \equiv Q_{XL1} \qquad \textit{Eq. 28}$$

The next step is to find the value of L_2. Using $G_2 = 1/\left(R_2(1+Q_L^2)\right)$ from Eq. 22 on Eq. 24, while keeping in mind that $Q_i = Q_s - \tilde{Z}$, Eq. 29 is derived.

$$\frac{R_2}{R_S} = \frac{1+Q_i^2}{1+Q_L^2} \qquad \textit{Eq. 29}$$

Replacing R_2 by its definition: $R_2 = N^2 R_L = k^2 R_L L_1/L_2$, Eq. 21, yields $R_2/R_S = k^2 L_1/L_2 \cdot R_L/R_S = k^2 \cdot \omega L_1/R_S \cdot R_L/(\omega L_2)$.

As the value of $\omega L_1/R_S$ has been already calculated in Eq. 28 while the ratio R_2/R_S is given by Eq. 29, it is possible to express the value of $\omega L_2/R_L$ as a function of the load and the source quality factor and a magnetic coupling coefficient Eq. 30.

$$\frac{\omega L_2}{R_L} = \frac{\tilde{Z}}{\alpha} \cdot \frac{1+Q_L^2}{1+Q_i^2} \equiv Q_{XL2} \qquad \textit{Eq. 30}$$

9. Conclusions

In this research, novel InP and CMOS mm-wave ICs for high data-rate optical and wireless coherent communication have been designed, manufactured and tested as a stand-alone IC and within a communication system.

In the area of optical communication three main ICs were demonstrated:

- A BPSK receiver IC with a $\pm 50\,GHz$ frequency detection range and a two-stable states phase detection characteristic was developed. The fully digital operation mode disables the IC dependency on the input photocurrents and increases the robustness of the design. For the first time, a highly integrated homodyne OPLL-based, DSP free, coherent optical receiver has been demonstrated. The OPLL system has been realized within a $10 \times 10\,mm^2$ area, with a closed loop bandwidth of $1.1\,GHz$ and a hold-in range of $30\,GHz$, that became possible by achieving a $120\,ps$ loop delay. The BPSK receiver based on the Costas loop exhibits error-free ($BER < 10^{-12}$) up to $35\,Gb/s$ and $BER < 10^{-7}$ for $40\,Gb/s$ with consuming less than $3\,W$ power. It might be a promising option for coherent optical receivers in short or mid distance optical communication.
- A novel broadband $\pm 20\,GHz$ optical frequency synthesis IC. The all-digital mixer topology eliminates the dependency on input photocurrent, increases the offset locking range, and improves the

design robustness by shifting to a digital domain. The IC, comprised of a single side band mixer and a Quadricorrelator PFD with frequency acquisition range up to $\pm 40\ GHz$. A full integration of the mixer with the PFD drastically reduces the limitation on loop delay, making larger loop bandwidths possible. In addition, system experiments with a single side-band frequency offset locking of $\pm 25\ GHz$ have been conducted.

- A coherent QPSK receiver IC for $100\ GBaud/s$ communication. The PFD of the receiver features a four stable states phase detection characteristics and a $\pm 50\ GHz$ frequency detection. The linear VG front end sports a $70\ dB\Omega$ transimpedance differential gain with $70\ GHz$ bandwidth, suitable for $100\ GBaud/s$ data rates. The first stage of the front-end is a linear Darlington RFA with a record bandwidth of a $107\ GHz$ and a $16\ dB$ differential. With a power consumption of $360\ mW$, a compression point of $-1\ dBm$ and a gain-bandwidth product of $657\ GHz$ the RFA is designed in a modular fashion, enables easily cascading additional stages and self-biased with a $-2\ V$ DC at the input ports to bias the PIC photodiodes.

  The QPSK receiver system was tested up to $10\ Gb/s$.

For wireless communication purposes, an F-band, $20.6\ Gb/s$ CMOS superheterodyne QPSK transmitter IC has been designed and measured. To the best of the authors knowledge, this is the first CMOS F-band transmitter to work above $20\ Gb/s$ data-rates. The use of ILFDs facilitates an accurate quadrature phase generation over an output frequency range of $100 - 118\ GHz$. The transmitter delivers an output power of $-5\ dBm$ at a carrier frequency of $115\ GHz$ ($-3\ dBm$ @ $111\ GHz$) with a calculated $BER = 6.4 \cdot 10^{-9}$ for a $30\ dB$

loss downconversion link. The overall IC power consumption is $280\,mW$ and the area is only $0.21\,mm^2$.

In parallel, a novel graphical tool for impedance matching using transformers was developed and demonstrated. The proposed tool enables a quick determination of the required transformer parameters to match given source and load impedances. In addition, the tool presents the designer the full span of design possibilities, trade-offs and alternatives, providing control on transformer sizing, winding ratio and matching bandwidth. The matching chart comes in dual impedance and admittance based notation to enable adjustments by using both series and parallel additional reactive components. The matching chart was validated using a numerical example and an electromagnetic simulation of a practical transformer designed using a 65nm CMOS process metal stack, showing only a 2.5% deviation from the target frequency. To complete the picture, an alternative algorithm for matching using a Smith chart was introduced as well.

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Hebrew Section

הכלי הגרפי שפותח במחקר זה הוא כלי אוניברסלי, מנורמל – ולכן ללא תלות בסוג התכנון, באימפדנסי המקור והעומס (כל עוד לא השראותיים) ובתדר התיאום. הכלי מראה למתכנן את כל מרחב האפשרויות התכנוניות העומדות לרשותו, למשל: שליטה ברוחב הסרט של התיאום, שליטה במספר הליפופים של כל סליל ויחס ההשנאה – וכתוצאה מכך בסימטריות ופשטות המימוש של השנאי (ממנו נגזר גם מקדם הצימוד). הכי הגרפי מתבסס על מודל אידיאלי של שנאי כזוג סלילים מצומדים אך במקרים של חוסר אידיאליות גבוה (מקדם טיב נמוך) פותח אלגוריתם למימוש בשני שלבים. בנוסף לכלי הגרפי, הוצגה גם שיטה למציאת התיאום באמצעות דיאגרמת סמית.

מקבילים בתחום תדרי ה- F-Band או ה- D-Band הפועלים עם מודולציות וקטוריות, המשדר המוצג בעבודה זו מומש בארכיטקטורת הטרודיין עם שתי דרגות ערבול, הראשונה ל- 40 GHz והשניה ל- 120 GHz. ישנן שתי סיבות עיקריות לבחירת טופולוגיה זו:

- ההגבר בתדרי ה- 120 GHz הוא מאוד נמוך ולכן על מנת להגביר את הסיגנל יש צורך במספר דרגות הגבר אשר מנצלות שטוח רב וצורכות הספק. לעומת זאת, טופולוגיית ההטרודיין נהנית מהגברים גבוהים יותר בתדרי ה- 40 GHz וה- 80 GHz.
- בנוסף, יצירת פאזות ה- I/Q ב- 120 GHz היא משימה הדורשת דיוק רב בתכנון הפיזי (Layout) ומספקת תחום כיוונון צר מאוד. לעומת זאת, יצירת פאזות I/Q ב- 40 GHz נעשית ע״י מחלקי תדר (Injection Locked Frequency Dividers) המוזנים ע״י סיגנל חיצוני ב- 80 GHz. בנוסף לחיווט הפשוט יותר ב- 40 GHz, ולרגישות הנמוכה יותר לאורכי הקווים, שימוש במחלקי תדר מאפשר טווח נעילה רחב יותר מבלי לפגוע בדיוק התיאום בין פאזת ה- I לפאזת ה- Q.

עבודה נוספת שנעשתה במקביל התמקדה בפיתוח כלי גרפי אוניברסלי לצורך תיאום עכבות באמצעות שנאים. ככל שטכנולוגיית ה- CMOS התפתחה, מספר שכבות המתכת גדל, ותדר העבודה עלה, כך השימוש בשנאים כסלילים מצומדים הפך לנפוץ יותר. השימוש בשנאים לצורך תיאום עכבות מאפשר הפרדת DC נוחה בין הדרגות, אספקת DC לכל דרגה בנפרד, תיאום דיפרציאלי וקיום אדמה וירטואלית. בניגוד לתיאום באמצעות קווי תמסורת ובאמצעות חוליות סליל-קבל דיסקרטיות, שם נעשה שימוש בדיאגרמת סמית׳, אין, נכון להיום, כלי מוגדר לביצוע תיאום עכבות באמצעות שנאים. גם אם ניתן לחשב מתמטית את ערכי הסלילים הנדרשים, אין למתכנן כל תובנה לגבי התוצאה או לגבי מרחב האפשרויות העומדות לרשותו.

- מזהה פאזה-תדר (Phase Frequency Detector) עם יכולת זיהוי הפרשת תדרים עד $\pm 50\,GHz$, עם רגישות לסימן ההפרש. עקום זיהוי הפאזה הינו בעל 2 או 4 מצבים יציבים לנעילה על אותות מאופנני BPSK או QPSK.
- מערבל דיגיטלי חד-אונתי (Digital Single Side Band Mixer), המאפשר למערכת להינעל על הפרש תדרים מוגדר, כולל סימן הנעילה. המערבל, מעצם היותו דיגיטלי, מאפשר טווח מאוד רחב של נעילה ($1 - 20\,GHz$) ואינו רגיש לעוצמת הסיגנל האופטי.
- מגבר טרנסאמפדנס ליניארי רחב סרט, עם בקרת הגבר, המאפשר מימוש מקלט QPSK בקצבי מידע של עד $100\,Gboud/s$.

המערכות שמומשו הן: מקלט BPSK קוהרנטי עם קצב מידע של $40\,Gb/s$, מקלט QPSK קוהרנטי עם קצב מידע של $10\,Gb/s$, ומערכת לנעילת פאזה בהפרש תדרים לצרכי פריסת מסרק WDM, אפליקציות ליצירת מקורות מילימטריים, מדידות וכיו"ב, עם יכולת נעילה בהפרש של עד $\pm 25\,GHz$.

גם בתחום התקשורת האלחוטית ישנה דרישה הולכת וגדלה לקצבי מידע גבוהים לאפליקציות כמו תחנות עגינה אלחוטיות, קולנוע ביתי אלחוטי, מחשוב ענן, בית חכם, סנכרון וכיו"ב. לא מזמן פותח תקן חדש לתקשורת ב-$60\,GHz$ (IEEE802.15c) עם רוחב ערוץ של $2.16\,GHz$. על מנת להמשיך ולהגדיל את רוחב הערוץ יש לעלות בתדר הנושא. תחום של $120\,GHz$ הינו תחום חדש, השייך ל- ISM. בתחום זה ישנו ניחות אטמוספרי יחסית נמוך של כ-$1\,dB/km$ המאפשר תקשורת קצרת טווח טובה.

המשדר במחקר זה מומש בטכנולוגיית CMOS 65nm לתחום ה- F-Band, למודולציית QPSK ונמדד בקצבי מידע של עד $20.6\,Gb/s$. בניגוד למשדרים

להתגבר על מגבלה זו יש לשאוף למזעור ולאינטגרציה מקסימלית של המעגלים הפוטוניים והחשמליים על מנת להקטין את השהיית החוג ככל הניתן.

- התדר האופטי (193 THz) גדול בסדרי גודל מרוחב הסרט של חוג נעול הפאזה (כ- 1 GHz) ולכן הפרש של חלקי אחוזים בין תדר הסיגנל הנכנס לתדר הלייזר המקומי יביא לסיגנל הפרש בתדר גדול בהרבה מרוחב הסרט של החוג, דבר היקשה בצורה משמעותית על הנעילה. אי לכך יש צורך בפיתוח מנגנונים לזיהוי תדר (בנוסף לזיהוי הפאזה) אשר יהיו מסוגלים לנעול סיגנלים אופטיים בהפרש תדרים התחלתי גבוה ככל שאלקטרוניקה מהירה יכולה לעבד (כ- 100 GHz).
- ע״מ לממש מקלטים קוהרנטים הננעלים על מודולציית BPSK או QPSK יש צורך לממש מנגנון גילוי פאזה שלא רגיש לקפיצות של 180° או 90°, כלומר מנגנון בעל 2 או 4 מצבים יציבים.
- בתקשורת רב ערוצית (WDM) יש צורך בשליטה מדוייקת במרווחים בין הערוצים. ע״מ לממש חוג נעילה בהיסט תדר (לעומת תדר זהה), על מנגנון זיהוי הפרש התדר להיות מסוגל לזהות גם את סימנו של ההפרש. ע״מ לממש מנגנון כזה יש צורך לחלץ גם את אלמנט ה- I וגם את אלמנט ה- Q של של גל ההפרש. חילוץ זה נעשה בזכות מעגלים פוטוניים מורכים יותר.
- ע״מ להקטין את הרגישות של ביצועי החוג בעוצמת הסיגנל האופטי, יש לתכנן מנגנונים לזיהוי פאזה ותדר עם הגבר קבוע שלא רגיש לזרמי הכניסה המסופקים על ידי הפוטודיודות.

המחקר מתמקד בפיתוח מעגלים משולבים חדישים מבוססי InP המאפשרים נעילת פאזה אופטית ומימוש מקלטים אופטיים קוהרנטיים. המנגנונים החדשים שפותחו הם:

תקציר

בעשורים האחרונים גדלה תעבורת האינטרנט העולמית בקצה אקספוננציאלי של 60% לשנה כאשר חלק מגורמי הצמיחה העיקריים הם וידאו מקוון ומחשוב ענן. כתוצאה מכך נעשו מחקרים נרחבים בנסיון להגדיל את יעילות וקיבולת הערוץ הן בערוצי תקשורת אופטית (בין-יבשתית) והן בערוצי תקשורת אלחוטית (אזורית, משתמשי קצה).

מחקר מעמיק בתחום תקשורת אופטית קוהרנטית החל עוד בשנות ה-80, כשהתעורר הצורך לשפר את רגישות הערוץ, אך נזנח בתחילת שנות ה-90 בגלל הקשיים הרבים במימוש, ובעיקר בעקבות המצאת המגבר האופטי מסומם הארביום (Erbium Doped Fiber Amplifier) שבזכותו פחת הצורך בשיפור רגישות הערוץ. מאז החל עידן של תקשורת לא קוהרנטית (Intradyne) בה ההמרה לתדרים נמוכים (IF) נעשית באמצעות לייזר לא נעול במקלט ולאחר מכן המידע מפוענח באמצעים דיגיטליים. שיטה זו מתאימה לתקשורת רב ערוצית למרחקים ארוכים אך דורשת ממירי אנלוג לדיגיטל ומעבדי אות דיגיטלי מהירים וחזקים. בשלהי העשור הראשון של המאה ה-21, בעקבות נפחי התעבורה ההולכים וגדלים, התעורר שוב הצורך להגדיל את קיבולת הערוץ האופטי ע״י שימוש במודולציה וקטורית. במקביל, חלה התקדמות משמעותית בכל הקשור לאינטגרציה ומזעור מעגלים פוטוניים וחשמליים, אשר איפשרה נעילת פאזה אופטית ומימוש ערוצי תקשורת קוהרנטיים למרחקים קצרים.

במימוש חוג נעול פאזה אופטי, החיוני לתקשורת קוהרנטית ישנן מספר מגבלות מהותיות:

- רוחב הסרט של החוג נעול פאזה, בגלל ההשהיה הרבה בו, קטן מרוחב הקו של הלייזר ועל כן יתקשה לשמור על נעילה. על מנת

המחקר נעשה בהנחייתם של פרופ. דן ריטר ודר׳ ערן סוחר בפקולטה להנדסת חשמל, ובשיתוף פעולה עם פרופ. מארק רודוול, אוניברסיטת קליפורניה סנטה ברברה, סנטה ברברה, ארה״ב

תודתי נתונה לטכניון – מכון טכנולוגי לישראל, ולקרן ג׳ייקובס קוואלקום על התמיכה הכספית הנדיבה בהשתלמותי

מעגלים משולבים בתדרי גלים מילימטריים בטכנולוגיית סיליקון ואינדיום-פוספיד לתקשורת אופטית ואלחוטית מהירה

חיבור על מחקר לשם מילוי חלקי של הדרישות לקבלת התואר דוקטור לפילוסופיה

אלי בלוך

הוגש לסנט הטכניון – מכון טכנולוגי לישראל

כסלו תשע״ד חיפה דצמבר 2014

מעגלים משולבים בתדרי גלים מילימטריים בטכנולוגיית סיליקון ואינדיום-פוספיד לתקשורת אופטית ואלחוטית מהירה

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