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Design and Fabrication of Sub-100 nm Base-Emitter Junctions of THz InP DHBTs

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of the requirements for the degree

Doctor of Philosophy
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Electrical and Computer Engineering

by

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Dedicated to my parents

for their love and support.

謹獻給

我的父母

Acknowledgements

It has been five amazing years since I joined Professor Rodwell's research group at UCSB. I can still vaguely recall the very first day I arrived at Los Angeles International Airport, where the adventure to doctorate degree began. Now, as I am moving towards the end of the expedition, I would like to express my gratitude to everyone who has helped me in this fantastic journey.

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Abstract

Design and Fabrication of Sub-100 nm Base-Emitter Junctions of THz InP DHBTs

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Because of their wide RF bandwidth (∼1 THz) and high breakdown voltages (BV_{CEO} >3 V), npn-$In_{0.53}Ga_{0.47}As$/InP double heterojunction bipolar transistors (DHBTs) have extensive applications in monolithic microwave integrated circuits (MMICs) such as high performance transceivers, near-terabit optical fiber link, and THz amplifiers in radar/imaging systems. The improvements in the performance of DHBTs were made possible because of device scaling. As the technology advances towards the next scaling generations, new challenges in the manufacturing techniques and the device designs are met. The purpose of this work is to provide solutions to the problems encountered in the fabrication and design of the base-emitter junction while scaling from 200 to sub-100 nm emitter width.

Two important issues regarding the base-emitter junction arises while scaling towards sub-100 nm emitter width. The process flow for the refractory emitter metal stack developed for 250-100 nm emitter width has already reached its limitation. In order to improve the transistor yield at a reduced linewidth without designing a new process flow, revisions have been made to the existing one. Employing the revised process flow, 75 nm-wide emitter is feasible. The overall transistor yield has also been improved. This increases the number of working

devices per sample, enabling thorough device analyses.

Experimentally, a reduction of current gain (β) associated with device scaling has been observed. In order to assess the causes of the reduction, the electron transport in the base is emulated by a commercial simulator. A model for DC-β at high injection current density ($25\,\mathrm{mA}/\mu\mathrm{m}^2$) was constructed by the comparison between the experimental and the simulation results. The model allows the estimation of β, which benefits the design of the future scaling generations of DHBTs.

It has been deduced from the model that the current originated from Auger recombination and lateral electron diffusion (via the surface and the bulk base semiconductor) are the dominant components that limits DC-β. To suppress the diffusion current via surface, a process flow is developed to form passivating sidewall onto the base surface. Such process flow has already been incorporated into DHBT fabrication. Moreover, new geometries for the base-emitter junction have been designed on the purpose of reducing the Auger recombination rate and lateral electron diffusion in the bulk base region. Using the model for β, the new designs could potentially improve DC-β beyond 50 if the corresponding process flow could be adequately integrated.

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Chapter 1

Introduction

Because of the escalating need for high-speed and low-power wireless communication systems at the radio-frequency (RF), high-performance transistors has been in rising demand for the past few decades. Among various transistor technologies, double-heterojunction bipolar transistors (DHBTs) offers number of advantages over its competitors. Being a vertical device, the key dimensions which determine the transit times are defined by epitaxy, whereas in planar devices such as the field-effect transistors (FETs), the dimensions are defined by lithography, which is limited by the wavelength of the photons or electrons. As a result, the current gain cut-off frequency (f_τ) of DHBTs has been rapidly improved over the years [1,2]. Because the current in DHBTs is conducted in the bulk semiconductor rather than in the surface inversion layer of a FET, the carriers are less subjected to scattering due to surface traps. This reduces the trap-induced frequency dispersion and results in lower $1/f$ noise [3].

Among the materials selections of DHBTs, npn-DHBTs based on the system of $In_{0.53}Ga_{0.47}As/InP$ has demonstrated superior performance at the near-THz regime [2]. InP DHBTs with the record current/power gain cut-off frequencies ($f_\tau/f_{\max}$) of $\sim$0.5/1 THz has been reported [4, 5], which is higher than the value reported from competing material systems such as GaAs/AlGaAs ($<$ 0.1 THz [6]), and SiGe ($\sim$0.3/0.4 THz [7–10]). Comparing with the FET approaches on RF technology, which is dominated by the high electron mobility transistors (HEMTs), InP DHBT gives higher $f_\tau/f_{\max}$ than GaN-based HEMT ($\sim$0.2/0.4 THz [11,12]). InP-based HEMTs attains similar $f_\tau/f_{\max}$ ($\sim$0.6/1.0 THz [13, 14]) as InP DHBTs, though InP DHBTs demonstrate higher open-circuit breakdown voltage, BV_{CEO} [4, 5, 15, 16]. The superior temporal response of InP

system can be attributed to the material properties. Because of high electron mobility and and large Γ-L valley separation in the conduction band of the InP collector [17], the electron could traverse at high velocity, reducing the transit times. Due to the low effective masses in both n- and p-InGaAs [17], the tunnelling probability of carriers is high, which in returns gives lower specific contact resistivity [18], decreasing the parasitic RC delays [2,3]. In addition to high $f_\tau/f_{\max}$, the wide band gap (1.4 eV) InP collector enables high BV_{CEO}, which is crucial for microwave power amplifiers [2]. Moreover, since it is based on the $In_{0.53}Ga_{0.47}As$/InP system, DHBTs are compatible with the 1.3 to 1.55 μm lightwave communication systems, which makes DHBTs favorable for optical fiber applications [19].

Because of the advantageous RF performance and the compatibility with other InP-base devices, several high performance MMICs utilizing InP DHBTs have been reported to demonstrated the potential of this technology [20, 21]. For high-resolution radar/imaging systems, power amplifiers oscillating at ∼220 GHz with high output power has been reported [22, 23]. For applications in fiber optical communication, a 1-20 GHz phase lock loops (PLLs) has been reported [24] and photonic-electronic integration for wavelength division de-multiplexing (WDM) optical communication systems has been demonstrated [25]. Such architecture has the potential to be scaled beyond the capacity of 1 Tbps [26].

In order to achieve high $f_\tau/f_{\max}$, DHBTs must be scaled epitaxially and lithographically to reduce transit times and RC delays. In addition, because the dimensions of emitter and base contact are nano-scaled, both n- and p-InGaAs are heavily doped to retain low access resistance [2]. Prior to the work reported in this dissertation, the emitter width of InP DHBTs has been successfully scaled to

sub-200 nm [27–29]. Based on this technology, half of this dissertation is dedicated to a reliable device scaling to sub-100 nm emitter width. In response to scaling, the reduction of the DC-current gain ($\beta = I_C/I_B$) has been observed experimentally among the devices at different scaling nodes [4, 30, 31]. Low β would result in a higher noise figure at the transistor level, causing more noise in microwave amplifiers and high error rate in analog ICs. In order to improve DC-β in the future scaling generations of DHBTs, another half of this dissertation is devoted to the modeling of DC-β in scaled DHBTs.

In the first half of chapter 2, the theory regarding DHBT scaling will be described. The reduction of DC-β accompanying with the scaling will be explained in the second half of chapter 2. Chapter 3 will cover the improvements in DHBT process flow which enable a reliable device scaling to 100 nm emitter width and an environments for enhanced accuracy in RF measurements. The experimental results of two samples, DHBT63B and DHBT58H, will be presented in chapter 4. TEM analysis verified the more controllable emitter process flow at the sub-100 nm emitter width node. DC characteristics of both devices shows that β reduces from 20 to 15 as the emitter width scales from 200 nm to 100 nm. According to this trend, a β <10 can be extrapolated at 75 nm emitter width assuming the current DHBT design process flow is unchanged. The devices reported in this work exhibit $f_\tau/f_{\max}$ of ∼500/700 GHz according to RF measurements, which is lower than expected. The parasitic resistance and capacitance will be analyzed to explain the discrepancy between the designed and experimental RF performance.

Using a commercial simulator, the 2-D electron transport in the base of a DHBT has been emulated, allowing the model for DC-β in DHBTs to be con-

structed [31, 32]. In chapter 5, the details regarding the current gain model will be addressed. The assumptions and parameters used in the simulation will be justified base on experimental data obtained from DHBT samples. The model indicates that DC-β in scaled DHBTs is limited by base current originated from bulk recombination and lateral electron diffusion. In order to suppress the base current and improve β, modifications to the design of base-emitter junction are proposed. The current gain in devices with the modified base-emitter junction has been computed using the established model, and will be presented at the end of chapter 5. If the modifications could be adequately integrated into DHBT fabrication, a device at sub-100 nm emitter node with simultaneously β of 50 [33] and $f_{\max}$ of 1 THz should be plausible.

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Chapter 2

DHBT Theory

In this chapter, the theory and the designs of mesa-DHBTs for THz applications will be examined from two aspects: RF and DC characteristics. The structure of the state of the art mesa-DHBT will be briefly described. The transit times and RC delays associated with the parasitic resistance and capacitance will be discussed. The expressions of two important figures of merit, current gain (H_{21}) cut-off frequency, f_τ, and the power gain (unilateral Mason's gain, U) cut-off frequency, $f_{\max}$), will be given. From the expressions, the scaling law of DHBTs to achieve higher f_τ and $f_{\max}$ will be defined. As the transistor scales, the DC-current gain (β) decreases. To investigate the decrease of β, various source of the base current will be examined.

2.1 Device Structure

A cross-section of a mesa-DHBT is shown in fig. 2.1a. The refractory metal contact, which defines the base-emitter (B-E) junction, is formed on a heavily doped n-$In_{0.53}Ga_{0.47}As$ emitter cap. The emitter cap and the n-InP emitter, encapsulated by SiN_x sidewall, are formed by a wet etch stopped at the doping graded p-$In_xGa_{1-x}As$ base, after which a self-aligned base contact is deposited on top of the base. Starting from the bottom of the base, the lightly doped n-type collector region is composed of the $In_{0.53}Ga_{0.47}As$ setback, the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ superlattice B-C grade, a δ-doping, and the InP collector. The setback beneath the base region supplies enough kinetic energy to the electrons for them to cross the B-C grade. The base-collector (B-C) junction, whose area defined by the base

contact, is formed by a wet etch terminated at the heavily doped n-type sub-collector. Finally, the collector contact are deposited on the sub-collector.

Fig. 2.1b is the top-down view a mesa-DHBTs. To isolate the devices, the sub-collector and a portion of the semi-insulating substrate in the field are wet etched. To avoid oscillation modes due to the InP substrate, the base ans the collector terminals are raised to the same plane as the emitter via metal posts on the contact pad, after which a transmission line structure is built on top of the device. Fig. 2.1d is the SEM of a device after the front end process.

The important dimensions of a DHBT is shown in fig. 2.1c. Due to symmetry, only half of the cross-section is shown. W_{E} and L_{E} is the B-E junction width and length defined by the emitter metal stack. The self-aligned base metals with a width of $(W_{\mathrm{B,cont.}} + W_{\mathrm{UC}})$ are deposited on both sides of the emitter. Because of the SiN_x sidewall, a gap (extrinsic base) is formed between the emitter and the self-aligned base contact. The distance between the emitter and the base contact is W_{gap}. The base contact penetrates the base semiconductor for a depth of $T_{\mathrm{B,sink}}$ due to the reaction between the base metal and InGaAs [1]. The width of the B-C mesa (W_{BM}) is defined by the widths of the base metal and the emitter. Due to the wet etch undercut (W_{UC}), the actual width of the base mesa is $(W_{\mathrm{BM}} - 2W_{\mathrm{UC}})$, and the base contact width is $W_{\mathrm{B,cont.}}$. T_{B} and T_{c} are the thickness of base and collector semiconductors, respectively.

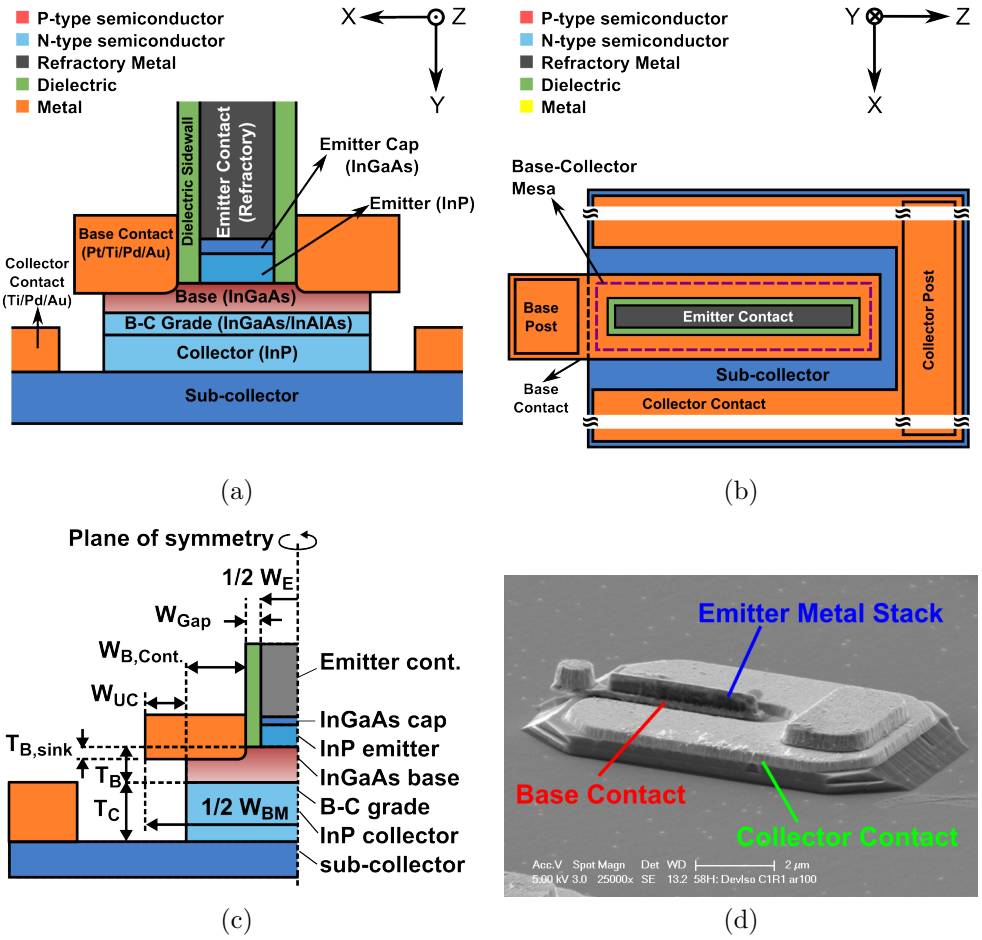

Figure 2.1: The structure of mesa-DHBTs. (a) The cross-section of a DHBT. (b) The top-down view of a DHBT. (c) The schematic showing the important dimensions in DHBTs. Only half of the device is shown due to symmetry. (d) The SEM of a experimental device after the front end process.

2.2 RF Characteristics and DHBT Scaling Laws

In this section, the design and scaling laws of THz DHBTs will be covered [2]. To understand the scaling laws, the RF characteristics of DHBTs must be addressed. The small-signal equivalent circuit of HBT based on the hybrid-π model [3] will be presented. Each delay term will be described, and the expressions of f_τ and $f_{\max}$ will be derived using these terms. By reducing the delays through device scaling, the cut-off frequencies of a DHBT can be increased.

2.2.1 Small-signal AC Equivalent Circuit

Fig. 2.2 is the small-signal equivalent circuit of a DHBT in the common emitter configuration approximated by hybrid-π model. R_{EX}, R_{BB}, and R_{C} are the access resistances of the emitter, base, and collector terminals. R_{BE} and C_{BE} are the input resistance and capacitance associated with the B-E junction. The feed back components, R_{CB} and C_{CB}, are the resistance and capacitance associated with the B-C junction. C_{CB} is separated into the intrinsic term ($C_{\mathrm{CB,i}}$), which is the component in the active region (beneath the B-E junction), and the extrinsic term ($C_{\mathrm{CB,x}}$), which accounts for the capacitance of the rest of the B-C mesa. g_{m} is the device transconductance. τ_{p} is the sum of the base transit time (τ_{B}) and collector transit time (τ_{C}). C_{CG} is the parasitic capacitance of the low-k dielectric resin (BCB) between the ground plane and the collector contact. The aforementioned parasitic terms and the delay associated with them will be discussed in the rest of the section.

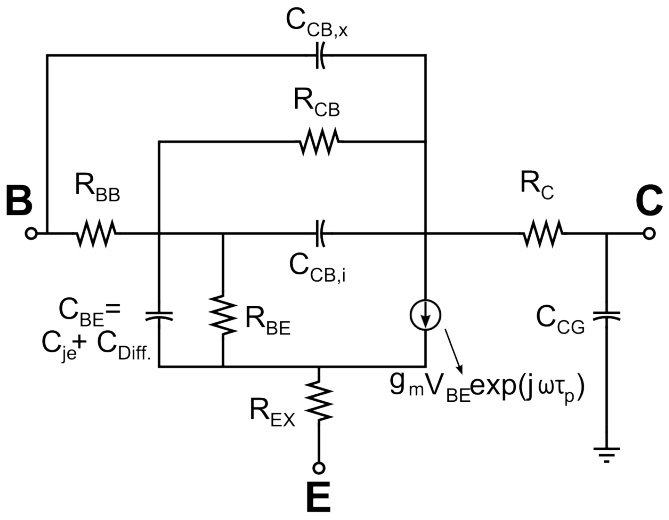

Figure 2.2: The small-signal equivalent circuit of a DHBT approximated by the hybrid-π model.

2.2.2 Base and Collector Transit Time

The base transit time (τ_{B}) and collector transit time (τ_{C}) are critical terms in determining the f_τ. Because $f_{\max}$ is determined by f_τ, it is also affected. The transit times depend on the designs of base and collector region. In this section, the relation between the base/collector transit times and the base/collector designs will be discussed.

In DHBTs, the base is usually graded (either via doping or alloy composition), causing an potential difference in the conduction band (ΔE_{C}) between the emitter side and the collector sides of the base, as shown in the band diagram in fig. 2.3. Thus, a quasi-electric field is generated, accelerating the electrons towards the collector region. In the presence of such electric field, the electron transit time in

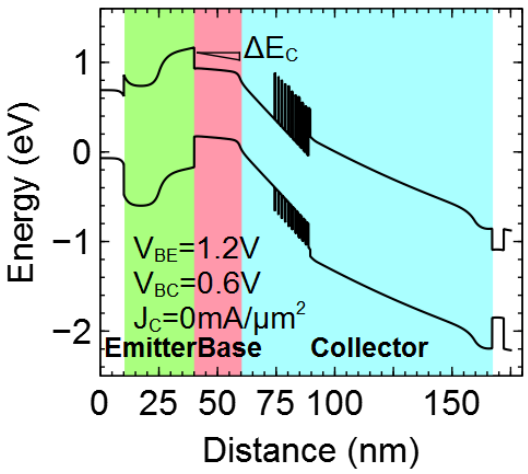

Figure 2.3: The band diagram of a DHBT in the forward active mode. The band gap narrowing effect and the space charge region in the collector are neglected.

the base region is given by [4]:

$$\tau_{\mathrm{B}} = \frac{T_{\mathrm{B}}^2}{D_{\mathrm{n}}}\frac{kT}{\Delta E_{\mathrm{C}}}[1 - \frac{kT}{\Delta E_{\mathrm{C}}}(1 - exp(-\frac{\Delta E_{\mathrm{C}}}{kT})] + \frac{T_{\mathrm{B}}}{v_{\mathrm{exit}}}\frac{kT}{\Delta E_{\mathrm{C}}}(1 - exp(\frac{\Delta E_{\mathrm{C}}}{kT})), \quad (2.1)$$

where $D_n = \mu_n kT/q$ is the electron diffusivity, k is the Boltzmann constant, and T is the temperature. v_{exit} is the velocity of the electrons leaving the base and entering the collector.

Increasing ΔE_{C} reduces τ_{B}, and hence improves f_τ and f_{max}. The UCSB DHBT designs employ the doping graded base, which generates $\Delta E_{\mathrm{C}} \approx$60 meV if the band gap narrowing effect at high doping concentration is ignored. In reality, the band gap narrowing (BGN) effect cannot be neglected [5], which decreases the ΔE_{C} induced by the doping grade. As a result, τ_{B} is underestimated. Therefore, for base designs with high doping concentration, band gap narrowing effect should

be taken into consideration when calculating τ_B. Decreasing the base thickness, T_B, also reduces τ_B. However, the base metal penetrates the InGaAs base for certain depth ($T_{B,sink}$) [1], as shown in fig. 2.1c. Thus, the B-C junction could be shorted if the base is too thin, i.e. when $T_B \approx T_{B,sink}$. According to the TEM analysis in chapter 4, $T_{B,sink}$ >5 nm for Pt/Ti/Pd/Au base contact. In order to decrease T_B without a shunt B-C junction, refractory metal should be used to replace Pt/Ti/Pd/Au for a shorter $T_{B,sink}$.

The collector transit time (τ_C) can be obtained using the charge control analysis. As more electrons are being injected into the collector due to an increase in the collector current (ΔI_C), a sheet of charge is induced at the collector side of the base (ΔQ_C). τ_C is defined as the amount of time required for ΔI_C to charge this induced ΔQ_C, i.e.

$$\tau_C = \frac{\Delta Q_C}{\Delta I_C} = \int_0^{T_C} \frac{1 - x/T_C}{v(x)}\, dx = \frac{T_C}{2v_{eff.}}\ , \tag{2.2}$$

where $v(x)$ and $v_{eff.}$ are the position-dependent and effective velocities in the collector. If electrons accumulates enough kinetic energy as they traverse through the collector, they may scatter from the Γ-valley into the L-valley in the conduction band. Because the velocity in the L-valley is lower, $v_{eff.}$ decreases and τ_C increases. For InGaAs and InP, the energy differences between the Γ- and the L-valleys, are 0.55 and 0.6 eV, respectively. Because of the large separations, the Γ-L scattering is less likely to occur in InP DHBTs [6].

2.2.3 Emitter Charging Time

The input capacitance, C_{BE}, in fig. 2.2 can be separated into two terms: the diffusion capacitance, $C_{\mathrm{Diff.}} = g\tau_{\mathrm{p}}$, and the depletion capacitance of the B-E junction, C_{je}. Because the base is heavily doped, the depletion region in the base can be neglected. The depletion term is given by:

$$C_{\mathrm{je}} = \frac{\epsilon_0 \epsilon_{\mathrm{r}} A_{\mathrm{je}}}{T_{\mathrm{E,dep.}}} \ , \tag{2.3}$$

where ϵ_0 and ϵ_{r} are the vacuum permittivity and the relative permittivity of InP ($\epsilon_{\mathrm{r}} \approx$13 [7]). $T_{\mathrm{E,dep.}}$ is the depletion region depth in the InP emitter.

The device transconductance, g_{m}, is defined as:

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{C}}}{\partial V_{\mathrm{BE}}} = \frac{qI_{\mathrm{E}}}{\eta kT} \ , \tag{2.4}$$

where η is the ideality factor. The values of g_{m} and η are usually obtained from the real part of the network expression, Y_{21}, measured at low frequency, which can be written as [8]:

$$\frac{1}{Re(Y_{21})} = R_{\mathrm{EX}} + \frac{R_{\mathrm{BB}}}{\beta} + \frac{\eta kT}{qI_{\mathrm{E}}} \ , \tag{2.5}$$

where β is obtained from DC measurements. From the slope of inverse $Re(Y_{21})$ vs. inverse I_{E}, η can be extrapolated.

The charging delay associated with C_{je} and g is

$$\frac{C_{\mathrm{je}}}{g_{\mathrm{m}}} = \frac{\eta kT}{qI_{\mathrm{E}}} C_{\mathrm{je}} \ . \tag{2.6}$$

2.2.4 Collector Charging Time

There is also the delay ,$(R_{\mathrm{EX}} + R_{\mathrm{C}} + 1/g_{\mathrm{m}})C_{\mathrm{CB}}$, in order to charge the feedback capacitance, C_{CB}. The value of C_{CB} is obtained from the imaginary part of Y_{12} in the network expression [9], i.e.

$$Im(Y_{21}) = \omega(C_{\mathrm{CB,i}} + C_{\mathrm{CB,x}}) \ . \tag{2.7}$$

C_{CB} includes terms associated with the static and the mobile (space) charge in depletion region of the base-collector junction, which can be written as

$$\begin{aligned} C_{\mathrm{CB}} &= \frac{dQ_{\mathrm{C}}}{dV_{\mathrm{CB}}} = \frac{\epsilon_0\epsilon_{\mathrm{r}}A_{\mathrm{C}}}{T_{\mathrm{C,eff}}} - \frac{\partial(I_{\mathrm{C}}\tau_{\mathrm{C}})}{\partial V_{\mathrm{CB}}} \\ &= \frac{\epsilon_0\epsilon_{\mathrm{r}}A_{\mathrm{C}}}{T_{\mathrm{C,dep.}}} - I_{\mathrm{C}}\frac{\partial\tau_{\mathrm{C}}}{\partial V_{\mathrm{CB}}} - \tau_{\mathrm{C}}\frac{\partial I_{\mathrm{C}}}{\partial V_{\mathrm{CB}}} \\ &\approx \frac{\epsilon_0\epsilon_{\mathrm{r}}A_{\mathrm{C}}}{T_{\mathrm{C,dep.}}} - I_{\mathrm{C}}\frac{\partial\tau_{\mathrm{C}}}{\partial V_{\mathrm{CB}}}, \end{aligned} \tag{2.8}$$

where A_{C} and $T_{C,dep.}$ are the area and the depletion region depth of the base-collector junction, respectively. I_{C} and τ_{C} are the collector current and transit time, respectively. Again, since the base is heavily doped, only the depletion region in the InP collector is considered and ϵ_{r} ≈13. The approximation holds when the output conductance $(\partial I_{\mathrm{C}}/\partial V_{\mathrm{CB}})$ is negligible, i.e. when R_{CB} is very high, which is the case for the reversed biased base-collector junction.

The collector of DHBTs is usually designed to be doped at the concentration where the collector is fully depleted, i.e. $T_{C,dep.} \approx T_{\mathrm{C}}$, at zero I_{C} and certain V_{CB}. Thus, at low I_{C}, the static term in eq. 2.8 remains constant. When I_{C} >0, the space charge due to injected electrons screens the positive charge in the depletion

region. Thus, as I_C increases, the electric field in the depletion region decreases in magnitude. Eventually, the field reverse its direction, inducing a barrier to electrons. This is known as the Kirk effect. The current density at the onset of the Kirk effect is given by

$$J_{C,Kirk} = \frac{2\epsilon_0\epsilon_r v_{eff.}}{T_C^2}(V_{bi} + V_{CB}) + qN_{D,C}v_{eff.} \ , \tag{2.9}$$

where V_{bi} is the built-in voltage of the B-C junction, and $N_{D,C}$ is the collector doping concentration. As J_C (or J_E) increases beyond $J_{C,Kirk}$, the effective depletion region depth in the collector reduces (base push-out), and the static term in eq. 2.8 starts to increase.

As V_{CB} increases, the electron velocity in the collector ($v_{eff.}$) decreases and hence τ_C increases, i.e. $\partial\tau_C/\partial V_{CB}$¿0 [10]. Therefore, the second term in eq. 2.8 decreases as I_C increases. Fig. 2.4 shows C_{CB} vs. J_E measured from an experimental device. As a result of velocity modulation and base push-out, when I_C increases, the overall C_{CB} first decreases. At the onset of the Kirk effect, C_{CB} reaches minimum, and then increases with I_C. Because C_{CB} is associated with multiple delay terms which determine f_τ and f_{max}, the current density when C_{CB} reaches minimum is usually close to the bias condition for peak RF performance for a given V_{CB}.

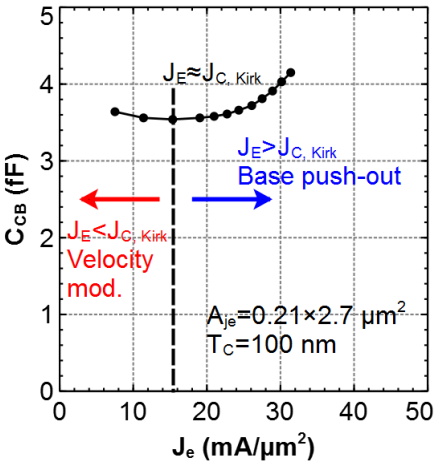

Figure 2.4: Experimental C_{CB} vs. J_{E} measured from a device with W_{E}=210 nm and T_{C}=100 nm (DHBT58H).

2.2.5 Cutoff Frequencies

The current gain cut-off frequency, f_τ, and the power gain cut-off frequency, $f_{\max}$), are two important figures of merit in evaluating the RF performance of a DHBT. The current gain cut-off frequency, f_τ, is the frequency when H_{21} drops to unity. From the summation of the transit times and the charging delays, f_τ is given by

$$\frac{1}{2\pi f_\tau} = \tau_{\mathrm{EC}} = \tau_{\mathrm{B}} + \tau_{\mathrm{B}} + \frac{\eta kT}{qI_{\mathrm{E}}} C_{\mathrm{je}} + (R_{\mathrm{EX}} + R_{\mathrm{C}} + \frac{\eta kT}{qI_{\mathrm{E}}}) C_{\mathrm{CB}} \ , \tag{2.10}$$

where τ_{EC} is the total delay between the emitter and collector contacts. If the transit times and the charging delays can be reduced, f_τ can be improved.

The power gain cut-off frequency, $f_{\max}$, is defined as the frequency when the unilateral Mason's gain becomes unity. Its value is determined by f_τ and the charging delay due to the distributed resistance-capacitance (R-C) network in the

B-C mesa. The expression of $f_{\max}$ is given by

$$f_{\max} = \sqrt{\frac{f_\tau}{8\pi(RC)_{eff.}}} \tag{2.11}$$

where $(RC)_{\text{eff.}}$ is the charging delay associated with the distributed R-C network in the B-C mesa. Fig. 2.5 is the zoomed-in cross-section of the B-C mesa showing the R-C network. $R_{\text{BE,spread}}$ is the spreading resistance beneath the B-E junction. R_{gap} is the resistance in the extrinsic base region between the B-E junction and the base contact. $R_{B,cont.}$ is the term from the network of the vertical base contact resistance, $R_{\text{B,cont. vert.}}$, and horizontal spreading resistance under the base contact, $R_{\text{B,cont. spread}}$. There is also a base metal resistance $R_{\text{B,metal}}$ along the direction of the emitter stripe, which is not shown in the schematic. Each resistance term is given by [8]

$$\begin{aligned} R_{\text{BE,spread}} &= \frac{R_{\text{sh,em}} W_{\text{E}}}{12 L_{\text{E}}} \qquad , R_{\text{gap}} = \frac{R_{\text{sh,gap}} W_{\text{gap}}}{2 L_{\text{E}}} \\ R_{\text{B,cont. vert.}} &= \rho_{\text{B,cont.}} W_{\text{B,cont.}} L_{\text{E}} \quad , R_{\text{B,cont. spread}} = \frac{R_{\text{sh,B,cont.}} W_{\text{B,cont.}}}{6 L_{\text{E}}} \\ R_{\text{B,metal}} &= \frac{R_{\text{sh,metal}} L_{\text{E}}}{6 W_{\text{B,cont.}}}, \end{aligned} \tag{2.12}$$

where $R_{\text{sh,em}}$, $R_{\text{sh,gap}}$, and $R_{\text{sh,B,cont.}}$ are the sheet resistance of the base semiconductor beneath the B-E junction, within the extrinsic base, and beneath the base contact. $R_{\text{sh,metal}}$ is the sheet resistance of the base metal, which is small when compared with other sheet resistance terms. As a result, $R_{\text{B,metal}} < 1\,\Omega$, and hence it is usually neglected. $\rho_{\text{B,cont.}}$ is the specific contact resistivity of the base contact. The transfer length of the base contact, L_{T}, is defined as $\sqrt{\rho_{\text{B,cont.}}/R_{\text{sh,B,cont.}}}$.

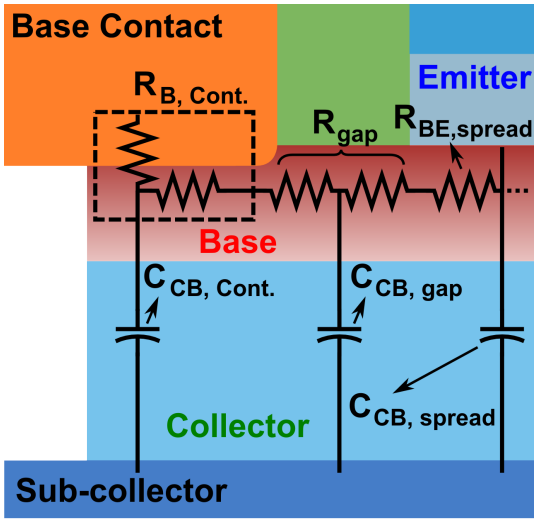

Figure 2.5: The schematic of the distributed R-C network in the base-collector mesa in a DHBT.

When $W_{\mathrm{B,cont.}} > 2L_{\mathrm{T}}$, $R_{B,cont.}$ can be written as

$$R_{B,cont.} = \frac{\sqrt{R_{\mathrm{sh,B,cont.}}\rho_{\mathrm{B,cont.}}}}{2L_{\mathrm{E}}} coth(\frac{W_{\mathrm{B,cont.}}}{L_{\mathrm{T}}}) \ , \tag{2.13}$$

For $\rho_{\mathrm{B,cont.}}$=4 Ω − μm^2 and $R_{\mathrm{sh,B,cont.}}$=800 Ω/□, L_{T} ≈70 nm. In scaled DHBTs, $W_{\mathrm{B,cont.}}$ is approaching L_{T}, and hence $R_{B,cont.}$ increases rapidly as $W_{\mathrm{B,cont.}}$ decreases. Thus, $R_{\mathrm{B,cont.}}$ is the dominant term of the base access resistance, R_{BB} [9].

The sum of the resistance terms is R_{BB}:

$$\begin{aligned} R_{\mathrm{BB}} &\approx R_{\mathrm{BE,spread}} + R_{\mathrm{gap}} + R_{\mathrm{B,cont.}} \\ &= \frac{R_{\mathrm{sh,em}}W_{\mathrm{E}}}{12L_{\mathrm{E}}} + \frac{R_{\mathrm{sh,gap}}W_{\mathrm{gap}}}{2L_{\mathrm{E}}} + \frac{\sqrt{R_{\mathrm{sh,B,cont.}}\rho_{\mathrm{B,cont.}}}}{2L_{\mathrm{E}}} coth(\frac{W_{\mathrm{B,cont.}}}{L_{\mathrm{T}}}) \ . \end{aligned} \tag{2.14}$$

As shown in fig. 2.5, C_{CB} is also separated into segments with a corresponding resistance associated with each of them. The total delay in the B-C mesa,

$(RC)_{\text{eff.}}$, is given by

$$\begin{aligned}(RC)_{\text{eff.}} &= C_{\text{CB,spread}}(R_{\text{BE,spread}} + R_{\text{gap}} + R_{\text{B,cont.}}) \\ &+ C_{\text{CB,gap}}(R_{\text{gap}}/2 + R_{\text{B,cont.}}) \\ &+ C_{\text{CB,cont.}}(\frac{1}{R_{\text{B,cont. vert.}}} + \frac{1}{R_{\text{B,cont. spread}}})^{-1} ,\end{aligned} \tag{2.15}$$

where the area for estimating $C_{\text{CB,spread}}$, $C_{\text{CB,gap}}$, and $C_{\text{CB,cont.}}$ scale with, W_{E}, W_{gap}, and $W_{\text{B,cont.}}$, respectively.

2.2.6 DHBT Scaling Law

In order to increase f_τ and f_{max} in a DHBT, the device has to be scaled in both lateral and epitaxial dimensions [11]. In this section, the scaling consideration in terms of cut-off frequencies will be discussed. A γ:1 increment in f_τ requires a γ:1 reduction in all transit times and charging delay in eq. 2.10. According to eq. 2.1, in order to reduce the base transit time, T_{B} need to be reduced approximately by $\gamma^{1/2}$:1. From eq. 2.2, a γ:1 reduction in T_{C} is necessary for the collector transit time to decrease by a factor of γ. However, decreasing T_{C} by a factor of γ causes the static term of C_{CB} in eq. 2.8 to rise by a factor of γ, which increases the collector charging time in eq. 2.10 by a factor of γ. Thus, in order to decrease the collector charging time by a factor of γ, the area of the B-C junction ($A_{\text{C}} = W_{\text{BM}}L_{\text{E}}$) must be reduced by a factor of γ^2 while the resistance terms associated with C_{CB} remain constant. For thermal and power dissipation considerations, the B-E junction area ($A_{\text{je}} = W_{\text{E}}L_{\text{E}}$) usually scales with A_{C}, and only W_{BM} and W_{E} are changed while L_{E} remains constant. As a result, the emitter

charging time in eq. 2.10 is also decreased by a factor of γ^2 if I_E remains the same. For constant I_E, the emitter current density J_E increases by a factor of γ^2 because A_{je} decreases by a factor of γ^2. Furthermore, since the emitter contact area and A_{je} are approximately the same, the specific emitter contact resistivity, $\rho_{E,cont.}$, must be decreased by a factor of γ^2.

According to eq. 2.11, in addition to the γ:1 increment in f_τ, the delay from the B-C mesa ($(RC)_{eff.}$) needs to be reduced by a factor of γ in order to improve f_{max} by a factor of γ. Since C_{CB} already need to be decreased by a factor of γ to increase f_τ, the reduction of $(RC)_{eff.}$ is achieved by keeping R_{BB} constant. From eq. 2.14, R_{BB} dominated by the base sheet resistance and contact resistance. As T_B scales to reduce τ_B, the base sheet resistance rises, increasing all terms in R_{BB}. To compensate the decrease of T_B, the doping concentration in the base must be increased. Moreover, as W_{BM} and W_E are scaled, W_{gap} and $W_{B,cont.}$ also decrease. A γ^2:1 reduction in $W_{B,cont.}$ causes $R_{B,cont.}$ to increases drastically. To prevent $R_{B,cont.}$ from rising, $\rho B, cont.$ needs to be reduced (approximately γ^2:1). This is also achieved by increasing the base doping concentration [12]. A summary of DHBT scaling laws for improving f_τ and f_{max} by a factor of γ is listed in table. 2.1 [2]

2.3 DC Current Gain of DHBT

The DC current gain (β) of a DHBT is defined as I_C/I_B. Although DC-β does not directly change the cut-off frequencies of a DHBT , when the device is

Parameters		Requirement
Base thickness	T_{B}	Decrease by a factor of $\gamma^{1/2}$
Collector thickness	T_{C}	Decrease by a factor of γ
B-C mesa width	W_{BM}	Decrease by a factor of γ^2
B-E junction width	W_{E}	Decrease by a factor of γ^2
Emitter current density	J_{E}	Increase by a factor of γ^2
Specific emitter contact resistivity	$\rho_{\mathrm{E,cont.}}$	Decrease by a factor of γ^2
Specific base contact resistivity	$\rho_{\mathrm{B,cont.}}$	Decrease by a factor $\approx \gamma^2$
Base sheet resistance	$R_{\mathrm{B,sh.}}$	Decrease by a factor of $\gamma^{1/2}$

Table 2.1: Scaling laws of DHBTs: the required change for improving f_τ and $f_{\max}$ by a factor of γ.

incorporated into circuitry, DC-β affects the efficiency and noise figure of a microwave circuit. A low DC-β would cause more noise in the RF amplifiers [13] and decreases DC-gain and precision in analog ICs [14, 15]. Therefore, high DC-β is desirable for circuit applications.

As dimensions of the devices scales to improve the cut-off frequencies, DC-β simultaneously reduces. The inverse DC-β vs. the B-E junction periphery ($P_{\mathrm{je}} = 2(W_{\mathrm{E}} + L_{\mathrm{E}})$) to area ($A_{\mathrm{je}}$) ratio measured from device with different base design is plotted in fig. 2.6. The base designs have doping graded where the highest and lowest doping concentration is at the emitter and collector side, respectively. Design I has a 25 nm thick base with doping varying from 9 to $5\times10^{19}\,\mathrm{cm}^{-3}$. Design II employs a 20 nm thick base with doping varying from 12 to $8\times10^{19}\,\mathrm{cm}^{-3}$. Design III includes a 18 nm thick base with doping varying from 14 to $9\times10^{19}\,\mathrm{cm}^{-3}$.At W_{E} $\approx$200 nm, where $P_{\mathrm{je}}/A_{\mathrm{je}}$ $\approx$10 $\mu\mathrm{m}^{-1}$, the DC-β is approximately 20. AS the device scales to W_{E}=100 nm, the DC current gain drops to $\sim$15. Eventually, when the device scales beyond 100 nm W_{E}, DC-β decreases to less than 10. Thus, it is important to understand and improve DC-β in scaled DHBTs.

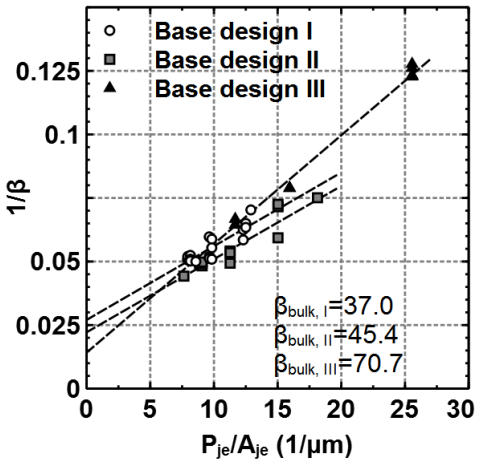

Figure 2.6: Inverse DC current gain ($1/\beta$) vs. HBT emitter periphery to area ratio ($P_{\mathrm{je}}/A_{\mathrm{je}} \approx 2/W_{\mathrm{E}}$) of experimental DHBTs with distance between base and emitter contacts (W_{gap}) ≈10 nm and different base designs. The values of β are measured at emitter current density $J_{\mathrm{E}} \approx 25\mathrm{mA}/\mu\mathrm{m}^2$.

The low DC-β is caused by the excessive base current, I_{B}. Fig. 2.7 shows the sources of I_{B}. Under bias, electrons are injected from the emitter into the base, I_{E}. Most injected electrons beneath the base-emitter junction traverse to the collector and become collector current, I_{C}. A fraction of the electrons recombine with holes, generating bulk base current, $I_{\mathrm{B,Bulk}}$. At the vicinity of emitter edge, a portion of injected electrons diffuse through the bulk base region towards the base contact. They then recombine at the contact, which leads to $I_{\mathrm{B,diff.}}$ (bulk lateral diffusion) [16].

At the p-InGaAs/dielectric interface within the extrinsic base, the surface Fermi level is pinned by donor-like interface trap states, resulting in a surface depletion region and generating the conduction band profile shown in fig. 2.8. After injected into the base, some fraction of electrons will diffuse towards this depletion region, where they will then be trapped by the high field. The trapped

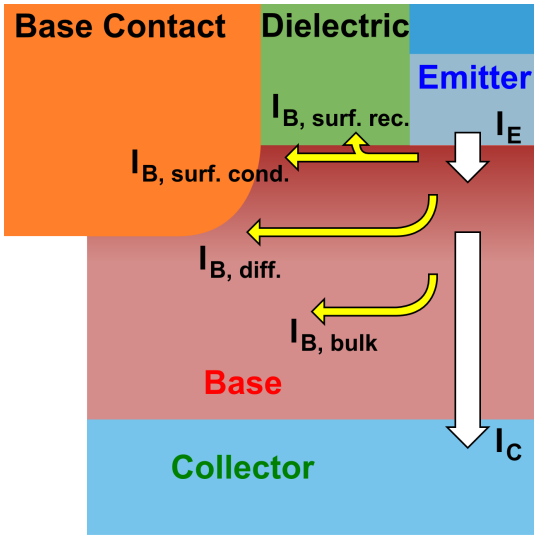

Figure 2.7: A schematic of the current components in the base of DHBTs.

electrons then diffuse laterally towards the base contact. The trapped electrons either recombine *en route* with interface trap states, leading to surface recombination current ($I_{\mathrm{B,surf.rec.}}$), or recombine after reaching the contact, contributing to the surface conduction current ($I_{\mathrm{B,surf.cond.}}$) [17, 18]. The $I_{\mathrm{B,surf.rec.}}$ and $I_{\mathrm{B,surf.cond.}}$ will be described in detail in the following context.

2.3.1 Bulk Base Current

The bulk base current, $I_{\mathrm{B,bulk}}$, was generated as the electrons (injected as I_{E}) recombines with a hole in the bulk base region. Hence, $I_{\mathrm{B,bulk}}$ scales in proportion to A_{je}, i.e. $I_{\mathrm{B,bulk}} = J_{\mathrm{B,bulk}} A_{\mathrm{je}}$, where $J_{\mathrm{B,bulk}}$ is the current density of the bulk base current.

Several recombination mechanisms in the bulk base region leads to $I_{\mathrm{B,bulk}}$. In this work, we considered three recombination mechanisms: Auger recombination, Shockley-Read-Hall (SRH) recombination , and radiative recombination. Accord-

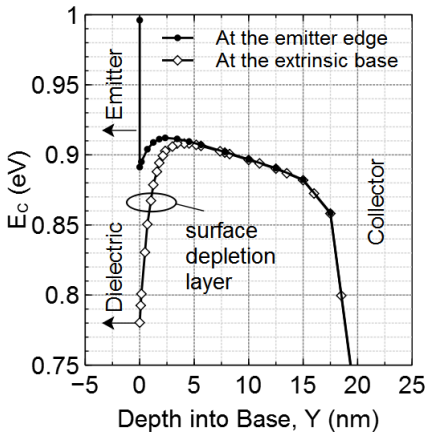

Figure 2.8: Simulated conduction band energy (E_C) at V_{BE} ≈1.2 V vs. depth into the base semiconductor at the edge of the emitter and in the extrinsic base. The simulation assumes a 20 nm thick base with doping varying from $1.2 \times 10^{20}\,\mathrm{cm}^{-3}$ at the emitter side to $8 \times 10^{19}\,\mathrm{cm}^{-3}$ at the collector side [18]. The energy is relative to the base Fermi level.

ing to the Matthiessen's rule, the total electron lifetime (τ_n) due to this three mechanisms cab be written as

$$\tau_{n,total} = \left(\frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad.}}\right)^{-1}, \tag{2.16}$$

where τ_{Auger}, τ_{SRH}, and $\tau_{rad.}$ are the lifetime of the Auger, SRH, and radiative recombination, respectively. The current gain associated with $I_{B,bulk}$, β_{bulk}, is the ratio of the electron lifetime to the base transit time [19], i.e. $\beta_{bulk} = \frac{\tau_{n,total}}{\tau_B}$

The (direct) Auger recombination is a collision process involving four states in the conduction band (VB) and the valance band (VB). There are several variants of Auger recombination. For III-V semiconductors with direct band gap, the process is depicted in Fig. 2.9 [20]. In the CCCH process, two electrons in CB collide, knocking one of them into the valence band and the other one to a

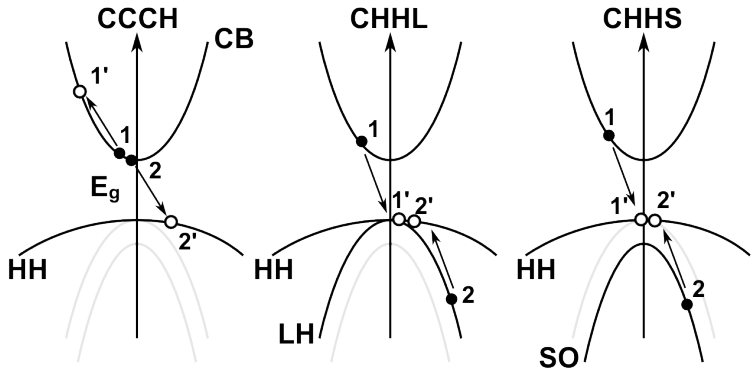

Figure 2.9: Three Auger processes in III-V semiconductors. [20]. The solid circles represent the occupied states, and the empty circles represent the empty states.

more energetic state in CB. The CHHL process involves one hole in the light hole band (LH) and one electron in CB. The CHHS, an analogy to CHHL, involves one hole in the split-off band (SO) and on electron in CB. In addition to the direct Auger processes, a phonon (phonon assisted Auger recombination) or a shallow trap (Auger recombination via shallow traps) could be involved in an indirect Auger process [20]. Nonetheless, the Auger recombination rate estimated from our experimental data includes the contributions from all processes, and isolating the components would be difficult. Hence, in this work, the contribution from the direct and indirect processes were incorporated into the same coefficients.

According to fig. 2.9, the Auger recombination rate depends on the probability of finding the occupied and empty states involved in the transition. The transition probabilities of the three processes are given by [21]

$$\begin{aligned} P_{\mathrm{CCCH}} &\approx \frac{n^2 p}{N_{\mathrm{C}}^2 N_{\mathrm{V}}} exp(-\frac{\Delta E_1 + \Delta E_2 + \Delta E_{2'}}{kT}), \quad \text{(CCCH)} \\ P_{\mathrm{CCCH}} &\approx \frac{n^2 p}{N_{\mathrm{C}}^2 N_{\mathrm{V}}} exp(-\frac{\Delta E_1 + \Delta E_{1'} + \Delta E_{2'}}{kT}), \quad \text{(CHHLandCHHS)} \end{aligned} \tag{2.17}$$

where n and p are the electron and hole densities. N_{C} and N_{V} are the effective densities of states in the conduction band and the valence band. $\Delta E_{\mathrm{i}} = E_{\mathrm{i}} - E_{\mathrm{C}}$ for states in the conduction band, and $\Delta E_{\mathrm{i}} = E_{\mathrm{V}} - E_{\mathrm{i}}$ for states in the valence band.

Because of the dependency in eq. 2.17, the Auger recombination rate is usually written in the the empirical form:

$$R_{\mathrm{Auger}} = C_{\mathrm{Auger,n}} n^2 p + C_{\mathrm{Auger,p}} n p^2 \ , \tag{2.18}$$

where $C_{\mathrm{Auger,n}}$ is the Auger coefficient of the CCCH process and $C_{\mathrm{Auger,p}}$ is the combination of Auger coefficient of the CHHL and the CHHS processes. In the case of DHBTs, the base is heavily doped and only the electrons are injected as minority carriers, i.e. $p \gg n$. Therefore, the dominating processes are CHHL and CHHS, and the term involving ($C_{\mathrm{Auger,n}}$ can be neglected.

The lifetime associated with the Auger recombination can be written as

$$\tau_{Auger} = \frac{\delta n}{R_{\mathrm{Auger}}} \approx \frac{1}{C_{\mathrm{Auger,p}} p^2} \ . \tag{2.19}$$

To estimate τ_{Auger}, it is important to obtain an accurate value of ($C_{\mathrm{Auger,p}}$. Various values of $C_{\mathrm{Auger,n}}$ and $C_{\mathrm{Auger,p}}$ have been reported in the literature for InGaAs [22–24]. However, some of the results were measured from p-i-n laser diodes (LDs), in which the electron and hole densities are the same, i.e. $p = n$. Hence, the coefficient obtained is in fact ($C_{\mathrm{Auger,n}} + C_{\mathrm{Auger,p}}$), and it is difficult to extract $C_{\mathrm{Auger,p}}$ from it. Combined coefficient ($C_{\mathrm{Auger,n}}$+$C_{\mathrm{Auger,p}}$) of $9\times10^{-29}\,\mathrm{cm}^6/\mathrm{s}$ has been reported [24]. Separated coefficients of $C_{\mathrm{Auger,n}} = 5 \times 10^{-30}\,\mathrm{cm}^6/\mathrm{s}$ and

$C_{\text{Auger,p}} = 3.6 \times 10^{-29}\,\text{cm}^6/\text{s}$ have been measured from n- and p- typed InGaAs, respectively [23].

According to the Shockley-Read-Hall (SRH) statistics [25], the net rate of recombination involving a single state follows the expression of

$$R_{\text{SRH}} = C_{\text{SRH}}(np - n_{\text{i}}^2) \ , \tag{2.20}$$

where n_{i} is the intrinsic carrier density. C_{SRH} is the SRH recombination coefficient, which is related to the capture cross-sections for electrons (σ_{n}) and holes (σ_{p}). Because σ_{n} and σ_{p} also depends on doping concentration [26], an empirical form is used to approximate the doping-dependent lifetime of SRH recombination. Using Scharfetter relation, with a reference lifetime (τ_{ref}) drawn from experimental data measured at the doping concentration ($N_{\text{ref},\tau}$), the SRH lifetime can be written as [22, 27]

$$\tau_{\text{SRH}}(N_A + N_D) = \frac{\tau_{\text{ref}}}{1 + (\frac{N_A+N_D}{N_{\text{ref},\tau}})^{\kappa}}, \tag{2.21}$$

where N_{A} and N_{D} are the acceptor and donor concentrations. The fudging factor κ is obtained from fitting multiple data points at various reference doping concentrations.

The radiative recombination rate follows the same expression as eq. 2.20, except the coefficient C_{SRH} is substituted by $C_{\text{rad.}}$. Value of $9.6 \times 10^{-11}\text{cm}^3/\text{s}$ has been reported for $C_{rad.}$ in InGaAs [28].

Fig. 2.10 is the computed electron lifetime of different recombination processes in the base of a DHBT. The Auger recombination has the shortest lifetime, and hence is the dominant recombination mechanism in the base of DHBTs. Accord-

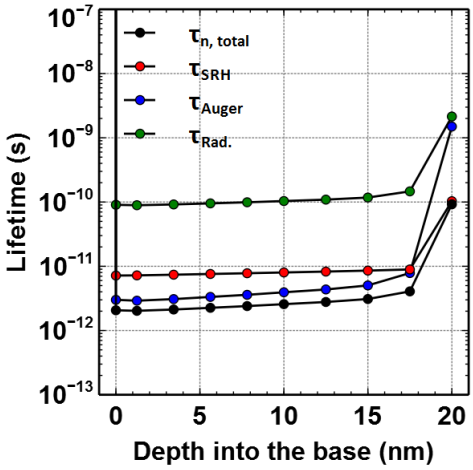

Figure 2.10: Computed electron lifetimes (Auger, SRH, radiative, and total) vs. the depth into the base of a DHBT. A 20 nm thick base with doping varying from $1.2 \times 10^{20}\,\mathrm{cm}^{-3}$ at the emitter side to $8 \times 10^{19}\,\mathrm{cm}^{-3}$ at the collector side was assumed. The emitter current density is assumed to be $27\,\mathrm{mA}/\mu\mathrm{m}^2$.

ing to the DHBT scaling laws in section 2.6, the doping concentration in the base region increases as the devices are being scaled, causing a quadratic decrease in τ_{Auger} according to eq. 2.19. Hence, in the future scaling generation DHBTs, a significant portion of base current will be contributed by Auger recombination.

2.3.2 Bulk Lateral Diffusion Current

In addition to the quasi-electric field towards the collector, the injected electrons near the edge of the B-E junction experience a lateral driving force towards the base contact induced by the density gradient. As a result, the electrons diffuse in the lateral direction, and a portion of them eventually reach the base contact. They then recombine at the contact, leading to the bulk lateral diffusion current, $I_{\mathrm{B,diff.}}$. Because the lateral component of the gradient only exists between

the B-E junction and the base contact, and is negligible elsewhere (beneath the B-E junction and the base contact), $I_{\mathrm{B,diff.}}$ originates near the edge of the B-E junction and terminates at the base contact. Therefore, $I_{\mathrm{B,diff.}}$ scales with the junction periphery, P_{je}, i.e. $I_{\mathrm{B,diff.}} = K_{\mathrm{B,diff}} P_{\mathrm{je}}$, where $K_{\mathrm{B,diff}}$ is the sheet current density of the bulk lateral diffusion current [16].

Since $I_{\mathrm{B,diff.}}$ is competing with the vertical drift-diffusion (I_{C}) for electrons, the magnitude of $I_{\mathrm{B,diff.}}$ depends on the gradients in both lateral and vertical directions. As the distance from the B-E junction to the base contact (W_{gap}) decreases for DHBT scaling, the lateral component of the density gradient becomes higher; hence $I_{\mathrm{B,diff.}}$ increases, reducing DC-β.

2.3.3 Surface Recombination and Conduction Current

At the interface between p-InGaAs and the dielectric (sidewall or native oxide), donor-like trap states exist. When occupied (capturing a hole), each trap state carries the charge of one hole. The positive charge at the interface pins the surface Fermi level and induces a depletion region [29], resulting in the conduction band profile depicted in fig. 2.8. As the electrons injected from the emitter diffuse laterally into the surface depletion region, they are trapped in the region due to the high field towards the surface. The density of the trapped electron, n_{s} depends on J_{E} and the field in the surface depletion region. The latter is determined by doping concentration near the base surface, the interface trap states density (D_{it}), and the energy of the trap states with respect to the valence band. For InGaAs, the majority of the traps are located $\sim$0.5 eV above the valance band edge [29]. The

trap states density, $D_{\rm it}$, is affected by bonding configuration at the interface, which depends on the surface treatment and the oxide/nitride formed on the surface [30]. For InGaAs terminated by Al_2O_3 deposited by the atomic layer deposition (ALD), $D_{\rm it}$ ranges from 2.5 to $5\times10^(12)\,{\rm cm}^{-2}{\rm eV}^{-1}$ when an adequate surface treatment is performed before ALD [31,32]. Nonetheless, $D_{\rm it}$ on the InGaAs base surface of a DHBT could be an order higher then these value because of the process damage to the surface and/or the contamination such as photoresist residues.

After being trapped, the electrons continue to diffuse towards the base contact because of the lateral driving force. A portion of them recombine *en route* with the trap states (surface SRH recombination), generating surface recombination current, $I_{\rm B,surf.rec.}$. Like other recombination current, the magnitude of $I_{\rm B,surf.rec.}$ depends on the surface recombination rate of electrons, which is given by

$$R_{\rm surf.SRH} = n_{\rm s}(x) v_{surf.rec.} \ , \tag{2.22}$$

where $v_{surf.rec.}$ is the surface recombination velocity (SRV) of electrons. The value of SRV depends on the interface trap state density, $D_{\rm it}$. For the InGaAs surface terminated by native oxide, SRV ranges from 10^3 to $10^4\,{\rm cm/s}$ [33].

Because only the electrons near the edge of the B-E junction can be trapped and participate in surface recombination [34], $I_{\rm B,surf.rec.}$ scales in proportion to $P_{\rm je}$, i.e. $I_{\rm B,surf.rec.} = K_{\rm B,surf.rec.} P_{\rm je}$, where $K_{\rm B,surf.rec.}$ is the sheet current density of the surface recombination current. $K_{\rm B,surf.rec.}$ can be written as $K_{\rm B,surf.rec.} = 2qW_{\rm gap}R_{\rm surf.SRH}$. The factor of 2 accounts for InGaAs surface on both sides of the emitter stripe. According to the expression, $I_{\rm B,surf.rec.}$ decreases when $W_{\rm gap}$

reduces as devices are scaled.

The rest of the trapped electrons, if not recombined with surface traps while diffusing towards the base contact, can reach the destination and recombine there, resulting in the surface conduction current [17]. Similar to $I_{\mathrm{B,surf.rec.}}$, $I_{\mathrm{B,surf.cond.}}$ also scales in proportion to P_{je}, i.e. $I_{\mathrm{B,surf.cond.}} = K_{\mathrm{B,surf.cond.}} P_{\mathrm{je}}$, where $K_{\mathrm{B,surf.cond.}}$ is the sheet current density of the surface conduction current. Analogous to the relationship between $I_{\mathrm{B,bulk}}$ and I_{C}, $I_{\mathrm{B,surf.rec.}}$ draws trapped electrons from $I_{\mathrm{B,surf.cond.}}$. Hence, the ratio of $I_{\mathrm{B,surf.rec.}}$ to $I_{\mathrm{B,surf.cond.}}$ depends on the magnitude of the lateral driving force and the SRV.

Both $K_{\mathrm{B,surf.rec.}}$ and $K_{\mathrm{B,surf.cond.}}$ are related to $n_{\mathrm{s}}(x)$. With a higher D_{it}, the surface depletion region becomes wider and more injected electron can be trapped by the surface depletion region. Thus, $n_{\mathrm{s}}(x)$ becomes larger ,and both $K_{\mathrm{B,surf.rec.}}$ and $K_{\mathrm{B,surf.cond.}}$ increase, reducing β.

2.3.4 DC Current Gain and DHBT Scaling

The total base current in a DHBT is the sum of the four components:

$$\begin{aligned} I_{\mathrm{B}} &= I_{\mathrm{B,bulk}} + I_{\mathrm{B,diff.}} + I_{\mathrm{B,surf.rec.}} + I_{\mathrm{B,surf.cond.}} \\ &= I_{\mathrm{B,bulk}} + I_{\mathrm{B,edge.}} \\ &= J_{\mathrm{B,bulk}} A_{\mathrm{je}} + (K_{\mathrm{B,diff.}} + K_{\mathrm{B,surf.rec.}} + K_{\mathrm{B,surf.cond.}}) P_{\mathrm{je}} \\ &= J_{\mathrm{B,bulk}} A_{\mathrm{je}} + K_{\mathrm{B,edge.}} P_{\mathrm{je}} \ , \end{aligned} \tag{2.23}$$

where $I_{\mathrm{B,edge.}}$ is the total current component originated from the edge of the B-E junction. $K_{\mathrm{B,edge.}}$ is the sheet current density of $I_{\mathrm{B,edge.}}$. By the definition of β the inverse current gain, $1/\beta$, can be written as

$$\begin{aligned}\frac{1}{\beta} &= \frac{1}{\beta_{\mathrm{bulk}}} + \frac{K_{\mathrm{B,edge.}} P_{\mathrm{je}}}{J_{\mathrm{C}} A_{\mathrm{je}}} \\ &\approx \frac{1}{\beta_{\mathrm{bulk}}} + \frac{K_{\mathrm{B,edge.}}}{2 J_{\mathrm{C}} W_{\mathrm{E}}},\end{aligned} \tag{2.24}$$

where J_{C} here is the collector current density at the base side of the collector. Because most of the current spreading occurs in the bulk collector region, J_{C} is associated with A_{je}. In scaled DHBT L_{E}:W_{E} >10, and hence the approximation holds.

In the plot of $1/\beta$ vs. $P_{\mathrm{je}}/A_{\mathrm{je}}$ measured from DHBTs, a linear relationship should be observed. The interception is the inverse β of a device with a very wide emitter, from which β_{bulk} can be extrapolated because the edge current component is negligible. The edge sheet current density, $K_{\mathrm{B,edge.}}$, is obtained from the product of the slope and J_{C}. As shown in fig. 2.6, design I, II, and III exhibits β_{bulk} of 37, 45.4, and 70.7, respectively. Assuming $J_{\mathrm{C}} \approx J_{\mathrm{E}}$=25 mA/$\mu$m^2, $K_{\mathrm{B,edge.}}$ are 72.5, 71.9, and 106.9 μA/μm for designs I, II, and III.

Two reasons causes the drop of β in a scaled DHBT. First, the increased base doping concentration resulting in higher Auger recombination rate and hence shorter τ_{Auger}. For base designs with the same T_{B} and similar τ_{B}, β_{bulk} decreases as doping concentration increases. Second, the edge current does not vary in proportion with W_{E}. For devices with narrow emitters, $I_{\mathrm{B,edge.}}$ will be more dominant with respect to $I_{\mathrm{B,bulk}}$. Thus, when devices are scaled, the magnitude of edge cur-

rent components remain the same, and β reduces.

In order to improve DC-β in the future scaling generations of DHBTs, a model incorporating the contribution from all four base current components would be a valuable design tool in addition to the RF scaling laws of DHBTs. Using a commercial TCAD simulation software, such model can be constructed [16, 18]. The model would enable an estimation of DC-β of devices for a given B-E junction design and geometry. Moreover, DC-β of device utilizing novel B-E junction geometries such as a recessed B-E junction in a emitter regrowth process can be evaluated as well. The details of TCAD simulation will be covered in chapter 5.

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Chapter 3

DHBT Process Improvement

A feasible and reliable process flow is the key to the realization of any semiconductor device. The development of process flow involves extensive calibrations, testing, and sometimes even the re-definition of the existing process flow. The last one is usually the case when the device dimensions approach the limitation of the existing process flow. As mentioned in chapter 2, device scaling in both epitaxial and lateral directions is necessary in order to attain higher cut-off frequencies. Therefore, developing a DHBT process flow which can be reliably scaled to sub-100 nm emitter width is one of the main goals of this dissertation. In this chapter, the development of both front end and back end process flows will be reported. Three improvements, discussed in designated sections, are ready to be incorporated into the fabrication of DHBTs.

The first improvement involves the recalibration of the process flow for the refractory emitter metal stack. With the new process flow, the emitter width has been successfully and reliably reduced to 75 nm. In the second section, the integration of a new process flow for a composite dielectric sidewall deposited by atomic layer deposition (ALD) and plasma enhanced chemical vapor deposition (PECVD) will be presented. The composite dielectric sidewall deposited immediately after the base metalization protects the extrinsic base from subsequent process damage. With adequate surface pretreatment technique before ALD, the sidewall could decrease the trap states density (D_{it}) on InGaAs surface [1, 2], reducing the density of the electrons trapped in the surface depletion region. Thus, the surface conduction via the surface depletion layer decreases and the DC-β will be improved [3]. Finally, a new process flow for the interconnects between metal layers at the back end process will be discussed. With the new intercon-

nects, metal to metal spacing has been increased to $\sim$3 μm. Therefore, low-loss microstrip lines can be built on top of the devices, enabling more accurate RF measurements and device de-embedding.

3.1 Refractory Emitter Metal Stack

According to the DHBT scaling law in chapter 2, the emitter current (I_{rmE}) at the bias point for peak f_τ and $f_{\max}$ must remain constant when the scaled base-emitter (B-E) junction width (W_{E}) decreases in order to reduce the RC delays. As a result, the emitter current density (J_{E}) at such bias point increases when DHBTs are scaled [4]. For DHBTs with 100 nm wide B-E junction and 70 nm thick collector, J_{E} for peak f_τ and $f_{\max}$ is approximately 30$\sim$40 mA/μm^2. At such current density, electron migration would degrade the conventional Ti/Pd/Au contact [5], causing reliability issues in the devices. Therefore, the emitter contact of scaled DHBTs is composed of refractory metal to mitigate the damage due to electron migration [6].

Furthermore, to reduce the base access resistance (R_{BB} and RC delay, the base contact of DHBTs needs to be very close to the B-E junction, i.e. $W_{\mathrm{gap}} \approx$10-20 nm in DHBTs with $\sim$100 nm emitter width [7]. In addition, the base contact of DHBTs is $\sim$100 nm-thick in order to have negligible base metal sheet resistance. To lift-off the base contact, resist must be few hundreds nanometers thick to achieve the required aspect ratio. With such resist thickness, lithography with $<$10 nm accuracy in alignment is challenging even with the direct write from a commercial e-beam lithography system [8]. Therefore, the base contact lift-off

has to be a self-aligned process. This is usually achieved by having a tall and narrow emitter metal surrounded by dielectric sidewall. The base metal is then deposited on the emitter metal and the base semiconductor. Because of the high aspect ratio. The emitter and base remain electrically separated, avoiding the shunt path for the B-E junction. For the self-aligned lift-off to work, the sidewall profile of the emitter metal must be nearly vertical [9].

A refractory metal stack with such shape would be difficult to be fabricated using a lift-off process. Moreover, refractory metal need to be evaporated at high power because of its high melting point, increasing the intensity of the bombardment due to X-ray and stray electrons. The e-beam resist could be damaged and the lift-off would fail. Therefore, a process involving blanket metal deposition and dry etch is more suitable for this purpose than the lift-off process. The emitter process flow of UCSB DHBTs has thus been developed based on this process flow [6, 10].

The composite emitter metal stack of UCSB DHBT is composed of three layers: molybdenum, tungsten, and titanium tungsten alloy (TiW). The Mo/W/TiW stack is ∼520 nm tall and is dry etched by SF_6/Ar plasma using a chromium hard mask. The Cr reacts in the dry etch chemistry and forms a resistive layer (chromium oxynitride/chromium nitride) which cannot be removed by wet or dry etch techniques without damaging the emitter metal or the substrate. Therefore, a layer of sacrificial dielectric (SiO_2/SiN_x) is inserted between Cr and TiW so the Cr mask can be lifted-off by undercutting the oxide with buffered HF (BHF).

Fig. 3.1 and 3.2 are the schematics of UCSB emitter process flow [10]. The fabrication starts with blanket Mo evaporation which forms emitter contact. A

layer of W and a layer of TiW are sputtered on top of Mo. The sacrificial dielectric is then deposited by PECVD. Cr mask is deposited via blanket evaporation, after which the emitter pattern is defined by e-beam lithography and transferred to Cr by Cl_2/O_2 inductively coupled plasma (ICP) etch. The dielectric and refractory metal are etched by two consecutive SF_6/Ar inductively coupled plasma (ICP) etch steps. The first etch recipe has high bias power (200 W) in order to remove the dielectric, TiW, W, and Mo. Because the plasma loses its kinetic energy as it travels deeper along the stack, the bottom of the stack is tapered after the first high power etch. To obtain a vertical sidewall profile, a SF_6/Ar etch with low bias power (15 W) is done to undercut the tapered stack, resulting in a metal stack shown in the upper left corner of fig. 3.2.

PECVD SiN_x encapsulating the emitter stack is deposited and then etched by CF_4/O_2 ICP to form sidewall. The InGaAs emitter cap is wet etched afterwards. Cr mask is lifted-off by undercutting the sacrificial dielectric in BHF, by which the first sidewall is also partially removed. A second layer of SiN_x sidewall is thus deposited to provide the electrical separation between the emitter and the self-aligned base contact. Finally, the InP emitter is wet etched prior to the base contact process, as shown in fig. 3.3, in order to have a pristine InGaAs surface for metalization. A step by step of UCSB DHBT process flow is listed in appendix A.

Since the base contact is self-aligned, base metal is evaporated not only on the base, but also the emitter stack and the sidewall, as illustrated in the right side of fig. 3.3. It is imperative to attain a nearly vertical sidewall profile, i.e. identical width at the top and at the bottom of the metal stack after the metal dry etch.

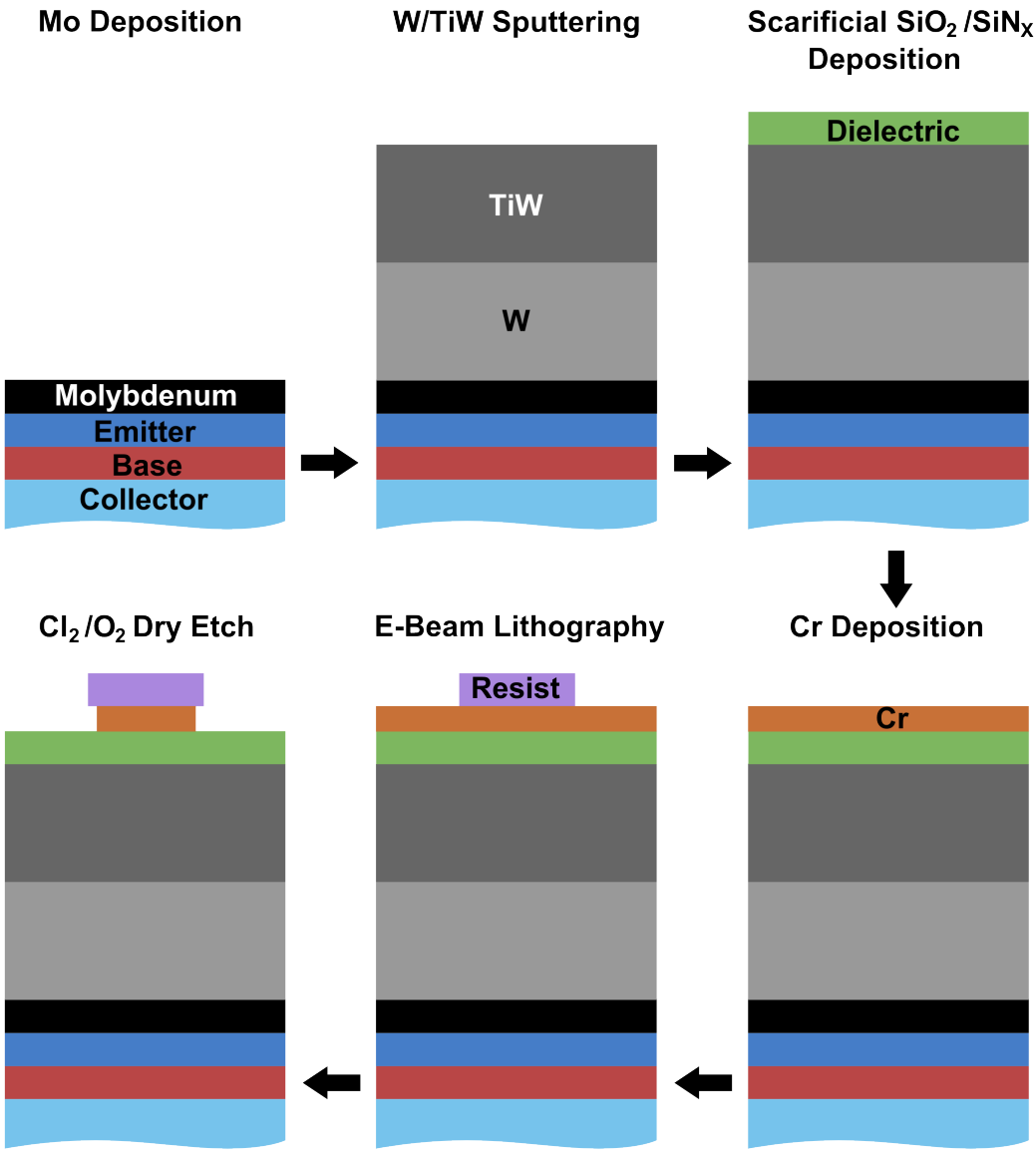


Figure 3.1: The schematics of UCSB DHBT emitter process flow.

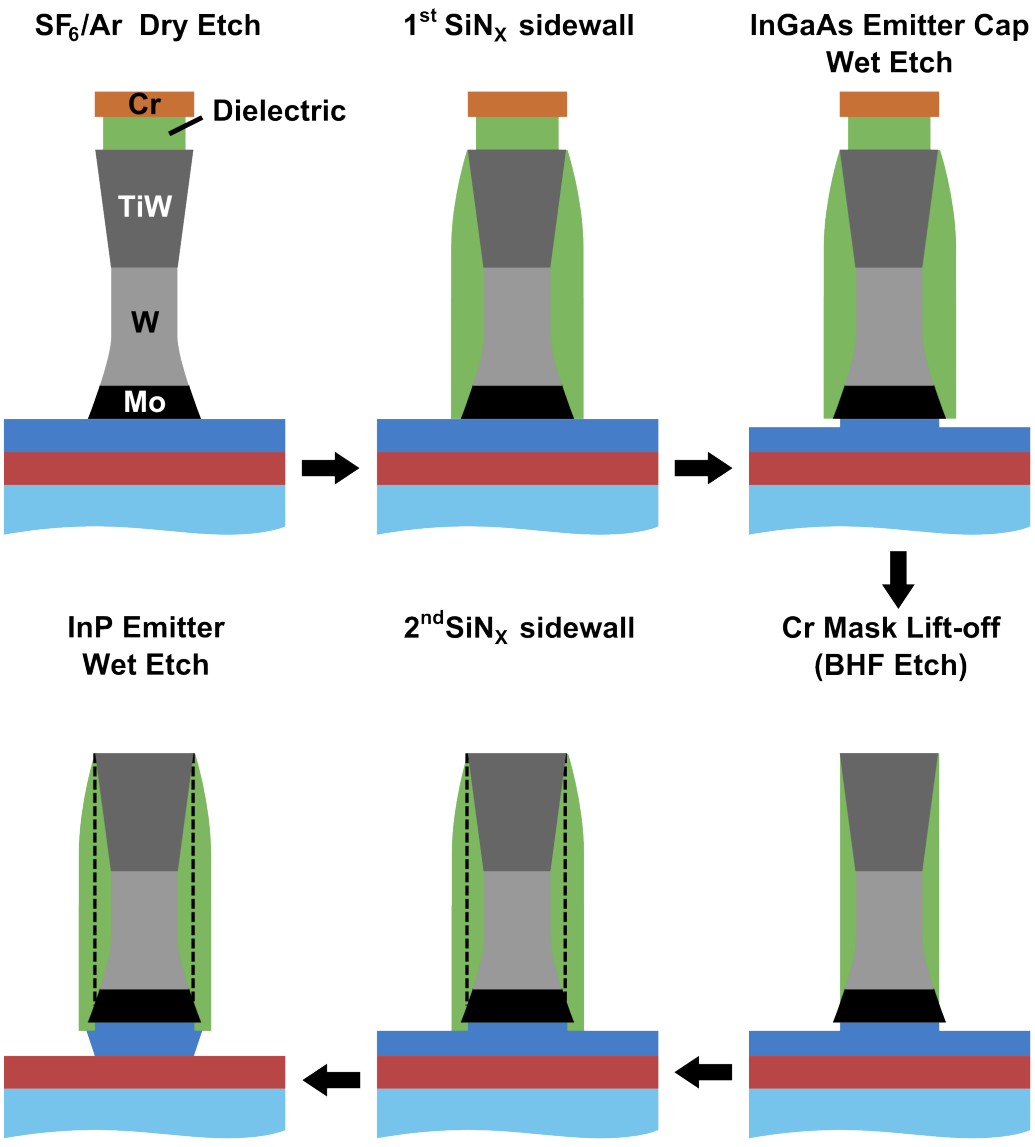


Figure 3.2: The schematics of UCSB DHBT emitter process flow (continued).

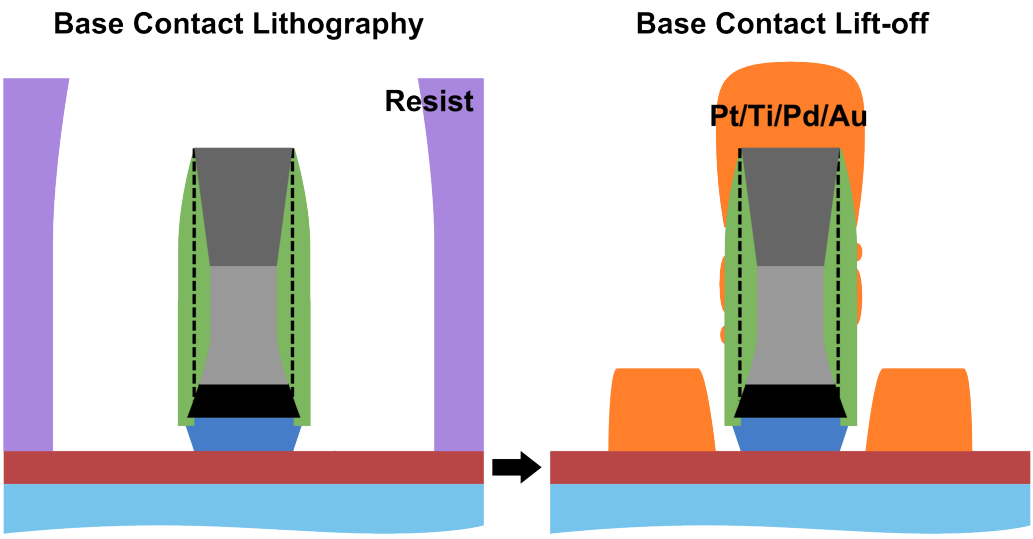


Figure 3.3: The schematics of the self-aligned base contact lift-off process.

As shown in fig. 3.4, if the sidewall profile of the emitter stack is tapered, more metal is evaporated onto the sidewall, potentially forming a shunt path between the base and emitter contacts. At the bottom of the emitter stack, as metal is being deposited on the sidewall, the InGaAs surface within the extrinsic base is sealed, and hence the surface can not be accessed for passivation. On the bare InGaAs surface, Fermi level is pinned by the defect states (D_{it}), causing more surface depletion. Therefore, surface conduction base current increases and DC-β drops. In an even worse scenario, residues from the resist for the base contact lift-off could be trapped on the extrinsic base surface, further increasing D_{it} and surface conduction.

Due to its high aspect ratio, the emitter metal stack is sensitive to its internal stress. If the W/TiW film is deposited with high internal compressive or tensile stress, the tall and narrow metal stacks would be mechanically unstable

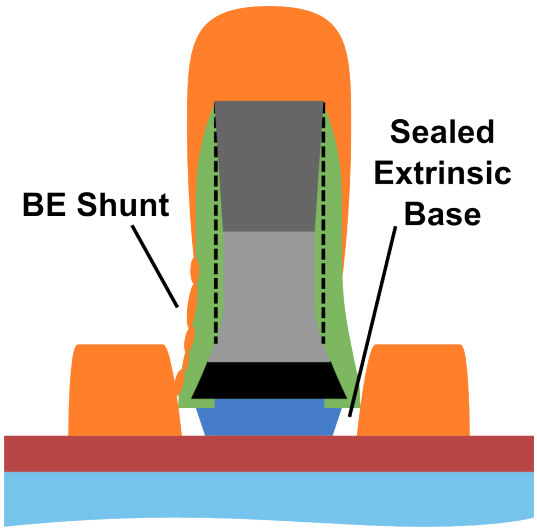


Figure 3.4: The schematics of a base contact lifted-off on a tapered emitter stack. A shunt path between the base and the emitter is formed and the extrinsic base is sealed by the base metal and the dielectric sidewall.

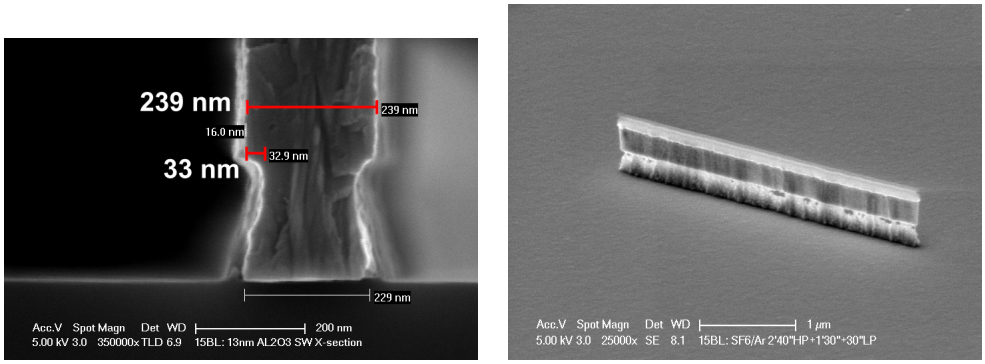
after metal dry etch. If the film is deposited with extremely high internal stress, stress relaxation could occur during the deposition, forming columnar grains [11] which increases the emitter metal resistivity. Thus, prior to the sputtering, the recipe for W/TiW stack must be calibrated to obtain a film with very low internal stress.

The internal stress of W/TiW film depend on the chamber pressure and the temperature on the sample surface. Because of the chamber configuration of the UCSB sputtering system (Sputter 4), the sample temperature is modulated by a radiation heat source located at the back side of the sample holder. Since the sample is heated from behind, temperature gradient exists between the back and front of the sample, and the temperature on the top surface depends on the thickness and the thermal conductance of the sample. Hence, the low stress sputtering recipe was calibrated using InP wafers, whose thickness and thermal properties

are similar to that of the DHBT samples.

As mentioned before, the emitter stack is tapered after the high power SF_6/Ar ICP etch, and the vertical sidewall profile is achieved by undercutting the stack with a low power SF_6/Ar ICP etch. The undercut to W is faster than that of TiW because W reacts faster with SF_6. Therefore, W has a more concave profile than TiW after the dry etch. The process flow developed for DHBTs with 250∼200 nm emitter width employs a metal stack with identical W and TiW thickness. Fig. 3.5a is the SEM cross-section of such emitter metal stack. In order to achieve the vertical stack profile, i.e. identical width at the top and the bottom of the stack, the undercut to W ($W_{UC,W}$) is approximately 30 nm on both sides. The bottleneck formed near the W/TiW interface is thus ∼60 nm narrower than W_E, as shown in the top row of fig. 3.6. As shown in the SEM image in fig. 3.5b, the process flow for 1:1 W:TiW can produce a <128 nm wide emitter junction, but at the price of the narrow bottleneck and increased emitter metal resistance. For the DHBT scaling generations beyond 64 nm, the process would fail because of the excessive undercut.

In order to scale the dry etch refractory metal process beyond 128 nm emitter width, $W_{UC,W}$ must be controlled. As shown in the schematics in bottom row of fig. 3.6, by increasing the TiW to W thickness ratio to 2.5 and recalibrate the low power SF_6/Ar ICP etch, $W_{UC,W}$ required for a vertical stack has been reduced to ∼10 nm. Fig. 3.7 shows the SEM cross-sections of the 1:2.5 W:TiW stacks at W_E=128 and 64 nm.



(a) (b)

Figure 3.5: SEM of 1:1 W:TiW metal stack on an InP test sample after SF_6/Ar ICP etch. (a) Cross-section of the stack with $W_{E\approx}$250 nm. (b) A stack with $W_E \approx$75 nm.

3.2 Composite Dielectric Sidewall

The InGaAs surface within the extrinsic base, once exposed after the InP emitter wet etch, is subject to process damage, if not properly sealed after base metalization. Additional surface trap states will be formed if the surface is contaminated by resist residues or damaged by plasma. The increased surface trap density (D_{it}) pins the surface Fermi level and induces a wider surface depletion region [12]. Thus, the sheet resistance increases, causing higher R_{BB}, and hence reduces f_{max}. Moreover, with higher D_{it} and wider surface depletion region, more electrons injected from the emitter will be trapped in the surface depletion region. Hence, surface conduction current ($I_{B,edge}$) increases and DC-β reduces [3].

For passivating the nano-scaled extrinsic base, a sidewall process is desirable because the field next to the base contact must remain accessible for the subsequent process steps. However, the SiN_x sidewall process in the formation of the emitter metal stack is not suitable here due to the plasma damage from PECVD. Furthermore, the PECVD deposition tends to form lips at the top of a step. A

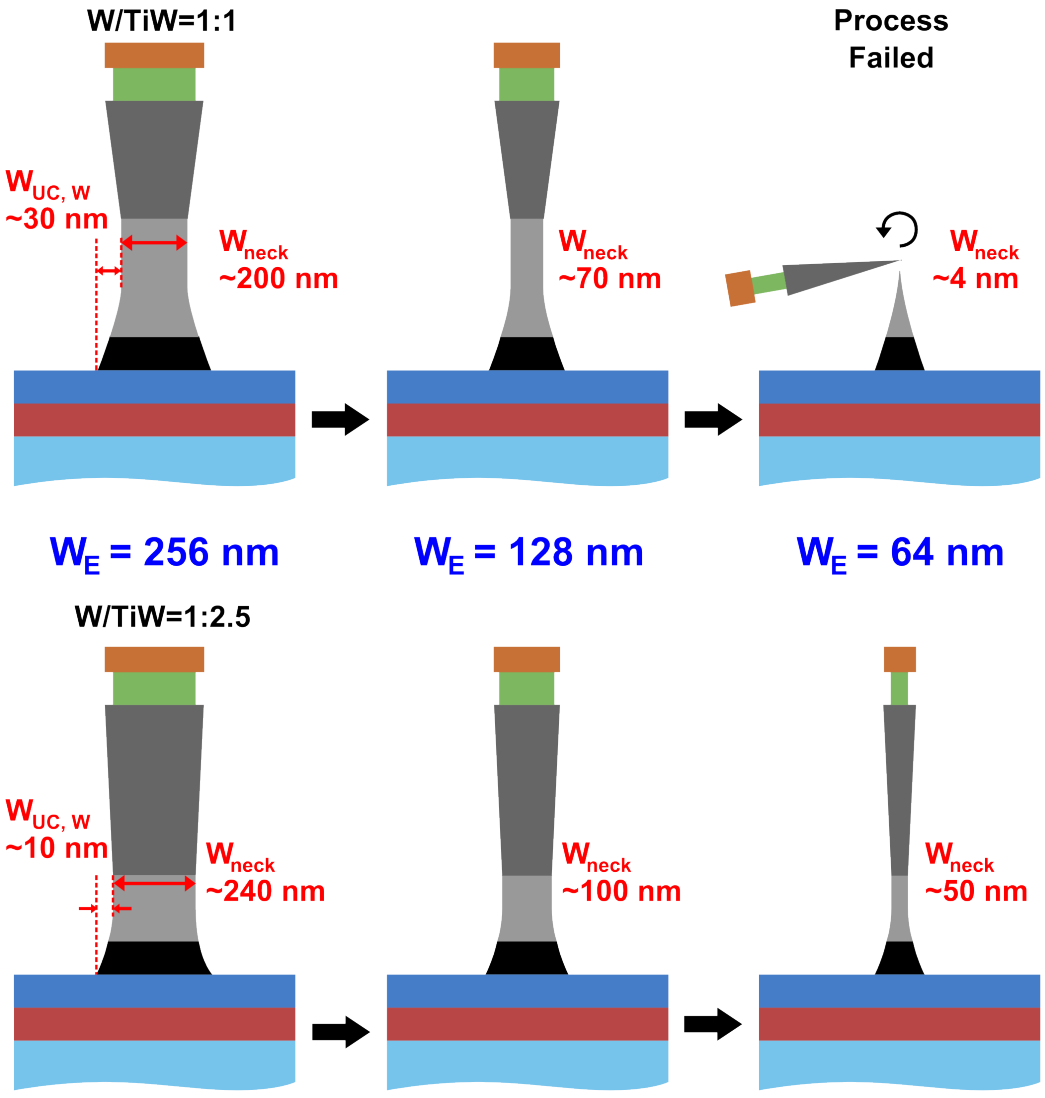
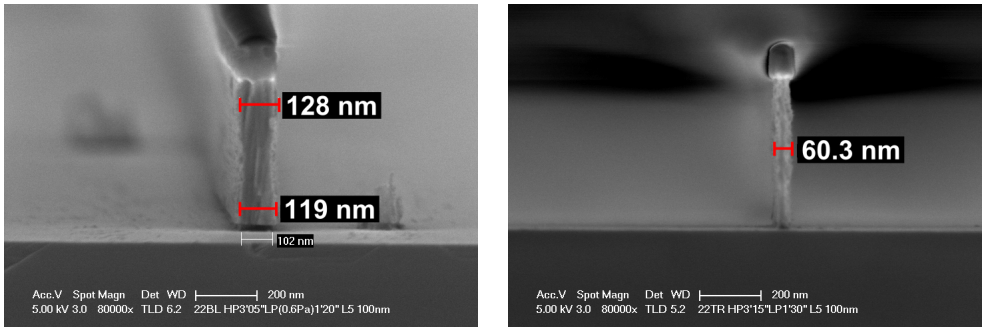


Figure 3.6: Schematics of 256, 128, and 64 nm wide emitter metal stacks after SF_6/Ar ICP etch. Upper row: 1:1 W:TiW. Bottom row: 1:2.5 W:TiW.



(a) (b)

Figure 3.7: SEM cross-sections of 1:2.5 W:TiW metal stack on an InP test sample after recalibrated SF_6/Ar ICP etch. (a) W_E=128 nm. (b) W_E=64 nm.

void could form in a narrow gap because the gap is sealed before it is filled. Because the gap between the base contact and the emitter stack is ∼10 nm, the gap would be quickly seal off in SiN_x deposition. As a result, the InGaAs surface would not be terminate adequately and D_{it} will remain high.

On the other hand, ALD, being a self-limiting deposition technique, is capable of filling narrow gaps. Al_2O_3 can be deposited without plasma by a thermal ALD at a moderate temperature (200°C) without inducing further base metal penetration/diffusion due to the thermal cycling [13]. However, there is no dry etch process for Al_2O_3 compatible with UCSB DHBT process flow.

A hybrid of PECDVD SiN_x sidewall process and ALD Al_2O_3 was thus developed to meet the requirements for the sidewall formation on the extrinsic base. Fig. 3.8 shows the process flow for a composite Al_2O_3/SiN_x sidewall. After base metalization, Al_2O_3 is blanket deposited by thermal ALD. SiN_x is deposited by PECVD on top of Al_2O_3, and then dry etched to form sidewall, which is the same sidewall process flow for the emitter stack. Finally, Al_2O_3 is wet etched using AZ300MIF developer with the SiN_x sidewall being the hardmask. Fig. 3.9a is the

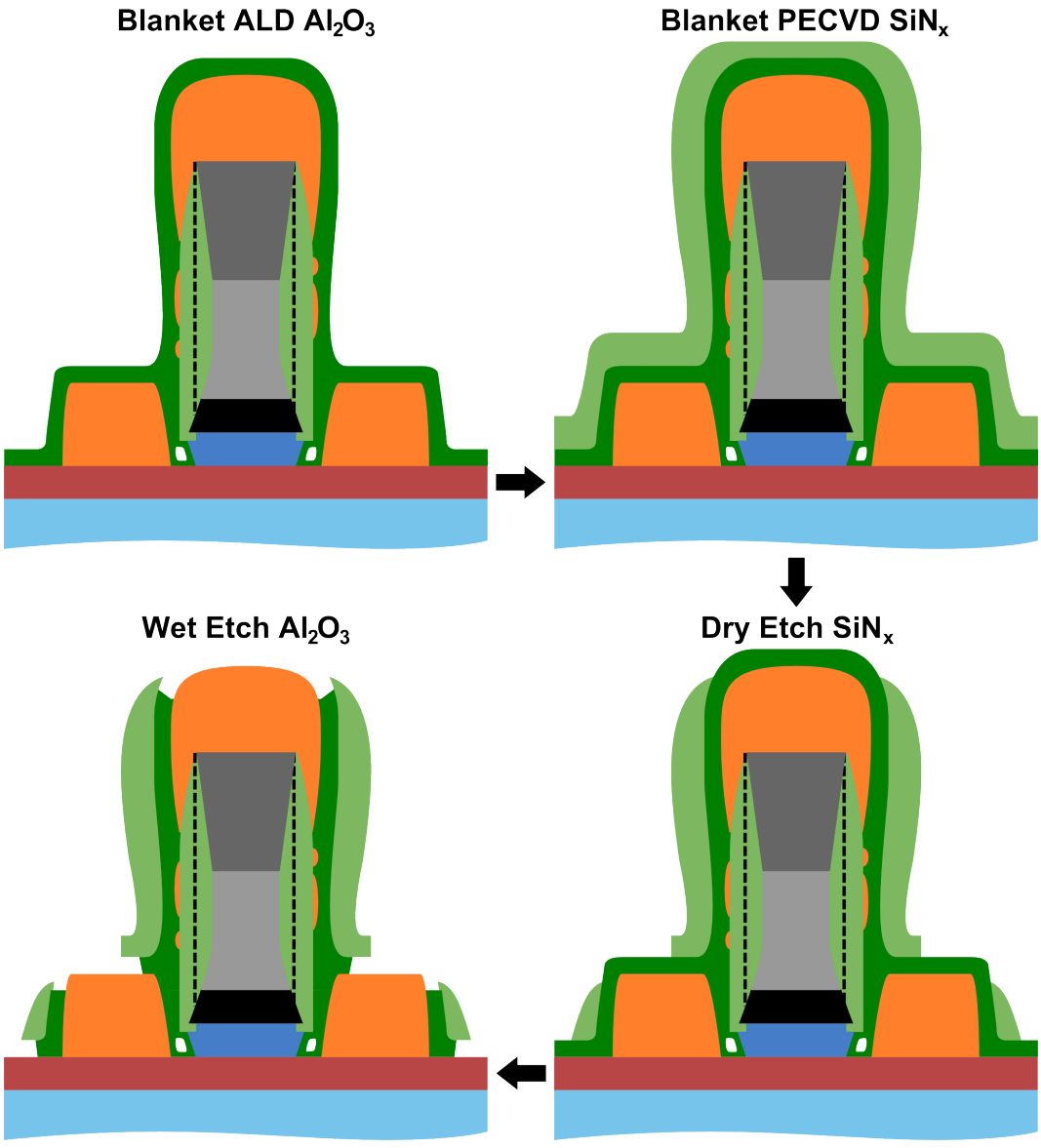
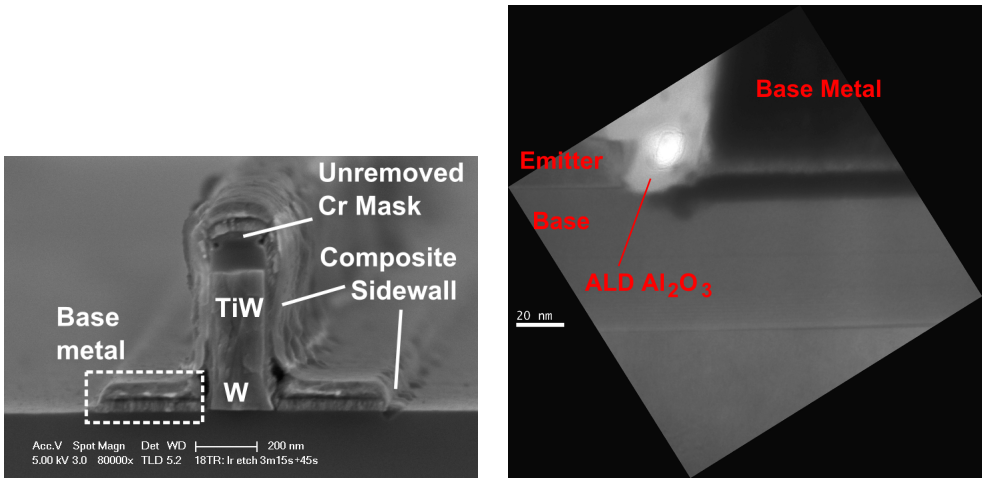


Figure 3.8: Process flow for the composite Al_2O_3/SiN_x sidewall.



(a) (b)

Figure 3.9: (a) SEM cross-section of a InP test sample with the composite sidewall around the emitter stack and the base contact. The bilayer base metal process was also being tested on the sample. (b) TEM cross-section of a experimental device with a composite sidewall sealing the extrinsic base region.

SEM cross-section of a test sample with composite Al_2O_3/SiN_x sidewall around the emitter and base contact, sealing the extrinsic base surface. The composite sidewall process has been incorporated into the fabrication of DHBT58H and 56K. Fig. 3.9b is the TEM cross-section of the extrinsic base of DHBT70A. The TEM image indicates that ALD Al_2O_3 has been deposited onto the extrinsic base.

3.3 Interconnects Between Metal Layers

As the cut-off frequencies of the DHBT increase, the frequency range of the measurement should also increase in order to perform a proper extrapolation to estimate the accurate cut-off frequencies. Moreover, in order to improve the accuracy in the RF measurement, it is imperative to not only perform adequate

calibrations prior to the measurements, but also have a clean transmission line environment to probe the device. Several calibration techniques exist for two-port measurements with a network analyzer (PNA). The techniques will be discussed in chapter 4. Coplanar waveguides (CPWs) and microstrip lines are two popular choices for interconnects for RF measurements [14].

CPW is a structure which is relatively easy to fabricate since it is built on a single metal layer. The CPW structure of UCSB DHBT sample are built on the first metal layer (Metal 1) which is $\sim$1 μm above the substrate. A 50 Ω CPW structure is designed according to the metal thickness (1 μm). The length of the CPW line must be negligible when compared to the wavelength of the probing frequencies for device de-embedding purpose. However, the probes should be kept at certain distance to reduce the cross-talk and ensure proper wave propagation [14]. The length of the CPW line on UCSB DHBT samples is thus $\sim$200 μm. As the frequency of a two-port measurement increases, the wavelength decreases and the device de-embedding using the CPW with a fixed length becomes less accurate.

Microstrip line is an alternative structure for RF measurements and is more popular for high frequency measurements. It enables the multiline thru-reflect-line (ML-TRL) calibration for the vector network analyzers to reduce random errors in the calibrations [15]. However, unlike CPW, since the ground plane and the signal line are at different level, microstrip line requires at least one ground via, which causes excessive inductance at high frequency. Microstrip lines had been incorporated into previous DHBT samples at UCSB by utilizing the sub-collector and Metal 1 as the ground plane and the signal line, respectively. The thickness of the low-k dielectric (BCB) between the sub-collector and Metal 1 is $<$1 μm,

which is determined by the height of the emitter stack (∼650 nm) and the total thickness of the active device (∼200 nm). As a result, the width of the microstrip line is few μm, and a long line may become lossy. In addition, the variation of the BCB thickness across the microstrip line changes the characteristic impedance randomly, causing reflection which decrease the accuracy in device de-embedding.

Increasing the BCB thickness is one solution to this problem. Nevertheless, increasing the distance between the substrate and Metal 1 would be counter productive as it causes unnecessary complexity in the already challenging process flow for the emitter stack. An alternative is to add another BCB (∼3 μm) and metal layer (Metal 2), and then build the microstrip line using Metal 1 and Metal 2. In order to build such structure, a process flow involving multiple sets of metal lift-off and BCB planarization was developed. However, not only is the process flow time consuming, but it also requires several thermal cycles due to multiple BCB planarization, causing more metal penetration at the contacts.

Therefore, a process flow with one lift-off and BCB process is desirable and has been developed at UCSB. Fig. 3.10 shows the process flow of interconnects between metal layers. On top of the bottom metal layer (Metal 1), a SiN_x adhesion layer is sputtered at room temperature instead of PECVD at 250°C to avoid thermal cycling. Photo-BCB (cyclotene 4024-40), a negative-tone photosensitive BCB resin, is applied on the sample instead of normal BCB resin. After exposure, the photosensitive compound inhibits the dissolution of the BCB resin in the solvent developer so it remains intact. By over exposing the Photo-BCB, a tapered sidewall shape could be created, which is preferable for the subsequent lift-off process. The patterned Photo-BCB resin can then be cured (cross-linked)

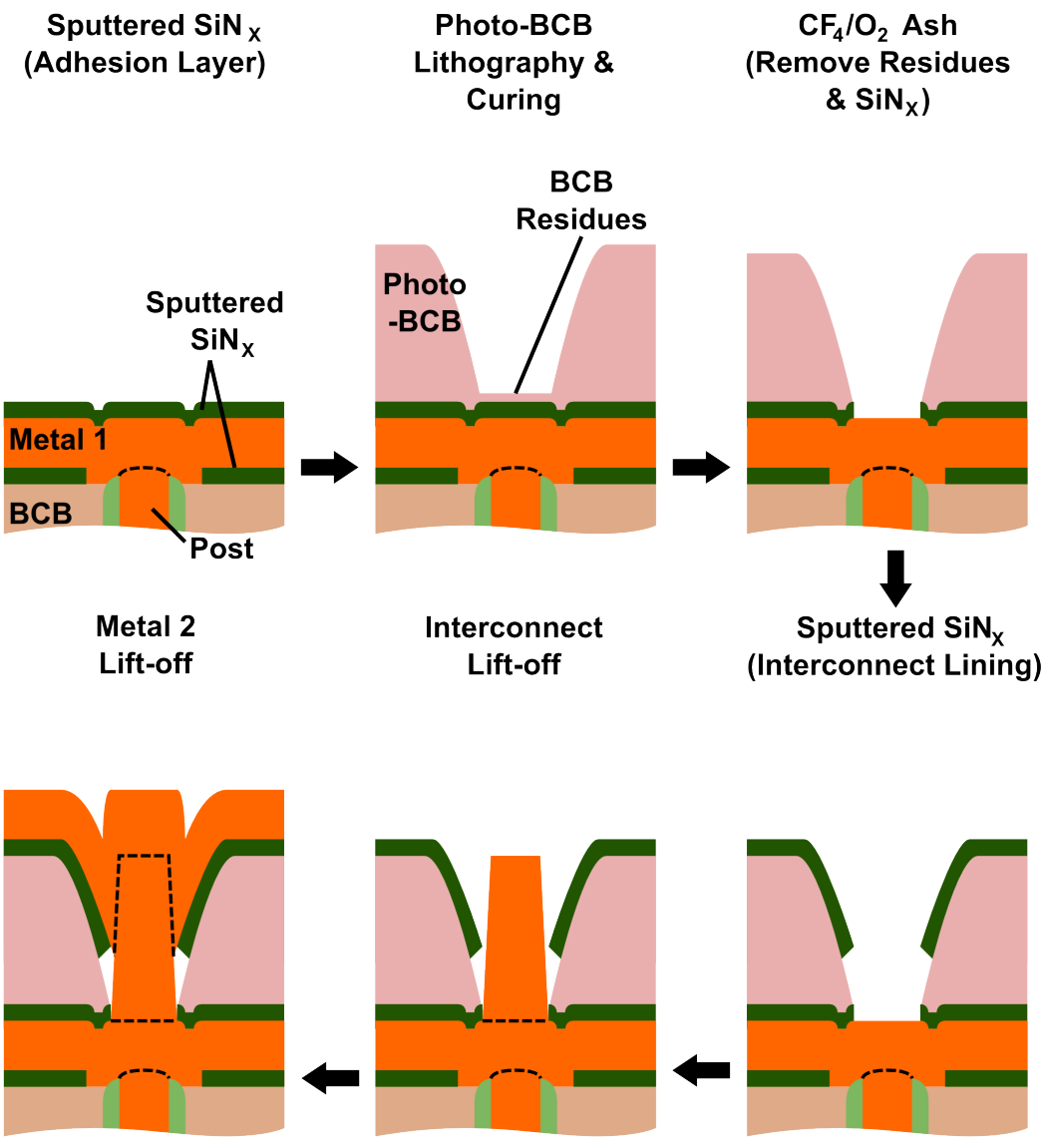


Figure 3.10: Process flow for interconnects between metal layers.

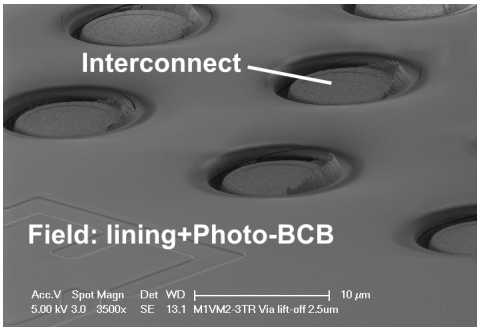


Figure 3.11: SEM of interconnects between metal layers on a test sample.

using the same recipe for normal BCB resin. Because the solvent development leaves residues, the sample is ashed by CF_4/O_2 plasma, which will also remove the SiN_x adhesion layer within the via. Another layer of SiN_x is sputtered, patterned and then etched to form a lining layer to promote the adhesion between metal and Photo-BCB resin. Because of the tapered resin profile, the interconnect metal can be directly lifted-off into the via. Finally, the upper metal layer is lifted-off on the top of the via. The process flow has been demonstrated on test samples, as shown in fig. 3.11, and ready to be integrated into DHBT fabrication.

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Chapter 4

Experimental Results

In this chapter, the DC and RF output characteristic of the DHBT samples, fabricated using the process flow in Appendix A, on two different epitaxial designs and with different process features will be reported. To achieve the highest possible cut-off frequencies ($f_\tau, f_{\max}$), the parasitic RC delays, which are determined by the physical dimensions of the devices as well as the specific contact resistivity ($\rho_{\text{Cont.}}$) at each terminals, need to be as low as possible. Since the device dimensions and $\rho_{\text{Cont.}}$ are process-dependent, the optimal dimensions remain unknown until the sample is probed. To ensure the presence of the device with the optimized dimension, an array of devices with different combinations of W_{E}, W_{BM}, and L_{E} were fabricated simultaneously on every DHBT sample.

DC characteristics were measured using Agilent 4155C semiconductor parameter analyzer. For RF measurements, the transistors were DC-biased using 4155C, and the two-port S-parameters were measured by Agilent E8361A network analyzer (PNA) at frequencies between 0.5 and 67 GHz. Using Agilent Advance Design System (ADS), the data were de-embedded. The results were then fitted with an hybrid-π equivalent circuit model, and thereby the parasitic resistance and capacitance of the devices were extracted.

4.1 Measurement set up and calibration

The f_τ and $f_{\max}$ of scaled DHBTs are few hundreds GHz, which exceeds the frequency span of most commercially available vector network analyzers (VNAs). Therefore RF measurements were performed at K or W band, and the cut-off

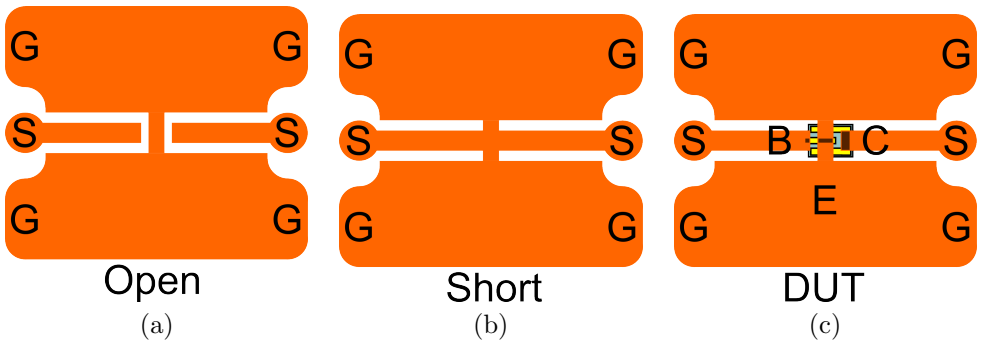


Figure 4.1: Top-down schematics of (a) open and (b) short calibration structures, and (c) CPW interconnect with device under test (DUT).

frequencies were then extrapolated from data measured at these bands. Accurate extrapolation requires clean RF data, and hence adequate microwave environment is crucial. CPW structures with 50 Ω characteristic impedance were constructed on Metal 1 for each device. Moreover, measurement performed with on-wafer probes is necessary for both precision and repeatability purposes. Metal pads capable of accommodating a 75 μm-pitch ground-signal-ground (GSG) on-wafer probe were incorporated into the CPW structures. To remove the parasitics associated with the CPW interconnect and de-embed the device, on-wafer open and short CPW standards were also fabricated simultaneously [1]. Fig.4.1 shows the schematics of the CPW interconnects for open and short calibration and device under test (DUT).

The on-wafer probes and the PNA terminals were connected by semi-rigid waveguides, which has a delay term associated with it. To compensate this delay and shift the reference plane from the PNA terminals to the on-wafer probe tips, calibration using either an on-wafer or an off-wafer impedance standard was performed before device measurement. There are several calibration techniques: Short-Open-Line-Thru (SOLT), Line-Reflect-Reflect-Match (LRRM), and Thru-

Reflect-Line (TRL), etc [1]. For the SOLT technique, the accuracy of the calibration depends on whether the connection to the standards is in consistency with the connection when the equivalent circuit of the standards are determined by the manufacturer [2]. Therefore, SOLT is generally suitable for coaxial measurements but undesirable for probe measurements, where variation induced by probe positioning exists. The LRRM technique, on the other hand, requires a fully known thru standard which defines the probe tips as the reference planes, two non-deal reflection standards with different reflection coefficients (short and open of SOLT), and finally a match standard, where only the DC resistance needs to be known [3]. Thus, compared with SOLT, LRRM is less prone to the error due to probing variation [1]. For the work in this thesis, LRRM calibration was performed prior to the RF measurements using a commercially available impedance standard for 75 μm-pitch GSG probes.

The parasitic associated with the CPW interconnect must be de-embedded so the temporal response of the transistor can be obtained. After the LRRM calibration, the two-port S-parameters of open and short structures shown in Fig. 4.1 were measured and translated into Y-parameters (Y_{open} and Y_{short}). The raw S-parameters of the DUT were then measured and translated to Y-parameter as well (Y_{DUT}). The actual Y-parameters of the transistor (Y_{HBT}) can be obtained from the following expression

$$Y_{\text{HBT}} = ((Y_{\text{DUT}} - Y_{\text{open}})^{-1} - (Y_{\text{DUT}} - Y_{\text{short}})^{-1})^{-1}. \tag{4.1}$$

The above equation is valid when the physical dimensions of the CPW is much smaller than the propagation wavelength at the probing frequency (few mm

at 0.5 67 GHz) [4]. However, if the distance between two on-wafer probe is too small, crosstalk or coupling between the probes can reduce the accuracy of the measurements. Therefore, the physical dimensions of the CPW cannot be scaled infinitely. The length of the CPW structures on UCSB HBT samples is $\sim$200 μm.

Fig. 4.2 is the circuit diagram of the measurement set up. The semi-rigid waveguides connecting the on-wafer probes and PNA are omitted because the delay associated with them has been removed after LRRM calibration. DUTs were DC-biased using 4155C via the internal bias tees of the PNA. Due to the small physical dimensions of THz HBTs, the base-emitter junction is extremely sensitive to the amount of base current and can easily breakdown at I_B of few mA. Since I_B varies exponentially with V_{BE}, an abrupt change in V_{BE} will induce high I_B, and could possibly lead to device failure. In order to avoid device failure, a resistor (R_{Bias}) was added as a voltage divider between the base terminal and 4155C. The actual V_{BE} at DUT is then $V_{BE} = V_{BB} - I_B R_{Bias}$. With R_{Bias}=10 kΩ, the $I_B R_{Bias}$ drop is 1 V every 100 μA, which mitigate the change in V_{BE} as we adjust V_{BE} for desired I_B and I_E.

4.2 DHBT63B

4.2.1 Device structure and process feature

The DHBT63 design utilizes a 30 nm thick InP emitter doped at 5×10^{19} cm^{-3} for the top 15 nm and 3×10^{18} cm^{-3} for the bottom 15 nm. The p-type base is composed of 25 nm of InGaAs with a doping-grade from 9×10^{19} cm^{-3} at

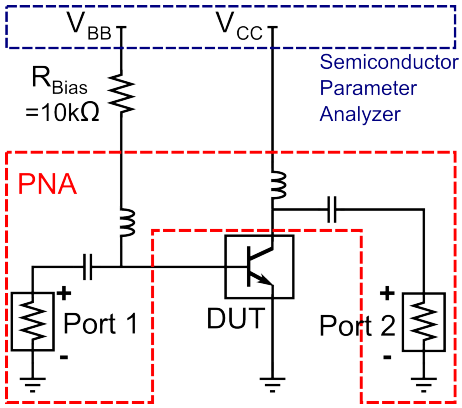


Figure 4.2: RF measurement set up. The delay associated with semi-rigid waveguides were removed after calibration. Hence the waveguides are neglected in the diagram.

the emitter side to $5 \times 10^{19}\,\mathrm{cm}^{-3}$ at the collector side. The design employs the 70 nm thick collector structure (setback, superlattice, InP collector) with doping concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$. The detailed epitaxial structure is listed in table. 4.1. The band diagram of the device under V_{BE}=1.2 V and V_{CB}=0.6 V is shown in fig. 4.3. The solid lines are the conduction band and the valance band if the space charge associated with the collector current in the collector region is neglected, whereas the dashed lines are the bands considering the space charge in the collector at $J_{\mathrm{C}} \approx 31\,\mathrm{mA}/\mu\mathrm{m}^2$.

The base metalization of DHBT63B was a lift-off process using UV-6 as the resist. According to the HBT samples fabricated prior to DHBT63B, UV-6, being both an UV and e-beam resists, is sensitive to bombardment from X-ray and stray electrons during e-beam evaporation. When damaged, the resist may form residues at the vicinity of the base contact define by lithography, as shown in Fig. 4.4. The residues alter the surface reconstruction on p-InGaAs, increasing the specific contact resistivity [5]. In a worse case, it could results in a failed lift-off

Layer	Semiconductor	Thickness (Å)	Doping (cm^{-3})
Emitter cap	$In_{0.53}Ga_{0.47}As$	100	8×10^{19}:Si
Emitter	InP	150	5×10^{19}:Si
Emitter	InP	150	3×10^{18}:Si
Base	$In_{0.53}Ga_{0.47}As$	250	$9 - 5 \times 10^{19}$:C
Setback	$In_{0.53}Ga_{0.47}As$	95	1×10^{17}:Si
B-C grade	-	120	1×10^{17}:Si
δ-doping	InP	30	5×10^{18}:Si
Collector	InP	455	1×10^{17}:Si
Sub-collector	InP	75	2×10^{19}:Si
Sub-collector	$In_{0.53}Ga_{0.47}As$	75	4×10^{19}:Si
Sub-collector	InP	3000	1×10^{19}:Si
Etch stop	$In_{0.53}Ga_{0.47}As$	35	undoped
Substrate	InP	-	undoped

Table 4.1: Epitaxial structure of DHBT63.

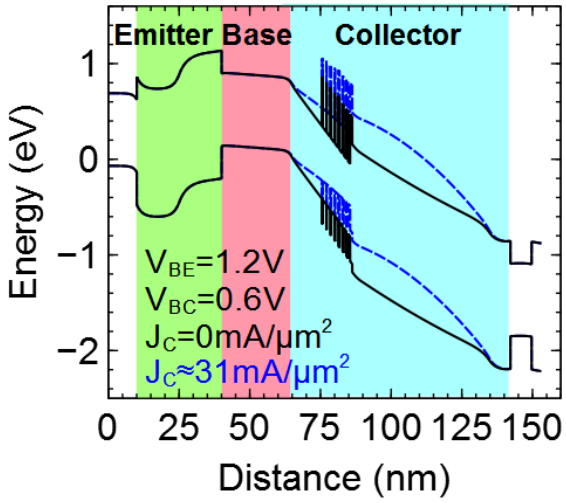


Figure 4.3: Computed band diagram of DHBT63 under V_{BE}=1.2 V and V_{CB} =0.6 V. The solid lines are the conduction and valance bands when J_C = 0 mA/μm^2, i.e. ignoring the space charge in the collector region. The dashed line represent the conduction and valance bands considering the space charge region in the collector at J_C ≈31 mA/μm^2.

process. The metalization process involving UCSB e-beam evaporation system (E-Beam 4) had been suffered from this damage due to excessive X-ray irradiation and electrons bombardment. The cause of this was later identified as a Nickel

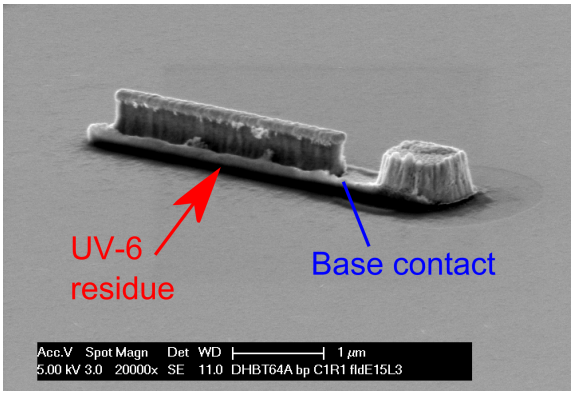


Figure 4.4: An SEM image of an HBT sample after base post lift-off. Residues of UV-6 were found around the base contact, possibly due to the damaged resist sidewall.

metal source in the evaporator, which would disrupt the magnetic field near the electron filament, generating the excessive X-ray and stray electrons. By removing the Ni source from the chamber, the damage to UV-6 has been alleviated. However, this discovery was made after the fabrication of DHBT63B is completed. To avoid the lift-off failure as well as high specific contact resistivity, a portion of the base metallization of DHBT63B was done using the e-beam evaporation system in the cleanroom at Teledyne Scientific Corporation (TSC).

The base contact of DHBT63B is composed of 3.5/17/17/70 nm of Pt/Ti/-Pd/Au. After e-beam lithography, 3.5 nm of Pt was deposited using E-Beam 4. The sample was then sealed in a nitrogen ambient environment and transferred to the e-beam evaporation system at TSC, where the subsequent Ti/Pd/Au deposition was done. The sample was then transferred back to UCSB in a nitrogen ambient environment for the lift-off process.

4.2.2 TEM analysis

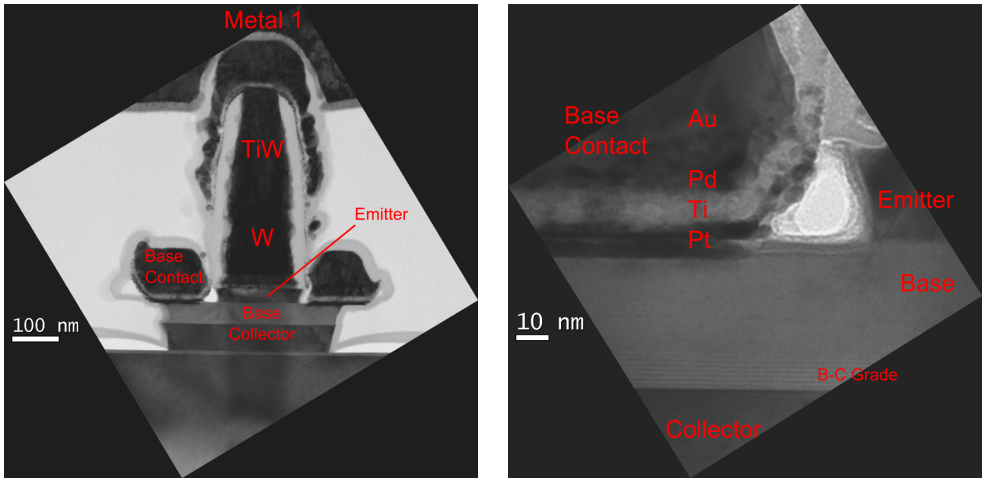
In order to analyze the electrical data, it is imperative to know the physical dimensions of the device. Transmission electron microscopy (TEM) cross-section of the devices is a suitable mean of obtaining the exact dimensions because of its magnification power and resolution. TEM *lamellae* were sliced from DHBT samples and polished using dual beam focused ion-beam/SEM (FEI Helios Nanolab 600i). The bright-field TEM images of the *lamellae* were obtained using FEI Tecnai G2 TEM.

Fig.4.5a is the TEM cross-section normal to the emitter stripe of the device with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=500 nm defined by e-beam lithography. The composite refractory metal stack above the Mo emitter contact consists of ∼250 nm of W and ∼250 nm of TiW. Due to the dry etch profile of W/TiW stack and the thickness of dual dielectric sidewalls (20 nm each), the base-emitter junction is 70 nm wider than the design, i.e. $W_{\mathrm{E,actual}}$=170 nm for $W_{\mathrm{E,design}}$=100 nm. According to TEM, W_{gap}=10∼20 nm, and the undercut to the base-collector mesa (W_{undercut}) is 50∼75 nm on both sides of the mesa. The average width of the base contact on each side of the emitter for the device with $W_{\mathrm{E,design}}$=100 nm and $W_{\mathrm{BM,design}}$=500 nm is then:

$W_{\mathrm{B,Cont.}} = (W_{\mathrm{BM,design}} - W_{\mathrm{E,actual}} - 2 \times (W_{\mathrm{gap}} + W_{\mathrm{undercut}}))/2$

$= (500 - 170 - 2 \times (15 + 62.5))/2$=87.5 nm.

Fig. 4.5b is the TEM cross-section of the same device as Fig. 4.5a under higher magnification power zoomed in at the vicinity of the emitter and the base contact. As shown in the TEM cross-section, 1 2 nm of InGaAs was removed from the surface of the base semiconductor, presumably due to the diluted HCl etch



(a) (b)

Figure 4.5: TEM cross-section normal to the emitter stripe of a device on DHBT63B with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=500 nm. (a) An overview of the device. (b) zoomed in at the vicinity of the base contact and emitter.

prior to the Pt deposition. Also shown in the TEM, the base metal penetrates the InGaAs base for 4 nm, which is caused by the reaction between Pt and As atoms [6]. As a result, the base contact is located at ∼5 nm below the base-emitter junction.

Fig. 4.6 is the TEM cross-section parallel to the emitter stripe of another device with $L_{\mathrm{E,design}}$=3 um zoomed in at the vicinity of the base post. The undercut to both sides of the InP emitter semiconductor stripe is ∼150 nm. Thus, the actual length of the emitter stripe ($L_{\mathrm{E,actual}}$) is 300 nm shorter than the design length ($L_{\mathrm{E,design}}$). The base-collector mesa beneath the base post pedestal was intentionally exposed and undercut (∼200 nm) during the device isolation wet etch to reduce C_{CB} and increase f_{max}.

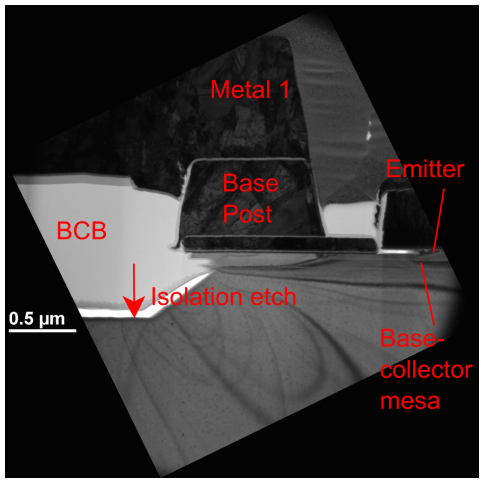
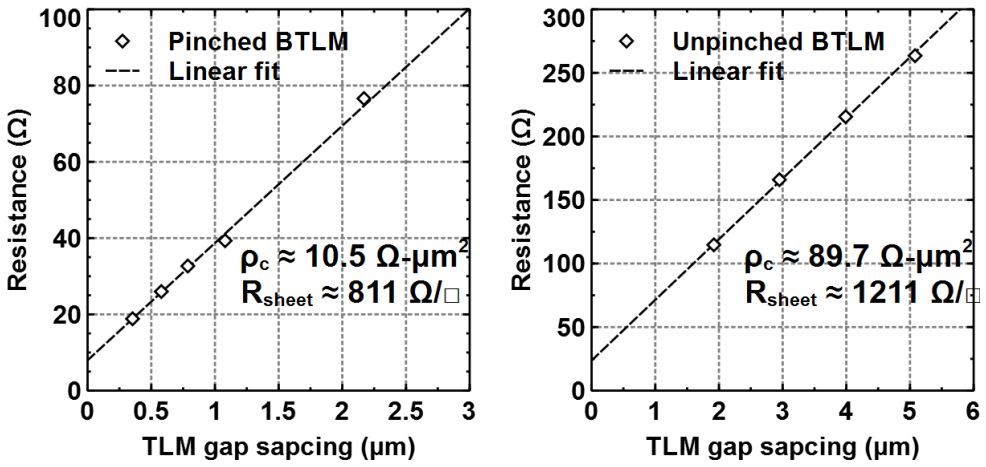


Figure 4.6: TEM cross-section parallel to the emitter stripe of a device on DHBT63B with $L_{\mathrm{E,design}}$=3 μm. The image is zoomed in at the vicinity of the base post.

4.2.3 TLM results

The pinched and unpinched base TLM results of DHBT63B are shown in fig. 4.7a and fig. 4.7b. The values of the base sheet resistance obtained from the pinched TLM and the unpinched TLM are 811 and 1211 $\Omega/\square$, respectively. The pinched TLM result agrees with the TLM result measured by IQE (768$\sim$792 $\Omega/\square$) on the DHBT63 wafer with the InGaAs surface terminated by the InP emitter layer. The specific base contact resistivity extrapolated from the pinched TLM results is 10.5 $\Omega-\mu\mathrm{m}^2$, which is more than twice the value required (4 $\Omega-\mu\mathrm{m}^2$) to achieve 1 THz f_{max} at W_{E}=100 nm. The high specific contact resistivity could be the result of UV-6 residues during the Pt deposition and/or contamination during sample transportation between TSC and UCSB. A more thorough analysis on the base contact resistivity will be addressed in the later section along with the base contact resistance extracted from the RF measurements. Fig. 4.8 is the collector TLM result of DHBT63B. The collector sheet resistance and specific



(a) (b)

Figure 4.7: (a) Pinched and (b) Unpinched base TLM data of DHBT63B. The width of TLM structure and the distances between metal pads (gap spacing) were measured with SEM.

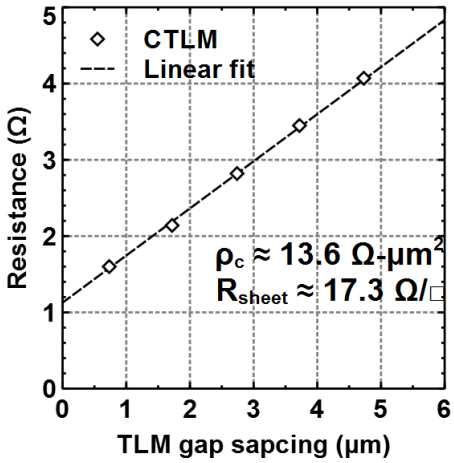


Figure 4.8: Collector TLM result of DHBT63B. The width of TLM structure and the distances between metal pads (gap spacing) were measured with SEM.

contact resistivity are $17.3\,\Omega/\square$ and $13.6\,\Omega - \mu\text{m}^2$, respectively.

4.2.4 Transistor DC characteristics

For the epitaxial design of DHBT63, the maximum emitter current density limited by the Kirk effect ($J_{C,Kirk}$) at v_{CB}=0.6 V is approximately 34-mA/μm^2. The actual limit could be ~20% higher if the current spreading effect in the collector region is included. However, most of the devices on DHBT63B could not reach this limit and the base-emitter junction failed at J_E= 30~35 mA/μm^2. Therefore, no Krik effect was observed from both DC and RF measurement. According to the TEM in fig. 4.5b, the distance the base metal and the sharp corner on the top of the emitter semiconductor is less than 10 nm. Hence, the failure mode of the B-E junction is possibly caused by the dielectric breakdown through the SiN_x sidewall between the base metal and the sharp corner on the top of the emitter. The DC measurements preceded the RF measurements. To avoid the failure of the B-E junction before the subsequent RF measurement, current and power compliance was set for the emitter terminal according to the emitter width of the DUT during every DC measurement. In addition, the sweeping range for V_{BE} was limited from 0 to 1 V in the measurement for diode I-V characteristics (Gummel plots).

Fig. 4.9a is the common emitter output characteristic of a device with $W_{E,design}$ =100 nm, $W_{BM,design}$=500 nm, and $L_{E,design}$=3 μm, i.e. $W_{E,actual}$=170 nm, $W_{B,Cont.}$= 87.5 nm, and $L_{E,actual}$=2.7 μm. The base current varies from 0 to 200 μA with a step of 20 μA. The Gummel plot of the same device at V_{CB}=0 V is shown in fig. 4.9b. At V_{BE}=1 V, the emitter current density and the DC current gain (β) are approximately 32.5 mA/μm^2 and 22, respectively. The base-emitter (B-E) and the base-collector (B-C) diode ideality factors, η_B and η_C, extrapolated from the data within V_{BE}=0.7 to 0.9 V are 2.49 and 1.66, respectively. Because the B-E

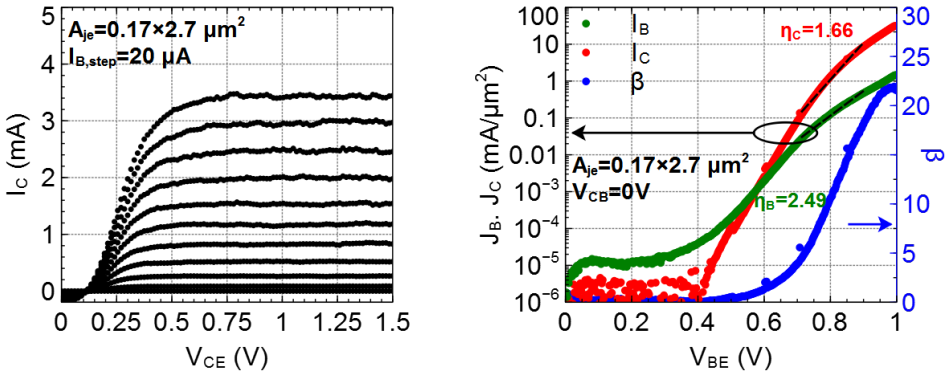


Figure 4.9: DC characteristics of the device with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$ = 500 nm, and $L_{\mathrm{E,design}}$=3 μm.(a) Common emitter output characteristics. The increment of the base current ($I_{\mathrm{B,step}}$) is 20 μA. (b) I-V characteristics of B-E and B-C diodes (Gummel plot).

diode is an abrupt junction, when increasing V_{BE} by an amount of δV_{BE} the barrier height for electron injection into the base is changed by $\delta V_{\mathrm{BE}} - \delta V_{\mathrm{BE,p}}$, where the drop $\delta V_{\mathrm{BE,p}}$ is due to the modulation of the electrostatic potential in the base region [7]. Therefore, more δV_{BE} is required to increase I_{E} to a given magnitude, and hence the ideality factor becomes higher.

Because of the improvement in both the composite emitter stack and the back end process flow, the transistor yield on DHBT63B has been greatly improved. Approximately 80 90% of the devices probed demonstrated DC characteristics previously shown. With the sufficient transistor yield, the dependence of DC-β on device dimensions could be analyzed. For a proper comparison, the DC-β of the devices are sampled at V_{CB}=0 V and J_{E} ≈25 mA/μm^2, which is below $J_{\mathrm{C,Kirk}}$ and close to J_{E} for peak f_τ and f_{max}. Inverse DC-β vs. base-emitter junction periphery to area ratio ($P_{\mathrm{je}}/A_{\mathrm{je}}$) of the devices on DHBT63B is plotted in fig. 4.10. According to the extrapolation, the DC-β (β_{Bulk}) of a device with a very

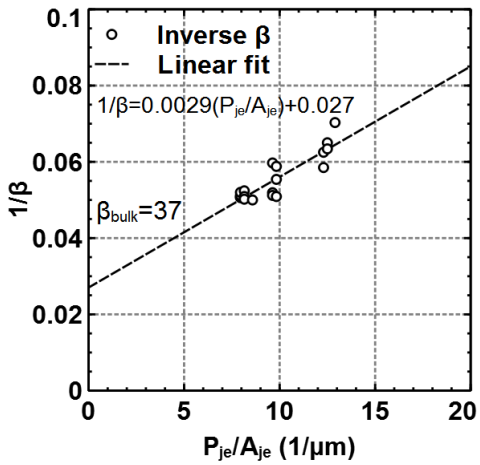


Figure 4.10: Inverse DC-β vs. base-emitter junction periphery to area ratio ($P_{\mathrm{je}}/A_{\mathrm{je}}$) of the devices on DHBT63B.

wide emitter, i.e. $P_{\mathrm{je}}/A_{\mathrm{je}} \rightarrow 0$, is $\sim$37, and the sheet current density of the base edge current ($K_{\mathrm{B,edge}}$) is 72.5 mA/μm. At W_{E}=150 nm, DC-$\beta \approx$15, which implies that approximately 29% of I_{B} is due to the edge current.

4.2.5 RF performance

For a device on DHBT63 with the assumed parameters listed in table. 4.2, the calculated f_τ and f_{max} are approximately 600 and 1100 GHz, respectively. However, the highest f_τ/f_{max} measured on DHBT63B is approximately 500/700 GHz, obtained from a device with $W_{\mathrm{E,actual}}$=220 nm, $W_{\mathrm{B,Cont.}}$=187.5 nm, $L_{\mathrm{E,actual}}$=2.7 μm. Fig. 4.11 is a summary of the peak cut-off frequencies measured on DHBT63B. The peak current gain cut-off frequency varies from 490 to 550 GHz, and the peak power gain cut-off frequency lies within 530 and 700 GHz.

A possible reason for the discrepancies between the calculated and measured

Parameters		Value	Unit
Emitter width	W_{E}	100	nm
Emitter length	L_{E}	3	μm
B-E spacing	W_{gap}	15	nm
Base contact width (single side)	$W_{\mathrm{B,Cont.}}$	100	nm
Excessive base post area	A_{BP}	0.8	$\mu\mathrm{m}^2$
Emitter contact resistivity	$\rho_{\mathrm{E,cont.}}$	4	$\Omega-\mu\mathrm{m}^2$
Base contact resistivity	$\rho_{\mathrm{B,cont.}}$	4	$\Omega-\mu\mathrm{m}^2$
Base sheet resistance	$R_{\mathrm{sheet,B}}$	820	$\Omega/\square$
e^- diffusivity in the base	$D_{\mathrm{n,B}}$	40	cm^2/s
e^- velocity in the collector	v_{C}	3.2×10^7	cm/s
Emitter current density	J_{E}	36	$\mathrm{mA}/\mu\mathrm{m}^2$
B-E diode ideality factor	η_{B}	2	

Table 4.2: Parameters assumed in the cut-off frequencies calculation of DHBT63.

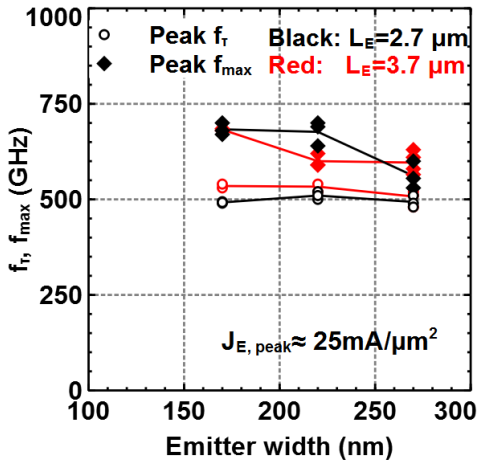


Figure 4.11: Peak f_τ and f_{max} vs. base-emitter junction width of the devices with emitter length (L_{E}) of 2.7 and 3.7 μm on DHBT63B.

$f_\tau/f_{\max}$ is the low emitter current density. The optimal bias condition for peak $f_\tau/f_{\max}$ of a DHBT is when r_e and C_{CB} are both near their minima, which usually lies within the vicinity of the onset of Kirk effect. As mentioned previously, the base-emitter junctions of DHBT63B could not sustain the current density limited by the Kirk effect, i.e. the diode failed before reaching $J_{C,KirK}$. Therefore, no Kirk effect nor the peaking of $f_\tau/f_{\max}$ has been observed. Another cause of low $f_{\max}$ is high base specific contact resistivity, which increases the RC delay in the base-collector mesa.

In this section, the RF measurement results of two devices on DHBT63B are selected and reported as examples for the probed devices. In order to understand measured RF performance, the base access resistances and the base-collector capacitances extracted from small-signal equivalent circuit model of each probed devices are analyzed.

The first device has $W_{E,design}$=150 nm, $W_{BM,design}$=750 nm, and $L_{E,design}$ =3 μm. According to the TEM analysis, the area of the base-emitter junction (A_{je}) is $\sim 0.22 \times 2.7\,\mu$m, and the average width of the base contact on both sides of the emitter ($W_{B,Cont.}$) is ~187.5 nm. Fig. 4.12a shows the unilateral Mason's gain (U) and current gain (H_{21}) vs. frequency at J_E=29 mA/μm^2, I_B=900 μA, and V_{CE}=1.5 V. Under this bias condition, the device exhibits $f_\tau/f_{\max}$ ≈509/702 GHz according to the single-pole fit (dashed lines). Fig. 4.12b is the Smith chart showing the de-embedded two-port S-parameters of this device from 0.1 to 67 GHz. Using ADS, a small-signal equivalent circuit model based on the hybrid-π model is simulated and fit to the experimental data. The dashed lines in fig. 4.12b are the ADS simulation results. The small-signal equivalent circuit model used in

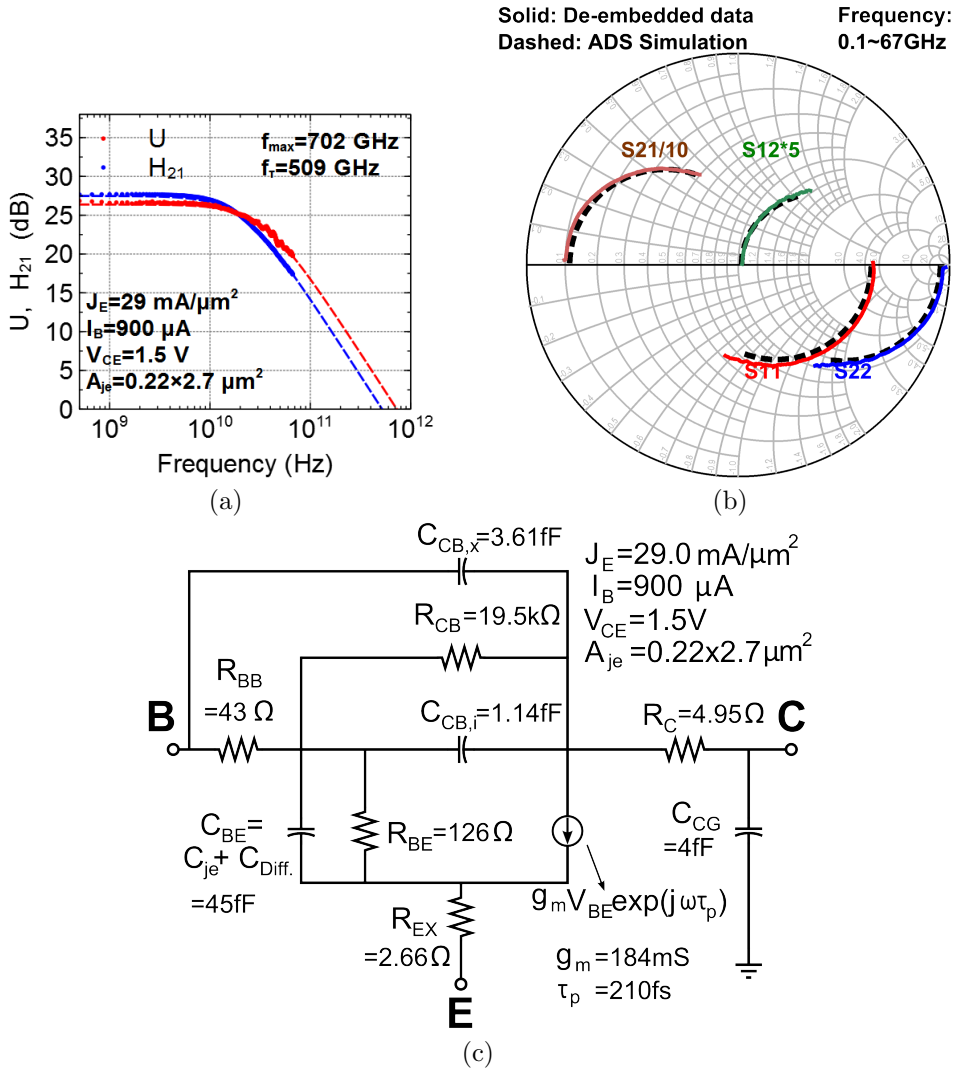
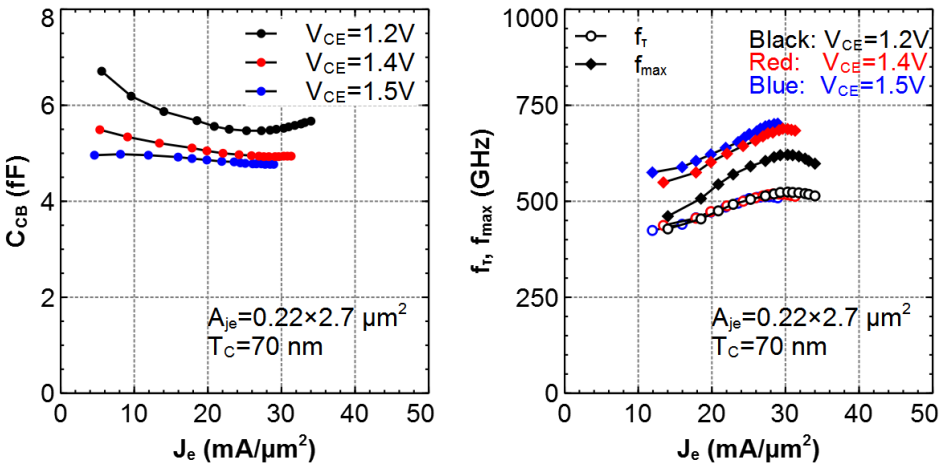


Figure 4.12: RF measurement results of a device DHBT63B with $W_{\mathrm{E,design}} = 150\,\mathrm{nm}$, $W_{\mathrm{BM,design}}$=750 nm, and $L_{\mathrm{E,design}}$=3 μm: (a) unilateral Mason's gain and H_{21} vs. frequency, (b) Two-port S-parameters vs. frequency, and (c) small-signal equivalent circuit. In both (a) and (b), the solid lines represent the experimental data, and the dashed lines are the ADS simulation results.

ADS simulation is shown in fig. 4.12c.

As mentioned in chapter 2, when $J_{\mathrm{E}} < J_{\mathrm{C,Kirk}}$, C_{CB} decreases as the current density increases due to velocity modulation citeRitter99TED. When $J_{\mathrm{E}} > J_{\mathrm{C,Kirk}}$,



(a) (b)

Figure 4.13: Current dependency of C_{CB} and cut-off frequencies extracted from the device on DHBT63B with $W_{E,design}$=150 nm, $W_{BM,design}$=750 nm, and $L_{E,design}$=3 μm at V_{CE}=1.2, 1.4, and 1.5 V.(a) C_{CB} vs. J_E. (b)f_τ and f_{max} vs. J_E

C_{CB} increases as the current density increases because of the base push-out (Kirk effect). For a given V_{CB} or V_{CE} , C_{CB} reaches minimum when $J_E \approx J_{C,Kirk}$. Fig. 4.13a shows the extracted C_{CB} vs. J_E from the device with $W_{E,design}$=150 nm, $W_{BM,design}$=750 nm, and $L_{E,design}$=3 μm at various V_{CE}. For V_{CE}=1.2 V, the minimum of C_{CB} was observed at J_E=27.3 mA/μm^2, which is ~18.7% higher then the calculated Kirk effect limited current density (23 mA/μm^2). The higher $J_{C,Kirk}$ was expected because the areas associated with J_E and J_C are A_{je} and A_{jc}, and $A_{je} < A_{jc}$ (current spreading effect). When V_{CE} was increased to 1.5 V, no C_{CB} minimum was observed because the base-emitter junction failed before reaching $J_{C,Kirk}$.

The cut-off frequencies vs. current density is shown in fig. 4.13b. The current gain cut-off frequency (f_τ) is almost independent of V_{CE} and peaks at $J_E \approx$30 mA/μm^2. The maxima of f_{max} are associated with the minima of C_{CB}.

Again, since the base-emitter junction failed before reaching $J_{C,Kirk}$ at V_{CE}=1.5 V, no maximum has been observed from f_{max} at this V_{CE}.

The RF measurement results of a device with $W_{E,design}$=100 nm, $W_{BM,design}$= 500 nm, and $L_{E,design}$=3 μm is shown in fig. 4.14. From TEM analysis, the area of the base-emitter junction (A_{je}) is $\sim$ 0.17 $\times$ 2.7 μm, and the average width of the base contact on both sides of the emitter ($W_{B,Cont.}$) is $\sim$87.5 nm. Fig. 4.14a shows the unilateral Mason's gain (U) and current gain (H_{21}) vs. frequency at J_E=28.5 mA/μm^2, I_B=900 μA, and V_{CE}=1.56 V. Under this bias condition, the device achieves peak $f_\tau/f_{max} \approx$ 490/670 GHz according to the single-pole fit (dashed lines). The Smith chart showing the de-embedded two-port S-parameters of this device from 0.1 to 67 GHz is plotted in fig. 4.14b. The dashed lines in fig. 4.14b are the S-parameters simulated by ADS using the small-signal hybrid-π equivalent circuit model shown in fig. 4.14c.

Fig. 4.15a is the extracted C_{CB} vs. J_E from the device with $W_{E,design}$= 100 nm, $W_{BM,design}$=500 nm, and $L_{E,design}$=3 μm at various V_{CB}. For V_{CB}=0.2 V, the minimum of C_{CB} was observed at J_E=29.2 mA/μm^2, which is $\sim$27% higher then the calculated value at 0.2 V (23 mA/μm^2). Similar to the device reported previously with a wider emitter, when V_{CB} was increased to 0.6 V, no C_{CB} minimum was observed because the base-emitter junction failed prior to reaching $J_{C,Kirk}$.

The cut-off frequencies vs. current density is shown in fig. 4.15b. Similarly, f_τ is independent of V_{CB} and peaks at $J_E \approx$30.5 mA/μm^2. The maxima of f_{max} were observed for V_{CB}=0.2 and 0.4 V. However, no maximum has been observed at V_{CB}=0.6 V because of the J_E which the B-E junction could sustain is lower than the Kirk effect limited current density.

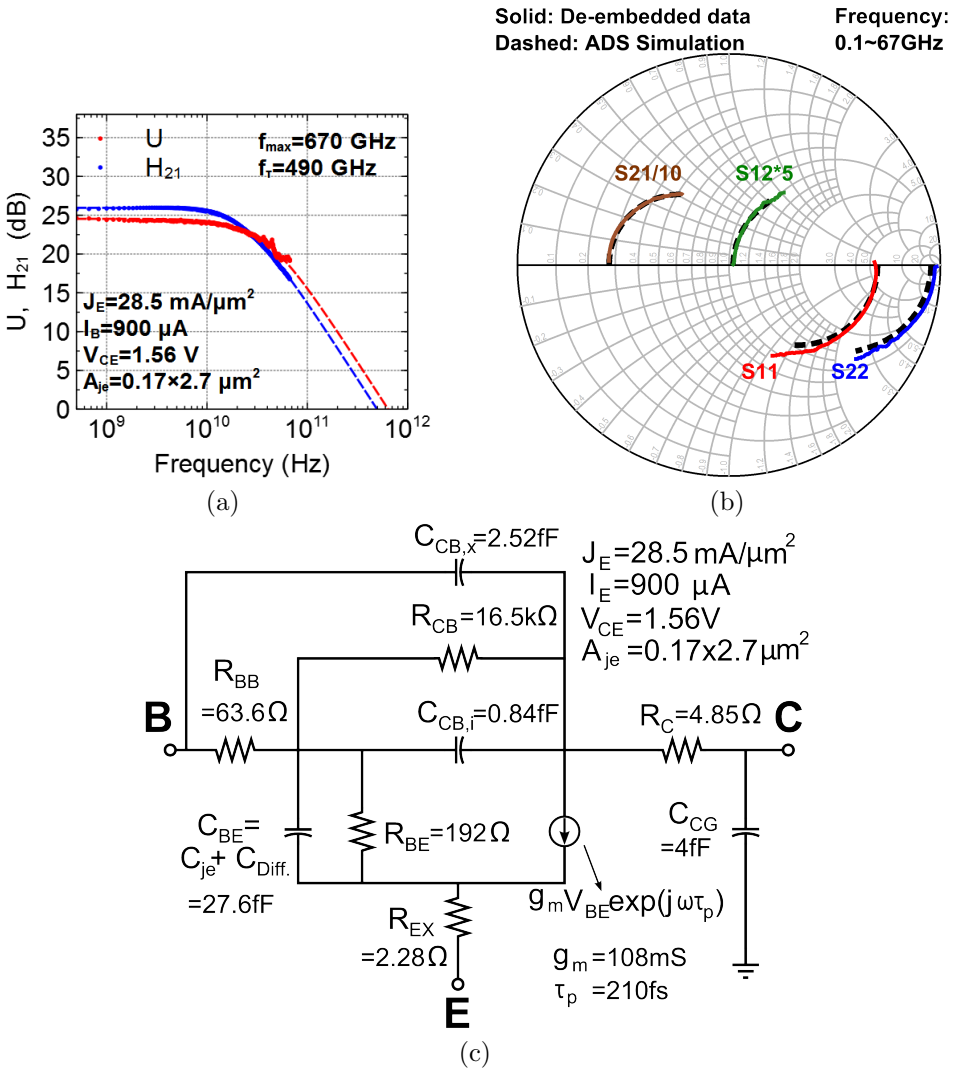
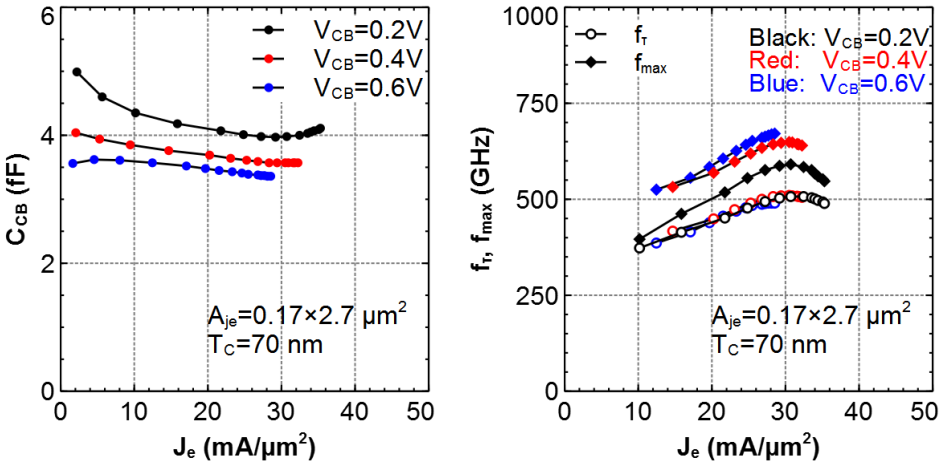


Figure 4.14: RF measurement results of a device on DHBT63B with $W_{\mathrm{E,design}} = 100\,\mathrm{nm}$, $W_{\mathrm{BM,design}}$=500 nm, and $L_{\mathrm{E,design}}$=3 μm: (a) unilateral Mason's gain and H_{21} vs. frequency, (b) Two-port S-parameters vs. frequency, and (c) small-signal equivalent circuit. In both (a) and (b), the solid lines represent the experimental data, and the dashed lines are the ADS simulation results.



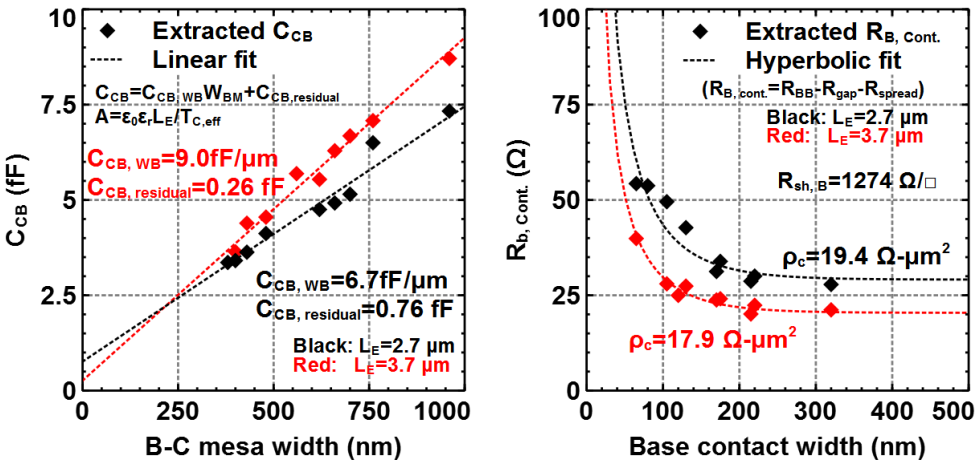
(a) (b)

Figure 4.15: Current dependency of C_{CB} and cut-off frequencies extracted from the device on DHBT63B with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=500 nm, and $L_{\mathrm{E,design}}$=3 μm at V_{CB}=0.2, 0.4, and 0.6 V.(a) C_{CB} vs. J_{E}. (b)f_τ and f_{max} vs. J_{E}

By fitting the small-signal equivalent circuit models to the experimental data using ADS simulation, the parasitic resistances and capacitances of every probed device were extracted from the results biased at V_{CB}=0.5∼0.6 V and J_{E}=25∼30 mA/μm^2. Two dominating parasitics of f_{max}, C_{CB} and the base access resistance (R_{BB}), have been analyzed in order to understand the causes of low cut-off frequencies (highest measured f_{max} ≈700 GHz).

The static (parallel-plate)component of C_{CB} can be written in the following expression:

$$\begin{aligned} C_{\mathrm{CB}} &= \frac{\epsilon_0\epsilon_{\mathrm{r}}A_{\mathrm{C}}}{T_{\mathrm{C,eff}}} = \frac{\epsilon_0\epsilon_{\mathrm{r}}L_{\mathrm{E}}}{T_{\mathrm{C,eff}}}(W_{BM,design} - 2W_{undercut} + \frac{A_{\mathrm{BP}}}{L_{\mathrm{E}}}) \\ &= \frac{\epsilon_0\epsilon_{\mathrm{r}}L_{\mathrm{E}}W_{BM,design}}{T_{\mathrm{C,eff}}} + C_{\mathrm{CB,residual}} \\ &= C_{\mathrm{CB,WB}} \times W_{BM,design} + C_{\mathrm{CB,residual}} \ , \end{aligned} \tag{4.2}$$



(a) (b)

Figure 4.16: Dimension dependence of (a) C_{CB} (vs. $W_{\mathrm{BM,design}}$) and (b) $R_{\mathrm{B,cont.}}$ (vs. $W_{\mathrm{B,cont.}}$) from device with L_{E}=2.7 and 3.7 μm biased at V_{CB} = 0.5∼0.6 V and J_{E}=25∼30 mA/μm^2.

where ϵ_0 and ϵ_{r} are the vacuum permittivity and the relative permittivity. For InP collector, ϵ_{r} ≈13. A_{C} and $T_{C,eff}$ are the area and the depletion region width of the base-collector junction, respectively. A_{BP} is the excessive portion of A_{C} beneath the base post. The slope, $C_{\mathrm{CB,WB}}$, is the capacitance per unit width of the B-C mesa. The intercept, $C_{\mathrm{CB,residual}}$, is the effect due to both the B-C mesa undercut and excessive base post area, which are independent to $W_{\mathrm{BM,design}}$.

The extracted C_{CB} vs. the designed base mesa width ($W_{BM,design}$) is plotted in Fig. 4.16a. The slopes of the curves, $C_{\mathrm{CB,WB}}$, for devices with L_{E}=2.7 and 3.7 μm are 6.7 and 9 fF/μm, respectively. The trend of $C_{\mathrm{CB,WB}}$ vs. L_{E} indicates that $T_{\mathrm{C,eff}}$ ≈50 nm, which is less than the overall collector thickness (70 nm). The intercepts of the curves, $C_{\mathrm{CB,residual}}$, for devices with L_{E}=2.7 and 3.7 μm are 0.76 and 0.26 fF, respectively.

Eq. 4.2 can be transformed into:

$$A_{\mathrm{BP}} = (\frac{C_{\mathrm{CB,residual}}}{C_{\mathrm{CB,WB}}} + 2W_{undercut})L_{\mathrm{E}}. \tag{4.3}$$

If $C_{\mathrm{CB,WB}}$, $C_{\mathrm{CB,residual}}$, $W_{undercut}$, and L_{E} known, the excessive area beneath the base post (A_{BP}) can be obtained. From TEM analysis, $W_{undercut}$=62.5 nm. Thus, A_{BP} is approximately 0.64 and 0.57 μm^2 for devices with L_{E}=2.7 and 3.7 μm, respectively.

From eq. 2.14, the base access resistance can be written as:

$$\begin{aligned} R_{\mathrm{BB}} &\approx R_{\mathrm{BE,spread}} + R_{\mathrm{gap}} + R_{\mathrm{B,cont.}} \\ &= \frac{R_{\mathrm{sh,em}}W_{\mathrm{E}}}{12L_{\mathrm{E}}} + \frac{R_{\mathrm{sh,gap}}W_{\mathrm{gap}}}{2L_{\mathrm{E}}} + \frac{\sqrt{R_{\mathrm{sh,B,cont.}}\rho_{\mathrm{B,cont.}}}}{2L_{\mathrm{E}}} coth(\frac{W_{\mathrm{B,cont.}}}{L_{\mathrm{T}}}) \ , \end{aligned} \tag{4.4}$$

where $R_{\mathrm{sh,em}}$, $R_{\mathrm{sh,gap}}$, and $R_{\mathrm{sh,B}}$ are the sheet resistance beneath the emitter, in the spacing between the base contact and the emitter (the extrinsic base), and beneath the base contact, respectively. $\rho_{\mathrm{B,cont.}}$ is the specific contact resistivity of the base contact. $L_{\mathrm{T}} = \sqrt{\rho_{\mathrm{B,cont.}}/R_{\mathrm{sh,B,cont.}}}$ is the transfer length.

The base contact resistance term ($R_{\mathrm{B,cont.}}$) is analyzed in order to estimate $\rho_{\mathrm{B,cont.}}$ of the experimental devices. To extract $R_{\mathrm{B,cont.}}$, eq. 4.4 can be transformed into:

$$\begin{aligned} R_{\mathrm{B,cont.}} &= R_{\mathrm{BB}} - R_{\mathrm{BE,spread}} - R_{\mathrm{gap}} \\ \frac{\sqrt{R_{\mathrm{sh,B,cont.}}\rho_{\mathrm{B,cont.}}}}{2L_{\mathrm{E}}} coth(\frac{W_{\mathrm{B,cont.}}}{L_{\mathrm{T}}}) &= R_{\mathrm{BB}} - \frac{R_{\mathrm{sh,em}}W_{\mathrm{E}}}{12L_{\mathrm{E}}} - \frac{R_{\mathrm{sh,gap}}W_{\mathrm{gap}}}{2L_{\mathrm{E}}} \ , \end{aligned} \tag{4.5}$$

From TEM analysis, the actual dimensions (W_{E}, L_{E}, W_{gap}, and $W_{\mathrm{B,cont.}}$) of the devices are known. $R_{\mathrm{sh,em}}$ and $R_{\mathrm{sh,gap}}$ are obtained from the pinched and the unpinched base TLM structure (fig. 4.7). The contribution of $R_{\mathrm{BE,spread}}$ and

R_{gap} were calculated and then subtracted from R_{BB} to extract $R_{B,cont.}$. Also from the TEM analysis, the base metal penetrated 5∼6 nm below the B-E junction. With 6 nm penetration depth and ∼ 2 nm depletion width under the base contact, $R_{sh,B}$ ≈1274 Ω/□. A plot of $R_{B,cont.}$ vs. $W_{B,cont.}$ is shown in fig. 4.16b. By fitting the hyperbolic expression of $R_{B,cont.}$, $\rho_{B,cont.}$ can be extrapolated. The result from device with L_E=2.7 and 3.7 μm indicates $\rho_{B,cont.}$=19.4 and 17.9 Omega − μm^2, respectively. Compare to $\rho_{B,cont.}$ obtained from base TLMs, $\rho_{B,cont.}$ extracted from two-port S-parameters are almost two times higher.

Such high $\rho_{B,cont.}$ causes high R_{BB} and longer RC delay in the B-C mesa, reducing f_{max}. High $\rho_{B,cont.}$ also increase the L_T, which means $R_{B,cont.}$ increases more rapidly when $W_{B,cont.}$ decreases. Therefore, the f_{max} of the devices with narrow emitter and B-C mesa are further reduced. The poor base specific contact resistivity explains the measured low f_{max}.

4.3 DHBT58H

4.3.1 Device structure and process feature

The design of DHBT58 utilizes a 30 nm thick InP emitter doped at $5 \times 10^{19}\,cm^{-3}$ for the top 15 nm and $2 \times 10^{18}\,cm^{-3}$ for the bottom 15 nm. The p-type base is composed of 20 nm of InGaAs with a doping-grade from $12 \times 10^{19}\,cm^{-3}$ at the emitter side to $8 \times 10^{19}\,cm^{-3}$ at the collector side. The design employs a 100 nm thick collector structure (setback, superlattice, InP collector) with doping concentration of $5 \times 10^{16}\,cm^{-3}$. The detailed epitaxial structure is listed in table. 4.3. The band diagram of the device under V_{BE}=1.2 V and V_{CB}=0.6 V is shown

in fig. 4.17. The solid lines are the conduction band and the valance band if the space charge associated with the collector current in the collector region is neglected, whereas the dashed lines are the bands considering the space charge in the collector at $J_C \approx 25\,\mathrm{mA}/\mu\mathrm{m}^2$.

The base-emitter junction width of the devices on DHBT63B is 70 nm wider

Layer	Semiconductor	Thickness (Å)	Doping (cm^{-3})
Emitter cap	$In_{0.53}Ga_{0.47}As$	100	8×10^{19}:Si
Emitter	InP	150	5×10^{19}:Si
Emitter	InP	150	2×10^{18}:Si
Base	$In_{0.53}Ga_{0.47}As$	200	$12 - 8 \times 10^{19}$:C
Setback	$In_{0.53}Ga_{0.47}As$	135	5×10^{16}:Si
B-C grade	-	165	5×10^{16}:Si
δ-doping	InP	30	3.6×10^{18}:Si
Collector	InP	670	5×10^{16}:Si
Sub-collector	InP	75	2×10^{19}:Si
Sub-collector	$In_{0.53}Ga_{0.47}As$	50	4×10^{19}:Si
Sub-collector	InP	3000	1×10^{19}:Si
Etch stop	$In_{0.53}Ga_{0.47}As$	35	undoped
Substrate	InP	-	undoped

Table 4.3: Epitaxial structure of DHBT58.

than the design value. As a result, the base contact width is 35 nm narrower than the design value. To compensate this effect, in the fabrication of DHBT58H, the emitter width including the SiN_x sidewall thickness (20 nm) is measured by SEM prior to the InP emitter wet etch. An extra 40 nm due to the SiN_x sidewall is added to the assumed emitter junction width ($W_{\mathrm{E,assumed}}$). In response to the extra $W_{\mathrm{E,design}}$, the B-C mesa width ($W_{\mathrm{BM,design}}$) was increased to $W_{\mathrm{BM,mod.}}$ to maintain the ratio between the emitter and base contact, i.e.

$$W_{\mathrm{BM,mod.}} = W_{\mathrm{E,assumed}} \frac{W_{\mathrm{BM,design}}}{W_{\mathrm{E,design}}} \ . \tag{4.6}$$

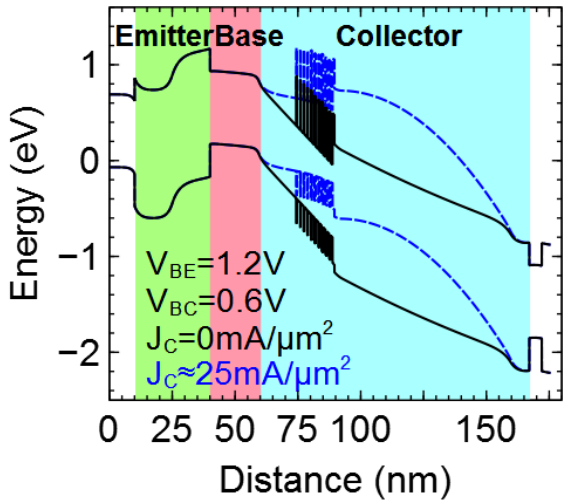


Figure 4.17: Computed band diagram of DHBT58 under V_{BE}=1.2 V and V_{CB}=0.6 V. The solid lines are the conduction and valance bands when J_{C}=0 mA/μm^2. The dashed line represent the conduction and valance bands considering the space charge region in the collector at J_{C} ≈25 mA/μm^2.

For device with $W_{\mathrm{E,design}}$=100 nm and $W_{\mathrm{BM,design}}$=450 nm, the B-C mesa width after modulation $W_{\mathrm{BM,mod.}}$ is 630 nm.

The base metalization of DHBT58H was also a lift-off process using UV-6 as the resist. Nonetheless, the resist damage problem due to electron bombardment in UCSB's E-Beam 4 have been solved by removing the Ni source from the chamber before the evaporation. Therefore, the base metalization was done entirely in E-Beam 4. In addition, the process flow for the composite third sidewall was incorporated into the fabrication of DHBT58H. The lift-off base contact of DHBT58H is composed of 6/12/17/65/10 nm of Pt/Ti/Pd/Au/Ti. The extra Ti layer on top of Au layer serves as an adhesion layer between Au and the dielectric of the third sidewall. After the base contact lift-off, the extrinsic base is encapsulated by ALD Al_2O_3 and PECVD SiN_x.

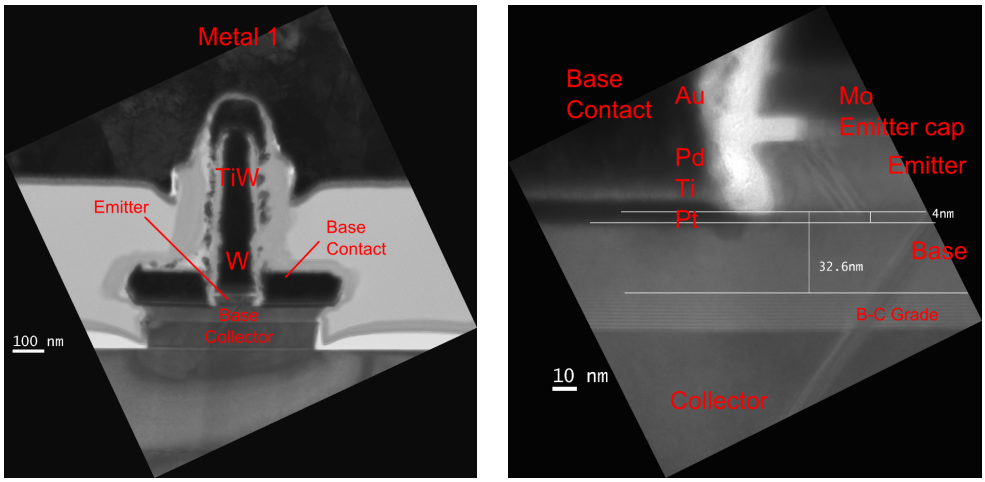
4.3.2 TEM analysis

Fig. 4.18a is the TEM cross-section normal to the emitter stripe of the device with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=450 nm defined by e-beam lithography. The composite refractory metal stack above the Mo emitter contact consists of ∼150 nm of W and ∼350 nm of TiW. With higher TiW to W thickness ratio and recalibrated dry etch recipe, a more vertical the sidewall profile was achieved. The width of the composite stack at its bottom is 10 nm wider than $W_{\mathrm{E,design}}$. The base-emitter junction width is approximately the same as stack width, i.e. $W_{\mathrm{E,actual}}$=110 nm for $W_{\mathrm{E,design}}$=100 nm. This means that $W_{\mathrm{E,assumed}}$ from SEM before InP emitter wet etch was incorrect, and the modulation for the B-C mesa width is unnecessary. Thus, the B-C mesa is too wide, causing unnecessary increase in C_{CB}. According to TEM, W_{gap} ≈10 nm, and the undercut to the base-collector mesa (W_{undercut}) is ∼50 nm on both sides of the mesa. The average width of the base contact on each side of the emitter for the device with $W_{\mathrm{E,design}}$=100 nm and $W_{\mathrm{BM,design}}$=450 nm is then:

$W_{\mathrm{BCont.}} = (W_{\mathrm{BM,mod.}} - W_{\mathrm{E,actual}} - 2 \times (W_{\mathrm{gap}} + W_{\mathrm{undercut}}))/2$

$= (630 - 110 - 2 \times (10 + 50))/2$=200 nm.

Fig. 4.18b is the TEM cross-section of the same device as Fig. 4.18a under higher magnification power zoomed in at the vicinity of the emitter and the base contact. As shown in the TEM cross-section, 1 nm of InGaAs was removed from the surface of the base semiconductor due to the diluted HCl etch prior to the base metalization. The base metal penetrates the InGaAs base for 4 nm because of the reaction between Pt and As atoms [6]. Hence, the base contact is located at ∼5 nm below the base-emitter junction. The cross-section parallel to the emit-



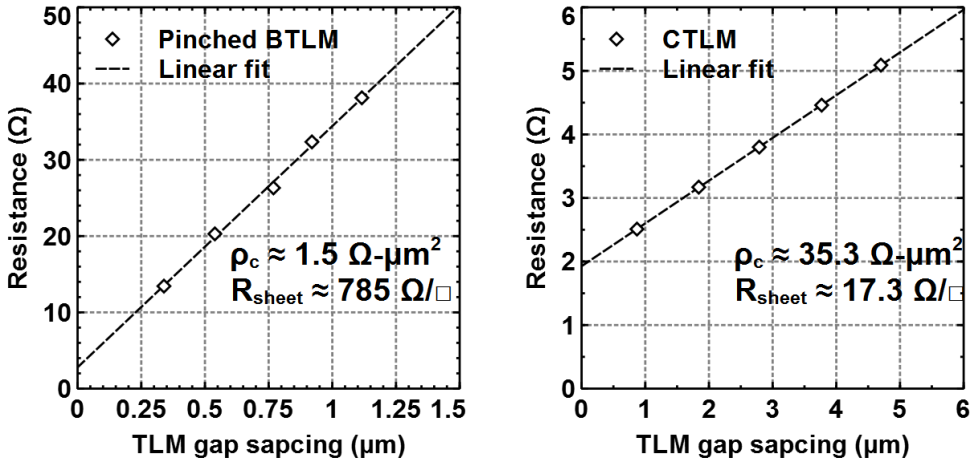
(a) (b)

Figure 4.18: TEM cross-section normal to the emitter stripe of a device on DHBT58H with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=450 nm. (a) An overview of the device. (b) zoomed in at the vicinity of the base contact and emitter.

ter stripe of DHBT58H has not been imaged by TEM. The undercut to the InP emitter along the stripe is assumed to be the same as in DHBT63B, i.e. 150 nm at both tips.

4.3.3 TLM results

The pinched base TLM results of DHBT58H is shown in fig. 4.19a. The values of the base sheet resistance obtained from the pinched TLM is 785 Ω/□, which is slightly higher than the value measured by IQE (717 Ω/□) with the InGaAs surface terminated by the InP emitter layer. The specific base contact resistivity extrapolated from the pinched TLM results is $1.5\,\Omega - \mu\mathrm{m}^2$, which is lower than the value required ($4\,\Omega - \mu\mathrm{m}^2$) to achieve 1 THz f_{max} at W_{E}=100 nm. A complete analysis on the $\rho_{\mathrm{B,cont.}}$ will be addressed in the later section along



(a) (b)

Figure 4.19: (a) Pinched base TLM and (b) Collector TLM data of DHBT58H. The width of TLM structure and the distances between metal pads (gap spacing) were measured with SEM.

with the R_{BB} extracted from the RF measurements. 4.19b is the collector TLM result of DHBT63B. The collector sheet resistance and specific contact resistivity are $35.3\,\Omega/\square$ and $17.3\,\Omega-\mu\mathrm{m}^2$, respectively.

4.3.4 Transistor DC characteristics

The maximum emitter current density limited by the Kirk effect ($J_{\mathrm{C,Kirk}}$) at v_{CB}=0.7 V for the epitaxial design of DHBT58 is approximately $20\,\mathrm{mA}/\mu\mathrm{m}^2$. The actual limit could be more than 20% higher when considering the current spreading effect in the collector region. Unlike DHBT63B, the B-E junction can sustain the Kirk effect limited current density. However, to protect the B-E junction from failure before the subsequent RF measurement, current and power compliance was set for the emitter terminal during the DC measurements. The sweeping range for V_{BE} was limited from 0 to 1 V in the measurement for diode I-V characteristics

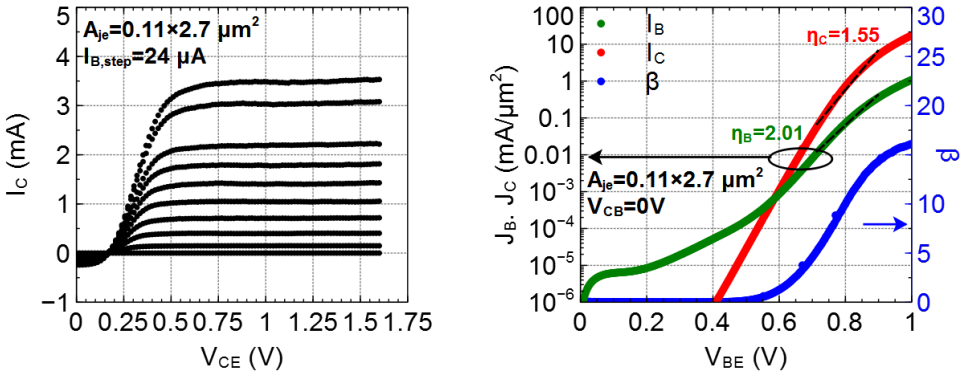


Figure 4.20: DC characteristics of the device with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$ = 600 nm, and $L_{\mathrm{E,design}}$=3 μm.(a) Common emitter output characteristics. The increment of the base current ($I_{\mathrm{B,step}}$) is 24 μA. (b) I-V characteristics of B-E and B-C diodes (Gummel plot).

(Gummel plots).

Fig. 4.20a is the common emitter output characteristic of a device with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=600 nm, and $L_{\mathrm{E,design}}$=3 μm, i.e. $W_{\mathrm{E,actual}}$ =110 nm, $W_{\mathrm{B,cont.}}$=305 nm, and $L_{\mathrm{E,actual}}$=2.7 μm. The base current varies from 0 to 240 μA with a step of 24 μA. The Gummel plot of the same device at V_{CB}=0 V is shown in fig. 4.20b. At V_{BE}=1 V, the emitter current density and the DC current gain (β) are approximately 18 mA/μm^2 and 16.1, respectively. The B-E and B-C diode ideality factors, η_{B} and η_{C}, extrapolated from the data within V_{BE}=0.7 to 0.9 V are 2.01 and 1.55, respectively.

With the better control on the sidewall profile of the emitter metal stack, working devices with $W_{\mathrm{E,actual}}$=85 nm has been achieved on DHBT58H. This extend the range of the device dimensions in the analysis of both DC and RF data. The dependence of DC-β on device dimensions of DHBT58H has been analyzed. The DC-β of the devices are sampled at V_{CB}=0 V and J_{E}=20$\sim$25 mA/μm^2, which

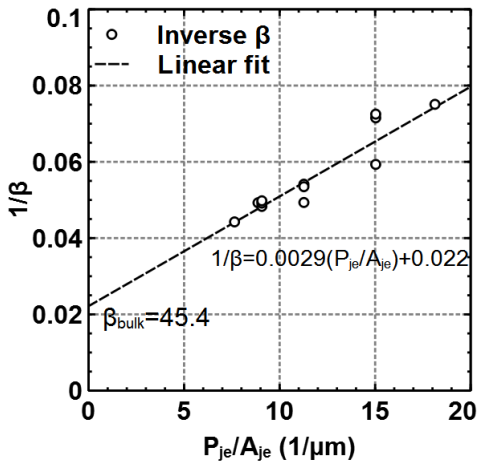


Figure 4.21: Inverse DC-β vs. base-emitter junction periphery to area ratio ($P_{\mathrm{je}}/A_{\mathrm{je}}$) of the devices on DHBT58H.

is close to $J_{\mathrm{C,Kirk}}$ and J_{E} for peak f_τ and f_{max}. Inverse DC-β vs. $P_{\mathrm{je}}/A_{\mathrm{je}}$ of the devices on DHBT58H is plotted in fig. 4.21. According to the extrapolation, the DC-β (β_{Bulk}) of a device with a very wide emitter, i.e. $P_{\mathrm{je}}/A_{\mathrm{je}}$ $\rightarrow$0, is $\sim$45.4, and the sheet current density of the base edge current ($K_{\mathrm{B,edge}}$) is $\sim$70 mA/μm. At W_{E}=85 nm, DC-β $\approx$13.3, which implies that approximately 44% of I_{B} could be attributed to the edge current.

4.3.5 RF performance

The calculated f_τ and f_{max} for a device on DHBT58 with the assumed parameters listed in table. 4.4 are approximately 530 and 1030 GHz, respectively. Nonetheless, the highest f_τ/f_{max} measured on DHBT58H is approximately 390/780 GHz, measured from a device with $W_{\mathrm{E,actual}}$=210 nm, $W_{\mathrm{B,Cont.}}$=255 nm, $L_{\mathrm{E,actual}}$=2.7 μm. Fig. 4.22 is a summary of the peak cut-off frequencies measured on DHBT58H. The peak current gain cut-off frequency varies from 250 to

Parameters		Value	Unit
Emitter width	W_{E}	200	nm
Emitter length	L_{E}	3	μm
B-E spacing	W_{gap}	10	nm
Base contact width (single side)	$W_{\mathrm{B,Cont.}}$	200	nm
Excessive base post area	A_{BP}	0.8	$\mu\mathrm{m}^2$
Emitter contact resistivity	$\rho_{\mathrm{E,cont.}}$	4	$\Omega-\mu\mathrm{m}^2$
Base contact resistivity	$\rho_{\mathrm{B,cont.}}$	4	$\Omega-\mu\mathrm{m}^2$
Base sheet resistance	$R_{\mathrm{sheet,B}}$	750	$\Omega/\square$
e^- diffusivity in the base	$D_{\mathrm{n,B}}$	40	cm^2/s
e^- velocity in the collector	v_{C}	3.2×10^7	cm/s
Emitter current density	J_{E}	17	$\mathrm{mA}/\mu\mathrm{m}^2$
B-E diode ideality factor	η_{B}	2	

Table 4.4: Parameters assumed in the cut-off frequencies calculation of DHBT63.

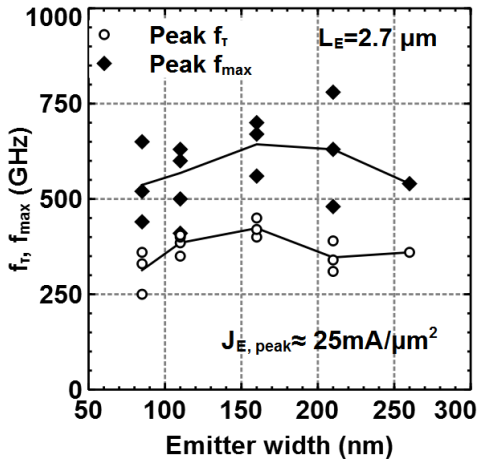


Figure 4.22: Peak f_τ and $f_{\max}$ vs. base-emitter junction width of the devices with emitter length, L_{E}=2.7 μm on DHBT58H.

450 GHz, and the peak power gain cut-off frequency lies within 410 and 780 GHz.

The measured low f_τ could be explained by the high B-E diode ideality factors ($\sim$2.5 for most devices), which result in lower transconductance (g_{m}) and high emitter resistance (r_{E}) [7]. Hence, the charging delays associated with r_{E} increases, reducing f_τ. The discrepancies between the calculated and measured

f_{max} is likely due to high $R_{BB}C_{CB}$ delay. Although the base TLMs of DHBT58H indicates low base specific contact resistivity ($\rho_{B,cont.}$), the $\rho_{B,cont.}$ of the device could still be high according to the analysis on the R_{BB} of DHBT63B. As a result, R_{BB} could be higher than expected, reducing f_{max}. Moreover, the actual emitter widths were overestimated during the fabrication. Therefore, the modulation for B-C mesa widths based on the incorrect estimation are too wide, resulting in more C_{CB}, and hence f_{max} drops.

Similar to DHBT63B, the RF measurement results of two devices on DHBT58H are selected and reported in this section as examples for the probed devices. To understand the measured RF performance, the base access resistances and the base-collector capacitances extracted from small-signal equivalent circuit model of each probed devices are analyzed.

The first device has $W_{E,design}$=200 nm, $W_{BM,design}$=700 nm, and $L_{E,design}$=3 μm. From the TEM analysis, the area of the base-emitter junction (A_{je}) is $\sim$ 0.21 $\times$ 2.7 μm, and the average width of the base contact on both sides of the emitter ($W_{B,Cont.}$) is $\sim$255 nm. Fig. 4.23a is the unilateral Mason's gain (U) and current gain (H_{21}) vs. frequency at J_E=23.3 mA/μm^2, I_B=650 μA, and V_{CE}=1.7 V. The device demonstrates f_τ/f_{max} $\approx$390/780 GHz according to the single-pole fit (dashed lines). Fig. 4.23b is the Smith chart showing the de-embedded two-port S-parameters of this device from 0.1 to 67 GHz. Using ADS, a small-signal equivalent circuit based on the hybrid-π model is simulated and fit to the experimental data. The dashed lines in fig. 4.23b are the ADS simulation results. The small-signal equivalent circuit model used in ADS simulation is shown in fig. 4.23c.

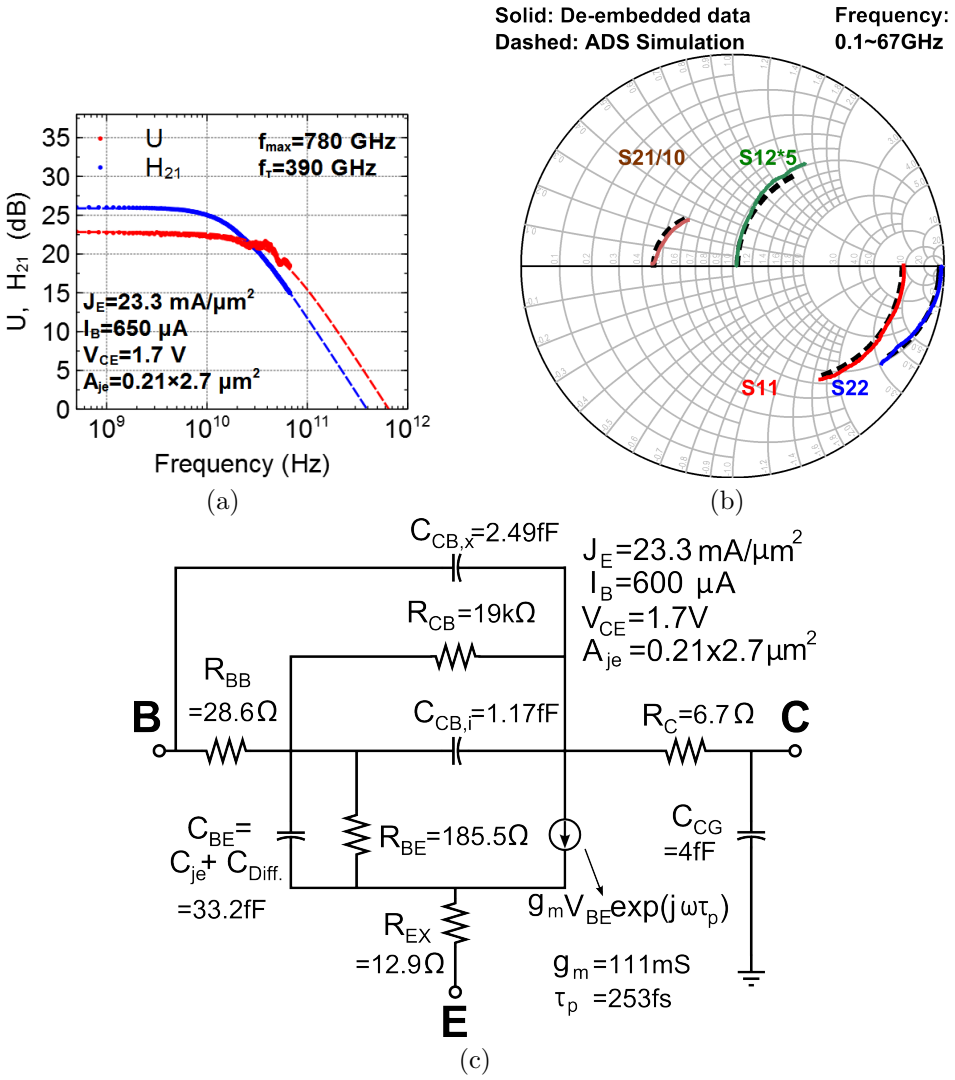
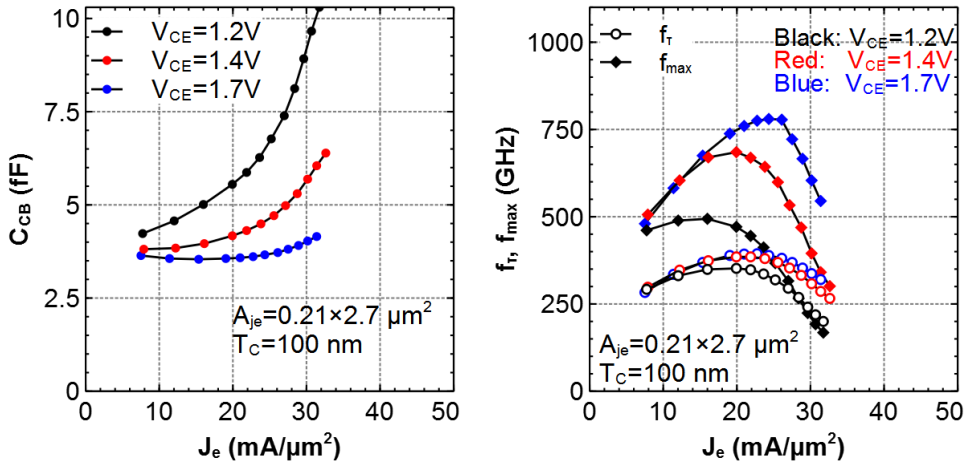


Figure 4.23: RF measurement results of a device on DHBT58H with $W_{\mathrm{E,design}}$ = 200 nm, $W_{\mathrm{BM,design}}$=700 nm, and $L_{\mathrm{E,design}}$=3 μm: (a) unilateral Mason's gain and H_{21} vs. frequency, (b) Two-port S-parameters vs. frequency, and (c) small-signal equivalent circuit. In (a) and (b), the solid lines represent the experimental data, and the dashed lines are the ADS simulation results.

Fig. 4.24a shows the extracted C_{CB} vs. J_{E} from the device with $W_{\mathrm{E,design}}$ =200 nm, $W_{\mathrm{BM,design}}$=700 nm, and $L_{\mathrm{E,design}}$=3 μm at V_{CE}=1.2, 1.4, and 1.7 V. For V_{CE}=1.7 V, V_{CB} ≈0.5 V, and the minimum of C_{CB} was observed at J_{E}=15.4 mA/μm^2,



(a) (b)

Figure 4.24: Current dependency of C_{CB} and cut-off frequencies extracted from the device on DHBT58H with $W_{E,design}$=200 nm, $W_{BM,design}$=700 nm, and $L_{E,design}$=3 μm at V_{CE}=1.2, 1.4, and 1.7 V.(a) C_{CB} vs. J_E. (b)f_τ and f_{max} vs. J_E

which is close to calculated Kirk effect limited current density (17 mA/μm^2).

The cut-off frequencies vs. current density is shown in fig. 4.24b. At V_{CE}=1.7 V, f_τ peaks at J_E ≈23 mA/μm^2. When V_{CE} increases, the current density limit ($J_{C,Kirk}$) becomes higher. Higher emitter current reduces r_e, and hence the emitter charging time decreases. Therefore, the peak f_τ and its corresponding J_E both increase as V_{CE} becomes higher. At V_{CE}=1.7 V, the maximum of f_{max} were also found at J_E ≈23 mA/μm^2 since C_{CB} rises slowly with J_E at the vicinity of the Kirk effect limit current density.

The RF performance of a device with $W_{E,design}$=100 nm, $W_{BM,design}$=600 nm, and $L_{E,design}$=3 μm is shown in fig. 4.25. From TEM analysis, the area of the base-emitter junction (A_{je}) is ∼ 0.11×2.7 μm, and the average width of the base contact on both sides of the emitter ($W_{B,Cont.}$) is ∼305 nm. Fig. 4.25a shows the unilateral Mason's gain (U) and current gain (H_{21}) vs. frequency at J_E=33.2 mA/μm^2,

I_B=600 μA, and V_{CE}=1.7 V. The device exhibits peak $f_\tau/f_{max} \approx 405/630$ GHz according to the single-pole fit (dashed lines). The Smith chart of the de-embedded two-port S-parameters of this device from 0.1 to 67 GHz is plotted in fig. 4.25b. The dashed lines in fig. 4.25b represent the S-parameters simulated by ADS using the small-signal hybrid-π equivalent circuit model shown in fig. 4.25c.

The extracted C_{CB} vs. J_E from the device with $W_{E,design}$=100 nm, $W_{BM,design}$ =600 nm, and $L_{E,design}$=3 μm at various V_{CB} is plotted in fig. 4.26a. At V_{CE}=1.7 V (V_{CB} $\approx$0.5 V), C_{CB} reaches minimum at J_E=30.1 mA/μm^2, which is 76% higher than the calculated value (17 mA/μm^2). The high emitter current density could be explained by the current spreading effect in the collector region. Because the width of the B-C mesa (740 nm) is far greater the width of the B-E junction (110 nm), $A_{jc} >> A_{jc}$, and more J_E is required for $J_C = J_{C,Kirk}$.

The cut-off frequencies vs. current density is shown in fig. 4.26b. The peak f_τ and its corresponding J_E both increase slightly as V_{CE} becomes higher. At V_{CE}=1.7 V, since C_{CB} nearly remains constant beteen 20 and 35 mA/μm^2, f_{max} is dominated by f_τ. The current density for peak f_τ (405 GHz) and peak f_{max} (630 GHz) coincide at 31.5 mA/μm^2.

The small-signal equivalent circuit models of the probed devices were computed and fitted to the RF measurement results biased at V_{CE}=1.7 V and J_E =25$\sim$30 mA/μm^2, the bias points for the peak RF performance. C_{CB} and R_{BB} have been analyzed in order to understand the causes of low cut-off frequencies.

C_{CB} vs. the designed base mesa width ($W_{BM,design}$) of devices with L_E=2.7 μm is plotted in Fig. 4.27a. The slopes of the curves, $C_{CB,WB}$,is 4.1 fF/μm, which indicates that $T_{C,eff}$ $\approx$76 nm instead of the design collector thickness (100 nm). The

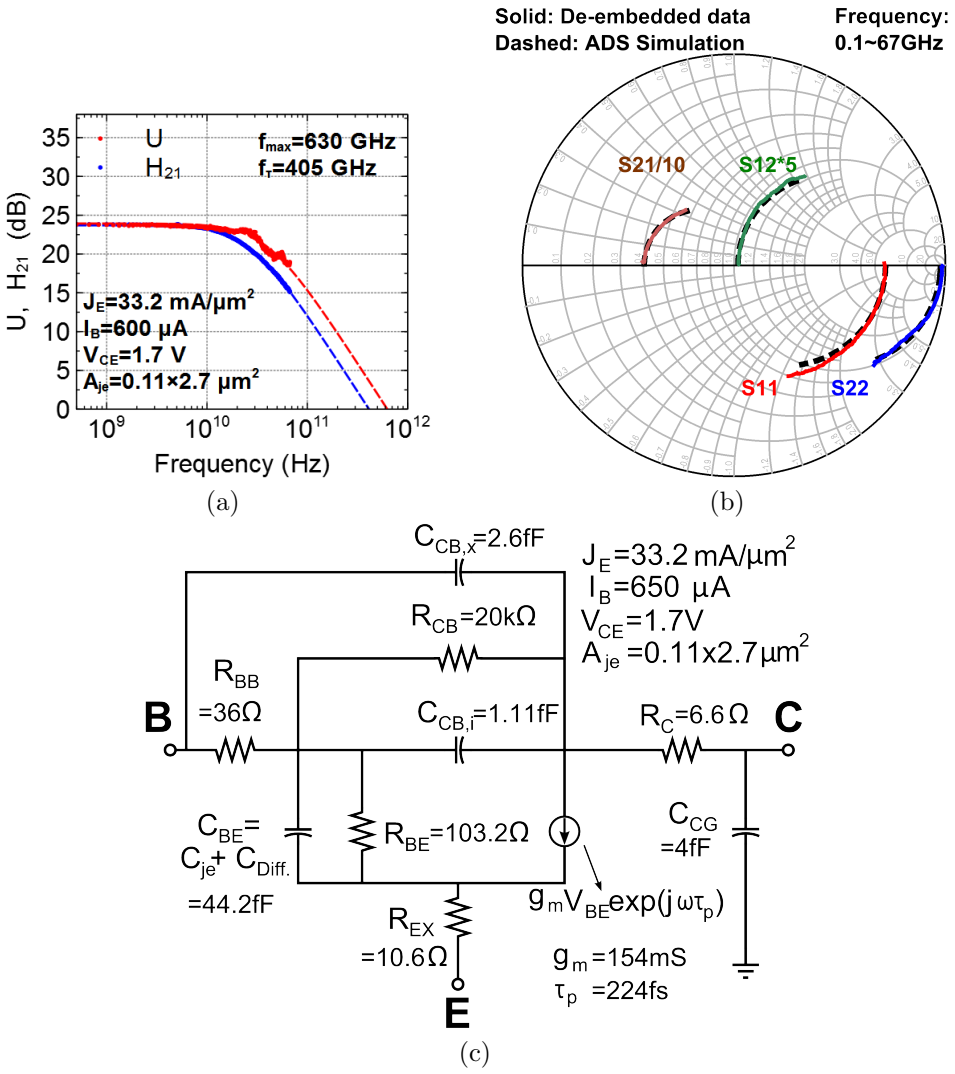


Figure 4.25: RF measurement results of a device on DHBT58H with $W_{\mathrm{E,design}} = 100\,\mathrm{nm}$, $W_{\mathrm{BM,design}}$=600 nm, and $L_{\mathrm{E,design}}$=3 μm: (a) unilateral Mason's gain and H_{21} vs. frequency, (b) Two-port S-parameters vs. frequency, and (c) small-signal equivalent circuit. In both (a) and (b), the solid lines represent the experimental data, and the dashed lines are the ADS simulation results.

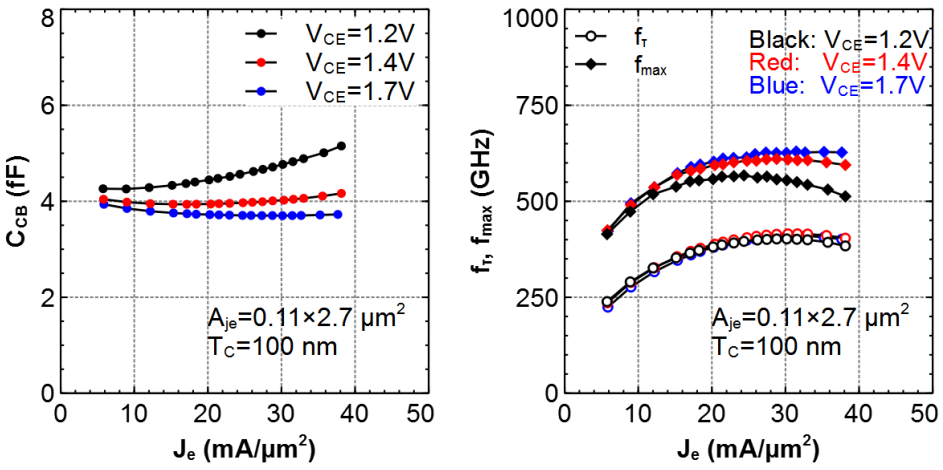
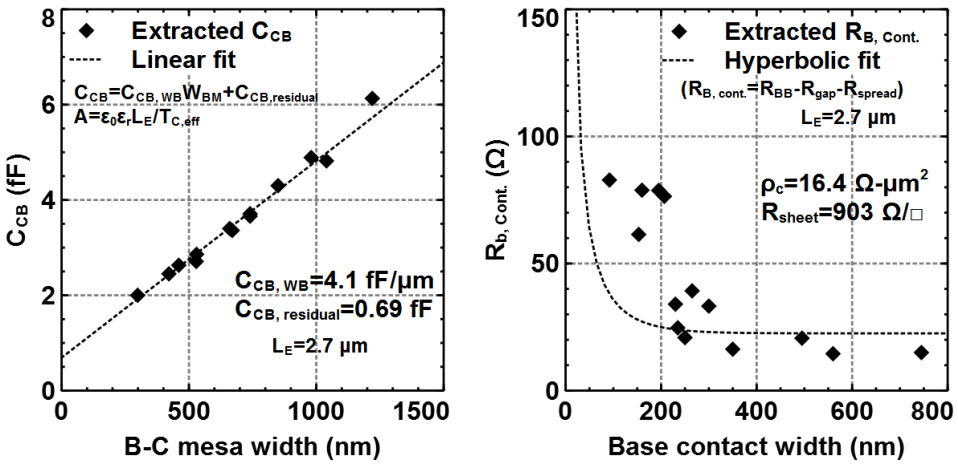


Figure 4.26: Current dependency of C_{CB} and cut-off frequencies extracted from the device on DHBT58H with $W_{\mathrm{E,design}}$=100 nm, $W_{\mathrm{BM,design}}$=600 nm, and $L_{\mathrm{E,design}}$=3 μm at V_{CB}=1.2, 1.4, and 1.7 V.(a) C_{CB} vs. J_{E}. (b)f_τ and f_{max} vs. J_{E}

intercepts of the curves, $C_{\mathrm{CB,residual}}$is 0.69 fF. From eq. 4.3, the excessive area beneath the base post (A_{BP}) is approximately 0.72 μm^2 for devices with L_{E}=2.7 μm and $W_{undercut}$=50 nm.

To estimate $R_{\mathrm{B,cont.}}$, the contribution of $R_{\mathrm{BE,spread}}$ and R_{gap} were calculated and then subtracted from R_{BB} extracted using the small-signal equivalent circuit model. The estimated $R_{\mathrm{B,cont.}}$ vs. $W_{\mathrm{B,cont.}}$ is plotted in fig. 4.27b. From TEM analysis, the base metal penetrated ~5 nm below the B-E junction. Based on the sheet resistance from the pinched base TLM (fig. 4.19a), $R_{\mathrm{sh,B}}$ ≈903 Ω/□ for metal penetration depth of 4 nm. By fitting $R_{\mathrm{B,cont.}}$ using this $R_{\mathrm{sh,B}}$ value, $\rho_{\mathrm{B,cont.}}$ of the devices can be obtained. For device with L_{E}=2.7 μm, $\rho_{\mathrm{B,cont.}}$=16.4 Omega − μm^2, which is higher than $\rho_{\mathrm{B,cont.}}$ obtained from base TLMs.

The power gain cut-off frequency (f_{max}) is governed by the RC delay of the B-C mesa. For a given L_{E}, C_{CB} reduces as the B-C mesa becomes narrower,



(a) (b)

Figure 4.27: Dimension dependence of (a) C_{CB} (vs. $W_{BM,design}$) and (b) $R_{B,cont.}$ (vs. $W_{B,cont.}$) from device on DHBT58H with L_E=2.7 μm biased at V_{CE}=1.7 V and J_E=25$\sim$30 mA/μm^2.

whereas R_{BB} decreases when the mesa width increases. Thus, the width of the base contact $W_{B,cont.}$ must be optimized according to the emitter width in order to achieve the highest possible f_{max}. Ideally, the optimal emitter/base contact width ratio is close to 1 if the parameters of devices follow the DHBT scaling rule in table. 2.1. However, since $W_{E,actual}$ was overestimated during fabrication, W_{BM} is too wide, causing high C_{CB} and low f_{max}. This also explains why the highest f_{max} is measured from a device with wide emitter and narrow B-C mesa, where $W_{E,actual}$=210 nm and $W_{B,Cont.}$=255 nm.

4.4 Summary

The DC and RF characteristics of DHBT63B and DHBT58H have been reported. At W=150 nm, the DC-β measured from DHBT63B and DHBT58H

are 16 and 18, respectively. On both samples, the current gain is limited by base current due to bulk recombination ($I_{\mathrm{B,bulk}}$) and edge conduction ($I_{\mathrm{B.edge}}$) [8, 9]. Detail analysis of the DC-β and and TCAD simulation will be addressed in the next chapter. For the RF performance, $f_{\max}$ measured from both sample are lower than 800 GHz. As discussed previously, $f_{\max}$ on DHBT63B and DHBT58H is limited by larger $R_{\mathrm{BB}}C_{\mathrm{CB}}$ delay in the B-C mesa. Despite the cut-off frequencies is lower than the reported value of $\sim$0.5/1.0 THz [10, 11], the analysis on RF results provided some useful insight on reducing $(RC)_{\mathrm{eff}}$ in DHBTs, in which $R_{\mathrm{B,cont.}}$ in a scaled device could deviate from the estimation from TLMs. Reducing the base specific contact resistivity will be the main limitation on the improvement of $f_\tau/f_{\max}$ in the future scaling generations DHBTs.

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Chapter 5

DC Current Gain of DHBTs: TCAD Simulation

As mentioned in chapter 2, the DC current gain (β) decreases as the DHBTs are scaled for higher cutoff frequencies. In order to increase DC-β in the future scaling generations of DHBTs, the carrier transport in the base of a DHBT must first be understood. Using a commercially available TCAD simulator (Synopsys ® Sentaurus), 2-D transport in the base region was simulated based on a drift-diffusion model. From the gradient of the carrier density, the magnitudes of current to each terminal of the DHBT were computed. DC-β was calculated from I_{B} and I_{C} obtained at V_{CB}=0 V and $J_{\mathrm{C}} \approx$25 mA/μm^2, which is close to the current density for peak f_τ and $f_{\max}$ for DHBTs with the 70 or 100 nm collector designs [1, 2].

Discussed in chapter 2 and 4, we have shown that the inverse DC-β can be written as

$$\begin{aligned} \frac{1}{\beta} &= \frac{1}{\beta_{\mathrm{bulk}}} + \frac{K_{\mathrm{B,edge.}} P_{\mathrm{je}}}{J_{\mathrm{C}} A_{\mathrm{je}}} \\ &\approx \frac{1}{\beta_{\mathrm{bulk}}} + \frac{K_{\mathrm{B,edge.}}}{2 J_{\mathrm{C}} W_{\mathrm{E}}}, \end{aligned} \tag{5.1}$$

where J_{C} here is the collector current density at the base side of the collector. Because most of the current spreading occurs in the bulk collector region, J_{C} is associated with A_{je}. The approximation holds when $L_{\mathrm{E}} \gg W_{\mathrm{E}}$. The current gain due to bulk recombination, β_{bulk}, is obtained from the reciprocal of the intercept. The total sheet edge current dentisy, $K_{B,edge}$, can be obtained from the product of J_{C} and the slope.

By comparing the DC-β obtained from TCAD simulation and experimental devices, the model has been verified and the magnitudes of various base current components were assessed. The model shows that the DC-β in scaled DHBTs is

governed by the base current due to Auger recombination and the lateral electron diffusion via the surface depletion region [3, 4].

In order to improve DC-β in the scaled devices, several new designs of B-E junction were constructed in Sentaurus. Based on the 2-D transport model, the DC-β in the designs were estimated. The simulation results indicate that DC-β could be enhanced to 50$\sim$100 if the process flow for the new designs can be integrated into the DHBT fabrication.

5.1 Simulation Setup

The structure of THz DHBT has been described in the previous chapters. To simulate the 2-D transport in the base of DHBTs, the coupled continuity, drift-diffusion, and Poisson's equations need to be self-consistently solved for the full DHBT structure by Sentaurus. Because of the complicated collector designs of the DHBTs, numerical solution to the coupled equations is computationally demanding. However, the intention of the simulation is to determine the transport in the base and estimate DC-/*beta* at J_C close to the bias condition for peak f_τ and f_{max}. At $J_C < J_{C,Kirk}$, i.e. before the base push-out occurs, the boundary condition of the coupled equations at the B-C junction depends only on the field in the setback region. The B-C grade and the InP collector designs have no effect on DC-/*beta* at such J_C. Thus, the DC-/*beta* of a DHBT and a single heterojunction bipolar transistor (SHBT), identical to the DHBT except without the complicated B-C grade and InP collector structures, are the same. Therefore,

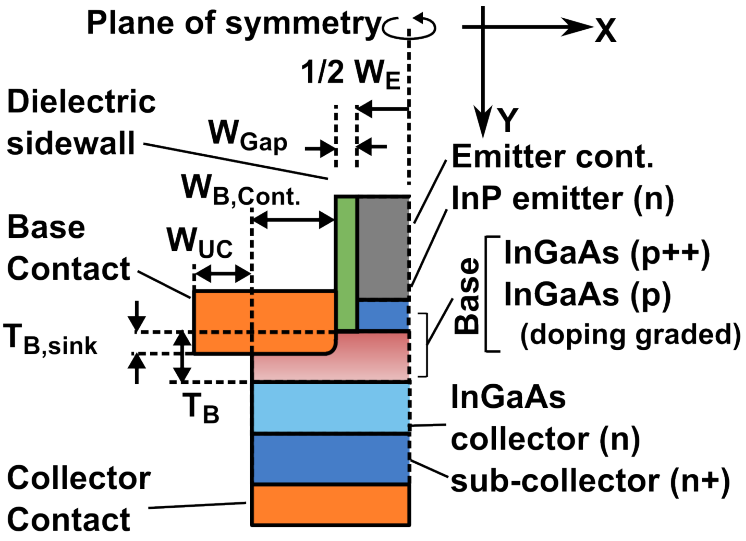


Figure 5.1: The cross-section of the SHBT structure simulated by Sentaurus.

SHBTs sturcutre were simulated by Sentaurus in order to construct a simplified and valid model for DC-β. Fig. 5.1 depicts the SHBT structure simulated by Sentaurus. The dimensions defined for the SHBTs are identical to that for the DHBTs in chapter 2. According to TEM analysis, $T_{b,sink}$ was assumed to be 5 nm for the simulation. For each design in epitaxy or geometry, devices with different $W_{\rm E}$ and $W_{\rm gap}$ have been simulated. $W_{\rm E}$=75, 100, 125, 150, 175, 200, 225, and 250 nm, whereas $W_{\rm gap}$=10, 15, 20, 25, and 30 nm. In addition to the 2×2-array of $W_{\rm E}$ and $W_{\rm gap}$, for every emitter width, SHBTs devices with the base metal widths ($W_{\rm B,cont.}+W_{\rm UC}$) of 1.2, 1.4, and 1.6$\times W_{\rm E}$ were simulated. As a result, a total of 120 variants of SHBTs were simulated for every design.

In order to construct a valid model for the carrier transport in the base region using Sentaurus, correct physical models for band structure, mobility, recombination coefficient, etc., must be incorporated. The parameters in these critical models are either obtained from literature, or estimated based on reported values.

The physical models used in this work will be described in the following sections.

5.1.1 Carrier Mobility and Velocity Saturation

As the doping concentration increases, the carrier mobility decreases due to the increased impurity scattering [5]. The doping-dependent carrier mobility is usually extrapolated in the using empirical expression based on the Caughey-Thomas model [6]

$$\mu(N) = \frac{\mu_{\max} - \mu_{\min}}{1 + (N/N_{\text{ref},\mu})^{\alpha}} + \mu_{\min} \ , \tag{5.2}$$

where N is the doping concentration and α is a fudging factor for the empirical formula. $N_{\text{ref},\mu}$ is a reference (low) doping concentration. Eq. 5.2, implies that $\mu_{\min}$ and $\mu_{\max}$ are the minimum and maximum mobilities at high and low doping concentrations, respectively. At very high doping concentration, where $N \gg N_{\text{ref},\mu}$, $\mu(N)$ reduces to $\mu_{\min}$. In our simulation, $N_{\text{ref},\mu}$ was set to the conduction-band effective density of states, N_{C}. The simulations assumed $\mu_{\min}$ and $\mu_{\max}$ of 1600 and $11600\,\text{cm}^2/\text{V}-\text{s}$ for electrons in p=InGaAs. For holes in p-InGaAs, the values were assumed to be 75 and $331\,\text{cm}^2/\text{V}-\text{s}$. The factor α for electrons and holes are 0.76 and 1.37, respectively [7, 8].

Velocity saturation occurs when the carriers are under either high electric fields or large diffusion gradients. In the composition- or doping-graded InGaAs base, the mobility of the injected electrons drops rapidly as the velocity saturation takes place [9]. The mobility under high field was modelled according to $v_{\text{drift}} =$

$\mu_{\text{highfield}}F$, where [10]

$$\mu_{\text{highfield}} = \frac{\mu_{\text{lowfield}}}{(1 + (\frac{\mu_{\text{lowfield}}F}{v_{\text{th}}})^{\gamma})^{1/\gamma}} \ , \tag{5.3}$$

where $F = q^{-1}\nabla E_{\text{fn}}$ is the driving force exerted upon the electrons due to the gradient in E_{fn}, the electron quasi-Fermi level. The electron threshold velocity, v_{th} was assumed to be $\sim 3 \times 10^7$ cm/s, and γ was set to 10 to ensure a rapid transition from low-field to high-field mobility, as is observed in the InGaAs material system [9].

5.1.2 Band Structure

It is imperative to have the correct conduction-band profile in order to simulate the electron transport in DHBTs. The current gain due to bulk recombination is determined by the electron lifetime and the base transit time, i.e. $\beta_{\text{bulk}} = \tau_{\text{n,total}}/\tau_{\text{B}}$, where $\tau_{\text{n,total}}$ and τ_{B} have been given in chapter 2 as [11]

$$\tau_{\text{B}} = \frac{T_{\text{B}}^2}{D_{\text{n}}}\frac{kT}{\Delta E_{\text{C}}}[1 - \frac{kT}{\Delta E_{\text{C}}}(1 - exp(-\frac{\Delta E_{\text{C}}}{kT})] + \frac{T_{\text{B}}}{v_{\text{exit}}}\frac{kT}{\Delta E_{\text{C}}}(1 - exp(\frac{\Delta E_{\text{C}}}{kT})), \tag{5.4}$$

and

$$\tau_{\text{n,total}} = (\frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{SRH}}} + \frac{1}{\tau_{\text{rad.}}})^{-1} \ . \tag{5.5}$$

Hence, β_{bulk} is affected by ΔE_{C}, the difference in the conduction-band energy between the top and the bottom the base. The value of ΔE_{C} is determined by the band gap energy (E_{g}), the magnitude of the band gap narrowing (BGN) effect [12],

as well as the effective density of states (N_C and N_V) of InGaAs. Most of the parameters can be found in an on-line database [13] or a semiconductor simulation handbook [14]. However, these values are usually obtained from a lattice matched or relaxed (low mechanical strain) semiconductors, which is not the case for the heavily doped p-InGaAs base. At high carbon doping concentration, the lattice constant of InGaAs changes due to the discrepancy in the atomic radii between As and C. In addition, the C source is CBr_4, and Br preferentially etch In during the MBE growth, changing the In/Ga ratio. As a result, the lattice contracts as doping concentration increases [15], causing strain in InGaAs. To minimize the lattice mismatch between InP and InGaAs, during the base growth of UCSB DHBT wafers, In/Ga ratio was adjusted in order to grow lattice-matched InGaAs doped at the median of the doping concentrations, e.g. $7\times10^{19}\,\mathrm{cm}^{-3}$ for the doping grade from 9 to $5\times10^{19}\,\mathrm{cm}^{-3}$. Even with this adjustment, the varying doping concentration still results in some extend of lattice mismatch so the InGaAs base of DHBTs is strained.

Therefore, the actual In/Ga ratio and strain in the InGaAs base is unknown, and determining the exact value of the band structure parameters would be difficult. This render the evaluation of ΔE_C very challenging. Instead of choosing the right parameters for the correct ΔE_C, different ΔE_C are generated by tuning the parameters. The simulated β_{bulk} and τ_B are then compared with the experimental result in order to determine the plausible conduction band profile. The E_g of InP and InGaAs were assumed to be 1.42 and 0.72 eV, respectively. For InP, $N_{C,InP}$ and $N_{V,InP}$ were set to be 5.66×10^{17} and $2.03\times10^{19}\,\mathrm{cm}^{-3}$, respectively. For InGaAs, $N_{C,InGaAs}$ and $N_{V,InGaAs}$ were assumed to be 2.54×10^{17} and $7.51\times10^{18}\,\mathrm{cm}^{-3}$. The

resulting ΔE_C various according to the base design, which will be discussed in the next section.

The built-in voltage (V_{bi}) of the B-E diode depends on the conduction band energy offset, $\Delta E_{C,offset}$, $G_{g,InGaAs}$, and E_{fp},the hole quasi Fermi level. In accurate parameters result in wrong V_{bi}, shifting the I-V curve in the Gummel plot horizontally. Similar to the estimation of ΔE_C, the uncertainty in the In/Ga ratio and lattice strain causes difficulty in determining the correct V_{bi}, and hence error in computing β as a function of V_{BE}. Therefore, β is evaluated as a function of J_C. The simulation and the experimental results are compared at the same J_C.

Experimentally, $\Delta E_{C,offset} = 0.3 \sim 0.4 \Delta E_{g,offset}$ for InGaAs/InP hetreojunction [16]. In our simulation, $\Delta E_{C,offset}$ is set to $\sim$0.28 eV. Sentaurus assumes a continuous vacuum level and computes the offset from the difference in electron affinities between InGaAs and InP, $\chi_{InGaAs} - \chi_{InP}$. The values reported in the literatures are χ_{InGaAs} $\approx$4.5 eV and χ_{InP} $\approx$4.4 eV [13]. To attain $\Delta E_{C,offset}$0.28 eV, a pseudo χ_{InGaAs} of 4.68 eV was used.

5.1.3 Carrier Recombination

Three recombination mechanisms in bulk InGaAs base were incorporated into the simulation for β: Auger, Shockley-Read-Hall (SRH), and radiative recombination. The total electron lifetime are obtained from eq. 5.5. Of the three mechanisms, Auger recombination is the governing process. Thus, accurate Auger coefficients, C_n and C_p is crucial to the simulation. From eq. 2.18, the Auger re-

combination rate can be written as

$$R_{\text{Auger}} = C_{\text{Auger,n}} n^2 p + C_{\text{Auger,p}} n p^2 \ . \tag{5.6}$$

As discussed in chapter 2, $C_{\text{Auger,n}}$ is associated with the CCCH process and $C_{\text{Auger,p}}$ is related to the CHHL and the CHHS proces [17, 18]. Most value reported in the literature are the combination of $C_{\text{Auger,n}}$ and $C_{\text{Auger,p}}$ since they were measured under ambipolar injection (such as laser diodes), where $n = p$. The reported $C_{\text{Auger,n}} + C_{\text{Auger,p}}$ scatters from 3.6 to $9\times10^{-29}\,\text{cm}^6/\text{s}$ [14, 19, 20]. In the heavily doped DHBT base, only the electron are injected, i.e. $p \gg n$, and CHHS/CHHL processes dominates. Therefore, knowing the value for $C_{\text{Auger,p}}$ is necessary. However, there are only few reports revealing the separated value so an adequate value of $C_{\text{Auger,p}}$ for the simulation is unknown. Similar to the solution to the problem in determining ΔE_{C}, $C_{\text{Auger,p}}$ were first assumed to be an arbitrary value and then tuned to fit τ_{Auger} and β_{bulk}. The $C_{\text{Auger,p}}$ value of $3.8\times10^{-29}\,\text{cm}^6/\text{s}$ was reported by [14] and used as a starting point for the simulations. Certain value of $C_{\text{Auger,n}}$ was also required by the simulation. Nevertheless, since the effect of the CCCH process can be neglected, we assumed $C_{\text{Auger,n}} = C_{\text{Auger,p}}$.

As described in chapter 2, the radiative recombination rate has a coefficient, $C_{\text{rad.}}$. The simulation assumed $C_{\text{rad.}} = 9.6 \times 10^{-11}\text{cm}^3/\text{s}$ in InGaAs [21]. As mentioned in chapter 2, the doping-dependent lifetime due to the SRH recombination is (eq. 2.21)

$$\tau_{\text{SRH}}(N_A + N_D) = \frac{\tau_{\text{ref}}}{1 + (\frac{N_A+N_D}{N_{\text{ref},\tau}})^{\kappa}}, \tag{5.7}$$

where the reference doping concentration, $N_{\mathrm{ref},\tau}$ is $1\times10^{19}\,\mathrm{cm}^{-3}$ for both holes and electrons. The simulation assumed the electron lifetime, $\tau_{\mathrm{ref,n}}$ =50/,ps, and the hole lifetime, $\tau_{\mathrm{ref,p}}$ =400/,ps. The factor κ was 0.73 for electrons and 1.2 for holes [7].

5.1.4 Surface Conduction and Recombination

At the p-InGaAs/dielectric interface on the extrinsic base region, the surface Fermi level is pinned by the trap states, inducing a surface depletion region. The electrons injected from the emitter could be trapped in the depletion region and leads to surface conduction or recombination. To emulate the surface depletion region, trap states were added to the interface between p-InGaAs and dielectric. The energy distribution of the state is assumed to be a Gaussian function centered at E_0=0.5 eV above the valence band edge [22], and with the standard deviation, E_{S}, of 0.1 eV. The density of the trap states, D_{it}, is usually obtained from C-V measurements at various frequencies. However, because the extrinsic base has witnessed most of the DHBT process flow starting from base metalization, the surface quality of p-InGaAs is unknown. The actual value of D_{it} on the extrinsic base would differ from the values obtained from the C-V measurements. Therefore, DC-β simulated at different values of D_{it} were computed. By fitting the simulation results to the experimental data, the correct D_{it} can be determined.

The surface recombination velocity, $v_{\mathrm{surf.rec.}}$, also depends on the InGaAs surface quality. For an InGaAs surface terminated by native oxide, values of $10^3 \sim 10^4\,\mathrm{cm/s}$ have been reported [23]. However, similar to D_{it}, it is difficult to

assess the accurate value of $v_{\text{surf.rec.}}$ on the extrinsic base surface. However, it has later been discovered from the simulation vs. experimental results (section 5.2) that even at high $v_{\text{surf.rec.}}$ (10^4 cm/s), the surface recombination current is negligible when comparing with lateral diffusion current. Thus, $v_{\text{surf.rec.}}$ were assumed to be 5000 cm/s.

The parameters for InGaAs assumed in the simulation and their references are listed in table. 5.1.

	Carrier Type		
Parameter	Electrons	Holes	unit
Carrier Mobility			
μ_{min} [7,8]	1600	75	$\text{cm}^2/\text{V}-\text{s}$
μ_{max} [7,8]	11600	331	$\text{cm}^2/\text{V}-\text{s}$
$N_{\text{ref},\mu}$ [7,8]	2.1×10^{17}	7.7×10^{18}	cm^{-3}
α [7,8]	0.76	1.37	
γ	10	10	
SRH Recombination			
τ_{ref} [7]	50	400	ps
$N_{\text{ref},\tau}$ [7]	1×10^{19}	1×10^{19}	cm^{-3}
κ [7]	0.73	1.2	
Auger Recombination			
C_{Auger} [14,19,20]	$2.5\sim4\times10^{-29}$	$2.5\sim4\times10^{-29}$	cm^6/s
Radiative Recombination			
$C_{\text{rad.}}$ [21]	9.6×10^{-11}		cm^3/s
Surface Recombination Velocity			
$v_{\text{surf.rec.}}$ [23]	5×10^3		cm/s

Table 5.1: $In_{0.53}Ga_{0.47}As$ parameter values used in simulation and corresponding references. The coefficients for Auger recombination are usually reported as a combined value.

5.2 Simulation and Experimental Results

As described in the previous section, the parameters regarding the band structure, Auger recombination coefficient, and the density of the interface trap states were unknown when constructing the trnaspot model in the DHBT base. In order to determine these parameters, DC-β was computed from several sets of simulation results assuming different parameter values. The calculated DC-β were then compared with the DC-β measured from the experimental device with the same B-E junction design. The experimental results from two DHBT samples with different base designs, DHBT63B and DHBT58H, were used to establish the model. The inverse DC-β vs. B-E junction periphery to area ratio ($P_{\mathrm{je}}/A_{\mathrm{je}}$) measured from two samples are shown in fig. 5.2.

5.2.1 Bulk Recombination and Lateral Diffusion Current

First, we would like to assess ΔE_{C}, and $C_{\mathrm{Auger,p}}$. The values of ΔE_{C} and $C_{\mathrm{Auger,p}}$ affect $\tau|_{\mathrm{B}}$ and $\tau_{\mathrm{n,total}}$, respectively. The ratio of $\tau_{\mathrm{n,total}}/$ to tau_{B} is the current gain due to the bulk recombination, β_{bulk}, which is the reciprocal of the y-axis intercepts in fig. 5.2. By fitting the computed β_{bulk} to the experimental β_{bulk}, is adequate ΔE_{C} and $C_{\mathrm{Auger,p}}$ are determined. In order to focus on ΔE_{C} and $C_{\mathrm{Auger,p}}$ only, the surface recombination and conduction were ignored, i.e. no surface depletion region and $v_{\mathrm{surf.rec.}}$ cm/s. This is done by removing the dielectric sidewall from the simulated structures.

The result from DHBT58H was analyzed first, which has the design of 20 nm

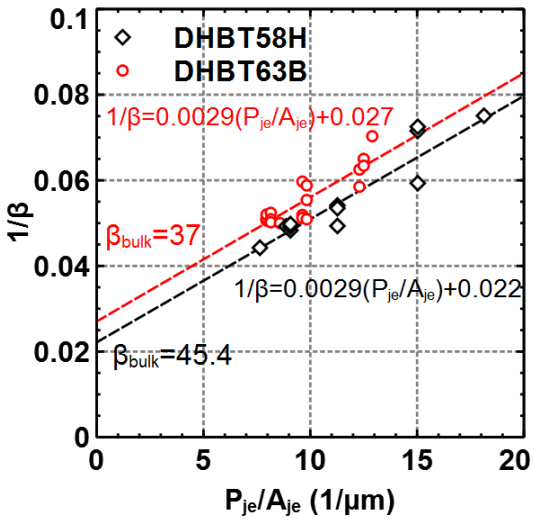


Figure 5.2: Inverse DC current gain ($1/\beta$) vs. HBT emitter periphery to area ratio ($P_{\rm je}/A_{\rm je}$) of DHBT58H and DHBT63B at $J_{\rm E} \approx 25{\rm mA}/\mu{\rm m}^2$. DHBT58H employs a 20 nm base with doping concentration of 12-8$\times10^{19}\,{\rm cm}^{-3}$ varying from the emitter side to the collector side. DHBT63B has a 25 nm base with lower doping concentration varying from 9 to $5\times10^{19}\,{\rm cm}^{-3}$. For both samples $W_{\rm gap}$) ≈10 nm according to TEM analysis.

base doping-graded from $1.2\times10^{20}\,{\rm cm}^{-3}$ at the emitter side to $8\times10^{19}\,{\rm cm}^{-3}$ at the collector side. Three magnitude of $\Delta E_{\rm C}$: 0, 26, and 54 meV were assumed. The value 54 meV was obtained from the conduction-band profile of the base ignoring the BGN effect, whereas the values of 0 and 26 meV were simulated under extreme and moderate BGN effects, respectively. With the three conduction-band profiles of the base, DC-β were computed assuming the literature value, $C_{\rm Auger,p} = 3.8 \times 10^{-29}\,{\rm cm}^6/{\rm s}$ [14].

However, the $\beta_{\rm bulk}$ estimated from all three simulation sets were lower than the experimental value of 45.4, indicating that either $tau_{\rm B}$ was overestimated or $tau_{\rm n,total}$ is underestimated. Since a shorter $tau_{\rm B}$ would require a higher $\Delta E_{\rm C}$, which is unlikely to be generated from the designed doping-grade, we deduced

that actual $tau_{\mathrm{n,total}}$ should be higher. In order to increase $\tau_{n,total}$, the assumed $C_{\mathrm{Auger,p}}$ needed to be reduced. The subsequent attempts assumed the same band profiles and $C_{\mathrm{Auger,p}} = 2.5 \times 10^{-29}\,\mathrm{cm}^6/\mathrm{s}$. The computation results are plotted in fig. 5.3 [3]. The $\beta_b ulk$ simulated at ΔE_{C}=0, 26, and 54 meV are 27.3, 36, and 43, respectively. The results from $C_{\mathrm{Auger,p}} = 2.5 \times 10^{-29}\,\mathrm{cm}^6/\mathrm{s}$ and ΔE_{C}=54 meV agrees with the experimental value of 45.4. It should be noted that with a even lower $C_{\mathrm{Auger,p}}$, the β_{bulk} simulated with lower ΔE_{C} (considering the BGN effect) would also fit the experimental β_{bulk}. However, simulations assuming such $C_{\mathrm{Auger,p}}$ which greatly deviates from the reported value could be invalid. Hence, we refrained from further decreasing $C_{\mathrm{Auger,p}}$, and assumed $C_{\mathrm{Auger,p}} = 2.5 \times 10^{-29}\,\mathrm{cm}^6/\mathrm{s}$ and no BGN effect.

As shown in fig. 5.3c, only the intercept, i.e. β_{bulk}, matches the experimental result. The slope of the computed and experimental $1/\beta$ are not consistent because the the lateral carrier diffusion ($I_{\mathrm{B,diff.}}$) was the only edge current component considered in the simulations and the effect of surface recombination ($I_{\mathrm{B,surf.rec.}}$) and conduction ($I_{\mathrm{B,surf.rec.}}$) was neglected. In other words, the slope of the computed current gain is solely due to $I_{\mathrm{B,diff.}}$. According to fig. 5.3c, the slopes of the simulation results corresponding to W_{gap}=10 and 30 nm indicate $K_{\mathrm{B,edge}}$=23.6 and 4.7 μA/μm, respectively. In the simulations, $K_{\mathrm{B,edge}}$ is essentially $K_{\mathrm{B,diff.}}$, which means the lateral diffusion current via the bulk base current increases 5 times when W_{gap} is scaled from 30 to 10 nm.

The experimental $K_{\mathrm{B,edge}}$ of DHBT58H is $sim72\,\mu\mathrm{A}/\mu\mathrm{m}$ at $J_{\mathrm{C}} \approx J_{\mathrm{E}}$ =25 mA/μm^2. From TEM analysis, W_{gap} ≈10 nm in experimental devices. Therefore, assuming the simulation result with W_{gap}=10 nm is a valid model for the

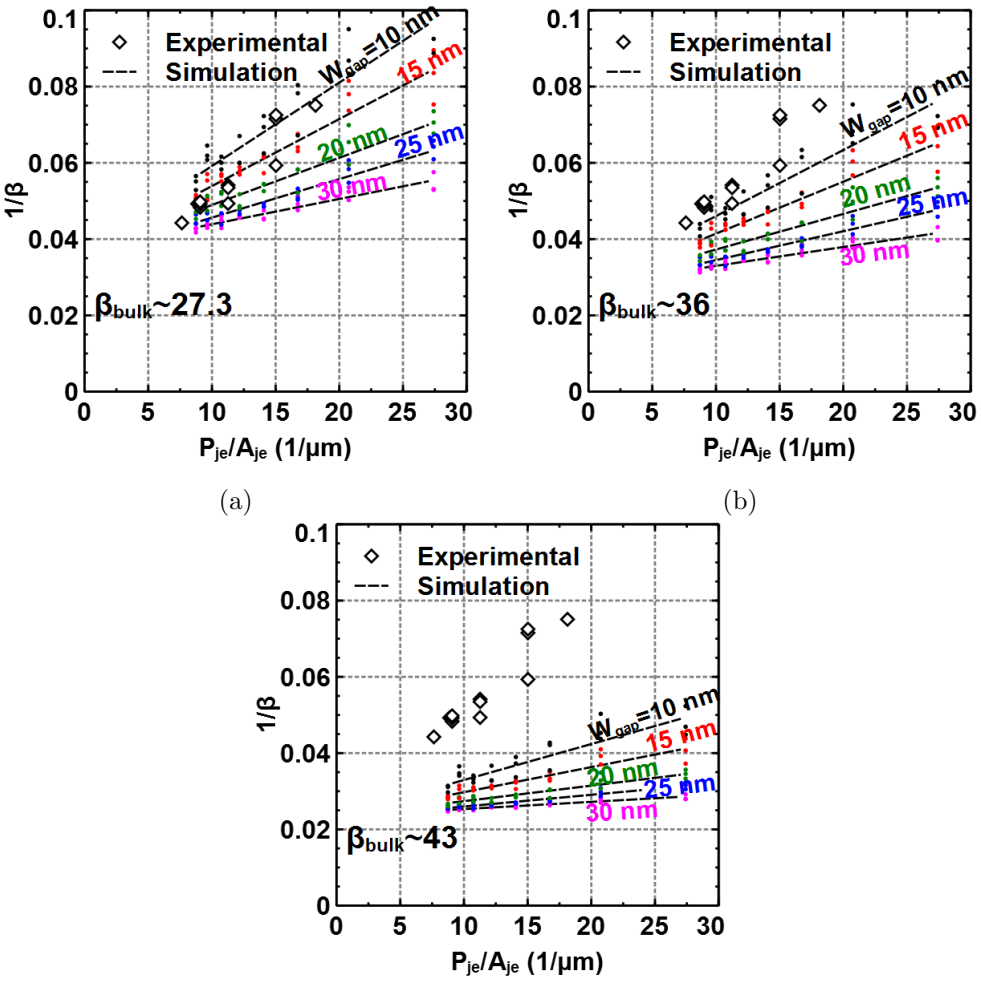


Figure 5.3: Experimental and computed inverse DC current gain ($1/\beta$) vs. HBT emitter periphery to area ratio ($P_{\rm je}/A_{\rm je}$) of DHBT58H at $J_{\rm E} \approx 25{\rm mA}/\mu{\rm m}^2$. The simulation assumed $\Delta E_{\rm C}$ of (a) 0 (b) 26, and (c) 54 meV.

transport in the bulk base region, $K_{\mathrm{B,diff.}}$ is approximately 33% of the total edge current in DHBTs. For an experimental device with W_{E}=100 nm, DC-β ≈13. For such device, the simulated β_{bulk} and $K_{\mathrm{B,diff.}}$ implies that $I_{\mathrm{B,bulk}}$ and $I_{\mathrm{B,diff.}}$ account for 30 and 24% (two sides of B-E junction considered) of the total base current, respectively.

5.2.2 Surface Recombination and Conduction Current

With adequate values of ΔE_{C} and $C_{\mathrm{Auger,p}}$ known, we would like to estimate $v_{\mathrm{surf.rec.}}$ and D_{it} on the extrinsic base surface. The value of D_{it} affects the magnitude of surface depletion and $v_{\mathrm{surf.rec.}}$, and hence governs both $I_{\mathrm{B,surf.rec.}}$ and $I_{\mathrm{B,surf.cond.}}$. To simulate transport with the presence of a surface depletion region, the dielectric sidewall was added back into the simulation structure, and donor-like trap states were introduced at the InGaAs/dielectric interface. The energy distribution of the states were assumed to be a Gaussian as described in section 5.1.4. The trap states density can be written as a function of energy,

$$D(E) = D_{\mathrm{it}} exp(-\frac{(E-E_0)^2}{2E_{\mathrm{s}}^2}) \ , \tag{5.8}$$

where E is the energy with respect to the valence band, i.e. $E = 0$ at the valence-band edge. E_0 and E_{S} were assumed to be 0.5 and 0.1 eV, respectively. In other words, $D(E)$ is a Gaussian function with a peak value of D_{it} at 0.5 eV above the valence band edge [22] with a standard deviation of 0.1 eV. E_{S} was chosen arbitrarily to be 0.1 eV to ensure most of the trap states are within ±0.1 eV from E_0.

Since the value of $D_{\rm it}$ is unknown, arbitrary numbers had to be assumed at first, and then the computed current gains were compared with the experimental values. To focus on $D_{\rm it}$ only, $v_{\rm surf.rec.}$ was assumed to be 5000 cm/s and independent of $D_{\rm it}$. We later discovered that $I_{\rm B,surf.rec.}$ is smaller then $I_{\rm B,surf.cond.}$ by few orders. Thus, assessing the correct value of $v_{\rm surf.rec.}$ is not as critical as that of $D_{\rm it}$. We will address this shortly in the remainder of this section.

Once again the structure of DHBT58H was used in the simulations. The simulations assumed $\Delta E_{\rm C}$=54m meV and $C_{\rm Auger,p} = 2.5 \times 10^{-29}\,{\rm cm}^6/{\rm s}$ according to result reported in the previous section. DC-β were computed assuming different $D_{\rm it}$ of 5×10^{12}, 10^{13}, and $5\times10^{13}\,{\rm cm}^{-2}{\rm eV}^{-1}$. The simulation result shown in fig. 5.3c was used as a control neglecting both $D_{\rm it}$ and $v_{\rm surf.rec.}$. Each simulation result was then compared with the DC-β obtained experimentally to determine the correct $D_{\rm it}$. The results are depicted in fig. 5.4 [4]. From $J_{\rm C}$ ($\sim$ 25mA/μm^2) and the slope of $1/\beta$ vs.$P_{\rm je}/A_{\rm je}$ at $W_{\rm gap}$=10 nm, $K_{\rm B,edge}$=39, 42, and 59 $rm\mu A/\mu m$ when assuming $D_{\rm it}$=5×10^{12}, 10^{13}, and $5\times10^{13}\,{\rm cm}^{-2}{\rm eV}^{-1}$, respectively. Among these three sets of simulations, the one assuming $D_{\rm it}$=$5\times10^{13}\,{\rm cm}^{-2}{\rm eV}^{-1}$ showed the result closest to the experimental data.

Simulations assuming a higher $D_{\rm it}$ would give a $K_{\rm B,edge}$ that matches the experimental value, 72 μA/μm. Although the $D_{\rm it}$ at the Al_2O_3/InGaAs interface in the extrinsic base of DHBT58H is expected to be high because no surface treatment was performed before ALD, the $D_{\rm it}$ of $5\times10^{13}\,{\rm cm}^{-2}{\rm eV}^{-1}$ is already more than an order higher than the value reported for the Al_2O_3/InGaAs interface with surface treatment prior to ALD [24, 25]. Therefore, assuming higher values of $D_{\rm it}$ could be invalid and misleading.

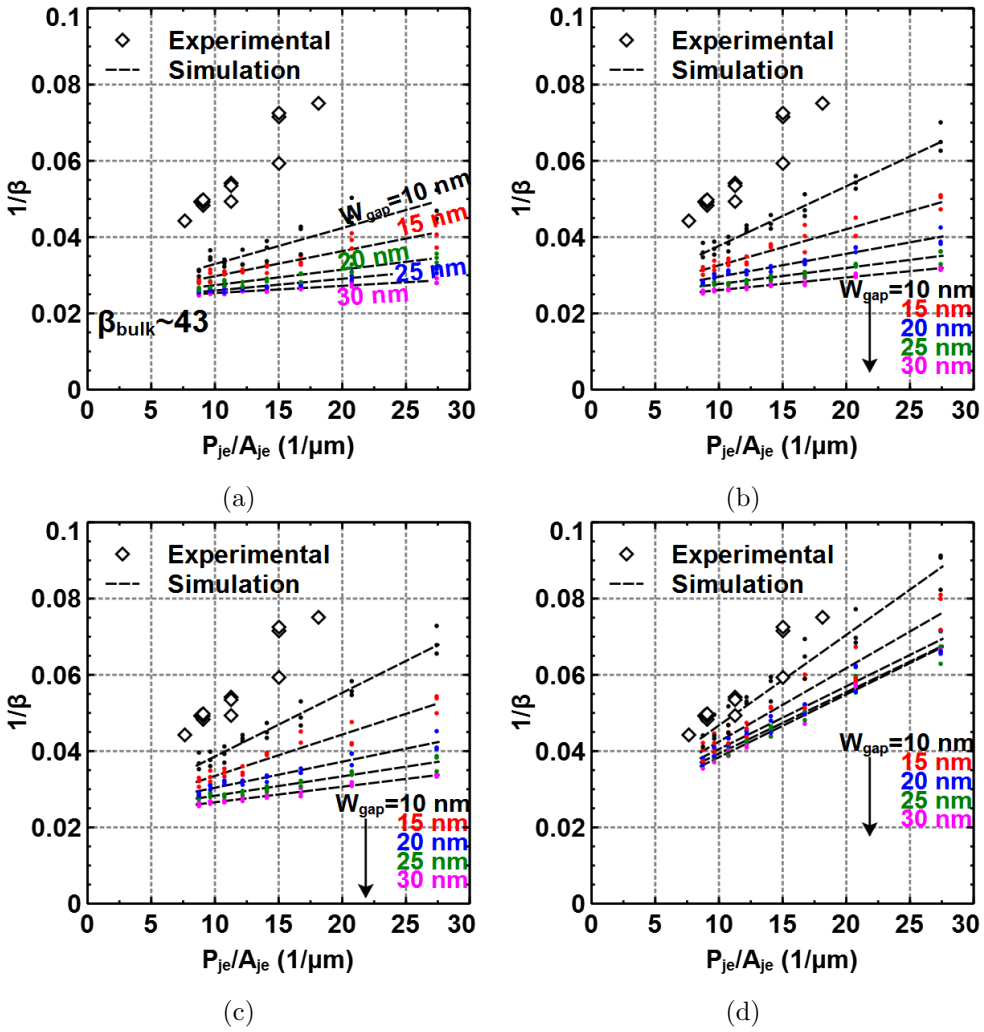


Figure 5.4: Experimental and computed inverse DC current gain ($1/\beta$) vs. $P_{\rm je}/A_{\rm je}$ of DHBT58H at $J_{\rm E} \approx 25{\rm mA}/\mu{\rm m}^2$. In (a), the simulation assumed zero $D_{\rm it}$ and $v_{\rm surf.rec.}$. In the rest of the figures, The simulation assumed $v_{\rm surf.rec.}$=5000 cm/s and $D_{\rm it}$ of (b) 5×10^{12}, (c) 1×10^{13}, and (d) $5\times10^{13}\,{\rm cm}^{-2}{\rm eV}^{-1}$.

Moreover, the emulation of the surface depletion region might not be entirely accurate since it used a classical model to describe the trapped electrons. In the classic model, the trapped electrons has a continuous energy distribution, and cannot escape from the depletion region once trapped. In a more accurate Quantum Mechanic model, the electrons are trapped in discrete bound states in the triangular quantum well (QW) near the interface induced by the surface Fermi level pinning. The electrons could either travel laterally in the QW like in the classic model, or tunnel through the QW barrier and return to the bulk base region again. Thus, the electron population in the triangular QW and a finite trapping time should be incorporated into the simulation. Simulations involving the aforementioned Quantum Mechanic model requires a demanding computational effort. Nonetheless, the goal of this work is to construct a simple model/tool to estimate DC-β in DHBTs, and then use the model as a quick-test platform to help designing B-E junction for improved β. Because of this intention, the Quantum Mechanic model is not considered in this work. Hence, a perfect match between the simulated vs. experimental surface recombination and conduction current should not be expected

The current components due to surface recombination and conduction, $K_{\mathrm{B,surf.rec.}}$ and $K_{\mathrm{B,surf.cond.}}$, can be estimated from the difference between $K_{\mathrm{B,edge}}$ obtain from simulations with and without the surface depletion region. The simulation result with W_{gap}=10 nm and D_{it}=$5\times10^{13}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ indicates $K_{\mathrm{B,surf.rec.}}$ + $K_{\mathrm{B,surf.cond.}}$ is $35.4\,rm\mu A/\mu m$, which accounts for ∼50% of the total $K_{\mathrm{B,edge}}$ of 72 μA/μm measured from DHBT58H. $K_{\mathrm{B,edge}}$ of 59 μA/μm also implies that the total edge current contributes ∼61% (two sides of B-E junction considered) of the total base

current in an experimental device with W_{E}=100 nm and W_{gap}=10 nm.

Next, we would like to determine the magnitudes of $K_{\mathrm{B,surf.rec.}}$ and $K_{\mathrm{B,surf.cond.}}$ separately. From chapter 2. the surface recombination rate can be written as

$$R_{\mathrm{surf.SRH}} = n_{\mathrm{s}}(x) v_{surf.rec.} \ , \tag{5.9}$$

where $n_{\mathrm{s}}(x)$ is the density of the electrons trapped at the vicinity of the InGaAs/dielectric interface. Fig. 5.5 is the electron density near the InGaAs/dielectric interface as a function of the depth in to the base. $n_{\mathrm{s}}(x)$ was defined as the average electron density within an arbitrary distance, T_{s}. By integrating $n_{\mathrm{s}}(x) v_{surf.rec.}$ over the extrinsic base, the edge sheet current density due to surface recombination could be calculated, i.e.

$$K_{\mathrm{B,surf.rec.}} = \int_{W_{\mathrm{E}}}^{W_{\mathrm{E}}+W_{\mathrm{gap}}} n_{\mathrm{s}}(x) v_{surf.rec.} dx \ . \tag{5.10}$$

Assuming $v_{\mathrm{surf.rec.}}$=5000 cm/s, the estimated $K_{\mathrm{B,surf.rec.}}$ is less than 1 μA/μm for device with W_{gap}=10 to 30 nm. The magnitude approximately doubles if $v_{\mathrm{surf.rec.}}$= 5000 cm/s is assumed. This implies that $K_{\mathrm{B,surf.rec.}}$ is negligible with respect to $K_{\mathrm{B,surf.cond.}}$ so almost the entirety of edge current originates from lateral diffusion via bulk ($I_{\mathrm{B,diff.}}$) and surface depletion region $I_{\mathrm{B,surf.cond.}}$.

5.2.3 Model Verification

The transport model has been constructed for DHBT. In order to verify the model, the experimental result of DHBT63B, which has a 25 nm base doping-

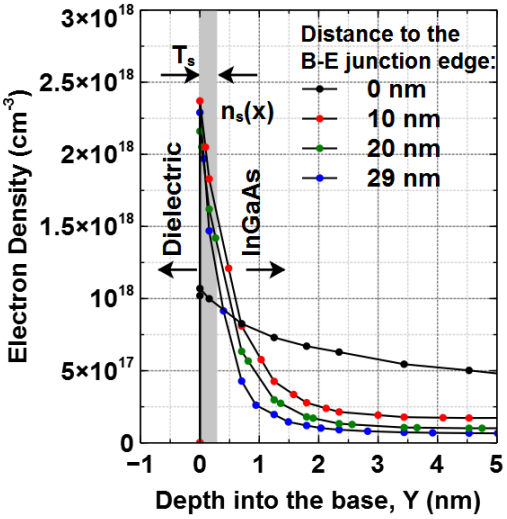


Figure 5.5: The computed electron density near the dielectric/InGaAs interface vs. the depth into the base, at different distance to the edge of the B-E junction. The simulation is base on the base design of DHBT58H with W_{gap}=30 nm and assumed D_{it}=5×10^{13} cm^{-2}eV^{-1}.

graded from 9 to 5×10^{19} cm^{-3}. Unlike DHBT58H, DHBT63B does not have composite Al_2O_3/SiN_x sidewall. The simulation for DHBT63B retained the assumption used in the simulations for DHBT58H: the BGN effect has been neglected, $C_{\text{Auger,p}}$=2.5×10^{-29} cm^6/s, D_{it}=5×10^{13} cm^{-2}eV^{-1}, and $v_{surf.rec.}$ =5000 cm/s. The computed β gave a matching $K_{\text{B,edge}}$, but the calculated β_{bulk} is higher than the experimental value of 37, indicating that the electron lifetime was too long. Therefore, $C_{\text{Auger,p}}$ was increased back to the literature value of 4×10^{-29} cm^6/s. Fig. 5.6 is the experimental and simulated $1/\beta$ vs. $P_{\text{je}}/A_{\text{je}}$, showing a consistent simulation and experimental results for W_{gap}=10 nm. Nonetheless, the reason for the discrepancy between $C_{\text{Auger,p}}$ of DHBT58H and DHBT63B remains unknown. It is possible that the simulation ignored other recombination mechanisms occurring in the base.

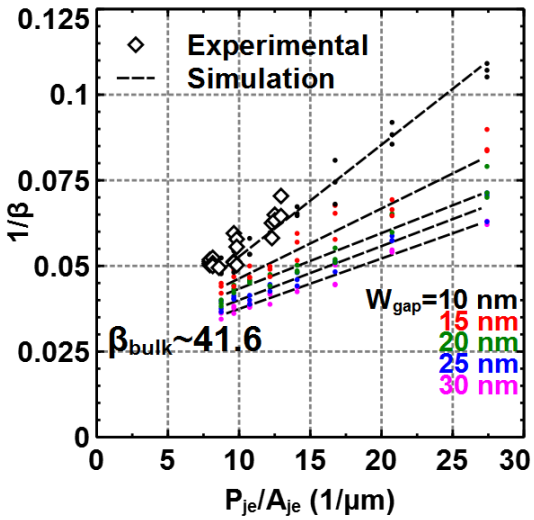


Figure 5.6: Experimental and computed inverse DC current gain ($1/\beta$) vs. $P_{\rm je}/A_{\rm je}$ of DHBT63B design at $J_{\rm E} \approx 25{\rm mA}/\mu{\rm m}^2$. The simulation assumed $v_{\rm surf.rec.}$=5000 cm/s, $D_{\rm it}$=$5\times10^{13}\,{\rm cm}^{-2}{\rm eV}^{-1}$, $C_{\rm Auger,p} = 4\times10^{-29}\,{\rm cm}^6/{\rm s}$, and ignored the BGN effect.

Whether with or without the Al_2O_3/SiN_x sidewall, the simulation results of DHBT58H and DHBT63B both indicate high $D_{\rm it}$ on the p-InGaAs surface. This implies that Al_2O_3 on the extrinsic base of DHBT58H has not adequately passivated/terminated the InGaAs surface, causing similar amount of surface trap states. In order to suppress the surface conduction current, $D_{\rm it}$ must be lowered. Low $D_{\rm it}$ at the interface between ALD dielectric and InGaAs has been achieved for III-V MOSFET application [24, 25]. This often involves a surface treatment techniques prior to ALD and/or an annealing after ALD. However, the hydrogen-trimethylaluminium (TMA) cycles reported in [25] is incompatible with DHBT process since the hydrogen plasma will react with the carbon dopants, reducing the doping concentration in p-InGaAs. On the other hand, the nitrogen-TMA cycles in [24] has the potential to be incorporated into the DHBT process flow

and reduces D_{it}. Because the edge current will be more dominant as W_{E} scales, attaining low D_{it} on the InGaAs surface will be more critical to improving DC-β in the future scaling generations of DHBTs.

5.3 Novel Base-Emitter Junction Designs

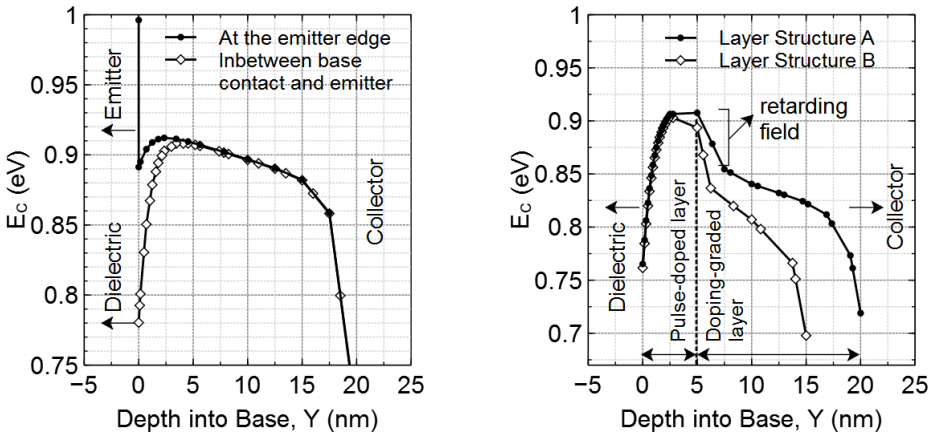
With the adequate surface pretreatments and ALD passivation, D_{it} could be reduced, decreasing $I_{\mathrm{B,surf.rec.}}$ and $I_{\mathrm{B,surf.cond.}}$. However, the base current components via the bulk region, $I_{\mathrm{B,diff.}}$ and $I_{\mathrm{B,bulk}}$, do not depend on the surface properties, and hence remain unaffected. As shown in fig. 5.4a, even in the absence of surface Fermi level pinning and surface recombination, the DC-β eventually drops to 20 at W_{E}=75 nm. Therefore, in addition to lowering D_{it}, modifications to the B-E junction should be made if decent DC-β is expected in the future scaling generations of DHBTs.

In this section, three potential designs for improving DC-β will be proposed and investigated. Before fabricating DHBTs with the new features in these designs, these new designs should be carefully evaluated. Using the TCAD model constructed and verified previously, DC-β of devices with the designed structures or geometries was computed. The simulation results from the three designs were compared. Their correspond improvement in β and the challenge in integrating these designs will be discussed at the end of this section.

5.3.1 Epitaxy Design: Graded Base with a Pulse-doped Layer

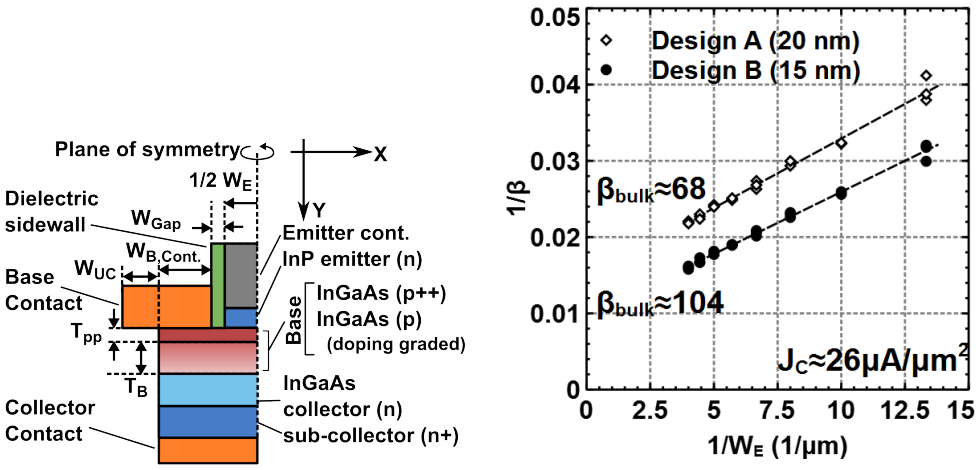
The simulation result of DHBT58H indicates that ∼24% of the total base current is contributed by the current due to lateral electron diffusion via the bulk base region, $I_{\mathrm{B,diff.}}$, at W_{E}=100 nm. Because $I_{\mathrm{B,diff.}}$ remain approximately the same as W_{E} scales for a given W_{gap}, the contribution of the lateral diffusion to the base current will increase in the future scaling generations of DHBTs. Thus, it is crucial to prevent the electrons from reaching the base contact as they diffuse laterally. By an insertion of a layer of heavily doped (pulse-doped) p-InGaAs between the base and emitter semiconductors, a retarding field which blocks the electron from diffusing backward is induced by the abrupt change in the doping concentration. Fig. 5.7 compares the conduction-band profiles vs. depth into the base at the extrinsic base of a conventional graded base design against base designs of a pulse-doped layer followed by graded region. As can be seen, a ∼0.5 eV barrier is generated in both designs employing the pulse-doped layer, preventing the electron from traversing towards the base contact. Moreover, since the specific contact resistivity reduces exponentially as the doping concentration increases [26], the base contact resistance decreases when utilizing the heavily doped layer as the contact layer, improving f_{max} simultaneously.

Two base designs with different doping-graded region are proposed. Both designs employs a 5 nm InGaAs doped at $1.2\times10^{20}\,\mathrm{cm}^{-3}$ as the pulse-doped layer. Beneath the pulse-doped layer, layer structure A has a 15 nm InGaAs graded from 7 to 4 $\times10^{19}\,\mathrm{cm}^{-3}$, whereas layer structure B has a 10 nm InGaAs graded from 5 to 3 $\times10^{19}\,\mathrm{cm}^{-3}$. Fig. 5.8a is the cross-section of the simulated SHBTs. The DC-β



(a) (b)

Figure 5.7: The conduction-band energy vs. the depth into the base at the extrinsic base of (a) a 20 nm base doping-graded from 12 to 8 $\times 10^{19}\,\mathrm{cm}^{-3}$, and (b) designs with a 5 nm pulse-doped ($1.2\times 10^{20}\,\mathrm{cm}^{-3}$) layer followed by a doping-graded base. Layer structure A has a 15 nm InGaAs graded from 7 to 4 $\times 10^{19}\,\mathrm{cm}^{-3}$. Layer structure B has a 10 nm InGaAs graded from 5 to 3 $\times 10^{19}\,\mathrm{cm}^{-3}$.



(a) (b)

Figure 5.8: (a) The Schematic of the simulated SHBTs with a pulse-doped layer. (b) Computed $1/\beta$ vs. $P_{\mathrm{je}}/A_{\mathrm{je}}$ of the designs at $J_{\mathrm{E}} \approx 26\,\mathrm{mA}/\mu\mathrm{m}^2$. The simulation retained the parameters ($v_{\mathrm{surf.rec.}}$, D_{it}, $C_{\mathrm{Auger,p}}$, etc.) of DHBT58H and assumed W_{gap}=10 nm.

of the devices with W_{gap}=10 nm was computed at $J_E \approx$26 mA/μm^2 assuming the same parameters for DHBT58H. The simulation results are shown in fig. 5.8b. For a device with W_E=100 nm and layer structure A, β=31 and $K_{B,edge.}$=23.6 μA/μm, which contributes ~28% of the total base current. For the same device with layer structure B, β=39 and $K_{B,edge.}$=21.2 μA/μm, indicating that approximately 32% of the total base current is due to the edge current. The edge current components due to $I_{B,surf.rec.}$ and $I_{B,surf.cond.}$ in both design are assumed to be similar to that in DHBT58H because they all share the same extrinsic base surface (doped at 1.2×10^{20} cm^{-3}). Therefore, the reduction in the edge current (61 to 28%) is mainly attributed to the suppression of $I_{B,diff.}$, indicating that the retarding field induced by the pulse-doped layer is effective. Because there are more electrons traversing towards the collector, the bulk current gain, β_{bulk}, has also been improved.

5.3.2 Supplement Process Flow: Trench in Extrinsic Base

Although the retarding field shown in fig. 5.7b has been proven effective in blocking the lateral diffusion current. The injected electrons in the pulse-doped layer (the top 5 nm) are not affected by this barrier, and may continue to diffuse laterally and eventually reach the base contact undeterred. In order to further suppress the later diffusion, the pulse-doped layer in the extrinsic base can be removed, forming a trench, and hence the retarding field is effective to all electrons in the bulk base region since they must first traverse into the graded region. The cross-section of the structure is shown in fig. 5.9a. This structure can be

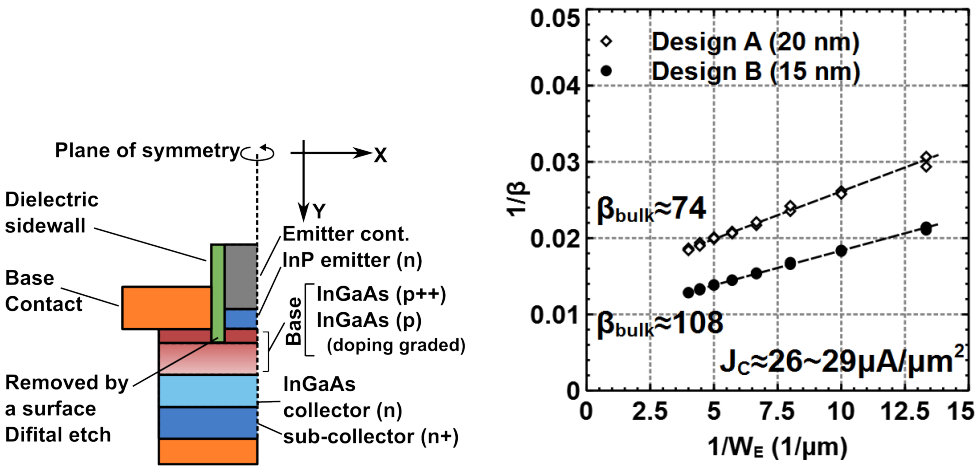


Figure 5.9: (a) The Schematic of the simulated SHBTs with the pulse-doped layer removed from the extrinsic base region. (b) Computed $1/\beta$ vs. $P_{\rm je}/A_{\rm je}$ of the designs at $J_{\rm E} \approx 26 \sim 29\,{\rm mA}/\mu{\rm m}^2$. The simulation retained the parameters ($v_{\rm surf.rec.}$, $D_{\rm it}$, $C_{\rm Auger,p}$, etc.) of DHBT58H and assumed $W_{\rm gap}$=10 nm.

achieved by partially removing the pulse-doped layer using a self-limiting digital etch process [27] after the base metalization.

The layer structures A and B are again studied to evaluate this approach. The computed β of devices with $W_{\rm gap}$=10 nm is shown in fig. 5.9b. $K_{\rm B,edge.}$ of layer structures A and B are 18.2 and 11.8 μA/μm, respectively. For a device with $W_{\rm E}$=100 nm, this means approximately 25% of the total base current is from the edge for both layer structures, and therefore indicates that the lateral diffusion has been further suppressed. Since the structure of the base beneath the B-E junction (active base region) remains the same as that in the pulse-doped design, $\beta_{\rm bulk}$ only increases slightly due to the suppression of $I_{\rm B,diff.}$.

The cyclic process flow for digital etch usually involves semiconductor oxidation followed by wet etch. For InGaAs, the oxidation is done by UV-ozone exposure, and the oxide can be removed by diluted BHF or HCl. The simplic-

ity of the digital etch process makes it fairly compatible with the current DHBT process flow. However, with the heavily doped region removed from the extrinsic base, the disadvantage of this approach is the increased sheet resistance and R_{gap}, which reduces f_{max}. Also, a heavily doped region still remains in the active base region, which leads to higher Auger recombination rate, limiting β.

5.3.3 New Process Flow: Recessed B-E Junction and Emitter Regrowth

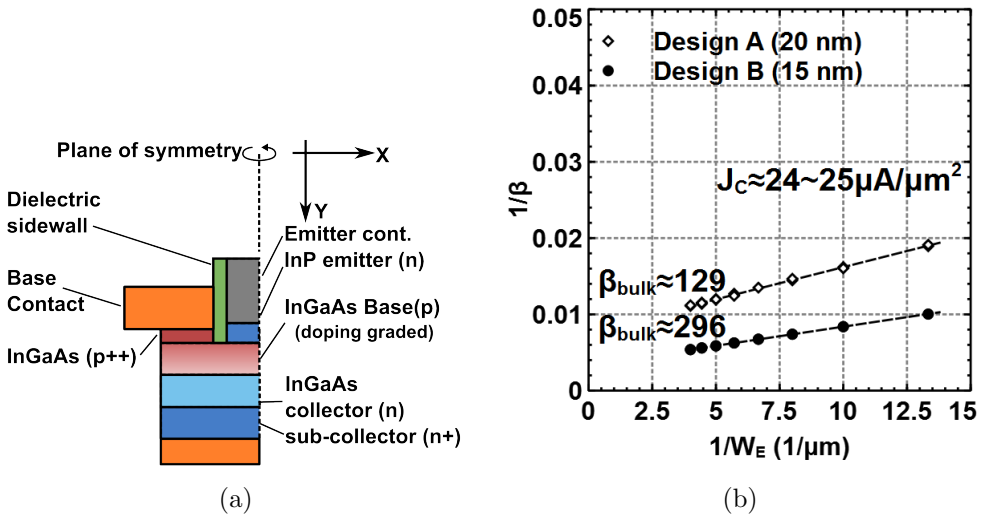
From the simulation results of DHBT58H and DHBT63B, approximately 30% of the base current is due to $I_{\mathrm{B,bulk}}$, which is dominated by the Auger recombination. Although $I_{\mathrm{B,bulk}}$ scales with the emitter width, it will remain a limiting factor on DC-β because the lifetime of the Auger recombination decreases quadratically as the doping concentration increase if the DHBT scaling laws discussed in chapter 2 is to be abided by. The need for high doping concentration results from the need to reduce the specific contact resistivity. For this purpose, only the semiconductor under the base contact has to be highly doped. Although this high doping concentration in the extrinsic base and the active base region does decrease the sheet resistance, the resistance terms associated with the sheet resistance ($R_{\mathrm{BE,spread}}$ and R_{gap}) eventually become less critical to R_{BB} as W_{E} and W_{gap} scale.

In order to de-couple the doping requirements for high β and for high f_{max} in the base, a new geometry for a recessed B-E junction is designed. Fig. 5.10a is the cross-section of the the design. As shown in the schematic, only the region

beneath the base contact is heavily doped. With this geometry, the doping concentration in the graded region does not need to be high, and hence the Auger recombination rate decreases. To fabricate this structure, a new process flow for the B-E junction involving semiconductor regrowth must be designed. On approach is to regrow the region for base contact. Such technique has already been developed for the GaAs/AlGaAs DHBT technology [28]. It requires conformal film growth with $> 10^{20}\,\mathrm{cm}^{-3}$ p-type doping concentration in order to minimize retain the self-aligned feature of InP DHBTs for reduction in R_{gap}, and to have low specific contact resistivity for reduction in $R_{\mathrm{B,cont.}}$. However, it is challenging to achieve this in either molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) systems [29]. Another approach involves the emitter regrowth, which requires conformal film growth and n-type doping concentration at $> 10^{19}\,\mathrm{cm}^{-3}$. Unlike the base regrowth, such growth has been achieved by MOCVD at a larger device dimension [30, 31].

A process flow has been developed for the regrown junction. Starting from a DHBT sample with the pulse-doped layer except without the emitter structure, the B-E junction is first defined, after which the base contact is formed in the field except in the B-E junction. After encapsulating the metal contact by ALD dielectric, the B-E junction is defined again for MOCVD regrowth. The pulse-doped layer in the junction is removed by a digital etch process before the emitter semiconductor is grown onto the junction area.

Based on the layer structures A and B, the devices with the recessed B-E junction were constructed in Sentaurus. The DC-β of the devices with W_{gap}=10 nm was computed at $J \approx 25\,\mathrm{mA}/\mu\mathrm{m}^2$, and the simulation results are shown in fig.



(a) (b)

Figure 5.10: (a) The Schematic of the simulated SHBTs with the recessed B-E junction. (b) Computed $1/\beta$ vs. $P_{\rm je}/A_{\rm je}$ of the designs at $J_{\rm E} \approx 24 \sim 25\,{\rm mA}/\mu{\rm m}^2$. The simulation retained the parameters ($v_{\rm surf.rec.}$, $D_{\rm it}$, $C_{\rm Auger,p}$, etc.) of DHBT58H and assumed $W_{\rm gap}$=10 nm.

5.10b. Because the active base region is thin and less-heavily doped, simulations indicated a significant improve in $\beta_{\rm bulk}$. $K_{\rm B,edge.}$ for layer structure A and B are reduced to 10.6 and 6.3 μA/μm, respectively.

Among the three designs, the pulse-doped layer and digital etch process are relatively easy to be integrated into the DHBT fabrication, and both have demonstrated suppression in $I_{\rm B,diff.}$. However, their improvement in β is still limited by Auger recombination because of high doping concentration in the active base region. The recessed B-E junction geometry, though difficult to incorporate due to its process flow involving emitter regrowth, has the potential to significantly increase DC-β. Moreover, it is the only design which exhibit a β greater than 50 at $w_{\rm E}$=75 nm. If the regrowth process can be successfully incorporated into the DHBT fabrication with adequately low defect states, the DC-current gain in the future scaling generations of DHBTs will be substantially improved [32].

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Chapter 6

Conclusion

6.1 Achievements

6.1.1 Process Improvements

The process flow for the composite emitter metal stack [1,2] has been modified. By adjusting the W:TiW ratio and recalibrating the refractory metal dry etch, the emitter width has been scaled below 100 nm while retaining the vertical sidewall profile necessary for the subsequent self-aligned base contact. This enables not only smaller base-emitter junction area, but also access to the extrinsic base surface after the base metalization. With the access to the extrinsic base surface, more adequate passivation technique could be applied to terminate InGaAs, reducing the interface trap density.

A process flow for forming composite ALD Al_2O_3/ PECVD SiN_x sidewall after the base metalization has been developed and integrated into the fabrication of DHBTs. Using a thermal ALD recipe, Al_2O_3 can be deposited onto the extrinsic base surface without the presence of plasma; hence avoid the plasma damage. In addition, the composite sidewall encapsulates the extrinsic base, preventing damage to the extrinsic base from the subsequent process flow. Moreover, the sidewall could potentially serve as hard mask which protects the B-E junction and the extrinsic base if a base metal dry etch process is to be included after the base contact. This is beneficial to the bi-layer refractory base metal process flow [3], which is currently being developed for its integration into the DHBT process flow.

The process flow forming interconnects between metal layers in the back end process has been reinvestigated. Using the photo-sensitive resin (Photo-BCB) and thick metal lift-off ($\sim 3\,\mu$m), the back end process flow has been expedited. This al-

lows the incorporation of more versatile circuit, and, more importantly, microstrip lines as well as on-wafer ML-TRL calibration standards [4] for RF measurements. This would not only enable RF measurements at various RF bandwidths, but also reduces the error/noise in the measurement and device de-embedding, allow a more accurate extrapolation of f_τ and $f_{\max}$.

6.1.2 Device Performance

Table. 6.1 summerized the device results from two DHBT runs reported in this dissertation, DHBT63B and DHBT58H. With the modified emitter metal stack process flow, the base-emitter junction width has been successfully scaled to 85 nm on DHBT58H. As the B-E junction width reduces from 210 to 85 nm, DC-β drops from 20 to 10. Although the devices have been scaled, the cutoff frequencies is still limited. Devices on DHBT63B exhibited low f_τ because they were unable to sustain sufficient emitter current density. Devices on DHBT58H suffered from high C_{CB} due to overestimated B-E junction width, resulting in low $f_{\max}$. Both samples demonstrates high specific base contact resistivity in the devices. This further limited $f_{\max}$. As a result, the highest $f_\tau f_{\max}$ product was $0.357\,\mathrm{THz}^2$, obtained from a device on DHBT63B with a 200 nm base-emitter junction.

Although the RF performances of DHBT63B and DHBT58H are not as good as designed, the overall transistor yields on both samples have been greatly improved. Approximately 80 to 90% of the probed device demonstrate a reasonable transistor DC characteristics. The improvement in transistor yield can be partially attributed to the adjustment in the process flow for the emitter metal stack.

Design	T_B	N_A	T_C	W_E	β	f_τ	f_{max}
Unit	nm	$\times 10^{19}$cm^{-3}	nm	nm		GHz	GHz
DHBT63B	25	9-5	75	270	18.2	510	600
				220	17.4	509	702
				170	14.6	490	670
DHBT58B	20	12-8	100	210	20.2	390	780
				160	18.4	450	700
				110	16.4	405	630
				85	10.7	330	650

Table 6.1: A summary of device performance of DHBT63B and DHBT58H.

The sufficient yield enabled a more thorough mapping of devices during DC and RF measurements. Moreover, we were also able to observe the trend of DC-β, parasitic resistance, and parasitic capacitance vs. the physical dimensions of the transistors, from which more analyses could be done.

6.1.3 Simulation Results

To further analyze the measured DC-β and understand the reduction of current gain in scaled DHBTs, transport phenomenon in the base was simulated using a TCAD software (Sentaurus) [5,6]. A model capable of estimating DC-*beta* to certain precision for a given DHBT design and geometry has been constructed and verified by comparison against the experimental results. Such model would be a useful tool when designing future scaling generations of DHBTs with adequate current gain.

6.2 Future Work

6.2.1 Refractory Base Contact

In order to enhance the RF performance (f_τ and $f_{\max}$) of DHBTs, the two impending issues must be solved: high specific base contact resistivity and B-E junction failure at high current density. To reduce the specific contact resistivity on a $\leq$20 nm base, the penetration or reaction between the metal and InGaAs [7] must be dealt with. Otherwise, the actual metal/InGaAs interface would be deep within the base, where the doping concentration is lower, causing a higher specific contact resistivity. Currently, a bi-layer refractory base contact is under development at UCSB, and the corresponding process flow is listed in appendix A. Several DHBT samples utilizing this process flow has been fabricated. Fig. 6.1 is the TEM cross-section of a DHBT employing such process flow [3]. The improvement in the contact resistivity is now being evaluated.

6.2.2 Extrinsic Base Passivation

If the surface preparation technique involving nitrogen-trimethylaluminium cycle prior to ALD in the fabrication of III-V MOSFET [8] can be applied to the DHBT process flow, D_{it} on the extrinsic base surface can be decreased; hence the surface recombination and surface conduction current reduces, increasing β in scaled DHBTs. However, potential challenges in the implementation are expected. It is unknown if the surface pretreatments developed for the i-InGaAs of the channel of III-V MOSFETs would be applicable to p-InGaAs base of DHBTs.

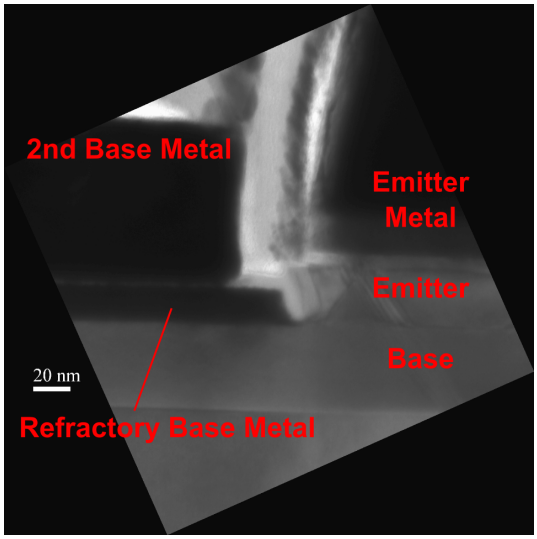

Figure 6.1: The TEM cross-section of a DHBT in bi-layer refractory base contact process flow; device courtesy of J. C. Rode.

In a worse case, thermal annealing might be necessary. The thermal stability of the base contact must be considered.

6.2.3 Emitter Width Scaling and Emitter Regrowth

We have demonstrated in chapter 3 a dry-etch process flow for emitter metal stack, in which the undercut to the middle of the refractory metal stack is ∼10 nm on both sides of the stack. Therefore, narrowest emitter stack this process flow could possible produce is ∼50 nm. For emitter width below 50 nm, the excessive undercut will cause the failure of the process flow. In order to successfully scale the emitter width below 50 nm, a new process flow is required. A process flow utilizing ALD metal is now being developed at UCSB. Because of the self-limiting nature of the ALD growth, a metal fin can be formed by filling

a narrow trench without void formation within the trench. However, as of this time, the process flow has not been fully integrated into the DHBT fabrication.

As discussed in chapter 5, a recessed base-emitter junction formed by a emitter regrowth process flow has the potential to improve DC-β in scaled DHBTs. As of this time, the process development is at its preliminary stage. Several issues including the characterization of the growth, defect state located at the regrown interface, etc. are currently being investigated. In order to evaluate β in the actual devices efficiently, the complicated DHBT process flow should be avoid and a fast-turnaround device structure is to be designed for this purpose.

With the aforementioned possible improvements implemented, a DHBT with the simultaneously decent DC (β >50) and RF ($f_{\max}$ >1 THz) performance will be feasible [9, 10].

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Appendix A

DHBT Process Flow

Acronym	Manufacturer	Model	Description
ALD	Oxford Instruments	FlexAL	Atomic layer deposition system
Autostepper	GCA	GCA 200	I-line (365 nm) wafer stepper
Blue Oven	Blue M Electric	N/A	High temperature oven
Dektak	Veeco Metrology LLC	Dektak 6M	Surface profilometer
E-Beam 1	Sharon Vacuum Co., Inc.	N/A	Four pocket electron beam evaporator
E-Beam 4	CHA Industries	SEC-600-RAP	Multi-wafer electron beam evaporator
EBL	JEOL	JBX-6300FS	Vector Scan Electron Beam Lithography System
Ellipsometer	J.A. Woollam Co., Inc.	M2000DI	Variable angle spectroscopic ellipsometer
ICP	Panasonic	E626I	Inductively coupled plasma etching system
Nanometrics	Nanometrics	N/A	Optical film thickness measurement
PE-II	Technic Inc.	PE-II	Parallel-plates plasma etching (ashing) system
PECVD	Plasma-Therm	790	Plasma enhanced chemical vapor deposition system
SEM	FEI	Sirion	Thermal field emission scanning electron microscopy
Sputter 4	AJA Int'l Inc.	ATC 2200-V	Seven-target DC/RF magnetron sputtering system
UV-Ozone	UVP Inc.	N/A	Uv-ozone cleaner

Table A.1: List of tools involved in DHBT fabrication.

The InP substrates with DHBT epitaxial structure were acquired from IQE corporation. Epitaxial structure is grown on a 4 inch semi-insulating InP substrate in MBE system at IQE. The physical properties of the layers (e.g. doping concentration, sheet resistance, capacitance, large area current gain, etc.) are characterized by IQE in order to monitor the growth condition and ensure the values are within the design tolerances. One-third of the 4 inch substrate is dedicated for the characterization. After receiving the SHBT substrates from IQE, the fabrication is done in the UCSB nanofabrication facility. In this appendix, the step-by-step process flow of DHBT fabrication is described. The acronyms, models and, manufacturers of tools involved in DHBT fabrication are listed in Table. A.1 according to the alphabetical order.

A.1 Overview

The MBE substrate from IQE is first cleaved along the direction of major flat ([011]) and minor flat ([01$\bar{1}$]) into piece-parts of 3×3 cm^2 in order to be accommodated by the UCSB E-beam lithography system. Five pieces are obtained from each DHBT substrate. Each piece/sample is processed separately. Fig. A.1 shows the process flow of the DHBT fabrication. There are two alternatives for base contact. For lift-off base contact (LO), the contact is first defined by EBL and then metalized. For refractory bi-layer base contact (RB), the refractory metal deposition precedes the lithography of the second metal layers.

A.2 Emitter Process Flow

A.2.1 Emitter Contact and Composite Metal Stack

To minimize the stress of the composite metal stack, the recipe in Sputter 4 for low-stress W/TiW stack should be tested and calibrated using dummy 2-inch InP wafers beforehand.

1. E-Beam 1: deposit 20 nm of molybdenum with the chamber empty to outgas the metal source. Wait 30 minutes for the source to cool down before venting the chamber. Load a new crystal monitor into E-Beam 1 after venting.

2. Run 30 minutes UV-Ozone with the chamber empty to clean the reactor.

3. Solvent clean the sample: rinse for 3 minutes each in acetone(ACE), isopropanol(IPA), and de-ionized water (D.I.) with a trickle. Dry the sample with N_2 gun.

4. 10 minutes dehydration bake at 110°C.

5. 15 minutes UV-Ozone treatment for the sample.

6. Etch the sample for 1 minute in 1:10 $HCl : H_2O$. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

7. Immediately load the sample into E-Beam 1. Deposit 20 nm of Mo at chamber pressure $< 10^{-7}$ Torr and deposition rate < 0.5Å/s. Wait 30 minutes for the source to cool down before venting the chamber.

8. Sputter 4: 20 minutes W and 20 minutes $Ti_{0.1}W_{0.9}$ deposition with the chamber empty to outgas the sputtering targets and coat the carrier chuck.

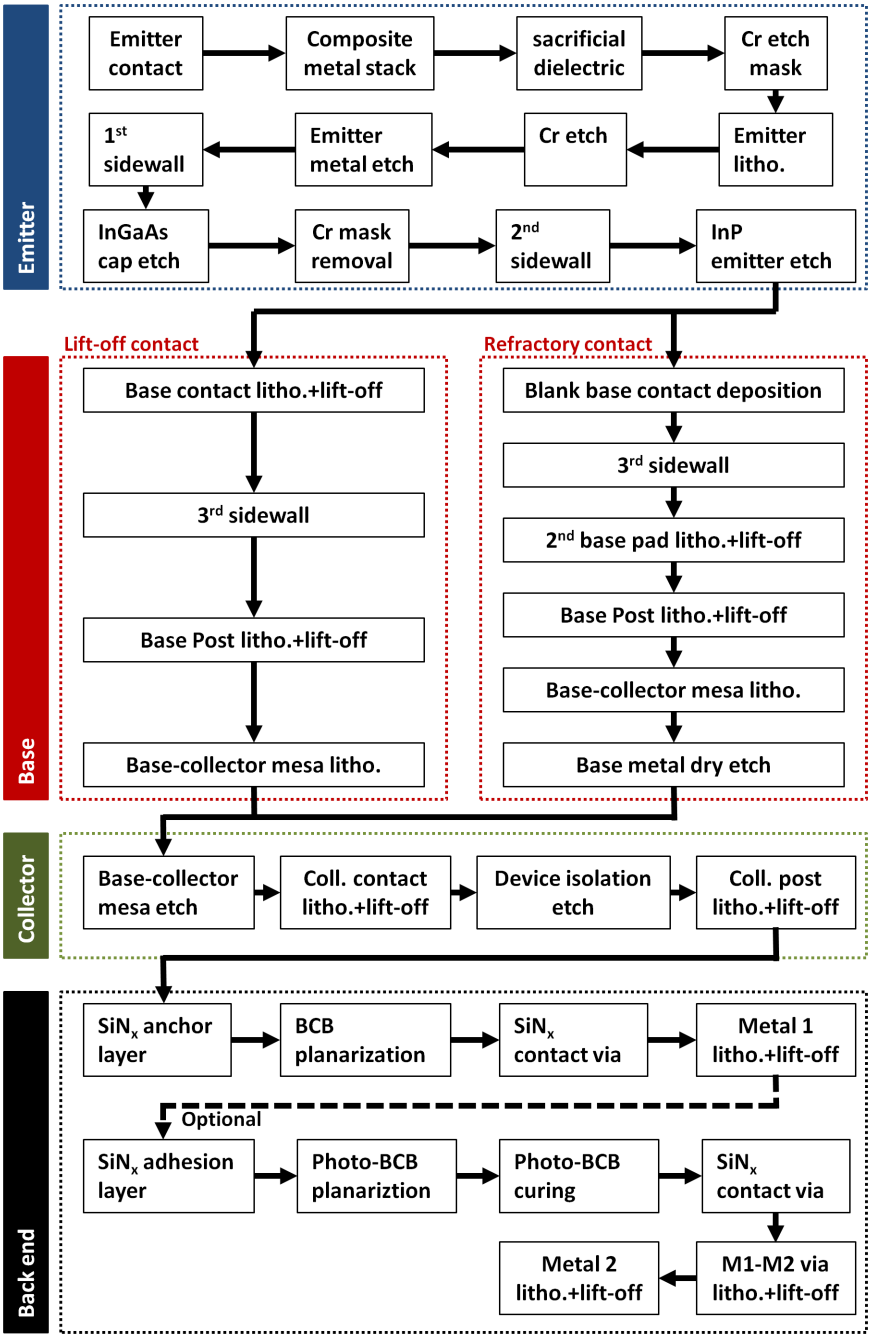

Figure A.1: Flow chart of mesa DHBT fabrication.

9. After venting E-Beam 1, immediately transfer the sample into Sputter 4 to avoid further oxidation of Mo.

10. Sputter 4: deposit 150 nm of W and 350 nm of $Ti_{0.1}W_{0.9}$ on the sample.

A.2.2 Sacrificial Dielectric Layer and Chromium Mask Deposition

1. PECVD: make sure the center chuck is at 250°C.

2. Carefully wipe the PECVD chamber wall with clean room wipe saturated with IPA. Refrain from touching the center chuck for your own safety and the the cleanliness of the chamber.

3. PECVD: run the standard 30 minute CF_4/O_2 etch + 200 ÅSiO_2 deposition to clean the chamber.

4. Deposit 80 nm of SiO_2 on the sample using the standard recipe.

5. Deposit 40 nm of SiN_x on the sample using the standard recipe.

6. E-Beam 1: deposit 40 nm of Cr on the sample.

A.2.3 Emitter Lithography

1. Solvent clean the sample. 10 minutes dehydration bake at 110°C.

2. PE-II: O_2 de-scum at 100 W and 300 mTorr for 30 seconds to clean the sample.

3. Apply ma-N 2403 resist on the sample using syringe and 0.2 μm filters. Spin-coat at 4000 rpm for 30 seconds. Bake at 90°Cfor 90 seconds.

4. EBL: load the sample into the cassette with the major flat direction parallel to the horizontal (x) direction of EBL.

5. EBL: expose the sample with the emitter pattern/job.

6. Develop in AZ300MIF for 35 seconds with slight agitation every 10 seconds. 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

7. verify the pattern using an optical microscope.

Note: 2:1 ma-N2405:Thinneris very comparable to maN2403 in terms of thickness and dose.

A.2.4 Chromium Mask Dry Etch

1. ICP: Make sure the etch chamber temperature is 50°C. Run 10 minutes standard O_2 clean.
2. Etch chemistry and gas flow: $Cl_2/O_2 = 26/4$ sccm; chamber pressure: 1 Pa; ICP/forward bias power 400/18 W.
3. Conditioning (chamber empty) run 125 seconds. Etch the sample for 125 seconds.
4. 3 minutes ACE rinse and 3 minutes IPA rinse.
5. Strip ma-N 2403 in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

A.2.5 Emitter Composite Stack Dry Etch

1. Solvent clean the sample.
2. ICP: Make sure the etch chamber temperature is 50 °C. Run 10 minutes standard O_2 clean.
3. (High power etch) Etch chemistry and gas flow: $SF_6/Ar = 20/5$ sccm, chamber pressure: 1 Pa; ICP/forward bias power 600/200 W; etch time: 195 seconds.
4. (Medium power etch) Etch chemistry and gas flow: $SF_6/Ar = 6.7/3.3$ sccm, chamber pressure: 1 Pa; ICP/forward bias power 600/50 W.
5. (Low power etch) Etch chemistry and gas flow: $SF_6/Ar = 6.7/3.3$ sccm, chamber pressure: 0.5 Pa; ICP/forward bias power 600/18 W; etch time: 70 seconds.
6. Run high power etch with the chamber empty for conditioning.
7. Etch the sample with consecutive high power etch (195 seconds) and low power etch (70 seconds). If the sample appearance is still metallic, run 30 seconds medium power etch.
8. Solvent clean the sample.
9. SEM: check the dry etch profile with SEM. If the bottom (W) flares out, etch the sample with low power etch for another 15 seconds and then solvent clean. Repeat this step until the etch profile is vertical.

10. Measure the stack thickness with Dektak.

A.2.6 First SiN_x Sidewall Formation

1. Solvent clean the sample.
2. PECVD: make sure the center chuck is at 250°C.
3. Carefully wipe the PECVD chamber wall with clean room wipe saturated with IPA. Refrain from touching the center chuck for your own safety and the the cleanliness of the chamber.
4. PECVD: run the standard 30 minute CF_4/O_2 etch + 200 Å SiN_x deposition to clean the chamber.
5. Etch the sample for 10 seconds in 1:10 $HCl : H_2O$. 1 minute D.I. rinse with a trickle.
6. Immediately transfer the sample into PECVD and deposit 20 nm of SiN_x.
7. Deposit 100 nm of SiN_x on a 2 inch Si wafer. Cleave the Si wafer so it and the sample are approximately of the same size.
8. Measure SiN_x thickness with Ellipsometer.
9. ICP: Make sure the etch chamber temperature is 50 °C. Run 10 minutes standard O_2 clean.
10. (High power etch) Etch chemistry and gas flow: $CF_4/O_2 = 20/5$ sccm; chamber pressure: 1 Pa; ICP/forward bias power 500/100 W.
11. (Low power etch) Etch chemistry and gas flow: $CF_4/O_2 = 20/2$ sccm; chamber pressure: 0.3 Pa; ICP/forward bias power 25/18 W.
12. Run high power etch for 5 minutes with the chamber empty for conditioning.
13. Etch the Si piece with low power etch for 4 minutes.
14. Measure SiN_x thickness again with Ellipsometer and determine the etch rate. Calculate the etch time for 20% overetch (120%) accordingly.
15. Etch the sample with low power etch for the calculated time.
16. Solvent clean the sample.
17. SEM: check the sample for any abnormality.

A.2.7 InGaAs Emitter Cap Wet Etch

1. Solvent clean the sample.
2. Mix 1:10 NH_4OH : H_2O solution and stir it with the wafer basket. Mix 1:1:25 H_3PO_4 : H_2O_2 : H_2O solution. Stir at 200 rpm for at least 5 minutes.
3. Etch the sample in NH_4OH : H_2O solution for 10 sec. D.I. rinse for 30 seconds with a trickle and dry the sample with N_2 gun.
4. Etch the sample in H_3PO_4 : H_2O_2 : H_2O solution for 5 to 7 seconds without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

A.2.8 Chromium Mask Removal

1. Solvent clean the sample.
2. (Optional) Dehydration bake for 10 minutes at 110°C.
3. (Optional) Apply SPR955CM-1.8 photoresist on the sample and spin-coat at 4000 rpm for 30 seconds. Bake at 90°Cfor 1 minute.
4. (Optional) Measure the photoresist thickness with Nanometrics using "Positive Resist on Si" recipe and refractive index of 1.6. Thickness should be 1.6 to 1.7 μm.
5. (Optional) PE-II: clean the chamber wall. Run 5 minutes O_2 de-scum at 300 W and 300 mTorr with chamber empty.
6. (Optional) PE-II: 8 minutes O_2 de-scum at 200 W and 300 mTorr on the sample.
7. (Optional) Measure the photoresist thickness again. Calculate the etch rate.
8. (Optional) Etch the sample with PE-II until photoresist surface is 50 to 100 nm lower than the TiW/SiO_2 interface.
9. (Optional) Bake at 110°Cfor 1 minute.
10. Mix Tergitol^{TM}:buffered-HF (BHF) solution (approximately 1:200). Carefully stir the solution with the wafer basket until foam appears.

11. Etch the sample in the Tergitol^{TM}:BHF solution for 65 seconds with slight agitation every 10 seconds. D.I. rinse with a trickle for 3 to 5 minute until the foam disappear. Dry the sample with N_2 gun.

12. (If followed the optional steps) Strip the photoresist in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

13. SEM: observe the sample and determine the removal yield.

A.2.9 Second SiN_x Sidewall Formation

Repeat the steps for the first SiN_x sidewall.

A.2.10 InP Emitter Wet Etch (LO)

1. Solvent clean the sample.

2. Mix 1:10 NH_4OH : H_2O solution and stir it with the wafer basket. Mix 4:1 H_3PO_4 : HCl solution. Stir at 200 rpm for at least 5 minutes.

3. Etch the sample in NH_4OH : H_2O solution for 10 sec. D.I. rinse for 30 seconds with a trickle and dry the sample with N_2 gun.

4. Etch the sample in H_3PO_4 : HCl solution for 8 to 10 seconds (depends on emitter thickness) without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

A.2.11 Base Contact Lithography and Lift-off(LO)

The base contact metalization steps must immediately follow the InP emitter etch to minimize specific contact resistivity.

1. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

2. Apply UV-6 resist on the sample and spin-coat at 3000 rpm and 400 rpm/s for 60 seconds. Bake at 115°Cfor 1 minute.

3. EBL: load the sample into the cassette with the major flat direction parallel to the horizontal (x) direction of EBL.

4. EBL: align and expose the sample with the base contact pattern/job.

5. Bake at 115°Cfor 2 minute immediately after EBL.

6. Develop in AZ300MIF for 70 to 75 seconds with slight agitation every 15 seconds. 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

7. E-Beam 4: load private Pd, Ti, Au, Pt sources, and a new crystal monitor.

8. Etch the sample in 1:10 HCl : H_2O solution for 10 sec. D.I. rinse for 1 minute with a trickle and dry the sample with N_2 gun.

9. After the chamber pressure $< 10^{-6}$ Torr, evaporate 25 Å of Pt at deposition rate $<$ 0.2Å/s, 170 Å of Ti at deposition rate $<$ 0.5Å/s, 170 Å of Pd at deposition rate $<$ 0.5Å/s, and 650 Å of Au at deposition rate $<$ 1Å/s on the sample.

10. Strip UV-6 and lift-off in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

11. SEM: observe the sample and check for any abnormality.

A.2.12 Third Sidewall Formation (LO/RB)

The third sidewall formation steps should immediately follow the base metalization to prevent further contamination on InGaAs surface of the extrinsic base.

1. ALD: set the chamber temperature to 200°C. Run 100 cycles of thermal Al_2O_3 deposition with the chamber empty.

2. ALD: deposit 150 cycles of thermal Al_2O_3 on a 2 inch Si wafer. Measure thickness with Ellipsometer and determine the deposition rate.

3. Solvent clean the sample.

4. (Optional) Run 30 minutes UV-Ozone with the chamber empty to clean the reactor. 10 to 15 minutes UV-Ozone treatment for the sample.

5. Etch the sample for 1 minute in 1:10 HCl : H_2O. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun. Immediately transfer the sample into ALD loadlock.

6. Based on the obtained rate, deposit 10 nm of Al_2O_3 on the sample.

7. Follow the steps of first/second SiN_x sidewall formation to form 20 to 30 nm thick sidewall.

8. Use the SiN_x sidewall as hard mask and etch Al_2O_3 in AZ300MIF for 120% overetch (etch rate$\approx$ 20Å/s). 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

9. SEM: observe the sample and check for any abnormality.

Note: AZ300MIF could be substituted by diluted BHF for etching Al_2O_3.

A.2.13 Base Post Lithography and Lift-off (LO/RB)

1. Measure the base contact pad thickness with Dektak.

2. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

3. Apply LOL resin on the sample and spin-coat at 3000 rpm for 30 seconds. Bake at 180°Cfor 2 minute.

4. Apply nLOF5510 photoresist on the sample and spin-coat at 1800 rpm and 350 rpm/s for 40 seconds. Bake at 90°Cfor 60 seconds.

5. Load the sample into Autostepper in the orientation 180°rotated from that of the EBL.

6. Align and expose the sample for 0.2 to 0.24 second with the base post mask.

7. Bake at 110°Cfor 60 seconds.

8. Develop the sample in AZ300MIF for 105 seconds without any agitation. 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

9. Verify the pattern and the alignment using an optical microscope with the green filter. Look for the undercut to LOL. Rework if no undercut is observed or the misalignment is too great.

10. PE-II: O_2 de-scum at 100 W and 300 mTorr for 20 seconds.

11. E-Beam 4: replace crystal monitor. Evaporate 200 Å of Ti at deposition rate < 0.5Å/s and x Å of Au at deposition rate $= 1 \sim 4$Å/s on the sample, where x equals the thickness required for the base post to be at least 50 nm taller than the emitter stack (W/Tiw plus base metal on top of it).

12. Strip the photoresist and lift-off in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

13. SEM: observe the sample and check for any abnormality.

Note: LOL resin could be substituted by 1:2 PMGI:T Thinner.

A.2.14 Base-collector Mesa Lithography (LO/RB)

1. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.
2. Apply HMDS on the sample and wait 20 seconds. Spin-coat at 3000 rpm for 60 seconds and wait for aonther 60 seconds.
3. Apply ma-N 2410 resist on the sample using syringe and 0.2 μm filters. Spin-coat at 3000 rpm and 450 rpm/s for 60 seconds. Bake at 90°Cfor 150 seconds.
4. EBL: load the sample into the cassette with the major flat direction parallel to the horizontal (x) direction of EBL.
5. EBL: align and expose the sample with the base mesa pattern/job.
6. Develop in AZ300MIF for 135 seconds with slight agitation every 10 seconds. 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.
7. PE-II: O_2 de-scum the sample at 100 W and 300 mTorr for 30 seconds.
8. SEM: verify the pattern and the alignment using a dummy DHBT structure.

A.2.15 InP Emitter Wet Etch (RB)

1. Run 15 minutes UV-Ozone with the chamber empty to clean the reactor.
2. Mix 1:10 HCl : H_2O solution and stir it with the wafer basket. Mix 4:1 H_3PO_4 : HCl solution. Stir at 200 rpm for at least 5 minutes.
3. Solvent clean the sample.
4. 10 minutes UV-Ozone treatment for the sample.
5. Etch the sample for 10 seconds in 1:10 HCl : H_2O. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.
6. Etch the sample in H_3PO_4 : HCl solution for 5 to 7 seconds (depends on emitter thickness) without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

7. Solvent clean the sample.

8. Etch the sample for 10 seconds in 1:10 $HCl : H_2O$. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

A.2.16 First Base Metalization (RB)

The base contact metalization steps must immediately follow the InP emitter etch to minimize specific contact resistivity.

1. Before InP emitter etch, deposit 20 nm of Pt and 20 nm of ruthenium with E-Beam 1 with the chamber empty to outgas the metal source. Wait 30 minutes for the source to cool down before venting the chamber. Load a new crystal monitor into E-Beam 1 after venting.

2. After InP emitter etch, immediately load the sample into E-Beam 1. After chamber pressure $< 10^{-7}$ Torr, deposit 20 Å of Pt at deposition rate $<$ 0.2Å/s, 200 Å of Ru at deposition rate $<$ 0.5Å/s, and 20 Å of Pt at deposition rate $<$ 0.5Å/s. Wait 30 minutes for the source to cool down before venting the chamber.

A.2.17 Second Base Metal Lithography and Lift-off (RB)

1. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

2. Apply PMGI SF-8 resin on the sample using syringe and 0.2 μm filters. Spin-coat at 4000 rpm and 400 rpm/s for 60 seconds. Bake at 180°Cfor 3 minutes.

3. Apply 1:1 ZEP520:A resist on the sample using syringe and 0.2 μm filters. Spin-coat at 3000 rpm for 60 seconds. Bake at 180°Cfor 3 minutes.

4. EBL: load the sample into the cassette with the major flat direction parallel to the horizontal (x) direction of EBL.

5. EBL: align and expose the sample with the base contact pattern/job.

6. ZEP development: 50 seconds amyl acetate and 60 seconds IPA. Dry the sample with N_2 gun.

7. PMGI development: 250 seconds AZ300MIF. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

8. E-Beam 4: load private Ti, Au sources, and a new crystal monitor.

9. After the chamber pressure $< 10^{-6}$ Torr, evaporate 200 Å of Ti at deposition rate < 0.5Å/s, and 650 Å of Au at deposition rate < 1Å/s on the sample.

10. Strip the resist and lift-off in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

11. SEM: observe the sample and check for any abnormality.

A.2.18 Refractory Metal Dry Etch (RB)

1. ICP: Make sure the etch chamber temperature is 50 °C. Run 10 minutes standard O_2 clean.

2. Etch chemistry and gas flow: $Ci_2/O_2 = 5/20$ sccm; chamber pressure: 0.67 Pa; ICP/forward bias power 400/100 W.

3. 50 seconds chamber conditioning using the above recipe. Etch the sample for 50 seconds (etch time scales with Ru thickness).

4. Carefully clean the back side of the sample with cleanroom solvent (ACE, IPA, D.I.) and swab. Dry the sample with N_2 gun.

5. Leave the resist on the sample for the subsequent base-collector mesa wet etch.

A.2.19 Base-collector Mesa Wet Etch

InGaAs wet etch for base, setback and InGaAs/InAlAs superlattice grade:

1. Measure the base mesa resist thickness with Dektak.

2. Mix 1:10 NH_4OH : H_2O solution and stir it with the wafer basket. Mix 1:1:25 H_3PO_4 : H_2O_2 : H_2O solution. Stir at 200 rpm for at least 5 minutes.

3. Etch the sample in NH_4OH : H_2O solution for 10 sec. D.I. rinse for 30 seconds with a trickle and dry the sample with N_2 gun.

4. Etch the sample in H_3PO_4 : H_2O_2 : H_2O solution for 25 to 30 seconds (depends on base/collector designs) without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

5. Measure thickness with Dektak again and make sure that target depth is reached. Otherwise, do additional InGaAs etch before proceeding.

InP wet etch for collector:

6. Mix 4:1 H_3PO_4 : HCl solution. Stir at 200 rpm for at least 5 minutes.
7. Etch the sample in H_3PO_4 : HCl solution for 22 to 32 seconds (time varies with collector designs) without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.
8. Measure thickness with Dektak again and make sure that target depth is reached. Otherwise, do additional InP etch.
9. Strip the resist in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.
10. SEM: observe the sample and verify the etch.

Note: both InGaAs and InP wet etch time depend on the epitaxial design. The etch time for 25 nm base, 14.5 nm setback, and 12 nm InGaAs/InAlAs grade is 27 seconds. The etch time for 77.5 nm InP collector is 28 seconds.

A.2.20 Collector Contact Lithography and Lift-off

1. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.
2. Apply nLOF2020 photoresist on the sample and spin-coat at 3500 rpm for 30 seconds. Bake at 110°Cfor 60 seconds.
3. Load the sample into Autostepper in the orientation 180°rotated from that of the EBL.
4. Align and expose the sample for 0.16 second with the collector contact mask.
5. Bake at 115°Cfor 60 seconds.
6. Develop the sample in AZ300MIF for 120 seconds with minor agitation every 30 seconds. 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.
7. Verify the pattern and the alignment using an optical microscope with the green filter. Rework if the misalignment is too great.
8. PE-II: O_2 de-scum at 100 W and 300 mTorr for 20 seconds.

9. Etch the sample for 10 seconds in 1:10 $HCl : H_2O$. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun. Immediately load the sample into E-Beam 4 afterwards.

10. E-Beam 4: replace crystal monitor. Evaporate 200 Å of Ti at deposition rate < 0.5Å/s, 200 Å of Pd at deposition rate < 0.5Å/s, and 2500 Å of Au at deposition rate $= 1 \sim 4$Å/s onto the sample.

11. Strip the photoresist and lift-off in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

12. SEM: observe the sample and check for any abnormality.

A.2.21 Device Isolation Lithography and Wet Etch

Lithography:

1. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

2. Apply SPR955CM-0.9 photoresist on the sample and spin-coat at 3000 rpm for 30 seconds. Bake at 95°Cfor 90 seconds.

3. Load the sample into Autostepper in the orientation 180°rotated from that of the EBL.

4. Align and expose the sample for 0.27 second with the device isolation mask.

5. Bake at 110°Cfor 90 seconds.

6. Develop the sample in AZ300MIF for 60 seconds with slight agitation every 15 seconds. 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

7. Verify the pattern and the alignment using an optical microscope with the green filter. Rework if the misalignment is too great.

8. PE-II: O_2 de-scum at 100 W and 300 mTorr for 20 seconds.

InGaAs sub-collector wet etch:

9. Measure the photoresist thickness with Dektak.

10. Mix 1:10 $NH_4OH : H_2O$ solution and stir it with the wafer basket. Mix 1:1:25 $H_3PO_4 : H_2O_2 : H_2O$ solution. Stir at 200 rpm for at least 5 minutes. Mix 4:1 $H_3PO_4 : HCl$ solution. Stir at 200 rpm for at least 5 minutes.

11. Etch the sample in NH_4OH : H_2O solution for 10 sec. D.I. rinse for 30 seconds with a trickle and dry the sample with N_2 gun.

12. InGaAs etch-stop etch: etch the sample in H_3PO_4 : H_2O_2 : H_2O solution for 15 seconds without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

13. InP sub-collector etch: etch the sample in H_3PO_4 : HCl solution for 30 seconds without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

14. Measure thickness with Dektak again and make sure that target depth is reached. Otherwise, do additional InP etch before proceeding.

Semi-insulating InP wet etch:

15. InGaAs etch-stop etch: etch the sample in H_3PO_4 : H_2O_2 : H_2O solution for 10 seconds without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

16. Semi-insulating InP etch: etch the sample in H_3PO_4 : HCl solution for 12 to 15 seconds without stirrer. D.I. rinse for 3 minute with a trickle and dry the sample with N_2 gun.

17. Measure thickness with Dektak again. Approximately 100 to 200 nm of semi-insulating InP should be removed.

18. Strip the photoresist in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

19. SEM: observe the sample and check for any abnormality.

A.2.22 Collector Post Lithography and Lift-off

1. Measure the base contact pad thickness with Dektak.

2. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

3. Apply nLOF2020 photoresist on the sample and spin-coat at 3500 rpm for 30 seconds. Bake at 110°Cfor 60 seconds.

4. Load the sample into Autostepper in the orientation 180°rotated from that of the EBL.

5. Align and expose the sample for 0.16 second with the collector post mask.

6. Bake at 115°Cfor 60 seconds.

7. Develop the sample in AZ300MIF for 120 seconds with minor agitation every 30 seconds. 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

8. Verify the pattern and the alignment using an optical microscope with the green filter. Rework if the misalignment is too great.

9. PE-II: O_2 de-scum at 100 W and 300 mTorr for 20 seconds.

10. Etch the sample for 10 seconds in 1:10 $HCl : H_2O$. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun. Immediately load the sample into E-Beam 4 afterwards.

11. E-Beam 4: replace crystal monitor. Evaporate 200 Å of Ti at deposition rate < 0.5Å/s and x Å of Au at deposition rate $= 1 \sim 4$Å/s onto the sample, where x equals the thickness required for the collector post to be at least 100 nm taller than the emitter stack (W/Tiw plus base metal on top of it).

12. Strip the photoresist and lift-off in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

13. SEM: observe the sample and check for any abnormality. Measure the gap spacing of the TLM structures.

A.2.23 SiN_x Anchor Layer Deposition

1. PECVD: make sure the center chuck is at 250°C.

2. Carefully wipe the PECVD chamber wall with clean room wipe saturated with IPA. Refrain from touching the center chuck for your own safety and the the cleanliness of the chamber.

3. PECVD: run the standard 30 minute CF_4/O_2 etch + 200 Å SiN_x deposition to clean the chamber.

4. Run 30 minutes UV-Ozone with the chamber empty to clean the reactor.

5. Solvent clean the sample.

6. 10 minutes UV-Ozone treatment for the sample.

7. Etch the sample for 10 seconds in 1:10 $HCl : H_2O$. 1 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

8. Immediately transfer the sample into PECVD and deposit 40 nm of SiN_x.

A.2.24 BCB Planarization

BCB curing:

1. Turn on the Blue Oven and set the N_2 flow to 100 units.

2. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

3. Apply cyclotene 3022-46 (BCB) resin on the sample using syringe and 0.2 μm filters. Wait 30 seconds and spin-coat at 1500 rpm and 150 rpm/s for 30 seconds.

4. Immediately transfer the sample into the Blue Oven. Set the N_2 flow to 60 units.

5. Ramp the temperature to 50°Cover 5 minutes and hold temperature for another 5 minutes.

6. Ramp the temperature to 100°Cover 15 minutes and hold temperature for another 15 minutes.

7. Ramp the temperature to 150°Cover 15 minutes and hold temperature for another 15 minutes.

8. Ramp the temperature to 250°Cover 1 hour and hold temperature for another 1 hour.

9. Wait approximately 12 hours for the chamber to cool down with the chamber door closed.

10. Measure the BCB thickness with Nanometrics.

BCB ash-back:

11. Solvent clean the sample.

12. ICP: Make sure the ash chamber temperature is 50°C.

13. Ash chemistry and gas flow: $CF_4/O_2 = 50/200$ sccm; chamber pressure: 40 Pa; plasma power 1000 W.

14. Conditioning (ash chamber empty) run 15 minutes.

15. Etch the sample for 4 minutes. Solvent clean the sample.

16. Measure the BCB thickness again with Nanometrics.

17. SEM: observe the sample at 2 to 5 kV and check if the emitter stack, base post, and collector posts are all revealed and no BCB residues on them.

18. If the posts are not revealed, do another 15 to 60 seconds BCB ash until they are > 50 nm above the BCB surface.

A.2.25 Dielectric Contact Via

Sputtered SiN_x deposition:

1. Solvent clean the sample.

2. Sputter 4: run 2700 seconds of room-temperature SiN_x recipe on a 2 inch wafer. Cleave the Si wafer so it and the sample are of the similar sizes.

3. Measure SiN_x thickness with Ellipsometer. Calculate the deposition rate.

4. Sputter 60 nm of SiN_x onto the sample.

Lithography:

5. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

6. Apply SPR955CM-0.9 photoresist on the sample and spin-coat at 3000 rpm for 30 seconds. Bake at 95°Cfor 90 seconds.

7. Load the sample into Autostepper in the orientation 180°rotated from that of the EBL.

8. Align and expose the sample for 0.27 second with the contact via mask.

9. Bake at 110°Cfor 90 seconds.

10. Develop the sample in AZ300MIF for 60 seconds with slight agitation every 15 seconds. 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

11. Verify the pattern and the alignment using an optical microscope with the green filter. Rework if the misalignment is too great.

12. PE-II: O_2 de-scum at 100 W and 300 mTorr for 20 seconds.

Lithography:

12. ICP: Make sure the etch chamber temperature is 50 °C. Run 10 minutes standard O_2 clean.

13. (High power etch) Etch chemistry and gas flow: $CF_4/O_2 = 20/5$ sccm; chamber pressure: 1 Pa; ICP/forward bias power 500/100 W.

14. (Low power etch) Etch chemistry and gas flow: $CF_4/O_2 = 20/2$ sccm; chamber pressure: 0.3 Pa; ICP/forward bias power 25/18 W.

15. Run high power etch for 5 minutes with the chamber empty for conditioning.

16. Etch the Si piece from sputtering using low power etch for 6 minutes.

17. Measure SiN_x thickness again with Ellipsometer and determine the etch rate. Calculate the etch time for $60nm \times 120\%$. The thickness of the SiN_x anchor layer is neglected because it has been removed by BCB ash.

18. Etch the sample with low power etch for the calculated time.

19. 3 minutes ACE rinse and 3 minutes IPA rinse.

20. Strip photoresist in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

21. PE-II: O_2 de-scum at 100 W and 300 mTorr for 30 seconds.

22. SEM: check the sample for any abnormality.

A.2.26 Metal 1 Lithography and Lift-off

1. Solvent clean the sample. Dehydration bake for 10 minutes at 110°C.

2. Apply nLOF2020 photoresist on the sample and spin-coat at 3500 rpm for 30 seconds. Bake at 110°Cfor 60 seconds.

3. Load the sample into Autostepper in the orientation 180°rotated from that of the EBL.

4. Align and expose the sample for 0.16 second with the metal 1 mask.

5. Bake at 115°Cfor 60 seconds.

6. Develop the sample in AZ300MIF for 120 seconds with minor agitation every 30 seconds. 3 minute D.I. rinse with a trickle. Dry the sample with N_2 gun.

7. Verify the pattern and the alignment using an optical microscope with the green filter. Rework if the misalignment is too great.

8. PE-II: O_2 de-scum at 100 W and 300 mTorr for 20 seconds.

9. E-Beam 4: replace crystal monitor. Evaporate 200 Å of Ti at deposition rate < 0.5Å/s, 10 kÅ of Au at deposition rate $= 1 \sim 4$Å/s, and 200 Å of Ti at deposition rate < 0.5Å/s onto the sample.

10. Strip the photoresist and lift-off in 1165 at 80°Cfor 1 hour. 3 minutes IPA rinse followed by 3 minutes D.I. rinse with a trickle. Dry the sample with N_2 gun.

11. SEM: inspect the sample and check for any abnormality.