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InP DHBTs in a Refractory Emitter Process for THz Electronics

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by

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for THz Electronics

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by

Vibhor Jain

Dedicated to

my grandparents

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Publications

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Abstract

InP DHBTs in a Refractory Emitter Process for THz Electronics

Vibhor Jain

High speed InP double heterojunction bipolar transistors (DHBTs) have potential applications in 0.3 - 1.0 THz ICs for imaging, sensing, radio astronomy and spectroscopy; in 2 - 20 GHz mixed signal ICs like wideband, high-resolution analog to digital converters, digital to analog converters, and direct digital frequency synthesizers; and in 100 - 500 GHz digital logic.

This dissertation presents the efforts pursued to increase the bandwidth of InP based DHBTs through improved processing techniques and design changes. Lithographic and epitaxial scaling of critical device dimensions and reduced access resistances have decreased the transit delays and *RC* delays associated with the device thereby improving device bandwidth. A new emitter process for high yield emitters, scalable to 70 nm node, has been demonstrated and device measurements at 110 nm and 220 nm junction nodes are presented. The emitter stack incorporates all refractory metals to sustain high current density without problems of electromigration and contact diffusion under stress. Emitter space charge region was redesigned to overcome problems of source starvation and high space charge

region resistance. New and improved surface preparation techniques were developed to achieve low contact resistivity. Reduction in base access resistance was achieved through modified epitaxial design and process optimization. Collector-base capacitance has been reduced by aggressively undercutting the base-collector semiconductor below the base post.

At 110 nm, the devices show excellent current carrying and power handling capabilities and can operate at current density greater than 40 $mA/\mu m^2$ and power density greater than 55 $mW/\mu m^2$ without destruction. At 220 nm node, device f_τ of 480 GHz and f_{max} of 1.0 THz has been demonstrated. Improved RF performance at smaller emitter junction widths can be achieved with improved lithographic procedures for base contact and base mesa definitions.

Measured device transconductance for these HBTs is much lower than expected. A theoretical analysis of the InP/InGaAs emitter base junction was performed to study significant contributors to g_m degradation. These include modulation of the electron injection barrier at emitter base heterojunction by the applied bias, drop in the electron quasi Fermi level in the emitter space charge region and degenerate electron injection and quantum mechanical reflection at the hetero-interface.

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Chapter 1

Introduction

High speed InP double heterojunction bipolar transistors (DHBTs) have potential applications in 0.3 - 1.0 THz ICs for imaging, sensing, radio astronomy and spectroscopy, in 2 - 20 GHz mixed signal ICs like wideband, high-resolution analog to digital converters, digital to analog converters, and direct digital frequency synthesizers and in 100 - 500 GHz digital logic to enable 0.1–1 Tbps optical fibre links [1–8].

Compared to SiGe bipolar transistors and Si CMOS devices, InP DHBTs attain higher bandwidth at a given lithographic feature size and attain higher device breakdown voltage at a given device bandwidth. This is an advantage for both mixed-signal ICs and mm-wave and sub-mm-wave power amplifiers and for low-volume fabrication of small-scale high performance circuits. These advantages

result from the high electron mobility of the InGaAs base [9], the high base doping made feasible by strong emitter-base heterojunctions [10] which results in lower sheet and contact resistance, and the high peak electron velocity and high breakdown field of the InP collector [11]. However, the maturity of advanced silicon processes has enabled aggressive SiGe scaling for improved device f_τ and f_{max}, in addition to an integration scale several orders of magnitude larger. SiGe HBTs having f_τ greater than 300 GHz and f_{max} greater than 400 GHz have already been reported [12–16].

Recently, in high frequency and high power applications, InP HBTs are facing a more serious challenge from GaN high electron mobility transistors (HEMTs) [17]. High frequency performance of GaN HEMTs has improved dramatically in recent years [18]. GaN HEMTs report a much higher breakdown voltage than InP HBTs owing to the high band gap of nitride material system. Use of N-polar face for device fabrication with InN contact layer having a high surface electron accumulation has resulted in very low contact resistivity [19]. Device f_τ in excess of 200 GHz and f_{max} greater than 400 GHz have been reported for GaN HEMTs [20, 21].

Despite all the progress made in SiGe bipolar and GaN HEMT technologies, InP HEMTs and HBTs still have much higher bandwidths than any other competitor material system. Both InP HEMTs and HBTs having f_τ greater than 600 GHz and f_{max} grater than 1.0 THz have been demonstrated, though DHBTs

have a higher breakdown voltage than HEMTs at the same device bandwidth [22–28]. Further device scaling and reduction in parasitic device capacitances and resistances will improve HBT high frequency performance.

Improved transistor bandwidth is achieved by reducing transit delays and RC charging delays associated with the device. Reducing the base and collector thicknesses (T_c) decreases transit delays and increases the current density J_e at the Kirk-effect limit $J_{kirk} \sim T_c^{-2}$; but it also increases the base-collector capacitance (C_{cb}) per unit junction area. RC delays are reduced by reducing junction areas and ohmic contact resistivities. Small-signal ($C_{cb}kT/qI$) and logic ($C_{cb}\Delta V/I$) delays are reduced by increasing J_e; junction lithographic dimensions are reduced partly to reduce the base spreading resistance but primarily to reduce device thermal resistance, accommodating the increased J_e [2, 3].

InP DHBTs described in this work utilize a triple-mesa structure. Collector, base, and emitter layers are grown atop of each other and device layers are isolated by mesa formation once electrical contacts have been made. Under bias, the carriers are swept vertically across the emitter, base and collector by their respective transport mechanisms to realize transistor behaviour. Specific challenges to improving HBT performance include fabricating narrow emitter and base junctions, reducing emitter and base ohmic contact and access resistivities and reliable operation of the transistors at high current density.

The dissertation has two components - HBT design, fabrication and characterization is discussed first, and then a study of the impact of high emitter current density on device transconductance is presented. In chapter 2, mesa DHBT technology with associated transit and RC delays is discussed. Emitter, base and collector design considerations for reducing parasitic delays and analysis of measured data are mentioned. DHBT scaling laws for improved device performance are also discussed. In Chapter 3 the efforts undertaken to improve the device fabrication processes for higher device yield and performance are reported. A new emitter process incorporating a refractory metal stack for sustaining high current density operation has been developed which is scalable to atleast 70 nm, allowing aggressive device scaling efforts for improved device bandwidth. The process also allows for low base access resistance and collector-base capacitance improving device f_{max} at the same device scaling generation. Emitter design and process improvements have reduced the emitter access resistance by more than a factor of 2 from 9 $\Omega \cdot \mu m^2$ [29] to less than 4 $\Omega \cdot \mu m^2$. A new base process for incorporating ultra low resistivity refractory base ohmics has been developed and demonstrated. E-beam writing is now being utilized for achieving sub-200 nm emitter-base junction widths and base contact widths. Chapter 4 reports the DHBT epitaxial design and obtained results. Simultaneous device f_τ and f_{max} of

0.48 and 1.0 THz have been achieved at emitter-base junction width of 220 nm due to reduced base access resistance and collector-base capacitance [27].

Chapter 5 discusses the possible causes of lower than expected device transconductance [30]. Because the collector-base capacitance per unit junction area (C_{cb}/A_c) increases as the collector depletion layer is thinned, the transconductance per unit emitter area g_m/A_e must increase in proportion to the square of transistor bandwidth to reduce the C_{cb}/g_m charging time. For the abrupt emitter-base junction HBTs studied in this thesis, g_m fails to increase in direct proportion to J_e at current densities greater than $\sim 2\ mA/\mu m^2$. The degradation in g_m increases the C_{cb}/g_m charging time and significantly degrades the bandwidth of HBTs having f_τ approaching or exceeding 500 GHz. Significant contributors to g_m degradation in abrupt emitter-base HBTs, including modulation of the emitter-base electron injection barrier by the applied bias, drops in the electron quasi-Fermi level in the emitter space charge region, and quantum mechanical reflection and degenerate electron injection at the emitter-base interface are analysed.

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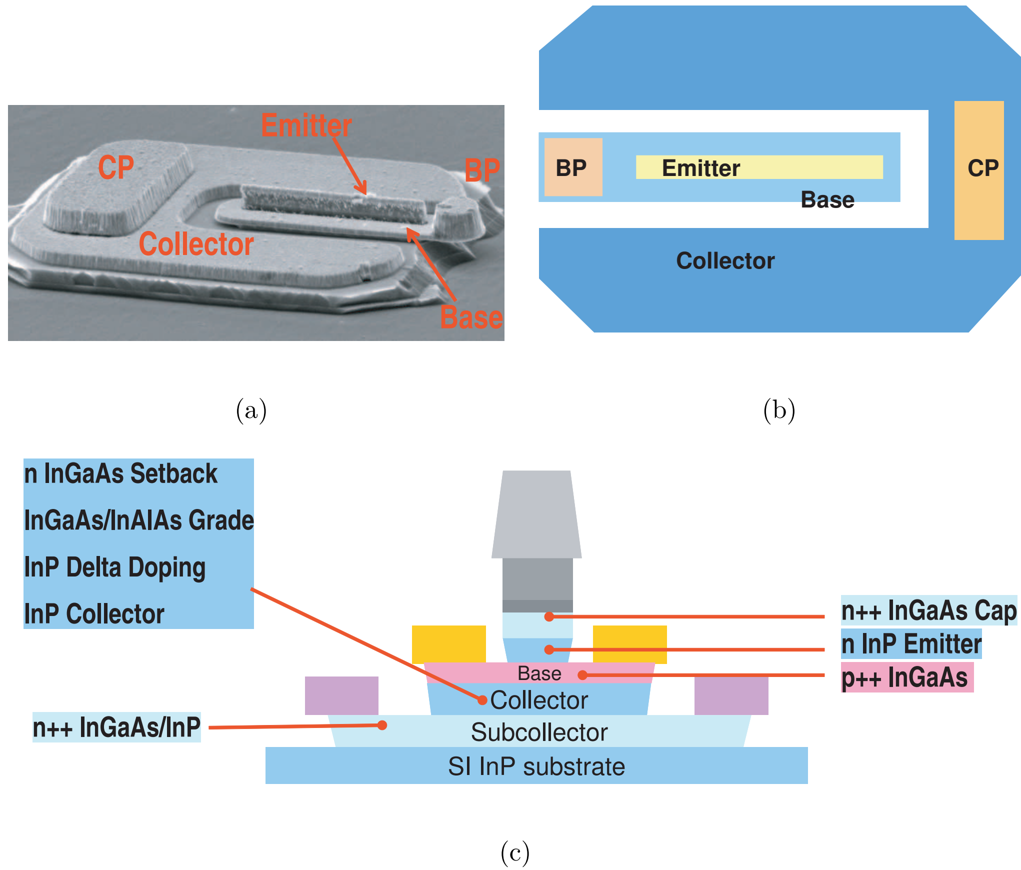
Chapter 2

HBT Theory and Design

In this chapter, different design considerations for emitter, base and collector design for a mesa DHBT are discussed. InP DHBTs described in this work utilize a triple mesa structure as shown in Fig. 2.1. Collector, base, and emitter layers are grown atop of each other and device layers are isolated by mesa formation once electrical contacts have been made. After the emitter contact is formed, the emitter mesa is etched down to the base where self-aligned base contacts are formed to minimize both base access resistance and collector-base capacitance. Base and collector mesa are then etched and collector contacts defined on a thick, highly doped n+ sub-collector as the collector layer is lightly doped and depleted. To isolate devices, the sub-collector is etched from the field through to the semi-insulating InP substrate to form the triple mesa structure.



(a) (b)

(c)

Figure 2.1: (a) SEM image, (b) Top View (layout) and (c) Cross-section schematic of a mesa DHBT

2.1 Emitter Design

2.1.1 Emitter Space Charge Region: Source Starvation Effect

As the DHBT dimensions are scaled, at constant collector current I_c, current density ($J_e = I_c/A_e$) in the emitter increases in proportion to the reduction in

emitter area [1]. For the same emitter length, a 2:1 reduction in emitter width increases emitter current density by a factor of 2. At 110 nm junction widths, measured emitter current density J_e is greater than 30 $mA/\mu m^2$ and will increase with further DHBT scaling [2]. The emitter space charge region should therefore be properly designed to be able to support high current density.

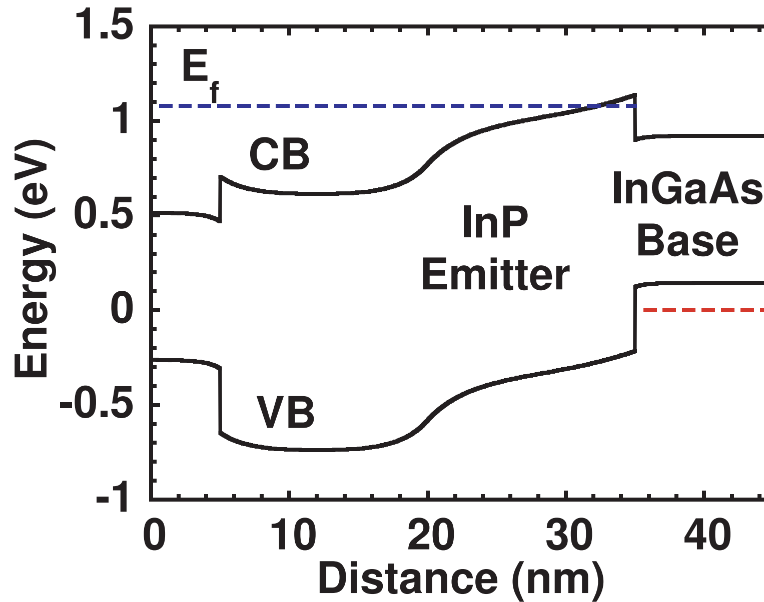


Figure 2.2: Abrupt InP/InGaAs emitter-base junction

Given a current density J_e, mobile charge carrier density in the space charge region (n) is calculated from the relationship $n = J_e/q \cdot v$ where v is the electron velocity. In an abrupt emitter base junction, as shown in Fig. 2.2, the emitter current density flowing into the base is given by $J_e = q \cdot n(W_b) \cdot v(W_b)$ where $n(W_b)$ and $v(W_b)$ are the electron density and velocity respectively at the junc-

tion. For an n++ emitter cap, an n- emitter and a p++ base structure, as V_{be} (or J_e) is increased, electric field in the n- emitter and base at the emitter-base junction decreases in magnitude and eventually reverses. This creates a barrier for the electrons in the emitter away from the hetero-interface (Fig. 2.3). As a result, the junction voltage partitioning factor N rises rapidly degrading the device transconductance g_m and therefore f_τ and f_{max}. This is the source starvation effect in the base-emitter junction [3]. The onset of field reversal depends on the thickness and doping of n- emitter layer.

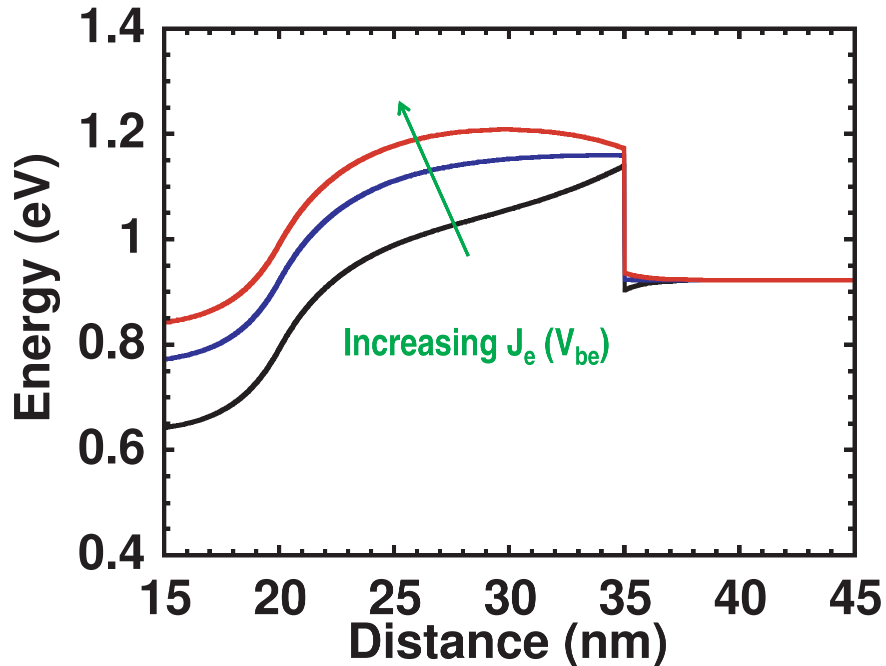


Figure 2.3: Conduction band profile of the abrupt emitter base junction with increasing J_e (V_{be}). As J_e is increased a barrier for the electrons is formed in emitter away from the heterointerface

While designing the emitter space charge region [4], it should be ensured that the J_e limit due to source starvation is much higher than the collector current density limit set by the collector Kirk effect J_{kirk}. It has been observed in some designs that f_τ and f_{max} start rolling off with increased J_e even though collector-base capacitance C_{cb} continues to decrease, indicating a roll off before Kirk limit [5, 6]. This could possibly be due to the source starvation effect.

For the n++ emitter cap, n- emitter and p++ base structure employed, source starvation effect can be reduced through increased n- emitter doping and thinner n- emitter layer. Emitter doping was therefore increased from 8×10^{17} cm^{-3} in DHBT49 design to 2×10^{18} cm^{-3} in DHBT53 and thickness reduced from 30 nm to 15 nm for reduced source starvation effects [2, 7]. The doping has been further increased to 5×10^{18} cm^{-3} in the next generation designs incorporating a thinner collector layer and thereby higher J_{kirk}.

A more accurate determination of J_e at the onset of source starvation will be discussed in Chap. 5. From the analysis in Chap. 5 it can be shown that for DHBT53 design which has a 15 nm InP emitter layer doped at 2×10^{18} cm^{-3} capped above by a 15 nm 5×10^{19} cm^{-3} doped InP layer, maximum $J_e \sim 28$ $mA/\mu m^2$ at room temperature. This analysis neglects the effect of device self heating which could be an important factor in determining maximum J_e.

2.1.2 Emitter Space Charge Region Resistance

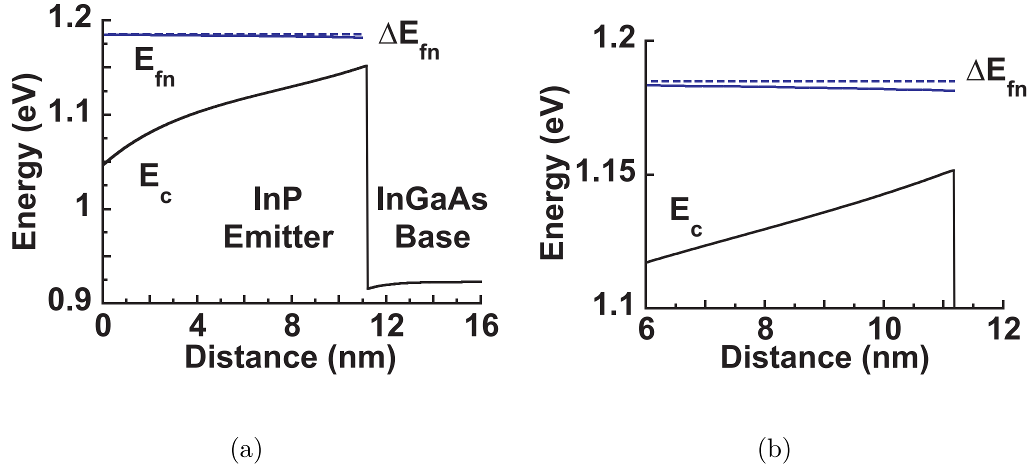
In order to support a high emitter current density without a substantial potential or quasi fermi level drop in the emitter - base space charge region layer, a high electron density $n(z)$ must be present at the base-emitter junction (Fig. 2.4). In high-speed HBTs, the thickness W_{dep} of the base-emitter space charge layer must then be small if significant charge storage effects – drop in quasi Fermi level and space charge region resistance are to be avoided. The drop in electron quasi Fermi level due to electron flux in the emitter space charge region is given by the relation [3]

$$\Delta E_{fn} = \int_{W_{dep}} \frac{J_e}{\mu_n(z).n(z)}\, dz \tag{2.1}$$

where W_{dep} is the emitter space charge region thickness, $\mu_n(z)$ the electron mobility, and $n(z)$ the electron charge density in the space charge region. This quasi Fermi level drop results in an additional space charge resistance R_{sc} which increases $1/g_m$ by an amount equal to R_{sc} where g_m is device transconductance. R_{sc} is calculated from

$$R_{sc} = \frac{1}{q} \cdot \frac{\delta(\Delta E_{fn})}{\delta J_e} \tag{2.2}$$

If the emitter space charge layer is improperly designed having a low doping and thick depletion region, then R_{sc} can be a significant fraction of the total emitter access resistance R_{ex}. For example, analysis of DHBT43 design [5] shows



(a)

(b)

Figure 2.4: (a) Band diagram from electrostatic simulation of InP/InGaAs emitter base junction; (b) Magnified E_c and E_{fn} profile at the emitter base junction showing a drop in the quasi Fermi level (ΔE_{fn}) in the emitter space charge region at high J_e. $J_e \sim 12\ mA/\mu m^2$ was used for this simulation

R_{sc} is $\sim 1.5 - 2\ \Omega \cdot \mu m^2$ for emitter doping of $6 \times 10^{17}\ cm^{-3}$ and depletion thickness of 40 nm. This is a large value especially when ohmic contact resistivities are less than $2\ \Omega \cdot \mu m^2$. From Eqs.(2.1) and (2.2), to reduce the emitter space charge resistance, doping in the emitter needs to be increased and emitter depletion region thickness reduced. Increasing the emitter doping to $2 \times 10^{18}\ cm^{-3}$ and reducing W_{dep} to 15 nm (DHBT53 design), the calculated R_{sc} was reduced to less than $0.1\ \Omega \cdot \mu m^2$, which is a significant improvement over prior designs. An electron mobility of 2000 cm^2/Vs in the emitter space charge region was used for these calculations. Charge density was obtained from electrostatic simulations using Band Prof [8] and J_e from simulations in Chap. 5.

Increasing the emitter doping and reducing W_{dep} reduces the source starvation effect and emitter space charge region resistance. However, there are other design considerations which constrain the choice in emitter doping and thickness. Reduction in W_{dep} increases the emitter-base junction depletion capacitance C_{je} which decreases device f_τ. Increasing emitter doping also worsens the Barrier Modulation effect discussed in Chap. 5 increasing the junction voltage partitioning factor N. It has also been observed that high emitter doping in addition to high base doping results in a degenerate emitter-base junction diode (Esaki diode) leading to high tunneling leakages [9]. It must be ensured that redesigns of the emitter-base junction to increase transconductance and hence reduce C/g_m charging times do not so markedly increase C_{je} as to produce an increase in the C_{je}/g_m charging time.

2.1.3 Emitter Access Resistance

Low emitter access resistivity (ρ_{ex}) is very critical for high f_τ devices. Due to small emitter junction area (A_e), emitter access resistance ($R_{ex} = \rho_{ex}/A_e$) is large and as a result $R_{ex}C_{cb}$ delay becomes a significant fraction of the total device delay. ρ_{ex} consists of different terms - metal resistance (ρ_m), metal-semiconductor contact resistance ($\rho_{c,m}$), InGaAs-InP interface resistance ($\rho_{c,s}$), emitter space charge resistance (ρ_{scr}) and emitter degeneracy resistance (ρ_{degen}). It is important

to identify relative contribution of these terms for future designs. Refractory metals have a high sheet resistance and for the W/TiW stack used currently, $\rho_m \sim 0.4 - 0.6\ \Omega/sq$. $\rho_{c,m}$ depends on the material and doping of emitter cap, surface preparation technique employed and contact metal. $\rho_{c,m}$ as low as $\sim 0.6\ \Omega \cdot \mu m^2$ has been achieved using InAs emitter cap doped at $8.2 \times 10^{19}\ cm^{-3}$ with *in-situ* Mo contacts [10]. $\rho_{c,s} \sim 0.3 - 1.0\ \Omega \cdot \mu m^2$ as computed in [11]. As discussed in the previous section, through improved emitter depletion region design – high emitter doping and thin depletion region, ρ_{scr} has been reduced to less than $0.1\ \Omega \cdot \mu m^2$ for DHBT53 onwards designs.

ρ_{degen} arises due to low density of states in InP emitter. At high current density, degenerate electron concentration is required at the emitter-base junction which results in deviation of J_e from Boltzmann characteristics [1, 12]. This deviation from Boltzmann characteristics will be discussed in detail in chap. 5. ρ_{degen} is a function of current density for a given emitter material and is $\sim 0.8\ \Omega \cdot \mu m^2$ at $J_e \sim 20\ mA/\mu m^2$ for InP emitter.

It is not possible to make emitter TLMs due to self-aligned emitter mesa etch. ρ_{ex} is generally extracted from RF measurements and this extracted ρ_{ex} value incorporates all the contributors discussed above. The intercept of a linear fit to the plot of measured low frequency (2-5 GHz) 1/Re(Y_{21}) as a function of $1/I_c$ is

equal to $R_{ex} + R_{bb}/\beta$.

$$\frac{1}{Re(Y_{21})} = R_{ex} + \frac{R_{bb}}{\beta} + \frac{NkT}{qI_c}$$

R_{bb}/β term is estimated from hybrid-π equivalent circuit and DC measurements. The intercept, however, may change with bias because of the variation in β, voltage partitioning factor N and ρ_{degen} with bias to be discussed in detail in Chap. 5.

R_{ex} can be reduced further by reducing the different associated components. ρ_m can be reduced by using Au emitters which have a lower bulk resistivity. However, with increase in emitter current density, Au emitters may electromigrate [13]. Hence a T-shaped emitter which has a small refractory contact and a larger Au post might be used to reduce ρ_m. $\rho_{c,m}$ can be reduced by making *in-situ* contacts to highly doped InAs emitter cap. Reduction in $\rho_{c,s}$ probably needs a grade from InGaAs to InP which means employing a very highly doped InAlAs/InGaAs chirped superlattice grade. $\rho_{c,s}$ can also be reduced by increasing the doping in both InP and InGaAs emitter layers. ρ_{degen} depends on the material properties, specifically electron effective mass m^* or density of states, and can be reduced by identifying and employing emitter materials having a higher effective mass.

2.2 Base Layer Design

Doping and thickness of the base layer are critical for both device RF performance – f_τ and f_{max} and DC performance – common emitter current gain β. Low base transit time τ_b and therefore thinner base is required for high device f_τ and low base access resistance R_{bb} is needed for high device f_{max}. Recombination in the base needs to be minimized for high device gain. In this section, base doping considerations and layer thickness for improved device performance are discussed.

2.2.1 Doping Considerations

Minority carrier transit time in the base in the presence of an electric field is given by

$$\tau_b = \frac{T_b^2}{D_n} \cdot \frac{kT}{\Delta E_c} \left[1 - \frac{kT}{\Delta E_c} \cdot \left(1 - \exp^{-\Delta E_c/kT}\right)\right] + \frac{T_b}{v_{exit}} \cdot \frac{kT}{\Delta E_c} \cdot \left(1 - \exp^{-\Delta E_c/kT}\right) \tag{2.3}$$

where T_b is the base thickness, v_{exit} the electron velocity at the base collector junction, D_n the minority carrier diffusion constant and ΔE_c change in the conduction band energy across the base [14]. Electric field can be introduced in the base either by using an alloy grade - changing the In:Ga ratio across the base resulting in ΔE_c, or by using a doping gradient - varying the doping across the base. In the DHBTs reported here having abrupt emitter-base junctions, doping

gradient is preferred over alloy grade to ensure a lattice matched epitaxial growth for InP emitter.

Two doping grades have been used here – $7 - 4 \times 10^{19}$ cm^{-3} which produces ΔE_c of $\sim$ 50 meV and $9 - 5 \times 10^{19}$ cm^{-3} which produces ΔE_c of $\sim$ 60 meV (using Joyce-Dixon statistics). Estimation of ΔE_c assumes that there is no band gap narrowing effect due to high doping. In reality, due to very high doping in the base, band gap narrowing effects cannot be neglected and must be included in ΔE_c calculations. Thus, due to doping calibration variations and band gap narrowing, actual ΔE_c might be much lower than the desired value leading to incorrect estimation of τ_b [15, 16]. To ensure lattice matched growth for the base and emitter at high base doping, the In:Ga ratio is kept constant and slightly In rich during the base growth [17]. In future, designs invoking a slightly higher ΔE_c might be used to ensure sufficiently high ΔE_c and low transit time despite of band gap narrowing effects.

2.2.2 Auger Recombination

High doping is required in the base to reduce base access resistance – base sheet resistance and base contact resistivity, for improved device f_{max}. However, with increase in base doping, Auger recombination becomes a prominent recombination mechanism in the base leading to significant drop in HBT current gain β [18,

19]. Assuming infinite base exit velocity, v_{exit}, for minority carriers (Shockley boundary conditions), for a uniformly doped base, the base transit time τ_b is given by $T_b^2/2D_n$ where T_b is the base thickness and D_n is the minority carrier diffusion constant. Auger recombination lifetime (or minority carrier lifetime) decreases with increased doping as $\tau_{Auger} = 1/(k_1.N_A^2)$ [20] where N_A is the active base doping ($N_A = p$). For Auger dominated base recombination current, β is given by τ_{Auger}/τ_b and it varies in proportion to the square of base sheet resistance $\beta \propto R_{sh}^2$. Thus for this simple design, β can be improved through increased R_{sh} in the base by decreasing the base thickness. This relation, however, fails to hold for finite exit velocity.

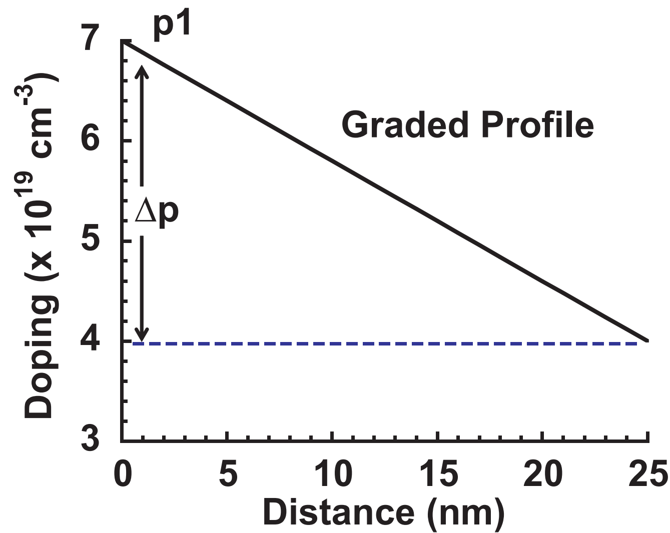


Figure 2.5: Doping profile of a linearly doped base resulting in ΔE_c change across the conduction band in the base

In the HBTs reported in this dissertation, linearly graded base designs have been employed to achieve low base transit time. For a linearly graded base, transit time τ_b is given by Eq. (2.3). Auger limited minority recombination current in the base is obtained from

$$J_b = \int_0^{T_b} k_1 n(x) p(x)^2 dx \tag{2.4}$$

where k_1 is the Auger recombination coefficient and $n(x)$ and $p(x)$ are the minority and majority carrier concentration in the base. For linear doping, majority carrier concentration in the base can be written as $p(x) = p_1 - \Delta p \cdot x/T_b$ (Fig. 2.5) where p_1 is the base doping on the emitter side, Δp is the change in doping across the base and T_b is the base thickness. β is then calculated from J_c/J_b and $1/\beta$ for a linearly graded base is given by

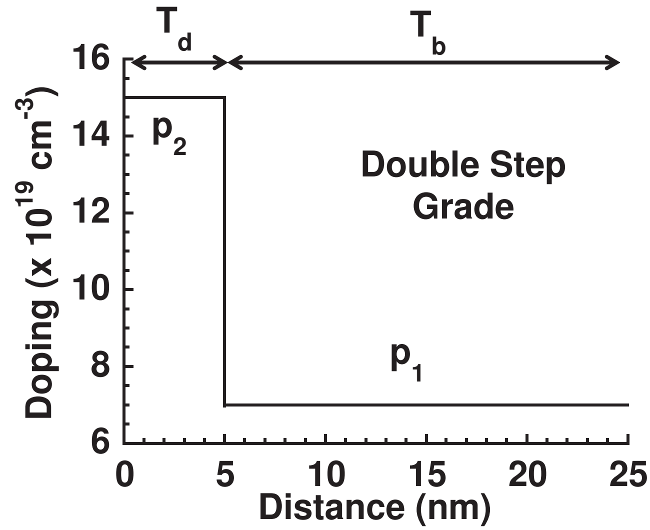
$$\begin{aligned}
\frac{1}{\beta} &= k_1 T_b^2 \frac{kT}{\Delta E_c} \frac{1}{D_n} \left[p_1^2 + \Delta p p_1 + \frac{(\Delta p)^2}{3} \right] \\
&+ k_1 p_1^2 T_b^2 \left(\frac{kT}{\Delta E_c} \right)^2 \left[1 - \exp\left(-\frac{\Delta E_c}{kT} \right) \right] \left[\frac{\Delta E_c}{kT T_b v_{exit}} - \frac{1}{D_n} \right] \\
&+ 2k_1 \Delta p p_1 T_b^2 \left(\frac{kT}{\Delta E_c} \right)^3 \left[\frac{\Delta E_c}{kT T_b v_{exit}} - \frac{1}{D_n} \right] \left[\exp\left(-\frac{\Delta E_c}{kT} \right) - 1 + \frac{\Delta E_c}{kT} \right] \\
&+ k_1 (\Delta p)^2 T_b^2 \left(\frac{kT}{\Delta E_c} \right)^4 \left[\frac{\Delta E_c}{kT T_b v_{exit}} - \frac{1}{D_n} \right] \left[2 - 2\exp\left(-\frac{\Delta E_c}{kT} \right) \right. \\
&\left. - 2\frac{\Delta E_c}{kT} + \left(\frac{\Delta E_c}{kT} \right)^2 \right]
\end{aligned} \tag{2.5}$$

Different research groups have reported different measured values of k_1. In the results below, $k_1 = 8.1 \times 10^{-29} cm^6/s$ is used which was independently measured

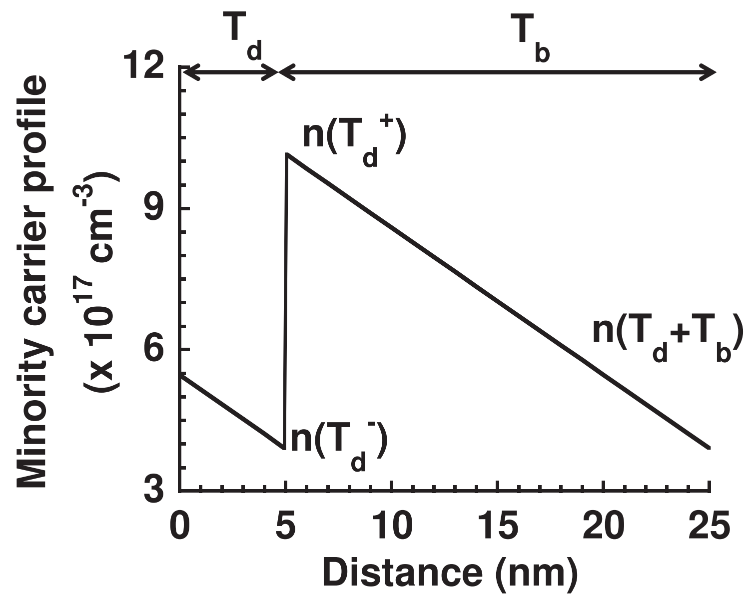
for p-type InGaAs by two groups [20, 21]. Henry et al. [22] have observed a higher minority carrier lifetime in their devices and therefore lower $k_1 \sim 5 \times 10^{-30} cm^6/s$. Auger limited minority carrier lifetime decreases, and therefore Auger coefficient k_1 increases, as In content is increased in InGaAs [23]. An Auger coefficient of $< 10^{-30} cm^6/s$ has been reported for highly doped p-GaAs [19, 24, 25] and as a result a larger reported value of $k_1 \sim 8.1 \times 10^{-29} cm^6/s$ is a reasonable estimate which is used in this work.

For a 25 nm thick base having a $7 - 4 \times 10^{19} cm^{-3}$ doping grade ($\Delta E_c =$ 50 meV), calculated β from Auger recombination is 47 which reduces to 34 for $9 - 5 \times 10^{19} cm^{-3}$ grade ($\Delta E_c = 62$ meV). This value is higher than the measured β value, indicating that β for the devices reported here is not limited by auger recombination. Further increase in doping in the base could lead to current gain collapse due to high Auger recombination.

An alternate design incorporating a highly p+++ doped delta layer at the emitter base junction has been proposed to reduce base contact resistivity without affecting β. To understand the design, consider a simplified doping profile for the base (Fig. 2.6(a)) having a thin (T_d) highly doped layer at the emitter junction and then a lightly doped layer (double step design). Base transit time for this design can be calculated using the charge control model. However, at the point where base doping changes abruptly from high to low ($x = T_d$), Boltzmann char-



(a)



(b)

Figure 2.6: (a) Doping profile and (b) minority carrier profile of a double step base having a thin highly doped layer at the emitter junction

acteristics cannot be used for determining minority carriers as it requires minority carrier velocity higher than thermal velocity. Therefore, finite carrier velocity is used at the doping change point ($x = T_d$) for minority carrier calculation as is used at the base-collector junction. As a result, $n(x)$ just to the right of the doping junction at T_d, $n(T_d^+)$, is given by $n(T_d^+) = J_c/qv_{exit} + J_cT_b/qD_n$ and to the left of the doping junction,$n(T_d^-)$, is given by $n(T_d^-) = J_c/qv_{th}$ where v_{th} is the thermal velocity (Fig. 2.6(b)). Base transit time for this design is given by

$$\tau_b = \frac{T_b + T_d}{v_{exit}} + \frac{T_b^2 + T_d^2}{2D_n} \tag{2.6}$$

assuming $v_{exit} = v_{th}$.

Auger recombination limited β for this design is calculated from J_c/J_b, where J_b is obtained from Eq. (2.4) and $1/\beta$ is given by

$$\frac{1}{\beta} = k_1p_1^2T_b\left(\frac{1}{v_{exit}} + \frac{T_b}{2D_n}\right) + k_1p_2^2T_d\left(\frac{1}{v_{exit}} + \frac{T_b}{2D_n}\right) \tag{2.7}$$

Transit time for a design having $T_d = 5$ nm, $T_b = 20$ nm, $p_2 = 1.5 \times 10^{20}cm^{-3}$ and $p_1 = 7 \times 10^{19}cm^{-3}$ is higher than the grade design of same thickness (0.13 psec as opposed to 0.08 psec) and consequently β is lower at 20.

Transit time and β can both be improved by replacing the uniform low doping in the design above with a doping grade as shown in Fig. 2.7 (step–grade design).

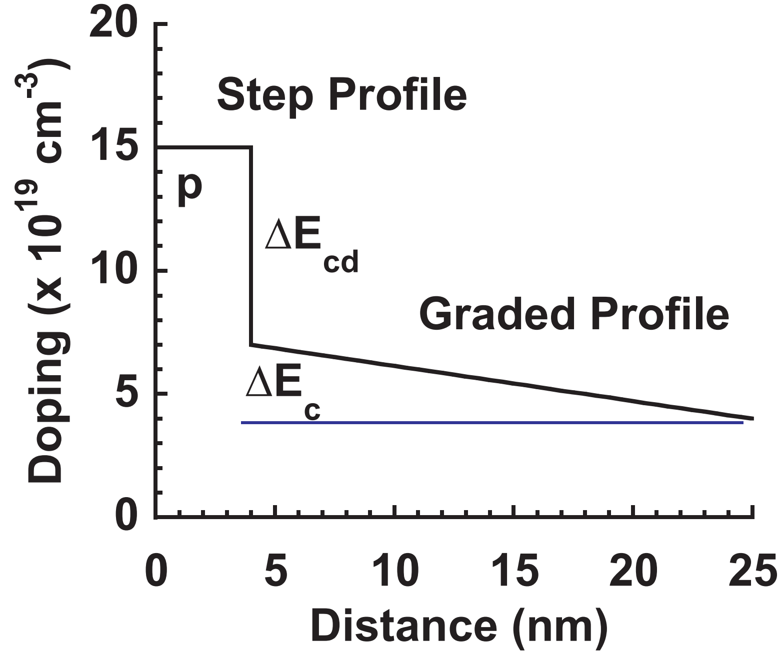


Figure 2.7: Doping profile of a suggested base design having a highly doped pulse layer at the emitter-base junction followed by a doping gradient

For such a design, new base transit time is given by

$$\tau_b = \frac{T_b^2}{D_n} \cdot \frac{kT}{\Delta E_c} \left[1 - \frac{kT}{\Delta E_c} \cdot \left(1 - \exp^{-\Delta E_c/kT}\right)\right] + \frac{T_b}{v_{exit}} \cdot \frac{kT}{\Delta E_c} \cdot \left(1 - \exp^{-\Delta E_c/kT}\right) + \frac{T_d}{v_{exit}} + \frac{T_d^2}{2D_n} \tag{2.8}$$

This calculation assumes finite carrier velocity, $v_{th} = v_{exit}$, at $x = T_d$ point where the doping changes from step to graded profile.

$1/\beta$ assuming Auger recombination dominated base current estimated using the relation in Eq.(2.4) is given by

$$\frac{1}{\beta} = \frac{1}{\beta_2} + k_1 p^2 T_d \left(\frac{1}{v_{exit}} + \frac{T_d}{2D_n}\right) \tag{2.9}$$

where $1/\beta_2$ is given by Eq.(2.5) and p is the doping of the thin, highly doped p+++ delta layer.

For a design having $T_d = 5$ nm, $T_b = 20$ nm, $p = 1.5 \times 10^{20} cm^{-3}$ and doping grade $7 - 4 \times 10^{19} cm^{-3}$, transit time is 0.75 psec and β is greater than 20. This design has multiple advantages over the previous designs – low base transit time, acceptable β, low base contact resistivity and low base sheet resistance. HBT device results incorporating a similar base design have been reported in [26].

Auger recombination current in the base can be reduced by decreasing the total base thickness. However, minimum base thickness is limited by contact metal diffusion in the base during device process steps and operation. The diffusive nature of Pd or Pt base contacts limits the base thickness to $\sim$ 25 nm. Thinner base design also leads to higher base contact resistivity [6, 27]. It was shown by Baraskar et al. [28–30] that very low contact resistivity to the base can be achieved by using refractory, non-diffusive metals like Mo, W and Ir as contacts to highly doped p-InGaAs layer – doping greater than 1.5×10^{20} cm^{-3}. These contacts can be incorporated on the step and grade base design having a highly doped delta layer. Since refractory contacts do not diffuse under device operation or processing, the base layer can be thinned to improve device current gain in addition to device f_τ and f_{max}. For example, given $T_d = 4$ nm, $T_b = 16$ nm, $p = 1.5 \times 10^{20} cm^{-3}$ and doping grade $7 - 4 \times 10^{19} cm^{-3}$, β is $\sim$ 28.

Although, for all the calculations discussed in this section, it has been assumed that τ_{Auger} varies as $1/N_A^2$, experimental data suggests that τ_{Auger} drops faster than $1/(N_A^2)$ at high doping and is approximately proportional to $1/(N_A^3)$ [31]. As a result, $\beta \propto R_{sh}^2/N_A$ and even if the base sheet resistance is kept constant through reduced thickness as doping increases, a reduction in β is expected.

For the devices reported in this thesis, measured β reduces with emitter width for the same emitter length and emitter-base gap as shown in Table 2.1. This shows that in the current design β is limited by surface recombination and not Auger recombination. Hence, it is possible to increase base doping in future designs before the gain becomes Auger recombination limited. It should also be noted that all the calculations are done assuming $k_1 = 8.1 \times 10^{-29} cm^6/s$. This number could change depending on the material growth quality for MBE grown InGaAs and would change the estimated Auger limited device β.

Emitter Width (nm)	**Current Gain β**
270	19
220	17
170	14
120	13

Table 2.1: Reduction in HBT common emitter current gain (β) with emitter width for same emitter-base gap and emitter length. $L_e = 3.5\mu m$, base doping $= 9 - 5 \times 10^{19} cm^{-3}$, base thickness = 30 nm.

2.2.3 Base Access Resistance and Collector - Base Capacitance

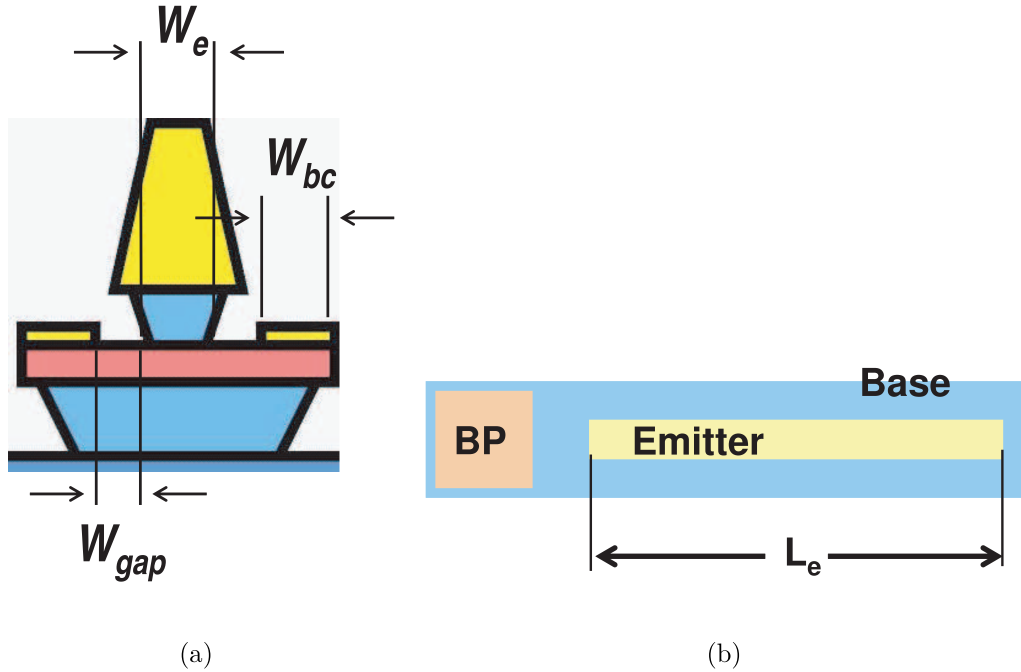
Base access resistance R_{bb} and collector-base capacitance C_{cb} are crucial in determining the device f_{max}. R_{bb} is the sum of the base contact resistance $R_{b,cont}$, gap resistance between the emitter semiconductor and the base contact R_{gap}, base spreading resistance below the emitter $R_{sp,em}$, base spreading resistance below the base contact $R_{sp,base}$ and base metal resistance R_{metal}. The expressions for all these terms are given below

$$R_{b,cont} = \frac{\rho_{b,cont}}{A_{base,contact}}, \qquad R_{gap} = \frac{R_{sh,gap} \cdot W_{gap}}{2L_e}$$
$$R_{sp,em} = \frac{R_{sh,em} \cdot W_e}{12L_e}, \qquad R_{sp,base} = \frac{R_{sh,base} \cdot W_{bc}}{6L_e}$$
$$R_{metal} = \frac{R_{sh,metal} \cdot L_e}{6W_{bc}}$$

where L_e and W_e are emitter length and width respectively; W_{bc} is the base contact width (Fig. 2.8); $\rho_{b,cont}$ is the base contact resistivity, $R_{sh,metal}$ is the base metal sheet resistance; $R_{sh,em}$, $R_{sh,base}$ and $R_{sh,gap}$ are the base sheet resistance below the emitter, below the base contact and in the emitter-base gap. These equations assume that base contact width (W_{bc}) is less than $2 \times L_T$ where L_T is the transfer length in the base given by $\sqrt{\rho_{b,cont}/R_{sh,base}}$. If W_{bc} is greater than $2 \times L_T$, then

$R_{sp,base} + R_{b,cont}$ is given by

$$R_{b,cont} + R_{sp,base} = \frac{1}{2}\left[\frac{\sqrt{\rho_{b,cont} \cdot R_{sh,base}}}{L_e} \cdot coth\left(\frac{W_{bc}}{L_T}\right)\right] \tag{2.10}$$



(a) (b)

Figure 2.8: Cross-section and top view of a mesa DHBT

Base contact resistance is most important in determining f_{max} as it charges the entire collector base capacitance C_{cb}. Surface preparation techniques to achieve low contact resistivity will be discussed in next chapter. Due to processing damage and surface depletion, $R_{sh,gap}$ is often significantly higher than $R_{sh,em}$ or $R_{sh,base}$. Surface depletion effects can be quite significant due to Fermi level pinning 0.2 eV below the conduction band in InGaAs [32–34]. For base layer doped at $7 \times 10^{19}\ cm^{-3}$ surface depletion is roughly 3.8 nm, thereby increasing the sheet

resistance by about 20% for a 25 nm base. This effect becomes less dominant for higher base doping but gets very significant for reduced base thickness. As a result, if the emitter semiconductor-base metal gap is wide, the gap resistance term starts dominating the base access resistance and lowers device f_{max}. It is therefore necessary to keep W_{gap} small for improved device performance.

Consider a 30 nm thick base, doped at $9-5\times10^{19}$ cm^{-3}, typical intrinsic and extrinsic sheet resistances are 660 Ω/sq and 900 Ω/sq. For 200 nm W_e, 300 nm W_b and 50 nm W_{gap} and contact resistivity of 4 $\Omega\cdot\mu m^2$, $R_{b,cont}+R_{sp,base}$ = 25.7 $\Omega\cdot\mu m$, $R_{sp,em}$ = 11 $\Omega\cdot\mu m$ and R_{gap} = 22.5 $\Omega\cdot\mu m$. This shows that R_{gap} contributes 38% to total base access resistance for W_{gap} = 50 nm which is a significant fraction. This becomes more prominent as the contact resistivity is reduced with improved surface preparations and metal choice. W_{gap} therefore has to be reduced for desired improvement in device performance. If W_{gap} reduces to 10 nm, relative contribution of R_{gap} to total R_{bb} reduces to 11% assuming all other values stay constant.

Base sheet resistances can be reduced by using a thicker base layer which increases τ_b. Base layer thickness should therefore be decided depending on the desired HBT performance, high f_τ or high f_{max}.

Base contact resistance and sheet resistances are measured using pinched and non-pinched base TLM structures. In non-pinched base TLMs the gap between

the metal base contacts is exposed to air, increasing the sheet resistivity due to surface depletion and/or processing as discussed earlier. In pinched TLMs, the gap is protected by the emitter layer. Details of extracting the contact resistance from these structures are given in [35].

Collector-base capacitance C_{cb} consists of four components - capacitance below the base contact $C_{cb,ex}$, capacitance due to base-emitter gap $C_{cb,gap}$, capacitance below the emitter $C_{cb,int}$ and capacitance from below the base post $C_{cb,post}$. Total C_{cb} is given by

$$C_{cb} = \frac{\epsilon_0 \epsilon_r L_e}{T_c} \cdot (2W_b + 2W_{gap} + W_e) + \frac{\epsilon_0 \epsilon_r A_{post}}{T_c} \tag{2.11}$$

where A_{post} is the area below the base post contributing to C_{cb}. C_{cb} can be reduced by proper device scaling - reducing the emitter and base junction widths. However, W_{gap} does not scale with device dimensions and needs to be reduced for lower C_{cb}. $C_{cb,post}$ can be minimized by etching the base-collector semiconductor from below the base post as will be shown in Chap. 4.

2.3 Collector Design

The base-collector region consists of InGaAs setback, InGaAs/InAlAs grade and InP pulse doped layers. The design should be such as to create a smooth conduction band profile with suppressed barriers at the hetero-interfaces. The

InGaAs base to InP collector grade is implemented using a chirped-superlattice or sub-monolayer InGaAs/InAlAs grade which smooths out the conduction band discontinuity ΔE_c between InGaAs and InP [36–39]. A quasi electric field is formed across the grade which is countered by inserting an n-doped InP pulse layer on the collector side of the grade. To ensure electrons traverse through the grade and are not reflected, kinetic energy is supplied to them over the n-InGaAs setback region. The design of all these layers to ensure no current blocking and high electron velocity is given in details in [35] and is not repeated here. In this section, collector doping considerations, collector transit time and velocity extraction method and collector current spreading are discussed.

2.3.1 Collector Doping

Doping in the drift collector is usually decided such that the collector is fully depleted at a given minimum V_{cb} for zero current. This minimizes the change in device C_{cb} with collector-base bias for the range of applied biases. The value of V_{cb} is based on the desired application of the HBTs. Higher doping in the collector is desired for higher Kirk limit, however, empirical data suggests that increase in doping for the same collector thickness reduces the device breakdown voltage which is a big trade-off. Reduction in breakdown voltage is believed to be due to higher electric field in the InP drift collector for higher doping. Collector current

spreading generally results in a Kirk limit higher than the designed value. This will be discussed in further detail later.

2.3.2 Collector Transit Time and Carrier Velocity

Transit time of the charge carriers across the collector (τ_c) can be estimated from the charge control analysis of the base collector junction. For a p+ base, a n- collector and a n+ sub-collector device structure, electrons injected from the base into the collector create a displacement current across the junction. From the charge control model, this delay is given by the change in induced base charge on the collector side of the base (δQ_{base}) with collector current δI_c. Thus,

$$\tau_c = \int_0^{T_c} \frac{1 - x/T_c}{v(x)}\, dx \;\equiv \frac{T_c}{2v_{eff}} \tag{2.12}$$

where T_c is the collector thickness and $v(x)$ and v_{eff} are the position-dependent and effective electron velocities in the collector. As electrons traverse through the collector, they experience ballistic transport and gain energy. When this energy exceeds the $\Gamma - L$ energy separation, they scatter into the L-valley having lower electron velocity. Because of the large energy separation between the $\Gamma - L$ conduction band valleys (0.55 eV for $In_{0.53}Ga_{0.47}As$, 0.6 eV for InP), electrons are able to traverse a significant fraction of the collector before attaining sufficient kinetic energy to cause scattering to the higher effective mass, lower velocity L-valley [40, 41].

The emitter-collector delay expression is given by

$$\tau_{ec} = \tau_b + \tau_c + (R_{ex} + R_c) \cdot C_{cb} + \frac{NkT}{qI_c} \cdot (C_{je} + C_{cb}) \tag{2.13}$$

where τ_b and τ_c are the base and collector transit delays. τ_{ec} is computed from device f_τ ($\tau_{ec} = 1/(2\pi f_\tau)$) at a given bias I_c; R_{ex}, C_{cb} and voltage partitioning factor N are computed from low frequency Y-parameter data and R_c from collector TLM measurements and device geometry. Transit delays are generally calculated from a plot of τ_{ec} vs $1/I_c$ which assumes a constant transit delay with bias. However, due to collector velocity modulation effects [42–44], τ_c is not constant and varies with V_{cb} and I_c. As a result, the variation of τ_{ec} with $1/I_c$ deviates from a linear relationship as shown in Fig. 2.9. A method for extracting collector velocity was proposed by Miguel Urteaga, Teledyne Scientific and is used here for velocity extraction.

At low current densities, $< 2\ mA/\mu m^2$, it is assumed that there is no modulation of collector transit time with current. Consequently, τ_c is constant at low I_c, and the rate of variation of τ_{ec} with $1/I_c$ plot at low I_c gives the correct value of $(NkT/q) \cdot (C_{je} + C_{cb})$. Extending this low I_c linear variation of τ_{ec} to higher I_c, and comparing with the measured τ_{ec} value, the difference is due to the reduction in τ_c with I_c because of the velocity modulation effect ($\partial\tau_{ec}/\partial I_c$). This difference is then subtracted from the low I_c intercept, to determine the actual intercept $\tau_b + \tau_c + (R_{ex} + R_c) \cdot C_{cb}$ at a given I_c. Transit delays ($\tau_b + \tau_c$) can be obtained

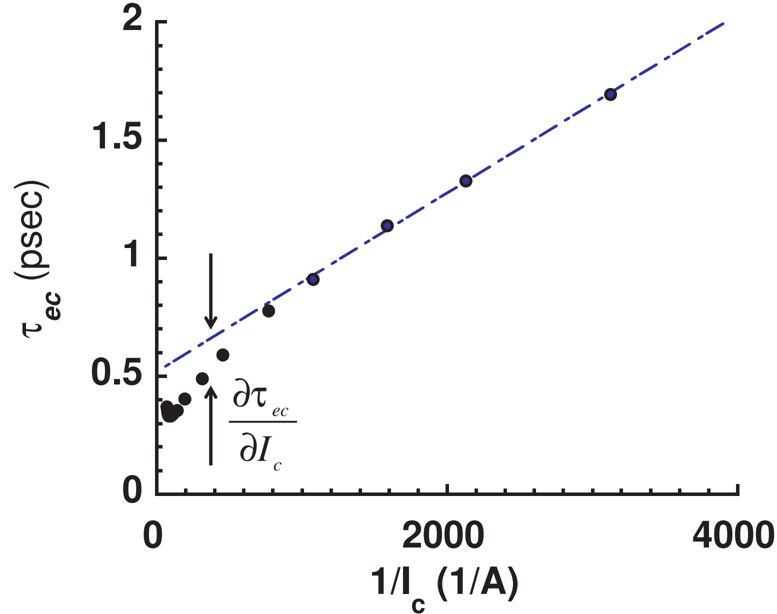


Figure 2.9: A plot of τ_{ec} calculated from measured device f_τ as a function of inverse collector current $1/I_c$

from the intercept by subtracting the $(R_{ex} + R_c) \cdot C_{cb}$ term. Base transit delay obtained using equations mentioned in the previous section can be subtracted from the total transit delay to obtain the collector transit time. Effective collector velocity is then simply $v_{eff} = T_c/(2\tau_c)$ where T_c is the collector thickness.

Collector velocity extraction is an effective way of determining the design quality of base-collector grade. For example, the extracted collector velocity of one HBT sample reported in this thesis, DHBT49, is 2.1×10^7 cm/s which is much lower than the expected value $3 - 3.5 \times 10^7$ cm/s. This is probably due to a faulty (too thin and high doping) base-collector setback and grade design. Improved

designs (DHBT56) having the same collector thickness of 100 nm, show a much higher velocity of 3.1×10^7 cm/s.

2.3.3 Collector Current Spreading

The current density at the onset of Kirk effect for a HBT is given by

$$J_{Kirk} = \frac{2\epsilon_0\epsilon_r v_{eff}}{T_c^2}(\phi_{bi} + V_{cb}) + qN_c v_{eff} \tag{2.14}$$

where ϕ_{bi}, the built-in potential, is approximately the base bandgap potential difference, V_{cb} is the applied potential difference across the base-collector junction and N_c is the collector doping. This assumes no lateral spreading of the current flux or electric field. However, J_{Kirk} measured in the DHBTs is much higher than that expected from Eq. (2.14). This is due to current spreading in the collector as discussed in [45, 46]. As a result of current spreading, reduction in emitter width increases J_{Kirk} for the same collector thickness. This reduces the C/I delays, an important parameter for digital logic applications.

Emitter Width (nm)	**Calculated** $J_{Kirk}(mA/\mu m^2)$
No spread	15
270	21
220	24
170	26
120	29

Table 2.2: Increase in Kirk current with reduction in emitter width for 100 nm collector at $V_{cb} = 0.7$ V

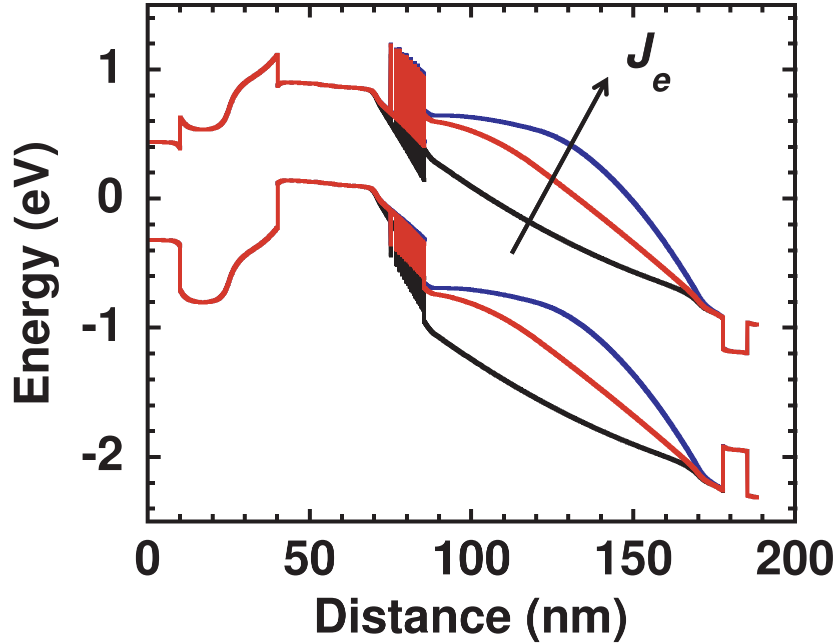


Figure 2.10: Simulated band structure of DHBT53 for $J_e = 0$, $0.5 \times J_{Kirk}$ and J_{Kirk} at $V_{be} = 1\ V$, $V_{cb} = 0.7\ V$. Current spreading was assumed in the collector for 220 nm wide emitter-base junction

Empirical fits to J_{Kirk} measured on HBTs as a function of W_e indicate current spreading in the collector is approximately T_c on either side of the emitter stripe i.e. current can be approximated to flow in a trapezoidal cross-section in the collector [45]. As the emitter length is much longer than the width or T_c, current spreading along the length can be neglected. For a 100 nm collector, current spreading is treated in the following way across the collector from base to subcollector: from x = 0 to $T_c/3$ no spreading; from x = $T_c/3$ to $2T_c/3$, spreading is $T_c/3$ on either side of the emitter, and from $2T_c/3$ to T_c, $2T_c/3$ of spreading on each side. For calculating J_{Kirk}, the electron velocity in the collector is treated as

a two step profile [40, 46, 47]. For the first half of the collector, velocity is assumed to be 4.5×10^7 cm/s and for the second half it is 1.5×10^7 cm/s. Fig. 2.10 shows the HBT band profile at $J_e = 0$, $0.5 \times J_{Kirk}$ and J_{Kirk} for a 100 nm collector and 220 nm wide emitter-base junction. Table 2.2 shows the calculated J_{Kirk} for DHBT53 design assuming no current spreading and the measured J_{Kirk} for different emitter widths and same emitter length (3.5 μm) at $V_{cb} = 0.7$ V.

2.3.4 Collector Resistance

Collector access resistance R_c is smaller in value than emitter and base resistances discussed so far due to large contact pads. Thus, collector contact resistance $R_{cc} = \rho_{cc}/A_c$ is much smaller than emitter access resistance where ρ_{cc} is the collector contact resistivity. However, processing damages can result in significant increase in ρ_{cc} adversely effecting device f_τ. ρ_{cc} can be reduced by using a thin highly doped InGaAs layer for making contacts. A 7.5 nm thick InGaAs layer doped at 4×10^{19} cm^{-3} gives low contact resistivity. Thinning the InGaAs layer further, increases contact resistivity presumably due to contact metal diffusion into the InP layer. Thinning the InGaAs layer from 7.5 nm to 5 nm at constant doping increased the measured collector contact resistivity from 6 $\Omega \cdot \mu m^2$ to 22 $\Omega \cdot \mu m^2$. Thick InGaAs layer however increases device thermal resistance. Doping is not increased beyond this value as it might create growth defects. A

300 nm thick InP sub-collector doped at 1×10^{19} cm^{-3} is used to reduce the sheet resistance. Non-pinched collector TLMs are used to extract ρ_{cc} and sheet resistance. Surface depletion is ignored due to thick sub-collector layer.

2.4 HBT Figures of Merit

HBT common-emitter unity current gain cut-off frequency f_τ is given by

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + (R_{ex} + R_c) \cdot C_{cb} + \frac{NkT}{qI_c} \cdot (C_{je} + C_{cb}) \tag{2.15}$$

where τ_b and τ_c are base and collector transit delays, C_{cb} and C_{je} are base-collector and base-emitter junction capacitances, R_c and R_{ex} are collector and emitter access resistances and $(NkT/qI_c)^{-1}$ is the device transconductance.

HBT maximum oscillation frequency or unit power gain frequency f_{max} is given by

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi(RC)_{eff}}} \tag{2.16}$$

where $(RC)_{eff}$ is the effective time constant of the base-collector junction [48, 49].

For a high f_{max} device, it is important to minimize R_{bb} and C_{cb} for reduced $(RC)_{eff}$ term. R_{bb} can be reduced through better contacts and junction size scaling which also reduces C_{cb}. High f_τ can be achieved through reduced transit delays by epitaxially scaling the device base and collector layer thickness which reduces the f_{max} through increased C_{cb}.

2.5 Hybrid-π Equivalent Circuit

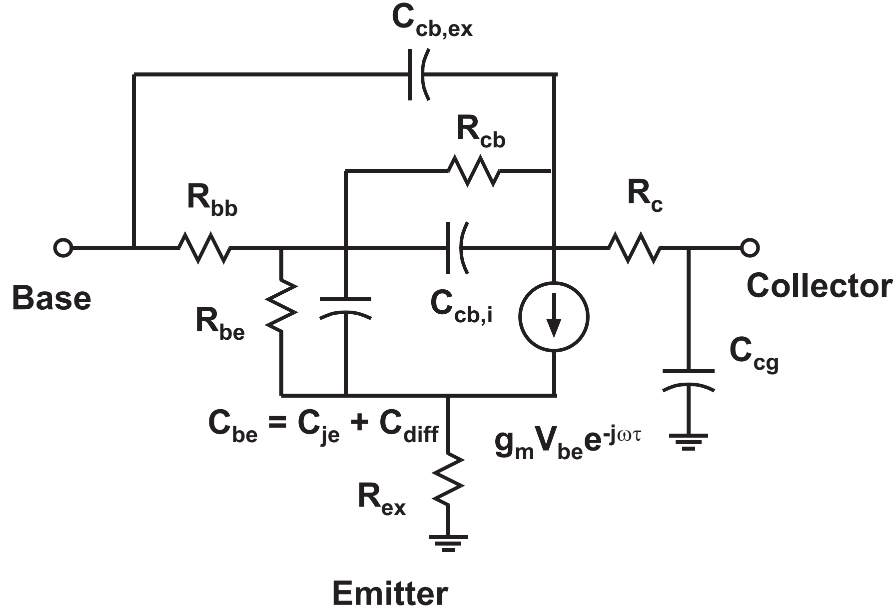


Figure 2.11: Small signal hybrid-π equivalent circuit for a DHBT

Fig. 2.11 shows the small signal hybrid-π equivalent circuit for a HBT [50]. The various components of the equivalent circuit can be extracted from TLM measurements and S-parameter measurements [35].

R_{ex} is extracted from low frequency Y_{21} data (2-5 GHz) from the equation below

$$\frac{1}{Re(Y_{21})} = R_{ex} + \frac{R_{bb}}{\beta} + \frac{NkT}{qI_c} \tag{2.17}$$

From a plot of 1/Re(Y_{21}) vs $1/I_c$, $R_{ex} + R_{bb}/\beta$ can be obtained from the intercept and N from slope. It is assumed that R_{ex}, R_{bb}, β and N stay constant with

bias which may not be correct (Fig. 2.12) due to degeneracy effects (discussed in Chap. 5), variation in β or junction temperature rise.

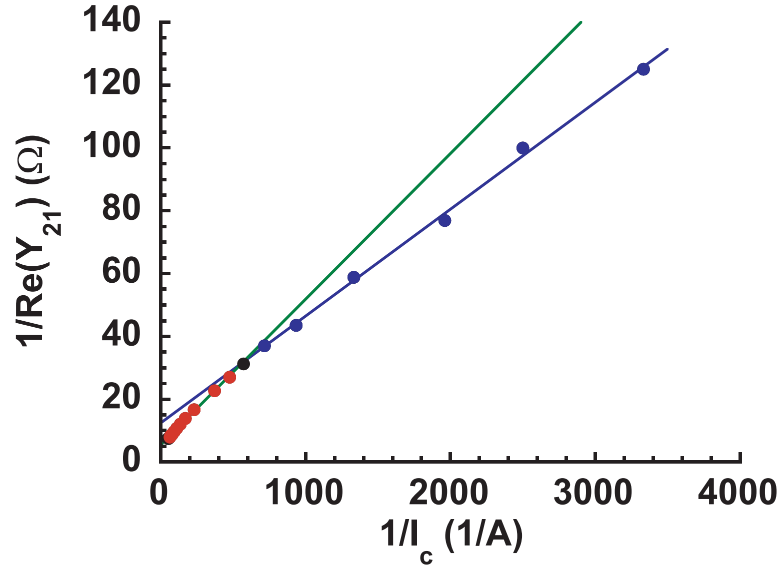


Figure 2.12: A plot of measured $1/Re(Y_{21})$ vs $1/I_c$ showing a deviation from the linear relationship

g_m is obtained by matching the low frequency portion of Re(Y_{21}). A wrong value of R_{ex} in the model will lead to incorrect g_m, hence g_m value in the model must be comparable to NkT/qI_c. R_c is generally small and can be estimated from collector TLM measurements. Total C_{cb} is obtained from Imag(Y_{12}) data where Imag(Y_{12}) $= j\omega(C_{cb,ex} + C_{cb,i})$. C_{je} is estimated from the slope of τ_{ec} vs $1/I_c$ plot. Collector-base resistance R_{cb} can be estimated from low frequency Re(Y_{12}) data where Re(Y_{12}) $= 1/R_{cb} + \omega^2 C_{cb} C_{cb,i} R_{bb}$. Curvature of Re($Y_{12}$) can be fit to obtain an accurate $C_{cb,ex}$ to $C_{cb,i}$ ratio. R_{be} and R_{bb} are estimated from Re(Y_{11}) data from

the relation

$$Re(Y_{11}) = \frac{1}{R_{be}} + \omega^2 C_{be}^2 R_{bb} \quad (2.18)$$

R_{be} is obtained by matching the low frequency portion of Re(Y_{11}) and R_{bb} by matching the curvature of Re(Y_{11}) (second order match). C_{be} is estimated by matching the Imag(Y_{11}) to first order in frequency. Finally, τ_c is obtained by matching Imag(Y_{21}) and C_{cg} by matching Imag(Y_{22}) to first order in frequency.

S-parameter, H_{21} and U plots should also be monitored simultaneously to ensure a good match between the measured data and simulated parameters. A few iterations are required to remove the effect of R_{bb}/β from the R_{ex} data. Fig. 2.13 shows the measured and simulated S-parameter, H_{21} and U data for a DHBT indicating good match between the measured and simulated data.

2.6 HBT Scaling Laws

HBT transit delays and major resistances and capacitances associated with the HBTs were discussed earlier in the chapter. For improvement in device performance, all transit and RC delays need to be reduced. A $\gamma : 1$ improvement in device bandwidth requires $\gamma : 1$ decrease in both transit and RC delays. This is done while keeping the resistances and current constant [1, 3].

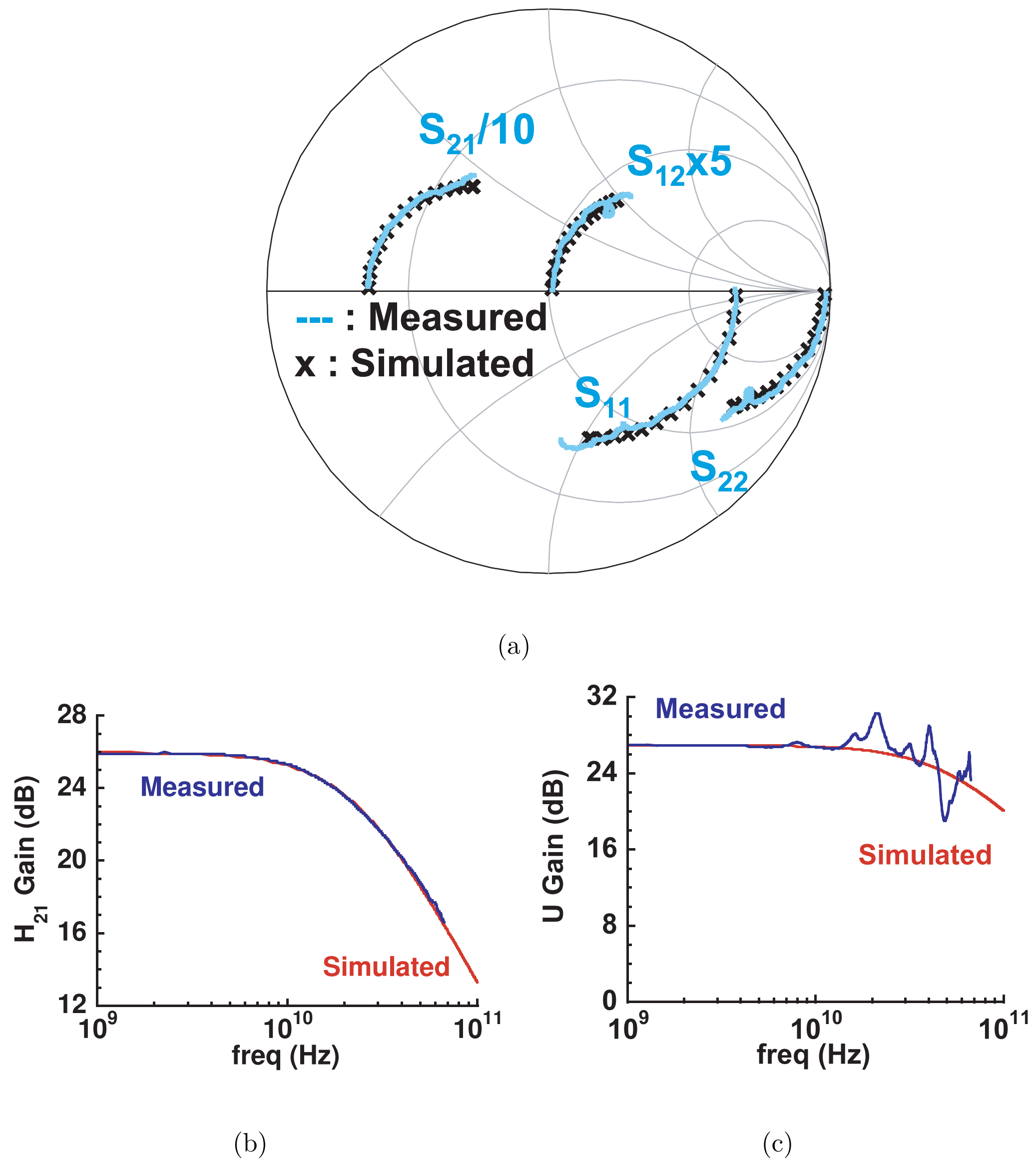


Figure 2.13: Measured and simulated (a) S-parameters, (b) H_{21} and (c) U of the HBT and hybrid-π equivalent circuit

Transit delays are reduced by reducing T_c by $\gamma : 1$ and T_b by $\gamma^{1/2} : 1$. Reducing T_c by $\gamma : 1$ increases C_{cb} per unit area in the same proportion. The base-collector mesa junction area must be reduced in proportion to $\gamma^2 : 1$ for desired $\gamma : 1$ reduction in C_{cb}. This is generally done by reducing the base-collector width that is emitter and base contact widths by $\gamma^2 : 1$ keeping the length constant due to thermal constraints. The area below the base post, A_{post}, should also be scaled for C_{cb} reduction. Emitter junction capacitance C_{je} also gets reduced by $\gamma^2 : 1$ due to width reduction. That means the emitter space charge region depth can be reduced by $\gamma : 1$ for desired $\gamma : 1$ reduction in C_{je}. Reduction in emitter space charge region depth alongwith increase in emitter doping is necessary to sustain high emitter current density without source starvation problems [3, 51]. T_c reduction also increases the Kirk current density J_{kirk} by $\gamma^2 : 1$ for constant I_c.

Base sheet resistance value increases by $\gamma^{1/2} : 1$ but the spreading resistance terms below the emitter and base contacts reduce due to junction width scaling. Sheet resistance increase in the emitter-base gap is more pronounced due to surface depletion and R_{gap} increases unless W_{gap} is also scaled. Reduction in W_b by $\gamma^2 : 1$ necessitates a $\gamma^2 : 1$ reduction in base contact resistivity $\rho_{b,cont}$ to keep base contact resistance constant.

Emitter access resistivity ρ_{ex} also needs to be reduced by $\gamma^2 : 1$ for constant R_{ex}. g_m stays constant for constant I_c and N. However, as will be shown later

in Chap. 5, g_m decreases due to degeneracy effects associated with InP emitter at high J_e [51]. Table 2.3 summarizes the scaling laws.

Device parameter)	**Required change**
Collector thickness	decrease $\gamma : 1$
Base thickness	decrease $\gamma^{1/2} : 1$
Base-emitter junction width	decrease $\gamma^2 : 1$
Base-collector junction width	decrease $\gamma^2 : 1$
Emitter current density	increase $\gamma^2 : 1$
Emitter access resistivity	decrease $\gamma^2 : 1$
Base contact resistivity	decrease $\gamma^2 : 1$

Table 2.3: Summary of parameter scaling requirements for a $\gamma : 1$ increase in HBT bandwidth keeping resistance and current constant

For Auger limited minority carrier lifetime, assuming τ_{recomb} is proportional to $1/N_A^3$ for very high base doping, to keep constant β with scaling, base doping needs to be increased in proportion to $\gamma^{1/3} : 1$ assuming electron mobility remains the same. If this scaling strategy is employed, then base sheet resistance value increases by only $\gamma^{1/6} : 1$ as opposed to $\gamma^{1/2} : 1$ resulting in lower base access resistance.

Junction temperature rise due to device self heating must be minimized for scaled devices. Approximating heat flow as half-cylindrical at radii $r < L_e/2$ and as hemispherical at greater distances, the junction temperature rise of an isolated HBT on a thick substrate is [1]

$$\Delta T = \frac{P}{\pi K_{InP} L_e} \ln(\frac{L_e}{W_e}) + \frac{P}{\pi K_{InP} L_e} \qquad (2.19)$$

where K_{InP} is the thermal conductivity of the substrate and P is the dissipated power. Reduction in emitter and base junction area by $\gamma^2 : 1$ can be achieved by reducing both L_e and W_e by $\gamma : 1$. However, due to the inverse relation between ΔT and L_e, ΔT would then rise by $\gamma : 1$ for each scaling generation. Hence, its preferable to reduce W_e by $\gamma^2 : 1$ keeping L_e constant.

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Chapter 3

HBT Process Improvements

In the previous chapter, various aspects of device design including lateral and vertical scaling to simultaneously improve f_τ and f_{max} were discussed. To ensure proper device scaling, its imperative to have a robust, reliable and scalable process flow with sufficient device yield. In this chapter, several process and design improvements to enable a scalable, reliable process especially for emitter are discussed. A new process flow for the base to incorporate low resistivity, refractory base contacts is also reported. Contact resistivity is a serious limitation to DHBT scaling and performance improvement and efforts to improve contact resistivity are also discussed.

3.1 Emitter Process Improvements

3.1.1 Emitter Contacts

Ti based contacts for n-InGaAs emitters have traditionally been used to achieve low contact resistivity due to its excellent oxygen gettering properties which getters (reduces) the semiconductor oxides at the surface. However, Ti has a tendency to diffuse into the semiconductor under thermal and electrical stress and as a result Ti based contacts are not suitable for high current density operation for long periods [1–3]. With device scaling, operational current density is expected to increase and at 128 nm emitter-base junction width, the emitter is operating at current density $J_e > 30\ mA/\mu m^2$ [4, 5]. Thus it is important to have a refractory, non-diffusive metal for emitter contacts to improve metal-semiconductor junction reliability [1].

Ex-situ TiW (10% Ti by weight) refractory sputtered contacts were initially studied for obtaining low contact resistivity using UV-O_3 oxidation and concentrated NH_4OH dip for oxide removal [6]. However, the same low contact resistivity numbers could not be repeated and detailed study showed faults in the design of the TLM (Transmission Line Models) pad structures. It was also observed from XPS study of NH_4OH dipped n-InGaAs samples that NH_4OH dip is not sufficient to remove surface oxides formed as a result of UV-O_3 oxidation. Even for

n-InGaAs samples doped at $> 5 \times 10^{19}$ cm^{-3}, contact resistivity of lower than $4\ \Omega \cdot \mu m^2$ could not be achieved for TiW contacts. Dilute HCl (1:10 HCl:DI) dip and subsequent DI rinse was found to be a much more effective way of removing surface oxides [7]. Sputtered TiW contacts were made to n-InGaAs using UV-O_3 oxidation and dilute HCl dip surface preparation. Inspite of effective oxide removal, the obtained contact resistivity was still $\sim 4\ \Omega \cdot \mu m^2$ [8]. It is believed that the Ar plasma used during sputter deposition damages the surface, increasing the contact resistance [9]. Fig. 3.1 shows a plot of measured contact resistivity of TiW contacts to n-InGaAs using different surface preparations at same doping. Contact resistivity was also found to be a very strong function of semiconductor doping and rises rapidly at lower doping. Thus highest possible doping is preferred for emitter contacts.

Further reduction in contact resistivity required cleaner semiconductor surfaces. A metal e-beam evaporator system was attached to the MBE system at UCSB by the MBE team for depositing *in-situ* metals on the semiconductor surface immediately after growth, without exposing the wafer to atmosphere. It is believed that this would form the best metal-semiconductor interface with minimum defects and lowest contact resistivity. So highly doped n-InGaAs layers were grown in the MBE system and *in-situ* refractory contact like Mo was deposited to obtain low contact resistivity. Contact resistivity as low as $1.1\ \Omega \cdot \mu m^2$ has been

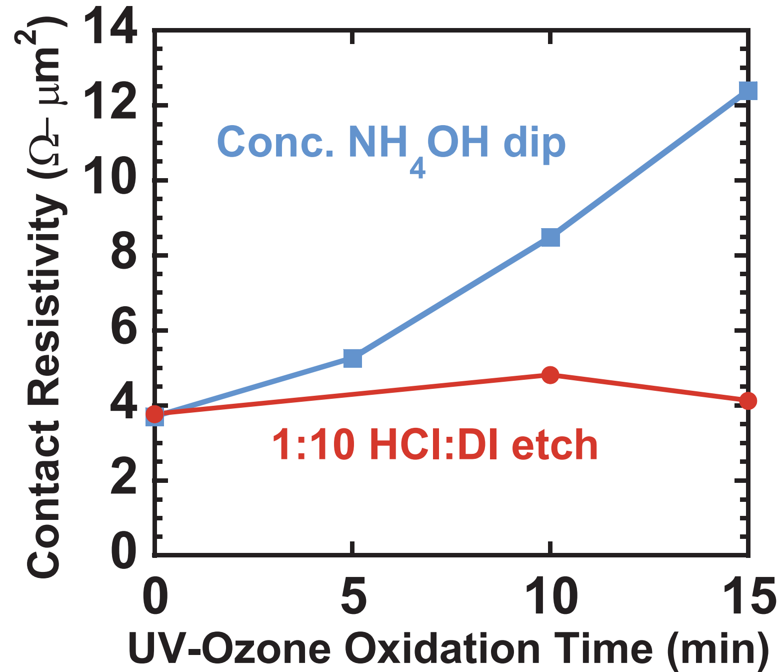


Figure 3.1: Measured contact resistivity of TiW contacts to n-InGaAs for different surface preparations - NH_4OH dip and 1:10 HCl:DI dip as a function of UV-O_3 oxidation time

achieved using *in-situ* Mo contacts to n-InGaAs [10]. Usage of e-beam evaporation system also saves the semiconductor from sputtering damage due to plasma.

Emitter regrowth and *in-situ* contact metal deposition process was first used to achieve low resistivity emitter contacts. IQE grown DHBT wafers had a thin 10 nm InGaAs cap grown on InP emitter. The wafers were first solvent cleaned and oxidized in UV-O_3 for 30 minutes. The oxide was etched for 1 minute in 1:10 HCl:DI solution and DI rinsed for 1 minute. The samples were immediately loaded into MBE system for highly doped n-InGaAs regrowth on the emitter cap.

Inside the MBE system, the wafer surface is cleaned using thermal desorption and H plasma to achieve a clean surface for regrowth. 10 nm of highly doped n-InGaAs $> 5 \times 10^{19}\ cm^{-3}$ doping is regrown and then 20 nm of *in-situ* Mo is deposited. Details of surface cleaning techniques and regrowth procedure are given in [11]. Contact resistivity of $1.1\ \Omega \cdot \mu m^2$ was attained using this process. The biggest advantage of this process is the reliability and repeatability of low contact resistivity obtained.

In a second technique, quasi *in-situ* contacts were formed for the emitter. The surface cleaning procedures are same as discussed above but in this case there was no regrown InGaAs cap. Mo contacts were deposited directly on IQE grown emitter cap after surface cleaning in the MBE system. Similar contact resistivity of $1.1\ \Omega \cdot \mu m^2$ was attained using this process. As a result the previous technique of regrown emitter and *in-situ* deposition was discontinued.

The third process involved depositing *ex-situ* contacts on the IQE grown emitter cap. In this process, the sample surface was oxidized for 15 minutes in UV-O_3 plasma followed by 10 secs of 1:10 HCl:DI etch and 1 minute DI rinse. The samples were immediately loaded into the e-beam evaporator for Mo deposition. To ensure source cleanliness and to remove any contaminants from the source surface (source degassing), dummy deposition of 20 nm Mo is done prior to contact deposition. Contact resistivity of $1.5\ \Omega \cdot \mu m^2$ was achieved using this process [12]. Since

the contact resistivity value is close to the one for *in-situ* contacts, this process is being used currently for making emitter contacts as it makes the process less demanding and time consuming and independent of UCSB MBE.

Emitter contact resistivity can be improved by using highly doped InAs cap for emitter contacts. However, interface resistance between InAs and InGaAs needs to be estimated first. Grading the emitter cap from InAs to InGaAs appears to be the best option currently. ρ_c can also be lowered by further increasing doping in the emitter cap contact layer.

3.1.2 Emitter Metal Stack

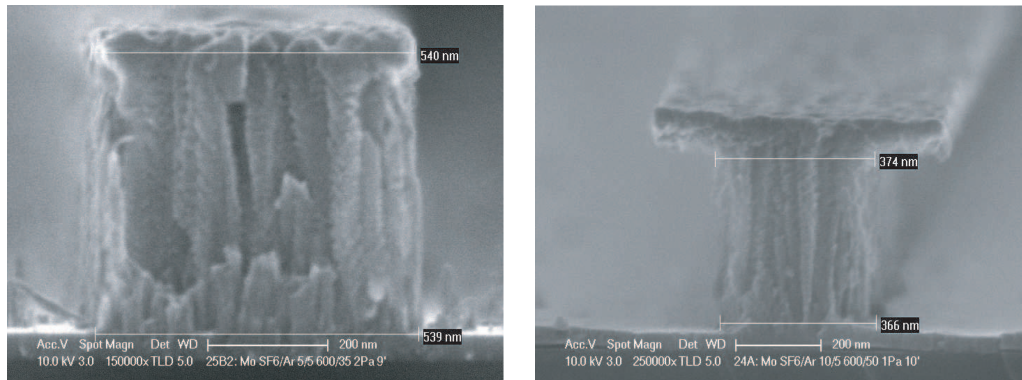
To sustain high operational current density in the emitter, refractory metals are preferred for use in emitter metal stack. Although Au plated emitters are also used in some processes [5], it is believed that with scaling as the current densities increase, Au might suffer from electromigration [13, 14]. Thus the efforts in this work are concentrated on developing a refractory emitter metal stack which can sustain high current density operation and high temperature processing.

Refractory metals used for emitter stack deposition should have the following properties –

- ease of deposition and etch

- vertical etch profile
- low stress
- low bulk resistivity

All the metals investigated - W, Mo and TiW are deposited using Ar-sputtering and then etched in SF_6/Ar chemistry. A vertical etch profile is needed for process scalability and low stress for high device yield. Prior to this work, refractory emitter metal stack development work involving W, Mo and TiW (10% Ti by weight) metals was pursued by Erik Lind and Evan Lobisser [15, 16].



(a) (b)

Figure 3.2: Mo emitters after the dry etch showing a vertical etch profile. Images courtesy: Evan Lobisser

Mo emitters were developed by Evan Lobisser and by optimizing the etch chemistry - SF_6 to Ar ratio and dry etch power, it is possible to obtain a vertical emitter profile as shown in Fig. 3.2. However, the etch is very unstable and not

repeatable. Further Mo etches had problems and it was not possible to repeat the vertical etch profile obtained earlier as shown in Fig. 3.3. Due to the unstable etch, Mo was discontinued as emitter metal. W was tried by Erik Lind as a dry etched emitter metal. However, W is highly reactive in SF_6 gas and tends to undercut greatly. As a result, emitters acquire an hour-glass-shaped structure as shown in Fig. 3.4. TiW etch optimization work was again done by Evan Lobisser but TiW is highly etch resistant and tends to flare at the bottom (Fig. 3.5). As drawn emitters of 100 nm width end up being close to 200 nm after the etch resulting in a non-scalable emitter process.

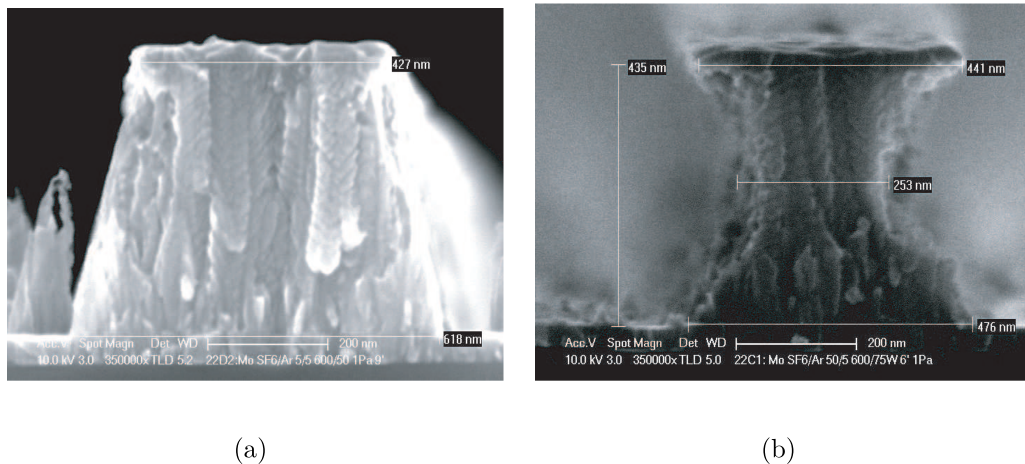
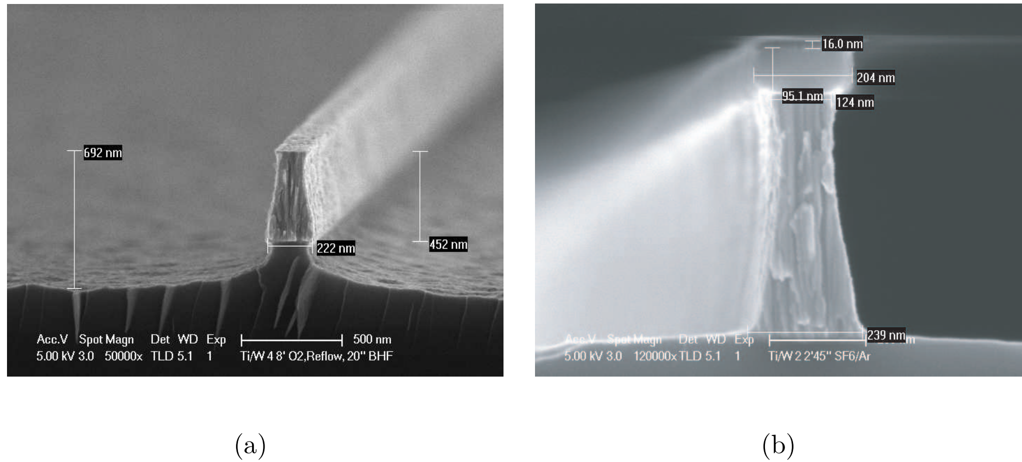


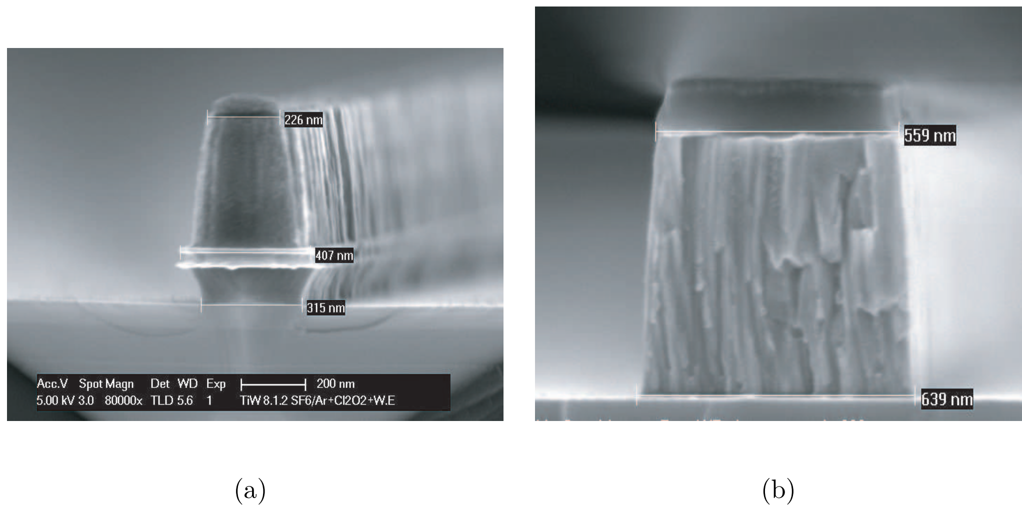
Figure 3.3: Mo emitters after the dry etch showing a flared or an undercut etch profile due to etch variations. Images courtesy: Evan Lobisser

A composite emitter metal stack consisting of 200 nm W at the bottom followed by 300 nm TiW was subsequently developed. W and TiW thickness were chosen so as to minimize the flaring problem of TiW and undercut problem of W. TiW



(a) (b)

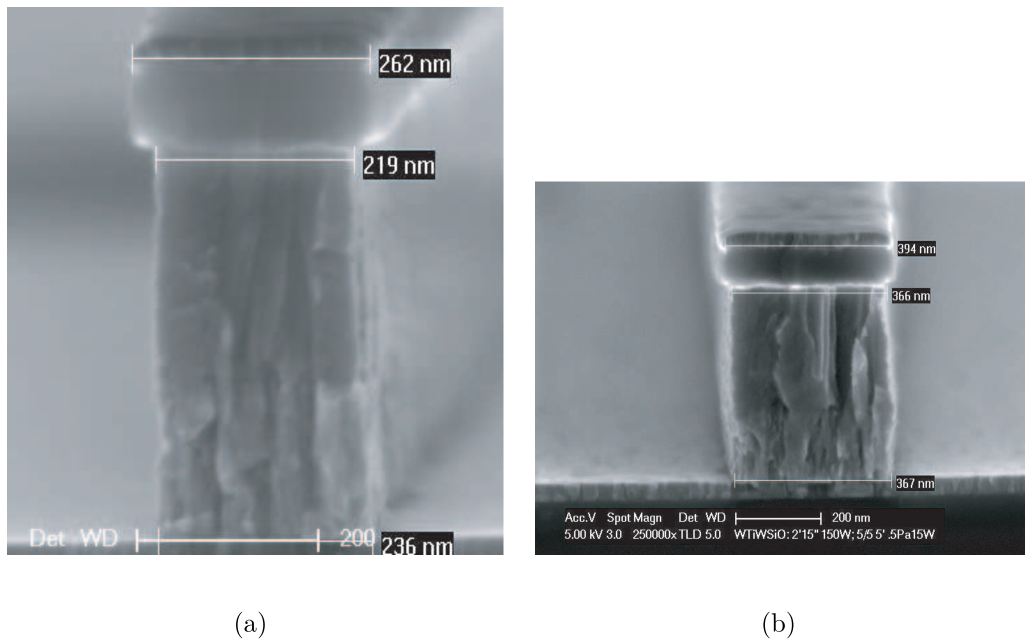
Figure 3.4: W emitters after the dry etch showing an undercut etch profile due to high reactivity of W to SF_6 gas used for the etch. Images courtesy: Erik Lind



(a) (b)

Figure 3.5: TiW emitters after the dry etch showing a flared etch profile due to relative inertness of TiW to SF_6 gas used for the etch. High power plasma is needed to etch TiW. Images courtesy: Erik Lind and Evan Lobisser

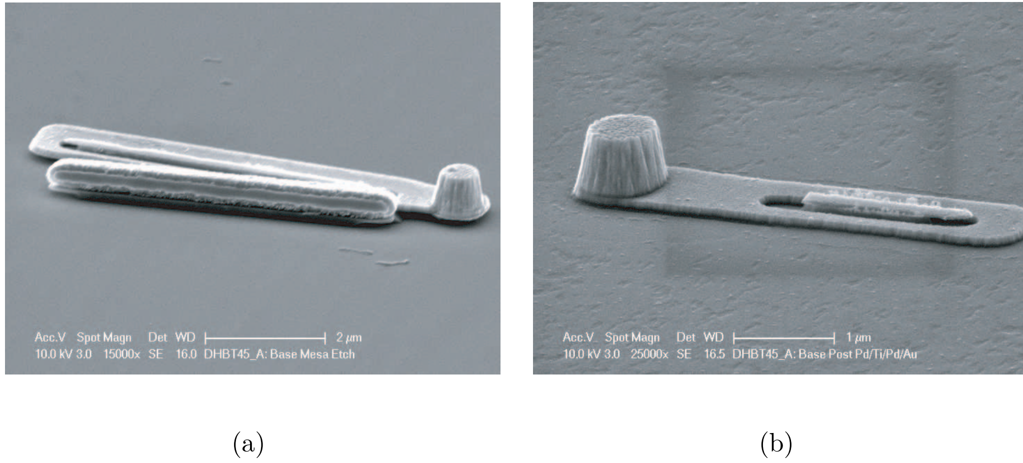
was etched in ICP using high SF_6 to Ar ratio and high etch power with a timed etch to stop in the W layer. Low power ICP etch involving low SF_6 to Ar ratio was then used to etch the remaining W and Mo contacts. The etch has been optimized to obtain an almost vertical profile for the emitter (Fig. 3.6). A vertical emitter profile is desired for self-aligned base lift-off process. The line of sight metal deposition for the base contact prevents any metal deposition on the sides of the emitter for a vertical profile, thereby preventing a short between the emitter and base metals [4, 17, 18].



(a) (b)

Figure 3.6: SEM images of emitter after the etch of composite metal stack consisting of 200 nm W and 300 nm of TiW

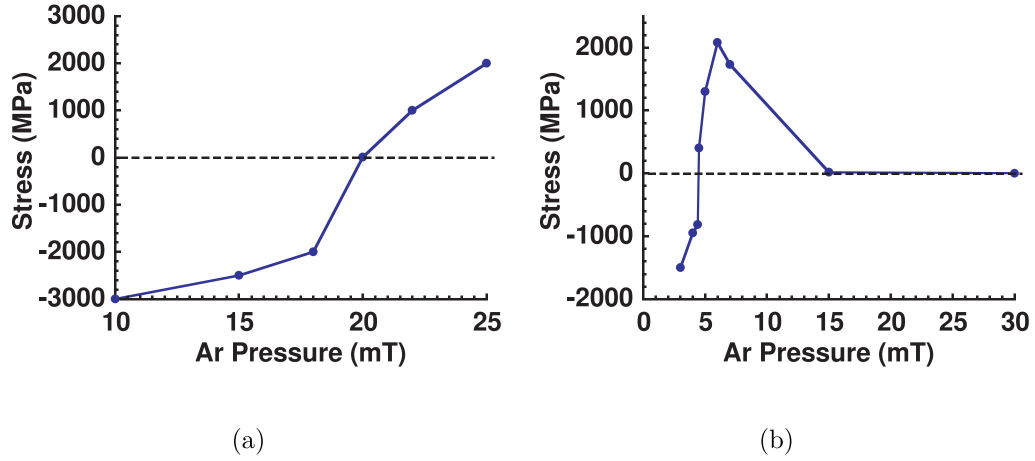
The sputter conditions were optimized to obtain a low stress sputtered film. Low stress sputtered film is needed to improve device yield at narrow emitter



(a) (b)

Figure 3.7: SEM images showing fallen off emitters after the base contact and base post lift-off steps resulting in very low processing yield

widths. Significant drop in emitter yield during various processing steps for sub-200 nm emitters was a major problem with the old process flow. It was observed that the emitters were unstable and would fall off during base contact and base post lift-off steps (Fig. 3.7). This was probably due to high stress in the sputtered film which was detrimental to emitter adhesion to InGaAs cap. As a result, W and TiW film deposition conditions were optimized to give low stress for both the films. The gas pressure for plasma generation in a sputtering system can be optimized for low stress – high pressure results in tensile stress in the film and low pressure compressive stress. At very high pressure, the film has negligible stress due to columnar metal deposition leading to high sheet resistance. There is a small pressure window where both the stress and sheet resistance are low and W/TiW depositions are done in that narrow pressure window. Fig. 3.8 shows



(a)

(b)

Figure 3.8: Variation in measured stress in sputter deposited W film using (a) Sputter #1 and (b) Sputter #4 systems. Sputter #4 characterization work was done by Jeremy Wachter, a REU intern at UCSB nanofab

the variation in stress in 200 nm thick W film deposited using different sputter systems. The pressure window for deposition is not stable and suffers both a short and long term drift. Sheet resistance for the 500 nm thick W/TiW stack is $\sim 0.4\ \Omega/sq$. This is much higher than ideal case and for narrow emitters metal resistance is comparable to contact resistance. Reduction in metal resistance can be achieved by using Au emitters.

3.1.3 Emitter Semiconductor Etch

Prior DHBT designs at UCSB incorporated a thick ($>$ 120 nm) InP emitter to enable a self-aligned base lift-off process where a short circuit between emitter and base metals was avoided by the undercut in the InP emitter during the emitter

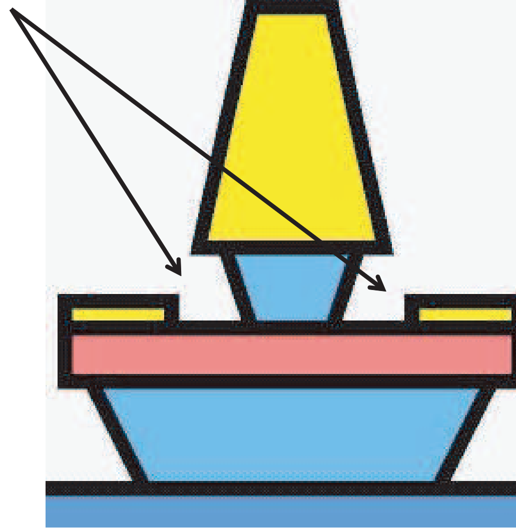
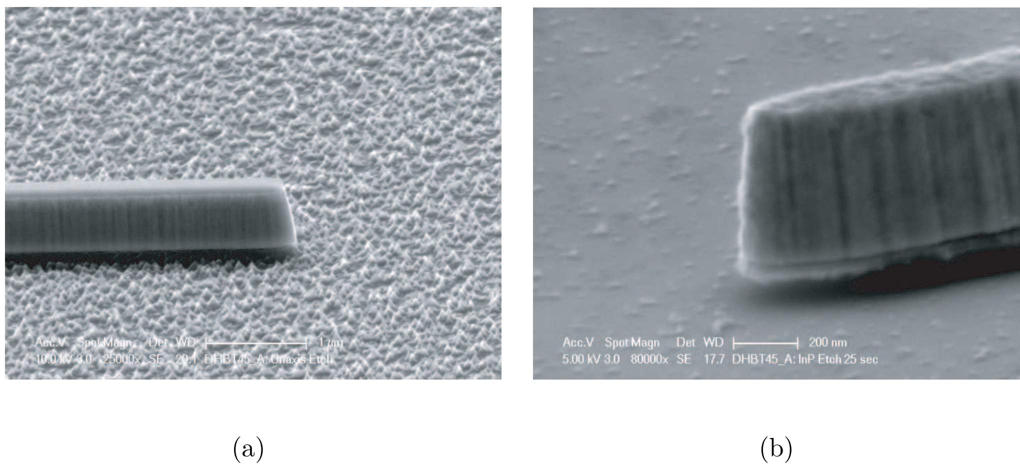


Figure 3.9: Schematic representation of emitter semiconductor undercut after the InP wet etch which provides a physical separation between the emitter and base metals avoiding shorts

wet etch [15, 16]. Thickness of the base metal was purposely kept less than the InP thickness to prevent any short circuit between emitter and base. This is shown schematically in Fig. 3.9 where undercut in the InP emitter creates a physical separation between the base contact metal and emitter metal during a self-aligned lift-off process. For wide emitter junctions, wet etch was employed for the emitter semiconductor [19]. A dry etch process for the emitter semiconductor was developed for sub-300 nm emitter features [16]. In this process, the emitter semiconductor was partially dry etched through the InGaAs cap and most of the InP layer and then remaining InP was wet etched to stop on the InGaAs

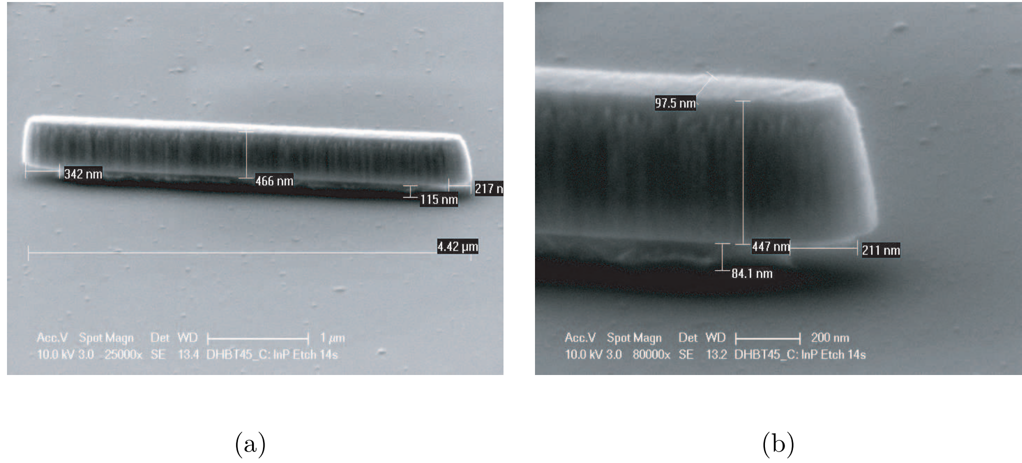
base. This was later changed to a hybrid wet-dry-wet etch process in which the InGaAs cap was wet etched, InP partially dry etched and then remaining InP wet etched [15]. Dry etch was done using a low power Cl_2/Ar chemistry at 200°C chuck temperature. $InCl_2$ formed as a by-product of the etch was removed from the semiconductor surface using a Ar sputter and DI rinse immediately after the etch. There were several issues with the semiconductor dry etch process, prominent amongst them being etch repeatability. Fig. 3.10 shows the semiconductor surface after semiconductor dry etch and subsequent wet etch. The surface after the dry etch is very rough and sometimes the roughness and the dry etch by-products are not removed after the wet etch.



(a) (b)

Figure 3.10: SEM images of the emitter and semiconductor surface after the (a) Unaxis dry etch and subsequent (b) InP wet etch

The wet etch of InP results in excessive undercut in the emitter semiconductor below emitter metal leading to wide gaps between the emitter and base metal

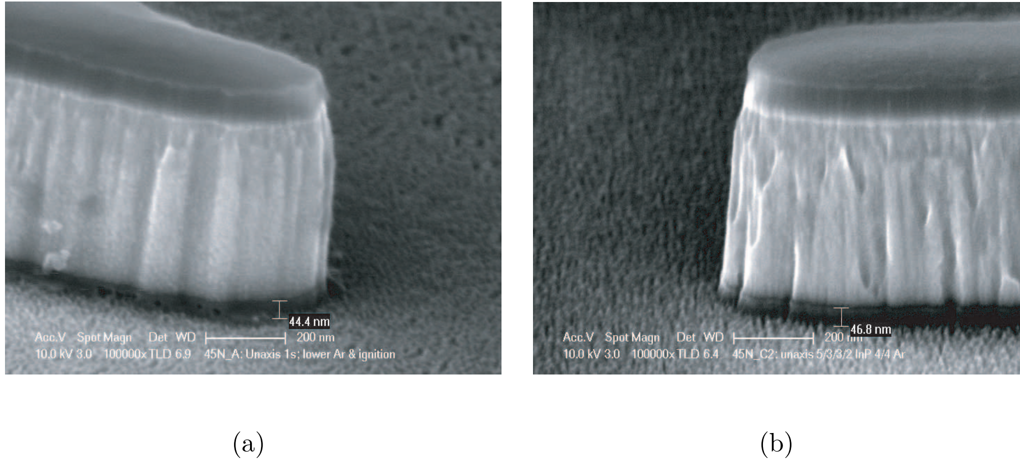


(a) (b)

Figure 3.11: SEM images of the emitter after InP wet etch to stop on the InGaAs base. There is a large undercut below the emitter metal due to thick semiconductor resulting in large emitter base gaps

(Fig. 3.11). This increases the base access resistance through increased W_{gap}. To reduce the undercut, the InP emitter layer needs to be thinned. The Ar sputtering step required to remove $InCl_2$ from the surface also etches 40-70 nm of InP emitter. This limits the minimum thickness of the InP emitter. Although it is possible to etch thin layers of semiconductor as well (Fig. 3.12), the surface cannot be cleaned afterwards by a wet etch.

Due to all the problems with the dry etch process, it was decided to thin the semiconductor down as much as possible and employ a wet-etch only procedure for the emitter semiconductor. With the vertical emitter metal profile, a thin semiconductor is now feasible as undercut in the emitter semiconductor is no longer needed for avoiding the emitter-base short circuit. The all-wet-etch pro-



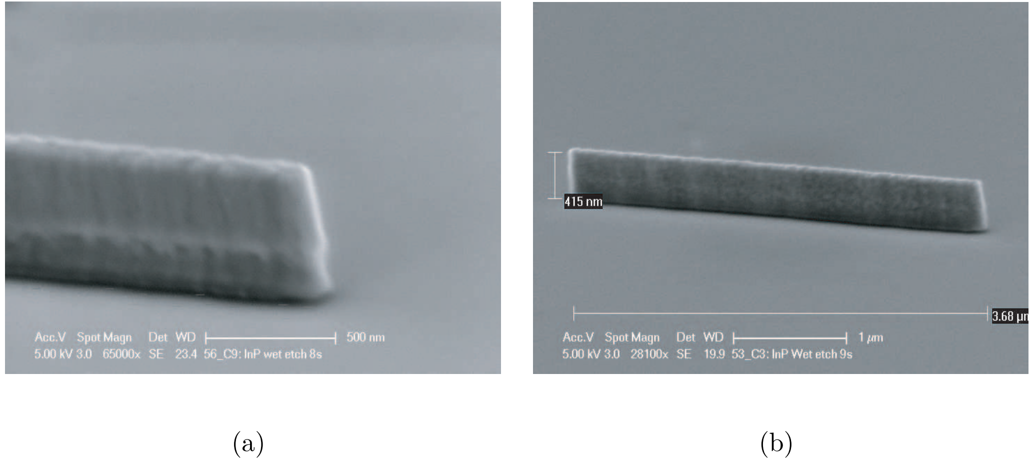
(a) (b)

Figure 3.12: SEM images of the semiconductor after very short Unaxis dry etch depicting less than 50 nm semiconductor dry etch

cess is highly repeatable and uniform across the sample and results in clean base surface for contact deposition. Fig. 3.13 shows the emitter stack and base surface after InP wet etch. Thin semiconductor reduces the emitter undercut resulting in narrow emitter base gap. This reduces the base access resistance and improves device f_{max} [17, 18, 20].

3.1.4 Dual Sidewall Process

To improve yield and to prevent the emitters from falling over during processing, a double SiN_x sidewall process is used to improve mechanical adhesion between the emitter metal and semiconductor [15]. The first sidewall is deposited after the emitter metal etch and in addition to mechanical support, it protects



(a) (b)

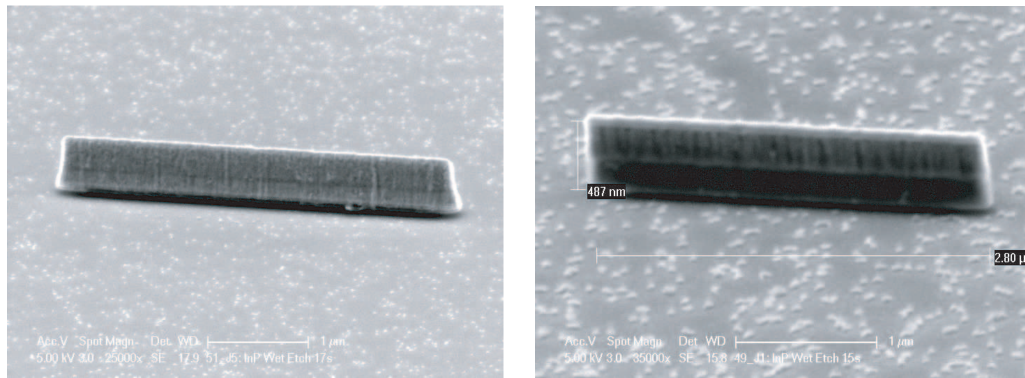
Figure 3.13: Emitters after the thin InP wet etch showing clean uniform base surface

the TiW/W emitter from getting attacked by the BHF etch used to remove Cr cap.

A fraction of the first sidewall is etched away during the Cr cap removal step. As a result a second SiN_x sidewall is used to improve mechanical stability. This is deposited after the InGaAs emitter cap etch and fills in below the emitter metal providing it with better anchorage. The first sidewall needs to be removed in future processes for scaled junction widths.

Prior to sidewall deposition, the sample is dipped in 1:10 HCl:DI solution for 10 secs and then DI rinsed for 1 minute. This removes any oxide formed on the surface due to prior steps. This is critical especially for second sidewall deposited after the Cr cap removal step. After Cr cap removal, the sample is exposed to oxygen plasma to remove any scum left from the planarization procedure. This plasma

oxidizes the InP emitter surface and leads to uneven deposition of PECVD SiN_x. Dry etch of the SiN_x sidewall then leaves behind clumps of SiN_x which cannot be removed. Previously, NH_4OH dip was used as surface preparation technique to remove surface oxides prior to sidewall deposition which is an ineffective method. Fig. 3.14 shows the surface of two different samples after the InP emitter etch having SiN_x particles from the sidewall etch left in the field.



(a) (b)

Figure 3.14: Emitters after the InP wet etch showing particles present in the field from the second sidewall etch due to surface oxides

3.1.5 Emitter E-beam Writing

A new recipe for emitter definition using e-beam writer was developed to reproducibly achieve sub-200 nm emitter features. Prior to e-beam writer, 200 nm emitter features were attained using optical lithography and photoresist burn back using oxygen plasma. This process is not scalable to sub-200 nm features and as

a result e-beam writer process was developed. Fig. 3.15 shows the SEM top view of emitters after the Cr etch. maN-2403 negative tone photoresist, which spins on to ∼ 250-300 nm thickness, is used for emitter definition. The dose for e-beam exposure depends on the feature size and is approximately 1600 $\mu C/cm^2$ for 100 nm features. Emitter widths as small as 20 nm have been demonstrated with this resist. The resist has adhesion issues with the Cr cap after solvent clean and a oxygen plasma oxidation of Cr prior to resist coating is preferred.

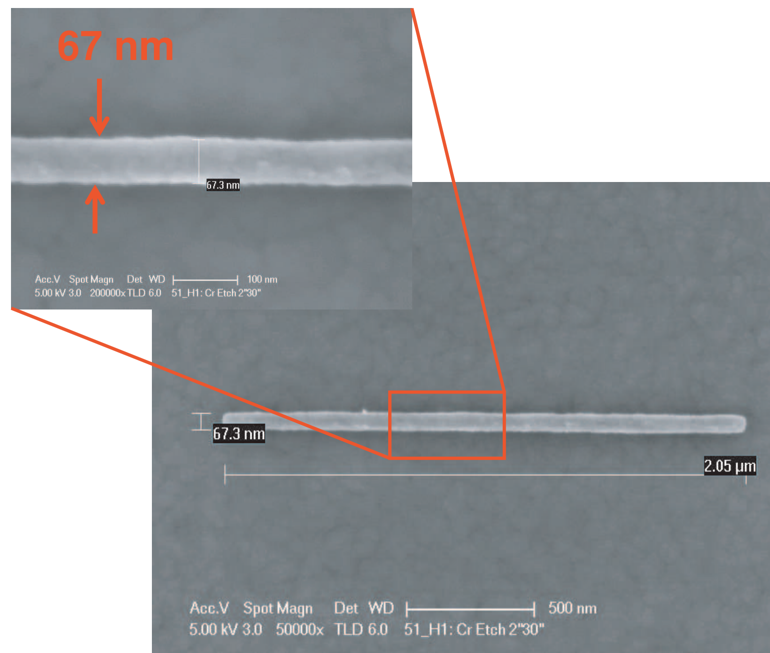


Figure 3.15: SEM image of the Cr cap after emitter definition using e-beam writer

Figs. 3.16 and 3.17 show cross-sectional FIB and TEM of two completed process runs. Fig. 3.16 is a FIB demonstrating 70 nm wide emitter base junction.

Fig. 3.17 shows TEM of a vertical emitter having W/TiW emitter stack with the dual sidewall process [20]. Line of sight base metal deposition and vertical emitter profile with high emitter aspect ratio prevents metal deposition on the sides of emitter thereby avoiding a short circuit between the base and emitter metals. There is very small undercut below the emitter metal in InP emitter resulting in $\sim$ 10-15 nm gap between the emitter semiconductor and base metal.

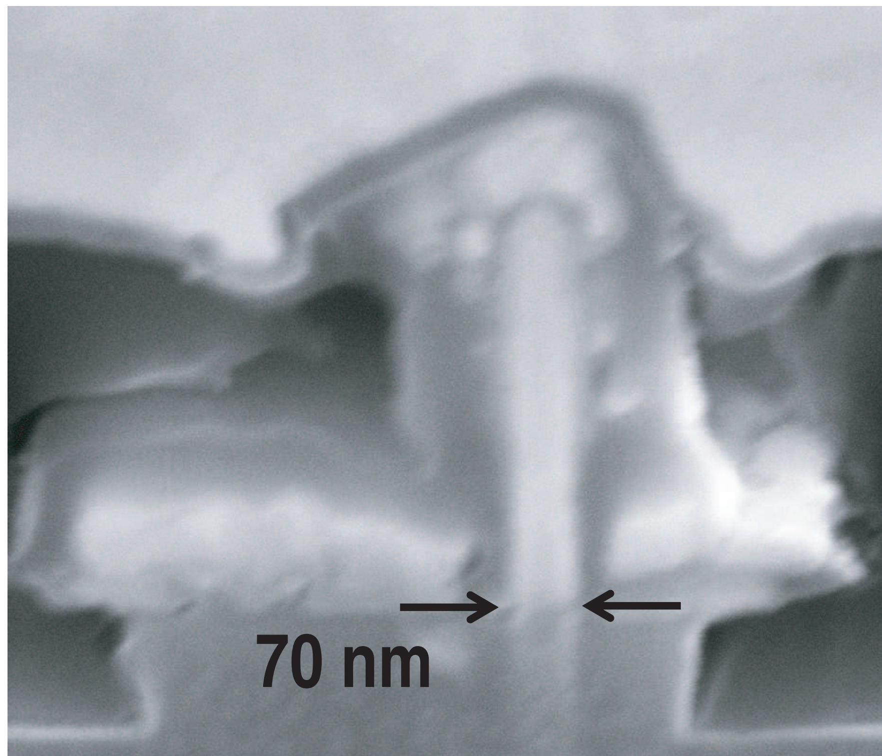
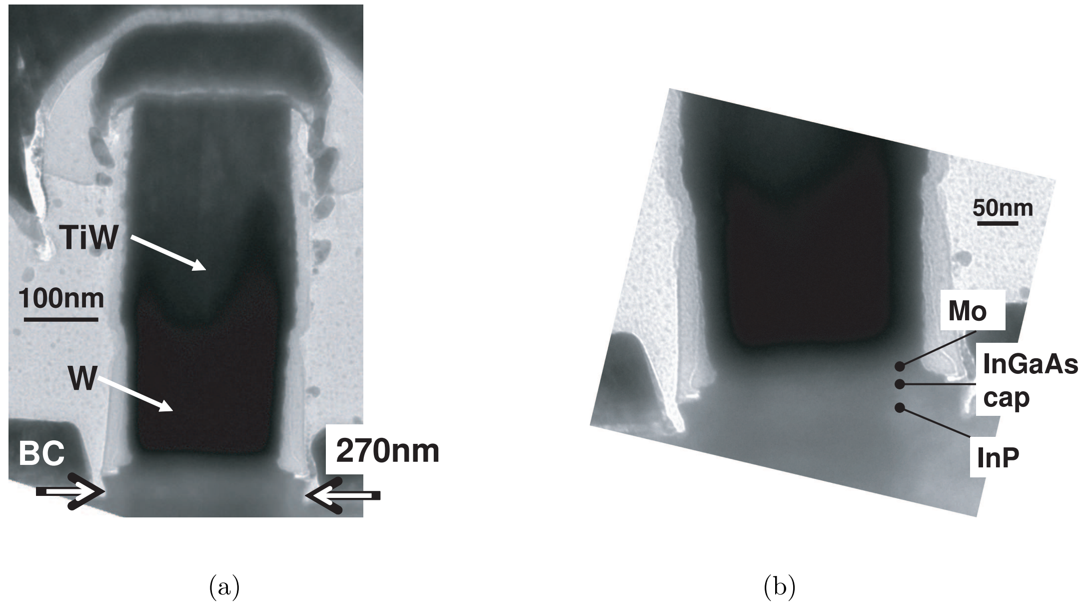


Figure 3.16: Cross-sectional FIB of a DHBT demonstrating 70 nm wide emitter base junction. FIB courtesy: Evan Lobisser



(a) (b)

Figure 3.17: Cross-sectional TEMs of emitter and base mesas of DHBT with 270 nm emitter-base junction. FIB/TEM courtesy: Evan Lobisser

3.2 Base Process Improvements

3.2.1 Lifted-off Base Contacts

Base contact resistivity is most critical to device performance as it directly impacts the device f_{max}. Lower contact resistivity to the base can be achieved through proper choice of contact metal and surface preparation. Previously, UV-O_3 oxidation and dilute NH_4OH dip (1:10 NH_4OH:DI) was used to achieve low contact resistivity. Results by Driad et al. [21] show that UV-O_3 treatment is an effective way of cleaning the surface of organic and non-organic materials. UV-O_3 also produces an oxide film which passivates the defective surface layers associated

with the native oxides of InP and InGaAs, and device processing. Based on this, after PR development and prior to loading the sample for contact deposition, the sample was exposed to UV-O_3 plasma for 10 minutes and then dipped in dilute NH_4OH for 10 secs to remove the oxides [19].

NH_4OH dip process is highly unreliable as it sometimes reacts with the nLOF-5510 photoresist used for base lift-off process and peels it off. The peeled off film sticks to the sample surface and has to be removed using a short oxygen plasma which damages the base surface. As mentioned earlier, UV-O_3 treatment oxidizes the InGaAs base surface and the oxides are then removed by surface treatment. Although this process cleans the surface of any organic contaminants, it also etches away a part of the base layer. It has been shown that 10 minutes of UV-O_3 oxidation forms $\sim$ 2 nm of oxide [22] which is a significant fraction of 25 nm thick base and increases base sheet resistance. Thus, UV-O_3 process was discontinued for the base contacts. NH_4OH dip was also discontinued due to its incompatibility with photoresists. For base contacts, a 10 secs dilute HCl dip (1:10 HCl:DI) and 1 minute DI rinse is now preferred as surface preparation procedure for obtaining low contact resistivity [17]. Generally, to obtain good contact resistivity for lifted-off contacts, descum is required to remove the residual photoresist/organics from the surface. However, this is not the case with the negative tone photoresist used for lift-off which leaves behind a clean surface after development.

In this work both Pd and Pt contacts have been used to achieve low base contact resistivity. It was shown by Chor et al. [23] that thin Pd layer contact to p-InGaAs reduces the contact resistivity. The metal stack used for base contacts is Pd/Ti/Pd/Au which is 2.5/17/17/70 nm thick. Initially Pd contacts were used for base but it was found that the contact resistivity increases after a 250°C bake for BCB. This increase in resistivity is probably due to Pd diffusion through the base doping grade. Miguel Urteaga at Teledyne Scientific found that Pt contacts are less diffusive than Pd during the BCB bake. He found that Pd contacts have lower contact resistivity than Pt for *as-deposited* material [24]. However, after BCB bake, degradation in measured contact resistivity is more for Pd than Pt due to Pd diffusion. Therefore, in latter half of this work, Pt contact - Pt/Ti/Pd/Au stack $\sim$ 2.5/17/17/70 nm thick was used.

3.2.2 Refractory Base Contacts

Lower base contact resistivity can be achieved using Pt/Pd contacts through increased base doping. However, this is not feasible due to increased Auger recombination in the base with doping which leads to β drop. Auger recombination can be reduced through reduction in base layer thickness but Pd, Pt and Ti based contacts diffuse into the base under thermal and electrical stress, increasing the base contact resistivity and limiting the minimum base thickness. 3 nm thick

Pd deposited on p-InGaAs as a part of Pd/Ti/Pd/Au stack (3/15/15/70 nm), diffuses about 15 nm into InGaAs after 1 hr 250°C BCB bake (Fig. 3.18). Thus to reduce base thickness and increase base doping, non-diffusive contacts are required which are refractory in nature. Work done by Ashish Baraskar [25–27] showed that very low contact resistivity can be achieved using refractory metals on highly doped p-InGaAs layer. Table 3.1 shows the measured contact resistivity of various refractory metals to p-InGaAs.

Doping (cm^{-3})	**Metal**	ρ_c ($\Omega \cdot \mu m^2$)
1.5×10^{20}	Mo	2.5
1.5×10^{20}	Ru/Mo	1.3
1.5×10^{20}	W/Mo	1.2
1.5×10^{20}	Ir/Mo	1.0
2.2×10^{20}	Ir/Mo	0.6

Table 3.1: Measured contact resistivity of refractory ohmic contacts to highly doped p-InGaAs layer

Based on these results, a new process flow for incorporating refractory base ohmics in DHBTs was designed. Low contact resistivity was achieved by blanket metal deposition without lift-off. A planarization and etch-back process flow was developed to etch the deposited refractory metal from the sides of the emitter. In this process, after the InP emitter is etched, blanket refractory metal is deposited on the base using e-beam evaporator system. Since the metal deposition in this case may not be line of sight, metal gets deposited on the sides of the emitter, short circuiting the emitter base junction and hence needs to be removed. PR

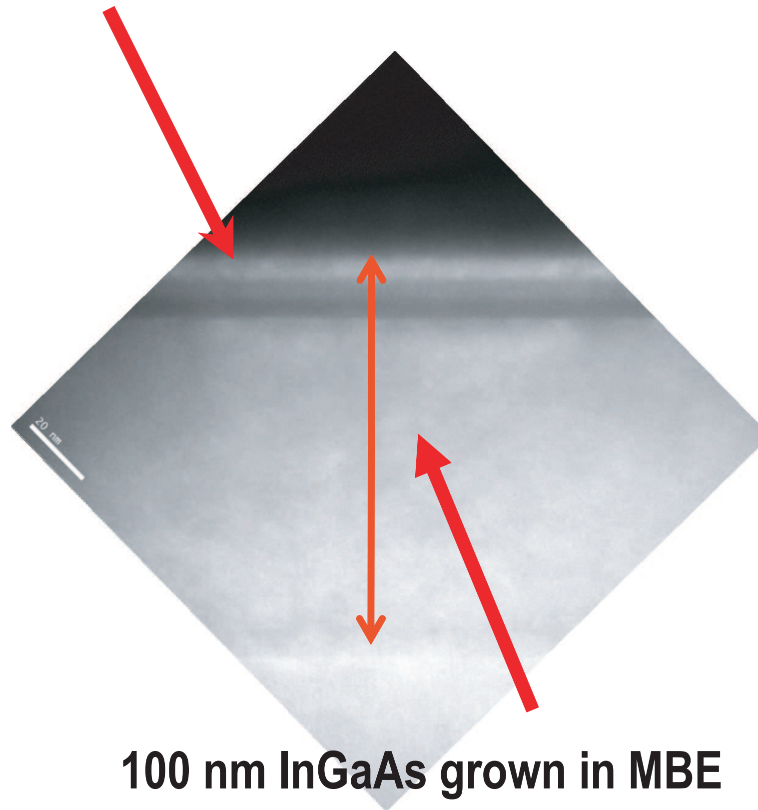
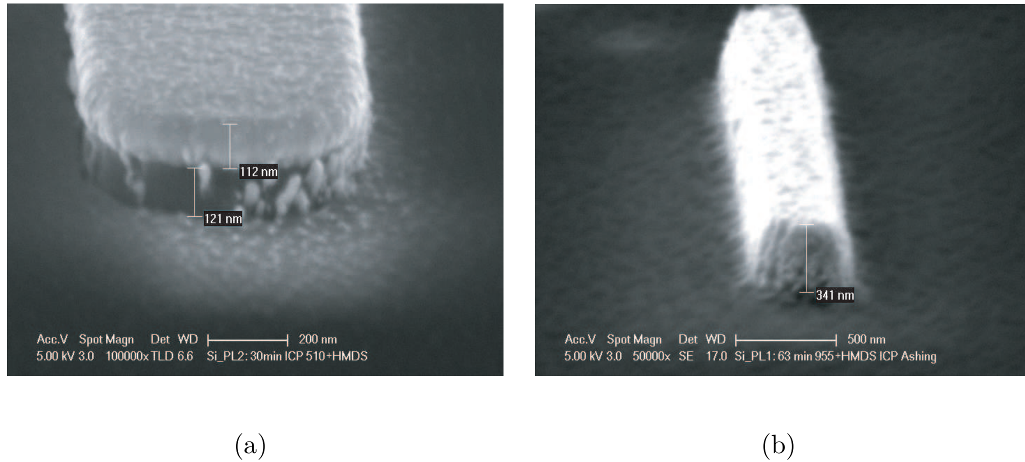


Figure 3.18: A TEM image showing the diffusion of 3 nm deposited Pd into 15 nm of p-InGaAs. Image courtesy: Ashish Baraskar and Evan Lobisser

is spincoated on the sample and burnt back (ashed) using oxygen plasma in a planarization step to expose part of the emitter. The height of the remaining PR is monitored to expose $\sim$ 250-300 nm of emitter. Refractory metal is then etched off in SF_6/Ar dry etch chemistry and the remaining PR is stripped off. Fig. 3.19 shows the emitters projecting out of the PR layer for planarization. Fig. 3.20 shows the emitters after etch-back and PR stripping step with the planarization

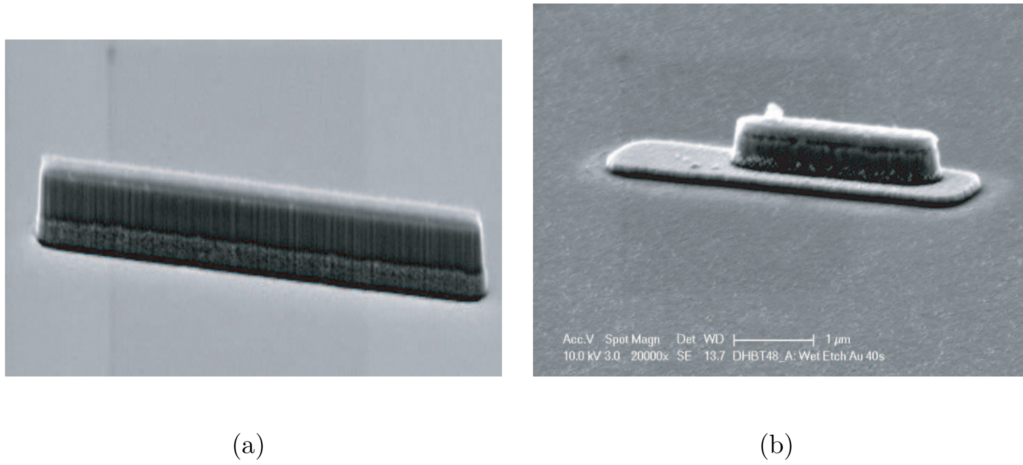
boundary. The planarization and etch-back steps can be avoided if base metal deposition is line of sight with no base-emitter shorts [28, 29].



(a) (b)

Figure 3.19: Emitters projecting out of the photoresist after planarization step for refractory dry etch

After the planarization step, Ti/Au base pads are lifted off to reduce base metal resistance. This is a very critical step as nLOF-5510 resist and 1165 stripper used for lift-off react with refractory metals and etch them off. Fig. 3.21 shows SEM of a sample where W contact has been etched from below the base Ti/Au pads. To reduce the lift-off time and improve reliability, a bilayer PR is used with LOL1000 forming the bottom adhesion layer. Base post lift-off is done after the base contact step. The sample is then blanket coated with $\sim$ 100 nm SiN_x hard mask. Base mesa mask is used to dry etch the SiN_x and refractory metal ohmic in the field followed by the wet etch of base mesa. This SiN_x hard mask also protects the narrow base-emitter gap from any further process damage. SiN_x gets etched from



(a) (b)

Figure 3.20: Emitters after the planarization and etch back steps showing the planarization boundary

the top of emitter and base post during the BCB etch step in the same chemistry. Fig. 3.22 shows the schematic representation of the base process flow for refractory base ohmics. Base mesa mask may not be required to etch SiN_x and refractory metal in the field and they can be etched in a manner similar to sidewall process for the emitter.

Blanket deposition of SiN_x after the base post step passivates the emitter-base junction with SiN_x rather than BCB as was the case with lifted-off base devices. PECVD deposition of SiN_x potentially damages the exposed emitter-base region due to plasma and presence of H (hydrogen) in the deposition gases. This degrades device current gain β after passivation [30, 31]. As a result better dielectrics need to be investigated for device passivation. ALD *high-k* dielectrics or thermal deposition of SiO_2 or SiN_x may be a better choice for device passivation [32].

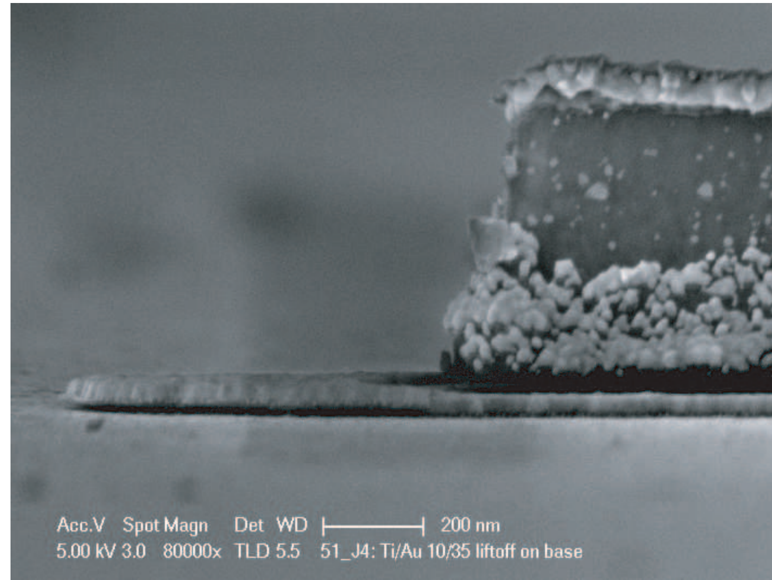
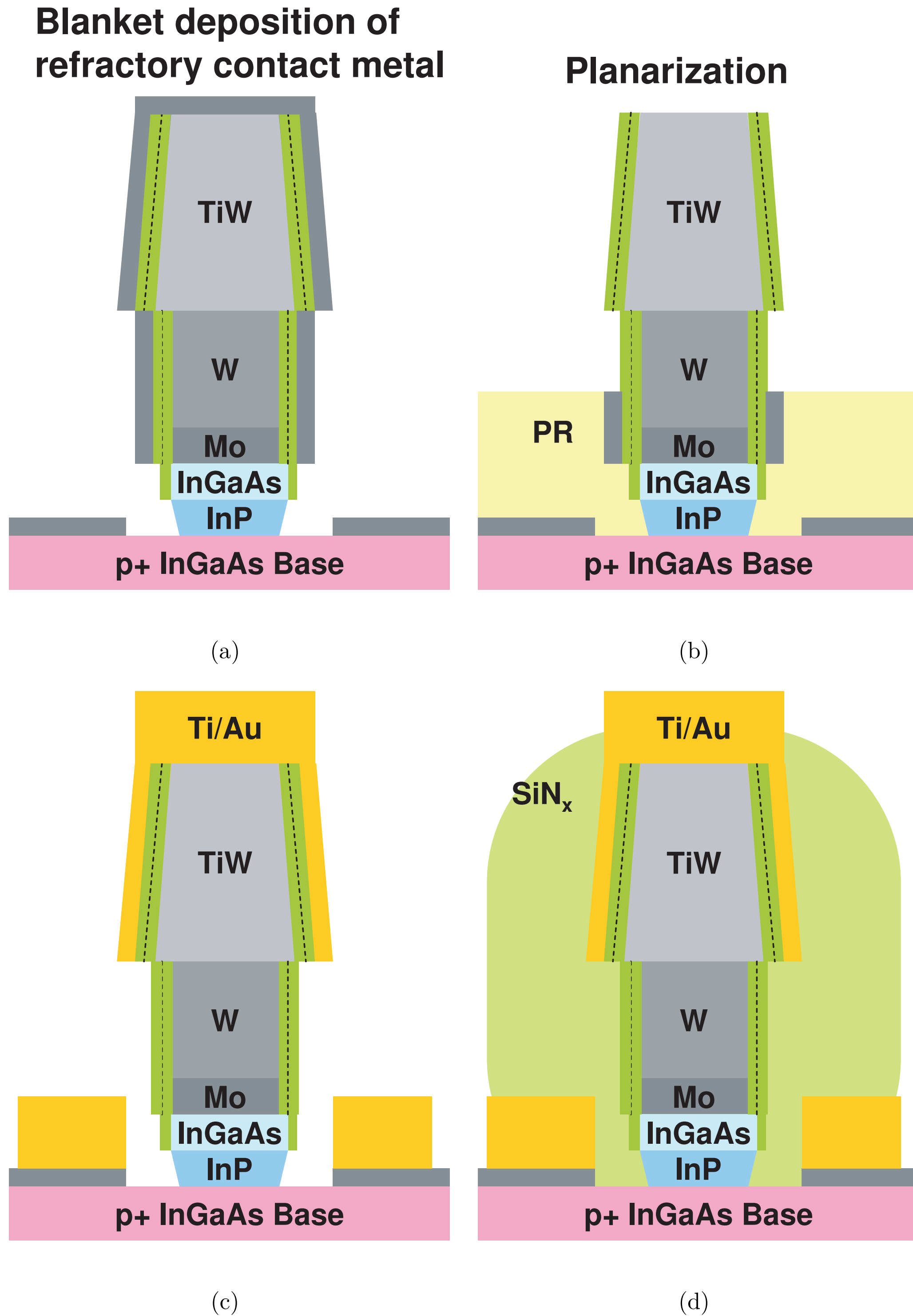


Figure 3.21: SEM of the emitter and base after Ti/Au pad lift-off. It can be observed that W has been etched off from below the base pad adjacent to the emitter

3.2.3 Base Post

Base post lift-off is challenging due to the high aspect ratio of the post. Typical base post height is 550 - 700 nm and the resist thickness is 1.1 μm. Thicker resist cannot be used due to loss in resolution. A bilayer resist process for base post lift-off was developed for easier and faster lift-off. LOL1000 adhesion layer is first spincoated to a thickness of about 70 nm and baked. The old process recipe of nLOF-5510 is then used. The bake time of LOL1000 can be optimized to achieve sufficient undercut in this layer during development so as to enable an easier lift-



(a) (b) (c) (d)

Figure 3.22: Schematic of DHBT process flow for refractory base contact formation

off step. LOL1000 is mandatory during base post lift-off for refractory ohmics due to PR issues discussed previously.

3.3 Collector Contacts

Collector contact resistivity has been reduced by increasing the doping in InGaAs sub-collector. Increased doping in the collector from 2×10^{19} cm^{-3} to 4×10^{19} cm^{-3} for the same InGaAs thickness of 7.5 nm reduced collector contact resistivity from 9 $\Omega \cdot \mu m^2$ to 6 $\Omega \cdot \mu m^2$. However, reduction in InGaAs thickness at the same 4×10^{19} cm^{-3} doping from 7.5 nm to 5 nm increased ρ_c to 22 $\Omega \cdot \mu m^2$. For lower contact resistivity, collector doping needs to be kept at 4×10^{19} cm^{-3} and thickness 7.5 nm. Doping cannot be increased further as it can cause defects in the growth of the epitaxial structure above collector. 10 secs dilute HCl dip (1:10 HCl:DI) and 1 minute DI rinse is used as surface preparation step before collector contact deposition. Ti/Pd/Au metal stack with 20 nm Ti is used for making collector contacts.

3.4 Device Passivation

After DHBT fabrication, the devices are passivated using bisbenzocyclobutene – BCB 3022-46 which spin coats to ~ 4.2 μm thickness. Before BCB spincoat,

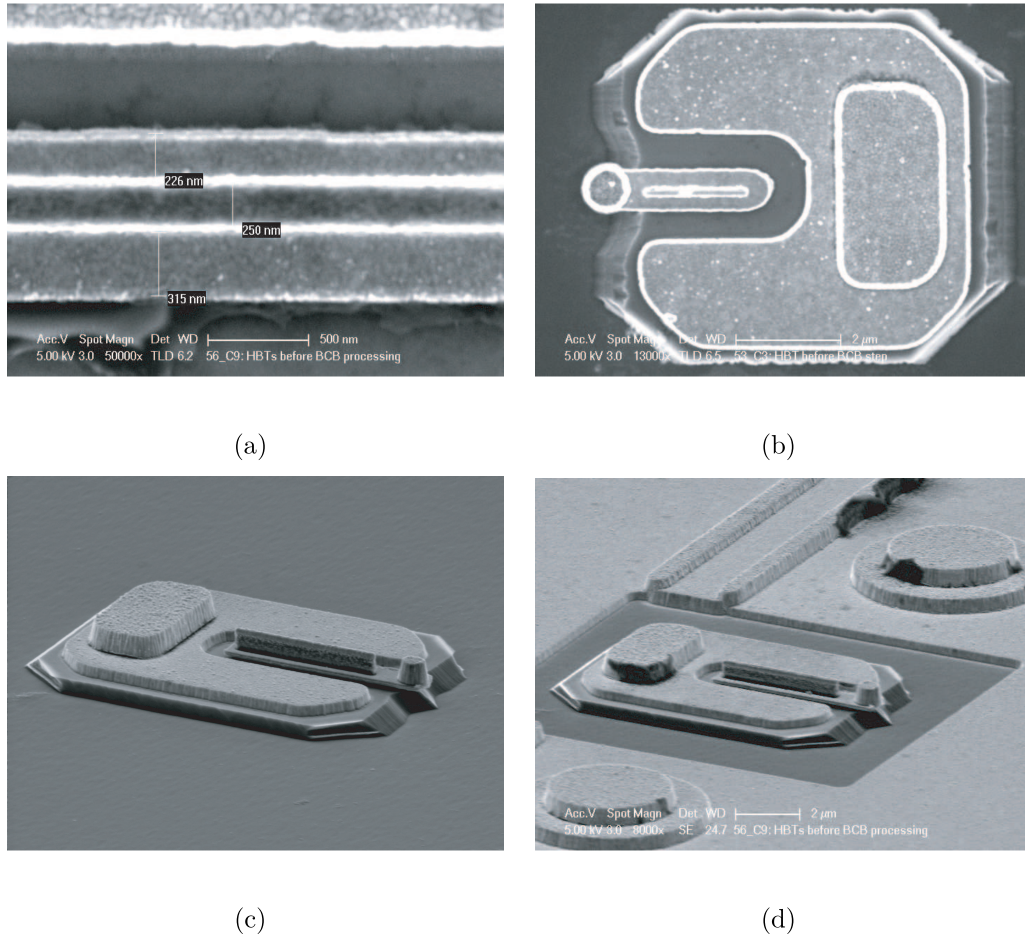


Figure 3.23: SEM images of the DHBT after front end processing and before device passivation. (a) Misalignment between the emitter and base layers, (b) top view of the completed HBT; Angular view of completed HBTs embedded in (c) coplanar waveguide environment and (d) on-wafer microstrip environment.

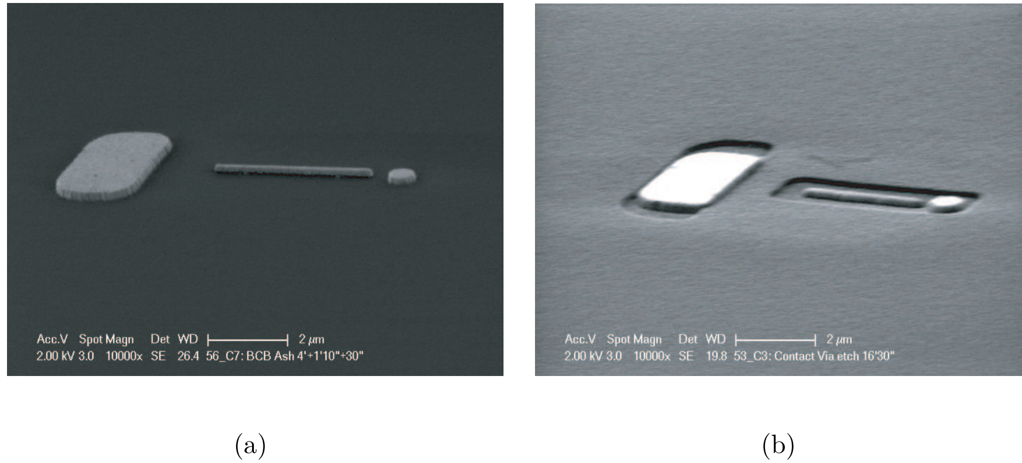


Figure 3.24: SEM images of the DHBT sample with the emitter, base post and collector post projecting out of BCB after the (a) BCB ash and (b) Contact via etch

the sample is treated with UV-O_3 plasma for 10 minutes and then dipped in conc. NH_4OH for 10 secs. The sample is immediately loaded for BCB bake at 250°C for 1 hr in nitrogen environment. The thickness of the BCB layer after bake can be estimated using Nanometrics tool. BCB is etched in CF_4/O_2 plasma for 4 minutes. Remaining BCB thickness is again measured using nanometrics tool to estimate the BCB ash rate. BCB ash rate is a strong function of ashing chuck/chamber temperature and varies with the chamber conditioning time prior to ashing. DHBT features - emitters and posts start projecting out of BCB when remaining BCB thickness is $\sim 1\ \mu m$. The sample is inspected under SEM to ensure that the BCB ash is complete and there is no over-ash. If the ash is incomplete, more ashing is done in increments of 1 minute or 30 secs depending on the amount

of BCB to be ashed. Fig. 3.23 shows DHBT SEMs after the DHBT fabrication and before BCB planarization. Fig. 3.24 shows the SEM images of the HBT posts and emitter visible through the BCB ash and after the contact via etch.

Process flow for the emitter formation and lifted-off base contacts is shown schematically in Figs. 3.25 and 3.26.

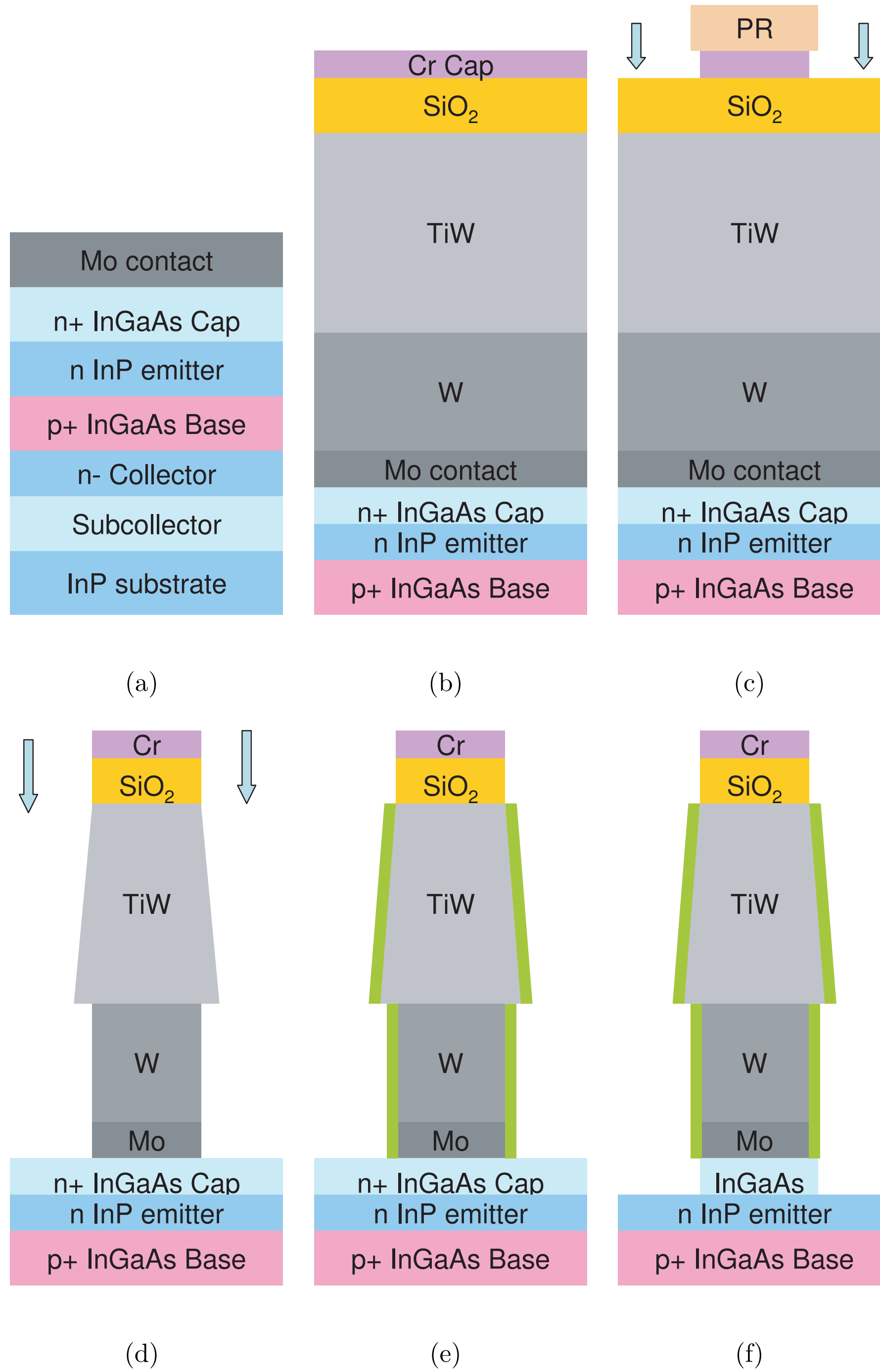


Figure 3.25: Schematic of the DHBT process flow for emitter formation - I

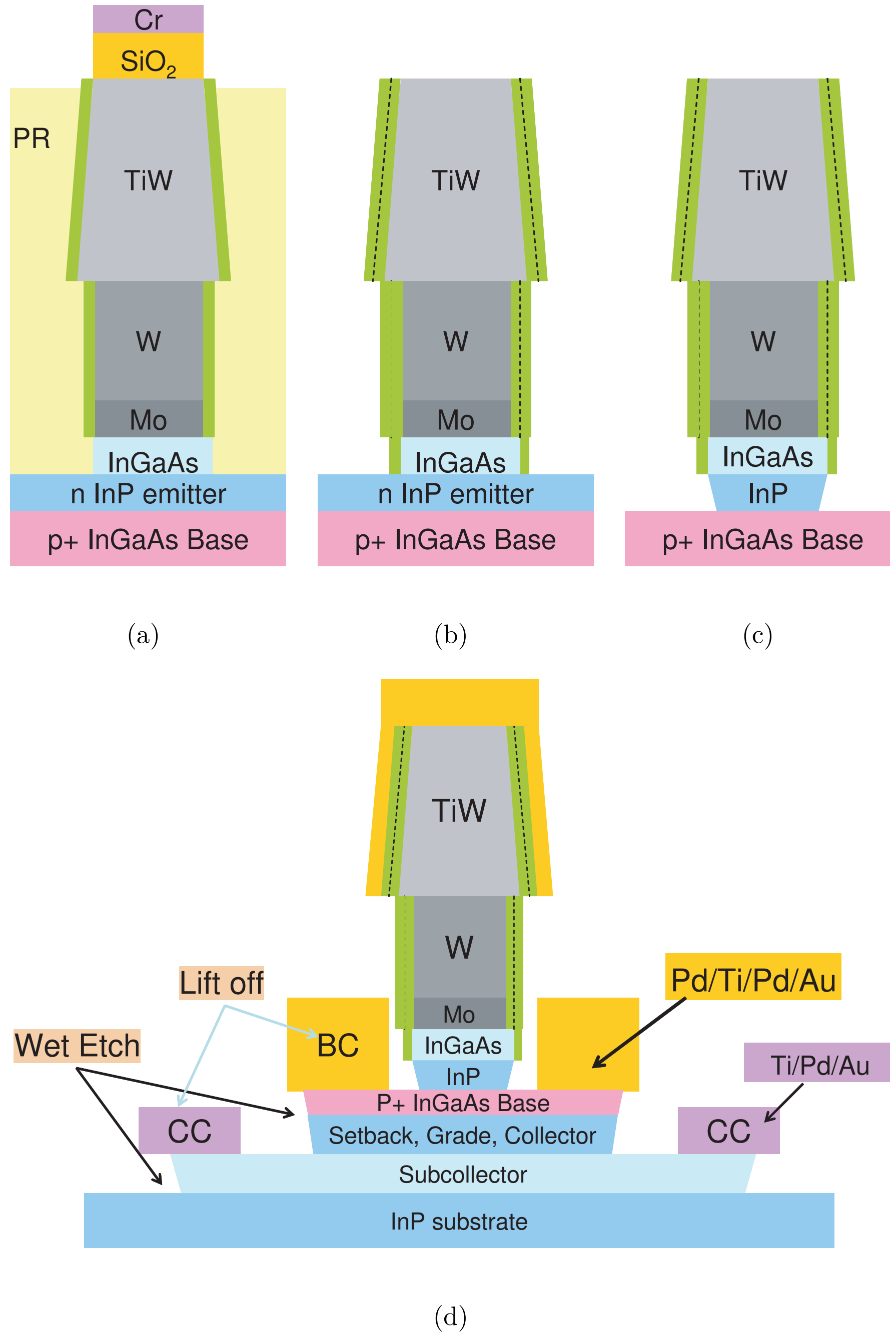


Figure 3.26: Schematic of the DHBT process flow for emitter formation - II and (d) the final DHBT cross-section

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Chapter 4

DHBT Results

In this chapter device results, both RF and DC, for InP DHBTs have been reported using the process modules discussed in Chap. 3. The device epitaxy was designed to improve both f_τ and f_{max} at a given emitter width. Emitter access resistance R_{ex}, base contact resistance ρ_c, sidewall thickness and thermal resistance are the key limitations to DHBT scaling.

4.1 PNA Calibration Methods

HBTs demonstrating very high f_{max} have extremely small reverse transmission characteristics and low shunt output conductance making device measurements challenging [1]. Accurate, reliable and repeatable DHBT measurements require

a well-characterized, calibrated measurement environment where the effects of the transmission medium in which the device is embedded for testing have been separated from actual device characteristics. The DHBTs reported in this work have cut-off frequencies far in excess of the frequency span covered by most of the commercially available vector netowrk analyzers (VNA) and hence accurate measurement of device S-parameters for cut-off frequency determination becomes very critical. In this work, Agilent E8361A network analyzer was used for device measurement which has a frequency range of 10 MHz - 67 GHz. Although modules are available for device measurements at higher frequencies, obtaining a good calibration and accurate measurements at frequencies greater than 67 GHz is quite challenging. The challenges associated with high frequency calibrations will not be discussed here. For f_τ and f_{max} extraction, accurate measurements till 67 GHz were found to be sufficient.

A full two-port VNA calibration is required to place the measurement reference planes precisely at the input and output of the device-under-test (DUT). This requires stripping from the measurements the systematic effects (contributions from delays and losses) associated with the PNA, the microwave cables, the wafer probes, and the on-wafer transmission line network that the DUT is embedded within. VNA calibration is performed by measuring a set of defined calibration standards. From the S-parameter measurements of these standards, a set of error

correction coefficients is determined and used to calibrate the VNA and subsequent measurements [2–5].

Two approaches are commonly used for *on-wafer* device measurement calibration. In one approach, calibration standards are realized on a separate calibration substrate. These calibration substrates are available commercially covering frequencies up to 220 GHz and are typically fabricated using thin-film processes on alumina (Al_2O_3) substrates. When using the calibration substrate approach, the calibration is designed to place the measurement references planes at the wafer-probe tips, and therefore this approach is often referred to as a *probe-tip* calibration. This calibration approach is commonly used for *on-wafer* device measurements and offers the advantage of having well-characterized precision calibration standards. It has been used for performing calibrations for all the RF measurements reported in this chapter. In the second *on-wafer* calibration approach, custom calibration standards are realized on the active device substrate. A short discussion on the *on-wafer* custom calibration structures for the UCSB DHBTs is given at the end of this chapter.

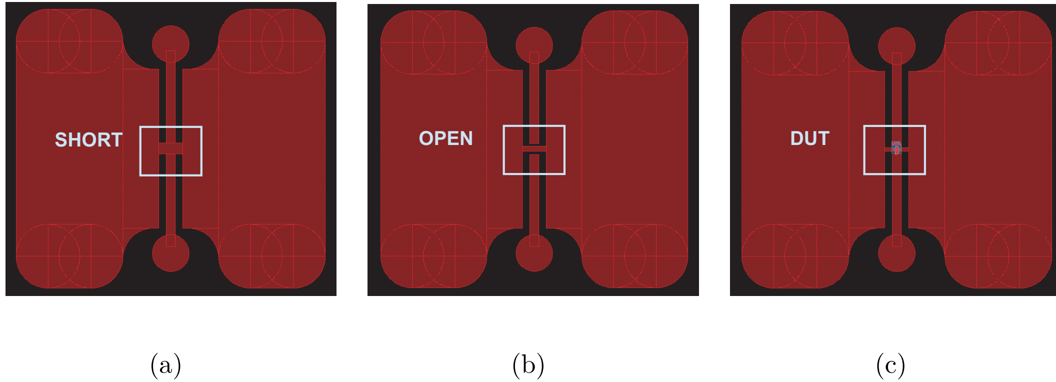
There are a number of different VNA calibration methods that could be utilized to calibrate the system. The calibrations differ in the standards that are measured, and in the assumptions made regarding the standards for determining the error-correction terms. The calibration methods include Short-Open-Line-Thru

(SOLT), Thru-Reflect-Line (TRL), Line-Reflect-Match (LRM), and Line-Reflect-Reflect-Match (LRRM). In this work, LRRM (probe-tip) technique is used for VNA calibration, and is briefly reviewed here.

The LRRM method [3] is well suited for two-port VNA calibration in a coaxial measurement environment where the desired frequency span to be tested is large like the 0.1-67 GHz single sweep on Agilent E8361A PNA system. The accuracy of the standard models used in the calibration need not be known to a high level of accuracy. The models expected include two independent reflect standards - a dual one-port device made up by two identical, isolated loads with a reflection coefficients Γ_{r1} and Γ_{r2} for Reflects 1 and 2. To assure independent measurements, a non-ideal open-circuit and non-ideal short-circuit are used in the determination of Γ_{r1} and Γ_{r2}. The LRRM calibration extracts the inductance of the load standard, so that only the DC resistance of the standard need be known.

VNA calibration using *off-wafer* LRRM standard sets the reference planes at the probe tips. The second step of the calibration procedure is to *de-embed* the parasitics associated with the *on-wafer* transmission line network that the DUT is embedded within. The parasitics associated with the wiring structure can be characterized by measuring two patterns after system calibration: an *open* interconnect pattern (Y_{open}) which corrects for the parallel parasitics and a *short* interconnect pattern (Y_{short}) to determine losses and phase rotation in the interconnect lines.

The actual transistor Y-parameters (Y_{trans}) can finally be obtained from measured DUT parameters (Y_{dut}) using $Y_{trans} = ((Y_{dut} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1})^{-1}$. The DUT, open and short structures used in this work are shown in Fig 4.1. This approach for calibration however is only valid if the physical length of the embedding network is small relative to the propagation wavelength at the measurement frequency [6].



(a) (b) (c)

Figure 4.1: (a) Open and (b) Short pad structures identical to that used by (c) DUT for deembedding the pad parasitics

In an *on-wafer* measurement environment, port-to-port crosstalk can be large due to radiative or near-field coupling between *on-wafer* probes. The coupling will depend on the impedance presented to the probes, and the conditions for an accurate isolation calibration are difficult, if not impossible, to achieve *on-wafer*. Highly scaled transistors have extremely small reverse transmission characteristics, and probe-to-probe coupling that is not accounted for in a measurement calibration can easily corrupt device measurements. Thus, at high frequency,

as the propagation wavelength decreases, the physical length of the embedding network cannot be reduced due to increase in probe-to-probe coupling.

4.2 DHBT49

DHBT49 design incorporates a 25 nm thick base having a doping gradient $7-4\times10^{19}$ cm^{-3} and 100 nm thick collector doped at 9×10^{16} cm^{-3}. The collector doping was chosen to fully deplete the collector at an applied V_{cb} =0.3 V at low J_e which is remnant of the collector designs used traditionally for emitter-coupled-logic (ECL) circuit designs. The design incorporates a thin 7.5 nm setback and 15 nm base-collector chirped super-lattice grade. The thin setback and grade were used to reduce the percentage of ternary alloys in the collector so as to improve thermal resistance [7]. For the *first time*, emitter $In_{0.53}Ga_{0.47}As$ regrowth and *in-situ* Mo contacts were used for HBTs. 10 nm highly doped n-$In_{0.53}Ga_{0.47}As$ doped at 5×10^{19} cm^{-3} was regrown on the IQE grown $In_{0.53}Ga_{0.47}As$ emitter cap also doped at 5×10^{19} cm^{-3}. *In-situ* Mo was then deposited using a e-beam evaporator attached to the MBE system to obtain very low resistance emitter contacts. The detailed procedure was discussed in the previous chapter. Two SiN_x sidewalls of 50 nm and 30 nm were used in this process. First sidewall was kept thick to provide stability to the emitters due to excessive W undercut during the emitter

stack dry etch. InP emitter has been thinned down to 50 nm to enable a wet etch process. The epitaxial structure for this DHBT is given in Table 4.1. Band diagram of the layer structure is shown in Fig 4.2 [8]. J_{kirk} value was obtained assuming current spreading in the collector for 110 nm emitter-base junction. A cross-sectional SEM and TEM of a HBT with 110 nm emitter-base junction and 100 nm emitter metal-semiconductor junction is shown in Fig. 4.3. From the cross-sectional TEM, it can be seen that the gap between base metal and emitter semiconductor is large $\sim$ 50 nm due to excessive undercut in the InP emitter during the wet etch, leading to extra base access resistance [9].

T(nm)	**Material**	**Doping** (cm^{-3})	**Description**
10	$In_{0.53}Ga_{0.47}As$	$5 \cdot 10^{19}$: Si	Regrown Cap
10	$In_{0.53}Ga_{0.47}As$	$5 \cdot 10^{19}$: Si	Emitter Cap
10	InP	$4 \cdot 10^{19}$: Si	Emitter
10	InP	$1 \cdot 10^{18}$: Si	Emitter
30	InP	$8 \cdot 10^{17}$: Si	Emitter
25	InGaAs	$7 - 4 \cdot 10^{19}$: C	Base
7.5	$In_{0.53}Ga_{0.47}As$	$9 \cdot 10^{16}$: Si	Setback
15	InGaAs/InAlAs	$9 \cdot 10^{16}$: Si	B-C Grade
3	InP	$5 \cdot 10^{18}$: Si	Pulse Doping
74.5	InP	$9 \cdot 10^{16}$: Si	Collector
7.5	InP	$1 \cdot 10^{19}$: Si	Sub-Collector
7.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Sub-Collector
300	InP	$2 \cdot 10^{19}$: Si	Sub-Collector
Substrate	SI:InP		

Table 4.1: Epitaxial layer structure of DHBT49

Fig. 4.4 shows the common-emitter $I - V$ curves and Gummel characteristics for DHBT49 for a device having emitter-base junction width of 110 nm. The de-

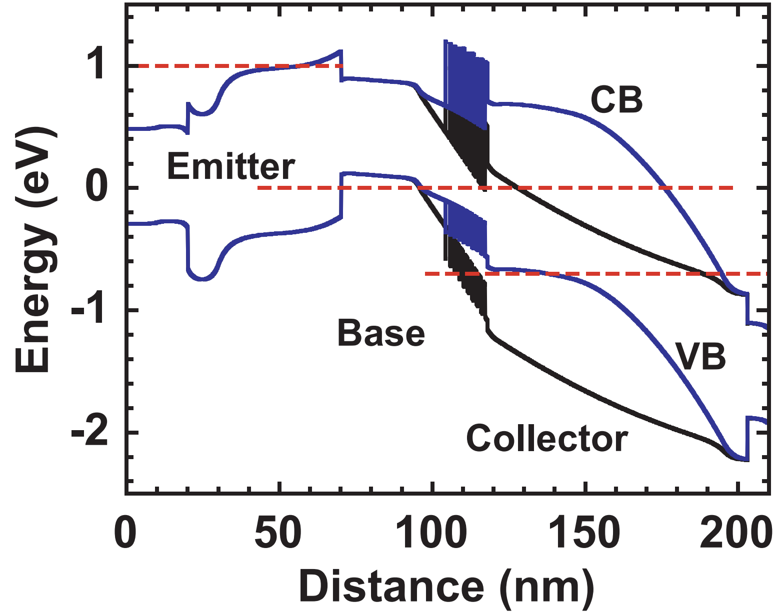
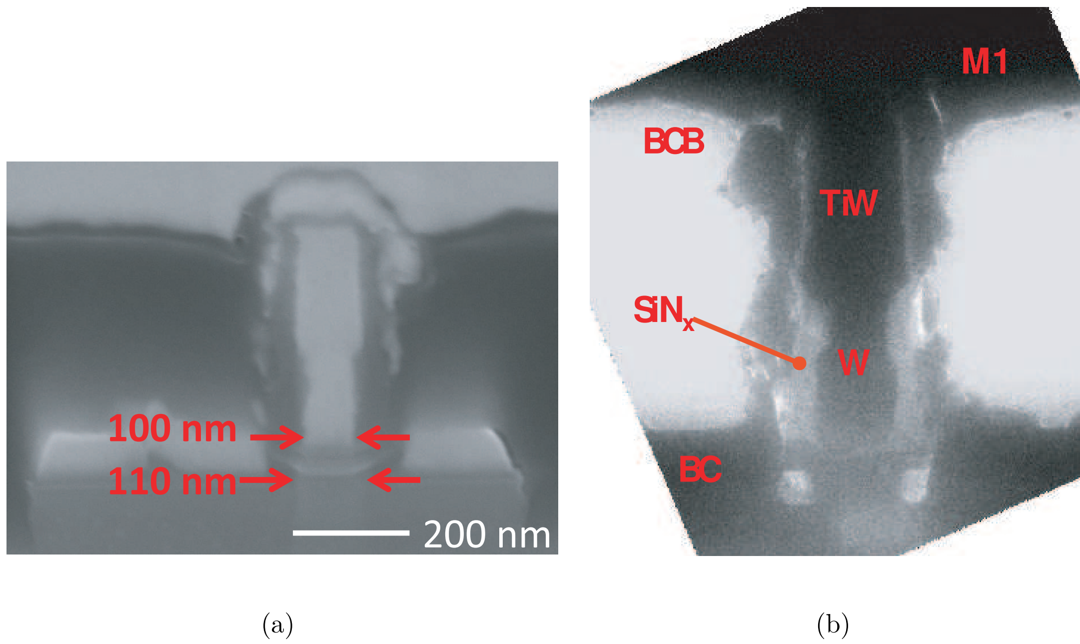


Figure 4.2: Simulated band structure of DHBT49 for $J_e = 0$ and 30 $mA/\mu m^2$, $V_{be} = 1\ V$, $V_{cb} = 0.7\ V$. Current spreading was assumed in the collector for 110 wide emitter-base junction

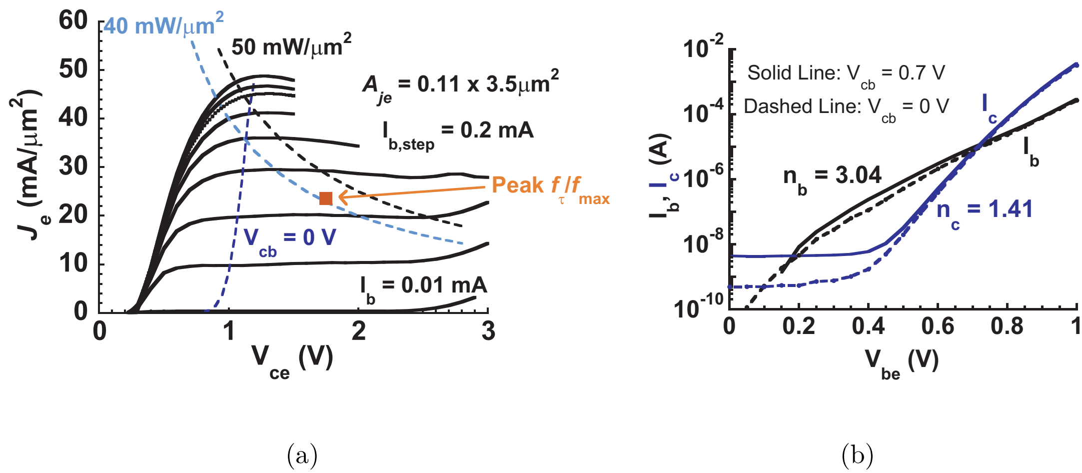
vices show excellent current carrying and power handling capabilities and can operate at $J_e > 40\ mA/\mu m^2$ and power density $P_{max} > 50\ mW/\mu m^2$ (Fig. 4.4(a)). The device can be biased without destruction above 55 $mW/\mu m^2$. HBTs with an emitter area $A_{je} = 0.11 \times 3.5\ \mu m^2$, have DC common emitter current gain $\beta = 18$ and common emitter breakdown voltage $V_{BR,CEO} = 2.5$ V ($J_e = 10\ kA/cm^2$). Base ideality factor n_b obtained from Gummel plot is much higher than expected and could be due to high emitter-base leakage due to damaged extrinsic base.

Fig. 4.5 shows the measured microwave gains - current gain H_{21}, Maximum Stable Gain (MSG) and Mason's Unilateral Gain (U) at the bias associated with



(a) (b)

Figure 4.3: Cross-sectional (a) SEM and (b) TEM of emitter and base mesas of DHBT with 100 nm emitter metal contact and 110 nm emitter-base junction



(a) (b)

Figure 4.4: (a) Common emitter $I-V$ and (b) Gummel characteristics for DHBT49 having 110 nm emitter-base junction

peak f_τ and f_{max}. Peak RF performance was obtained at I_c = 9.6 mA and V_{ce} = 1.74 V (V_{cb} = 0.7 V, $J_e = 24.9\ mA/\mu m^2$, $P = 43.3\ mW/\mu m^2$, C_{cb}/I_c = 0.4 psec/V). Extrapolations from single pole fit indicate f_τ = 400 GHz and f_{max} = 660 GHz. RF measurements were done using *off-wafer*, probe-tip, Line-Reflect-Reflect-Match (LRRM) calibration and parasitic de-embedding as discussed in section 4.1. Kirk effect is observed at $J_e = 32\ mA/\mu m^2$ (V_{ce} = 1.75 V) when f_τ falls to 95% of its peak value. Variation in measured f_τ, f_{max} and C_{cb} with J_e for various V_{cb} is shown in Fig. 4.6.

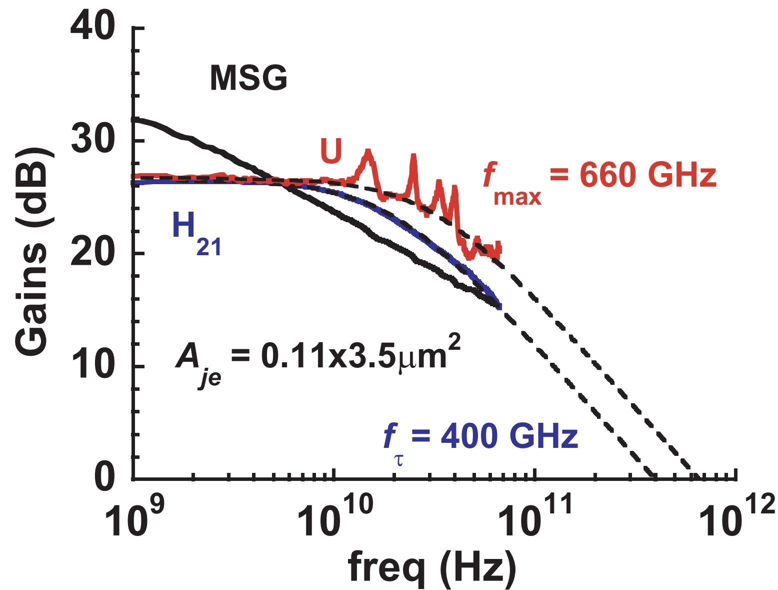
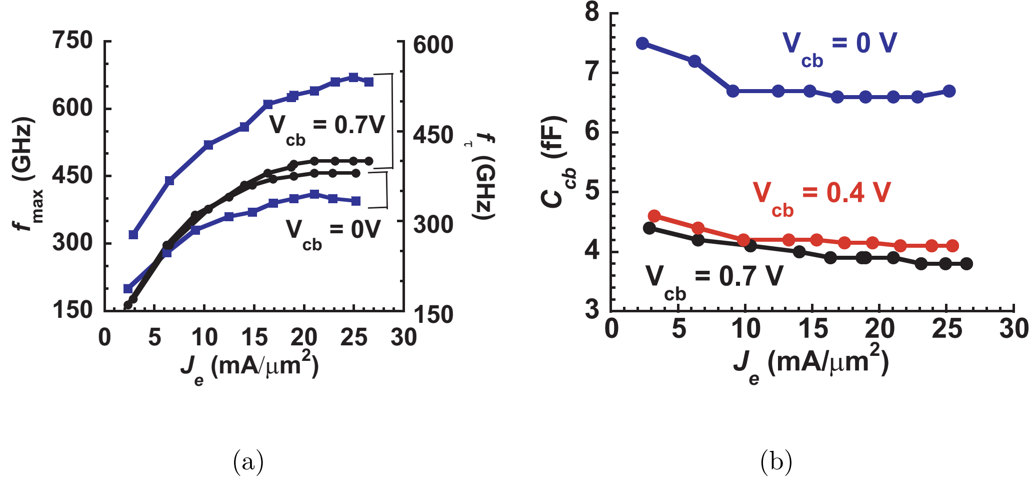


Figure 4.5: Measured RF gains for the DHBT in 1 - 67 GHz band using off-wafer LRRM calibration



(a) (b)

Figure 4.6: (a) f_τ / f_{max} and (b) C_{cb} dependence on V_{cb} and J_e

Transmission Line Model (TLM) measurements show base $R_{sh} = 732\ \Omega/sq$ and $\rho_c < 4\ \Omega \cdot \mu m^2$ and collector $R_{sh} = 12\ \Omega/sq$ and $\rho_c < 9\ \Omega \cdot \mu m^2$. Emitter access resistance $R_{ex} < 4\ \Omega \cdot \mu m^2$ was extracted from RF data.

Although these devices were the first set of working devices using the new emitter process flow, measured f_τ and f_{max} were much lower than the designed values. A lower than expected f_{max} in spite of a good base ohmic was measured due to high base access resistance (R_{bb}) as extracted from the hybrid-π equivalent circuit shown in Fig. 4.7. This is probably to be due to high gap resistance (R_{gap}) term associated with R_{bb} and high C_{cb} due to wide base mesa. As mentioned earlier, due to excessive undercut in the InP emitter, the gap between base metal and emitter semiconductor was $\sim$ 50 nm. In addition, from non-pinched TLM measurements, base sheet resistance $R_{sh,np}$ of greater than 3000 Ω/sq was

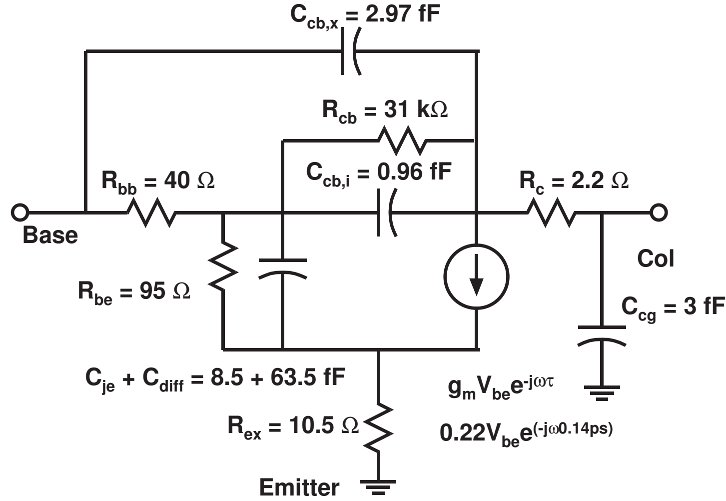


Figure 4.7: Hybrid-π equivalent circuit at peak RF performance from 1-67 GHz RF data

extracted as opposed to an expected value of 860 Ω/sq. This is due to surface damage caused by multiple base lithography failures and O_2 ashing to remove scum. The combination of large gap and high sheet resistance led to high R_{gap} value, reducing f_{max} ($R_{gap} = R_{sh,gap} \cdot W_{gap}/2L_e$).

Lower than expected f_τ was due to low collector velocity. Velocity extraction in the collector was done by method discussed in Chap. 2. Assuming that there were no growth issues with the base growth, extracted collector velocity is $\sim 2.1 \times 10^7\ cm/s$ which is much less than the $3 - 3.5 \times 10^7\ cm/s$ value expected for a 100 nm InP collector design. Although the extracted velocity value is approximate as exact RC delays cannot be calculated, the measured velocity is still too low to be explained by errors in determination of the RC charging times. Collector

velocity could be low due to faulty base-collector setback and grade design (too thin) or growth issues. However, the low collector velocity assumption completely explains the measured f_τ and f_{max} values.

4.3 DHBT53

T(nm)	**Material**	**Doping** (cm^{-3})	**Description**
10	$In_{0.53}Ga_{0.47}As$	$8 \cdot 10^{19}$: Si	Emitter Cap
15	InP	$5 \cdot 10^{19}$: Si	Emitter
15	InP	$2 \cdot 10^{18}$: Si	Emitter
30	InGaAs	$9 - 5 \cdot 10^{19}$: C	Base
4.5	$In_{0.53}Ga_{0.47}As$	$9 \cdot 10^{16}$: Si	Setback
10.8	InGaAs/InAlAs	$9 \cdot 10^{16}$: Si	B-C Grade
3	InP	$6 \cdot 10^{18}$: Si	Pulse Doping
81.7	InP	$9 \cdot 10^{16}$: Si	Collector
7.5	InP	$1 \cdot 10^{19}$: Si	Sub-Collector
7.5	$In_{0.53}Ga_{0.47}As$	$4 \cdot 10^{19}$: Si	Sub-Collector
300	InP	$2 \cdot 10^{19}$: Si	Sub-Collector
3.5	$In_{0.53}Ga_{0.47}As$	Undoped	Etch Stop
Substrate	SI:InP		

Table 4.2: Epitaxial layer structure of DHBT53

This design also had a 100 nm thick collector. There were quite a few problems with DHBT49 epitaxial design that were fixed in this design. High base access resistance was observed in DHBT49 due to excess emitter undercut and high base sheet resistance. In this design, base doping gradient was increased to $9 - 5 \times 10^{19}$ cm^{-3} and thickness increased to 30 nm to reduce base sheet resistance. To reduce emitter undercut during wet etch, InP emitter thickness was decreased to

30 nm. This design also incorporates a thin and higher doped n-InP emitter region to sustain high current density. Base-collector grade was changed from chirped superlattice to sub-monolayer grade [10]. Setback and grade combined thickness was reduced to 18.3 nm. However, collector doping was left unchanged. Doping in the InGaAs sub-collector was also increased to 4×10^{19} cm^{-3} for reduced collector contact resistance. Complete layer structure and simulated band diagram are shown in Table 4.2 and Fig. 4.8 respectively.

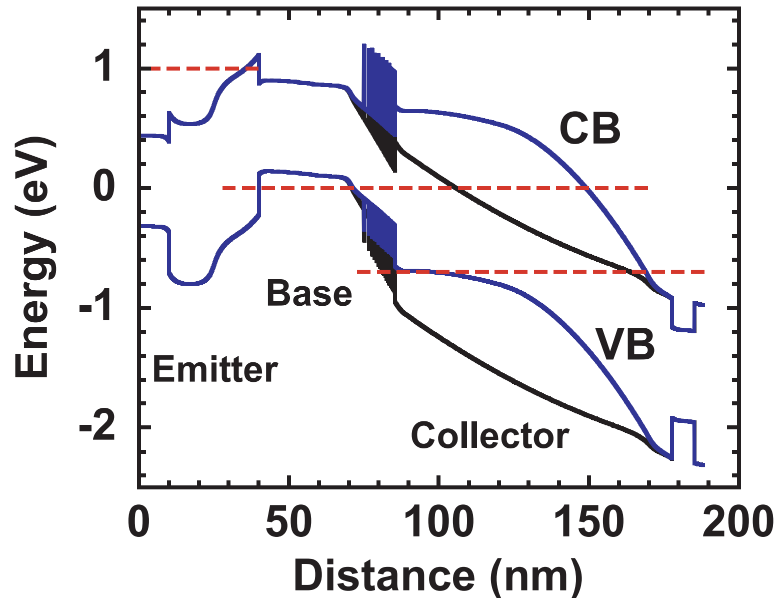
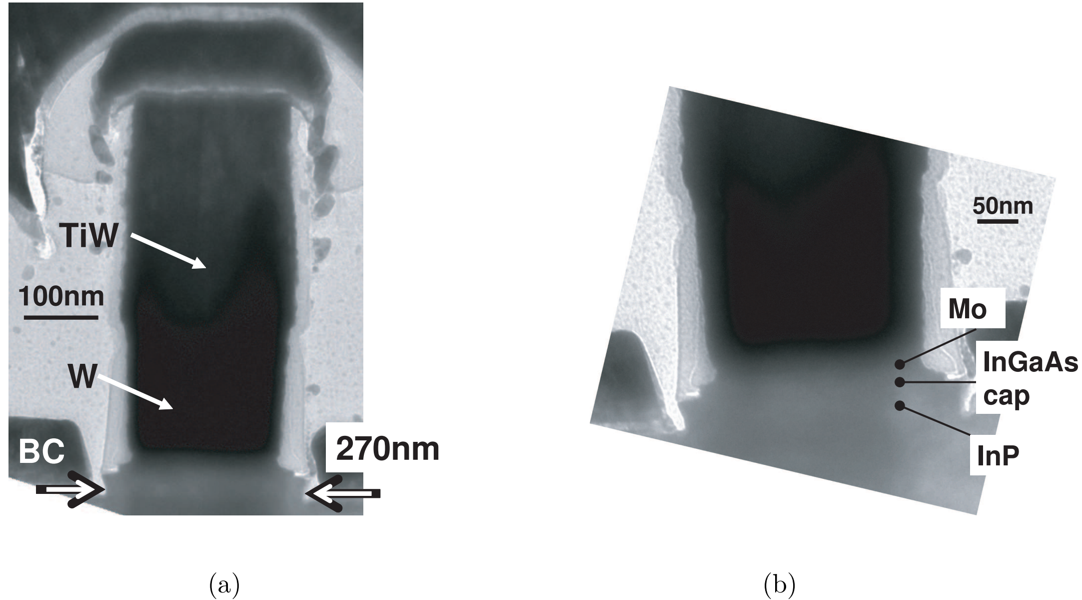


Figure 4.8: Simulated band structure of DHBT53 for $J_e = 0$ and 25 $mA/\mu m^2$, $V_{be} = 1$ V, $V_{cb} = 0.7$ V. Current spreading was assumed in the collector for 220 nm wide emitter-base junction

It was hypothesized that H cleaning on the emitter for emitter regrowth and Mo contact deposition could deactivate some C in the base [11]. As a result, in

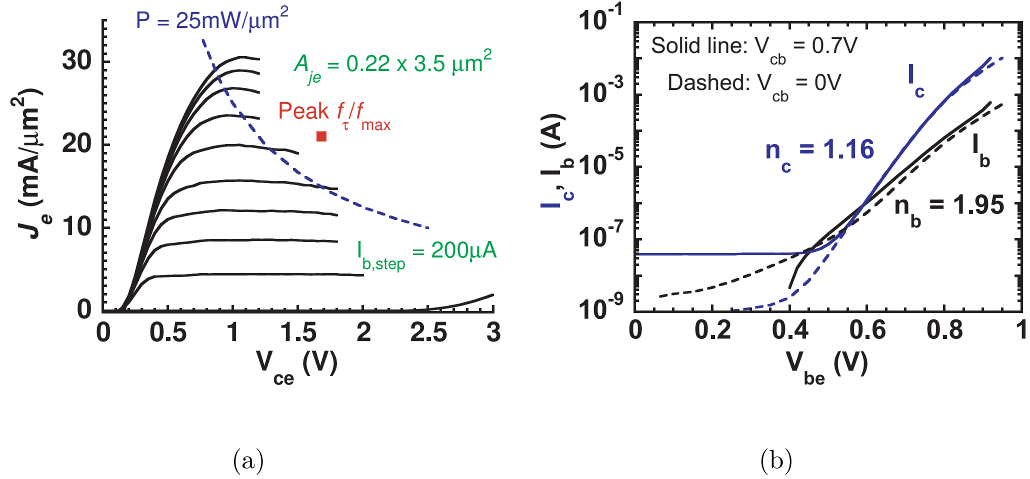


(a) (b)

Figure 4.9: Cross-sectional TEMs of emitter and base mesas of DHBT with 270 nm emitter-base junction

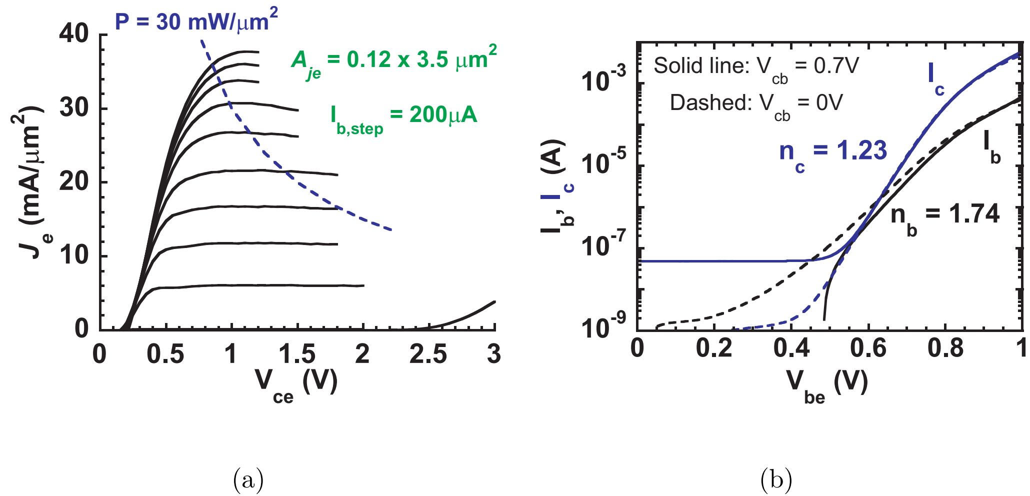
this process run, *ex-situ* Mo contacts on IQE grown InGaAs emitter cap were formed by e-beam deposition in the cleanroom. Dual SiN_x sidewalls, each 30 nm thick, were used in this process. The process had excellent yield and emitters ranging from 120 nm to 270 nm width were measured.

A cross-sectional FIB/TEM of the emitter having 270 nm wide emitter-base junction is shown in Fig. 4.9. Although emitter metal-semiconductor junction is only 220 nm wide, due to the dual sidewalls, actual emitter-base junction is wider at 270 nm. More importantly, due to controlled InP emitter undercut, base metal to emitter semiconductor gap has been reduced to less than 10 nm. This greatly helps in reducing base access resistance for these HBTs.



(a) (b)

Figure 4.10: (a) Common emitter $I-V$ and (b) Gummel characteristics for DHBT53 having 220 nm emitter-base junction



(a) (b)

Figure 4.11: (a) Common emitter $I-V$ and (b) Gummel characteristics for DHBT53 having 120 nm emitter-base junction

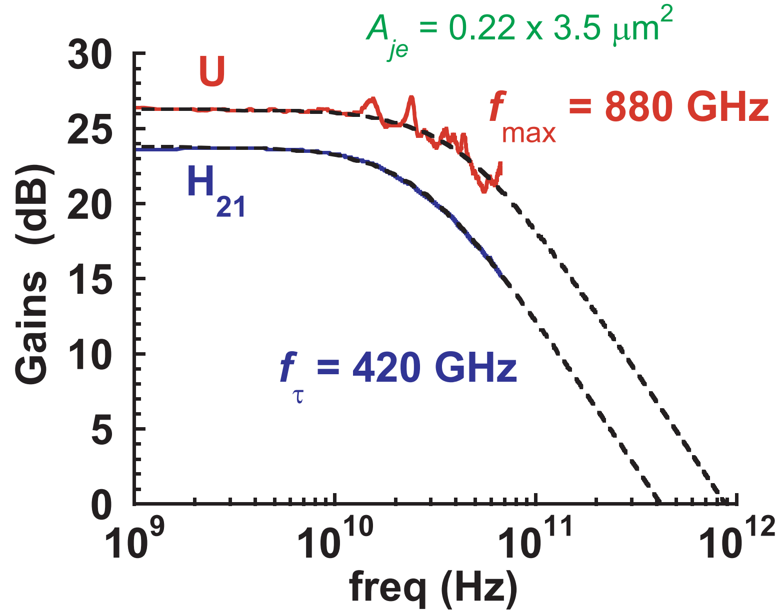


Figure 4.12: Measured RF gains for the DHBT having 220 nm emitter-base junction in 1 - 67 GHz band using off-wafer LRRM calibration

Figs. 4.10 and 4.11 show the common-emitter $I-V$ curves and Gummel characteristics for DHBT53 for devices having emitter-base junction widths of 220 nm and 120 nm respectively. HBTs with an emitter area $A_{je} = 0.22 \times 3.5\ \mu m^2$, have DC common emitter current gain $\beta = 17$ and common emitter breakdown voltage $V_{BR,CEO} = 2.5$ V ($J_e = 10\ kA/cm^2$). β is a function of emitter width and decreases with emitter size. For 120 nm emitters, β is ~ 13. Variation in DC parameters like current gain β, current carrying and power handling capabilities with emitter width for the same emitter length is mentioned in Table 4.3. Common emitter breakdown voltage for these devices was lower than expected and could be due to thin base-collector grade and high collector doping.

Properties	$270nm$	$220nm$	$170nm$	$120nm$
β	19	17	14	13
$J_{e,max}$	18.4	21.0	20.7	24.5
P_{max}	30.9	35.4	36.9	41.6
f_τ (GHz)	430	420	400	370
f_{max} (GHz)	800	880	830	720

Table 4.3: Variation in different DHBT parameters with emitter-base junction width; $J_{e,max}$ and P_{max} represent the current and power density at peak RF performance

Transmission Line Model (TLM) measurements show base $R_{sh} = 620\ \Omega/sq$ and $\rho_c < 7\ \Omega \cdot \mu m^2$ and collector $R_{sh} = 11\ \Omega/sq$ and $\rho_c < 6\ \Omega \cdot \mu m^2$. Base contact resistivity was higher than expected probably due to lithography failure at the base step and presence of possible scum. In addition, no surface preparation was done prior to base contact resistance for this sample. Emitter access resistance $\rho_{ex} < 4\ \Omega \cdot \mu m^2$ was extracted from RF data.

Fig. 4.12 shows the measured microwave gains - current gain H_{21} and Mason's Unilateral Gain (U) for a 220 nm wide device at the bias associated with peak f_τ and f_{max} for 1-67 GHz range. Peak RF performance was obtained at $I_c =$ 16.2 mA and $V_{ce} = 1.68$ V ($V_{cb} = 0.7$ V, $J_e = 21\ mA/\mu m^2$, $P = 35.3\ mW/\mu m^2$, $C_{cb}/I_c = 0.24$ psec/V). Extrapolations from single pole fit indicate $f_\tau = 420$ GHz and $f_{max} = 880$ GHz. Kirk effect is observed at $J_e = 24\ mA/\mu m^2$ ($V_{cb} = 0.7$ V) when f_τ falls to 95% of its peak value.

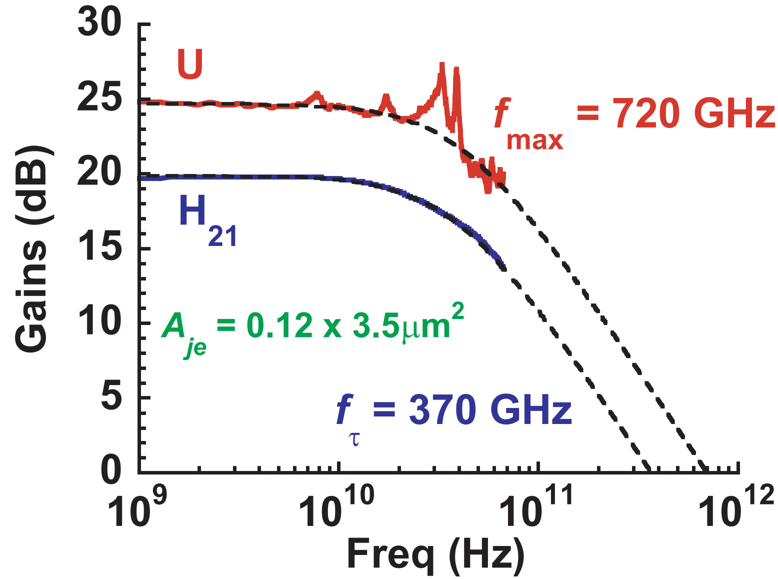
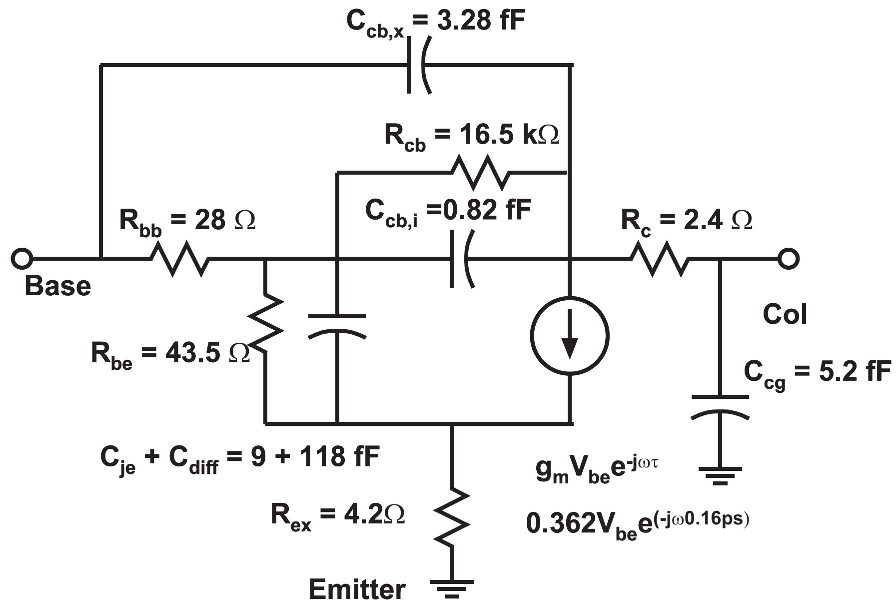


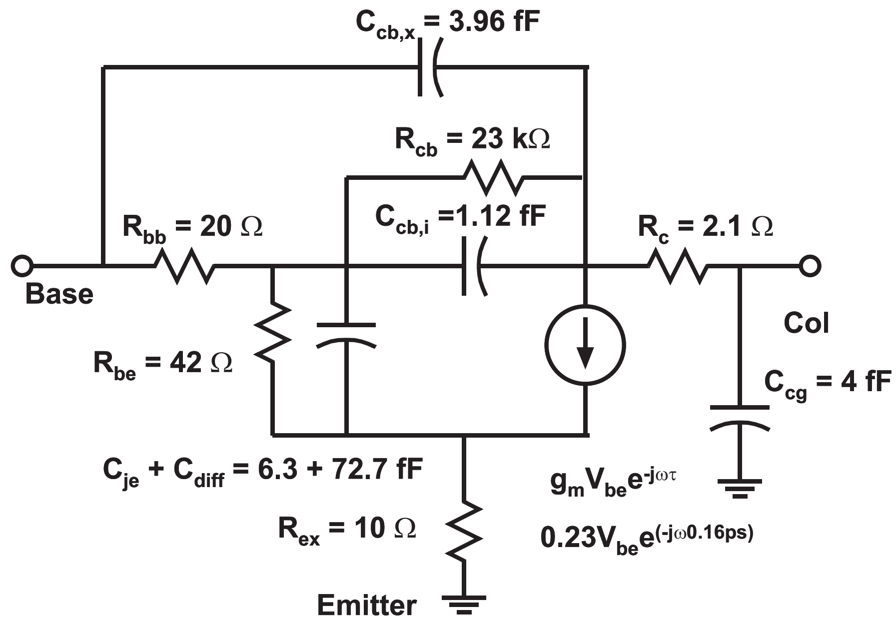
Figure 4.13: Measured RF gains for the DHBT having 120 nm emitter-base junction in 1 - 67 GHz band using off-wafer LRRM calibration

Fig. 4.13 shows the measured microwave gains - H_{21} and U for a 120 nm wide emitter-base junction. Peak RF performance was obtained at I_c = 10.3 mA and V_{ce} = 1.70 V (V_{cb} = 0.7 V, $J_e = 24.5\ mA/\mu m^2$, $P = 41.6\ mW/\mu m^2$, C_{cb}/I_c = 0.48 psec/V). Extrapolations from single pole fit indicate f_τ = 370 GHz and f_{max} = 720 GHz. Hybrid-π equivalent circuits for the two RF results shown above are given in Fig. 4.14. It can be seen from the hybrid-π circuits that 120 nm emitter HBTs have a lower f_{max} due to much higher C_{cb} than 220 nm HBTs as a result of large base mesa.

Variation in measured f_τ and f_{max} with emitter width is given in Table 4.3. f_τ is observed to decrease with emitter width due to scaled emitter-base junction



(a)



(b)

Figure 4.14: Hybrid-π equivalent circuit at peak RF performance from 1-67 GHz RF data for (a) 220 nm and (b) 120 nm wide emitter HBTs

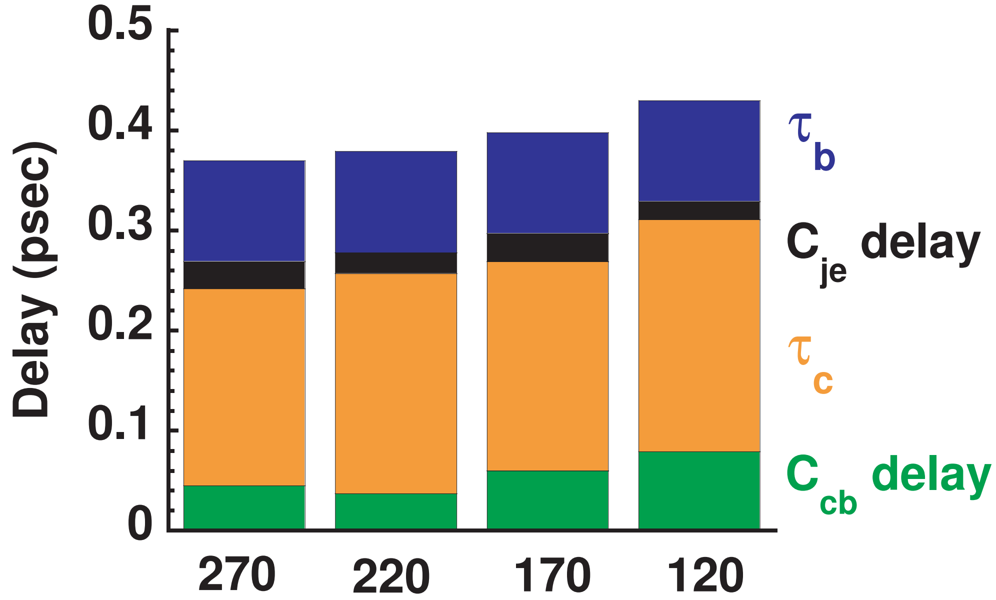


Figure 4.15: A comparison of transit and *RC* delays for four different emitter widths - 270, 220, 170 and 120 nm for same emitter length (3.5 μm) for DHBT53

width without scaling the base mesa size. Fig. 4.15 compares the transit and *RC* delays for the devices having different emitter widths - 270, 220, 170 and 120 nm for same emitter length (3.5 μm). C_{cb} delay given by $C_{cb} \cdot (R_{ex} + R_c + 1/g_m)$ increases for smaller junction widths due to increase in A_{jc}/A_{je} ratio resulting in lower f_τ where A_{jc} is the base-collector junction area and A_{je} is the emitter-base junction area. A_{jc}/A_{je} ratio is expected to remain constant with device scaling.

The devices have slightly different collector transit delay (τ_c) which is due to different collector velocity. Extracted collector velocity varies from 2.2×10^7 cm/s to 2.5×10^7 cm/s for different emitter widths. The variation is probably because of inaccurate determination of *RC* delays for the devices. It could also be an artefact

of collector current spreading. Remaining delays - base transit delay τ_b and C_{je} delay given by C_{je}/g_m approximately remain constant. Although the velocity is slightly better than that in the previous sample which could be due to different base-collector setback and grade design, it is still much lower than expected and could be due to thin setback and grade design and high doping in the collector.

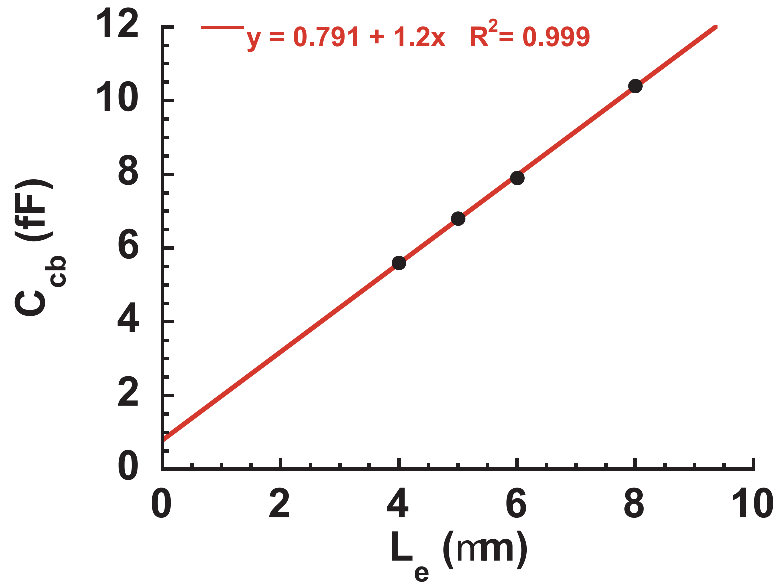


Figure 4.16: Extracted C_{cb} as a function of emitter length for the same emitter and base widths. Intercept shows $\sim$ 0.8 fF contribution to total C_{cb} from below the base post

These HBTs also have high C_{cb} values associated with them. In order to separate the C_{cb} term due to base post region, extracted C_{cb} as a function of emitter length (L_e) for the same emitter and base width was plotted. The intercept shows $C_{cb,post}$ to be $\sim$ 0.8 fF (Fig. 4.16). For a properly scaled 128 nm HBT having

100 nm thick collector, expected C_{cb} is less than 2 fF. This means, $C_{cb,post}$ needs to be reduced with scaling to improve device performance.

4.4 DHBT56

HBTs fabricated using DHBT53 epitaxial design had lower than expected collector velocity and breakdown voltage. As a result, in DHBT56, the base-collector grade and setback designs were reverted back to an old design that was successful [12]. DHBT56 design also incorporates a 100 nm thick collector and a 30 nm base. The base-collector setback and chirped-superlattice grade thicknesses were increased to 13.5 nm and 16.5 nm respectively. The collector doping was reduced to 5×10^{19} cm^{-3} similar to the growths for Teledyne Scientific. InGaAs subcollector was thinned down to 5 nm for improved thermal resistance and InP emitter was kept at 35 nm. Complete layer structure and simulated band diagram are shown in Table 4.4 and Fig. 4.17.

Dual SiN_x sidewalls, 20 nm and 30 nm thick respectively, and *ex-situ* Mo emitter contacts on IQE grown InGaAs emitter cap were used in this process. For base contacts, Pt/Ti/Pd/Au metal stack was used. It was found that Pt-based contacts are more stable to thermal cycling and give lower contact resistivity after BCB bake. Hence, Pt was used for this epitaxial design. NNH_4OH dip before base

T(nm)	**Material**	**Doping** (cm^{-3})	**Description**
10	$In_{0.53}Ga_{0.47}As$	$8 \cdot 10^{19}$: Si	Emitter Cap
20	InP	$5 \cdot 10^{19}$: Si	Emitter
15	InP	$2 \cdot 10^{18}$: Si	Emitter
30	InGaAs	$9 - 5 \cdot 10^{19}$: C	Base
13.5	$In_{0.53}Ga_{0.47}As$	$5 \cdot 10^{16}$: Si	Setback
16.5	InGaAs/InAlAs	$5 \cdot 10^{16}$: Si	B-C Grade
3	InP	$3.6 \cdot 10^{18}$: Si	Pulse Doping
67	InP	$5 \cdot 10^{16}$: Si	Collector
7.5	InP	$2 \cdot 10^{19}$: Si	Sub-Collector
5	$In_{0.53}Ga_{0.47}As$	$4 \cdot 10^{19}$: Si	Sub-Collector
300	InP	$1 \cdot 10^{19}$: Si	Sub-Collector
3.5	$In_{0.53}Ga_{0.47}As$	Undoped	Etch Stop
Substrate	SI:InP		

Table 4.4: Epitaxial layer structure of DHBT56

contact deposition was discontinued as it reacted with photoresist, thereby peeling it. Instead, sample was dipped in 1:10 solution of HCl:DI for 10 secs followed by 1 minute of DI rinse before contact deposition.

4.4.1 Base Definition Using Optical Lithography

In the first process run with DHBT56, base contacts and base mesa layers were defined using optical lithography. Fig. 4.18 shows the common-emitter $I-V$ curve and Gummel characteristics for devices having emitter-base junction width of 220 nm. HBTs with an emitter area $A_{je} = 0.22 \times 2.7\ \mu m^2$, have peak DC common emitter current gain $\beta = 20$. Common emitter breakdown voltage $V_{BR,CEO}$

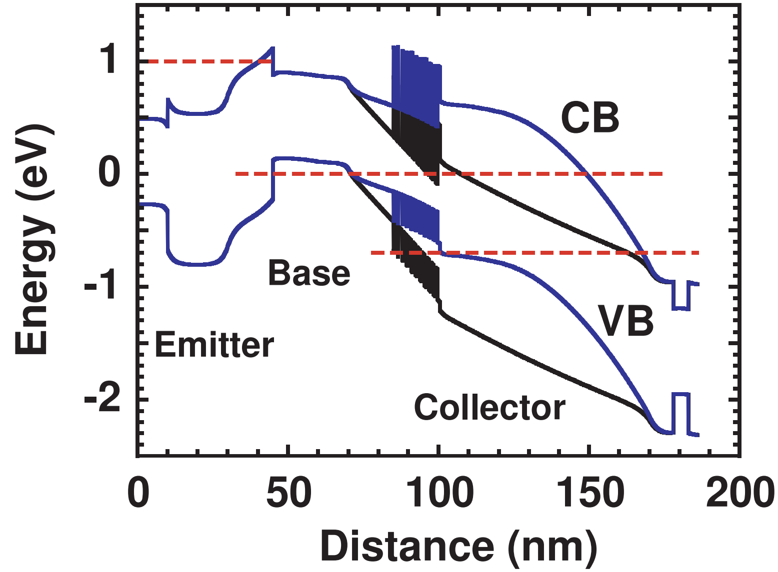
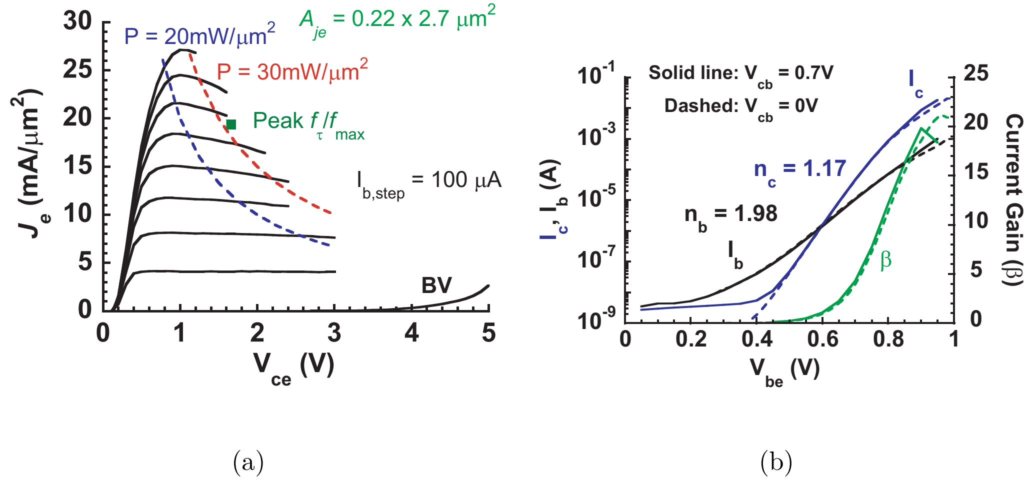


Figure 4.17: Simulated band structure of DHBT53 for $J_e = 0$ and 24 $mA/\mu m^2$, $V_{be} = 1\ V$, $V_{cb} = 0.7\ V$. Current spreading was assumed in the collector for 220 nm wide emitter-base junction

increased as was expected with the thick grade and lower collector doping and was 3.7 V ($J_e = 10\ kA/cm^2$).

Transmission Line Model (TLM) measurements show base $R_{sh} = 710\ \Omega/sq$ and $\rho_c < 5\ \Omega \cdot \mu m^2$ and collector $R_{sh} = 15\ \Omega/sq$ and $\rho_c = 22\ \Omega \cdot \mu m^2$. Higher than expected R_{sh} and ρ_c for the collector has been observed compared to previous designs presumably due to thinner InGaAs subcollector layer. Emitter access resistance $\rho_{ex} < 4\ \Omega \cdot \mu m^2$ was extracted from RF data.

Fig. 4.19 shows the measured microwave gains - current gain H_{21}, Maximum Stable Gain (MSG) and Mason's Unilateral Gain (U) at the bias associated with peak f_τ and f_{max} for 1-67 GHz range. Peak RF performance was obtained at $I_c =$



(a) (b)

Figure 4.18: (a) Common emitter $I-V$ and (b) Gummel characteristics for DHBT56 having 220 nm emitter-base junction

11.5 mA and $V_{ce} = 1.66$ V ($V_{cb} = 0.7$ V, $J_e = 19.4\ mA/\mu m^2$, $P = 32\ mW/\mu m^2$, $C_{cb}/I_c = 0.38$ psec/V). Extrapolations from single pole fit indicate $f_\tau = 460$ GHz and $f_{max} = 850$ GHz. Kirk effect is observed at $J_e = 23\ mA/\mu m^2$ ($V_{cb} = 0.7$ V) when f_τ falls to 95% of its peak value. $J_{e,max}$ and J_{kirk} are slightly lower than previous designs due to lower collector doping. f_τ improved significantly over previous results due to improved collector velocity. Extracted collector velocity for this design was $\sim\ 3.1 \times 10^7\ cm/s$ which is much more than the previous designs. Hybrid-π equivalent circuit extracted from the RF data of Fig. 4.19 is shown in Fig. 4.20.

In spite of improvement in f_τ, f_{max} was still lower than the expected value. This was because of high C_{cb} value due to large base mesa associated with the

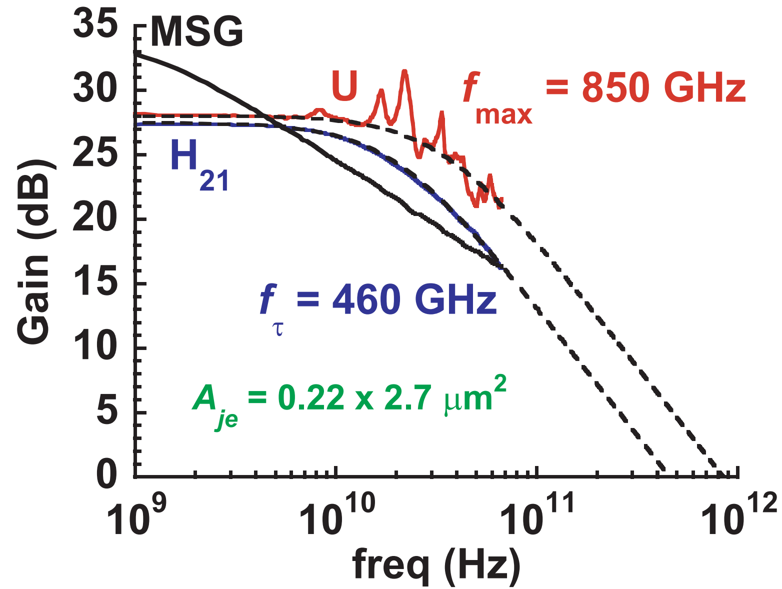


Figure 4.19: Measured RF gains 1 - 67 GHz band using off-wafer LRRM calibration

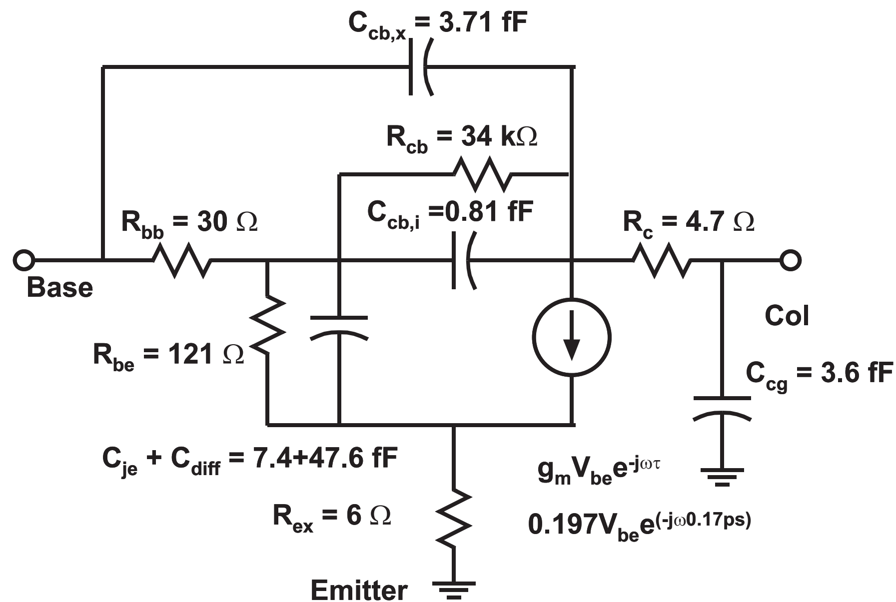


Figure 4.20: Hybrid-π equivalent circuit at peak RF performance from 1-67 GHz RF data

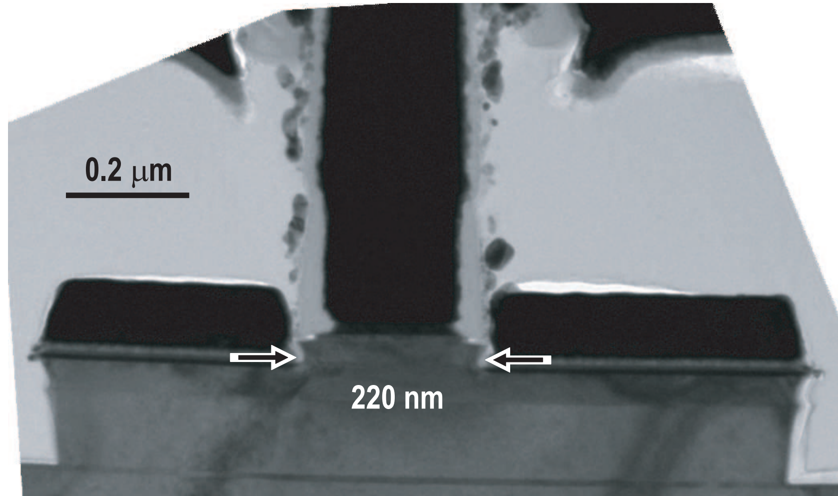
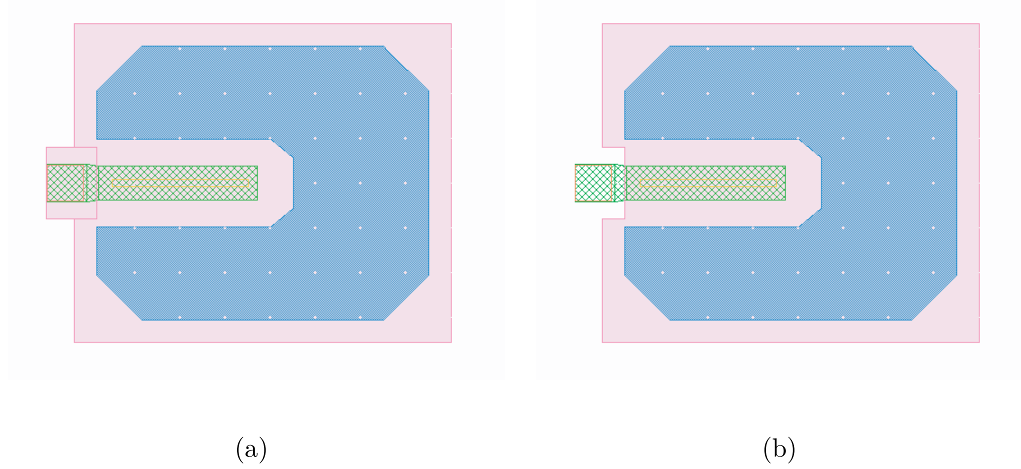


Figure 4.21: Cross-sectional TEM of the HBT showing the 220 nm emitter-base junction and greater than 1.1 μm base-collector junction

HBTs for a 220 nm emitter node. This is evident in the cross-sectional TEM of the emitter-base junction shown in Fig. 4.21 where the base mesa width is > 1.1 μm for a 220 nm wide junction.

4.4.2 Base Definition Using E-beam Writing

In the second process run using DHBT56, the emitter process was kept exactly the same as previous run. However, base contact and mesa were defined using e-beam writing. This was done to obtain a better aligned, smaller mesa. Device isolation mask design was changed as shown in Fig. 4.22(b) to increase undercut in the collector layer below the base post for reduced C_{cb}.

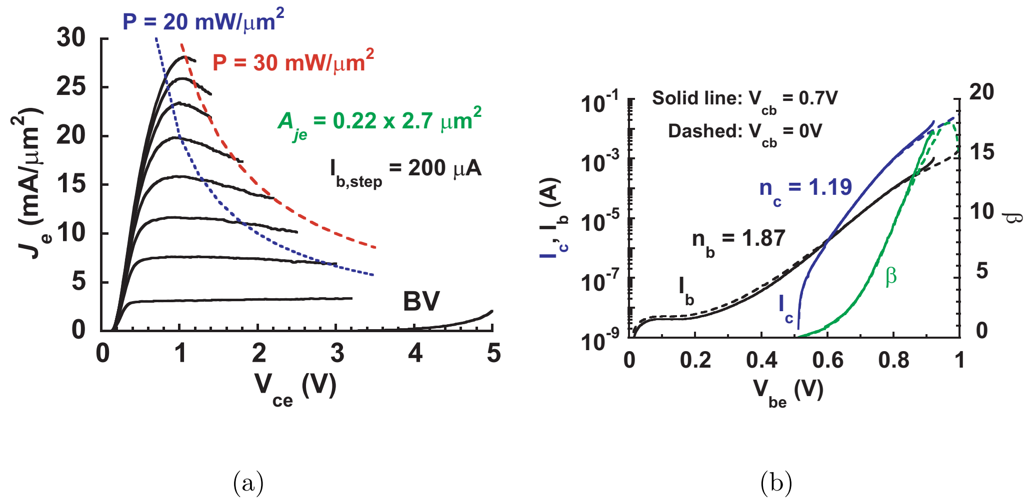


(a) (b)

Figure 4.22: HBT mask design showing the device isolation layer for (a) optical lithography and (b) e-beam writing runs. Device isolation edges were brought closer to emitter around the base post region to increase undercut in the collector region below base post

Fig. 4.23 shows the common-emitter $I-V$ curve and Gummel characteristics for devices having emitter-base junction width of 220 nm. HBTs with an emitter area $A_{je} = 0.22 \times 2.7\ \mu m^2$, have peak DC common emitter current gain $\beta = 17$ and $V_{BR,CEO} = 3.7$ V ($J_e = 10\ kA/cm^2$).

For these HBTs, RF measurements were done using *off-wafer* LRRM calibrations in the 1-67 GHz range after de-embedding associated transistor pad parasitics. Measurements were also done on an Agilent 8510XF system at Teledyne in the 80-105 GHz range using the same calibration procedure. Fig. 4.24 shows the measured gains - current gain H_{21}, Maximum Stable Gain (MSG) and Mason's Unilateral Gain (U) of the device with 220 nm wide emitter-base junction. Peak RF performance was obtained at $I_c = 12.1$ mA and $V_{ce} = 1.64$ V ($V_{cb} = 0.7$ V,



(a) (b)

Figure 4.23: (a) Common emitter $I - V$ and (b) Gummel characteristics for DHBT56 having 220 nm emitter-base junction

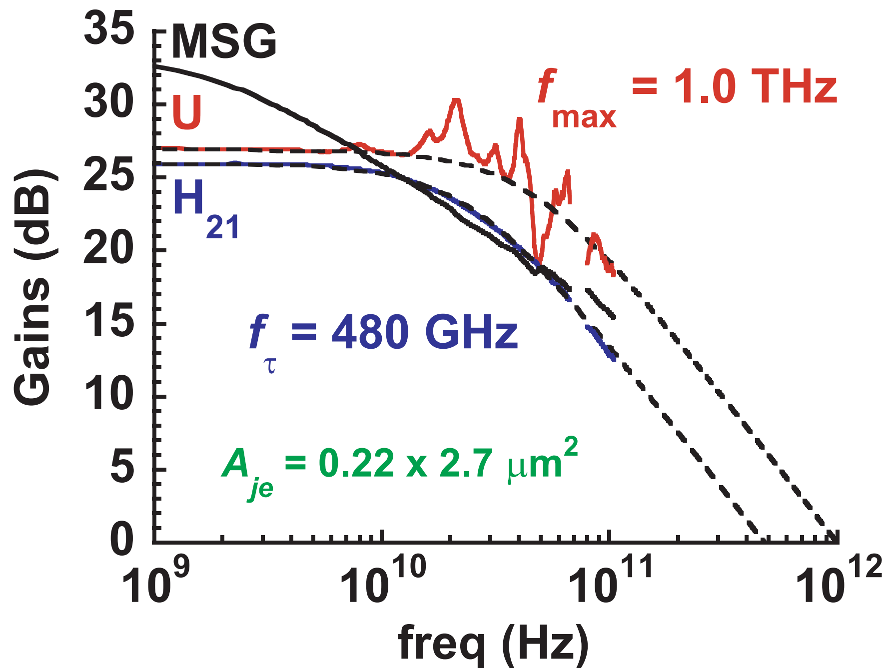
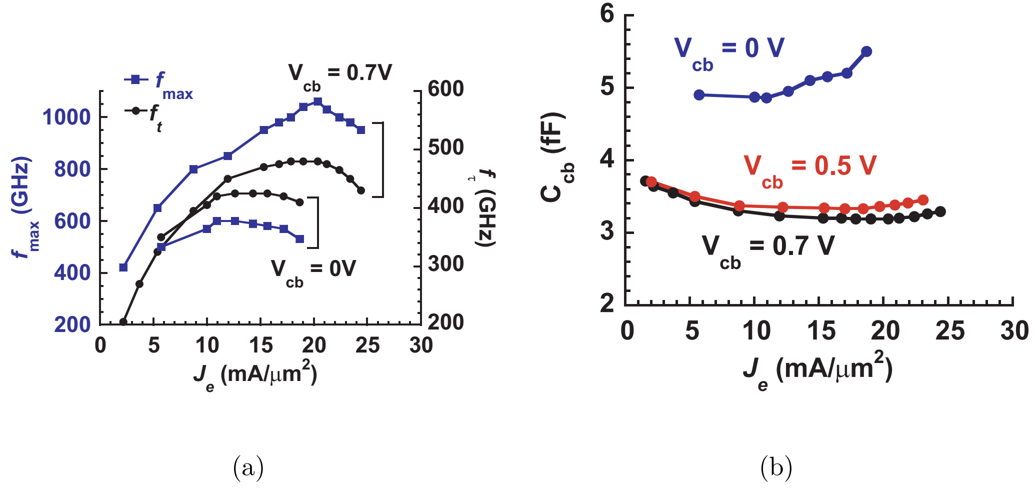


Figure 4.24: Measured RF gains in 1 - 67 GHz and 80-105 GHz bands using off-wafer LRRM calibration



(a) (b)

Figure 4.25: (a) f_τ / f_{max} and (b) C_{cb} dependence on V_{cb} and J_e

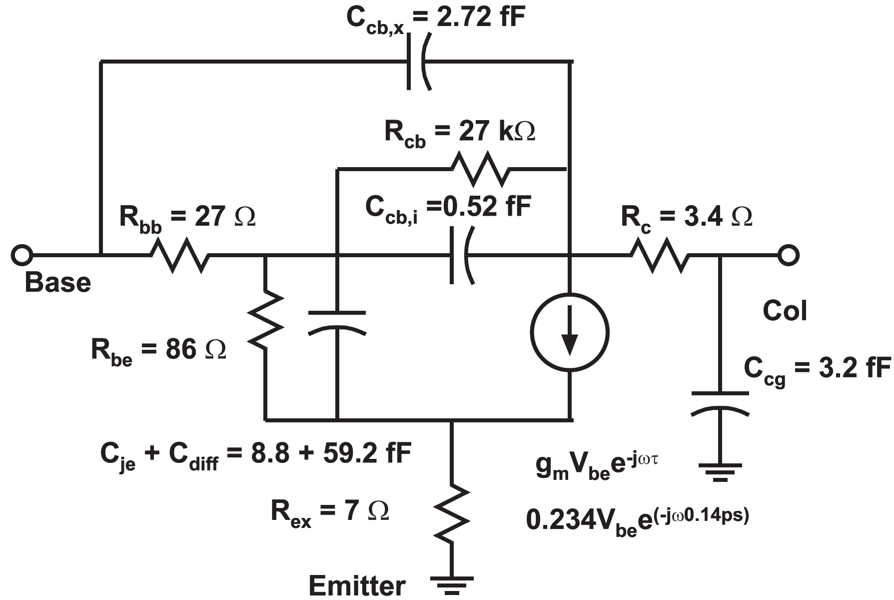


Figure 4.26: Hybrid-π equivalent circuit at peak RF performance from 1-67 GHz RF data

$J_e = 20.4\ mA/\mu m^2$, $P = 33.4\ mW/\mu m^2$, $C_{cb}/I_c = 0.264$ psec/V). Extrapolations from single pole fit indicate $f_\tau = 480$ GHz and $f_{max} = 1$ THz. Kirk

effect is observed at $J_e = 23\ mA/\mu m^2$ ($V_{cb} = 0.7$ V) when f_τ falls to 95% of its peak value. Unfortunately, base and collector TLMs could not be measured on this wafer due to BCB planarization failure over the TLM pads. Emitter access resistivity $\rho_{ex} \sim 4.5\ \Omega \cdot \mu m^2$ was extracted from RF data.

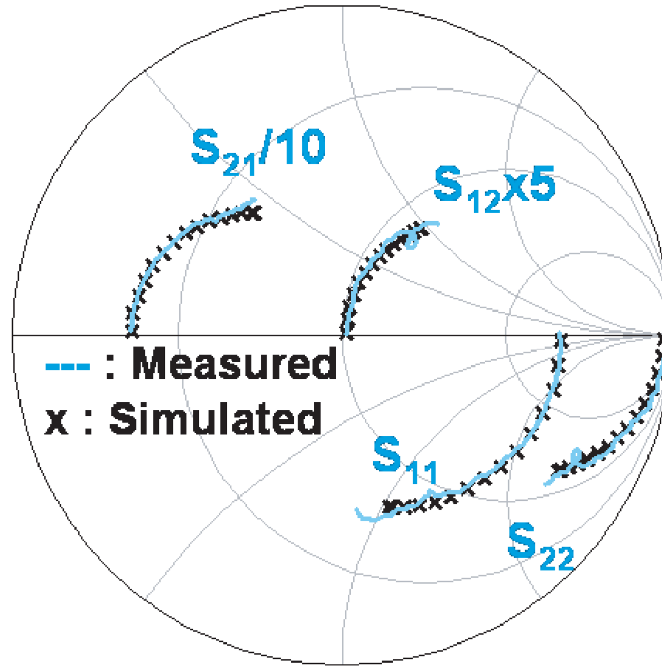


Figure 4.27: 1 - 67 GHz measured and simulated S-Parameters from equivalent circuit model in Fig. 4.26

Variation in measured f_τ/f_{max} and extracted C_{cb} with J_e for different V_{cb} values is shown in Fig. 4.25. Hybrid-π equivalent circuit extracted from 1-67 GHz RF data is shown in Fig. 4.26. Fig. 4.27 shows the match between the measured S-parameter data and calculated S-parameters from the hybrid-π equivalent circuit of Fig. 4.26.

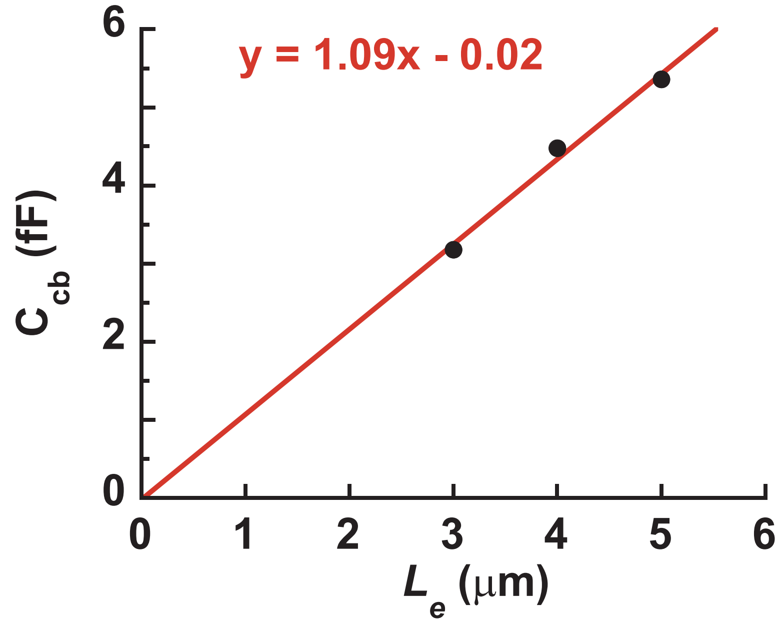
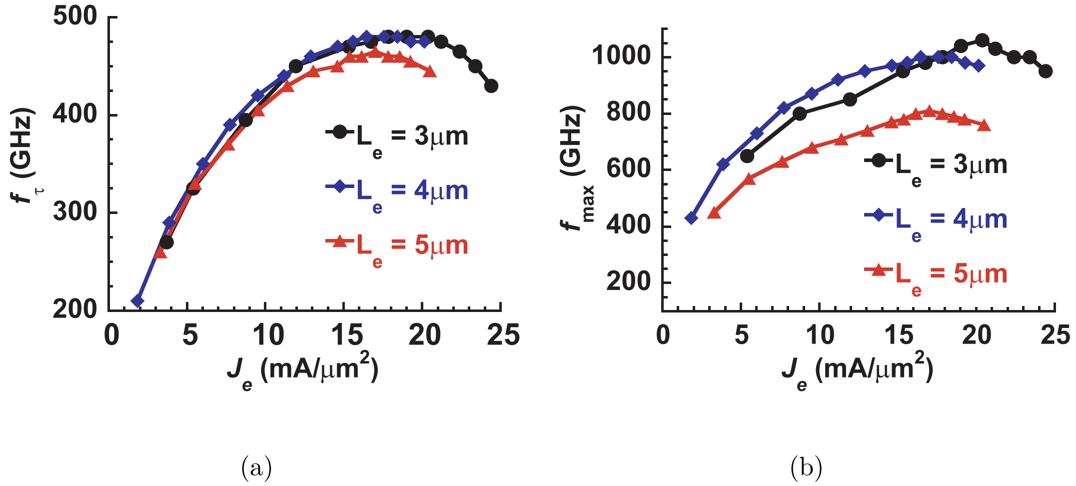


Figure 4.28: Extracted C_{cb} as a function of emitter length for the same emitter and base widths. Intercept shows no contribution to total C_{cb} from below the base post

A linear fit to the extracted C_{cb} variation with emitter length (L_e) has $\sim$ 0 fF intercept suggesting negligible capacitance contribution from the base post (Fig. 4.28). This is an improvement from the DHBT53 process run where $C_{cb,post}$ was $\sim$ 0.8 fF. This could be due to smaller base mesa definition and redesigned device isolation mask which led to undercut below the base post. This is also evident from weak dependence of f_τ on L_e; peak f_τ changes from 480 GHz to 465 GHz for L_e increase from 3 μm to 5 μm for the same emitter width (220 nm) at V_{cb} = 0.7 V (Fig. 4.29(a)). If base post capacitance was present, peak f_τ increases with emitter length [12]. Fig. 4.29(b) shows the variation in measured

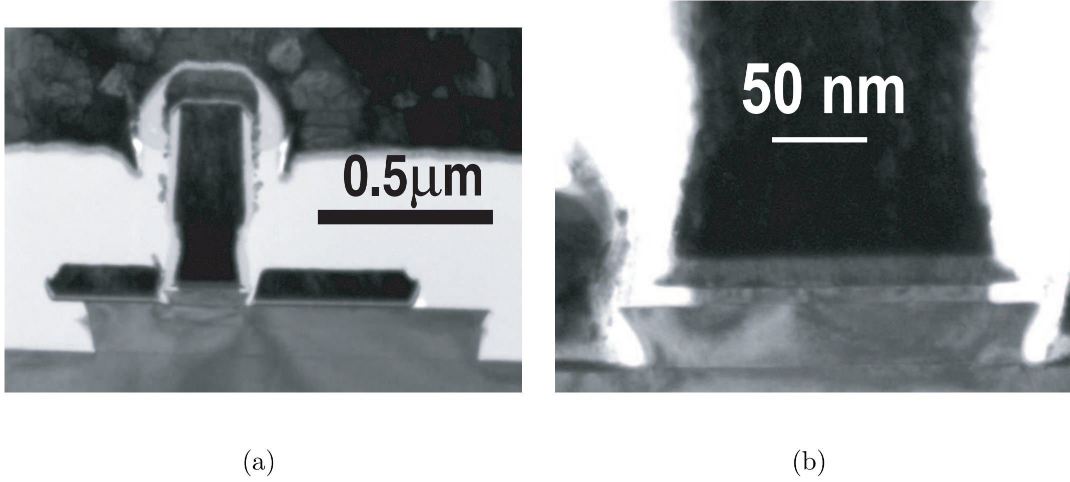


(a) (b)

Figure 4.29: Variation in (a) f_τ and (b) f_{max} with J_e for different L_e at V_{cb} = 0.7 V for DHBTs having W_e = 220 nm and same base-collector mesa width

f_{max} with emitter length. It is seen that the peak f_{max} value decreases with increase in L_e. This is probably because of finite metal resistance ($R_{bb,metal}$) in the total base access resistance (R_{bb}). For low R_{bb}, $R_{bb,metal} = R_{sh,metal} \cdot L_e/6W_{bc}$, becomes a significant fraction of the total R_{bb} and therefore f_{max} decreases with L_e.

Fig. 4.30 shows the cross-sectional FIB/TEM images of the emitter base junction demonstrating 220 nm wide junction and base-collector mesa. It can be observed from the TEM image that despite using the e-beam writer for aligning the base layer to the emitter, there still was significant misalignment in the base mesa layer. However, there was enough undercut in the collector layer below the base contact and base post to reduce total C_{cb}. R_{bb} for these devices was low due



(a) (b)

Figure 4.30: Cross-sectional TEMs of emitter and base mesas of DHBT with 220 nm emitter-base junction and 1.1 μm base-collector junction

to low resistivity base ohmic contacts and small emitter-base gap. Therefore, due to reduced C_{cb} and R_{bb} terms, measured f_{max} was greater than 1 THz even at 220 nm wide emitter with a 1.1 μm wide, misaligned base mesa.

f_τ for the devices has improved from 400 GHz for the DHBT49 sample to 480 GHz for the DHBT56 sample with e-beam base definition. Fig. 4.31 compares the transit and RC delays associated with the four devices presented – DHBT49 having 110 nm emitter junction, DHBT53 having 220 nm junction, DHBT56 having 220 nm junction and optically defined base and DHBT56 having 220 nm junction and base definition using e-beam writer. As can be observed from this plot, this improvement has been mostly due to significant reduction in collector transit delay due to improved carrier velocity. The remaining delays - τ_b, C_{cb} delay

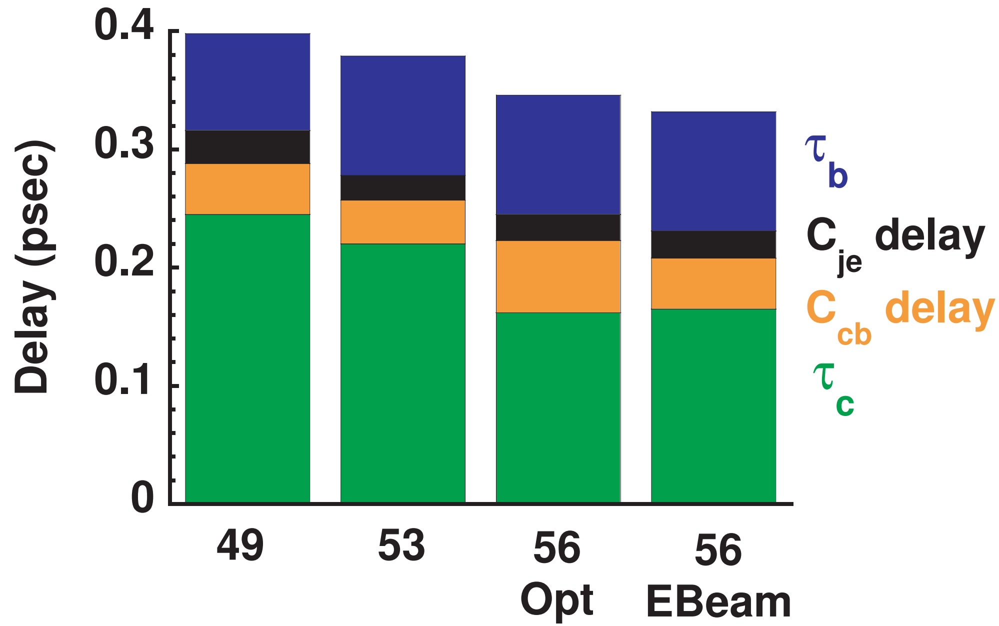


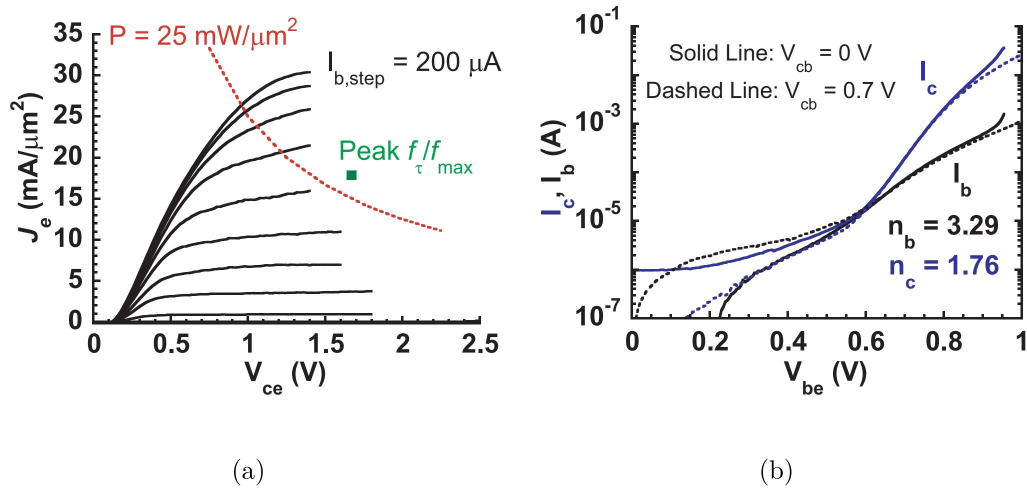
Figure 4.31: A comparison of transit and RC delays for the four device results discussed previously - DHBT49, DHBT53 and the two DHBT56 results

and C_{je} delay have not changed much. C_{cb} delay is actually higher for DHBT56 devices due to higher collector resistance for these devices.

Another important observation is that transit delays dominate RC delays for all the devices. This shows that the collector and base thicknesses are much more than that required for this scaling generation and need to be scaled for future devices for increased f_τ.

4.5 Next Generation DHBTs

As discussed in Chap. 3, a new planarization and etch-back base process flow incorporating refractory base ohmics for next generation DHBTs was implemented using DHBT53 epi. To achieve low base contact resistance using refractory metals, very high base doping ($> 1.5 \times 10^{20}\ cm^{-3}$) is required. Since an epitaxial design with very high base doping was unavailable, the new process flow was tested using Pd/W contact layer for base contacts to obtain low contact resistivity. In this process, 1.0 nm Pd was deposited by e-beam evaporation followed by 20 nm sputtered W deposition. The remainder of the process flow is as discussed in Chap. 3. The layer structure for DHBT53 is given in Table 4.2.



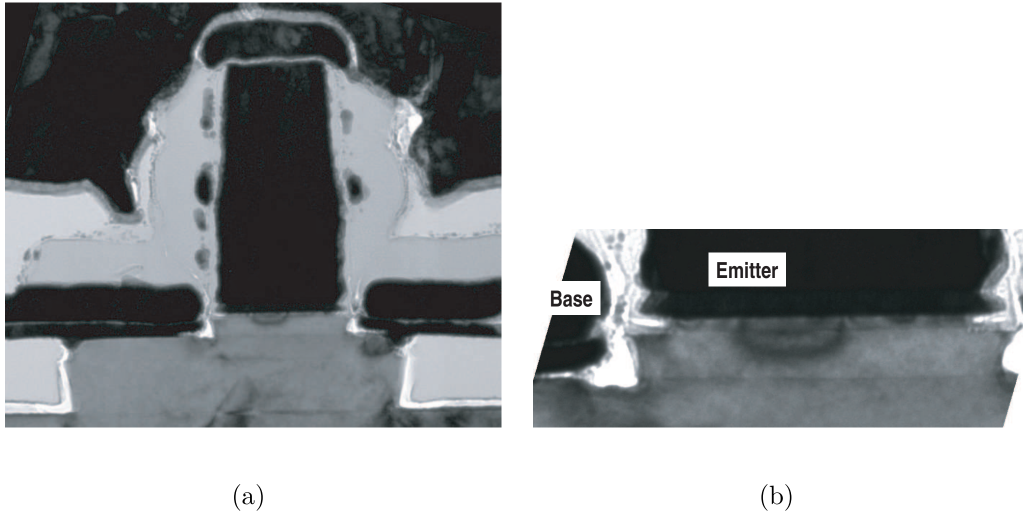
(a) (b)

Figure 4.32: (a) Common emitter $I-V$ and (b) Gummel characteristics for DHBTs having Pd/W base contacts

Fig. 4.32 shows the common-emitter $I-V$ curves and Gummel characteristics for DHBT53 devices having emitter-base junction width of 220 nm. HBTs with an emitter area $A_{je} = 0.22 \times 5.7\ \mu m^2$, have DC common emitter current gain $\beta =$ 26 and common emitter breakdown voltage $V_{BR,CEO} = 2.4$ V ($J_e\ =\ 1\ kA/cm^2$). Base and collector ideality factors n_b/n_c for these devices are high at 3.29 and 1.76. This could be due to poor passivation and base surface damage as is evident from TEM images in Fig. 4.33. n_c could be high due to presence of a thin dielectric film at the metal-metal interface as discussed later. Due to processing problems, it was not possible to measure base and collector TLMs on this sample. Hence, the exact contact and sheet resistance for the base and collector cannot be estimated. Emitter access resistance $\rho_{ex}\ =\ 6\ \Omega \cdot \mu m^2$ was extracted from RF data. The extracted ρ_{ex} is higher than previous samples and is believed to be due to high metal-metal resistance. Its possible that the thin Pd base contact layer on top of the emitter was fluorinated during W-planarization step and increased the resistance between Ti/Au layer and emitter metal. This should not be a problem with pure W base contacts.

Fig. 4.34 shows the measured microwave gains - current gain H_{21}, MSG, and Mason's Unilateral Gain (U) at the bias associated with peak f_τ and f_{max} for 1-67 GHz range. Peak RF performance for HBTs with $A_{je} = 0.22 \times 5.7\ \mu m^2$ was obtained at $I_c = 22.4$ mA and $V_{ce} = 1.67$ V ($V_{cb} = 0.7$ V, $J_e\ =\ 17.9\ mA/\mu m^2$,

$P = 30\ mW/\mu m^2$). Extrapolations from single pole fit indicate $f_\tau = 410$ GHz and $f_{max} = 690$ GHz. Kirk effect is observed at $J_e = 21\ mA/\mu m^2$ ($V_{cb} = 0.7$ V) when f_τ falls to 95% of its peak value. Hybrid-π equivalent circuit for the peak RF performance is shown in Fig. 4.35. It can be observed from the equivalent circuit that these devices have a high R_{bb} resulting in lower f_{max}.



(a) (b)

Figure 4.33: Cross-sectional TEMs of emitter and base mesas of DHBT fabricated using Pd/W base contacts

Fig. 4.33 shows the cross-sectional FIB/TEMs of emitter-base junction and base-collector mesa for these HBTs. There are quite a few failure points that can be observed in these TEMs. There is significant damage to the exposed base layer between the emitter semiconductor and base metal which reduced the device f_{max} and increased ideality factors. Base surface damage could be from the plasma during PECVD of SiN_x for protecting the W base. It is possible that the SiN_x

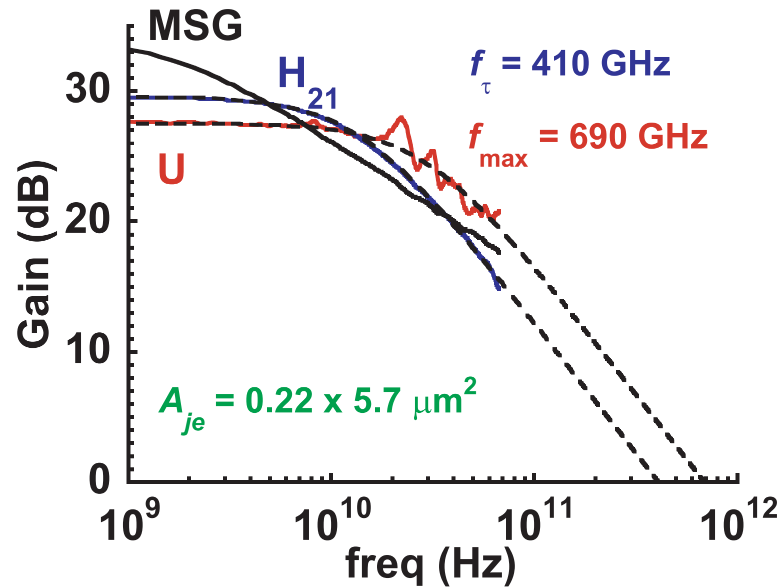


Figure 4.34: Measured RF gains for the DHBT fabricated using Pd/W base contacts in 1 - 67 GHz band using off-wafer LRRM calibration

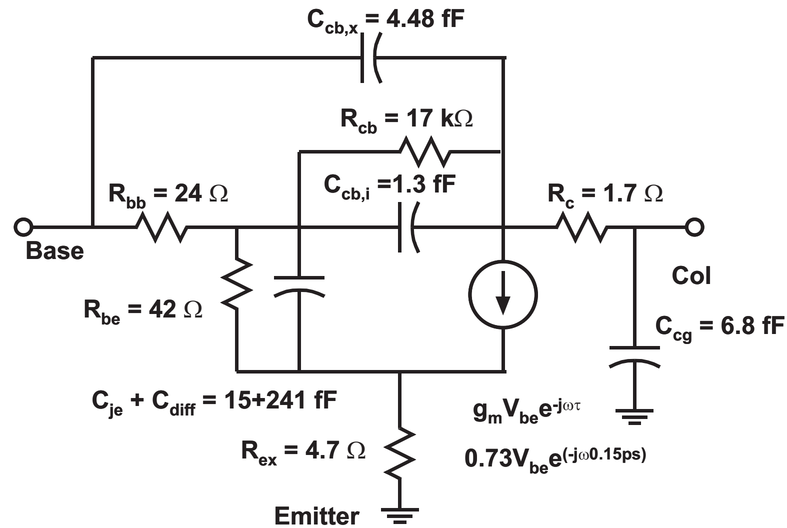


Figure 4.35: Hybrid-π equivalent circuit at peak RF performance from 1-67 GHz RF data for DHBTs having Pd/W base contacts

deposition is non-conformal leaving cracks through which wet etchants during the base mesa etch might have seeped through, etching the base. Damage to the base could also be from the oxygen plasma after the planarization step to remove scum. It can also be observed that the base metal stack is peeling off from near the emitters which further increased R_{bb}. This could again be due to cracks in SiN_x protection layer as mentioned before or it is possible that W doesn't stick well on Pd and its the W peeling off but not Pd. All these are speculations at this point and more samples without Pd need to be processed to identify the cause. Also, there is significant undercut in the base mesa below the base contact resulting in almost one-sided base contacts which needs to be controlled in future runs. BCB adhesion to the substrate and on the sides of the mesas is also an issue (Fig. 4.33(a)) which needs to be addressed.

4.6 Resonances in Mason's Unilateral Gain

Several resonance peaks and dips can be observed in measured Mason's Unilateral Gain (U) data in the previous sections. This is believed to be due to the *off-wafer* calibration standard used for the measurement and the shared ground pad structure. Fig. 4.36 shows the pad layouts for the measured devices. It can be observed that the ground pad is shared between devices and in an actual wafer

there are 30 devices sharing a common ground pad. To check the effect of shared ground planes, one of the devices was isolated by cutting through the ground plane using FIB (Fig. 4.37). The S-parameters of the device under identical bias conditions and calibration technique were then remeasured.

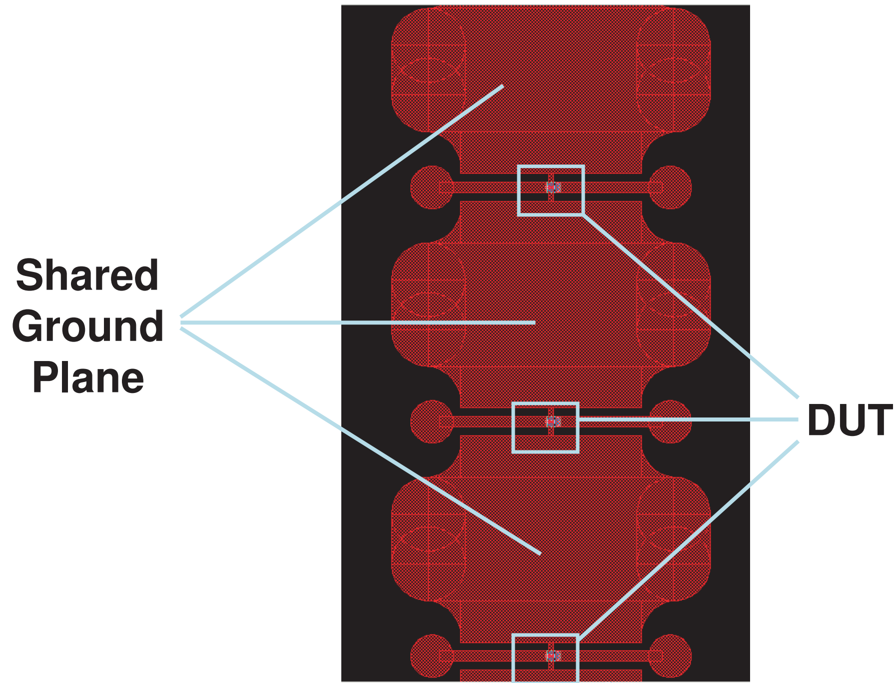


Figure 4.36: Mask layout of the DHBTs having a shared ground plane. The image shows 3 DHBTs embedded out of a total 30 DHBTs

Fig. 4.38 shows the measured Mason's Gain (U) data of the same device ($A_{je} = 0.22 \times 4.7\ \mu m^2$) with the shared ground pad and after isolating (splitting) the ground pad. The same bias conditions for the two measurements were identical – $I_c = 16.7\ mA$, $V_{cb} = 0.7\ V$. Multiple single-pole curve fits to the measured U data for isolated ground plane structure is shown in Fig. 4.39. It can be observed

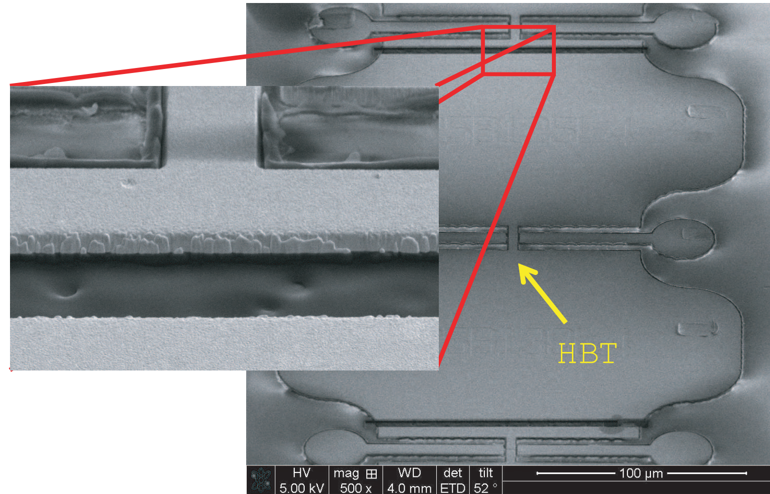


Figure 4.37: SEM of the HBT with isolated ground plane created using FIB

that with the split ground plane, the resonances at low frequency (< 30 GHz) are no longer present. However, the measured curve does not follow a single pole fit beyond 25 GHz which is problematic. Hence, accurate determination of device f_{max} is not possible for both the pad structures due to resonances in the data. These resonances are probably due to the *off-wafer* calibration technique used. Improved *on-wafer* calibration procedures are required to obtain noise free measurements. One of the techniques used is *on-wafer* TRL calibration to be discussed in the next section. Clean RF measurements can be obtained using TRL calibrations as reported in [12, 13].

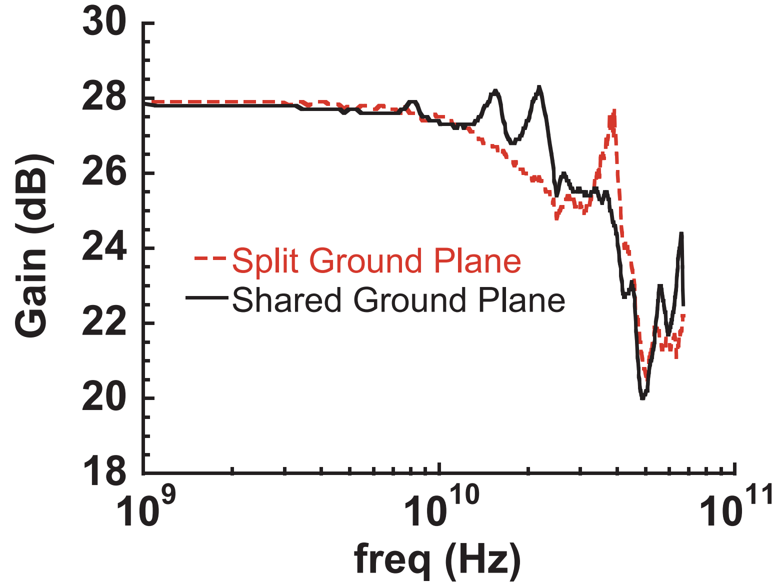


Figure 4.38: Measured Mason's Gain U for a device with $A_{je} = 0.22 \times 4.7\ \mu m^2$ at $I_c = 16.7\ mA$, $V_{cb} = 0.7\ V$ with shared and split ground plane

4.7 High Frequency Measurements

DHBT RF results discussed in this chapter so far were measured using *off-wafer* LRRM calibration in 1-67 GHz band as discussed in Section 4.1. High frequency device measurements are needed for transistors having high cut-off frequencies as noise in the low frequency measurements makes it impossible to accurately determine the extrapolated f_τ and f_{max}. However the same *off-wafer* probe tip calibrations are generally not preferred for frequencies greater than 50 GHz as the error-terms associated with the *off-wafer* calibrations become significant at higher frequencies corrupting the measurements [1, 14]. The probe spacing between the calibration standards is of a distance where electro-magnetic field coupling

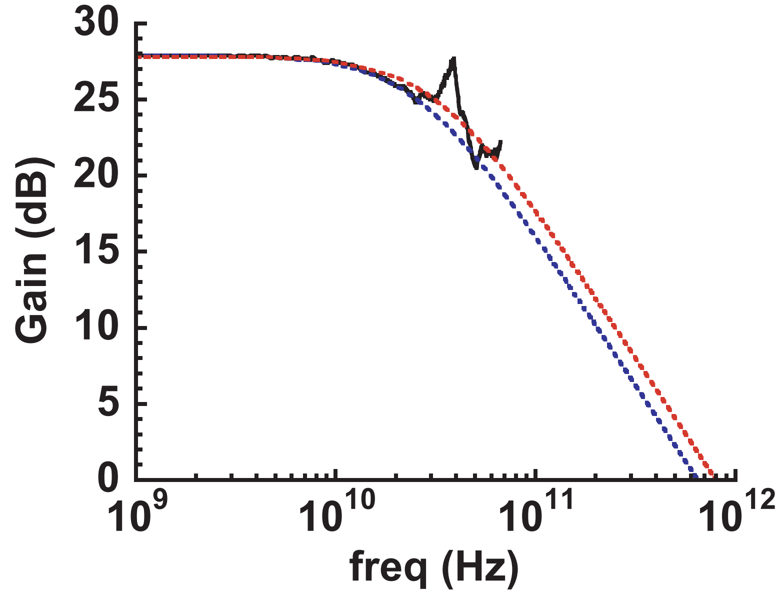


Figure 4.39: Measured Mason's Gain U for a device with split ground plane at $I_c = 16.7\ mA, V_{cb} = 0.7\ V$ having $A_{je} = 0.22 \times 4.7\ \mu m^2$. The measured data does not follow the single pole fit and multiple single pole fit curves can be used to extract different f_{max}

between port 1 and port 2 is experienced. If the coupling is constant and same for all standards measured during the calibration, their effects are calibrated out. At frequencies greater than 50 GHz, this is not a reasonable expectation. The signal-line spacing between the probe-pad and terminals of the device needs to be increased to lessen the effects of the fringing fields. This results in increased pad parasitics from the open and short pads and de-embedding them leads to significant errors. Thus *on-wafer* calibration structures are preferred for high frequency device measurements as the calibration structures are embedded in the same wiring environment as the devices (transmission lines, substrate etc.) and

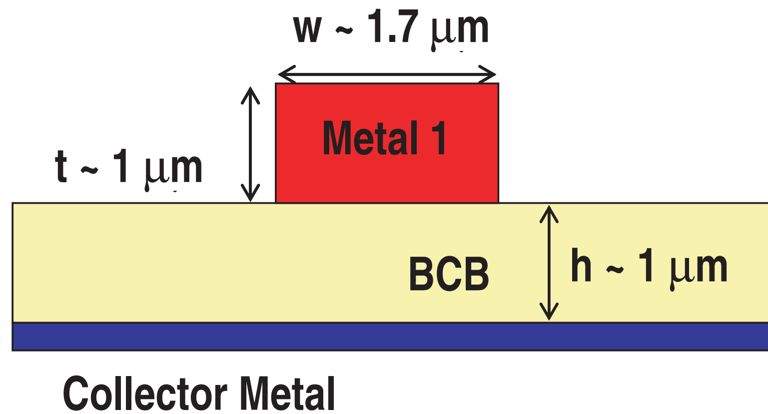
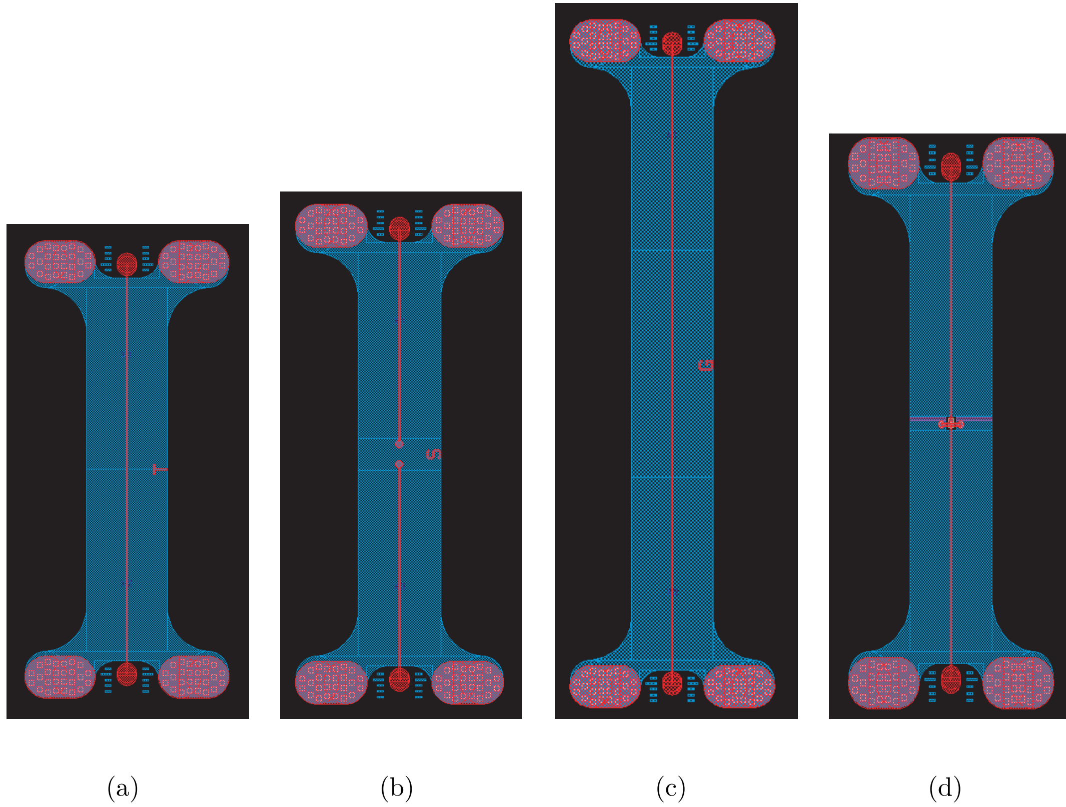


Figure 4.40: Cross-sectional schematic of the thin film, microstrip style TRL structures. Ground plane is formed in collector metal and M1 forms the signal line separated by $\sim 1\ \mu m$ BCB

the reference planes are directly set at the device terminals without any need for parasitic de-embedding resulting in more accurate and repeatable calibration standards. The trade-off of this approach is that the realization of precision calibration standards repeatably on the substrate over numerous process runs may be challenging and require some post-processing of the S-parameter data to account for such deviations between the expected and realized calibration standard values.

Thru-Reflect-Line (TRL) calibration technique is generally preferred for *on-wafer* calibration as it does not require an accurate characterization of all the calibration standards. The only parameter that must be known is the characteristic impedance (Z_0) of the *Line* standard. This characteristic impedance becomes the reference impedance for calibrated measurements, and it is important to real-



(a) (b) (c) (d)

Figure 4.41: Top view of the three calibration standards (a) Through (b) Short (c) Line and (d) DUT pads

ize that this impedance has frequency dependent real and imaginary parts. Z_0 in our case is obtained using electromagnetic simulation software. Alternatively, it can be calculated from measurements of the capacitance and propagation constant of *line* standard [15, 16]. The calibration uses two transmission line standards one of which is designated *Through*, and the other of which is designated *Line*. The *Line* standard differs from the *Through* by some electrical length ΔL generally kept at $\lambda_g/4$ at the center of frequency span. The Reflect standard may be an

open or short circuit termination. Multiple *line* standards can be used to provide measurement redundancy in a band and to reduce errors due to probe placement repeatability [17].

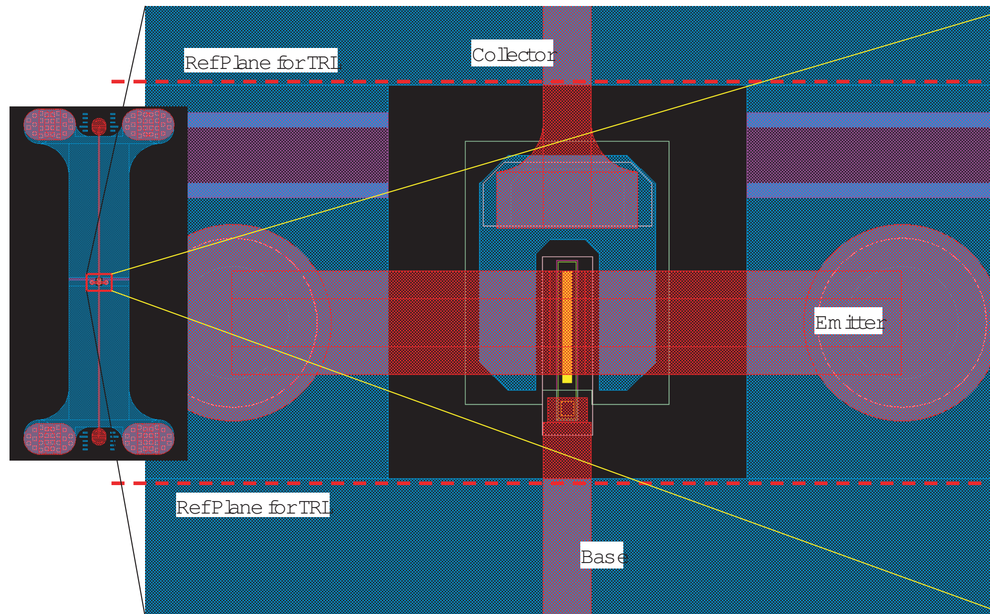


Figure 4.42: Magnified view of the device embedded in the TRL structure showing the signal lines for collector and base posts and emitter ground plane. Reference plane for device measurements after calibration is set at the device terminals

In our process run, TRL calibration was implemented using thin microstrip transmission lines. Ground plane was formed using collector metal and signal line was in Metal 1. A cross-section of the TRL structure is shown in Fig 4.40. Length of the *through* was 237 μm and *line* standard was $\lambda_g/4$ longer than the thru standard where λ_g depends on the band of interest. The TRL standards used

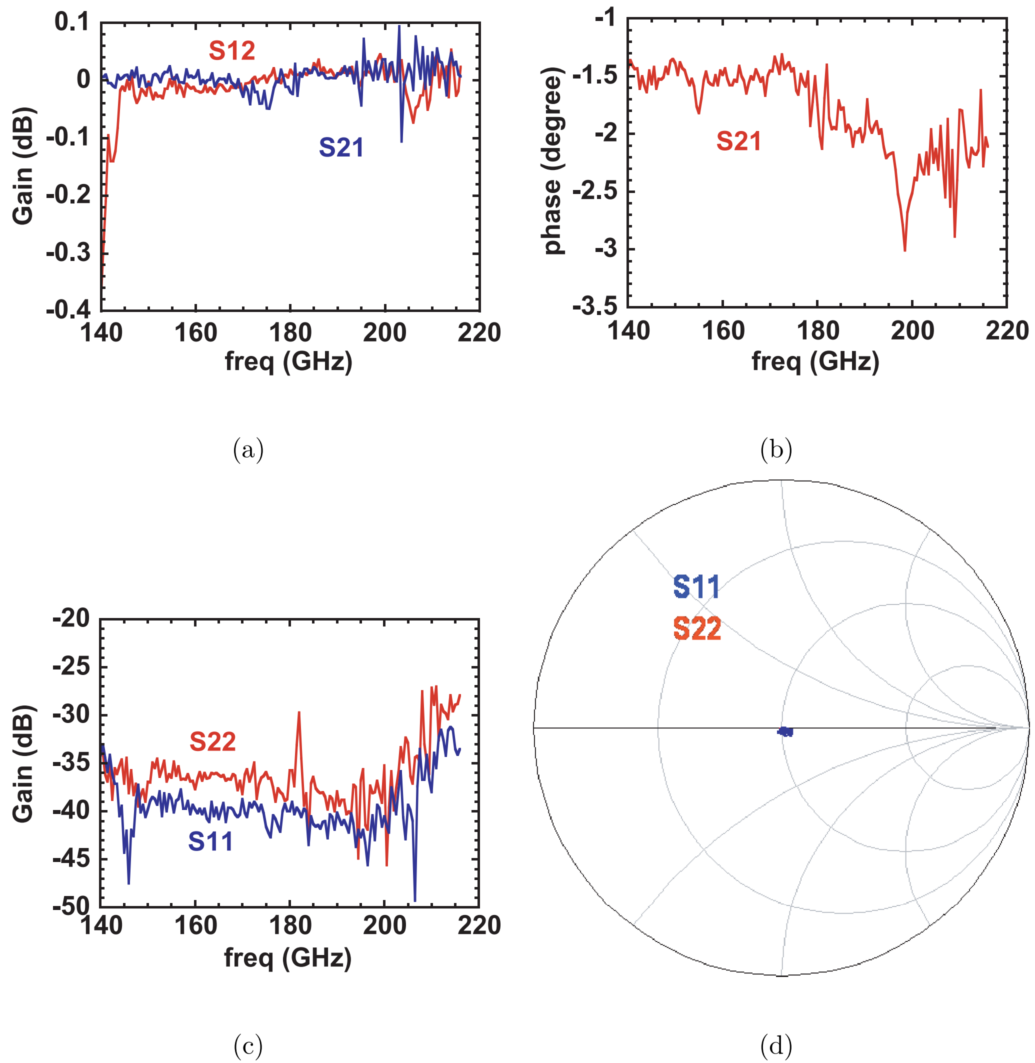


Figure 4.43: S-paramters of the *through* standard measured after calibration. Good calibration is obtained in the 145-180 GHz range where the insertion and return losses are low

in these measurements are shown in Figs. 4.41 and 4.42. The design of these TRL structures was done by Evan Lobisser and Sebastian Bartsch.

Calibrations were done in WR5 (140-220 GHz) band using *on-wafer* thin film microstrip style TRL structures. After calibrations the *through* and *line* structures were measured again to check the quality of the calibration. Measured data from these calibration structures is shown in Figs. 4.43 and 4.44. Good calibration was obtained in the 145-180 GHz range. The calibration appears unsatisfactory beyond this range and could be due to dynamic range limitations of the PNA or limitations of the *on-wafer* calibration structures or the frequency multiplier modules. This is evident from the remeasured *line* and *through* calibration standards. In 145-180 GHz range, the *through* line shows a return loss better than -35 dB and insertion loss better than 0.1 dB. The phase of S_{21} and S_{12} is less than $2°$. The *line* standard shows a return loss better than - 30 dB and insertion loss less than - 1.5 dB. The phase of S_{21} and S_{12} is linear with less than $2°$ variation in the mentioned band. The phase is $90°$ for the *line* standard at a frequency of $\sim$ 160 GHz which is slightly lower than the designed frequency of 180 GHz.

Using this calibration, DHBTs having identical emitter length (3.5 μm) and width (110 nm), embedded in TRL structures were measured for DHBT49 sample. The measurements directly give the device S-parameters without any need for pad parasitic de-embedding. Device current gain H_{21} and mason's unilateral gain U

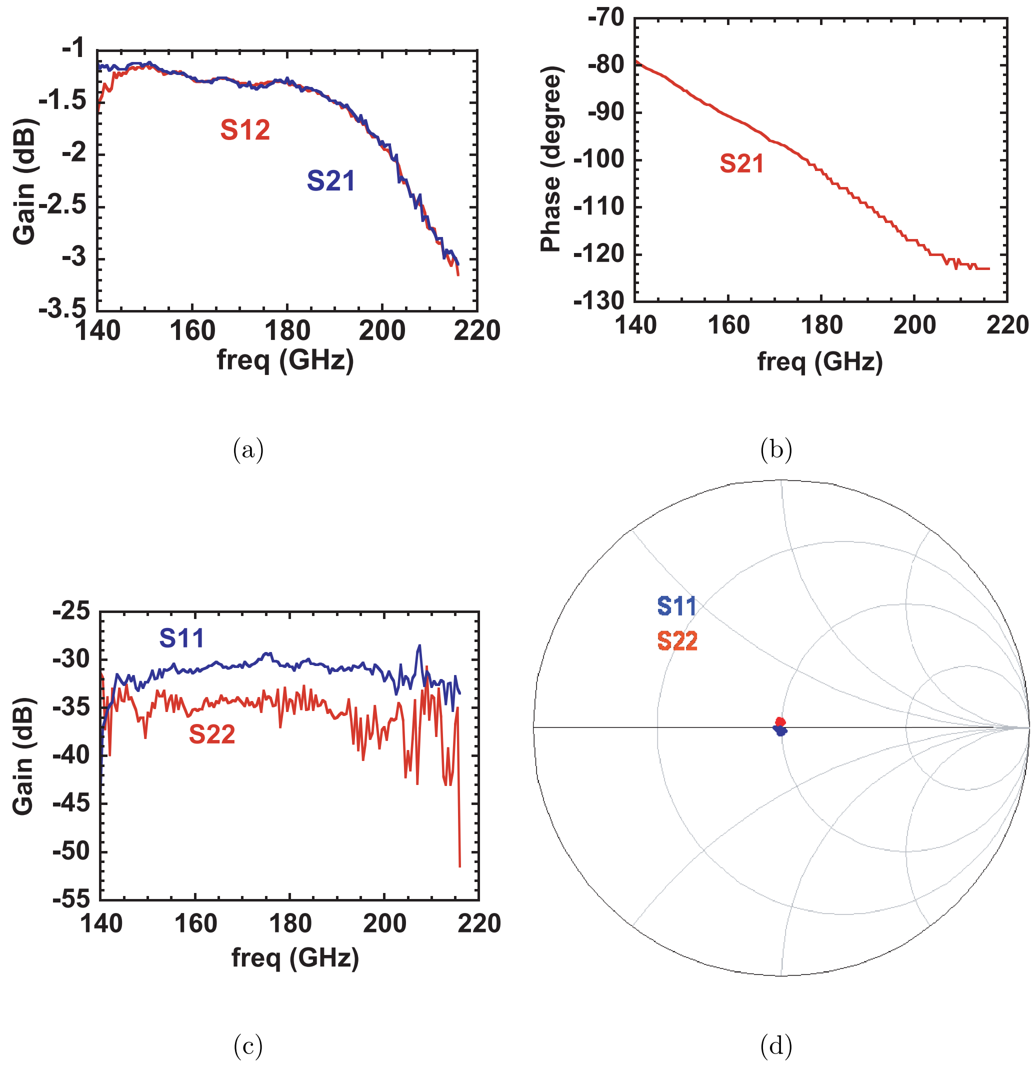


Figure 4.44: S-paramters of the *line* standard measured after calibration. Good calibration is obtained in the 145-180 GHz range where the insertion and return losses are low and S_{21} phase is linear

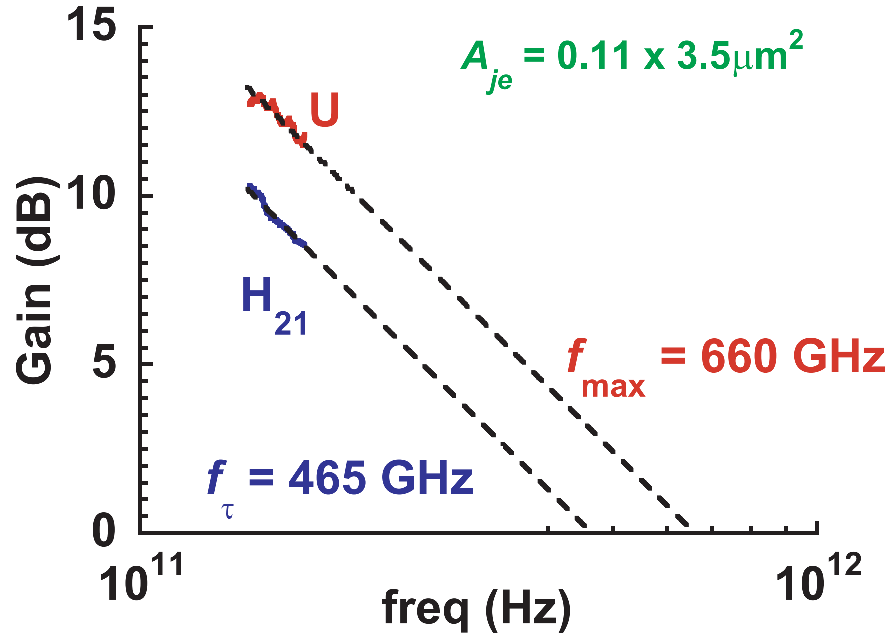


Figure 4.45: Measured RF gains for the DHBT having $A_{je} = 0.11 \times 3.5\mu m^2$ in 145 - 180 GHz band using on-wafer TRL calibration

T(nm)	Material	Doping (cm^{-3})	Description
25	$In_{0.53}Ga_{0.47}As$	$8 \cdot 10^{19}$: Si	Emitter Cap
10	$In_{0.53}Ga_{0.47}As$	$5 \cdot 10^{19}$: Si	Emitter Cap
50	InP	$5 \cdot 10^{19}$: Si	Emitter
15	InP	$2 \cdot 10^{18}$: Si	Emitter
25	InGaAs	$7 - 4 \cdot 10^{19}$: C	Base
4.5	$In_{0.53}Ga_{0.47}As$	$9 \cdot 10^{16}$: Si	Setback
10.8	InGaAs/InAlAs	$9 \cdot 10^{16}$: Si	B-C Grade
3	InP	$6 \cdot 10^{18}$: Si	Pulse Doping
81.7	InP	$9 \cdot 10^{16}$: Si	Collector
7.5	InP	$1 \cdot 10^{19}$: Si	Sub-Collector
7.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Sub-Collector
300	InP	$2 \cdot 10^{19}$: Si	Sub-Collector
3.5	$In_{0.53}Ga_{0.47}As$	Undoped	Etch Stop
Substrate	SI:InP		

Table 4.5: Epitaxial layer structure of DHBT51

were obtained from the S-parameters and cut-off frequencies f_τ and f_{max} were extrapolated using - 20 dB/decade curve fits. Peak RF performance was obtained at I_c = 9.1 mA and V_{ce} = 1.75 V (V_{cb} = 0.7 V, J_e = 23.6 $mA/\mu m^2$, P = 41.3 $mW/\mu m^2$, C_{cb}/I_c = 0.43 psec/V). Extrapolations from - 20 dB/decade fit indicate f_τ = 465 GHz and f_{max} = 660 GHz as shown in Fig. 4.45.

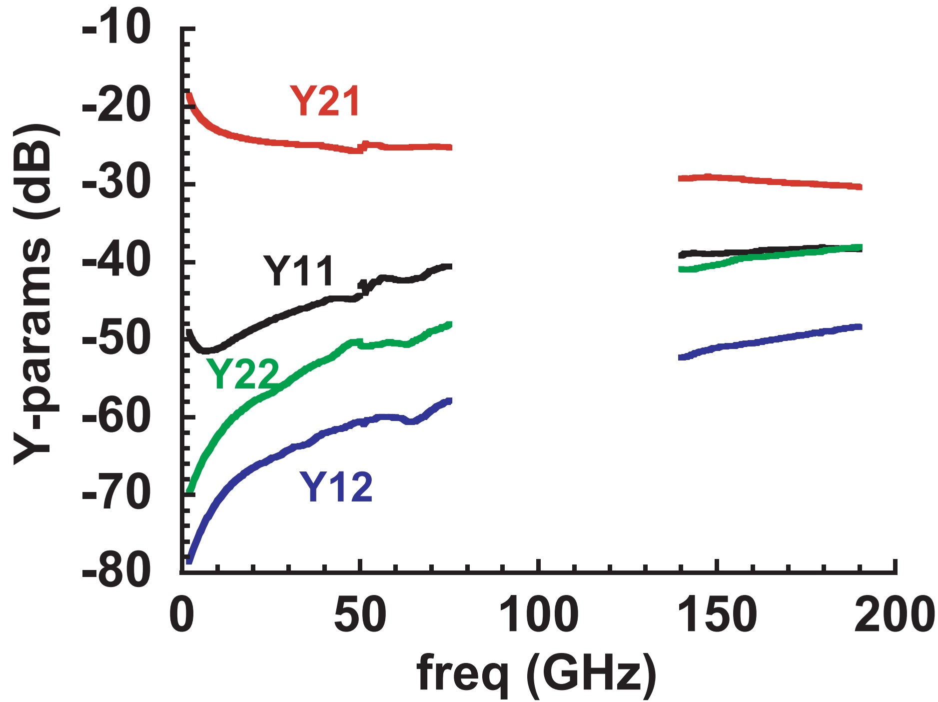


Figure 4.46: Measured Y-parameters for the DHBT having $A_{je} = 0.23 \times 1.7 \mu m^2$ in 2-50 GHz, 50-75 GHz and 140-190 GHz bands after *on-wafer* TRL calibration. Good agreement in the measured data across the bands can be observed

TRL calibration methods were also used to measure device performance in 2-50 GHz and 50-75 GHz bands. Same *through* and reflect standards as the ones employed for WR5 measurements were used. The *line* standard was appropriately

changed depending on the measurement band. This was done to compare the DHBT performance across different bands and also to check the accuracy of the TRL calibrations. For these measurements, DHBT51 sample was used. The layer structure of DHBT51 is shown in Table 4.5. Fig. 4.46 shows the measured Y-parameters for different frequency bands 2-50 GHz, 50-75 GHz and 140-185 GHz after on-wafer TRL calibration. It can be observed that a good match is obtained across bands showing the accuracy of the TRL standards. The data shown is for a HBT having $A_{je} = 0.23 \times 1.7 \mu m^2$ at $I_c = 6.3$ mA and $V_{cb} = 0.7$ V.

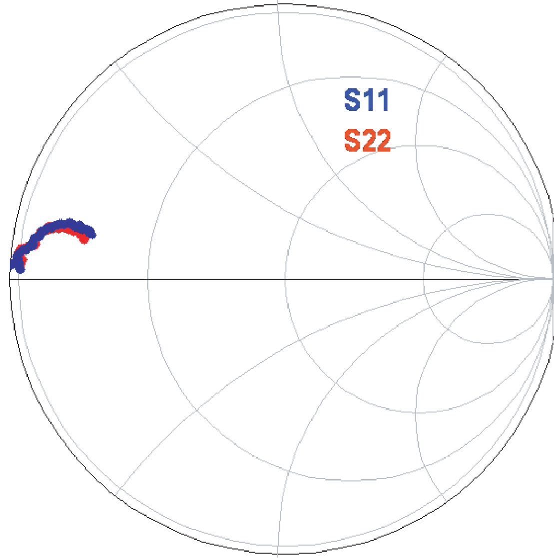


Figure 4.47: S-parameters of remeasured short standard after calibration. High substrate and resistive losses can be observed from the measured S_{11} and S_{22} data

Although the data shown in this section shows that the thin film, microstrip style, TRL calibration techniques developed at UCSB can be used for high fre-

quency measurements, some times the results were highly inconsistent. It is believed that BCB thickness variation within the die, high resistance of the signal lines and resistive losses could result in significant measurement errors. Fig. 4.47 shows measured S-parameters of the short standard after calibration. As can be observed from the plot, short standard has high resistive losses in the WR5 band possibly leading to errors in the measurement. There were also errors due to probe placement repeatability and repeated measurements on the same HBT at same bias resulted in different RF gains.

On-wafer TRL calibrations are a must for high frequency DHBT measurements. As the transistor cut-off frequencies are increasing, it is important to be able to measure device characteristics in higher frequency bands for accurate model extraction. TRL calibration accuracy can be improved by implementing the microstrip lines in Metal 3 having a thicker BCB and metal layers. This would have lower signal line resistance, less resistive losses and less variation in BCB thickness across the die resulting in a more robust and reliable calibration standard.

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Chapter 5

Transconductance Non Scaling

HBT bandwidth is improved by lithographic and epitaxial scaling of key HBT dimensions. Transit times are decreased through reduced base (T_b) and collector (T_c) thicknesses and RC charging delays are decreased through reduced junction widths and lower ohmic contact resistivities. Reducing T_c increases the collector-base capacitance per unit collector junction area (C_{cb}/A_c), therefore transconductance per unit emitter area (g_m/A_e) must increase in proportion to square of the transistor bandwidth to reduce C_{cb}/g_m charging delay [1–3].

At a moderate applied emitter-base voltage V_{be} such that the electron density in the base and emitter-base heterojunction is non-degenerate, the current density (J_e) can be approximated by using the Boltzmann approximation for carrier density and varies exponentially with V_{be}. Thus $J_e \propto exp(qV_{be}/NkT)$ and

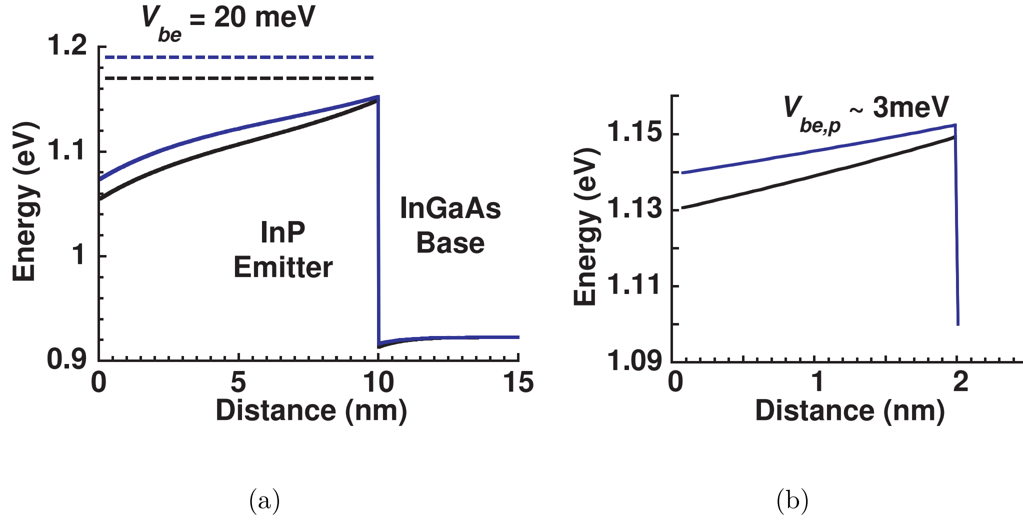
$g_m/A_e = \partial J_e/\partial V_{be} = qJ_e/NkT$. g_m/A_e is consequently proportional to J_e, and J_e must therefore vary in proportion to the square of the HBT bandwidth to obtain the desired level of g_m scaling.

InP/InGaAs DHBTs fabricated at UCSB have an abrupt emitter-base junction and for these HBTs g_m fails to increase in direct proportion to J_e at current densities greater than ~ 2 mA/μm^2. This increases the C_{cb}/g_m charging time and significantly degrades the bandwidth of HBTs having f_τ approaching or in excess of 500 GHz [4–6].

In this chapter, significant contributors to g_m non-scalability in abrupt emitter-base junction HBTs have been discussed. These include modulation of the electron injection barrier at emitter base heterojunction by the applied V_{be}, drop in the electron quasi Fermi level in the emitter space charge region and degenerate electron injection and quantum mechanical reflection at the hetero-interface [7].

5.1 Barrier Modulation

Given a finite base doping N_A, the applied base-emitter voltage V_{be} modulates the depletion region electrostatic potential on both the emitter and base sides of the barrier. For a homojunction or a graded heterojunction at the emitter-base interface, the barrier to electron injection from emitter to base is



(a)

(b)

Figure 5.1: (a) Band diagram from electrostatic simulation of InP/InGaAs emitter base junction at two different applied V_{be} ($\delta V_{be} = 20\ meV$). (b) Magnified E_c profile at the emitter base junction showing $\delta V_{be,p} = 3\ meV$ due to barrier modulation effect; $\delta V_{injection} = 17\ meV$

set by the conduction band edge in the bulk base. If the applied voltage is changed by an amount δV_{be}, barrier for electron injection reduces by an amount $\delta V_{injection} = \delta V_{be}$ where $\delta V_{injection}$ is the potential at the emitter-base interface given by $qV_{injection} = E_{fn} - E_c$. But this does not hold for an abrupt emitter base junction like the InP/InGaAs junction discussed here. For InP/InGaAs heterojunction, the barrier to electron injection is set by the conduction band edge at the InP/InGaAs interface. Thus any modulation of electrostatic potential in the base region does not contribute to lowering the injection barrier. Therefore, for an applied δV_{be}, barrier for electron injection is reduced by $\delta V_{injection} = \delta V_{be} - \delta V_{be,p}$ where $\delta V_{be,p}$ is the modulation of the electrostatic potential in the base (Fig. 5.1).

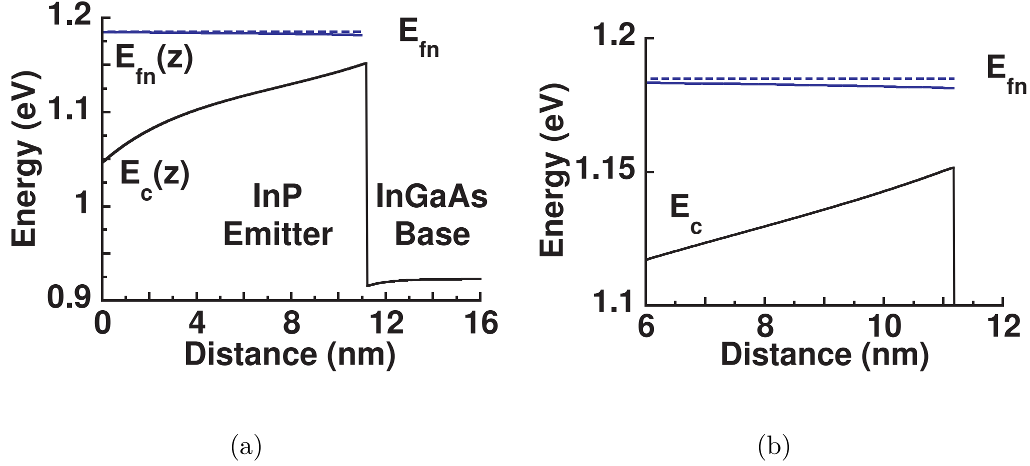
$\delta V_{be,p}$ was calculated at different applied biases by numerical simulation of the junction using a self-consistent Poisson/Fermi-Dirac algorithm [8].

5.2 Quasi Fermi Level Drop

The electron flux in the emitter space charge region has associated with it a drop in the electron quasi Fermi level given by the relation [1]

$$\Delta E_{fn} = \int_{W_{dep}} \frac{J_e}{\mu_n(z).n(z)}\, dz \tag{5.1}$$

where W_{dep} is the emitter space charge region thickness, $\mu_n(z)$ the electron mobility, and $n(z)$ the electron charge density (Fig 5.2). ΔE_{fn} increases with J_e for both graded and abrupt emitter-base junctions. In order to support a high emitter current density without substantial potential drop in the emitter space charge region, a high electron density must be present at the emitter-base junction in addition to narrow depletion region width. Small depletion region width also reduces the mobile charge storage in the emitter region, reducing the delay effects due to mobile charge storage [1]. For an applied δV_{be}, quasi Fermi level drop reduces the potential $\delta V_{injection}$ at the interface to $\delta V_{injection} = \delta V_{be} - \delta(\Delta E_{fn})/q$. $\delta(\Delta E_{fn})$ was calculated at different applied biases by numerical simulation of the junction using a self-consistent Poisson/Fermi-Dirac algorithm.



(a) (b)

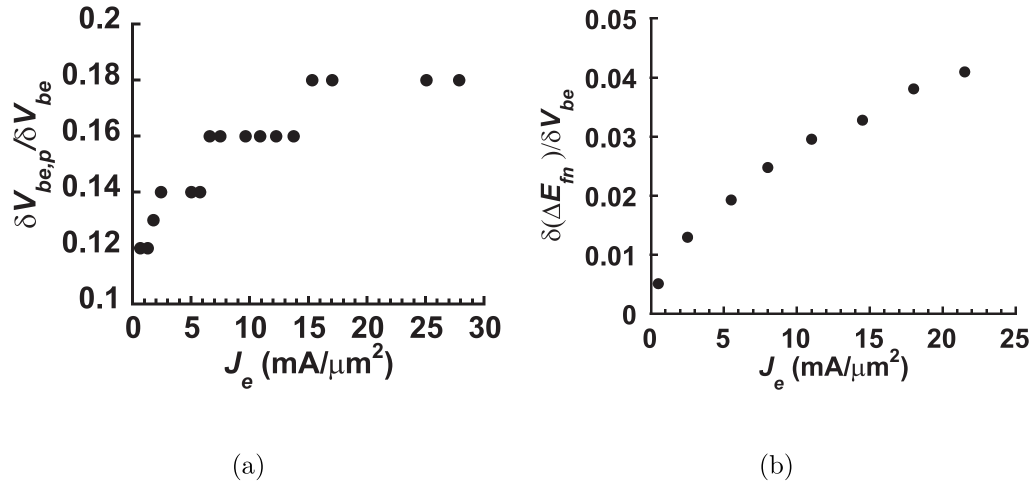
Figure 5.2: (a) Band diagram from electrostatic simulation of InP/InGaAs emitter base junction; (b) Magnified E_c and E_{fn} profile at the emitter base junction showing a drop in the quasi Fermi level (ΔE_{fn}) in the emitter space charge region at high J_e. $J_e \sim 12\ mA/\mu m^2$ was used for this simulation

Independent of the carrier statistics, these two effects act as voltage partitioning factors where the entire applied δV_{be} does not contribute to electron injection barrier lowering due to potential drop in the emitter-base space charge regions. Combining these two effects together, $\delta V_{injection} = \delta V_{be} - \delta(\Delta E_{fn}) - \delta V_{be,p}$ and

$$\frac{\delta V_{injection}}{\delta V_{be}} = N = 1 - \frac{\delta V_{be,p}}{\delta V_{be}} - \frac{\delta(\Delta E_{fn})}{\delta V_{be}} \tag{5.2}$$

Here N is the voltage partitioning factor less than unity. Thus intrinsic junction g_m ($g_{m,int}$) given by $\partial J_e/\partial V_{injection}$ and extrinsic device g_m ($g_{m,ext}$), excluding extrinsic resistances, given by $\partial J_e/\partial V_{be}$ are related through the relation $g_{m,ext} = N \cdot g_{m,int}$. As a consequence, due to the two effects discussed - barrier modulation and quasi Fermi level drop, extrinsic device g_m is always less than the intrinsic value.

Given a 15 nm (W_{dep}) thick InP emitter doped at 2×10^{18} cm^{-3} capped above by 5×10^{19} cm^{-3} doped n+ InP, and a p+ InGaAs base doped at 9×10^{19} cm^{-3} [9], both $n(z)$ and $\delta V_{be,p}/\delta V_{be}$ are found by numerical simulation of the junction using a self-consistent Poisson/Fermi-Dirac algorithm (BandProf) [8]. J_e is determined from E_{fn} at the InP/InGaAs interface using the methods described in section 5.4. $\delta(\Delta E_{fn})$ is finally computed from Eq. (5.1). At an applied V_{be} such that J_e = 20 $mA/\mu m^2$, $\delta V_{be,p}/\delta V_{be}$ = 0.17 and $\delta(\Delta E_{fn})/\delta V_{be}$ = 0.05, thus $\delta V_{injection}/\delta V_{be}$ = 0.78. Plots of computed $\delta V_{be,p}/\delta V_{be}$ and $\delta(\Delta E_{fn})/\delta V_{be}$ for the emitter design mentioned above are given in Fig. 5.3.



(a)

(b)

Figure 5.3: Plot of calculated (a) $\delta(V_{be,p})/\delta V_{be}$ and (b) $\delta(\Delta E_{fn})/\delta V_{be}$ as a function of J_e obtained from the derivations in section 5.4

5.3 Degenerate Injection

For an InP emitter, neglecting any reflection and finite transmission effects at the InP/InGaAs interface, the device current can be computed by integrating over all *k-space* of the fermi function multiplied by the electron distribution function and velocity in the direction of current flow. In the expressions below, q is the electronic charge, m^* the effective elctron mass in InP, k_B Boltzmann's constant, v electron velocity and $f(E)$ the electron distribution function. The prefactor $-q/4\pi^3$ comes from the 3D density of states calculations and spin degeneracy.

$$J = \frac{-q}{4\pi^3} \int_{k_x=-\infty}^{\infty} \int_{k_y=-\infty}^{\infty} \int_{k_z=0}^{\infty} v_z \cdot f(E)\, dk_x\, dk_y\, dk_z \tag{5.3}$$

$$= \frac{-q}{4\pi^3} \int_{k=0}^{\infty} \int_{\phi=0}^{2\pi} \int_{\theta=0}^{\pi/2} v \cdot \cos\theta \cdot f(E) \cdot \sin\theta \cdot k^2\, d\theta\, d\phi\, dk \tag{5.4}$$

$$= \frac{-q}{4\pi^3} \int_{k=0}^{\infty} k^2 \cdot v \cdot f(E)\, dk \tag{5.5}$$

Note that k_z is only integrated for $k_z > 0$ as electrons having forward momentum will contribute to forward current flow. Reverse current flow is not considered due to large reverse bias at the collector-base junction. Assuming parabolic conduction band, $E = m^*v^2/2 \ = \ \hbar^2k^2/2m^*$, and thus

$$J = \frac{qm^*}{2\pi^2\hbar^3} \int_0^{\infty} E \cdot f(E)\, dE \tag{5.6}$$

Here $f(E)$ represents the electron distribution function which could be Boltzmann approximation ($f(E) = exp((E_f - E)/kT)$) or Fermi-Dirac distribution ($f(E) =$

$1/(1 + exp\ ((E_f - E)/kT)))$. Under highly degenerate injection, such that $E_{fn} - E_c >> kT/q$, $f(E)$ can be approximated as a step function and $J_e = q^2 m^* (E_{fn} - E_c)^2 / 4\pi^2 \hbar^3$. Thus at high biases, current only varies in proportion to square of the applied V_{be}. A plot of current density for InP emitter at T = 300 K as a function of electron fermi level position relative to conduction band edge for the three distributions mentioned is shown in Fig. 5.4.

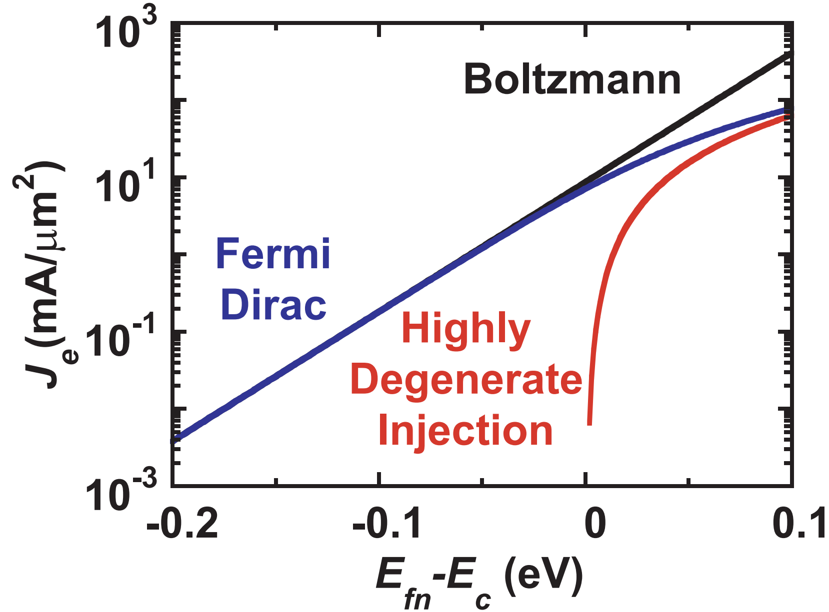


Figure 5.4: Calculated J_e as a function of Fermi Level (E_{fn}) position relative to conduction band edge (E_c) for InP emitter for Boltzmann approximation, Fermi-Dirac distribution function and highly degenerate injection

High emitter current density is necessary for high f_τ/f_{max} devices. At 10 - 35 mA/μm^2 current density needed for 0.5 - 1 THz f_τ, the electron Fermi level at the InP/InGaAs junction must be higher than the conduction band edge E_c. The

electron thermal statistics can then no longer be approximated by a Boltzmann distribution, and J_e no longer varies exponentially with E_{fn}. The emitter current density has to be computed using Fermi-Dirac statistics as shown before [2, 10–12].

$$J = \frac{qm^*}{2\pi^2\hbar^3}\int_0^\infty \frac{E}{1 + exp((E-(E_{fn}-E_c))/kT)}\,dE \tag{5.7}$$

$E_{fc} = E_{fn} - E_c$ is the relative position of Fermi level with respect to conduction band edge at the InP/InGaAs heterointerface.

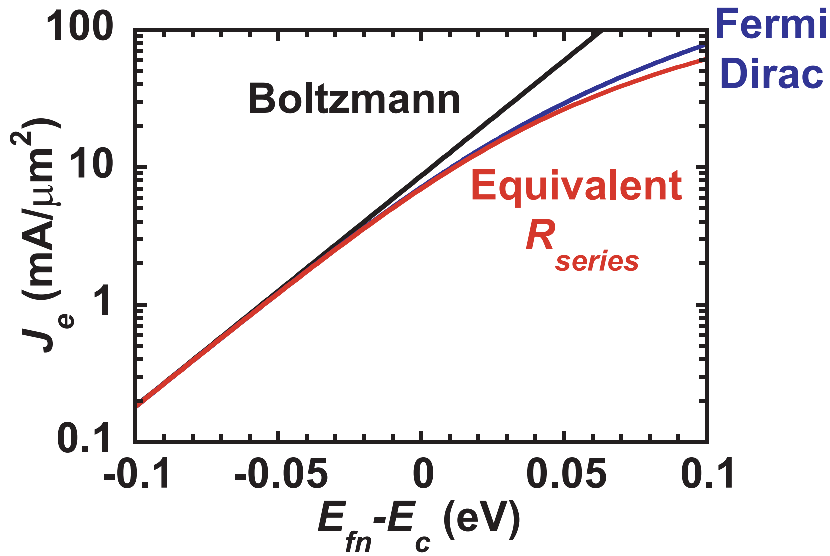


Figure 5.5: Calculated J_e as a function of Fermi Level (E_{fn}) position relative to conduction band edge (E_c) for InP emitter for Boltzmann approximation, Fermi-Dirac distribution function and deviation from Boltzmann modeled as an equivalent series resistance of $0.8\ \Omega - \mu m^2$

Previously, it has been shown that the deviation from Boltzmann approximation can be modelled as a current-independent equivalent series resistance [2, 13]. Due to the current-independent nature of the equivalent series resistance, these

models fail to fit well the HBT characteristics for the entire range of bias currents. Fig. 5.5 shows a plot of calculated current density as a function of $E_{fn} - E_c$ for Boltzmann approximation, Fermi Dirac distribution and deviation from Boltzmann modelled as an equivalent series resistance of 0.8 $\Omega - \mu m^2$. This model fails to fit the Fermi-Dirac distribution beyond J_e = 10 mA/μm^2

For $V_{be} = V_{injection}$, at $J_e = 30\ mA/\mu m^2$, degenerate electron statistics reduce g_m 1.7:1 relative to the non-degenerate case. A plot of transconductance per unit junction area (g_m/A_e) as a function of emitter current density is shown in Fig. 5.6.

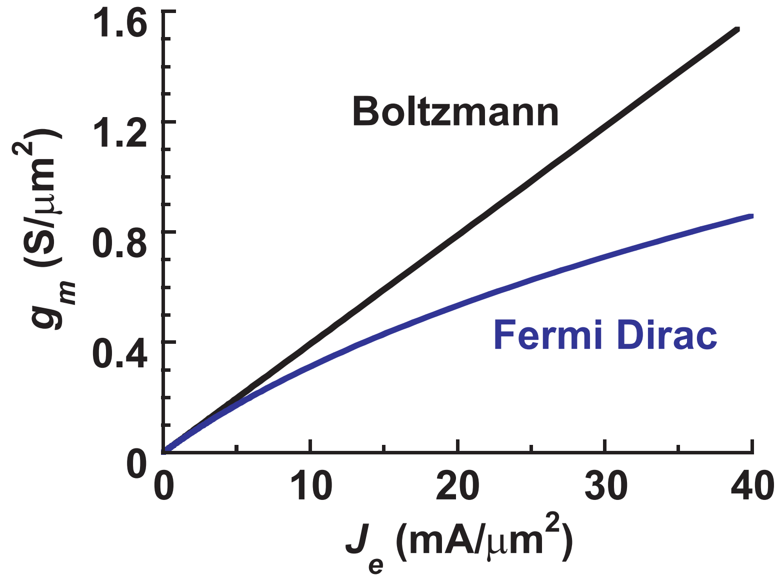


Figure 5.6: Calculated g_m as a function of J_e for InP emitter for Boltzmann approximation and Fermi-Dirac distribution function

5.4 Quantum Mechanical Reflection

At the emitter-base interface due to abrupt change in the conduction band potential E_c and effective electron mass m^*, a fraction of the electron flux incident from the emitter gets reflected even though the electron Fermi level E_{fn} is higher than E_c [14, 15]. The transmission coefficient at the interface has been computed assuming a potential step at the interface as shown in Fig. 5.7. Any additional reflection term due to potential gradient in the emitter space charge region has been neglected. Tunneling at the emitter-base interface has also been neglected [10, 11].

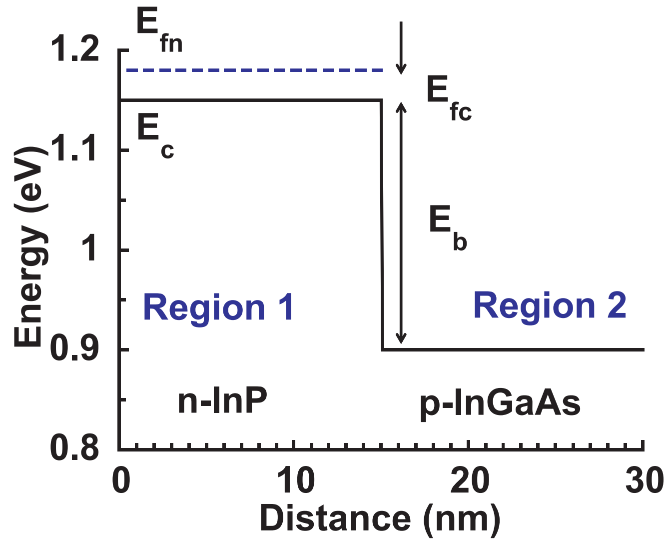


Figure 5.7: Energy band diagram for computing the transmission coefficient $T(E_{fc})$ over the emitter-base energy barrier (E_b)

The electron wavefunctions in the two regions are given by

$$\psi_1(z) = Ae^{-jk_{1z}z} + Be^{jk_{1z}z}$$
$$\psi_2(z) = Ce^{-jk_{2z}z} \tag{5.8}$$

where $k_{1z} = \sqrt{2m_1E_{1z}/\hbar^2}$ and $k_{2z} = \sqrt{2m_2E_{2z}/\hbar^2}$ are the wave-vectors in the direction of current flow. $m_1 = 0.08m^*$ is the effective electron mass in material 1 (InP) and $m_2 = 0.04m^*$ is the effective electron mass in material 2 (InGaAs) [16]. Using the boundary conditions at $z = 0$, $\psi_1(0) = \psi_2(0)$ and $\psi_1'(0)/m_1 = \psi_2'(0)/m_2$, the amplitude ratio C/A is given by

$$\frac{C}{A} = \frac{2k_{1z}}{k_{1z} + \frac{m_1}{m_2}k_{2z}} \tag{5.9}$$

The transmission coefficient $T(E_z)$ is then computed as [17]

$$\begin{aligned} T(E_z) &= \frac{k_{2z}}{k_{1z}} \cdot \frac{m_1}{m_2} \cdot \left|\frac{C}{A}\right|^2 \\ &= \frac{4\sqrt{\frac{m_1}{m_2}}\sqrt{E_{1z}E_{2z}}}{E_{1z} + \frac{m_1}{m_2}E_{2z} + 2\sqrt{\frac{m_1}{m_2}}\sqrt{E_{1z}E_{2z}}} \end{aligned} \tag{5.10}$$

The above derivation assumes that only the transverse k-vector in the direction of current flow k_z is affected by the electron flux reflection at the interface and the longitudinal k-vectors k_x and k_y are unaffected by the presence of the interface, thus $k_{1x} = k_{2x}$ and $k_{1y} = k_{2y}$. The assumption is valid for specular transmission when scattering from the interface is neglected [18, 19]. Defining $k_{xy}^2 = k_x^2 + k_y^2$,

$E_{xy} = \hbar^2 k_{xy}^2/2m$ and $E_z = \hbar^2 k_z^2/2m$ in both the regions and using conservation of momentum ($k_{xy1} = k_{xy2}$), and conservation of total energy across the interface ($E_{1z} + E_{1xy} + E_b = E_{2z} + E_{2xy}$), the energy parameters of material 2 (InGaAs) can be written in terms of energy parameters of material 1 (InP). E_{xy} and E_z are the electron kinetic energies in the longitudinal and transverse directions.

$$E_{2xy} = \frac{m_1}{m_2} \cdot E_{1xy}$$

$$E_{2z} = E_b + E_{1z} + E_{1xy} \cdot (1 - \frac{m_1}{m_2}) \tag{5.11}$$

Here E_b represents the conduction band energy discontinuity at the interface. The calculated $T(E_{fc})$ as a function of energy E_{fc} for 1D case where $E_{fc,xy} = 0$ at the InP/InGaAs heterointerface is shown in Fig. 5.8.

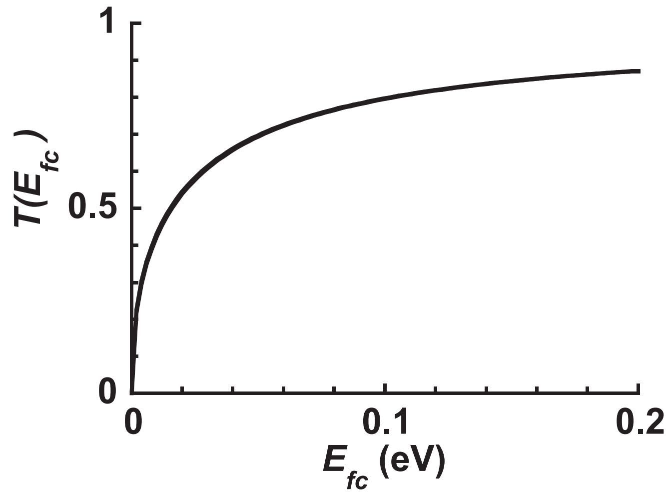


Figure 5.8: $T(E_{fc})$ as a function of energy E_{fc} above the barrier for 1D case where $E_{fc,xy} = 0$ at the InP/InGaAs interface

The current density across the interface given by Eq. (5.7) needs to be modified to incorporate transmission coefficient across the interface. The current density is now calculated by integrating the probability of transmission at the interface multiplied by the electron distribution function and velocity in the direction of current flow over the entire *k-space* of the Fermi statistics in InP emitter.

$$J = \frac{-q}{4\pi^3} \int_{k_x=-\infty}^{\infty} \int_{k_y=-\infty}^{\infty} \int_{k_z=0}^{\infty} v(E_z) \cdot f(E_{xy}, E_z) \cdot T(E_{xy}, E_z) \; dk_x \; dk_y \; dk_z \quad (5.12)$$

$$= \frac{-q}{4\pi^3} \int_{k_{xy}=0}^{\infty} \int_{k_z=0}^{\infty} \int_{\theta=0}^{2\pi} v(E_z) \cdot f(E_{xy}, E_z) \cdot T(E_{xy}, E_z) \cdot k_{xy} \; d\theta \; dk_z \; dk_{xy} \quad (5.13)$$

$$= \frac{-qm^*}{2\pi^2\hbar^3} \int_{E_{xy}=0}^{\infty} \int_{E_z=0}^{\infty} f(E_{xy}, E_z) \cdot T(E_{xy}, E_z) \; dE_z \; dE_{xy} \quad (5.14)$$

where $T(E_{xy}, E_z)$ is given by Eq. (5.10) and

$$f(E_{xy}, E_z) = \frac{1}{1 + \exp\left(\dfrac{E_{xy} + E_z - E_f}{kT}\right)} \quad (5.15)$$

A plot of the computed current density as a function of total kinetic energy ($E_{fn} - E_c$) is shown in Fig 5.9. Tunneling at the interface has been neglected and $T(E)$ has been assumed to be 0 for incident energies below the barrier height [10, 11].

5.5 Comparison to Measured Transconductance

In this section, the computed variation of transconductance per unit emitter area g_m/A_e with J_e for all the effects discussed in prior sections has been compared for their relative contributions in g_m non-scaling. The final computed g_m/A_e has

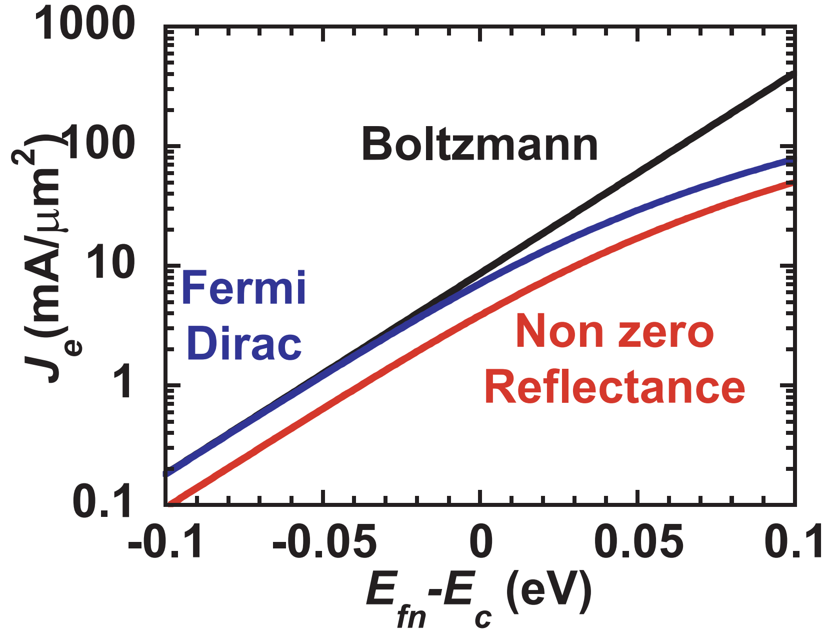


Figure 5.9: Calculated J_e as a function of Fermi Level (E_{fn}) position relative to conduction band edge (E_c) for InP emitter for Boltzmann approximation, Fermi-Dirac distribution function and including a non-zero electron flux reflectance at the heterointerface

also been compared to measured data. Fig. 5.10 compares the computed g_m/A_e for all the discussed effects that degrade g_m including barrier modulation effect, quasi Fermi level drop, degenerate injection and quantum mechanical reflection. For clarity in presentation, the curves assume zero extrinsic emitter resistance R_{ex}, zero base access resistance R_{bb}, and infinite DC current gain β. At $J_e \sim 20\ mA/\mu m^2$, there is more than a 2:1 reduction in g_m compared to the Boltzmann approximation.

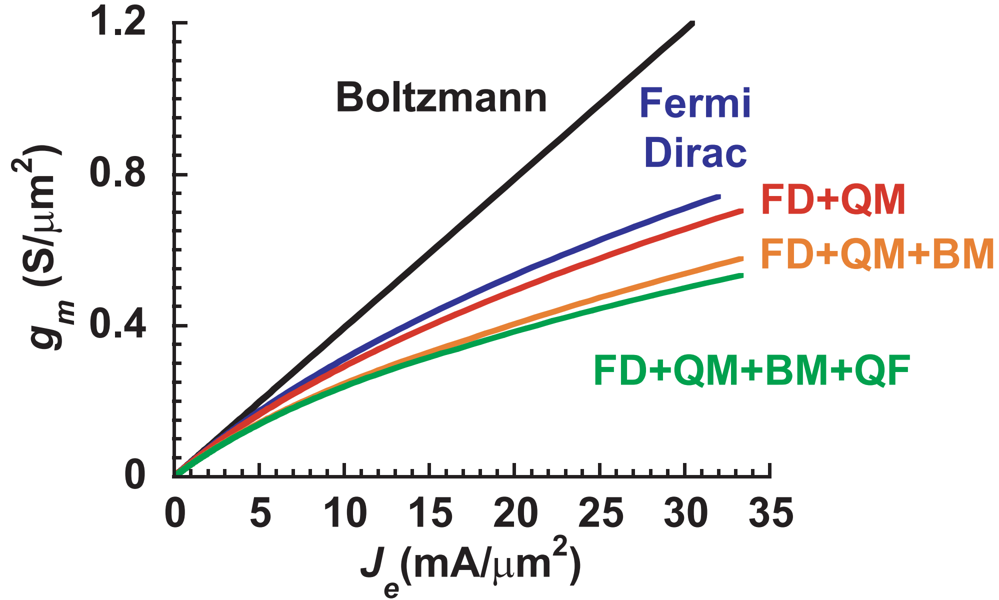


Figure 5.10: Calculated g_m as a function of J_e at 300K including all possible effects causing g_m degradation. FD - Fermi-Dirac, QM - Quantum Mechanical Reflection, BM - Barrier Modulation effect, QF - Quasi Fermi level drop

Measured g_m data includes the effects of R_{ex}, R_{bb}, β [9] and device self heating/junction temperature rise which need to be incorporated in the computed g_m curves. TLM measurements of metal/InGaAs emitter contact on a separate TLM wafer were performed to estimate emitter contact resistivity while InGaAs/InP interface resistivity was obtained from literature [20]. These two values are used to estimate R_{ex}. R_{bb} is obtained from S-parameter measurements and β from DC measurements. The calculated g_m curves include $R_{ex} = 3\ \Omega \cdot \mu m^2$ and $R_{bb}/\beta = 1\ \Omega \cdot \mu m^2$. To include the effect of device self-heating, thermal resistance R_{th} and device junction temperature rise was measured by the method described

in [21]. The measurement was done at different V_{cb} to vary the electric field distribution and power dissipation in the collector region. R_{th} is then calculated from the relation

$$\delta V_{be}|_{fixed\ I_c} = \frac{dV_{be}}{dT} \cdot \frac{dT}{dP} \cdot \frac{dP}{dV_{ce}} \cdot \delta V_{ce} = -\phi \cdot R_{th} \cdot I_c \cdot \delta V_{ce} \tag{5.16}$$

where ϕ is the thermo-electric feedback coefficient (V/°C). ϕ is estimated from literature and is roughly given by $\phi(V/°C) = 0.00066 - 0.00007958 \cdot \ln(I_c(A))$ [21]. Fig. 5.11 shows the calculated thermal resistance for the DHBT53 device having 270 nm wide emitter-base junction as a function of applied V_{cb} for $I_c = 10$ mA.

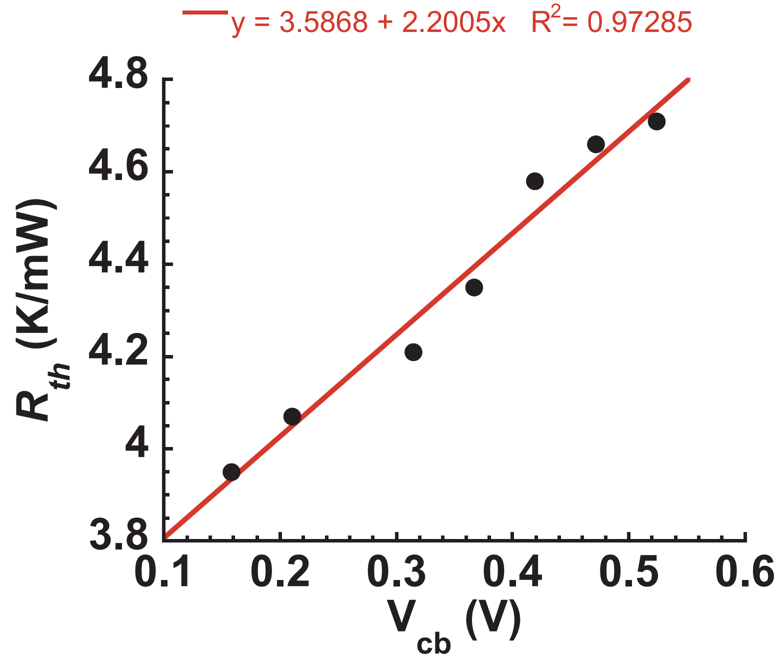


Figure 5.11: Calculated thermal resistance (R_{th}) as a function of applied V_{cb} for constant $I_c = 10$ mA

Using this relation, R_{th} for $I_c = 10$ mA and $V_{cb} = 0.7$ V is computed to be 5.13 K/mW. Rise in junction device temperature is computed from

$$T = T_{amb} + R_{th} \cdot V_{ce} \cdot I_c \tag{5.17}$$

For temperature rise calculation, $V_{ce} = 1.65$ V was used. Including the effects of R_{ex}, R_{bb}/β and junction temperature rise in addition to all the effects discussed earlier in this chapter for transconductance non-scaling – barrier modulation, quasi Fermi level drop, degenerate carrier injection and quantum mechanical reflection, the final computed g_m as a function of J_e is plotted in Fig. 5.12. Measured g_m curves are for HBTs on the same wafer (DHBT53) with $L_e = 3.5\ \mu m$ and $W_e =$ 110, 170, 220 and 270 nm. For these devices $R_{ex} + R_{bb}/\beta$ of $\sim 4\ \Omega \cdot \mu m^2$ is a good approximation based on the TLM measurements and low frequency RF data.

There is still some discrepancy between the measured and calculated g_m curves. This could result from neglecting tunneling through the emitter-base barrier or approximating the barrier with a step function or from additional reflections in the emitter space charge region due to the potential profile [22, 23]. Another possible explanation could be bias dependent nature of the InGaAs/InP interface resistance.

Fig. 5.13 shows a plot of measured g_m as a function of applied V_{cb}. It is observed that the measured g_m value does not change with V_{cb} suggesting that device self-heating is not a critical factor in degrading g_m at high current biases.

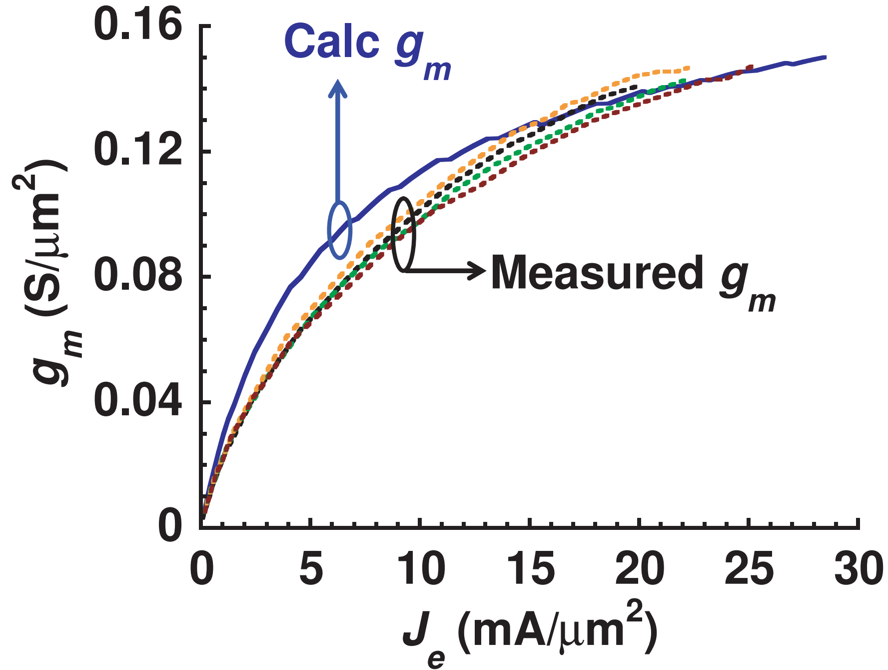


Figure 5.12: Measured and calculated g_m of different HBTs as a function of J_e including the effects of R_{ex}, R_{bb} and device self-heating

Barrier modulation effect can be reduced through increased base doping. Quasi-Fermi level drop can be reduced through increased doping in the emitter and base regions and through thinner emitter depletion layers. Higher doping in the n-InP emitter and thinner space charge layer thickness will also increase the maximum current density in the emitter prior to source starvation effect. Quantum mechanical reflection can be reduced by grading the emitter-base heterojunction. To avoid g_m reduction from electron degeneracy, emitter semiconductor material with increased density of states needs to be identified and employed.

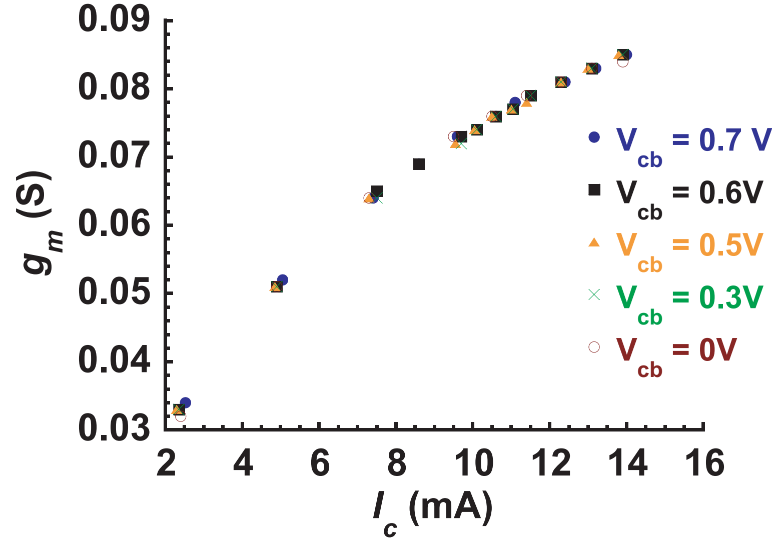


Figure 5.13: Measured g_m of the same HBT as a function of I_c for different V_{ce}. g_m stays constant with V_{ce} indicating that junction temperature rise has small impact on g_m degradation

Measured g_m at a given I_c can also be improved by grading the emitter-base junction from InP emitter to InGaAs base as mentioned in [24]. Graded junction does not suffer from barrier modulation effect and quantum mechanical reflection. As a result it has much higher intrinsic g_m for the same I_c. A plot of measured and calculated g_m as a function of J_e is shown in Fig. 5.14 for graded emitter-base junction of [24]. For the calculations, effective electron mass m^* in the chirped superlattice grade of 0.05 and $R_{ex} + R_{bb}/\beta$ of $\sim 2.5\ \Omega \cdot \mu m^2$ are assumed [16]. $R_{ex} + R_{bb}/\beta$ is estimated from RF extractions. Device self-heating effects are included using the same thermal resistance as computed earlier.

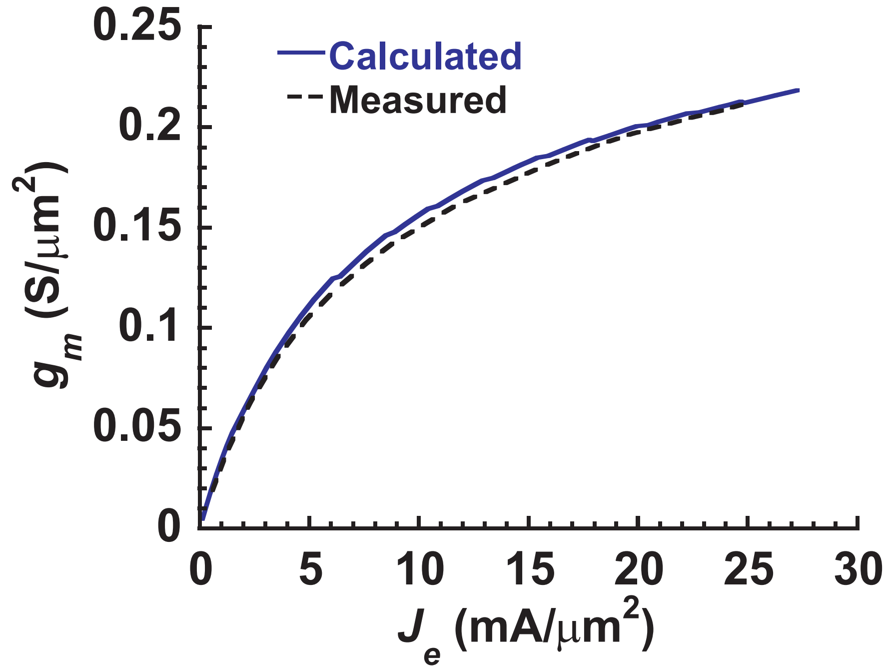


Figure 5.14: Measured and calculated g_m of the HBT as a function of J_e for a graded emitter-base heterojunction

The calculations and discussion in this chapter show that although transconductance non-scaling is a problem, it is not a significant factor in the measured g_m value for the current generation of devices due to high emitter access resistance. The measured g_m value is still dominated by extrinsic resistances (Fig. 5.15) and with scaling, as emitter contact and access resistivity values will decrease, g_m non-scaling will become an important factor in device scaling laws.

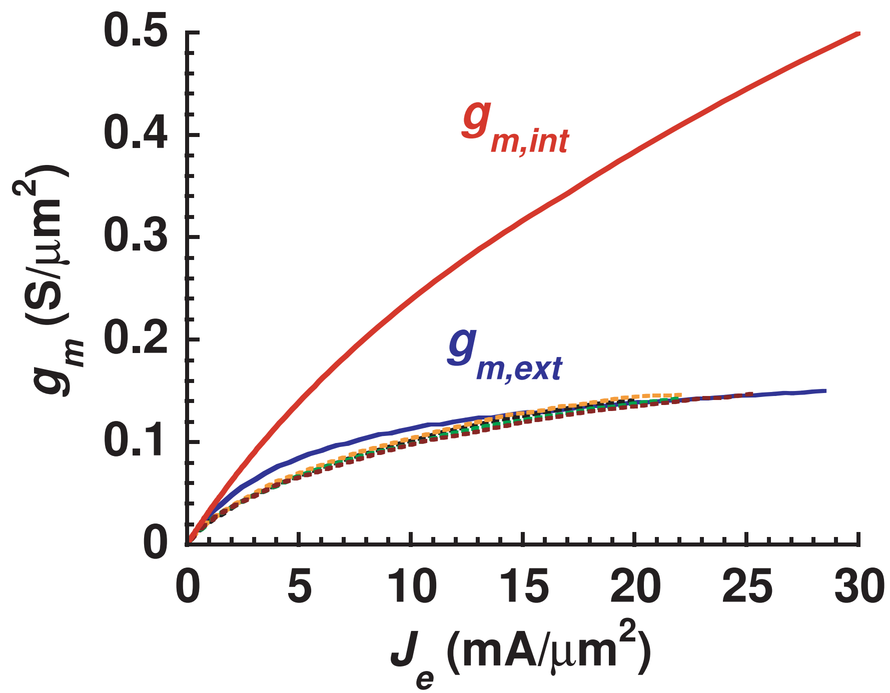


Figure 5.15: Intrinsic and extrinsic g_m for the HBTs. Intrinsic g_m values are from calculations as in Fig. 5.10

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Chapter 6

Conclusions

6.1 Accomplishments

6.1.1 Process Improvements

Several changes were made to the DHBT fabrication process flow to enable a reliable, scalable and robust process for improved device performance. Use of e-beam writer for emitter definition helped in achieving sub-100 nm emitter features on a regular scale. Processes for base contact and base mesa definitions using e-beam writer are under development at this time and would take some time to stabilize. That would enable small emitters with well aligned, narrow base contacts and collector-base mesa resulting in low parasitics and huge improvement in device performance. To permit operation at high current density without elec-

tromigration or contact degradation issues, Mo based refractory emitter contacts and W/TiW emitter stack process was developed. The low stress W/TiW emitter stack process significantly improved the emitter yield. Dry etch of this emitter stack has been optimized to attain a vertical emitter profile which reduces the emitter-base gap, reducing the base access resistance. Device results at 220 nm and 110 nm wide emitter-base junctions have been demonstrated in this work and the process is scalable to atleast 70 nm node as well. Dual sidewall process was used to provide extra mechanical support to emitter metal stack. InP emitter has been thinned down sufficiently to enable an all-wet-etch emitter process with controlled undercut helping in improving the reliability and scalability of the process. New surface preparation techniques for emitter and base contacts were developed to achieve low contact resistivities. A new process flow for incorporating refractory, ultra-low resistance ohmic contacts to p-InGaAs base was developed for the next generation DHBTs.

6.1.2 Design Improvements

Emitter design has been changed significantly to reduce emitter space charge region resistance and to overcome source starvation effect. As a result of source starvation, device f_τ and f_{max} roll-off with increasing current density at a much lower J_e than that expected from Kirk limits. Initially, this roll-off was attributed

to device junction temperature rise but now it is believed to be from emitter source starvation effect [1]. Emitter source starvation effect increases the junction voltage partitioning factor very rapidly, degrading device transconductance which adversely effects RF performance. Theoretical analysis showed that emitter space charge region resistance for old emitter designs was comparable or even more than the contact resistance; therefore, the emitter layer was redesigned to significantly reduce this resistance. A new base design involving step grade for reduced transit times and contact resistivity has been proposed.

6.1.3 Device Results

DHBT	**Base thickness**	**Emitter width**	β	**BV**$_{CEO}$	**J**$_{kirk}$	f_τ	f_{max}
	(nm)	**(nm)**		**(V)**	$(mA/\mu m^2)$	**(GHz)**	**(GHz)**
49	25	110	18	2.5	32	400	660
51	25	230	50	2.4	24	410	620
53	30	270	19	2.5	21	430	800
53	30	220	17	2.5	24	420	880
53	30	170	14	2.5	25	400	830
53	30	120	13	2.5	29	370	720
56	30	220	20	3.7	23	460	850
56	30	220	17	3.7	23	480	1000
53	30	220	26	2.4	21	410	690

Table 6.1: Summary of electrical characteristics for all HBTs fabricated in this work. Collector thickness was same (100 nm) for all the wafers. The last row of DHBT53 result is for the refractory base process

Table 6.1 summarizes the measured RF and DC performance of the different epitaxial designs investigated in this work. Improvement in base and emitter access resistances and process improvements to reduce parasitic resistances and capacitances have made it possible to achieve 1.0 THz device f_{max} at 220 nm wide emitter-base junction with more than 1.1 μm wide, misaligned base mesa. The bias conditions associated with peak f_τ and f_{max} are well below the bias where device self heating affects performance. Current spreading in the collector for narrow emitter base junctions allows the transistor to operate at high current and power density. Common emitter breakdown voltage increased from 2.5 V to 3.7 V by changing the base-collector grade design and doping in the InP collector.

6.1.4 Transconductance Scaling

It was observed that InP/InGaAs DHBTs fabricated at UCSB having an abrupt emitter-base junction have a very low transconductance than that estimated from simple calculations. For these HBTs g_m failed to increase in direct proportion to J_e at current densities greater than $\sim$ 2 mA/μm^2. This increased the C_{cb}/g_m charging time and significantly degraded the bandwidth of HBTs. Significant contributors to g_m non-scalability in abrupt emitter-base junction HBTs were identified and studied for their impact on g_m. These included modulation of the electron injection barrier at emitter base heterojunction by the applied

bias, drop in the electron quasi Fermi level in the emitter space charge region and degenerate electron injection and quantum mechanical reflection at the hetero-interface. Based on these factors, an attempt has been made to explain low value of the measured g_m. The theory has been extended to graded emitter-base junctions fabricated at Teledyne Scientific, and a good match between theory and measured data has been attained.

6.2 Future Work

InP DHBTs have achieved higher bandwidth than any of the contemporary technologies and circuit design attempts to achieve higher circuit bandwidth employing these HBTs is under way [2–10]. For InP DHBTs to gain wider acceptance, the integration level of these HBTs needs to be improved and circuits involving large number of HBTs need to be demonstrated.

At device level, continued aggressive scaling of emitter width and base collector junction width will reduce parasitic capacitances improving device performance. Base contact resistivity needs to be lowered which is attainable by using refractory ohmic contacts to highly doped base layer. Thin sidewalls, less than 20 nm, using ALD SiO_2 have been demonstrated by the FET team (Fig. 6.1) and these sidewalls need to be incorporated in the DHBT process flow for reduced spreading resistance

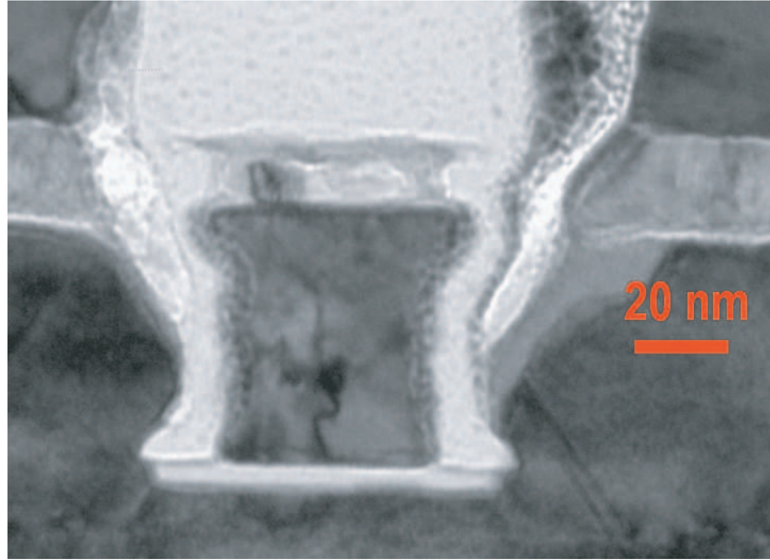

Figure 6.1: 15 nm SiO_2 sidewall on a InGaAs MOSFET using ALD. Image courtesy: Andrew Carter

in the base. Thinner ALD sidewalls $\sim$ 5 nm thick, involving high-k dielectrics like Al_2O_3, HFO_2 etc. may be required for further reduction in sidewall gap and spreading resistance. It has been demonstrated that high-k dielectrics are better for surface passivation than SiN_x, SiO_2 or BCB [11]. They may need to be included for device passivation to reduce leakage currents for increased β and also to reduce the base access resistance.

Base regrowth will be needed for reduced base transit delay and access resistance. Base regrowth will allow the intrinsic base layer to be thin and lightly doped for higher β and lower transit time, and will also reduce the sheet resistance in extrinsic base and base contact resistivity. Emitter access resistance needs to

be reduced further and can be done by reducing the contact resistivity using InAs contacts and reducing metal resistance using a two step emitter process involving a thin refractory and thick Au layer. Device transconductance at the same current density can be increased by grading the emitter-base junction.

With continued device scaling, smaller emitter and base mesas, lower base contact resistivity and thinner sidewalls, device f_{max} in excess of 1.5 THz can be achieved.

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Appendix A

Process Flow

In this appendix, the process flow details for lifted-off base ohmics is described.

1. **Wafer cleaving and preparation**

   The wafers grown at IQE (US flat option wafer) have minor flat on the right of the major flat. For these wafers, the long-axis of the emitter should be oriented **parallel** to the major flat to ensure proper semiconductor mesa etch undercut.

2. **Emitter surface preparation for *in-situ* contacts**

   - *NO PR and NO Au* tweezers and beakers are used for this step
   - Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
   - Dehydration bake - 110°C for 10 mins, 2 mins cool down
   - Prepare UV-O_3 reactor - run empty for 30 mins
   - Surface Preparation - oxidize wafer surface in UV-O_3 reactor for 30 mins
   - Immediately transfer the wafers to MBE lab
   - Surface Etch - In MBE lab, etch the oxide for 1 min in 1:10 HCl:DI solution and 1 min DI rinse
   - Load in the MBE system for (regrowth and) contact metal deposition

- 20 nm Mo is deposited in the MBE system

3. **Emitter surface preparation and contact deposition for *ex-situ* contacts**

    - Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
    - Dehydration bake - 110°C for 10 mins, 2 mins cool down
    - Prepare UV-O_3 reactor - run empty for 20 mins
    - Surface Preparation - oxidize wafer surface in UV-O_3 reactor for 15 mins
    - Surface Etch - Etch the oxide for 1 min in 1:10 HCl:DI solution and 1 min DI rinse
    - Immediately load the sample in E-beam#1 for contact metal deposition.
    - E-beam #1 deposition chamber preparation - Deposit 20 nm of Mo before loading the sample. This is to degas the source and clean the source surface.
    - Emitter contact - Deposit 20 nm of Mo as emitter contact metal. Ensure that the pressure in the e-beam chamber does not rise significantly. Cool the chamber for atleast 30 mins after deposition before venting it.

4. **Emitter stack deposition**

    - The procedure is for Sputter#1 system
    - Sputter deposition rate - estimate the deposition rate of W and TiW through dummy depositions and SEM
    - Stress in W only film - optimize the W sputter deposition process to minimize stress in 200 nm thick W film (stress less than 100 MPa)
    - Stress measurement tool - Use 2 inch Si wafer for stress measurement, measure the stress of the wafer before any metal deposition prior to loading it for sputtering
    - W Sputtering - Do a 15 min dummy deposition of W with the shutter closed at 200 W, 25 sccm Ar flow, 20 mTorr pressure. Then open the shutter and deposit about 200 nm of W on the sample.

- TiW Sputtering - Do a 15 min dummy deposition of TiW with the shutter closed at 200 W, 25 sccm Ar flow. Then open the shutter and deposit about 300 nm of TiW on the sample.
- Stress measurement - Measure the stress in the films, if stress is less than 150 MPa, repeat exactly the same deposition conditions on the actual sample, else change the deposition pressure and redo the depositions and stress measurements.
- Stress reduction - Keep the W deposition conditions same and vary the deposition pressure for TiW film, increasing the pressure makes the film more tensile.
- PECVD SiO_2 deposition - Deposit 100 nm SiO_2 on the sample
- E-beam Cr deposition - Deposit 40 nm Cr on the sample.
- Surface cleaning is not required before SiO_2 and Cr depositions if all are done on the same day

5. **Emitter lithography - e-beam write**

- Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- Descum - 1 min descum in oxygen plasma (PE-II system) at 100 W, 300 mT
- PR coat - Use PR filter for coating, spin coat maN-2403 @4000 rpm, 30 s, recipe #7
- PR bake - 90°C, 90 secs
- Expose the sample using e-beam writer, ensure that the emitters are *parallel* to the major flat
- PR development - 30 sec development in AZ-300MIF developer, slight agitation after every 10 sec, 3 min DI rinse
- Inspect under microscope to ensure that there is no scum, all the emitters have developed, the global and local alignment marks have properly been exposed and developed with no bulging at the center.

6. **Cr cap dry etch**

- Panasonic ICP #1

- Clean the chamber - Run 10 mins of O_2 clean and conditioning recipe (2 min 30 sec, Cl_2/O_2 at 26/4 sccm gas flow, 400 W/15 W ICP/RF power and 1 Pa pressure) prior to etch
- Dry etch - Etch 40 nm Cr for 2 min 30 sec in Cl_2/O_2 chemistry at 26/4 sccm gas flow, 400 W/15 W ICP/RF power and 1 Pa pressure
- Immediately rinse in water
- PR removal - Dip for 3 min each in ACE and ISO to remove the dry etch oil, then leave in 1165 stripper for 1 hr at 80°C, clean sample in 3 min ISO and 3 min DI rinse. Ensure that 1165 does not dry out on the sample.
- Descum - 1 min descum in oxygen plasma (PE-II system) at 100 W, 300 mT
- SEM - Look at the sample under SEM to check the emitter sizes and ensure that the alignment marks and emitters look good. Use horizontal mount. If there is scum in the field, do another 1 min long descum

7. **Emitter metal stack dry etch**

- Panasonic ICP #1
- Clean the chamber - Run 10 mins of O_2 clean and conditioning recipe (3 min, SF_6/Ar at 25/5 sccm gas flow, 600 W/150 W ICP/RF power and 1 Pa pressure) prior to etch
- TiW dry etch (high power etch) - Etch the sample for 2 min 45 sec in SF_6/Ar chemistry at 25/5 sccm gas flow, 600 W/150 W ICP/RF power and 1 Pa pressure. Immediately dip the sample in DI. Solvent clean to remove the etch oil.
- DEKTAK - measure the height of the etched layer.
- Repeat etch in increments of 15 secs till InGaAs is visible on 20-30% of the wafer (visual inspection).
- W/Mo etch (low power etch) - Etch the sample for 1 min 30 sec in SF_6/Ar chemistry at 5/5 sccm gas flow, 600 W/15 W ICP/RF power and 0.5 Pa pressure. The sample should be uniform after the etch with InGaAs visible on the entire wafer. If not, do another 30 sec etch
- Overetch - Etch the sample for 15 secs in SF_6/Ar chemistry at 5/5 sccm gas flow, 600 W/50 W ICP/RF power and 0.5 Pa pressure to remove any particles of W/Mo/TiW left on the surface.

- Solvent clean the sample and do a DEKTAK measurement to check the height of the emitter stack
- SEM - Observe the sample using 70° chuck and ensure a vertical emitter profile and undercut at the TiW/W interface. If the emitter is not vertical repeat the low power etch used for W etch.
- Etch times for both the high power (TiW etch) and low power (W/Mo etch) etches might change depending on the chamber conditioning and precise emitter stack height.
- ICP chamber - Ensure that the plasma ignites for the low power etch as it is very susceptible to chamber cleanliness.

8. **First SiN_x sidewall formation**
   - PECVD
   - Etch rate calibration sample - Deposit 100 nm SiN_x on a 2 inch Si wafer. Cleave the sample such that the area of the wafer is approximately same as that of the actual DHBT sample.
   - Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
   - Dehydration bake - 110°C for 10 mins, 2 mins cool down
   - Surface Preparation - Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load in the PECVD system
   - Sidewall deposition - Deposit 30 nm SiN_x sidewall on the sample
   - Ellipsometer - measure the thickness of deposited SiN_x on Si sample prior to etch. Measure the thickness at 3-5 points for accurate etch rate determination
   - Panasonic ICP #1
   - Clean the chamber - Run 10 mins of O_2 clean and conditioning recipe (5 min, CF_4/O_2 at 20/5 sccm gas flow, 500 W/100 W ICP/RF power and 1 Pa pressure) prior to etch
   - Etch rate calibration - Etch the Si sample with SiN_x for 4 mins in low power sidewall etch recipe - CF_4/O_2 at 20/2 sccm gas flow, 25 W/15 W ICP/RF power and 0.3 Pa pressure
   - Ellipsometer - measure SiN_x thickness again at the same points and estimate the etch rate. Etch rate may vary from 5-9 nm/min.

- Sidewall etch - Calculate the etch time assuming a 20% overetch. Etch rate varies with the sample location on the carrier wafer, so load the sample at the same location as the etch rate calibration sample.
- SEM - Observe the sample using 70° chuck and ensure there are no SiN_x flakes left in the field.

9. **InGaAs cap wet etch**

- DEKTAK - measure the height of emitter stack prior to InGaAs etch
- Prepare two beakers with –
  (a) 1:10 NH_4OH:DI
  (b) 1:1:25 H_2O_2:H_3PO_4:DI - use stirrer at 200 rpm, ensure that the hot plate is off and at room temperature
- Dip sample in NH_4OH:DI solution for 10 secs and 1 min DI rinse, N_2 dry
- Etch InGaAs in H_2O_2:H_3PO_4:DI solution for 6 secs (for 10 nm thick emitter cap), DI rinse 3 mins
- Visual inspection - sample surface should be of uniform colour
- DEKTAK - measure the height of emitter stack after InGaAs etch
- SEM - Observe the sample using 70° chuck and ensure surface is smooth

10. **Cr cap removal**

- Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- PR coat - Spin coat SPR955CM-1.8 resist @4000 rpm, 30 s, recipe #7
- PR bake - 90°C, 60 secs
- Nanometrics - measure the PR thickness before ashing, should be $\sim 1.6\mu m$
- PR ash - Ash PR in oxygen plasma (PE-II) at 200W/300mT for 8 mins
- Repeat PR thickness measurement to estimate the ash rate. Continue ashing till the PR height is $\sim$ 200 nm less than the emitter stack height
- PR bake - 110°C, 60 secs

- BHF etch - dip the sample in BHF for 50 secs with slight agitation every 15 secs, 3 mins DI rinse
- PR strip - Remove the PR in 1165 at 80°C for 1 hr.
- Descum - 30 secs descum in oxygen plasma (PE-II system) at 100 W, 300 mT
- SEM - Observe the sample using 70° chuck and check that the Cr cap has successfully come off and the top of emitters is smooth with no SiO_2 or Cr or scum left

11. **Second SiN_x sidewall formation**

- PECVD
- Etch rate calibration sample - Deposit 100 nm SiN_x on a 2 inch Si wafer. Cleave the sample such that the area of the wafer is approximately same as that of the actual DHBT sample.
- Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- Surface Preparation - Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load in the PECVD system
- Sidewall deposition - Deposit 30 nm SiN_x sidewall on the sample
- Ellipsometer - measure the thickness of deposited SiN_x on Si sample prior to etch. Measure the thickness at 3-5 points for accurate etch rate determination
- Panasonic ICP #1
- Clean the chamber - Run 10 mins of O_2 clean and conditioning recipe (5 min, CF_4/O_2 at 20/5 sccm gas flow, 500 W/100 W ICP/RF power and 1 Pa pressure) prior to etch
- Etch rate calibration - Etch the Si sample with SiN_x for 4 mins in low power sidewall etch recipe - CF_4/O_2 at 20/2 sccm gas flow, 25 W/15 W ICP/RF power and 0.3 Pa pressure
- Ellipsometer - measure SiN_x thickness again at the same points and estimate the etch rate. Etch rate may vary from 5-9 nm/min.
- Sidewall etch - Calculate the etch time assuming a 20% overetch. Etch rate varies with the sample location on the carrier wafer, so load the sample at the same location as the etch rate calibration sample.

- SEM - Observe the sample using 70° chuck and ensure there are no SiN_x flakes left in the field.

12. **InP wet etch**

- DEKTAK - measure the height of emitter stack prior to InP etch
- Prepare two beakers with –
  (a) 1:10 NH_4OH:DI
  (b) 1:4 HCl:H_3PO_4 - use stirrer at 200 rpm, ensure that the hot plate is off and at room temperature
- Dip sample in NH_4OH:DI solution for 10 secs and 1 min DI rinse, N_2 dry
- Etch InGaAs in HCl:H_3PO_4 solution for 8 secs (for 30 nm thick InP emitter), DI rinse 3 mins. Colour change occurs after 4-5 secs. Etch for another 2-3 secs after colour change is complete
- Visual inspection - sample surface should be of uniform colour
- DEKTAK - measure the height of emitter stack after InP etch and ensure that the entire layer has been etched off
- SEM - Observe the sample using 70° chuck and ensure surface is smooth

13. **Base Contact Lithography and Deposition**

- E-beam writing
- PR - UV-6 is used for base contact lithography. It should be removed from the fridge 1 hr prior to spin coating
- Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- HMDS coat - Spin coat HMDS @3000 rpm, 60 s, ramp 400 rpm/sec, wait 20 sec after applying HMDS and spin coating
- Wait for 1 min before applying the resist
- PR coat - Spin coat UV-6 @3000 rpm, 60 s, ramp 400 rpm/sec
- PR bake - 115°C, 60 secs
- Expose using e-beam writer
- PR post bake - immediately bake at 115°C, 120 secs

- PR development - 70-75 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
- Optical microscope - inspect the verniers and emitters, make sure that the base-emitter alignment is good.
- Deposition using E-beam#4 system
- Load private Pt/Ti/Pd/Au source in E-beam#4
- Surface preparation - Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load for deposition - orient long-axis of emitter in the same direction as the sample rotation. Cover the edge of sample with Al foil to help with lift-off
- Deposition - deposit Pt/Ti/Pd/Au contact – 25/170/170/700 A thick. Deposit Pt at 0.2 A/sec and the rest at 1 A/sec
- Lift-off - Heat up the 1165 stripper at 80°C for 20-30 mins prior to sample immersion. Leave the sample in 1165 at 80°C for 1 hr. Use vertical sample holder basket. Gently agitate with pipette to remove metal fragments. clean the sample in 3 mins ISO and 3 mins DI rinse.
- SEM - Observe the sample using horizontal chuck and measure base-emitter misalignment. Also check the yield of small emitters and base contacts.
- Measure the height of base metal using DEKTAK
- The field probably will have lots of scum, leave the scum as it is if the top of base metal for base post deposition looks clean

14. **Base Post Lithography and Deposition**

- Optical lithography - GCA autostepper
- PR - nLOF-5510 and LOL1000 are used for base post lithography.
- Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- LOL1000 coat - Spin coat @4000 rpm, 30 s, recipe #7
- LOL1000 bake - Bake at 180°C, 120 sec
- Wait for 1 min before applying the resist
- PR coat - Spin coat nLOF-5510 @1800 rpm, 40 s, ramp 350 rpm/sec

- PR bake - 90°C, 60 secs
- Expose - 0.22 sec exposure time
- PR post bake - bake at 110°C, 60 secs
- PR development - 90-100 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
- Optical microscope - inspect the verniers and emitters, make sure that the alignment is good. You should see undercut in the LOL1000 layer - If not, strip PR in 1165 stripper and use a shorter bake time for LOL1000 or a longer development time
- Deposition using E-beam#4 system
- Load private Ti/Pd/Au sources in E-beam#4
- Surface preparation - Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load for deposition - orient long-axis of emitter in the same direction as the sample rotation. Cover the edge of sample with Al foil to help with lift-off
- Metal thickness - Base post is generally kept 50-100 nm higher than the emitter stripe. Calculate the total base post thickness using $Emitter\ height - Cr\ Cap(\sim 120\ nm) + 50\ nm$, estimate Au thickness (XX A) from this
- Deposition - deposit Ti/Pd/Au contact – 170/170/XX A thick. Deposit the metals at 1 A/sec. Deposition rate of Au can be increased to 2 A/sec after 200 A deposition and then to 4 A/sec beyond 500 A thickness.
- Lift-off - Heat up the 1165 stripper at 80°C for 20-30 mins prior to sample immersion. Leave the sample in 1165 at 80°C for 1 hr. Use vertical sample holder basket. Gently agitate with pipette to remove metal fragments. Clean the sample in 3 mins ISO and 3 mins DI rinse.
- SEM - Observe the sample to check yield.

15. **Base Mesa Lithography and Etch**

    - E-beam writing
    - Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
    - Dehydration bake - 110°C for 10 mins, 2 mins cool down

- HMDS coat - Spin coat @3000 rpm, 60 s, ramp 450 rpm/sec
- Wait for 1 min before applying the resist
- PR coat - Spin coat maN-2410 @3000 rpm, 60 s, ramp 450 rpm/sec
- PR bake - 90°C, 2 mins 30 secs
- Expose
- PR development - 2 min 30 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
- Optical microscope - inspect the verniers and emitters, make sure that the alignment is good. If there are rainbows around the features, do another 15 sec development
- Descum - 1 min descum in oxygen plasma (PE-II system) at 100 W, 300 mT. This will remove the scum from base contact lift-off and also reduce the PR tail after base mesa lithography. A longer descum might be done to reduce the PR tail.
- SEM - ensure there is no PR scum left in the field
- Prepare three beakers with –
  (a) 1:10 HCl:DI
  (b) 1:1:25 H_2O_2:H_3PO_4:DI - use stirrer at 200 rpm, ensure that the hot plate is off and at room
  (c) 1:4 HCl:H_3PO_4 - use stirrer at 200 rpm, ensure that the hot plate is off and at room temperature
- DEKTAK - measure the height of PR prior to etch
- Dip the sample in 1:10 HCl:DI for 10 secs and 1 min DI rinse
- Etch the base and grade in 1:1:25 H_2O_2:H_3PO_4:DI solution for $\sim$ 30 secs. 20-25 secs etch is sufficient. The remaining time is to aggressively undercut the mesa below the contact.
- DEKTAK to ensure that the desired thickness has been etched.
- Etch the InP collector in 1:4 HCl:H_3PO_4 solution for $\sim$ 30 secs. Bubbles are seen for 15 secs. Overetch by another 15 secs for undercuts.
- REMEMBER these etch times are for 30 nm thick base and 100 nm thick collector. Adjust the etch times according to base and collector thickness.
- DEKTAK to ensure that the desired thickness has been etched.

- PR strip - remove the PR in 1165 for 1 hr at 80°C
- SEM - use the 70° chuck and look at the undercut in base mesa below the base contact

16. **Collector Contact Lithography and Deposition**

    - Optical lithography - GCA autostepper
    - Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
    - Dehydration bake - 110°C for 10 mins, 2 mins cool down
    - PR coat - Spin coat nLOF-2020 @3500 rpm, 30 s, recipe #6
    - PR bake - 110°C bake for 60 secs
    - Expose for 0.16 secs
    - PR bake - 115°C bake for 60 secs
    - PR development - 120 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
    - Optical microscope - inspect the verniers and emitters, make sure that the alignment is good.
    - Deposition using E-beam#4 system
    - Load private Ti/Pd/Au sources in E-beam#4
    - Surface preparation - Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load for deposition - orient long-axis of emitter in the same direction as the sample rotation.
    - Deposition - deposit Ti/Pd/Au contact – 200/200/2500 A thick. Deposit the metals at 1 A/sec. Deposition rate of Au can be increased to 2 A/sec after 200 A deposition and then to 4 A/sec beyond 500 A thickness.
    - Lift-off - Heat up the 1165 stripper at 80°C for 20-30 mins prior to sample immersion. Leave the sample in 1165 at 80°C for 1 hr. Use vertical sample holder basket. Gently agitate with pipette to remove metal fragments. Clean the sample in 3 mins ISO and 3 mins DI rinse.
    - SEM - Observe the sample to check yield.

17. **Device Isolation Lithography and Etch**

    - Optical lithography - GCA autostepper

- Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- PR coat - Spin coat SPR510 @4000 rpm, 30 s, recipe #7
- PR bake - 90°C, 60 secs
- Expose - 0.27 secs exposure time
- PR development - 60 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
- Optical microscope - inspect the verniers and emitters, make sure that the alignment is good.
- Prepare three beakers with –
  (a) 1:10 NH_4OH:DI
  (b) 1:1:25 H_2O_2:H_3PO_4:DI - use stirrer at 200 rpm, ensure that the hot plate is off and at room
  (c) 1:4 HCl:H_3PO_4 - use stirrer at 200 rpm, ensure that the hot plate is off and at room temperature
- DEKTAK - measure the height of PR prior to etch
- Dip the sample in 1:10 1:10 NH_4OH:DI for 10 secs and 1 min DI rinse
- Etch the InGaAs subcollector in 1:1:25 H_2O_2:H_3PO_4:DI solution for $\sim$ 10 secs. This is an overetch to undercut the semiconductor below the base post.
- Etch the InP sub-collector in 1:4 HCl:H_3PO_4 solution for $\sim$ 50 secs. Bubbles are seen for 35-40 secs. Overetch by another 15 secs for undercuts.
- DEKTAK to ensure that the desired thickness has been etched.
- Etch the InGaAs etch-stop in 1:1:25 H_2O_2:H_3PO_4:DI solution for $\sim$ 7 secs.
- Etch the semi-insulating InP substrate in 1:4 HCl:H_3PO_4 solution for $\sim$ 15 secs. This etches about 100-150 nm into the substrate and ensures proper device isolation
- DEKTAK to ensure that the desired thickness has been etched.
- PR strip - remove the PR in 1165 for 1 hr at 80°C
- SEM - use the 70° chuck and look at the undercut below the base post

18. **Collector Post Lithography and Deposition**

    - Optical lithography - GCA autostepper
    - Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
    - Dehydration bake - 110°C for 10 mins, 2 mins cool down
    - PR coat - Spin coat nLOF-2020 @3500 rpm, 30 s, recipe #6
    - PR bake - 110°C bake for 60 secs
    - Expose for 0.16 secs
    - PR bake - 115°C bake for 60 secs
    - PR development - 120 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
    - Optical microscope - inspect the verniers and emitters, make sure that the alignment is good.
    - Deposition using E-beam#4 system
    - Load private Ti/Pd/Au sources in E-beam#4
    - Surface preparation - Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load for deposition - orient long-axis of emitter in the same direction as the sample rotation.
    - Metal thickness - Collector post should be about 50-100 nm higher than the emitter stripe. Calculate the metal height (Au thickness = XX A) using $Emitter - Cr\ cap(\sim 120\ nm) + Base\ contact - Device\ Isolation - Collector\ Contact + 100\ nm$ where all the heights are estimated using DEKTAK
    - Deposition - deposit Ti/Pd/Au contact – 200/200/XX A thick. Deposit the metals at 1 A/sec. Deposition rate of Au can be increased to 2 A/sec after 200 A deposition and then to 4 A/sec beyond 500 A thickness.
    - Lift-off - Heat up the 1165 stripper at 80°C for 20-30 mins prior to sample immersion. Leave the sample in 1165 at 80°C for 1 hr. Use vertical sample holder basket. Gently agitate with pipette to remove metal fragments. Clean the sample in 3 mins ISO and 3 mins DI rinse.
    - SEM - Observe the sample to check yield.

19. **BCB Passivation**

- Blue oven is used for BCB cure - it should be at room temperature before beginning
- Set the bake recipe in blue oven (#5) and run N_2 at 100% flow for atleast 20 mins prior to sample loading
- Solvent clean the wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- UV-Ozone oxidation - oxidize the sample in UV-O_3 system for 10 mins
- Dip the sample in conc. NH_4OH solution for 10 secs. Blow dry with N_2 and *NO DI RINSE*
- Coat wafer with BCB3022-46 and wait for 30 secs
- Spin coat @1500 rpm, 30 s, ramp 150 rpm/sec
- Immediately load the sample in Blue Oven for cure and reduce the N_2 flow to 60%
- Program sequence
  (a) 5 min ramp to 50°C, 5 min soak
  (b) 15 min ramp to 100°C, 15 min soak
  (c) 15 min ramp to 150°C, 15 min soak
  (d) 60 min ramp to 250°C, 60 min soak
  (e) Natural cool down
- Remove sample from the oven when the temperature has fallen to below 30°C

20. **BCB Ashing**

- Nanometrics - Estimate BCB thickness, should be approximately 4.1-4.2 μm
- Panasonic ICP#1 - Ashing chamber
- Condition the ashing chamber for 15 mins - CF_4/O_2 50/200 sccm, 1000 W, 40 Pa
- Ash the sample for 4 mins, ashing rate depends on the chuck temperature and thus on the conditioning time and time lag between conditioning and ashing
- Nanometrics - Measure BCB thickness again and estimate an ash rate.

- SEM - Observe the sample using horizontal chuck and check whether the posts have started poking out of the BCB
- Repeat the ash and BCB height measurements in increments of 1 min or 30 secs depending on the ash rate and the amount of BCB to be ashed.
- SEM after every ashing step using horizontal chuck. If the posts start to appear, look at the sample using 70° chuck and estimate the amount of all posts and emitters projecting out of BCB. this usually happens when BCB is $\sim$1 μm thick.
- Repeat ash till about 100-200 nm of emitter is visible along with all the posts.
- Do not overash the BCB - BCB also gets etched during SiN_x contact via etch and may create problems of emitter-base shorts; also BCB ash chemistry also etches SiN_x, W and TiW thereby affecting emitter

21. **Contact Via Deposition**

    - PECVD
    - Etch rate calibration sample - Deposit 150 nm SiN_x on a 2 inch Si wafer. Cleave the sample such that the area of the wafer is approximately same as that of the actual DHBT sample.
    - Solvent clean the DHBT wafer - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
    - Dehydration bake - 110°C for 10 mins, 2 mins cool down
    - Surface Preparation - Etch the sample for 10 sec in 1:10 NH_4OH:DI solution. Immediately load in the PECVD system
    - Contact via deposition - Deposit 100 nm SiN_x the sample
    - Ellipsometer or Filmetrics - measure the thickness of deposited SiN_x on Si sample prior to etch. Measure the thickness at 3-5 points for accurate etch rate determination

22. **Contact Via Lithography and Etch**

    - Optical lithography - GCA Autostepper
    - Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
    - Dehydration bake - 110°C for 10 mins, 2 mins cool down

- PR coat - Spin coat SPR510 @4000 rpm, 30 s, recipe #7
- PR bake - 90°C, 60 secs
- Expose - 0.27 secs exposure time
- PR development - 60 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse
- Optical microscope - inspect the verniers and emitters, make sure that the alignment is good.
- Panasonic ICP #1
- Clean the etching chamber - Run 10 mins of O_2 clean and conditioning recipe (5 min, CF_4/O_2 at 20/5 sccm gas flow, 500 W/100 W ICP/RF power and 1 Pa pressure) prior to etch
- Etch rate calibration - Etch the Si sample with SiN_x for 12 mins in low power sidewall etch recipe - CF_4/O_2 at 20/2 sccm gas flow, 25 W/15 W ICP/RF power and 0.3 Pa pressure
- Ellipsometer - measure SiN_x thickness again at the same points and estimate the etch rate. Etch rate may vary from 5-9 nm/min.
- Contact via etch - Calculate the etch time assuming a 10% overetch. Etch rate varies with the sample location on the carrier wafer, so load the sample at the same location as the etch rate calibration sample.
- SEM - Observe the sample using 70° chuck and ensure that the posts and emitters are projecting out of the dielectric with no charging issues

23. **Metal I Lithography and Deposition**

- Optical lithography - GCA autostepper
- Solvent clean - 3 mins ACE, 3 mins ISO and 3 mins DI rinse
- Dehydration bake - 110°C for 10 mins, 2 mins cool down
- PR coat - Spin coat nLOF-2020 @3500 rpm, 30 s, recipe #6
- PR bake - 110°C bake for 60 secs
- Expose for 0.16 secs
- PR bake - 115°C bake for 60 secs
- PR development - 120 sec development in AZ-300MIF developer, slight agitation after every 15 sec, 3 min DI rinse

- Optical microscope - inspect the verniers and DHBTs, make sure that the alignment is good.
- Deposition using E-beam#4 system
- Load private Ti and Au sources in E-beam#4
- Surface preparation - Oxidize the surface in UV-O_3 chamber for 5 mins. Etch the sample for 10 sec in 1:10 HCl:DI solution and 1 min DI rinse. Immediately load for deposition - orient long-axis of emitter in the same direction as the sample rotation.
- Deposition - deposit Ti/Au contact – 300/10000 A (1 μm Au) thick. Deposit the metals at 1 A/sec. Deposition rate of Au can be increased to 2 A/sec after 200 A deposition and then to 4 A/sec beyond 500 A thickness.
- Lift-off - Heat up the 1165 stripper at 80°C for 20-30 mins prior to sample immersion. Leave the sample in 1165 at 80°C for 1 hr. Use vertical sample holder basket. Gently agitate with pipette to remove metal fragments. Clean the sample in 3 mins ISO and 3 mins DI rinse.
- If the metal does not lift off cleanly, leave the sample in AZ300T stripper for 30 mins at 80°C. Clean the sample in 3 mins ISO and 3 mins DI rinse.
- Optical microscope - check that the lift-off is clean