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MMIC Power Amplifiers in GaN HEMT and InP HBT Technologies

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by

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Abstract

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Key components in any wireless communication system are the high frequency power amplifiers that must meet strict performance specifications regarding power gain, output power, linearity and power added efficiency (PAE). Class A power amplifiers have high linearity, but exhibit PAE well below 50%. Improved efficiency is obtained with switched-mode circuits. These, unfortunately, show high distortion. Push-pull class B amplifiers offer the potential for improved efficiency, at a theoretical limit of 78.6%, combined with distortion as low as class A. For operation in sub-octave bandwidths, a classical push-pull class B can be replaced by a single-ended class B amplifier with an output bandpass or lowpass filter. The high breakdown voltage ($>$50 V) and 50 GHz current gain cutoff frequency f_τ of an AlGaN/GaN high electron mobility transistors (HEMT) result in record power densities ($>$12.1 W/mm) in the 7-10-GHz frequency band. A common-source class B circuit fabri-

cated in this technology demonstrated 4 W maximum saturated output power at 8 GHz with 13-dB power gain. High linearity, $>$35-dBc intermodulation suppression under two-tone operation and high PAE of 34$\%$ has been achieved under class B operation.

The second phase of research involved developing 75-220-GHz power amplifiers which have applications in wide-band communication systems, atmospheric sensing and automotive radar. Modern InP double heterojunction bipolar transistors (DHBTs) simultaneously exhibit 6 V V_{br}, 400 GHz f_{max}, 3.5 mA/μm^2 collector current density and high thermal conductivity, resulting in high power density in the 75-220-GHz frequency band. The common-base topology exhibits higher maximum stable gain in this band when compared to common-emitter and common-collector topologies. Layout parasitics including base inductance, L_b and collector to emitter overlap capacitance, C_{ce} can cause instability. A single-sided collector contact has been employed to reduce C_{ce}. A single-stage common-base tuned amplifier exhibited 7-dB small-signal gain at 176 GHz. This amplifier demonstrated 8.77 dBm output power with 5-dB associated power gain at 172 GHz. A two-stage common-base amplifier exhibited 8.1 dBm output power with 6.35-dB associated power gain at 176 GHz and demonstrated 9.13 dBm of saturated output power. This two-stage

common-base amplifier exhibited 10.3 dBm output power at 150.2 GHz.

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1 Introduction

The first phase of this research involved developing linear and efficient power amplifiers in Gallium Nitride High Electron Mobility Transistor (GaN HEMT) technology. Common-source class B power amplifiers were built with high linearity and high efficiency. The second phase of research focused on designing and fabricating ultra-high frequency (75-220-GHz) tuned power amplifiers in Indium Phosphide Double Heterojunction Bipolar Transistor (InP DHBT) technology. The common-base topology is used to build these amplifiers as this topology has higher maximum stable gain (MSG) in the 75-220-GHz frequency range, when compared to common-emitter and common-collector topologies.

1.1 GaN HEMT Power Amplifiers

1.1.1 Objective

Modern communications networks using complex modulation formats require efficient power amplifiers with low distortion. class A amplifiers exhibit low distortion but exhibit power added efficiency (PAE) well below 50% [10]. Improved efficiency is obtained with switched-mode amplifiers [2, 3]. These, unfortunately, exhibit high intermodulation distortion (IMD) in multi-tone applications [2, 4]. Push-pull class B amplifiers offer the potential for improved efficiency, at a theoretical limit of 78.6%, combined with distortion potentially as low as class A.

Several key points should be noted regarding efficiency and linearity as a function of amplifier bias point (class A vs classes B and C). First, unlike class A, class B and C amplifiers do not dissipate power when input signals are not present. This is a key advantage in transmitters where signals of strong amplitude or pulse modulation are present. Second, at moderate power levels, approaching but below the amplifier 1-dB compression point ($P_{1-\mathrm{dB}}$), class B amplifier shows higher PAE than class A. Finally, when class A amplifiers are operated at output power levels well beyond the 1-dB gain compression point, the device is driven strongly into both cut-off and

saturation on the peaks of the signal swing, and PAE can substantially exceed the theoretical 50% PAE limit of linear unsaturated class A amplification. These points are relevant to amplifier linearity. In class B operation, at power levels well below $P_{1-\mathrm{dB}}$, it is expected that the distortion is increased relative to that of class A as a result of device switching. This is the penalty incurred for increased PAE. At power levels approaching or beyond $P_{1-\mathrm{dB}}$, in both class A and B the devices are driven into saturation, and substantial distortion is generated. Such high distortion operation is not acceptable in many RF and microwave systems, and the amplifier has to be operated at power levels below $P_{1-\mathrm{dB}}$.

The Gallium Nitride material system is a leading contender for microwave wireless applications due to its superior electrical properties. High electron velocity ($> 10^7$ cm/sec) and wide bandgap (3.4 eV) of AlGaN/GaN material system result in high breakdown voltage ($> 50\ V$) for a current gain cut-off frequency, f_τ of 50 GHz. This results in record power densities. The high thermal conductivity (3.5 W/(cm.K)) of SiC substrates significantly reduces thermal limitations, leading to power density as high as 11.2 W/mm [5].

Previous work in GaN based circuits has demonstrated broadband amplification in class A topology with good linearity [6, 7, 8]. Efficient and linear amplification is

necessary to make this material system useful in the competitive field of RF power amplifiers.

1.1.2 This Work

Switched-mode power amplifiers use transistors as power switches, resulting in high efficiency. In this work, current-mode class D amplifiers are investigated for high efficiency. Class D amplifiers have potential for high efficiency but exhibit poor distortion characteristics.

Classic audio class B amplifiers are implemented in the push-pull configuration [9] today in complementary form, but originally transformer-coupled. In the RF regime, power division and power combining are done using transformers. These transformers provide broadband an even-harmonic short circuit, which is a requirement for efficienct class B operation. The push-pull configuration with transformers results in high bandwidth class B operation. At microwave frequencies, transformers are replaced by microwave baluns. Unfortunately, these baluns cannot produce a broadband even-harmonic short circuit, leading to degradation in PAE. Baluns also occupy expensive die area resulting in associated power losses which further degrade PAE. In this work, a theoretical framework has been developed to understand

the difference between the push-pull topology and single-ended configuration with output band-pass filter in terms of efficiency and linearity. It has been proved that the push-pull and single-ended versions have equivalent linearity. Hence, a push-pull amplifier could effectively be replaced by a single-ended amplifier with an appropriate output band-pass filtering.

The I_d vs. V_{gs} non-linearity and the C_{gs} vs. V_{gs} nonlinearity are prime sources of distortion in class B amplifiers. Bias design has been performed in the framework of a push-pull design. Class B bias has been proven to be the optimum bias condition for best linearity and efficiency. A single-ended class B power amplifier has been successfully fabricated with 13-dB class B gain at 8 GHz. The common-source class B circuit demonstrates high linearity, $>$35-dBc intermodulation suppression, and high PAE of 34$\%$.

The common-drain class B topology is proposed to further improve linearity. Simulations of common-drain class B designs predict a PAE of 45$\%$ with a superior IM_3 suppression of more than 45-dBc over a wide range of bias due to the strong series-series feedback offered by the load resistance. PAE is low for the common-drain amplifier as the transistor exhibits low maximum stable gain in this configuration, requiring an improvement in transistor f_{max} to obtain higher PAE.

1.2 InP DHBT Power Amplifiers

1.2.1 Objective

W-band (75-110-GHz) and G-Band (140-220-GHz) power amplifiers have applications in wide-band communication systems, atmospheric sensing and automotive radar. Successful realisation of amplifiers in this frequency range demands wide-bandwidth transistors. The high electron saturation velocity of InP material system ($3 \times 10^7 \mathrm{cm/sec}$) and deep submicron scaling result in wide-bandwith transistors with high available gain in 75-220-GHz frequency range. New generation InP Double Heterojunction Bipolar Transistors (DHBTs) simulatneously exhibit V_{br} = 6 V, f_{max} = 450 GHz, Collector current density = $3.5 \mathrm{mA}/\mu\mathrm{m}^2$ and high thermal conductivity, resulting in high power density in the 75-220-GHz frequency range.

In a transferred substrate InP Single Heterojunction Bipolar Transistor (SHBT) process, 6.3 dB gain is reported at 175 GHz with a single stage amplifier [11]. However, SHBTs exhibit lower power density due to low breakdown voltage and high thermal resistance. Previous work in W-band amplifiers in transferred substrate process include demonstration of 80 mW output power at 75 GHz [3] and 40 mW output power at 85 GHz [4]. State-of-the-art results in InP HEMT technologies include a

three stage amplifier with 30-dB gain at 140 GHz, a three stage amplifier with 12-15-dB gain from 160-190 GHz, and a three-stage power amplifier with 10-dB gain from 144-170 GHz [14, 15, 16].

1.2.2 This Work

Obtaining high microwave power gain in the 140-220-GHz frequency band is a challenge as the frequency of operation is close to 50% of the f_{max} of the transistors[17, 18]. Class A operation is only possible mode of operation due to power gain considerations.

The common-base topology is chosen as it has higher MSG in this band when compared to common-emitter and common-collector topologies. Common-base gain is, however, reduced by the effect of base lead inductance (L_b) and collector to emitter overlap capacitance (C_{ce}). While these parasitics reduce the common-base MSG, in G-band, the common-base topology still provides the highest gain when compared to the common-emitter and common-collector configurations. If not modeled in the designs, L_b and C_{ce} can cause instability. Base inductance is due to the long thin base contact metal stripes on either side of the emitter. Loop inductance depends upon the current return path; this is difficult to identify in the transistor

geometry, hence L_b is not readily modeled with accuracy. This creates uncertainty in the stability analysis. The collector to emitter overlap capacitance (C_{ce}) also reduces MSG. C_{ce} is the capacitance between the emitter interconnect metal and the collector ohmic contact metal. These metals are separated by $\sim$ 400-500 nm polyimide. This thickness varies in our process, rendering C_{ce} variable. Potential instability in the small-signal characteristics due to L_b and C_{ce} was observed in the first-generation amplifiers fabricated. In second-generation designs, the collector to emitter overlap capacitance was significantly reduced by employing single-sided collector contacts as opposed to double-sided collector contacts. In addition to reducing C_{ce}, this also increases the collector resistance and thus, further increases circuit stability. NiCr resistors provide additional resistive stabilization in some designs.

A single-stage common-base tuned amplifier exhibited 7-dB small-signal gain at 176 GHz. This amplifier demonstrated 8.77 dBm output power with 5-dB associated power gain at 172 GHz. A two-stage common-base amplifier exhibited 8.1 dBm output power with 6.3-dB associated power gain at 176 GHz and demonstrated 9.1 dBm of saturated output power. This amplifier exhibited 10.3 dBm output power at 150.2 GHz. A W-band amplifier demonstrated 15.1 dBm saturated output power at 84 GHz with $>$ 4-dB associated power gain.

1.3 Dissertation Organisation

In chapter 2, the design relationships involving between efficiency and linearity are discussed. Principles of high linearity class A operation are described. Class D amplifiers are presented as an illustration to explain advantages and limitations of switched-mode amplifiers. Design of class D amplifiers is briefly described followed by PAE and linearity simulations based on a simple GaN HEMT model. Class B operation is presented followed by a discussion concluding that the push-pull topology is equivalent to a sigle-ended class B amplifier with appropriate band-pass filtering. Bias design for high linearity and high efficiency class B operation is described. Common-drain topology is proposed to improve class B distortion characteristics further.

Chapter 3 describes GaN HEMT modeling, bias dependent parasitic extraction, GaN HEMT process, simulations and results of common-source class B amplifier.

Chapter 4 presents InP DHBT model extraction, InP DHBT MMIC process, comparison of MSG/MAG between common-base, common-emitter, common-collector topologies, influence of layout parasitics circuit power gain, circuit design methodology and simulations of 75-220-GHz InP DHBT power amplifiers.

Chapter 5 describes device DC and microwave measurements, small-signal and

power measurements for 75-220-GHz power amplifiers and power amplifier results.

Future work and the conclusions are presented in chapter 6. Future work include a design of a frequency doubler at 500 GHz in InP DHBT technology with approximately 22% conversion efficiency.

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2

Tradeoff between Linearity and Efficiency

Simultaneously obtaining high efficiency and high linearity is a constant challenge in designing power amplifiers for communication systems with amplitude or phase modulation. During early history of audio power amplifiers, several ideas for efficient amplification evolved [1]. Different classes of amplification were invented, each presenting its own advantages in terms of efficiency and linearity [2]. Most of these audio-frequency power amplifier configurations could potentially be adapted to design RF wireless applications [3]. The key difference is that, unlike audio power amplifier design, in RF power amplifiers high frequency parasitics have to be carefully considered. For RF power amplifiers whose frequency of operation is a significant fraction of the transistor cutoff frequencies, f_τ and f_{max}, power gain is small, resulting in reduced efficiency. Capacitive non-linearities also influence

circuit distortion characteristics. Input matching is influenced by large-signal input complex impedance which varies with input drive.

2.1 Fundamentals of Power Amplifier Design

Power amplifier design differs from small-signal amplifier design in the way the output of the transistor is matched. Power amplifiers are best designed for maximum output power rather than maximum gain [3]. Power amplifiers also need to be designed for efficiency and linearity.

2.1.1 Power Match vs. Gain Match

In small-signal amplifiers, the amplifier is designed for gain equal to the maximum stable gain (MSG) of the transistor. After stabilising the transistor, the output of the transistor is presented with an impedance that is the complex conjugate of the impedance seen into the output of the transistor (Fig. 2.1).

In power amplifiers, the intrinsic transistor output is presented with an optimum load dictated by the bias point and the large-signal I-V characteristics of the transistor in order to obtain maximum available output power (Fig. 2.2). The optimum

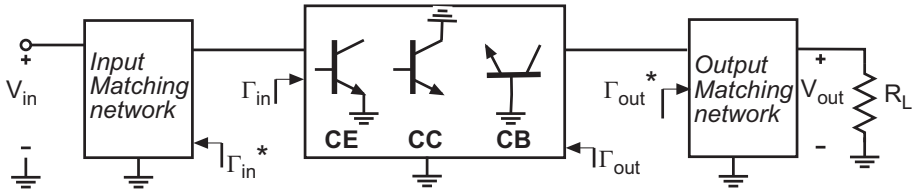

Figure 2.1: Schematic of a small-signal Amplifier

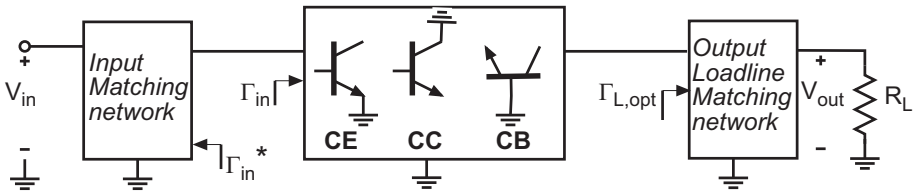

Figure 2.2: Schematic of a power Amplifier

load is given by

$$R_{L,opt} = \left(\frac{V_{br} - V_{knee}}{I_{dss}} \right) , \tag{2.1.1}$$

where I_{dss} is the maximum current, V_{br} is the breakdown voltage and V_{knee} is the knee voltage. As an example, if I_{dss} = 1 A, V_{br} = 55 V and V_{knee} = 5 V, then the optimum load when the transistor is biased at the center of the I-V plane is 50 Ohms. The optimum loadline is shown in Fig. 2.3.

If the load impedance presented to the transistor differs from Eqn. 2.1.1, the

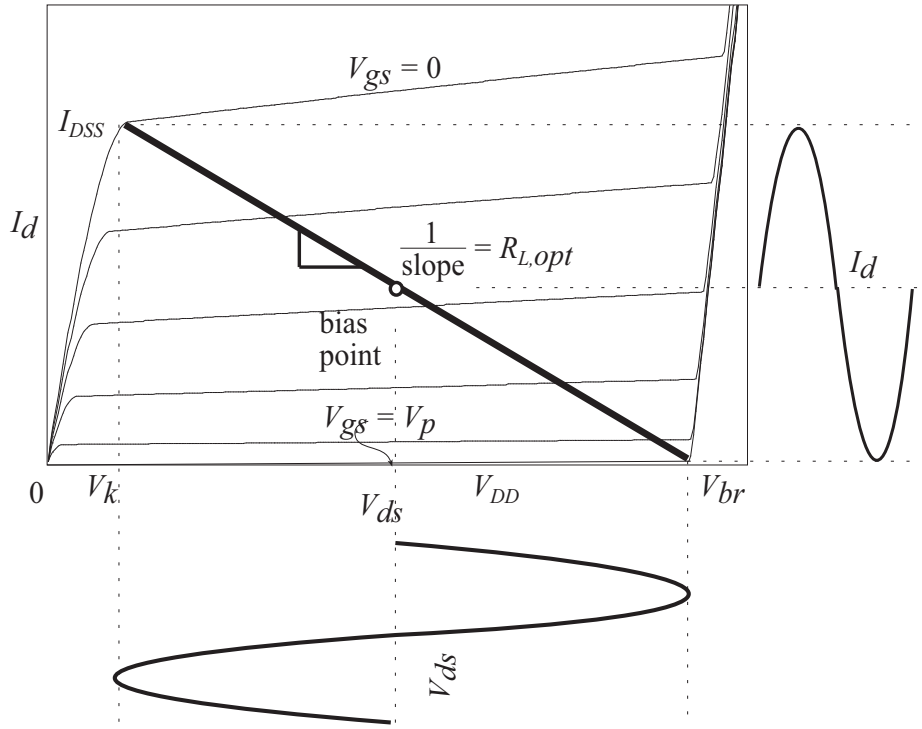

Figure 2.3: Loadline for class A operation

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output power is reduced. In addition to resistive mismatch, the transistor output impedance will itself mistune the load impedance unless compensated by an external inductance.

2.1.2 Efficiency

Commercial power amplifiers are usually designed for high efficiency. Efficient amplification results in extended battery life and less complex thermal management. A few figures of merits to quantify amplifier efficiency are introduced here. Drain efficiency is defined as

$$\text{Drain Efficiency (DE)} = \left(\frac{P_{out}}{P_{DC}}\right) , \tag{2.1.2}$$

where P_{out} is the total RF output power and P_{DC} is the total DC power consumption. Drain efficiency is independent of the power gain of the amplifier. Power Added Efficiency (PAE) is defined as

$$\text{Power Added Efficiency (PAE)} = \left(\frac{P_{out} - P_{in}}{P_{DC}}\right) , \tag{2.1.3}$$

PAE gives the overall efficiency of the power amplifier [3]. Most importantly, observing drain efficiency and power added efficiency gives insight into the influence of power gain on circuit overall efficiency. If the gain is low, PAE would be low even if the drain efficiency is high. In this case, it would be beneficial for the designer to use a transistor with higher gain.

For applications with complex modulation schemes, average efficiency is the best figure of merit to describe circuit efficiency [4]. For signals with high peak to

average ratio, the overall efficiency is low. If P_o is the total RF output power of the amplifier and P_{dc} is the total input DC power of the amplifier, then the average efficiency of the amplifier, η_E is given by

$$\text{Average Efficiency, } \eta_E = \left(\frac{P_o}{P_{dc}}\right) , \tag{2.1.4}$$

Amplifier average efficiency depends on crest factor and peak to average power ratio, which are defined as

$$\text{Crest Factor (CF)} = \left(\frac{\text{Peak Amplitude}}{\text{Average Amplitude}}\right) , \tag{2.1.5}$$

The expression for PAPR is given by

$$\text{Peak to Average Power Ratio, (PAPR)} = \left(\frac{\text{Peak Power}}{\text{Average Power}}\right) , \tag{2.1.6}$$

For example, Orthogonal Frequency Division Multiplexing (OFDM) signals exhibit a high ratio of peak to average power, and the amplifier is therefore operating most frequently at power levels well below saturation. PAE is, thus, impaired.

2.1.3 Linearity

Typically, linearity is achieved at the expense of efficiency. Linear amplification implies that in multi-tone operation, output has no spurious tones in its spectrum.

There are several sources of distortion, and designing for high spurious free dynamic range is challenging. In this section, a few figures of merits to characterise the linearity of a power amplifier are presented.

$\mathrm{IM_3}$ suppression

Ignoring dynamics, the transfer function of a weakly nonlinear system can be approximated by a simple Taylor series expansion.

$$\text{Output Voltage, } V_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 + a_5 V_{in}^5 + ... \quad (2.1.7)$$

When two in-band sinusoidal signals at frequencies ω_1 and ω_2 are applied to the circuit, spurious in-band frequency content is produced due to the odd part of the transfer function. The third-order coefficient, a_3 gives rise to spurious frequency content at ($2\omega_1$-ω_2) and ($2\omega_2$-ω_1). Distortion at these frequencies is called $\mathrm{IM_3}$ distortion. The fifth-order coefficient also creates in-band intermodulation distortion (IMD) at ($3\omega_1$-$2\omega_2$), ($3\omega_2$-$2\omega_1$),($2\omega_1$-ω_2) and ($2\omega_2$-ω_1). The distortion at($3\omega_1$-$2\omega_2$) and ($3\omega_2$-$2\omega_1$) is called $\mathrm{IM_5}$ distortion. Similarly, extending the logic, $\mathrm{IM_7}$ is created due to the seventh-order coefficient. Since, these frequencies are in-band, they cannot be removed by filtering. The harmonic frequency content created due to the nonlinear terms could be removed by filtering by an output tuning network. The

ratio of the power in the fundamental frequencies and the power in IM_3 spurious frequency content is called IM_3 suppression.

$$\mathrm{IM}_3 \text{ Suppression} = 10 \log \left(\frac{\text{Power in fundamental frequencies}}{\text{Power at } (2\omega_1\text{-}\omega_2) \text{ and } (2\omega_2\text{-}\omega_1)} \right) , \qquad (2.1.8)$$

For systems whose transfer functions could be represented by a cubic polynomial that remains the same irrespective of the output power, the slope of the intermodulation distortion with respect to the output power is 3:1. However, many transfer functions are not infinitely differentiable and could not accurately be represented by a simple Taylor series expansion. Apart from this, fifth-order and seventh-order coefficients also create distortion at ($2\omega_1$-ω_2) and ($2\omega_2$-ω_1) with amplitude varying in proportion to the fifth and seventh power of the input signal amplitude. This leads to a significant deviation from that 3:1 slope.

Adjacent Channel Power Ratio (ACPR)

Two-tone analysis gives a first order understanding to the amplifier's linearity. For complex modulation schemes, two-tone analysis may not be sufficient. ACPR takes into consideration the intermixing of several in-band frequencies that create the adjacent channel spurious frequency content. ACPR is defined as the ratio of the power in the signal frequency band to the power in the adjacent channel (Fig. 2.4).

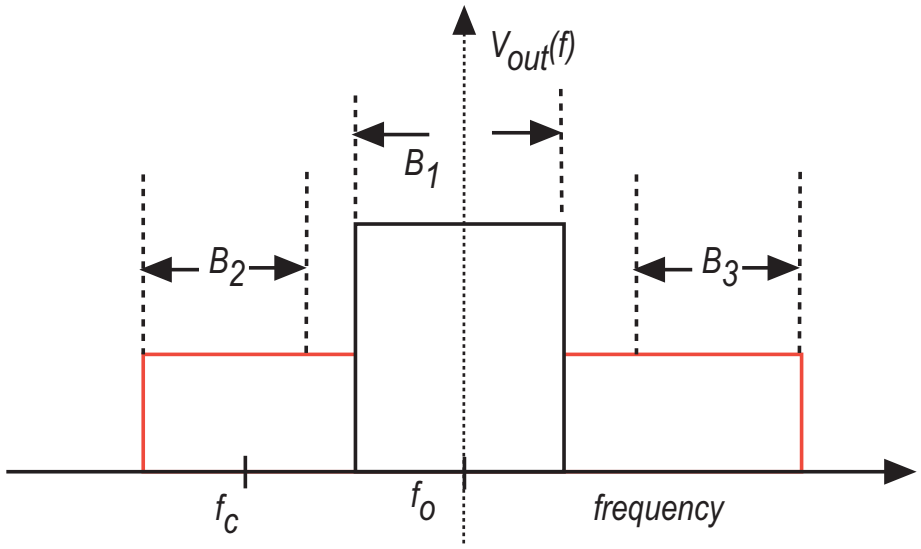

Figure 2.4: Adjacent Channel Power Ratio

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[6] ACPR can be expressed as

$$\text{ACPR } = 10 \log \left(\frac{\text{Power in } B_1}{\text{Power in } B_2, B_3} \right) , \tag{2.1.9}$$

2.2 Summary of Different Classes of Operation

The class of a power amplifier is dependent on the bias point and the transistor output loadline. The class A power amplifier exhibits maximum power gain, high linearity, but low PAE. For power amplifiers whose frequency of operation is

a significant fraction of transistor f_τ and f_{max}, class A could be the only mode of operation due to power gain considerations.

Class B power amplifiers are biased with V_{gs} equal to the threshold voltage. They exhibit approximately 6-dB less power gain than class A. Average efficiency of class B is higher than that of class A. Linearity of class B power amplification will be considered later. Class A amplifiers are biased such that the drain current is 50% of its maximum value over the signal swing. Class AB amplifiers are biased at a drain current less than half of the maximum value.

Switched-mode amplifiers employ transistors as power switches. Class D, class F and class E are switched-mode amplifiers and they differ from each other in the way the transistor output is tuned at various harmonic frequencies. These amplifiers exhibit low gain, high PAE and very poor distortion.

Class H and class G amplifiers use class A or class B input bias, but the output bias is modulated depending on the input drive, rendering high PAE operation. During the course of this work, class H and class G amplifiers are investigated. These topologies exhibit high PAE and linearity at frequencies well below f_τ/10. At frequencies beyond f_τ/10, however, these topologies suffer from high distortion.

2.3 Class A Operation

In class A operation, the transistor is biased in the middle of the I_d vs. V_{ds} plane as shown in Fig. 2.3. At sufficiently high input power, the drain voltage and current waveforms reach the cut-off and the knee voltage of the transistor. Distortion generated by the amplifier increases rapidly once the transistor is driven to this point. The total output power,P_{out} at the threshold clipping is given by

$$P_{out} = \left(\frac{V_{br} \times I_{dss}}{8} \right) , \tag{2.3.1}$$

2.3.1 Advantages

In class A, the transistor small-signal parasitic elements are relatively invariant through the signal swing operation yielding low distortion operation. This simplifies the design. However, the linearity degrades at higher input powers when the load-line reaches the knee or cutoff. High bandwidth could be obtained as the harmonic frequencies need not be tuned.

Since the transistor is always on, the large-signal gain is the highest in this configuration. For power amplifiers whose frequency of operation is a significant fraction of f_{max}, class A can be the only possible mode of operation with reasonable

power gain.

2.3.2 Disadvantages

Efficiency of class A operation is low. The maximum output power is $1/8$th of the area of the I_d-V_{ds} plane, while the DC input power is 25% of the I_d-V_{ds} plane resulting in a maximum theoretical drain efficiency of 50%. For modulation schemes with high Peak to Average Power Ratio (PAPR) average efficiency of class A is low. Average efficiency of the amplifier in class A operation falls well below 50% as the transistor is always on irrespective of input signal power level. This results in very low PAE for signals whose average to peak ratio is small.

Since PAE is very low, high power class A amplifiers must have efficient heat removal. Substrate with high thermal conductivity is needed for high power operation. For HBTs, thermal runaway and associated current instability must be suppressed. This often needs added extra ballasting resistances that reduce power gain.

2.3.3 Example

To illustrate class A power amplifier operation, the following example is considered with a simple transistor model, as shown in Fig. 2.5.

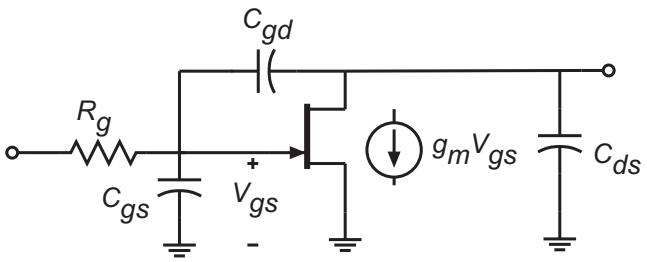

Figure 2.5: A simple transistor model

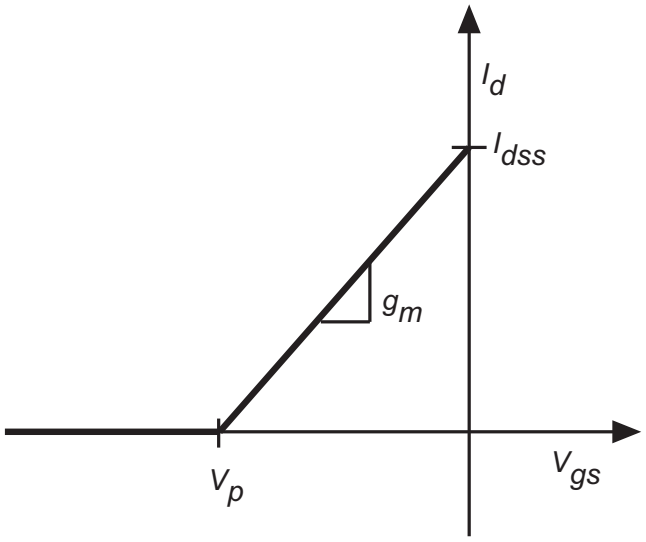

Figure 2.6: Transfer characteristics of the model shown in Fig. 2.5

The I_d vs. V_{gs} of the transistor is shown in Fig. 2.6. Let us assume the following. Transistor parameters, maximum saturation current, I_{dss} = 1 A/mm, V_{br} = 50 V,

V_{knee} = 5 V, V_p = -5 V. Assuming linear characteristics above threshold, g_m = 0.2 S/mm. If f_τ = 50 GHz, and if C_{gd} = 0.2 $\times$ C_{gs}, then C_{gs} is given by

$$C_{gs} + C_{gd} = \left(\frac{g_m}{2\pi f_t}\right) = 0.64\text{pF/mm}, \tag{2.3.2}$$

If f_{max} = 100 GHz, gate resistance R_g is given by

$$R_g = \left(\frac{{f_{max}}^2}{8\pi f_t C_{gd}}\right) = 1.5 \text{ Ohm.mm.}, \tag{2.3.3}$$

The drain-source capacitance, C_{ds} occurs due to field coupling between the drain and the source through the substrate and is assumed to be 0.15 pF/mm. The model is highly simplified; parasitics are bias variant and the overall model includes numerous other elements.

A class A power amplifier is designed at 5 GHz. The circuit schematic is shown in Fig. 2.7. The transistor is biased at the center of the output I_d- V_{ds} plane. The gate is biased at $V_p/2 = -2.5V$. The drain is biased at 0.5$\times$(V_{br}-V_k)= 27.5 V. The load line of the transistor is shown in Fig. 2.8. The power gain is 12.5 dB. P_{in} Vs. P_{out} and PAE vs. P_{in} are shown in Fig. 2.9. $P_{1-\text{dB}}$ is 38 dBm with a corresponding one-tone efficiency of 55%. $PAE > 55\%$ is achieved after the transistor is driven into saturation. This, however, is not linear class A operation as the transistor is

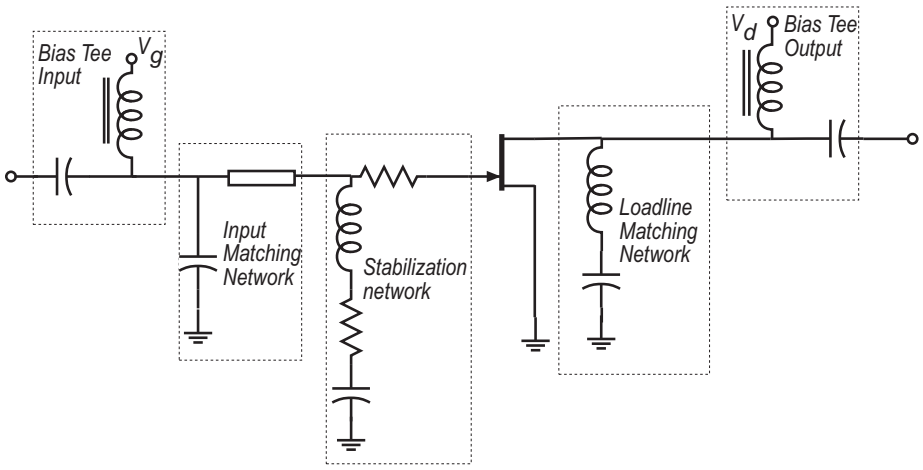

Figure 2.7: class A power amplifier schematic

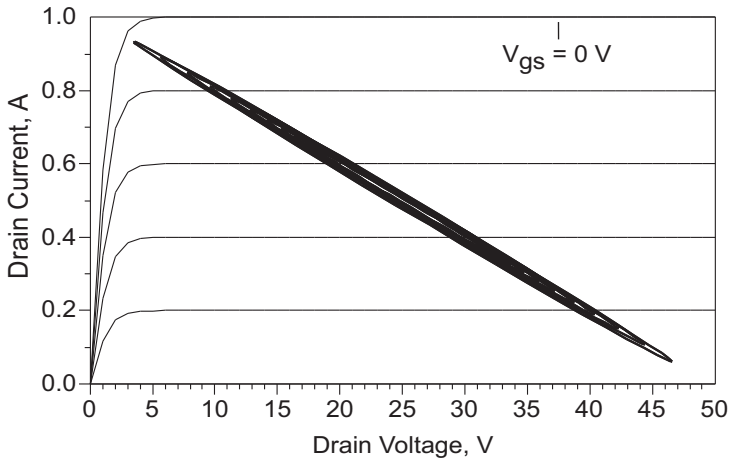

Figure 2.8: Loadline of the class A amplifier

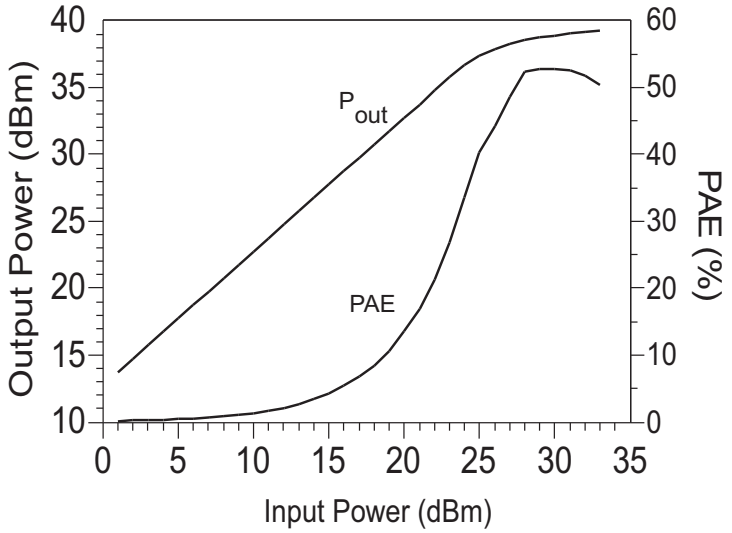

Figure 2.9: Output power, PAE vs. input power

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driven into saturation and distortion is high. Efficiency at 6 dB below the $P_{1-\mathrm{dB}}$ is only 12%. IM_3 suppression as a function of the output power is shown in Fig. 2.10. Since the model assumes linear I_d vs. V_{gs} above threshold, there is no distortion till the drain voltage reaches V_{knee} or until drain current reaches 0 A. Hence, at high output power levels close to $P_{1-\mathrm{dB}}$ IM_3 suppression rapidly becomes worse. From the above simulations, it could be concluded that class A IM_3 performance is good, but that efficiency is poor. Note that in this analysis we assumed that g_m is constant above threshold. This, however, depends on the specific transistor technology. If

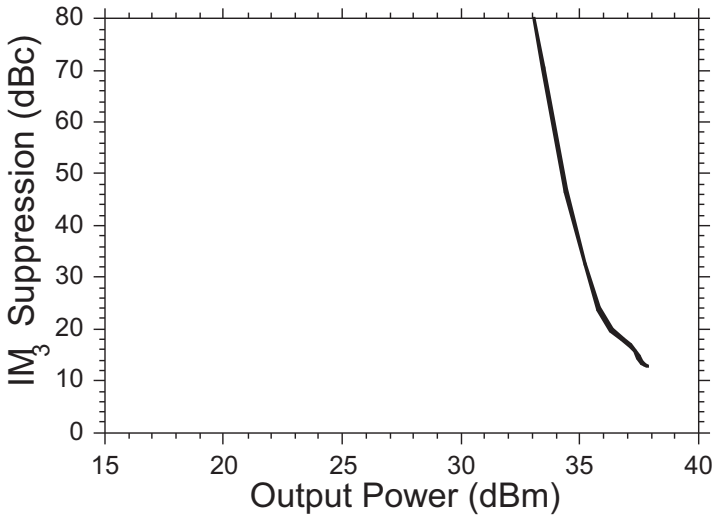

Figure 2.10: IM_3 suppression as a function of the output voltage

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high linearity is required, source degeneration (Fig. 2.11) can be used to improve the linearity at the expense of reduced power gain and PAE. By making the load as the source degeneration resistance, i.e by switching to common-drain topology, it is possible to have high drain efficiency. High PAE is then obtained if the gain is high. Typically, common-drain topology exhibits low maximum stable power gain leading to a much degraded PAE. If the signal frequency is well below f_{max}, however, gain can be high, hence high PAE can be obtained.

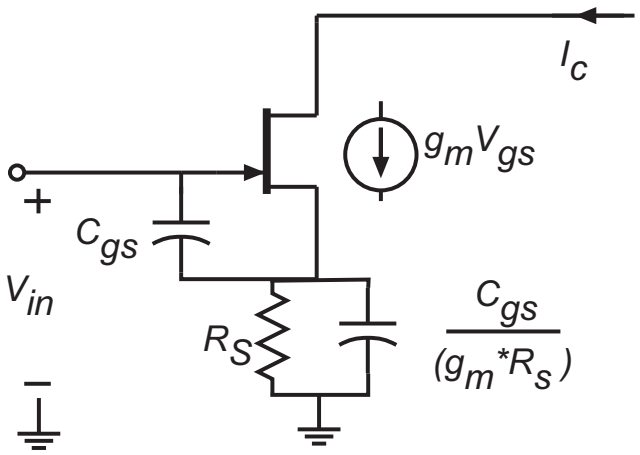

Figure 2.11: Source degeneration to improve linearity

2.4 Class D operation

Switched-mode amplifiers can potentially provide a maximum theoretical PAE of 100% [2]. Transistors act as power switches for switched-mode high efficiency power amplification. The class D amplifier is described below as an illustration to understand the advantages and limitations of switched-mode operation.

2.4.1 Principle of Operation

The idealised voltage-mode class D switch is shown in Fig. 2.12. The switched-mode amplifier should have 100% efficiency in the idealization of infinite switch

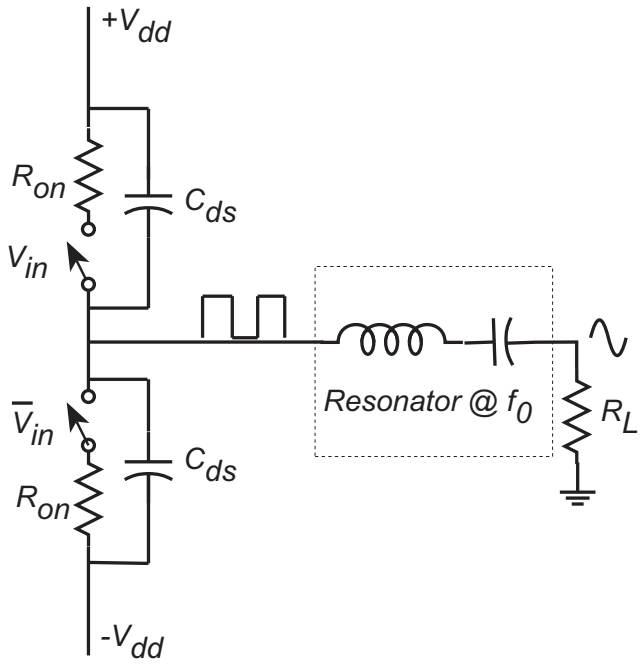

Figure 2.12: Voltage-mode class D Operation

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bandwidth and zero on resistance.

The idealized voltage-mode Class-D power switch converts the driving data pattern to amplitude $[+V_{dd}, -V_{dd}]$. With a filter in the form of a series resonant circuit, there is zero out-of-band dissipation in the load resistance, and circuit efficiency is 100%. At a frequency of operation approaching the transistor bandwidth, switching losses will reduce the amplifier power-added-efficiency (PAE). The drain-source ca-

pacitance, C_{ds} must be charged and discharged to the full power supply voltage for each clock cycle. In the limit of small R_{on}, its direct influence on efficiency is negligible. However, the energy $1/2\mathrm{V}_{\mathrm{dd}}^{2}\mathrm{C}_{\mathrm{ds}}$ stored in the capacitor C_{ds} is dissipated in R_{on}, during each switching cycle, even for infinitesimally small R_{on}. Consequently, the voltage-mode class D power amplifier has less than 100% PAE. Expressions for P_{out}, P_{wasted}, P_{wasted}/P_{out} are shown below.

$$P_{out} = \frac{2V_{dd}I_{peak}}{\pi} \tag{2.4.1}$$

$$V_{br} = \frac{V_{dd}}{2} \tag{2.4.2}$$

$$P_{wasted} = C_{ds}(2V_{dd})^2 f \tag{2.4.3}$$

$$\frac{P_{wasted}}{P_{out}} = \pi \frac{V_{br}}{I_{peak}} C_{ds} f \tag{2.4.4}$$

Use of a current-mode class D switch immediately reduces output switching losses [7]. The current-mode class D schematic is shown in Fig. 2.13. This configuration is obtained by applying duality to the voltage-mode class D configuration. Losses are low for the current-mode class D beacuase the switches close synchronous to the times when V_{ds} is zero.

Since, the voltage across the power switch is small when the switch is closed, the C_{ds} switching losses could be minimised. With the model depicted in the Fig. 2.5,

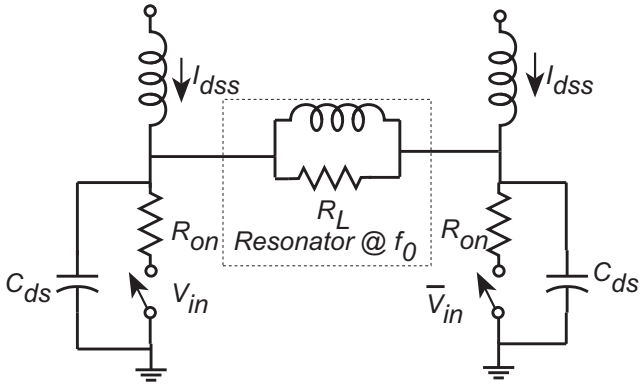

Figure 2.13: Current-mode class D Operation

simulations for the current-mode class D could be performed at 5 GHz. The circuit diagram is shown in Fig. 2.14. Ideally, the voltage waveforms at the two drains are half sinusoids and the drain current waveforms are square waveforms. The peak voltage of any of the drain half sinusoids should not exceed V_{br}. The maximum current is I_{dss}. Under the maximum drive conditions, when the peak drain voltage is V_{br}, the drain bias should be V_{br}/π, i.e, with V_{br} = 50 V, V_{dd} is approximately 15 V. The gates are biased at the pinch-off voltage. The output tuning network is designed so that the switching takes place when the drain voltage is minimum to minimise power losses in discharging C_{ds} through the transistors. The drain current and the drain voltage waveforms are shown in Fig. 2.15. Note that under high input powers,

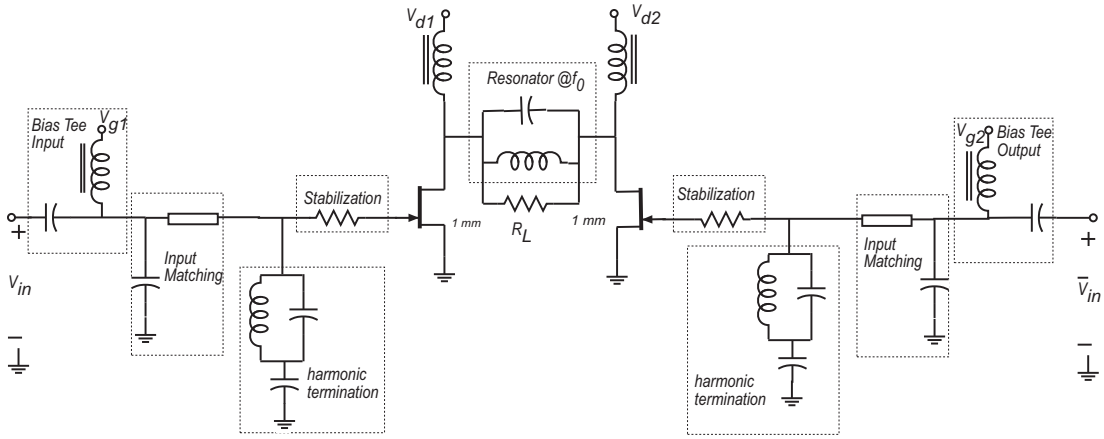

Figure 2.14: Current-mode class D Schematic

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the drain current is close to I_{dss} and V_{ds} is close to zero. When the drain voltage is high, the drain current is zero. This leads to high PAE operation. The output power and PAE vs. input power are shown in Fig. 2.16. The maximum saturated output power is 41 dBm and the maximum PAE is 72%. IM_3 suppression vs. output power is shown in Fig. 2.17. The IM_3 suppression is close to 7 dBc. The distortion is very high, as expected. To summarize, PAE is high(72%), but linearity is very poor (<10-dBc). Other switched-mode amplifiers including classes E and F have performance similar to that of Class D. Such amplifiers can be used effectively with constant envelope signals (QPSK and BPSK signals).

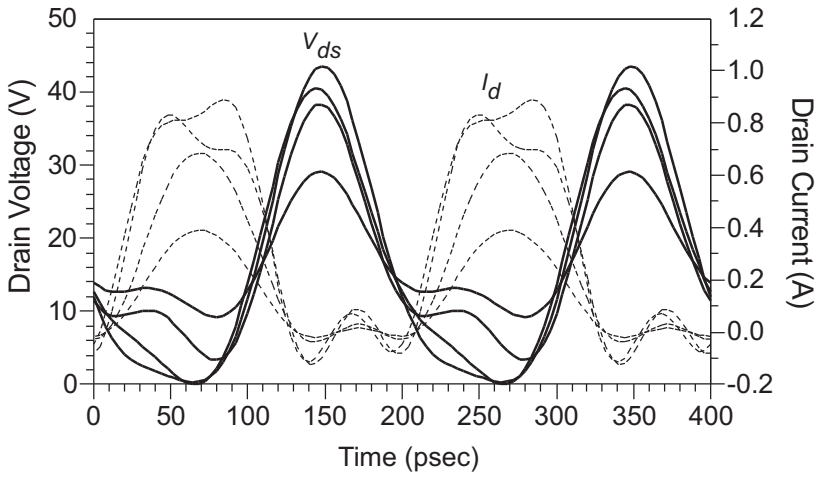

Figure 2.15: Transistor drain voltage and drain current waveforms. The input power is increased in steps of 5 dB.

2.5 Push-pull Class B Operation

The transistor is biased at the threshold voltage for class B operation. Drain voltage bias for class B operation is $V_{br}/2$. The desired loadline is shown in Fig. 2.18.

Push-pull common drain class B is popular in audio power amplifiers. The usage of push-pull configurations dates back to the age of vacuum tubes [1]. Complementary devices or transformers are necessary for push-pull operation (Fig. 2.19) [8]. The transformers provide with the even-mode output short circuit that is necessary for efficient class B amplification (Fig. 2.20).

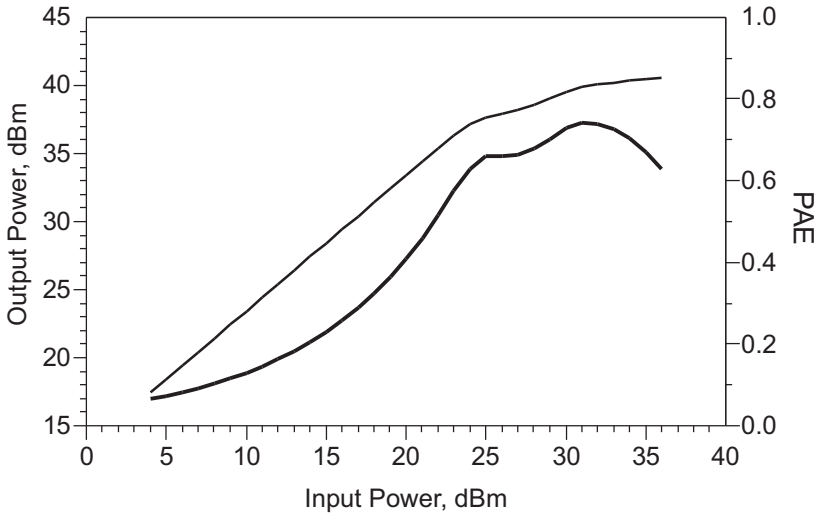

Figure 2.16: Output Power and PAE vs. input power for current-mode class D

Efficient broadband class B amplification is unfortunately not feasible at microwave frequencies due to the lack of available baluns with the required zero-ohm even-mode impedance. Push-pull operation cancels even-order distortion by means of symmetry. The push-pull configuration takes an exact replica of the single device transfer function and creates an image about the current (Y) axis and subtracts it from the original transfer function. If the transfer function of a single device is

$$\text{Output Current, } I_d = f(V_{in}) = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 + a_4 V_{in}^4 + a_5 V_{in}^5 + \ldots\ldots \quad (2.5.1)$$

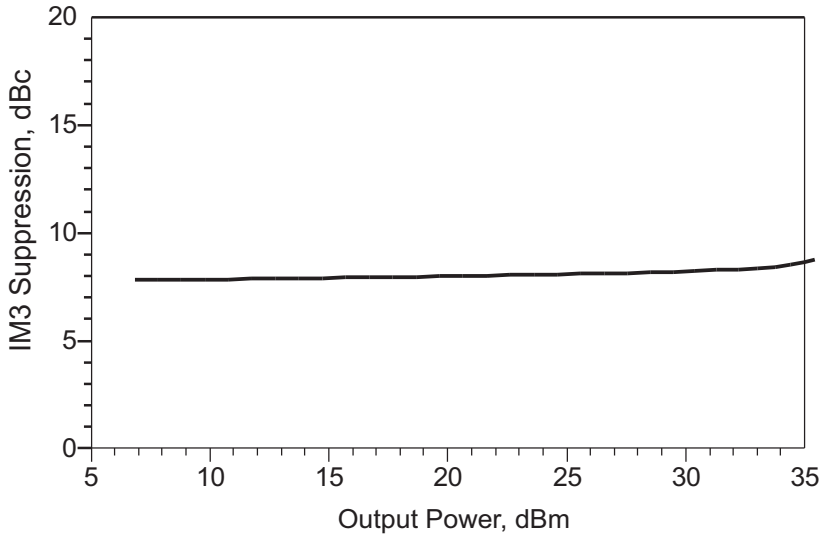

Figure 2.17: IM_3 suppression vs. Output power for current-mode class D

Then, with push-pull the total transfer function becomes

$$\text{Output Current, } I_d = f(V_{in}) - f(-V_{in}) = 2(a_1 V_{in} + a_3 V_{in}^3 + a_5 V_{in}^5 + ...) \quad (2.5.2)$$

We must emphasize that push-pull operation, through its symmetry, suppresses only even-order (second-harmonic) distortion (Fig. 2.21). Odd-order components in the circuit transfer function, and the resulting two-tone third order intermodulation distortion are not suppressed. Efficient class B requires significant drain currents at even harmonic frequencies in order to realize the ideal half-sinusoidal drain current waveform. For example, at the class B conduction angle of 180 degrees, the second

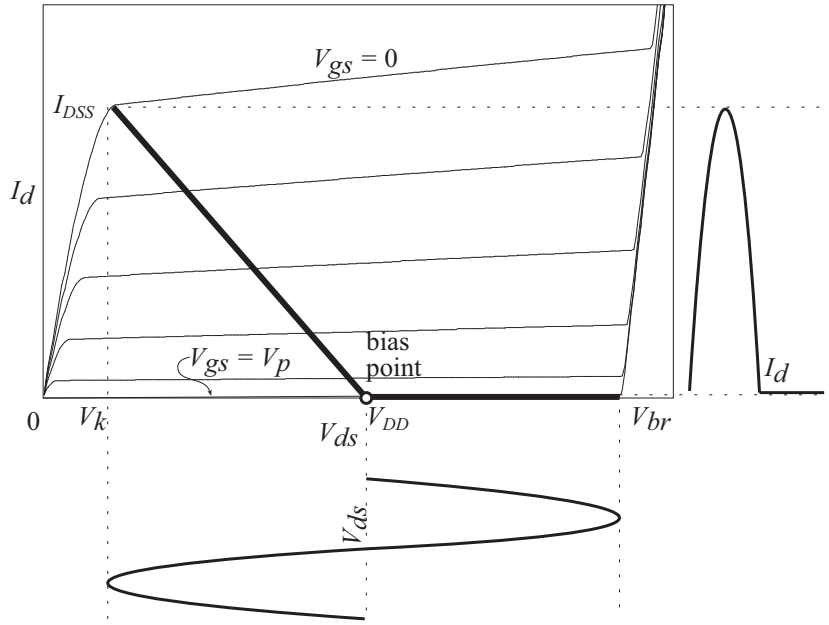

Figure 2.18: Loadline under class B bias

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harmonic current is $\left(\frac{4}{3\pi}\right)$ times the fundamental current to achieve this condition. Yet, the drain voltage amplitude at the second-harmonic must be zero. This requires either a second harmonic short circuit or suppression of the second harmonic current by push-pull symmetry. Marchand, Lange and Wilkinson baluns that present high impedance at even-mode signals, do not provide the required even-mode short circuit. This is in marked contrast to the situation at radio frequencies, where ferrite loaded baluns provide the required even-mode impedance. The permeability of most

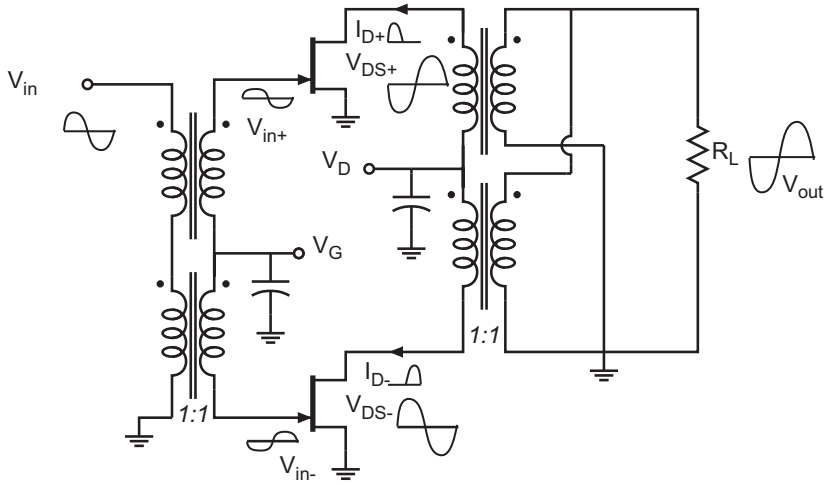

Figure 2.19: Class B schematic with transformers

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ferrites is, however, low at microwave frequencies and transformers are therefore not feasible. Given the use of baluns without the required even-mode termination, efficiency will be degraded. In addition, microwave baluns are physically large (of the order $\lambda/2$), which results both in large excess consumed IC die area and in large excess line losses with resulting further degradation in efficiency.

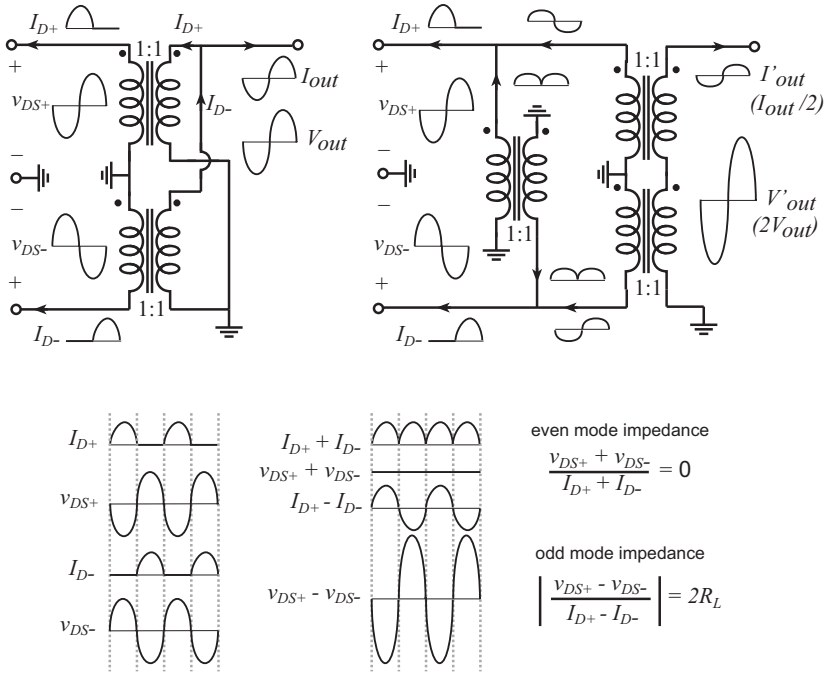

Figure 2.20: Even-mode, Odd-mode analysis of class B amplifier with the transformers

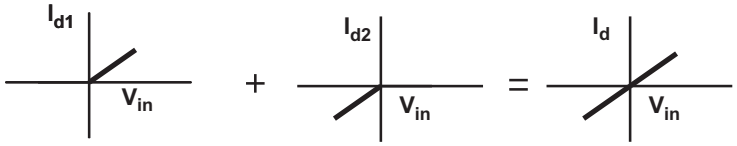

Figure 2.21: Graphical representation of push-pull configuration

2.6 Single-ended Class B Operation

Let us consider the effect of band-pass filtering on the transfer function of a single device. Any function can be written as a sum of an even and an odd function,

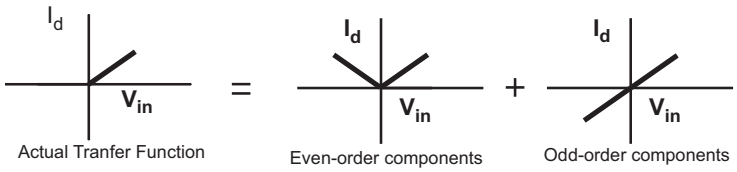

Figure 2.22: Decomposition of single-ended class B transfer function

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as shown in Fig. 2.22.

$$I_d = f(V_{in}) = \left(\frac{1}{2}\right)(f(V_{in}) + f(-V_{in})) + \left(\frac{1}{2}\right)(f(V_{in}) - f(-V_{in})) \qquad (2.6.1)$$

The even part consists of the DC term and the even powers of V_{in}, and the odd part consists of the odd powers of V_{in}.

$$\left(\frac{1}{2}\right)(f(V_{in}) + f(-V_{in})) = a_0 + a_2 V_{in}^2 + a_4 V_{in}^4 + ..., \qquad (2.6.2)$$

$$\left(\frac{1}{2}\right)(f(V_{in}) - f(-V_{in})) = a_1 V_{in} + a_3 V_{in}^3 + a_5 V_{in}^5 + ... \qquad (2.6.3)$$

The even part of the transfer function creates harmonic frequency content and even-order intermodulation distortions, which are removed by the band-pass filter. The odd part creates in-band intermodulation distortions, which cannot be filtered. A bandpass filter centered at the signal frequency, filter removes the harmonic distortion caused by the odd components of the transfer function. Third-order in-band intermodulation distortion characteristics of class B push-pull circuits, therefore, do

not differ from that of a single-ended class B amplifier. Consequently, for power amplifier applications requiring less than 2:1 frequency coverage, push-pull operation is entirely unnecessary. Instead, all harmonic Fourier components of the transistor drain current waveform can be supplied (provided with the required low impedance) through use of an output band-pass filter, centered at the signal fundamental, and a single transistor stage can be employed. Drain voltage harmonic distortion is likewise suppressed by the low impedance at harmonic frequencies presented by the output filter. Third-order intermodulation characteristics are identical for both push-pull and the single-ended configurations. Given an operating bandwidth requirement of less than an octave, a single-ended class B amplifier can provide both high linearity and drain efficiency approaching 78.6$\%$.

Two-tone third-order distortion characteristics depend critically upon the class B bias point, whether for single-ended or for the equivalent push-pull configuration. Bias design is, however, most easily discussed in the framework of the push-pull stage. With drain current, I_d, the push-pull output current is

$$I_{out} = I_d(V_{in}) - I_d(-V_{in}) \tag{2.6.4}$$

The circuit diagram of the push-pull common source class B is shown in Fig. 2.19. An ideal push-pull power amplifier is assumed and the transfer function is observed

as a function of the bias voltage relative to threshold. The class C has a range of input voltage for which neither of the devices is on. This non-linearity causes cross-over distortion. At class B bias, there is no cross-over distortion, and if the transfer function of the device is linear above threshold, the net transfer function is linear. For class AB bias, the two devices will be simultaneously on for part of the signal cycle. In this case, if the transfer function is linear above threshold, circuit gain is doubled for that portion of the transfer function in which both devices are on. Distortion is therefore generated. Finally, for class A bias, both devices will be on simultaneously over the entire signal cycle. Hence, the transconductance will be twice of a single device, and the transfer function will be linear, provided that the device has constant g_m above threshold. Class B can therefore provide both high efficiency and moderately low distortion provided that the device g_m is constant near threshold. The distortion of class B is very sensitive to the specific slope of I_d-V_{gs} characteristic, particularly near threshold. The arguments above are graphically described in Fig. 2.23.

In the above discussion, distortion due to voltage variable input capacitance, C_{gs} was neglected. For signal frequencies larger than approximately f_τ/10, the distortion due to input capacitance variation can be comparable to that arising from the

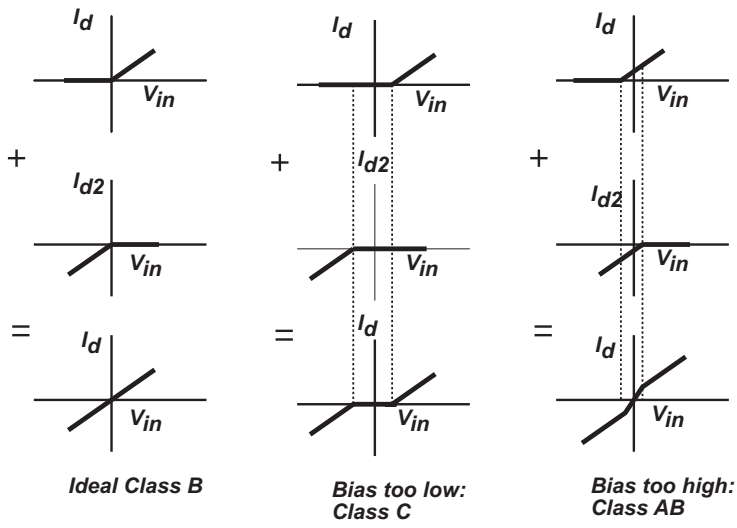

Figure 2.23: Bias design for common-source power amplifier

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g_m variation above threshold. The non-linearity in the gate charge and therefore input capacitance introduces distortion in the gate voltage waveform. The third-order charge term contributes to the in-band IMD. The charge stored in C_{gs} can be expressed as

$$Q = q_0 + q_1 V_{in} + q_2 V_{in}^2 + q_3 V_{in}^3 + ... \tag{2.6.5}$$

The gate current is then

$$i = \frac{dQ}{dt} = q_1 \frac{dV_{in}}{dt} + 2q_2 V_{in} \frac{dV_{in}}{dt} + 3q_3 {V_{in}}^2 \frac{V_{in}}{dt} + ... \tag{2.6.6}$$

By definition,

$$C(V) = \frac{dQ}{dV} = q_1 + 2q_2V_{in} + 3q_3{V_{in}}^2 + ... = c_0 + c_1V_{in} + c_2V_{in}^2 + ... \quad (2.6.7)$$

Hence, the gate current is

$$i = c_0\frac{dV_{in}}{dt} + c_1V_{in}\frac{dV_{in}}{dt} + c_2{V_{in}}^2\frac{V_{in}}{dt} + ... \quad (2.6.8)$$

The second-order coefficient, c_2 in C(V)characteristics contributes to in-band 3rd-order intermodulation distortion, while the fourth-order coefficient, c_4 contributes to in-band IM_5 distortion. In general, all even-order terms in 2.6.7 contribute to in-band intermodulation distortion, and should be compensated or canceled for best linearity. Zero IM_3 requires that the even components $C_{gs,even}$, be zero.

$$C_{even} = c_2V_{in}^2 + c_4V_{in}^4..... = \left(\frac{1}{2}\right)(C_{gs}(V_{gs}) + C_{gs}(-V_{gs})) - c_0 \quad (2.6.9)$$

Experimental data of GaN HEMTs exhibit a $C_{gs}(V_{gs})$ which is very nearly anti-symmetric about $V_{gs} = V_{th}$. In this case, biasing the devices at class B results in minimum $\mathrm{C}_{\mathrm{even}}$, and minimum resulting IM_3. This is shown graphically in Fig. 2.24 for different bias conditions. If biased at class B, the even order components of C_{gs} are small due to the anti-symmetric characteristics of the C_{gs} about the pinch-off voltage. When biased slightly above threshold (class AB), the C_{gs} characteristic

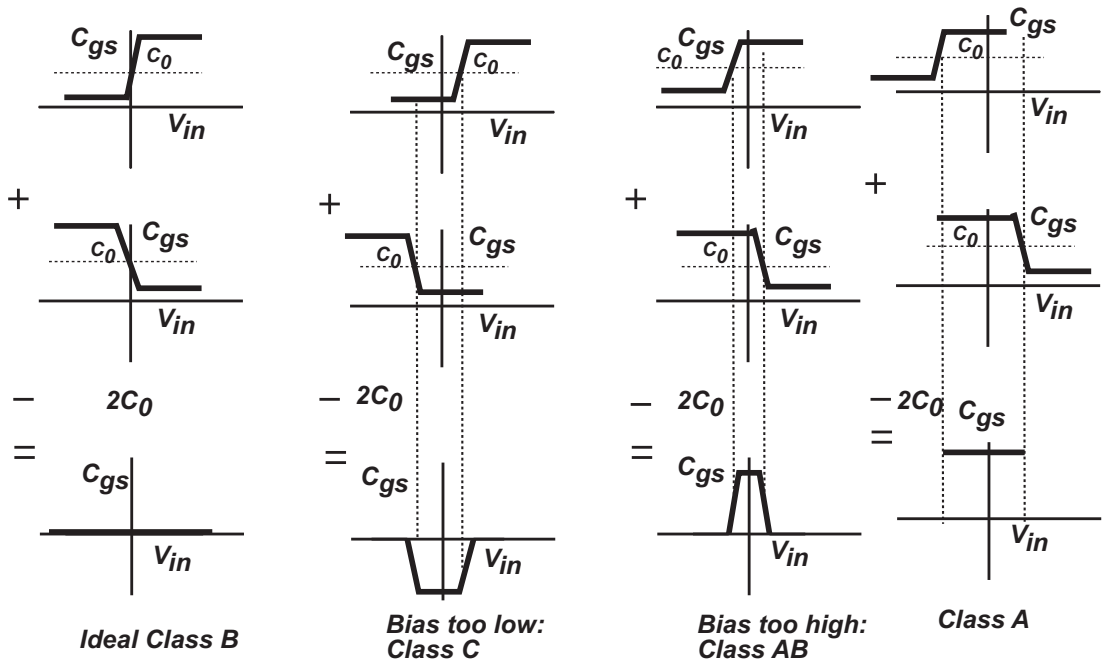

Figure 2.24: Bias design for nonlinear C_{gs} for a common-source amplifier

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has significant even order components that contribute to the distortion in the gate voltage waveform with resulting degradation in the distortion. In class A operation, however, the input capacitance is almost constant over the signal swing and the distortion is low. Once again, to the extent to which C_{gs} is anti-symmetric about the device threshold, distortion is suppressed by biasing the device at threshold, e.g. class B bias.

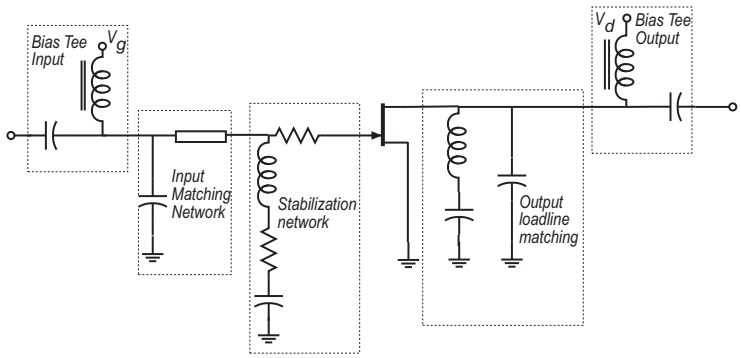

Figure 2.25: Schematic of a class B circuit

2.6.1 Example

With the model depicted in the Fig. 2.5, simulations for the class B power amplifier are performed at 5 GHz. The circuit diagram is shown in Fig. 2.25. The even-harmonic at the drain are short circuited for maximum PAE. Note that the drain current waveform is a half sinusoid with strong even-harmonic currents. If the even-harmonics are not short-circuited, the drain voltage will have a non-zero even-harmonic. This will cause the loadline to deviate from Class B, resulting in a reduction in PAE. In the schematic shown in Fig. 2.25, a parallel LC band pass filter is used to provide this even harmonic short. The drain-source capacitance (C_{ds}) of the transistor is absorbed in the output network. The class B load line, P_{in} vs. P_{out}

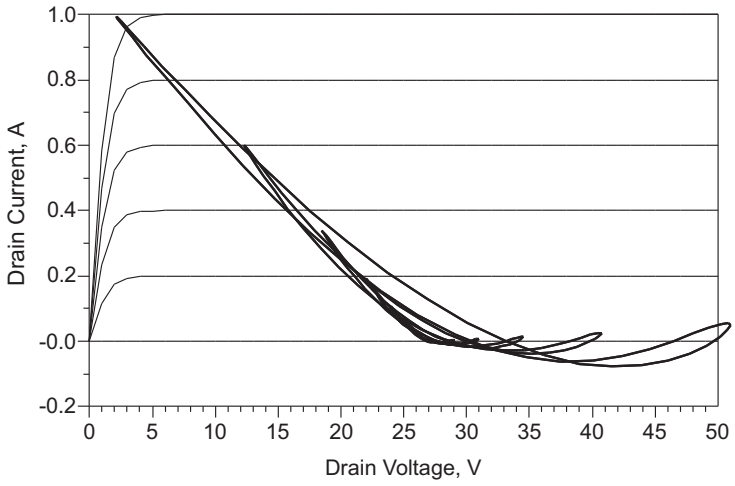

Figure 2.26: Class B loadline at $P_{1-\mathrm{dB}}$ and at 5 dB and 10 dB below $P_{1-\mathrm{dB}}$

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and the IM_3 suppression as a function of the output power are shown in Fig. 2.26, Fig. 2.27 and Fig. 2.28. The transistor is biased at the threshold voltage and the drain bias voltage is equidistant between the knee voltage ($\sim$5V) and the breakdown voltage (50 V). The channel width is 1 mm. The $P_{1-\mathrm{dB}}$ gain compression point is 38 dBm (6.3 W/mm power density). Since linear characteristics are assumed above the threshold, IM_3 suppression is high (Fig. 2.28). Given transistors with finite non-linearity in its I_{ds} vs. V_{gs} characteristics, distortion will be produced. The bias point is changed from class AB (V_{gs} is biased between class A and class B) to class C (biased below pinchoff). The IM_3 performance for class AB, class B and class A as

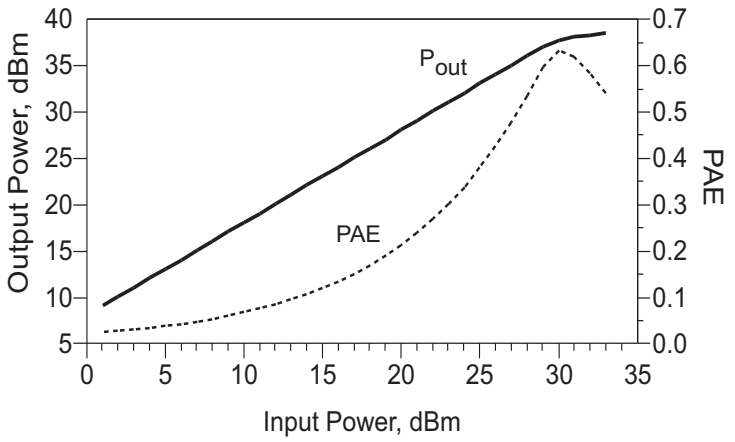

Figure 2.27: Output Power vs. Input Power for class B

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a function of output power is shown in Fig. 2.29. Class AB has good IM_3 performance at low power levels, but becomes poor at medium power levels as can be seen in Fig. 2.29. Class C has high distortion due to crossover distortion. To complete the analysis, the single tone PAE of class AB, B and C are shown in Fig. 2.30. Class C and class B exhibit similar efficiency, but the efficiency of class AB is lower. From above comparisons, it is clear that for transistors with characteristics similar to those shown in Fig. 2.6, class B is the optimum bias point in terms of linearity and efficiency. A common-drain class B topology is also proposed to improve the linearity further using strong series-series feedback offered by the load resistance.

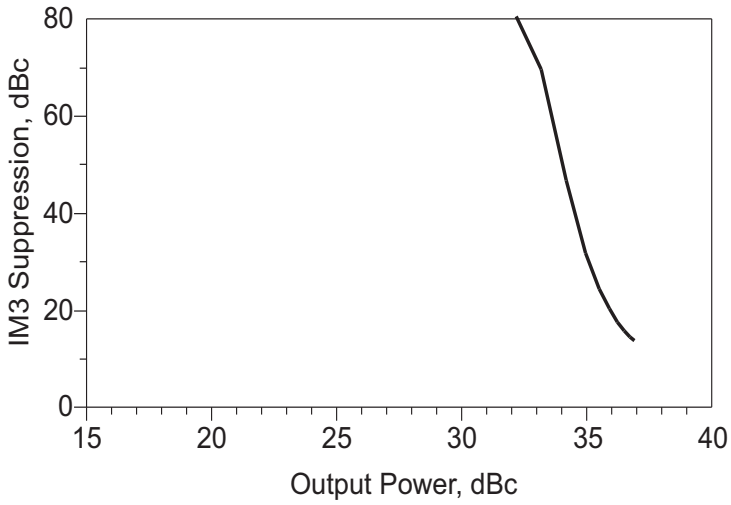

Figure 2.28: IM_3 suppression vs. Output Power for class B

2.7 Common-drain Class B

Bipolar implementation of the push-pull common collector class AB amplifier is the most widely used topology in the audio regime. The High Electron Mobility transistor (HEMT) equivalent, the common-drain amplifier, has the potential to a linear amplification with good efficiency, when biased at or above class B. For common source class B the transfer function is

$$\left(\frac{V_{out}}{V_{in}}\right) = g_{m,nonlinear} R_{Load} \tag{2.7.1}$$

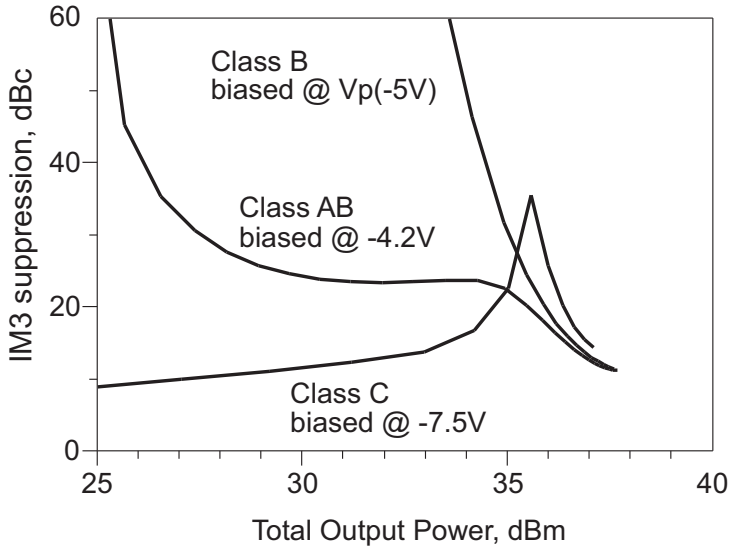

Figure 2.29: Comparison of IM_3 suppression vs. output Power for class AB, B and C

Variation in the transconductance, $g_{m,nonlinear}$ directly produces non-linearity of the overall circuit transfer function. However, for the common-drain configuration, the transfer function is

$$\left(\frac{V_{out}}{V_{in}}\right) = \left(\frac{g_{m,nonlinear} \times R_{Load}}{1 + g_{m,nonlinear} \times R_{Load}}\right) \tag{2.7.2}$$

As $g_{m,nonlinear}$ is made large in comparison with the conductance of the load ($1/\mathrm{R}_{\mathrm{Load}}$), the effect of transconductance variation, $g_{m,nonlinear}$ on circuit gain is reduced. The strong series-series negative feedback presented by the load linearises the amplifier. The linearity is most directly analysed in the framework of the push-pull con-

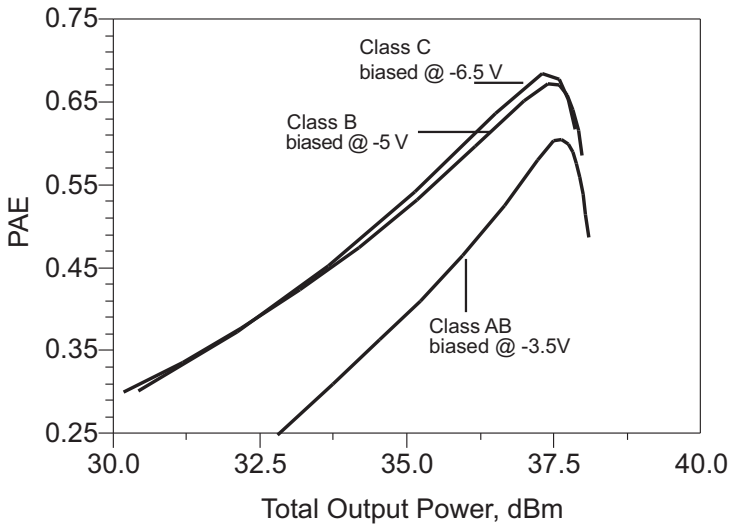

Figure 2.30: Comparison of single tone PAE vs. Output Power for class AB,B,C

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figuration. Single-ended operation with an octave band-pass filter is, once again, equivalent to push-pull. The bias design done in the previous section still holds for common-drain configuration. Common-drain , however, has smaller MSG than the common-source and common-gate configurations due to the excessive series-series feedback. Reduction in the power gain results in degraded efficiency when the transistor operating frequency is a significant fraction of the transistor cut-off frequencies f_τ and f_{max}. When the amplifier's distortion is very low, second-order effects due to nonlinear input capacitance dominate the linearity analysis.

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3
Common Source Class B

GaN HEMT device modeling, GaN MMIC process and technology and common-source class B circuit results are presented in this chapter. Advantages and limitations of common-drain class B based on the simulations performed are discussed.

3.1 GaN HEMT Modeling

This section starts with a framework to extract various bias dependent transistor parasitics using measured small-signal S-parameters. First-generation GaN HEMTs are modeled using the Agilent ADS JFET library model. The I_d vs. V_{gs} characteristics of these JFET models exhibit square-law characteristics. GaN HEMT I_d vs. V_{gs} characteristics are significantly different from square-law characteristics. Hence, for next phase of device simulations, the Walter Curtice model is used [1]. The

Curtice model employs a cubic polynomial to model the I_d vs. V_{gs} characteristics above threshold. It also provides a means to model the C_{gs} vs. V_{gs} characteristics of typical GaN HEMTs. This model is effective in explaining the measured IM_3 performance of a class B HEMT amplifier. To optimise the amplifier for superior linearity characteristics, accurate modeling of various transistor parasitics is crucial. A custom-made GaN HEMT model is developed using equation-based nonlinear elements available in ADS. Using simple programming instructions, it is possible to define device transfer characteristics to an arbitrary complexity based on device measurements. C_{gs} vs. V_{gs} can also be modeled using user-defined charge equations of arbitrary complexity. Based on the S-parameter extractions, the output conductance is observed to be drain bias dependent. This artefact could be modeled using a drain bias dependent threshold shift which is normal for GaN HEMTs. The equation based model creates an ideal platform for superior device models to optimise power amplifiers for improved linearity in GaN HEMT technology.

3.1.1 Device Parameter Extraction Procedure

S-parameters are measured using a network analyser. Y-parameters readily describe transistor hybrid-π model parasitics. Note that modeling guidelines given

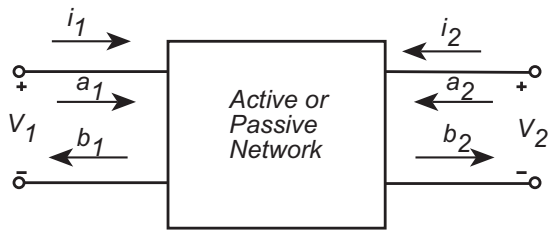

Figure 3.1: Two Port Parameters

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below could be applied to both HEMTs and HBTs. For a two-port network shown in Fig. 3.1, S-parameters are given by

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{3.1.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{3.1.2}$$

By definition, Y-parameters are given by

$$i_1 = Y_{11}v_1 + Y_{12}v_2 \tag{3.1.3}$$

$$i_2 = Y_{21}v_1 + Y_{22}v_2 \tag{3.1.4}$$

By definition, Z-parameters are given by

$$v_1 = Z_{11}i_1 + Z_{12}i_2 \tag{3.1.5}$$

$$v_2 = Z_{21}i_1 + Z_{22}i_2 \tag{3.1.6}$$

S-parameters are converted into Y-parameters using the following equations.

$$Y = [I - S]^{-1}[I + S] \tag{3.1.7}$$

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{D} \tag{3.1.8}$$

$$Y_{12} = -2\frac{S_{12}}{D} \tag{3.1.9}$$

$$Y_{21} = -2\frac{S_{21}}{D} \tag{3.1.10}$$

$$Y_{22} = \frac{(1 - S_{22})(1 + S_{11}) + S_{12}S_{21}}{D}, \tag{3.1.11}$$

$$\text{where } D = (1 + S_{11})(1 + S_{22}) - S_{12}S_{21} \tag{3.1.12}$$

Agilent ADS employs above equations to convert the measured S-parameter data into Y-parameters. These Y-parameters need to fitted to the device model shown in Fig. 3.2.

Extrinsic layout parasitics C_{pgs}, C_{pgd}, C_{pds}, L_g, L_d, L_s need to be calibrated out using open and short structures. The open structure is obtained by etching the active region between the source and the drain contacts. The short structure is realised by short-circuiting the drain,gate and source contacts.

First, the open structure Y-parameters are measured. Open structure equivalent circuit is given in Fig. 3.3. Layout capacitances are obtained as

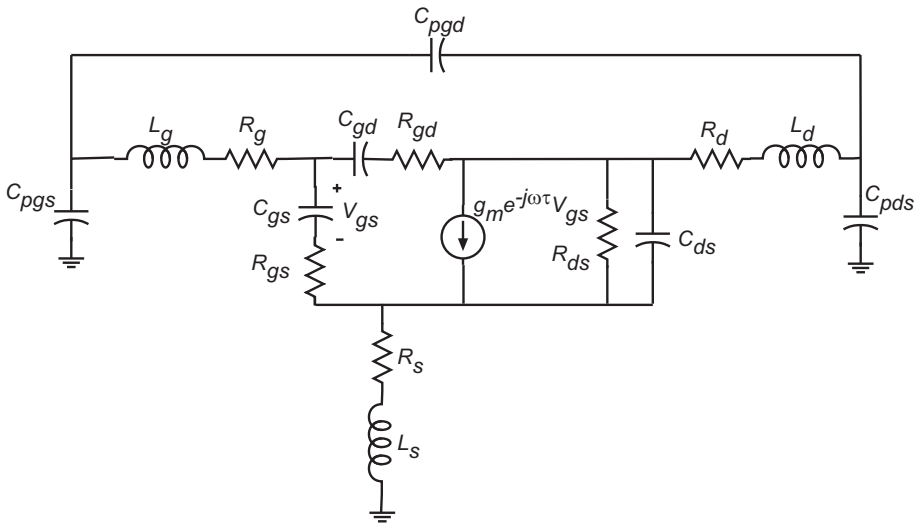

Figure 3.2: Small-signal GaN HEMT Model

$$C_{pgd} = -\Im(Y_{12})/\omega \tag{3.1.13}$$

$$C_{pgs} = \Im(Y_{11})/\omega - C_{pgd} \tag{3.1.14}$$

$$C_{pds} = \Im(Y_{22})/\omega - C_{pgd} \tag{3.1.15}$$

The layout capacitances are deembedded from the measured S-parameters by taking the S-parameters and adding negative capacitive elements as shown in Fig. 3.4. Once the capacitors are deembedded the short structure equivalent circuit is as shown in Fig. 3.5. This structure is best modeled by Z-parameters. The layout parasitic

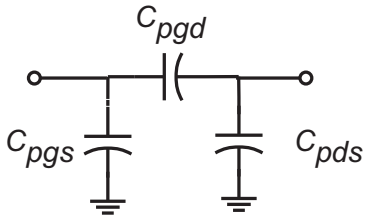

Figure 3.3: Open structure equivalent circuit

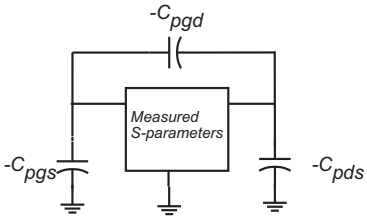

Figure 3.4: Deemdebbing layout capacitances

inductances are given by

$$L_s = \Im(Z_{12})/\omega \tag{3.1.16}$$

$$L_g = \Im(Z_{11})/\omega - L_s \tag{3.1.17}$$

$$L_d = \Im(Z_{22})/\omega - L_s \tag{3.1.18}$$

Once the layout capacitances and the inductors are deembedded, the intrinsic device parameters are obtained from the following equations [2, 3, 4, 5, 6, 7, 8]. R_g is

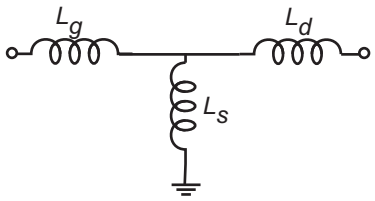

Figure 3.5: Equivalent circuit of the deembedded short structure

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lumped into R_{gs} and the expression for R_{gs} is given below.

$$Y_{gs} = Y_{11} + Y_{12} \tag{3.1.19}$$

$$Y_{gd} = -Y_{12} \tag{3.1.20}$$

$$Y_{ds} = Y_{22} + Y_{12} \tag{3.1.21}$$

$$Y_{gm} = Y_{21} - Y_{12} \tag{3.1.22}$$

$$C_{gs} = \frac{-1}{\Im\left(\frac{1}{Y_{gs}}\right)\omega} \tag{3.1.23}$$

$$R_{gs} = \Re\left(\frac{1}{Y_{gs}}\right) \tag{3.1.24}$$

$$C_{gd} = \frac{-1}{\Im\left(\frac{1}{Y_{gd}}\right)\omega} \tag{3.1.25}$$

$$R_{gd} = \Re\left(\frac{1}{Y_{gd}}\right) \tag{3.1.26}$$

$$C_{ds} = \Im\left(\frac{Y_{ds}}{\omega}\right) \tag{3.1.27}$$

$$G_{ds} = \Re(Y_{ds}) \tag{3.1.28}$$

$$g_m = g_{mo}e^{-j\omega\tau} = Y_{gm}(1 + j\omega\tau) \tag{3.1.29}$$

$$g_{mo} = mag(Y_{gm}(1 + j\omega\tau)) \tag{3.1.30}$$

$$\tau = \frac{phase(Y_{gm}(1 + j\omega\tau))}{\omega} \tag{3.1.31}$$

3.1.2 Extracted Device Parameters

Multi-finger GaN HEMTs are employed to realise high efficiency power amplifiers. Device models are developed for GaN HEMTs of different gate widths. Gates are defined by e-beam lithography and the nominal gate length (L_g) of the fabricated GaN HEMTs is approximately 0.25 μm. The source to drain separation is approximately 3 μm. The gate contact is formed 0.7-0.9 μm from the source end. Device parameters are extracted for 600 μm and 1200 μm single gate and dual gate GaN HEMTs. The device epitaxial structure is shown in Fig. 3.6.

Fig. 3.7 shows drain current vs. V_{gs}. From Fig. 3.7, it is clear that for a multi-finger 600 μm GaN HEMT device, the pinchoff voltage shifts with drain bias. At V_{ds}=5 V, the threshold voltage obtained by extrapolating from linear region is -5.1 V. However, for V_{ds}=10, 15, 20 V, V_p is approximately -5.4, -5.7 and -6.0 V respec-

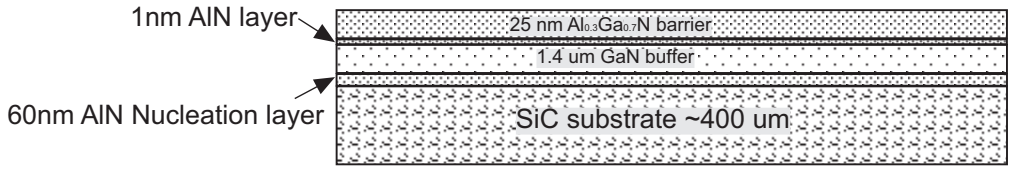

Figure 3.6: Layer structure of GaN HEMTs

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tively. Hence, the threshold shift is modeled as

$$V_p \;=\; [V_p|_{V_{ds}\,=\,5\;V}] - (0.06) \times (V_{ds} - 5) \tag{3.1.32}$$

Gain compression seen in Fig. 3.7 for $V_{ds} = 20\ V$ data is partially due to device heating. DC data should be correlated to RF data to better understand the large-signal I_d vs. V_{gs} characteristics. Note that in the discussion thus far ignored DC-RF dispersion. Assuming good passivation and ignoring DC-RF dispersion, I_d vs. V_{gs} characteristics can be reconstructed from measured microwave g_m vs. bias.

$$I_d(V_{gs}) = \int_{-\infty}^{V_{gs}} g_m(V_{gs}) \;\times\; dV_{gs} \tag{3.1.33}$$

The reconstructed drain current characteristic compared with measured DC characteristics at $V_{ds} \;=\; 20V$ is shown in Fig. 3.9. From Fig. 3.9, the pinch-off voltage is estimated as -6.1 V. This is obtained by fitting a straight line through the linear portion of the I_d vs. V_{gs} characteristics and observing its X-intercept. Above -6 V,

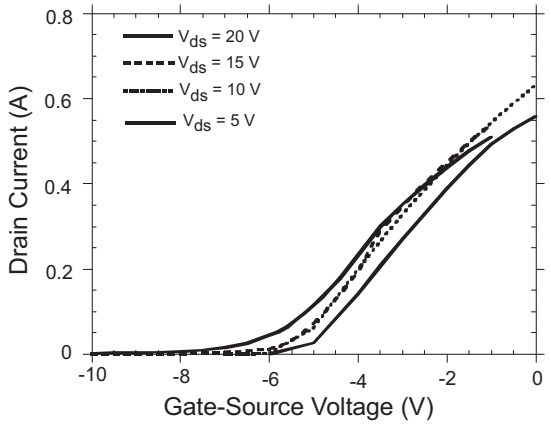

Figure 3.7: I_d vs. V_{gs} as for 600 μm device at V_{ds}=5 V, 10 V, 15 V, 20 V

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a polynomial fit model the nonlinearity above the threshold voltage. The I_d vs. V_{gs} polynomial above threshold, is given by

$$I_d = 0.0461 + 0.06(V_{gs} - V_p) + 0.038(V_{gs} - V_p)^2 + 0.0003(V_{gs} - V_p)^3 - 0.0041(V_{gs} - V_p)^4 \tag{3.1.34}$$

The output conductance, G_{ds} as a function of V_{gs} for V_{ds} = 10 V, 15 V and 20 V is shown in Fig. 3.10. G_{ds} is anti-symmetric with respect to V_{gs}. At higher V_{ds}, the curve shifts to lower V_{gs}, indicating a threshold shift [9]. For a $g_{\text{m,effective}} = \frac{I_{dss}}{V_p} = \frac{0.6\ A}{6\ V} = 0.1\ S$, the output conductance due to pinchoff shift is given by

$$G_{ds} = \frac{\partial I_d}{\partial V_{ds}} = \frac{\partial I_d}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial V_{ds}} = g_{\text{m,effective}} \times (0.06) = 0.006\ S \tag{3.1.35}$$

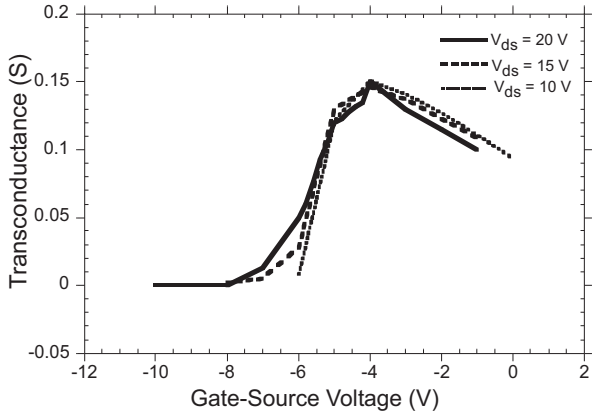

Figure 3.8: g_m vs. V_{gs} as for 600 μm device at V_{ds} = 10 V, 15 V, 20 V

The residual G_{ds} is modeled as a parallel resistance to account for $\Re(Y_{22})$. Extracted C_{gs} as a function of V_{gs} is shown in Fig. 3.11. Note that the C_{gs} vs. V_{gs} characteristics are anti-symmetric and the point of inflection does not shift with V_{ds} significantly. Above threshold the capacitance is due to the channel charge. Below threshold the capacitance is due to fringing fields and depletion capacitances. The C_{gs} vs. V_{gs} characteristic can be modeled by an anti-symmetric hyperbolic-tangent function. However, the capacitance drops by 20$\%$ at high V_{gs}. Two-tone intermodulation characteristics are influenced by the input capacitance and hence, accurate modeling is desired. Gate to drain capacitance C_{gd} vs. V_{gs} is shown in Fig. 3.12. C_{gd} increases at V_{gs} close to 0 V due to reduction in depletion width. Drain to source

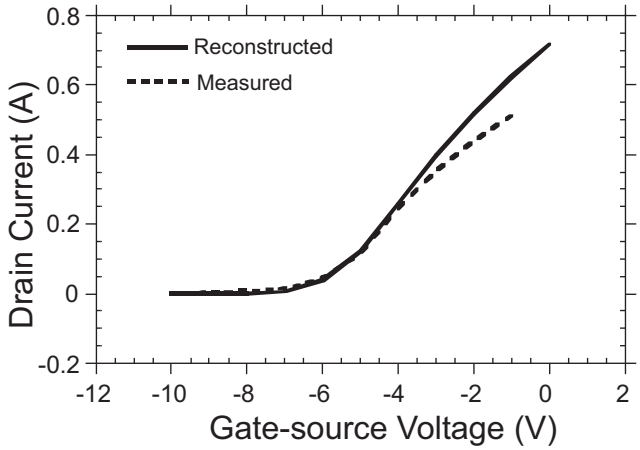

Figure 3.9: Reconstructed drain current characteristic from microwave g_m vs. V_{gs}

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capacitance, C_{ds} vs. V_{gs} is shown in Fig. 3.13. C_{ds} is also anti-symmetric with V_{gs}. Similar trends are observed in the work presented by [9].

3.1.3 Walter-Curtice GaN HEMT Model

First generation GaN HEMT models are developed using ADS JFET library model. These models exhibited Berkeley-Spice I_d vs. V_{gs} characteristics, which are quadratic characteristics. GaN HEMT common-source characteristics significantly differ from such quadratic characteristics. Hence, linearity predictions would be wrong if JFET models are used.

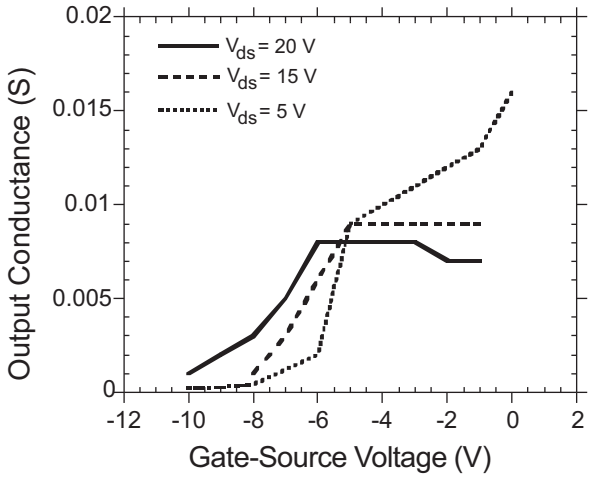

Figure 3.10: g_{ds} vs. V_{gs} as for 600 μm device at V_{ds}=10 V, 15 V and 20 V

The GaN HEMT model provided by Dr. Walter Curtice [1] employs a third-order polynomial to model the I_d vs. V_{gs} characteristics above the pinch-off voltage. It is possible to model nonlinear C_{gs} using a tangent hyperbolic function. Data fitting to the curtice-model for a 600 μm GaN HEMT is presented below.

The HEMT I_d vs. V_{gs} characteristics are defined as,

$$I_d = (a_0 + a_1(V_{gs} - V_p) + a_2(V_{gs} - V_p)^2 + a_3(V_{gs} - V_p)^3)\tanh(\gamma \mathrm{V_{ds}}) \quad (3.1.36)$$

Reconstructed I_d vs. V_{gs} characteristics shown in Fig. 3.9 and Curtice third-order polynomial fit are shown in Fig. 3.14. The two curves track each other well with little deviation. Fitting parameters for Curtice model are $a_0 = 0.7237,\ a_1 =$

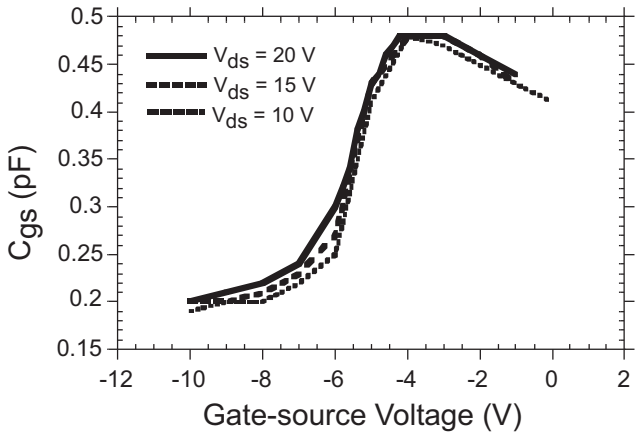

Figure 3.11: C_{gs} vs. V_{gs} as for 600 μm device at V_{ds}= 10 V, 15 V and 20 V

$0.0769,\ a_2 = -0.0201,\ a_3 = -0.0023.$

C_{gs} as a function of V_{gs} is modeled as a tangent hyperbolic function given by

$$C_{gs} = P05 + P01\ \times\ \tanh(\mathrm{P02}(\mathrm{V_{gs}} + \mathrm{P04})) \tag{3.1.37}$$

C_{gs} vs. V_{gs} characteristic of Curtice-model and the actual capacitance characteristics are compared in Fig. 3.15. Fitting parameters for C_{gs} vs. V_{gs} characteristics are P05 = 0.34 pF, P01 = 0.13 pF, P02 = 1.1, P04 = 5.7. The Curtice model ignores the C_{ds} and G_{ds} nonlinearities. G_{ds} nonlinearity is modeled using an external equation based ADS nonlinear element. The Curtice model shows an excellent agreement between the simulated and measured S-parameters in DC-40 GHz frequency

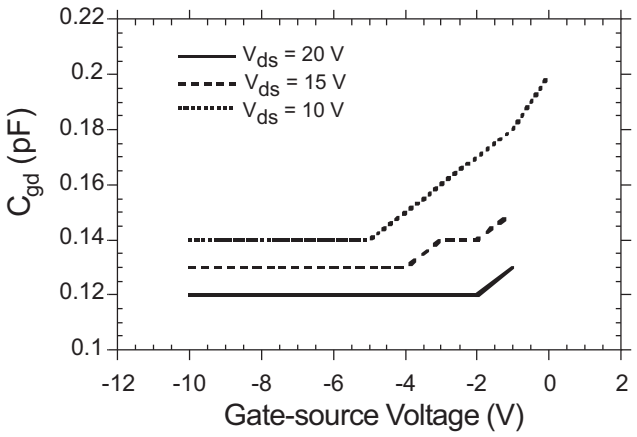

Figure 3.12: C_{gd} vs. V_{gs} as for 600 μm device at V_{ds}=10 V, 15 V and 20 V

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band. The Curtice model with the external parasitics for a 600 μm single gate GaN HEMT is shown in Fig. 3.16. This figure includes the specific parasitic capacitances and the fitting parameters for Curtice model. This model, however, does not accurately model G_{ds}, leading to a discrepancy between linearity measurements and simulations. Hence, for linearity predictions, the G_{ds} nonlinearity is neglected and a constant output resistance is used.

Modeling a dual-gate GaN HEMT is more complex as it is a three port device and only two-port S-parameters are measured using a Vector Network Analyser(VNA). However, a dual-gate GaN HEMT is equivalent to a cascode stage. The modeling

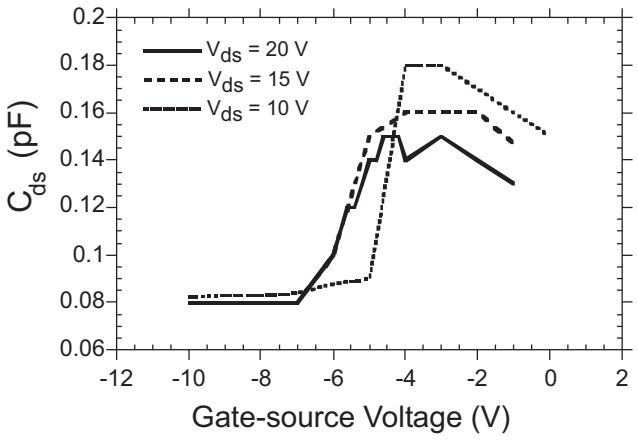

Figure 3.13: C_{ds} vs. V_{gs} as for 600 μm device at V_{ds} = 10 V, 15 V and 20 V

strategy employed is to use the developed single-gate HEMT model to create a cascode stage model. The resulting model is then adjusted to fine tune the model so that it reproduces S-parameter measurement data for the dual-gate GaN HEMTs.

3.1.4 Equation-based ADS GaN HEMT Model

The Curtice model cannot model the drain-induced threshold shift and its effect upon G_{ds}. It also does not provide the designer with flexibility to incorporate complex parasitic bias dependencies. ADS provides nonlinear equation-based elements whose characteristics can be defined as a function of V_{gs} and V_{ds} and ADS also pro-

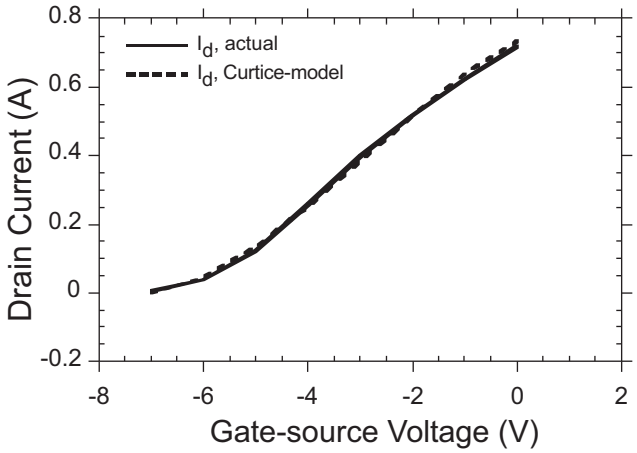

Figure 3.14: Comparison of I_d vs. V_{gs} data between Curtice fit and the reconstructed I_d data shown in Fig. 3.9 for a 600 μm device

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vides an easy way to simplify the parasitic dependencies based on simple equations so that the designer can get a fundamental insight into the problem. Drain-induced modulation of V_p can be modeled as

$$V_p = [V_p|_{V_{ds}=5\,V}] \times (1 + 0.06 \times (V_{ds} - 5)) \tag{3.1.38}$$

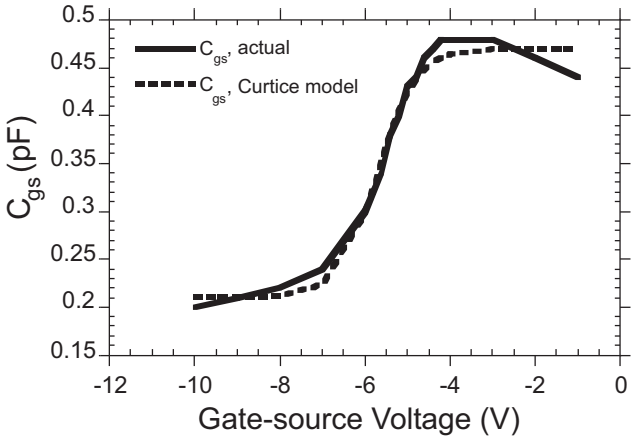

Figure 3.15: Comparison of C_{gs} vs. V_{gs} data between Curtice fit and the actual C_{gs} data for a 600 μm single gate GaN HEMT

The drain current as a function of V_{gs} and V_{ds} can be modeled by the following expressions

$$I_d = I_{d1}(V_{gs}) \tanh(\gamma V_{ds}) \quad \text{for} \quad V_{gs} > V_{th} \tag{3.1.39}$$

$$I_d = 0 \quad \text{for} \quad V_{gs} < V_{th} \tag{3.1.40}$$

$$\text{where} \;\; I_{d1}(V_{gs}) = a_0 + a_1(V_{gs} - V_p) + a_2(V_{gs} - V_p)^2 + ... \tag{3.1.41}$$

More complex equations for I_{d1} could more closely model the S-parameter measurements. In particular, the characteristics near V_{gs} = V_p are modeled with more complex expressions.

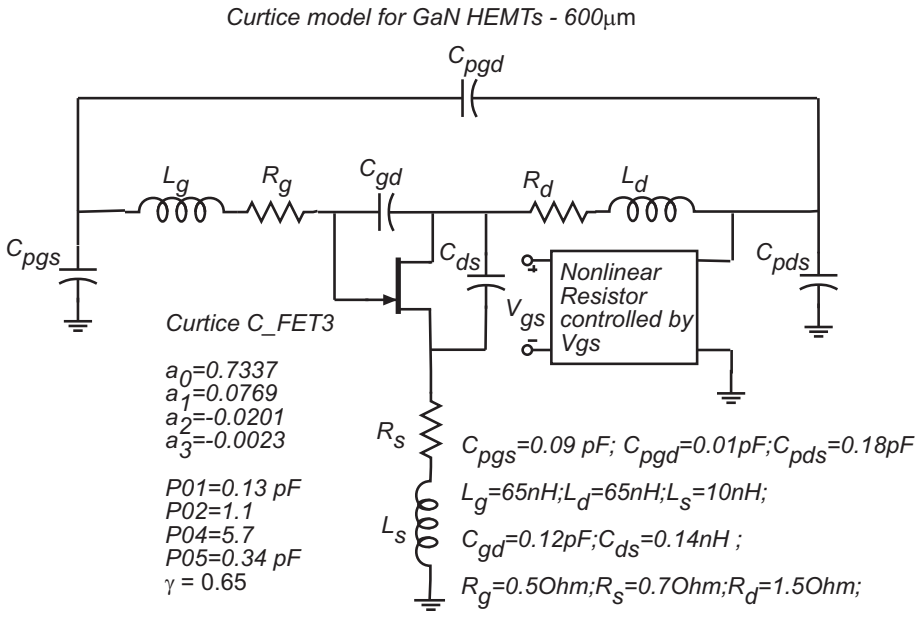

Figure 3.16: Curtice model for a 600 μm single gate GaN HEMTs

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The device input capacitance is modeled using a hyperbolic tangent expression.

$$Q(C_{gs}(V_{gs})) = q_1(V_{gs}) + q_2 ln(cosh(\alpha(V_{gs} - V_p))) \tag{3.1.42}$$

Again, more complex expressions would permit more accurate modeling. Apart from these modified functions for I_d, C_{gs} and G_{ds} the external parasitics for the ADS model are the same as for the Curtice-model. Main advantage of this custom-made model over Curtice-model is that it is possible to incorporate changes in the functional dependencies of the transistor parasitics due to process variations and

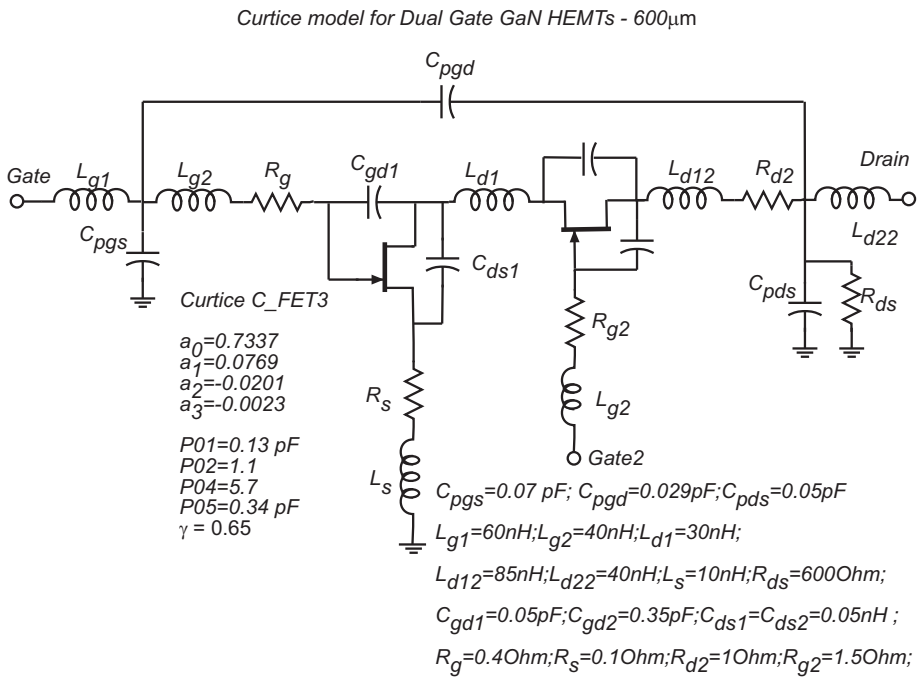

Figure 3.17: Curtice model for a 600 μm dual gate GaN HEMTs

changing device structures.

3.2 GaN MMIC Process

The Gallium Nitride material system is a leading contender for microwave wireless applications due to its superior electrical transport properties. The high electron velocity ($> 10^7 \mathrm{cm/sec}$), wide bandgap (3.4 eV) and high breakdown voltage

($> 50\ V$ for a current gain cut-off frequency f_τ of 50 GHz) of the AlGaN/GaN system result in record power densities. The high thermal conductivity (3.5 W/cm K) of SiC substrates significantly reduces device heating, leading to power density as high as 11.2 W/mm [11].

The material for the AlGaN/GaN HEMTs is grown using Metal Organic Chemical Vapor Deposition (MOCVD) on SiC substrates. SiC is used as the substrate for the MMICs due to its high thermal conductivity. Earlier work in power amplifiers in AlGaN/GaN system used HEMTs grown on sapphire substrates. These FETs were then flip-chip bonded on to an AlN substrate, a material with much higher thermal conductivity than sapphire [10].

The circuit process has ten mask steps. Gates are defined using an e-beam lithography. Features as small as 150 nm can be so defined. The remaining mask steps use an i-line optical projection lithography. The process first fabricates active devices and then passive elements. The active device process includes ohmic contact formation, mesa-isolation, gate lithography and $\mathrm{SiN_x}$ passivation. The passive element processing involves NiCr resistors, $\mathrm{SiN_x}$ capacitors and plated airbridge process.

The layer structure is shown in Fig. 3.6. GaN HEMT process involves four optical lithography mask steps and one e-beam lithography step. Ohmic contacts for

source and drain are formed by evaporating a Ti/Al/Ni/Au metal stack of thickness 20/220/55/45 nm respectively. Ti is known to form TiN upon annealing, resulting in Nitrogen deficiency in GaN, which is equivalent to n-type doping. The n+-GaN interface along with the conductive TiN forms low ohmic contacts. Ni acts as a barrier between Al and Au and stops intermixing. Au is used to improve the conductivity of the ohmic contacts. Reactive Ion Etching (RIE) using Cl_2 at 5 mT pressure, 10 sccms flow rate at 100 W RF power for 15 sec is used to damage the ohmic contact region prior to metal evaporation. A 10$\%$ HCl solution is used to clean the surface of the semiconductor before ohmic contact evaporation.

The next process step involves creating an e-beam detectable alignment mark in order to align gate Schottky contacts to the source and drain ohmic contacts. Ideally, the e-beam alignment marks should be a part of the ohmic contact mask, so that the net alignment error between ohmics and gate is minimized. After the ohmic contact anneal at 870 degrees Celsius, however, the e-beam alignment marks are partially melted and are undetectable by an electron-beam. In avoid this problem, a new mask step is added to the process. An e-beam alignment mark shown in Fig. 3.18, is formed along with ohmic contacts. A 3.0 μm photoresist AZ 4330 is used to mask all the regions except where the e-beam alignment mark needs to be there after the

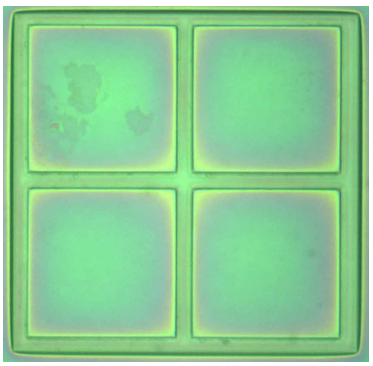

Figure 3.18: E-beam alignment mark

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ohmic contact lift-off. Reactive Ion Etching with Cl_2 at 5 mT pressure, 10 sccm flow rate at 100 W RF power for 10 min is used to etch approximately 5000-6000 Å, creating trenches defined by the photoresist (AZ 4330) and e-beam alignment mark metal. E-beam alignment metal marks are stripped by wet-etching Au, Ni, Al, Ti in that order. E-beam alignment marks (Fig. 3.18) formed this way are not going to be partially melted during the high temperature anneal. The wafer is then annealed at 870 degrees Celsius for 30 sec in a Rapid Thermal Annealer (RTA). The temperature of the RTA should be carefully calibrated to accurately apply the required temperature to the wafer to obtain low ohmic contact resistance.

Device mesa-isolation trenches are then formed by Reactive-ion-etching Al-

GaN/GaN using Cl_2 gas in an RIE system. A 1.8 μm thick SPR 518A photoresist masks the active regions. Cl_2 at 5 mT pressure, 10 sccm flow rate at 100 W RF power for 2 min etches approximately 1000 Å. This ensures device isolation. Best obtained ohmic contact resistance is 0.5-0.6 Ω-mm.

The next step is the gate Schottky contacts deposition. A JEOL e-beam writer defines the gate contacts. A bi-layer process is developed to obtain features that could be as small as 0.15 μm in size. Earlier work at UCSB used a tri-layer e-beam resist process to write T-gates. The top resist creates a lift off profile to facilitate good lift-off. This trilayer process, however, yields T-gates that have a narrow T-top shape increasing the gate access resistance reducing transistor f_{max}. The bi-layer process is less complex and produces a T-top without narrowing. A 950K e-beam resist is the bottom layer while a co-polymer MMA is the top layer. The bottom layer is approximately 150 nm thick and the top MMA layer is approximately 350 nm thick. A thin Al layer ($\sim$10 nm) is thermally evaporated on top of the e-beam resist so that the wafer is not electrically charged during the alignment, focus and exposure. After the exposure, the Al layer is stripped by a 25% developer (AZ 400K) solution, and the e-beam resist is then developed in a Methyl Iso-butyl Ketone (MIBK) solution. An oxygen descum is performed at 300 mT, 100 W for 7-10 sec; this step is a critical

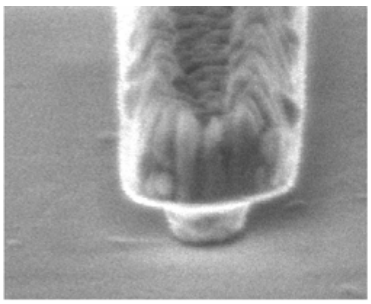

Figure 3.19: T-gate (0.25μm)

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in determining yield. After a 10$\%$ HCl surface treatment, a Ni/Au metal stack of thickness 30/300 nm is evaporated (Fig. 3.19, Fig. 3.20).

After the gate contacts, Ti/SiO_2/NiCr (30/300/480 Å) resistors are evaporated. The sheet resistance is a function of the quality and age of the NiCr source. Measured sheet resistance is approximately 40Ω/square. Later in the process the resistors are covered with SiN_x to prevent the oxidation of NiCr, which would cause degradation of in the sheet resistance of NiCr resistors with time. The first layer of contact metal Ti/Au/Ti (200/10,000/100 Å) is e-beam evaporated and lifted off. This metal layer contacts gate, source and drain terminals of the transistor and the rest of the circuit passive elements. This metal layer also forms the coplanar waveguide transmission lines and forms one plate of the SiN_x capacitors.

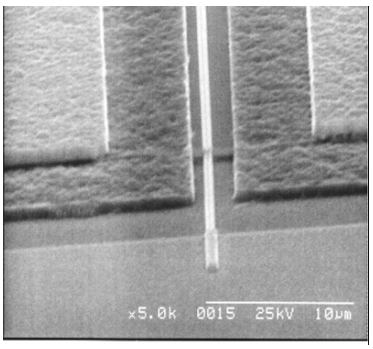

Figure 3.20: GaN HEMT device before passivation

Unpassivated GaN HEMTs suffer from DC-RF dispersion. This term refers to the difference between DC and the high frequency transconductance due to surface states between the gate and the drain. SiN_x removes these surface states and hence improves RF large-signal transconductance. Success in passivation is sensitive to the quality of the SiN deposited. A Plasma Enhanced Chemical Vapor Deposition (PECVD) deposited SiN_x passivates the GaN surface. SPR 518A optical photoresist masks the active region during the SiN_x etch. Silicon Nitride is etched using CF_4 at 150 mT, 100 W RF power for 2 min. Another layer of PECVD SiN of 400 nm thickness is then deposited to act as the dielectric of the metal-insulator-metal capacitors. Thin film SiN is again masked using SPR 518A photoresist and is etched using Oxygen at 50 mT presure, 20 sccm flow rate, 500 V RF bias for 5 min in an

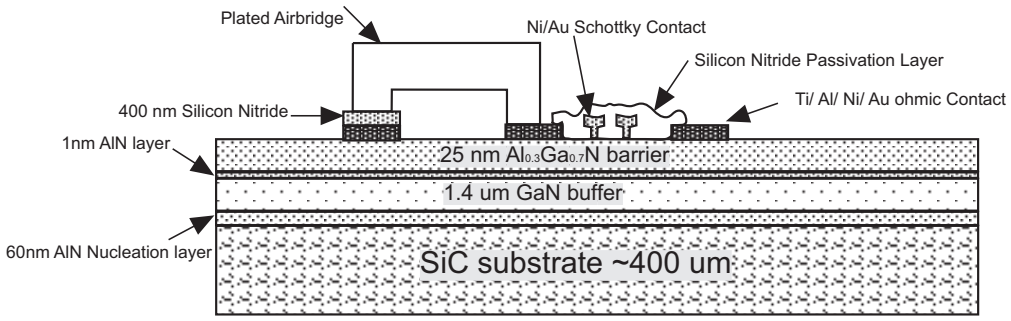

Figure 3.21: GaN MMIC cross-section

RIE system. The capacitance is approximately 0.13 fF/μm^2.

The next process step is fabrication of airbridges. These bridge the coplanar waveguide ground planes to suppress slot-line modes. Airbridges also connect source contacts to the ground plane in multi-finger transistor layouts. The plated airbridges are fabricated using a two mask process. The first layer of photoresist (AZ 4330) is patterned and opened at the bases of the airbridges. The resist is then reflowed at 120 degrees Celsius. This forms a smooth resist edge profile so that the subsequent sputtered Ti/Au/Ti film forms a continuous layer. The second layer of photoresist is patterned to define the top layer of the bridge and gold is plated. Plating is stopped when the total plating thickness is approximately 3 μm. The flash layer and the top and bottom layer resists are removed to obtain an airbridge with approximately 3

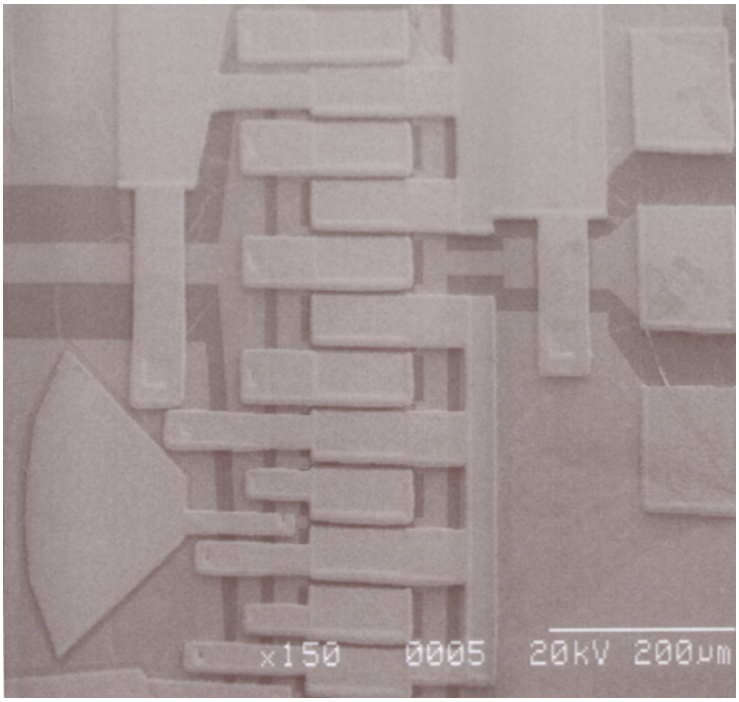

Figure 3.22: Multi-finger dual-gate GaN HEMT

μm air height and 3 μm thickness. A process cross-section is shown in Fig. 3.21. A completed dual-gate multi-finger device and a single-gate multi-finger device are shown in Fig. 3.22, Fig. 3.23 respectively.

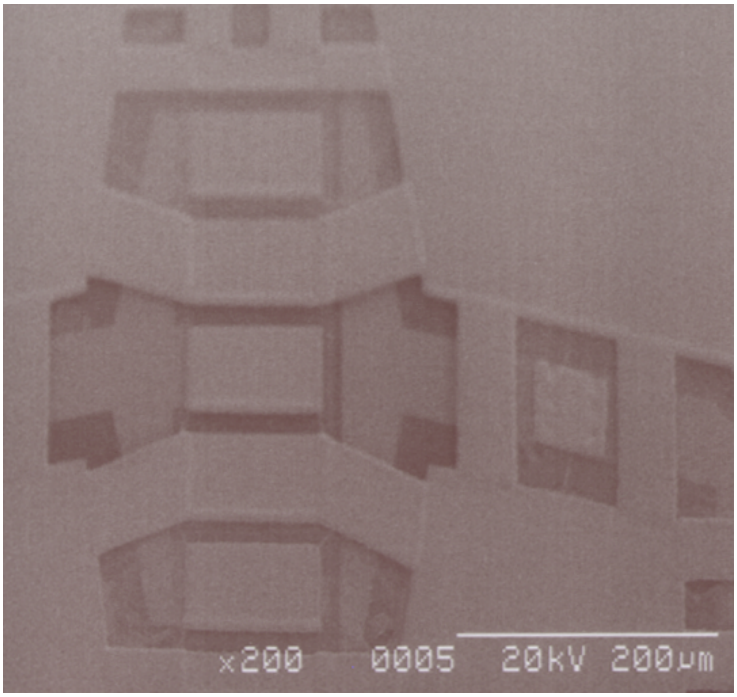

Figure 3.23: Multi-finger single-gate GaN HEMT

3.3 Device Performance

During the course of this work, several process runs have been performed on both Sapphire and SiC substrates. In this section, GaN HEMT DC characteristics and microwave performance are presented.

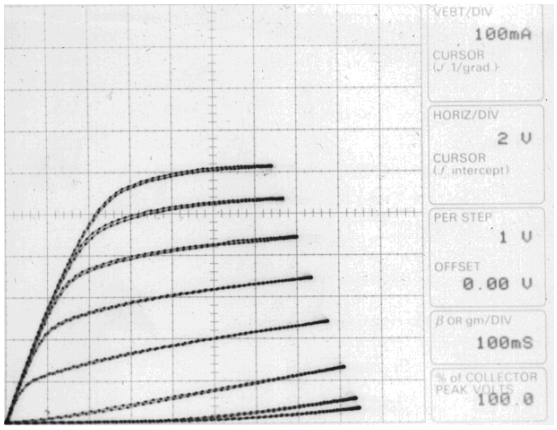

Figure 3.24: I_d vs. V_{ds} characteristics of a 600 μm wide single-gate GaN HEMT

3.3.1 DC Performance

The saturation current, I_{dss} of both the single and dual gate GaN HEMTs is approximately 1 A/mm (Fig. 3.24, Fig. 3.25). Fig. 3.24 shows the DC common-source characteristics and common-source curves with V_{gs} pulsed at 80 μsec. There is minimal difference between the DC common-source curves and the pulsed common-source characteristics. The breakdown voltage, V_{br} of a single gate device is $>$35 V and the breakdown voltage of a dual-gate multi-finger transistor is $>$55 V (Fig. 3.26).

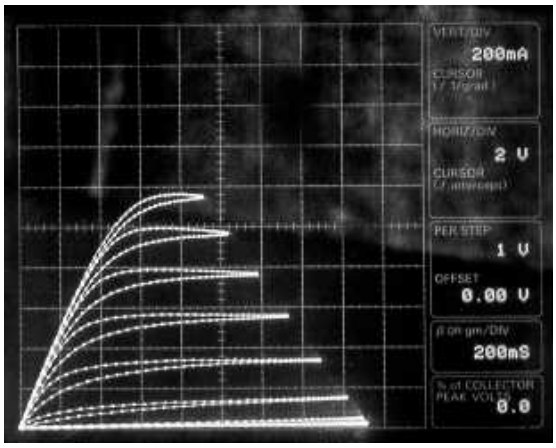

Figure 3.25: I_d vs. V_{ds} characteristics of a 1.2 mm wide dual-gate GaN HEMT

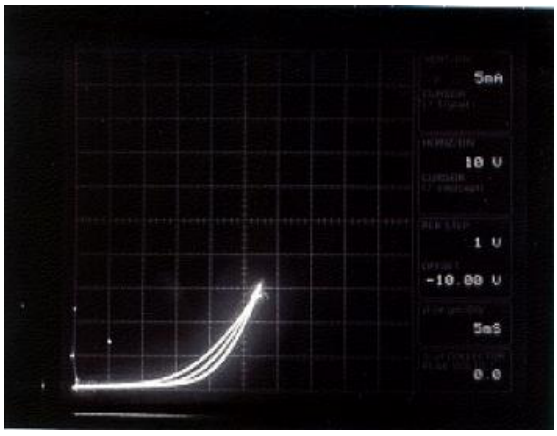

Figure 3.26: Breakdown voltage of a 1.2 mm dual-gate GaN HEMT

3.3.2 Microwave Performance

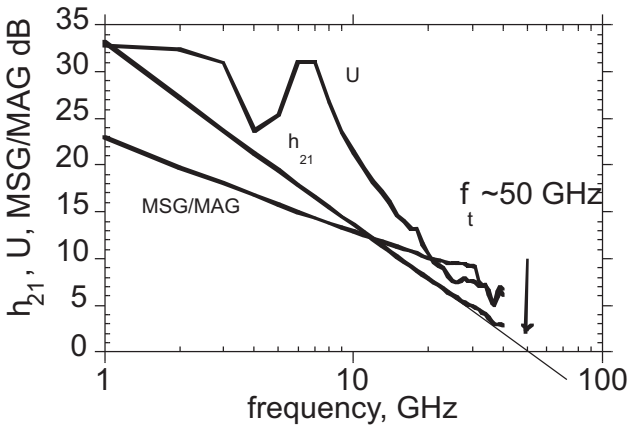

Figure 3.27: H_{21}, MSG/MAG and U of a 150 μm width single-gate GaN HEMT. The gate length is 0.25 μm

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The S-parameter measurements are calibrated based on an off-wafer SOLT (Short open Load through) calibration. Small-signal S-parameters are extrapolated to estimate f_τ and f_{max} of the devices. The short circuit current gain (h_{21}), MSG/MAG, unilateral power gain, U of a 150 μm wide single-gate GaN HEMT measured at V_{gs} =3 V, V_{ds} = 15 V and I_d = 91 mA are shown in Fig. 3.27. This device exhibited 50 GHz f_τ. This single-gate GaN HEMT exhibited 13-dB maximum stable gain (MSG) at 10 GHz and 10-dB at 20 GHz (Fig. 3.27). Short circuit current gain, MSG/MAG

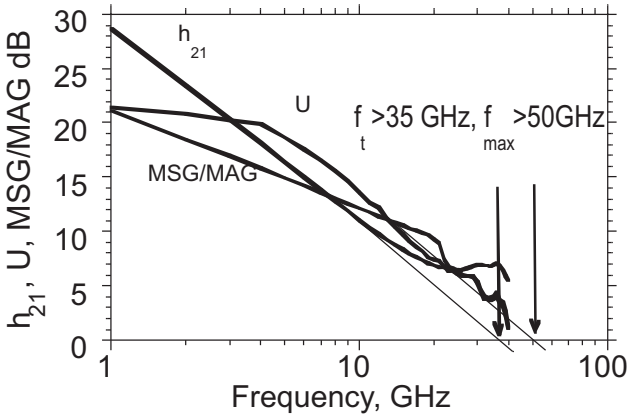

Figure 3.28: H_{21}, MSG/MAG and U of a 600 μm width single-gate GaN HEMT

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and unilateral power gain of a 600 μm wide multi-finger single gate GaN HEMT measured at V_{gs} = 3.5 V and V_{ds} = 15 V are shown in Fig. 3.28. This device exhibited f_τ >35 GHz, f_{max} >50 GHz. Degradation in f_τ is due to the layout parasitics of a multi-finger device and the increased gate to source separation aimed at improving e-beam gate yield. The MSG/MAG of a dual-gate multi-finger GaN HEMT with 600μm gate periphery is biased at V_{gs} = 4 V, V_{ds} = 20 V and the second gate is biased at 4 V is shown in Fig. 3.29. The maximum stable gain of this device at 10 GHz is more than 20 dB.

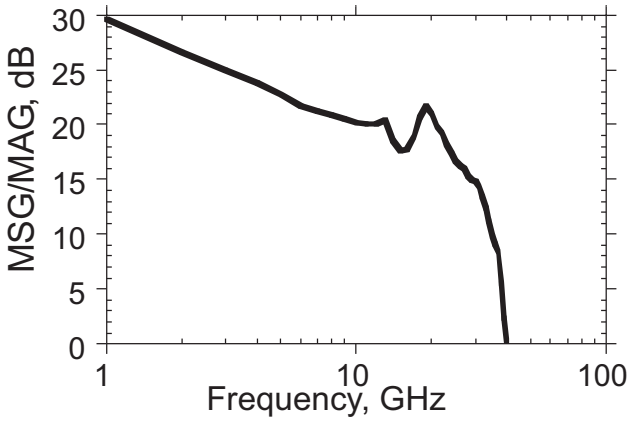

Figure 3.29: MSG/MAG of a 600 μm dual-gate GaN HEMT

3.4 Single-ended Common-source Class B Design

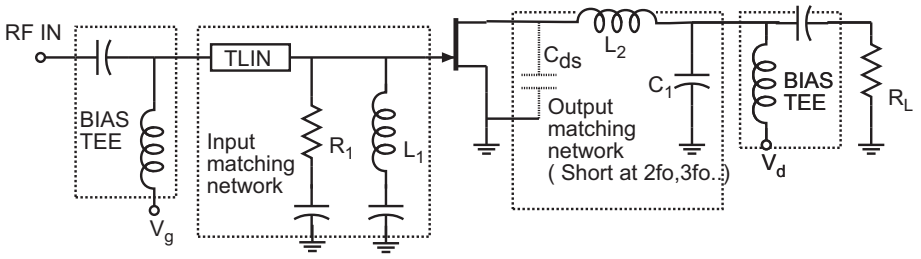

Figure 3.30: Circuit Schematic of a common-source class B power amplifier

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The circuit schematic is shown in Fig. 3.30. The input is matched at 10 GHz, and the output is tuned to present a low impedance for the harmonic frequencies. The Curtice model is used to perform the simulations at this section. The drain-source capacitance C_{ds} is absorbed into the output Π-section for high bandwidth and for optimum load-line matching. PAE simulations are shown in Fig. 3.31. The circuit, using a GaN HEMT with 1.2 mm channel width, produced in simulations 48$\%$ of saturated PAE with 36 dBm of output power at 10 GHz. Two-tone simulation ($2f_1 - f_2$) predicts 40-dBc IM_3 suppression when the total output power is 3dB below the 1-dB compression point. The bias has been varied from class C bias to class A, and simulated IM_3 performance at 6-dB backoff from $P_{1-\mathrm{dB}}$ together

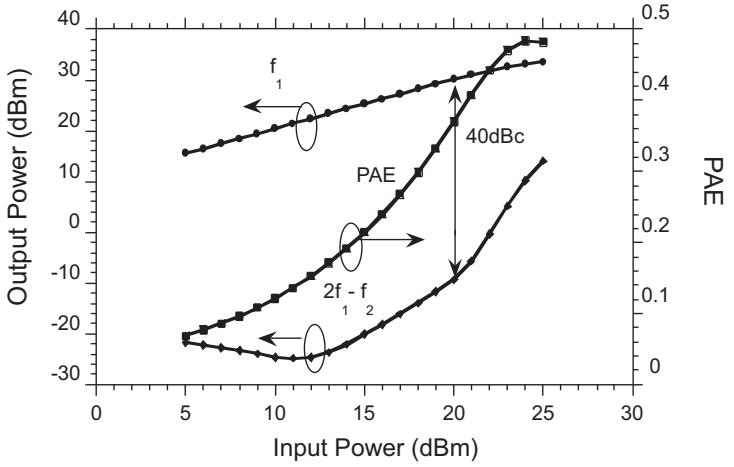

Figure 3.31: Simulated Output Power and PAE vs. input power for the common-source class B

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with maximum one-tone PAE are plotted in Fig. 3.32. From these simulations, it can be inferred that class B bias achieves better efficiency and linearity than class AB or class C. The distortion degrades very rapidly as gate bias is varied from V_p (class B bias) confirming the theoretical predictions. At lower frequencies, the linearity is improved and follows the same trend (Fig. 3.33) with bias. Simulated IM_3 performance degradation at higher frequencies is due to capacitive nonlinearities.

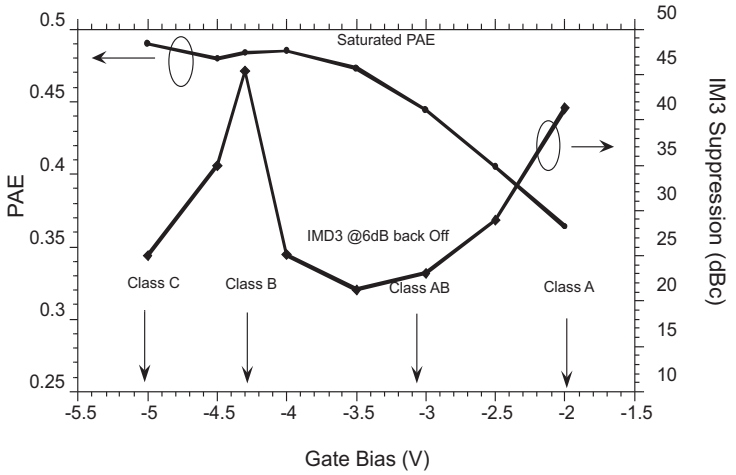

Figure 3.32: Simulated Single-tone PAE and IM_3 suppression vs. bias point for the common-source class B

3.5 Common-source Class B Results

The MMIC class B power amplifier is fabricated on a SiC substrate in GaN HEMT technology (Fig. 3.34). The 1.2 mm dual gate GaN HEMT has 1 A/mm I_{dss} and $>$55 V V_{br}. The measured f_τ for the 0.25 μm L_g device is approximately 40 GHz. Fabricated devices have V_p =-5.1 V.

Input and output tuning networks are on chip. Bias feeds for gate 1, gate 2 and drain were provided through off-wafer Bias Tees for convenience. The circuit is tested with four different gate bias conditions: -3.1 V for class A, -4 V for class AB, -5.1 V for class B and -5.5 V for class C, respectively. Single tone and two-

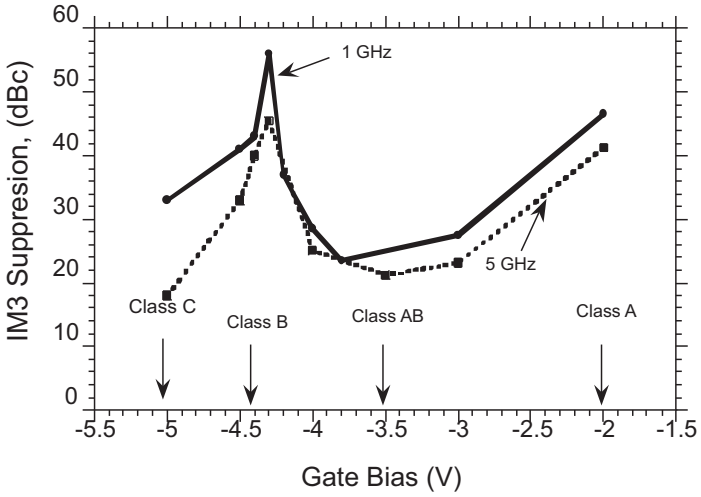

Figure 3.33: Simulated IM_3 suppression at 1 GHz, 5 GHz vs. bias point for the common-source class B

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tone measurements were performed. The 3rd order output powers, $2f_1 - f_2$ and $2f_2 - f_1$, are measured with two input signals at $f_1 = 8\ GHz$, and $f_2 = 8.001\ GHz$. The power and IM_3 suppression measurement setup is shown in Fig. 3.35. Two separate signal generators at f_1, f_2 are summed using a waveguide power combiner. Input power at this point is sensed using a waveguide directional coupler and is measured using a power sensor and a power meter. Output power is also sensed using a waveguide directional coupler and measured with a power meter. A spectrum analyser monitors the output spectrum.

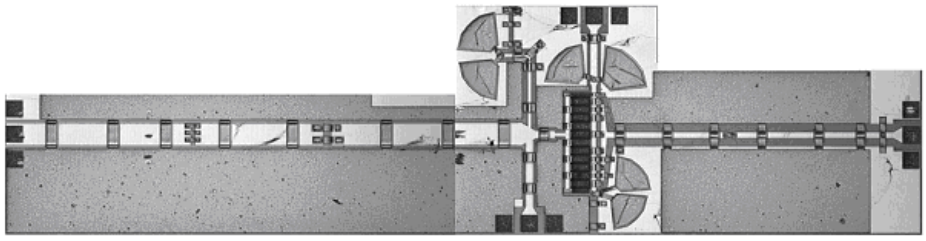

Figure 3.34: Chip photograph of the common-source class B amplifier

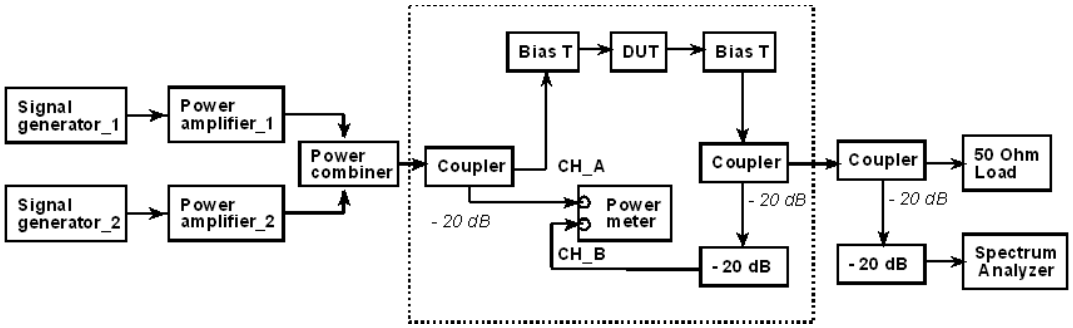

Figure 3.35: Measurement setup for power and IM_3 suppression

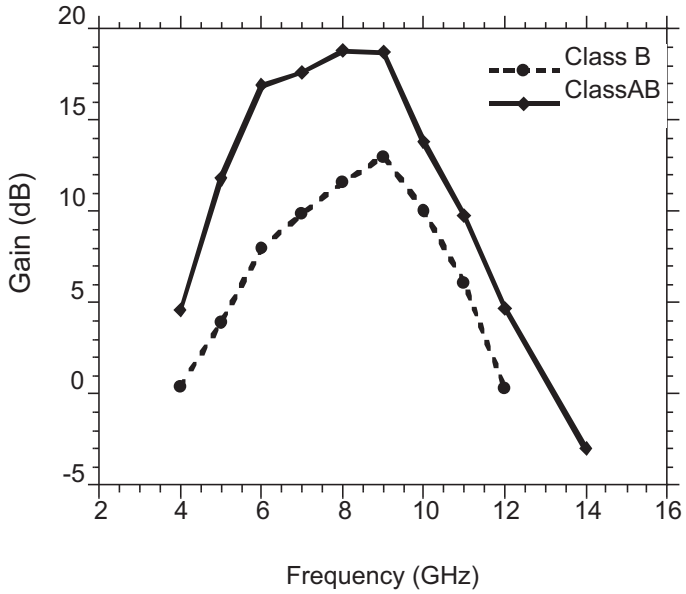

Figure 3.36: Measured power gain vs. frequency for the class B amplifier

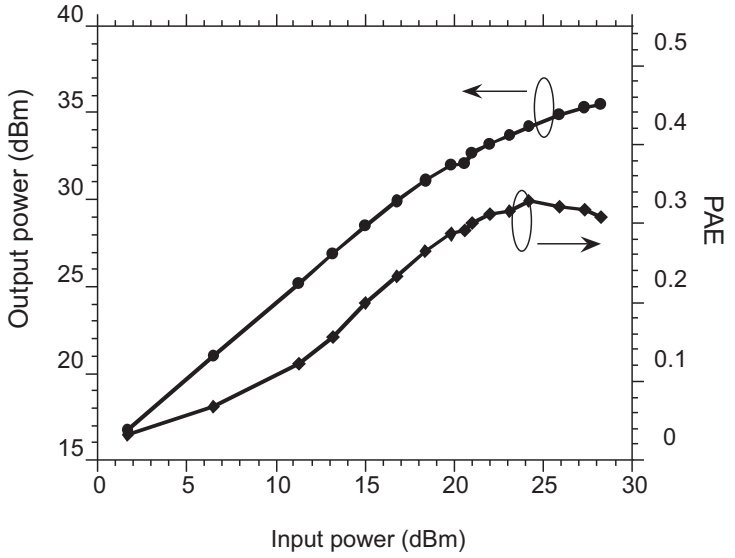

Figure 3.37: Measured single-tone output power and PAE for the common-source amplifier under class B bias

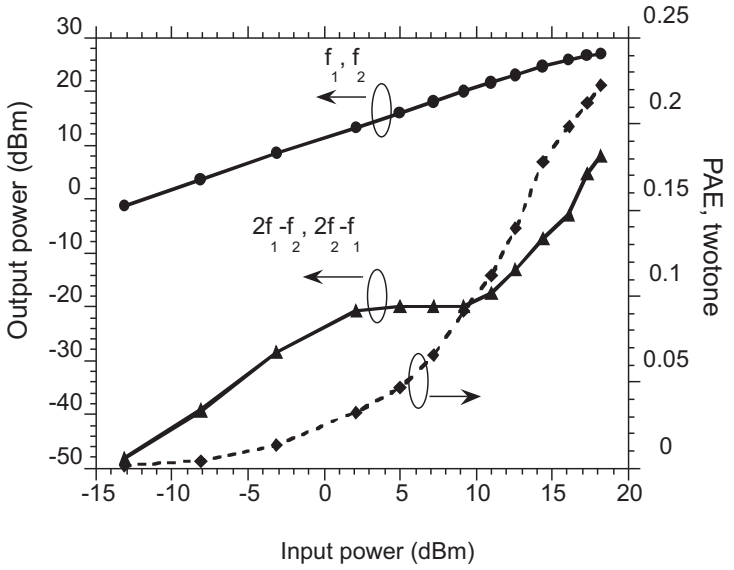

Figure 3.38: Class B bias common-source power amplifier two-tone output power and IM_3 suppression; measured data

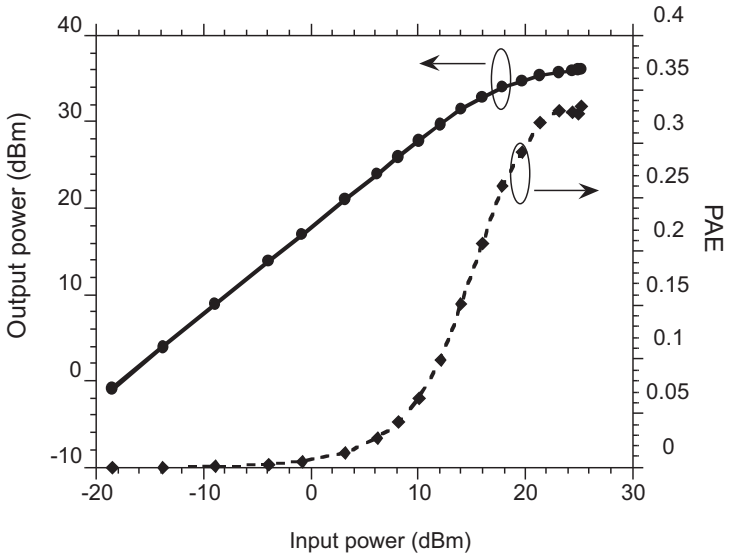

Figure 3.39: Class A bias power amplifier single-tone output power and PAE; measured data

The circuit under class B bias exhibits 13-dB gain at 8 GHz with a 7-10 GHz 3-dB bandwidth as shown in Fig. 3.36. Gain under class AB or A bias was approximately 6-dB greater than in class B, as is expected. 36-dBm saturated output power and 34% of maximum PAE are obtained under class B bias for single-tone operation(Fig. 3.37), under class B biasing high IM_3 suppression is obtained over a wide output power range for two-tone input signals (Fig. 3.38). Note that the IM_3 amplitude does not vary in proportion to the cube of the input power, because the circuit transfer characteristics are not well modeled by a cubic polynomial and fifth-order coefficients also produce spurious frequency content at ($2f_1$-f_2). Device models provide only an approximate fit to the device characteristics and hence the discrepancy between simulations (Fig. 3.32) and measurement (Fig. 3.38). Under class A bias, shown in Fig. 3.39 and Fig. 3.40, the measured IM_3 output power increases rapidly with the input power making IM_3 suppression very poor at high output power levels.

Comparison of the PAE and IM_3 suppression vs. output power for class A and class B are shown in Fig. 3.41 and Fig. 3.42 respectively. At low output power levels, class A has very low distortion (IM_3 suppression $>$50 dBc), while IM_3 suppression of class B also maintains a $>$35 dBc level. At high power levels, however, class B and class A have similar IM_3 suppression, but class B provides 10% improved

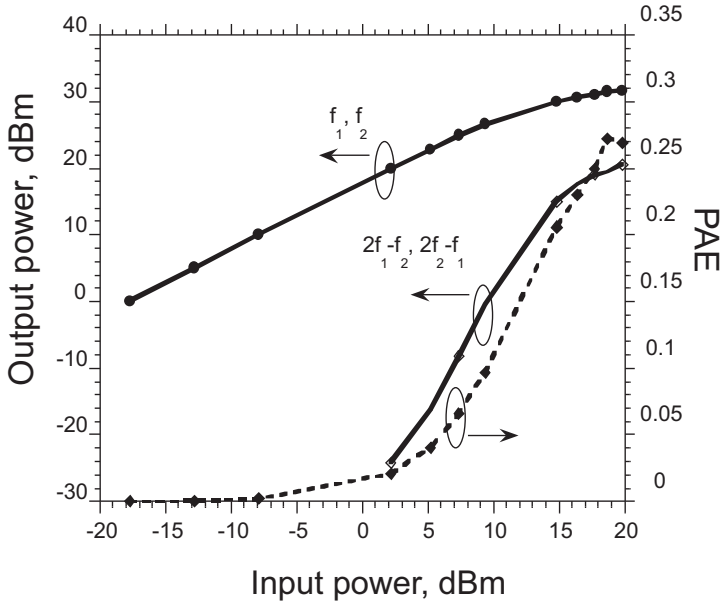

Figure 3.40: Class A bias power amplifier two-tone output power and IM_3 suppression; measured data

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PAE, as can be seen in Fig. 3.42. The IM_3 performance vs. output power for classes A, AB, B and C are compared in Fig. 3.43. Class AB and class C have higher intermodulation distortion when compared to classes A and B.

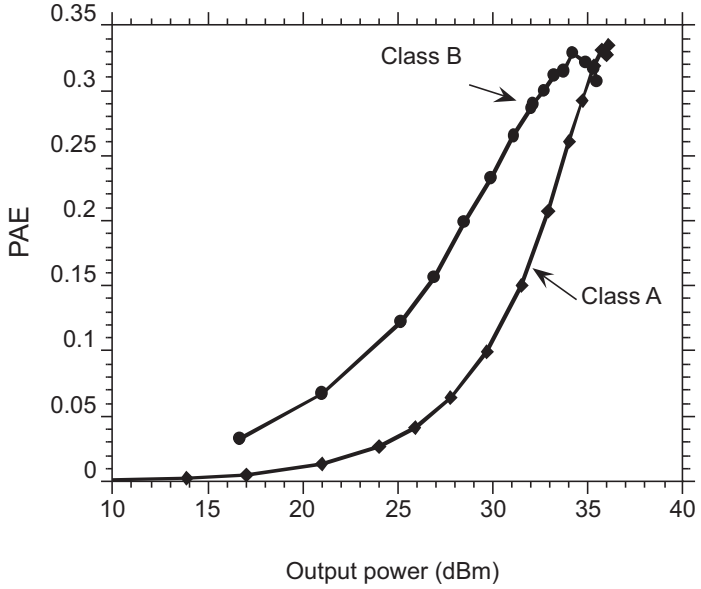

Figure 3.41: Summary of comparison between class B and class A - Single tone PAE; measured data

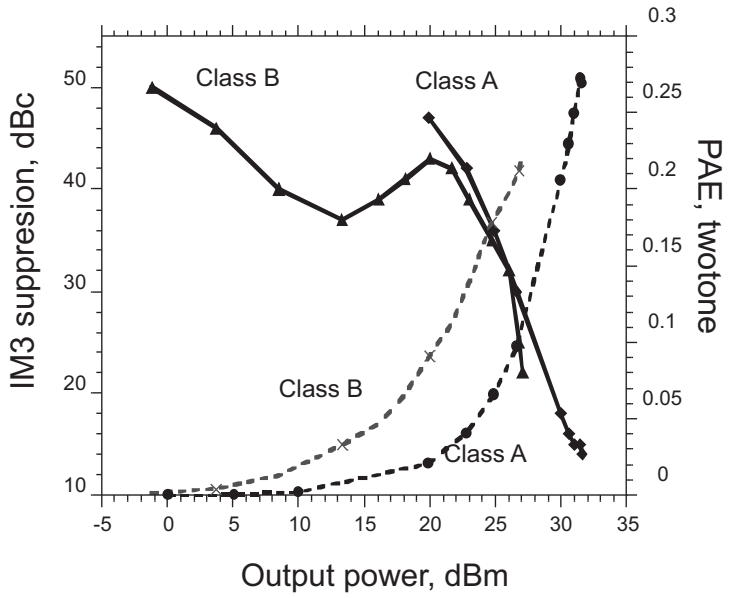

Figure 3.42: Summary of comparison between class B and class A - Two-tone PAE and IM_3 suppression; measured data

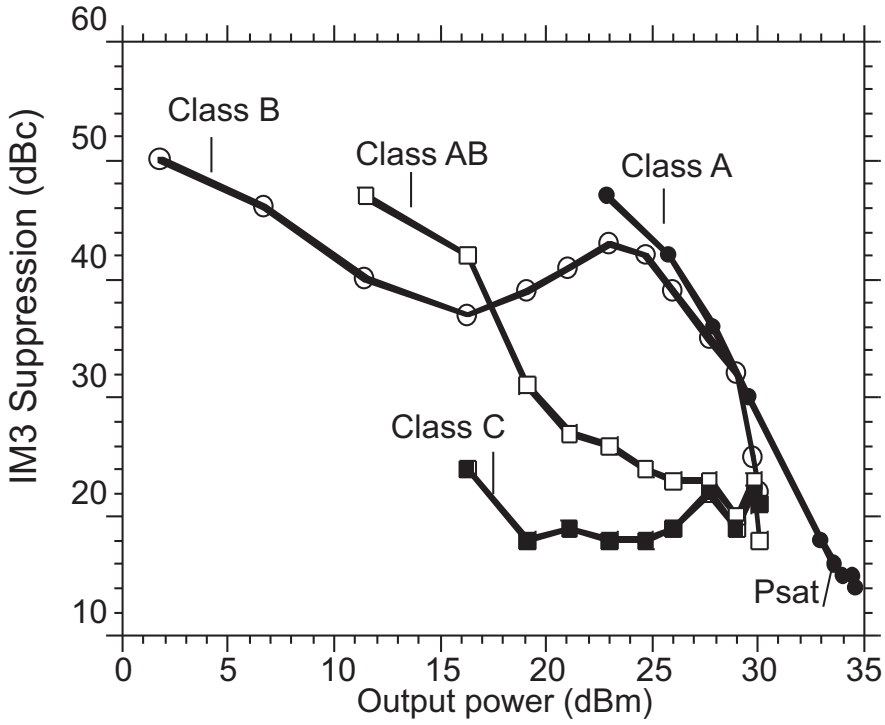

Figure 3.43: IM_3 suppressions for all bias conditions as a function of output power for the common-source amplifier; measured data

3.6 Common-drain Class B Design

The circuit diagram of a common-drain class B amplifier is shown in Fig. 3.47. The common-drain topology has low maximum stable gain because of strong feedback through C_{gs}. This can be understood through the following expression.

$$MSG = \frac{|Y_{21}|}{|Y_{12}|} \sim \frac{g_m}{\omega C_{gs}} \tag{3.6.1}$$

The multi-finger common-drain device layout similar to that of a common-source transistor. A lossy input-matching network is required to ensure stability. A band-pass LC tank circuit at the output short circuits the signal harmonics. The IC layout is shown in Fig. 3.48. This amplifier is designed at 5 GHz operation instead of 10 GHz due to the low maximum stable gain at 10 GHz.

These ICs were designed, but no ICs were successfully fabricated, due to low yield on the associated process run. The PAE simulations are shown in Fig. 3.44. In simulations, the circuit produces 36 dBm saturated output power with a maximum PAE of 37$\%$ at 5 GHz. In simulations, the circuit exhibited IM_3 suppression $\geq$42 dBc at output power levels below 2 W, when biased at class B (Fig. 3.45). In simulation, the bias was varied from class C to class A, and the IMD performance of the common-drain design is compared to that of an equivalent common-source

design. The simulated results are plotted in Fig. 3.46. The IM_3 improvement should be approximately $(1 + g_m \times R_L)^2 = 10$-dB. This improvement is observed under all bias conidtions ranging from class C to class A.

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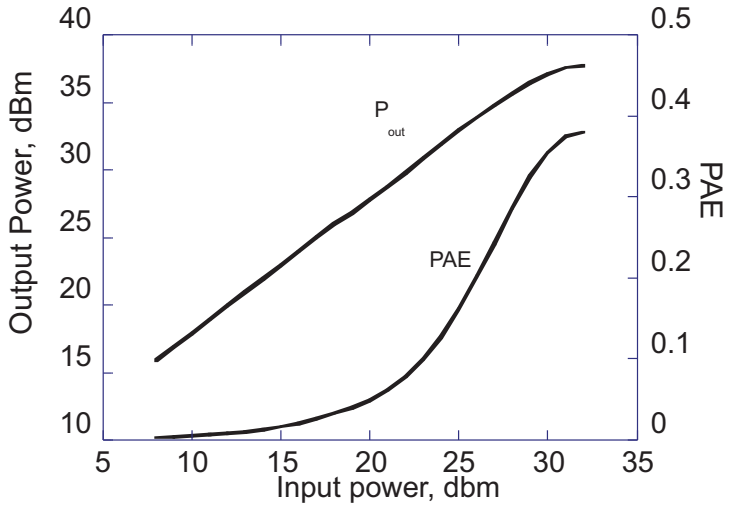

Figure 3.44: Simulated output power and PAE of a common-drain class B vs. input power

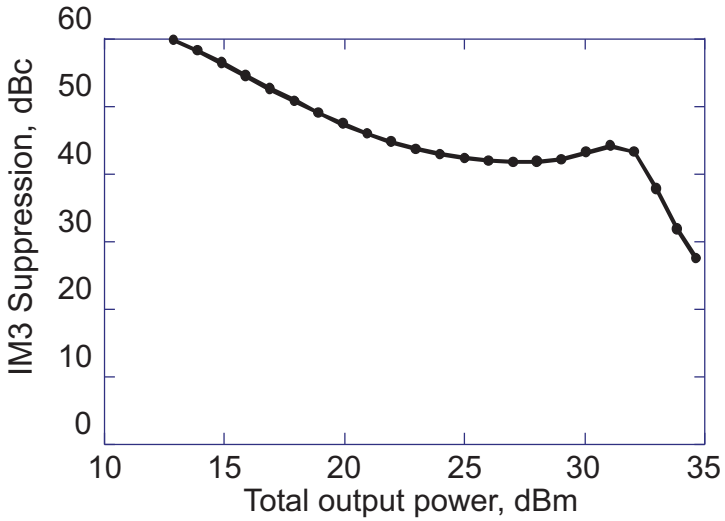

Figure 3.45: Simulated IM_3 suppression vs. output power for the common-drain class B amplifier

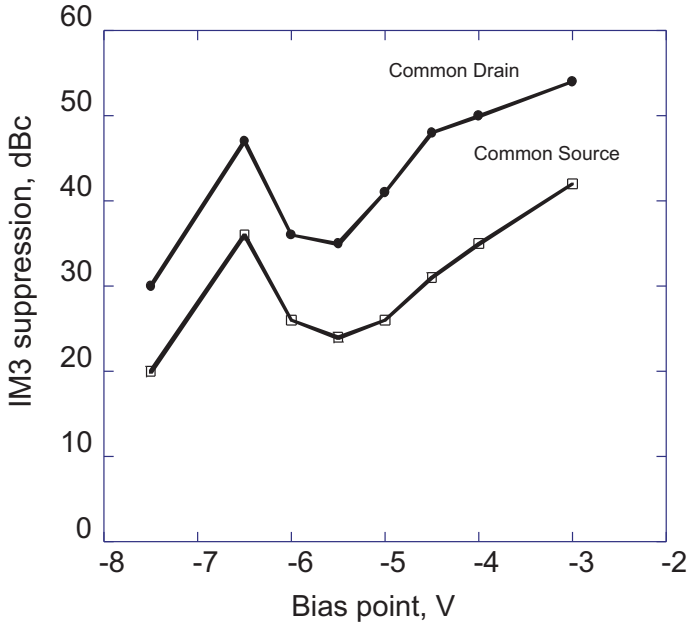

Figure 3.46: Simulated IM_3 suppression vs. bias point of common-drain and an equivalent common-source designs at a total P_{out} = 1 W

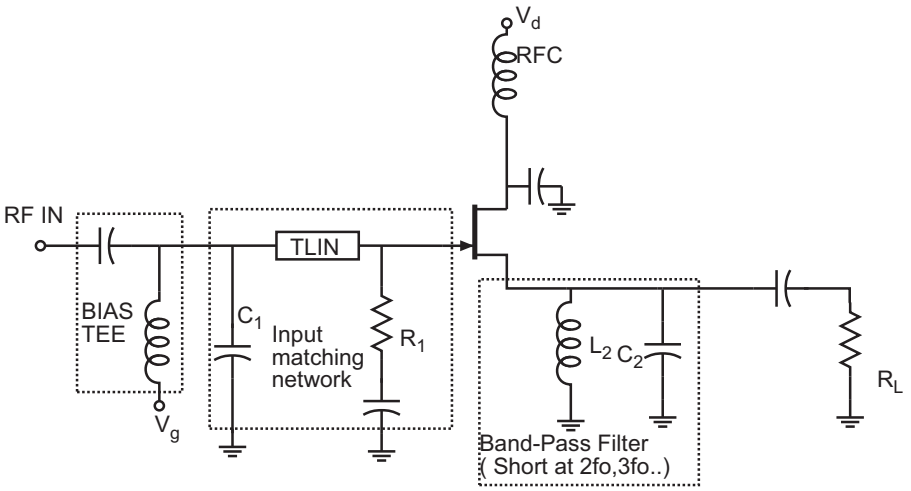

Figure 3.47: Common-drain class B circuit schematic

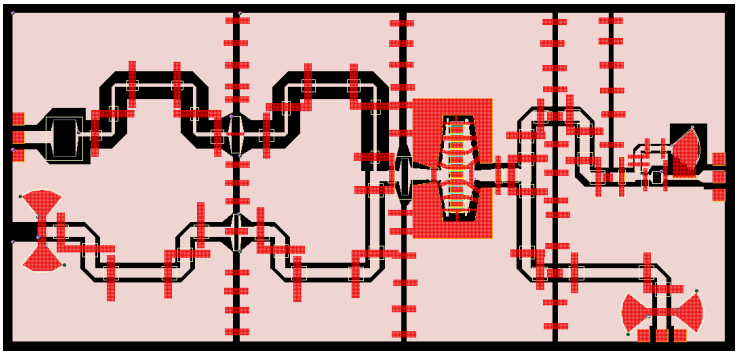

Figure 3.48: Layout of common-drain class B circuit

4

InP DHBT Power Amplifier Design

The second part of this thesis describes designs and results of InP HBT ultra-high-frequency power amplifiers. The objective was to demonstrate amplifiers at the highest possible frequency. High mobility of InGaAs, high electron saturation velocity of InP and submicron scaling result in wide-bandwidth transistors with high available gain in this frequency band. In a transferred-substrate InP HBT process, 6.3 dB gain is reported at 175 GHz with a single stage amplifier [1]. State-of-the-art results in InP HEMT technologies include a six-stage amplifier with 30-dB gain at 140 GHz [2], a three-stage amplifier with 12-15-dB gain from 160-190-GHz [3], and another three-stage power amplifier with 10-dB gain from 144-170-GHz [4]. Recent work in scaled InP/InGaAs/InP mesa DHBT with 30 nm Carbon-doped InGaAs base with graded base doping and 150 nm of total depleted collector thickness achieved wide-bandwidth transistors with 370 GHz f_τ and 459 GHz f_{max} [5, 6]. In

this chapter, realising several power amplifiers built in this technology for applications in the 75-220-GHz frequency range are described.

Since the desired frequency of operation is a significant fraction of the transistor cut-off frequencies (f_τ, f_{max}), a transistor topology that exhibits the highest Maximum Stable Gain (MSG) needs to be chosen [7]. Power amplifiers exhibit less gain than the MSG because output must be large-signal matched, not small-signal matched. The common-base topology exhibits higher MSG than the common-emitter and the common-collector configurations. Further, the higher common-base breakdown voltage is typically more than common-emitter breakdown, resulting in improved power density. IC layout parasitics including the collector to emitter overlap capacitance (C_{ce}) and the base lead inductance (L_b) increase the reverse transmission of the amplifier and significantly reduce MSG of the common-base configuration. If these layout parasitics are not modeled correctly, amplifiers exhibit instability. Advantages and limitations of the common-base topology are discussed in §4.3.

The power density of an HBT amplifier depends upon the output loadline. This loadline should be within the HBT safe operating area (SOA) to avoid device destruction. The safe operating area for InP HBTs is determined by device heating

and collector-base junction breakdown [8]. In addition, the device must be biased below the Kirk effect current if high bandwidth is to be maintained. These limits are described in detail in §4.4.

Design methodology and simulation results of 180 GHz single-stage, two-stage and cascode amplifier designs are presented in §4.4.3.

4.1 InP DHBT Model

The InP DHBT model used is an equation-based physical model. This model gives the designer required flexibility to modify device models based on the changes in the device physical dimensions and process variations. The model parameters can be adjusted to fit the measured DC characteristics and microwave S-parameters. The transistor side view and end view are shown in Fig. 4.1.

The current gain cutoff frequency, f_τ of the transistor is given by

$$\frac{1}{2\pi f_t} = \tau_b + \tau_c + \frac{1}{g_m}(C_{je} + C_{cb}) + (R_{ex} + R_c)C_{cb} \tag{4.1.1}$$

where τ_b is the base transit time, τ_c is the collector transit time, C_{je} is the base emitter junction depletion capacitance. τ_b depends on the rate of diffusion of electrons through the p-type base. The introduction of a quasi-electric field in the base through compositional or doping grading significantly reduces base transit time. For

the HBT results presented in this work, the base is doped with carbon with a concentration gradient. The base doping at the emitter side is 8×10^{19}/cm^3 and at the collector side is 5×10^{19}/cm^3. Electrons entering from the base and traveling through the collector space charge region introduce a displacement current at the collector terminal. The mean delay of this displacement current defines the collector transit time. To a first order in frequency, the collector transit time is given by

$$\tau_c = \frac{T_c}{2v_{\text{eff}}} \tag{4.1.2}$$

where T_c is the thickness of the collector and v_{eff} is the effective collector velocity [9]. Extracted v_{eff} for the mesa InP DHBT devices is between 2.25×10^7 cm/sec and 3×10^7 cm/sec. Collector transit time is directly proportional to the thickness of the collector. The collector thickness also plays a critical role in determining the collector capacitance (C_{cb}).

The emitter resistance, R_{ex} is given by

$$R_{ex} = \frac{\rho_c}{A_E} \tag{4.1.3}$$

where ρ_c is the emitter contact resistivity and A_E is the emitter area. The emitter metal contacts a low bandgap InGaAs layer for low ρ_c.

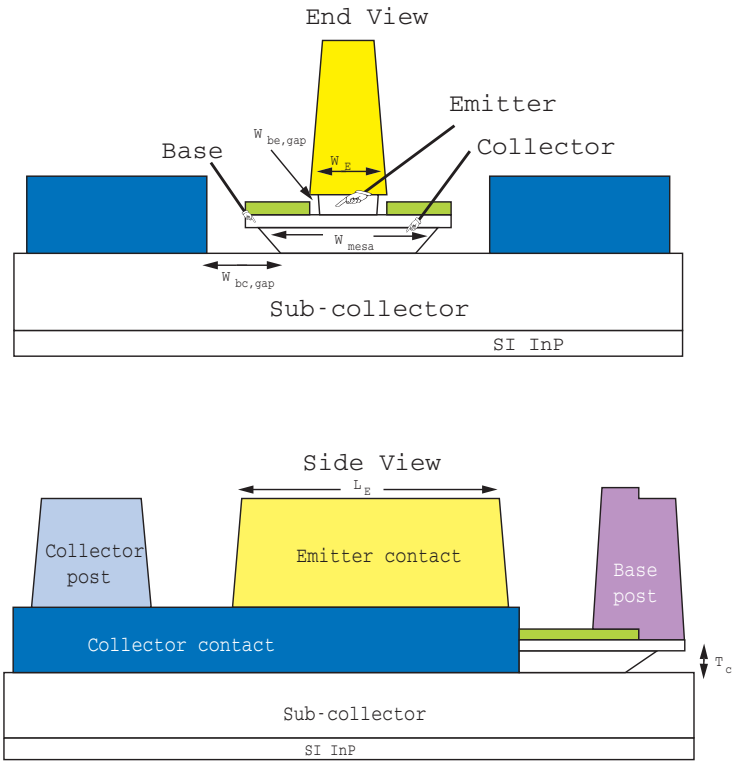

Figure 4.1: End view and side view of an InP HBT

The power gain cutoff frequency, f_{max} is given by

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_{bb} C_{cbi}}} \tag{4.1.4}$$

Where R_{bb} is the base resistance and C_{cbi} is the collector base junction depletion capacitance which is charged through R_{bb}. R_{bb} is composed of base contact resistance,

base gap resistance and the base spreading resistance.

$$R_{bb} = \frac{\sqrt{\rho_c \rho_s}}{2L} + \frac{W_{gap}\rho_s}{2L} + \frac{W_E \rho_s}{12L} \tag{4.1.5}$$

where ρ_c is the base contact resistivity, ρ_s is the base sheet resistance, W_E is emitter contact width and W_{gap} is the gap between the emitter and base. For self aligned base contacts W_{gap} is equal to the emitter undercut during the wet-etch. The collector base capacitance C_{cb} is

$$C_{cb} = \frac{\epsilon W_{mesa}}{T_c}(L_e + 2\ L_{\mathrm{end}}) + C_{\mathrm{cbpad}} \tag{4.1.6}$$

where W_{mesa} is the entire base mesa width and T_c is the thickness of the collector. During the collector wet-etch, semiconductor under the base is heavily undercut to reduce C_{cb} as much as possible. Collector access resistance R_c is given by

$$R_c = \frac{\sqrt{\rho_c \rho_s}}{2L} + \frac{W_{bc,gap}\rho_s}{2L} + \frac{W_{mesa}\rho_s}{12L} \tag{4.1.7}$$

Where ρ_c is the collector contact resistivity, ρ_s is the collector sheet resistance, W_{mesa} is the width of base mesa, $W_{bc,gap}$ is the gap between base and collector contacts. The transistor model is shown in Fig. 4.2

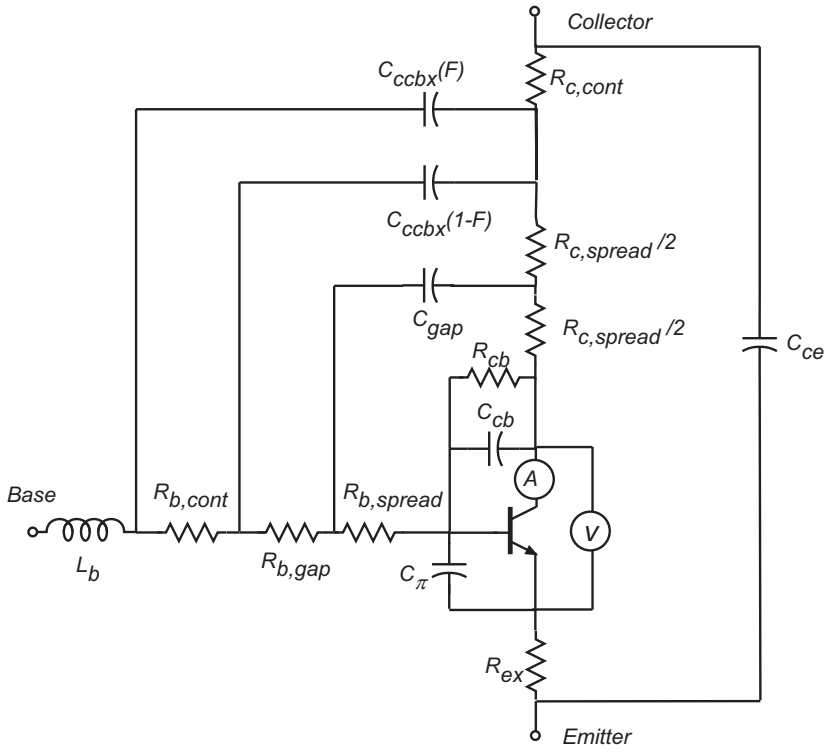

Figure 4.2: InP mesa DHBT model

4.2 InP mesa-DHBT Process

The transistors in the circuit are formed from a Molecular Beam Epitaxial (MBE) layer structure with a highly doped 35 nm InGaAs base and a 210 nm collector and are fabricated in a triple mesa process with both active junctions defined by selective wet etch chemistry. The epitaxial layer structure used in this work is shown

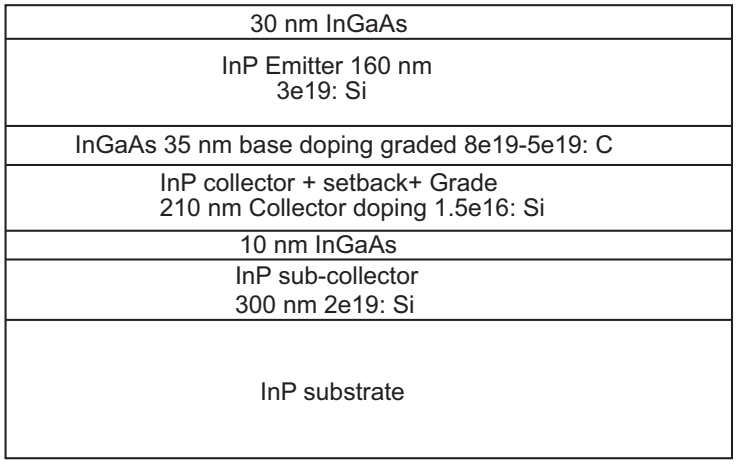

Figure 4.3: InP DHBT layer structure

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in Fig. 4.3. Details of epi-layer design are discussed in [2]. The increased collector thickness over [5] is intended to maintain high f_{max} despite increases in device critical dimensions, motivated by the desire for improved transistor yield. Polyimide passivates and planarises the devices. One level of deposited metal forms circuit interconnects and electrical contacts to transistors and resistors. Silicon Nitride metal-insulator-metal (MIM) capacitors and coplanar waveguide transmission lines are employed to synthesize the tuning elements. Plated airbridges bridge the ground planes and suppress the coplanar waveguide slot-line modes.

The InP mesa-DHBT process flow has been discussed in detail in previous pub-

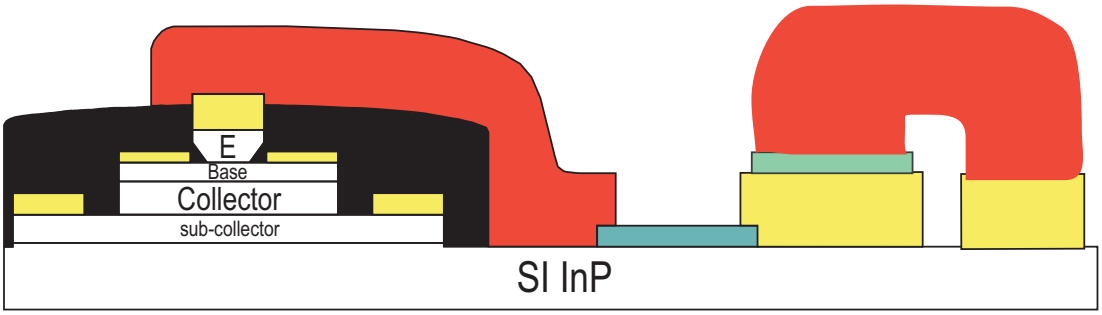

Figure 4.4: Process cross-section of an InP DHBT

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lications [6]. For completeness, a brief discussion of process features is presented here. The emitter- mesa is defined using an all wet-etch self-aligned process. After emitter contact evaporation (Ti/Pd/Au - 20/40/1000 nm), the emitter cap and grade layer are etched using an InGaAs etchant that is composed of H_2O_2:H_3PO_4:H_2O (1:1:20) solution. The InP emitter layer is etched using a HCl:H_3PO_4 (1:4) solution and this etch is selective and stops at the InGaAs base layer. A Pd/Ti/Pd/Au metal stack of thickness 2.5/17/17/85 nm has been shown to provide with low base-contact resistivity. To achieve high f_{max}, it is critical to minimise base-contact resistance. Prior to ohmic contact metallisation, the surface is prepared using Ozone ashing for 10 minutes followed by an etch in 10% NH_4OH with no subsequent Deionised-water rinse. Base and collector materials are etched after masking the emitter-base junction

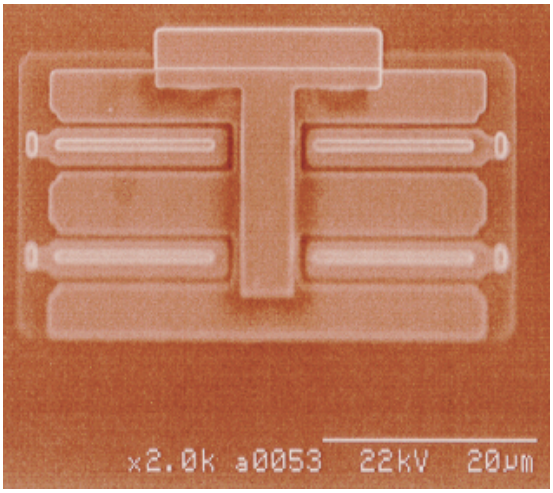

Figure 4.5: Four-finger InP DHBT

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with photoresist. A metal stack Ti/Pd/Au of thickness 20/40/1000 nm is evaporated on top of the base-pad area, so that it projects above the passivation dielectric after a planar etch-back. This base post allows the base to be contacted by the first interconnect metal layer. Collector contacts (Ti/Pd/Au - 20/40/390 nm) are evaporated followed by a mesa-isolation etch (Fig. 4.5, Fig. 4.6). Polyimide passivates the transistors. A 3 μm thick photoresist (AZ 4330) is spun over the polyimide and it is etched back in an O_2 based RIE system to planarise the polyimide and expose the emitter contact, base post and collector post. A Ti/Au metal stack of thickness 10/1000 nm is evaporated as the first interconnect metal layer in order to contact

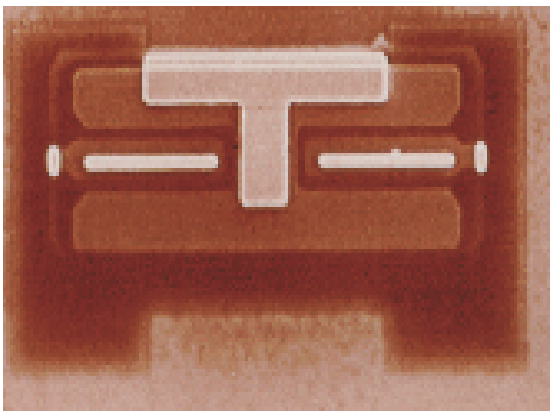

Figure 4.6: Two-finger common-base InP DHBT

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the base, emitter and collector contacts (Fig. 4.7). A Ti/SiO_2/NiCr (2.5/30/48 nm) stack is evaporated to synthesize the resistors. The NiCr resistors exhibited a sheet resistance of 40 $\Omega/\square$. A 400 nm PECVD SiN_x layer forms the dielectric for MIM capacitors. An airbridge process is used to bridge the ground planes to cut-off the slot-line modes of the coplanar waveguide transmission lines. Details of this airbridge process have already been discussed in Chapter 3. The next process step involves fabrication of airbridges that are necessary to bridge the ground planes in coplanar waveguide environment to avoid ground plane discontinuity and suppress slot-line modes. Airbridges also act as a second level of interconnect metal for the MIM capacitor contacts.

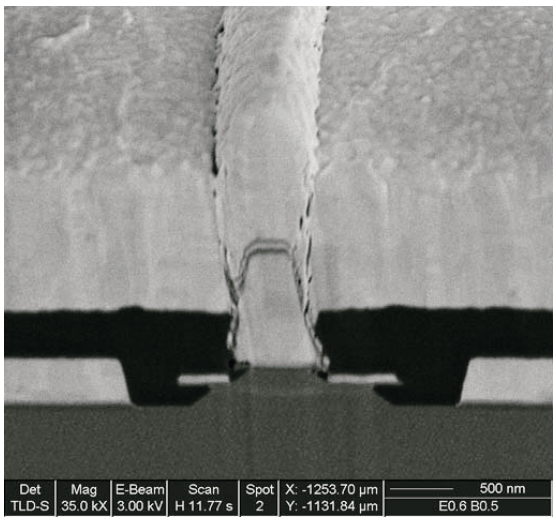

Figure 4.7: Cross-section of an InP DHBT

4.3 Comparison of MSG/MAG

An amplifier is unconditionally stable for all possible combinations of input and load impedances if the stability factor (k) is more than unity and the stability measure $|\Delta|$ is less than unity [7]. The Roulette stability factor, k is defined as

$$k = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{11}|^2}{2|S_{12}S_{21}|} \tag{4.3.1}$$

The stability measure, Δ is given by

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.3.2}$$

When $k < 1$, the amplifier tuning networks require resistive stabilisation and the maximum stable gain (MSG) is given by

$$\mathrm{MSG} = \frac{|S_{21}|}{|S_{12}|} \tag{4.3.3}$$

when $k > 1$, the amplifier's maximum available gain (MAG) is given by

$$\mathrm{MAG} = \frac{|S_{21}|}{|S_{12}|}(k - \sqrt{k^2 - 1}) \tag{4.3.4}$$

The common-base topology is chosen as it has higher maximum stable gain in this band when compared to the common-emitter and common-collector topologies (Fig. 4.8). At present, however, we ignore both the base feed inductance, L_b and the collector-emitter overlap capacitance, C_{ce}. At 180 GHz, the common-base topology exhibits 10-dB MSG while the common-emitter and common-collector topologies exhibit 4 dB and 3 dB respectively. Recall again that power amplifiers use a large-signal load match, rather than a small-signal output match, the power gain falls below the MSG.

The above comparison between different configurations ignores the effect of L_b and C_{ce}. While these parasitics reduce the common-base MSG, in G-band, the common-base topology still provides the highest gain when compared to the common-emitter and common-collector configurations. If not modeled in the de-

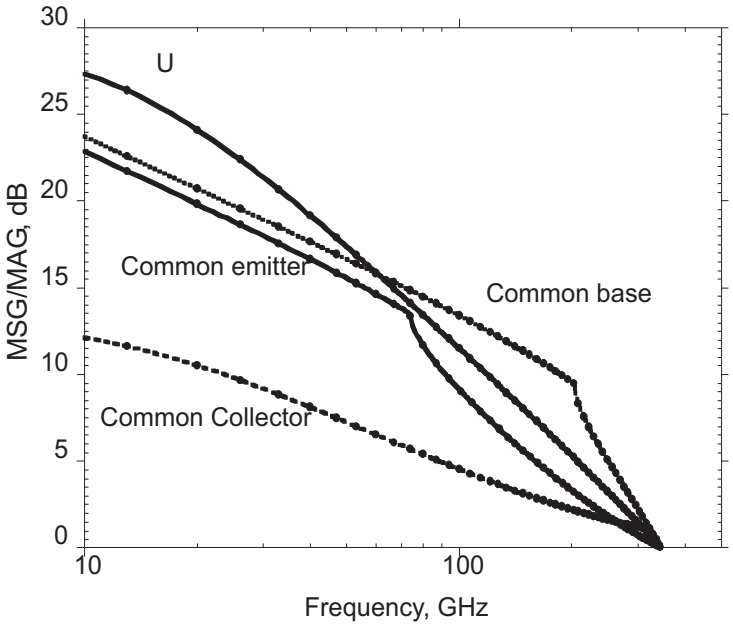

Figure 4.8: Comparison of the simulations MSG/MAG of common-base, common-emitter and common-collector configuration of an InP DHBT. L_b and C_{ce} are omitted in this simulations.

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signs, L_b and C_{ce} could potentially cause instability. Base inductance is due to the long thin base contact metal stripes on either side of the emitter (Fig. 4.9). S-parameter extractions indicate approximately 3 pH base feed inductance per 12 μm long emitter finger having 0.8 μm base contact width on either side of the emitter. The collector to emitter overlap capacitance (C_{ce}) also reduces MSG. C_{ce} is the capacitance between the emitter interconnect metal and the collector ohmic contact metal (Fig. 4.9, Fig. 4.10). These metals are separated by 400-500 nm poly-

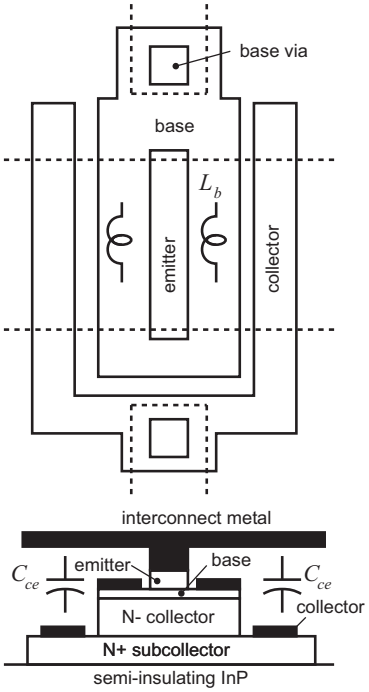

Figure 4.9: Cross-section and top view of an InP mesa DHBT with double-sided collector contacts.

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imide. This thickness varies in our process, rendering C_{ce} variable. Degradation in MSG/MAG of a common-base topology due to the layout parasitics L_b and C_{ce} of an InP DHBT with double-sided collector contacts is shown in Fig. 4.11. The collector to emitter overlap capacitance is significantly reduced by employing single-sided collector contacts as opposed to double-sided collector contacts resulting in improvement in MSG(Fig. 4.12). In addition to reducing C_{ce}, this also increases the

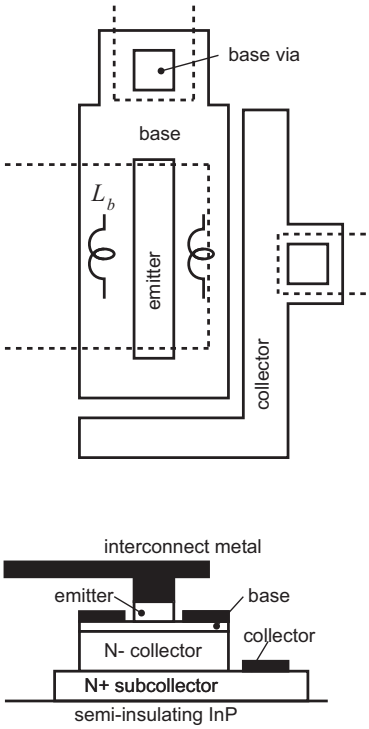

Figure 4.10: Cross-section and top view of an InP mesa DHBT with single-sided collector contact.

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collector resistance and thus, further improves circuit stability.

4.4 Circuit Design

Similar to HEMT power amplifier design, HBT power amplifiers are designed with small-signal input match and large-signal loadline match for the output. HBT

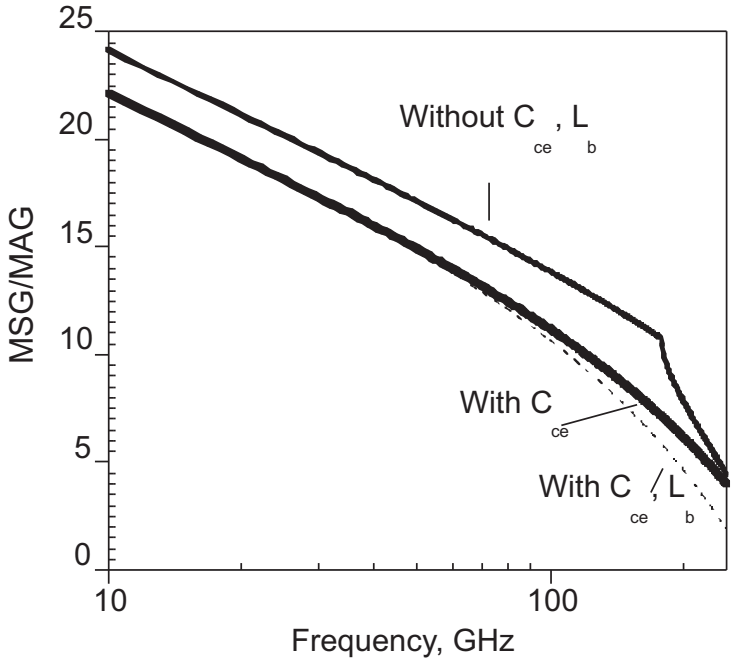

Figure 4.11: Comparison of common-base MSG/MAG with and without layout parasitics. The InP DHBT has a double-sided collector contact.

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output loadline depends upon Kirk current threshold which is a function of the collector-base junction voltage, device heating and the breakdown voltage.

4.4.1 Kirk Current limit

Kirk effect, screening of the applied collector field by the collector electron flux, is observed in bipolar transistors at high bias collector current density. In both ho-

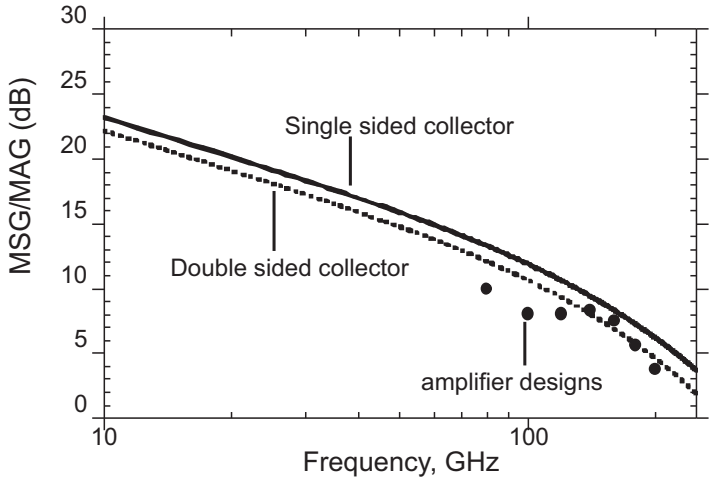

Figure 4.12: Comparison of MSG/MAG of common-base HBT with single-sided collector contact and double-sided collector contacts. The design values of the power amplifier gains are also shown.

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mojunction and single heterojunction bipolar transistors, Kirk effect leads to base push-out, which results in current gain collapse and increased base transit time. Base push-out, however, is prevented in double heterojunction bipolar transistors because the valence energy band barrier at the base-collector junction blocks the holes from spilling into collector. Instead, Kirk effect in DHBTs results in formation of a conduction band barrier in the collector depletion region which impedes current flow. In DHBTs, the collector doping density N_D should be chosen so that the collector is fully depleted at zero collector current. At low current density, $J_c < q \times v_{eff} \times N_D$,

the injected electrons travel at a saturated velocity v_{sat} to the $n+$ sub-collector. As the current density increases from J_c, the injected electron density $(J_c/(qv_{eff}))$ in the depleted $n-$ region can exceed that of the ionized dopant, reversing the sign of the rate of change of the electric field (E) in that region. Kirk effect is defined as the current at which the electric field near the base-collector junction is below the threshold to sustain the electrons saturated velocity. Further increases in collector current density will decrease device bandwidth through base pushout or through conduction barrier formation. This increases the electron density near the junction (Q_e). If the current is further increased, the retarded electrons Q_e will reverse the electric field near the collector-base junction, forming a barrier in the conduction band.

As Kirk effect is approached in a DHBT, the collector transit time τ_c increases due to reduction in the effective electron velocity. The Kirk threshold current density , J_{Kirk} is given by

$$J_{Kirk} = \frac{2\epsilon v_{\text{eff}}(V_{\text{cbmin}} + 2\phi + V_{ce})}{T_c^2} \tag{4.4.1}$$

where V_{cbmin} is the minimum collector-base voltage needed to fully deplete the collector at zero collector current density, ϕ is the base semiconductor bandgap and V_{ce} is applied collector-emitter voltage. A detailed analysis of Kirk threshold current for InP DHBTs is given in [6]. As shown in Eqn. 4.4.1, maximum bias current of

the transistor is set by Kirk threshold and it is inversely proportional to square of the collector thickness. Breakdown voltage is directly proportional to the thickness of the collector. Hence, the power density of HBTs is inversely proprtional to collector thickness. At constant lithography dimensions, reducing collector thickness improves power density at the expense of f_{max}. For a given output power, improved power density results in reduction in finger size. Decreased finger size reduces L_b and improves electrical and thermal stability. If the device f_{max} is improved by lateral dimensional scaling, it is beneficial to use a thinner collector for superior thermal and electrical characteristics of the power amplifier.

4.4.2 Thermal Limit and Breakdown Voltage

The common-base breakdown Voltage (V_{br}), is $>$7 V for an InP DHBT with 210 nm collector thickness. The thermal limit is determined experimentally by determining the failure bias points of the transistor. Based on these three limits the effective safe operating area is determined. The loadline should be within the safe operating area for non destructive power amplifier operation. The safe operating area for an InP common-base DHBT with 2 fingers of 0.8 μm $\times$ 12 μm area is shown in Fig. 4.13.

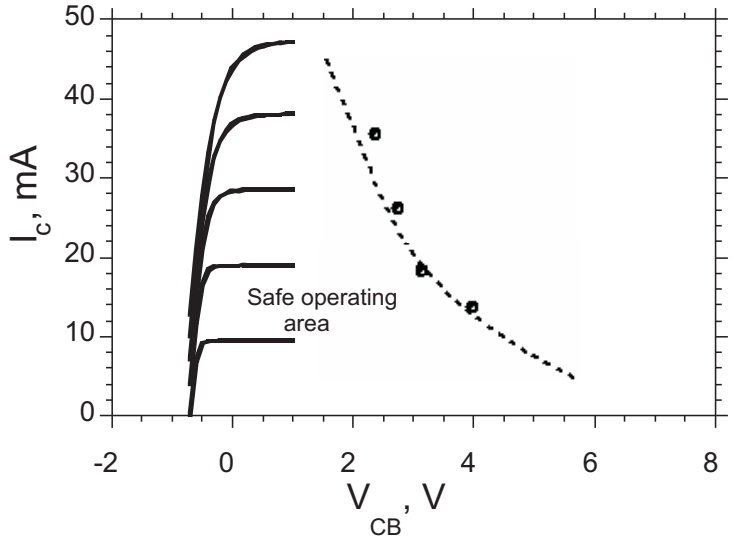

Figure 4.13: Common-base DC characteristics of a two finger 0.7 μm$\times$11 μm common-base DHBT

4.4.3 Tuned Amplifier Designs

Fig. 4.14 shows a single-stage amplifier circuit schematic. Shunt capacitors are either SiN_x MIM capacitors or CPW open-circuit stubs. A multi-section input matching network is used to increase the bandwidth of the tuned amplifier. Output large-signal match determines the overall bandwidth of the amplifier. Two-stage amplifiers (Fig. 4.15) are formed by cascading two identical single-stage designs. The output of the first stage is large-signal matched to the second-stage input, avoiding first stage premature power gain compression. Since two identical stages are cas-

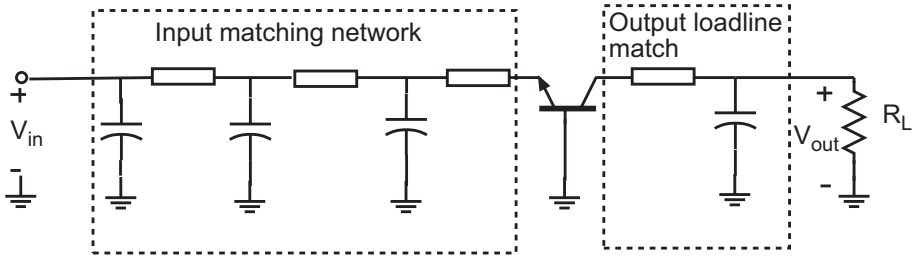

Figure 4.14: Single-stage common-base amplifier

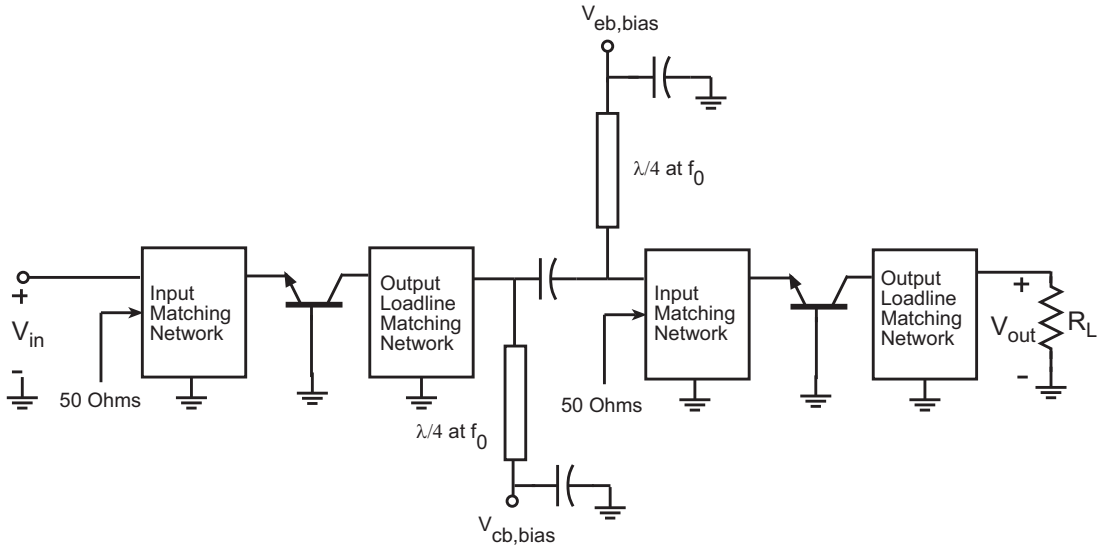

Figure 4.15: Two-stage common-base amplifier

caded, they have similar characteristics, resulting in high bandwidth. The two stages are individually stabilised resulting in simpler overall stability analysis.

4.4.4 Electromagnetic Momentum Simulations

Coplanar waveguide transmission lines, SiN_x capacitors and NiCr resistors synthesise the tuning elements in the amplifier input matching and output loadline matching networks. ADS momentum simulations are performed for the CPW transmission lines to obtain their S-parameters. These S-parameter blocks are then used in the overall amplifier simulations. The physical structure of the NiCr resistors are also simulated using the ADS momentum so that their electromagnetic parasitics are included in the circuit designs. SiN_x capacitors are similarly modeled in ADS momentum.

4.5 Power Amplifier Simulations

The InP HBTs used in the amplifier designs have Kirk current density approximately 3.5 mA/μm^2 when V_{cb} = 0 V. The common-base breakdown voltage is approximately 7 V. The f_τ and f_{max} of the transistors are 250 GHz and 350 GHz when the HBT is biased at collector current density J_c = 1.5 mA/μm^2 and V_{ce} = 3 V. 140-220-GHz designs employed two separate InP HBT fingers, each of 0.8 μm $\times$ 12 μm. The length of the emitter is small due to the reduced base access resistance, base lead

inductance and to reduce the tendency for current crowding within the HBT fingers. Design examples for a single-stage amplifier, a two-stage amplifier and a cascode amplifier are presented below.

4.5.1 180 GHz Single-Stage Amplifier

The circuit schematic is shown in Fig. 4.16. This design consists of two InP DHBTs ($2 \times 0.8\mu m \times 12\ \mu m$) each input matched to $50\ \Omega$ and output loadline matched to $100\ \Omega$. Input power is divided and output power combined by employing $\lambda/4$ length CPW transmission lines with 70.7 Ω characteristic impedance.

This amplifier is designed to exhibit 5.3-dB power gain at 180 GHz (Fig. 4.17) when biased at I_c = 65 mA and V_{cb} =2.3 V. The simulated 3-dB bandwidth is approximately 45 GHz and is set by the input matching network. The designed loadline at 180 GHz of this amplifier is shown in Fig. 4.18. The device model does not model the Kirk current phenomena and the breakdown voltage, and hence the designer must manually check that the loadline does not exceed the Kirk current or leave the transistor safe operating area and breakdown voltage.

For this amplifier, in simulations, the maximum saturated output power is approximately 20 dBm (Fig. 4.19) and maximum PAE is approximately 17%. The

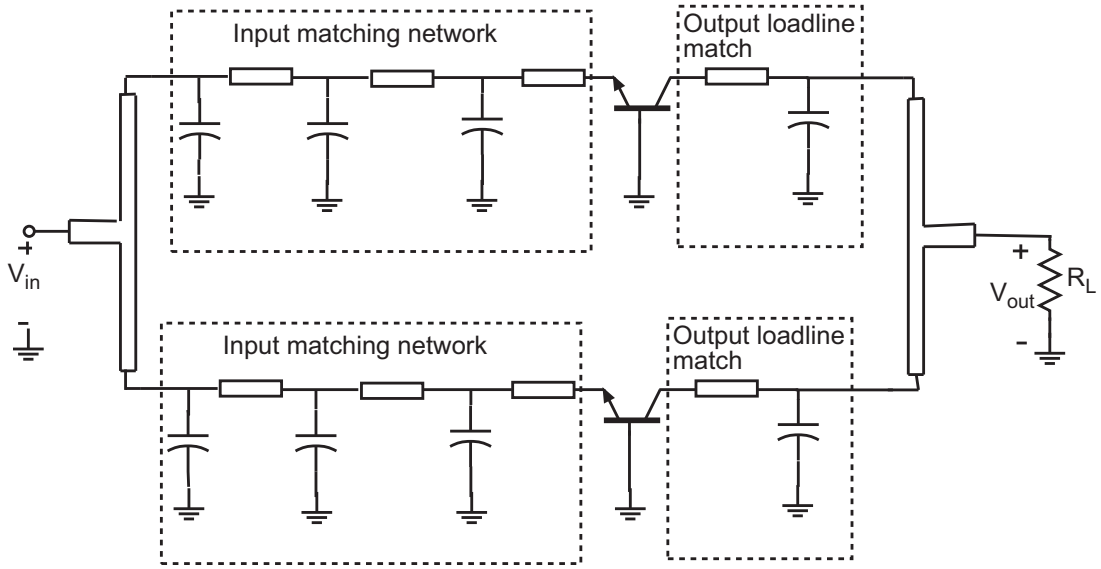

Figure 4.16: Circuit Schematic of a 180 GHz amplifier

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simulated 1-dB gain compression point, $P_{1-\mathrm{dB}}$ is 19 dBm.

4.5.2 180 GHz Two-Stage Amplifier

Two-stage amplifiers (Fig. 4.15) are formed by cascading two identical single-stage designs. The output of the first-stage is large-signal matched to the second stage input, avoiding first stage premature power gain compression.

The first-stage employs an InP DHBT that consists of two separate 0.8 μm $\times$ 12 μm emitter fingers. This stage drives a second stage that has two separate two-finger

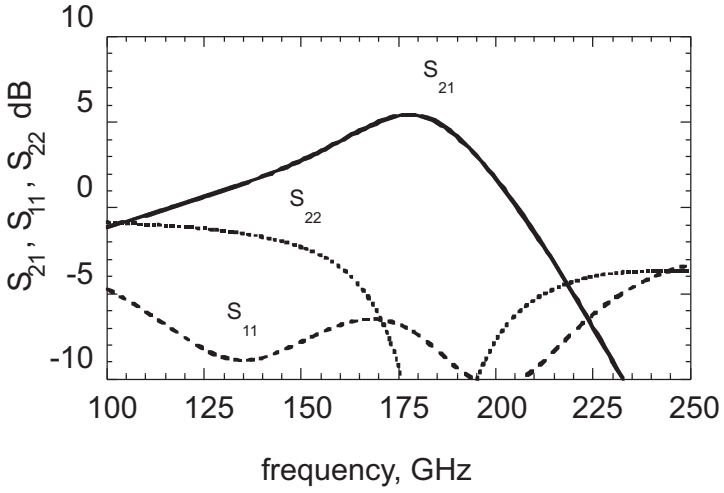

Figure 4.17: Simulated S-parameters of the 180 GHz amplifier of Fig. 4.16

DHBTs with input power division and output power combining (as discussed in the previous section). This amplifier is designed to exhibit 8.7-dB power gain at 180 GHz (Fig. 4.20) when the first-stage is biased at I_c = 32 mA and V_{cb} = 2.3 V and the second-stage is biased at I_c = 65 mA and V_{cb} = 2.3 V. The two stages are biased separately with a coupling capacitor between the stages. The coupling capacitor and the big feed transmission lines have been designed using ADS momentum. The simulated 3 dB bandwidth is approximately 45 GHz. The maximum saturated output power is approximately 20 dBm (Fig. 4.21).

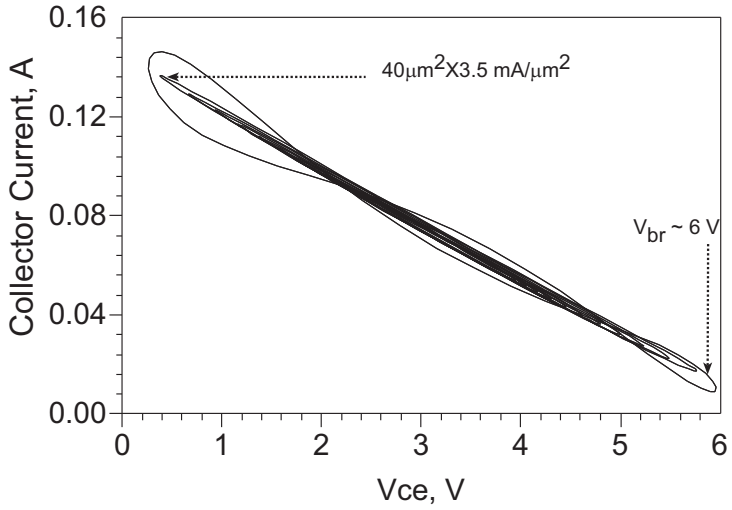

Figure 4.18: Simulated output loadline of the 180 GHz power amplifier of Fig. 4.16

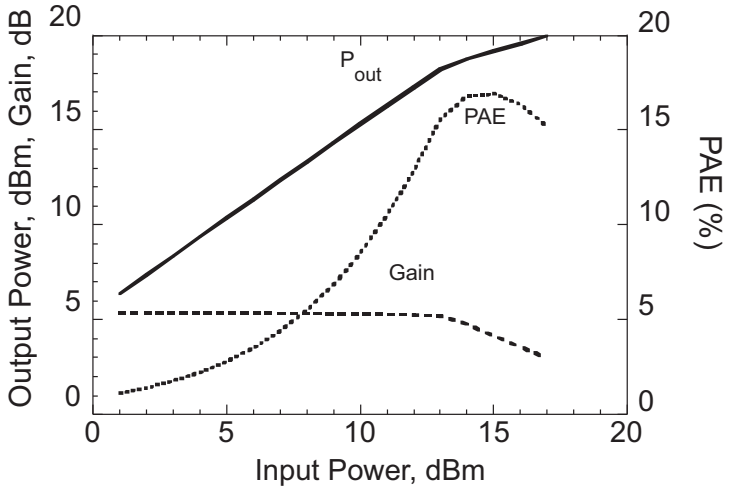

Figure 4.19: Simulated output Power and gain vs. input power of the 180 GHz power amplifier of Fig. 4.16

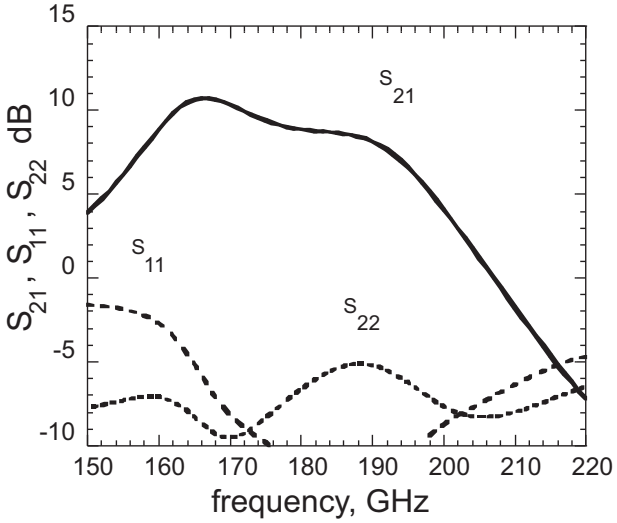

Figure 4.20: Simulated S-parameters of the 180 GHz two-stage amplifier

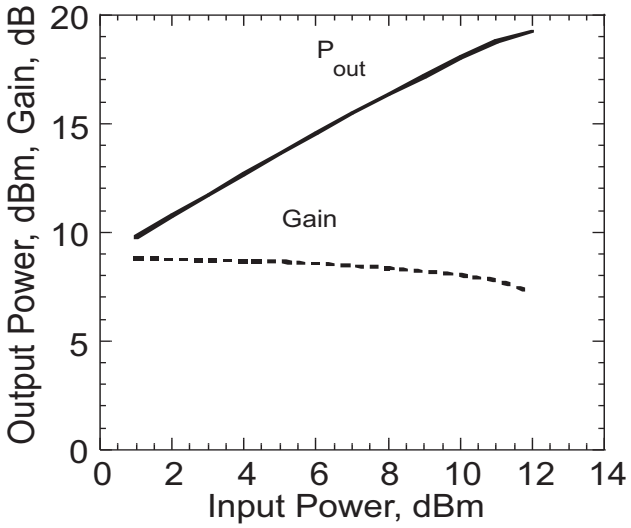

Figure 4.21: Simulated output power and gain vs. input power of the 180 GHz two-stage power amplifier

4.5.3 180 GHz Cascode Amplifier

This amplifier employs two separate two finger DHBTs to realize the common-emitter, common-base transistors for the cascode topology (Fig. 4.22). The two stages are biased separately with a coupling capacitor between the stages. This amplifier is designed to exhibit 8-dB power gain at 180 GHz (Fig. 4.17). The maximum saturated output power is simulated to be approximately 16.5 dBm (Fig. 4.19).

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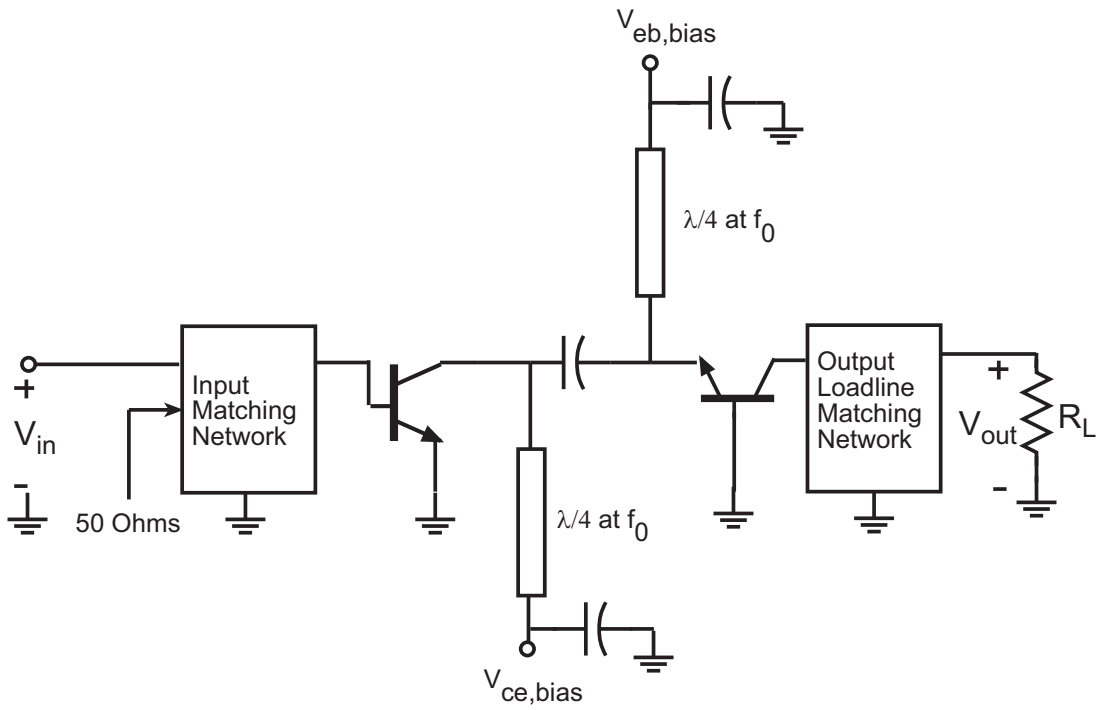

Figure 4.22: Circuit Schematic of a 180 GHz cascode amplifier

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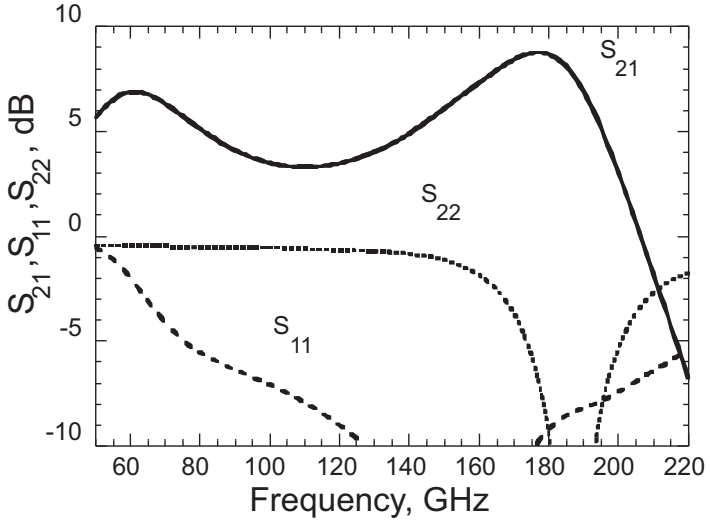

Figure 4.23: Simulated S-parameters of the 180 GHz cascode amplifier

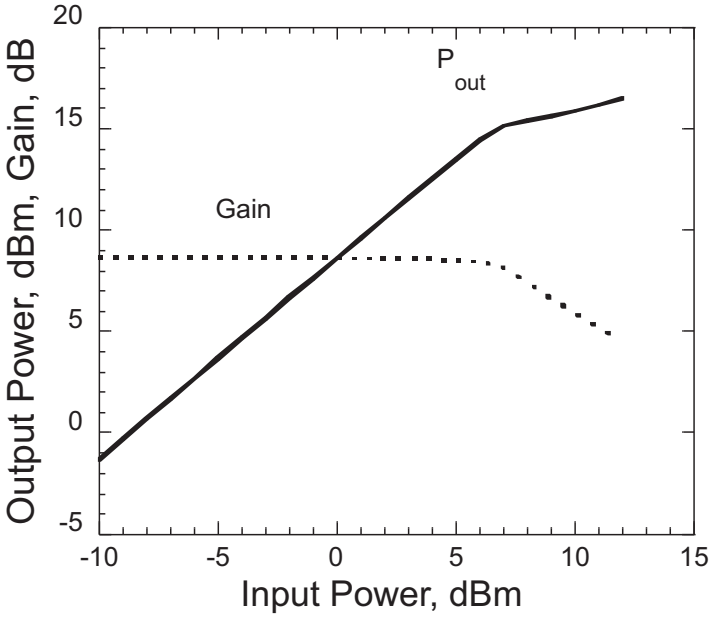

Figure 4.24: Simulated output power and gain vs. input power of the 180 GHz cascode power amplifier

5 InP Power Amplifier Results

In this chapter, the small-signal power measurement setup is described followed by the small-signal and power simulations and measurement results of the power amplifiers.

5.1 DC Characteristics

DC measurements are presented in this section. The Transmission line model (TLM) structure measurement data for base contacts and DC common-emitter characteristics of InP HBTs are shown below.

5.1.1 TLM Measurements

Two different kinds of base TLMs are measured to estimate base-contact resistance. Pinched base TLMs have a floating emitter-base junction as opposed to

unpinched TLMs that do not have a base-emitter junction. Comparing sheet resistance of pinched and unpinched TLMs, it is possible to determine the extent to which base semiconductor is etched during emitter wet-etch. Reduction of base thickness in unpinched TLMs could also be due to surface depletion after the emitter semiconductor wetetch. Unpinched TLMs measure higher sheet resistance than pinched TLMs. TLM measurements are performed using a four-probe measurement technique for accurate measurement. On these HBTs, with a 35 nm base thickness and with a doping concentration gradient from 8×10^7/cm^3 to 5×10^7/cm^3, the base sheet resistance is $500\ \Omega/\square$ and the base-contact resistivity is 9 Ω-μm^2 (Fig. 5.1). These measurements are subject to error due to shrinkage in the TLM pad separation due to optical lithography process tolerances. This TLM pad separation shrinkage results in an error in the contact resistivity measurement. The pinched TLM measurement (Fig. 5.2) give $\rho_s = 420\ \Omega/\square$ and ρ_c = 50 Ω-μ m^2. The extrapolated contact resistivity for pinched and unpinched TLMs is different due to two reasons. First, in pinched TLMs, the sheet resistance in the undercut-gap is different from that of the portion with emitter semiconductor on the top. Second, typically, base and emitter metals expand beyond the mask dimensions during lithography and metallisation. For pinched TLMs, the TLM pad separation increases as the emitter metal

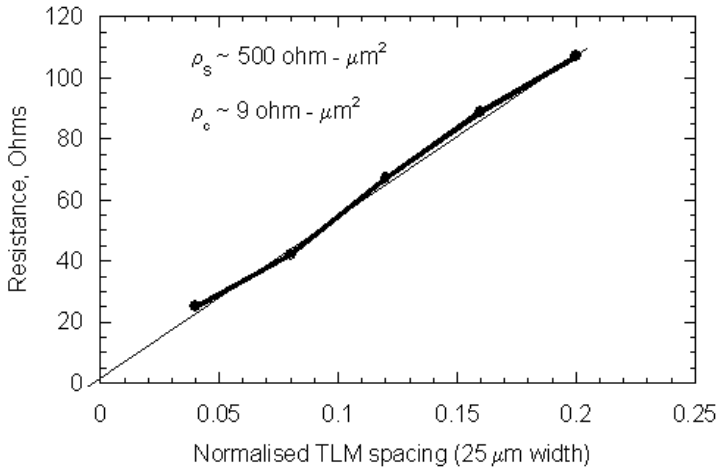

Figure 5.1: Unpinched base TLM measurements

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determines the TLM pad spacing. This leads to false increase in the extrapolated base-contact resistivity. For unpinched TLMs, however, the TLM pad separation decreases. From above arguments, it can be inferred that the actual contact resistivity is between the values measured using pinched and unpinched TLMs. To accurately determine the contact resistivity, TLM pad separation for pinched and unpinched TLMs need to be measured with a Scanning Electron Microscope with high resolution.

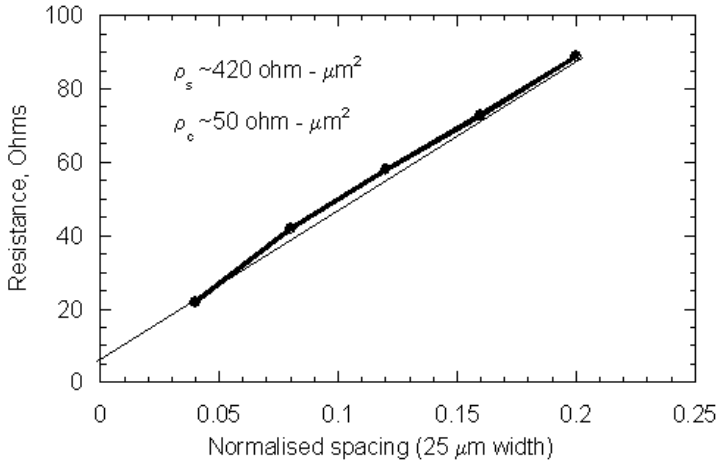

Figure 5.2: Pinched base TLM measurements

5.1.2 Common-emitter Characteristics

DC measurements are performed using an Agilent parameter analyser (4155C) with GSG probes to contact the transistor terminals. DC characteristics of a common-emitter device with 1 μm emitter width and 8 μm emitter length (mask dimensions) are shown in Fig. 5.3 and Fig. 5.4. Fig. 5.3 shows collector current as a function of collector-emitter voltage when base current is increased from 150 μA in steps of 150 μA. β is approximately 24. Fig. 5.4 shows that the common-emitter breakdown voltage is $> 6\ V$.

Gummel measurements for this common-emitter device are shown in Fig. 5.5.

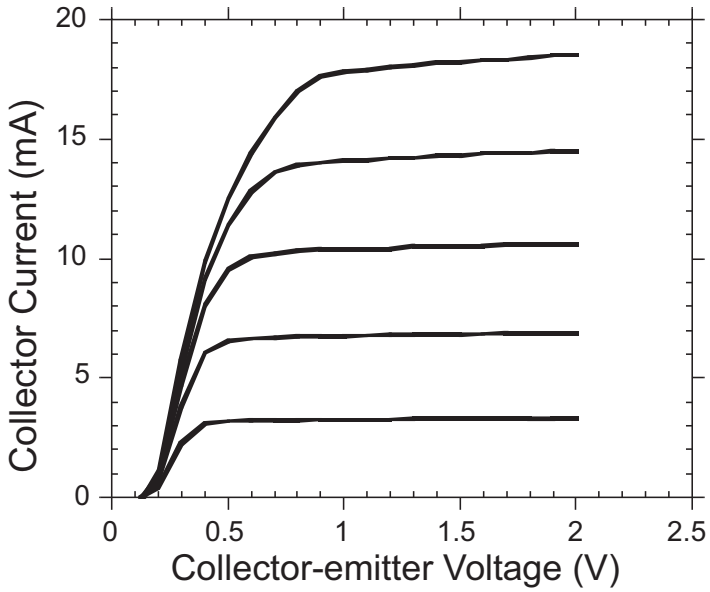

Figure 5.3: DC common-emitter characteristics of a 2×0.8 μm$\times 12$ μm (mask) InP DHBT at I_b = 150, 300, 450, 600, 750 μA

The extracted collector and base current ideality factors are found to be 1.7 and 2 respectively.

5.1.3 Common-base Characteristics

DC characteristics of a two-finger common-base device with 0.8 μm emitter width and 12 μm emitter length are shown in Fig. 5.6 and Fig. 5.7. Fig. 5.7 shows that the common-base breakdown voltage is $> 7\ V$.

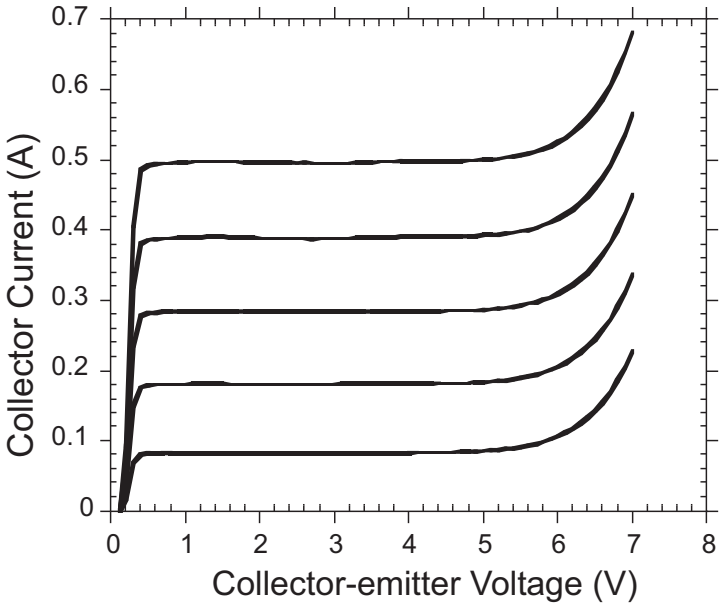

Figure 5.4: DC common-emitter characteristics of a 2×0.8 μm$\times12$ μm (mask) InP DHBT at I_b = 5, 10, 15, 20, 25 μA

DC characteristics of a four-finger common-base device with 0.8 μm emitter width and 12 μm emitter length (mask dimensions) are shown in Fig. 5.8.

5.2 Microwave Measurements

Small-signal and power measurement setups for different frequency bands are discussed in this section. Device S-parameter measurements are also presented to ascertain f_τ, f_{max} of the HBTs.

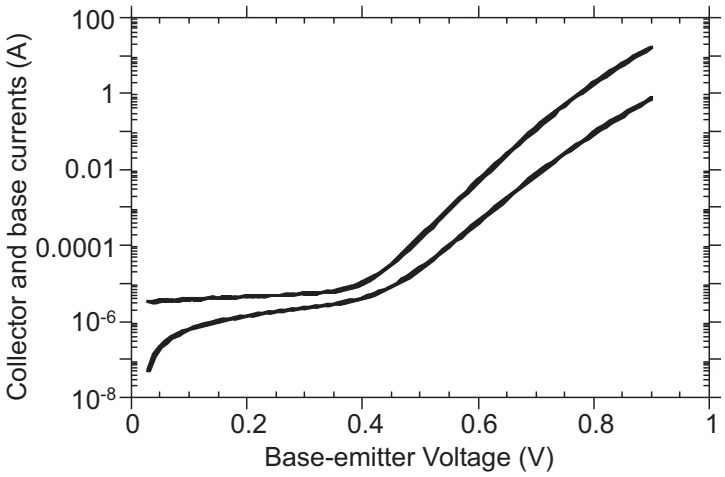

Figure 5.5: Gummel measurements of a common-emitter HBT with 0.8 μm emitter width and 8 μm emitter length (mask dimensions)

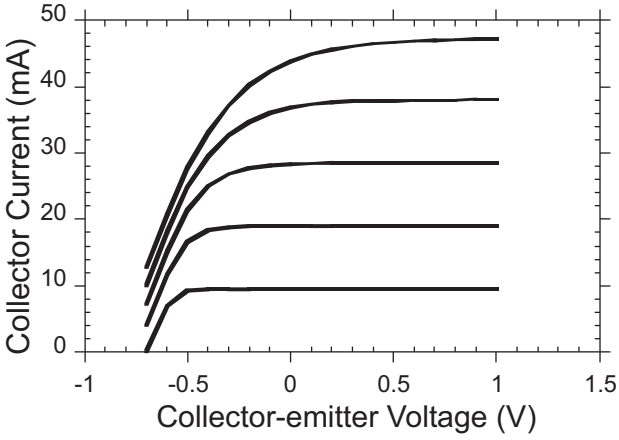

Figure 5.6: DC common-base characteristics of a 2×0.8 μm$\times12$ μm (mask) InP DHBT

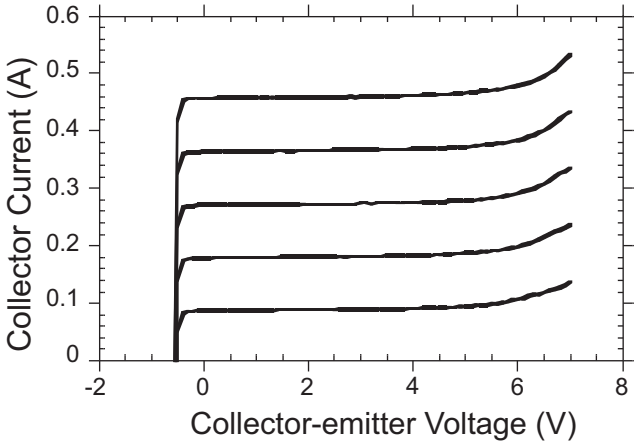

Figure 5.7: DC common-base characteristics of a 2×0.8 μm$\times12$ μm (mask) InP DHBT

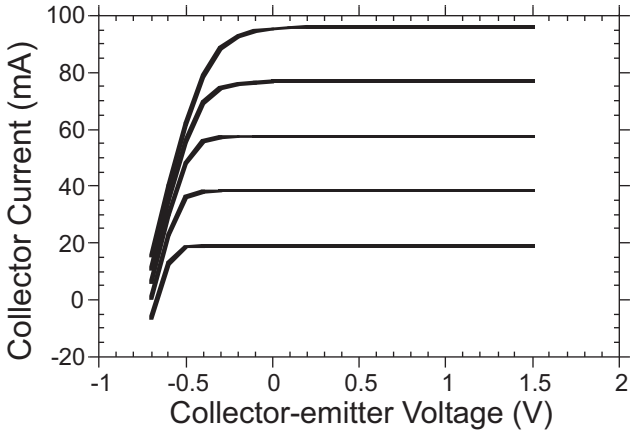

Figure 5.8: DC common-base characteristics of a 4×0.8 μm$\times12$ μm (mask) InP DHBT

5.2.1 Small-signal Measurements

G-band amplifiers are measured on wafer using an HP 8510C Vector Network Analyser with Oleson Microwave Labs Millimeter Wave VNA extensions. The test-set extensions are connected to GGB Industries coplanar wafer probes via WR-5 waveguides. The amplifier measurements are calibrated using off-wafer (Thru-Reflect-Line) TRL calibration standards. W-band amplifier small-signal gains and return losses were measured on-wafer using a W-band Agilent 8510 Network Analyzer calibrated with an off-wafer calibration using TRL calibration standards.

The devices have shown 240 GHz f_τ and 290 GHz f_{max} when biased at current density, J_E = 3 mA/μm^2 and V_{ce} = 1.7 V (Fig. 5.9). The degradation in f_{max} relative to [2] is due to a wider base mesa intended to improve yield and due to relatively poor base ohmic contacts in this process run.

5.2.2 Power Measurements

G-band power measurements were performed at Jet Propulsion Laboratories (JPL), Caltech., USA. The 170-180-GHz power measurement setup is shown in Fig. 5.10. W-band power from a Backward Wave Oscillator (BWO) power source is amplified and is doubled in frequency using a Schottky-diode frequency-doubler.

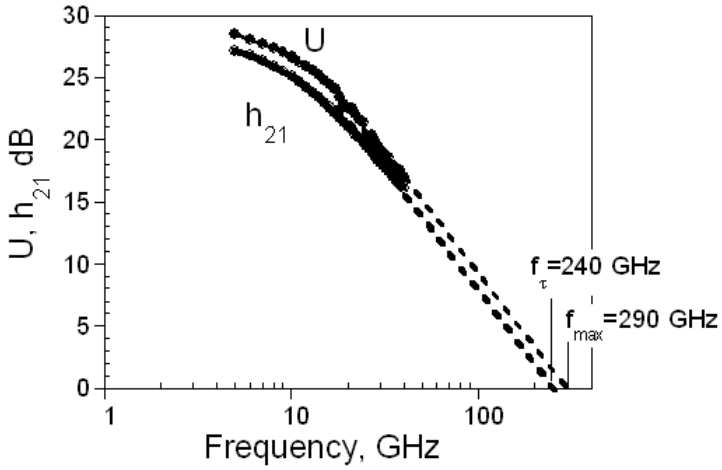

Figure 5.9: Measured short circuit current gain and Mason's gain as a function of frequency of a single finger 0.8 μm$\times$ 8 μm (mask) common-emitter DHBT

The frequency doubler output drives the input of the device under test (DUT). The DUT output power is measured using a calorimeter. Because the input and output power are measured at separate times, the saturated power gain measurements are subject to approximately 1-dB drift in gain. Input power is measured when the input and output probes are connected through a short transmission line. When the amplifier is probed, some of the input power is reflected back due to impedance mismatch between the source and the amplifier input and the amplifier absorbs less input power to the extent of the mismatch. Given that the Schottky diode frequency doubler has significant S_{22}, and that there is little attenuation between the

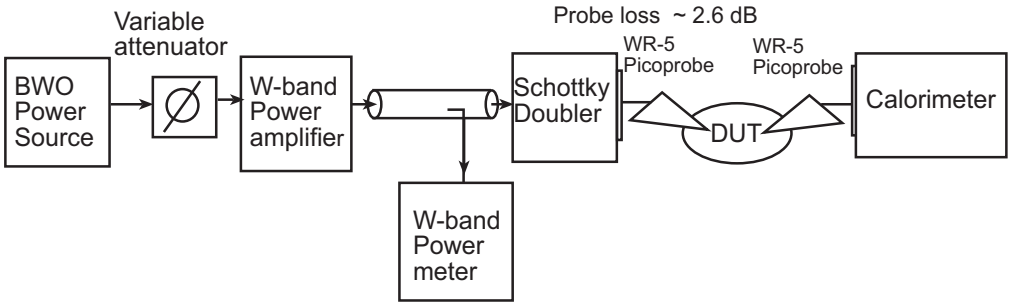

Figure 5.10: 170-180-GHz power measurement setup

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doubler and DUT, standing waves between the doubler and the DUT may introduce a strong frequency dependence to the input drive, of a form of approximately $(1 - S_{22,\text{source}} \times S_{11,\text{amp}} \times e^{-2j\beta l})^{-1}$. The saturated output power measurement is not subject to this drift as the output power is measured directly using a calorimeter, we estimate the output power data is accurate to 0.5-dB. Data is corrected for measured probe attenuation. At 172 GHz and 176 GHz, the maximum input drive power is 3.7 dBm and 9 dBm respectively.

The 148-152 GHz measurement setup is shown in Fig. 5.11. A 150 GHz Gunn oscillator drives the DUT. A variable attenuator adjusts the input power. Output power is measured using an Ericsson Calorimeter. At 150.2 GHz, maximum input power is 7 dBm.

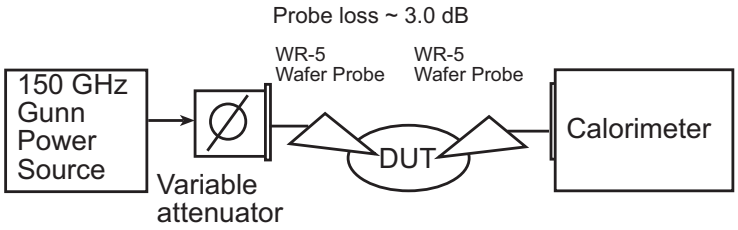

Figure 5.11: 148-152-GHz power measurement setup

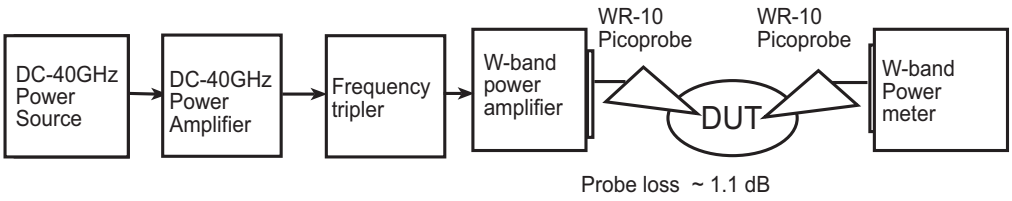

Figure 5.12: 75-110-GHz power measurement setup

The 75-110-GHz power measurement setup is shown in Fig. 5.12. The output of a DC-40-GHz frequency synthesizer is amplified and tripled in frequency to 75-110-GHz. This signal is further amplified to drive the DUT input. The DUT output power is measured using a W-band power sensor. The maximum input power is 11 dBm.

5.3 Circuit Results

5.3.1 176 GHz Single-Stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.13. The transistor used in this circuit has two separate 0.8 μm $\times$12 μm fingers. The amplifier bandwidth is limited by the output tuning network. The transistor output is large-signal load-line matched for maximum saturated output power as opposed to a small-signal match for maximum gain. The amplifier is biased using off-wafer bias-Tees at the input and the output. Input and output probe pads are also included in the circuit simulation. This circuit is simulated with 5-dB small-signal gain at 185 GHz (Fig. 5.14) with 24 GHz 3-dB bandwidth. Maximum saturated output power of 16.3 dBm is simulated at 185 GHz (Fig. 5.15). These simulations are performed when the transistor is biased at I_c = 30 mA and V_{cb} = 2.6 V.

Measurements

A die photograph is shown in Fig. 5.16. This amplifier exhibited 7-dB small-signal gain at 176 GHz when biased at I_c = 30 mA and V_{cb} = 1.0 V. (Fig. 5.17)

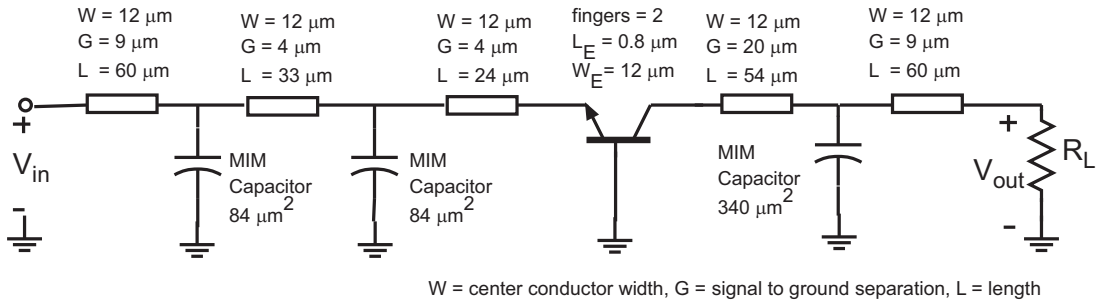

Figure 5.13: Schematic of the 176 GHz single-stage amplifier

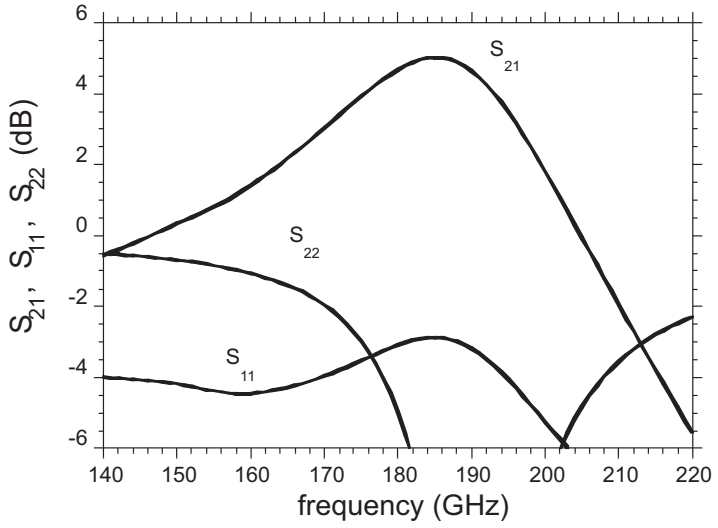

Figure 5.14: Simulated S-parameters of the 176 GHz single-stage amplifier

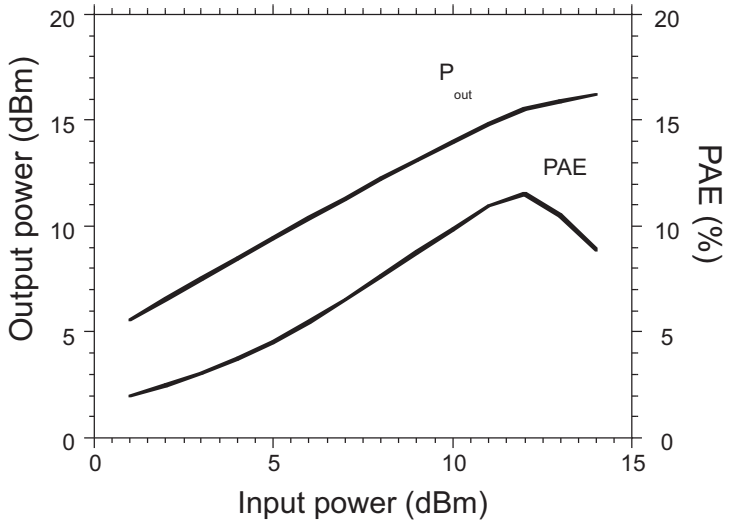

Figure 5.15: Simulated output power and PAE vs. input power of the 176 GHz single-stage amplifier

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The output power vs. input power characteristic is shown in Fig. 5.18. The amplifier exhibited a saturated output power of 8.77 dBm with an associated power gain of 5-dB at 172 GHz when biased at I_c = 40 mA and V_{cb} = 2.06 V. This power amplifier demonstrated $>$ 8-dBm saturated output power between 172-176-GHz (Fig. 5.19). The circuit exhibited 7.9-dB uncompressed gain under the above conditions at 172 GHz. The measured S-parameter data exhibits potential instablility in the 140-170-GHz range due to feedback parasitics L_b and C_{ce}. Output power is significantly less than the designed value. This could be due to significant deviation

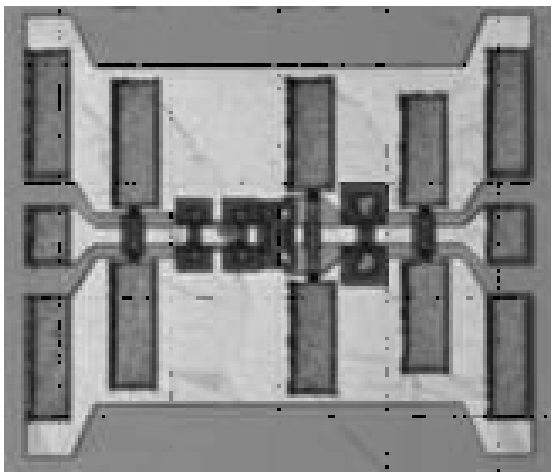

Figure 5.16: Die photograph of the single-stage common-base MMIC amplifier centered at 176 GHz. This measures 0.36 mm $\times$ 0.3 mm

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in the output large-signal match from the designed load owing to variation in SiN_x thickness resulting in variation in capacitor values.

5.3.2 165 GHz Single-stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.20. The transistor used in this circuit has two separate 0.8 μm $\times$12 μm fingers. Input match is designed to have wide bandwidth by employing a three fold L-matching network. The amplifier bandwidth is limited by the output tuning network. The amplifier is biased using off-wafer bias-

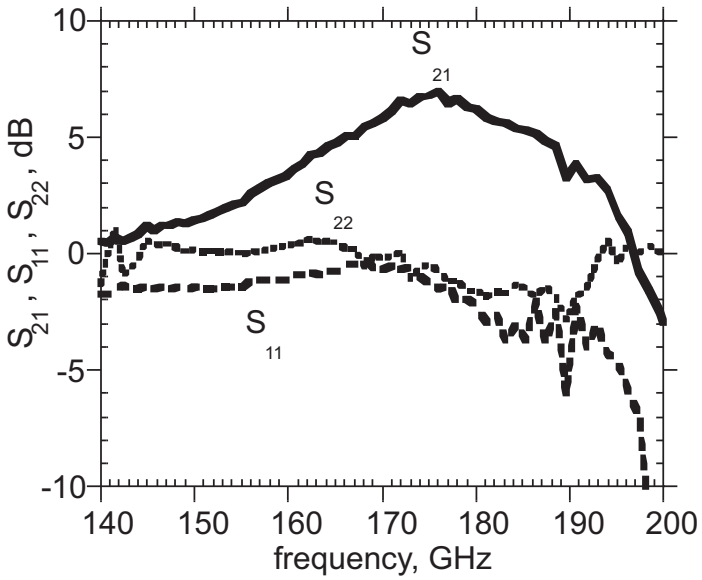

Figure 5.17: Measured S-parameters of the 176 GHz single-stage amplifier shown in Fig. 5.16

Tees at the input and the output. Input and output probe pads are also included in the circuit simulation. This circuit is simulated with 6.2-dB small-signal gain at 175 GHz (Fig. 5.21) with 40 GHz 3-dB bandwidth. Maximum saturated output power of 16.4 dBm is simulated at 175 GHz (Fig. 5.22). These simulations are performed when the transistor is biased at I_c = 30 mA and V_{cb} = 2.6 V.

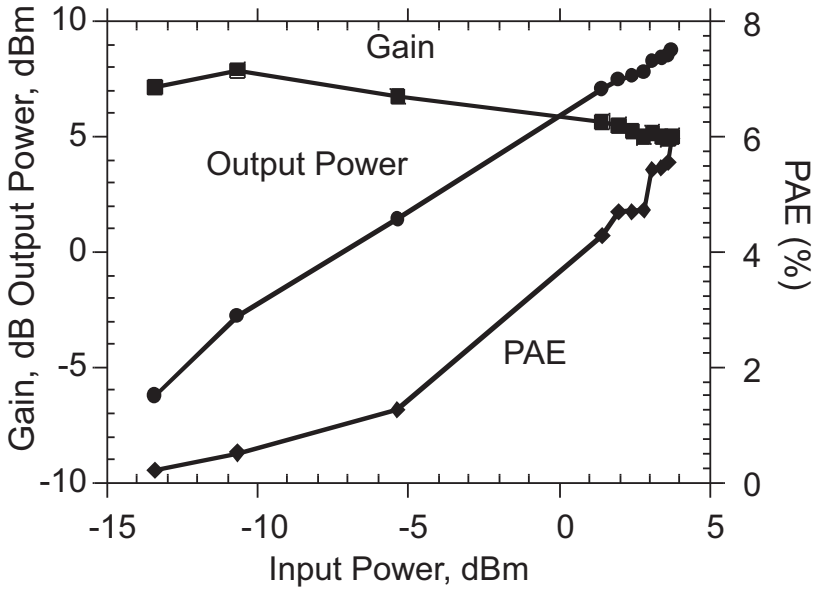

Figure 5.18: Measured output power and Power Added Efficiency (PAE) vs. input power of the 176 GHz single-stage amplifier (Fig. 5.16) at 172 GHz

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Measurements

This single-stage common-base amplifier (Fig. 5.23) exhibited 6.5-dB small-signal gain at 165 GHz (Fig. 5.24) when biased at I_c = 31 mA and V_{cb} = 1.0 V. This amplifier's small-signal gain is $>$ 3-dB between 152-180-GHz. The transistor has two separate 0.8 μm$\times$12 μm fingers.

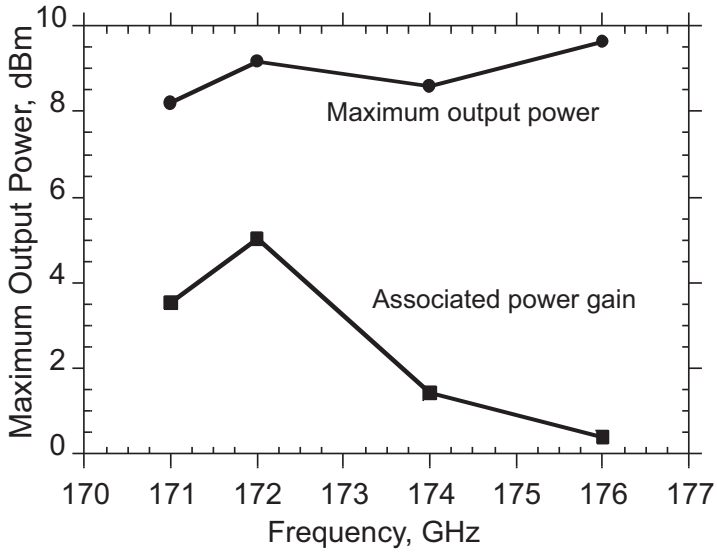

Figure 5.19: Measured 176 GHz amplifier (Fig. 5.16) saturated output power as a function of frequency

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This power amplifier exhibited 8.3 dBm saturated output power with 4.5-dB associated power gain at 172 GHz (Fig. 5.25) when biased at I_c = 47 mA and V_{cb} = 2.1 V. Uncompressed power gain is 6 dB at 172 GHz. The gain at maximum measured power has not compressed significantly indicating higher output power could be achieved by providing higher input drive power.

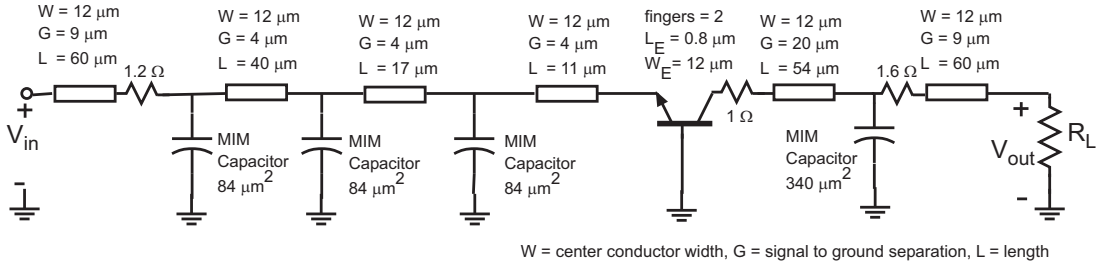

Figure 5.20: Schematic of the 165 GHz single-stage amplifier

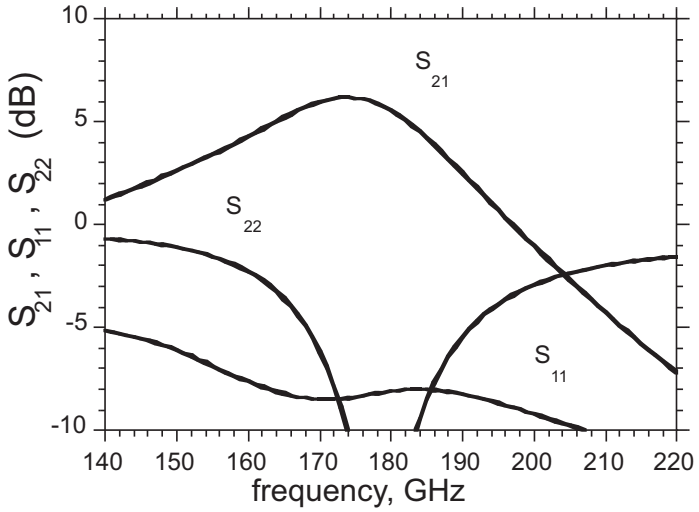

Figure 5.21: Simulated S-parameters of the 165 GHz single-stage amplifier

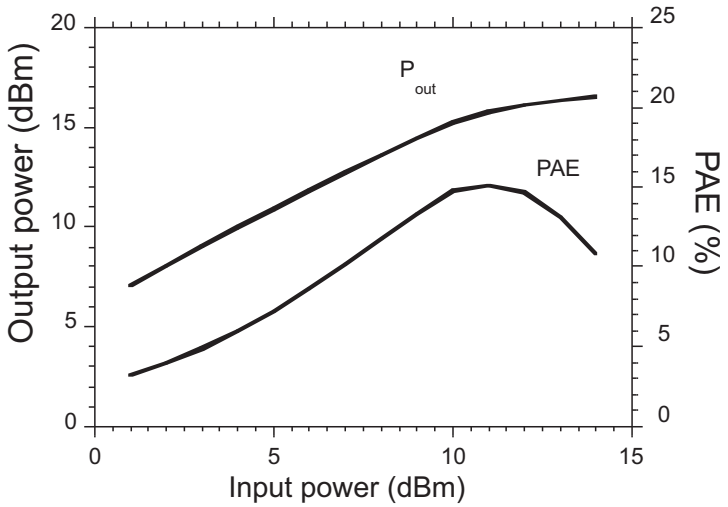

Figure 5.22: Simulated output power and PAE vs. input power of the 165 GHz single-stage amplifier

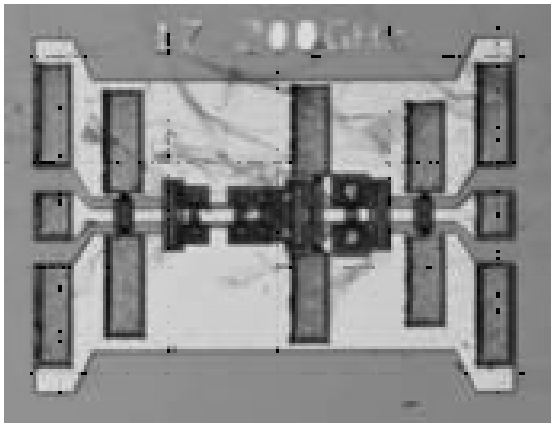

Figure 5.23: Die photograph of a 165 GHz amplifier.

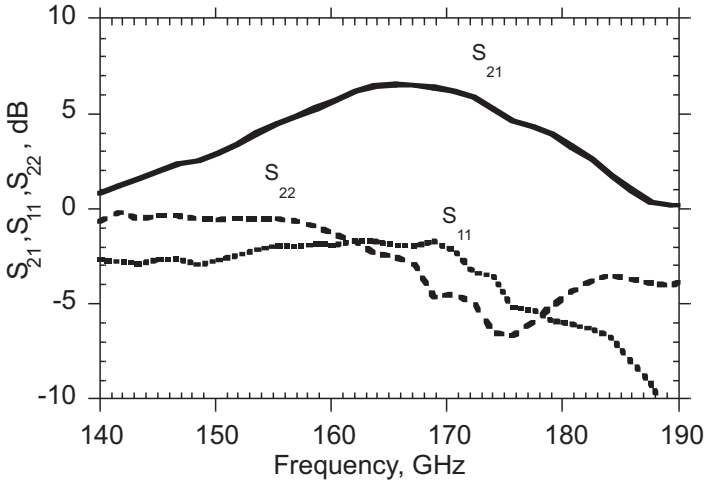

Figure 5.24: Measured S-parameters of a 165 GHz single-stage amplifier shown in Fig. 5.24

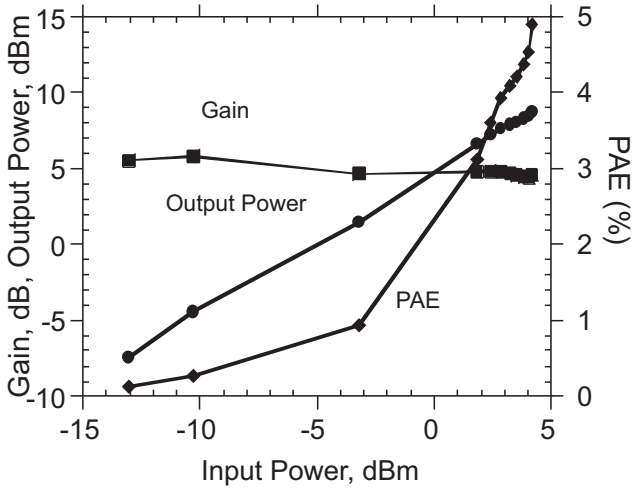

Figure 5.25: Measured output power and PAE vs. input power at 172 GHz of the 165 GHz single-stage amplifier shown in Fig. 5.23

5.3.3 176 GHz Two-stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.26. The transistor used in each of the two stages has two separate 0.8 μm$\times$12 μm fingers. Input match is designed to have wide bandwidth by employing a two fold L-matching network. The amplifier bandwidth is limited by the output tuning network. The amplifier is biased using off-wafer bias-Tees at the input and the output. The input and output probe pads are also included in the circuit simulation. This circuit is simulated with 7 dB small-signal gain at 170 GHz (Fig. 5.27) with 40 GHz 3-dB bandwidth. Maximum saturated output power of 16.5 dBm is simulated at 170 GHz (Fig. 5.28). These simulations are performed when the transistors in each of the two stages are biased at I_c = 30 mA and V_{cb} = 2.6 V.

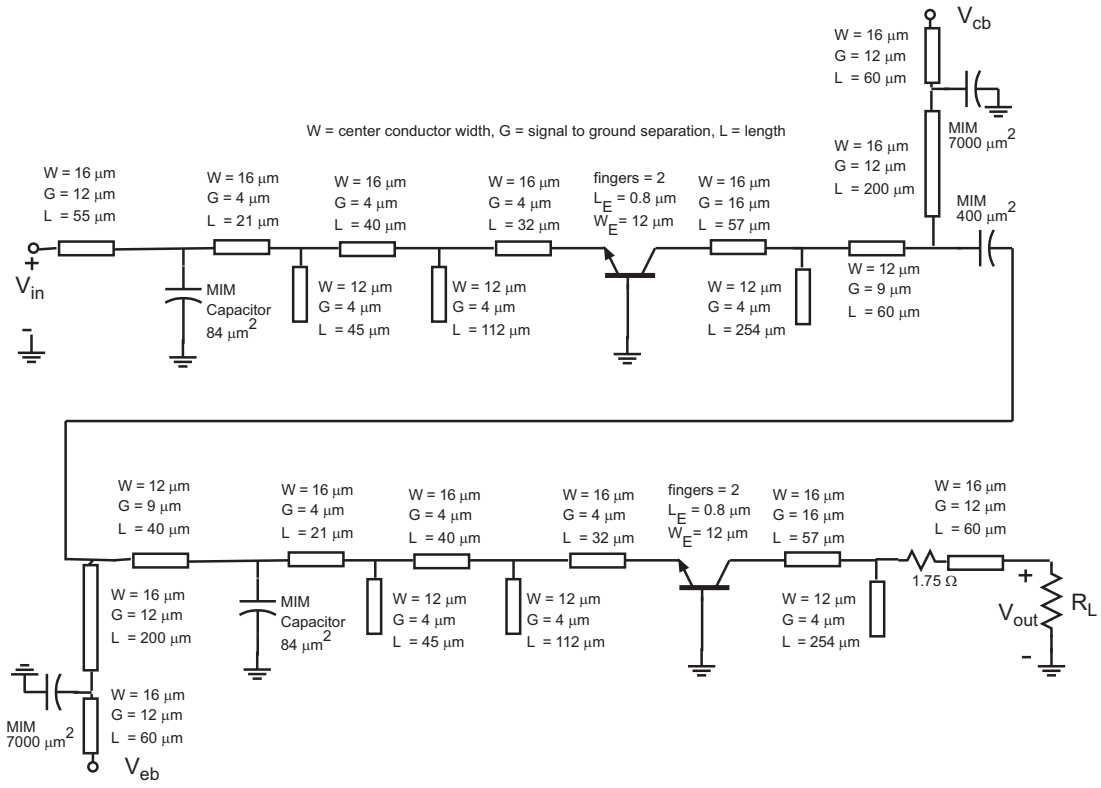

Figure 5.26: Schematic of the 176 GHz two-stage amplifier

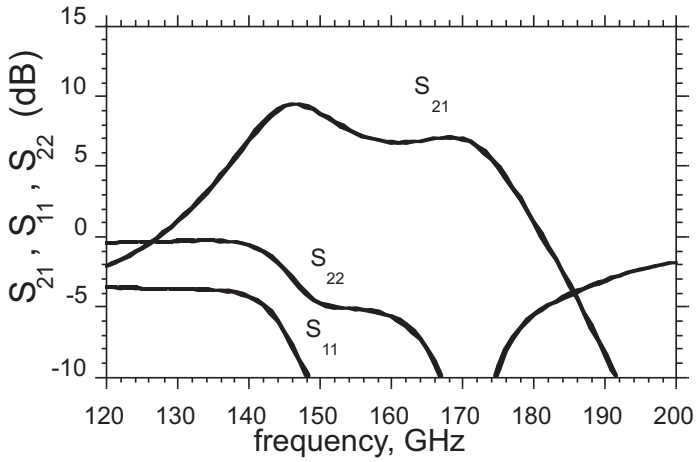

Figure 5.27: Simulated S-parameters of the 176 GHz two-stage amplifier

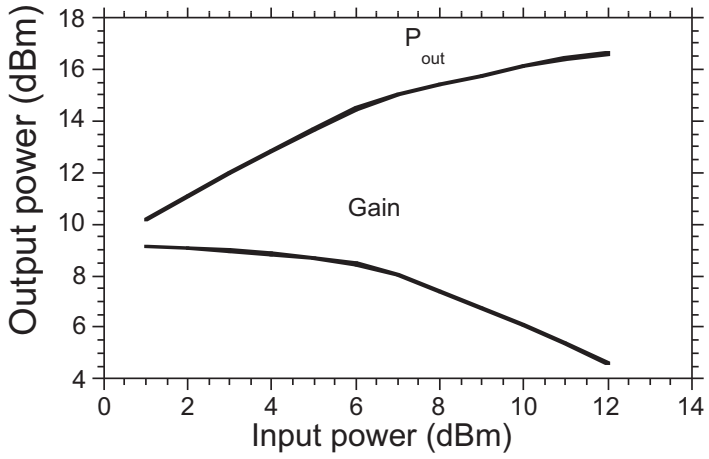

Figure 5.28: Simulated output power and gain vs. input power of the 176 GHz two-stage amplifier

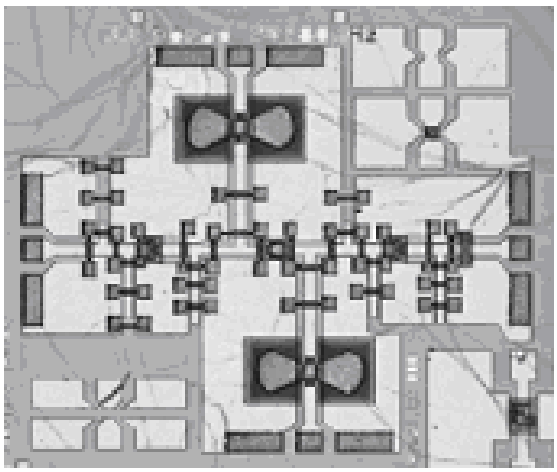

Figure 5.29: Die photograph of a 176 GHz two-stage MMIC amplifier. This measures 1 mm $\times$ 0.7 mm

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Measurements

A die photograph is shown in Fig. 5.29. This amplifier is a cascaded version of two individual amplifiers designed for 50 Ω input resistance and 50 Ω load. Each stage employs two separate 0.8 μm$\times$12 μm HBT fingers. The small-signal measurements are performed with the first stage biased at I_c = 25 mA and V_{cb} = 1.0 V and the second-stage biased at I_c = 30 mA and V_{cb} = 1.0 V. Small-signal measurements indicate 7-dB gain at 176 GHz and 13-dB gain at 150 GHz. There is a potential instability in S_{22} in 140-150-GHz range (Fig. 5.30).

This amplifier exhibited 8.1 dBm output power with 6.35-dB associated power

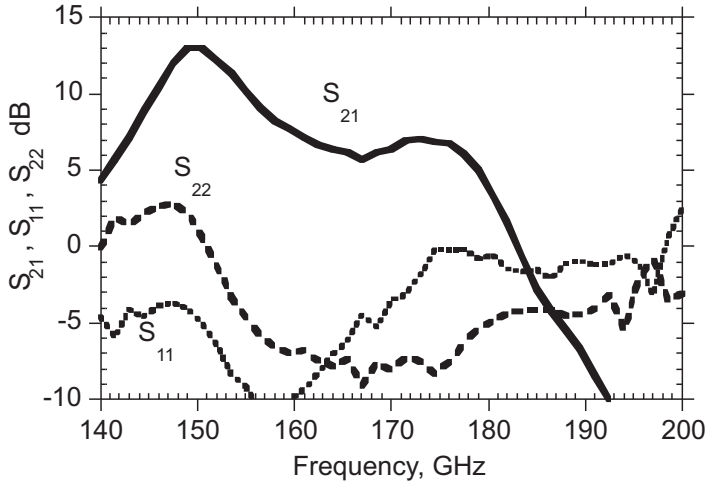

Figure 5.30: Small-signal measurements of the 176 GHz two stage amplifier shown in Fig. 5.29

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gain at 176 GHz and demonstrated 9.1 dBm saturated output power (Fig. 5.31). These measurements are performed with the first-stage is biased at I_c = 45 mA and V_{cb} = 2.05 V and the second-stage biased at I_c = 49 mA and V_{cb} = 1.84 V. At 150.2 GHz, the power amplifier exhibited 10.3 dBm output power with 3.4-dB associated power gain (Fig. 5.32). The first-stage is then biased at I_c = 40 mA and V_{cb} = 2.04 V and the second-stage is biased at I_c = 51 mA and V_{cb} = 2.11V. Uncompressed gain at 150.2 GHz is 9.2-dB.

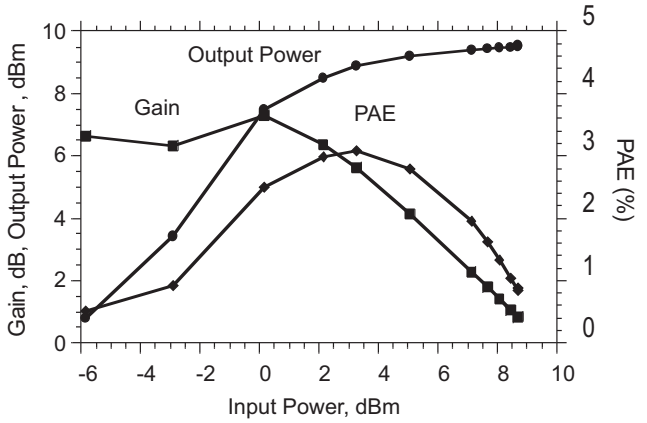

Figure 5.31: Power measurements of the 176 GHz two-stage amplifier at 176 GHz (Fig. 5.29)

5.3.4 150 GHz Two-stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.33. The transistor used in each of the two stages has two separate 0.8 μm $\times$12 μm fingers. The amplifier is biased using off-wafer bias-Tees at the input and the output. Input and output probe pads are also included in the circuit simulation. This circuit is simulated with 9.2 dB small-signal gain at 183 GHz (Fig. 5.34) with 30 GHz 3-dB bandwidth. Maximum saturated output power of 16.8 dBm is simulated at 183 GHz (Fig. 5.28). These simulations are performed when the transistors in each of the two stages are biased at I_c = 30

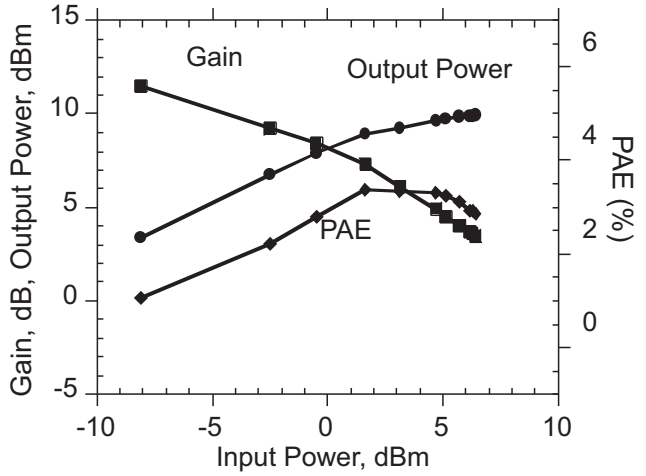

Figure 5.32: Power measurements of the 176 GHz two-stage amplifier at 150.2 GHz (Fig. 5.29)

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mA and V_{cb} = 2.6 V.

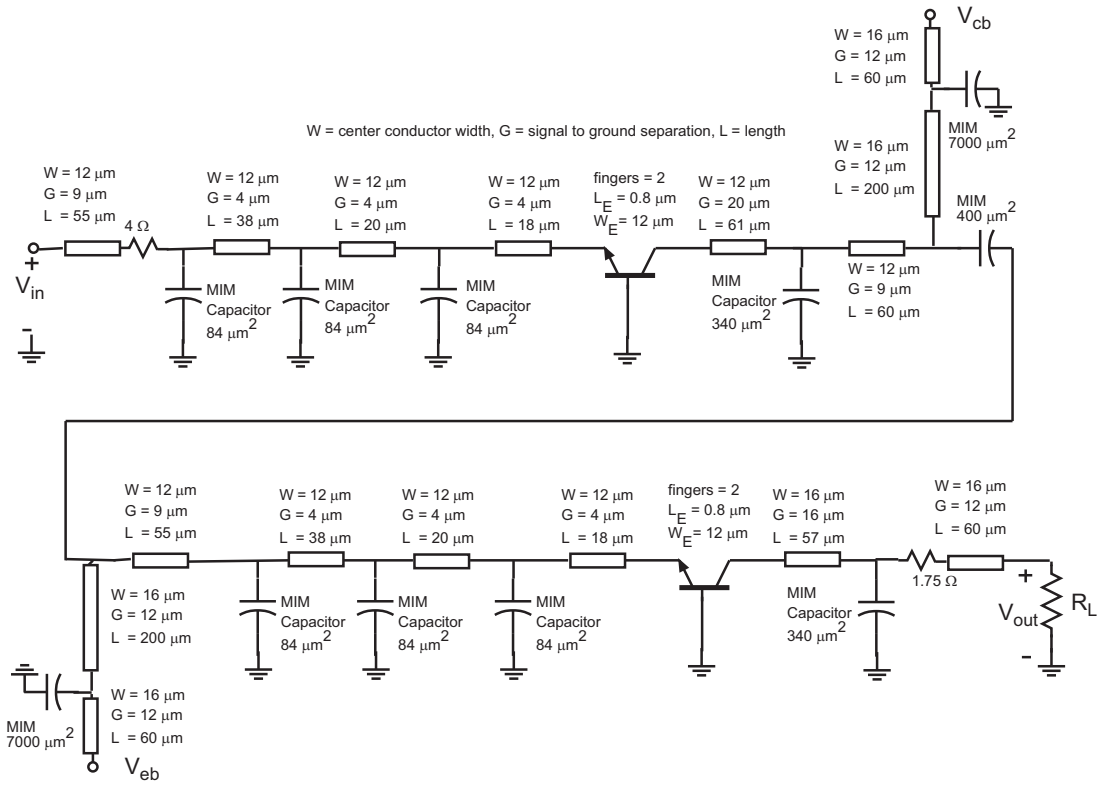

Figure 5.33: Schematic of the 150 GHz two-stage amplifier

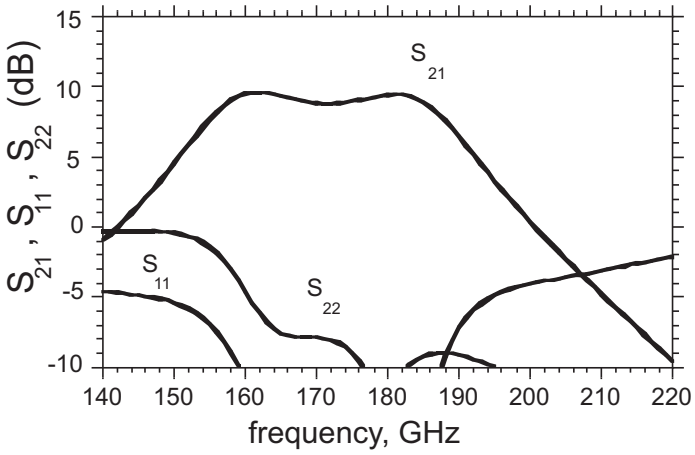

Figure 5.34: Simulated S-parameters of the 150 GHz two-stage amplifier

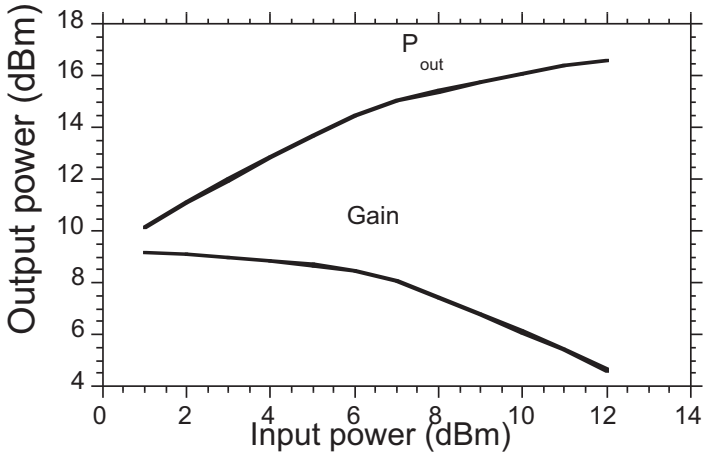

Figure 5.35: Simulated output power and gain vs. input power of the 150 GHz two-stage amplifier

Measurements

This two-stage amplifier (Fig. 5.36) exhibited 10-dB gain at 150 GHz with the first stage is biased at I_c = 30 mA and V_{cb} = 1.0 V and the second stage biased at I_c = 20 mA and V_{cb} = 1.0 V (Fig. 5.37). This two-stage amplifier demonstrated 11 dBm output power at 150.2 GHz with 4.2-dB associated power gain (Fig. 5.38). At 148 GHz, 11.6 dBm saturated output power is obtained with an associated power gain of 4.5 dB. These power measurements are performed with the first-stage biased at I_c = 43 mA and V_{cb} = 2.0 V, and the second-stage biased at I_c = 49 mA and V_{cb} = 2.07 V.

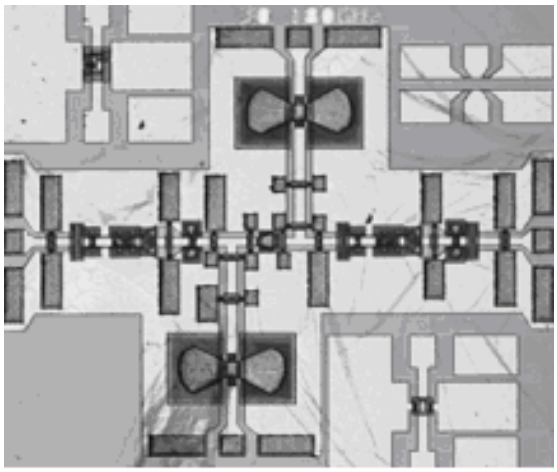

Figure 5.36: Die photograph of a 150 GHz two-stage MMIC amplifier

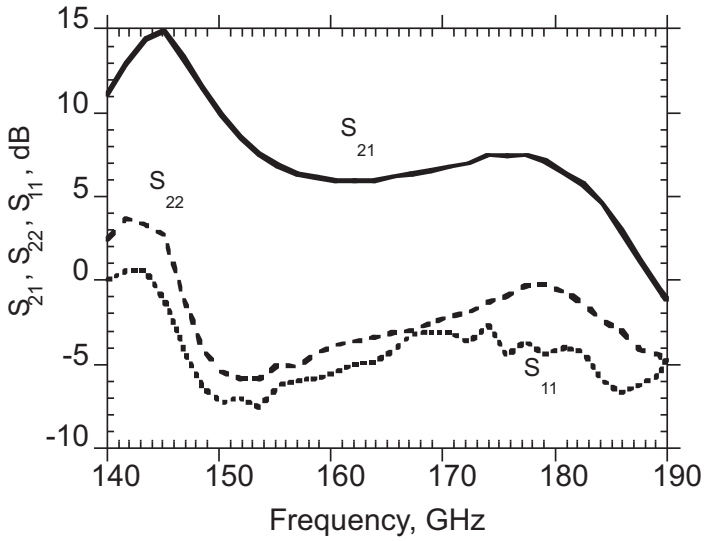

Figure 5.37: Small-signal measurements of the 150 GHz two-stage amplifier shown in Fig. 5.36

5.3.5 Another 150 GHz two-stage Amplifier

Simulations

Simulations for this amplifier are already discussed in Chapter 4.5.2. Recall that this amplifier simulated with 100 mW output power with 8.7-dB uncompressed power gain at 180 GHz.

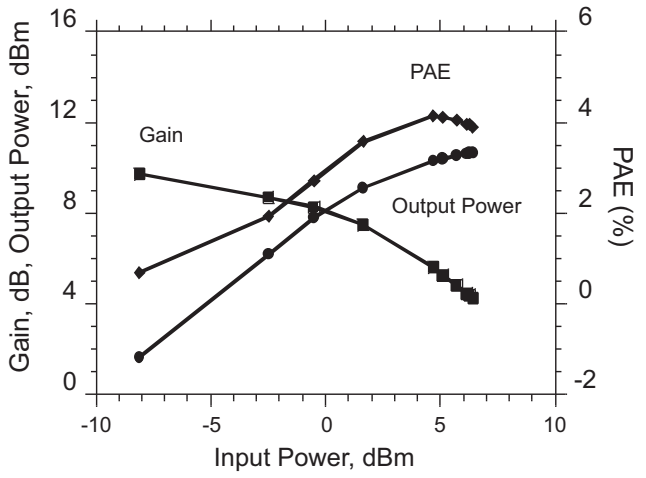

Figure 5.38: Measured power measurements of the 150 GHz two-stage amplifier shown in Fig. 5.36

Measurements

This two-stage amplifier (Fig. 5.39) exhibited 10-dB gain at 150 GHz with the first stage is biased at I_c = 28 mA and V_{cb} = 1.0 V and the second stage biased at I_c = 58 mA and V_{cb} = 1.0 V (Fig. 5.40). This two-stage amplifier demonstrated 11.2 dBm output power at 150.2 GHz with 4-dB associated power gain (Fig. 5.41). These power measurements are performed with the first-stage biased at I_c = 43 mA and V_{cb} = 2.0 V, and the second-stage biased at I_c = 92 mA and V_{cb} = 2.15 V.

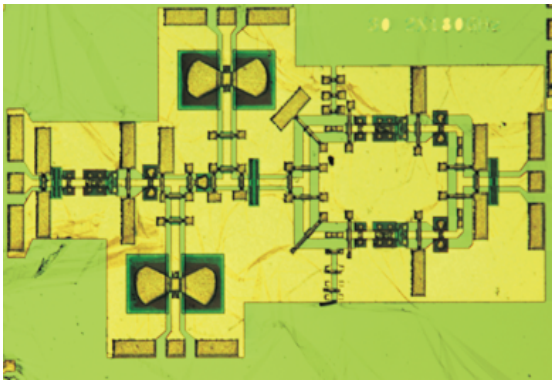

Figure 5.39: Die photograph of a 150 GHz two-stage MMIC amplifier designed with 100 mW output power

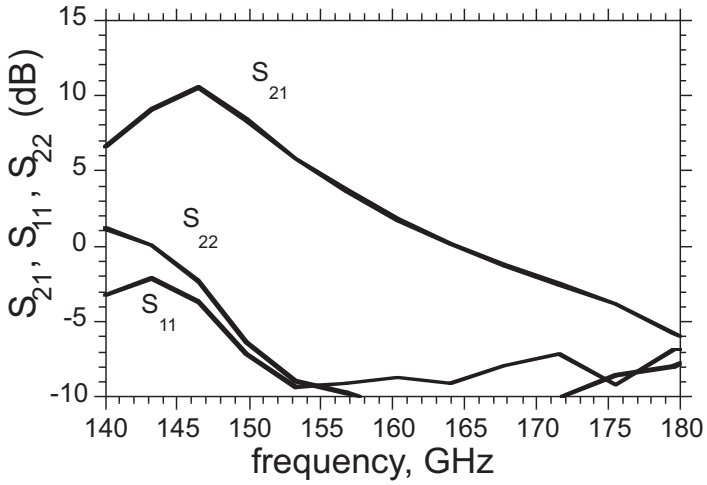

Figure 5.40: Small-signal measurements of the 150 GHz two-stage amplifier of Fig. 5.39

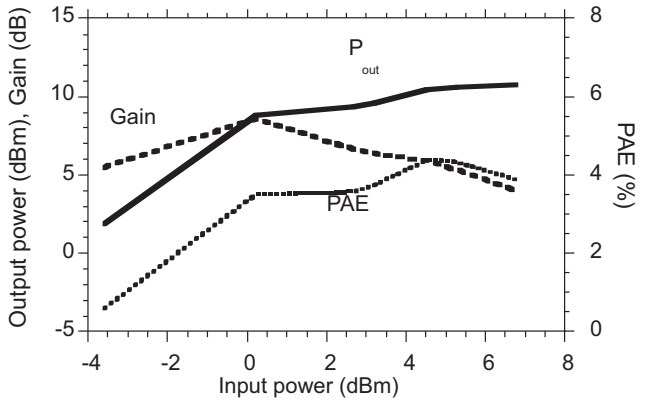

Figure 5.41: Power measurements of the 150 GHz two-stage amplifier shown in Fig. 5.39

5.3.6 84 GHz Single-stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.42. The transistor used in this circuit has four separate 0.8 μm $\times$12 μm fingers. The transistor output is large-signal load-line matched for maximum saturated output power. Input and output probe pads are also included in the circuit simulation. This circuit is simulated with 8.5 dB small-signal gain at 93 GHz (Fig. 5.43) with 25 GHz 3-dB bandwidth. Maximum saturated output power of 20 dBm is simulated at 93 GHz (Fig. 5.44). These simulations are

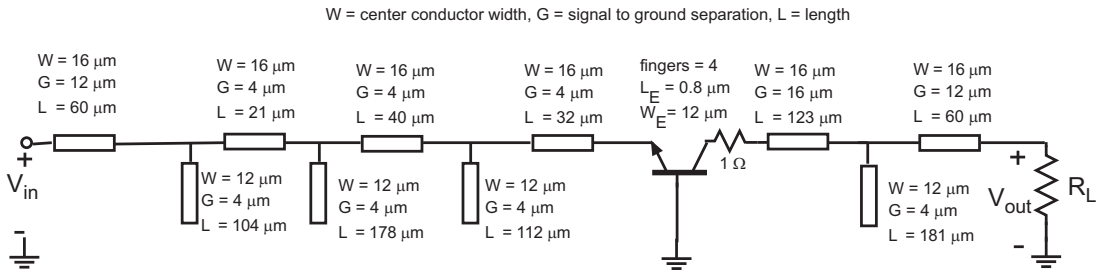

Figure 5.42: Schematic of the 84 GHz single-stage amplifier

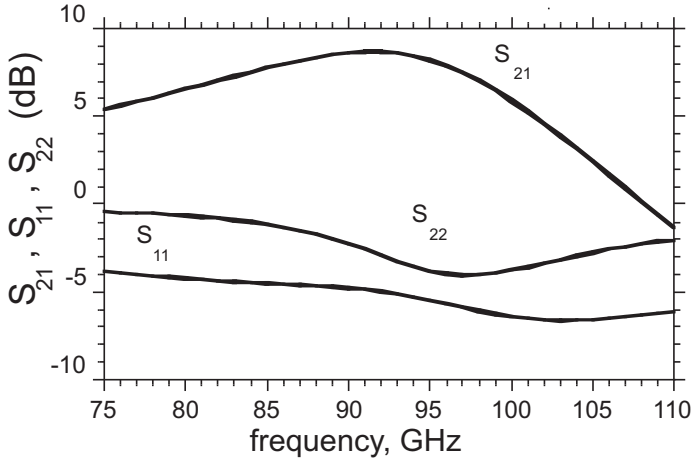

Figure 5.43: Simulated S-parameters of the 84 GHz single-stage amplifier

performed when the transistor is biased at I_c = 60 mA and V_{cb} = 2.6 V.

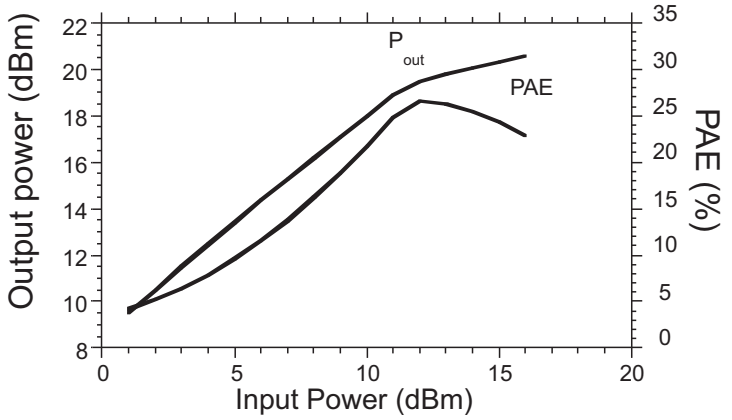

Figure 5.44: Simulated output power and PAE vs. input power of the 84 GHz single-stage amplifier

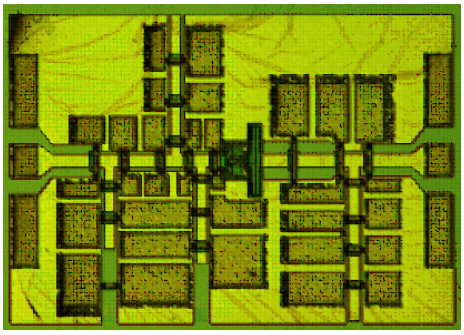

Figure 5.45: Die photograph of a 84 GHz single-stage amplifier

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Measurements

A single-stage amplifier (Fig. 5.45) exhibited 5.6-dB small signal gain at 84 GHz (Fig. 5.46) when biased at I_c = 37 mA and V_{cb} = 1.0 V. The transistor has four separate 0.8 μm $\times$12 μm fingers. This circuit demonstrated 15.1 dBm saturated output power at 84 GHz with $>$4-dB associated power gain (Fig. 5.47).

5.3.7 92 GHz Single-stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.48. The transistor used in this circuit has four separate 0.8 μm $\times$12 μm fingers. The transistor output is large-signal load-line

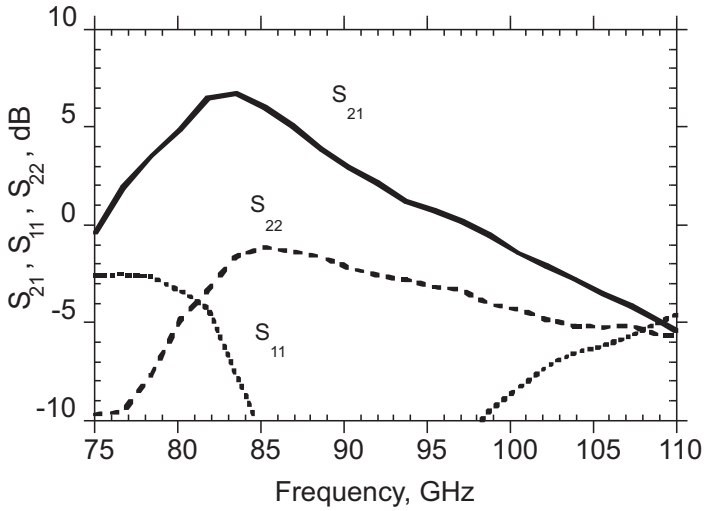

Figure 5.46: Small-signal measurements of the 84 GHz amplifier shown in Fig. 5.45

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matched for maximum saturated output power. Input and output probe pads are also included in the circuit simulation. This circuit is simulated with 7.1 dB small-signal gain at 103 GHz (Fig. 5.49) with 35 GHz 3-dB bandwidth. Maximum saturated output power of 19.5 dBm is simulated at 103 GHz (Fig. 5.50). These simulations are performed when the transistor is biased at I_c = 60 mA and V_{cb} = 2.6 V.

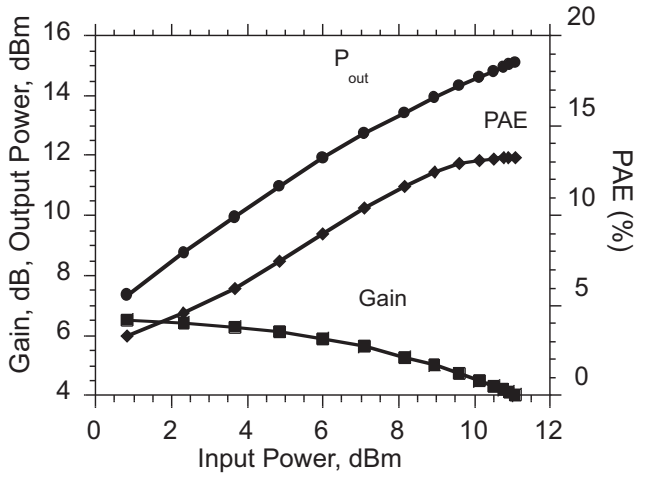

Figure 5.47: Power measurements of a 84 GHz amplifier shown in Fig. 5.45

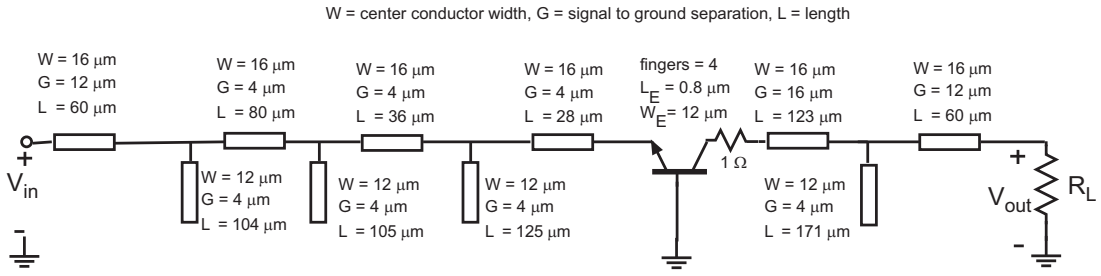

Figure 5.48: Schematic of the 92 GHz single-stage amplifier

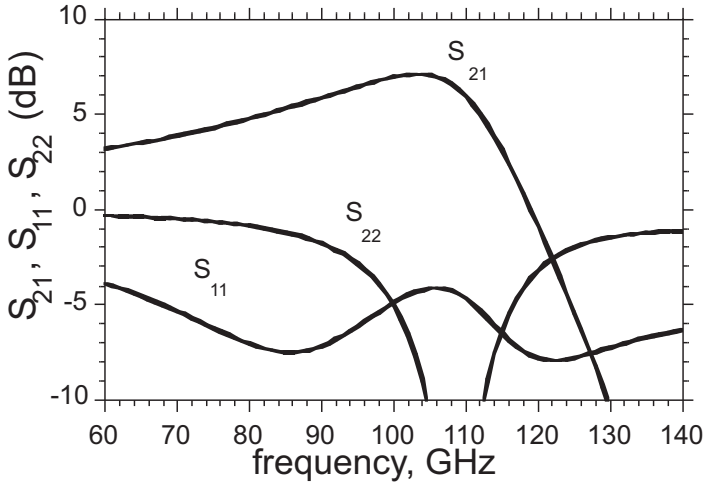

Figure 5.49: Simulated S-parameters of the 92 GHz single-stage amplifier

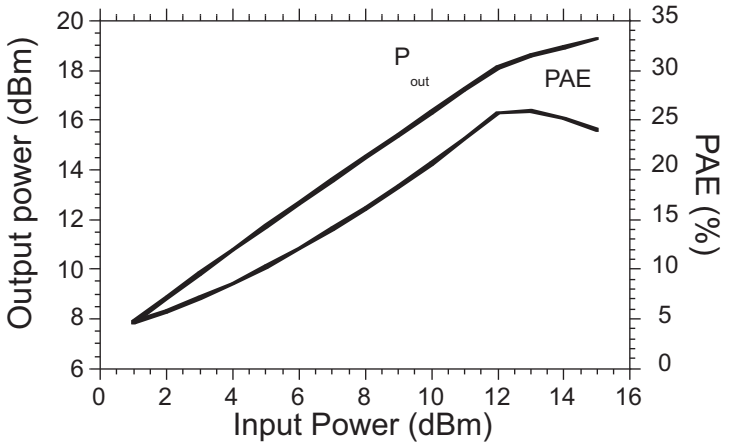

Figure 5.50: Simulated output power and PAE vs. input power of the 92 GHz single-stage amplifier

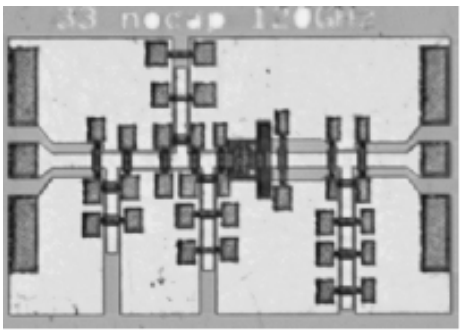

Figure 5.51: Die photograph of a 92 GHz single stage amplifier

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Measurements

This common-base amplifier (Fig. 5.51) exhibited 5-dB small-signal gain at 92 GHz when biased at I_c = 39 mA and V_{cb} = 1.0 V (Fig. 5.52). This amplifier demonstrated 13.7 dBm saturated output power at 93 GHz (Fig. 5.53) when biased at I_c = 46 mA and V_{cb} = 2.25 V.

5.3.8 110 GHz Single-stage Amplifier

Simulations

The circuit schematic is shown in Fig. 5.54. The transistor used in this circuit has two separate 0.8 μm $\times$12 μm fingers. The transistor output is large-signal load-line

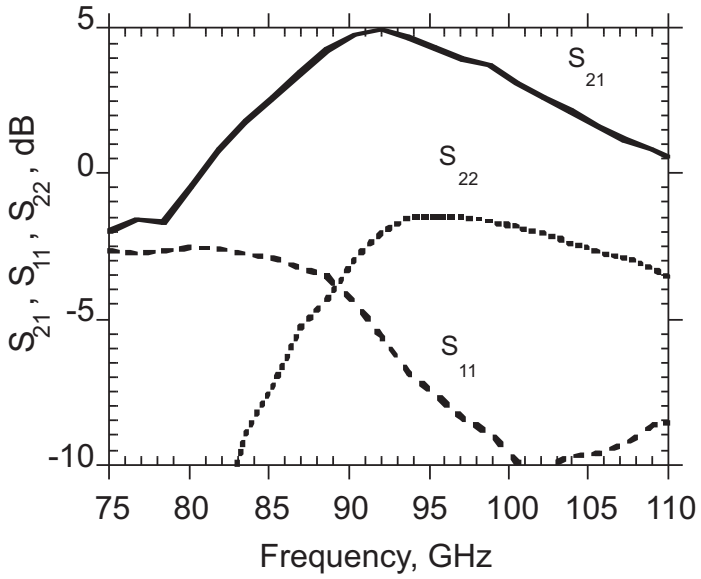

Figure 5.52: Small-signal measurements of 92 GHz amplifier shown in Fig. 5.51

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matched for maximum saturated output power. Input and output probe pads are also included in the circuit simulation. This circuit is simulated with 7.5 dB small-signal gain at 123 GHz (Fig. 5.55) with 45 GHz 3-dB bandwidth. Maximum saturated output power of 17 dBm is simulated at 123 GHz (Fig. 5.56). These simulations are performed when the transistor is biased at I_c = 30 mA and V_{cb} = 2.6 V.

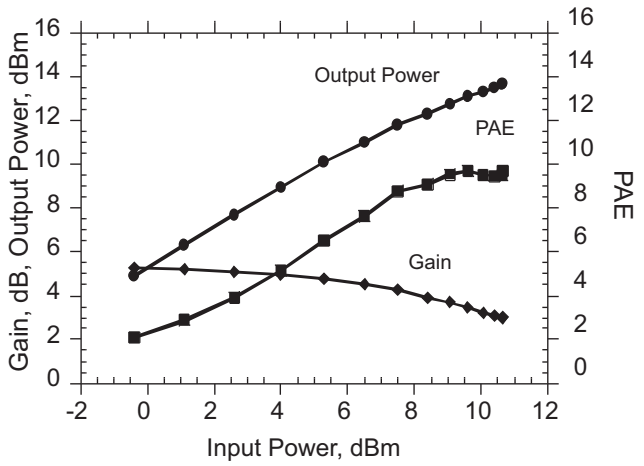

Figure 5.53: Power measurements of the 92 GHz amplifier at 93 GHz shown in Fig. 5.51

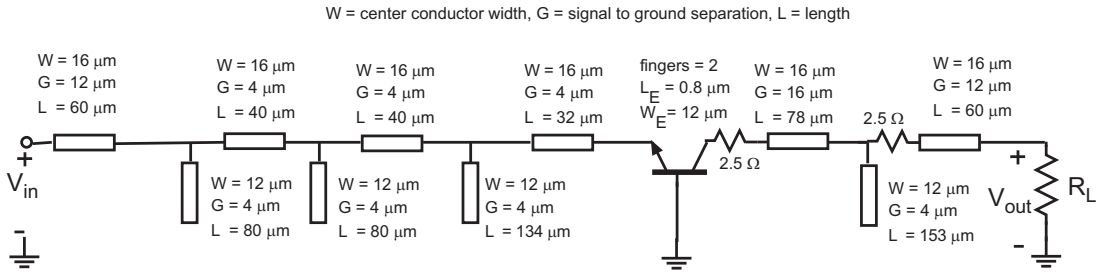

Figure 5.54: Schematic of the 92 GHz single-stage amplifier

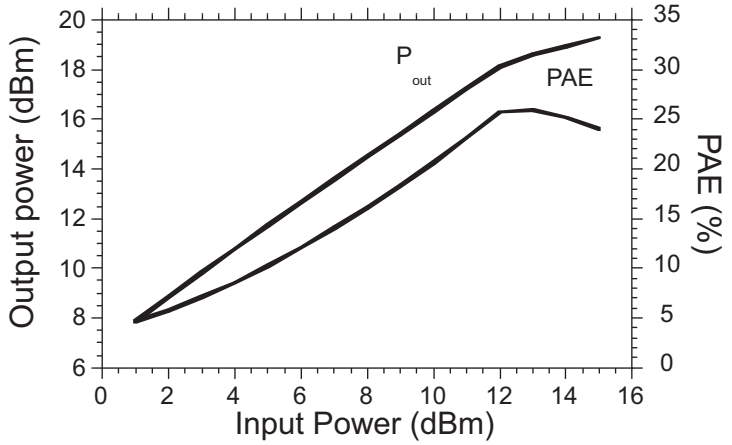

Figure 5.55: Simulated S-parameters of the 92 GHz single-stage amplifier

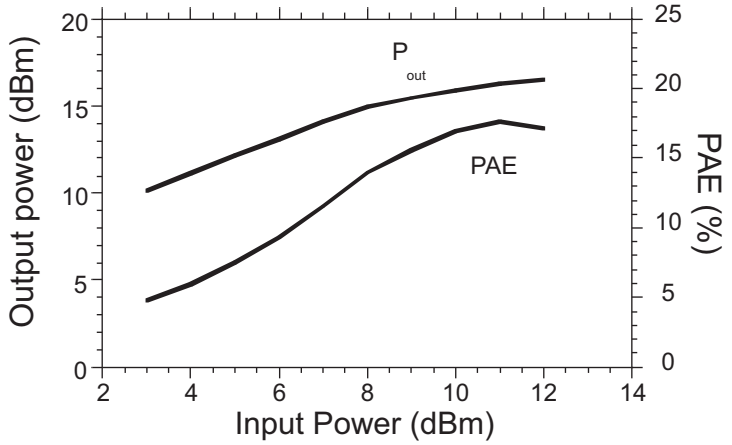

Figure 5.56: Simulated output power and PAE vs. input power of the 92 GHz single-stage amplifier

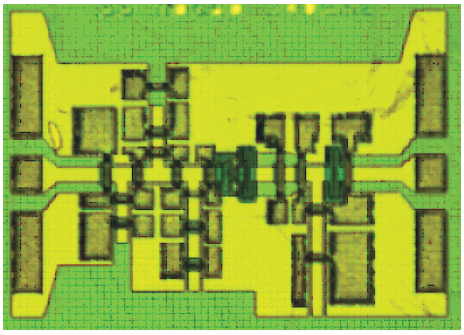

Figure 5.57: Die photograph of a 110 GHz single-stage amplifier

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Measurements

This common-base amplifier design (Fig. 5.57) exhibited 4.5-dB small-signal gain at 110 GHz when biased at I_c = 37 mA, V_{cb} = 1.0 V (Fig. 5.58). This design employed an InP DHBT that consists of two separate 0.8 μm$\times$12 μm fingers. This amplifier demonstrated 10.2 dBm of saturated output power at 109.8 GHz (Fig. 5.59) when biased at I_c = 45 mA and V_{cb} = 2.0 V. This circuit is originally designed to operate at 125 GHz. From Fig. 5.58, it is clear that power gain is increasing with frequency at 109.8 GHz showing that there is potential for this circuit to exhibit higher gain and output power beyond 109.8 GHz.

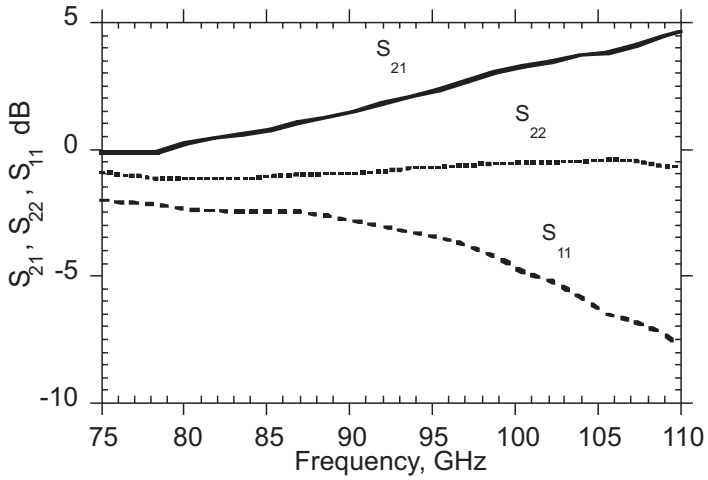

Figure 5.58: Small-signal measurements of 110 GHz amplifier shown in Fig. 5.57

References

[1] M. Dahlstrom, et al., "InGaAs/InP DHBTs with >370 GHz and using a Graded Carbon-Doped base", *2003 IEEE Device Research Conference* Salt Lake City, UT, June 23-25, 2003, Late news submission.

[2] M. Dahlstrom, "Ultra High Speed InP Heterojunction Bipolar Transistors", *Doctoral Dissertation*, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden.

[3] Y. Wei, M. Urteaga, Z. Griffith, D. Scott, S. Xie, V. Paidi, N. Parthasarathy, M. J. W. Rodwell "75 GHz, 80 mW InP DHBT power amplifier", *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 919-921, Philadelphia, PA, June 2003.

[4] Y. Wei, S. Krishnan, M. Urteaga, Z. Griffith, D. Scott, V. Paidi, N. Parthasarathy, M. J. W. Rodwell "40 GHz MMIC Power amplfiers in InP DHBT Technology", *IEEE Lester Eastman Conference on High Performance Devices*, Newark, Delaware, August 2002.

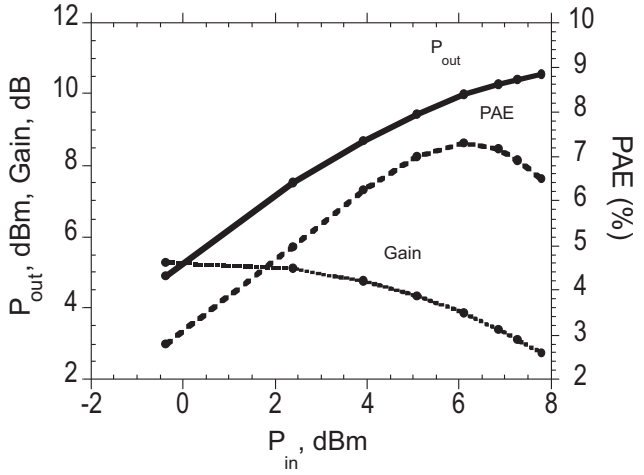

Figure 5.59: Power measurements of the single-stage Common-base power amplifier at 109.8 GHz (Fig. 5.57)

6 Conclusions and Future Work

In this chapter, the achievements of GaN HEMT power amplifier work and InP DHBT power amplifier work are summarised and improvements to the present work are suggested.

6.1 Conclusions on GaN HEMT Power Amplifier Work

For class B amplifiers with fractional bandwidth less than 2:1, the push-pull configuration is unnecessary and can be replaced by a single-ended configuration with output filtering. This avoids the difficulty of fabricating balun transformers with correct even-mode termination at microwave frequencies. If the HEMT transconductance is independent of gate bias above threshold, low IM_3 levels can be attained. The single-ended common-source class B amplifier has shown $>$35 dBc of IM_3 suppression at 8 GHz with approximately 34$\%$ PAE. The class B mode of operation can

have similar distortion at moderate and high output powers as that of class A if biased at V_{gs} = V_p, and can yield more than 10% improved PAE over class A. The common-drain class B power amplifier has lower distortion when compared to a common-source amplifier due to its integral negative feedback mechanism. However, the common-drain topology suffers from low power gain resulting in degradation of efficiency. Next generation GaN HEMTs with $>$150 GHz f_{max} could potentially be used to build common-drain power amplifiers with superior linearity and efficiency when compared to the common-source class B power amplifiers. Present GaN HEMTs [1] have demonstrated $>$30 W/mm of power density at 8 GHz and they are superior than those used in this work. Designing class B power amplifiers with modern HEMTs would result in power amplifiers with superior efficiency and linearity.

6.2 Conclusions on InP DHBT Power Amplifier Work

Common-base high-gain G-band and W-band power amplifiers in InP mesa DHBT technology are successfully designed and fabricated. A single-stage common-base tuned amplifier with 7-dB small-signal gain at 176 GHz exhibited 8.7 dBm output power with 5-dB associated power gain at 172 GHz. The common-base topology

provides the largest maximum stable gain. This configuration requires careful layout to minimize C_{ce} and L_b, or the maximum stable gain will be reduced. Despite large-signal loadline matching, the design values of gain remain high at 180 GHz, and close to the MSG. Power levels, efficiency and center frequency are below design values, an effect we attribute to modeling errors. Recent DHBTs have been reported at 459 GHz f_{max} [2], suggesting feasibility of power amplifiers at 250 GHz. Increasing the number of HBT fingers should result in power amplifiers with output power more than 100 mW. Multi-stage amplifiers should be employed so that high output power can be obtained with power sources with limited available power. Coplanar waveguide transmission lines are better modeled than MIM capacitors because the permittivity and thickness of SiN_x dielectric change from process to process. By designing tuning networks by using only transmission lines, sensitivity to mistuning is improved.

6.3 500 GHz Frequency Doubler Design

With $>$100 mW at 250 GHz, it should be feasible to fabricate frequency doublers with InP DHBTs in common-base topology to obtain power sources at 500 GHz. RADAR systems operating at frequency $>$500 GHz result in high resultion imaging.

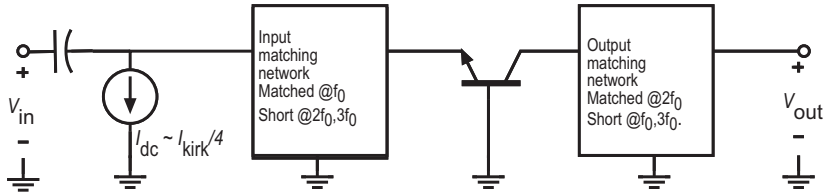

Figure 6.1: Circuit schematic of a 500 GHz frequency doubler

The simulations of an active frequency doubler fabricated in InP bipolar technology are shown below.

The frequency-doubler schematic is shown in Fig. 6.1. The common-base topology is used as it provides with the highest gain at these frequencies. The transistor is biased at 25% of the Kirk current. The input is driven to obtain a pulse shaped collector current waveform with approximately 25% duty cycle. A 25% duty cycle waveform has strong Fourier content at frequencies up to $2f_0$. This results in high conversion efficiency and the circuit doubles in frequency effectively. Transistor size is chosen to make sure that the maximum current is less than the Kirk threshold. Output is matched at $2f_0$ and the input is matched at f_0 to optimise for maximum gain (Fig. 6.2). V_{ce} is kept well below V_{br} under large-signal operation.

The InP DHBTs used in the simulations consist of four separate fingers of InP HBTs with 0.5 μm emitter width and 12 μm emitter length (mask). The transistors

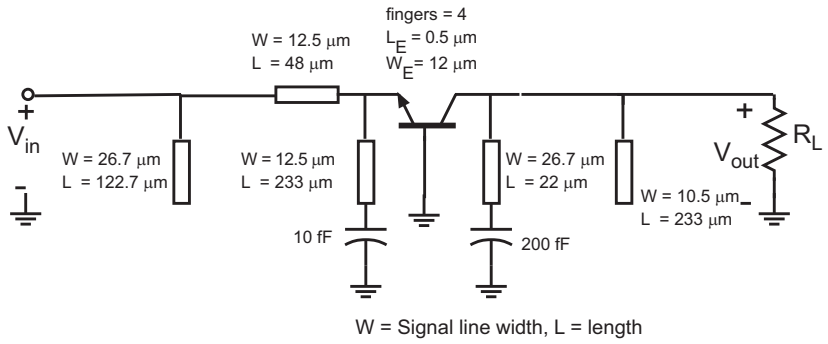

Figure 6.2: Detailed circuit diagram of a 500 GHz frequency doubler

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used in the simulations exhibit 400 GHz f_τ and 560 GHz f_{max}. Collector current and base to emitter voltage waveforms are shown in Fig. 6.3. The output power at 500 GHz as a function of input power is shown in Fig. 6.4. The maximum conversion efficiency when the input power is 20 dBm and output power is 13.5 dBm is 22%. The tuning elements used in these simulations are implemented by microstrip transmission lines which exhibit high attenuation at 500 GHz.

The results presented here demonstrate the potential of InP DHBT technology for high performance ultra-high-frequency sub millimeter-wave circuit applications.

References

[1] Y. Wu, et al., "30-W/mm GaN HEMTs by Field Plate Optimization", *2003 IEEE electron device letters*, vol. 25, no. 3, Marchc 2004.

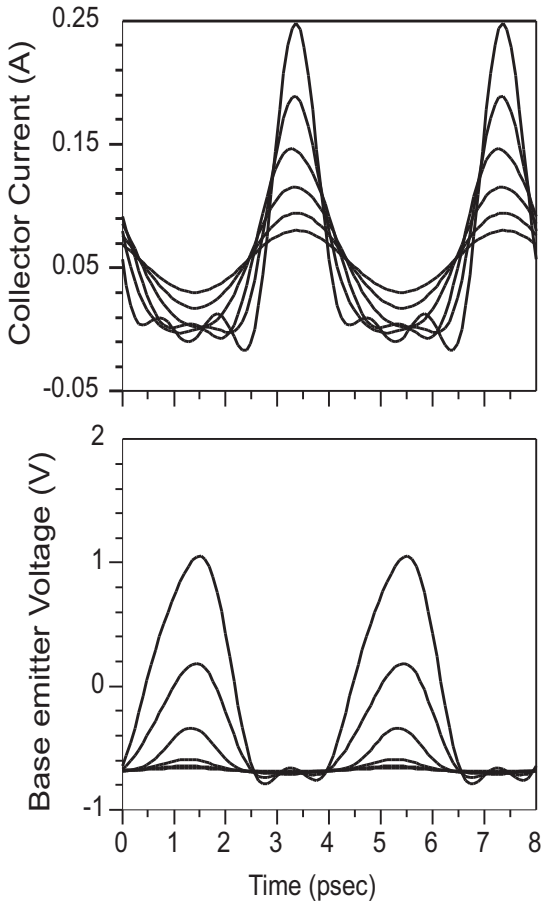

Figure 6.3: Collector current and base-emitter voltage of a 500 GHz frequency doubler

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[2] M. Dahlstrom, et al., "InGaAs/InP DHBTs with > 370 GHz and using a Graded Carbon-Doped base", *2003 IEEE Device Research Conference* Salt Lake City, UT, June 23-25, 2003, Late news submission.

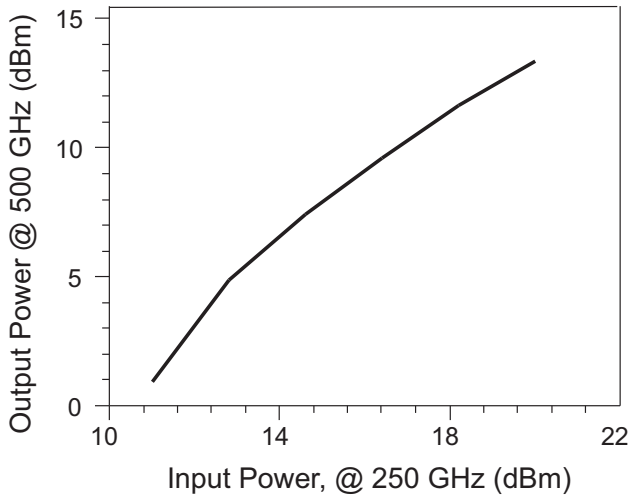

Figure 6.4: Output power at 500 GHz vs. input power at 250 GHz of the frequency doubler