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In0.53Ga0.47As MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth

A Dissertation submitted in partial satisfaction
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by

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To mom, dad, sister and brother

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Abstract

In0.53Ga0.47As MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth

Uttam Singisetti

InGaAs has been extensively studied as a potential channel material for sub-22nm gate length VLSI MOSFETs because of its low electron effective mass (m^*) hence high electron velocity (υ). At 22 nm gate lengths, a maximum 1 nm EOT dielectric and 5 nm thick channel with strong vertical confinement are required for low subthreshold swing and low drain induced barrier lowering (DIBL). Most reported InGaAs MOSFETs and HEMTs have typically $\geq$ 10 nm channel thickness. The source/drain (S/D) junctions must be very shallow ($\sim$ 5 nm) with abrupt vertical and lateral profiles, yet extremely low ($\sim$ 50 $\Omega - \mu m$) source access resistance and consequently very low ($\sim$ 1 $\Omega - \mu m^2$) contact and ($\sim$ 400 $\Omega/\square$) sheet resistivities are required to minimize degradation of the drive current (I_d) and transconductance (g_m). Such parameters are difficult to achieve in InGaAs by ion implantation of the n^+ source/drain, particularly if an InAlAs bottom confinement layer is used. Source/drain contacts must also be self-aligned to the gate, yet there is no known equivalent of self-aligned silicides in III-V materials. This dissertation addresses these requirements and shows InGaAs MOSFETs with

self-aligned S/D access regions and self-aligned metal contacts formed by MBE regrowth and in-situ metal deposition.

A scalable all dry etch gate process with minimal damage to thin channel layers was developed. A *ex-situ* and *in-situ* clean of the wafer leaves a contamination free channel surface suitable for epitaxial regrowth. Self-aligned source/drain regions were defined by MBE regrowth. Self-aligned *in-situ* Mo contacts were defined by 25 nm SiN_x sidewalls and a height selective etch. MOSFETs were demonstrated with this process with $\sim$ 5 nm channel. The source/drain regrowth process is optimized and an InAs source/drain regrowth process was developed. The 200 nm L_g device showed 0.7 $mA/\mu m$ peak drive current at $V_{gs} = 4.0\ V$ and $V_{ds} = 1.0\ V$ with 2.5 nm EOT and has an on resistance of 600 $\Omega - \mu m$. The technology shows the potential to scale to sub-22nm gate lengths.

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Chapter 1

Introduction

Silicon based CMOS devices have continued to scale as predicted by Moore's Law and have reached 32 nm L_g in production technology with 11 billion transistors per μm^2 of Si [1, 2]. This has been possible mainly because of continuous scaling the gate dielectric capacitance or equivalent oxide thickness (EOT) along with the gate length. The EOT has been scaled to 0.9 nm using hafnia high-k dielectric. Scaling the device increases the operation frequency and at the same time decreases the cost because of increased package density. This leads to an increased circuit functionality at lower cost. Using novel Tri-gate device structure, gate lengths can be further scaled to 22 nm [3]. But continued difficulties in scaling EOT to below 1 nm necessitates investigation of alternative III-V channel materials as possible replacement to Si [4, 5]. $In_{0.53}Ga_{0.47}As$ with a low electron effective mass (m^*) and large inter-valley separation is a promising channel material.

This chapter give a brief introduction to Si MOSFET scaling and motivation for InGaAs MOSFETs.

1.1 Si MOSFET Scaling

As the gate length (L_g) of the devices are scaled down for increased package density the gate dielectric must also be scaled down to keep two-dimensional (2-D) electrostatic integrity. The increased gate capacitance ($c_{ox} \propto \frac{1}{t_{ox}}$) induces higher electron or hole charge ($n \propto c_{ox}(V_{dd} - V_{th})$) in the channel if the supply voltage V_{dd} is kept constant. This increased charge translates to higher drive currents and consequently lower circuit delay (τ). An expected outcome of the scaling is increased switching power density $P_{SW} \sim C_{SW}V_{dd}^2/\tau$. Another undesirable outcome of the scaling is the increase in the standby or passive power density.

The passive power density is given by $P_{off} \sim W_{total}V_{dd}I_0 \exp(-qV_t/mkT)$, where I_0 is the drain current at the threshold voltage, and m is the dimensionless ideality factor which depends on the 2-D electrostatics of the device [7]. As the SiO_2 thickness or EOT is scaled with gate length, the leakage current $I_0 \propto C_{ox}$ is also increased. Other sources of I_{off} in scaled MOSFETs are gate to channel tunneling currents, subthreshold channel currents, source to drain tunneling currents, and defect induced channel currents. As seen in Fig. (1.1) the standby

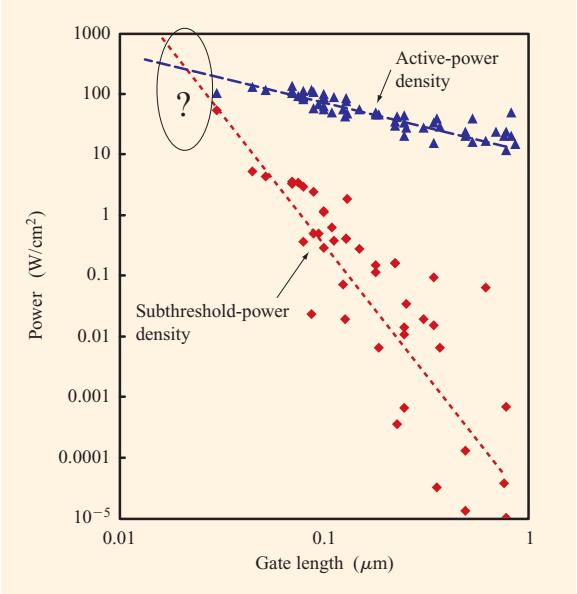


Figure 1.1: Calculated active power density and subthreshold power density for various gate lengths [6].

power density increases more rapidly than the switching power density vastly increasing the chip power consumption [6]. The gate tunneling leakage currents can be reduced by using a high-k dielectric material. Using high-k dielectric enables to decrease the EOT but at the same time physical thickness of the dielectric is large enough to avoid tunneling effects.

The subthreshold currents are more fundamental and cannot be improved by changing the material. The electrons from source are injected to the channel through thermionic emission over the barrier (Fig. 1.2) giving 60 mV/decade as the absolute theoretical limit to the subthreshold slope ($S \sim (\partial\theta_b/\partial V_g)^{-1}$). The subthreshold swing also depends on the electrostatic integrity of the device. If the

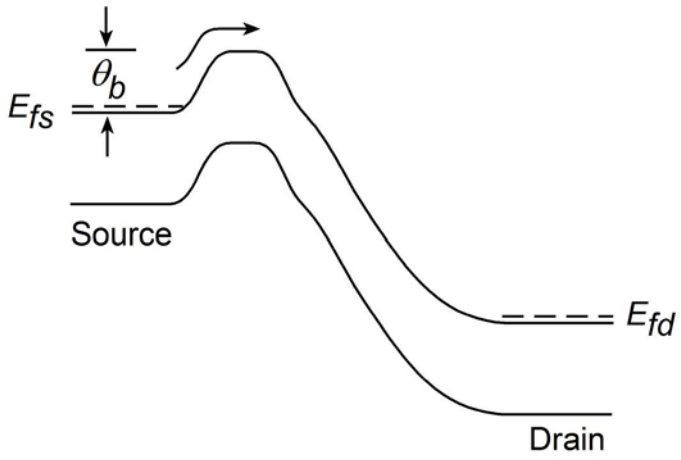


Figure 1.2: Thermionic emission of electrons over the barrier θ_b determines the current.

oxide or EOT does not scale at the same rate as the gate length then the the drain modulation of channel ($\partial\theta_b/\partial V_d$) increases degrading the subthreshold slope. Use of double gate transistor structure can improve the short channel effects as the gate is coupled strongly to the channel, but complicates the device fabrication process.

Si MOSFETs have implemented high-k dielectric and metal gate to scale the gate length to 32 nm with an EOT of 0.9 nm. And use of Tri-gate structure may further scale the gate length to 22 nm [3]. However a thin interfacial silicon oxide layer($\sim$ 6Å) [2, 8] is usually present below the high-k dielectric (Fig. (1.3)) in order to have a low D_{it} and minimize the channel mobility degradation. This interfacial layer makes makes it difficult to scale the gate dielectric to (EOT)

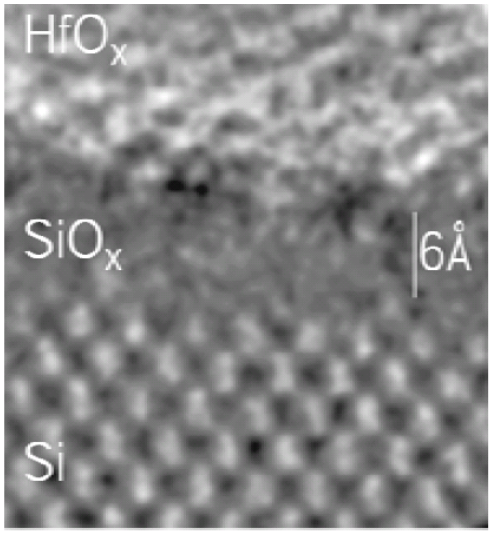


Figure 1.3: High resolution transmission electron microscope image of high-k dielectric on Si shwing the presence of thin silicon dioxide layer [2]

< 0.5 nm; required for beyond 22 nm L_g [9]. This may limit the Si MOSFET scaling. Another possible roadblock to scaling is the parasitic source resistance. The source access resistance and junction depth must also scale with gate length. An extremely low source access resistance of $150\ \Omega - \mu$m and a ultra shallow junction depths of ~ 6 nm is required for 22 nm L_g devices; these have no known solutions according to the ITRS 2008 Roadmap [9]. In this possible scenario, use of an alternative channel material with higher electron velocities may give higher performance at the same EOT scaling generation. $In_xGa_{1-x}As$ ($x \geq 0.53$) is a promising alternative channel material because of the experimentally observed high electron velocities in HEMTs [10, 11]. Besides the high electron velocity,

extremely low contact resistance to InGaAs has been realized, making it possible to achieve the low source access resistance in scaled MOSFETs.

In this thesis, we explore a $In_{0.53}Ga_{0.47}As$ channel MOSFET with scaled channel having $In_{0.48}Al_{0.52}As$ bottom confinement layer and Al_2O_3 high-k dielectric. The devices have self-aligned source/drain regions by MBE regrowth of n^{++} $In_{0.53}Ga_{0.47}As$ or InAs and self-aligned source/drain *in-situ* Mo contacts. The key motivation is to reduce the source access resistance by integrating low resistance *in-situ* Mo contacts [12] to degenerately doped InGaAs or InAs. The channel layer was vertically scaled to 5 nm with a InAlAs bottom confinement layer suitable to maintain 2-D electrostatic integrity at 22 nm L_g.

Chapter 2

General MOSFET Scaling Theory

This chapter summarizes the theory of MOSFET operation and general scaling laws. We will use n-channel MOSFET as an example to explain the device operation. The basic structure of a typical MOSFET is shown in Fig. (2.1). It is a three terminal device with *gate, source* and *drain* electrodes. The gate oxide or barrier can be a Schottky barrier as in the case of HEMTs. Applying a positive bias on the gate attracts mobile electrons to the channel from the source, and applying a positive drain bias gives rise to drain current. Similarly applying a negative voltage bias on the gate repels electrons from the channel turning the device off.

Table 2.1: List of commonly used abbreviations.

DIBL	Drain induced barrier lowering
DOS	Density of states
EOT	Equivalent oxide thickness

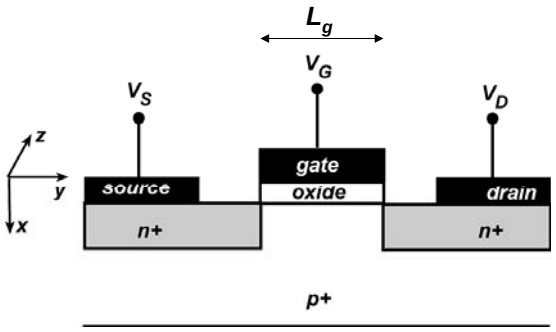


Figure 2.1: Cross section schematic of a Si MOSFET

2.1 MOSFET I-V

Typical long channel ($\frac{L_g}{\epsilon_{ch}} \gg \frac{t_{ox}}{\epsilon_{ox}}$) MOSFET I-V is shown in Fig. (2.2).The long channel I-V can be derived through a gradual channel approximation (GCA) *i.e.* the variation of electric field in the y-direction (along the channel) is much less than the corresponding variation in the x-direction (perpendicular to the channel). The expression for the saturated drain current is given by

$$I_{ds} = I_{dsat} = \mu_{eff} c_{ox} W_g (V_g - V_t)^2 / (2L_g) \tag{2.1}$$

where μ_{eff} is the channel mobility, c_{ox} is the gate capacitance per unit area, L_g and W_g are the gate length and width of the MOSFET. The key point to note is that the I_{dsat} increases as the square of gate overdrive $(V_g - V_t)$ and also increases with decrease in gate length. But the gradual channel approximation fails in short channel devices (typically $L_g < 0.5\mu m$ or more precisely when $\frac{L_g}{\epsilon_{ch}} < 2\frac{t_{ox}}{\epsilon_{ox}}$) when two-dimensional effects come into play and both gate and drain start modulating

the channel potential. Also, in a short channel device the drain current saturates at lower voltage than $(V_g - V_t)$ as predicted by GCA due to velocity saturation. In a short channel device the I_{dsat} varies linearly with gate overdrive $(V_g - V_t)$ and it does not scale with decreasing gate lengths.

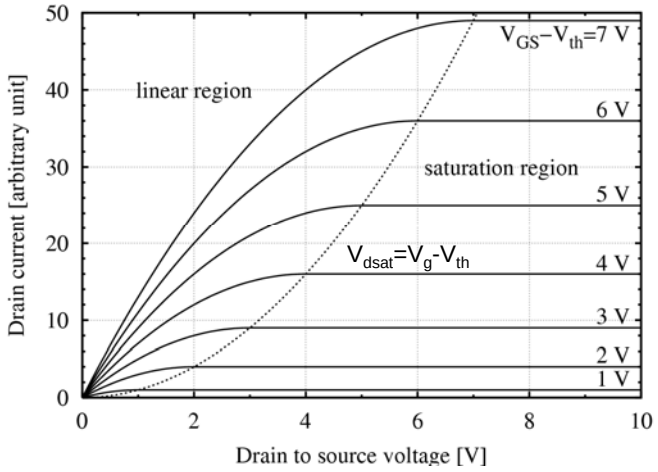
Fig.(2.3) shows typical experimentally observed velocity-field relationship for electrons in silicon MOSFETs, similar behavior is also observed for III-V semiconductors. The velocity saturates once a critical electric field (ε_c) is reached. The slope of the velocity field plot in the linear region gives the channel mobility (μ) of the device. In short channel devices the critical field ($V_{dd}/L_g > \varepsilon_c$) is easily reached and the drive current saturation occurs due to velocity saturation. The I-V relationship for short channel devices can be derived from drift-diffusion analysis assuming a velocity-field relationship as shown in Fig. (2.3). The saturated drain current is given by

$$I_{dsat} \approx c_{ox} W_g \upsilon_{sat} (V_g - V_t - \upsilon_{sat} L_g / \mu_n) \tag{2.2}$$

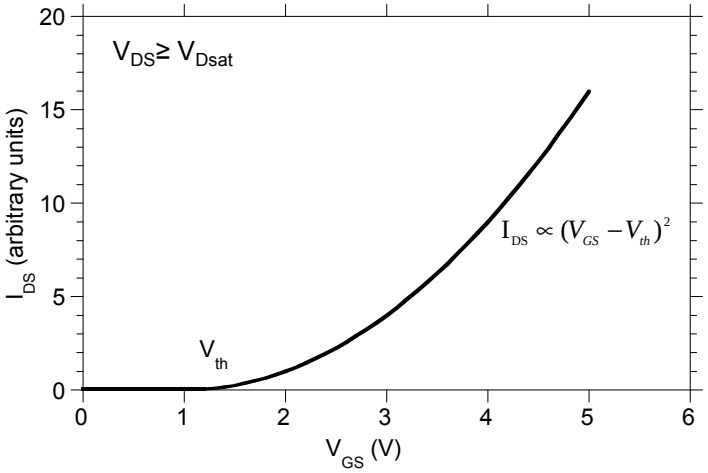
for $(V_g - V_t) \gg \upsilon_{sat} L_g / \mu_n$ [13]. As the gate length L_g is decreased the third term in parenthesis becomes negligible and the I_{dsat} can be approximated by

$$I_{dsat} \approx c_{ox} W_g \upsilon_{sat} (V_g - V_t) \tag{2.3}$$

and becomes independent of gate length.



(a) Typical long channel MOSFET I_d-V_d curves (Image source: Wikipedia)



(b) Long channel MOSFET I_d-V_g curves showing a quadratic turn on behavior

Figure 2.2: Long channel MOSFET characteristics

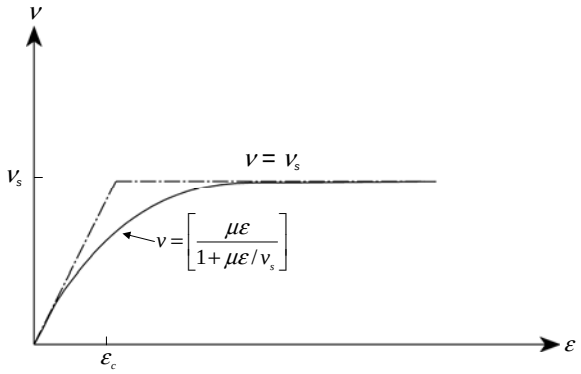


Figure 2.3: Approximate velocity field curve in a MOSFET [14]. The critical field for velocity saturation is marked out.

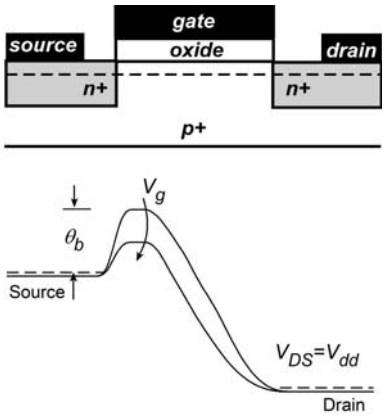


Figure 2.4: Conduction band profile along the dotted line in the channel from source to drain. The gate modulation of the barrier (θ_b) determines the transconductance

The saturated drain current in scaled devices is also derived using electron scattering theory in Ref. [15, 16] and is presented here. Fig. (2.4) shows a schematic band diagram of a MOSFET going along the channel from source to drain. Applying a gate voltage lowers the barrier height (θ_b) and electrons are injected into the channel from the source. The expression for I_{dsat} from scattering theory is

$$I_{dsat} = c_{ox} W_g \upsilon_{inj} \frac{1 - r_c}{1 + r_c} (V_g - V_t) \tag{2.4}$$

where υ_{inj} is the average injection velocity of electrons emitted from top of the barrier θ_b and r_c(backscatter coefficient) is the fraction backscattered electrons from channel into the source. The backscattering coefficient r_c is given by

$$r \approx \frac{l}{l + \lambda} \tag{2.5}$$

where λ is the mean free path electron between scattering events and $l \approx kT/qE$ is the distance along the channel over which the potential drops by kt/q. The device is said to operate in ballistic limit when $r_c = 0$. A backscatter coefficient of 0.4 is calculated for 0.3 μm Si MOSFET [17] and will approach 0 as the gate length is scaled to 22 nm and beyond. Without loss of generality we will use the the following expression for short channel ($L_g < 100$ nm) I_{dsat}.

$$I_{dsat} = c_{ox} W_g \upsilon_{inj} (V_g - V_t) \tag{2.6}$$

The transconductance of the transistor is therefore given by

$$\partial I_d / \partial V_g = g_m = c_{ox} W_g \upsilon_{inj} \tag{2.7}$$

The injection velocity υ_{inj} is the average thermal velocity of electrons injected over the potential barrier θ_b . In the degenerately doped source/drain case it is approximated by

$$\upsilon_{inj} = (4/3\pi)\upsilon_f = (4/3\pi)(2(E_f - E_c)/m^*)^{1/2} \tag{2.8}$$

where υ_f is the fermi velocity and m^* is the electron effective mass. It is clear from Eqs. (2.6), (2.7) and (2.8) that using a low electron effective mass channel material will increase both the drive current and transconductance.

The previous analysis assumes that the source/drain regions are perfectly conducting with zero resistance. But in reality there is always parasitic source/drain resistances due to finite semiconductor sheet and finite metal-semiconductor contact resistances. When the devices are scaled to short channel lengths to higher drive currents the parasitic source resistances becomes significant fraction of the total on resistance ($R_{on} = \frac{V_{DS}}{I_{DS}}$) and hence degrades the available drive current and transconductance. Fig. (2.5) shows a MOSFET with the parasitic resistances. The voltage drop across the source/drain resistances changes the intrinsic bias voltages as follows:

$$V'_{gs} = V_{gs} - R_s I_d \tag{2.9}$$

$$V'_{ds} = V_{ds} - (R_s + R_d) I_d \tag{2.10}$$

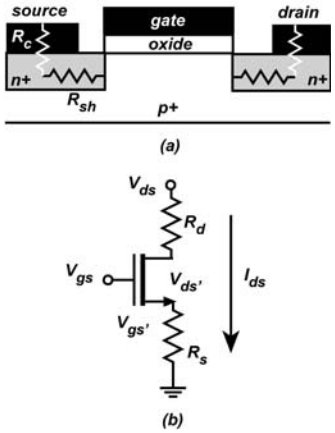


Figure 2.5: (a) MOSFET schematic showing the source access resistance components. (b) MOSFET circuit schematic with source and drain resistances.

Therefore the extrinsic I_d and g_m are related to the intrinsic parameters in Eqs. (2.6), (2.7) by

$$I_d = \frac{I_{di}}{1 + g_{mi}R_s} \tag{2.11}$$

$$g_m = \frac{g_{mi}}{1 + g_{mi}R_s} \tag{2.12}$$

2.2 MOSFET Scaling

CMOS devices have been scaling the device dimensions to achieve higher density, speed and lower cost of production. As the the gate length is scaled down short channel effects become dominant. A constant electric field field scaling was proposed by Dennard *et al* [18] where the device dimensions and voltages were

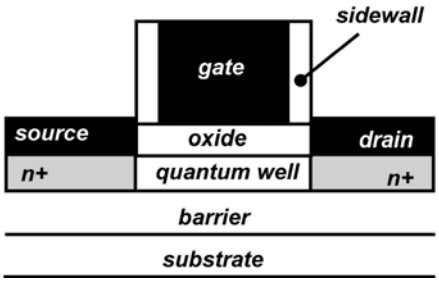


Figure 2.6: Schematic of a self-aligned SOI like III-V MOSFET. The quantum well is the channel.

scaled so that the short channel effects are under control. But in general the voltage has not been scaling at the same rate as the gate length partly due to threshold voltage non scalability and reluctance to depart from standardized voltage levels. So a constant voltage scaling is usually followed with supply voltage being scaled at a far slower rate than gate length scaling. In this section we will describe constant voltage scaling of MOSFETs to increase the bandwidth. For the scaling analysis we will use a self-aligned SOI like device structure as shown in Fig. (2.6). For $In_{0.53}Ga_{0.47}As$ channel FETs the $In_{0.48}Al_{0.52}As$ heterostructure barrier has the same role as the buried oxide in SOI devices. The channel is usually labeled as quantum well as quantum effects come into play at the typical channel thicknesses ($5 - 10$ nm). The analysis can be translated to to bulk Si like structure by replacing the quantum well thickness with the depletion width under the gate.

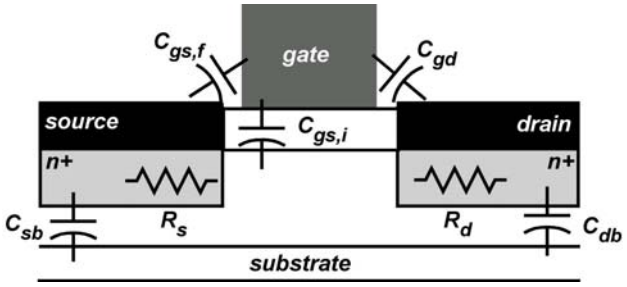


Figure 2.7: MOSFET schematic showing all the relevant capacitances and resistance in the on state ($V_{gs} = V_{ds} = V_{dd}$).

2.2.1 Constant Voltage Scaling

Fig. (2.7) shows a MOSFET with all the relevant capacitances and resistances for the scaling analysis. The delay hence bandwidth of any device will be given by both the transport delay and RC time constant of the device. The current gain cutoff frequency f_t of MOSFET is given by

$$\frac{1}{2\pi f_t} = \frac{C_{gg,t}}{g_m} + \frac{C_{gg,t}}{g_m}(R_s + R_d)g_d + (R_s + R_d)C_{gd,t} \tag{2.13}$$

where $C_{gg,t} = C_{gs,t} + C_{gd,t} = C_{gs,i} + C_{gs,f} + C_{gd,t}$ is the total gate capacitance, $C_{gd,t}$ is the total gate to drain capacitance, g_d is the output conductance and R_s, R_d are the parasitic source and drain resistances [19]. When the gate length is long, the first term in Eq. (2.13) can be approximated to $\frac{C_{gs,i}}{g_m}$. This is usually referred to as the intrinsic delay of the transistor and is approximately given by $\tau_{int} = L_g/\upsilon$ where υ is the electron velocity under the gate. The second and third term are the RC delay time of the transistor. In the constant voltage scaling the aim is to

double the device bandwidth by reducing all the transport delays and capacitances by $2:1$ while keeping constant all resistances, voltages and currents [13, 20]. This is accomplished by scaling down both the lateral and vertical device dimensions by a factor of $2:1$.

Scaling the oxide thickness t_{ox} increases the equivalent gate capacitance $c_{gs,i} = c_{eq} \sim 1/t_{ox}$ per unit area. Reducing the gate width W_g by a factor of two keeps the $g_m \sim W_g c_{eq} \upsilon_{inj}$ and $I_d \sim W_g c_{eq} \upsilon_{inj}(V_g - V_t)$ constant. Reducing the gate length L_g by a factor of two reduces the total gate capacitance $C_{gs} = c_{eq} W_g L_g + \alpha W_g$ by a factor of two. The second term in C_{gs} is the fringing capacitance. Other parasitic capacitances C_{gd}, C_{sb} and $C_{db} \propto W_g$ are also scaled down by a factor of two. The source/drain contact length $L_{s/d}$ is also scaled by a factor of two in proportion with the gate length. This requires a four fold decrease in the specific contact resistivity to keep the source resistance $R_s = \rho_c/(L_{s/d} W g) + \rho_s L_{s/d}/W_g$ constant. Following the above mentioned scaling laws the device bandwidth is doubled as can be seen from Eq. (2.13). We will consider the implications of each of the above mentioned scaling laws.

2.2.2 Gate oxide(EOT) scaling

In all the previous analysis the gate capacitance was calculated by $c_{gs,i} = c_{eq} = c_{ox} = \epsilon_{ox}/t_{ox}$ assuming the inversion layer charge as a sheet of charge of zero thick-

ness at the oxide-semiconductor interface. This assumption breaks down when the oxide thickness is decreased and the charge centroid of the inversion layer or the effective "electrical" inversion layer distance ($\frac{t_{inv}}{\epsilon_s}$) of the sheet charge from the oxide-semiconductor distance becomes comparable to the "electrical" oxide thickness ($\frac{t_{ox}}{\epsilon_{ox}}$). Fig. (2.8) shows a schematic band diagram of a MOSFET in the on state. The inversion electrons are confined in the triangular potential well formed at the oxide-semiconductor interface. Because of the confinement in the x- direction, the inversion layer electrons have to be treated quantum mechanically as 2-D system. A self-consistent Schrodinger-Poisson solution of a 5 nm $In_{0.53}Ga_{0.47}As$ channel MOSFET is shown in Fig. (2.9). The peak of electron density is away from the oxide-interface meaning the equivalent oxide thickness (EOT) is slightly larger than the physical oxide thickness. In the case of SOI like MOSFETs with back barrier the peak of the the electron wave function can be assumed to be the center of the quantum well as a first order approximation. So the equivalent gate capacitance is given by

$$\begin{aligned} \frac{1}{c_{eq}} &= \frac{1}{c_{ox}} + \frac{1}{c_{qw}} \\ &= \frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{qw}}{2\epsilon_{qw}} \end{aligned} \tag{2.14}$$

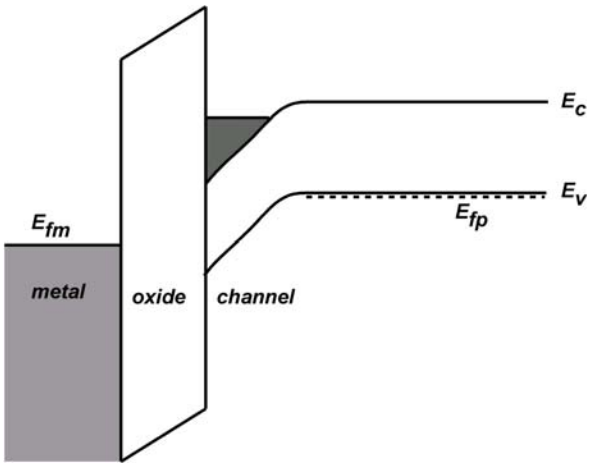


Figure 2.8: MOSFET band diagram in on state, channel thickness is comparable to the oxide thickness.

where t_{qw} and ϵ_{qw} are the thickness and dielectric constant of the quantum well. Following the scaling laws outlined in the previous section the quantum well thickness (t_{qw}) must also scale along with the gate oxide thickness (t_{ox}).

Another capacitance that comes into play in extremely scaled EOT devices is the density of states capacitance (c_{dos}) or quantum capacitance. The origin of c_{dos} is in quantum mechanics and it is due to the finite density of states of a 2-D electron system [22]. Because of the finite density of states in a quantum mechanical 2-D system, it takes additional energy to add extra electrons to a system. In other words there is voltage drop associated with addition of electrons to a 2-D system. This effect can be modeled as voltage drop across a density of

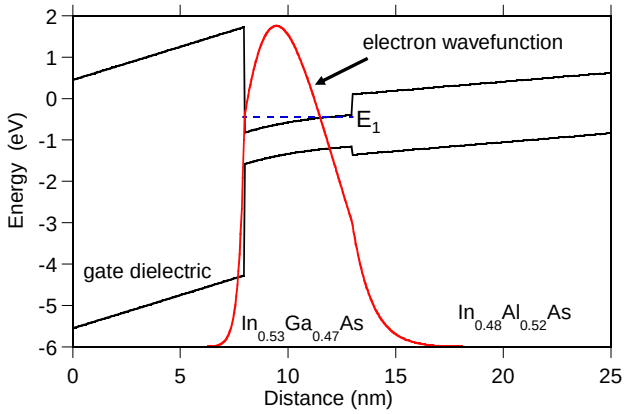


Figure 2.9: Electron wavefunction in a $In_{0.53}Ga_{0.47}As$ MOSFET calculated using a self-consistent Schröndinger and Poisson Solver [21]. The dotted line shows the bottom Eigen state energy.

capacitance (c_{dos}). The (c_{dos}) is given by

$$c_{dos} = \frac{m^* e^2}{\pi \hbar^2} L_g W_g \tag{2.15}$$

where m^* is the effective mass of electron and e is electron charge [22]. The equivalent gate capacitance including the quantum well capacitance and density of states capacitance is given by

$$\begin{aligned} \frac{1}{c_{eq}} &= \frac{1}{c_{ox}} + \frac{1}{c_{qw}} + \frac{1}{c_{dos}} \\ C_{eq} &= (\frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{qw}}{\epsilon_{qw}} + \frac{\pi \hbar^2}{m^* e^2}) L_g W_g \end{aligned} \tag{2.16}$$

This is shown schematically in Fig. (2.10). As the gate oxide is scaled the density of states capacitance becomes significant portion of the total capacitance. Once the density of states capacitance dominates the equivalent capacitance ceases to

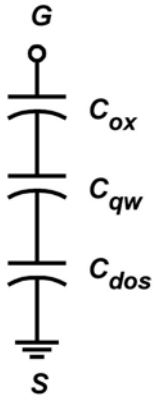


Figure 2.10: Equivalent gate source capacitance in the on state.

scale with gate oxide and quantum well scaling. It is clear from Eq. (2.16) that this effect will be more prominent in materials with lower electron effective mass (m^*).

The result of silicon dioxide scaling in Si MOSFETs to below 10 nm thickness is an increase in gate leakage current due to increased tunneling probability across the physically thin oxide. This results in rapid increase in the standby power consumption. To mitigate this problem a high-k (ϵ) dielectric is used. This enables to scale the oxide capacitance ($c_{ox} = \epsilon_{ox}/t_{ox}$) and at the same time keep the physical thickness large to avoid tunneling currents.

The quantum well scaling starts to slow down when the quantum well thickness is $< 5\ nm$. Because of quantum confinement, the lowest bound state energy level ($E1$) rises as $\sim 1/m^* t_{qw}^2$ in deep wells. This may increase $E1$ to the point where carriers are poorly confined. This situation is more severe in low effective mass

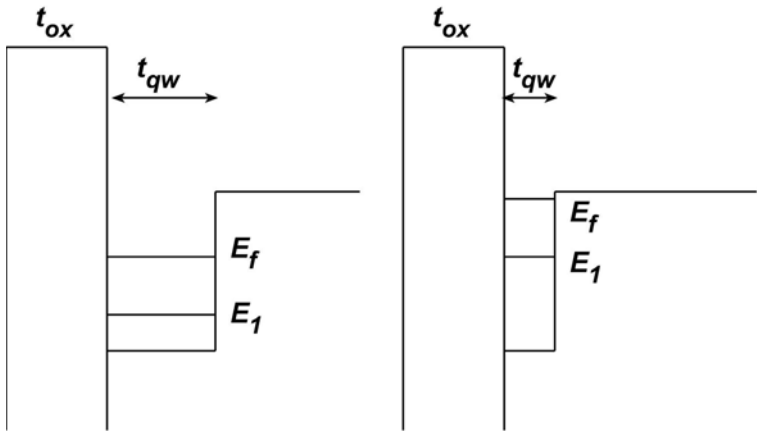


Figure 2.11: Thinning down the quantum well raises the 1st Eigen state energy and electron may lose confinement.

(m^*) semiconductors like indium rich InGaAs. This is shown conceptually in Fig. (2.11). This condition sets the minimum quantum well thickness and consequently the equivalent gate capacitance does not scale in commensurate with the gate oxide scaling. The quantum well thickness can be scaled beyond this limit if a bottom barrier height is increased through use of a double gate structure or a wide bandgap semiconductor. When the quantum well is scaled to such thin layers the roughness scattering can degrade the mobility. The mobility may deteriorate to a point such that it may degrade the current density as seen from Eq. (2.3). The minimum quantum well thickness and the density of states capacitance may determine the minimum achievable EOT for a particular channel material rather than the high-k dielectric scaling.

2.2.3 Source/drain resistance scaling

As outlined in Sec. (2.2.1) the source/drain resistance should stay constant with scaling. Fig. (2.12) shows different components of the source resistance. The total source resistance is given by [13]

$$\begin{aligned} R_s &= R_{contact} + R_{access} \\ R_s &= \frac{\rho_c}{W_g L_{s/d}} + \frac{\rho_s L_{s/d}}{2W_g} \end{aligned} \tag{2.17}$$

where Ls/d is the source/drain contact length, ρ_c is the specific contact resistivity and ρ_s is the sheet resistance of n^+ source region. The sidewall thickness is assumed small compared to $L_{s/d}$. The effect of sidewall thickness on source resistance will be discussed in later chapters. The source/drain contact resistance $L_{s/d}$ and gate width W_g must scale down with the gate length L_g in order to increase the IC package density and also to scale down parasitic capacitances ($C_{par} \propto W_g$). As a result the specific contact resistivity ρ_c must scale as the inverse square of gate length to keep the resistance constant. The sheet resistivity ρ_s in the source/drain region is given by

$$\rho_c = \frac{1}{t_{qw} n e \mu_s} \tag{2.18}$$

where n is the electron density in the source region, μ_s is the mobility of electrons in the source region. The t_{qw} scales with the gate length, so to keep the sheet resistance constant the electron density (n) and consequently doping density (N_d)

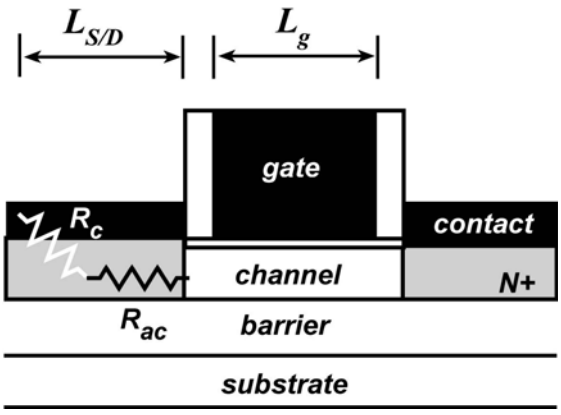


Figure 2.12: MOSFET schematic showing the source resistance components.

in the source has to scale up. But the mobility μ_s usually degrades with doping so the doping density has to scale faster than the gate length to keep the source resistance constant. So even though the total source resistance needs to be constant the specific contact resistivity and doping density have to scale at a faster rate than the gate length.

The contact resistance scaling presents considerable technological challenges. Contact resistance can be reduced by decreasing the Schottky barrier height between metal and the semiconductor and also by increasing the doping in the semiconductor. But in reality surface states at the metal semiconductor interface play a major role. They deplete the semiconductor in order to maintain charge neutrality thus increasing the depletion width. This results in increased contact resistance. So careful surface passivation techniques are done to reduce the contact resistance.

Unlike H passivation of Si by buffered HF treatment, III-V semiconductors do not have good surface passivation techniques. This creates considerable challenge to realize repeatable ultra low contact resistances ($\rho_c \leq 1\Omega - \mu m^2$) in III-V semiconductors. The issues and solutions to obtaining ultra low contact resistances to InGaAs is discussed in detail in Refs. [12, 23, 24]. The contact resistance is also one of the technological bottleneck to scaling in Si MOSFETs.

The doping density scaling in source/drain regions is also a considerable technological challenge. The doping densities requirements for sub-22nm L_g Si MOSFETs are $\sim 1 \times 10^{20}\ cm^{-3}$. These doping densities are reaching the solid solubility limits beyond which there is no increase in carrier concentration with doping. Similarly, for III-V semiconductors amphoteric nature of donor dopant atoms causes self-compensation. This sets the limit of maximum achievable active carriers. The sheet and contact resistance have not been scaling at the same pace as the gate length.

2.2.4 Short channel effects

The quantum well thickness t_{qw} thickness has to scale with the gate length not only to scale the EOT as explained in Sec. (2.2.2), but also in order to keep the electrostatic integrity of the device. This is very critical in the subthreshold region of the device. Fig. (2.13) shows a typical sub-threshold $I_d - V_g$ plots of

long channel and short channel FETs on a log scale. In the subthreshold region we can write the drain current as

$$\Delta I_d = \frac{\partial I_d}{\partial V_{gs}} \Delta V_{gs} + \frac{\partial I_d}{\partial V_{ds}} \Delta V_{ds} \tag{2.19}$$

where the first term is drain current modulation by the gate voltage and the second term is modulation by the drain voltage. The inverse slope of the $Log(I_d) - V_g$ plot $(\frac{\partial \log I_d}{\partial V_g})^{-1}$ at low drain bias (typically 50-100mV) is known as the subthreshold swing. This slope changes in high drain bias conditions for the short channel FETs. The ratio $(\frac{\Delta V_{th}}{\Delta V_d})$ is known as the drain induced barrier lowering or DIBL factor (λ_d). As gate length is scaled down the drain modulation (Fig. (2.16)) $(\frac{\partial \theta_b}{\partial V_{ds}})$ of the barrier increases as the drain electric field couples with the channel and consequently the drain modulation of the drive current $(\frac{\partial I_d}{\partial V_{ds}} \delta V_{ds})$ increases. This has strong implication on the off state leakage current of the device. In the subthreshold regime drain current is dominated by diffusion rather than drift. Hence the current has exponential dependence on the control voltage. Therefore, the off state leakage current below threshold voltage is given by [25]

$$I_{off} = I_{th} 10^{-\frac{1}{S}[\Delta V_g + \lambda_d \Delta V_d]} \tag{2.20}$$

where I_{th} is the drain current at threshold voltage, S is the sub-threshold swing, λ_d is the DIBL factor. So, both subthreshold slope and DIBL effect have to be reduced for low off state leakage current. Because of the exponential dependence

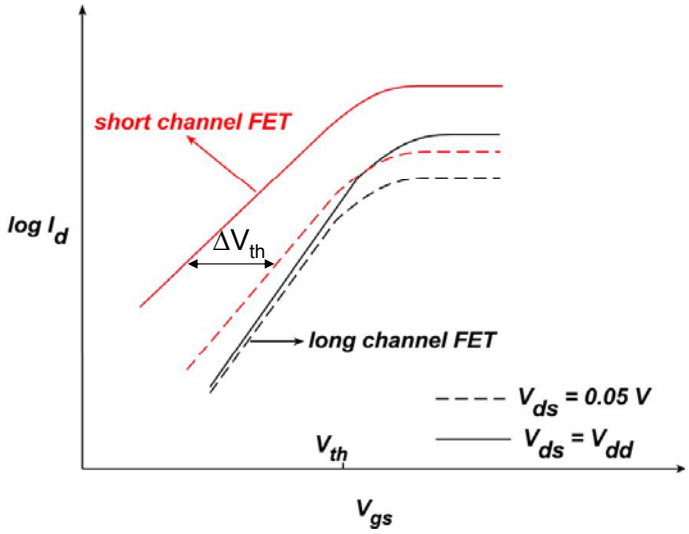


Figure 2.13: Schematic plot of typical subthreshold characteristics of a long channel and short channel MOSFETs.

even a 10% change in subthreshold swing (S) can result in increase of the off state current by a factor of 10 (Fig. 2.14).

The MOSFET capacitance in the subthreshold operation is shown in Fig. (2.15). The depletion capacitance can be approximated to be the capacitance of the channel or quantum well ($C_d = \epsilon_s A/t_{qw}$). The subthreshold swing for a device is given by

$$S = \frac{C_{ox} + C_d}{C_{ox}} 60mV/decade \tag{2.21}$$

where C_d is the depletion capacitance in the subthreshold operation. To minimize the subthreshold swing (S) the ratio of depletion capacitance to gate capacitance ($\frac{C_d}{C_{ox}}$) should be minimized. This can be done either by decreasing the oxide

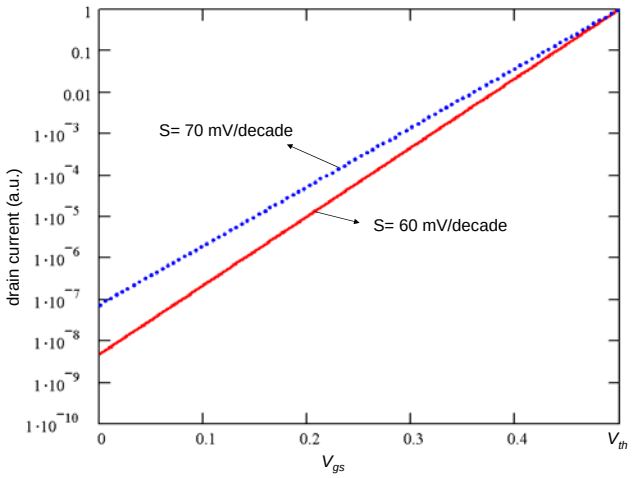


Figure 2.14: Subthreshold currents for two devices with subthreshold swing of 60 mV/decade and 70 mV/decade. The threshold voltage for both the devices is 0.5 V. The device with 70 mV/decade subthreshold swing has $10\times$ more leakage current at $V_{gs} = 0V$.

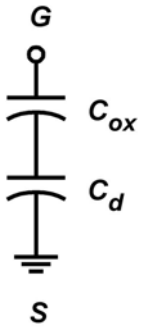


Figure 2.15: MOSFET capacitance in the subthreshold regime.

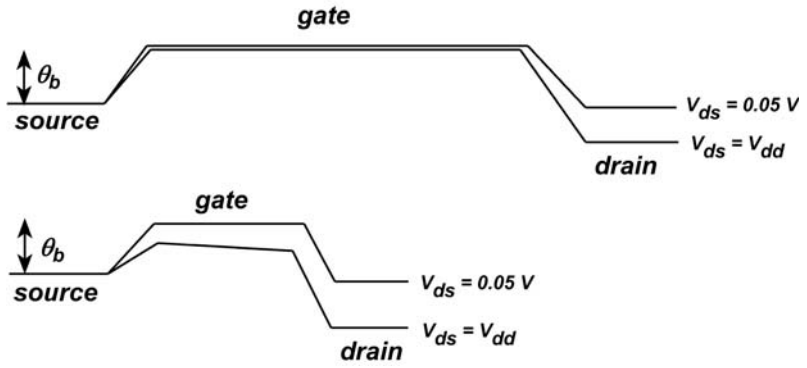


Figure 2.16: Schematic band diagram of long channel (top) and short channel (bottom) MOSFETs. The drain modulation of $\theta_{barrier}$ in the short channel FETs gives rise to the DIBL effect.

thickness or by increasing the quantum well thickness. But increasing the quantum well thickness increases DIBL.

The DIBL effect is given by the two-dimensional electrostatics of the device in the sub-threshold operation of the MOSFET [26, 27]. The DIBL effect can be reduced by scaling the the quantum well thickness with the gate length so that the drain electric field penetration into the channel is minimized. The source/drain junction thickness also needs to be scaled to the same thickness as the quantum well thickness to control DIBL. Deep source/drain junctions give low sheet resistance but degrade short channel effects as the drain field penetrates into the channel as shown schematically in Fig. (2.17). The quantum well thickness has opposite effects on the subthreshold swing (Eq. (2.21)) and DIBL. So the device

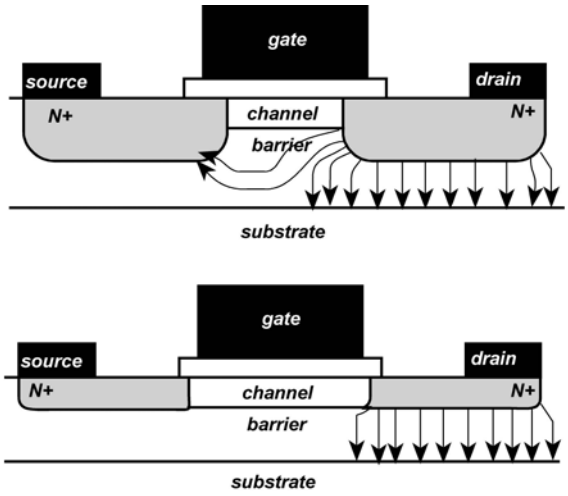


Figure 2.17: Schematic diagram showing drain field penetration into source for deep junctions compared to a shallow junction.

structure is usually optimized to meet the target sub threshold slope and DIBL for particular application.

Another source of off state current in scaled devices is the tunneling leakage between source and drain. Fig. (2.18) shows a schematic band diagram of a MOSFET in the off state. There are two possible tunneling leakage currents [28] as shown in the figure . The tunneling probability depends on the electron effective mass, barrier height and electric field ($T_t \propto exp(-\frac{m^* \theta_b^{3/2}}{\varepsilon})$); in the case of band to band tunneling (inter-band) the barrier height is equal to the bandgap of the semiconductor *i.e.* ($\theta_b = E_g$). As the gate length is scaled down the peak electric field near the drain side increases thus increasing the band to band tunneling tunneling component of the off state leakage current (I_{off}). This effect is very

important in the narrow gap semiconductors with the low electron effective mass and need to be considered during the device design.

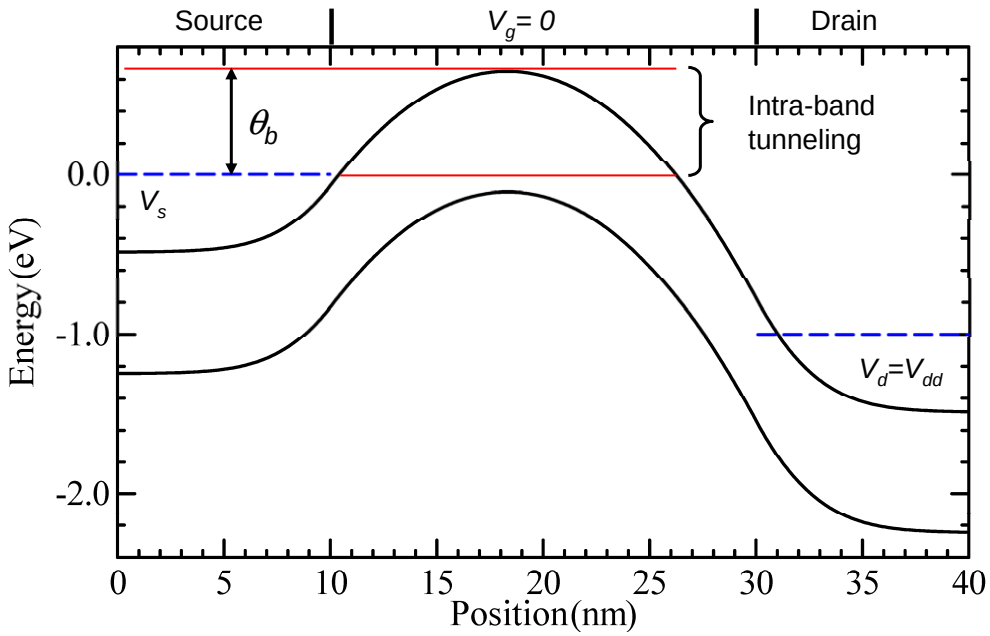
2.2.5 CMOS circuit delay

The basic element in a digital CMOS circuit is a CMOS inverter. Fig. (2.19) shows the schematic of a typical inverter with all the relevant capacitances. The delay of the inverter is given by

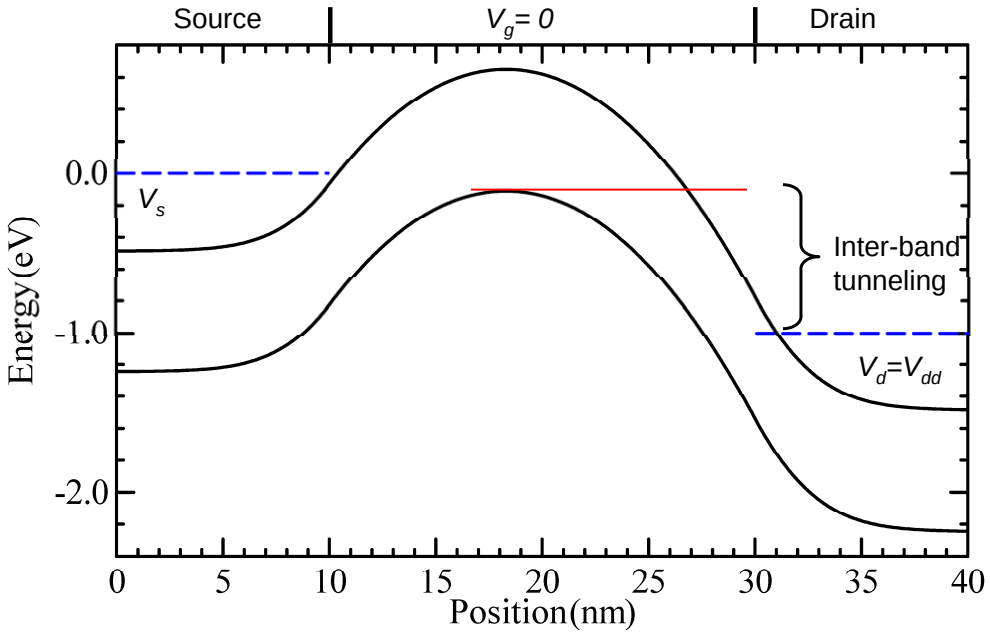
$$\tau = \frac{C_{output} V_{dd}}{I} \tag{2.22}$$

where $C_{output} = C_{gs} + 4C_{gd} + C_{db} + C_w$. Because of Miller effect the gate drain capacitance appears both on the input and output of the transistors. At sub-100nm gate length transistors all the parasitic capacitances are comparable to the intrinsic gate capacitance $C_{gs,i}$ and do not scale with gate length scaling. The switching delay can be reduced only through increased drive current. The intrinsic switching delay ($\frac{C_{gs,i}V}{I_{ds}}$) is no longer a relevant figure of merit. For sub-100nm gate length devices the parasitic capacitances ($C_p = C_{gs} + 4C_{gd} + C_{db} + C_w$) dominates and becomes a constant across different technologies. The extrinsic switching delay given by

$$\tau = \frac{C_p V_{dd}}{I} \tag{2.23}$$



(a) Intra-band tunneling in a scaled MOSFET



(b) Inter-band tunneling in a scaled MOSFET

Figure 2.18: Schematic band diagram along the channel of 20 nm $In_{0.53}Ga_{0.47}As$ channel MOSFET at $V_{gs} = 0V$ and $V_{ds} = V_{dd} = 1V$.

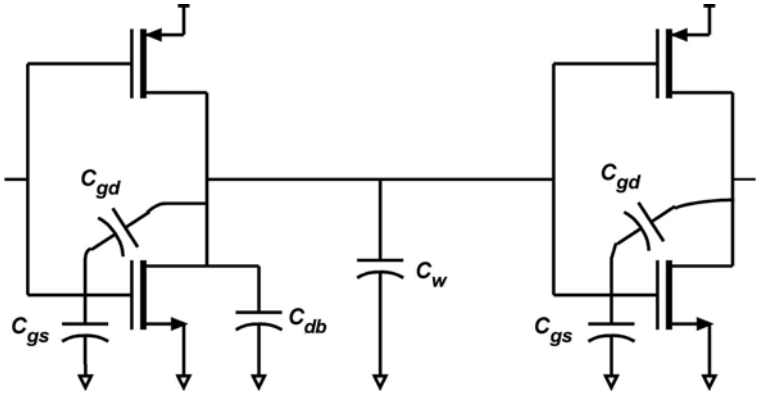


Figure 2.19: A CMOS invertor with all the relevant capacitances.

is a good figure of merit for comparing different technologies. With constant C_p, the transconductance ($g_m = \frac{I}{V_{dd}}$) becomes the significant figure of merit and needs to be improved with scaling.

2.3 Conclusions

In this chapter we summarized constant voltage scaling principles for MOSFETs. In the above analysis power density was not considered. As a result of constant voltage scaling the peak electric field increases in the device. This increases the probability of device breakdown through impact ionization. Taking these considerations the voltage may have to scale. The constant voltage scaling is just a design guide. Devices are usually designed for specific application. The performance parameters for a CMOS VLSI circuit are the integration den-

sity, switching speed, active and passive power dissipation. CMOS devices can be designed for different performance parameters depending on the application. A device can be designed for high switching speeds compromising the passive power performance and vice versa. A device technology where the circuit designer has the flexibility to choose devices for high performance vs low power is preferred. This flexibility is usually available in present Si CMOS device technologies. Any III-V MOS technology should also aim to have with this flexibility.

Chapter 3

22 nm InGaAs MOSFET design

Because of high electron velocities observed experimentally in InGaAs-based HEMTs [10, 11], MOSFETs with $In_xGa_{1-x}As$ ($x \geq 0.53$) channels are being developed for potential application in VLSI logic circuits at technology nodes below 22 nm gate length (L_g). There are several challenges faced in rendering these devices suitable for very-large-scale circuits. For integration into ICs on silicon substrates, methods must be developed to grow $In_xGa_{1-x}As$ with low defect density on Si. The semiconductor-dielectric interface state density must be small ($\leq 1 \times 10^{12} cm^{-2}$), and various gate dielectrics and deposition techniques are therefore being investigated [29–32].

In this chapter we design a high performance 22 nm L_g $In_{0.53}Ga_{0.47}As$ channel N-MOSFET for VLSI logic application as an alternative to Si N-MOSFETs. We compare the potential scalability of this device with Si N-MOSFET.

3.1 FET Design

The design goal is significantly higher drive currents and transconductances than a 22 nm Si N-MOSFET. The devices are designed for 1V V_{dd}.

3.1.1 Channel Material Selection and threshold voltage

Table 3.1: Ballistic transconductances and drive currents for Si and $In_{0.53}Ga_{0.47}As$ channel MOSFETs with 1 nm EOT ($(\frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{qw}}{\epsilon_{qw}})\epsilon_{SiO_2}$) and 0.5 nm EOT. c_{dos} for $In_{0.53}Ga_{0.47}As$ and Si are 1.23 nm and 0.02 nm respectively.

Channel	V_t (V)	c_{eot} (nm)	c_{eq} (nm)	g_m $(mS/\mu m)$	$I_d(V_{gs}$=1.0V) $(mA/\mu m)$
$In_{0.53}Ga_{0.47}As$	0.3	1	2.23	4.41	3.0
Si	0.3	1	1.02	3.22	2.25
$In_{0.53}Ga_{0.47}As$	0.3	0.5	1.73	5.82	4.0
Si	0.3	0.5	0.52	6.70	4.70

We will compare $In_{0.53}Ga_{0.47}As$, and Si as channel material for 22 nm L_g N-MOSFETs. Our goal is to obtain maximum transconductance per unit length g_m/W_g given by $c_{eq}v_{inj}$. $In_{0.53}Ga_{0.47}As$ is investigated as channel material not only because of its low electron effective masse (m^*) but also because of the maturity of the InGaAs/InP material technology in HEMTs and HBTs. We will use ballistic FET theory to calculate and compare potential transconductances (g_m) and drive currents for the these material systems. The equation for calculating the ballistic

g_m is

$$g_m = W_g c_{eq} \upsilon_{inj} \tag{3.1}$$

where c_{eq} is given by Eq. (2.16). The injection velocities of $3 \times 10^7 cm/s$ and $1 \times 10^7 cm/s$ were used for $In_{0.53}Ga_{0.47}As$ and Si respectively. Table (3.1) shows the ballistic drive current for $In_{0.53}Ga_{0.47}As$ and Si channel devices for two different dielectric thickness. At 1 nm EOT $In_{0.53}Ga_{0.47}As$ shows moderately higher drive current than Si, but at 0.5 nm EOT Si has more drive current than $In_{0.53}Ga_{0.47}As$ because of the lower c_{dos} of $In_{0.53}Ga_{0.47}As$. InGaAs channel provides advantage only if EOT cannot be scaled below 0.5 nm in Si MOSFETs or Si cannot reach ballistic operation due to degraded mobility or due to high source resistance. $In_{0.53}Ga_{0.47}As$ based FETs offer the simultaneous advantage of higher mobilities and lower source access resistance. A high field electron mobility of 1000 $cm^2/V{\cdot}s$ is experimentally observed in $In_{0.53}Ga_{0.47}As$ channels with high-k dielectric [30]. The threshold voltage shift $\Delta V = \upsilon_{exit} L_g/\mu_n$ due to a mobility of 1000 cm^2/V-s for the 22 nm L_g $In_{0.53}Ga_{0.47}As$ channel device is 0.07 V [13] and does not degrade the drive current significantly. A peak drive current of 3 $mA/\mu m$ at $V_{dd} = 1.0V$ can be achieved in 22 nm $In_{0.53}Ga_{0.47}As$ MOSFET with 1.0 nm EOT (quantum well + gate dielectric).

With a given V_{dd}, the lower the threshold voltage, the higher the drive current thus faster switching speed. But the maximum off state leakage current

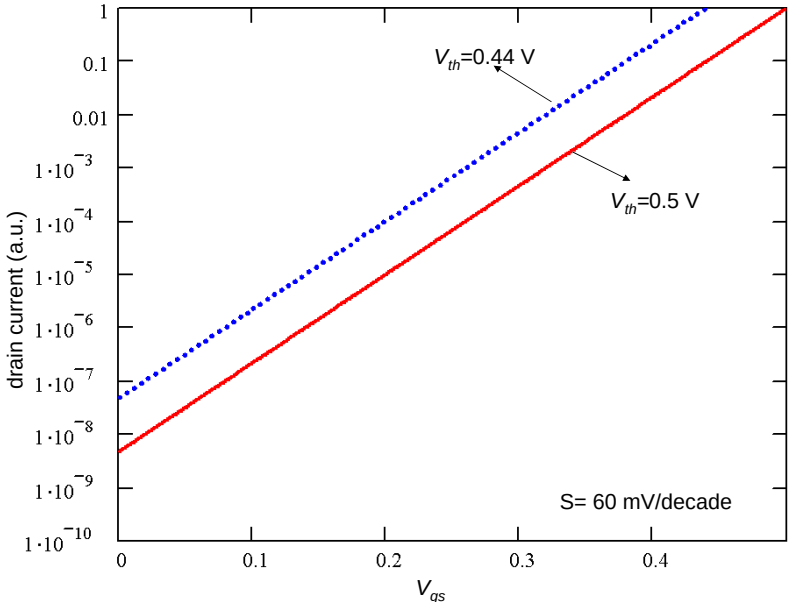


Figure 3.1: A 10 % change in the threshold voltage results in almost an order of magnitude increase in the off state leakage current ($I_{off}(V_{gs} = 0$ V)).

$I_{off}(V_g = 0)$ requirement determines the minimum threshold voltage. The threshold voltage has to be large enough to withstand typical process variations (film thicknesses, doping etc.) and at the same time maintain the maximum off state leakage requirement. Fig. (3.1) shows the effect of threshold voltage shift on the off state leakage current (I_{off}). Depending on applications the ITRS roadmap [9] recommends a threshold voltage between 0.1 V to 0.5 V. The threshold voltage can be tailored by the gate metal workfunction and pulse doping in the back barrier. Fig. (3.2) shows the sheet electron density calculated using 1-D Poisson

solver and the change in threshold voltage with pulse doping in the confinement layer. We are using a threshold voltage of 0.3 V as design target in this thesis.

3.1.2 Quantum well thickness

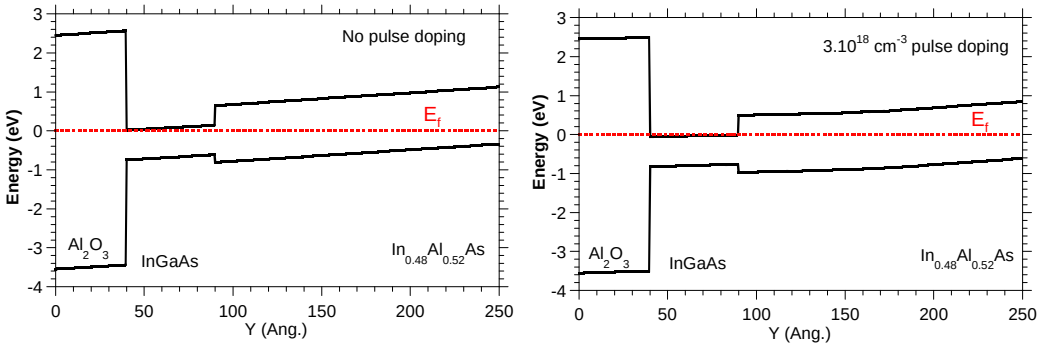
The quantum well thickness needs to scale to minimize both the drain induced barrier lowering (DIBL) and g_{ds}/g_m ratio in short channel devices. The depletion layer in the subthreshold regime of the transistor can be approximated by a rectangle as show in Fig. (3.3). The magnitude of DIBL is set by the aspect ratio of the rectangle. The length of the rectangle should be at least twice the width in order to minimize DIBL. For a 22 nm gate length device a maximum depletion width of 10 nm is required. This can be achieved by having 5 nm $In_{0.53}Ga_{0.47}As$ channel and 5 nm $In_{0.48}Al_{0.52}As$ setback with p^+ ground plane. Doping the $In_{0.48}Al_{0.52}As$ barrier next to the channel can give rise to tunneling leakage into the substrate.

There is also a minimum depletion width requirement from subthreshold slope point view. Fig. (3.4) shows the body effect in a MOSFET. The subthreshold slope is given by

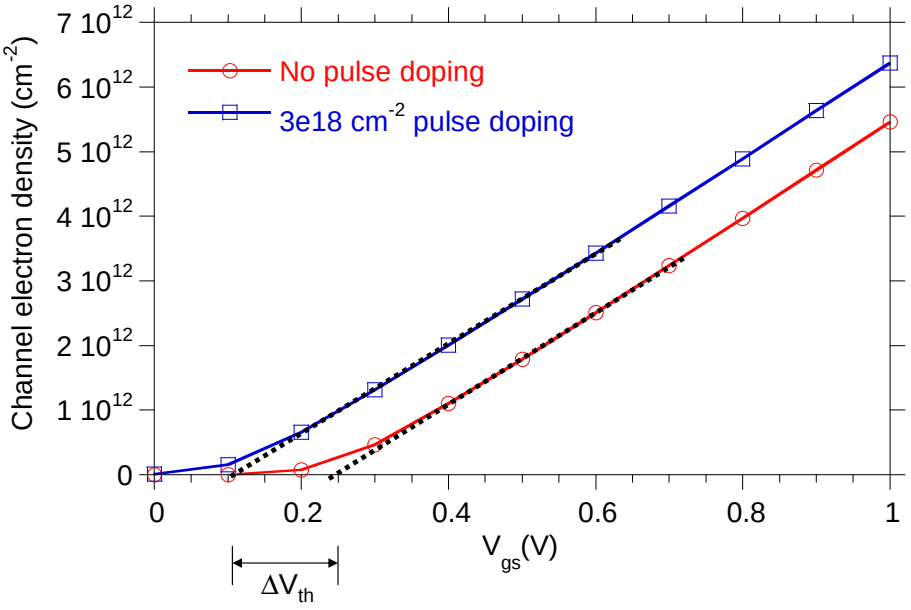
$$S = m * 60mV/decade, \tag{3.2}$$

where the body coefficient m is given by

$$m = \frac{\Delta V_g}{\Delta V_s} = 1 + \frac{\epsilon_d t_{ox}}{\epsilon_{ox} W_d} \tag{3.3}$$



(a) Band diagram of MOSFET with and without pulse doping



(b) Calculated channel electron density. The pulse doping in the back barrier shifts the threshold voltage. The threshold voltage can be tailored by choosing the gate work function and the pulse doping.

Figure 3.2: MOSFET V_t tuning.

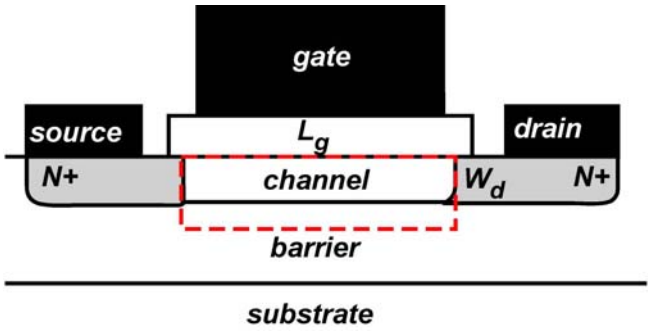


Figure 3.3: The aspect ratio of the depletion rectangle of the MOSFET in subthreshold regime sets the DIBL.

A 80 mV/decade subthreshold target translates to m=1.3 which gives a minimum depletion width of 10 nm with a depletion dielectric coefficient ϵ_d of 14 for 1 nm EOT device. This condition is satisfied in our structure of 5 nm channel with 5 nm setback.

3.1.3 Gate Dielectric

The choice of gate dielectric material is based on the EOT, gate leakage and interface state (D_{it}) requirements. Fig. (3.5) shows a band diagram schematic of the MOSFET in the on state. Depending on the barrier the gate leakage current mechanism can be thermionic emission over the barrier or tunneling leakage through barrier. The conduction band offset between the $In_{0.53}Ga_{0.47}As$ channel and gate dielectric should be at least ($V_{dd} = 1V$) from the the fermi level in the channel to avoid thermionic emission current. This requirement rules out

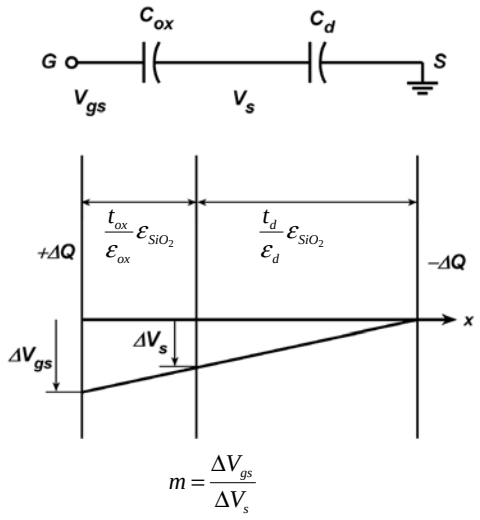


Figure 3.4: The body coefficient of MOSFET determines the subthreshold swing.

$In_{0.48}Al_{0.52}As$ as the gate barrier as the conduction band offset is 0.5 V. The tunneling gate leakage current depends on the barrier height and width of the gate dielectric. There are two mechanism of tunneling current: Fowler-Nordheim, where the electrons tunnel from the conduction band of the channel to the conduction band of the gate dielectric and direct tunneling where the electrons tunnel from the conduction band in the channel to the gate metal. Direct tunneling current starts to dominate when the physical gate dielectric is thin ($\leq$ 3.5 nm) and increases rapidly with thinning the dielectric thickness [33, 34]. Depending on the gate dielectric constant and EOT the gate leakage may be dominated by direct tunneling or Fowler-Nordheim tunnling.

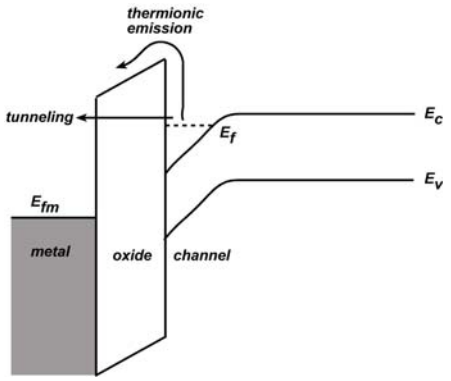


Figure 3.5: The gate leakage mechanisms: thermionic emission and tunneling.

In section (3.1.1) we designed the $In_{0.53}Ga_{0.47}As$ MOSFET with 1 nm EOT gate dielectric. The quantum well contribution to the EOT ($\frac{t_{qw}}{\epsilon_{qw}}\epsilon_{SiO_2}$) is 0.5 nm. That leaves 0.5 nm EOT from the high-k gate dielectric. Table (3.2) shows the the choices to realize 0.5 nm EOT from the published list of high-k dielectrics on InGaAs. With target minimum physical thickness of 3.0 nm from leakage considerations, a minimum dielectric constant of 16 is required. A combination of high-k dielectrics can also be used for the desired physical thickness and EOT.

The most important parameter for dielectric selection is the interface state density (D_{it}) at the semiconductor-dielectric interface. The interface states affect both the subthreshold swing and the maximum drive current of the device. In the subthreshold operation of the device the effect of interface states can be modeled as a capacitance in parallel with the depletion capacitance (Fig.3.6(a)). This

Table 3.2: Different high-k dielectric materials with their dielectric constants [30, 31] and required physical thickness ($t_{ox} = 0.5\frac{\epsilon_{ox}}{\epsilon_{SiO_2}}$) corresponding to 0.5 nm EOT.

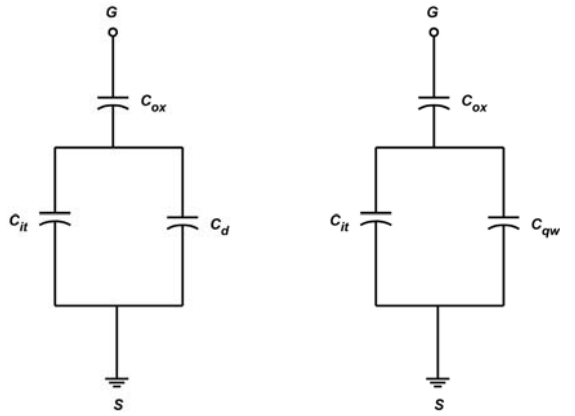
Gate dielectric	Dielectric constant (κ)	c_{eot} (nm)	t_{ox} (nm)
Al_2O_3	9	0.5	1.2
ZrO_2	30	0.5	4.0
HfO_2	19	0.5	2.5
$Hf_{0.8}Si_{0.2}O$	13	0.5	1.7
$Hf_{0.5}Al_{0.5}O$	12	0.5	1.5

results in degradation of the subthreshold swing (S) of the device which is given by [14]

$$S = \frac{C_{ox} + C_d + qD_{it}}{C_{ox}} 60mV/decade \tag{3.4}$$

where the depletion capacitance is set by the thickness of the quantum well and the thickness of the setback. The degradation in subthreshold slope results in increased off state current as given by Eq. (2.20) and explained schematically in Fig. (2.14). With a subthreshold target value of 90 mV/decade a maximum (D_{it}) of $1 \times 10^{12} cm^{-2}$ is required. The effect of D_{it} in the on state of the device is modeled as a parallel capacitance to the quantum well capacitance as shown in Fig. (3.6(b)). The resulting degradation in inversion capacitance causes a degradation in the drive current and transconductance of the device. The inversion capacitance in the presence of D_{it} is given by

$$C_{inv} = \frac{C_{ox}C_{qw}}{C_{ox} + C_{qw} + qD_{it}}. \tag{3.5}$$



(a) Effect of D_{it} in the subthreshold region can be modeled as a parallel capacitance to the depletion capacitance.

(b) Effect of D_{it} on the on state of the device can be modeled as a parallel capacitance to the quantum well capacitance.

Figure 3.6: D_{it} effect in MOSFETs

In the previous analysis the density of states capacitance is ignored for simplicity. A Dit value of $1 \times 10^{12} cm^{-2}$ results an acceptable 2% reduction in the inversion capacitance and 0.1 V shift in the threshold voltage ($\Delta V_t = \frac{qD_{it}}{C_{ox}}$). A summary of the required dielectric parameters is shown in Table. (3.3).

Table 3.3: Target high-k dielectric parameters for 22 nm $In_{0.53}Ga_{0.47}As$ MOSFET.

c_{eot} (nm)	D_{it} (cm^{-2})	t_{ox} (nm)	κ_{ox}
0.5	1×10^{12}	≥ 3	≥ 16

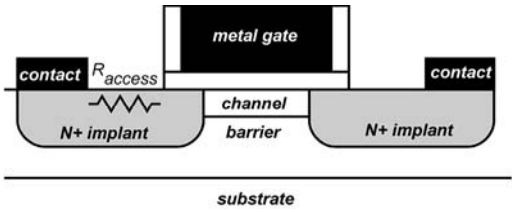


Figure 3.7: Cross-section schematic of an ion-implanted MOSFET.

3.1.4 Source Resistance

As described in Sec. (2.2.3) the source access resistance degrades the available drive current and transconductance. From Eq. (2.11) even a source resistance of 25 $\Omega - \mu m$ will degrade the drive current to 2.7 $mA/\mu m$. Fig. (2.12) shows various component of the source resistance. With a contact length L_c of 22 nm for 22 nm L_g device Eq. (2.17) gives a required contact resistance of 0.5 $\Omega - \mu m^2$ and a sheet resistance of 400 $\frac{\Omega}{\square}$ in a 5 nm thick $n+$ layer. Such low sheet and contact resistances would require an extremely high active doping ($\geq 2 \times 10^{19} cm^{-3}$) in the semiconductor. Besides low sheet and contact resistances, both the vertical and lateral doping profile needs to be abrupt ($\sim$5 nm) in order to control short channel effects. Fig. (3.7) shows an schematic diagram of an ion implanted MOSFET with deep junctions. As a result of the lateral diffusion of dopants, drain to source distance is reduced and consequently the DIBL is increased.

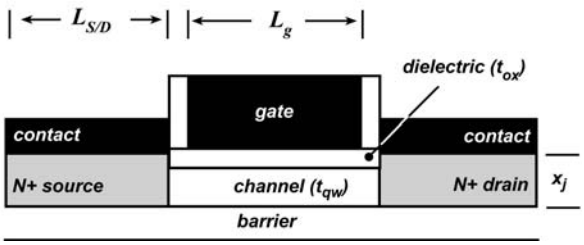


Figure 3.8: 22 nm $In_{0.53}Ga_{0.47}As$ MOSFET structure.

3.2 Conclusions

In this chapter we designed a 22 nm L_g InGaAs n-MOSFET giving the design parameters. The MOSFET has a simulated peak drive current of 3 $mA/\mu m$ and peak transconductance of 4.4 $mS/\mu m$. The device structure and parameters to realize this transistor is summarized in Table (3.4) and Fig. (3.8).

Table 3.4: 22 nm $In_{0.53}Ga_{0.47}As$ MOSFET parameters.

Gate dielectric	0.5 nm EOT, $t_{ox} > 3$ nm, $D_{it} \leq 1 \times 10^{12}\ cm^{-2}$
Channel	5 nm
Source resistance	$\leq 50\ \Omega - \mu m$, $L_{s/d} = 22$ nm $\rho_c \leq 1.0\ \Omega - \mu m^2$, $x_j = 5$ nm $R_{sh} = 400\ \Omega/\square$

Chapter 4

InGaAs MOSFET with self-aligned Source/Drain by MBE regrowth

In this chapter we will describe the self-aligned MOSFET technology developed in order to meet the design targets for 22 nm L_g InGaAs n-MOSFETs. The device structure is same as designed in last chapter, however the minimum gate length of the devices was limited to 200 nm as set by the optical lithography tool at UCSB Nanofab cleanroom. However the technology is scalable to 22 nm gate lengths by using electron beam lithography for gate definition.

4.1 High-k Dielectric on InGaAs

Unlike silicon dioxide passivation of Si, the native oxide of nearly all III-V semiconductor pins the Fermi level at midgap with surface states density [35].

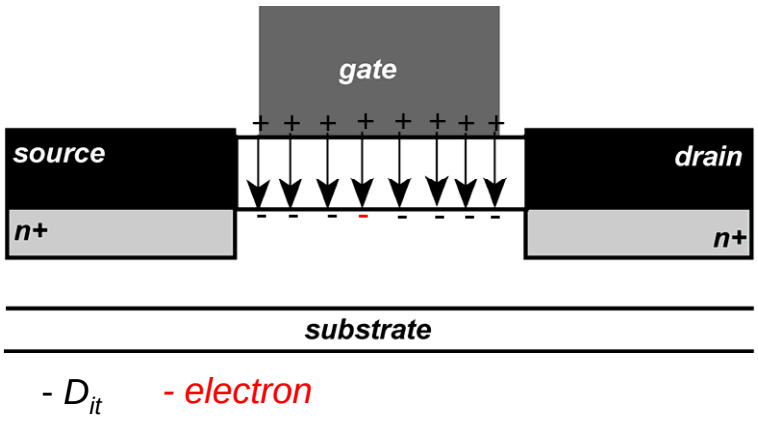


Figure 4.1: Device cross-section schematic showing the effect of high D_{it} in III-V MOSFETs.

As a result III-V MOSFET drive currents were limited because the applied gate electric fields terminate on the surface states rather inducing electrons in the channel (Fig. 4.1). Application of larger gate voltage results in the breakdown of the gate dielectric. Also unlike H passivation of Si by HF treatment, III-V materials lack good surface passivation techniques which made it difficult to get low D_{it} gate dielectrics on III-V semiconductors. The origin of surface states in III-V semiconductors is attributed to oxygen adsorption [36]. So, a high-k gate dielectric deposition process where the III-V channel is not exposed to oxygen may be a viable technique for low D_{it} dielectric-semiconductor interface. Arsenic capping of the $In_{0.53}Ga_{0.47}As$ channel after MBE growth before transferring to an oxide deposition system is being investigated as an effective technology for low

D_{it} gate dielectrics [37]. Various other gate dielectrics and deposition techniques are also being investigated by different groups [29, 30, 32, 38, 39].

The focus of this thesis is not high-k dielectric development on $In_{0.53}Ga_{0.47}As$, but a MOSFET technology development which would realize drive currents not limited by the source resistance, given a good dielectric. The gate dielectric used in this work was Al_2O_3 deposited by atomic layer deposition. After a 5 nm thick $In_{0.53}Ga_{0.47}As$ channel was grown by MBE, the wafer was then cooled down to 50 °C and 80 nm of arsenic was deposited. The wafers were then transferred in a vacuum container to Paul McIntyre Lab, Stanford University, where they were loaded into an atomic layer deposition tool (ALD), the arsenic cap layer desorbed at 480 °C [37], and Al_2O_3 gate dielectric was deposited. The wafers were than transferred back to UCSB for device fabrication.

4.1.1 Source-Drain Regrowth

From Sec. (3.1.4) the maximum source access resistance design target is 50 $\Omega - \mu m$ for 22 nm L_g InGaAs channel MOSFETs. Unlike silicon, ion-implantation may not a viable technique in III-V semiconductors due to a number of difficulties as described below. The III-V ternaries usually have high residual damage even after annealing, and these defects compensate shallow dopants making it difficult to achieve target high carrier densities [40]. Moreover, loss of group V

elements during high temperature anneals irreversibly ruins the stoichiometry of the semiconductor [40] and thus increases the resistance. The surface damage from ion-implantation may increase the contact resistance. The residual damage may also increase the junction leakage. The difficulty is made more serious in the presence of a bottom confinement InAlAs layer. Furthermore abrupt vertical and lateral dopant profile is necessary for sub-22nm gate length devices to control short channel effects. The lateral straggle of the ion implantation needs to be small ($\sim$ 5 nm) in order to avoid punch through from source to drain when the gate length is scaled beyond 22 nm L_g. Ion implanted InGaAs MOSFETs have been demonstrated with good output characteristics at longer gate lengths (~ 0.4 μm), but show severe short channel and punch through effects at deep sub-micron gate lengths ($\sim$ 100 nm) [41, 42]. The deep sub-micron ion implanted MOSFETs also show high junction leakages [41, 42].

Traditionally, epitaxial growth techniques such as metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE) and chemical beam epitaxy (CBE) have been the strength of III-V semiconductors. These epitaxial techniques can all produce high active doping densities ($4 - 10 \times 10^{19}$ cm^{-3}) in InGaAs without the necessity of high temperature anneals. These densities are higher than available by ion implantation and avoid the damage and crystal disordering

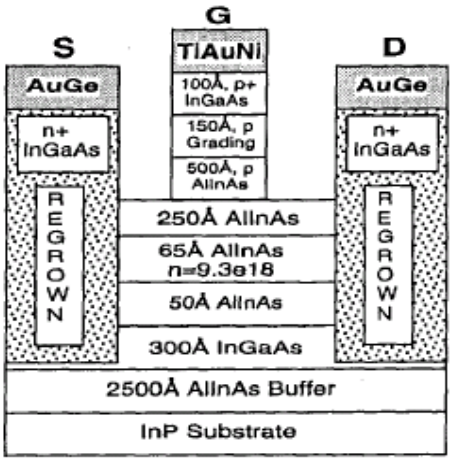


Figure 4.2: Device cross-section schematic of a JHEMT with source/drain regrowth [43].

from implantation as well. In addition, *in-situ* Mo contacts to n^{++} $In_{0.53}Ga_{0.47}As$ have shown very low 1.0 $\Omega - \mu m^2$ contact resistivities [24].

In this thesis, InGaAs MOSFETs with n^+ source/drain regions formed by MBE regrowth and self-aligned *in-situ* Mo contacts are developed and demonstrated. Source/drain regrowth to minimize the access resistance in HEMTS has been investigated previously by various groups [43–46]. These devices had either non-self aligned source/drain or non-self aligned contacts as shown schematically in Fig. (4.2). The n^+ source/drain regions were also deep, extending below the channel, making them susceptible to short channel effects in deep sub-micron gate length devices. A cross-section schematic of the self-aligned source/drain regrowth MOSFET studied in this thesis is shown in Fig. (4.3). The key feature of

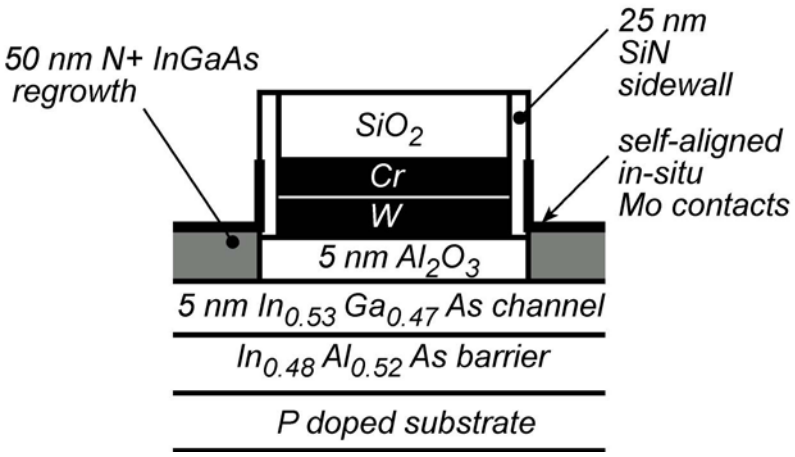


Figure 4.3: Device cross-section schematic of scaled channel $In_{0.53}Ga_{0.47}As$ MOSFET with self-aligned source/drain regrowth and self-aligned contacts.

this technology are self-aligned source/drain, self-aligned source/drain contacts, scaled channel ($\sim$ 5nm) suitable for 22 nm L_g devices. In the following section we describe the fabrication technology to realize the structure shown in Fig. (4.3).

The overall process flow is shown schematically in Fig. (4.4); first 5 nm InGaAs channel with InAlAs back barrier is grown on InP substrate by molecular beam epitaxy (MBE) and capped with arsenic. The cap layer was desorbed *in-situ* in an atomic layer deposition (ALD) chamber at 480 °C, and 4.7 nm of Al_2O_3 was deposited. A dry etched metal gate stack was then defined and sidewalls deposited. The high-k dielectric was wet etched and n^+ InGaAs is regrown by MBE for source/drain definition. Next self-aligned *in-situ* Mo contacts were defined. The final device (Fig. 4.3) has both self-aligned source/drain and contacts, the source

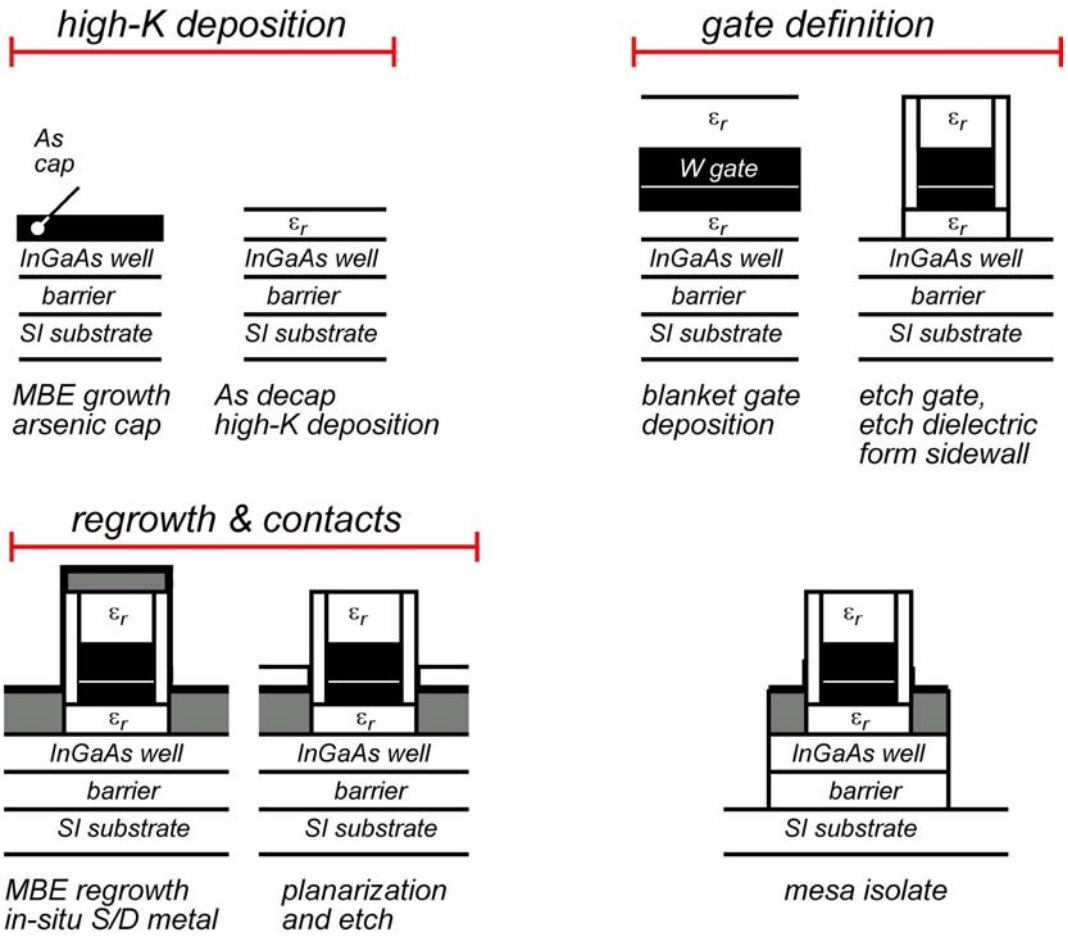


Figure 4.4: Process flow schematic for self-aligned source/drain $In_{0.53}Ga_{0.47}As$ channel MOSFET

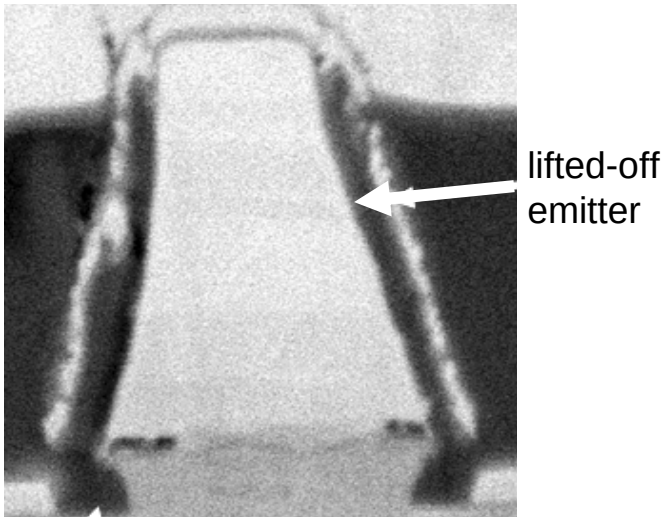


Figure 4.5: Cross-section scanning electron microscope [47] image of an HBT emitter showing the slanted sidewall profile.

access distance given by the well controlled SiNx sidewall thickness. The details of the process is discussed in the following sections.

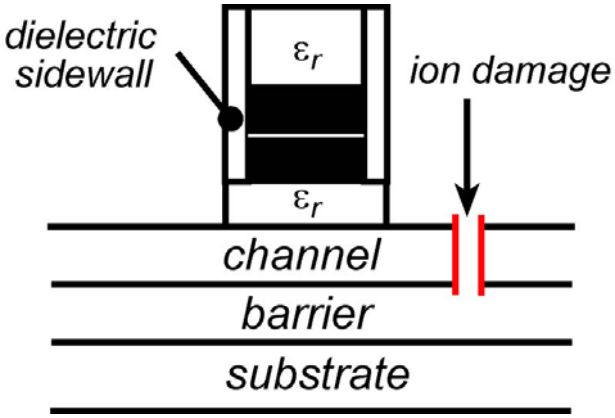
4.1.2 Gate Process

Traditionally, gates in III-V HEMTs have been fabricated using lift-off technique. But this technology may not be scalable to 22 nm L_g self-aligned MOSFETs because of the profile as seen in Fig. (4.5). The slant profile makes it hard to scale to deep sub-micron gate lengths. This also makes it difficult to form self aligned contacts using sidewalls which are formed by anisotropic dry etch. Gates

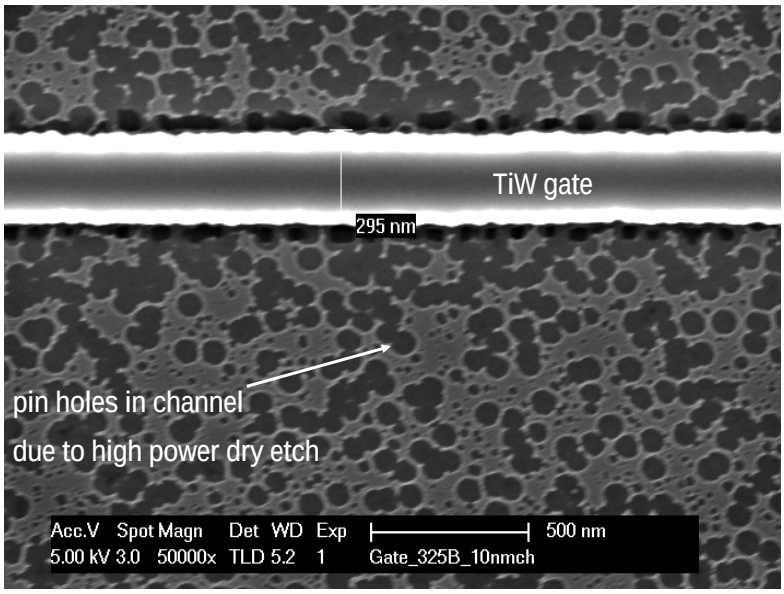
with vertical profile formed by dry etch is a preferred process for deep sub micron gate lengths.

The gate process for regrown MOSFET process has to meet a number of criterion before being loaded into MBE for regrowth. The gate metal must be encapsulated in all directions with dielectric in order to avoid possible metal contamination in the MBE chamber. High diffusivity metals like Au, Al have to be avoided to prevent contamination to MBE. So, refractory gate metals with high melting points are preferred. High quality regrowth by MBE requires a damage-free starting surface. Thin channel layers ($\sim$ 5 nm) are prone to ion damage and contamination during processing (Fig. 4.6). A damaged channel layer would result in imperfect S/D regrowth, which leads to high source resistances. Additionally, any pinholes introduced in this layer would expose the underlying InAlAs layer. The aluminum containing layer is rapidly oxidized in air which can prevent good epitaxial regrowth. Fig. (4.7) shows the faceted and resistive poly-InGaAs which results from regrowth on the damaged channel (Fig. (4.6(b))) after a high power dry etch.

Therefore a multiple layer gate stack is defined in which each layer is an etch stop for the layer above it (Fig. 4.8(a)). The top Cr layer was used as a dry etch mask after patterning it with photoresist and i-line photolithography, followed by a Cl_2/O_2 dry etch. The Cr was removed before the channel was exposed. Next,



(a) Cross-section schematic showing ion damage to 5 nm channel.



(b) Top view SEM of a TiW gate on 5 nm channel defined by 150 W RF power dry etch. The high power etch causes pinholes in the channel. A 5 second selective InAlAs etch was done to improve contrast in the SEM.

Figure 4.6: Ion damage to thin channels.

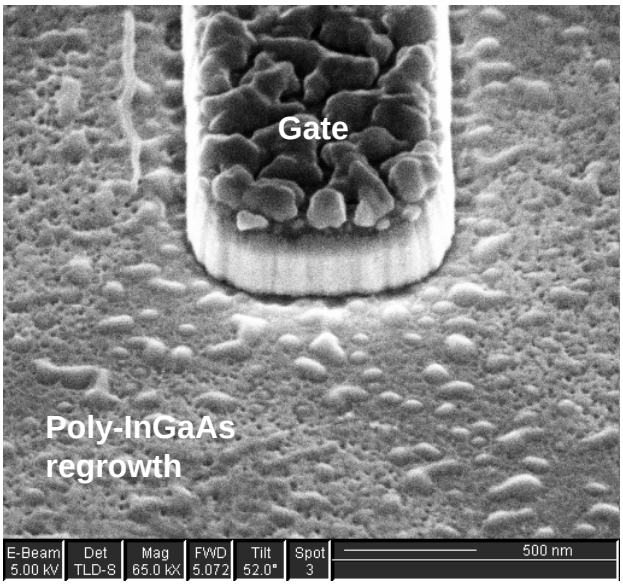
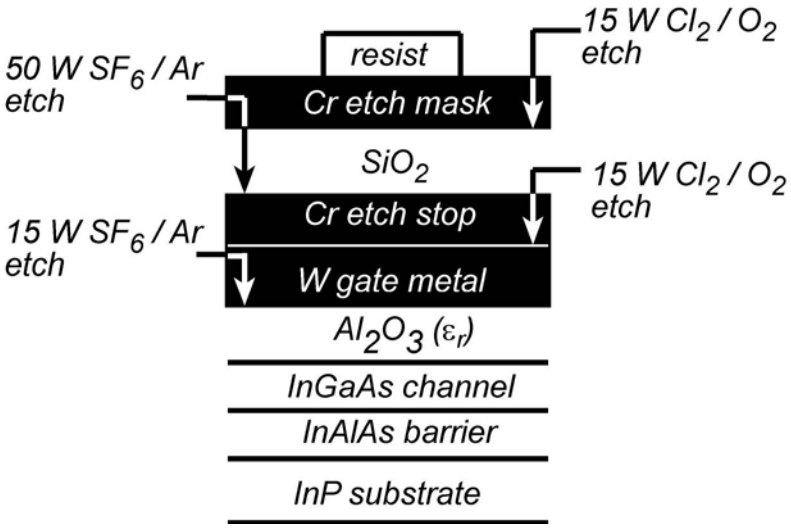
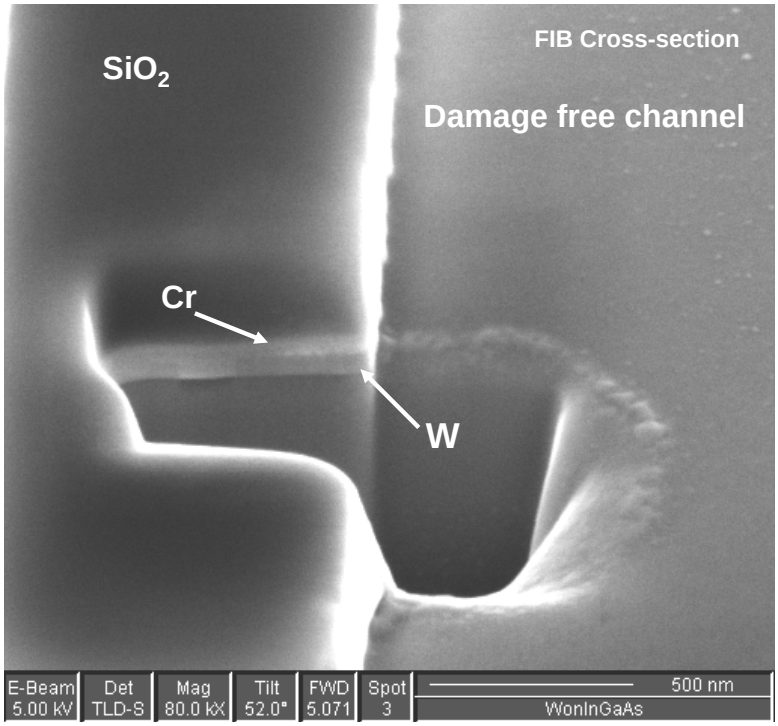


Figure 4.7: Oblique view SEM of faceted poly-InGaAs regrowth on ion damaged channel shown in Fig. (4.6(b)).

before the SiO_2 was etched, the photo-resist was stripped and O_2 plasma etched; the SiO_2 protected the channel from damage, and the aggressive O_2 etch prevented organic contamination of the MBE chamber. The alternating selective dry etch scheme (Fig. 4.8(a)) allows a final low power dry etch of the W layer without damaging the channel. As a result, 300 nm long and 400 nm thick gate stacks with vertical sidewall profile were fabricated on 5 nm $In_{0.53}Ga_{0.47}As$ channel (Fig. 4.8(b)). The process is scalable and can be used to fabricate sub-50 nm gate features by using electron beam lithography.



(a) Multiple layer gate stack and alternating selective dry etch process for gate definition



(b) Focused ion beam cross-section SEM of a dry etched gate stack showing an apparently undamaged 5 nm $In_{0.53}Ga_{0.47}As$ channel.

Figure 4.8: Dry etched gate process

4.1.3 Sidewall and Al_2O_3 etch

In the self-aligned structure the source access distance is set by the sidewall thickness, so it needs to be minimized as much possible at the same time electrically isolating source/drain from gate. Also, unlike Si MOSFETS, the raised source/drain structure (Fig. 4.9) where the n^+ $In_{0.53}Ga_{0.47}As$ is regrown on the $In_{0.53}Ga_{0.47}As$ channel, does not have doping under the sidewalls. The electron spill over from the n^{++} source layer provides the link from source to channel. Fig. (4.9) shows the electron concentration profile under sidewall simulated in Atlas for different sidewall thicknesses. The electron concentration is $> 1 \times 10^{19}$ cm^{-3} under 10 nm sidewall. But the concentration under sidewalls drops rapidly with increasing sidewall thickness and drops to $\sim 4 \times 10^{18}$ cm^{-3} for 30 nm sidewalls which adds $\sim$60 $\Omega - \mu m$ to the source resistance. Table (4.1) shows the added contribution to the source access resistance from the region under the sidewall. The sidewalls need to be a maximum of 20-25 nm in the proposed raised source/drain MOSFETs. Pulse doping in the back barrier can further provide more electrons in this region to reduce source access resistance.

A recessed source/drain regrowth FET (Fig. (4.10)) where the regrowth is done on a phosphide sub-channel layer relaxes the sidewall thickness requirement. This structure can provide conduction under the sidewall by the regrowth of the

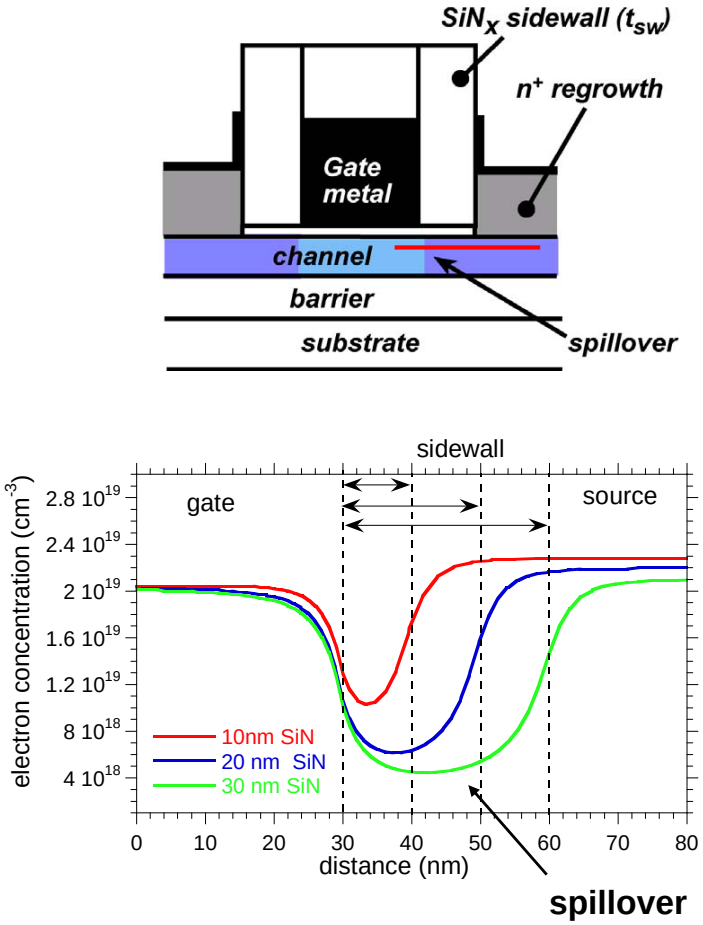


Figure 4.9: Raised source/drain FET. Electron spill over from n^+ region provides the necessary carriers under the sidewall. 2-D electrostatics Atlas simulation of electron concentration profile in the channel going from the active device to the source region. There is $\sim 1 \times 10^{19}\ cm^{-3}$ electrons under 10 nm sidewall.

Table 4.1: Source resistance contribution for different sidewall thicknesses.

t_{sw} (nm)	n (cm^{-3})	R_s ($\Omega - \mu m$)
10	$\geq 1 \times 10^{19}$	~ 6
20	$\geq 5 \times 10^{18}$	~ 20
30	$\sim 4 \times 10^{18}$	~ 60

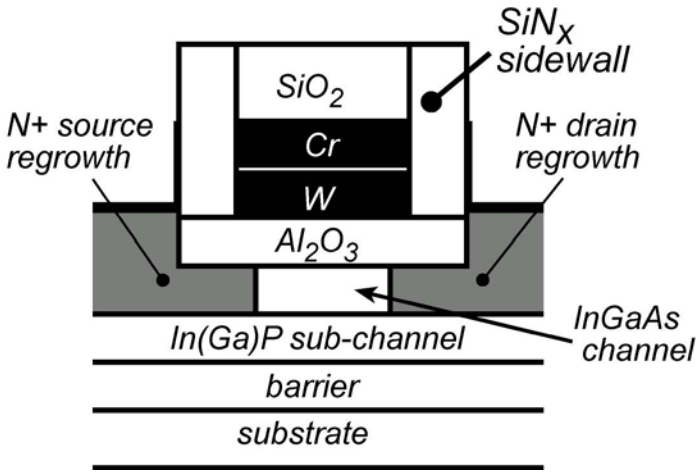


Figure 4.10: Recessed source/drain MOSFET. MBE regrowth fills in n^+ material under the sidewalls.

n^{++} material under the sidewalls. The challenge in this structure is filling the 30 nm by 5 nm region by regrowth.

Silicon nitride sidewalls are used in the devices presented in this thesis. A 25 nm sidewall is defined by blanket PECVD deposition and a low power anisotropic ICP RIE etch. The RIE power is kept low to ensure minimal damage to the 5 nm channel. Fig. (4.11) shows a cross-section SEM of a gate showing 20-25 nm thick sidewalls.

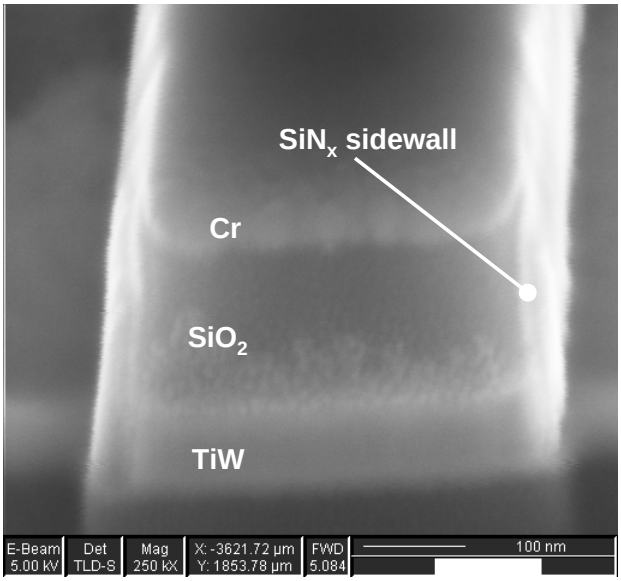


Figure 4.11: FIB cross-section SEM of gate stack with 20-25 nm SiN_x sidewalls.

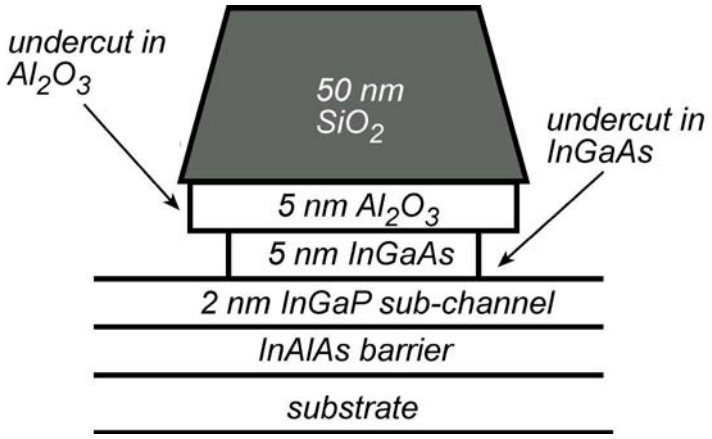
The final high-k dielectric etch is a very critical etch. A selective wet etch which does not etch the SiN_x sidewalls, the top SiO_2 cap and 5 nm $In_{0.53}Ga_{0.47}As$ channel is required. A wet etch is preferred over dry etch so that there is no ion damage to channel on which regrowth will occur. An overetch is required in order to make sure there is no trace of high-k on the channel which may hinder the regrowth, this is particularly very important in the case of Al_2O_3 as any trace Al will oxidize making the regrowth difficult. At the same time the undercut needs to be minimum. The Al_2O_3 dielectric in the MOSFETs are wet etched in dilute KOH (AZ 400K developer), which selectively stops on the 5 nm $In_{0.53}Ga_{0.47}As$ channel. There is ≤ 5 nm undercut in this wet etch as seen in the high resolution

cross-section transmission electron microscope (TEM) image in Fig. (4.12(b)). In these samples the dielectric was 100 % overetched. Fig. (4.13) shows an SEM of the gate after high-k etch showing a pin holes free channel before regrowth.

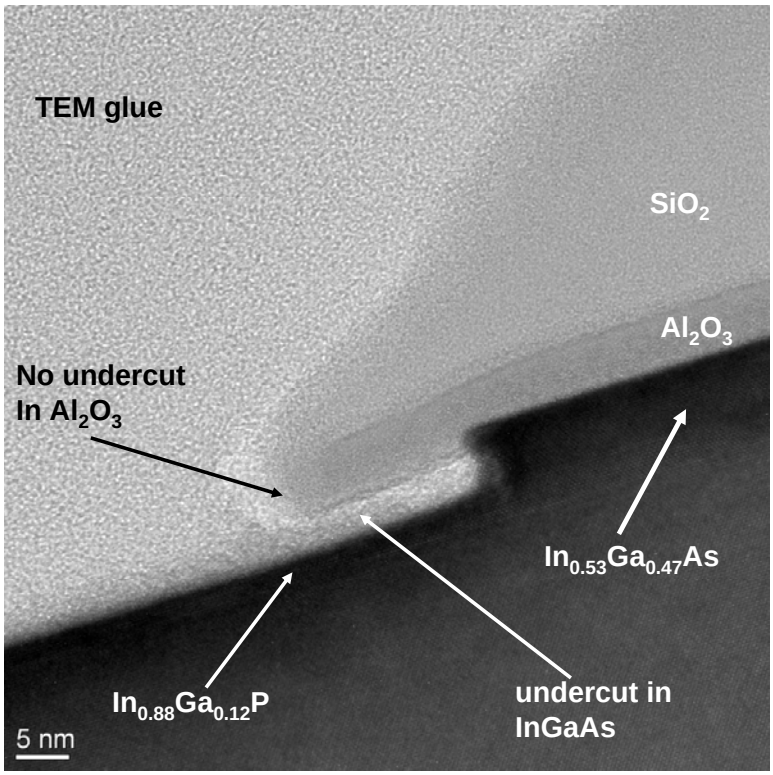
4.1.4 Source/drain regrowth and contacts

The wafer was then cleaned by exposure to UV-ozone, followed by a 1 minute dilute HCl treatment and a DI rinse. Following cleaning, the wafer was immediately loaded into the MBE chamber and cleaned with atomic H at 400 °C for 30-60 minutes. The wafer was then heated to 560 °C under arsenic overpressure to thermally desorb any native oxide on the channel. A c(4×2) reconstruction was seen in reflection high electron energy diffraction (RHEED) before regrowth indicating an epi-ready surface. 50 nm of Si doped $In_{0.53}Ga_{0.47}As$ or InAs source/drain was grown. Fig. (4.14) shows an high-resolution TEM of $In_{0.53}Ga_{0.47}As$ regrowth on $In_{0.53}Ga_{0.47}As$ following the above mentioned cleaning procedure.

After growth the wafer was transferred under ultra high vacuum (UHV) to an electron beam evaporator connected to the MBE and 20 nm of molybdenum (Mo) was deposited for source/drain contacts. As deposited, the Mo film covered the entire wafer surface, bridging over the dielectric-encapsulated gate, and therefore short-circuited the source and drain electrodes. This source/drain contact metal covering the gate electrode was therefore removed with a height-selective etch [48].



(a) Cross-section schematic of the TEM sample prepared to study the undercut in Al_2O_3.



(b) High resolution TEM of a SiO_2 gate, showing negligible undercut in Al_2O_3 from the SiO_2 mask edge. The Al_2O_3 was 100 % overetched.

Figure 4.12: TEM sample to study the undercut in Al_2O_3 etch. TEM image by Dr. Joël Cagnon, Prof. Susanne Stemmer group, UCSB.

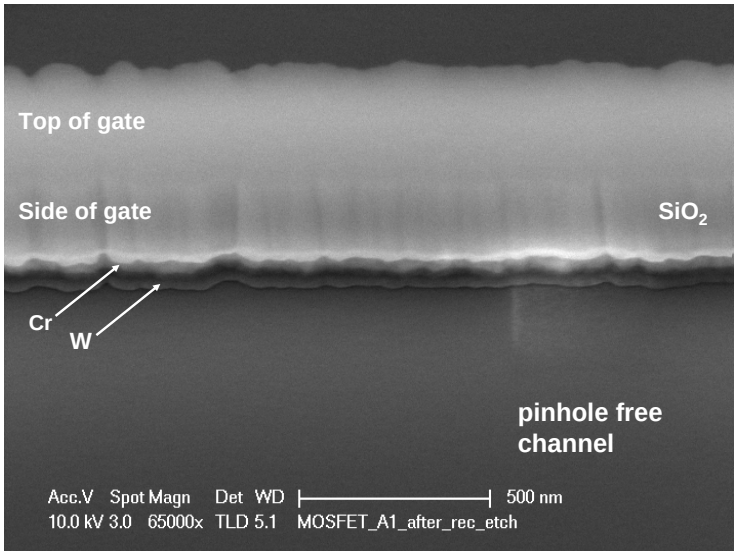


Figure 4.13: Oblique view SEM of a W/Cr/SiO_2 gate defined on 5 nm $In_{0.53}Ga_{0.47}As$ channel before regrowth showing apparently clean surface.

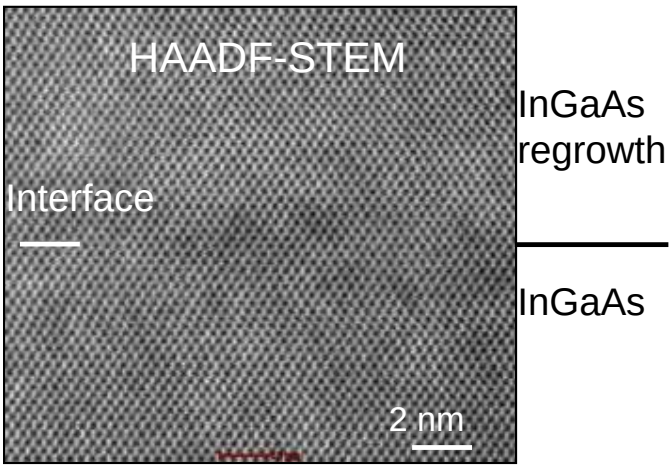


Figure 4.14: High-resolution TEM of $In_{0.53}Ga_{0.47}As$ regrowth on $In_{0.53}Ga_{0.47}As$, showing a crystalline epitaxial regrowth. MBE regrowth was done by Dr. Mark Wistey and TEM by Dr Joël Cagnon.

In this process (Fig. (4.15)) the wafer was planarized by spinning SPR-510 photo-resist. Then the photo-resist was etched back in a ICP ashing chamber till the tops of the gates are exposed. The Mo on tip of the gates was etched in a low power SF_6/Ar etch with the remaining PR as etch mask. The PR was stripped to give a self-aligned S/D MOSFET. Fig. (4.15) shows a cross-section SEM of device after height selective etching showing the self-aligned source/drain contacts. Source/drain pads were then deposited and devices mesa-isolated. To contact the gates, the silicon dioxide covering the gate pads was removed by etching in buffered HF.

For RF measurements, the back-end process similar (Fig. (4.16(a))) to UCSB InP DHBT process [47] was adapted. Source/drain and gate posts are lifted off, planarized using benzocyclobutene (BCB), etched back in CF_4/O_2 ICP ashing chamber and interconnect metal and pads are deposited. Fig. (4.16(b)) shows a SEM of the device with back end processing.

4.2 Conclusions

A scalable dry etched gate process was developed minimizing the damage to thin channel. *Ex-situ* wet clean and *in-situ* H clean of the wafers left an epi-ready surface suitable for high quality MBE regrowth. A self-aligned source/drain

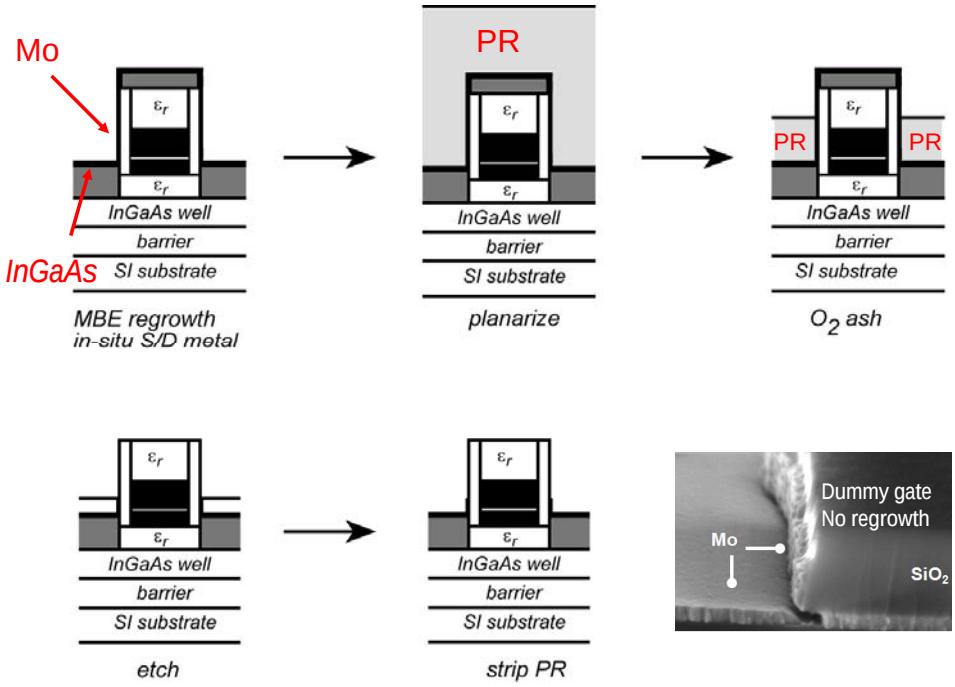
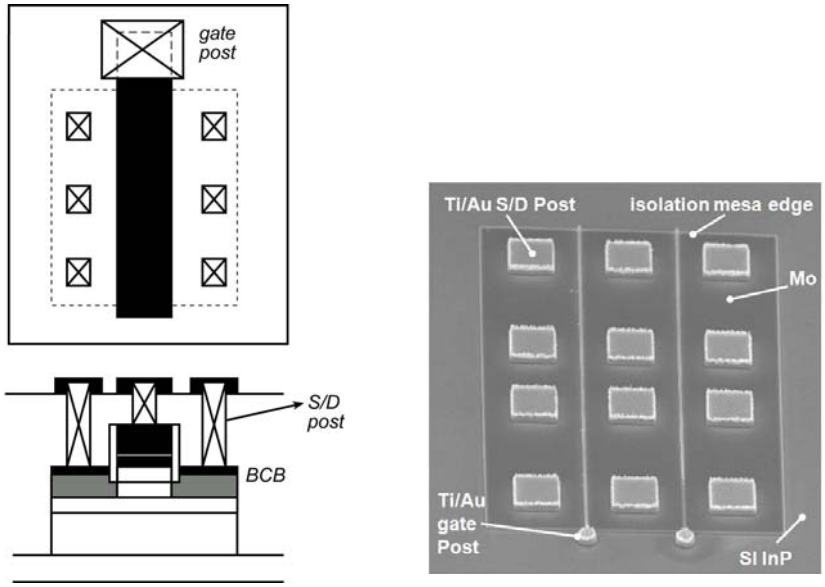


Figure 4.15: Process flow schematic of the height selective etch to define self-aligned source/drain contacts. SEM by Greg Burek.



(a) Cross-section schematic of the MOSFET after back-end process.

(b) Top view SEM of MOSFET after s/d and gate post deposition.

Figure 4.16: MOSFET back-end process.

contact scheme was also developed using height selective etching. In the next chapter we discuss the results of the MOSFETs fabricated using this process.

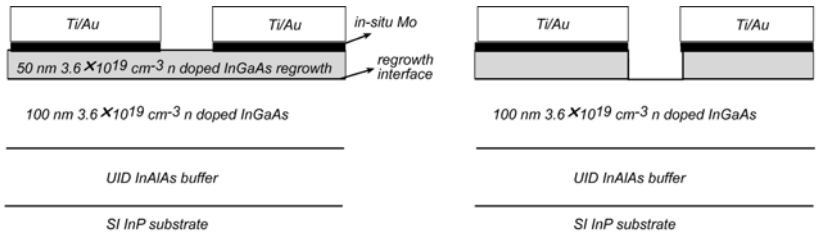
Chapter 5

MOSFET and contact results

In this chapter we will describe the FET and contact results of the regrowth MOSFETs. The results will be presented in a near chronological order. All the MBE regrowths on these devices were carried out by Dr. Mark Wistey. In all the TLM data presented here the finite interconnect metal resistance correction as described in [24] has been applied.

Table 5.1: List of commonly used abbreviations.

DIBL	Drain induced barrier lowering
MBE	Molecular beam epiaxy
MEE	Migration enhanced epitaxy
RHEED	Reflection high electron energy diffraction
TLM	Transfer length method



(a) TLM structure on the regrowth.

(b) TLM structure to measure interface resistance. The regrown materials between TLM pads was wet etched to force the current through the regrowth interface.

Figure 5.1: Regrowth TLM

5.1 Regrowth on processed wafers

The TEM shown in Fig. (4.14) is of $In_{0.53}Ga_{0.47}As$ regrowth on a un-processed wafer to establish a baseline regrowth process. 20 nm *in-situ* Mo was deposited on this wafer and TLMs were fabricated to evaluate the regrowth material quality, contact and interface resistances. Fig. (5.1) shows the cross-section schematic of the layer structure. TLMs were measured to extract the top Mo/regrowth InGaAs contact resistance and the sheet resistance. Next, a wet etch of 1:1:25 H_3PO_4:H_2O_2:H_2O was used to etch 50 nm (verified by Dektak Profilometer) into the $In_{0.53}Ga_{0.47}As$ (Fig. (5.1(b))), in order to force all current through the deeper regrowth interface, and the TLMs were measured again. The sample showed a specific contact resistivity of $\rho_c = 3.0\ \Omega - \mu m^2$ before etching. After the etch, it showed $\rho_c = 3.0\ \Omega - \mu m^2$, including both the M-S and regrowth interfaces giving

an upper limit of 3.0 $\Omega - \mu m^2$ for the n^{++}regrowth/n^{++} $In_{0.53}Ga_{0.47}As$ interface resistance. This result is comparable to the *in-situ* contacts on new, non-regrowth epitaxy [24].

The interface resistance number calculated above is the best case scenario. However, in a real transistor fabrication the source/drain regrowth is done on the channel which has been exposed to various processing steps. The regrowth on processed wafer could be bad if there is any residual contamination or damage introduced during various process steps. In order to evaluate the effect of gate process on regrowth, regrowths were performed on blanket wafers with various simulated processing done. Fig. (5.2) shows the SEM of regrowths done on various processed wafer. In all cases, after *ex-situ* and *in-situ* clean RHEED showed a c(4×2) pattern indicating epi-ready surface with minimum contamination from processing. The key to contamination free surface before regrowth is an immediate 3 minute DI rinse after every etch. This makes sure that any adsorbed etch products are washed away. X-ray photoelectron spectroscopy (XPS) was done on an InGaAs surface after a fluorine dry etch with and without DI rinse. The data (not shown here) showed that non-rinsed sample have substantial fluorine adsorption on the surface. TLM measurements on n^+ $In_{0.53}Ga_{0.47}As$ regrowth on n^+ InP gave an upper limit of 6.7 $\Omega - \mu m^2$. on the interface resistance.

Figure 5.2: SEM image of n^+ $In_{0.53}Ga_{0.47}As$ regrowth on various processed wafers. The surface is smooth and crystalline. The bright spots are "oval" defects used to focus the image.

5.2 First generation source/drain regrowth MOSFETs

Table 5.2: Layer structure of the recessed source/drain MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping (cm^{-3})
1	Oxide	Al_2O_3	4.7	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Sub-channel	InP	2.5	-
4	Setback	$In_{0.48}Al_{0.52}As$	5	-
5	Pulsedoping	$In_{0.48}Al_{0.52}As$	5	1×10^{17}
6	Buffer	$In_{0.48}Al_{0.52}As$	200	-
7	Substrate	InP	-	SI

The layer structure of the first regrowth MOSFET is shown in Table. (5.2) and the corresponding band diagram in Fig. (5.3). It is a recessed source/drain MOSFET with a composite 5 nm /2.5 nm InGaAs/InP channel. After the gate definition the Al_2O_3 dielectric was wet etched and 45 nm of SiNx sidewalls were defined. The top InGaAs channel was wet-etched stopping on InP sub-channel. The regrowth was done on 2.5 nm InP sub-channel. After *in-situ* H clean the RHEED showed a surface reconstruction, but RHEED immediately became spotty on start of regrowth indicating a faceted growth which was seen in SEM (Fig. (5.5(a))). This could be attributed to InP to InAs conversion during the initial stage of regrowth because of P→As exchange [49, 50]. The lattice mismatched InAs layer

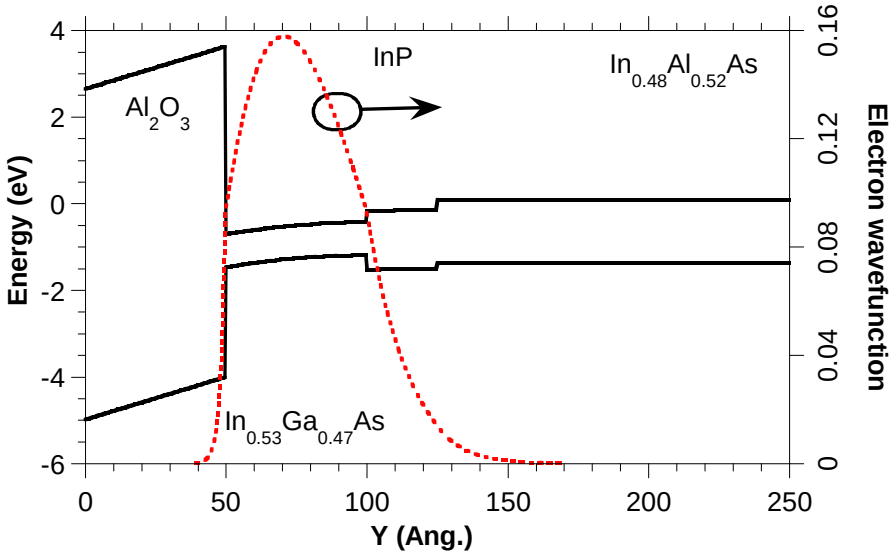


Figure 5.3: Band diagram of recessed source/drain MOSFET

relaxed, and the subsequent InGaAs growth became rough. This phenomenon was confirmed by the failure of the selective arsenide wet etch to stop on the InP layer after regrowth. Spotty RHEED and rough InGaAs regrowth were also observed (Fig. (5.5(b))) on unprocessed wafers with 2.5 nm InP on $In_{0.48}Al_{0.52}As$. A similar rough surface was observed even in chemical beam epitaxy (CBE) growth. This strongly suggests that the problem was a growth related issue, rather than process related contamination. TLMs on the MOSFET regrowth layer gave a high sheet resistance of $310\Omega/\square$ and a contact resistance of 130 $\Omega-\mu m^2$. A MOSFET source resistance of 300 $\Omega - \mu m$ was expected from the TLM data and the self-aligned MOSFET structure. A low sheet resistance of 28 $\Omega/\square$ and contact resistance of

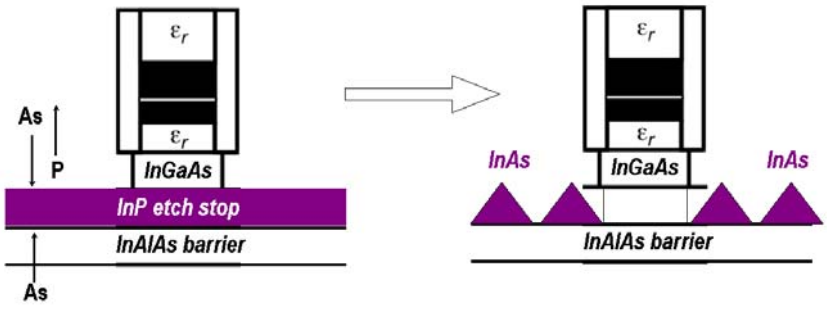
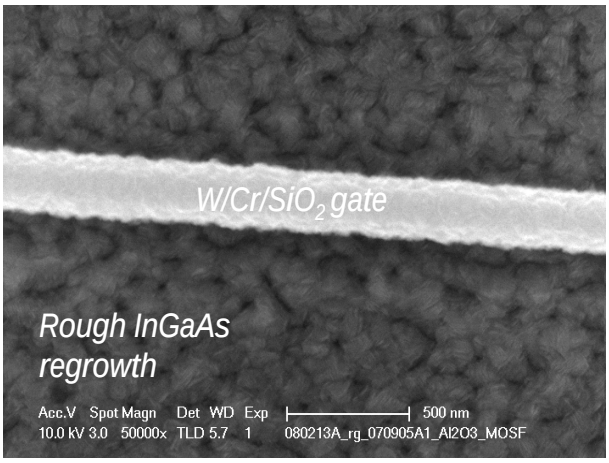


Figure 5.4: InP to InAs conversion on thin InP subchannel layers [51].

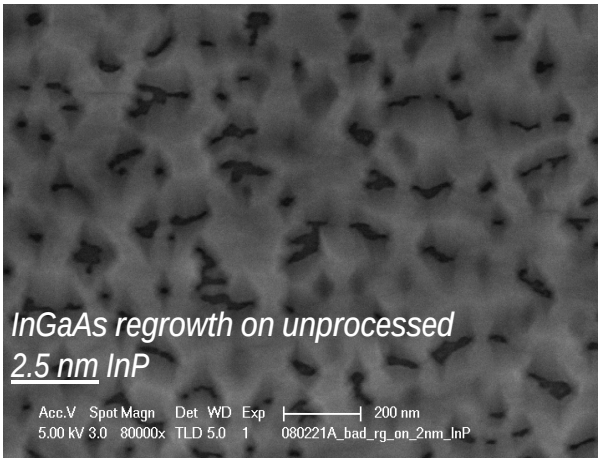
$9\ \Omega - \mu m^2$ were measured on a co-processed control wafer with no high-k and no InP, confirming the possibility of high quality regrowth on a processed wafer. We attribute the higher resistance observed in the MOSFET wafer to relaxation and rough growth on the thin InP layer.

Fig. (5.6) shows the output characteristics of a $10\mu m$ gate length device. The maximum drive current is $\sim 2\ \mu A/\mu m$ at $V_{gs} = 2.0V$ and $V_{ds} = 2.0V$. Similar low drive currents were observed for the shorter gate length devices. The $I_d - V_g$ characteristics showed an extremely high source resistance limited linear behavior with $R_{on} \sim 715\ k\Omega - \mu m$. The on resistance is orders of magnitude higher than the $300\ \Omega - \mu m$ source resistance calculated from the TLM structures.

A scanning electron microscope (SEM) image (Fig. (5.7(a)))of the device showed a 150-200 nm gap between the n^+ regrowth regions and the gate. Similar gaps in regrowth were observed on co-processed wafers with gates but without high-k (Fig. (5.7(b))). The gap is most likely due to shadowing by the gate during



(a) Top view SEM of the MOSFET after regrowth. The regrowth surface is rough.



(b) SEM of $In_{0.53}Ga_{0.47}As$ regrowth on unprocessed 2.5 nm InP on $In_{0.48}Al_{0.52}As$.

Figure 5.5: $In_{0.53}Ga_{0.47}As$ regrowth on thin InP.

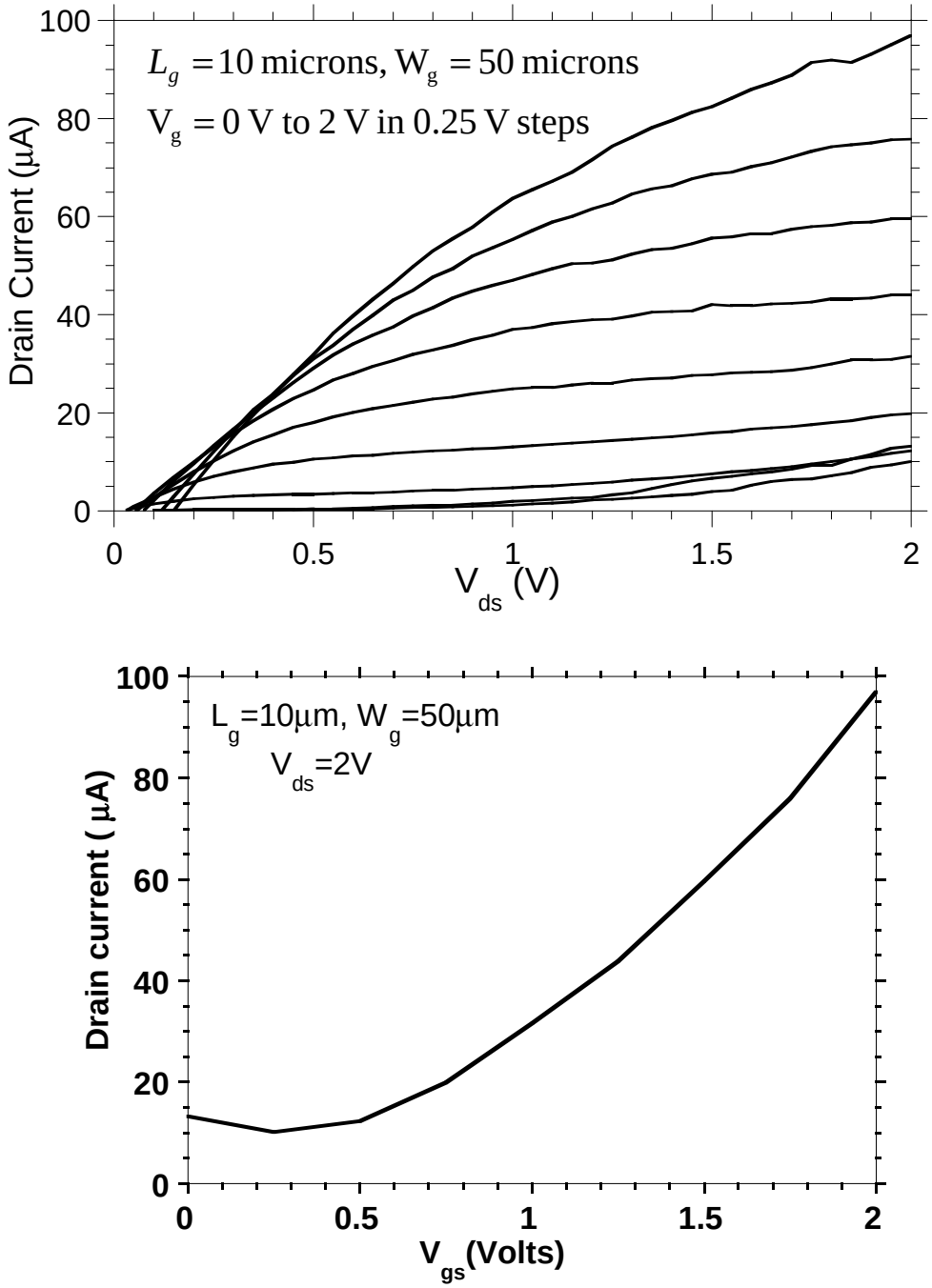
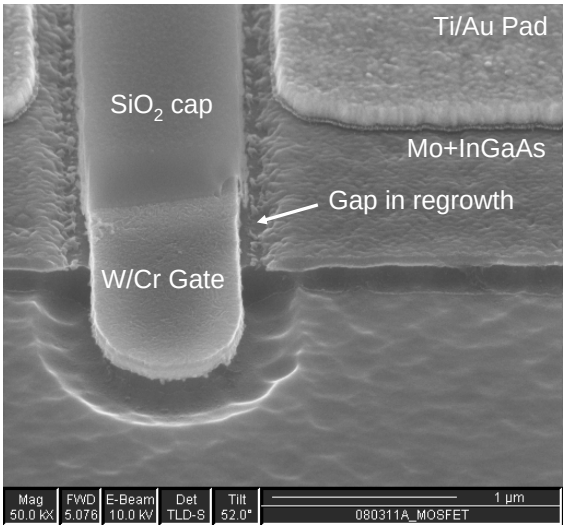


Figure 5.6: Output and input characteristics of the recess source/drain MOSFET

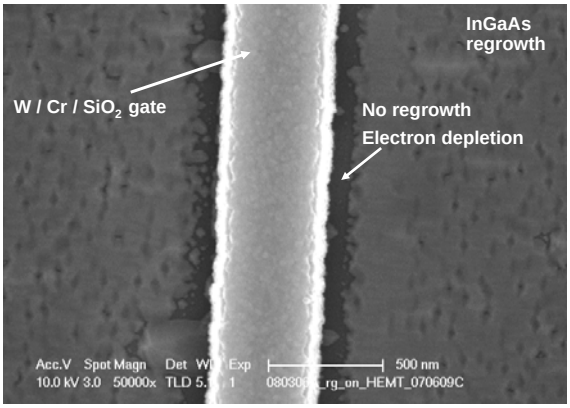
MBE regrowth and/or by a thin ($\sim$ 1 nm) layer of SiNx remaining on the surface near the gate even after the sidewall etch. But similar gap was also observed in process monitor wafers on which no sidewall was deposited. We attribute this to shadowing by the tall gate features as well as reduced surface mobility of group III adatoms at the growth temperature (400 °C). As a result, the channel surface next to gate is starved of group III elements, resulting in a gap [49]. Without the high doping from regrowth, the channel in the gap region is depleted of all electrons because of the pinning of Fermi-level well below the conduction band edge due to surface states. Fig. (5.8) shows $I_d - V_{ds}$ of a raised source/drain device where the InGaAs channel was not etched. The breakdown voltage is 8 V consistent with an InGaAs breakdown of 20 V/μm [52] for total S/D to gate gap of 400 nm as seen in SEM. Thus the low drive currents resulted from the undoped gaps in regrowth.

5.3 MEE regrowth and InGaP sub-channel

The two main reasons for the high source resistance are the inability to re-grow low resistance epitaxial InGaAs on thin InP sub-channel, and a gap region with no regrowth next to the gate. Instead of the thin InP layer, introducing a 2.5 nm strained $In_{0.88}Ga_{0.12}P$ (InGaP) sub-channel etch stop layer allowed successful



(a) Oblique view SEM of MOSFET after device isolation etch.



(b) Top view SEM of the co-processed wafer with no high-k. There is no regrowth next to gate.

Figure 5.7: Gap in regrowth next to gate.

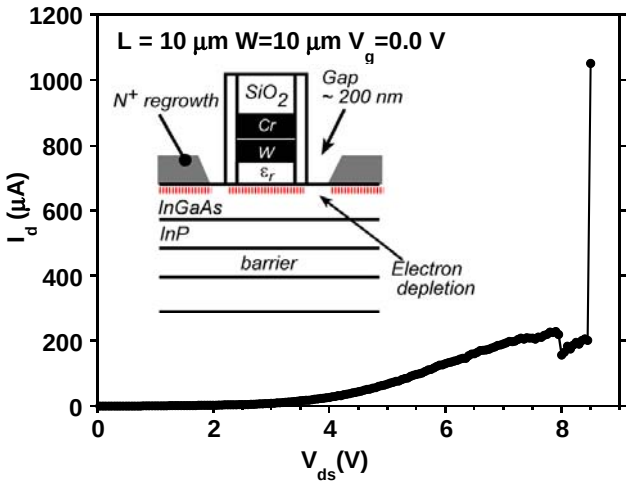


Figure 5.8: Zero gate bias breakdown characteristics of the raised source/drain $In_{0.53}Ga_{0.47}As$ MOSFET.

regrowth of low resistance InGaAs. A high temperature migration enhanced epitaxy (MEE) regrowth technique showed no gaps next to the gate. These will be discussed in the following sections.

$In_{0.53}Ga_{0.47}As$ regrowth on thick (80 nm) InP layer was smooth and crystalline without any faceting (Fig. (5.2)). The sheet resistance of the regrowth layer was low and comparable to $In_{0.53}Ga_{0.47}As$ regrowth on $In_{0.53}Ga_{0.47}As$. However the regrowth on thin 2.5 nm InP sub-channel was rough. A series of regrowth was done where the InP sub-channel thickness on $In_{0.48}Al_{0.52}As$ was varied from 2 nm to 10 nm. All the wafers showed surface reconstruction before regrowth but on start of regrowth the RHEED showed surface reconstruction only for wafers with sub-channel thicknesses $\geq 6nm$ [49–51]. This suggests that P to As exchange

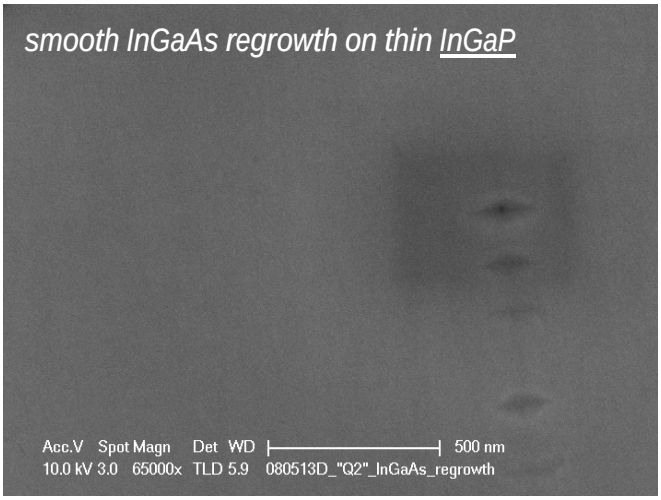


Figure 5.9: Top view SEM of $In_{0.53}Ga_{0.47}As$ regrowth on 2 nm $In_{0.88}Ga_{0.12}P$ on $In_{0.48}Al_{0.52}As$, showing smooth crystalline growth.

takes place and complete conversion of thin InP to InAs as the possible cause of observed rough growths on 2 nm InP sub-channel (Fig. (5.4)).

An $In_{0.88}Ga_{0.12}P$ sub-channel was studied as alternative to InP. The InGaAs/InP selective etch is also selective to $In_{0.88}Ga_{0.12}P$ and the top InGaAs channel can be etched stopping on the thin $In_{0.88}Ga_{0.12}P$ channel without exposing the underlying $In_{0.48}Al_{0.52}As$ layer. Moreover, P to As conversion would create strained InGaAs which will not relax and crystalline $In_{0.53}Ga_{0.47}As$ could be regrown.

Fig. (5.9) shows an SEM of blanket $In_{0.53}Ga_{0.47}As$ regrowth (with no gates) on 2.5 nm InGaP, showing smooth crystalline regrowth [50]. The RHEED showed surface reconstruction both before and during regrowth. TLMs on the 100 nm $In_{0.53}Ga_{0.47}As$ regrowth on $In_{0.88}Ga_{0.12}P$ showed a low 18 $\Omega/\square$ sheet resistance

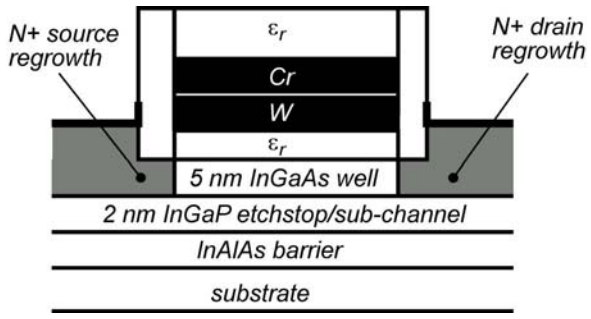
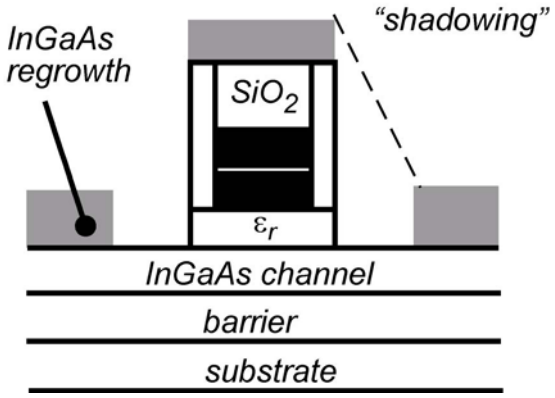


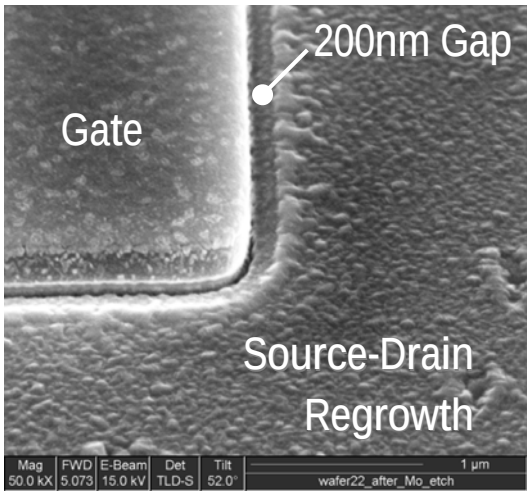
Figure 5.10: Cross-section schematic structure of recessed soure/drain MOSFET with $In_{0.88}Ga_{0.12}P$ sub-channel.

comparable to $In_{0.53}Ga_{0.47}As$ regrowth on $In_{0.53}Ga_{0.47}As$. The new recessed source/drain FET layer structure is shown in Fig. (5.10) and MOSFET results will be presented in the next section.

MBE is a line of sight deposition technique, the region next to gate can be shadowed by the gate. This will introduce gaps next to gate where there is no regrowth. Fig. (5.11(a)) shows a schematic and SEM of regrowth next to gate in MBE showing gaps next to gate. A migration enhanced epitaxy (MEE) regrowth where the group III atoms were deposited with a flux ratio V/III$\sim$ 3, separated by a 15 sec pulsing showed uniform filling in next to gate [49, 50]. Pulsing of the group III gives sufficient time for the adatoms on top of the gate to migrate down to the region next to gate. Fig. (5.12) shows cross-section SEMs of gate after MEE regrowths, showing no gap next to gate. Fig. (5.13) shows angled view SEMs of MEE regrowths near gate. From the SEMs it is clear that a higher



(a) Cross-schematic showing shadowing by gate.



(b) Top view SEM of MBE regrowth showing gaps because of shadowing effect.

Figure 5.11: Shadowing effect in MBE.

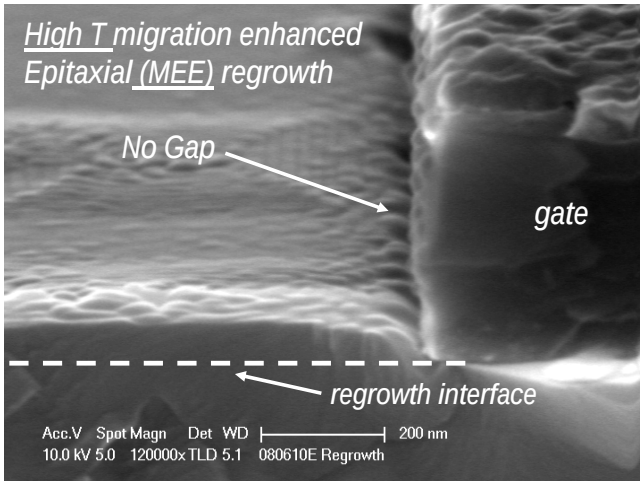


Figure 5.12: Cross-section SEM of a gate after MEE regrowth showing no gaps next to gate.

temperature MEE regrowth is preferred for lateral fill in and the regrowth filling is uniform across the wafer.

The 2nd generation of source/drain regrowth FETs were fabricated using MEE regrowth and InGaP sub-channel layer for recessed source/drain FETs.

5.4 MOSFETs with MEE regrowth

In this section we discuss the MOSFET results with MEE source/drain regrowth. MOSFETs with four different layer structures were fabricated. They are depletion mode and enhancement mode raised source/drain FETs; and depletion mode and enhancement mode recessed source/drain FETs. The schematics of

Figure 5.13: SEM image of MEE $In_{0.53}Ga_{0.47}As$ regrowth at two different growth temperatures. No gaps were observed across the whole wafer.

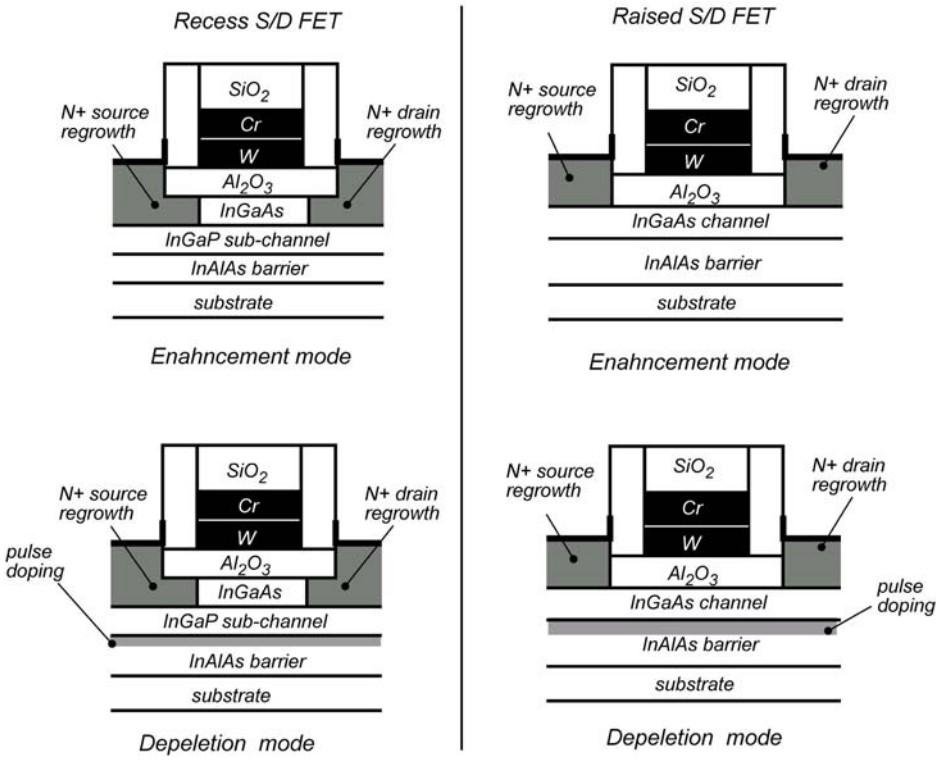


Figure 5.14: Cross-section schematics of the four different types of MOSFETs fabricated with MEE regrowth.

these devices is shown in Fig. (5.14). The depletion mode FETs had Si pulse doping in the InAlAs back barrier to compensate for any unexpected gaps and interfacial defects. Unlike the first generation of devices, the sidewall thickness on these devices were nominally 20-25 nm thick and were defined on top of the gate dielectric (Al_2O_3). This was done with the presumption that the D_{it} at the $In_{0.53}Ga_{0.47}As$ interface under the sidewall is controlled by the well investigated high-k process rather than SiNx/InGaAs interface.

5.4.1 Recessed source/drain FETs

The layer structure of the recessed source/drain FETs is shown in Tables (5.5, 5.4) and Fig. (5.15). The pulse doping in the depletion FETs was extremely high ($1 \times 10^{13} cm^{-2}$) because the D_{it} at the $In_{0.53}Ga_{0.47}As/Al_2O_3$ interface was completely unknown at the time of fabricating these devices. This ensured that there is sufficient carriers in the access region from the source contacts to the channel under the gate. There is a 10 nm $In_{0.48}Al_{0.52}As$ setback; a thick setback was chosen to minimize possible mobility degradation in thin ($\sim$ 5 nm) channel because of ionized impurity scattering.

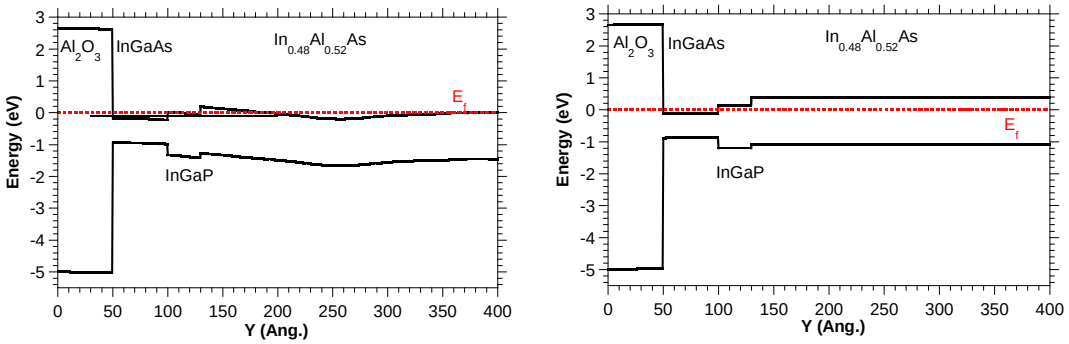
Table 5.3: Layer structure of the $In_{0.88}Ga_{0.12}P$ recessed source/drain depletion MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping n (cm^{-3})
1	Oxide	Al_2O_3	4.7	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Sub-channel	$In_{0.88}Ga_{0.12}P$	2.5	-
4	Setback	$In_{0.48}Al_{0.52}As$	10	-
5	Pulsedoping	$In_{0.48}Al_{0.52}As$	5	2×10^{19}
6	Buffer	$In_{0.48}Al_{0.52}As$	200	-
7	Substrate	InP	-	SI

Fig. (5.16) shows the SEMs on the recessed source/drain FETs after regrowth and *in-situ* Mo deposition. There is no apparent gap in regrowth next to gate. Figs. (5.17,5.18) show the $I_d - V_{ds}$ curves for recessed source/drain depletion MOSFET while the Figs. (5.19, 5.20) show the $I_d - V_{ds}$ curves for the enhance-

Table 5.4: Layer structure of the $In_{0.88}Ga_{0.12}P$ recessed source/drain enhancement mode MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping n (cm^{-3})
1	Oxide	Al_2O_3	4.7	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Sub-channel	$In_{0.88}Ga_{0.12}P$	2.5	-
4	Buffer	$In_{0.48}Al_{0.52}As$	100	-
5	Substrate	InP	-	SI



(a) Band diagram of the InGaP recessed source/drain depletion mode MOSFET (Table (5.5)) at V_g=0 V.

(b) Band diagram of the InGaP recessed source/drain enhancement mode MOSFET (Table (5.4)) at V_g=0 V.

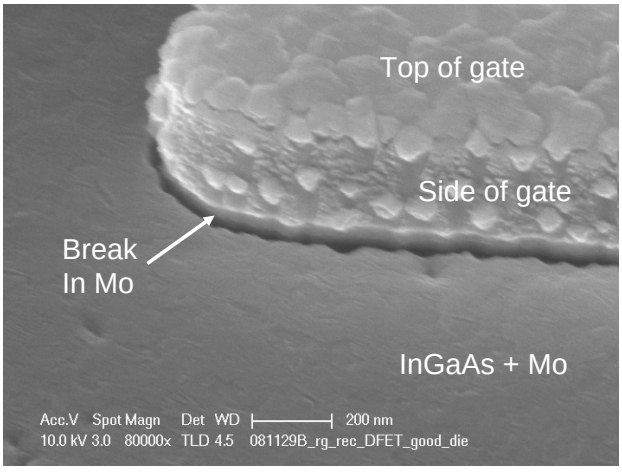
Figure 5.15: InGaP sub-channel recessed source/drain MOSFETs.

ment mode MOSFETs. The depletion mode devices with pulse doping show gate modulation with a transonductance of 0.2 $mS/\mu m$ for 1 μm L_g device. The depletion MOSFET has peak drive current of 1.1 $mA/\mu m$ at $V_{gs} = 2V$ and $V_{ds} = 2.0V$ for the 1μm L_g device, while the MOSFET with no pulse doping has a peak drive current of 0.1 $mA/\mu m$ for the 0.6 μm L_g device. The depletion mode devices with pulse doping do not turn off at all. This is because of the presence of a parasitic

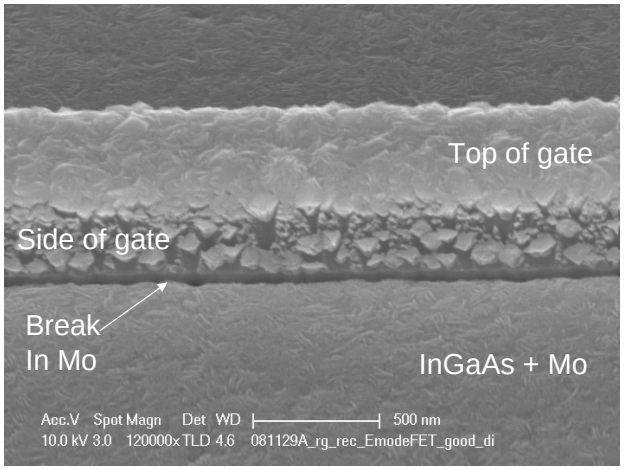
electron conduction layer in the pulse-doping layer with 10 nm setback as shown in Fig. (5.21). The MOSFETs with no pulse doping also do not turnoff. This also suggests a parasitic conduction path under the channel. There could be a parasitic conduction layer in the strained $In_{0.88}Ga_{0.12}P$ layer under the $In_{0.53}Ga_{0.47}As$ channel.

The total parasitic resistance can be estimated by studying devices at high gate voltages. The on resistance R_{on} Vs. L_g is plotted in Fig. (5.22), indicating that at L_g =0, a large series resistivity of 0.94 $k\Omega - \mu m$ remains. Similar analysis for the MOSFET with no pulse doping shows an extremely high series access resistance of $\sim$ 20 $k\Omega - \mu m$. The difference in the source access resistance between these two types of devices could be due to much larger electron depletion in the access region of MOSFET with no pulse doping.

A second series of recessed source/drain MOSFETs were fabricated. The setback in these devices was 5 nm and the Al_2O_3 thickness was 2.5 nm ($\sim$ 1.25 nm EOT). The gate process in these devices were done by Greg Burek. The output characteristics of these devices is shown in Figs. (5.23,5.24). The peak drive current and transconductance for these devices are 1.2 $mA/\mu m$ and 0.44 $mS/\mu m$ at $V_{gs} = 1.0V$ and $V_{ds} = 2.0V$ for the 0.6 μm L_g device. The larger transconductance compared to the previous recessed source/drain depletion MOSFETs due to the thinner dielectric. The off current in these devices was lower than the previous



(a) Angled SEM of InGaP sub-channel recessed source/drain depletion MOSFET.



(b) Angled SEM of InGaP sub-channel recessed source/drain enhancement MOSFET.

Figure 5.16: MOSFET SEMs after regrowth and Mo deposition.

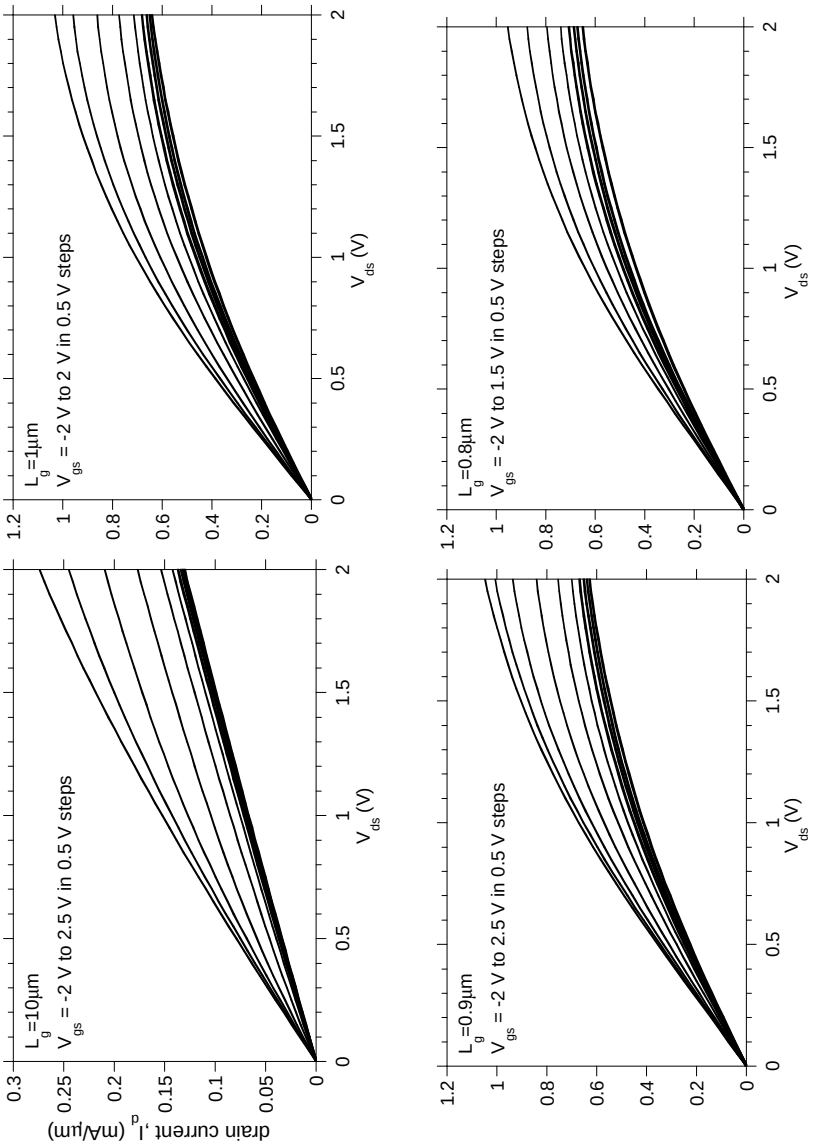


Figure 5.17: Output characteristics of InGaP sub-channel recessed source/drain depletion MOSFETs.

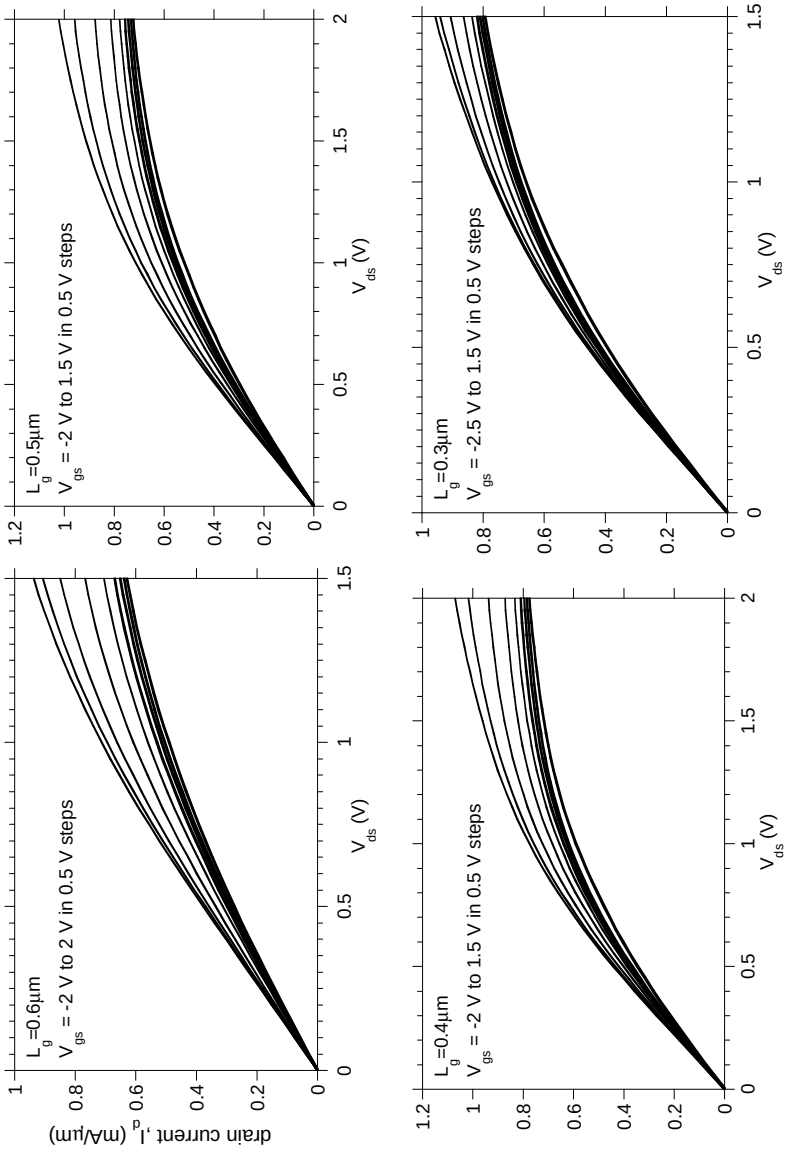


Figure 5.18: Output characteristics of InGaP sub-channel recessed source/drain depletion MOSFETs.

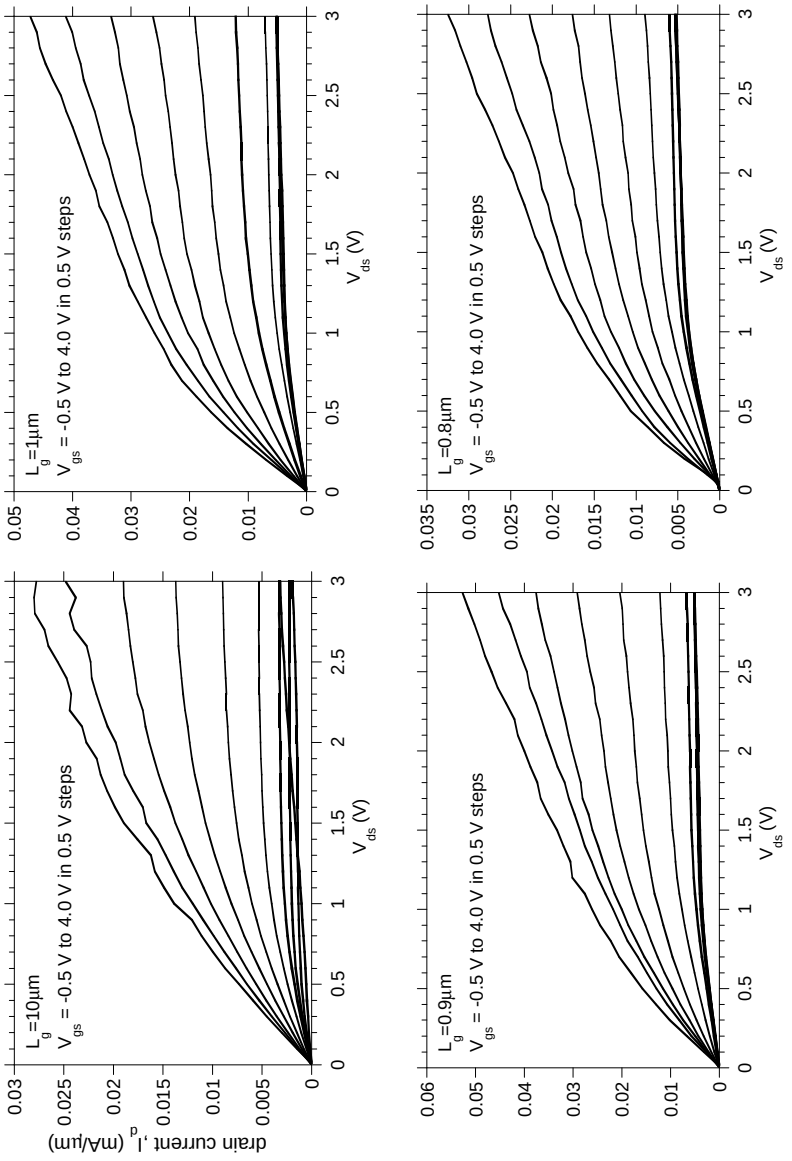


Figure 5.19: Output characteristics of InGaP sub-channel recessed source/drain enhancement mode MOSFETs.

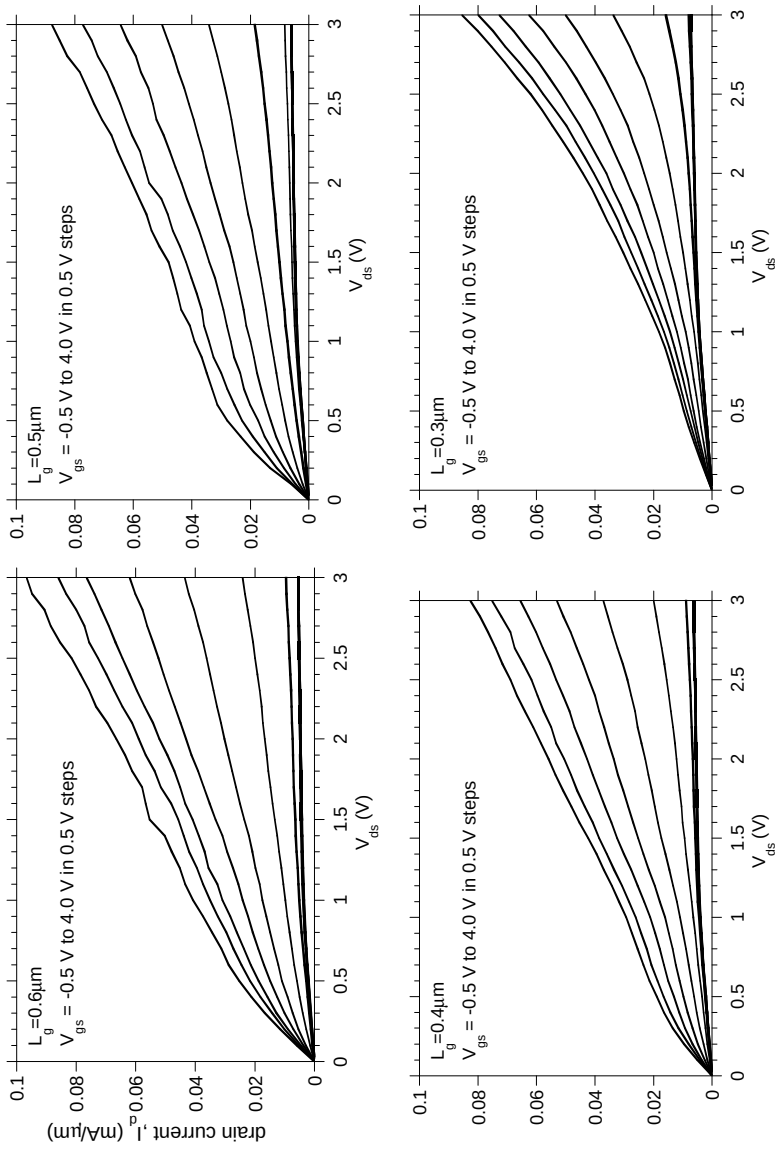


Figure 5.20: Output characteristics of InGaP sub-channel recessed source/drain enhancement mode MOSFETs.

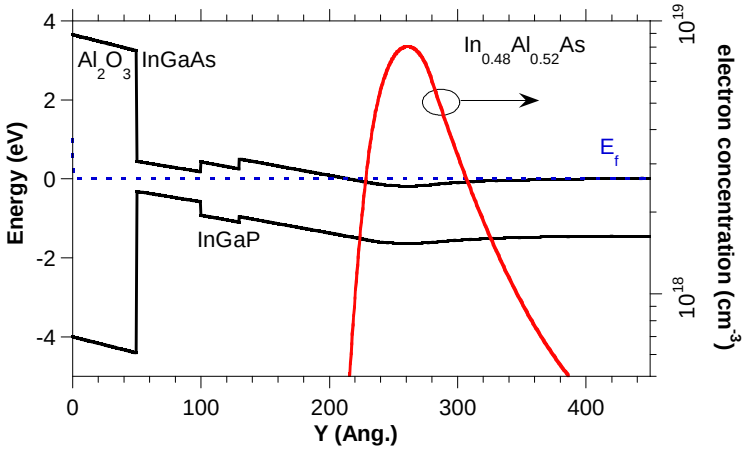


Figure 5.21: InGaP sub-channel recessed source/drain depletion MOSFET band diagram at $V_{gs} = -1V$. Parasitic conduction layer exists in the pulse doping layer.

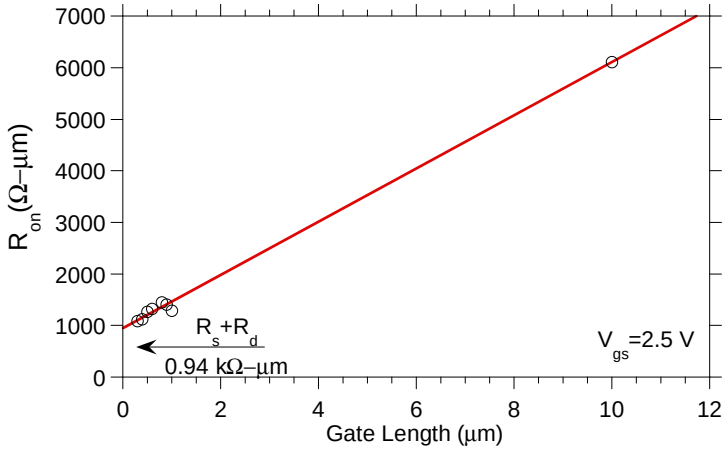


Figure 5.22: MOSFET on resistance Vs. gate length for the InGaP sub-channel recessed source/drain depletion mode MOSFETs.

$In_{0.88}Ga_{0.12}P$ sub-channel devices with pulse doping. This is partly due to the thinner setback and thinner high-k dielectric. The source access resistance for these devices is estimated to be 230 $\Omega - \mu m$ (Fig. (5.25)). The intrinsic peak g_m is calculated to be 0.5 $mS/\mu m$ from Eq. (2.12).

Table 5.5: Layer structure of the $In_{0.88}Ga_{0.12}P$ recessed source/drain depletion MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping n (cm^{-3})
1	Oxide	Al_2O_3	2.5	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Sub-channel	$In_{0.88}Ga_{0.12}P$	2.5	-
4	Setback	$In_{0.48}Al_{0.52}As$	5	-
5	Pulsedoping	$In_{0.48}Al_{0.52}As$	5	2×10^{19}
6	Buffer	$In_{0.48}Al_{0.52}As$	200	-
7	Substrate	InP	-	SI

The drive currents and source resistance of the MEE regrown recessed source/drain MOSFETs is significantly better than the 1st generation of devices shown in Sec. (5.2). The improvement is because of absence of gaps near the gate and consequently less surface depletion of electrons. It is also partly due to the pulse doping in the back barrier which compensates any surface or interface states providing sufficient conduction path from the source contact to the channel under the gate. Although the depletion mode MOSFET shows low source access resistance of 230 $\Omega - \mu m$, it does not conclusively prove the ability of the MEE regrowth to fill in under the sidewall (Fig. (5.26)). An enhancement mode device with low source

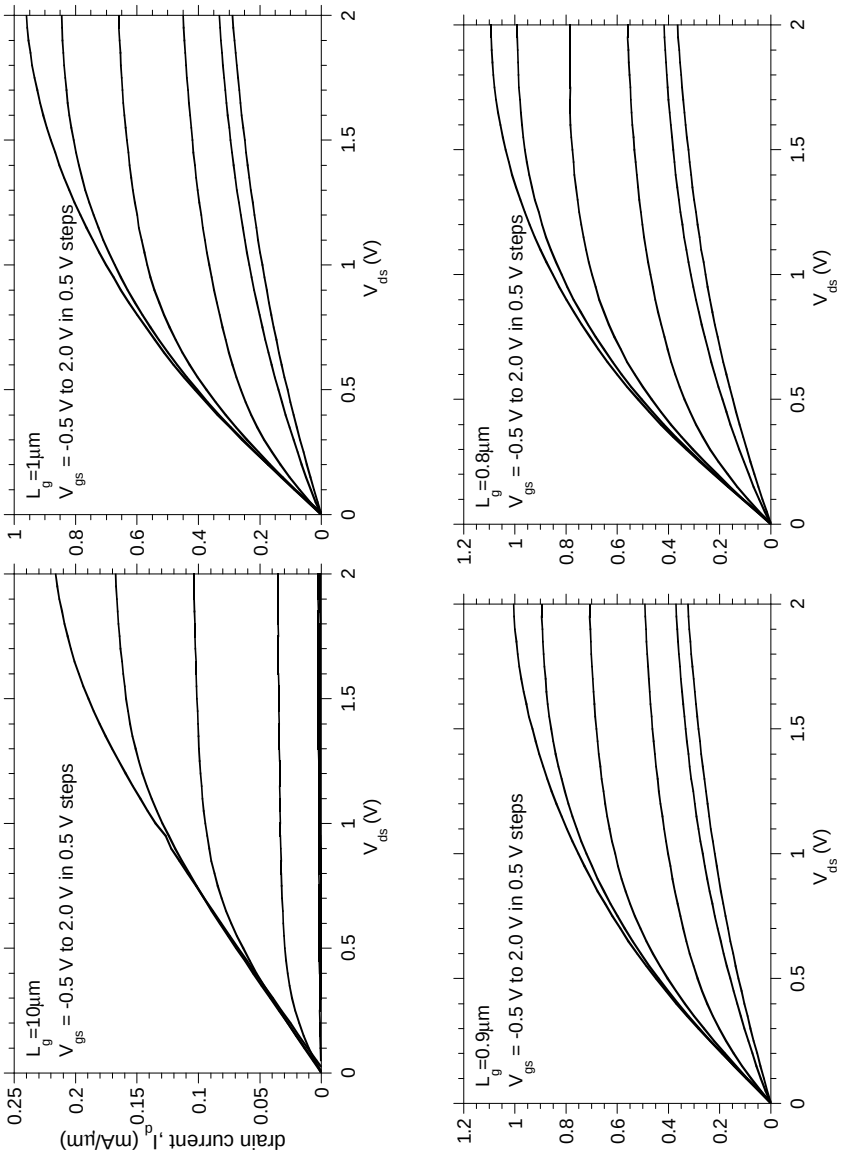


Figure 5.23: Output characteristics of InGaP sub-channel recessed source/drain depletion MOSFETs with 1.5 nm EOT.

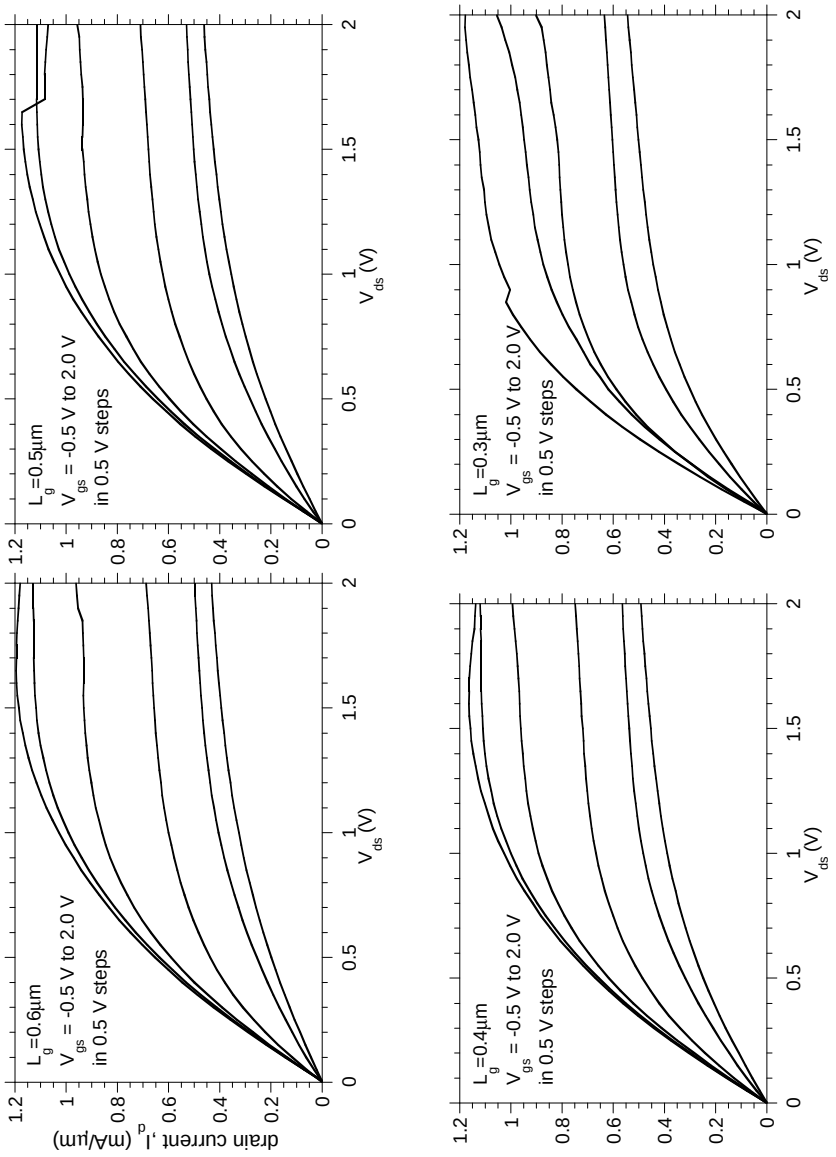


Figure 5.24: Output characteristics of InGaP sub-channel recessed source/drain depletion MOSFETs with 1.5 nm EOT.

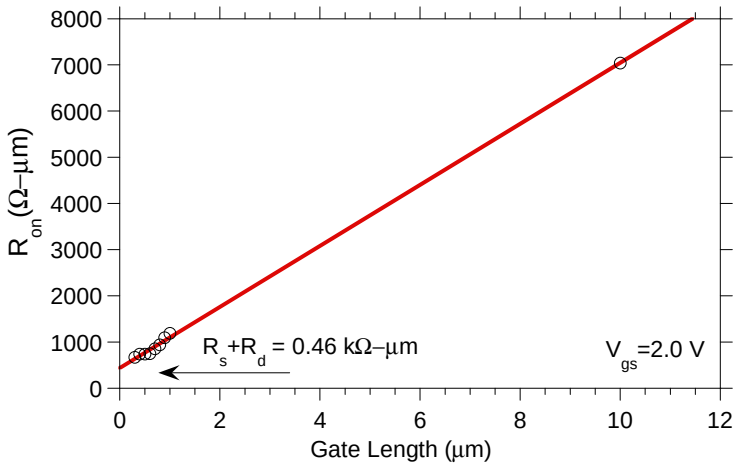


Figure 5.25: MOSFET on resistance Vs. gate length for the InGaP sub-channel recessed source/drain depletion mode MOSFETs with 2.5 nm Al_2O_3.

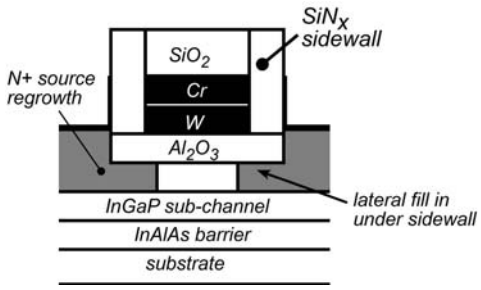


Figure 5.26: n^{++} regrowth filling under the sidewall is necessary for low source access resistance.

access resistance needs to be demonstrated to completely qualify the scalability of the recessed source/drain regrowth technology.

5.4.2 Raised source/drain FETs

Table 5.6: Layer structure of the raised source/drain enhancement mode MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping n (cm^{-3})
1	Oxide	Al_2O_3	4.7	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Buffer	$In_{0.48}Al_{0.52}As$	100	-
4	Substrate	InP	-	SI

Table 5.7: Layer structure of the raised source/drain depletion mode MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping n (cm^{-3})
1	Oxide	Al_2O_3	4.7	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Pulse-doping	$In_{0.48}Al_{0.52}As$	5	2×10^{19}
4	Buffer	$In_{0.48}Al_{0.52}As$	200	-
5	Substrate	InP	-	SI

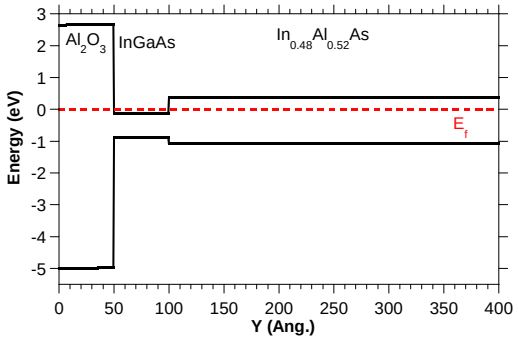
In the raised source/drain device structure the n^{++} region is regrown on the channel as shown in Fig. (5.14). The key to the raised source/drain structure is the sidewall thickness. They need to be narrow in order to avoid electron depletion in the channel under the sidewalls. One advantage of this structure over the recessed source/drain structure is that thicker sidewalls can be deposited

on the drain side which can improve DIBL and at the same time the source side sidewall can be thin and be optimized for low source access resistance.

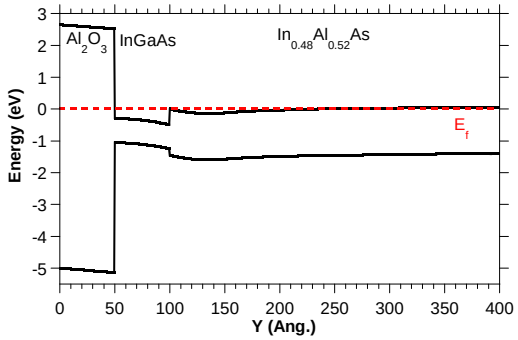
Two sets of raised source/drain MOSFETs were fabricated *i.e* enhancement mode and depletion mode. The depletion mode FETs had $1 \times 10^{13} cm^{-2}$ Si pulse doping under the $In_{0.53}Ga_{0.47}As$ channel with no setback. Unlike the recessed source/drain MOSFETs in the previous section, the setback was removed to ensure the devices turn off. The layer structures of these devices is shown in and Tables (5.6, 5.7) and Fig. (5.27).

Fig. (5.28) shows an oblique view and cross-section SEM of the finished device. The sidewalls can be seen to be 20-25 nm thick. The regrowth is quasi-selective, i.e. material is deposited on the gate top surface, but there is little growth on the gate sidewalls.

The output characteristics of the enhancement mode MOSFETs is shown in Fig. (5.29,5.30) for different gate lengths. The devices show good saturation and the drive current I_d scales with gate length from $10\mu m$ to sub-micron gate lengths. The threshold voltage is $\sim$ 0.75 V. The peak I_d and peak g_m of the devices are 0.11 $mA/\mu m$ and 0.02 $mS/\mu m$ for the 0.7 μm L_g device. The drive currents and transconductances are pretty low with device on resistance on the order of $\sim$ 10 $k\Omega - \mu m$ suggesting large parasitic resistance. From the zero bias on resistance vs. gate length the source access resistance is predicted to be 3.3 $k\Omega - \mu m$. TLMs were

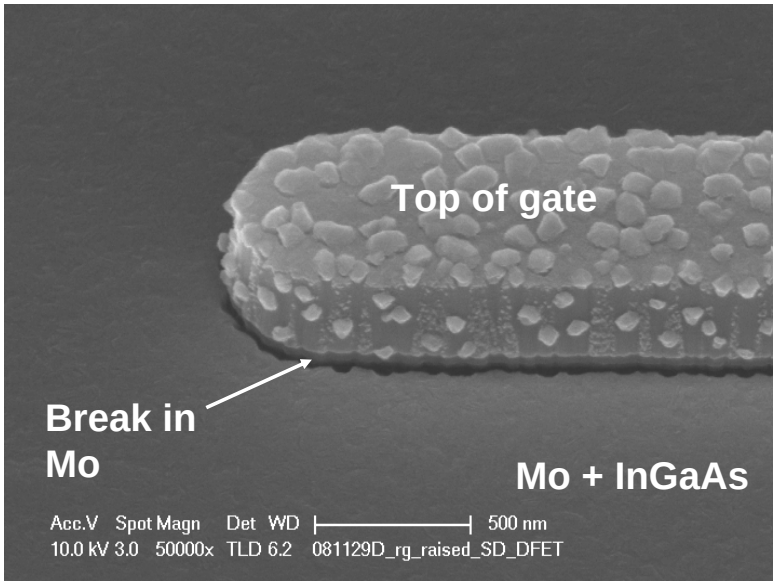


(a) Band diagram of the raised source/drain enhancement mode MOSFET (Table (5.6)) at V_g=0 V.

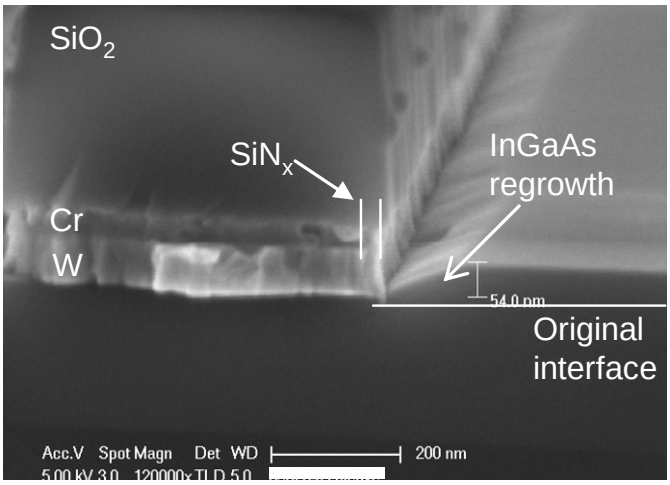


(b) Band diagram of the raised source/drain depletion mode MOSFET (Table (5.7)) at V_g=0 V.

Figure 5.27: Raised source/drain MOSFETs.



(a) Angled SEM of a MOSFET after regrowth and $in-situ$ Mo deposition.



(b) Cross-section SEM of a MOSFET after regrowth but before MO deposition.

Figure 5.28: Raised source/drain MOSFETs.

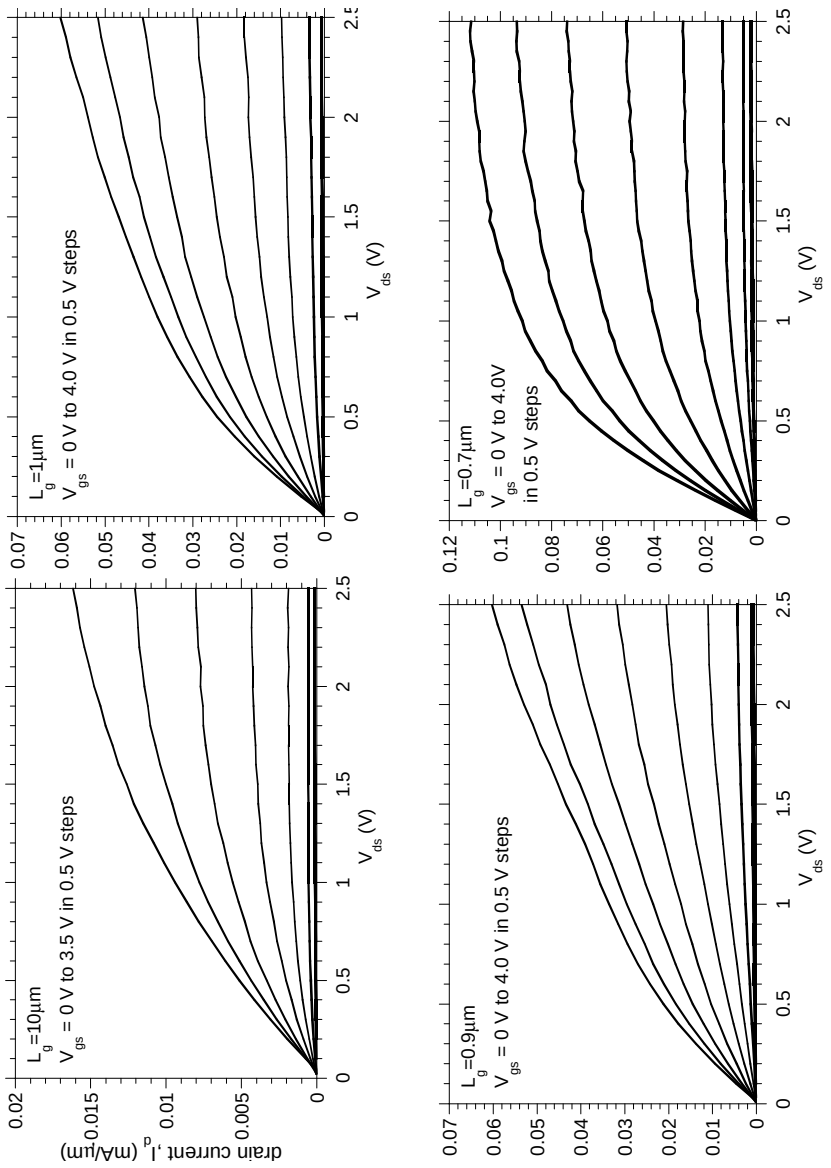


Figure 5.29: Output characteristics of the raised source/drain **enhancement mode MOSFETs**.

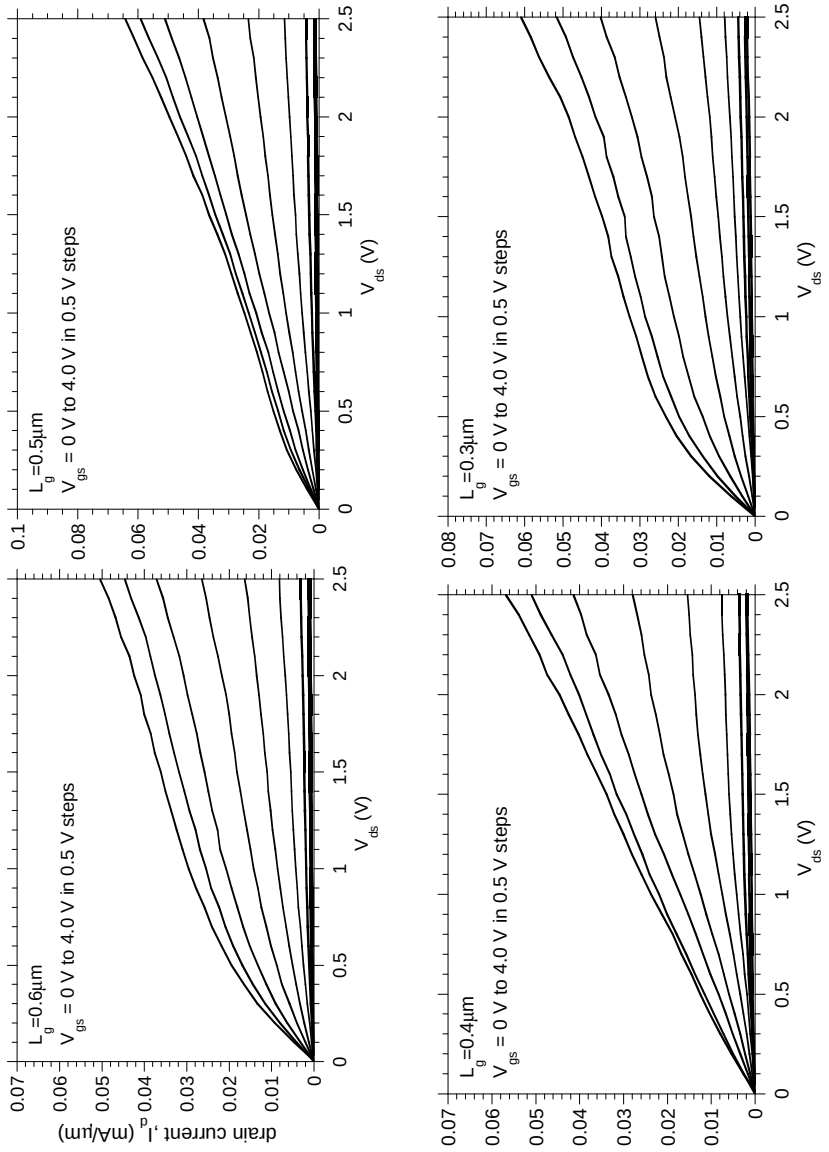


Figure 5.30: Output characteristics of the raised source/drain **enhancement mode MOSFETs**.

fabricated to evaluate the regrowth material quality far away from the devices. The sheet and contact resistance are 30 $\Omega/\Box$, and 13.0 $\Omega - \mu m^2$.

The depletion mode raised source/drain output characteristics are shown in Figs. (5.31,5.32). The threshold voltage of the devices is $-1\ to - 0.75$ V. The drive current I_d scales with gate length from $10\mu m$ to sub-micron gate lengths. The peak I_d and peak g_m are 0.95 $mA/\mu m$ and 0.37 $mS/\mu m$ at L_g =0.8 μm. At 2 V V_{ds} the 0.3 μm L_g device shows signs of impact ionization. Both the drive currents and transconductances are an order of magnitude larger than the enhancement mode devices.

From measurements of zero-bias on-resistance (Fig. 5.33), a 500 $\Omega - \mu m$ source access resistance is determined. TLM measurements (Fig. (5.34)) on the regrown material located far from MOSFET showed 29 Ω/square sheet resistance, 5.5 $\Omega - \mu m^2$ vertical contact resistance and 12 Ω μm Mo/InGaAs (lateral) contact resistance. The large discrepancy between the source resistance observed in the MOSFET and lateral access resistance observed in TLM patterns may indicate that the regrown InGaAs close to the gate has higher resistivity than in the far field. MBE is a line-of-sight deposition technique, hence growth adjacent to the gate may be disturbed by shadowing. Fig. (5.35) shows a cross-section schematic of the MOSFET after regrowth. There is reduction in InGaAs thickness next to gate. Insufficient thickness next to gate will deplete electrons in the channel

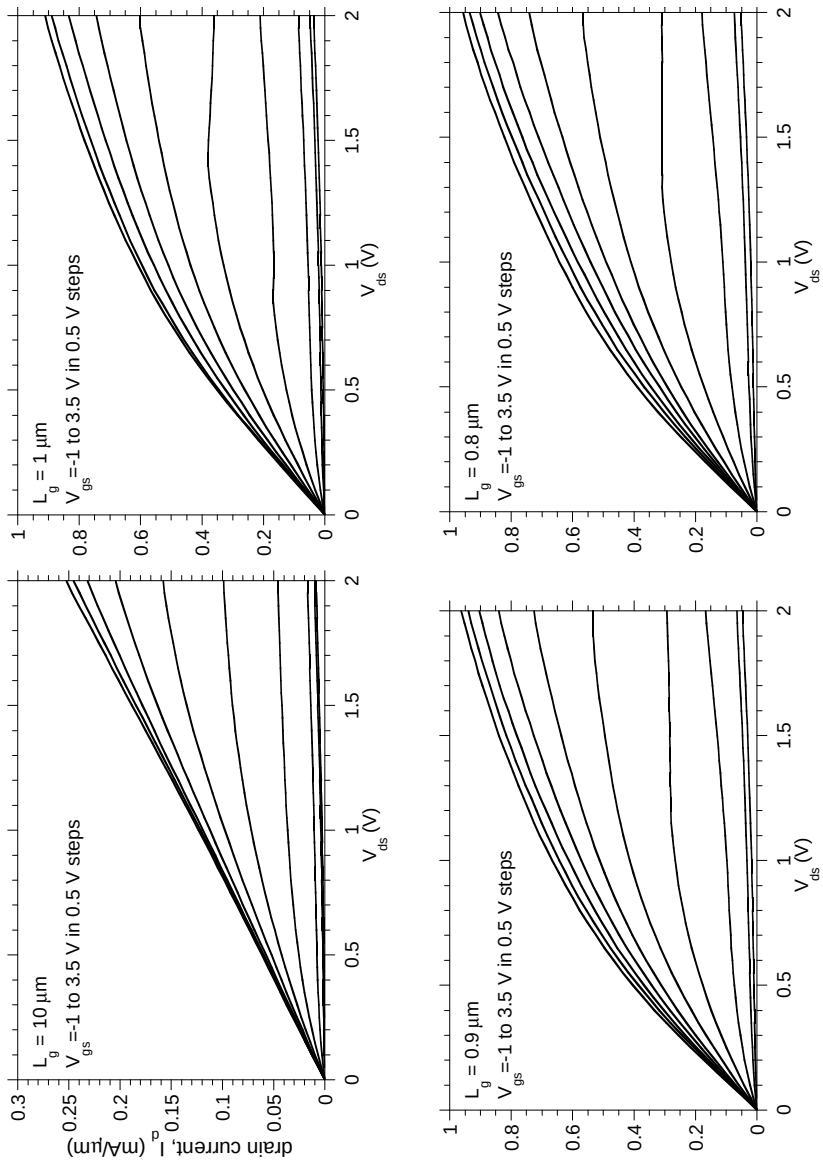


Figure 5.31: Output characteristics of the raised source/drain depletion mode MOSFETs.

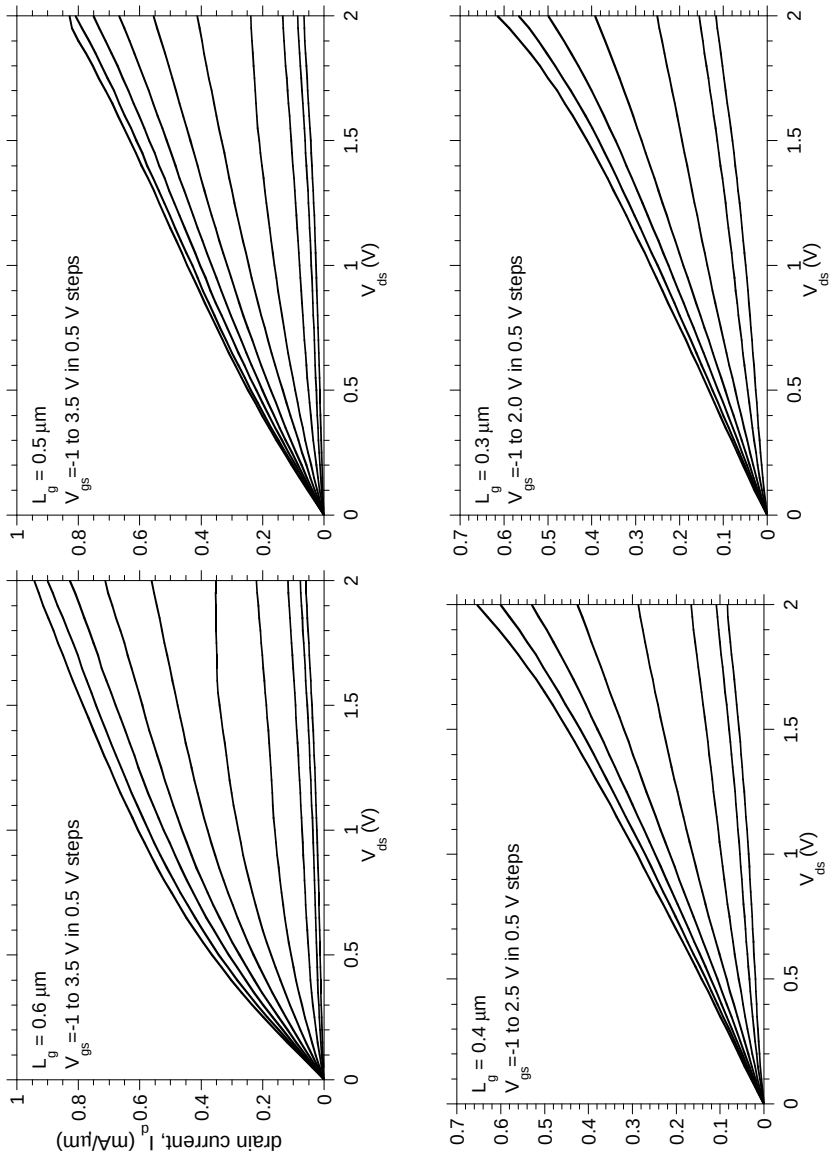


Figure 5.32: Output characteristics of the raised source/drain depletion mode MOSFETs.

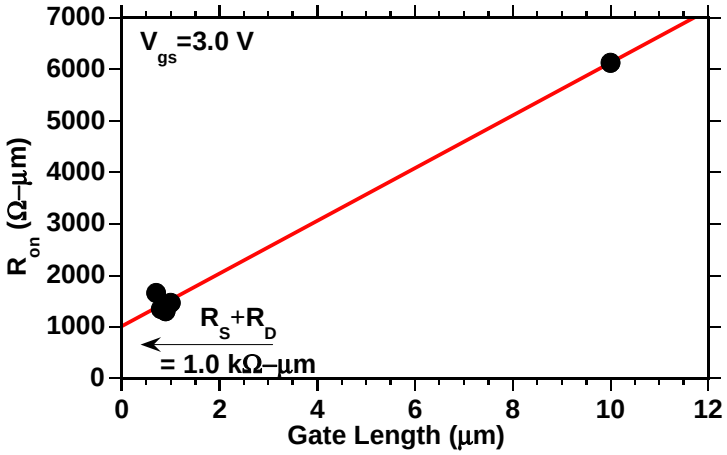


Figure 5.33: (MOSFET on resistance Vs. gate length for the raised source/drain depletion FETs.

increasing the source resistance. Other possible causes of high source resistance include lack of Si doping next to gate, lattice mismatched growth next to gate causing dislocations which deplete electrons, or high defect density at the regrowth interface. Any defects induced at Al_2O_3/InGaAs interface during regrowth will also deplete electrons in the channel under the sidewall.

Devices were also fabricated with the gate oriented at 45° to [100] direction to see if there is any dependence of regrowth on crystal directions. Fig. (5.36) shows the output characteristics of the device gates oriented 45° to [100]. There is no significant difference in the drive current and on resistance, hence possibly no significant dependence of regrowth on the crystal direction. Fig. (5.37) plots the on resistance of the MOSFETs with gate length, and it can be seen that the on

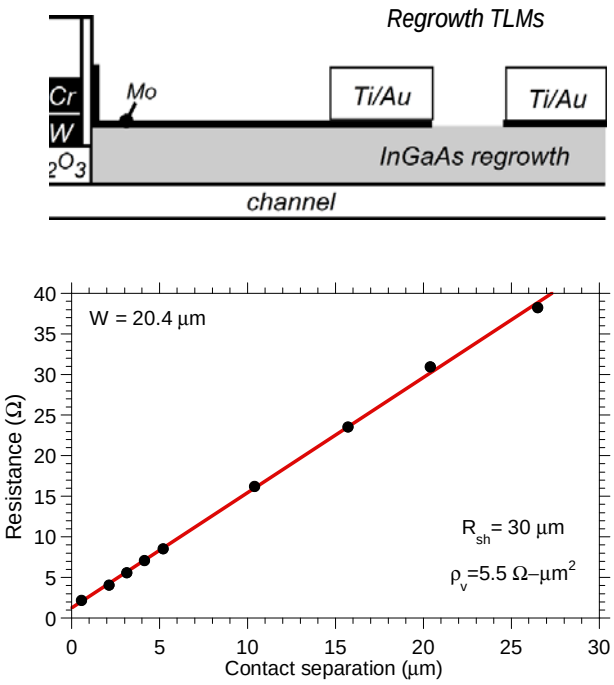


Figure 5.34: (Top) TLM schematic to evaluate regrowth material quality and (bottom) measured TLM data. Metal interconnect resistance [24] correction has been applied to the plotted resistance.

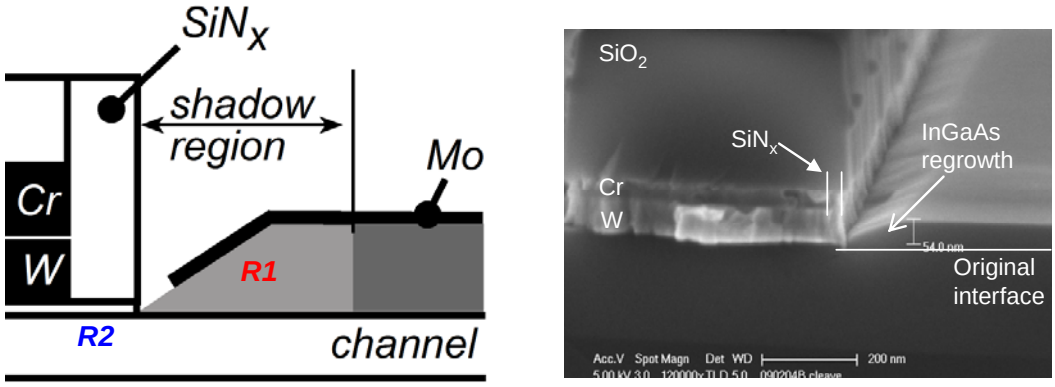


Figure 5.35: (Left) Cross-section schematic of regrowth next to a gate and (right) cross-section SEM of regrowth next a gate. Electron depletion in the regrowth next to gate (R1) and electron depletion under the sidewall (R2) contribute to the source resistance.

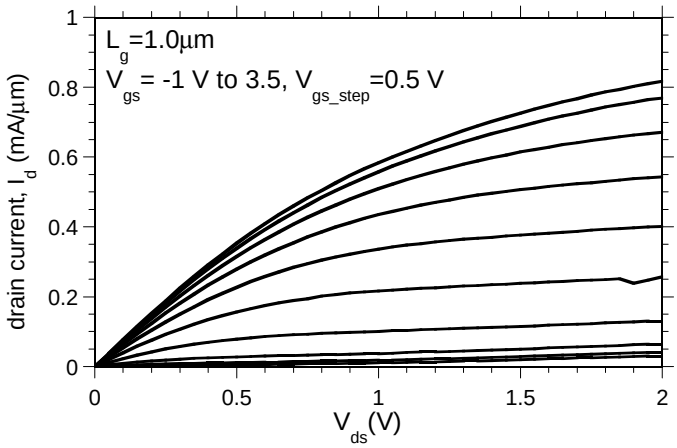


Figure 5.36: Output characteristics of $1\mu m$ L_g MOSFET with the gate aligned at 45 °to [100] direction.

resistance increases when gate length is below 0.7 μm L_g. This trend was observed across the whole wafer and also on two other co-processed wafers. This suggests a dependence of regrowth on the gate length.

The gate leakage in these devices were small. As seen in Fig. (5.38), the gate leakage was not scaling with gate area. The leakage is probably through the SiN_x sidewalls. Fig. (5.39) shows the isolation current between devices for different mesa heights. The mesa etch depth needs to reach the SI InP substrate to get good device to device isolation.

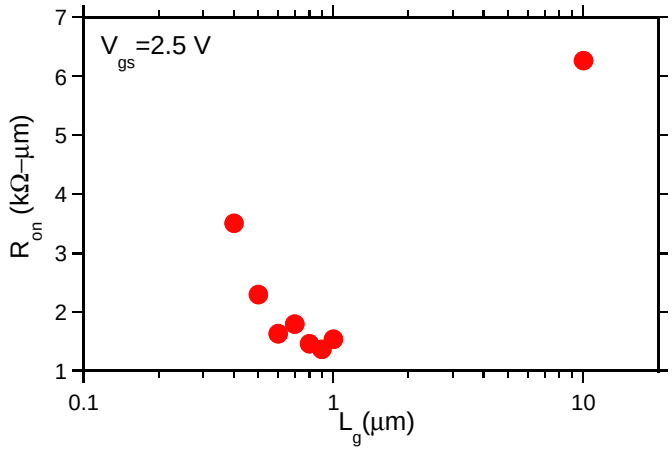


Figure 5.37: On resistance of MOSFET Vs. gate length for V_{gs}=2.5 V. The R_{on} increases for gate lengths $< 0.6\mu m$, suggesting source resistance and hence regrowth dependence on gate length.

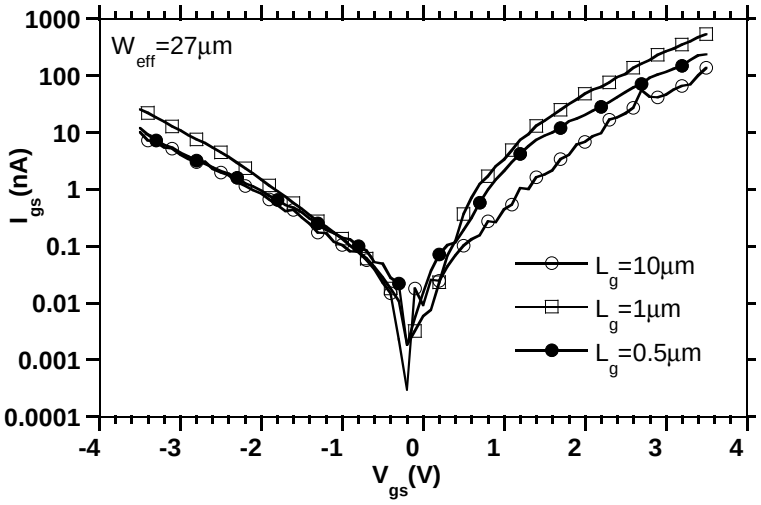


Figure 5.38: MOSFET gate leakage for different gate lengths.

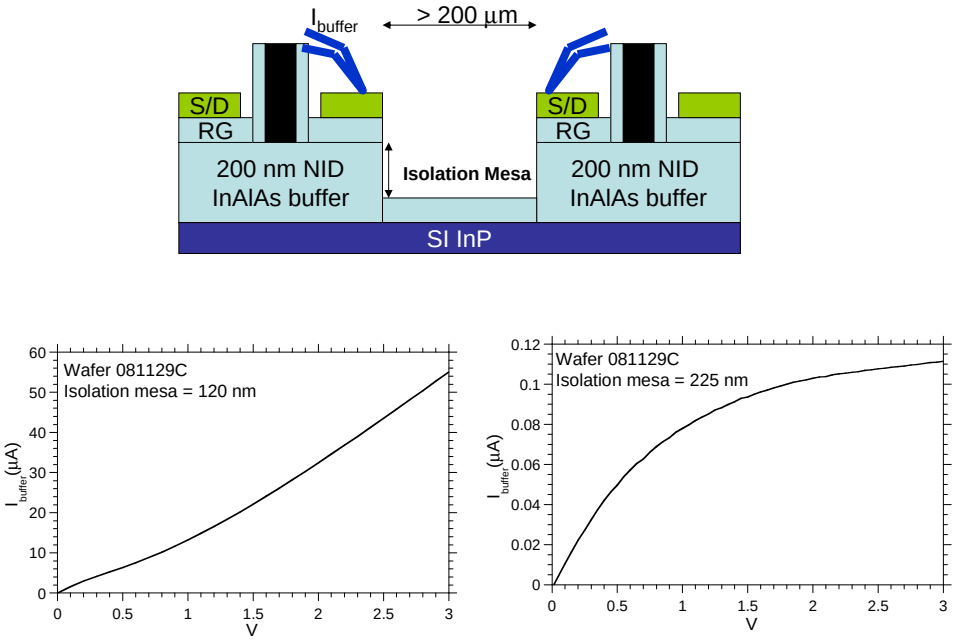


Figure 5.39: Device to device isolation current dependence on mesa height.

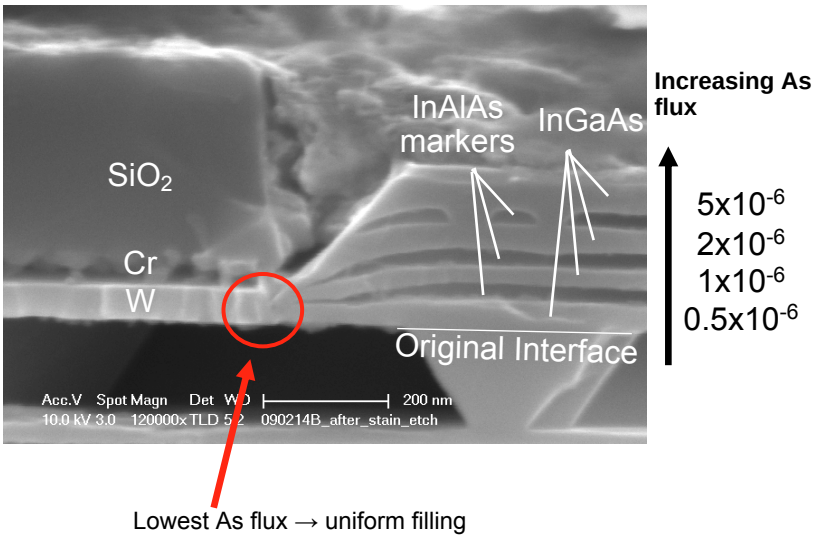


Figure 5.40: SEM of regrowth series with different growth condition [49].

5.5 Low arsenic (As) MEE $In_{0.53}Ga_{0.47}As$ and InAs regrowth

It was pointed out in the last section that there may be electron depletion in the regrowth next to gate either due to insufficient thickness or due to defects. A regrowth study was done to optimize the conditions for uniform filling of regrowth next to gate [49]. In this study 4 layers of 50 nm $In_{0.53}Ga_{0.47}As$ was grown with $In_{0.48}Al_{0.52}As$ marker layers. The wafer was etched for 10 sec in concentrated HCl to selectively etch $In_{0.48}Al_{0.52}As$ layers. Fig. (5.40) shows the cross-section SEM of the regrowth near the gate. The four $In_{0.53}Ga_{0.47}As$ regrowth layers can be seen

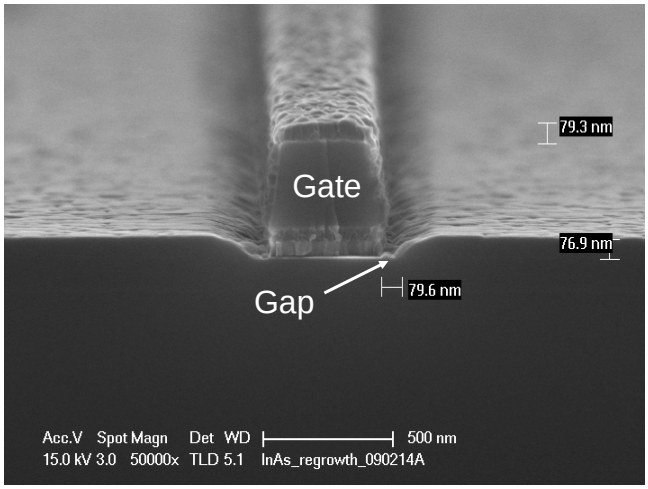


Figure 5.41: SEM of InAs MBE (non-MEE) regrowth, showing gap next to gate.

clearly. The SEM suggests lower As flux gives uniform regrowth with minimum reduction in regrowth thickness next to gate.

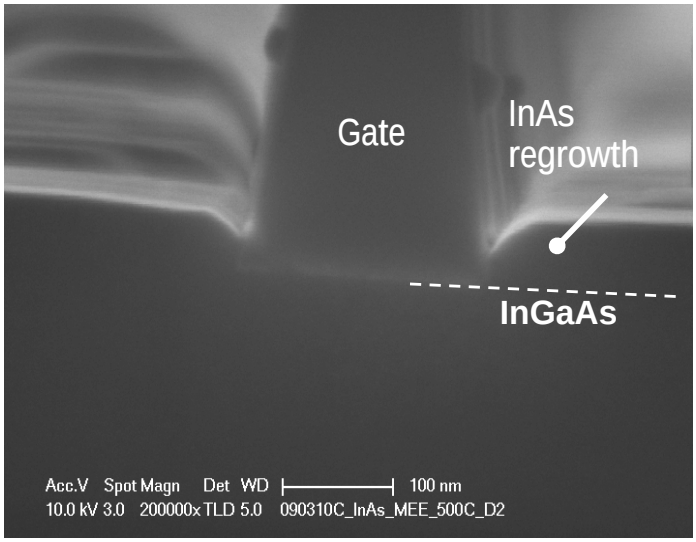
InAs is less prone to electron depletion compared to $In_{0.53}Ga_{0.47}As$ because of the Fermi level pinning inside conduction band edge [53]. An InAs source/drain regrowth on $In_{0.53}Ga_{0.47}As$ will be less prone to electron depletion compared to $In_{0.53}Ga_{0.47}As$ regrowth. The InAs/$In_{0.53}Ga_{0.47}As$ interface resistance is measured to be less than 2.0 $\Omega - \mu m^2$ [54] and will not significantly degrade the source resistance. Fig. (5.41) shows an oblique view SEM of InAs MBE (non-MEE) regrowth done at 410 °C. An MEE regrowth was not done on this sample with the assumption that In has a higher surface mobility and hence normal MBE would not lead to gaps. But as seen in the SEM there is a gap in the regrowth

next to gate similar to the initial $In_{0.53}Ga_{0.47}As$ MBE (non-MEE) regrowths (Fig. 5.7). In the second series of InAs regrowth tests an MEE regrowth was done. These InAs regrowths were carried out by Ashish K. Baraskar. Fig. (5.42) show cross-section SEM of low As flux ($\sim 5 - 6 \times 10^{-7}$ $torr$) InAs MEE regrowth done at two different temperatures. The cross-section SEMs show that low As flux InAs MEE regrowth shows uniform filling in with no reduction in thickness next to gates. Also, there is minimal growth on the sidewalls of the gate compared in $In_{0.53}Ga_{0.47}As$ regrowth. At 540 °C the regrowth surface is rough compared to the regrowth at 500 °C.

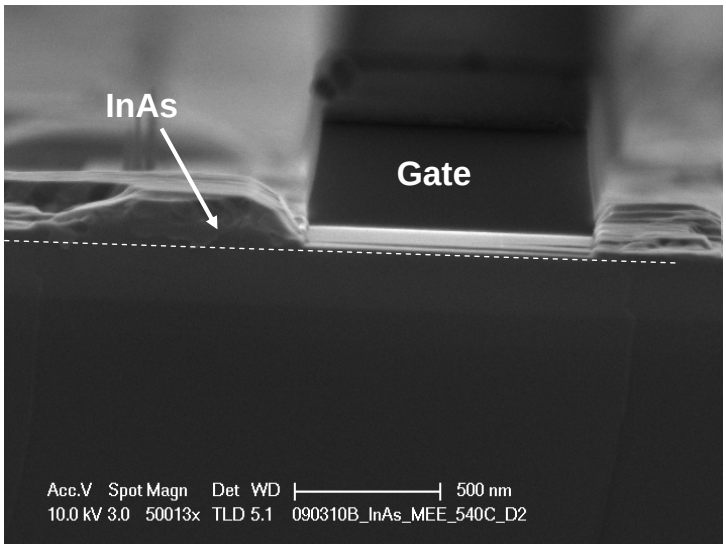
The arsenic flux is found to be a critical parameter for the regrowth profile next to gate. A low ($\sim 5 - 6 \times 10^{-7}$ $torr$) flux is needed to get uniform filling. InAs regrowth on $In_{0.53}Ga_{0.47}As$ gave uniform filling.

5.6 Low As flux InAs and InGaAs MEE regrowth source/drain MOSFETs

The final series of MOSFETs fabricated as a part of this thesis work were devices with low arsenic flux regrowth. The pulse doping in the previous series of MOSFETs was high (1×10^{13} cm^{-2}) and as a result the devices could not be completely turned off. The pulse doping was thus dropped to 6×10^{12} cm^{-2} to



(a) Cross-section SEM of MEE InAs regrowth at 500 °C. No gaps and no reduction in thickness are observed next to gate.



(b) Cross-section SEM of MEE InAs regrowth at 540 °C. No gaps and no reduction in thickness are observed next to gate.

Figure 5.42: InAs MEE regrowth

Table 5.8: Layer structure of the low As flux raised source/drain MOSFET.

Layer	Comment	Composition	Thickness (nm)	Doping(cm^{-3})
1	Oxide	Al_2O_3	4.7	-
2	Channel	$In_{0.53}Ga_{0.47}As$	5	-
3	Pulse-doping	$In_{0.48}Al_{0.52}As$	3.3	$n = 2 \times 10^{19}$
4	Buffer	$In_{0.48}Al_{0.52}As$	12	NID
5	Buffer	$In_{0.48}Al_{0.52}As$	180	$p = 1 \times 10^{-17}$
5	Substrate	InP	-	p^+

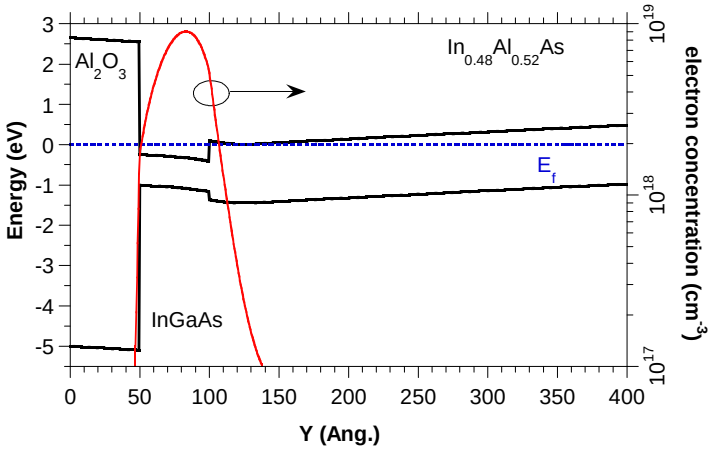


Figure 5.43: Band diagram of low As flux raised source/drain MOSFET at $V_g = 0V$.

make sure the device turns off. This would also enable a sub-threshold plot where the device is all the way turned off and hence give information about the D_{it} at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. The layer structure of the MOSFET is shown in Table (5.8) and Fig. (5.43). The buffer was lightly p doped with Be to provide barrier to electron flow into the buffer. The Al_2O_3 thickness was 4.7 nm ($\sim$ 2.5 nm

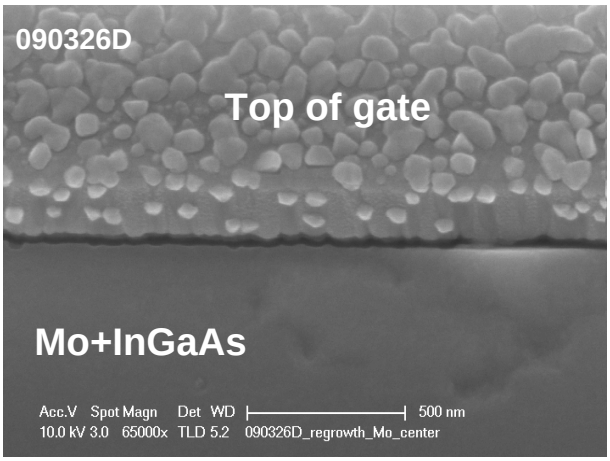


Figure 5.44: Angled SEM of the low As flux $In_{0.53}Ga_{0.47}As$ source/drain MOSFET (090326D)

EOT). The 2" wafer was cleaved into four pieces and MOSFETs were fabricated with four different regrowth conditions.

Table 5.9: Regrowth variation on the MOSFETs.

Wafer	Regrowth	Thickness (nm)	As flux (torr)	Doping (cm^{-3})
090326A	InAs	50	2×10^{-6}	1.6×10^{20}
090326B	InAs	50	5×10^{-7}	1.6×10^{20}
090326C	InAs	50	5×10^{-7}	8×10^{19}
090326D	$In_{0.53}Ga_{0.47}As$	50	6.7×10^{-6}	4×10^{19}

The four different regrowth conditions are summarized in Table (5.9). The device results from these runs [55] are discussed in the following sections.

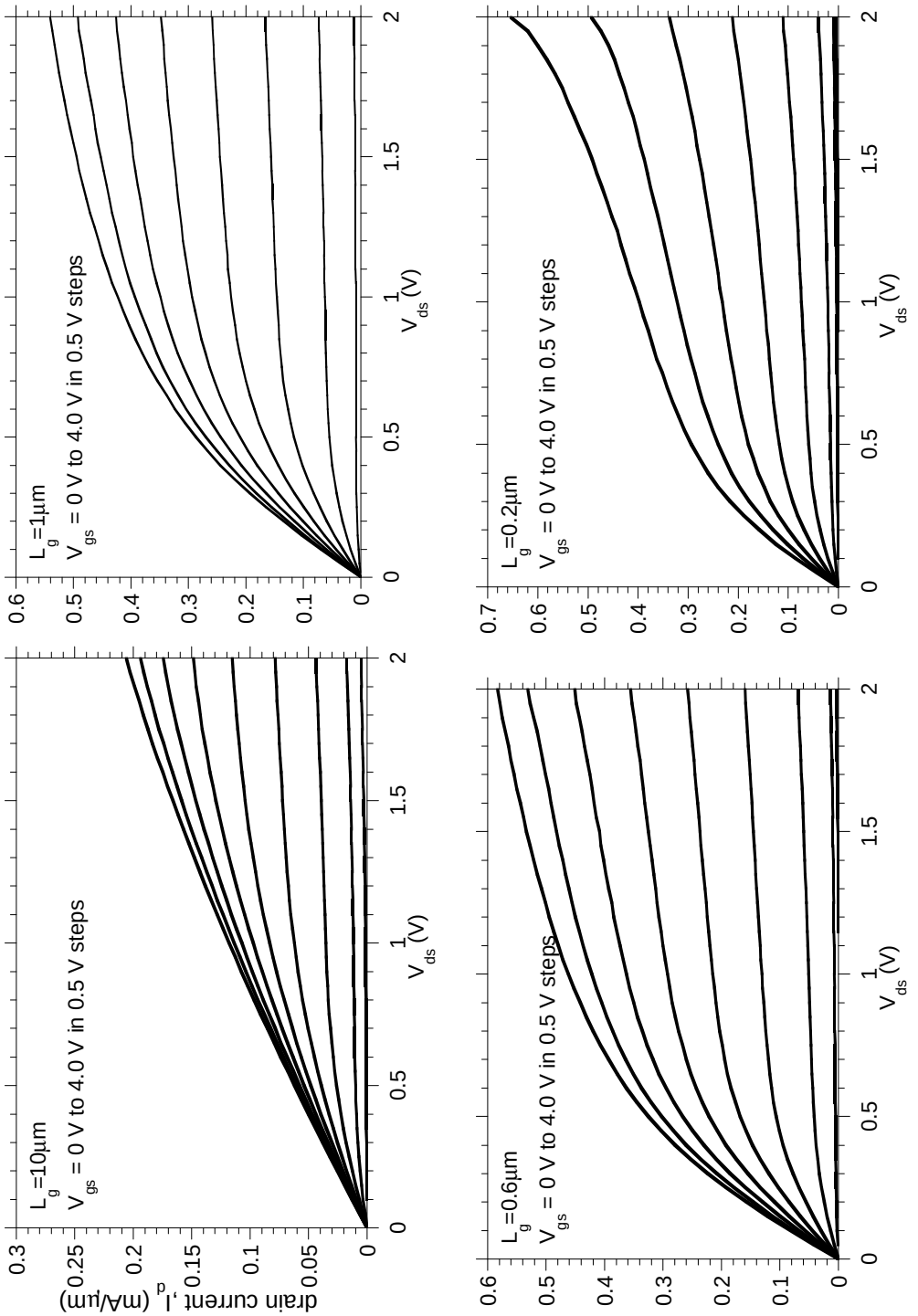


Figure 5.45: Output characteristics of the raised source/drain MOSFETs (090326D) with low As flux MEE $In_{0.53}Ga_{0.47}As$ regrowth.

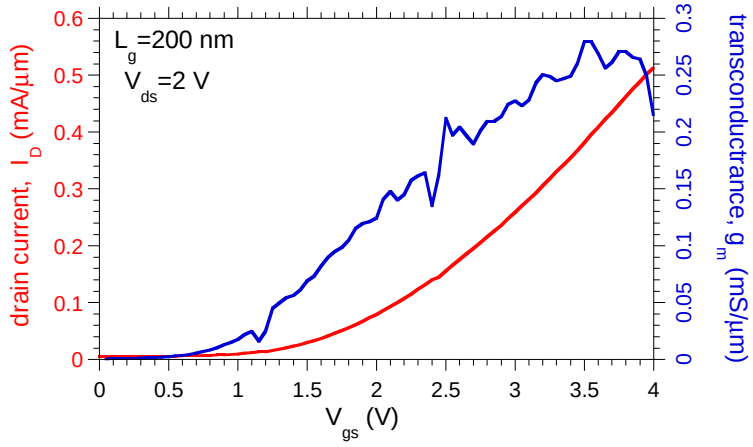


Figure 5.46: Input characteristics of 200 nm L_g 090326D MOSFET.

5.6.1 Low As flux InGaAs source/drain regrowth

50 nm of $In_{0.53}Ga_{0.47}As$ was grown at 540 °C at low arsenic flux of 6.7×10^{-7} *torr*. The SEMs (Fig. (5.44)) of the regrowth showed smooth surface and uniform filling in. The output characteristics of the devices for various gate lengths is shown in Fig. (5.45). Theses devices are enhancement mode with a $V_t \sim 0.75V$. There is $\sim$ 8% enhancement in the drive current for the 200 nm L_g device at $V_{gs} = 4.0$ V and $V_{ds} = 2.0$ V due to impact ionization. The input characteristics of the 200 nm L_g device is shown in Fig. (5.46). The peak drive current and transconductance of the device are 0.5 mA/μm and 0.3 mS/μm $V_{gs} = 4.0$ V and $V_{ds} = 2.0$ V. The on resistance of the devices scale with gate length (Fig. (5.47)), and do not show the increase in R_{on} for $L_g < 0.7\mu m$ devices as was observed in the "normal" As flux regrowth MOSFETs in Sec. (5.4.2). The sub-threshold

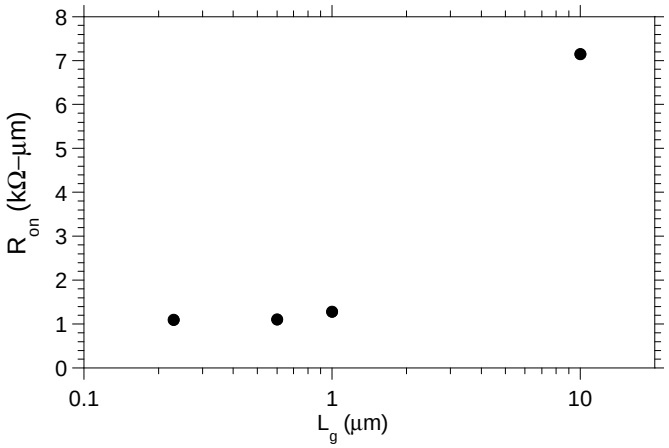


Figure 5.47: R_{on} Vs. L_g for 090326D MOSFET.

characteristics for two different gate lengths is shown in Fig. (5.48). The long channel MOSFET has a high sub-threshold swing of $\sim$ 300 mV/decade. The devices can be turned off completely; the I_{off} at $V_{ds} = 0.1$ V for the 200 nm L_g device is 3×10^{-6} $mA/\mu m$.

5.6.2 Normal As flux InAs source/drain regrowth

On wafer 090326A, 50 nm of InAs was regrowth at 500 °C at a "normal" arsenic flux of 2×10^{-6} *torr* with 1.6×10^{20} Si doping. In the oblique view SEM (Fig. (5.49)) there is an apparent slope in the regrowth, with a possible reduction in regrowth thickness next to gate. The output characteristics of the MOSFET is shown in Fig. (5.50). The $10\mu m$ device shows good saturation and has a threshold voltage of 0.6-0.75 V. Short $L_g \leq 1$ μm devices show good

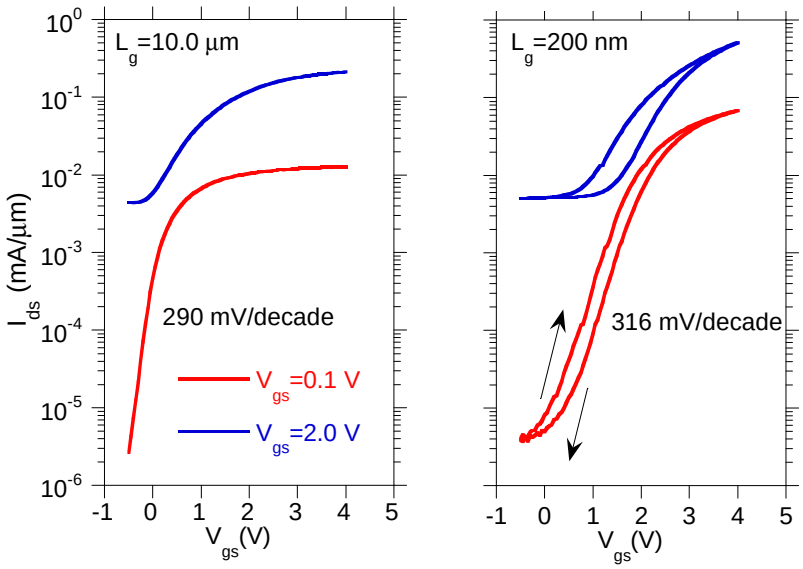


Figure 5.48: Subthreshold characteristics of 10 μm and 200 nm L_g 090326D MOSFETs.

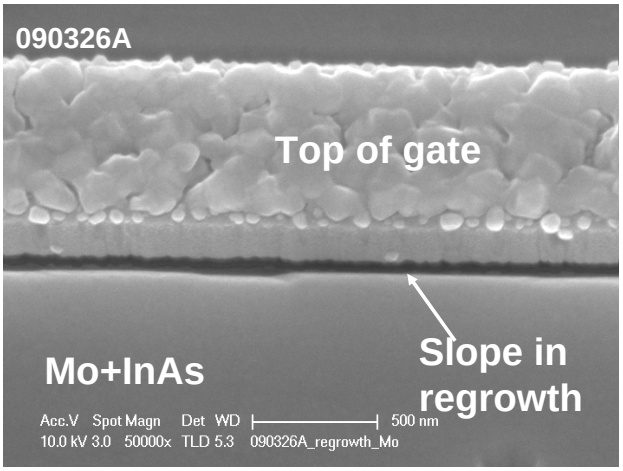


Figure 5.49: Angled SEM of normal As flux InAs source/drain MOSFET (090326A)

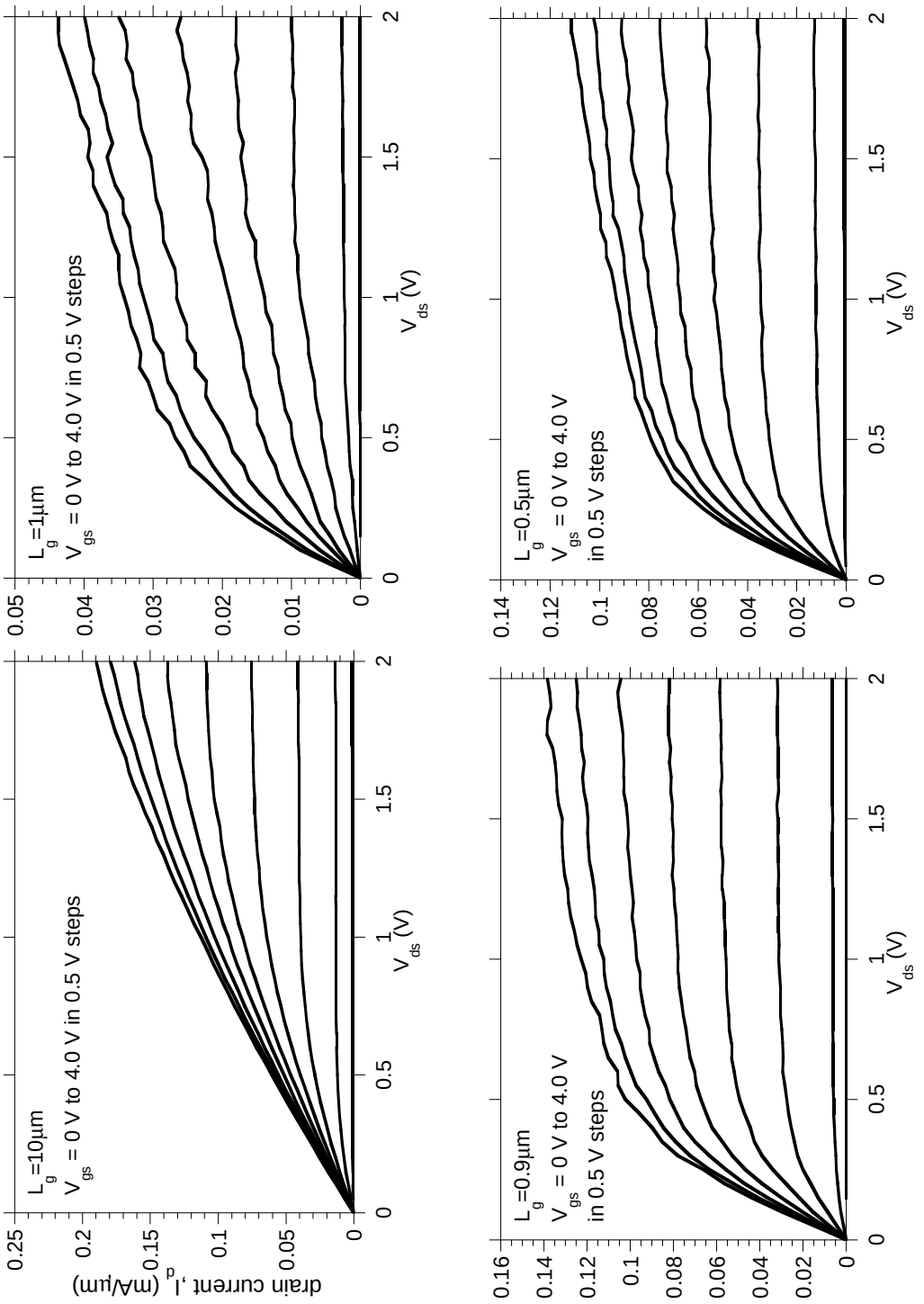


Figure 5.50: Output characteristics of the raised source/drain MOSFETs (090326A) with "normal" As flux MEE InAs regrowth.

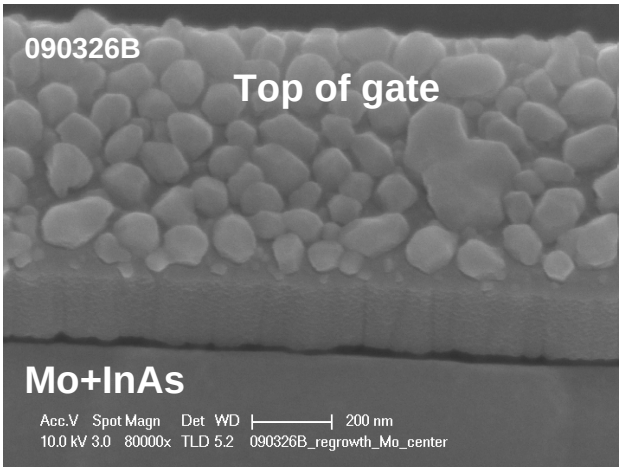


Figure 5.51: Angled SEM of low As flux InAs source/drain MOSFET (090326B)

saturation but the peak drive current is same as the 10 μm L_g device. This suggests a source resistance limited drive current. The slope seen is SEM could explain for the observed behavior. The $In_{0.53}Ga_{0.47}As$ channel can be depleted if there is insufficient regrowth thickness next to gate and thus increase the source resistance. Subsequently the current is same independent of gate length. Normal (2×10^{-6} $torr$) As flux InAs regrowth is not suitable for scaled devices.

5.6.3 Low As flux InAs source/drain regrowth

Two MOSFETs were fabricated with low arsenic flux MEE InAs regrowth. The results are presented below.

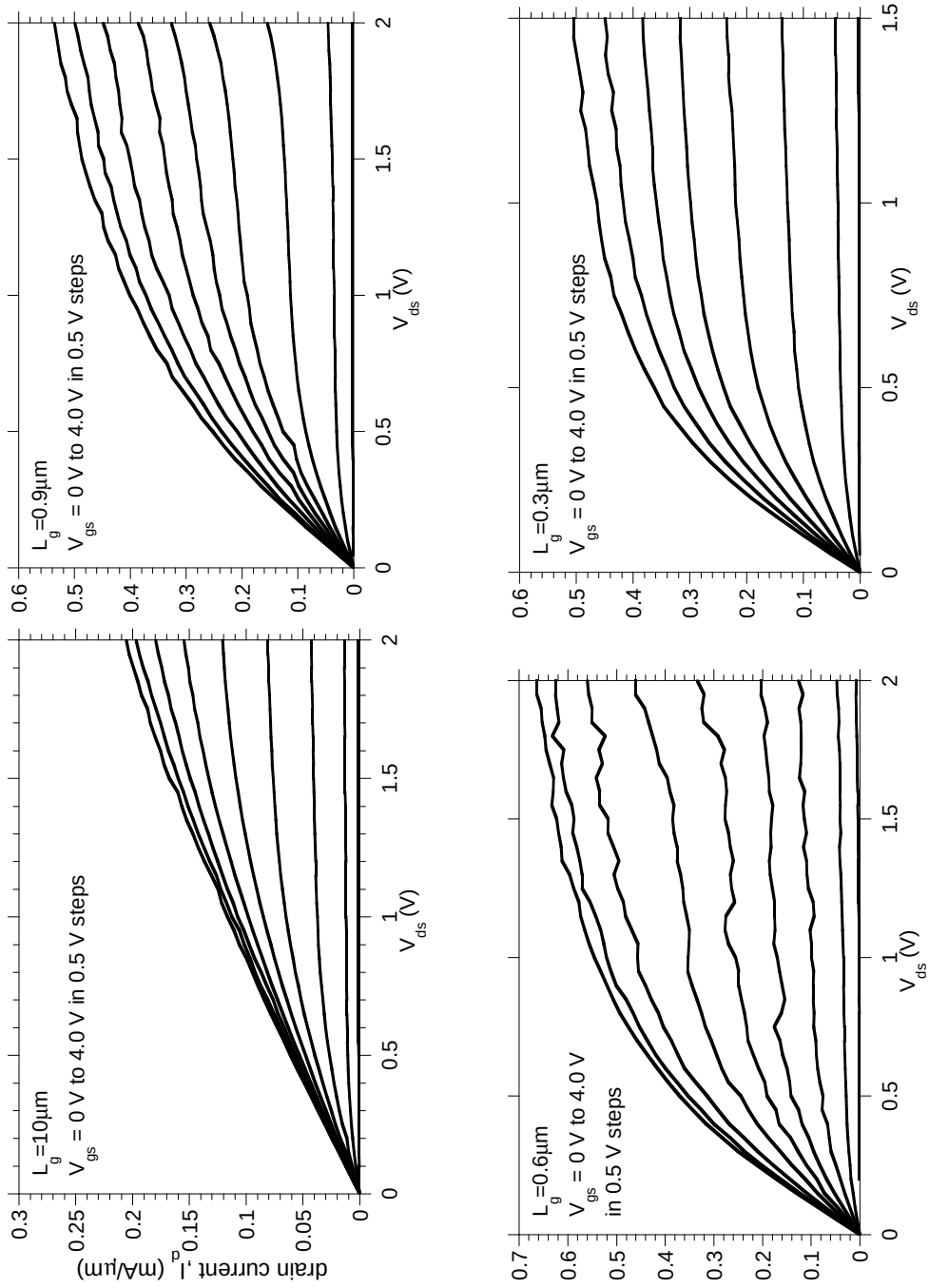


Figure 5.52: Output characteristics of the raised source/drain MOSFETs (090326B) with low As flux MEE InAs regrowth.

Wafer 090326B

On wafer 090326B, 50 nm of InAs was regrown at a lower 5×10^{-7} *torr* As flux. The InAs source/drain region was n type doped with Si at $1.6 \times 10^{20} cm^{-3}$. Before regrowth the wafer was H cleaned and also thermally desorbed. A 30 minute post regrowth H anneal was done on the wafer to improve the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. During regrowth RHEED was streaky indicating smooth regrowth. Fig. (5.51) shows an SEM of the regrowth, there is no slope observed as was the case of the MOSFETs with normal As flux regrowth in the previous section (090326A).

The output characteristics of the MOSFETs for different gate lengths is shown in Fig. (5.52). The devices have good saturation for gate lengths $10\mu m$ to 0.2 μm. The threshold voltage is approximately $0.6V - 0.75$ V. The input and output characteristics of the 0.2 L_g device is shown in Fig. (5.53). The device shows microwave oscillations because of poor shielding of the measurement setup. The peak drive current and transconductance for this device are 0.68 mA/μm and 0.35 mS/μm at $V_{gs} = 4V$ and $V_{ds} = 1.0V$ with an on resistance of 720 $\Omega - \mu m$. Both the on resistance and drive current scale with the gate length. The sub-threshold characteristics for two different gate lengths is shown in Fig. (5.54). The long channel MOSFET has a high sub-threshold swing of $\sim$ 300 mV/decade.

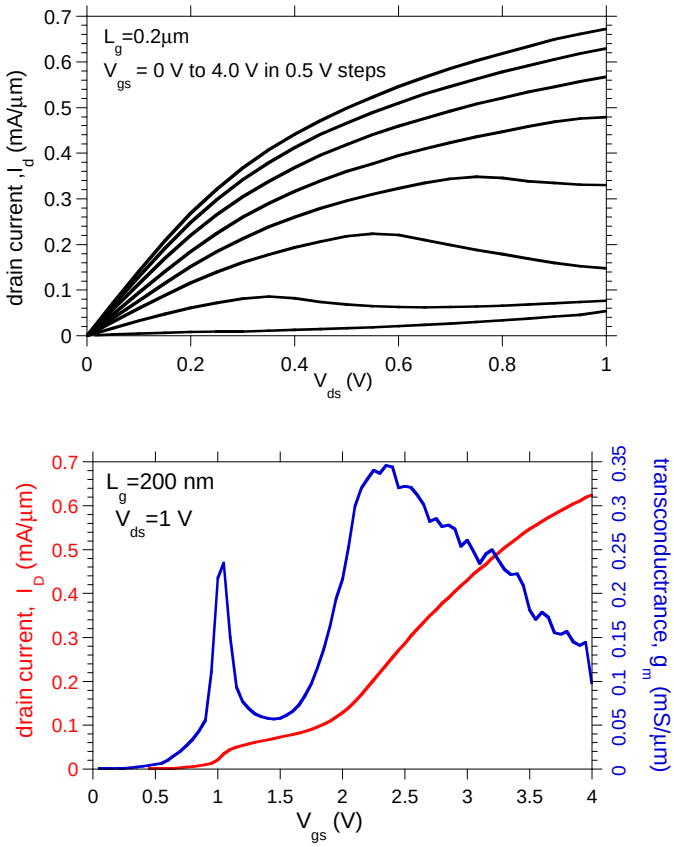


Figure 5.53: Output (top) and input (bottom) characteristics of a 200 nm L_g 090326B MOSFET.

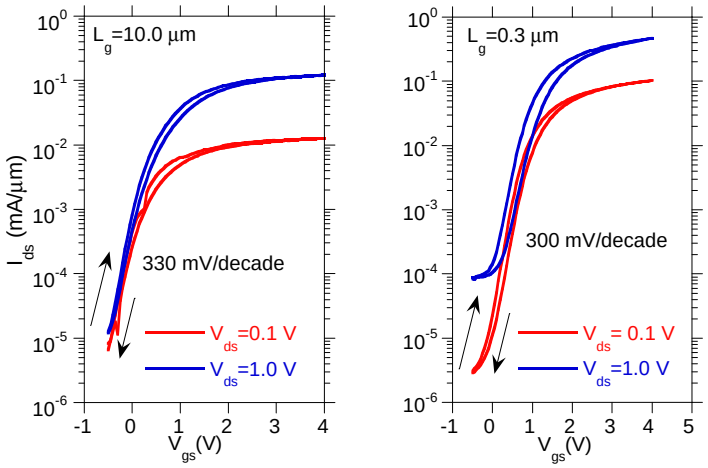


Figure 5.54: Subthreshold characteristics of 10 μm and 200 nm L_g 090326B MOSFETs.

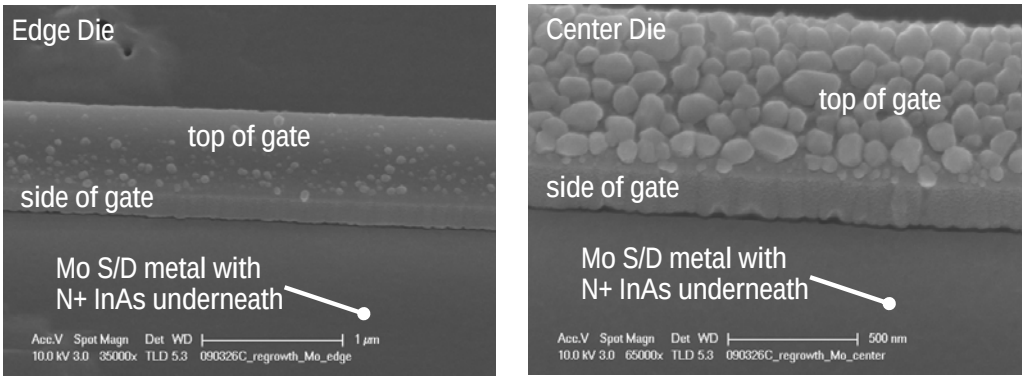


Figure 5.55: Angled SEM of MOSFET 090326C.

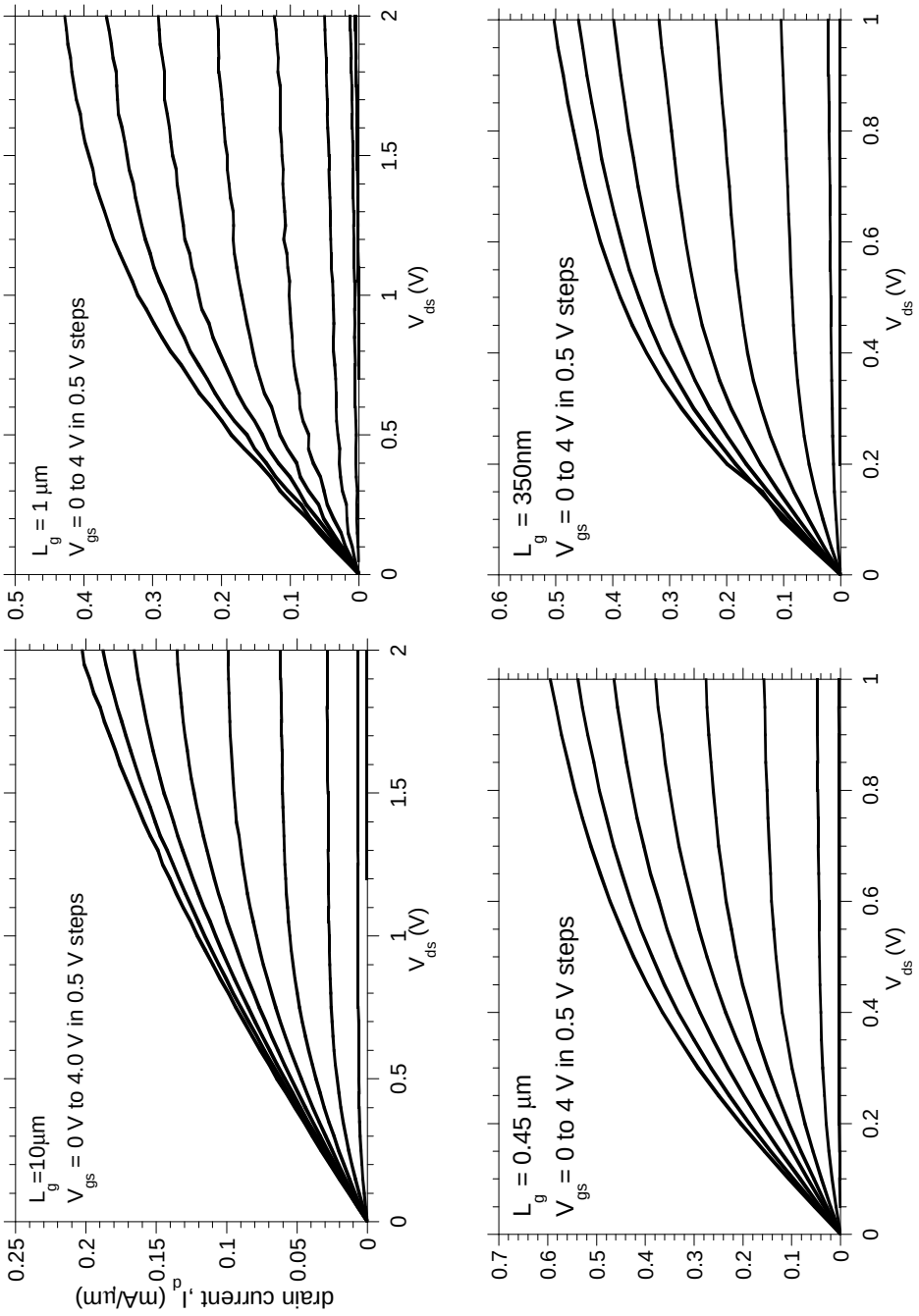


Figure 5.56: Output characteristics of the raised source/drain MOSFETs (090326C) with low As flux MEE InAs regrowth.

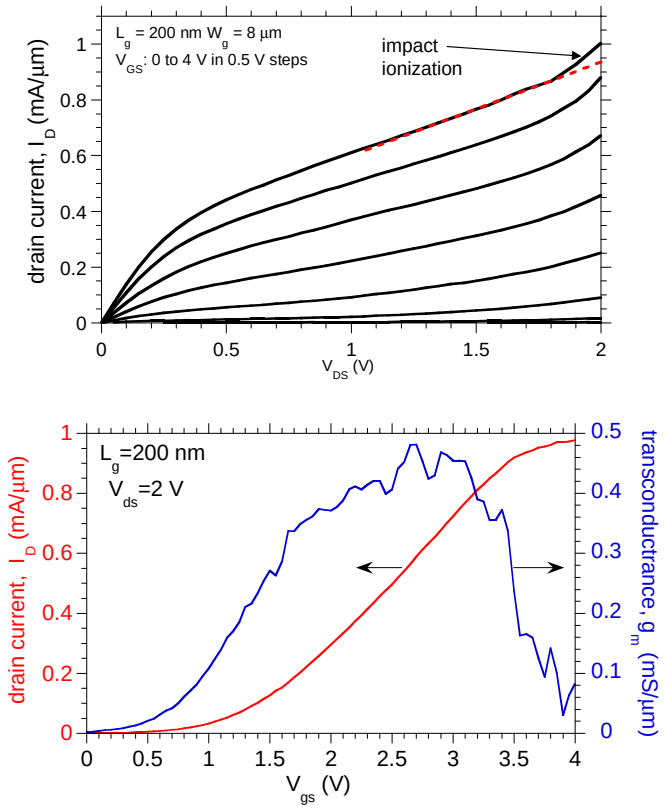


Figure 5.57: Output (top) and input (bottom) characteristics of a 200 nm L_g 090326C MOSFET.

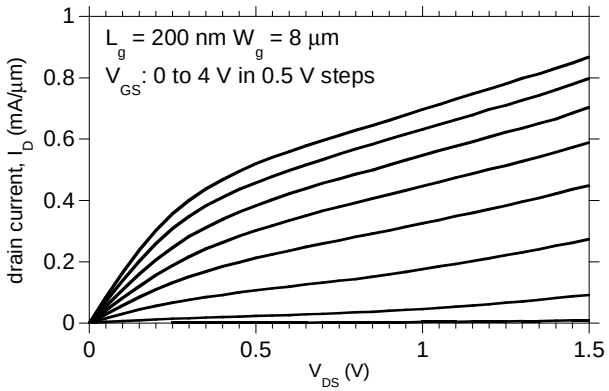


Figure 5.58: Output characteristics of a 2nd 200 nm L_g MOSFET with $V_{ds} = 1.5$ V

Wafer 090326C

50 nm of $8\times10^{19}cm-3$ Si doped InAs was grown on wafer 090326C at 500 °C at a low arsenic flux of 6.7×10^{-7} $torr$ [55]. Both H anneal and thermal desorption was done before regrowth. This regrowth is similar to the previous regrowth except for the doping and absence of post regrowth H clean. Surface reconstruction was seen before regrowth and RHEED was streaky during regrowth indicating a smooth crystalline regrowth. The SEMs show uniform filling with no slope in the regrowth profile next to gate. Gates towards the edge of the wafer show complete selectivity in regrowth. The output characteristics of the MOSFETs for different gate lengths is shown in Fig. (5.56). The devices have good saturation for gate lengths $10\mu m$ to 0.2 μm. The threshold voltage is approximately $0.6 - 0.75V$. The output and input characteristics of the 0.2 L_g device is shown in Fig. (5.57). The drive

current and transconductance at $V_{gs} = 4$ V and $V_{ds} = 2.0$ V is enhanced by $\sim 20\%$ because of impact ionization. The peak drive current and transconductance are 0.95 mA/μm and 45 mS/μm at $V_{gs} = 4.0V$ and $V_{ds} = 2.0V$. Fig. (5.58) shows another 200 nm L_g device with $V_{ds} = 1.5$ V, the peak drive current is 0.8 $mA/\mu m$ at $V_{gs} = 4.0$ V with a low on resistance of 600 $\Omega - \mu m$. TLMs on of the regrowth show sheet resistance of 23 $\Omega/\square$ and contact resistance of 3.5 Ω μm ^{2}. The on resistance scales with the gate length as shown in Fig. (5.59). Because of the scatter in the R_{on} vs. gate length plot, the intercept depends on the fit used hence giving different value for the access resistance. But The R_{on} of the $0.2\mu m$ device puts 300 Ω-μm as the upper limit on the source resistance. The sub-threshold characteristics for two different gate lengths is shown in Fig. (5.60). The long channel MOSFET has a high sub-threshold swing of $\sim$ 300 mV/decade and the 200 nm L_g device has a sub-threshold swing of $\sim$ 500 mV/decade.

5.6.4 Analysis

Several improvement in these devices are evident compared to the devices reported in Sec.(5.4). The selectivity and regrowth profile next gate has improved with low arsenic flux. These are enhancement mode devices with low on resistances, proving the scalability of the MBE regrowth. The on resistance of the devices do not saturate and degrade at sub-0.5 μm gate lengths as was the case

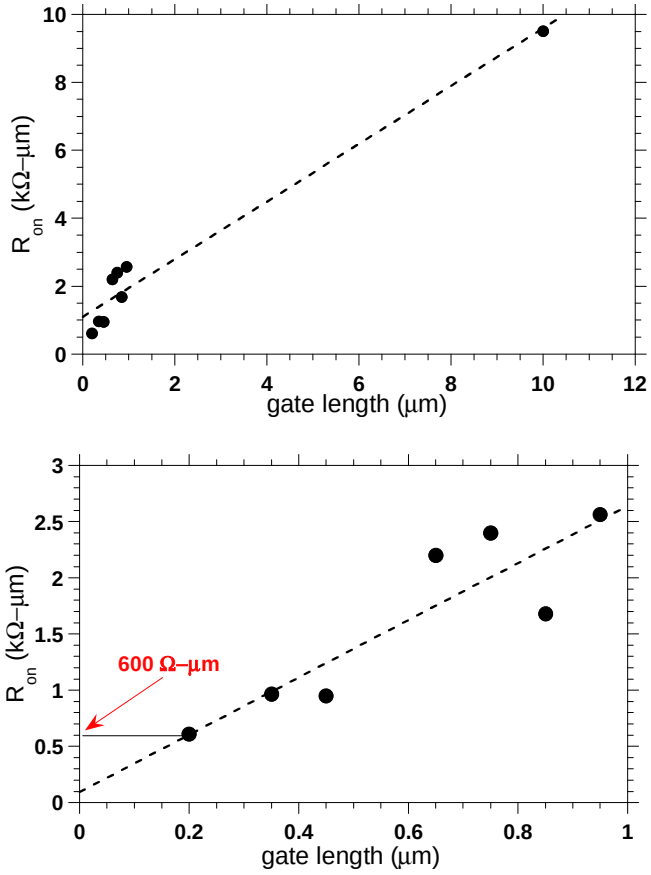


Figure 5.59: R_{on} Vs. L_g for 090326C MOSFET.

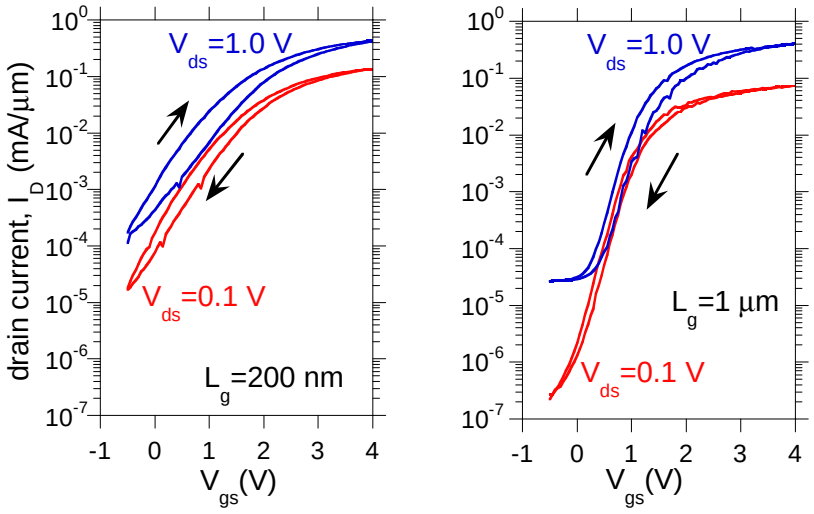


Figure 5.60: Subthreshold characteristics of 1 μm and 200 nm L_g 090326C MOSFETs.

with the devices in Sec.(5.4). This suggests that regrowth has no significant dependence on the gate length and can be used for sub-100nm gate lengths. The performance of InAs source/drain FETs is comparable in fact marginally better than $In_{0.53}Ga_{0.47}As$ source/drain FETs, indicating the InAs/$In_{0.53}Ga_{0.47}As$ interfacial resistance is not limiting the source resistance in these devices. Among InAs source/drain FETs, wafer 090326A with normal As flux regrowth has significantly lower drive current at sub-micron gate lengths compared to wafers 090326B and 090326C. The regrowth profile for 090326A, as seen in the SEMs (Fig. (5.49)) has a slope near the gate, which leads to electron depletion next to the gate. Low

arsenic flux MEE regrowth is found to be the key to low resistive regrowth next to gate. Table (5.10) summarizes the different regrowth techniques.

Table 5.10: Summary of different regrowth techniques.

Growth	Observation	Effect on R_s
MBE	Gaps near gate	Electron depletion and high R_s ($\sim M\Omega - \mu m$)
MEE	No Gaps near gate, slope in regrowth	Low R_s, but increase in R_s for $L_g \leq 0.6\mu m$
Low As MEE	No gaps, uniform filling next to gate	Lowest R_s, R_{on} scales with L_g

The sub-threshold swing for all four MOSFET wafers were similar. Wafer 090326B had undergone a post regrowth H anneal for 30 minutes. But there is no significant change in the sub-threshold swing compared to other wafers, hence the 30 min H anneal may be insufficient to anneal out traps if any. The sub-threshold swing of the long channel devices ($L_g = 10\ \mu m$ and $1\ \mu m$) is 300 mV/decade for all the devices. There is substantial dispersion in the subthreshold plots suggesting charge trapping at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. From Eq. (3.4), with a depletion width equal to quantum well width of 5 nm the extracted D_{it} of the high-k dielectric is $2 \times 10^{13}\ cm^{-2}eV^{-1}$. The calculated threshold voltage of the device (090326C) assuming a tungsten vacuum work function of 4.55 eV [56] and no D_{it} at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface is -0.75 V. The observed threshold

voltage is approximately 0.6-0.75 Volts. The discrepancy in threshold can be attributed to dielectric-semiconductor interface charge D_{it}. Given the dielectric thickness ($2.5nm$ EOT), a defect density of $D_{it} = C_{ox} \cdot \Delta V/q = 1 \times 10^{13} cm^{-2}$ (1.5×10^{13} $cm^{-2}eV^{-1}$) at the interface, negatively charged, would explain the discrepancy between measured and calculated threshold voltage. This number is comparable to the extracted D_{it} from the sub-threshold swing. The threshold voltage shift could also be due to a small shift in the work function of the sputtered W on Al_2O_3 [56].

The sub-threshold swing is 500 mV/decade for the 0.2 μm device (Fig. (5.60)). This higher value cannot be completely attributed to DIBL or electrostatics as the gate length is 40 times larger than the quantum well thickness of 5 nm. The possible explanation is loss of electron confinement under source/drain regions. Fig. (5.61) shows the band diagram under the source/drain regions. The InAs layer was assumed to be completely relaxed and has a bandgap of 0.36eV. The Poisson solution using parabolic statistics show 2×10^{19} cm^{-3} electron concentration in the channel and the Fermi level is above the $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As$ conduction band offset (Fig. (5.61)). Given high doping levels non-parabolic statistics has to be used. With n=$4 \times 10^{19} cm^{-3}$ ([Si]=$8 \times 10^{19} cm^{-3}$) in the InAs source/drain regions and 6×10^{12} cm^{-2} pulse doping, electron concentration in the 5 nm channel is approximately between $2 \times 10^{19} cm^{-3}$ to $4 \times 10^{19} cm^{-3}$. Carrier

density statistics including nonparabolic effects is reported in [57]. Given high doping, the expression simplifies to

$$n = \frac{4}{3 \cdot \sqrt{\pi}}[\phi(1 + \alpha\phi)]^{3/2} \tag{5.1}$$

where n is the electron concentration, N_c is the effective density of states, $\phi = (E_f - E_c)/kT$ and α is the non-parabolic coefficient. From this, we find $E_{fn} = 0.44eV$ at $n = 2 \times 10^{19} cm^{-3}$ and $E_{fn} = 0.61eV$ at $n = 4 \times 10^{19} cm^{-3}$ for. This is very close to the 500 meV conduction band offset between the channel and the $In_{0.48}Al_{0.52}As$ bottom barrier. This leads to poor vertical confinement of the electron current, hence poor short-channel effects. Increased p^+ back barrier doping or an increased bottom barrier energy (using e.g. an AlAsSb bottom barrier) would improve short-channel effects. Fig. (5.62) shows a band diagram of the source/drain region with higher p^+ doping and the electrons are well confined in the channel. Note that in typical HEMTs (Fig. 5.63), n_s in the source/drain regions is typically $5 \times 10^{12} cm^{-2}$ in 10 nm thick channel, the associated is approximately 350 meV, and consequently an updoped $In_{0.48}Al_{0.52}As$ bottom barrier is sufficient for electron vertical confinement.

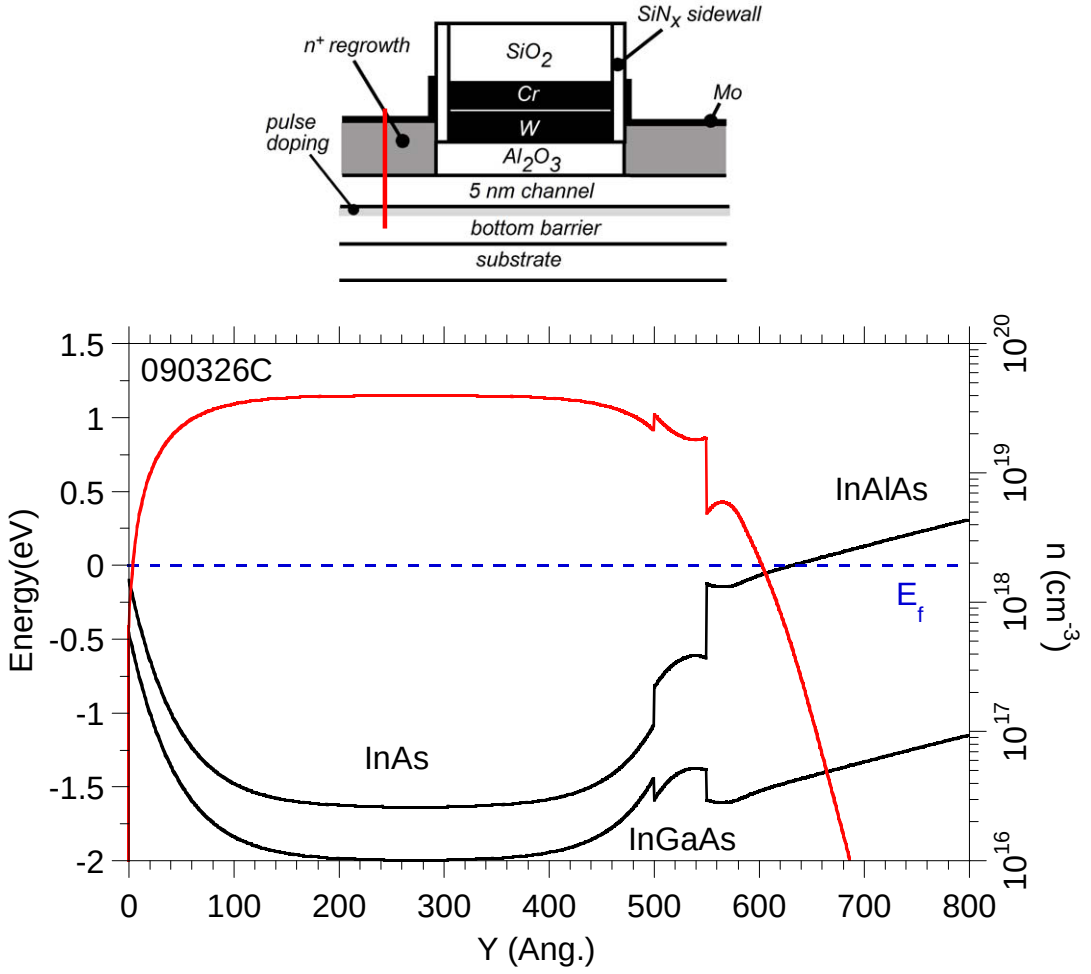


Figure 5.61: Banddiagram across the InAs source/drain region of MOSFET 090326C.

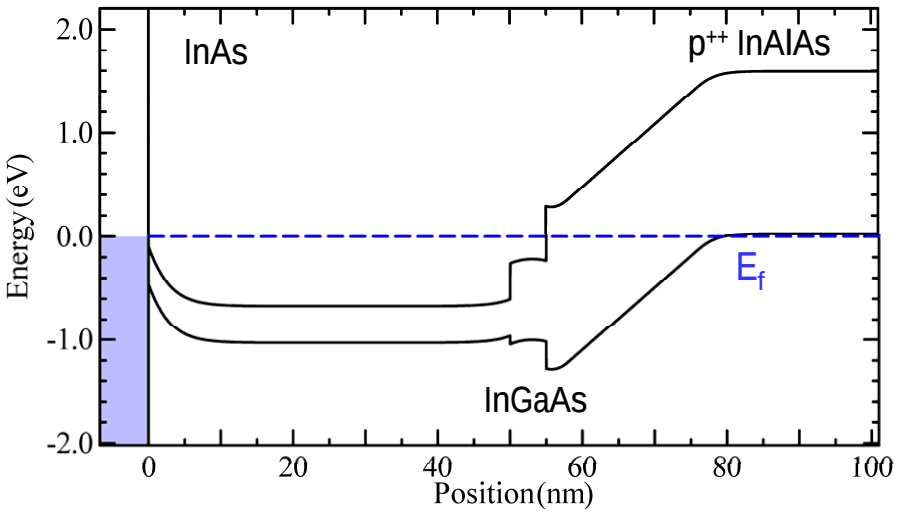


Figure 5.62: Banddiagram across the InAs source/drain region with higher p+ buffer doping

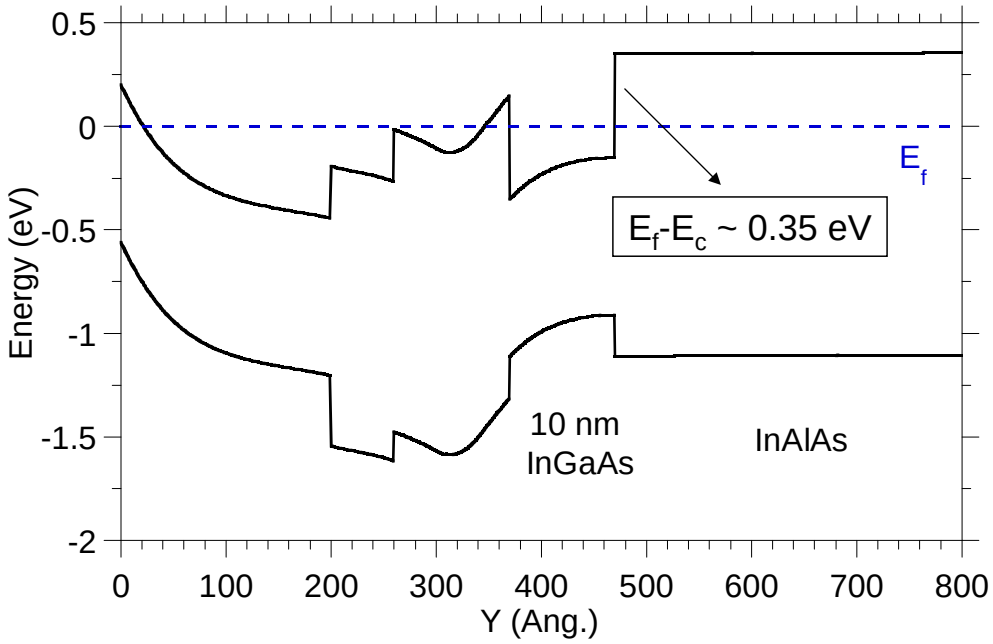


Figure 5.63: Banddiagram across the source region in a typical InGaAs HEMT.

5.6.5 Mobility Measurements

The drive current in scaled devices is given by Eq. (2.2) and is repeated here

$$I_{dsat} \approx c_{ox} W_g \upsilon_{sat} (V_g - V_t - \upsilon_{sat} L_g / \mu_n) \tag{5.2}$$

At 22 nm L_g a mobility of 1000 $cm^2/V \cdot s$ would degrade the gate overdrive only by 10 %. A major concern in scaled $In_{0.53}Ga_{0.47}As$ MOSFETs is the mobility in a 5 nm channel with high-k dielectric may degrade to such a low value ($\leq$ 100) that the MOSFET may not realize the ballistic currents. Mobility extraction for these devices was carried out by Prof. Yuan Taur's group at UCSD, the data is presented below.

The on resistance of a device is given by

$$R_{on} = R_{ch} + R_s + R_d \tag{5.3}$$

which can be approximated to $R_{on} = R_{ch}$ at large gate lengths when the channel resistance dominates. So the on resistance at low V_{ds} is therefore

$$R_{on} = \frac{V_{ds}}{I_{ds}} \approx \frac{L_g}{\mu_{eff} W_g Q_i} \tag{5.4}$$

where μ_{eff} is the channel mobility and Q_i is the inversion or electron charge. A typical C-V measurement of a MOSFET with source and drain tied to ground is shown in Fig. (5.64). The area under the C-V curve gives the inversion charge

$$Q_i = \int_{-\infty}^{V_{gs}} C_{inv}(V_{gs})\, dV_{gs}. \tag{5.5}$$

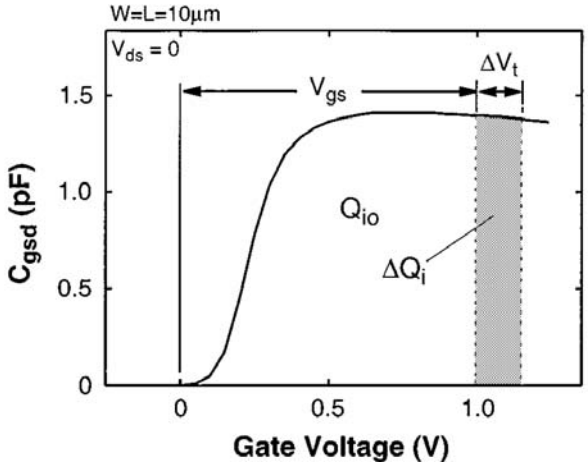


Figure 5.64: Experimental gate to source/drain capacitance in a Si MOSFET [58]. The area under the C-V curve gives the inversion or electron charge.

From Eqs. (5.4) and (5.5) the channel mobility (μ_{eff}) is extracted as a function of gate voltage.

In the presence of D_{it} the C-V profile will have a frequency dependence. In the presence of D_{it} the equivalent circuit in a C-V set up is shown in Fig. (5.65). If the frequency of measurement is higher than the characteristic frequency response of the traps ($f_{it} \propto 1/\tau_{it}$) then the measured capacitance is only from the electrons in the channel or inversion charge. The equivalent capacitance at high frequency ($f > f_{it}$) is then given by (Fig. 5.65)

$$C_{inv} = \frac{C_{ox}C_{qw}}{C_{ox} + C_{qw}}. \tag{5.6}$$

Fig. (5.66) shows the measured C-V for the InAs source/drain MOSFET (090326C) with frequency. The measured capacitance drops with frequency indi-

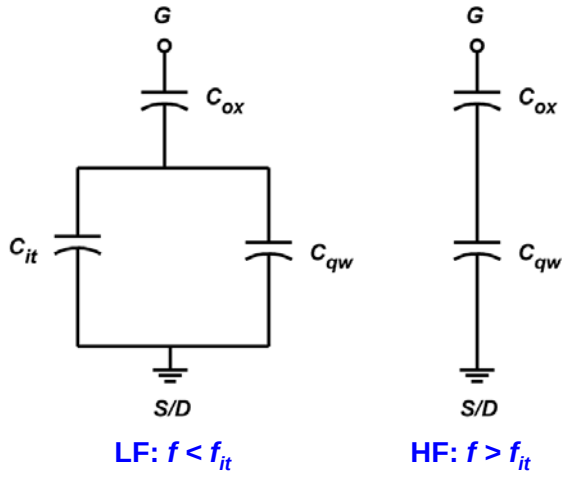


Figure 5.65: Simplified MOSFET C-V equivalent circuit in the on state with D_{it}.

cating a presence of D_{it} at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. Fig. (5.67) shows the C-V data for different gate lengths at a frequency of 100 kHz. The data shows that the capacitance value does not scale with the gate length. This is because of incomplete isolation of the gate pad as shown in Fig. (5.68). Because of incomplete isolation the gate pad also contributes to the measured capacitance. The gate pad is isolated from the active device at gate lengths below 0.5 μm, but the measured capacitance drops to very low value because of small area. Because of this small capacitance, the signal to noise ratio is high for short gate length devices. Hence C-V data with respect to frequency was carried out for long 10 μm L_g devices.

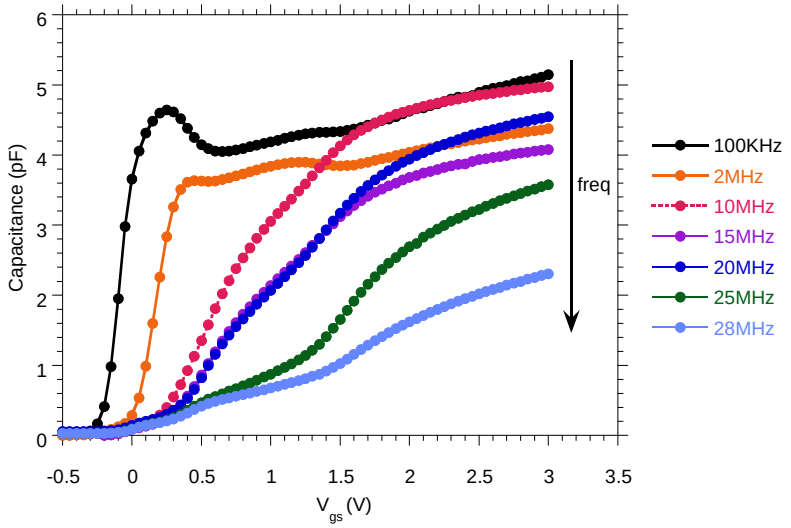


Figure 5.66: Frequency dependant gate-source/drain C-V for 10 μm L_g 090326C MOSFET. C-V measurement by Yu Yuan, Yaun Taur group, UCSD.

Fig. (5.69) shows the extracted mobility versus gate voltage from the C-V data in Fig. (5.66) and $I_d - V_g$ plot at $V_{ds} = 0.1V$. The extracted mobility could be an overestimation because of the pad capacitance contribution to the total measured capacitance. Fig. (5.70) shows the extracted D_{it} from the C-V measurement. It shows the D_{it} which respond at 100 kHZ but do not respond at 28 MHz.

Although the C-V data suggests acceptable mobility in the channel, more accurate C-V measurements are required to confirm the numbers. A C-V test structure where the pad capacitance does not contribute to the measurement is necessary. The highest frequency of measurement was also limited in the present wafer because of unshielded wafer probes used in the measurements. The present wafer

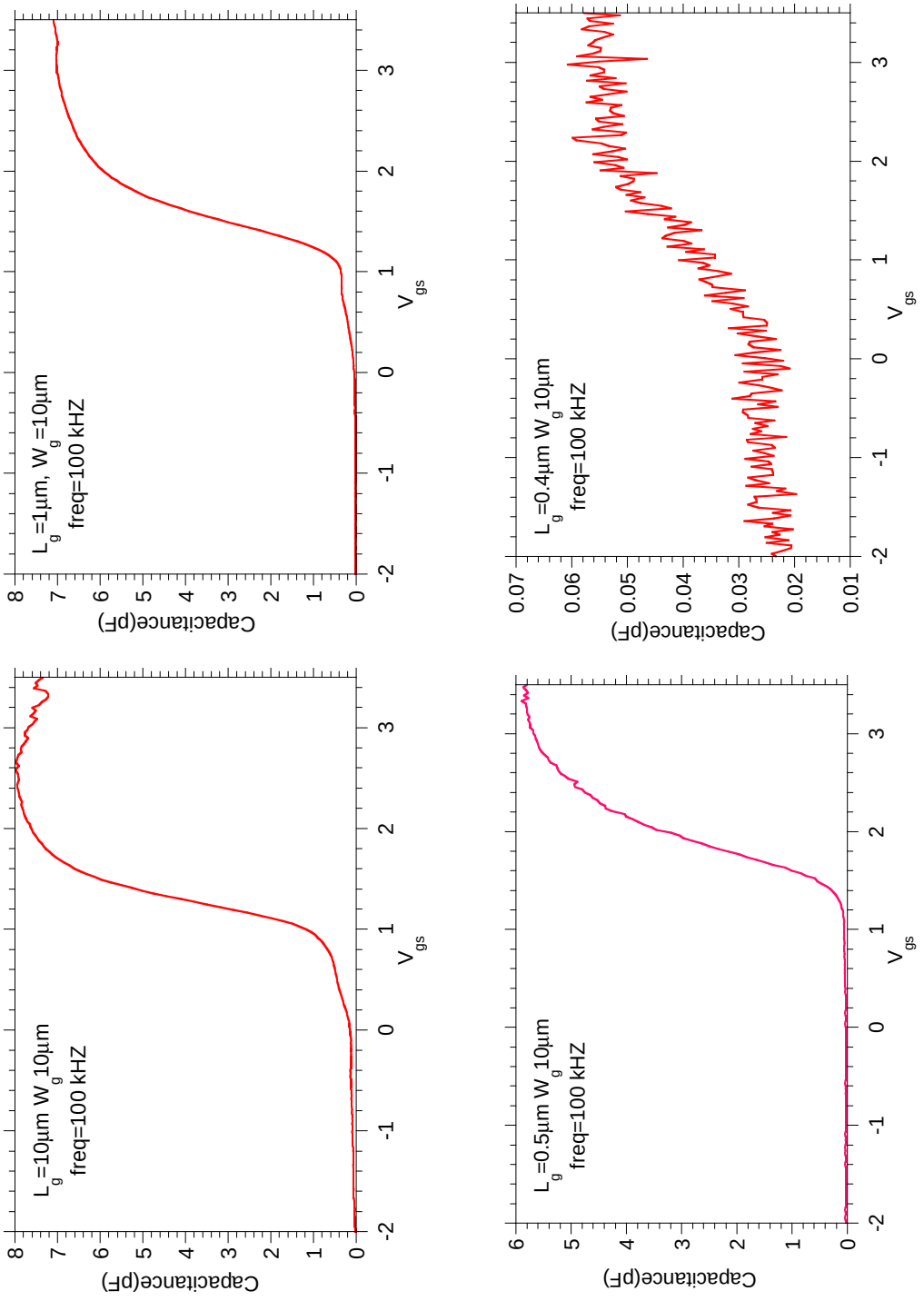


Figure 5.67: CV data for different gate lengths for raised source/drain enhancement mode MOSFETs. C-V measurement done at UCSB.

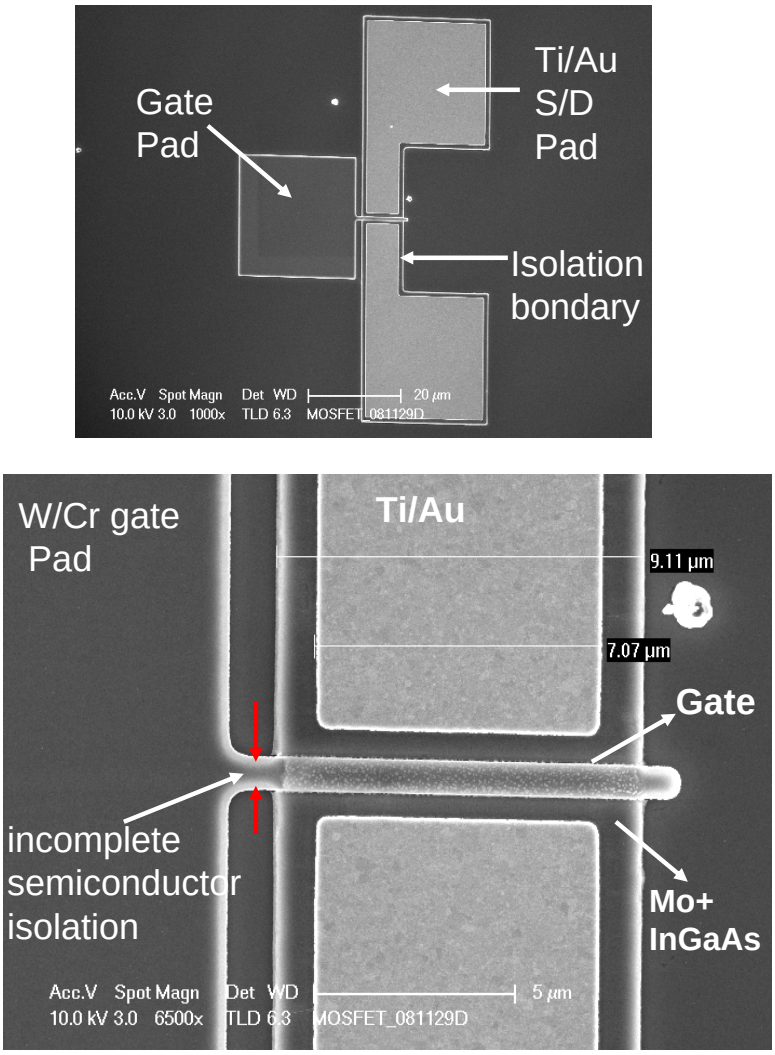


Figure 5.68: Top view SEMs of completed MOSFETs. The $In_{0.53}Ga_{0.47}As$ channel under the semiconductor is electrically connected to the active device because of insufficient undercut in long channel $L_g \geq 0.5\mu m$ devices.

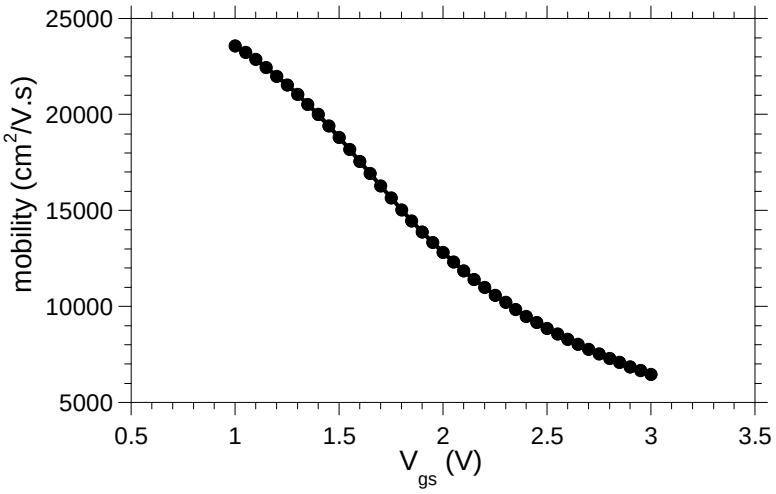


Figure 5.69: Extracted mobility Vs. gate voltage for MOSFET 090326C. Data from Yu Yuan, Yuan Taur group, UCSD

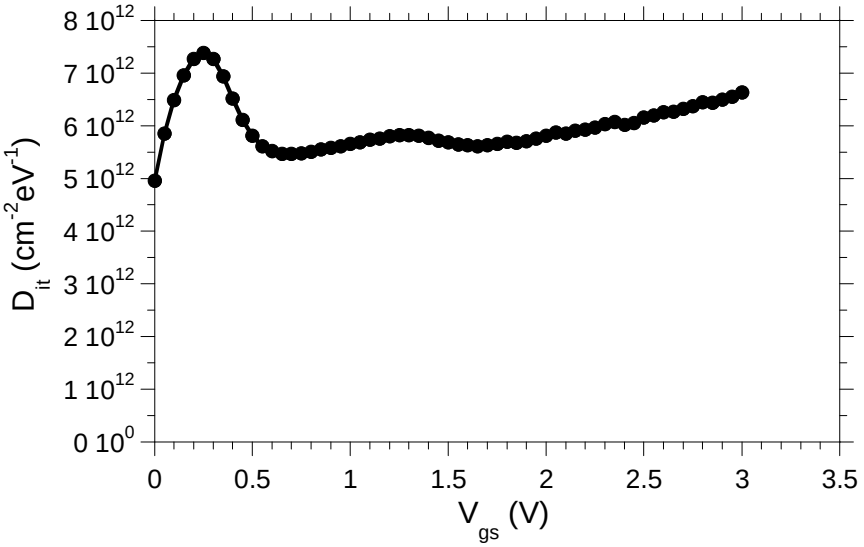


Figure 5.70: Extracted interface state density D_{it} which respond at 100 kHz but not at 28 MHz, from C-V measurement of MOSFET 090326C. Data from Yu Yuan, Yuan Taur group, UCSD

does not have probe footprints compatible with microwave wafer probes. This due to the fact that the back-end process was not done for lack of time. Finishing the back-end process (4.16) on the wafers would enable these measurements.

Chapter 6

Conclusions

Scaled $In_{0.53}Ga_{0.47}As$ channel (5 nm) MOSFETs with both self-aligned source/drain and self-aligned source/drain contacts were demonstrated. The $In_{0.53}Ga_{0.47}As$ channel layer is vertically scaled to 5 nm with $In_{0.48}Al_{0.52}As$ bottom confinement layer suitable for 22 nm L_g devices. The drive current and transconductances are not limited by the source access resistance. In this chapter, key achievements are summarized, with suggestions for future work.

6.1 Accomplishments

An all dry etch selective gate process was developed which minimizes the damage to thin channels suitable for regrowth. Following gate definition an $ex-situ$ UV ozone treatment and dilute HCl clean and $in-situ$ H clean leave an epi-ready 5 nm $In_{0.53}Ga_{0.47}As$ channel surface suitable for high quality MBE or MOCVD regrowth. Incorporating MBE regrowth and height selective etch process suc-

cessfully demonstrated self-aligned $In_{0.53}Ga_{0.47}As$ MOSFET process. Low arsenic flux InAs MEE regrown source/drain MOSFETs show the potential scalability of this process to sub-100 nm gate length devices. The ultimate scalability of $In_{0.53}Ga_{0.47}As$ MOSFETs critically depends on the minimum channel thickness that can be realized. Self-aligned regrown source/drain process can also be used as source/drain technology for extremely scaled channel thickness ($< 5nm$) devices.

$In_{0.88}Ga_{0.12}P$ sub-channel layer was developed as an alternative to InP sub-channel for recessed source/drain MOSFETs. Regrowth on thin $In_{0.88}Ga_{0.12}P$ layers was successfully demonstrated [49]. Depletion mode recess source/drain MOSFETs were also demonstrated [51].

Traditional III-V HEMT technologies have only one degree of freedom; the pulse doping to control both the threshold voltage and source resistance. With the demonstrated regrown source/drain technology both the source resistance and threshold voltages can be independently designed. Self-aligned source/drain regrowth process can also be used to scale $In_{0.53}Ga_{0.47}As$ HEMTs also by replacing the high-k with $In_{0.48}Al_{0.52}As$ gate barrier. This process can also be used to fabricate self-aligned HBTs where the base region is regrown similar to source/drain in a FET.

6.2 Future Work

Building on this successful demonstration of self-aligned process the gate length has to be scaled to sub-100 nm dimensions by using electron beam lithography. The SiN_x sidewalls must also scale to $\sim$ 10-15 nm to reduce in order to reduce source resistance to below 50 $\Omega - \mu m$. Scaling of the high-k dielectric to sub-1 nm EOT thicknesses is critical to successful demonstration of high drive currents in $In_{0.53}Ga_{0.47}As$ MOSFETs. The D_{it} of the high-k also has to improve significantly from the extracted values in the MOSFETs presented in this work.

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Appendix A

Self-aligned InGaAs MOSFET Process Flow

This appendix describes the process flow for fabricating InGaAs MOSFETs with self-aligned source/drain by MBE regrowth.

- It is very important to avoid Au and PR on wafers that are loaded into the MBE for regrowth.
  - Use separate clean tweezers and glassware with no Au contamination for pre-regrowth wafer handling

1. **Wafer cleaving and preparation**
   - The gates are oriented similar to the emitters in the UCSB DHBT process. InP substrates are cut in two different standards
     (a) European / Japan flat option wafer where the minor flat is to the left of the major flat
     (b) US flat option wafer where the minor flat is to the right of the major flat
   - To ensure proper semiconductor mesa etch undercut, the width of the gate should be oriented...
     - Perpendicular to the major flat for European / Japan flat option wafers
     - Parallel to the major flat for US flat option wafers
2. **Gate stack deposition**

- Use pre-regrowth No-Au, No-PR tweezers and glassware only
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min
- Cool wafer, 5 min
- Load into Sputter # 1
- Pump down to $\sim 10^{-6}$ *torr*, fill the Liquid N_2 trap
- Wait till the pressure reaches $5{\times}10^{-7}$ *torr* before starting the deposition
- Sputter clean the W source for 5 minutes at 200 W, 25 sccm Ar and 10 mT
- Deposit W on the MOSFET wafers for 2 minutes at 200W, 25 sccm Ar and 10 mT
- 2 minutes sputtering will deposit 80-100 nm of W, if the deposition rate changes increase or decrease time accordingly
- Unload the wafer and immediately load into E-beam evaporator #1 for Cr deposition
- Use No-Au, No-Pr tweezers and clips to handel wafer and Cr source
- Load the private Cr source
- Pump down the system to 3×10^{-6} *torr*
- Deposit 50 nm of Cr
- Unload the wafer
- During the E-beam evaporator pump-down clean the PECVD tool for 1 hour
- Deposit 370 nm of SiO_2 on the MOSFET wafer
- Unload the wafer and load into E-beam evaporator #1 for the final Cr deposition
- Pump down the system to 3×10^{-6} *torr*
- Deposit 50 nm of Cr
- Unload the wafers

3. **Gate lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min

- Cool wafer, 5 min
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'MOSFET-gate' pattern in GCA Autostepper, 0.23 sec
- Post-exposure PR bake – 110°C, 60 sec
- Develop for 2 min in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

4. **O_2 ashing and Cr etch**

   - Make sure the PE-II asher is at least 10 minute O_2 cleaned after a CF_4 etch
   - Load the wafers into the PE-II asher
   - Run 6 minute 100 W, 300 mT O_2 plasma clean to shrink the gate features
   - Unload the wafers
   - Run 10 minute O_2 clean in the Panasonic ICP etcher #1, make sure the the plasma is dull white at the end of the clean, if not run the O_2 clean again till the plasma is dull white
   - Run a 5 minute Cl_2/O_2 Cr etch to condition the chamber
   - Etch the Cr on MOSFET wafers for 2 min 30 sec with Prog 163 (26/4 Cl_2/O_2, 1 Pa, 400 W ICP, 15 W RF)
   - Unload the wafer, remove the PR by soaking the wafers in AZ 300T at 80°C for 2 hours
   - Rinse sample in 2-propanol and do solvent clean
   - Load the wafer into PE-II asher
   - Run 5 min 100 W, 300 mT O_2 plasma to remove any PR scum
   - Inspect under microscope to ensure there is no scum on the wafer

5. **Gate stack etch**

   - Run standard O_2 clean in ICP #1 till the plasma is dull white
   - Run 5 min 150 W RF SF_6/Ar SiO_2 recipe to condition the chamber

- Etch SiO_2 on MOSFET wafers for 5 min with Prog 162 (50/5 SF_6/Ar, 1 Pa, 600W ICP, 50 W RF)
- Unload the carrier wafer immediately after they come out of the ICP chamber and squirt DI water on the MOSFET wafers
- Dismount the MOSFET wafers from the Si carrier wafer, dip the wafers in a DI water beaker and rinse in DI water for 3 min
- Solvent clean and DI rinse
- Wafer should be metallic if the oxide is completely etched off, if not run the oxide etch for 1 min
- Inspect under microscope and measure the height in dektak
- Run standard O_2 clean in ICP #1 till the plasma is dull white
- Run a 5 minute Cl_2/O_2 Cr etch to condition the chamber
- Etch the Cr on MOSFET wafers for 2 min with Prog 163 (26/4 Cl_2/O_2, 1 Pa, 400 W ICP, 15 W RF)
- Unload the carrier wafer immediately after they come out of the ICP chamber and squirt DI water on the MOSFET wafers
- Dismount the MOSFET wafers from the Si carrier wafer, dip the wafers in a DI water beaker and rinse in DI water for 3 min
- Solvent clean and DI rinse
- Slight color change is visible after the Cr etch, inspect under microscope, the top Cr should be gone and the oxide is visible on the gates
- Run standard O_2 clean in ICP #1 till the plasma is dull white
- Run 5 min 150 W RF SF_6/Ar SiO_2 recipe to condition the chamber
- Etch W on MOSFET wafers for 2 min with Prog 162 (5/5 SF_6/Ar, 0.5 Pa, 600W ICP, 15 W RF)
- Unload the carrier wafer immediately after they come out of the ICP chamber and squirt DI water on the MOSFET wafers
- Dismount the MOSFET wafers from the Si carrier wafer, dip the wafers in a DI water beaker and rinse in DI water for 3 min
- Solvent clean and DI rinse
- Inspect under microscope and make sure that W is completely etched off

6. **SiN_x Sidewalls**

- Clean PECVD for 1 hour and deposit 20 nm of SiN_x
- Solvent clean
- Deposit 30 nm of SiN_x on MOSFET wafers and a Si dummy
- Deposit 100 nm of SiN_x on a 2 inch Si wafer
- Measure the SiN_x thickness on the Si wafers in Ellipsometer
- Run standard O_2 clean in ICP #1 till the plasma is dull white
- Run a 5 minute CF_2/O_2 etch to condition the chamber
- Etch the 100 nm SiN_x on Si wafers with 10/2 CF_2/O_2, 0.3 Pa, 100 W ICP and 15W RF power to calculate the etch rate
- Run SiN_x etch on MOSFET wafers using the etch rate calculated from the previous step, do a 15 % over-etch
- Unload the carrier wafer immediately after they come out of the ICP chamber and squirt DI water on the MOSFET wafers
- Dismount the MOSFET wafers from the Si carrier wafer, dip the wafers in a DI water beaker and rinse in DI water for 3 min
- Solvent clean and DI rinse
- Inspect under microscope

7. **Al_2O_3 etch**

   - Solvent clean
   - Etch 5 nm of Al_2O_3 in AZ 400K developer for 5 min
   - DI rinse for 5 min and N_2 dry
   - Inspect under microscope, surface should be smooth

8. **Surface preparation before regrowth**

   - Prepare the UV-Ozone reactor – run empty for 30 min
   - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
   - Dehydration bake – 120°C, 5 min
   - Cool wafer, 5 min
   - Surface preparation – oxidize wafer surface in ozone reactor, 30 min
   - Prepare 1:10 HCl:H_2O solution in the MBE lab
   - Unload the wafers from the ozone reactor, take them to MBE lab

- Etch the surface oxide in 1:10 HCl:H_2O for 1 min, DI rinse for 1 min, N_2 dry
- Mount onto MBE wafer carrier and load into the MBE chamber
- InGaAs or InAs regrowth and *in-situ* Mo deposition

9. **Height selective etching**

   - Inspect the wafers in SEM
   - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
   - Dehydration bake – 120°C, 5 min
   - Cool wafer, 5 min
   - Photoresist spin – SPR-510, 4 kRPM, 30 sec
   - Pre-exposure PR bake – 90°C, 60 sec
   - Measure PR thickness in Filmetrics – should be $\sim$ 1000 nm
   - Run 30 min O_2 ashing in ICP #1 with 300 sccm O_2, 50 Pa, 1500W at 50°C to condition the chamber
   - Run 35-40 min O_2 ashing in ICP #1 with 300 sccm O_2, 50 Pa, 1500W at 50°C on MOSFET wafers till the top of the gates are exposed
   - Measure the PR thickness using Filmetrics, target thickness is 300-350 nm
   - Dektak on the gate feature to make sure the top of the gates are exposed
   - Run standard O_2 clean in ICP #1 till the plasma is dull white
   - Run 5 min 150 W RF SF_6/Ar SiO_2 recipe to condition the chamber
   - Etch Mo on MOSFET wafers for 2 min with Prog 162 (5/5 SF_6/Ar, 0.5 Pa, 600W ICP, 15 W RF)
   - Unload the wafer, remove the PR by soaking the wafers in AZ 300T at 80°C for 2 hours
   - Rinse sample in 2-propanol and do solvent clean
   - Inspect wafer using optical microscope, should see the top SiO_2 on top of sub-micron gates if the Mo is etched off
   - Inspect the wafers in SEM to make sure the Mo is etched off from top of the gates, if not re-do the height selective etch

10. **Source/drain Pad Lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min
- Cool wafer, 5 min
- Photoresist spin – nLOF-5510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'MOSFET-SD' pattern in GCA Autostepper, 0.7 sec
- Post-exposure PR bake – 110°C, 60 sec
- Develop for 1 min 30sec in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

11. **Source/drain Pad metal deposition**

- Vent E-beam 4, load private sources – Ti, Pd, and Au
- Load wafers in E-beam 4
- Allow system to pump-down for 90 min to 3×10^{-6} torr
- Deposit source/drain contact
  - Ti 20 nm
  - Pd 40 nm
  - Au 150 nm
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Rinse sample in 2-propanol and do solvent clean
- Inspect wafer using optical microscope, dektak the source/drain pad metal thickness

12. **Device isolation-1 lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min
- Cool wafer, 5 min
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'MOSFET-ISO1' pattern in GCA Autostepper, 0.3 sec

- Post-exposure PR bake – 110°C, 60 sec
- Develop for 2 min in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope, measure PR height in dektak

13. **Device isolation-1 etch**

- Run standard O_2 clean in ICP #1 till the plasma is dull white
- Run 5 min 150 W RF SF_6/Ar SiO_2 recipe to condition the chamber
- Etch Mo on MOSFET wafers for 2 min 30 sec using Prog 162 (5/5 SF_6/Ar, 0.5 Pa, 600W ICP, 15 W RF)
- The field should be greenish-blue if all the Mo is etched
- Measure the PR height in dektak
- Prepare three beakers with
- H_3PO_4:H_2O_2:H_2O, 1:1:25 – use stirrer at 200 RPM
- Etch InGaAs or InAs regrowth, InAlAs buffer in H_3PO_4:H_2O_2:H_2O $\approx$ 2 min 30 sec
- Rinse sample in DI for 2 min
- Measure PR height by dektak to make sure the the etch has reached the InP substrate
- Strip PR mask – 1165 stripper, 80°C, 30 min
- Rinse sample in 2-propanol and do solvent clean
- Inspect under microscope and measure mesa height using dektak

14. **Device isolation-2 lithography**

- A second isolation is done to etch the Mo between TLM pads
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min
- Cool wafer, 5 min
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'MOSFET-ISO2' pattern in GCA Autostepper, 0.3 sec
- Post-exposure PR bake – 110°C, 60 sec

- Develop for 2 min in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope, measure PR height in dektak

15. **Device isolation-2 etch**

- Run standard O_2 clean in ICP #1 till the plasma is dull white
- Run 5 min 150 W RF SF_6/Ar SiO_2 recipe to condition the chamber
- Etch Mo on MOSFET wafers for 2 min 30 sec using Prog 162 (5/5 SF_6/Ar, 0.5 Pa, 600W ICP, 15 W RF)
- Inspect under microscope
- Measure the DC gate pad height in dektak
- Etch the top SiO_2 cap on the DC pads in BHF for 1 min 30 sec
- Inspect and dektak to make sure the SiO_2 cap is gone on the DC gate pads
- Strip PR mask – 1165 stripper, 80°C, 30 min
- Rinse sample in 2-propanol and do solvent clean
- Inspect under microscope
- Measure devices and TLMs, if the device performance is good proceed to the back-end process

16. **Gate post Lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min
- Cool wafer, 5 min
- Photoresist spin – nLOF-2020, 4 kRPM, 30 sec
- Pre-exposure PR bake – 110°C, 60 sec
- Shoot 'MOSFET-GVIA' pattern in GCA Autostepper, 0.16 sec
- Post-exposure PR bake – 110°C, 60 sec
- Develop for 2 min in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope, measure PR height in dektak

17. **Gate Post deposition**

    - Vent E-beam 4, load private sources – Ti and Au
    - Surface preparation – BHF 30 sec, DI rinse and N_2 dry
    - Load sample in E-beam 4
    - Allow system to pump-down for 90 min to 3×10^{-6} torr
    - Deposit gate post
      - Ti 20 nm
      - Au 1000 nm
    - Metal liftoff – 1165 stripper, 80°C, 2 hr
    - Rinse sample in 2-propanol and do a solvent clean
    - Inspect wafer using optical microscope, measure the metal height using dektak

18. **Source/drain Post Lithography**

    - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
    - Dehydration bake – 120°C, 5 min
    - Cool wafer, 5 min
    - Photoresist spin – nLOF-2020, 4 kRPM, 30 sec
    - Pre-exposure PR bake – 110°C, 60 sec
    - Shoot 'MOSFET-SDVIA' pattern in GCA Autostepper, 0.16 sec
    - Post-exposure PR bake – 110°C, 60 sec
    - Develop for 2 min in AZ 300-MIF developer
    - Rinse wafer – DI water for 2 min, N_2 dry
    - Inspect wafer using optical microscope, measure PR height in dektak

19. **Source/drain Post deposition**

    - Vent E-beam 4, load private sources – Ti and Au
    - Load sample in E-beam 4
    - Allow system to pump-down for 90 min to 3×10^{-6} torr
    - Deposit S/D post
      - Ti 20 nm

  - Au xxx nm
- The S/D Au thickness should be such that the top of S/D post lines up with the top of gate post
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Rinse sample in 2-propanol and do a solvent clean
- Inspect wafer using optical microscope, measure the metal height using dektak

20. **BCB passivation**

- Prepare the 'Blue Oven' – run N_2 through chamber at 100%
- Prepare ozone reactor – run empty, 20 min
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 5 min
- Cool wafer, 5 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Spin coat wafer with BCB 3022-46 at 4k rpm for 30 sec
- Soft bake 110°C 60 sec
- Cure in 'Blue Oven'
- Load and run Program 5 (confirm in case it has been altered)
- Program sequence:
  (a) 5 min ramp to 50°C, 5 min soak
  (b) 15 min ramp to 100°C, 15 min soak
  (c) 15 min ramp to 150°C, 15 min soak
  (d) 60 min ramp to 250°C, 60 min soak
  (e) Natural cool down
  (f) Oven off
- Remove sample and inspect under the microscope
- Measure BCB thickness using Nanometrics should be ≈ 1.88 μm
- Turn off the 'Blue Oven'

21. **Wafer planarization**

- Make sure the temperature of the ashing stage is 50 °C
- Clean and condition the ashing chamber ICP #1 – CF_4/O_2 50:200 sccm, 7 min
- Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 2 min
- Measure the BCB height using Nanometrics, etch till the top of the posts are exposed
- Inspect sample in FEI SEM to see if the device contacts and interconnect posts are exposed
- Repeat the above etch (1 min increments) and inspection until all contact and posts are exposed

22. **SiN_x deposition and etch**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120°C, 5 min
- Cool wafer, 5 min
- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:H_2O 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Deposit 100 nm SiN_x on the BCB surface by PECVD
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90°C, 60 sec
- Shoot 'MOSFET-PAD' pattern in stepper, 0.3 sec
- Post-exposure PR bake – 110°C, 60 sec
- Develop for 2 min in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope, measure PR height in dektak
- Run standard O_2 clean in ICP #1 till the plasma is dull white
- Run a 5 minute CF_2/O_2 etch to condition the chamber
- Run SiN_x etch on MOSFET wafers using the etch rate calculated from the Sidewall etch step, do a 15 % over-etch

- Inspect wafer in SEM to make sure the posts are exposed
- Strip PR in 1165 stripper, 80°C, 20 min
- Rinse sample in 2-propanol and do a solvent clean
- Inspect wafer using optical microscope,

23. **Metal-1 interconnect lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Photoresist spin – nLOF 2020, 4 kRPM, 30 sec
- Pre-exposure PR bake – 110°C, 60 sec
- Shoot 'Metal 1' pattern in GCA Autostepper, 0.16 sec
- Post-exposure PR bake – 110°C, 60 sec
- Develop for 2 min in AZ 300-MIF developer
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope, measure PR height in dektak

24. **Metal-1 interconnect deposition**

- Vent E-beam 4, load private sources – Ti and Au
- Load sample in E-beam 4
- Allow system to pump-down for 90 min to 3×10^{-6} torr
- Deposit Metal 1
  - Ti 20 nm
  - Au 1000 nm
- Metal liftoff – 1165 stripper, 80°C, 2 hr
- Rinse sample in 2-propanol and do a solvent clean
- Inspect wafer using optical microscope, measure the metal height using dektak
- Measure devices