University of California
Santa Barbara

Gate Last InGaAs MOSFETs with Regrown Source-Drain Regions and ALD Dielectrics

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

Andrew Carter

Committee in charge:

Professor Mark Rodwell, *Chairman*

Professor John Bowers

Professor Arthur Gossard

Professor Umesh Mishra

June 2013

The dissertation of
Andrew Carter is approved:

Professor John Bowers

Professor Arthur Gossard

Professor Umesh Mishra

Professor Mark Rodwell, *Committee Chairman*

June 2013

Gate Last InGaAs MOSFETs with

Regrown Source-Drain Regions and

ALD Dielectrics

by

Andrew Carter

Acknowledgments

These last four and some odd years would not be possible with the help and dedication of everyone in my life. I want to thank my committee members for overseeing this research and providing guidance as necessary. Mark Rodwell has been a tremendous Ph.D. advisor and colleague during my time at UCSB. His commitment to excellence in cleanroom work, device physics, and circuit design is second to none. Without his constant motivation, none of this work would have been possible. Thanks to Art Gossard for maintaining a top-notch MBE facility to supply epi material for this project. Last but not least, thanks to Umesh Mishra and John Bowers for their comments on the dissertation.

These days, an experimental device physicist is nothing without a cleanroom. I am proud to say the UCSB cleanroom is one of, if not the best, university cleanroom in the world. Jack Whaley and Tom Reynolds have put together a great team that never skips a beat. Brian Thibeault and Bill Mitchell have provided an unending supply of advice and support in my experiments. Their help has made these device results possible. Also, thanks to all the other staff members: Brian Lingg, Adam, Tony, Don, Ning, Aidan, Mike Silva, Mike Day, Luis, and Tino. Rest in peace Pat!

The Rodwell Group members, past and present, have always kept a smile on my face through four years of arduous cleanroom work. Jeremy Law and I started on III-V MOS at the same time, working through all the processing and regrowth issues. Sanghoon Lee's process development on gate last FETs made the process what it is today. Thanks to Cheng-Ying for growing our epi, and Doron for getting the MOCVD regrowth fired up and making the final results of this dissertation possible.

Thanks to the other research groups in ECE, especially my friends in the Bowers and Mishra labs. A big thanks also goes out to the staff of CNSI. Thanks to Tom Mates for running the XPS and SIMS tools. Thanks to Stephan Kramer for making FIB and TEM seem easy!

Other than my Ph.D. committee, I have two important mentors in my electrical engineering career. Sheldon Epstein, K9APE, introduced me to amateur radio when I was in high school. He gave me a taste for soldering and electronic tinkering. It served me well ever since. My other mentor is Prof. Gary Bernstein at the University of Notre Dame. Thanks to his patience with an over-excitable engineering summer camp attendee, I gained an appreciation for cleanroom work and semiconductor devices.

My friends and family have been always encouraged me to set my standards high and my chin up. My parents, siblings, aunts, uncles, and cousins have always been there for me during my Ph.D. work. My friends, both local and abroad, have been a dependable sounding board all my life. Special thanks to Peter Mage for proofreading this entire manuscript in record time. Your mastery of the English language is second to none. Thanks to Evan Lobisser for providing me his LaTeX template to typeset my dissertation. You saved me at least a day of work.

Last, thanks to Sasha for putting up with homebrewing, incredibly late nights in the cleanroom, and in general being baffled about what I do. I guarantee this document will not help.

Andy Carter
June 2013

Curriculum Vitæ of
Andrew Carter

Research Interests

III-V MOSFETs, Semiconductor Device Characterization, Atomic Layer Deposition, Scanning Electron Microscopy

Education

2013	Ph.D. in Electrical and Computer Engineering University of California, Santa Barbara, CA
2010	M.S. in Electrical and Computer Engineering University of California, Santa Barbara, CA
2008	B.S. in Electrical and Computer Engineering University of Notre Dame, IN

Experience

2008–2013	Graduate Student Researcher University of California, Santa Barbara, CA
2005–2008	Undergraduate Researcher University of Notre Dame, IN

Journal Publications

Sanghoon Lee, Jeremy J. M. Law, **Andrew D. Carter**, Brian J. Thibeault, William Mitchell, Varistha Chobpattana, Stephan Krämer, Susanne Stemmer, Art C. Gossard, and Mark J. W. Rodwell. "Substitutional-Gate MOSFETs with Composite ($In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$) Channels and Self - Aligned MBE Source - Drain Regrowth." IEEE Electron Device Letters, Electron Device Letters, IEEE, Vol. 33, No. 11, pp.1553-1555, Nov. 2012.

Gary H. Bernstein,**Andrew D. Carter**, and David C. Joy. "Do SE_{II} Electrons Really Degrade SEM Image Quality?" Scanning, accepted.

Andrew D. Carter, William J. Mitchell, Brian J. Thibeault, Jeremy J.M. Law,

and Mark J.W. Rodwell. "Al_2O_3Growth on (100) $In_{0.53}Ga_{0.47}As$ Initiated by Cyclic Trimethylaluminum and Hydrogen Plasma Exposures." Appl. Phys. Express, 4 (2011) 091102.

Greg J. Burek , Yoontae Hwang, **Andrew D. Carter**, Varistha Chobpattana, Jeremy L. M. Law, William J. Mitchell, Mark J.W. Rodwell. "Influence of Gate Metallization Processes on the Electrical Characteristics of High-k/$In_{0.53}Ga_{0.47}As$ Interfaces." J. Vac. Sci. Technol. B 29 (2011) 040603.

Conference Publications

Sanghoon Lee, Cheng-Ying Huang, **Andrew D.Carter**, Jeremy J. M. Law, Doron C. Elias,Varistha Chobpattana, Brian J. Thibeault, William Mitchell, Susanne Stemmer, Arthur C. Gossard, Mark J. W. Rodwell. "High Transconductance Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFETs Using MBE Source-Drain Regrowth and Surface Digital Etching." 25th IEEE International Conference on Indium Phosphide and Related Materials(IPRM) 2013, Kobe, Japan.

Andrew D. Carter, S. Lee, D.C. Elias, C.-Y. Huang, J. J. M. Law, W. J. Mitchell1, B. J. Thibeault, V. Chobpattana, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell. "Performance Impact of Post-Regrowth Channel Etching on InGaAs MOSFETs Having MOCVD Source-Drain Regrowth." Device Research Conference 2013, Notre Dame, Indiana.

J. J. M. Law, **Andrew D. Carter**, S. Lee, A. C. Gossard, and M. J. W. Rodwell Regrown Ohmic Contacts to InxGa1-xAs Approaching the Quantum Conductivity Limit. Device Research Conference 2012.

S. Lee, **A. D. Carter**, J. J. M. Law, D. C. Elias, V. Chobpattana, H. Lu, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "High Performance Substitutional-Gate MOSFETs Using MBE Source-Drain Regrowth and Scaled Gate Oxides." 24th IEEE International Conference on Indium Phosphide and Related Materials, August 27-30, 2012 University of California, Santa Barbara, CA USA.

J. J. M. Law, **A. D. Carter**, S. Lee, A. C. Gossard, M. J. W. Rodwell "Contact Resistance Limits of Ohmic Contacts to Thin Semiconductor Channels." Conference on the Physics and Chemistry of Surfaces and Interfaces, 22 Jan 2012 to 26 Jan 2012, Santa Fe, New Mexico.

J. J. M. Law, **A. D. Carter**, G. B. Burek, B. Thibeault, M. J. W. Rodwell, A. C. Gossard, "Selective Area Regrowth of Self-Aligned, Low-Resistance Ohmic Contacts on InGaAs." 28th North American MBE Conference, August 14-17, University of California, San Diego, La Jolla, CA.

J. J. M. Law, **Andrew D. Carter**, G. Burek, B. Thibeault, M. J. W. Rodwell, and A. C. Gossard, and "Selective Area Regrowth of Self-Aligned, Low Resistance Ohmic Contacts on InGaAs." Fall American Vacuum Society 58th International Symposium & Exhibition, Nashville, Tennessee.

David T. Martin, Sergio Sandoval, **Andy Carter**, Mark Rodwell, Stefan Smith, Andrew C. Kummel, and Davorka Messmer. "Fabrication of Silicon on Borosilicate Glass Microarrays for Quantitative Live Cell Imaging." 2011 MRS Spring Meeting.

Andrew D. Carter, J. J. M. Law, E. Lobisser, G. J. Burek, W. J. Mitchell, B. J. Thibeault, A. C. Gossard, and M. J. W. Rodwell "60 nm gate length Al_2O_3/ $In_{0.53}Ga_{0.47}As$ gate-first MOSFETs using InAs raised source- drain regrowth. Device Research Conference 2011, Santa Barbara, California.

Andrew D. Carter, Jeremy J. M. Law, William Mitchell, Gregory J. Burek, Brian J. Thibeault, Arthur C. Gossard, Mark. J. W. Rodwell. "Gate first $In_{0.53}Ga_{0.47}As/Al_2O_3$MOSFETs with in-situ channel surface cleaning." Electronic Materials Conference 2011.

Gregory Burek, **Andrew Carter**, Jeremy Law; Brian Thibeault, William Mitchell, Mark Rodwell. "Comparison of Metal Deposition Methods by CV Analysis of ALD Al_2O_3on $In_{0.53}Ga_{0.47}As$." Electronic Materials Conference 2011.

Seshadri Kolluri, David Brown, **Andrew Carter**, Stacia Keller, Steven DenBaars, Umesh Mishra. "Al_2O_3Based Etch-Stop Technology for the Gate Recess in N-Polar AlGaN/GaN MIS-HEMTs with Si_xN_yPassivation." Electronic Materials Conference 2011.

M. J. W. Rodwell, U. Singisetti, M.Wistey, G. J. Burek, **A. Carter**, A. Baraskar, J. Law, B. J. Thibeault, Eun Ji Kim, B. Shin, Yong-ju Lee, S. Steiger, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, E. Chagarov, A.C. Gossard, W. Frensley, A. Kummel, C. Palmstrm, Paul C McIntyre, T. Boykin, G. Klimek, P. Asbeck. "III-V MOSFETs: Scaling Laws, Scaling Limits, Fabrication Processes." IEEE 22nd International Conference on Indium Phosphide and Related Materials, May 2010.

M. J.W. Rodwell, **A. D. Carter**, G. J. Burek, M. A. Wistey, B. J. Thibeault, A. Baraskar, U. Singisetti, Byungha Shin, E. Kim, J. Cagnon, Y.-J. Lee, S. Stemmer, P. C. McIntyre, A. C. Gossard, C. Palmstrm, D. Wang, B. Yue, P. Asbeck, Y. Taur. "A Self-Aligned Epitaxial Regrowth Process for Sub-100-nm III-V FETs." 2010 MRS Spring Meeting, April 2010.

C. Liang, W. Buckhanan, **A. Carter**, P. Fay, M. Khan, D. Kopp, J. Kulick, Y. Lee, M. Padberg, R. Savino, G. Snider, and G. H. Bernstein, "Novel Packaging via Solder Joints at Chip Edges." IMAPS 2009, Scottsdale, AZ, March, 2009.

Bernstein, G.H., Brockman, J., Buckle, M., **Carter, A.**, Fay, P., Fuja, T., Gedde, N., Govea., S, Lewis, A., McWilliams, L.H., Meyers, K.L., Porod, W., Silliman, S.E., Suhendra, C., "Information and Nanotechnologies in an Introductory Engineering Course." 2006 ASEE Illinois-Indiana and North Central Conference, March 2006.

Abstract

Gate Last InGaAs MOSFETs with Regrown Source-Drain Regions and ALD Dielectrics

Andrew Carter

III-V-based MOSFETs have the potential to meet or exceed the performance of silicon-based MOSFETs due to their small electron effective mass. Modern Si-based MOSFETs with 22 nm gate lengths utilize high-k gate dielectrics and non-planar device geometries to optimize device performance. III-V HEMT technology has achieved similar gate lengths, but large source-drain access regions and the lack of high-quality gate insulators prevent further device performance scaling. Sub-22 nm gate length III-V MOSFETs require gate insulators with <1 nm effective oxide thickness, semiconductor-insulator interface trap densities less than 2×10^{12} cm^{-2} eV^{-1}, and metal-semiconductor contact resistivities less than 1 $\Omega\cdot\mu m^2$.

This dissertation presents InGaAs-based III-V MOSFET process flows and device results to assess their use in VLSI circuits. Previous III-V MOSFET results focused on long (>100 nm) gate lengths and ion implantation for source-drain region formation. Scaling III-V MOSFETs to shorter gate lengths requires source-drain regions that are: self-aligned to the channel, have low sheet resistance, have high mobile charge densities, and have low metal-semiconductor contact resistance. MBE- and MOCVD-based raised epitaxial source-drain regrowth meet these requirements. MBE InAs source-drain regrowth samples have shown 0.5 to 2 $\Omega\cdot\mu m^2$ metal-semiconductor contact resistivities. MOCVD source-drain regrowth samples have shown <100 $\Omega\cdot\mu m$ single-sided access resistance to InGaAs MOSFETs.

Gate insulators on III-V materials require wide bandgaps, high dielectric permittivities, and low insulator-semiconductor interface trap densities. *In-situ* hydrogen plasma / trimethylaluminum treatment prior to gate dielectric deposition was shown to lower MOSCAP interface trap densities by more than a factor of two.

Devices using gate first MBE regrowth, gate last MBE regrowth, and gate last MOCVD regrowth were fabricated and the resulting devices were characterized. 65 nm gate length gate first MBE regrowth devices employing a 2.2 nm EOT Al_2O_3 gate insulator show a peak transconductance of 0.3 mS/micron at 1 V V_{ds}. Gate-first FET performance scaling is limited by processing-induced damage and ungated access regions. 64 nm gate length gate last MBE regrowth devices employing a 1.21 nm EOT Al_2O_3/ HfO_2 bi-layer gate insulator show transconductance of 1.4 mS/micron at 0.5 V V_{ds}. Other gate last MBE samples had long channel subthreshold swings as low as 117 mV/dec. 48 nm gate length gate last MOCVD MOSFETs employing a 0.8 nm EOT HfO_2 gate insulator show peak transconductances of 2 mS/micron at 0.5 V_{ds}, with long channel devices having 97 mV/dec subthreshold swing. These results show strong promise for III-V MOS devices in future VLSI applications.

Professor Mark Rodwell
Dissertation Committee Chair

For Dale Carter

Contents

Figures

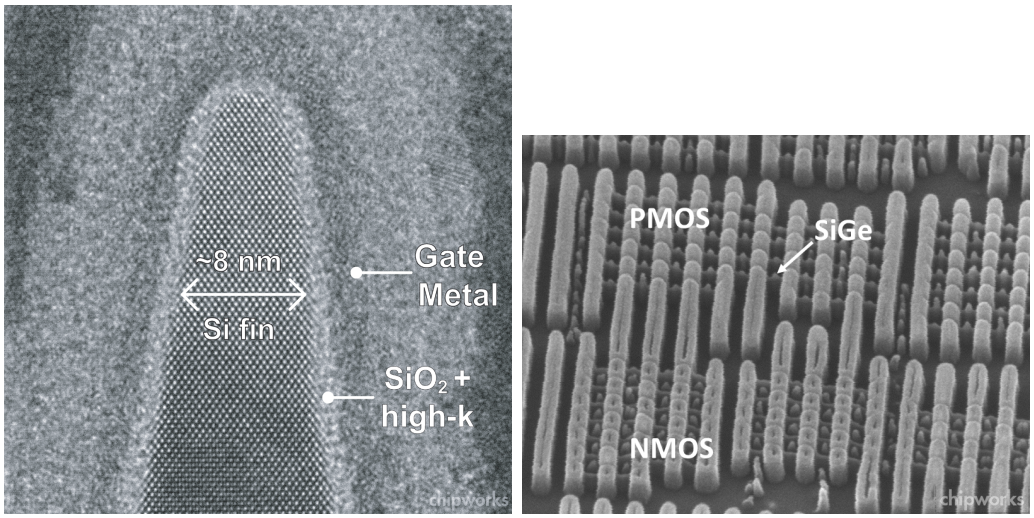
Tables

Chapter 1

Introduction

One of the most ubiquitous electronic technologies to date is the metal-oxide-semiconductor field effect transistor (MOSFET). Its success has been driven by silicon's ability to be electrically passivated with its native oxide, SiO_2. This oxide allows for induced mobile charge inside the semiconductor, a fundamental property of the MOSFET. In its development history, the gate length has scaled from multiple microns, to today, just a few nanometers. Along the way, key process advances had to be made, such as development of high-k dielectrics and metal gate electrodes. Modern silicon MOSFETs are now 22 nm gate-pitch spacing, and utilizing non-planar device geometries. Figure 1.1 shows a cross-section of an Intel NMOS FinFET, and a zoomed out perspective of a CMOS circuit in the same technology.

There are limits to silicon MOSFET scaling. As the gate insulator thickness decreases to improve gate-channel control, gate leakage currents rise exponentially, increasing the static power dissipation of the total circuit. High-k dielectrics relax the requirements on total gate insulator thickness, but Si MOSFETs require 0.4 to 0.6 nanometers of SiO_2, or suffer degraded channel mobilities and hence overall device performance. Silicon's electron effective mass along the direction of current propagation is 0.2 m_0; in the ballistic FET limit, this mass will limit maximum



(a) TEM cross-section, NMOS FinFET (b) Tilted SEM landscape, CMOS circuit

Figure 1.1: Images of Intel 22-nm FinFET devices [1],[2].

current density, and hence overall device performance.

III-V-based materials, such as GaAs, InGaAs, and InP, have been studied extensively for semiconductor devices. Their small effective masses, on the order of one quarter or less than that of silicon, allow for higher device current densities. InGaAs HEMTs using InAlAs gate insulators are useful field effect devices, but the gate insulator's small conduction band offset can cause large gate leakage currents. III-V devices are missing an electrically passivating, wide bandgap native oxide, to enable scaled VLSI devices in the material system.

Given the prospects of limited silicon CMOS scaling, research has recently turned towards highly scaled III-V MOSFETs to obtain performance better than that of silicon. Major goals include a heterogeneous, passivating wide band gap insulator; shallow, heavily doped, source/drain formation technology; and ultra low metal-semiconductor contacts. In this dissertation, an overview of MOS devices, process modules for III-V MOSFET fabrication, and results from two process flows will be

covered.

Chapter 2 (MOS Theory) examines the semiconductor device theory of a MOSFET. It examines long channel models, short channel behavior, and the ballistic FET model, and outlines the key concepts for field effect device scaling and optimization of performance.

Chapter 3 (Gate Insulator Development) examines gate insulator development using atomic layer deposition (ALD). A new *in-situ* surface treatment using trimethylaluminum and hydrogen plasma can reduce the interface trap density on InGaAs. MOS capacitor data analysis extracts interface trap density as a function of electron band energy.

Chapter 4 (Source/Drain Regrowth Development) examines source/drain regrowth development for the III-V MOSFET. Regrowth was pursued using both molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). MBE-grown relaxed InAs on InGaAs provides low metal-semiconductor access resistances, while MOCVD-grown lattice-matched InGaAs on InGaAs provides a defect-free source-drain region to III-V MOSFETs.

Chapter 5 (Gate First Process Flow and Results) outlines the UCSB gate first process flow and subsequent scaling to 65 nm gate lengths. Strengths and weakness are analyzed in terms of FET figures of merit, such as peak current density, transconductance, and off-state performance.

Chapter 6 (Gate Last Process Flow and Results) outlines the UCSB gate last process flow. Comparisons between gate first and gate last processes are made, showing how a gate last process is more amenable to device scaling. A variety of experiments were done to analyze MOSFET behavior with varied channel thickness, delta doping concentration, and surface preparation. Both MBE and MOCVD

source/drain regrown devices are analyzed. 48 nm gate length devices using digital channel etching (≈6.5 nm channel thickness) show peak transconductance of 2 mS/micron and drain currents in excess of 1 mA/micron. Further channel thickness reduction or removal of back barrier delta doping degrades device performance, while improving short channel effects. CV-extracted mobility data suggests mobility reduction in thin InGaAs quantum wells is the source of device performance degradation.

Chapter 7 (Conclusions) concludes the dissertation by summarizing the device results, discussing areas for improvement, and looks forward to future process flows, devices, and paths for continued MOS scaling.

References

[1] Chipworks. Intel's 22-nm Tri-gate Transistors Exposed, May 2013.

[2] Chipworks. Plenty of room at the bottom? Intel thinks so!, May 2013.

Chapter 2

MOSFET Theory

2.1 Introduction

MOSFET device physics has been treated extensively in the literature since silicon-based structures were first fabricated [1]. Proper physical understanding of how MOSFETs work is critical to engineering new devices and improving their performance. This chapter focuses on MOSFET device physics, with special considerations for III-V-based MOSFETs, short channel effects in MOSFETs, and scaling MOSFET dimensions and material parameters for improved performance.

2.2 MOSFET Long Channel Theory

Figure 2.1 is a cross-section cartoon of a generic MOSFET. A MOSFET has four terminals: gate, source, drain, and body. A MOSFET works on the principle of the field effect [2]; charges on the gate induce opposite charges in the material, which alters the material conductivity. This induced charge layer can be quite thin, leading to high sheet carrier densities (cm^{-2}). The source and drain regions contact this conductive layer. Depending on the voltage conditions of the gate,

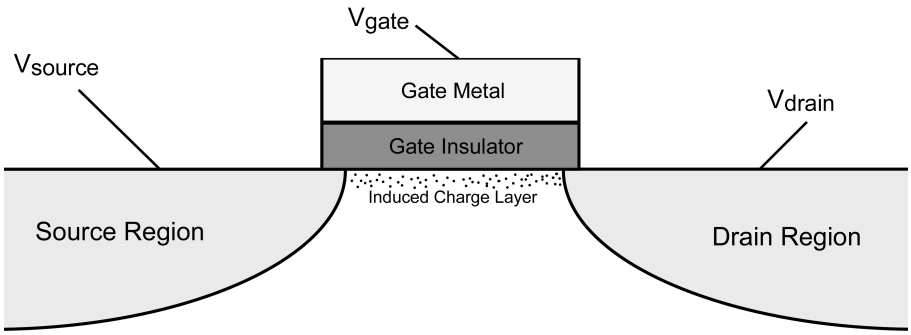


Figure 2.1: Cartoon of generic MOSFET.

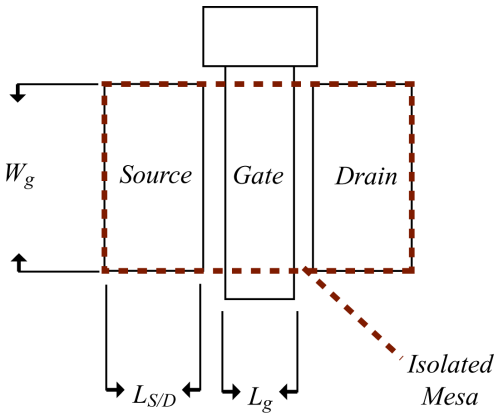


Figure 2.2: Top-down schematic of a MOSFET.

source, and drain, the current-voltage relationship between the drain and source can be an open circuit, resistive (linear I-V), constant current (current source), or exponential (thermionic emission). The body contact is typically connected to the source terminal.

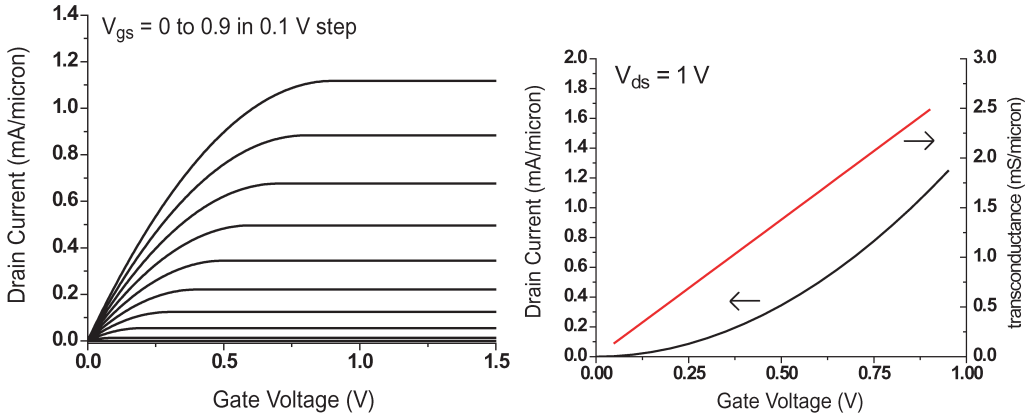
Here are equations for the I-V relationship of the long-channel (i.e. long gate length) MOSFET [3],[4],[5]:

$$\frac{I_{linear}}{W} = \frac{1}{L}\mu C_{g-ch}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad V_{ds} \leq V_{ds,sat}, V_{gs} \geq V_{th} \tag{2.2.1}$$

$$\frac{I_{saturated}}{W} = \frac{1}{L}\mu C_{g-th}\left[\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds,sat}\right] \qquad V_{ds} \geq V_{ds,sat}, V_{gs} \geq V_{th} \tag{2.2.2}$$

$$V_{ds,sat} = V_{gs} - V_{th} \tag{2.2.3}$$

where W is the gate width, L is the gate length, C_{g-th} is the gate-channel capacitance, and V_{th} is the device threshold or turn-on voltage. C_{g-th} represents the capacitive coupling between charges on the gate metal and inside the semiconductor. See Section 2.4 for further analysis. The electron mobility, μ, is the relationship between electric field and electron velocity inside the semiconductor: $v_{electron} = \mu E$, where E is the electric field inside the semiconductor along the direction of current flow. Figure 2.3 illustrates the current-voltage relationship of the transistor. While $V_{ds} \ll V_{gs}$-V_{th}, the device behaves like a resistor. Varying the gate voltage varies the induced charge in the channel, and hence the resistance of the channel. As



(a) J_{drain}-V_{ds} (b) J_{drain}-V_{gs}

Figure 2.3: Long Channel FET Model: J_{drain}-V_{ds} and J_{drain}-V_{gs}

V_{ds} approaches V_{gs}-V_{th}, the current increases more slowly with V_{ds}. This is due to depletion region formation near the drain contact, "pinching off" the conductive channel. After $V_{ds} \geq V_{gs}$-V_{th}, the channel is fully pinched off and all additional voltage V_{ds} is dropped in the depletion region near the drain. At this point the FET behaves like a current source across the drain-source contacts. The threshold voltage is the gate voltage required to induce a charge density large enough to create a conductive channel. Threshold voltage is typically defined as the V_{gs} necessary to have a specific drain current density (e.g. $1\mu A/\mu m$)at a fixed V_{ds}.

Figure 2.3b illustrates the case where the device has been biased into current saturation ($V_{ds} \geq V_{gs}$-V_{th}). From Eqn. 2.2.3 J_{drain}-V_{gs} has a quadratic relationship. The DC transconductance gain of the device, $\frac{dJ_{drain}}{dV_{gs}}$, is therefore linear. It should be noted that in this model the device transconductance increases without bound.

When the device is turned "off," i.e. V_{gs}<V_{th}, a significant amount of induced charge is not present due to a potential barrier between the source and drain. J_{drain} is now thermionically limited:

$$\frac{I_{ds,off}}{W} \approx I_0 \exp \frac{q(V_{gs} - V_{th})}{mk_BT} \tag{2.2.4}$$

where I_0 represents a "dark current" for this barrier-limited device, k_B is Boltzmann's constant, T is the device temperature, and m represents the gate's control on the channel semiconductor barrier. A typical figure of merit for MOSFET off-state performance is the subthreshold swing. This represents the amount of gate voltage required to reduce the subthreshold current by one order of magnitude, typically written in mV/dec. Including interface trap density, the subthreshold swing is [6]:

$$SS = ln(10)\frac{k_BT}{q}\left(\frac{C_{ox} + C_{it}}{C_{ox}}\right) \tag{2.2.5}$$

where C_{it} is the gate insulator-semiconductor interface trap density. Interface traps are electron states that trap electrons or holes, inhibiting channel conduction. They are typically dangling bonds at the insulator - semiconductor interface, but can be located inside the gate insulator, or inside the semiconductor as well. In terms of energy, they are typically within the band gap of the semiconductor, but can be above (below) the conduction (valence) band edges as well. Since interface traps are electrically active, they must be charged and discharged in parallel with the device channel. For device bias above threshold, this reduces the gate's capacitive effect on the channel, reducing current density at a given gate bias above threshold. For device bias into the subthreshold regime, the same effect will increase subthreshold swing.

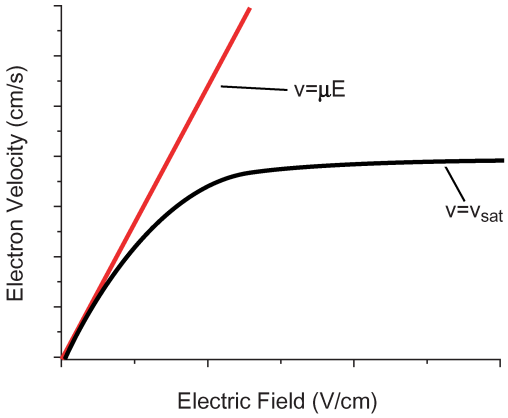


Figure 2.4: Semiconductor electron velocity versus electric field.

2.3 MOSFET Short Channel Theory

MOSFET long-channel theory does not accurately predict on-state device behavior as the gate length is decreased. As the applied gate bias increases, vertical electric fields present in the channel decrease the mobility of the electrons in the channel, due to increased surface scattering. As the transistor gate length decreases, the horizontal electric fields increase to a point where the electron velocity is no longer linearly dependent on electric field (Figure 2.4). As previously stated, semiconductor mobility is the linear response of electron velocity to electric field. Taken to a limit, this suggests an electron can have an infinite velocity inside the semicondcutor. In reality, once the electric field approaches a critical field strength, electrons will dissipate their kinetic energy in the form of phonons into the semiconductor crystal. This dissipation will slow the electron down; as the field increases, the scattering increases, and the electron will reach a velocity limit, typically called the saturation velocity.

In the case of a semiconductor MOSFET, a small enough gate length will allow a moderate drain-source bias to reach the critical field strength, and hence the

mobility approximation is no longer valid. The electron velocity in the device is no higher than v_{sat}, and now, rather than having an electrostatic pinch-off point, the transistor is limited by electron velocity. A new model can be derived similar to the long-channel model [3], but allowing mobility to change as a function of drain-source field:

$$\mu = \frac{\mu_{lf}}{1 + \frac{\mu_{lf} E_{ds}}{v_{sat}}} \tag{2.3.1}$$

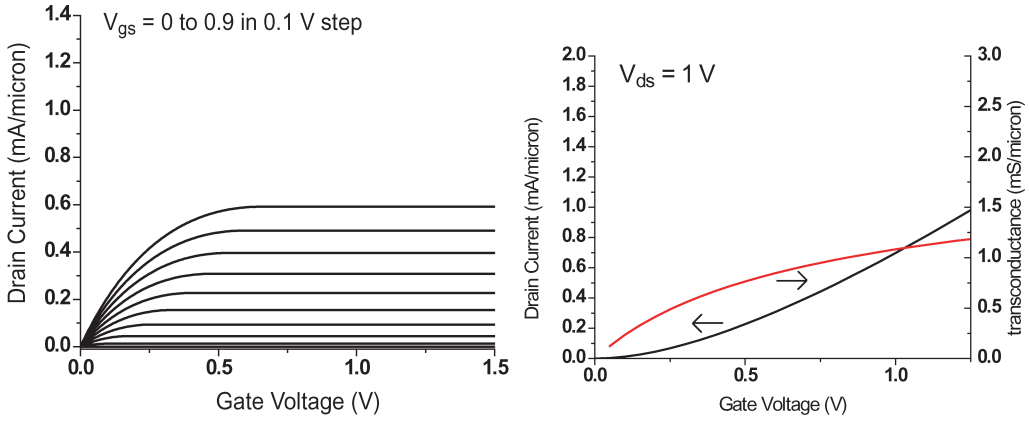
where μ_{lf} is the "low field" mobility, a linear approximation of the electron velocity-field curve for electric fields $\ll E_{critical}$; and E_{ds} is the drain-source field. The transistor's current-voltage behavior is now:

$$\frac{I_{linear}}{W} = \frac{1}{L + \frac{\mu_{lf} V_{ds}}{v_{sat}}} \mu_{lf} C_{g-ch} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \qquad V_{ds} \leq V_{ds,sat}, V_{gs} \geq V_{th} \tag{2.3.2}$$

$$\frac{I_{saturated}}{W} = \frac{1}{L + \frac{\mu_{lf} V_{ds,sat}}{v_{sat}}} \mu_{lf} C_{g-th} \left[\left(V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) V_{ds,sat} \right] \quad V_{ds} \geq V_{ds,sat}, V_{gs} \geq V_{th} \tag{2.3.3}$$

$$V_{ds,sat} = L \frac{v_{sat}}{\mu_{lf}} \left[\left(1 + \frac{2\mu_{lf} (V_{gs} - V_{th})}{v_{sat} L} \right)^{\frac{1}{2}} - 1 \right] \tag{2.3.4}$$

Compare Figures 2.3 and 2.5. For the same applied gate bias, the saturated drain current density is lower. This is due to electron velocity saturation in the channel. The FET makes the transition from the resistive to current saturation region with a smaller V_{ds} for the same reason. Combining Eqns. 2.3.3 and 2.3.3:



(a) J_{drain}-V_{ds} (b) J_{drain}-V_{gs}

Figure 2.5: Short channel FET Model: J_{drain}-V_{ds} and J_{drain}-V_{gs}

$$\frac{I_{saturated}}{W} = C_{g-th} v_{sat} \left(V_{gs} - V_{th} - V_{ds,sat}\right) \tag{2.3.5}$$

and taking a derivative with respect to V_{gs}:

$$\frac{dI_{saturated}}{dV_{gs}} = WC_{g-ch} v_{sat} - \frac{WC_{g-th} v_{sat}}{\sqrt{1 + \frac{2\mu_{lf}(V_{gs}-V_{th})}{v_{sat}L}}} \tag{2.3.6}$$

Comparing 2.3b and 2.5b, the transconductance no longer increases linearly with gate bias; it begins to turn over due to velocity saturation in the channel. As gate length decreases and/or the channel mobility increases, the second term in equation 2.3.6 decreases; the electron is now traveling for most of the channel length at v_{sat}. In the limiting case where the mobility tends to infinity or the gate length tends to zero, $g_m = WC_{g-ch} v_{sat}$.

2.4 MOSFET Gate-Channel Control

Gate control of the channel charge density is a fundamental parameter for a MOSFET. This section reviews the components that compromise C_{g-ch}.

In transistor current-voltage equations, the C_{g-ch} term represents the gate control of the semiconductor channel charge density. Terms are of the form dQ/dE, the derivative of charge density with respect to Fermi level energy. This derivative can be converted into a capacitance with the equation $C = q(dQ/dE) = dQ/dV$, allowing C_{g-ch} to be intuitively understood.

The gate insulator capacitance is:

$$C_{ox} = \frac{\epsilon_{ins}}{T_{ins}} \tag{2.4.1}$$

where ϵ_{ins} is the relative permittivity of the insulator multiplied by the vacuum permittivity, ϵ_0, and T_{ins} is the oxide physical thickness. When comparing the relative capacitances of various insulators, it is helpful to normalize all oxides to silicon dioxide; therefore, an effective oxide thickness (EOT), can be defined:

$$EOT = \frac{T_{ins}\epsilon_{sio_2}}{\epsilon_{ins}} \tag{2.4.2}$$

where $\epsilon_{sio_2} = 3.9\epsilon_0$.

Due to the high charge densities seen in MOSFET channels, significant semiconductor band bending occurs, and this charge confinement quantizes the semiconductor bands at the surface. The lowest energy of the electron is no longer the semiconductor band edge, but a quantum eigenstate. The eigenstate energy is determined by the electron effective mass perpendicular to current flow, i.e. along the

gate-insulator-channel axis. For the case of an infinite quantum well [7, pp. 44], eigenstate energy is:

$$E_n = \frac{n^2\pi^2\hbar^2}{2m_l^* a^2} \tag{2.4.3}$$

where n is the specific eigenstate, $\hbar$ is the reduced Planck constant, m_l^* is the electron effective mass perpendicular to current flow, and a is the well thickness. Therefore, as confinement increases, the heavy effective mass for silicon keeps the eigenstate energy increase minimal, while for InGaAs the increase is significant.

Due to electron confinement, the electron quantum mechanical wavefunction must be considered when calculating the position of the centroid of the charge density. Using a self-consistent Schrödinger-Poisson solver, one can obtain accurate simulations of the bound state wavefunction. There is an effective capacitance associated with the setback of the charge density from the surface, called C_{depth}. Rigorously, this is the change in charge density centroid due to the change in surface potential, requiring self-consistent simulation for an accurate result. An approximation for thin quantum wells (less than 10 nm for InGaAs):

$$C_{depth} \approx \frac{\epsilon_{semi}}{\frac{T_{well}}{2}} \tag{2.4.4}$$

where ϵ_{semi} is the relative permittivity of the insulator multiplied by the vacuum permittivity, and T_{well} is the thickness of the quantum well. Clearly, C_{depth} will change with applied bias, and this approximation should only be used as an intuitive guide.

The charge density in the channel is the integration of the semiconductor density of states and the Fermi-Dirac distribution function. Due to quantization, the two-

dimensional density of states is used:

$$D_{2D} = \frac{m_t^*}{\pi\hbar^2} \tag{2.4.5}$$

where m_t^* is the electron effective mass along the direction of current flow. For silicon MOSFETs, $m_t^* \sim 0.19m_0$, and for InGaAs, $m_t^* \sim 0.04m_0$. n_{sheet} is:

$$n_{sheet} = N_{2D}F_0 = N_{2D}ln\left(1 + \exp\frac{E_f - E_1}{k_BT}\right) \tag{2.4.6}$$

where $N_{2D} = (D_{2D})k_BT$, E_f is the channel Fermi level, and E_1 is the energy of eigenstate(s) participating in conduction. N_{2D} comes from the use of Fermi-Dirac integrals [8] to solve the integral.

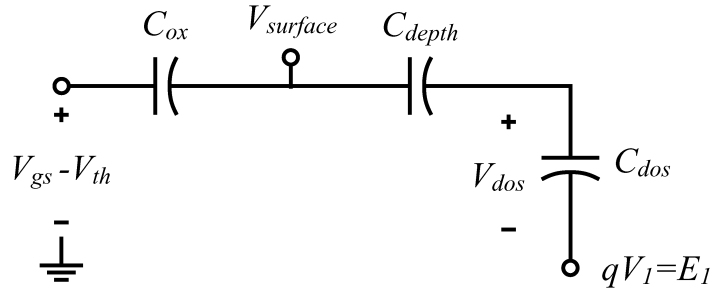
To find an equivalent capacitance, one first takes a derivative of 2.4.6 with respect to E_f:

$$C_{dos} = q\frac{d(n_{sheet})}{dE_f} = \frac{qN_{2D}\exp\frac{E_f}{k_BT}}{k_BT\left(\exp\frac{E_f}{k_BT} + \exp\frac{E_1}{k_BT}\right)} \tag{2.4.7}$$

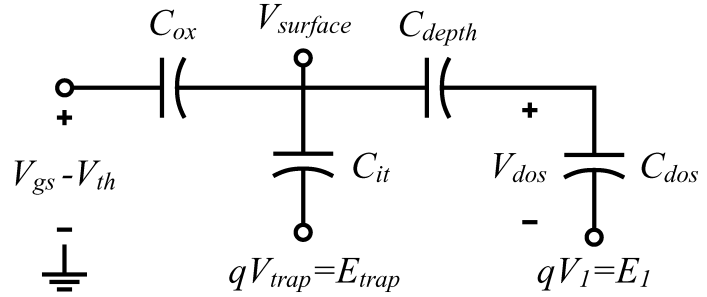
Multiplying top and bottom by $\exp\frac{-E_f}{k_BT}$ gives,

$$C_{dos} = \frac{qN_{2D}}{k_BT\left(1 + \exp\frac{E_1 - E_f}{k_BT}\right)} = \frac{q^2D_{2D}}{\left(1 + \exp\frac{E_1 - E_f}{k_BT}\right)} \tag{2.4.8}$$

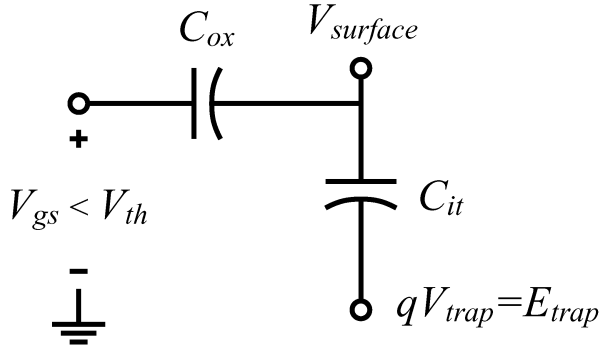
See Figure 2.6a. If multiple eigenstates are occupied, then the capacitance network changes bysimple addition of C_{depth} and C_{dos} terms. Ideally, the semiconductor-insulator interface is free of electrically active traps; in III-V materials, the trap density can be significant, on the order of C_{dos} or greater. The occupation of these traps is defined by the difference in surface Fermi energy and the energy trap level,



(a) Network without interface traps



(b) Network with interface traps



(c) Network with interface traps, V_{gs} <V_{th}

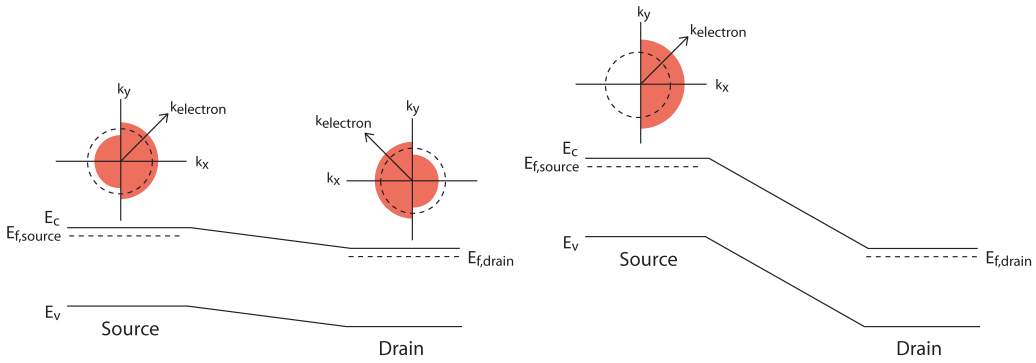
Figure 2.6: Capacitance equivalent network for C_{g-ch}

(E_f-E_{trap}). In Figure 2.6b, an interface trap term is added, $C_{it} = q^2 D_{it}$. The interface trap capacitance tends to lower the surface Fermi energy, taking away induced mobile channel charge. The C_{it} used is not necessarily the one derived from subthreshold swing measurements, since the interface trap densities can vary with energy. Finally, Figure 2.6c shows that for subthreshold bias, $C_{dos} \ll C_{ox}$ and the subthreshold swing is controlled by the gate insulator capacitance and interface trap density, as defined in Eqn. 2.2.5.

2.5 MOSFET Ballistic Transport Theory

In the previous sections, the mobility term plays a dominant role in dictating device performance. Mobility in a semiconductor can be defined as $\mu = q\tau/m^*$, where , where q is the Coulomb charge, m^* is effective mass, and τ is the mean scattering time for the electron. Assuming an average velocity $\bar{v}_{electron}$, an electron should travel a distance $\tau\bar{v}_{electron}$ before scattering. Thus, it is of interest to explore device behavior at gate lengths of this order. Approximations for this distance can come from using the bulk low-field mobility and the saturation velocity of the semiconductor; however, simplifying assumptions were taken to create those terms (e.g., non-degenerate carrier statistics, unconfined carriers). Instead, starting with the assumption that there is no electron scattering in the channel, one can derive a "ballistic" model of an FET [9],[5],[10].

Figure 2.7 shows electron band diagrams of a ballistic FET channel at low and high V_{ds} bias. The two circles represent the electron k-states in k_x and k_y, the k-states in the direction of current flow. k_x is along the gate length, and k_y is along the gate width. Given no channel scattering, the source right-going k-states fill the drain



(a) V_{gs}>V_{th}, low V_{ds} (b) V_{gs}>V_{th}, high V_{ds}

Figure 2.7: Ballistic FET electron band diagrams along the source-channel-drain region

right-going k-states, and similarly for the drain electrons into the source. As drain-source bias is applied, the source Fermi half-circle loses its negative k momentum electrons, since they came from the drain and are now blocked by applied bias.

At high V_{ds} bias, only the right-going source electrons contribute to channel current:

$$J_{source} = q\ n_{source}(E_f - E_1)v_{source}(E_f - E_1) \tag{2.5.1}$$

where n_{source} is the sheet carrier density, a function of $E_f - E_1$, the difference in electron Fermi energy and the occupied eigenstate energy, and v_{source} is the velocity of the electrons. The electron density can be calculated, similar to Eqn 2.4.6:

$$n_{source} = \frac{N_{2D}}{2}F_0 = \frac{N_{2D}}{2}ln\left(1 + \exp\frac{E_f - E_1}{k_B T}\right) \tag{2.5.2}$$

where F_0 is the Fermi-Dirac integral of order zero. This time the density of states term is divided by two because only the right-going k-states participate in the

channel current. The electron velocities are calculated using the directed moment:

$$v_{source} = \frac{\sum_{k_x>0,k_y} v_x f_0(E_f - E_1)}{\sum_{k_x>0,k_y} f_0(E_f - E_1)} \tag{2.5.3}$$

where $v_x = \frac{\hbar k_x}{m_t^*}$ is x-directed component of each k-state, and f_0 is the Fermi-Dirac occupancy function. Assuming a continuum of states where Δ k_x,Δ k_y is small compared to the device dimensions, summations become integrals and the moment can be evaluated analytically. For devices biased such that $E_f \gg E_1$, the degenerate (0K) approximation can be applied. Assuming parabolic semiconductor bands, in k-space the equations are:

$$E_f - E_1 = \frac{\hbar^2 k^2}{2m_t^*} \tag{2.5.4}$$

$$n_{source,degen} = \frac{D_{2D}}{2}\frac{\hbar^2 k_f^2}{2m_t^*} = \frac{k_f^2}{4\pi} \tag{2.5.5}$$

The velocity of the carriers at the Fermi level is $v_f = \hbar k_f / m_t^*$. Not all carriers participating in the current density have this velocity, since not all are at E_f. The mean velocity of the carrier density is the centroid of occupied k-space:

$$v_{source,degen} = \frac{4}{3\pi} v_f = \frac{4}{3\pi}\frac{\hbar k_f}{m_t^*} \tag{2.5.6}$$

Combining Eqns. 2.5.1, 2.5.4, and 2.5.6, and converting back into energy space:

$$J_{source,degen} = \frac{2q\sqrt{2m_t^*}}{3\pi^2\hbar^2}\left(E_f - E_1\right)^{\frac{3}{2}} \tag{2.5.7}$$

E_f is the Fermi level in the channel; it is related to the gate voltage by the capacitive voltage divider described in Section 2.4. Continuing to assume the degenerate approximation and assuming no interface traps are present: $C_{g-ch} = (1/C_{ox} + 1/C_{depth} + 1/C_{dos})^{-1}$. The "voltage" across the density of states capacitance as a function of gate voltage is then:

$$V_{dos} = \frac{C_{g-ch}}{C_{dos}}(V_g - V_{th}) \tag{2.5.8}$$

A transconductance can be defined by taking the derivative of Eqn. 2.5.7 with respect to the E_f:

$$g_{m,source} = \frac{q\sqrt{2m_t^*}}{\pi^2\hbar^2}\left(E_f - E_1\right)^{\frac{1}{2}} \tag{2.5.9}$$

Recapitulating the above mathematics: in ballistic FETs, the electrons from the source traverse a scatter-free channel. In the degenerate limit, the ballistic FET current density is proportional to the 3/2 power of E_f - E_1, and transconductance is proportional to the square root of E_f - E_1. Eqn 2.5.7 is also independent of V_{ds}; ballistic FETs have current saturation behavior similar to the long and short channel device models.

In the ballistic limit, there is a trade-off between a low and high density of states [10]. Too few states means high-velocity carriers are in the channel, but there are too few of them. Too many states mean many carriers, but since the Fermi level cannot be much above the eigenstate, the carriers do not have much velocity, and therefore cannot have high current densities.

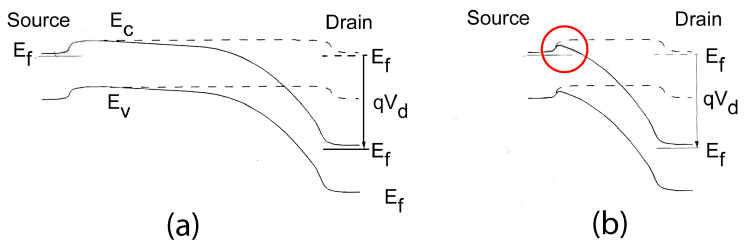


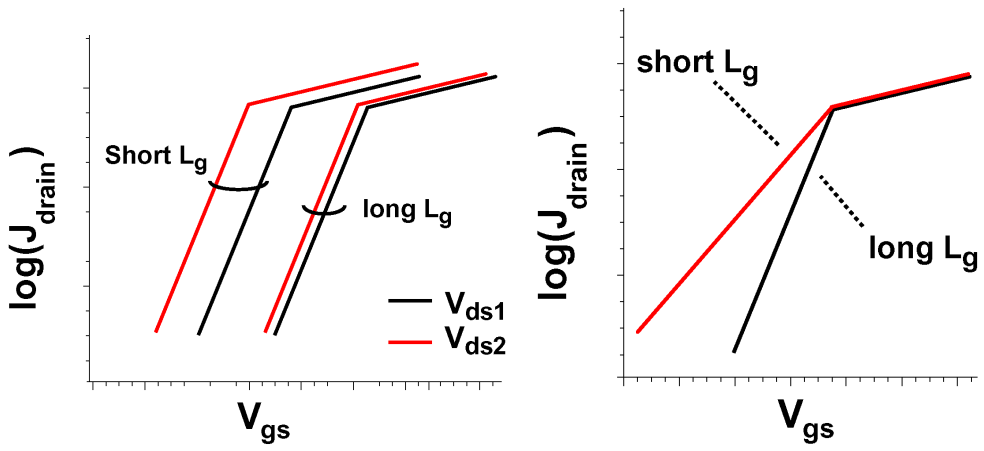
Figure 2.8: Electron band diagram along the source-channel-drain axis for a)long gate length device, and b) short gate length device. Adapted from [6].

2.6 MOSFET Short Channel Effects

A MOSFET is inherently a two-dimensional device. The equations used thus far have assumed one-dimensional electrostatics are dominant in device operation. As the gate length scales down, more of the channel is capacitively coupled to drain. Further scaling leaves the gate without control of the channel, and drain electric fields control device performance.

As seen in Figure 2.8, the drain electric fields begin to influence the channel charge and the source directly; this is called "drain induced barrier lowering," or DIBL [11]. It is the root cause of many short channel effects, including: threshold voltage rolloff, subthreshold swing increase, and output conductance modulation.

Threshold voltage rolloff occurs due to the drain electric field "pulling down" the source-channel barrier. As the drain voltage increases, it capacitively lowers the barrier, allowing more carriers into the channel, effectively lowering the threshold voltage. This is illustrated in the I-V curves of Figure 2.9a. This is characterized in MOSFETs by subtracting the threshold voltage of two different V_{ds} biases on the same FET. DIBL is typically specified in mV (change V_{th}) per V (change V_{ds}). Similarly, the subthreshold swing increases due to stronger drain-channel coupling than gate-channel coupling, preventing proper subthreshold gate modulation (Fig-



(a) DIBL increase with L_g decrease

(b) Subthreshold swing increase with L_g decrease

Figure 2.9: log J_{drain}-$V_{gs}$for long and short gate lengths, DIBL and subthreshold swing behavior

ure 2.9b).

As V_{ds} increases beyond saturation, the electrostatic pinch-off region in the device absorbs this voltage drop. This region can increase in length, pushing the pinch off point towards the source, effectively decreasing the gate length. For long-channel devices, this is effect is small, but for devices where this decrease is a large fraction of the overall gate length, the output conductance of the device increases, essentially placing a resistor in parallel with the transistor.

Intuitively, to prevent short channel effects, one must ensure the gate metal has stronger capacitive control over the channel than the drain. In light of this, Brews *et al* [12] published an empirical formula for minimum gate lengths in inversion-mode MOSFETs. Gate lengths smaller than the minimum would tend to suffer short channel effects. For inversion-mode n-channel MOSFETs, the bulk semiconductor is p-type, and the surface is inverted to form a conducting n-type channel. In general, planar inversion mode MOSFETs are electrostatically improved by increasing

substrate p-doping to better confine carriers and prevent drain field penetration. However, there is a limit to this doping. Too much p-doping will add another term to the subthreshold swing equation:

$$SS = ln(10)\frac{k_B T}{q}\left(\frac{C_{ox} + C_{it} + C_{dep}}{C_{ox}}\right) \tag{2.6.1}$$

where C_{dep} is the depletion region capacitance from the p-doped substrate. As the doping increases, C_{dep} increases since the depletion width will decrease. Since the p-doping is typically tied to the source, it affects the channel potential barrier. This capacitance acts similarly to interface traps in that it prevents the gate from modulating the channel barrier effectively, increasing subthreshold swing.

Instead of increasing p-doping, a different method of electron confinement must be implemented. Heterobarriers are employed for HEMTs and the III-V MOSFETs described in this dissertation. The conduction band offset of the channel and back barrier effectively limits the accumulation charge layer thickness. Another way to improve confinement is to remove semiconductor from under the channel. This can be done using SOI [13], finFET geometry [14], or a nanowire [15]. These techniques have tradeoffs; the selection is based on specific application.

Scaling rules for these non-planar gating scenarios have been derived [16]. There is a simple "effective length" rule developed for silicon devices than can be applied to III-V devices with heterojunction back barriers:

$$\lambda_{SOI} = \sqrt{\frac{\epsilon_{r,chan}}{\epsilon_{r,ins}} T_{chan} T_{ins}} \tag{2.6.2}$$

$$\lambda_{DG} = \sqrt{\frac{\epsilon_{r,chan}}{2\epsilon_{r,ins}} T_{chan} T_{ins}} \tag{2.6.3}$$

where $\epsilon_{r,chan}$ is the channel relative permittivity, $\epsilon_{r,ins}$ is the gate insulator relative permittivity, T_{chan} is the channel thickness, and T_{ins} is the insulator thickness. λ_{SOI} is derived for the case of semiconductor-on-insulator, where gate metal is present on one side of the channel, while λ_{DG} is derived for gate metal on two sides of the channel. As the channel permittivity increases for the same C_{EOT}, the minimum channel length increases. Since InGaAs $\epsilon_{r,semi}$ is larger than silicon $\epsilon_{r,semi}$, InGaAs channels will suffer increased short channel effects as the gate length is decreased. For deep sub-micron SOI, the source-drain separation will decrease, and for thick bottom insulators, their fields will terminate in the channel [17]. This will lead to poor short channel behavior, and require the bottom insulator be thinned to bring a ground plane closer to the drain for field termination. A semiconductor bottom barrier will have a larger permittivity than SiO_2, and therefore this effect is increased proportionally. Rigorous semiconductor transport simulations [18] have shown III-V-based MOSFET electrostatics do not scale as well as silicon; multi-gate solutions are required.

2.7 MOSFET Scaling Laws

While MOSFET device behavior is important to understand, how it relates to intended application is also important. This section examines important behavior for MOSFETs in VLSI and scaling laws for improving their performance.

In a digital circuit such as a VLSI microprocessor, MOSFETs are integrated in such a way to make Boolean logic gates [19]. CMOS circuits pair NMOS and PMOS FETs to minimize static power dissipation in the circuit. The most basic switching element is the inverter (Figure 2.10). This circuit drives a capacitor C_{out}, which

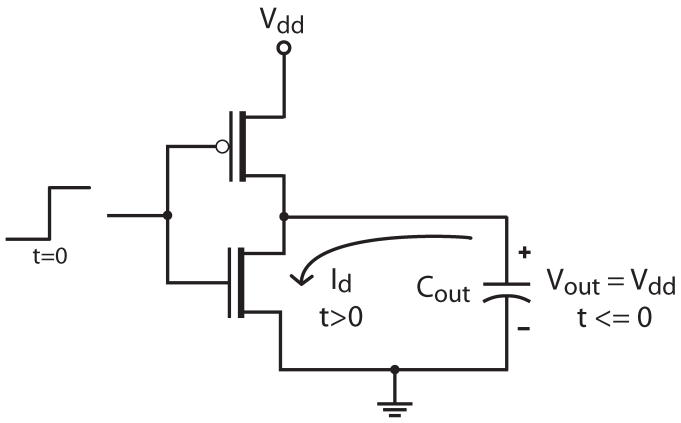


Figure 2.10: CMOS inverter schematic with load capacitor.

could be another logic gate or a long interconnect wire. This capacitor is charged with voltage V_{dd}. The NFET gate bias is zero. When the NFET gate is turned on at t=0, the NFET is biased into saturation, and has current source behavior. The current flowing, $I_{d,sat}$, removes charge from C_{out}. As long as the voltage across C_{out} maintains current saturation, the capacitor voltage will decrease linearly. The time constant for dissipating the energy from the capacitor is approximated as:

$$\tau \approx \frac{C_{out} V_{dd}}{I_{d,sat}} \tag{2.7.1}$$

Therefore, in general, VLSI switches will operate faster if load capacitance is small, rail voltage is small, or saturated drive currents are high.

While the transistors themselves are analog, in the "digital" limit the ability to drive the output capacitance is limited by the circuit rail voltage and the saturated drive current available to the device. If the switches are closely spaced, wiring delays will be small compared to device resistances and capacitances, and they will define C_{out}. Similarly, if switches are far apart, wiring delays will dominate C_{out}. MOSFETs require high transconductance at gate bias between V_{th} and V_{rail} to

have high saturated current densities and therefore fast switching behavior.

Minimizing total power consumption is important for VLSI devices. While the CMOS circuit topology minimizes static power dissipation, leakage currents can become a significant percentage of standby power dissipation. For a given device threshold voltage and subthreshold swing, one can calculate the off-state current. Threshold voltages can be taken at fixed device currents (e.g. 1μA/micron), and subthreshold swing dictates device leakage at zero bias. Lowering the threshold voltage for a fixed subthreshold swing will increase off-state current, increasing standby power consumption.

Given the information outlined in the previous sections, device researchers created a set of scaling laws by which MOSFET circuits could be improved while maintaining device reliability and low power dissipation. There are two main types of scaling: constant field scaling, and constant voltage scaling [4], and both are based on the classic planar silicon MOSFET. Both increase device density by shrinking device area.

Constant field scaling aims to maintain the absolute field (V/m) inside the device [20]. This ensures short channel effects will not increase with each scaling node. It also improves device reliability, since high-field effects (such as impact ionization and hot electron degradation) decrease total circuit life. Since electric field must stay constant, rail voltages must decrease by a factor of two. Inversion charge density stays constant since both oxide thickness and gate voltage are decreasing by a factor of two. Since absolute power and current both scale by two, power dissipation decreases by four, and since the circuit density also scales by four, we maintain power density between each scaling generation. This ensures circuit power can be dissipated without exotic cooling techniques. Time delays will scale by a

factor of two.

Constant voltage scaling aims to maintain the applied biases while scaling the device geometry. This is necessary since multiple factors inside the transistor are not scalable within a technology, e.g. semiconductor bandgap and thermal voltage. Unlike constant field scaling, inversion charge density will increase since channel capacitance will increase, but voltage will stay constant. Constant voltage scaling also decreases time delays by a factor of two, but sacrifices power dissipation; it will increase by a factor of two, requiring better cooling technology with each node.

Industrial VLSI production has implemented both constant field and constant voltage scaling simultaneously; both scaling paradigms can be combined in "generalized scaling" [21]. Depending on the most pressing problem at a given node, a balance must be struck between device performance and total power dissipation. Because gate leakage currents overwhelmed device performance earlier than expected on industry roadmaps, one of the most important advancements in recent CMOS development was the introduction of high-k dielectrics [22]. Switching to hafnium-based oxides and metal gates improves gate capacitance without thinning the oxide, limiting gate tunneling currents.

For ballistic FET scaling, to increase the drain current density by a factor of two at a constant V_{gs}-V_{th}, C_{g-ch} must increase by factor of two. In the absence of an interface traps, increasing C_{g-ch} requires increasing C_{ox}, C_{depth}, and C_{dos} all by a factor of two. C_{ox} increase requires increasing dielectric permittivity or decreasing thickness. These are limited by available materials and process tool maturity. C_{depth} increase requires thin channels to minimize the wavefunction distance from the surface. C_{dos} increase requires either more conducting semiconductor eigenstates or larger effective mass electrons. New semiconductor material orientations can

simultaneously increase the semiconductor density of states while maintaining an adequately low effective mass for high velocity electron conduction [10].

2.8 MOSFET: Conclusions

In this chapter, MOSFET theory, quantum mechanical effects, and transistor figures of merit have been outlined. In general, the best MOSFET must have strong capacitive control over the channel, and that channel must have a relatively large density of states to manipulate. This control must be stronger than the drain control on the channel. With optimized gate control, large current densities and transconductances are possible, which are key drivers for VLSI technology applications.

References

[1] Dawon Kahng. US Patent 3102230: ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE, 08 1963.

[2] Julius Edgar Lilienfeld. US Patent 1900018: Device for controlling electric current, 03 1933.

[3] BL Anderson and RL Anderson. *Fundamentals of Semiconductor Devices*. McGraw-Hill Companies, Inc, 2005.

[4] Yuan Taur and Tak H Ning. *Fundamentals of modern VLSI devices*. Cambridge University Press, 2009.

[5] Mark Lundstrom and Jing Guo. *Nanoscale transistors: Device physics, modeling and simulation*. Springer New York, 2006.

[6] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. Wiley-interscience, 2006.

[7] David J Griffiths. *Introduction to quantum mechanics*. Pearson, 2007.

[8] Raseong Kim and Mark Lundstrom. Notes on fermi-dirac integrals. *arXiv preprint arXiv:0811.0116*, 2008.

[9] Kenji Natori. Ballistic metal-oxide-semiconductor field effect transistor. *Journal of Applied Physics*, 76(8):4879–4890, 1994.

[10] Mark Rodwell, W Frensley, S Steiger, E Chagarov, S Lee, H Ryu, Y Tan, G Hegde, L Wang, J Law, et al. III–V FET channel designs for high current densities and thin inversion layers. In *Device Research Conference (DRC), 2010*, pages 149–152. IEEE, 2010.

[11] Ronald R Troutman. VLSI limitations from drain-induced barrier lowering. *Solid-State Circuits, IEEE Journal of*, 14(2):383–391, 1979.

[12] JR Brews, W Fichtner, EH Nicollian, and SM Sze. Generalized guide for MOSFET miniaturization. *Electron Device Letters, IEEE*, 1(1):2–4, 1980.

[13] Chenming u. SOI (Silicon-on-Insulator) for High Speed Ultra Large Scale Integration. *Japanese Journal of Applied Physics*, 33:365–369, 1994.

[14] Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *Electron Devices, IEEE Transactions on*, 47(12):2320–2325, 2000.

[15] N Singh, A Agarwal, LK Bera, TY Liow, R Yang, SC Rustagi, CH Tung, R Kumar, GQ Lo, N Balasubramanian, et al. High-performance fully depleted silicon nanowire (diameter 5 nm) gate-all-around CMOS devices. *Electron Device Letters, IEEE*, 27(5):383–386, 2006.

[16] R-H Yan, Abbas Ourmazd, and Kwing F Lee. Scaling the Si MOSFET: From bulk to SOI to bulk. *Electron Devices, IEEE Transactions on*, 39(7):1704–1710, 1992.

[17] Wei-Yuan Lu and Yuan Taur. On the scaling limit of ultrathin SOI MOSFETs. *Electron Devices, IEEE Transactions on*, 53(5):1137–1141, 2006.

[18] Seung Hyun Park, Yang Liu, Neerav Kharche, Mehdi Salmani Jelodar, Gerhard Klimeck, Mark S Lundstrom, and Mathieu Luisier. Performance Comparisons of III–V and Strained-Si in Planar FETs and Nonplanar FinFETs at Ultrashort Gate Length (12 nm). *Electron Devices, IEEE Transactions on*, 59(8):2107–2114, 2012.

[19] Frank M. Wanlass. US Patent 3356858: LOW STAND-BY POWER COMPLEMENTARY FIELD EFFECT CIRCUITRY, 12 1967.

[20] Robert H Dennard, Fritz H Gaensslen, V Leo Rideout, Ernest Bassous, and Andre R LeBlanc. Design of ion-implanted MOSFET's with very small physical dimensions. *Solid-State Circuits, IEEE Journal of*, 9(5):256–268, 1974.

[21] G Baccarani, MR Wordeman, and RH Dennard. Generalized scaling theory and its application to a 1/4 micrometer MOSFET design. *Electron Devices, IEEE Transactions on*, 31(4):452–462, 1984.

[22] Robert Chau et al. Advanced Metal Gate/High-K Dielectric Stacks for High-Performance CMOS Transistors. In *AVS 5th Int. Microelectronics Interfaces Conf*, pages 3–5, 2004.

Chapter 3

Gate Insulator Development

3.1 Introduction: Gate Insulator Development

As described in Chapter 2, the intrinsic MOSFET drive current and transconductance is proportional to the gate-channel capacitance. One of the capacitors that comprises $C_{gate-channel}$ is the wide bandgap insulator capacitance. For HEMTs, this is a semiconductor with a conduction band offset to the channel. However, this offset is not large (InGaAs/InAlAs $\sim$ 0.5 eV) compared to oxide-based insulators (InGaAs/$Al_2O_3$$\sim$ 2.5 eV) and has a fixed dielectric permittivity (InAlAs $\sim$ 12.5). This chapter will overview the use of atomic layer deposition to form insulators on InGaAs channels.

3.2 Why ALD Dielectrics?

Figure 3.1 is a cartoon of a HEMT and an electron band diagram under the gated channel region of the device. The gate insulator for the HEMT is InAlAs, having a 0.5 eV conduction band offset to InGaAs, when lattice-matched to InP [1]. The permittivity of InAlAs is also fixed at 12.5 [2]. These place limits on the scalability

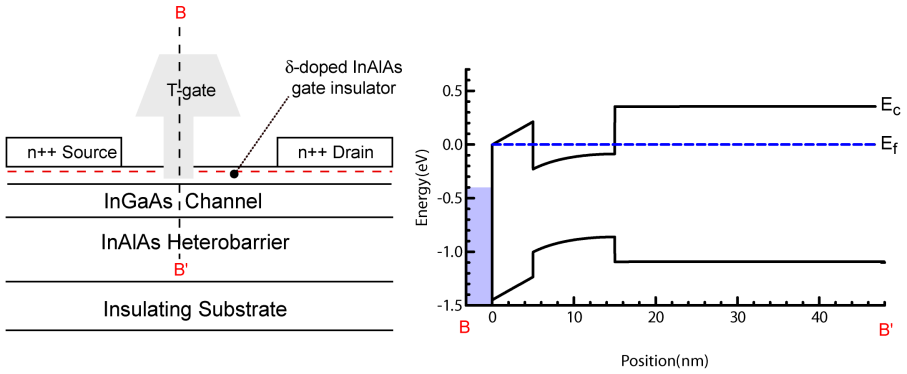


Figure 3.1: HEMT cartoon cross-section with electron band diagram under the gated channel region.

of InGaAs/InAlAs HEMTs. As outlined in Chapter 2, a III-V MOSFET needs the highest possible capacitive coupling to the channel without excessive gate leakage currents. In a HEMT, the low gate insulator barrier height will create significant gate leakage currents with moderate positive gate bias, due to thermionic emission over the small heterobarrier and tunneling current through the barrier. As we scale the thickness of the insulator to improve performance, tunneling currents will increase rapidly, rendering the transistor inoperable.

One solution to this problem is oxygen- or nitrogen-based insulators, offering larger bandgaps, favorable electron band offsets to InGaAs, and high dielectric permittivity (aka, "high-k"). Figure 3.2 is a cartoon of a source/drain regrowth MOSFET and an electron band diagram under the gated channel region of the device. High-k insulators can be thicker than lower permittivity dielectrics for the same capacitance density, and simultaneously have low gate leakage currents.

The current best method for forming these high-k dielectrics is atomic layer deposition (ALD). ALD is a specialized form of chemical vapor deposition [3]. During each cycle of ALD, a metal-organic precursor is conformally deposited over the entire

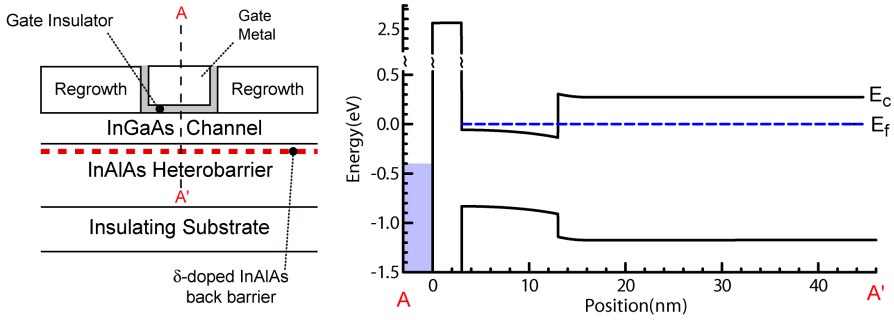


Figure 3.2: MOSFET cartoon cross-section with electron band diagram under the gated channel region.

sample. Then, metal-organic is evacuated from the chamber. A second precursor enters the chamber and reacts with the covered surface, creating approximately one monolayer of the desired material. This cyclic deposition technique allows for self-limiting growth, enabling precise thickness control of MOSFET gate insulators. It is by nature a conformal process, critical for future non-planar MOSFET geometries. It is compatible with relativity low temperatures ($\sim 300°C$), favorable for the limited thermal budget in III-V device processing.

However, with any dielectric material deposition on III-V-based materials, the interface trap density between the dielectric and semiconductor can be quite large. As outlined in Chapter 2, this interface trap distribution can negatively impact transistor performance, specifically lowering drive currents and increasing subthreshold swing. Since the 1960s [4], researchers have invested significant resources to passivate III-V surfaces [5]. A few groups have shown success with $GaGdO_x$-based materials [6]. Other groups have tried careful oxidation of some III-V materials [7], with success. Sulfur passivation has been shown to work as well [8],[9],[10]. The majority of work in the last five years of $In_xGa_{1-x}As$-based MOSFET technology has focused on sulfur passivation; this dissertation has focused on alternatives to

sulfur passivation.

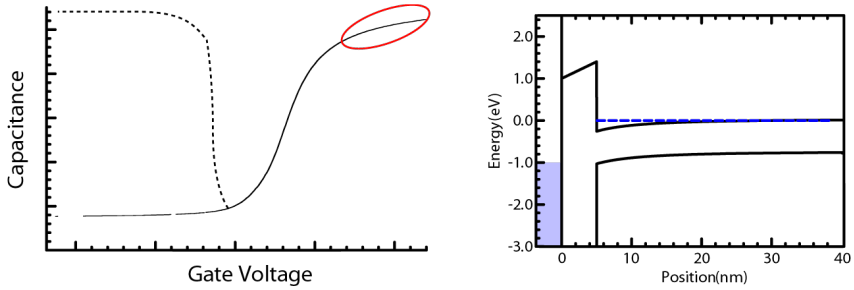
3.3 MOSCAP Theory

Figure 3.3 is a series of electron band diagrams depicting regions of operation for a MOS capacitor (MOSCAP). In this example the substrate is doped n-type.

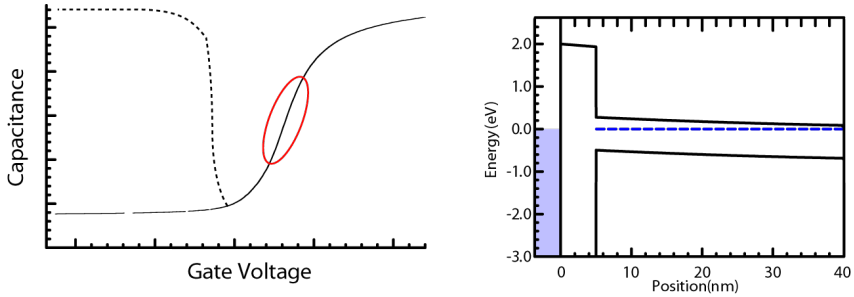
Accumulation: (Figure 3.3a) When the gate bias is positive with respect to the substrate, electrons accumulate on the surface of the semiconductor. Since the bulk semiconductor has the same majority carrier as the accumulated surface, the mobile charges can respond rapidly, making this capacitance constant with frequency.

Depletion: (Figure 3.3b) Further decreases in gate bias remove any majority carriers from the surface, and now gate charge images on the mobile charges near the edge of the depletion region. This will decrease the measured capacitance. As the negative bias increases, this depletion region increases, lowering the capacitance even further.

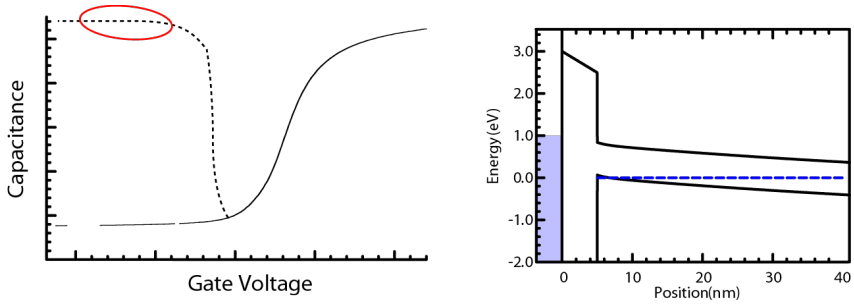
Inversion: (Figure 3.3c) As the gate bias continues negative, the surface Fermi level reaches the minority carrier band edge (in this case, the valence band). The hole response is governed by generation-recombination with the majority carriers; therefore, it is frequency dependent. For low-frequency AC signals on the order of the minority carrier generation-recombination time constants, the inversion layer can respond to the gate charge, and we can measure the valence band density of states capacitance. This inversion layer screens out the charge at the depletion region edge. For high-frequency AC signals, the inversion layer cannot respond, and the gate charge must image on the depletion region mobile charge. This is high-frequency depletion (Figure 3.3d). From the oxide thickness and depletion



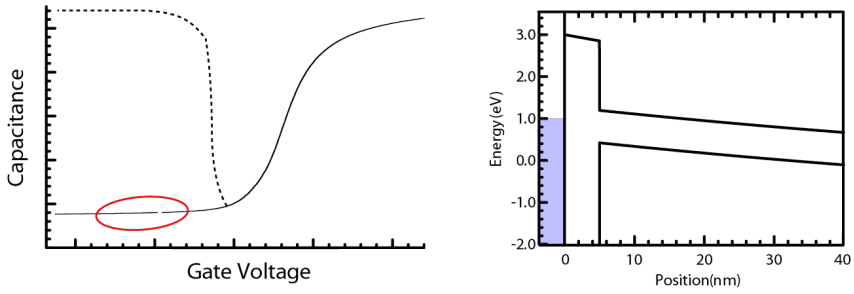
(a) Accumulation



(b) Depletion



(c) Inversion



(d) High-frequency depletion

Figure 3.3: C-V and Electron Band Diagrams of an example MOSCAP

region thickness, one can calculate the minimum capacitance in this region. The equation is [11]:

$$C_{min} = \frac{1}{C_{ox}} + \sqrt{\frac{4k_B T \ln(N_d/n_i)}{\epsilon_{semi} q^2 N_d}} \tag{3.3.1}$$

where C_{ox} is the insulator capacitance, k_B is Boltzmann's constant, T is the temperature, N_d is the semiconductor doping concentration, n_i is the intrinsic carrier concentration at the given temperature, and ϵ_{semi} is the semiconductor permittivity. For $C_{ox} = 1.59\ \mu F/\text{cm}^2$ (5nm Al_2O_3), T = 300 K, $N_d = 1{\times}10^{17}\ \text{cm}^{-3}$, $n_i = 8.4{\times}10^{11}\ \text{cm}^{-3}$, $\epsilon_{semi} = 13$, $C_{min} = 0.114\ \mu F/\text{cm}^2$.

In classic silicon MOSFETs, n-type material surfaces would be inverted for PMOS transistors, where the n-type doping serves to confine holes to the surface during inversion. III-V MOS operates similar to accumulation, where the device is already somewhat n-type, and under gate bias it has more conduction band charge.

3.4 InGaAs Passivation: Arsenic Capping

Arsenic capping of III-V material is useful for quasi *in-situ* characterization of materials [12]. The cap can be deposited in a solid-source MBE immediately after wafer growth. When the cap is thick and/or dense enough, and shipped in sealed UHV containers, the material can leave the MBE chamber for reasonable amounts of time and maintain underlying surface quality. MOS capacitor experiments using arsenic caps and Al_2O_3/InGaAs structures have shown world-record low capacitance frequency dispersion [13].

However, arsenic caps have process constraints. Each cap is unique, leading

to process variances during decapping. One benefit of the cap is its low desorption temperature (350°C for [12], 460°C for [13]), but this prevents any intervening moderate temperature process steps, since the arsenic decapping may contaminate tooling. Finally, non-planar device structures will likely be incompatible with arsenic capping due to the types of processing required to create those non-planar structures.

3.5 InGaAs Passivation: *In-Situ* Treatment

In 2009, an ALD tool was installed in the UCSB Nanofabrication Lab. Thermal desorption of an arsenic cap is not allowed to prevent sample cross-contamination. Instead, an *in-situ* dry treatment method was developed using hydrogen plasma and trimethylaluminum. This method was developed to restore an air-exposed InGaAs surface, removing the need for arsenic capping.

For the treatment experiments, samples with 300 nm 1×10^{17} cm^{-3} Si-doped n-type InGaAs on 3×10^{18} cm^{-3} S-doped n-type InP were grown by MBE. Before Al_2O_3 deposition, samples were dipped for 10 seconds in 10:1 deionized H_2O:HCl to remove surface oxides and provide a controlled surface going into the reactor. Samples were then immediately loaded in air into a commercial ALD reactor (Oxford Instruments FlexAL ALD). The base pressure of the reactor was approximately 1×10^{-6} Torr; pressure was held at 0.2 Torr during the deposition. The substrate temperature was held constant at 300°C. Prior to ALD Al_2O_3 film growth, four different treatments involving remote ICP on the initial InGaAs surface were investigated. Treatment A was the reference point in which the surface was not treated in the chamber prior to ALD oxide growth. Treatment B exposed the surface to five

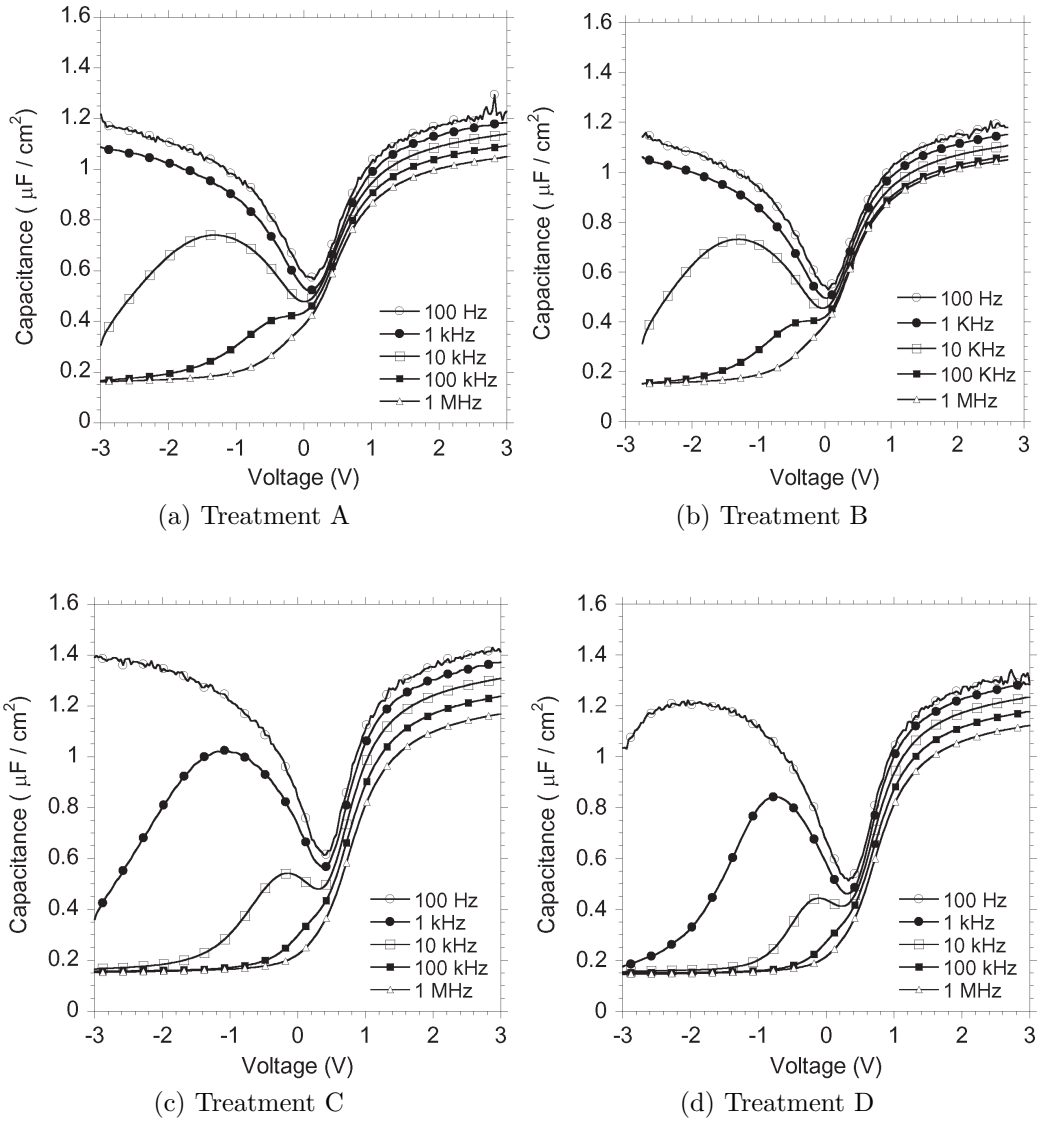
cycles of trimethylaluminum (during each cycle: TMA pulse for 40 msec, 5 second Ar purge, and 10 second H_2 gas stabilization step) as a probe of TMA half cycle reactions on the surface prior to growth. Treatment C exposed the surface to five cycles of hydrogen plasma (during each cycle: 20 mTorr H_2 pressure at 100W ICP power for 2 seconds, 5 second Ar purge, and 10 second H_2 stabilization step) as a probe of *in-situ* surface oxide removal prior to growth. Treatment D subjected the surface to five cycles of hydrogen plasma and TMA exposure (during each cycle: 20 mTorr H_2 pressure at 100 W ICP power for 2 seconds, TMA pulse for 40 msec, 5 second Ar purge, and 10 second H_2 stabilization step) in order to determine the effects of active hydrogen not only on the surface oxide removal but also on the quality of the initial Al interface layer prior to bulk Al_2O_3 growth. During each cycle of Al_2O_3 film growth, TMA was pulsed for 20 msec followed by a 7 second Ar purge, deionized H_2O was pulsed for 100 msec followed by a 7 s Ar purge, the reactor was pumped down for 7 seconds, and finally Ar was flowed at 0.2 Torr for 7 seconds. 50 such growth cycles were completed for all samples. *Ex-situ* measurements using variable angle spectroscopic ellipsometry (J.A. Woollam M-2000DI) estimated the nominal Al_2O_3 growth rate at 0.11 nm per cycle (5.5 nm total oxide thickness).

After oxide deposition, the samples were annealed at 400°C for one hour in a rapid thermal annealer using 10 L/min forming gas flow at atmospheric pressure. In order to form MOSCAPs, 150 micron diameter, 100 nm thick nickel gate electrodes were deposited by thermal evaporation on the Al_2O_3 side of the sample through a shadow mask. Thermal evaporation was chosen to avoid sample damage by exposure to x-ray photons or high kinetic energy ions associated with electron beam evaporators and sputter deposition plasmas [14]. A back side ohmic contact was formed by blanket thermal evaporation of 10 nm Cr and 100 nm Au. Samples

were then bonded to a gold-coated silicon carrier wafer with indium for subsequent measurements.

All electrical measurements used an Agilent 4294A impedance analyzer in a shielded dark box. The DC bias was swept from negative to positive voltages with a 50 mV RMS AC modulation signal. In order to accurately extract C_{oxide} , MOSCAPs using Treatment D (H_2/TMA cycles) on sample material with different Al_2O_3 thicknesses were fabricated and measured at positive gate bias. From the variation of the measured capacitance with Al_2O_3 thickness, a relative permittivity of 8.7 ± 0.2 was determined.

Figures 3.4 and 3.5 show measurements of capacitance and conductance as a function of bias voltage and frequency. Samples having different surface preparations show clear differences in the capacitance dispersion in accumulation, in the "false inversion" capacitance peak [15], in the rate of change of high-frequency capacitance with bias voltage, and in the conductance. Comparing accumulation capacitance at +2.75 V bias, the ratio of low-frequency (100 Hz) to high-frequency (1 MHz) capacitance is 1.17:1 for the untreated sample (Treatment A), 1.12:1 for TMA-only treatment (Treatment B), 1.2:1 for H_2-only treatment (Treatment C), and 1.15:1 for H_2 /TMA surface treatment (Treatment D). Yuan *et al.* [16] attribute dispersion in accumulation to border traps near the oxide/semiconductor interface. Measurement of a peak in capacitance at biases below accumulation for n-type InGaAs samples is an indication of mid-gap interface trap density, not semiconductor surface inversion [15]. This false inversion capacitance peak is strongest in the untreated and TMA-only treated samples (Treatments A and B), moderate with H_2-only treatment (Treatment C), and smallest for H_2/TMA surface treatment (Treatment D).



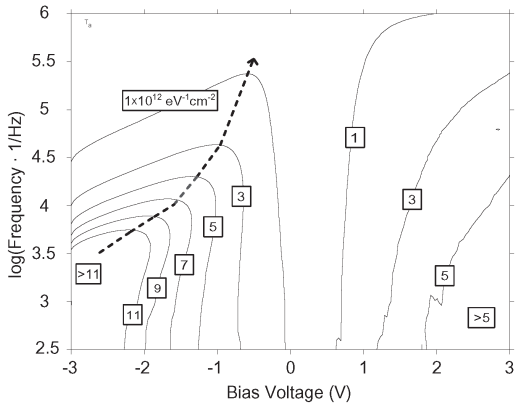
(a) Treatment A

(b) Treatment B

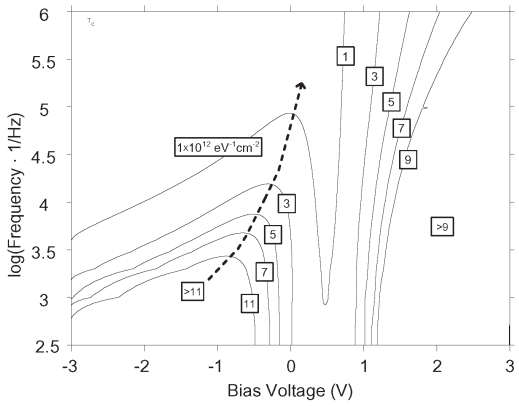
(c) Treatment C

(d) Treatment D

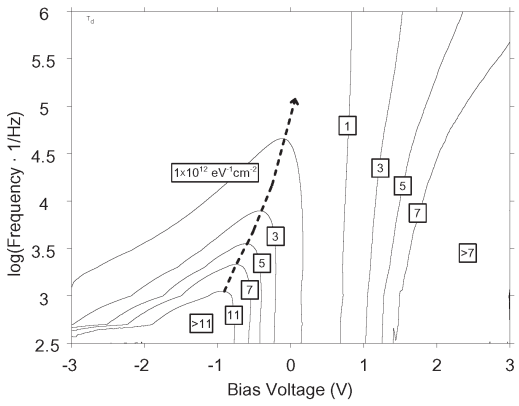
Figure 3.4: C-V measurements of four ALD treatments



(a) Treatment A



(b) Treatment C



(c) Treatment D

Figure 3.5: G-V measurements of four ALD treatments

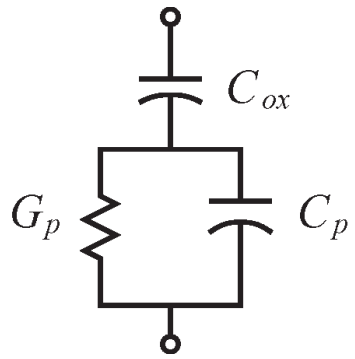


Figure 3.6: Circuit model for parallel conductance extraction.

Another comparative measure of interface trap density is the rate of change of high-frequency capacitance with bias voltage. This is typically called "stretch out" [17, p. 325]. For the untreated and TMA-only treated samples, dC / dV = 0.62 μF cm^{-2}V^{-1}, while both for the H_2 and H_2/TMA samples (Treatments C and D), dC / dV = 0.9 μF cm^{-2}V^{-1}. For all four samples, there is no inversion response at negative bias. Further, all samples fail to reach the minimum depletion capacitance ($\sim$ 0.15 μF/cm^2) measured versus 0.114 μF/cm^2 (Eqn. 3.3.1) expected for this epitaxial design at strong negative biases.

Herbert *et al.* have demonstrated quantitative measurement of interface trap density from measurement of the variation of conductance with bias voltage and frequency; Figure 3.5 shows the normalized conductance-voltage maps for treatments A, C, and D. The parallel conductance, G_p is derived from the circuit model of Figure 3.6 and is expressed as:

$$G_p = \frac{\omega^2 C_{ox}^2 G_{measure}}{G_{measure}^2 + \omega^2 \left(C_{ox} - C_{measure}\right)^2} \tag{3.5.1}$$

where ω is the applied angular frequency, and $C_{measure}$ and $G_{measure}$ are the measured capacitance and conductance. Assuming Shockley-Read-Hall statistics

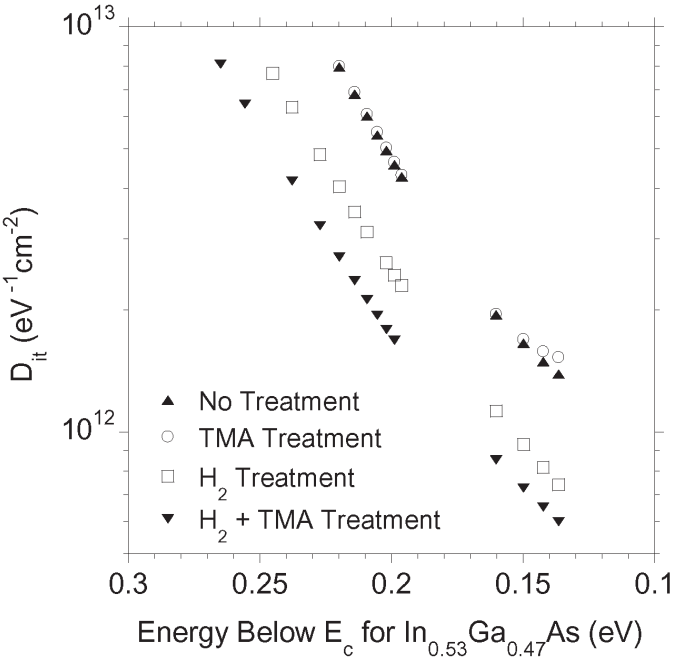


Figure 3.7: Interface trap density as a function of energy level below the (100) InGaAs conduction band edge for all four treatments.

for the traps, one can estimate the trap energy level below the conduction band edge from the applied measurement frequency:

$$\Delta E = \frac{k_B T}{q} \ln \left[\frac{\sigma v_{thermal} D_{3D}}{\omega} \right] \tag{3.5.2}$$

where σ is the capture cross section, $v_{thermal}$ is the semiconductor electron thermal velocity, and D_{3D} is the three-dimensional effective conduction band density of states. The methods of Herbert *et al.* are used to determine interface traps as a function of ΔE below the InGaAs conduction band, and are described in detail in Reference [15].

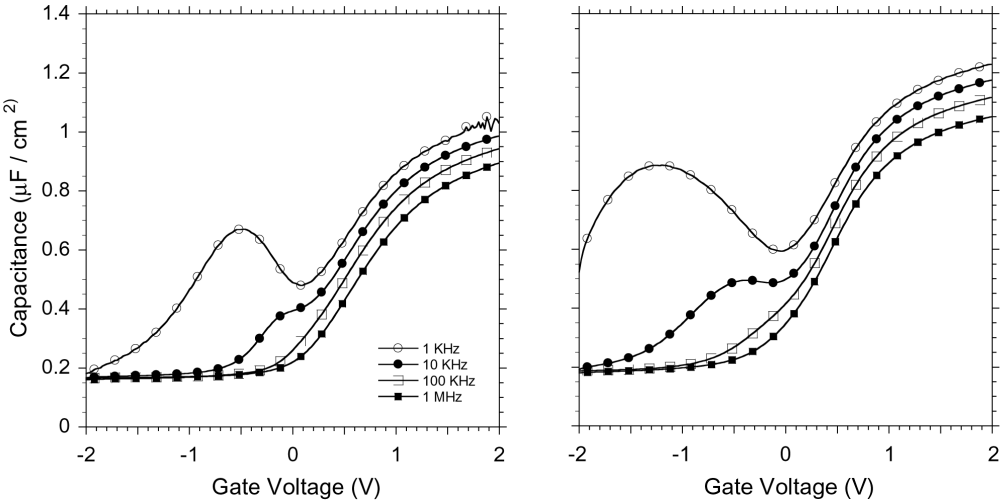
Figure 3.7 shows interface trap density as a function of ΔE below the InGaAs conduction band. For InGaAs lattice-matched to InP, we assume $\sigma = 1{\times}10^{-16}$

cm^{-2}, $v_{thermal}$ = 5.6×10^7 cm s^{-1}, and D_{3D} = 2.2×10^{17} cm^{-3}. Interface trap density extracted by this method is highest for the untreated and TMA-only treated samples (Treatments A and B), both having 4.6×10^{12} $eV^{-1}cm^{-2}$, 0.2 eV below E_c. Interface trap density is moderate at 2.5×10^{12} $eV^{-1}cm^{-2}$ with H_2-only treatment (Treatment C) and smallest at 1.7×10^{12} $eV^{-1}cm^{-2}$ for H_2 /TMA surface treatment (Treatment D). Figure 3.7 does not include measurements where $C_{ox} > q^2 D_{it}$ since the conductance method is known to be inaccurate for this condition. The conductance map trend is clear in indicating the efficacy of the hydrogen plasma treatments to the InGaAs / Al_2O_3 interface. It has been shown in the literature that forming gas (5% H_2 / 95% N2) annealing of Pt/high-k/InGaAs MOSCAPs improves the CV frequency dispersion and subsequently lowers the interface trap density extracted by the conductance method.

3.6 High-k Process Damage

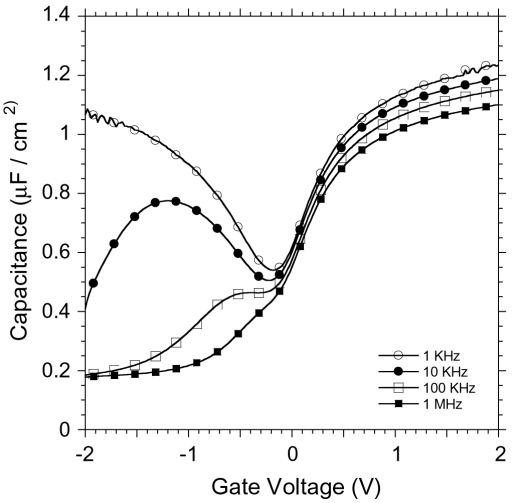
The MOSCAP process flow outlined in Section 3.5 is useful for comparative tests between new ALD recipes; however, a MOSFET process flow (See Chapter 5 and 6) has more processing steps, and therefore more chances to alter the interface trap distribution of the insulator/semiconductor interface. A few process damage cases were examined with MOSCAPs.

The gate first process flow (see Chapter 5) uses a sputter-deposited tungsten gate electrode. Sputter deposition uses high-energy plasma ions to eject metal from a target; these metal atoms then travel to and bond with the sample. These metal ions and the plasma ions are in proximity to the sample, and can cause ion damage to the material. In Figures 3.8a and 3.8b, 5 nm of Al_2O_3 was deposited



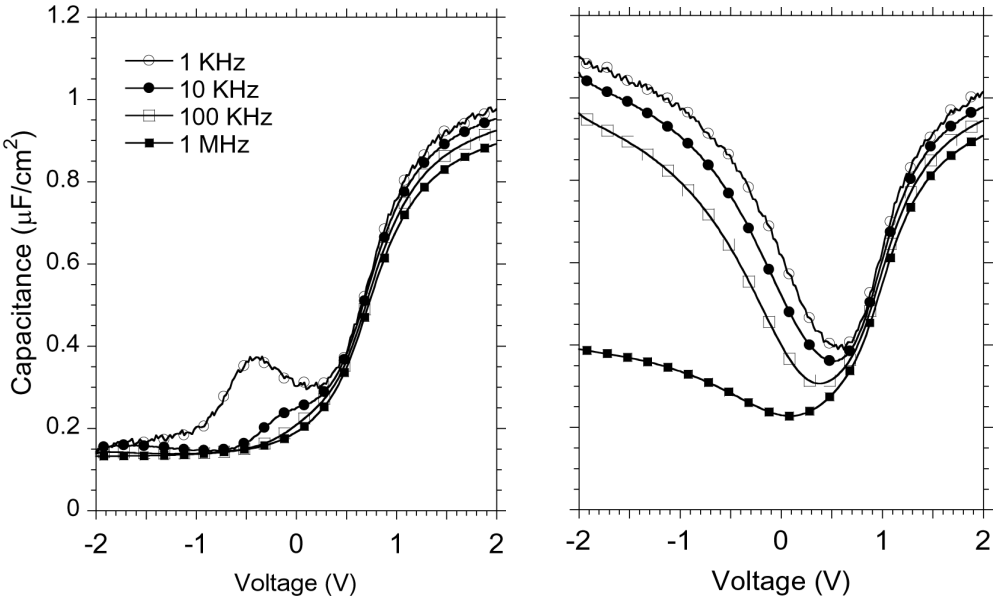
(a) Ni metal, no pre-metal anneal

(b) W metal, no pre-metal anneal



(c) W metal, pre-metal anneal 500°C

Figure 3.8: 5 nm Al_2O_3 on MOSCAP epi, gate metal damage experiment.

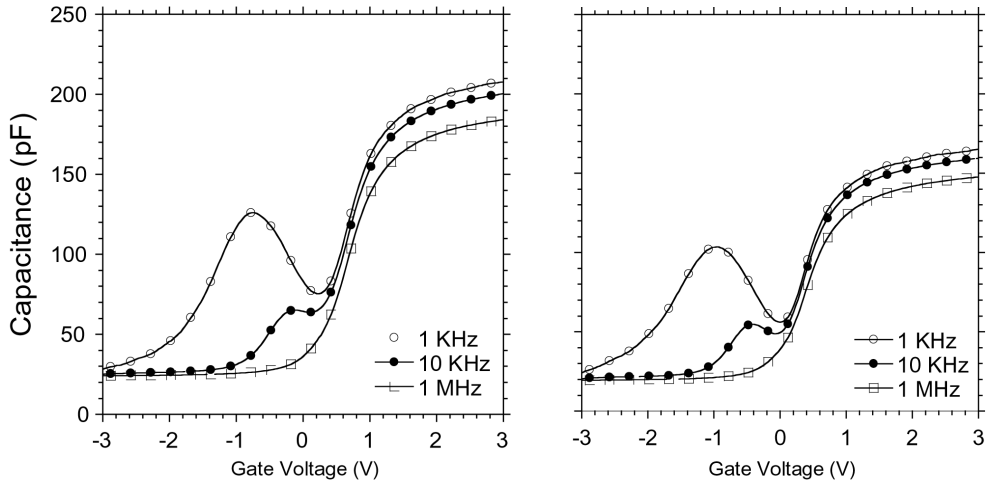


(a) SiO_xdeposition, no anneal (b) SiO_xdeposition, 500 °C anneal

Figure 3.9: 5 nm Al_2O_3 on MOSCAP epi, dummy gate anneal experiment.

on MOSCAP epi. One sample had nickel thermal evaporation and the other had sputtered tungsten evaporation. Neither were annealed before metal deposition. It is clear the sputtered metal increases the depletion region dispersion, indicating a potential increase in interface trap density. Figure 3.8c shows the MOSCAPs after a PECVD SiO_x coating and 500°C RTA anneal to simulate MBE regrowth conditions. While annealing improves frequency dispersion around zero bias, it increases depletion dispersion considerably.

In the gate last process, an SiO_xdummy gate is deposited by PECVD directly on epitaxial material, the gate is defined, and source/drain regions are regrown. Figure 3.9 shows two 5 nm Al_2O_3 MOSCAP measurements. The sample in 3.9a had PECVD deposition, oxide removal with BOE, and immediate high-k deposition, while the sample in Figure 3.9b had a 500°C RTA anneal prior to cap removal. There



(a) 5 nm Al_2O_3, Ni gate electrode

(b) 5 nm Al_2O_3, 1 nm HfO_2, Ni gate electrode

Figure 3.10: Single layer versus bi-layer gate insulator

was a dramatic increase in depletion dispersion due to this anneal. This suggests the MOSCAP epi is damaged during this SiO_x-capped anneal, and MOSFET epi would likely suffer similar damage during a regrowth process.

3.7 Summary of Current Insulator Development

Since the development of this surface treatment, research groups at UCSB expanded on the technique to further reduce interface trap density and increase effective oxide capacitance.

Al_2O_3/HfO_2 bi-layers: Initially, Al_2O_3 was found to adequately passivate InGaAs. For the gate last process flow (Chapter 6), gate metal liftoff occurs directly on device insulator; optical photoresist developer will etch Al_2O_3. An etch stop barrier was needed; HfO_2 will not etch significantly in developer. Figure 3.10 shows capacitors with and without this etch stop layer. The bi-layer does not significantly

increase interface trap density, making it suitable for our process flow.

The Stemmer Group used this process flow to further improve the high-k dielectrics on InGaAs. Increased hydrogen treatments further reduced interface traps [18], and use of nitrogen plasma rather than hydrogen plasma [19] allowed for HfO_2-only gate oxides without a significant increase in interface trap density.

3.8 Conclusions

Intrinsic field effect device performance is defined by the capacitive control of the channel by the gate electrode. One can increase this capacitance by decrease the gate insulator thickness or increasing its permittivity. For HEMTs, thinning rapidly increases gate leakage, rendering devices inoperable. Development of high-k dielectrics with reasonable interface trap densities is one way to continue scaling field effect devices. A method of *in-situ* surface treatment was developed to minimize the interface trap density. These concepts were further developed by other research groups to provide sub-nanometer EOT dielectrics with reasonable interface trap densities.

References

[1] R People, KW Wecht, K Alavi, and AY Cho. Measurement of the conduction-band discontinuity of molecular beam epitaxial grown $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$, N-n heterojunction by C-V profiling. *Applied Physics Letters*, 43(1):118–120, 1983.

[2] P Bhattacharya, editor. *Properties of Lattice-Matched and Strained Indium Gallium Arsenide*. INSPEC, London, 1993.

[3] Steven M George. Atomic layer deposition: an overview. *Chem Rev*, 110:111–131, 2010.

[4] H Becke, R Hall, and J White. Gallium arsenide MOS transistors. *Solid-State Electronics*, 8(10):813–823, 1965.

[5] BJ Skromme, CJ Sandroff, E Yablonovitch, and T Gmitter. Effects of passivating ionic films on the photoluminescence properties of GaAs. *Applied Physics Letters*, 51(24):2022–2024, 1987.

[6] Matthias Passlack. Development methodology for high-κ gate dielectrics on III–V semiconductors: $Gd_xGa_{0.4-x}O_{0.6}/Ga_2O_3$ dielectric stacks on GaAs. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 23(4):1773–1781, 2005.

[7] Xiu Xing and Patrick J Fay. Enhancement-Mode Pseudomorphic $In_{0.22}Ga_{0.78}As$-channel MOSFETs With Ultrathin InAlP Native Oxide Gate Dielectric and a Cutoff Frequency of 60 GHz. *Electron Device Letters, IEEE*, 31(11):1214–1216, 2010.

[8] VN Bessolov, MV Lebedev, EB Novikov, and BV Tsarenkov. Sulfide Passivation of III–V Semiconductors: Kinetics of the Photoelectrochemical Reaction. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 11(1):10–14, 1993.

[9] YQ Wu, M Xu, RS Wang, O Koybasi, and PD Ye. High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum G m exceeding 1.1 mS/μm: New HBr pretreatment and channel engineering. In *Electron Devices Meeting (IEDM), 2009 IEEE International*, pages 1–4. IEEE, 2009.

[10] Han-Chung Lin, Wei-E Wang, Guy Brammertz, Marc Meuris, and Marc Heyns. Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator. *Microelectronic Engineering*, 86(7-9):1554–1557, 2009.

[11] Yuan Taur and Tak H Ning. *Fundamentals of modern VLSI devices*. Cambridge University Press, 2009.

[12] WM Lau, RNS Sodhi, S Jin, S Ingrey, N Puetz, and A Springthorpe. Capping and decapping of InP and InGaAs surfaces. *Journal of Applied Physics*, 67(2):768–773, 1990.

[13] Eun Ji Kim, Lingquan Wang, Peter M Asbeck, Krishna C Saraswat, and Paul C McIntyre. Border Traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) Gate Stacks and Their Passivation by Hydrogen Anneals. *Applied Physics Letters*, 96:012906, 2010.

[14] Ching-Hui Chen, Evelyn L Hu, Winston V Schoenfeld, and Pierre M Petroff. Metallization-induced damage in III–V semiconductors. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 16(6):3354–3358, 1998.

[15] Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces, author=Engel-Herbert, Roman and Hwang, Yoontae and Stemmer, Susanne. *Journal of Applied Physics*, 108(12):124101–124101, 2010.

[16] Yu Yuan, Lingquan Wang, Bo Yu, Byungha Shin, Jaesoo Ahn, Paul C McIntyre, Peter M Asbeck, Mark JW Rodwell, and Yuan Taur. A distributed model for border traps in Al_2O_3-InGaAs MOS devices. *IEEE Electron Device Letters*, 32(4):485, 2011.

[17] EH Nicollian and JR Brews. *MOS (Metal Oxide Semiconductor) Physics and Technology*. Wiley, New York, 2002.

[18] Gift Chobpattana. Private communication. 2013.

[19] Varistha Chobpattana, Junwoo Son, Jeremy JM Law, Roman Engel-Herbert, Cheng-Ying Huang, and Susanne Stemmer. Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities. *Applied Physics Letters*, 102(2):022907–022907, 2013.

Chapter 4

Source-Drain Regrowth Development

4.1 Introduction

MOSFET source-drain regions must be designed to not degrade intrinsic device performance. They must have low access resistance to the channel, sufficiently high doping, low sheet resistance, and be capable of low contact resistivities to metal. In silicon processing, techniques have been developed and refined to meet or exceed these goals [1],[2]. III-V-based devices have not been able to take advantage of this research, opting for other techniques that ultimately limit device performance. In this chapter, we examines the source-drain region formation by epitaxial regrowth. This process module meets the needs of MOSFETs measured in this dissertation, with the ability to scale for future device performance.

4.2 Why Source-Drain Regrowth?

As outlined in Chapter 2, field effect devices have a layer of induced charge on their surface; the shape of this layer is driven by surrounding electrostatics. By definition,

the rest of the substrate is of a lower sheet carrier density than the induced layer, or there would be no change in conductivity. Highly conductive regions of the same induced charge type (electrons or holes) need to be added to contact this induced charge.

In silicon MOSFETs, these source-drain regions have been formed a few ways, depending on process maturity. Initially, dopant diffusion via thermal furnaces was used [3, p.374]. Dopant diffusion is governed by Fick's First Law; buried, heavily-doped, narrow regions are hard to form and maintain with a low thermal budget. Ion implantation of dopants allows for flexibility in dopant depth and concentration. However, annealing is typically required to remove crystal damage during implantation; dopant diffusion will occur and, once again, heavily-doped, narrow regions are "smeared" out. Another downside of ion implantation is straggle. While the distribution of ions is statistically well-known, the ions at the edges of the distribution can diffuse far away from the implant centroid. Channeling of the dopant along crystal axes exacerbates this effect. This causes fluctuations of the source-drain regions near the gate edge. This effect has the potential of shorting the source and drain out at very small gate lengths. New techniques for ion implantation and annealing, such as plasma deposition [4] and laser annealing [5], are being explored to overcome these challenges.

The source-drain semiconductor is only part of the total source-drain region. Metal-semiconductor resistances are also important. This resistance is dictated by the semiconductor surface Fermi level pinning, the level of doping, and the choice of metal. For silicon, the silicide process [1] provides the necessary low contact resistance to the semiconductor.

While silicon MOSFETs have relatively well-understood source and drain tech-

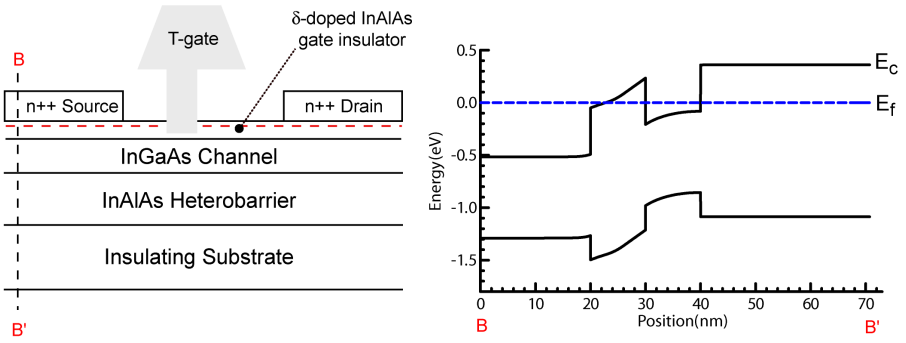


Figure 4.1: HEMT cartoon cross-section with electron band diagram under source-drain region.

niques, the same cannot be said for III-V-based semiconductors. Ion implantation techniques do not readily translate. Implants must be annealed, and while the crystal structure can be partially repaired, it is never as defect-free as prior to implant. This leads to traps inside the semiconductor, reducing mobility and charge densities. Figure 4.1 is a cartoon of a HEMT and an electron band diagram under the source-drain region of the device. HEMT structures [6] rely on as-grown heavily-doped surfaces to provide source-drain contact. InGaAs/InAlAs HEMTs also require etch-stop layers of a different composition than the channel; this creates a electron potential step-barrier between the source-drain and the channel regions, leading to increased access resistance. Moreover, the gate region is now defined by semiconductor etching; the heavily-doped contact material must be removed. This might put a lower bound on gate length depending on the gate definition process employed.

Rather than etch to define the channel region, it would be better to define it first and then add back the source and drain, much like a silicon MOSFET process flow. Figure 4.2 is a cartoon of a regrowth MOSFET and an electron band diagram underneath the source-drain contact. Semiconductor regrowth is a

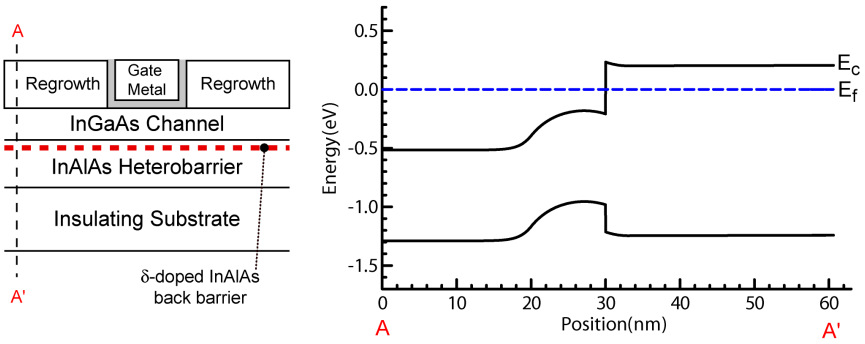


Figure 4.2: MOSFET cartoon cross-section with electron band diagram under source-drain region.

technique used in silicon MOSFETs [7], [8], and III-V photonic devices [9]. For silicon MOSFETs, regrowth allows for well-controlled source-drain regions with the ability to drive-in dopants closer to the channel underneath sidewall spacers. For photonic applications, regrowth can serve as both a heavily-doped semiconductor for contacts and current blocking layers in laser structures. In the case of Figure 4.2, the regrowth lies directly on the semiconductor without intervening wide-bandgap etch stops that could limit current flow. One limitation is that the channel material is still undoped; one can recess the channel prior to regrowth, therefore replacing it with heavily-doped regrown semiconductor.

Rather than a silicide process, the III-V regrowth process relies on simple metal evaporation onto the source-drain. Groups have developed silicide-like processes using Ni-InGaAs and Ni-InAs [10], [11]. As will be shown in this chapter, simple metal evaporation provides adequately low resistance contacts to the heavily doped source-drain regions for the given current densities.

Given the tools available at the time, MBE regrowth was attempted for the source and drain regions. In 2013, MOCVD at UCSB became a viable regrowth

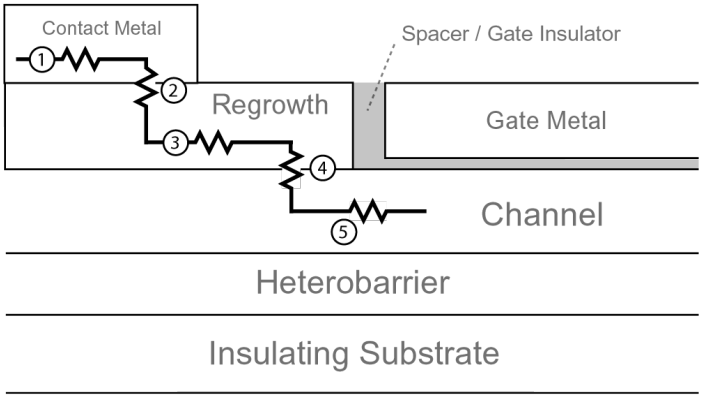


Figure 4.3: MOSFET with access resistance breakdown

technique, and was employed.

4.3 Regrowth Resistance Characterization

Figure 4.3 outlines the resistances in the source-drain region of a MOSFET:

1) Contact metal sheet resistance ($\Omega/\square$): If the device has any planar contact metal, current flows along this sheet until it reaches the device. This sheet resistance should be much smaller than the device resistance. In VLSI, the lateral distance is minimized to maximize device density.

2) Metal-semiconductor contact resistivity ($\Omega \cdot \mu m^2$): This resistivity is a function of contact metal, surface preparation, semiconductor type, and semiconductor doping density. The smaller this number is, the smaller the contact area can be in (1).

3) Semiconductor regrowth sheet resistance ($\Omega/\square$): This sheet resistance is a function of semiconductor type, thickness, and doping density. This should be

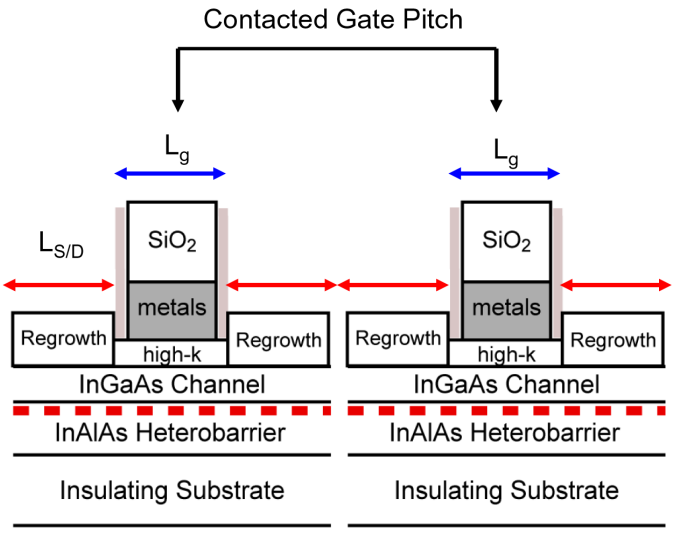


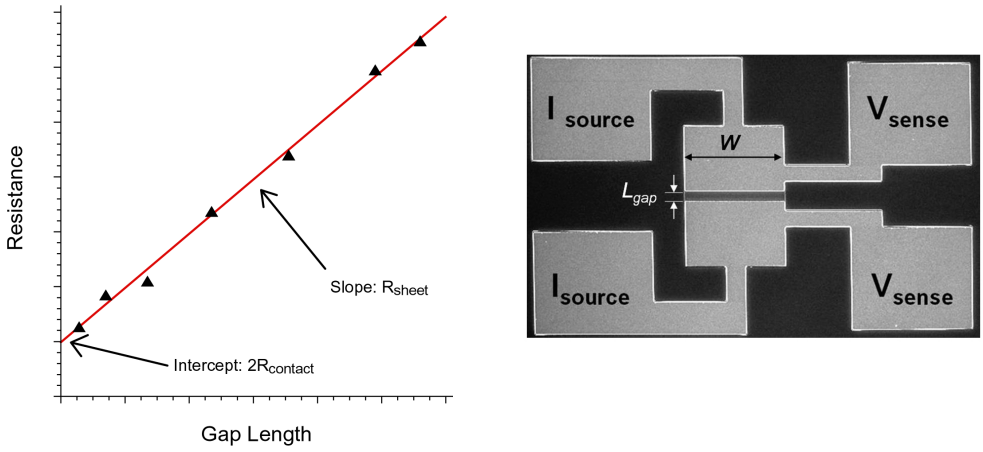
Figure 4.4: Cartoon of adjacent MOSFETs, contacted gate pitch

minimized to minimize parasitic access resistances.

4) Regrowth-metal contact resistance (Ω·μm): This resistance term occurs due to removal of the epitaxial material from the MBE for processing. Channel oxidation and process damage will increase this term.

5) Spacer-channel sheet resistance (Ω/□): This gap underneath the gate spacer is typically doped channel material. In silicon CMOS, ion implantation and other doping techniques ensure this is a small component of the total device access resistance. For III-V materials, where ion implant at this scale is difficult, this distance must be a small as possible, or a recessed channel regrowth must be employed.

For VLSI circuits, an important metric is gate pitch spacing, or the distance between adjacent gates. Figure 4.4 defines contacted gate pitch. The contacted gate pitch is the gate length and the two source-drain contact lengths. While the gate length is usually determined by the process node and optimized for best electrostatic channel control, the source-drain metallization lateral dimensions are



(a) TLM data with least squares fit (b) SEM of TLM test structure

Figure 4.5: TLM data analysis and test structure

determined by metal-semiconductor contact resistivity. The smaller the contact resistivity, the smaller we can make the source-drain contact length, and the more devices can be "packed in" per unit die area.

The best n-type contacts to InAs or InGaAs can be made *in-situ* or *ex-situ*, assuming the semiconductor doping is high ($\sim \times 10^{19}$ or more). For both InAs and InGaAs the best is on the order of 0.5 to 1 $\Omega \cdot \mu m^2$ [12][13].

High-performance MOSFETs require intimate knowledge and precise control of all five parasitic terms. Sheet resistances are typically trivial to characterize with four-point probe resistance measurements. Semiconductor regrowth resistance parameters are determined by growth technique, and can be calibrated independently from transistor fabrication. However, the metal-semiconductor contact resistivity is difficult to predict *a priori*; it must be measured on the sample. "Transmission line" or "transfer length" measurements (TLMs) are used to measure the contact resistivity.

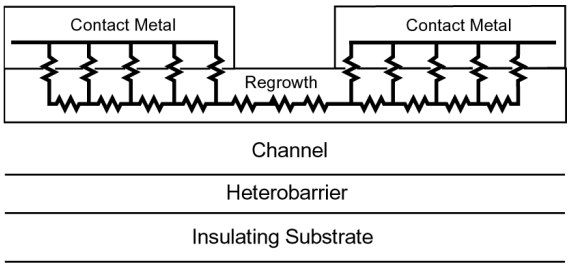


Figure 4.6: SEM image of a TLM structure

Figure 4.5a is a plot of TLM data versus gap spacing. Figure 4.5b is a SEM of a TLM test structure. Current is forced through the I_{source} pads, and voltage measured on the V_{sense} pads, and resistance determined. Plotting measured resistance as a function of gap length, one can extract gap sheet resistance ($\Omega/\square$) and metal-semiconductor contact resistance ($\Omega\cdot\mu m$). Mathematically:

$$R_{measured} = R_{sheet}L_{gap} + 2R_{contact} \tag{4.3.1}$$

where $R_{measured}$ is the width-normalized measured resistance ($\Omega\cdot\mu m$), R_{sheet} is the semiconductor sheet resistance in the gap, L_{gap} is the gap length, and $R_{contact}$ is the end resistance of the test structure. The $R_{contact}$ term (y-intercept) captures the metal-semiconductor resistance; however, the planar nature of current flow in a TLM does not immediately provide the specific contact resistivity ($\Omega\cdot\mu m^2$). Most of the current flows along the low-resistance metal and "crowds" near the gap. Modeling the contact region as a semi-infinite resistor network 4.6, solving the differential equation for voltage and current [14], the resistance measured equals:

$$R_c = Z\coth(\alpha d) \tag{4.3.2}$$

$$Z = \frac{1}{w}\sqrt{R_{sheet}\rho_{contact}} \tag{4.3.3}$$

$$\alpha = \sqrt{\frac{R_{sheet}}{\rho_{contact}}} \tag{4.3.4}$$

where w is the physical contact width and d is the physical contact length. If $\alpha d \geq 2$, $\coth(\alpha d)$ approaches 1; therefore the measured resistance equals Z, and $\rho_{contact} = R_c^2 \ / \ R_{sheet}$. Therefore, smaller $\rho_{contact}$ terms provide smaller device contact lengths and smaller transistor access resistances. This model assumes the extrapolated sheet resistance is equal in the gap and under the contact. This assumption may be wrong if there is significant depletion underneath the contact, or the contact metal diffuses into the semiconductor. Given the large regrowth doping and relatively thick regrowth, the assumption is valid.

4.4 MBE Source-Drain Regrowth

The MOSFET source-drain regions need to be self-aligned to the device channel to minimize parasitic sheet resistance, must be heavily doped, and should have no intervening barrier that could increase access resistance or choke off source charge. The first iteration of the regrowth process module used MBE. The following sections briefly outline MBE technology, the development of MBE regrowth, and characterization of its material in the MOSFET process.

4.4.1 MBE Overview

Molecular beam epitaxy (MBE) is one crystal growth technique employed in III-V device fabrication. Starting in the 1970s [15], MBE has become one of the most important tools for both characterization of III-V materials and precision fabrication of the substrates used in making semiconductor devices. All of the device

epitaxial material used in this dissertation came from MBE. MBE can use solid-source evaporation, metal-organics, and plasma-based precursors for the growth. This dissertation focuses on solid-source MBE material.

Solid-source MBE systems are composed of a growth chamber fitted with effusion cells containing the source material. The specific orientation of the sample holder and sources depends on the equipment manufacturer. The growth chamber is typically kept at a pressure in 1×10^{-7} to 1×10^{-9} Torr or lower. This is a key feature of MBE; ultra-high vacuum minimizes contamination during epitaxial growth. It also increases the mean free path of the source material (mean free path is inversely proportional to pressure), allowing for greater distance between the source and substrate, which improves sample uniformity. To minimize contamination of the growth chamber, a loading chamber is typically employed. This chamber can be vented independently of the growth chamber to load samples. Samples can also be prepared and treated in high vacuum in this chamber.

During epitaxial growth, the sample is heated to predetermined temperatures optimized for the specific growth. The source effusion cells are heated to evaporate their material, and shuttered to control the composition of the growth. Depending on which sources are open and their temperatures, different compositions of material can be grown. This is important for ternary semiconductors (such as InGaAs and InAlAs) to ensure lattice matched growth. The growth can be monitored with reflection high energy electron diffraction (RHEED) [16]. The electron beam interacts with the crystal structure, allowing interpretation of the growth mechanisms present on the substrate.

4.4.2 MBE "Quasi-MEE" Rerowth

By its nature, solid-source MBE is a line-of-sight process. This is a problem for gate first and gate last MOSFET processing, as the covered gate region prevents the effusion sources from "seeing" the substrate near its edges. Migration-enhanced epitaxy (MEE) [17] allows for smooth, two-dimensional epitaxial growth with increased adatom mobility. By periodically shuttering off the arsenic source, atomic gallium mobility increases significantly. This enhanced adatom mobility ensures smooth epitaxial growth.

During development of the MBE regrowth module, standard MEE was found ineffective [18]. InGaAs regrowth could not fill in near covered gate regions. A modified form of MEE called "Quasi-MEE" [19] keeps the arsenic source shutter open during the entire growth, while periodically opening the indium, gallium, and silicon source shutters. This strategy, combined with a higher substrate temperature than normal MBE, enabled epitaxy near the edge. However, defects were still present in the regrowth, increasing sheet resistance. A transition to InAs regrowth [20] fixed the defect problem; defective InAs is still highly n+ [21], allowing for low sheet resistance source-drain contacts.

4.4.3 MBE TLM Data

Based on the mathematics in the previous section, we can extract a semiconductor sheet resistance ($\Omega/\square$), metal-semiconductor access resistance ($\Omega\cdot\mu m$), and metal-semiconductor contact resistivity ($\Omega\cdot\mu m^2$) for our devices. Table 4.1 is a list of the various regrowth types and their specifics.

InAs, Si Doping, In-Situ: This recipes developed in [19] and [20] are the base-

line for the regrowth module. *In-situ* deposition should provide the lowest contact resistance given little to no oxide can form on the semiconductor surface in vacuum. Molybdenum is used as contact metal since it is refractory, providing a thermally-stable metal contact to the InAs. In the gate first process flow, this *in-situ* evaporation also provides self-aligned metal to the gate, minimizing parasitic sheet resistance.

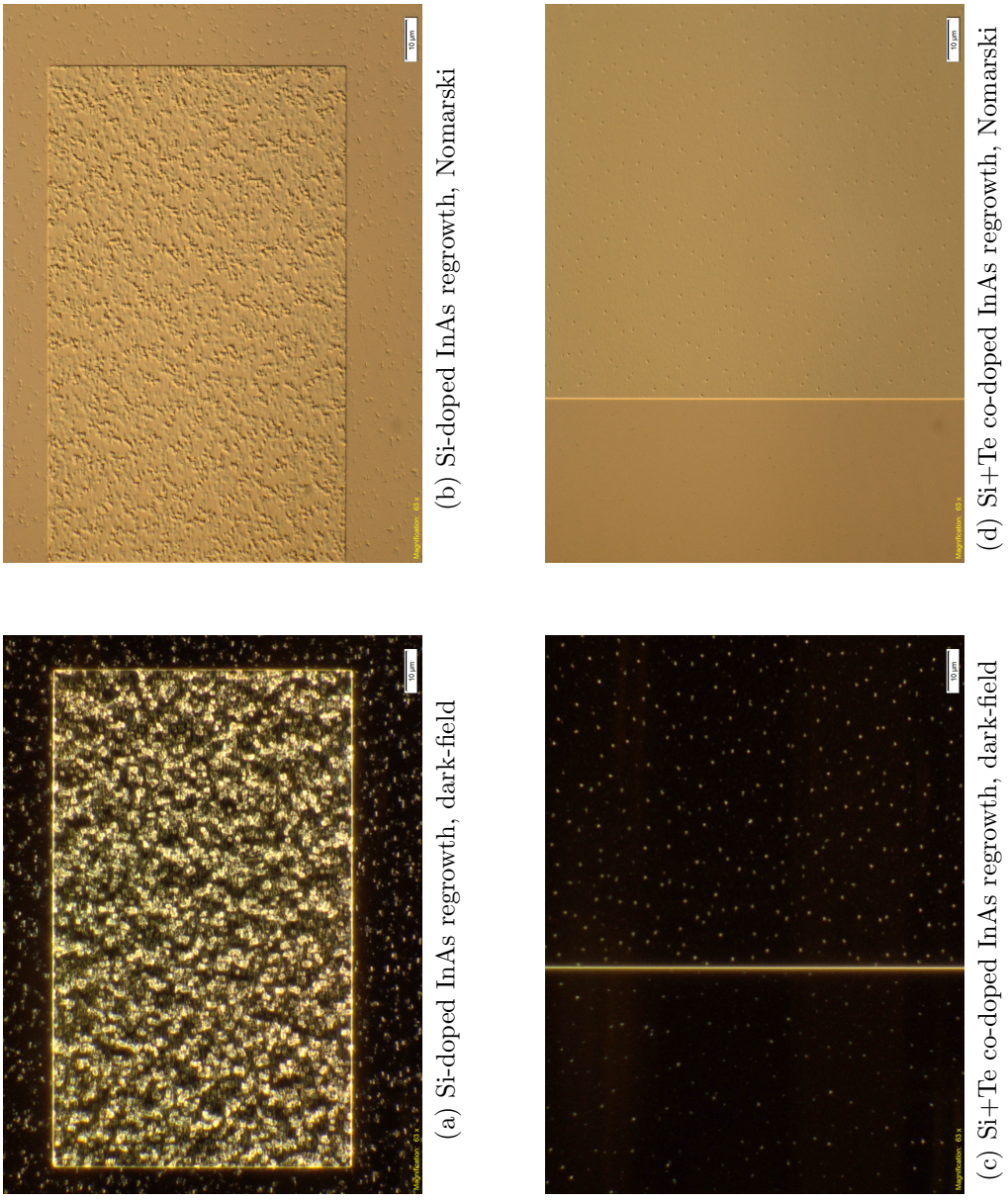
InAs, Si Doping, Ex-Situ: It is well-known that Ti/Pd/Au provides an adequate contact to InAs and InGaAs. However, the Ti readily reacts with the semiconductor; this can cause metal sinking into the semiconductor, potentially increasing resistance or damaging very thin semiconductor layers. However, in our devices, the metal-semiconductor access resistance term ($\sim$ 6 to 15 $\Omega\cdot\mu$m, single-sided), is small compared to the total device on resistance ($\sim$ 200 $\Omega\cdot\mu$m, single-sided). See Figure 4.7a and 4.7b. These are optical microscope images of the regrowth. As see in the electrical data, the visible roughness appears to not affect the sheet resistance of the material.

InAs, Si+Te Doping, Ex-Situ: While silicon-doped InAs provides low sheet and access resistances, gate last devices (Chapter 6) reached a plateau of on-state performance. It was discovered that tellurium could dope InGaAs well [22]. Samples were then fabricated with Si and Te as co-dopants. This tended to lower both the semiconductor sheet resistance and metal-semiconductor access resistance. When Si+Te co-doping was used in FET fabrication, the devices had higher performance and uniformity across the sample. Furthermore, Te appears to be a growth surfactant during MBE regrowth. Surfactant elements in MBE growth help create smoother epitaxial material [23]. See Figure 4.7. Compared to Si-only regrowth, Si+Te co-doping dramatically improves regrowth smoothness.

InGaAs, Si+Te Doping, Ex-Situ: While InAs provides a superior metal- semiconductor access resistance, III-V MOSFETs may be limited in performance by this junction (See Section 6.2.4). It would be better to eliminate the conduction band offset from InAs to InGaAs found on our transistors. Furthermore, lattice-matched epitaxy would provide higher-quality semiconductor material.

Name	**Dopant (cm^{-3})**	**Thickness (nm)**	**Contact Metal**	$\mathbf{R}_{sheet}$ ($\Omega/\square$)	$\mathbf{R}_{Access}$ ($\Omega\cdot\mu m$)	$\rho_{contact}$ ($\Omega\cdot\mu m^2$)	**Ref.**
MBE							
n-InGaAs	Si, $\sim 5\times10^{19}$	$\sim$50	Mo, *In-Situ*	29	12	5.5	[18]
n-InAs	Si, $\sim 4\times10^{19}$	$\sim$50	Mo, *In-Situ*	23	8.5	3.5	[20]
n-InAs (1)	Si, $\sim 5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	21.4	6.5	2	[24]
n-InAs (2)	Si, $\sim 5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	25.3	9.9	3.9	
n-InAs (1)	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	17	4.7	1.29	
n-InAs (2)	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	18.9	6.56	2.2	
n-InAs (3)	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	17.8	10.6	6.32	
n-InAs	Si+Te, $\sim 6\times10^{19}$	$\sim$ 60	Ni/Pd/Au †, *Ex-Situ*	17.8	3.25	0.5	
n-InGaAs	Si+Te, $\sim 5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	43.3	17.7	7.22	
MOCVD							
n-InGaAs (1)	Si, $\sim 4.5\times10^{19}$	$\sim$ 30	Ti/Pd/Au, *Ex-Situ*	41.8	32.44	25.2	
n-InGaAs (2)	Si, $\sim 4.5\times10^{19}$	$\sim$ 30	Ti/Pd/Au, *Ex-Situ*	39.4	16.97	7.29	
n-InGaAs (3)	Si, $\sim 4.5\times10^{19}$	$\sim$ 30	Ti/Pd/Au, *Ex-Situ*	46	19.8	8.5	
n-InGaAs	Si, $\sim 4.5\times10^{19}$	$\sim$ 60	Ti/Pd/Au, *Ex-Situ*	23.5	13.02	7.2	

Table 4.1: Summary of MBE and MOCVD regrowth data. Dopant concentration is active carrier concentration. Electron beam evaporation for metal contacts, unless otherwise noted. † : thermal metal evaporation.



(a) Si-doped InAs regrowth, dark-field

(b) Si-doped InAs regrowth, Nomarski

(c) Si+Te co-doped InAs regrowth, dark-field

(d) Si+Te co-doped InAs regrowth, Nomarski

Figure 4.7: Optical microscope images of InAs regrowth

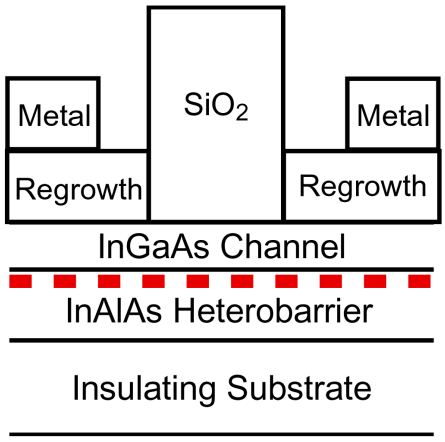


Figure 4.8: QWTLM test structure cartoon schematic

4.4.4 MBE QWTLM Data

Metal-semiconductor TLMs do not capture all of the possible parasitic resistances in the final FET. There is no characterization of the regrowth-channel interface; this is typically analyzed in transistor process flow, eliminating the other known resistances. Early in gate first process development (Chapter 5), devices did not exhibit any channel charge modulation. The regrowth-channel interface needed to be characterized independently from the gate insulator-channel interface. Therefore, the quantum-well TLM (QWTLM) was developed.

Figure 4.8 shows a schematic of a QWTLM. A QWTLM is heavily delta-doped transistor epi design without any gate terminal. All channel charge is provided

Channel Thickness	**Delta Doping**	$\mathbf{R}_{sheet}$ ($\Omega/\square$)	$\mathbf{R}_{Access}$ ($\Omega\cdot\mu$m)
25 nm	2×10^{19} cm^{-3} in 3 nm	538	135
15 nm (1)	3×10^{19} cm^{-3} in 3 nm	893	44
15 nm (2)	3×10^{19} cm^{-3} in 3 nm	960	91
10 nm	3×10^{19} cm^{-3} in 3 nm	2548	—

Table 4.2: QWTLM test structure data

by the delta doping and the assumed surface Fermi level pinning, 0.2eV below the conduction band edge. It is not by chance the QWTLM looks like a transistor; it is imperative the test structure measurements could be applied to actual transistor fabrication.

Table 4.2 lists a series of QWTLM measurement data. In general, the QWTLMs show the regrowth-channel resistance does not explain the lack of device yield in the gate first process flow. The 10 nm channel access resistance is not listed due to y-intercept extrapolation error. Approximately 100 Ω·µm single-sided channel access resistance would not prevent proper device operation. However, these channels are all thicker than 5 nm; there may be regrowth effects for these ultra-thin channels that are not present in these test structures.

4.5 MOCVD Source-Drain Regrowth

MBE source-drain regrowth provides low metal-semiconductor contact resistances using either InAs or InGaAs. However, it can cause serious processing issues. The non-selective nature of the regrowth leaves unwanted semiconductor material on the sample, hindering device dimension scaling. Regrowth material tends to have crystalline defects in it, lowering overall carrier densities in most cases. Finally, experiments were found to be unrepeatable or inconsistent with theory, where all other potential variables had been explored to explain the data. MOCVD-regrown III-V MOSFETs in the literature ([25],[26],[27]) had better performance than the MBE devices; the process flow transitioned to this technology in early 2013.

4.5.1 MOCVD Overview

Rather than solid-source evaporation in MBE, metal-organic chemical vapor deposition (MOCVD) is primarily a gas-phase process. MOCVD has been successfully used in semiconductor regrowth for solid-state laser cladding regions [9], where the final device requires active and passive regions in close proximity. III-V transistor research groups have also used MOCVD for source-drain regrowth ([25],[26],[27]). The former result was strong motivation to pursue MOCVD.

4.5.2 MOCVD TLM Data

Table 4.1 lists MOCVD TLM data taken from FET samples. While the sheet resistance and contact resistivities are higher for MOCVD, their contribution to the parasitic access resistance does not currently limit device performance. However, as MOSFETs continue to increase in drive current and transconductance, their contribution will become important.

4.6 Conclusions

Both MBE and MOCVD are capable of providing epitaxial regrowth for semiconductor devices. While MBE can provide ultra-low metal-semiconductor access resistances and sheet resistances, it tends to limit performance in the devices analyzed in this dissertation. MOCVD regrowth is a promising technology for MOSFET source-drain regions; with more research, it will likely reach the low parasitic resistances found in MBE regrowth, without the processing problems associated with non-selective MBE regrowth.

References

[1] CY Ting. Silicide for contacts and interconnects. In *Electron Devices Meeting, 1984 International*, volume 30, pages 110–113. IEEE, 1984.

[2] Kazuya Ohuchi, Naoki Kusunoki, and Fumitomo Matsuoka. Accurate Measurement of Silicide Specific Contact Resistivity by Cross Bridge Kelvin Resistor for 28 nm Complementary Metal–Oxide–Semiconductor Technology and Beyond. *Japanese Journal of Applied Physics*, 50(4):04DA03–1–6, 2011.

[3] Deal MD Plummer, JD and Griffin PB. *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*. Prentice Hall, 2000.

[4] B Mizuno, I Nakayama, M Takase, H Nakaoka, and M Kubota. Plasma doping for silicon. *Surface and Coatings Technology*, 85(1):51–55, 1996.

[5] RT Young, CW White, GJ Clark, J Narayan, WH Christie, M Murakami, PW King, and SD Kramer. Laser annealing of boron-implanted silicon. *Applied Physics Letters*, 32(3):139–141, 1978.

[6] Dae-Hyun Kim and Jesús A Del Alamo. 30-nm InAs PHEMTs with f_τ= 644 GHz and f_{max}= 681 GHz. *IEEE Electron Device Letters*, 31(8):806, 2010.

[7] K Cheng, A Khakifirooz, P Kulkarni, S Ponoth, J Kuss, LF Edge, A Kimball, S Kanakasabapathy, S Schmitz, A Reznicek, et al. Extremely thin SOI (ETSOI) technology: Past, present, and future. In *SOI Conference (SOI), 2010 IEEE International*, pages 1–4. IEEE, 2010.

[8] Mark Rodder and D Yeakley. Raised source/drain MOSFET with dual sidewall spacers. *Electron Device Letters, IEEE*, 12(3):89–91, 1991.

[9] John S Parker, Ashish Bhardwaj, Pietro RA Binetti, Yung-Jr Hung, and Larry A Coldren. Monolithically integrated gain-flattened ring mode-locked laser for comb-line generation. *Photonics Technology Letters, IEEE*, 24(2):131–133, 2012.

[10] SangHyeon Kim, Masafumi Yokoyama, Noriyuki Taoka, Ryo Iida, Sunghoon Lee, Ryosho Nakane, Yuji Urabe, Noriyuki Miyata, Tetsuji Yasuda, Hisashi Yamada, et al. Self-Aligned Metal Source/Drain InxGa1-xAs n-Metal–Oxide–Semiconductor Field-Effect Transistors Using Ni-InGaAs Alloy. *Applied physics express*, 4(2):4201, 2011.

[11] R Oxland, SW Chang, Xu Li, SW Wang, G Radhakrishnan, W Priyantha, MJH van Dal, CH Hsieh, G Vellianitis, G Doornbos, et al. An ultralow-resistance

ultrashallow metallic source/drain contact scheme for III-V NMOS. *Electron Device Letters, IEEE*, 33(4):501–503, 2012.

[12] Ashish K Baraskar, Mark A Wistey, Vibhor Jain, Uttam Singisetti, Greg Burek, Brian J Thibeault, Yong Ju Lee, Arthur C Gossard, and Mark JW Rodwell. Ultralow resistance, nonalloyed Ohmic contacts to¡ equation¿ n-InGaAs. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 27(4):2036–2039, 2009.

[13] AK Baraskar. *Development of Ultra-Low Resistance Ohmic Contacts for InGaAs/InP HBTs*. PhD thesis, UC Santa Barbara, 2011.

[14] HH Berger. Models for contacts to planar devices. *Solid-State Electronics*, 15(2):145–158, 1972.

[15] CT Foxon. Three decades of molecular beam epitaxy. *Journal of Crystal Growth*, 251(1):1–8, 2003.

[16] AY Cho. Film deposition by molecular-beam techniques. *Journal of Vacuum Science and Technology*, 8(5):S31–S38, 1971.

[17] Yoshiji Horikoshi, Minoru Kawashima, and Hiroshi Yamaguchi. Low-temperature growth of GaAs and AlAs-GaAs quantum-well layers by modified molecular beam epitaxy. *Japanese Journal of Applied Physics*, 25:L868–L870, 1986.

[18] U Singisetti. *$In_{0.53}Ga_{0.47}As$ MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth*. PhD thesis, UC Santa Barbara, 2009.

[19] G. J. Burek B. Thibeault J. Cagnon S. Stemmer S. R. Bank Y. Sun E. J. Kiewra D. K. Sadana A. C. Gossard M. A. Wistey, U. Singisetti and M. J. W. Rodwell. Regrowth of self-aligned, ultra low resistance ohmic contacts on InGaAs . In *Proc. 15th Int. Conf. Mol. Beam Epitaxy*, 2008.

[20] Uttam Singisetti, Mark A Wistey, Gregory J Burek, Ashish K Baraskar, Brian J Thibeault, Arthur C Gossard, Mark JW Rodwell, Byungha Shin, Eun J Kim, Paul C McIntyre, et al. $In_{0.53}Ga_{0.47}As$ Channel MOSFETs With Self-Aligned InAs Source/Drain Formed by MEE Regrowth. *Electron Device Letters, IEEE*, 30(11):1128–1130, 2009.

[21] S Bhargava, H-R Blank, V Narayanamurti, and H Kroemer. Fermi-level pinning position at the Au–InAs interface determined using ballistic electron emission microscopy. *Applied Physics Letters*, 70(6):759–761, 1997.

[22] Carter AD Lee S Huang C-Y Lu H Rodwell MJW Gossard AC Law, JJM. Co-doping of $In_xGa_{1-x}As$ As with silicon and tellurium for improved ultra-low contact resistance. *Journal of Crystal Growth*, 2013.

[23] M Copel, MC Reuter, Efthimios Kaxiras, and RM Tromp. Surfactants in epitaxial growth. *Physical review letters*, 63(6):632–635, 1989.

[24] Andrew D Carter, JJM Law, E Lobisser, GJ Burek, WJ Mitchell, BJ Thibeault, AC Gossard, and MJW Rodwell. 60 nm gate length Al_2O_3 / $In_{0.53}Ga_{0.47}As$ gate-first MOSFETs using InAs raised source-drain regrowth. In *Device Research Conference (DRC), 2011 69th Annual*, pages 19–20. IEEE, 2011.

[25] Ryousuke Terao, Toru Kanazawa, Shunsuke Ikeda, Yoshiharu Yonai, Atsushi Kato, and Yasuyuki Miyamoto. InP/InGaAs Composite Metal–Oxide–Semiconductor Field-Effect Transistors with Regrown Source and Al2O3 Gate Dielectric Exhibiting Maximum Drain Current Exceeding 1.3 mA/μm. *Applied physics express*, 4(5):4201, 2011.

[26] Mikael Egard, Lars Ohlsson, B Mattias Borg, L-E Wernersson, and Erik Lind. Self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ As MOSFET with selectively regrown source and drain contact layers. In *Device Research Conference (DRC), 2011 69th Annual*, pages 1–2. IEEE, 2011.

[27] M Egard, L Ohlsson, BM Borg, F Lenrick, R Wallenberg, L-E Wernersson, and E Lind. High transconductance self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 13–2. IEEE, 2011.

Chapter 5

Gate First MOSFET: Process and Results

As outlined in Chapter 2, III-V MOSFETs require short gate lengths, thin dielectrics, and self-aligned heavily-doped source drain regions. A process flow depositing gate metal first and employing MBE regrowth was developed over the course of three years at UC Santa Barbara. This process was scaled to 60 nm gate length devices showing drive currents in excess of 1 mA/micron at high V_{ds} and approximately 0.3 mS/micron at 1 V V_{ds}. This chapter outlines the gate first process flow, analysis of the transistor data, and the intrinsic process scaling issues.

5.1 Overview: Gate First MOSFETs

III-V MOS devices are sensitive to surface passivation. Research groups have attempted to passivate GaAs [1] and InGaAs [2]-based MOSFETs. Unlike their HEMT counterparts, the insulator-channel interface of a III-V MOSFET is not free from electrically-active surface traps. This underpins the design of a gate first MOSFET. One must protect the as-grown III-V surface from any oxidation, which would increase the interface trap density. Extensive work has been done to protect

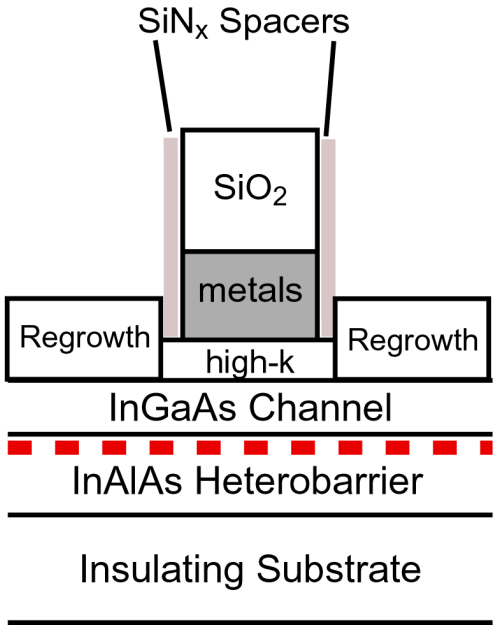


Figure 5.1: Gate First MOSFET cartoon schematic.

the as-grown interface from corruption (See Chapter 3). Also, transistors must have scaled gate lengths for peak performance at DC (g_m, J_{drain}) and AC (capacitances); for short gate lengths, the device design must minimize short channel effects, requiring thin transistor channels. Excessive oxidation of the semiconductor during a vacuum break could render most of the channel inactive, changing intended device design.

Devices from this process flow from earlier work [3] saw 200 nm gate length, enhancement-mode operation, and reasonable pinch-off characteristics. For the 200 nm gate length device at 5 nm Al_2O_3 gate insulators, peak currents were 0.6 mA/micron at $\sim$ 3 V above threshold at 1 V V_{ds} 1.3 V threshold, linear extraction), peak transconductance of 0.4 mS/micron at 1 V V_{ds}, and subthreshold swing of 500 mV/decade at 0.1 V V_{ds}. Given 5 nm of Al_2O_3, Eqn. 2.2.5 of Chapter 2, predicts an interface trap density of $\sim 7{\times}10^{13}$ $cm^{-2}eV^{-1}$.

Region	Material Type	Thickness
Channel	InGaAs, not doped	5 to 15 nm
Delta Doping	InAlAs, Si-doped (variable)	3 nm
Heterobarrioer	InAlAs	200 to 400 nm
Semi-insulating Substr.	InP, Fe-doped	500 μm

Table 5.1: MOSFET Epitaxial Design

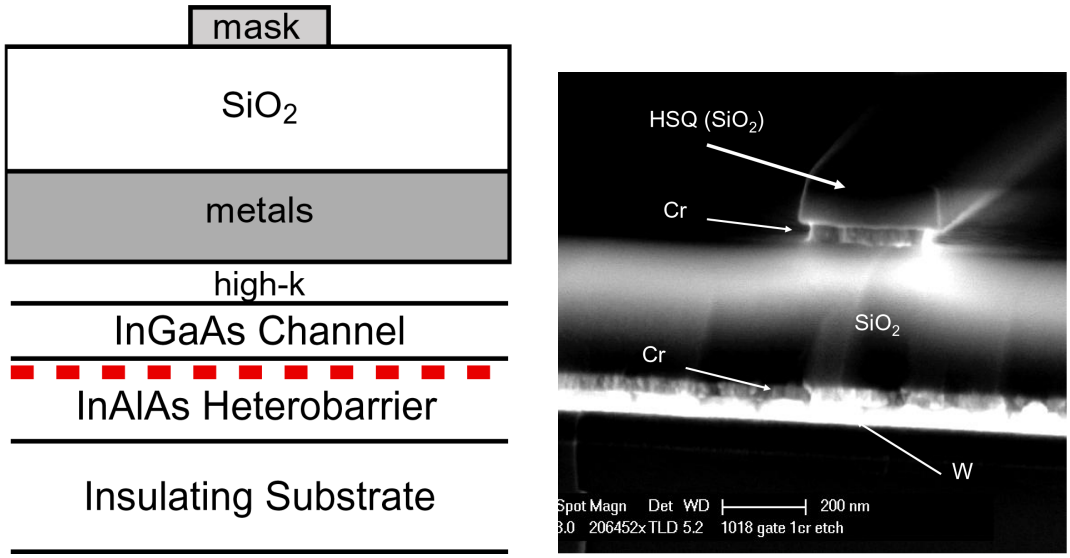
Continuing with that process flow, it is necessary to see if device performance can be improved at a scaled gate length. The process can scale to sub-100 nm metallurgical gate length with modest process changes.

5.2 Gate-First MOSFET Process Flow

The wafer epitaxial design for the gate first process can be found in Table 5.1. Semi-insulating InP and undoped InAlAs are used to minimize device-to-device leakage; delta-doping below the channel is for controlling threshold voltage and ensuring channel charge below the ungated sidewall spacers. The lattice-matched InGaAs channel offers low effective mass electrons for high device current densities.

Original processing used solid arsenic caps [4] to maintain an unexposed InGaAs channel. Solid arsenic cap MOSCAP fabrication shows excellent CV dispersion, consistent with the hypothesis that air exposure corrupts the MOSCAP surface. Arsenic caps can be desorbed at 460°C and 1 Torr [4]. Immediately after desorption, gate insulator is deposited. It can be deposited either in an ALD chamber [4], or a modified MBE chamber for chemical beam deposition [5]. The original gate first process used ALD desorption and Al_2O_3, while the sub-100 nm processing used cyclic H_2/TMA treatment without arsenic capping [6].

As soon as possible after dielectric deposition, to minimize subcutaneous oxi-



(a) Gate First: Gate stack cartoon

(b) Gate First: SEM of gate stack

Figure 5.2: Gate First: Gate stack and etching experiment

dation of the Al_2O_3-InGaAs interface, the gate stack is deposited on the sample (Figure 5.2a). Gate metal is sputtered tungsten. Tungsten is chosen for its high-temperature stability and ease of dry etching in low-power SF_6-Ar chemistries. Low power (10W ICP power) is necessary in order to avoid damaging the thin high-k and channel below the gate metal. Next, electron beam evaporated chromium is deposited. Chromium is an excellent etch stop for SF_6-Ar chemistry, and is itself etched in low power Cl_2/O_2 chemistries. Next, plasma enhanced chemical vapor deposition $SiO_x$is deposited on the sample. This layer is thicker than others to assist in photoresist planarization [7] later in the process flow. Last, another layer of chromium is deposited on the sample to serve as a dry etch hard mask during gate stack dry etching.

To achieve sub-100 nm gate lengths, electron beam lithography (EBL) is chosen. Using hydrogen silsesquioxane (HSQ) resist, one can achieve $\sim$ 20 nm patterns.

Upon exposure and development, HSQ turns into essentially SiO_x, serving immediately as a hard mask for subsequent processing. HSQ is also used in our process for "mix-and-match" lithography. "Mix-and-match" lithography uses EBL for fine features and photolithography for large features.

The combined EBL/optical lithography patterns are dry etched in an inductively coupled plasma reactive ion etch (ICP-RIE), patterning the chromium into gate lengths ranging from 50 nm to 1 micron. A brief O_2 plasma descum is after dry etching to minimize polymerized photoresist debris from accumulating on the sample. As Figure 5.2b shows, the Cr is undercut, leaving the Cr gate length smaller than written by HSQ. After photoresist stripping in solvents, the $SiO_x$is dry etched in SF_6/Ar, the chromium gate metal in Cl_2/O_2, and the tungsten gate metal in SF_6/Ar. For sub-100 nm gate lengths, the SiO_xetch power was increased to achieve a more vertical structure, maintaining the small gate length. Also, undercutting in the chromium and tungsten gate metal layers can decrease the final gate length, at the risk of lower yield.

Since the source-drain regrowth is self-aligned to the gate metal, a sidewall spacer is required to prevent source-drain-gate short circuits. PECVD Si_xN_y is chosen for its conformal deposition and low leakage current. After Si_xN_y is deposited, it is dry etched in CF_4/O_2. Since the gate stack is highly vertical and the Si_xN_y is conformal, the dry etch removes Si_xN_y in the field and at the top of the gate, while not etching most of the Si_xN_y on the gate stack.

Al_2O_3 gate dielectric is still present on the surface of the sample; it must be etched away prior to source-drain regrowth. Al_2O_3 is easily etched in photoresist developer (AZ400K). The developer does not etch other layers of the gate stack. After oxide removal, the semiconductor surface is exposed to ultraviolet (UV) O_3.

O_3 creates a favorable native oxide on InGaAs, restoring stoichiometry to the surface [8]. This surface oxide is etched in dilute HCl immediately before loading the sample in the MBE loadlock.

Inside the MBE chamber, the InGaAs surface is prepared for epitaxy. After loading into the buffer chamber, the samples are baked at 200°C overnight. The temperature is then raised to 325°C. An atomic hydrogen surface clean is done at 420°C to remove more surface oxides in an UHV environment. After letting the sample cool down and buffer chamber pressure stabilize, the sample is loaded into the growth chamber. RHEED is used to confirm a crystalline surface prior to regrowth.

The quasi-MEE [9] technique produces relaxed InAs source-drain regions that come up to the edges of the Si_xN_y-encapsulated gate stack. Since the InAs lattice constant (0.60583 nm) is significantly different from InGaAs/InP (0.58687 nm),[10] and since the layer is thicker than the critical thickness [11], the InAs will relax on the substrate. However, relaxed InAs is highly conductive [12], and therefore does not pose an issue for source-drain sheet resistance.

After regrowth, there is an option for *in-situ* metal deposition in an adjacent electron beam evaporator. *In-situ* metal contacts to n- and p-type material have some of the lowest metal-semiconductor contact resistances [13]. Molybdenum is evaporated over the entire sample.

Since the InAs regrowth is non-selective, it can grow on all surfaces of the gate stack. Also, the *in-situ* Mo evaporation could create a source-to-drain short. To remove the InAs and Mo, photoresist planarization is used [7]. By accounting for the height of the gate stack, proper photoresist thickness, and remote oxygen plasma, material can be removed from the top of narrow features. Given 1 micron resist

and 350 nm tall structures, 1 micron gate lengths and lower can be successfully planarized. After planarization, wet or dry etching can remove material from the top of the gate stack.

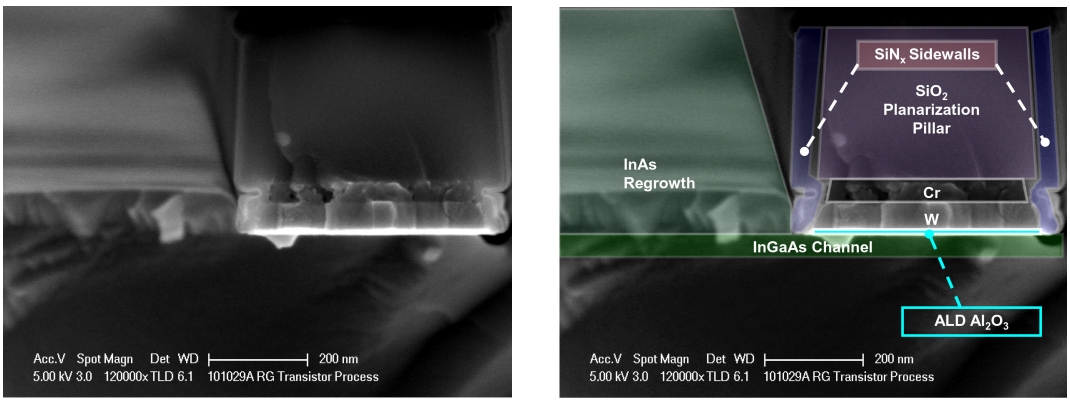
Devices must be isolated from one another to prevent device-device short circuits and source-to-drain short circuits. After photoresist patterning, the semiconductor can be etched in H_3PO_4:H_2O_2:DI. If *in-situ* Mo was used, it can also be etched in this solution, or dry-etched in SF_6/Ar if undercut is a concern.

Low-resistance source-drain metal must contact either the InAs or the *in-situ* Mo. The metal must be thick and of a low resistivity to prevent large end-resistances from obscuring the intrinsic device performance. Typically, Ti/Pd/Au stacks are used when metal-semiconductor sinking is not an issue. Ti/Pd/Au makes excellent *ex-situ* contact to InGaAs and InAs (See Chapter 4).

The final step in the process is gate pad opening. The gate pad is buried in PECVD SiO_x; buffered HF will remove this and the device can be electrically probed.

5.3 Gate First: Device Results

Multiple samples in this process flow failed to have any transistor performance. Analysis of QWTLMs (see Chapter 4) proved 10 nm InGaAs channels to be feasible. This section details select process lots from the gate first process, examining common-source characteristics, device on-state performance, and extrapolation of access resistance. Figure 5.3 is a cross-section SEM of a MOSFET and a colorized version for region identification.



(a) SEM cross-section (b) Colorized version

Figure 5.3: Gate First MOSFET SEM cross-section

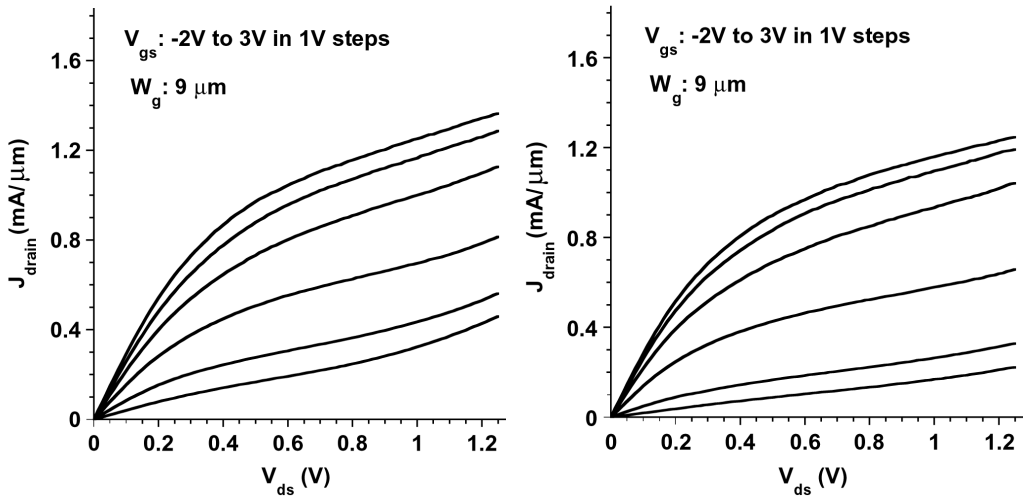
Gate First A1			
Channel Thickness	10 nm	Oxide Type	Al_2O_3
Delta doping	3 nm, 9×10^{12} cm^{-2}	Oxide Thickness	5 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	110302D	Regrowth Doping	Si

Table 5.2: Gate First Lot A1 Process Specifications

5.3.1 Gate First Lot A1: Depletion-Mode MOSFET

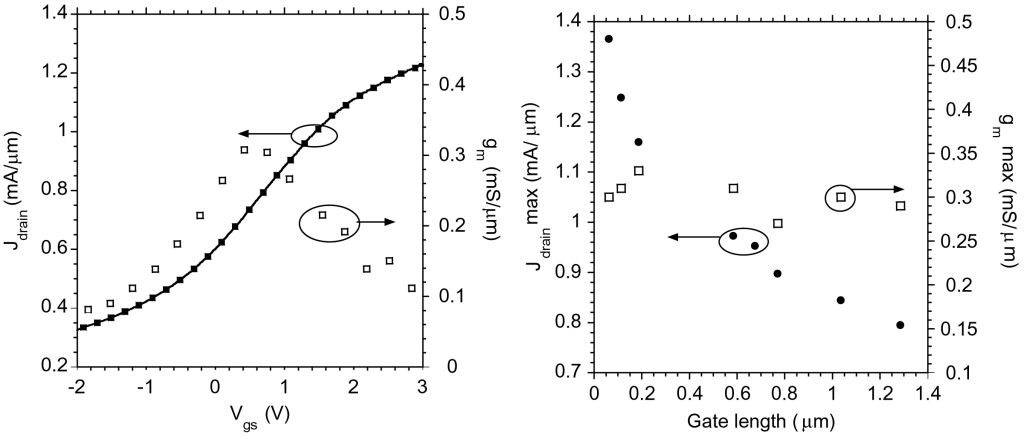
Figure 5.6 is a TEM cross-section of a finished 60 nm gate length gate first MOSFET from Lot A1. The source/drain epitaxial regrowth fills in to the Si_xN_ysidewall. The gate metals are vertical and slightly undercut from the SiO_xmasking. Apparent regrowth "sinking" is present near the source-drain-Si_xN_yinterface. This process flow is focused on raised source-drain regrowth; this sinking is not intentional, and is an unexplained byproduct of the MBE regrowth process. Sinking only occurs near gate edges. Figure 5.7 shows STEM imaging of a similarly processed sample and EDX analysis shows no gallium where there should be for an InGaAs channel.

Figure 5.4 shows the J_{drain}-V_{ds} plots for the 60 nm and 115 nm gate length devices. Figure 5.5a is the J_d-V_{gs} plot for the 60 nm gate length device. The 60 nm



(a) 60 nm J_d-V_{ds} (b) 115 nm J_d-V_{ds}

Figure 5.4: Lot A1: J_d-V_{ds}



(a) 60 nm J_d-V_{gs} (b) J_{max} and g_m versus L_g

Figure 5.5: Lot A1: J_d-V_{gs}

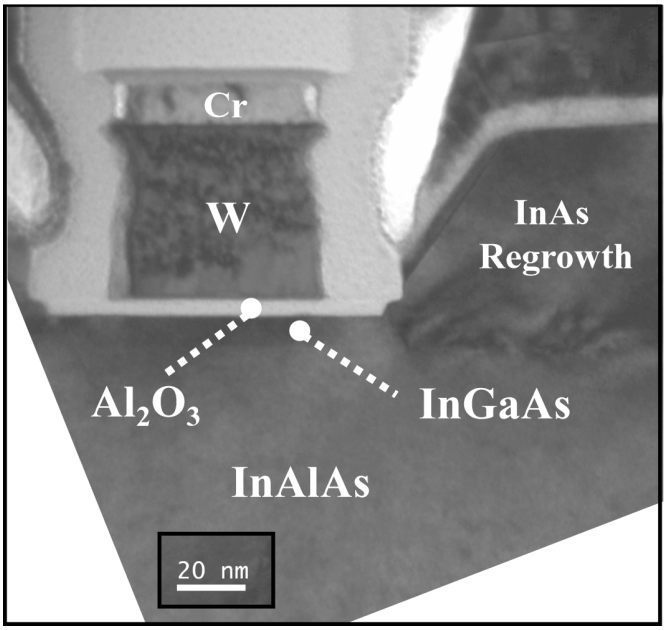


Figure 5.6: Lot A1: 60 nm gate length TEM

device shows high on-current (1.37 mA/micron) and a low on-resistance (341 Ω·µm). However, the 60 nm transconductance (0.3 mS/micron) is no better than the 500 nm gate length transconductance. Figure 5.5b shows the drain current (at V_{ds}= 1.25 V, V_{gs}= 3V) and peak transconductance (at V_{ds}= 1V) for all gate lengths. The low performance could be indicative of the thickness of the InGaAs channel (10 nm compared to 5 in [3]), or the heavy delta doping forcing the wave function to the back of the quantum well. However, the insensitivity of transconductance to gate length does not support this theory.

Long gate length devices on this sample could not be brought into subthreshold, preventing subthreshold swing and DIBL measurements. This may be due to the large delta doping in the device creating a parasitic resistance underneath the channel. It could also be due to large interface trap density at the Al_2O_3-InGaAs

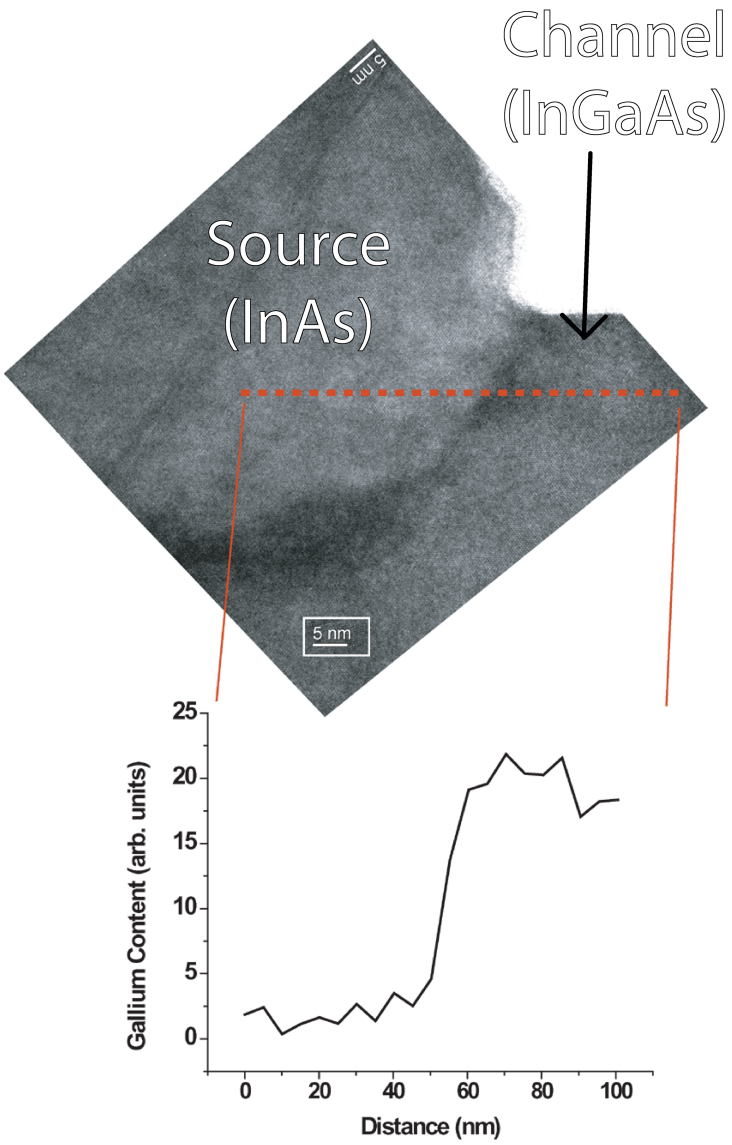


Figure 5.7: Lot A1: Gate First FET STEM near source/drain, EDX inset

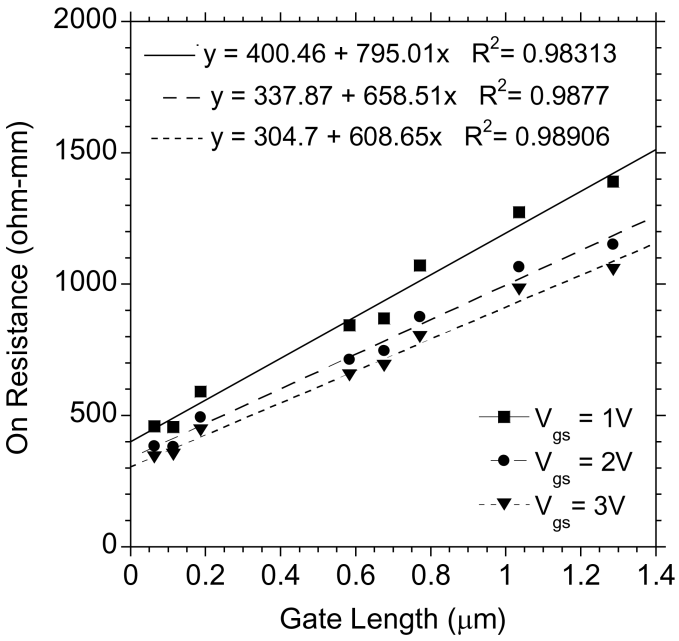


Figure 5.8: Lot A1: R_{on}versus L_g

interface.

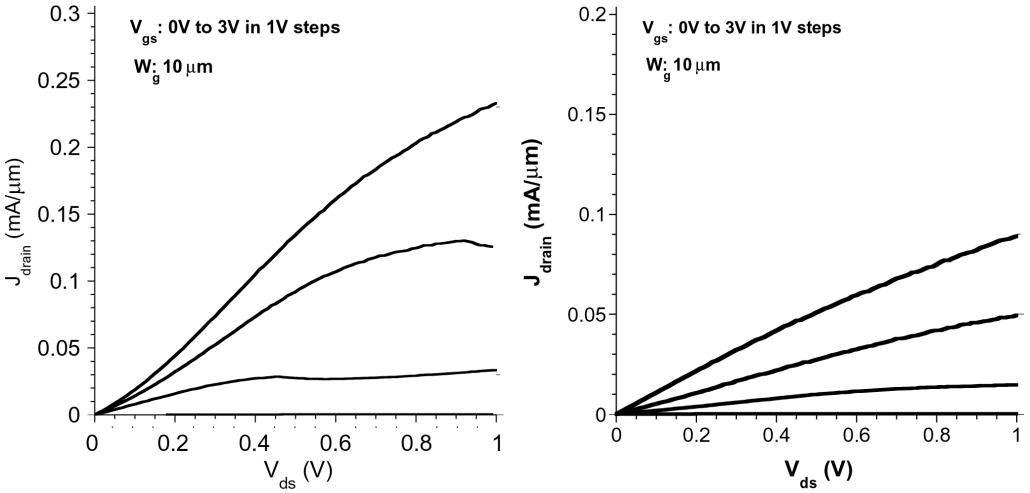
Figure 5.8 shows R_{on} versus gate length for Lot A1. The extrapolated end resistance is higher than found in QWTLM structures (Chapter 4). This could be due to the difference in quantum well thickness; Lot A1 is 10 nm InGaAs, while the QWTLMs are 15 nm and thicker. However, the access resistance high enough to explain the low peak transconductance. Gate leakage currents were less than 20 nA / micron for all devices measured.

5.3.2 Gate First Lot A2: Enhancement-Mode MOSFET

Figure 5.9 and 5.10 are the J_{drain}-V_{ds} and J_{drain}-V_{gs} plots for the 0.3, 0.7, and 1.4 micron gate length devices in Lot A2. The apparent negative resistance in the J_d-V_{ds} plots is due to poor impedance termination of the DC bias probes, leading to instabilities during measurement. Figure 5.11 is the R_{on} versus gate length

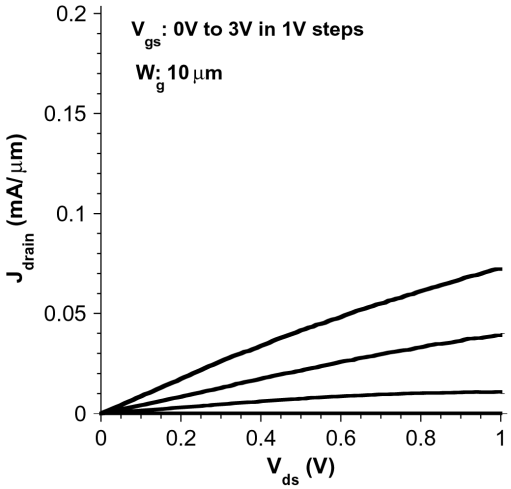
Gate First A2			
Channel Thickness	10 nm	Oxide Type	Al_2O_3
Delta doping	3 nm, 3×10^{12} cm^{-2}	Oxide Thickness	5 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	110128B	Regrowth Doping	Si

Table 5.3: Gate First Lot A2 Process Specifications



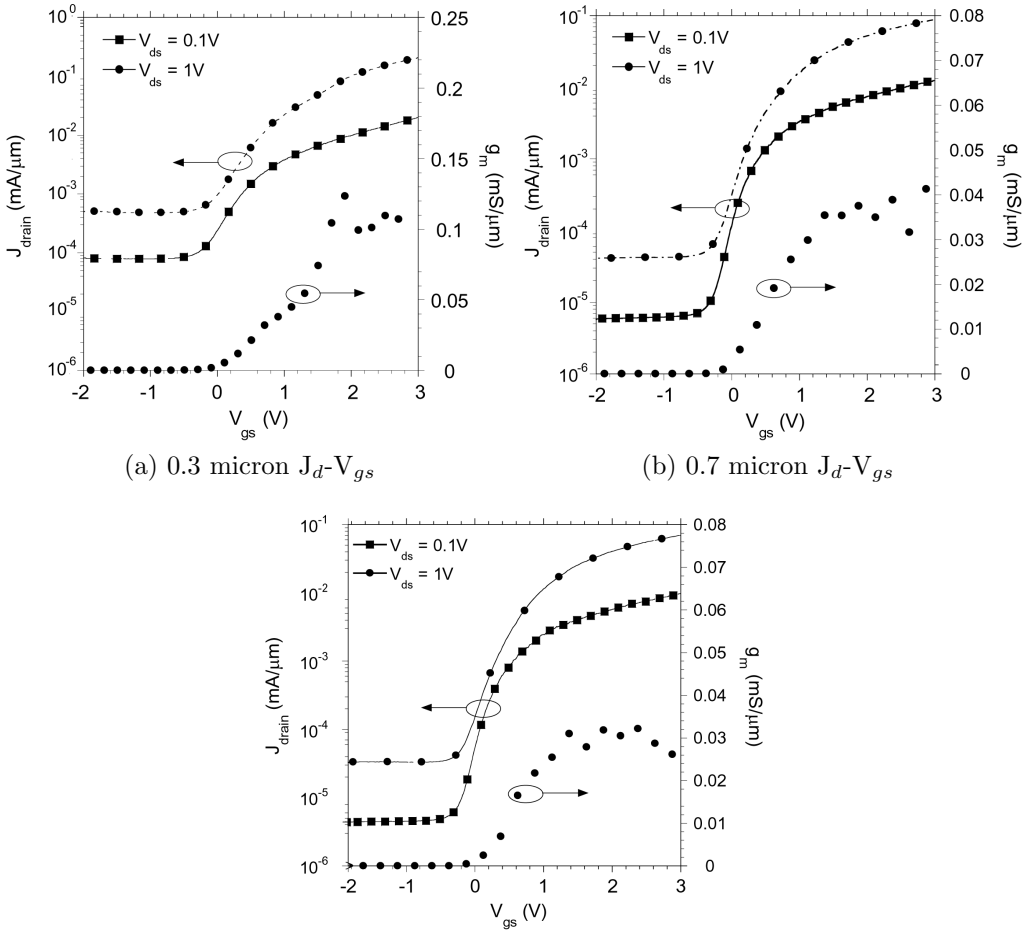
(a) 0.3 micron J_d-V_{ds}

(b) 0.7 micron J_d-V_{ds}



(c) 1.4 micron J_d-V_{ds}

Figure 5.9: Lot A2: J_d-V_{ds}



(a) 0.3 micron J_d-V_{gs}

(b) 0.7 micron J_d-V_{gs}

(c) 1.4 micron J_d-V_{gs}

Figure 5.10: Lot A2: J_d-V_{gs}

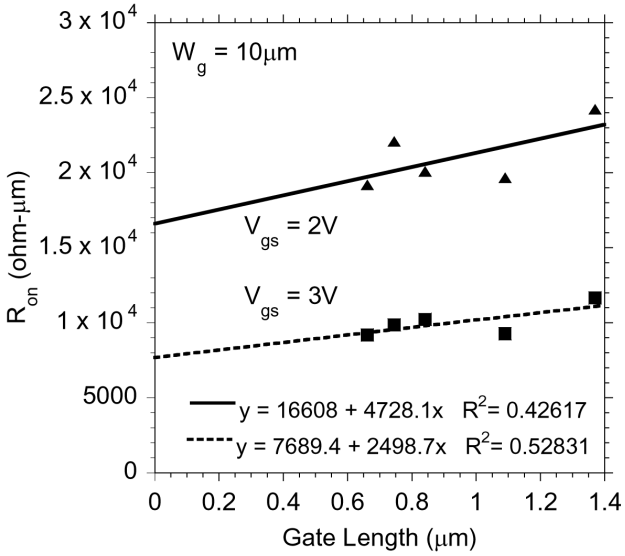


Figure 5.11: Lot A2: R_{on}versus L_g

plot for Lot A2. The lower concentration delta doping removes induced mobile charge from the channel, increasing the threshold voltage. This lot has a lower peak transconductance, reaching 0.1 mS/micron for the 300 nm gate length device. Sub-100 nm gate lengths were not available on this lot. Comparing Figures 5.8 and 5.11, the lower concentration delta doping dramatically increased the device access resistance. This could be due to channel depletion under the ungated sidewall region.

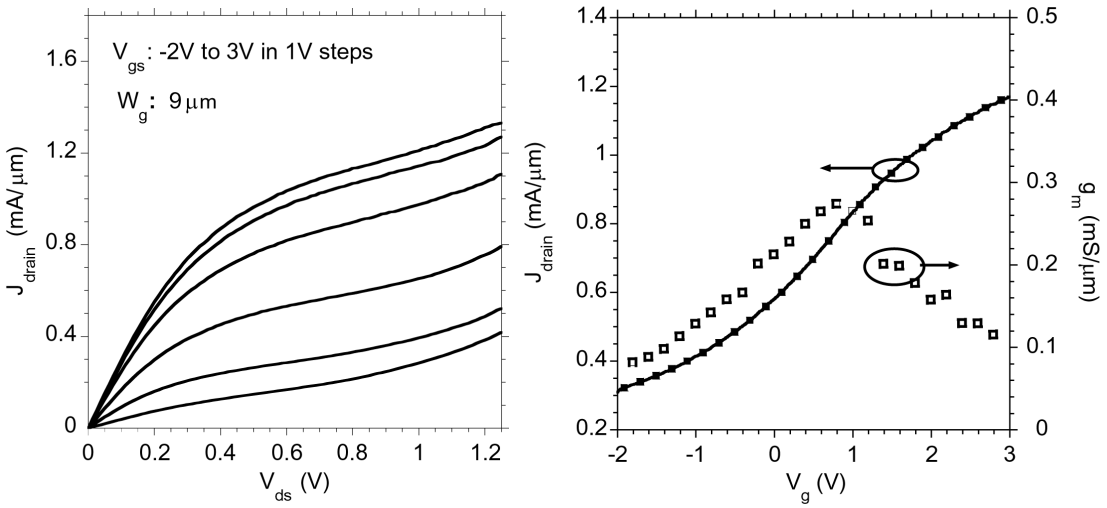
5.3.3 Gate First Lot A3: Depletion-Mode MOSFET with ALD Sidewalls

The ungated sidewall spacer and delta doping likely control channel access resistance; this ungated region must be minimized. However, PECVD Si_xN_ycannot be scaled indefinitely, due to its low porosity which increases gate leakage current.

Figure 5.12 contains the J_{drain}-V_{ds} and J_{drain}-V_{gs} plots for the 80 nm gate length

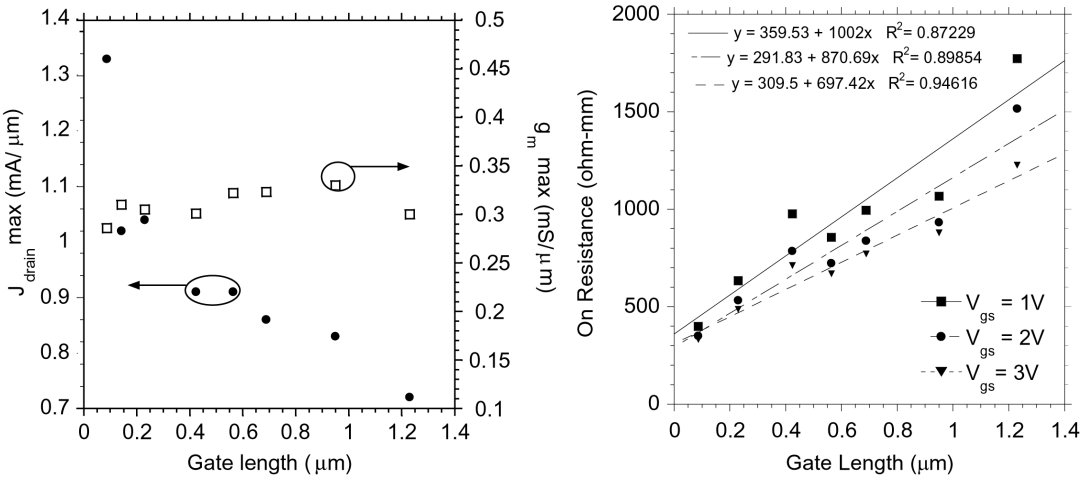
Gate First A3			
Channel Thickness	10 nm	Oxide Type	Al_2O_3
Delta doping	3 nm, 9×10^{12} cm^{-2}	Oxide Thickness	5 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	110302F	Regrowth Doping	Si

Table 5.4: Gate First Lot A3 Process Specifications



(a) 80 nm J_d-V_{ds} (b) 80 nm J_d-V_{gs}

Figure 5.12: Lot A3: 80 nm FET J_d-V_{ds} and J_d-V_{gs}



(a) A3: g_m and j_{max} versus l_g (b) A3: R_{on}versus l_g

Figure 5.13: Lot A3: g_m, j_{max}, R_{on}versus gate length

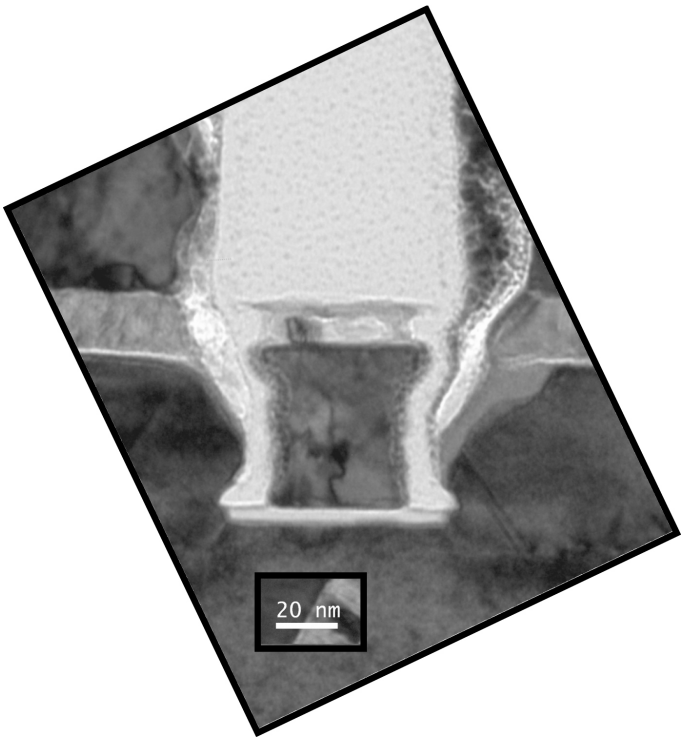


Figure 5.14: Lot A3: 40 nm gate length TEM

devices in Lot A3. Figure 5.13 shows the g_m, J_{max}, and R_{on}versus gate length plots for Lot A3. Compared to Figure 5.5b, the ALD sidewall appears to not affect the peak performance of the transistors. Figure 5.14 shows a TEM of a 40 nm gate length device in Lot A3; the uncontrolled gate metal recess shadows the sidewall from vertical etching. Even though the sidewall was $\sim 50\%$ thinner, in process the "foot" is the same thickness. The uncontrolled nature of the gate undercut puts serious process limits on shrinking the sidewall spacer thickness.

5.4 Gate First: Discussion

Initial sub-100 nm gate first results were no better in terms of transconductance for longer gate lengths in the same lot or enhancement mode results in previous lots.

There are a few likely explanations for the lack of performance scaling:

MOSCAP Damage Study: MOSCAPs were fabricated with 5 nm of $Al_2O_3$and either a) thermally evaporated nickel or b) sputtered tungsten. See Chapter/Section 3.6. When Ni/Al_2O_3 is not annealed, large threshold frequency dispersion is prevent, but the negative gate bias false inversion peaks are low. When W/Al_2O_3 is not annealed, the negative gate bias false inversion peaks increase. Furthermore, after 500°C annealing to simulate regrowth, the false inversion response gets worse. This is a concern for the gate first process using tungsten gate metal. Unfortunately, refractory metals are required for MBE regrowth. In an extensive study [7], it was found that thermal gate metals had the best false inversion response. Experiments with electron-beam evaporated tungsten would help determine the specific process issue.

Sidewall Spacer Channel Depletion: The gate first process requires sidewall spacers to prevent source-drain-gate shorting during regrowth. This sidewall, typically 20 nm thick, creates an ungated region in the device. In silicon MOSFET processing, this region is heavily doped to prevent an increase in FET access resistance, or if too lightly doped, a current choke. In the gate first process, back-barrier delta doping is used to overcome this bottle neck. However, this delta doping must be large in order to have proper device operation, as seen in Lots A1 and A2. Making this region smaller will help, but due to process constraints (see Lot A3), that would be difficult.

Surface Fermi Level Position: Delta doping of the back barrier poses multiple problems for reaching maximum device performance. Large delta doping pushes the channel wavefunction to the back of the channel, in essence, creating a buried channel device. This decreases C_{depth}, decreasing overall device performance (see

Chapter 2). The delta doping also affects the threshold voltage of the device. As the device is taken into subthreshold, the surface Fermi level depends on the delta doping level; large delta-doping requires the Fermi level to be close to mid-gap. As shown in Chapter 3, the interface trap density increases towards mid-bandgap. Therefore, during subthreshold operation of the transistor, the surface Fermi level of the device may be aligned with a large interface trap distribution, increasing the subthreshold swing of the device. Last, the large delta doping seems to increase the device's off-state leakage current, preventing the device from reaching the proper I_{on}/I_{off} ratios for modern VLSI technology.

Overall, the gate first process limits design choices for the FET. Along with poor performance when the delta doping is lowered, the device's gate oxide must be deposited before any subsequent process steps. For other high-k insulators, like HfO_2, it is difficult to remove the oxide after high-temperature deposition without significant substrate damage. In the case of a III-V MOSFET, the processing involved would likely ruin the source-drain channel regions, making regrowth impossible.

5.5 Gate First: Conclusions

The gate first process flow is intended to protect the insulator-InGaAs surface from oxidation causing a large interface trap density. However, the processing involved ends up removing all benefits predicted. Moreover, the process does not scale to improve device performance. Therefore, the process development moved towards a gate last solution to III-V MOSFET fabrication. In gate last, the gate dielectric and metal are one of the last steps in the process flow. As long as the insulator-InGaAs surface can be restored to an effectively un-oxidized state, we can have the benefits

of gate first with increased process flexibility.

References

[1] Matthias Passlack. Development methodology for high-κ gate dielectrics on III–V semiconductors: $Gd_xGa_{0.4-x}O_{0.6}/Ga_2O_3$ dielectric stacks on GaAs. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 23(4):1773–1781, 2005.

[2] YQ Wu, M Xu, RS Wang, O Koybasi, and PD Ye. High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum G m exceeding 1.1 mS/μm: New HBr pretreatment and channel engineering. In *Electron Devices Meeting (IEDM), 2009 IEEE International*, pages 1–4. IEEE, 2009.

[3] Uttam Singisetti, Mark A Wistey, Gregory J Burek, Ashish K Baraskar, Brian J Thibeault, Arthur C Gossard, Mark JW Rodwell, Byungha Shin, Eun J Kim, Paul C McIntyre, et al. $In_{0.53}Ga_{0.47}As$ Channel MOSFETs With Self-Aligned InAs Source/Drain Formed by MEE Regrowth. *Electron Device Letters, IEEE*, 30(11):1128–1130, 2009.

[4] Eun Ji Kim, Lingquan Wang, Peter M Asbeck, Krishna C Saraswat, and Paul C McIntyre. Border Traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) Gate Stacks and Their Passivation by Hydrogen Anneals. *Applied Physics Letters*, 96:012906, 2010.

[5] Yoontae Hwang, Roman Engel-Herbert, and Susanne Stemmer. Influence of Trimethylaluminum on the Growth and Properties of HfO_2 / $In_{0.53}Ga_{0.47}As$ nterfaces. *Applied Physics Letters*, 98(5):052911–052911, 2011.

[6] Andrew D Carter, William J Mitchell, Brian J Thibeault, Jeremy JM Law, and Mark JW Rodwell. Al_2O_3 growth on (100) $In_{0.53}Ga_{0.47}As$ initiated by cyclic trimethylaluminum and hydrogen plasma exposures. *Applied physics express*, 4(9):091102–091102, 2011.

[7] GJ Burek, MA Wistey, U Singisetti, A Nelson, BJ Thibeault, SR Bank, MJW Rodwell, and AC Gossard. Height-selective etching for regrowth of self-aligned contacts using MBE. *Journal of Crystal Growth*, 311(7):1984–1987, 2009.

[8] Rachid Driad, Zheng-Hong Lu, SylvainLaframboise SylvainLaframboise, Donald Scansen, William RossMcKinnon, and Sean McAlister. Reduction of surface recombination in InGaAs/InP heterostructures using UV-irradiation and ozone. *Japanese Journal of Applied Physics*, 38:1124, 1999.

[9] G. J. Burek B. Thibeault J. Cagnon S. Stemmer S. R. Bank Y. Sun E. J. Kiewra D. K. Sadana A. C. Gossard M. A. Wistey, U. Singisetti and M. J. W. Rodwell. Regrowth of self-aligned, ultra low resistance ohmic contacts on InGaAs . In *Proc. 15th Int. Conf. Mol. Beam Epitaxy*, 2008.

[10] IOFFE. NSM Archive Physical Properties of Semiconductors, 2013.

[11] JW Matthews and AE Blakeslee. Defects in epitaxial multilayers: I. Misfit dislocations. *Journal of Crystal Growth*, 27:118–125, 1974.

[12] S Bhargava, H-R Blank, V Narayanamurti, and H Kroemer. Fermi-level pinning position at the Au–InAs interface determined using ballistic electron emission microscopy. *Applied Physics Letters*, 70(6):759–761, 1997.

[13] AK Baraskar. *Development of Ultra-Low Resistance Ohmic Contacts for InGaAs/InP HBTs*. PhD thesis, UC Santa Barbara, 2011.

Chapter 6

Gate Last MOSFET: Process and Results

As concluded in Chapter 5, gate first III-V MOSFETs suffer from high interface trap densities, due to process damage, and lack trends of device improvement with gate length. Since the development of H_2/TMA treatments, arsenic cap processing is no longer necessary to maintain interface quality; gate last processing is now possible. This chapter outlines the process flow for gate last using either MBE regrowth or MOCVD regrowth. Select transistor process lot data is analyzed. The MOCVD process flow gate length scales to 50 nm with the possibility of further gate length decrease. Best device results at 48 nm gate length and 0.8 nm EOT show 0.85 mA/micron at 0.5 V V_{ds} and 0.6 V V_{gs}-V_{th}, and peak transconductance of 2 mS/micron at a V_{ds}= 0.5 V. Subthreshold swing was brought to down to 97 mV/dec for long channel devices with InGaAs channels and *in-situ* N_2/TMA treatment [1].

6.1 Gate-Last MOSFET Process Flow (MBE)

The gate last process draws on modules from both the gate first process (Chapter 5) and the QWTLM process (Chapter 4). After MBE growth, the substrate is covered

in PECVD $SiO_x$for a dummy gate. For MBE regrowth, this dummy gate must be capable of being photoresist planarized; therefore, this layer is 300 nm thick. Next, electron beam evaporated chromium is deposited as a gate hard mask. Chromium is necessary since the power and chemistry of the dry etches erodes resist too quickly, preventing a highly vertical structure from being formed. Any "foot" left at the bottom of the dummy gate would allow non-selective InAs growth to occur, leaving an ungated access region in the device. EBL for device gate definition is done using HSQ resist to allow "mix-and-match" lithography with the optical stepper.

Dry etches are the same as used in the gate first process. Chromium is etched in Cl_2/O_2, and SiO_x etched in SF_6/Ar. After SiO_x etching, the Cr at the top of the gates must be removed to prevent inconsistent regrowth conditions near gate edges. Photoresist planarization is used to remove the regrowth from structures less than 1 micron in gate length. Careful removal of the photoresist is important at this step; otherwise, the resist cannot be removed without damaging the InGaAs channel. After etching the Cr in Cl_2/O_2, the sample must be O_2 ashed prior to immersion in photoresist remover 1165. Without this ash, polymerized photoresist will remain on the sample.

After photoresist removal, the same surface preparation is done for regrowth. Regrowth in the MBE is identical compared to gate first processing. *In-situ* Mo was not explored at this time, but is worth investigation to lower contact resistivity to the final transistor.

Since MBE regrowth is non-selective (that is to say, it will grow material on surfaces other than the crystal), one must remove the amorphous InAs from the top and sides of the gate edge. If the InAs is not removed, the material will fall into the channel, preventing proper device operation. Photoresist planarization is done

again, and the InAs is wet etched.

Devices are then isolated with a photoresist mask and a combination of selective wet etches. Isolation must occur at this point in the process to minimize short circuits. The gate metal length is large compared to the wet etch depth required for proper device isolation. Device isolation after gate metal deposition would create a mask for long gate length, leaving a regrowth short circuit between source and drain. Furthermore, isolation before gate insulator deposition creates an interlevel dielectric for later processing. Ground-signal-ground (GSG) pads can be lifted off on top of the gate oxide and a low-leakage RF-terminated measurement can be done. This reduces device processing time since a spun-on interlevel dielectric (e.g., BCB) processing is not necessary. Also, having gate insulator material on the isolation mesa likely improves device passivation.

The SiO_xdummy gate is removed using a dilute buffered oxide etch and a surfactant. The surfactant (Tergitol or Triton) helps remove both amorphous InAs from the top and sides of the gate, and excess chromium left on dummy gates that have incorrect lateral aspect ratio for photoresist planarization. Positioning the sample upside-down also aids in the sedimentation of the InAs and chromium. Extensive experiments show this process works well, but is not capable of removing all debris. Altering regrowth conditions changes particulate formation, to the improvement or detriment of device yield.

Immediately after dummy gate removal, the samples are loaded into the ALD loadlock. The buffered oxide etch for dummy gate removal also achieves native oxide removal and surface preparation. H_2/TMA treatment is done prior to gate dielectric deposition; N_2/TMA treatment can also be done and has been shown to maintain interface trap density better than H_2/TMA treatment for sub-nm EOT oxides [1].

Unlike gate first processing, Al_2O_3 gate insulators cannot be used. As found in gate first processing, Al_2O_3 readily etches in photoresist developer; the gate metal liftoff process would have to use solvent-based lithography, e.g. EBL, to not etch the gate insulator. Instead, a bilayer of Al_2O_3 and $HfO_2$was employed. This allows the H_2 treatment and Al_2O_3 deposition to provide the best interface trap density, while the HfO_2 acts as an etch barrier. HfO_2 can also be thinned for smaller EOT. Inclusion of the HfO_2 layer did not significantly change the CV dispersion on MOSCAP samples (See Chapter 3, Figure 3.10). Alternatively, Al_2O_3 or HfO_2 single layers could be used if a blanket metal process were developed, such as *in-situ* gate metal (ruthenium, tungsten nitride),([2], [3]) or *ex-situ* metal evaporation and photoresist gate definition.

After ALD, the oxide is annealed in a RTA or a tube furnace under forming gas (10% H_2 / 90% N_2). The RTA and tube furnace provide similar MOSCAP results, but due to the large user base of the RTA, its cleanliness and therefore repeatability is suspect. This could cause increases in interface trap density that are not associated with ALD treatments. Also, there is a large temperature variance across the sample holder in the RTA [4], preventing multiple samples from being in one lot. The quartzware can accommodate four samples, with more if a new quartz boat were fabricated. With every FET lot, a MOSCAP epi (see Chapter 3) is included as an ALD witness sample. This ensures independent monitoring of the ALD, insulator annealing, and gate metallization steps.

Gate metal metallization is accomplished with photoresist liftoff. Gate metal length is longer than dummy gate length to prevent an ungated channel due to stepper misalignment. Since gate metal will cover the entire active gate length, obscuring gate length confirmation post-measurement, extra dummy gate width

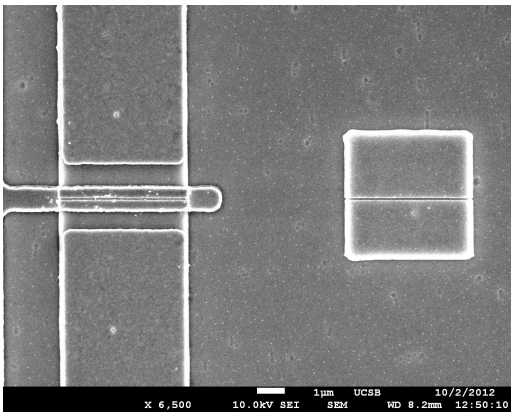


Figure 6.1: SEM image of extra device mesa and gate width for gate length verification.

was written. See Figure 6.1. This allows the actual gate length to be confirmed after device processing without device destruction. There is some ambiguity in gate length due to the presence of gate insulator in this region; selective removal of insulator here will allow a more accurate gate length measurement. Gate metal is thermally evaporated to minimize process-induced interface trap density increase [5]. Nickel is the gate metal, with gold optionally evaporated as well to minimize metal oxidation and to increase total metal height. Nickel oxidation may increase gate access resistance in back-end processing. Since nickel tends to deposit with stress, a thick film may cause resist to peel and the liftoff to fail. A thin layer of nickel and a thick layer of gold minimize stress and allow the gate metal to connect to the gate pad over the isolation mesa step height.

Source-drain metallization is accomplished with photoresist liftoff. Immediately prior to metallization, gate insulator is etched off in buffered oxide etch. Etching cannot be performed for too long or the resist will peel and the liftoff will fail. Thermal or electron-beam evaporation is performed, with either nickel/gold or titanium/palladium/gold respectively. For InGaAs regrowths, electron beam evap-

Gate Last B1			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 9×10^{12} cm^{-2}	Oxide Thickness	5 nm, 1 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	100406	Regrowth Doping	Si

Table 6.1: Gate Last Lot B1 Process Specifications

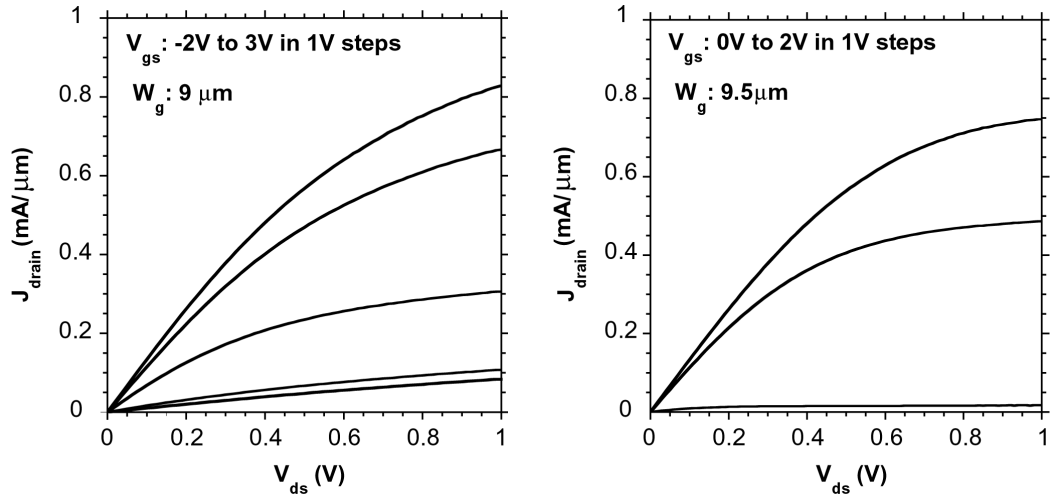
oration is preferred due to its ability to deposit titanium. Ti/Pd/Au is known to provide low specific contact resistivity to n-InGaAs (See Chapter 4).

6.2 Gate Last: Device Results (MBE Regrowth)

A large number of process lots were accomplished using MBE source-drain regrowth. Below is a select review of those process lots. These lots capture the performance possible with MBE source-drain regrowth, and its limitations.

6.2.1 Gate Last Lot B1: Initial gate last, long L_g Comparison

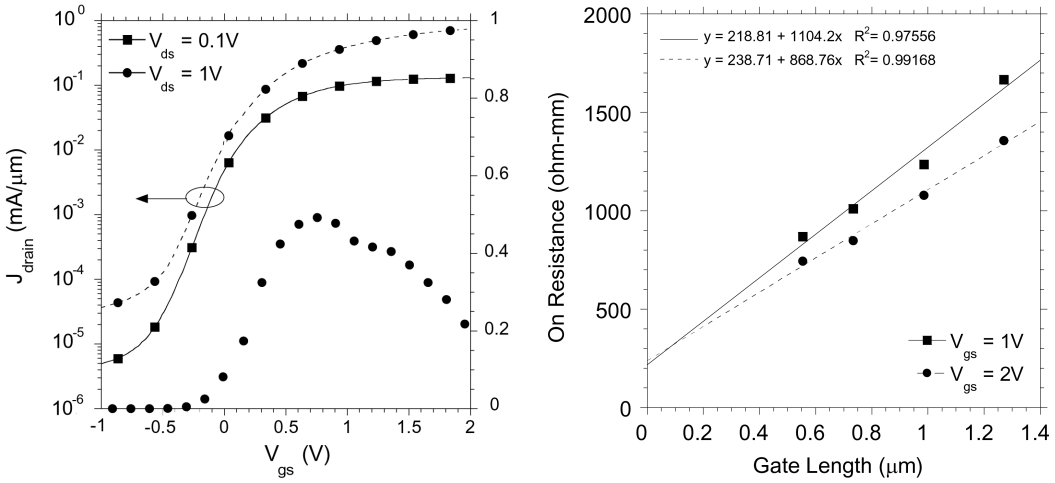
The goal of the first experiment was to see a head-to-head comparison of gate first to gate last on the same epi design (though not the same epi identically). As seen in Figure 6.2, the J_d-V_{ds} at the same gate length is startlingly different. Comparing gate first and gate last at the same gate biases, the transconductance has increased and the output conductance has decreased. See Figure 6.3a. Lots A1, A3, and B1 have identical epi design, but only Lot B1 could be brought into subthreshold. The increased transconductance and superior subthreshold performance suggest smaller interface trap density for Lot B1. The access resistance for Lot B1 (approx. 200 Ω·µm, double-sided) is also lower than A1 or A3 (both around



(a) Lot A1, 500 nm L_g (as drawn) (b) Lot B1, 500 nm L_g (as drawn)

Figure 6.2: Lot B1: J_{drain}-V_{ds} comparison to gate first, 500 nm L_g(as drawn).

300 Ω·μm, double-sided); removal of the ungated access region is improving the transistor access resistance.



(a) Lot B1, 500 nm L_g (as drawn)

(b) Lot B1, R_{on} versus L_g

Figure 6.3: Lot B1: J_{drain}-V_{gs} and R_{on}.

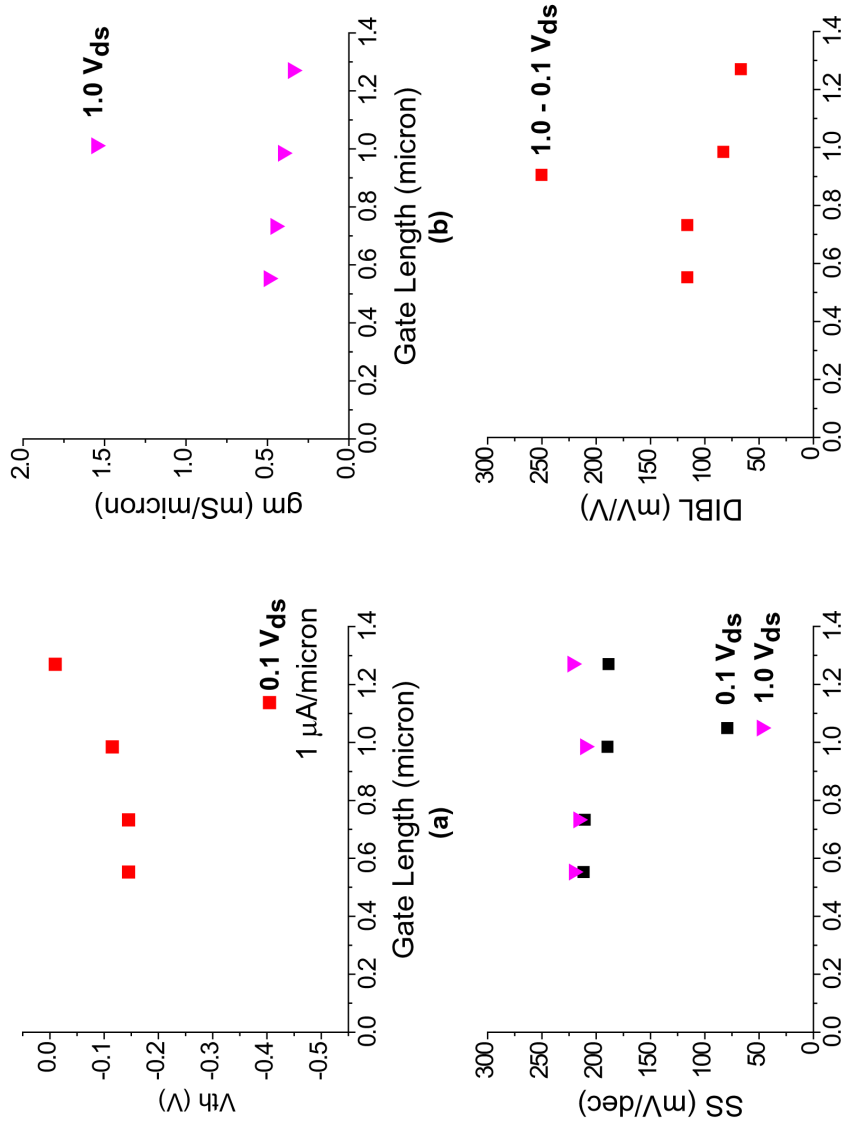


Figure 6.4: Lot B1: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

Gate Last B3			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	3.3 nm, 1.5 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	120110E	Regrowth Doping	Si+Te

Table 6.2: Gate Last Lot B3 Process Specifications

6.2.2 Gate Last Lot B2: Short L_g Process Refinement

Between Lots B1 and B3, extensive process flow enhancements were made to accommodate short gate length processing. It was found that a source-drain to channel gap could form if the dummy gate dry etch was done improperly [6]. After fixing this, gate lengths could scale appropriately, and device fabrication work for improved device performance commenced.

6.2.3 Gate Last Lot B3: Si/Te co-doping

One possible reason for low performance is poor source charge. It is possible that, while Hall data confirms 5×10^{19} cm^{-3} charge in the regrowth, there is a difference in doping density near a gate edge. Si and Te co-doping experiments were done (See Chapter 4) and found regrowth to have a lower overall sheet resistance and higher charge densities. In terms of process flow, the regrowth is smoother using Si/Te co-doping (Figure 4.7). This eases device processing and alignment during lithography. Delta doping density was decreased to move the electron wavefunction closer to the surface.

Figure 6.6 shows J_d-V_{ds} and -V_{gs} data for long and short gate length devices in Lot B3. Peak transconductance at 500 nm gate length is similar to Lot B1. In Figure 6.5, access resistances are similar to Lot B1, even though the delta doping

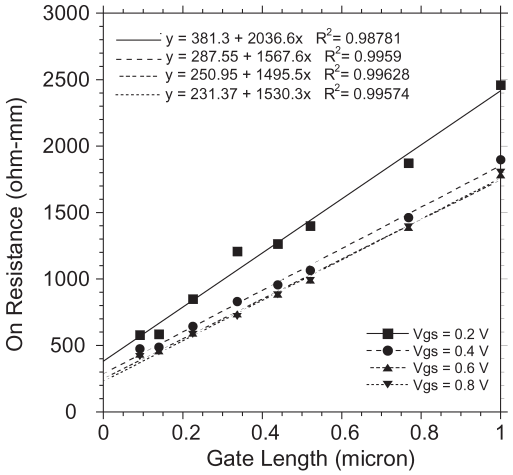


Figure 6.5: Lot B3: R_{on} versus L_g.

has been decreased. In Figure 6.7, short gate lengths suffer from threshold voltage rolloff and subthreshold swing increase due to the large delta doping and thick channel. The smallest gate length (81 nm) showed aggressive short channel effects and lower peak transconductance than longer gate lengths. For the long gate length devices, a minimum subthreshold swing of $\sim$ 120 mV/dec correlates to an interface trap density of $1{\times}10^{13}\text{cm}^{-2}$ eV^{-1}.

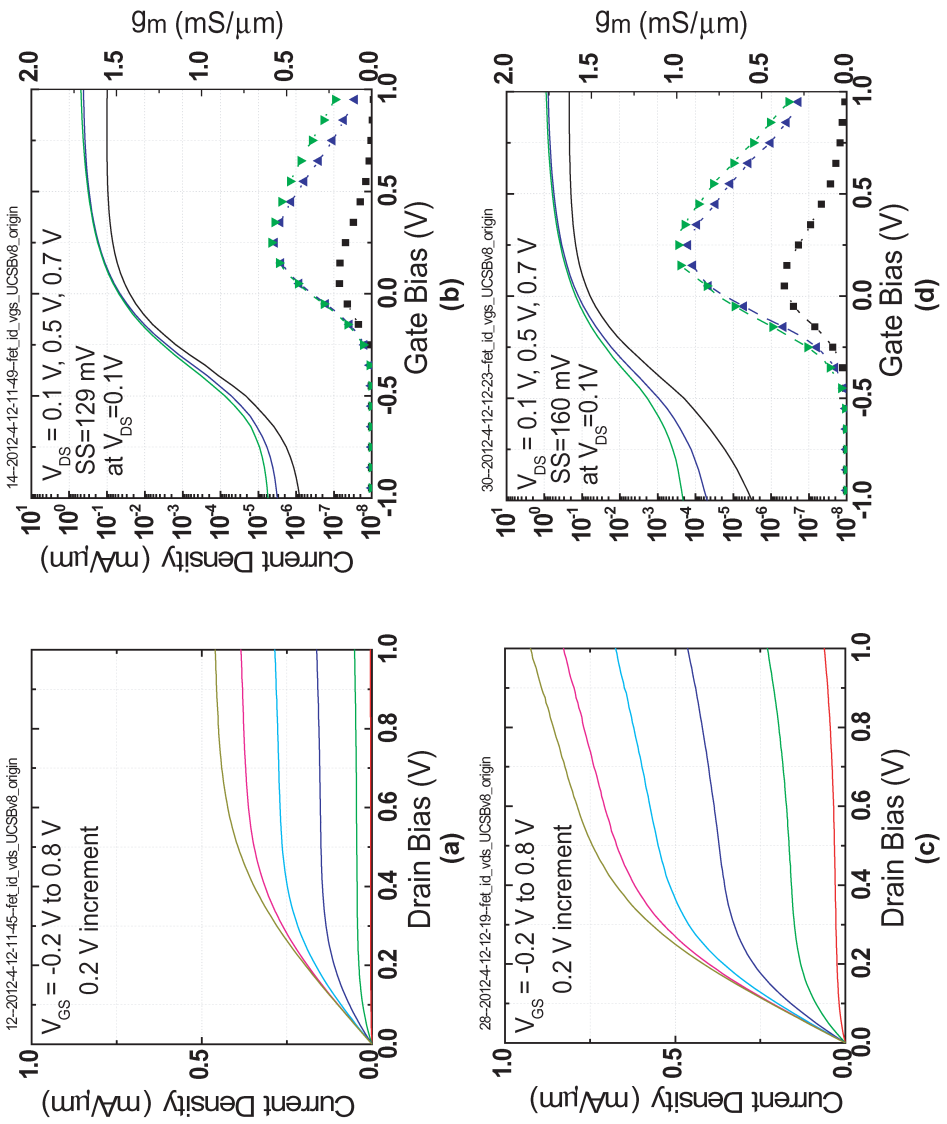


Figure 6.6: Lot B3: J_{drain} versus V_{ds} and V_{gs}. a) 520 nm L_g J_d-V_{ds} b)520 nm L_g J_d-V_{gs} c) 140 nm L_g J_d-V_{ds} d)140 nm L_g J_d-V_{gs}.

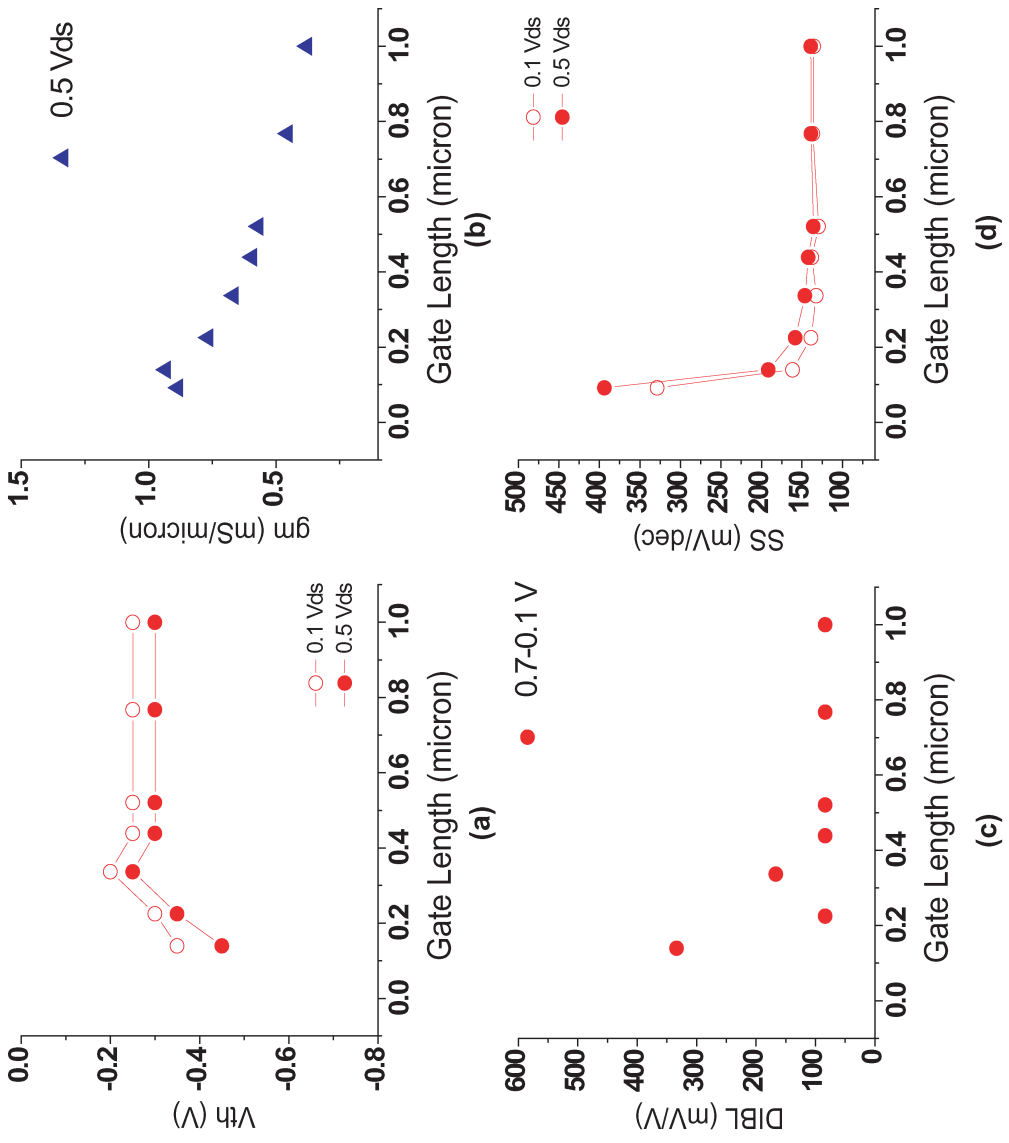


Figure 6.7: Lot B3: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

Gate Last B4			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MBE	Regrowth Spec	InGaAs, 50 nm
Epi Lot #	120110E	Regrowth Doping	Si+Te

Table 6.3: Gate Last Lot B4 Process Specifications

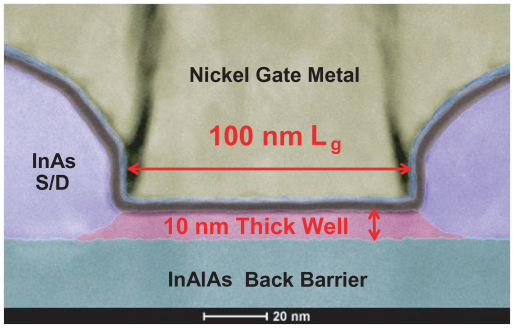


Figure 6.8: STEM cross-section of gate last FET, chemistry color-coding. Image courtesy Jeremy Law.

6.2.4 Gate Last Lot B4: InGaAs MBE Regrowth

Figure 6.8 shows a STEM image of a gate last FET with regions color-coded by chemistry. Chemical information was provided by energy dispersive x-ray spectroscopy (EDX). This confirms TEM imaging from the gate first process: InAs regrowth "sinks" into the channel region. This moves the InAs/InGaAs heterointerface to a small region near the gate edge of the device.

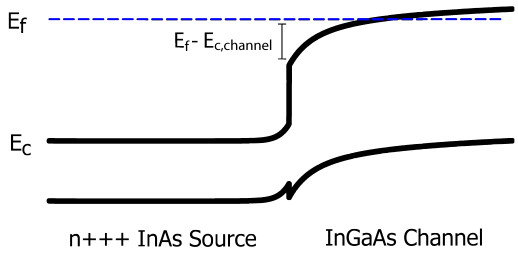


Figure 6.9: Electron band diagram along the regrowth/channel interface.

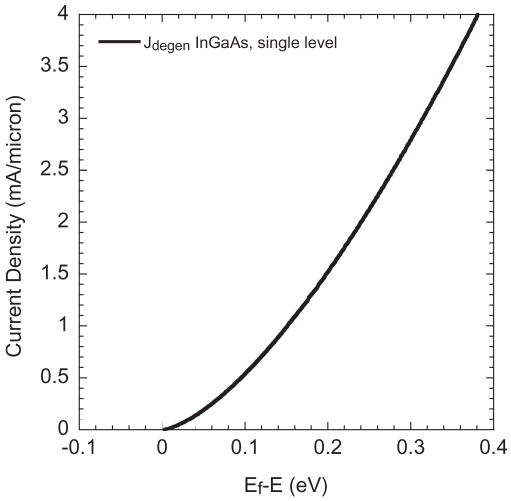


Figure 6.10: Drain current versus electron Fermi level, degenerate approximation

Even if the regrowth did not sink, the InAs/InGaAs heterointerface has the potential to limit source charge. Figure 6.9 is an electron band diagram along the source-to-channel interface in source semiconductor. Given the high doping concentration in the source, nonparabolicity of the semiconductor must be considered [7]. Nonparabolicity effectively increases the semiconductor density of states with Fermi level. Using a 1D-Poisson semiconductor solver using nonparabolicity (Bandprof), we can obtain Figure 6.9. The E_f-$E_{c,channel}$ puts a limit on source charge. From Chapter 2, ballistic FET current in the degenerate limit is given by:

$$J_{degenerate} = \frac{2q\sqrt{2m^*}}{3\hbar^2\pi^2}(E_f - E_1)^{\frac{3}{2}} \tag{6.2.1}$$

and Figure 6.10 is a plot of charge density versus Fermi level above the band edge. For 5×10^{19} cm^{-3} n-doped relaxed InAs to NID InGaAs lattice-matched InP, E_f-$E_{c,channel}$ is 0.25 eV. From Figure 6.10, that corresponds to a drain current of 2.15 mA/micron. The calculation did not consider quantization of the InGaAs channel, which will decease E_f-$E_{c,channel}$ and therefore decrease maximum current density.

Since the Te acts as a surfactant during InAs regrowth, it should improve InGaAs regrowth quality. Previous InGaAs MBE regrowths suffered from gaps near the gate edge [8]. Te should help minimize this gap and also give higher material quality.

As Figure 6.11 shows, long gate length performance with InGaAs is worse than with InAs regrowth, specifically in subthreshold swing and on-state transconductance. This could be due to a few factors, including process variation and damage, increasing interface trap density and lowering channel mobility. However, short-channel on-state performance has improved to $\sim$ 1.17 mS/micron at 0.5 V_{ds} for 87 nm gate length. Figure 6.12 shows slightly increased access resistances, which is likely due to increased parasitic access resistance from InGaAs regrowth. The sheet resistance is twice that of InAs (43 versus 17 $\Omega/\square$, Table 4.1), and also shows increased metal-semiconductor resistance (17 versus 8 $\Omega\cdot\mu$m). The two metal contacts and the $\sim$ 500 nm source-drain to metal gap on either side of the channel account for this increase. The sheet resistance is almost double for similar V_{gs}-V_{th}, suggesting Lot B4 has worse mobility, even though the samples are from an identical epi Lot.

Figure 6.13 shows the V_{th}, g_m, DIBL, and subthreshold swing for Lot B4. Lots B3 and B4 are similar in off-state performance except at the shortest gate length. The transconductances for B3 are higher versus gate length, but do not reach the same level for the shortest gate length.

While InGaAs MBE regrowth appears to work the same or better than InAs, it is also a more challenging regrowth to reproduce. Due to the potential for lot-to-lot variance, InAs regrowth was kept as the standard technique for MBE gate last.

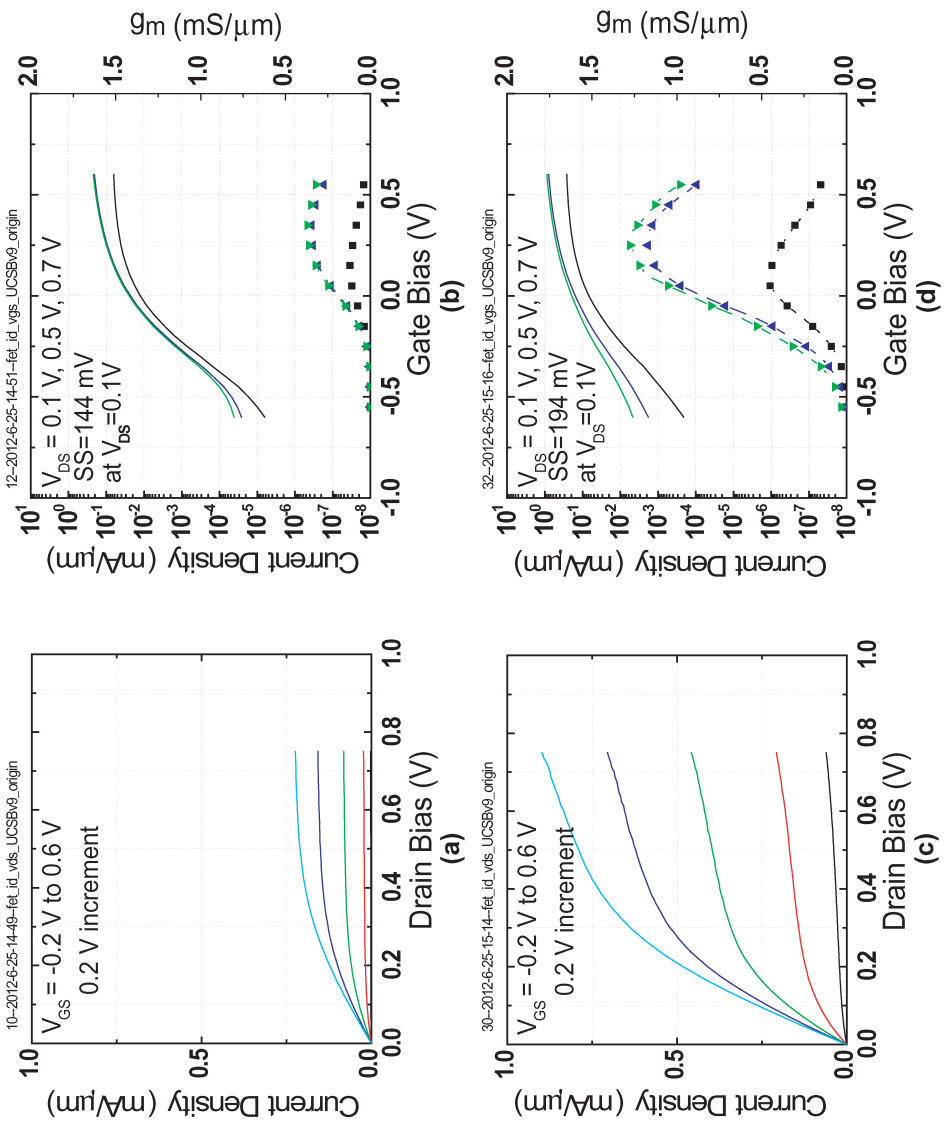


Figure 6.11: Lot B4: J_{drain}versus V_{ds} and V_{gs}. a) 495 nm L_g J_d-V_{ds} b)495 nm L_g J_d-V_{gs} c) 81 nm L_g J_d-V_{ds} d)81 nm L_g J_d-V_{gs}.

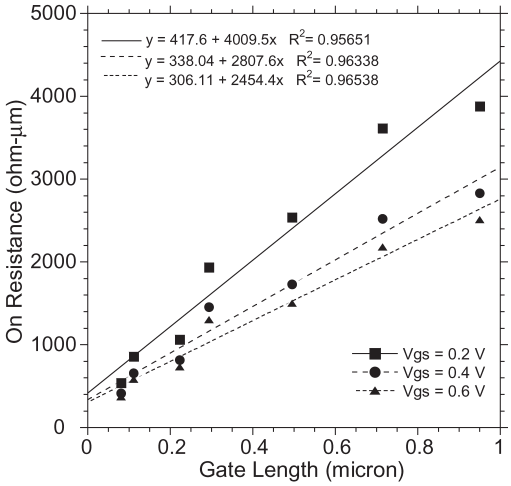


Figure 6.12: Lot B4: R_{on} versus L_g.

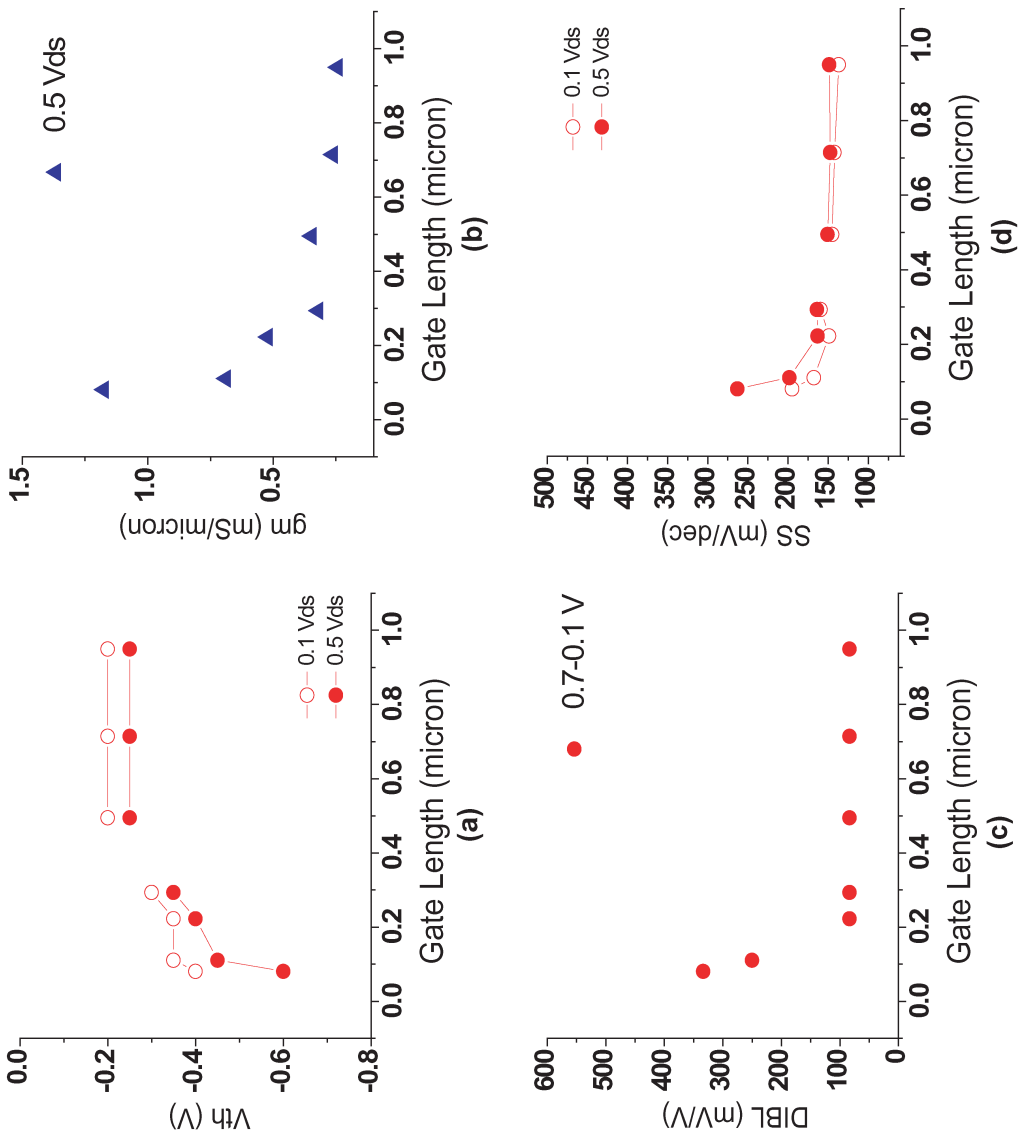


Figure 6.13: Lot B4: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

Gate Last B5			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	IQE Rev4	Regrowth Doping	Si+Te

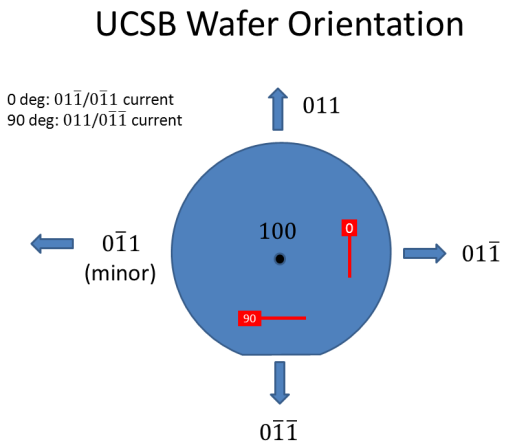
Table 6.4: Gate Last Lot B5 Process Specifications

6.2.5 Gate Last Lot B5: Commercial Epitaxy

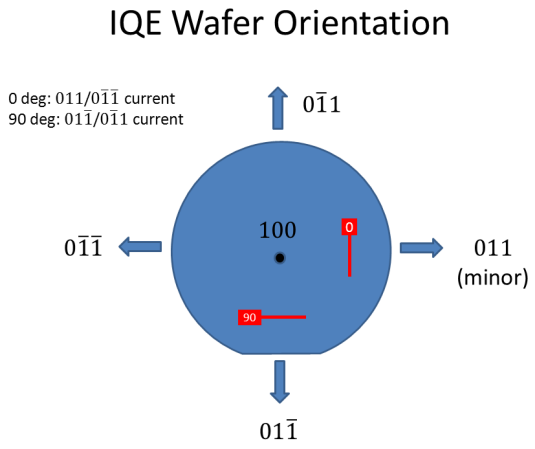
Most of the epitaxial material for this thesis was grown in the USCB Materials MBE Lab. It is likely that commercial epitaxy vendors provide material with higher mobilities, more repeatable wafer specifications, and lower growth defect densities. Therefore, a standard wafer specification (10 nm InGaAs channel, delta doping 3 nm, 3.9×10^{12} cm^{-2}), identical to Lots B3 and B4, was grown by IQE Inc.

As Figure 6.15 shows, initial J_d-V_{ds} and V_{gs} results indicate performance similar to or worse than previous lots using UCSB-grown epi material. Short gate length devices only reached 0.9 mS/micron at 0.5 V_{ds}. However, devices that are 90 degrees perpendicular to typically measured devices showed improved performance (Figure 6.14). UCSB semi-insulating InP uses the "European/Japan" or "E/J" wafer flat designation, while IQE uses "US" flat designation. However, the standard FET process flow always orients "0 degree" transistors with gate stripes perpendicular to the major flat, regardless of wafer flat designation. Therefore, when processing on IQE epi, the sample current flow direction for "0 degree" devices is equivalent to an orientation of "90 degree" on UCSB epi.

As seen in Figure 6.16, J_d-V_{ds} and V_{gs} results on 90 degree devices show improved on-state performance. For the 87 nm gate length device, peak transconductance was 1.2 mS/micron at 0.5 V_{ds}. However, off-state performance worsened for both short



(a) UCSB epi, device orientations



(b) IQE epi, device orientations

Figure 6.14: Wafer orientations with respect to device layout.

and long L_g devices. Subthreshold swing increased from 117 to 134 and 181 to 209 mV/dec at 0.1 Vds for $\sim$ 500 nm and $\sim$ 70 nm L_g, respectively.

Figures 6.17 and 6.18 are the V_{th}, g_m, DIBL, and subthreshold swing for Lot B5 0 and 90 degree devices, respectively. For both orientations, two different gate length series of either device orientation are provided to increase confidence in data. It is clear that the 90 degree devices have a negative threshold voltage shift, improved transconductance, and increased subthreshold swing at almost all gate lengths. There are two possible reasons: axis dependence on MBE regrowth, and axis dependence on interface trap density. MBE axis dependence on regrowth could increase charge density, and therefore improve device performance, if that is a limiting factor. Interface trap density, specifically its distribution and frequency response, could affect V_{th}, g_m, and subthreshold swing simultaneously.

Comparison to similarly processed UCSB epi is important to confirm the axis dependent effect. Figure 6.19 shows transconductance and subthreshold swing at short gate lengths for Lot B5 and epi 120615A#2, a FET with a similar process flow. For UCSB epi, there is a trend for higher on-state performance with 0 degree devices, but better off-state performance with 90 degree devices. IQE epi shows the opposite trend.

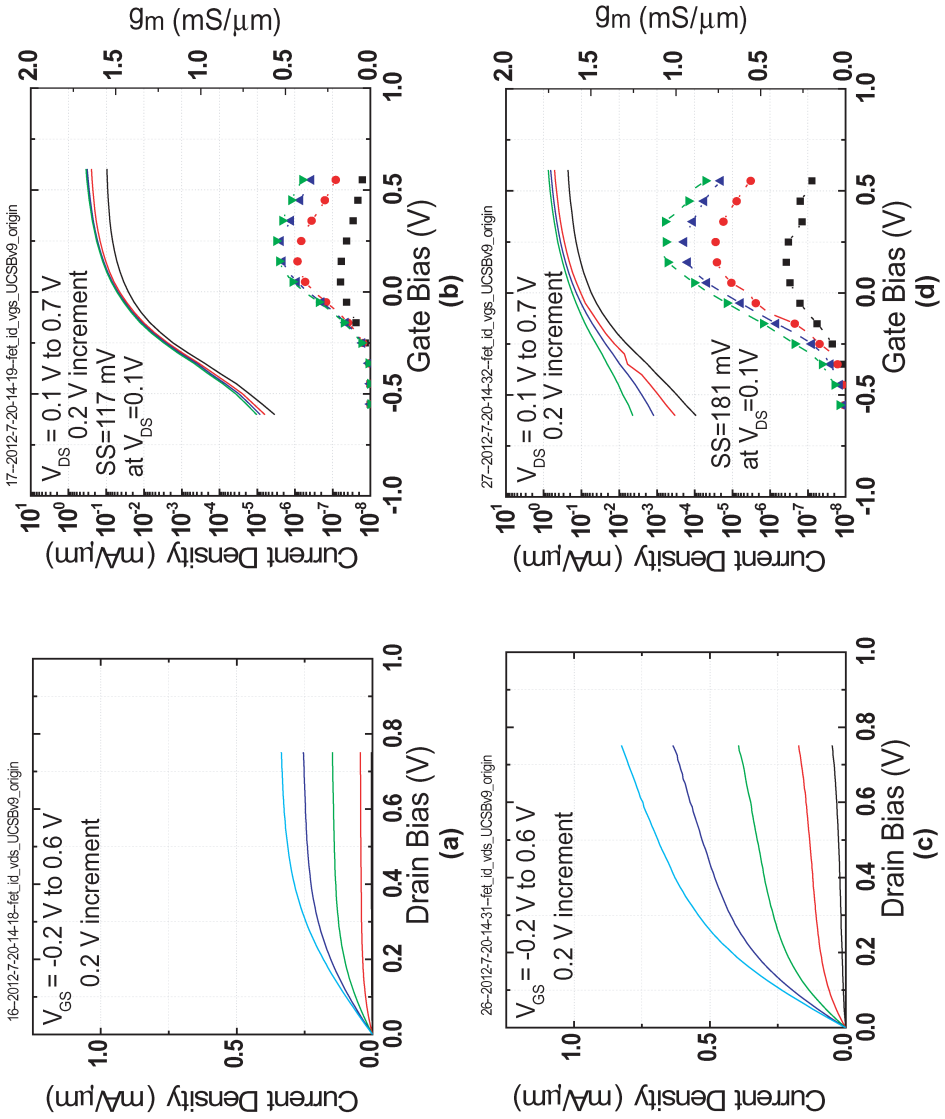


Figure 6.15: Lot B5, 0 degree: J_{drain}versus V_{ds} and V_{gs}. a) 501 nm L_g J_d-V_{ds} b)501 nm L_g J_d-V_{gs} c) 64 nm L_g J_d-V_{ds} d)64 nm L_g J_d-V_{gs}.

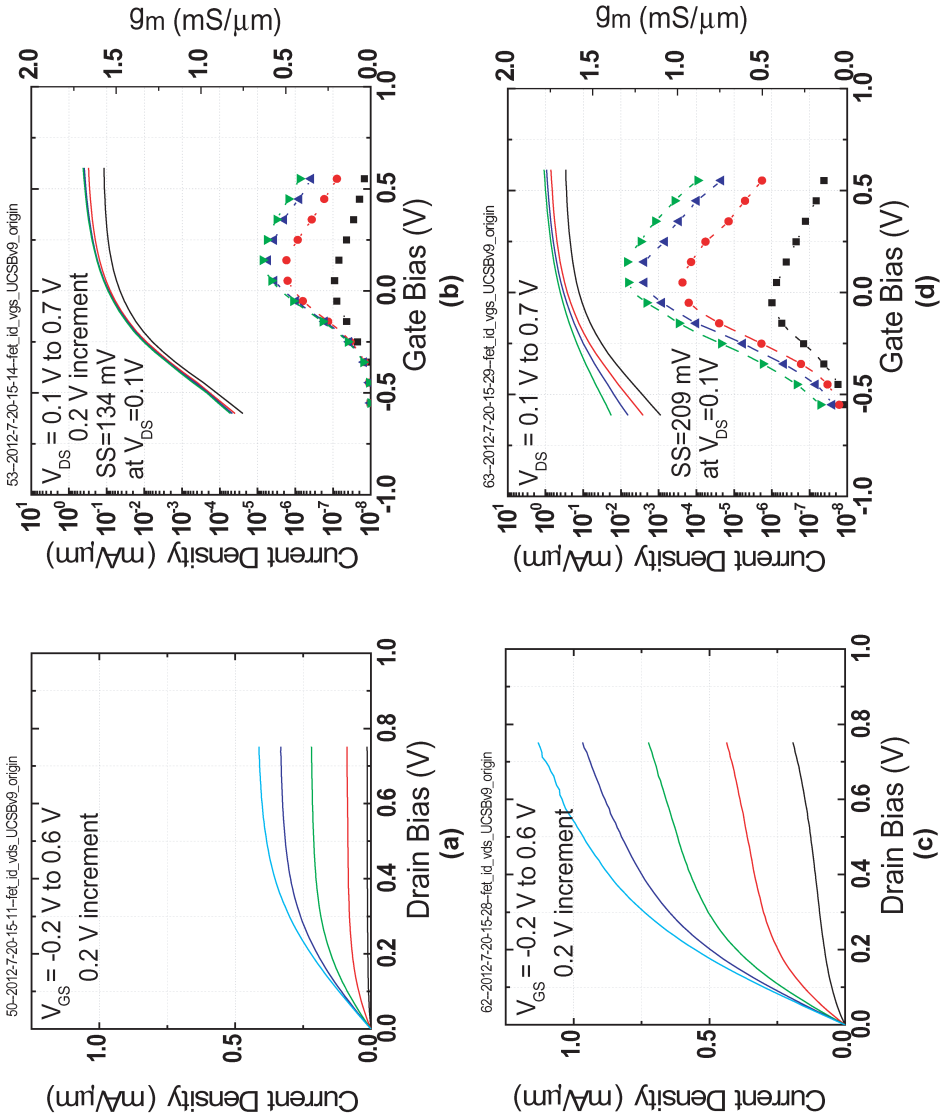


Figure 6.16: Lot B5, 90 degree: J_{drain}versus V_{ds} and V_{gs}. a) 515 nm L_g J_d-V_{ds} b)515 nm L_g J_d-V_{gs} c) 87 nm L_g J_d-V_{ds} d)87 nm L_g J_d-V_{gs}.

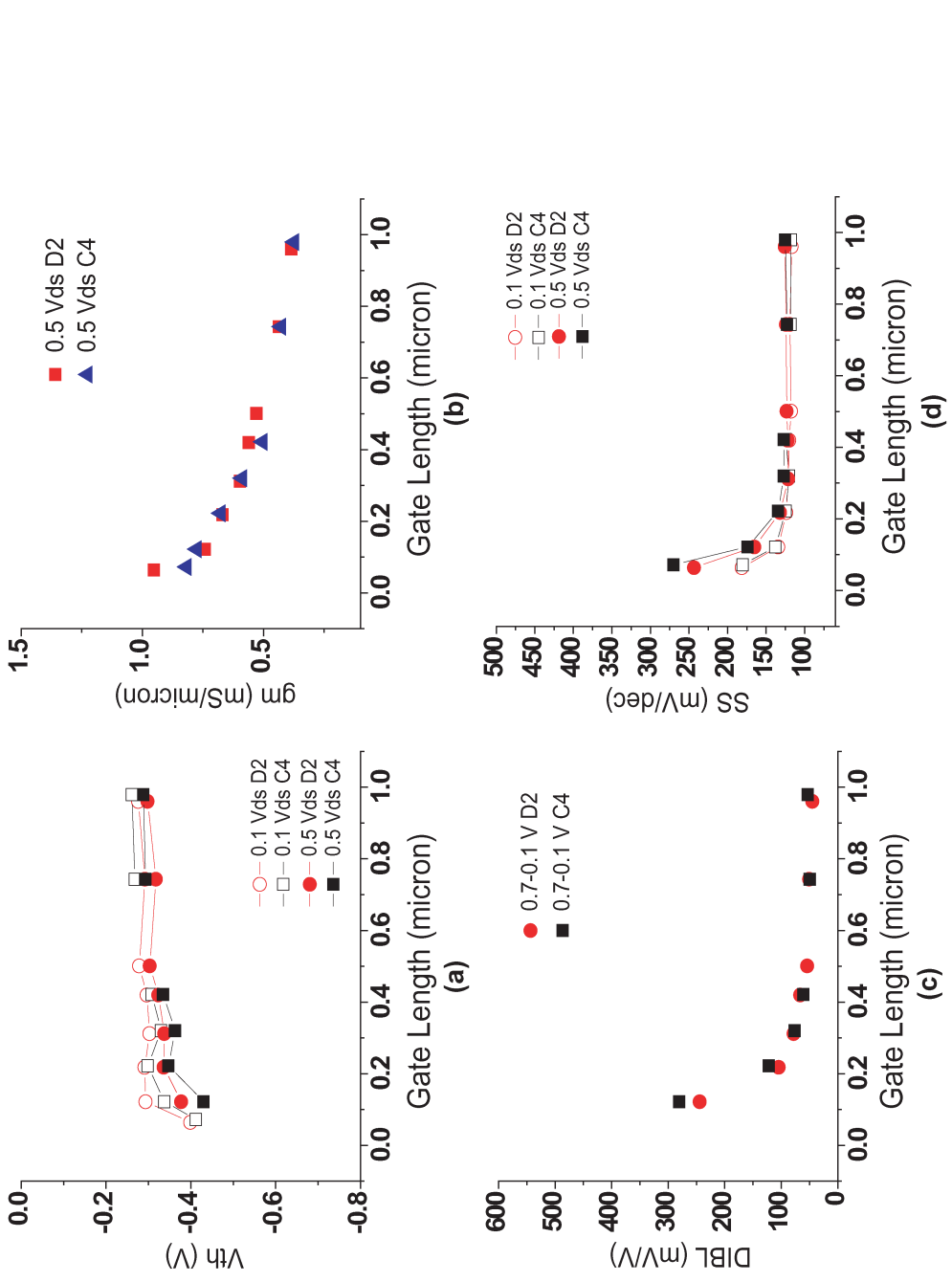


Figure 6.17: Lot B5: Figures of merit versus $L_g$for 0 degree FETs. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

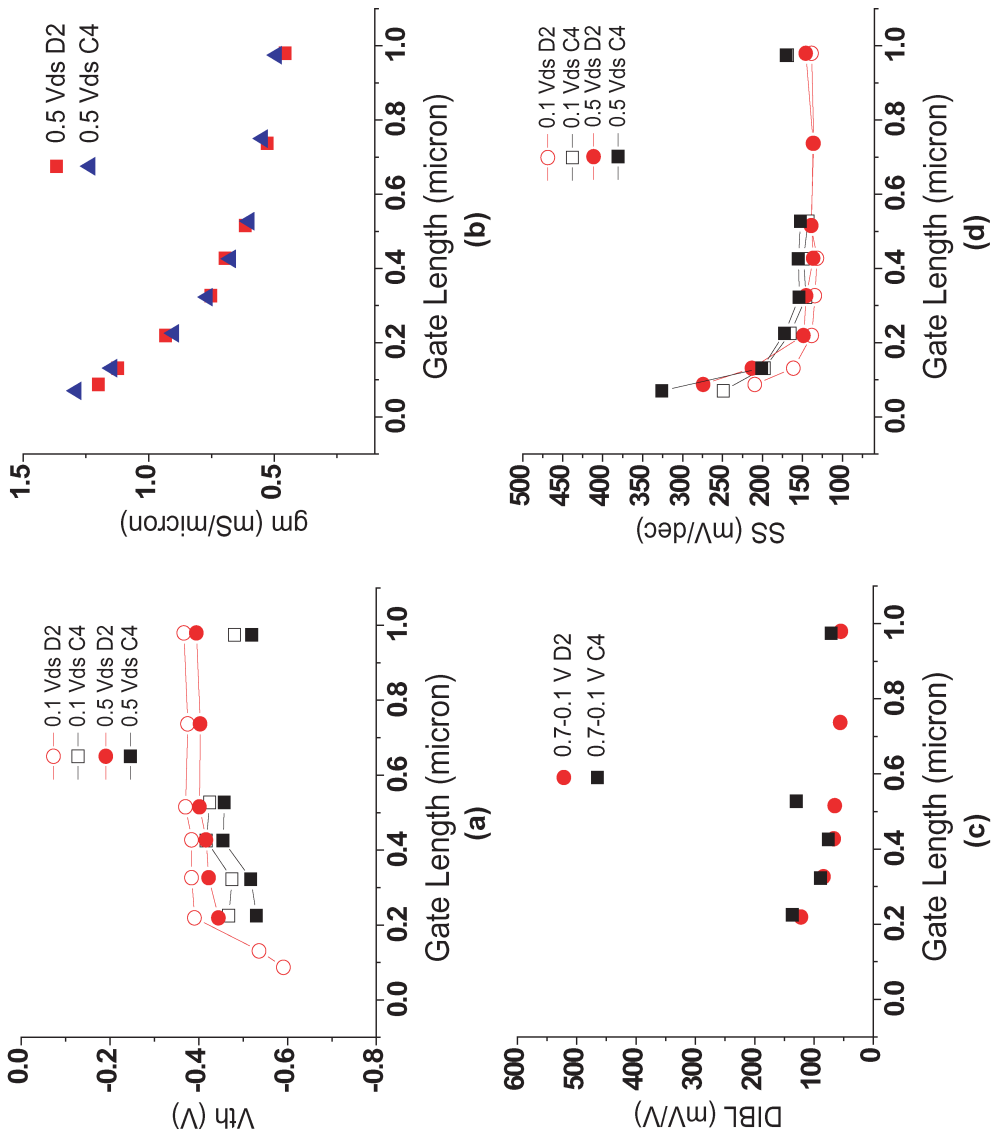


Figure 6.18: Lot B5: Figures of merit versus $L_g$for 90 degree FETs. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

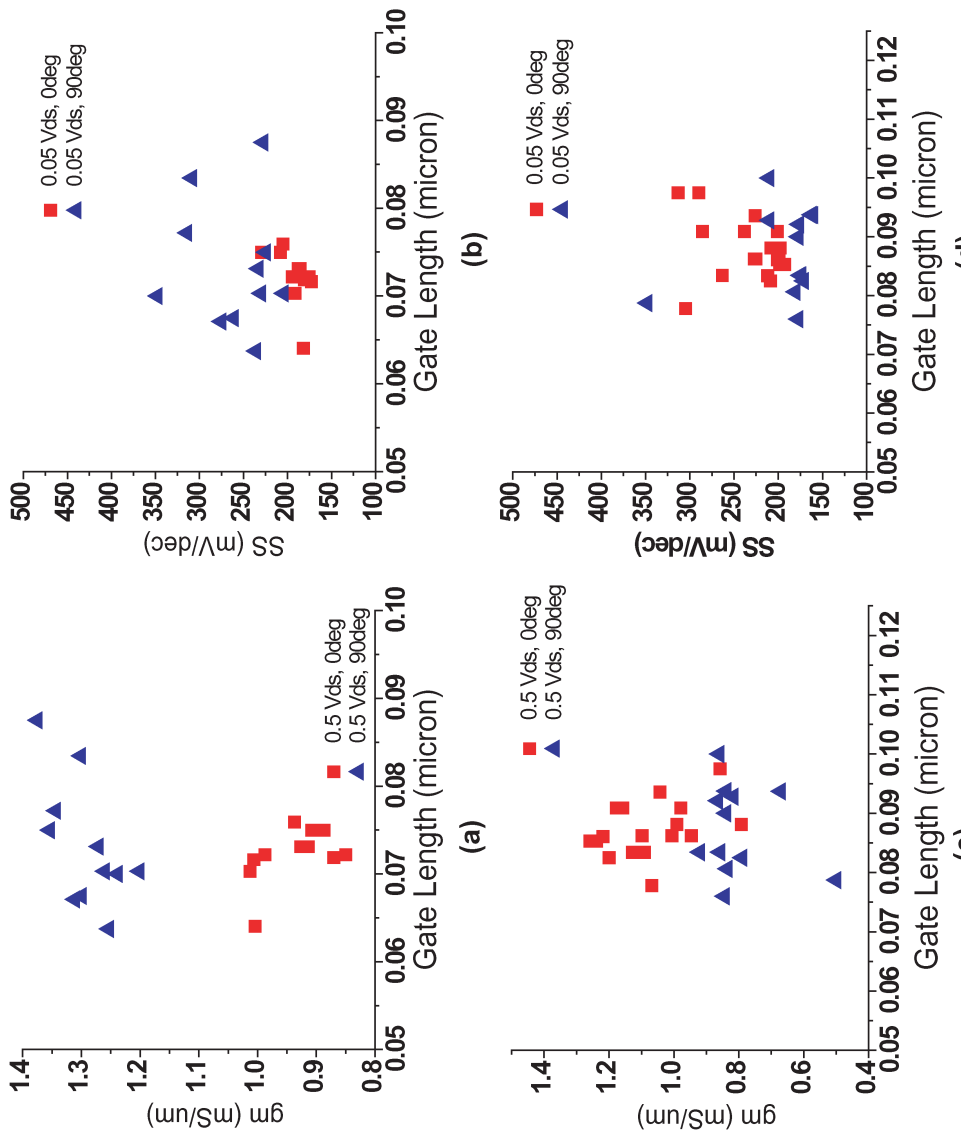


Figure 6.19: Lot B5: g_m and subthreshold swing at short gate lengths a) g_m, IQE Epi b) SS, IQE Epi c) g_m, UCSB Epi d) SS, UCSB epi.

Gate Last B6			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	120615A	Regrowth Doping	Si+Te

Table 6.5: Gate Last Lot B6 Process Specifications

6.2.6 Gate Last Lot B6: Sulfur Treatment

Even with the research and development put into developing an *in-situ* cleaning method for InGaAs surfaces, this may not be as effective as other techniques. Measured subthreshold swings suggest large amounts of interface traps are still present. Other III-V MOS research groups use hydrogen sulfide passivation ([9], [10], [11], [12], [13]). Therefore, sulfur treatment was applied to a transistor lot without H_2/TMA treatment. After dummy gate removal in buffered oxide etch, the sample was rinsed in DI and transferred to a bath of 10.5% $(NH_4)_2S$. The sample was left for 20 minutes, rinsed in DI and immediately loaded into the ALD loadlock.

Figure 6.20 shows 500 nm and 50 nm L_g (as drawn) J_d-V_{ds} and J_d-V_{gs}plots. Performance is similar to previous lots, showing $\sim$ 1 mS/micron transconductance at 0.5 V_{ds}. Subthreshold swing is also similar for long channel devices at 127 mV/dec.

As seen in Figure 6.21, trends are similar to previous lots. The sulfur treated devices have a more negative threshold voltage compared to other lots. This could be due to the sulfur treatment creating a flatband voltage shift at the channel/insulator interface. This could also be due to process variation. More importantly, subthreshold swing and transconductances are similar across all gate lengths. This means the interface trap density is similar for these lots. This could mean: a) the sulfur

and the H_2/TMA process provide similar interface trap densities or b) the interface trap density is determined by factors other than wafer treatment.

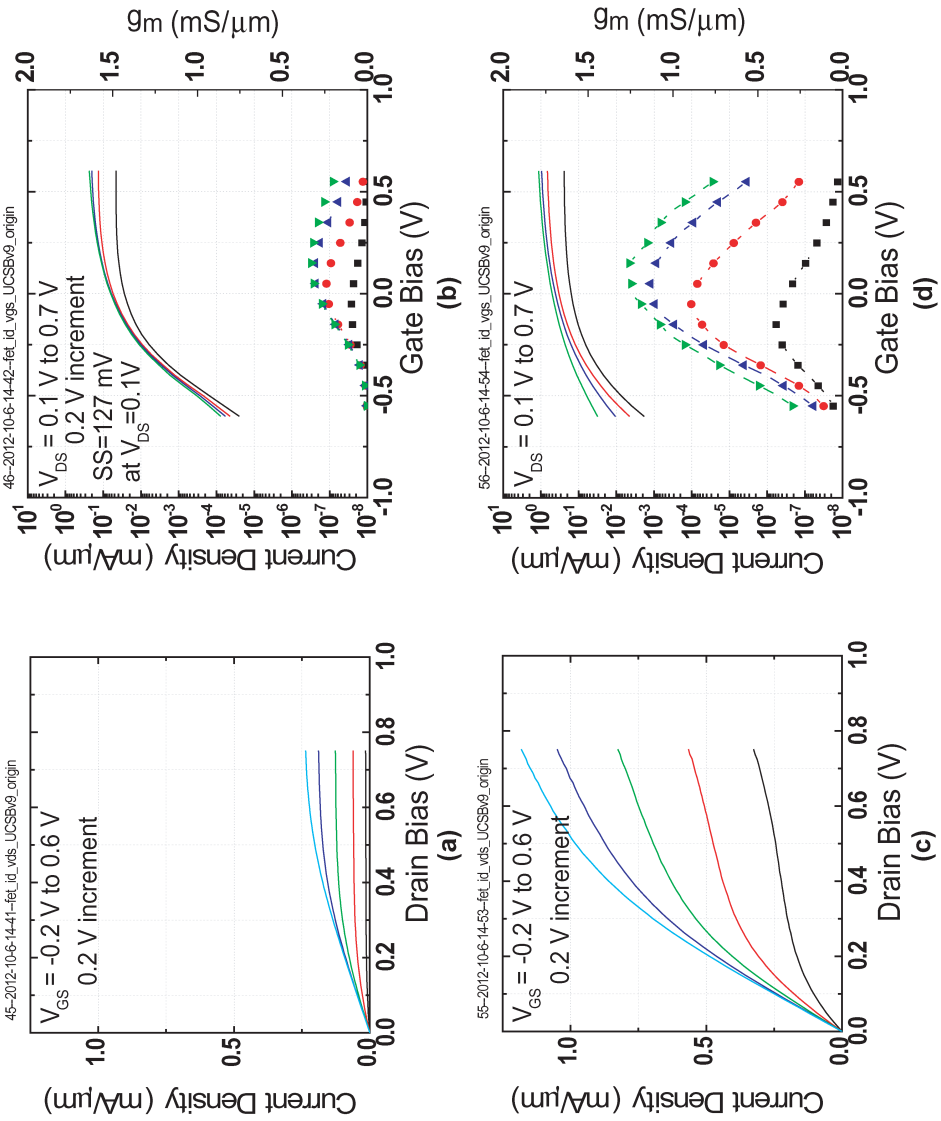


Figure 6.20: Lot B6: J_{drain}versus V_{ds} and V_{gs}. a) 500 nm (as drawn) L_g J_d-V_{ds} b)500 nm (as drawn) L_g J_d-V_{gs} c) 50 nm (as drawn) L_g J_d-V_{ds} d)50 nm (as drawn) L_g J_d-V_{gs}.

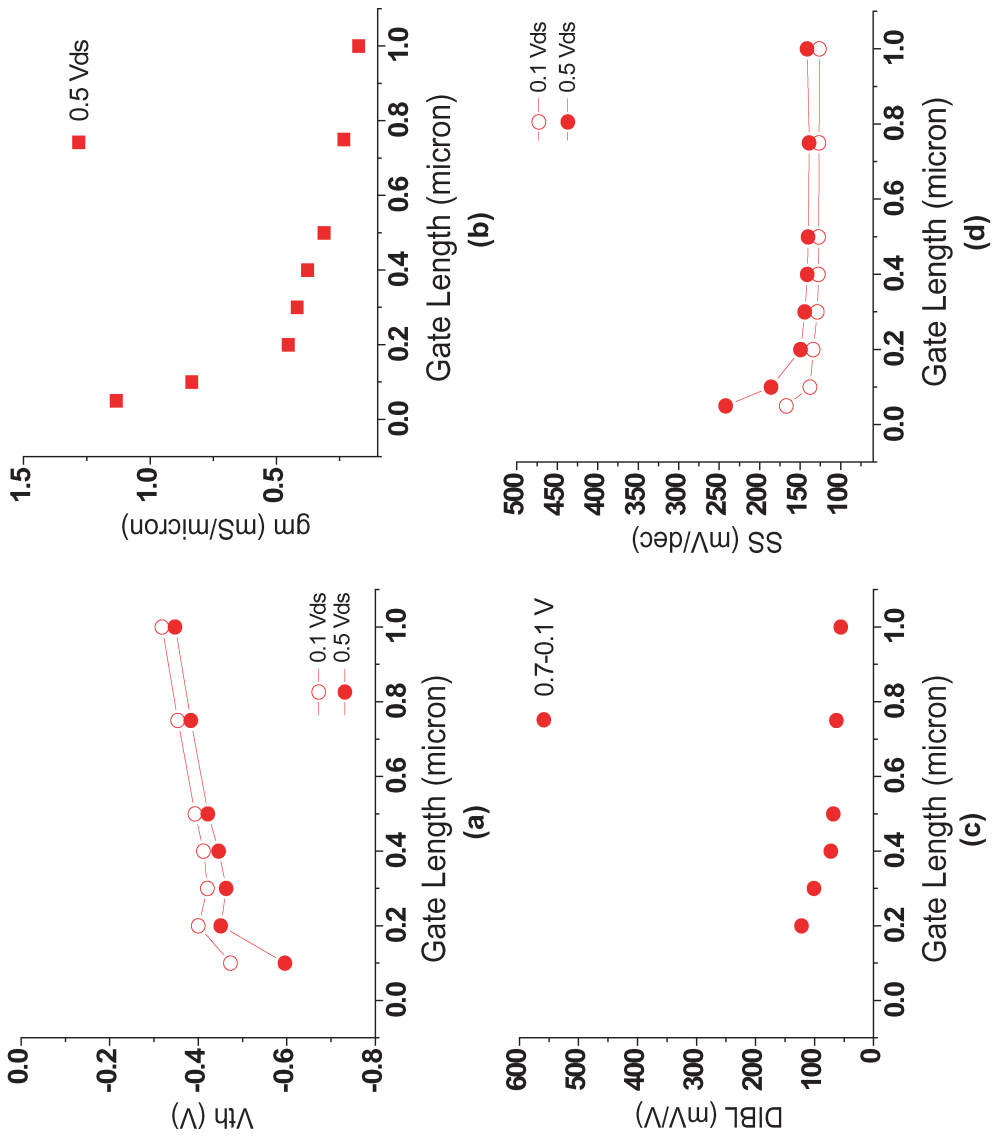


Figure 6.21: Lot B6: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

Gate Last B7			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	IQE Rev5	Regrowth Doping	Si+Te

Table 6.6: Gate Last Lot B7 Process Specifications

6.2.7 Gate Last Lot B7a and B7b: InP Channel Capping

MBE regrowth lots never see subthreshold swings less than 120 mV/dec, a sign of significant interface trap density still present on the channel surface. The device samples see processes that the witness MOSCAP in every lot does not see; process-induced damage may be occurring without measurement by the witness MOSCAP. CV experiments with MOSCAP epi were done to assess annealing damage during MBE regrowth. In Chapter 3, Figure 3.9 shows CV of SiO_x-capped MOSCAP material; one sample was annealed in an RTA at 500°C for 30 minutes, while the other sample had no annealing. After anneal, the caps were stripped and a standard 5 nm Al_2O_3 recipe was deposited with H_2/TMA cleaning. It is clear from the Figure that with annealing, the semiconductor surface is degraded. This degradation is consistent with an increase in interface traps [14]. Therefore, a sacrificial layer must be put in place to protect the channel during the high-temperature regrowth. ALD Al_2O_3 did not result in improved performance [6]. An InP layer may provide adequate channel protection. It can be grown in the epitaxial stack, and removed in HCl:DI. However, due to the lack of phosphorus in the UCSB MBE lab, the wafer was grown by IQE. To reduce back barrier leakage currents, the InAlAs buffer and back barrier were lightly p-doped (Be, 5×10^{16} cm^{-3}). This is a low enough concentration to not significantly deplete the delta doping. See Lot C6 (Section

6.4.6) for more information on the source of back barrier leakage. B7a and B7b are the same sample; B7 was cleaved into two halves after regrowth.

B7a was the first sample from this IQE wafer to be processed. The InP cap was removed immediately prior to loading in the ALD loadlock. Figure 6.22 shows J_d-V_{ds} and -V_{gs} plots for long and short gate lengths. While on-state performance for B7a is the highest of all MBE regrowth lots- 1.4 mS/micron at 0.5 V_{ds}- the subthreshold swing is the worst: 394 mV/dec for long channel and 450 mV/dec for short channel. 394 mV/dec subthreshold swing for this EOT corresponds to and interface trap density of more than $5\times10^{13}\text{cm}^{-2}$ eV^{-1}.

B7b has the same processing as B7a, but with longer HCl:DI etching to remove the InP capping. It also had ALD dielectric deposition performed on a different day. Figure 6.24 shows J_d-V_{gs} for a long and short L_g in this lot. While the subthreshold swing improved considerably for both gate lengths, the peak transconductance decreased from 1.4 mS/micron to 1.1 mS/micron at 0.5 V_{ds}. InP capping has only increased subthreshold swing, and has not shown significantly higher on-state performance. The cap removal might not be complete or optimized. Residual cap material may negatively interact with H_2/TMA treatment, increasing interface trap density.

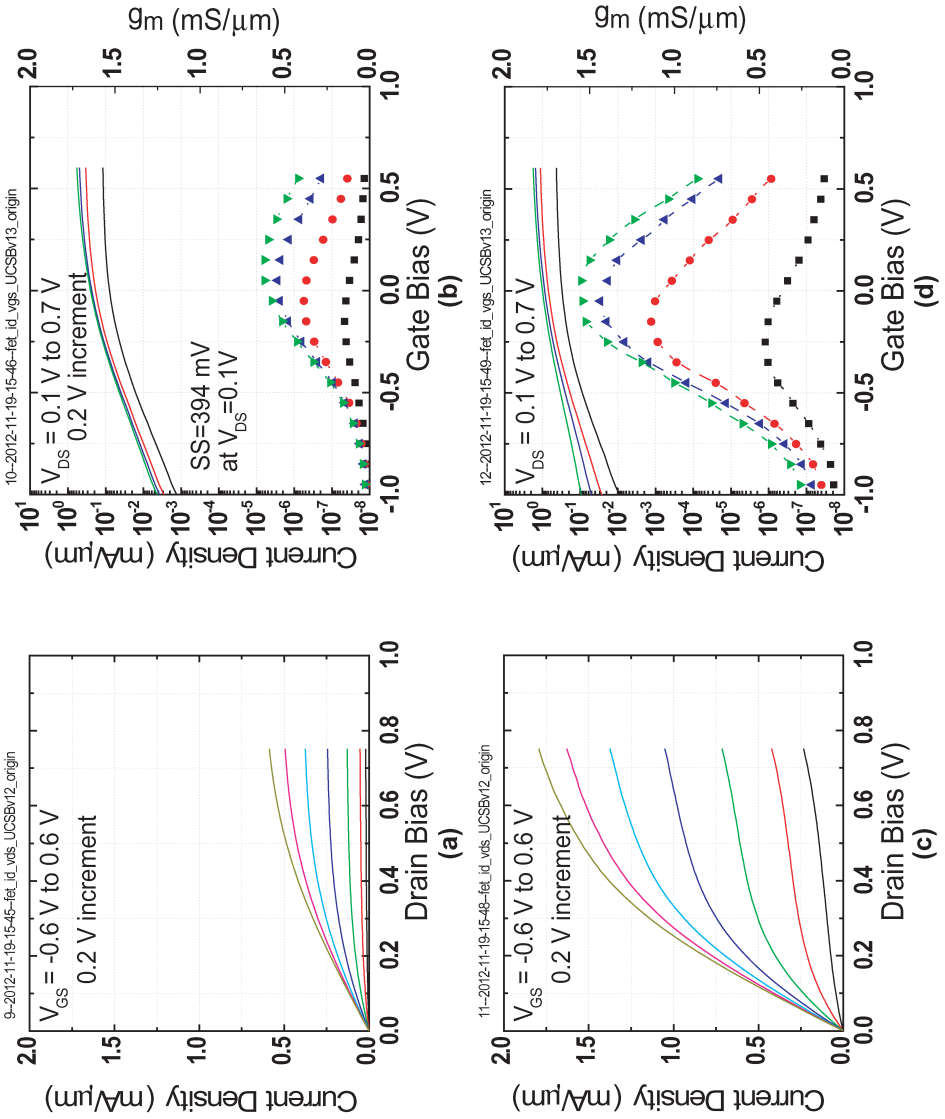


Figure 6.22: Lot B7a: J_{drain}versus V_{ds} and V_{gs}. a) 980 nm L_g J_d-V_{ds} b)980 nm L_g J_d-V_{gs} c) 64 nm L_g J_d-V_{ds} d)64 nm L_g J_d-V_{gs}.

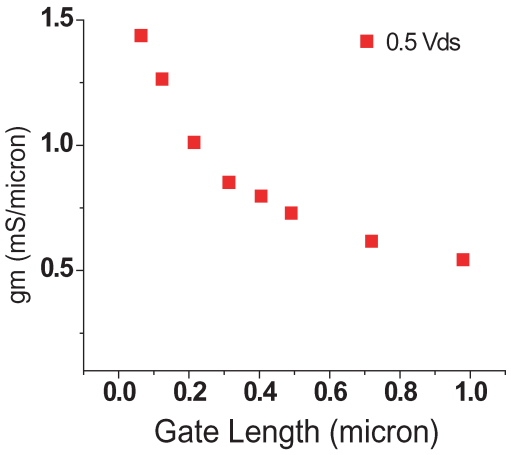


Figure 6.23: Lot B7a: g_m versus L_g.

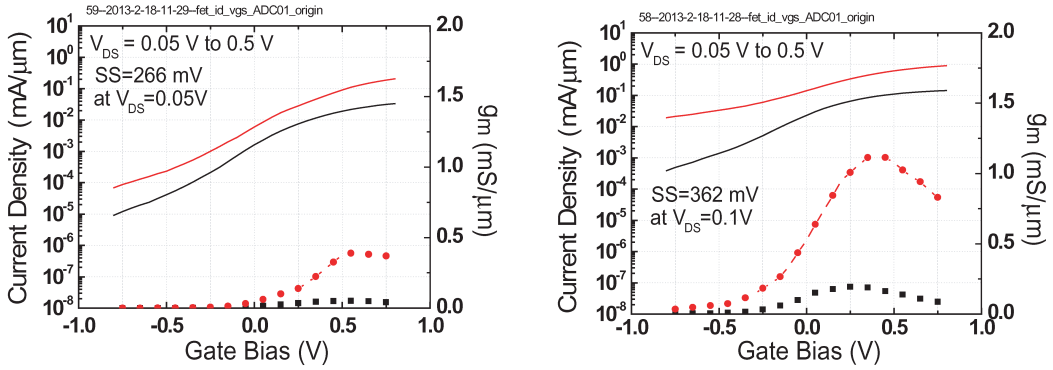
6.2.8 Gate Last Lot B8: Channel Thickness Series

To assess the scaling potential of the MBE regrowth process, a sample lot with two channel thicknesses were fabricated. 10 nm and 7.5 nm InGaAs channels were processed simultaneously. Due to the serial nature of MBE, regrowth may be different on each sample due to fluctuations in surface cleaning and general regrowth conditions. Also, for this regrowth, tellurium was not used for regrowth doping. The Te cell was near end-of-life, and could not be used for reliable or repeatable doping levels.

Figure 6.25 shows peak g_m maps across the 10 and 7.5 nm channels. The 10 nm channel showed worse performance when compared to similar lots, with only

Gate Last B8			
Channel Thickness	varied	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MBE	Regrowth Spec	InAs, 50 nm
Epi Lot #	121216F (10 nm ch.)	Regrowth Doping	Si
	121216D (7.5 nm ch.)		

Table 6.7: Gate Last Lot B8 Process Specifications



(a) Lot B7b: 1 micron L_g (as drawn) J_d-V_{ds} (b) Lot B7b: 50 nm L_g (as drawn) J_d-V_{ds}

Figure 6.24: Lot B7b: J_d-$V_{ds}$for 1 micron and 50 nm L_g(as drawn).

0.6 mS/micron at 0.5 V_{ds} for the shortest gate length ($\sim$ 60 nm). 7.5 nm channel thickness saw even lower performance, with 0.25 mS/micron peak transconductance, with most devices much worse. The lack of performance could be due to the lack of tellurium in the MBE regrowth, or contamination in the ALD. The decrease in performance with the 7.5 nm channel suggests MBE regrowth cannot make adequate contact to thin MOSFET channels.

6.3 Gate Last: MBE Regrowth Discussion

MBE source-drain regrowth provides low access resistance contacts to InGaAs MOSFETs. The use of tellurium in the MBE regrowth improves semiconductor morphology, and tends to improve on-state device performance. The use of commercial epitaxial material also improves device performance compared to university-grown material. Subthreshold swing with MBE was never lower than $\sim$ 120 mV/dec, and did not improve using alternative surface treatments. The process failure in B8 suggests MBE regrowth is not a reliable process. Also, performance decreased

	A	B	C	D	E	F
1	N/A	N/A				
2	N/A	N/A	N/A			
3	N/A	Blank	N/A	N/A		
4	0.56	Blank	0.56	0.41	0.53	
5	0.54	0.6	0.52	0.37	0.57	X
6	0.5	0.46	0.41	0.57	0.59	0.33

(a) Lot B8: 10 nm channel thickness g_m map

	A	B	C	D	E	F
1				X	0.04	X
2			0.13	0.2	0.06	X
3		X	0.18	X	0.15	X
4	X	X	X	X	Blank	0.37
5	X	0.18	0.18	0.25	0.19	Blank
6	X	0.19	X	0.11	X	X

(b) Lot B8: 7.5 nm channel thickness g_m map

Figure 6.25: Lot B8: 50 nm L_g (as drawn), peak g_m (0.5 V_{ds}) wafer map. BD = blank die, X = non-functional device, N/A = no data recorded.

with thinner channels; thin channels are imperative to improving device performance by moving the channel wavefunction closer to the surface. MBE regrown source-drain devices with lower back barrier delta doping have shown decreased performance [6]; decreasing or removing delta doping is also critical for improving device performance. MBE regrowth development for thin channels and channels without delta doping would be process-intensive and time consuming. Therefore, MOCVD regrowth was explored.

6.4 Gate-Last MOSFET Process Flow (MOCVD)

After finding a lack of reproducibility and device scaling with MBE regrowth, MOCVD regrowth was pursued. MOCVD regrowth is known to work well for photonic devices [15] and for III-V MOSFETs [12],[13]. The process flow for MOCVD

Gate Last C1			
Channel Thickness	10 nm	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MOCVD	Regrowth Spec	InGaAs, 30 nm
Epi Lot #	121216F	Regrowth Doping	Si

Table 6.8: Gate Last Lot C1 Process Specifications

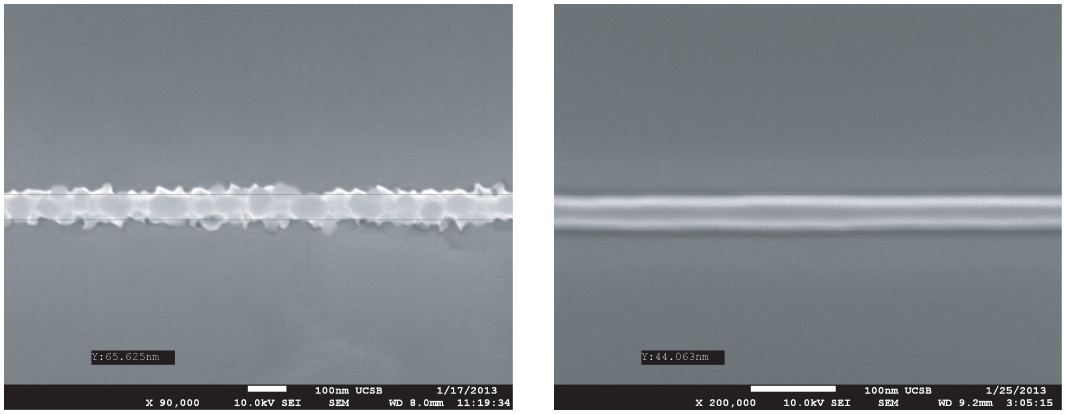
regrowth is very similar to MBE regrowth, and will be briefly summarized.

The PECVD SiO_xdummy gate is shortened since photoresist planarization is no longer required. This allows the dummy gate mask to be only photoresist and still maintain a vertical dry etch. Also, MOCVD does not grow on the SiO_xdummy gate; a foot at the bottom of the dummy gate merely increases gate length, rather than overgrow. *Ex-situ* regrowth surface preparation is identical to MBE surface preparation. Inside the MOCVD chamber, the samples are heated to remove native oxide, and material is regrown. After regrowth, since MOCVD regrowth is selective, planarization of the dummy gate is not required. Processing proceeds as defined in the MBE regrowth process.

A large number of process lots were processed using MOCVD source-drain regrowth. Below is a select review of those process lots. These lots capture the performance possible with MOCVD source-drain regrowth.

6.4.1 Gate Last Lot C1: Initial result, comparison with MBE

A process lot using existing epi (121216F) was done. This is the same epi that was used for Lot B8 (10 nm channel), allowing for direct comparison of MBE and MOCVD regrowth. Figure 6.26 shows SEM images of Lot B8 (MBE) and Lot C1



(a) Lot B8: 10 nm channel, post-MBE regrowth

(b) Lot C1: 10 nm channel, post-MOCVD regrowth

Figure 6.26: SEM images of dummy gates after source-drain regrowth

(MOCVD) just after source-drain regrowth. B8 dummy gates are covered in polycrystalline InAs, which is removed with photoresist planarization and wet etching. C1 dummy gate is virtually free of InGaAs.

Unlike B8, long and short gate lengths show performance equivalent to that of previous MBE regrowth lots (6.27), confirming epi quality was not the reason for Lot B8 poor performance. However, C1 devices show much worse off-state performance. Both long and short channel devices have larger than expected subthreshold swings (Figure 6.28). The dramatic increase in subthreshold swing has moved the threshold voltage negative.

Figure 6.29 shows a peak g_m map and R_{on} for C1. Again, we see the transconductance is high and similar across the sample for the short gate length devices. The R_{on} versus L_g is also encouraging, showing $\sim 250\ \Omega{\cdot}\mu m$ (double-sided) contacts. A fraction of this access resistance is the parasitic sheet resistances (40 $\Omega/\square$) from source-drain metal to channel gap and metal-semiconductor contact resistances. This is similar to that seen in Lot B4 (InGaAs MBE regrowth).

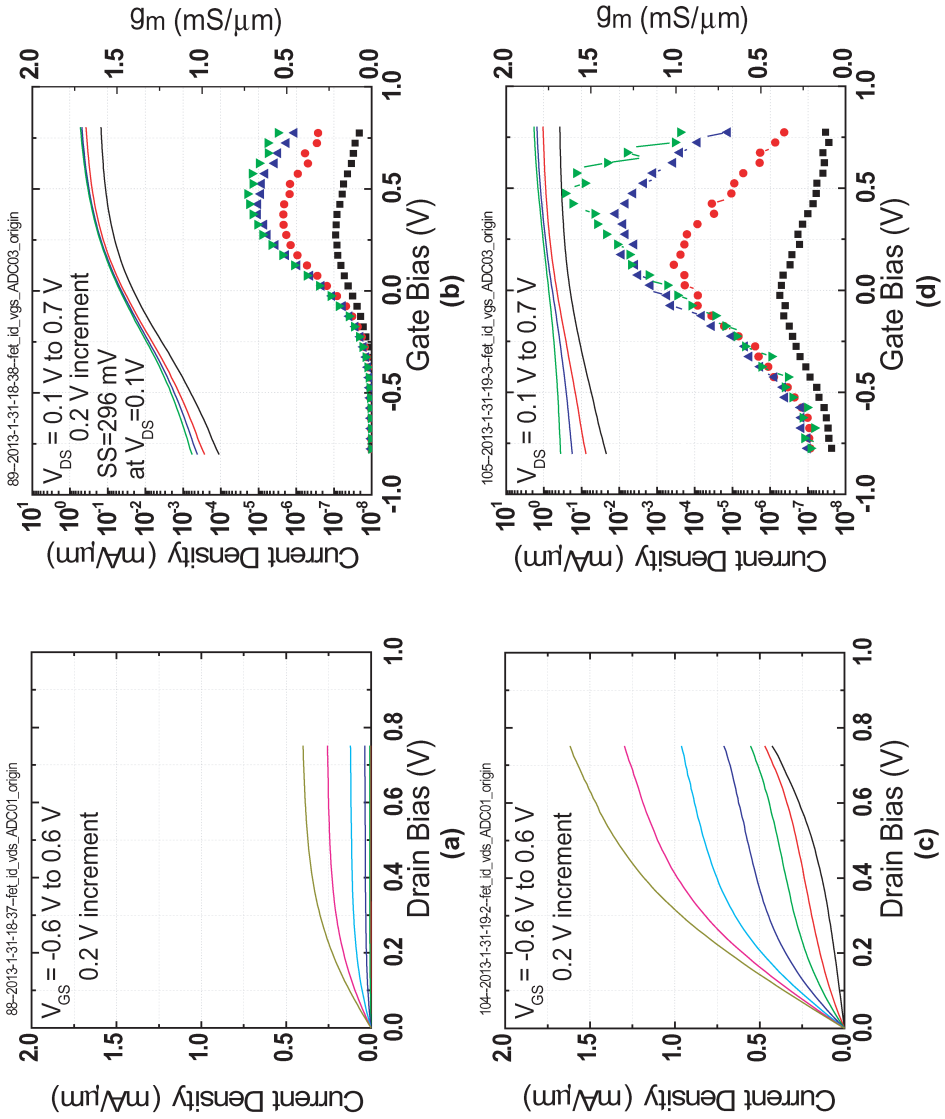


Figure 6.27: Lot C1: J_{drain}versus V_{ds} and V_{gs}. a) 501 nm L_g J_d-V_{ds} b)501 nm L_g J_d-V_{gs} c) 47 nm L_g J_d-V_{ds} d)47 nm L_g J_d-V_{gs}.

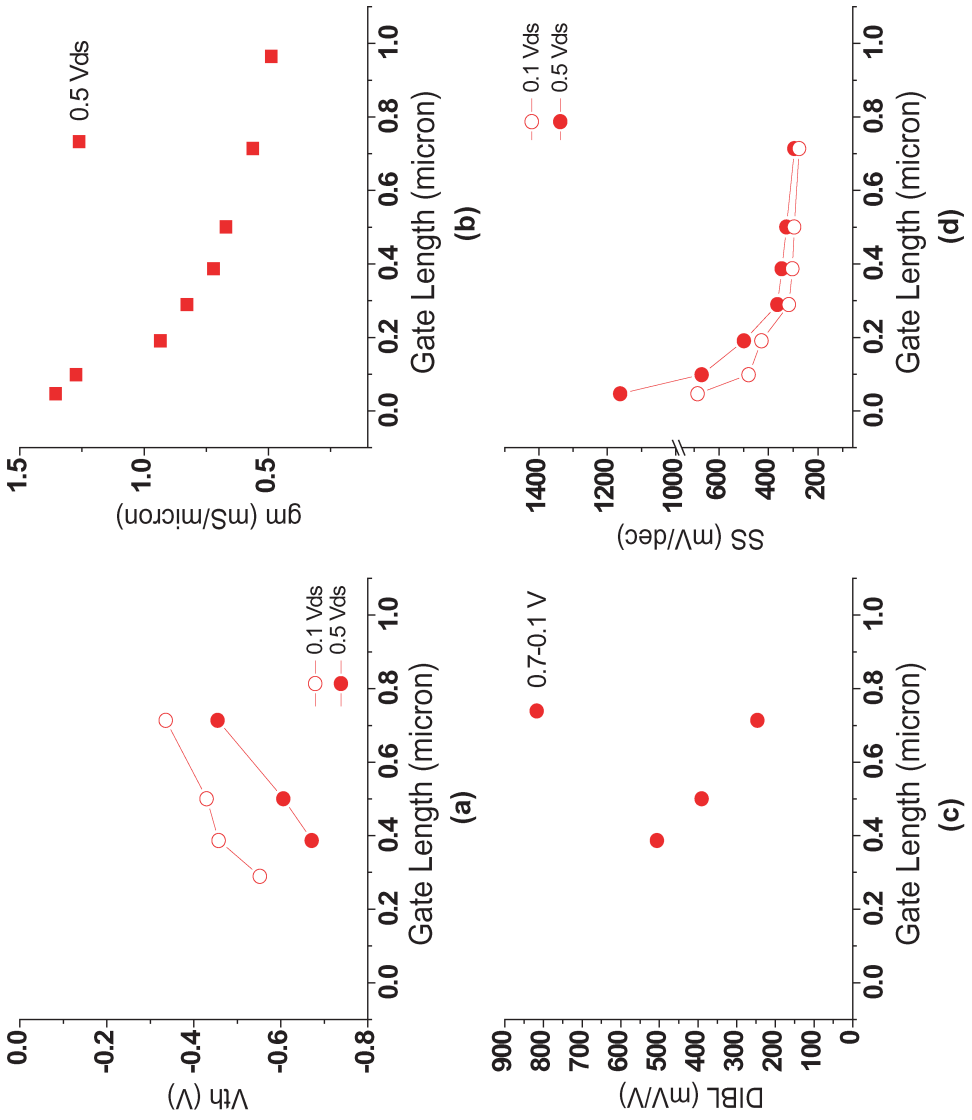
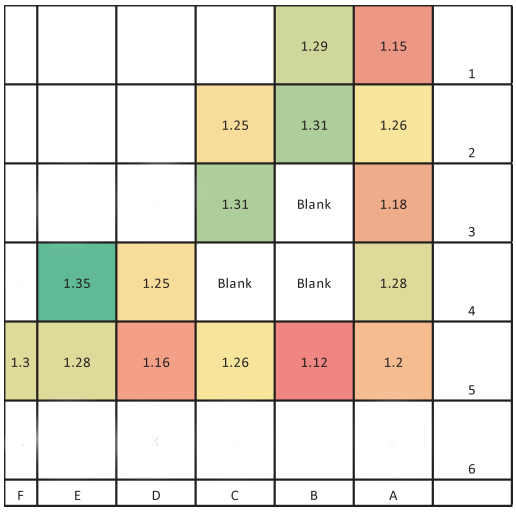
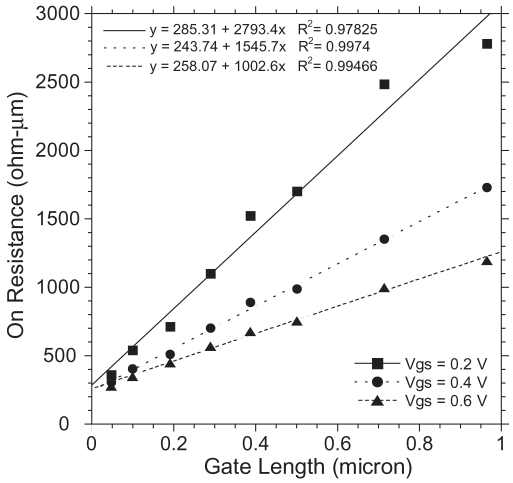


Figure 6.28: Lot C1: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.



(a) Lot C1: 50 nm L_g (as drawn), peak g_m (0.5 V_{ds}) wafer map



(b) Lot C1: R_{on} versus L_g

Figure 6.29: Lot C1: g_m wafer map and R_{on} versus L_g

6.4.2 Gate Last Lot C2: Channel Series (10, 7.5, 5)

Continuing the experiments of Lot B8, a channel thickness series was performed using MOCVD regrowth. It is important to scale the channel thickness to maximize C_{depth}. Since MBE regrowth was failing with thin channels, it is important to assess the MOCVD regrowth for the same epi. Figure 6.30 contains plots of J_d-V_{ds} and -V_{ds} for 10, 7.5 and 5 nm channels and short gate lengths (50 nm as drawn). Unlike Lot B8, these devices have adequate on-state performance. As the channel thickness was scaled, the threshold voltage of the devices increased. This is due to less channel sheet charge with decreasing thickness and eigenstate energy increase with decreasing channel thickness.

Gate-channel control is improved with decreasing channel thickness, as predicted by L_g-to-body thickness scaling. While the 10 nm channel has significant breakdown at high V_{ds} and negative V_{gs}, 7.5 and 5 nm channels do not. Output conductance

Gate Last C2			
Channel Thickness	varied	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MOCVD	Regrowth Spec	InGaAs, 30 nm
Epi Lot #	121216F (10 nm ch.)	Regrowth Doping	Si
	121216D (7.5 nm ch.)		
	121216C (5 nm ch.)		

Table 6.9: Gate Last Lot C2 Process Specifications

improves with decreasing channel thickness. Off-state performance also improves with decreasing channel thickness. Given the short gate length, short channel effects will dominate subthreshold swing. Decreasing the channel thickness improves gate control, and subsequently the subthreshold swing and DIBL. All three samples show buffer leakage at long gate lengths, preventing more accurate off-state analysis.

Figure 6.31 contains g_m maps for all three channel thicknesses. All samples show consistent transconductance across their areas. On-state performance is best with the 7.5 nm channel, and worst with the 5 nm channel. This may be due to mobility; as the channel thickness decreases, the channel control improves, but the mobility may decrease considerably, hurting overall device performance. This should not be an issue for ballistic FETs, but increased scattering due to decreased mobility requires even shorter gate lengths to witness ballistic transport. Therefore, some minimum mobility must be necessary.

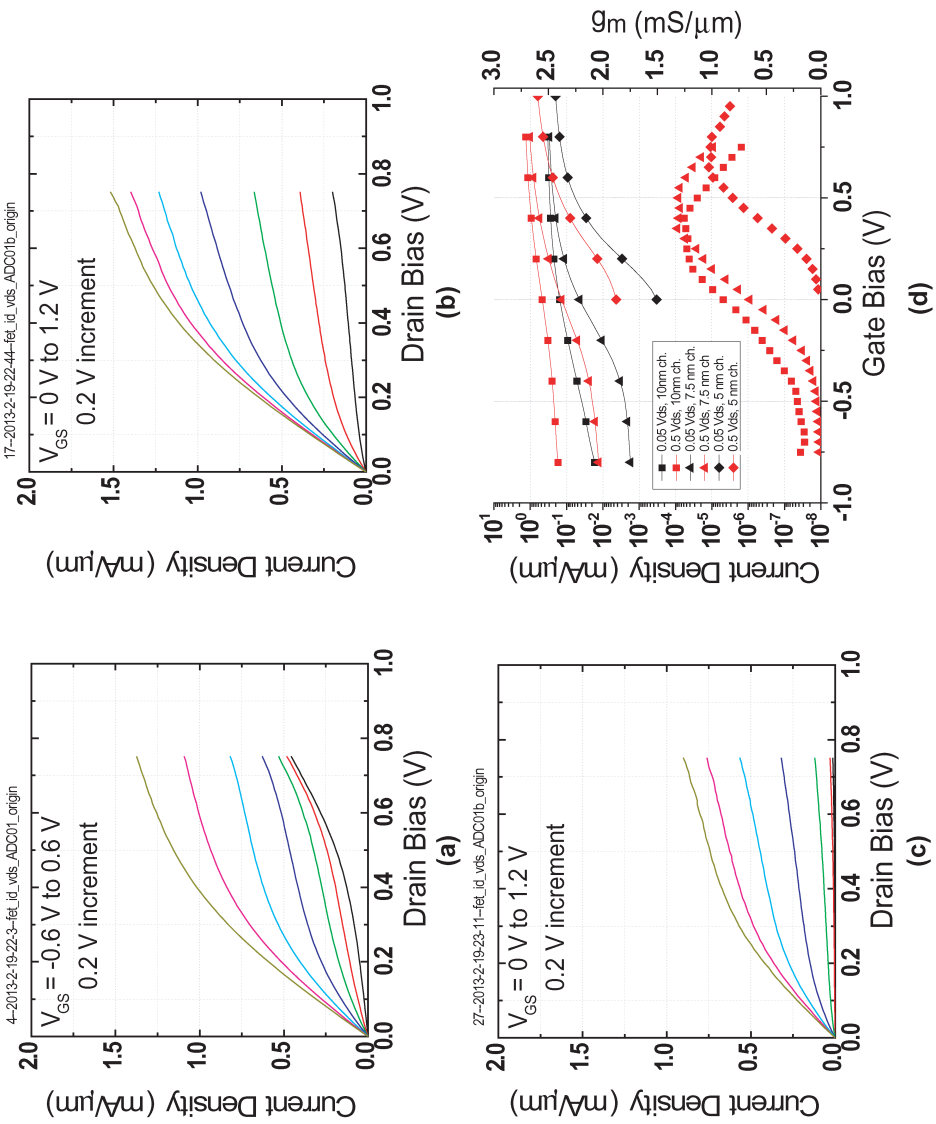


Figure 6.30: Lot C2: 50 nm L_g(as drawn) J_{drain}versus V_{ds} and V_{gs}. a) 10 nm channel J_d-V_{ds} b) 7.5 nm channel J_d-V_{ds} c) 5 nm channel J_d-V_{ds} d)10,7.5,5 nm channel J_d-V_{gs}.

Gate Last C3			
Channel Thickness	varied	Oxide Type	Al_2O_3+HfO_2
Delta doping	3 nm, 3.9×10^{12} cm^{-2}	Oxide Thickness	1 nm, 4 nm
Regrowth Type	MOCVD	Regrowth Spec	InGaAs, 30 nm
Epi Lot #	130130B (10 nm)	Regrowth Doping	Si
	130130B ($\sim$ 6.5 nm)		

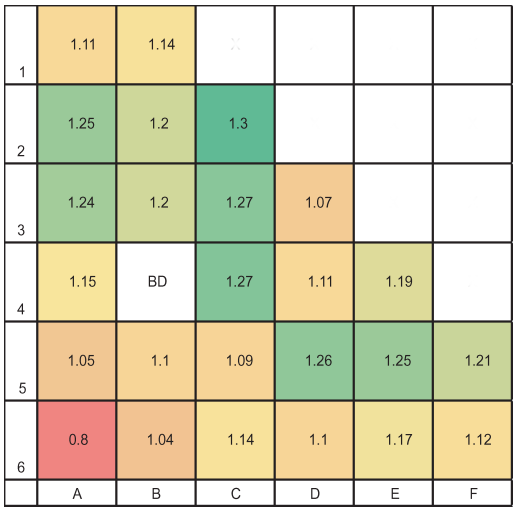
Table 6.10: Gate Last Lot C3 Process Specifications

6.4.3 Gate Last Lot C3: Digital etch: 0 cycle versus 2 cycle

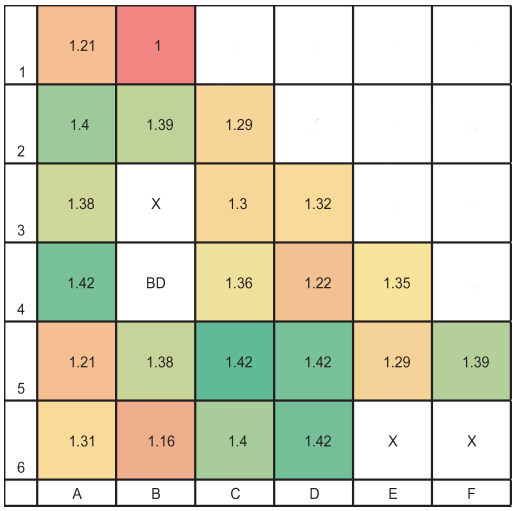
Due to a lack of success with InP channel capping (Lots B7a and B7b), alternative capping techniques had to be pursued. Rather than capping with InP, a heavily-doped InGaAs layer was grown above the channel surface [16]. This layer would be etched away using a recently developed digital etching process, offering nearly nanometer control over etch depth. This process immediately improved MBE re-growth gate last device performance.

Using epi that did not have an InGaAs capping layer, 10 nm InGaAs channel surfaces were etched to remove the damage region of the channel. Etching is done with cyclic UV ozone exposures and dilute HCl:DI etching. One quarter was left as a control sample, and one was etched with two cycles of treatment (UV, wet etch, UV, wet etch). The etch removes $\sim$ 1.2 nm per cycle, and the epi has about 1 nm of native oxide on it prior to any etching that is removed during dummy gate removal [6]. Etching occurs just prior to loading in the ALD loadlock.

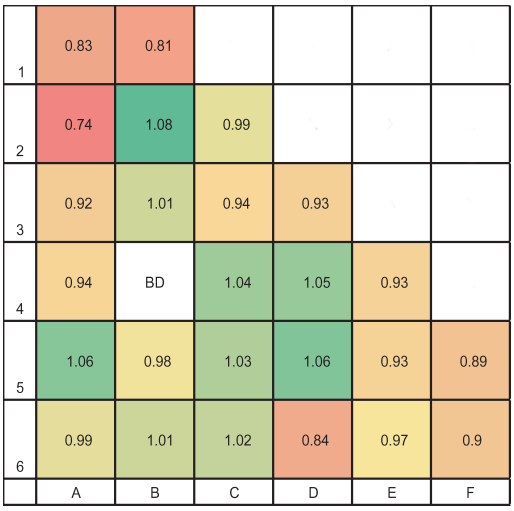
Comparing J_d-V_{ds} and V_{gs} data for C3 in Figures 6.32 and 6.33, it is evident that there is a large threshold voltage shift for unetched and etched samples. For the short gate length unetched sample, the high V_{ds} and negative V_{gs} breakdown is present, but not for the etched sample; this correlates with improved gate control, similar to Lot C2 thinner channels.



(a) Lot C2: 10 nm channel wafer map



(b) Lot C2: 7.5 nm channel wafer map



(c) Lot C2: 5 nm channel wafer map

Figure 6.31: Lot C2: 50 nm L_g (as drawn), peak g_m (0.5 V_{ds}) wafer map. BD = blank die, X = non-functional device.

Figure 6.33 demonstrates the off-state performance. DIBL and subthreshold swing improve considerably with channel etching. This correlates to the damaged interfacial layer providing large interface trap density. Comparing this to MBE regrowth lots, the subthreshold swing is now comparable to that found in MBE regrowth processes without channel etching. It is likely that the higher temperature MOCVD regrowth (600°C versus 500°C) increases interface density.

All figures of merit have been improved with channel etching (Figure 6.34). The increased channel control due to the decreased interface trap density and thinner body are shown in more positive threshold voltage, reduced DIBL, and reduced subthreshold swing for all gate lengths. A moderate improvement in transconductance is also seen with channel etching. Figure 6.35 shows g_m maps for both samples. For the unetched sample, peak transconductances are lower than similarly processed Lot (C1, C2). For the etched sample, improved transconductance was seen across the sample.

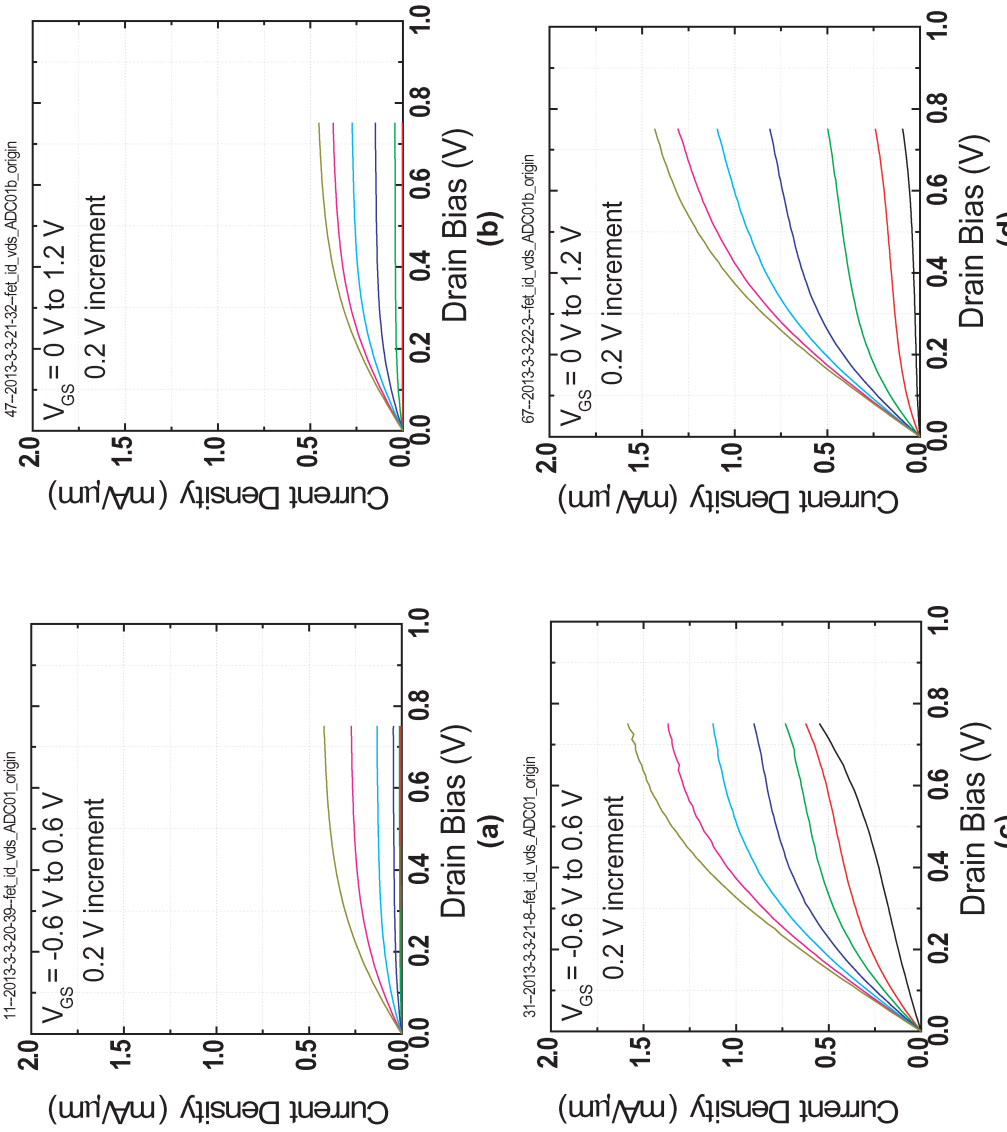


Figure 6.32: Lot C3: J_{drain} versus V_{ds}. a) 512 nm not etched b)508 nm etched c) 68 nm not etched d)65 nm etched

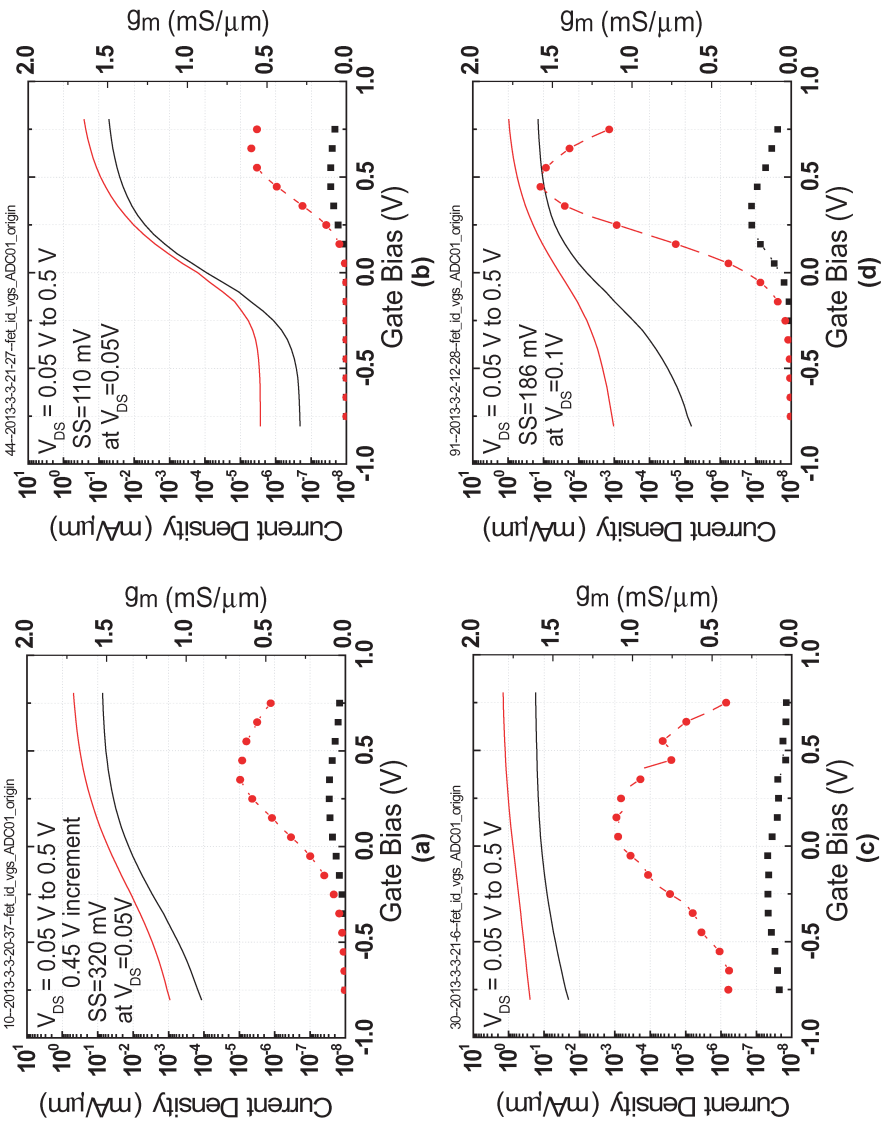


Figure 6.33: Lot C3: J_{drain} versus V_{gs}. a) 512 nm not etched b)508 nm etched c) 68 nm not etched d)65 nm etched

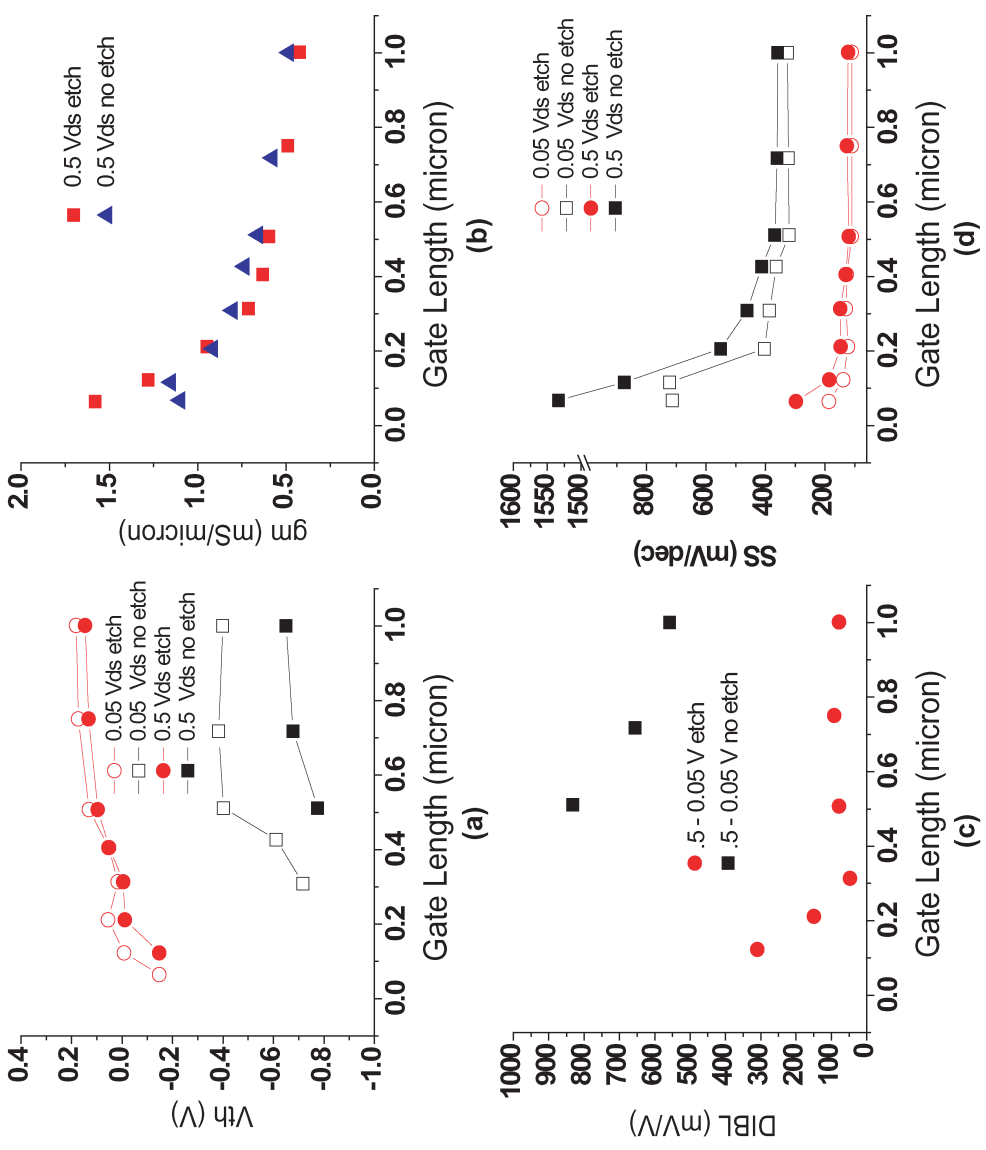
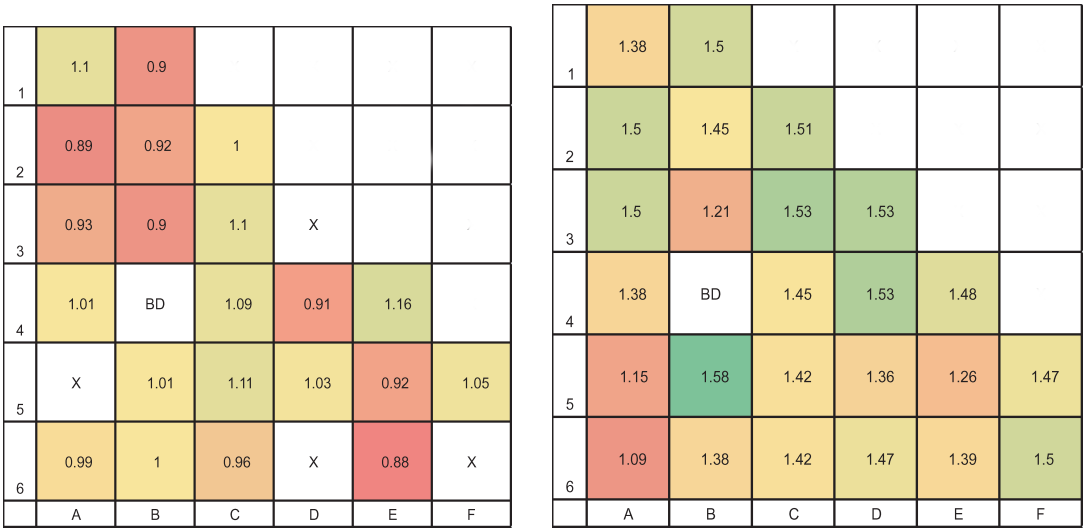


Figure 6.34: Lot C3: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.



(a) Lot C3: No channel etching g_m map

(b) Lot C3: 2 cycle channel etching g_m map

Figure 6.35: Lot C3: 50 nm L_g (as drawn), peak g_m (0.5 V_{ds}) wafer map. BD = blank die, X = non-functional device.

6.4.4 Gate Last Lot C4: Less delta doping, 2 cycle versus 3 cycle etching

From Lot C3, it is clear the channel etching is necessary for improving device performance. The damage layer prevents device improvement, and the channel etching provides a simple way to thin device channels and therefore improve $C_{gate-channel}$. Therefore, it is worth exploring scaling channel thickness using this technique. One

Gate Last C4			
Channel Thickness	varied	Oxide Type	HfO_2
Delta doping	3 nm, 2×10^{12} cm^{-2}	Oxide Thickness	4 nm
Regrowth Type	MOCVD	Regrowth Spec	InGaAs, 30 nm
Epi Lot #	130130A ($\sim$ 6.5 nm)	Regrowth Doping	Si
	130130A ($\sim$ 5.2 nm)		

Table 6.11: Gate Last Lot C4 Process Specifications

sample was thinned two cycles ($\sim$ 6.5 nm channel) and the other three cycles ($\sim$ 5.25 nm channel).

In this lot, delta doping was also decreased to 50% standard (2×10^{12} cm^{-2} versus 4×10^{12} cm^{-2}) to move the channel wave function closer to the surface. Given the success with MOCVD and thin channels, it was predicted the decreased delta doping would not affect device performance. Last, this and the two following Lots (C5, C6) use HfO_2-only gate insulators, rather than bi-layers. When combined with the N_2/TMA treatment, low interface trap densities are possible.

As expected, the two devices see a threshold voltage shift from channel thinning (Figure 6.36). Transconductance has decreased for both short and long gate lengths. Off-state performance has improved for the thinner channel (Figure 6.37). Improved DIBL and subthreshold swing are seen for the thinner channel. See Figure 6.38. Threshold voltage moves positive for the thinner channel, as expected. The short channel roll-off is better than that for the thicker channel, consistent with better gate control. DIBL and subthreshold swing also improved at all gate lengths, suggesting decreased interface trap density for the thinner channel. This could be due to the damage layer extending deeper than two cycles of digital etching. It could also be due to a favorable surface Fermi level position for the thinner sample (see Chapter 3). Long channel subthreshold swing increase is due to buffer leakage currents affecting SS extraction. The peak transconductances are all worse for the thinner channel. This is likely due to a lower channel mobility for the thinner channel (see Section 6.5).

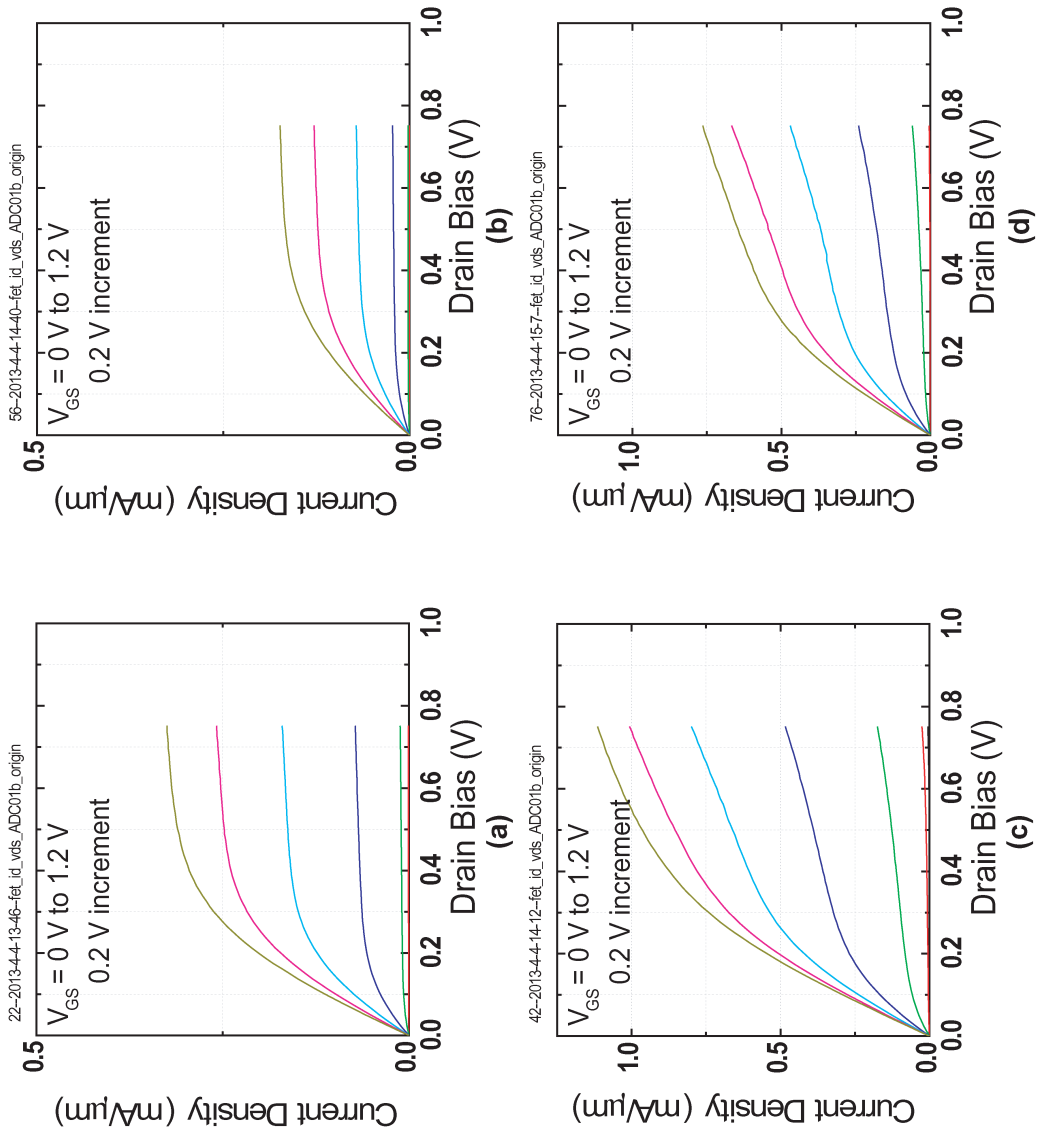


Figure 6.36: Lot C4: J_{drain}versus V_{ds}. a) 524 nm 2 cycle etch b)501 nm 3 cycle etch c) 68 nm 2 cycle etch d)47 nm 3 cycle etch

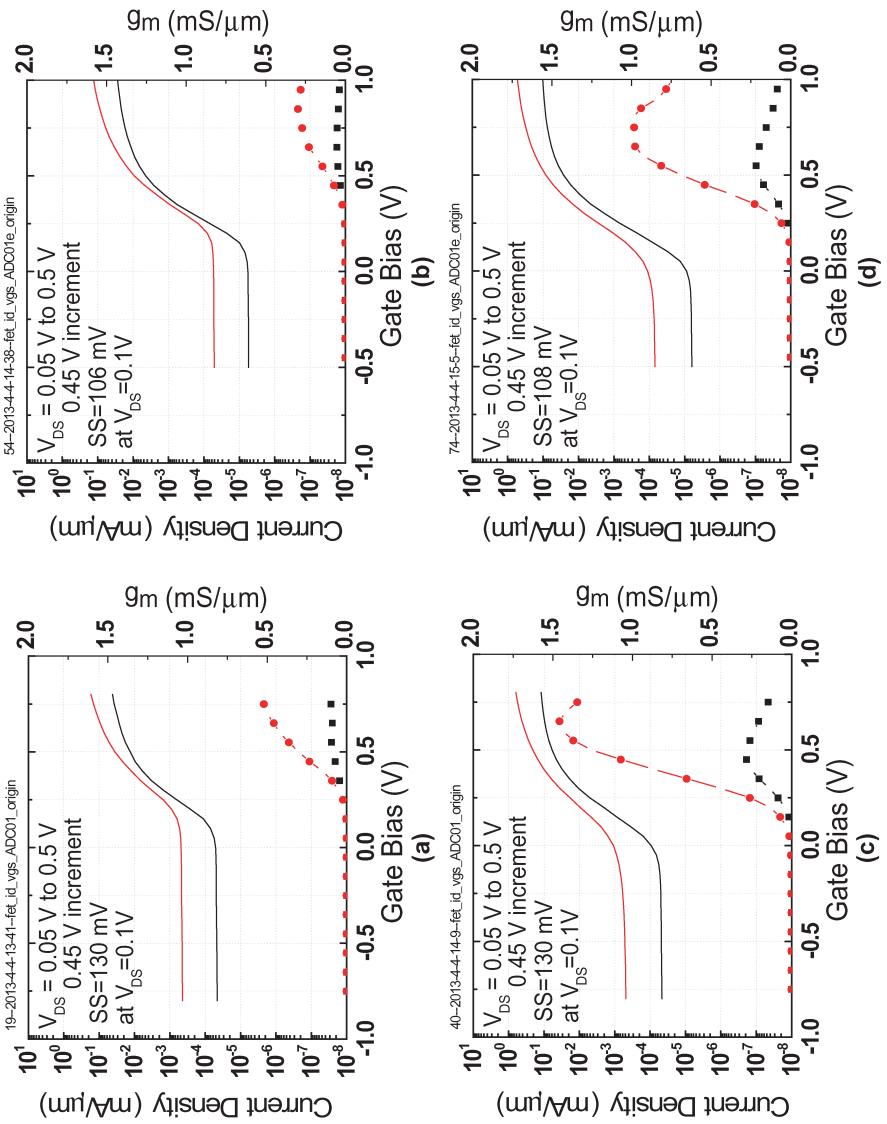


Figure 6.37: Lot C4: J_{drain}versus V_{gs}. a) 524 nm 2 cycle etch b)501 nm 3 cycle etch c) 68 nm 2 cycle etch d)47 nm 3 cycle etch

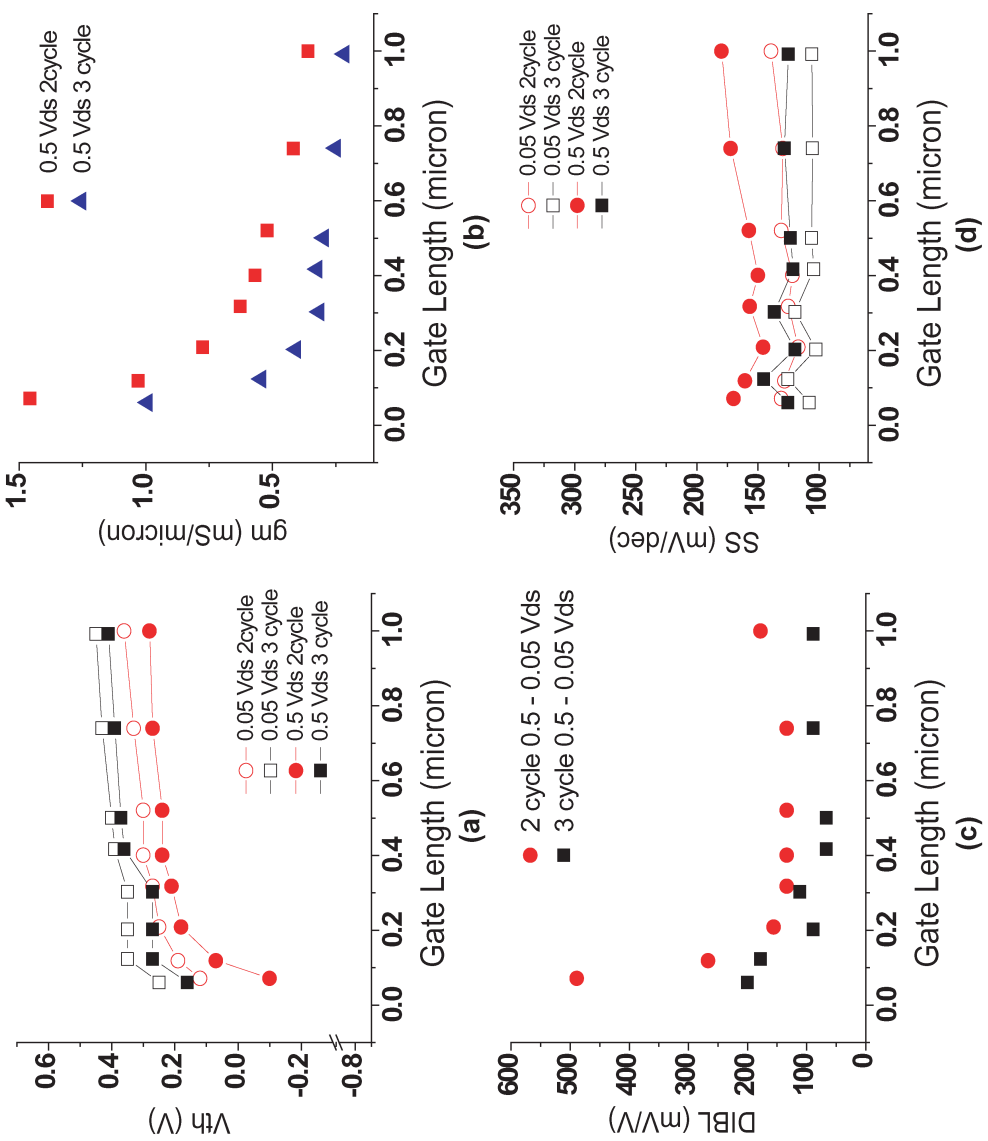


Figure 6.38: Lot C4: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

Gate Last C5			
Channel Thickness	$\sim$ 6.5 nm	Oxide Type	HfO_2
Delta doping	3 nm, varied	Oxide Thickness	4 nm
Regrowth Type	MOCVD	Regrowth Spec	InGaAs, 60 nm
Epi Lot #	130130B 4×10^{12} cm^{-2}	Regrowth Doping	Si
	130130A 2×10^{12} cm^{-2}		
	130227B 1×10^{12} cm^{-2}		

Table 6.12: Gate Last Lot C5 Process Specifications

6.4.5 Gate Last Lot C5: Delta Doping Series

Delta doping of the back barrier has effects on three important parameters: threshold voltage control, electron wave function depth, and surface Fermi level position. Threshold voltage control is an important tool for VLSI design, but this is better controlled with metal work function. Electron wave function depth must be kept shallow for best gate control, and consequently optimal interface trap density. However, less delta doping may impact source-drain charge. Therefore, a series of delta doping concentrations was explored. Given the deleterious effects of three cycle digital etching in Lot C4, all samples experienced two cycles. HfO_2 and N_2/TMA treatment was employed for this lot. Regrowth thickness was also increased to 60 nm to improve access resistance.

Figure 6.39 shows J_d-V_{ds} and -V_{gs} for Lot C5. Consistent with theory, and similar to channel thickness scaling (Lot C2), the delta doping affects the threshold of all three samples, moving V_{th} positive. Also similar to C2, the decreased delta doping improves DIBL at short gate lengths.

Figure 6.40 characterizes V_{th}, g_m, DIBL, and subthreshold swing for all three samples. Less delta doping decreases threshold voltage roll-off for short gate lengths. DIBL is similar across samples for long gate lengths, but better at short gate

lengths for less delta doping. Transconductance decreased with delta doping. Peak transconductance for 50% delta doping was only about 1 mS/micron at 0.5 V_{ds}, even though this epi lot was the same used in Lot C4. This suggests variation during ALD gate insulator deposition affecting channel mobility (see Section 6.5).

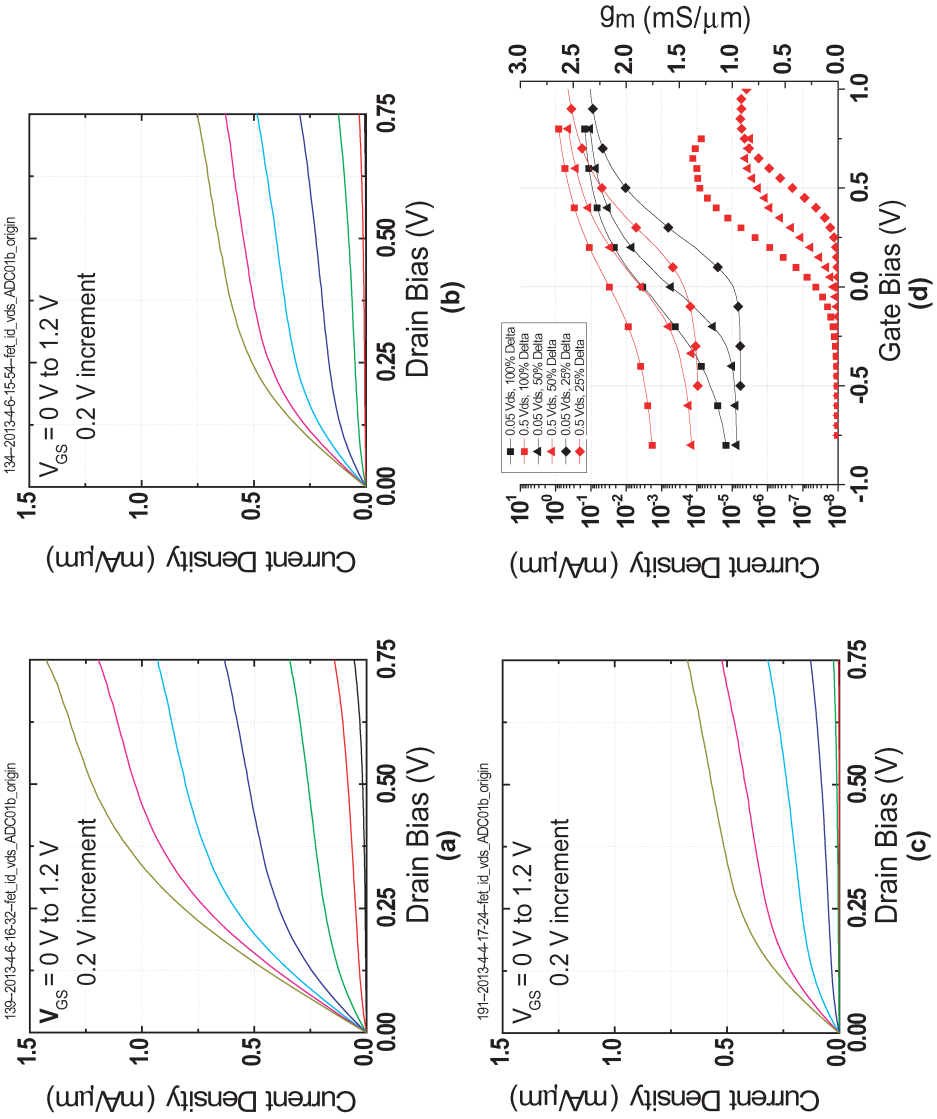


Figure 6.39: Lot C5: Short L_g V_{ds} and V_{gs}. a) 100% delta doping J_d-V_{ds} b) 50% delta doping J_d-V_{ds} c) 25% delta doping J_d-V_{ds} d)100,50,and 25% J_d-V_{gs}.

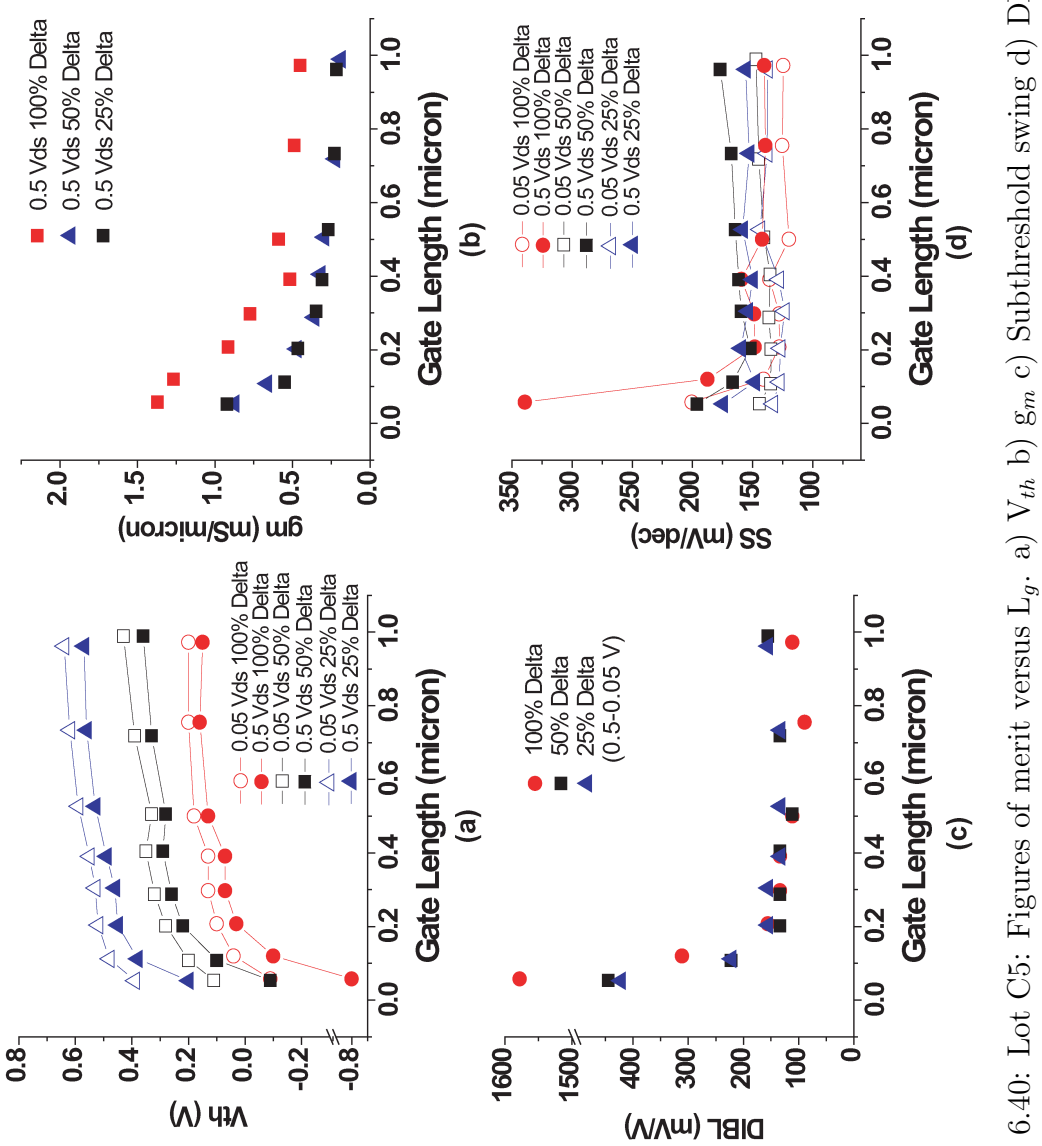


Figure 6.40: Lot C5: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

Gate Last C6			
Channel Thickness	$\sim$ 6.5 nm	Oxide Type	HfO_2
Delta doping	3 nm, 4×10^{12} cm^{-2}	Oxide Thickness	4 nm
Regrowth Type	MOCVD	Regrowth Spec	InGaAs, 60 nm
Epi Lot #	1302227A	Regrowth Doping	Si

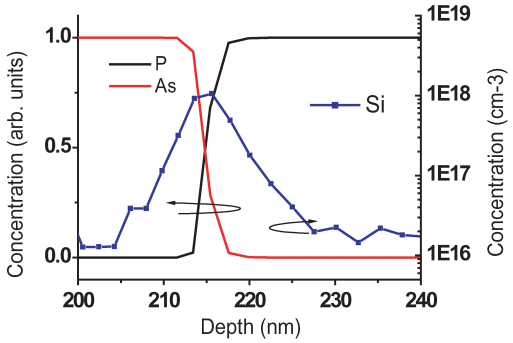
Table 6.13: Gate Last Lot C6 Process Specifications

6.4.6 Gate Last Lot C6: PIN Back Back Barrier

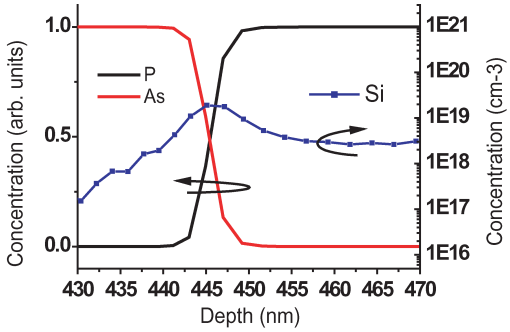
Examining previous lot data at negative V_{gs} and various V_{ds}, a random source-drain leakage current is universally present at all gate lengths. At long gate lengths, the leakage tends to have an ohmic response. This is most likely a buffer or back barrier leakage resistance. This resistance prevents accurate subthreshold measurements of FETs.

Device buffer leakage is not a new phenomenon. It has been seen in MBE [17] and MOCVD grown devices [18]. Theoretically, epitaxial material has few defects. However, initial growth on substrates, even lattice-matched, is imperfect. During initial MBE growth, an "epi-ready" oxide is removed by thermal desorption, and "buffer" material is grown. Since phosphorus is not available at UCSB, the buffer is InAlAs. Fluctuations in oxide desorption and buffer growth can lead to crystal defects. Buffers are grown to terminate these defects.

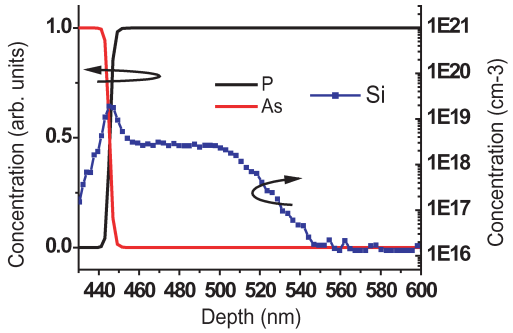
Another effect is unintentional silicon at the epi/substrate interface. During "epi-ready" preparation, silicon accumulates on the InP surface. Figure 6.41 contains SIMS profiles of IQE and UCSB epi material. For UCSB epi, there is a large amount of silicon in the buffer and in the InP wafer. IQE epi has a Si spike at the surface, but not in the buffer or the InP substrate. Even though the InP wafer is semi-insulating, the Fe concentration is typically low, 5×10^{16} cm^{-3}, not enough to



(a) Commerical epi, buffer/substrate interface



(b) UCSB epi, buffer/substrate interface

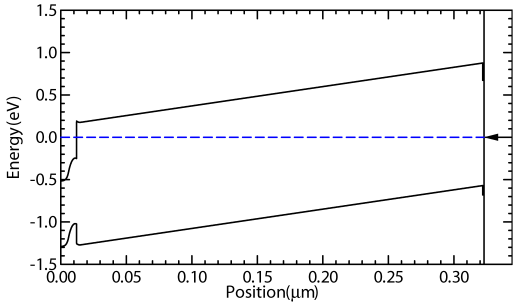


(c) UCSB epi, buffer/substrate interface

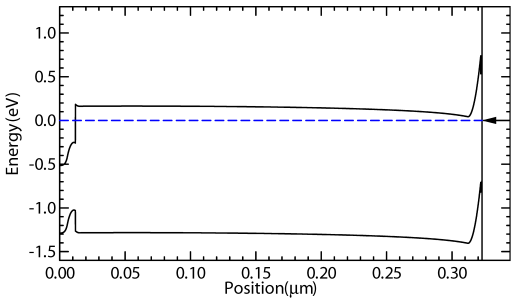
Figure 6.41: SIMS data for UCSB epi and Commercial epi

deplete the silicon doping.

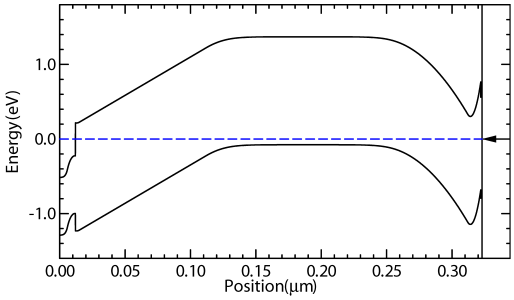
Figure 6.42 contains electron band diagrams under the source-drain region with and without this interfacial silicon. This silicon can increase back barrier mobile charge significantly, creating the parasitic resistance witnessed in UCSB epi material. C8 epi design has 100% delta doping, a 100 nm InAlAs NID setback region, and the remaining InAlAs doped to a density of 3×10^{17} cm^{-3} Be (p-doping). Figure 6.42c is an electron band diagram of Lot C8 in the source-drain region. The low p concentration and setback are to prevent source-to-buffer tunneling currents. The low p concentration also minimizes depletion of the delta doping.



(a) Ideal back barrier/buffer



(b) Buffer with 10 nm, 1×10^{19} cm^{-3} n-type spike



(c) Same as b, with 200 nm 3×10^{17} cm^{-3} p-type compensation

Figure 6.42: Electron band diagrams for back barrier doping levels

As shown in Figure 6.43, C6 shows the lowest device leakage currents, $\sim 1\times10^{-8}$ mA / micron, at long gate lengths. However, at short gate lengths, short channel effects still dominate, even with $\sim$ 6 nm channel thickness. This is due to the 100% delta doping employed. However, 48 nm gate length has a peak transconductance of 2 mS/micron at 0.5 Vds, the highest of any lot in this dissertation.

Figure 6.44 shows that V_{th} is similar to Lot C5 100% delta doping, confirming the p-doping did not affect the delta doping. Due to the low leakage, C6 has very low long-channel DIBL and subthreshold swing. The peak transconductance is also high for all transconductances. As Figure 6.45 shows, the low R_{on} is due to increased regrowth thickness, decreasing its sheet resistance by a factor of two.

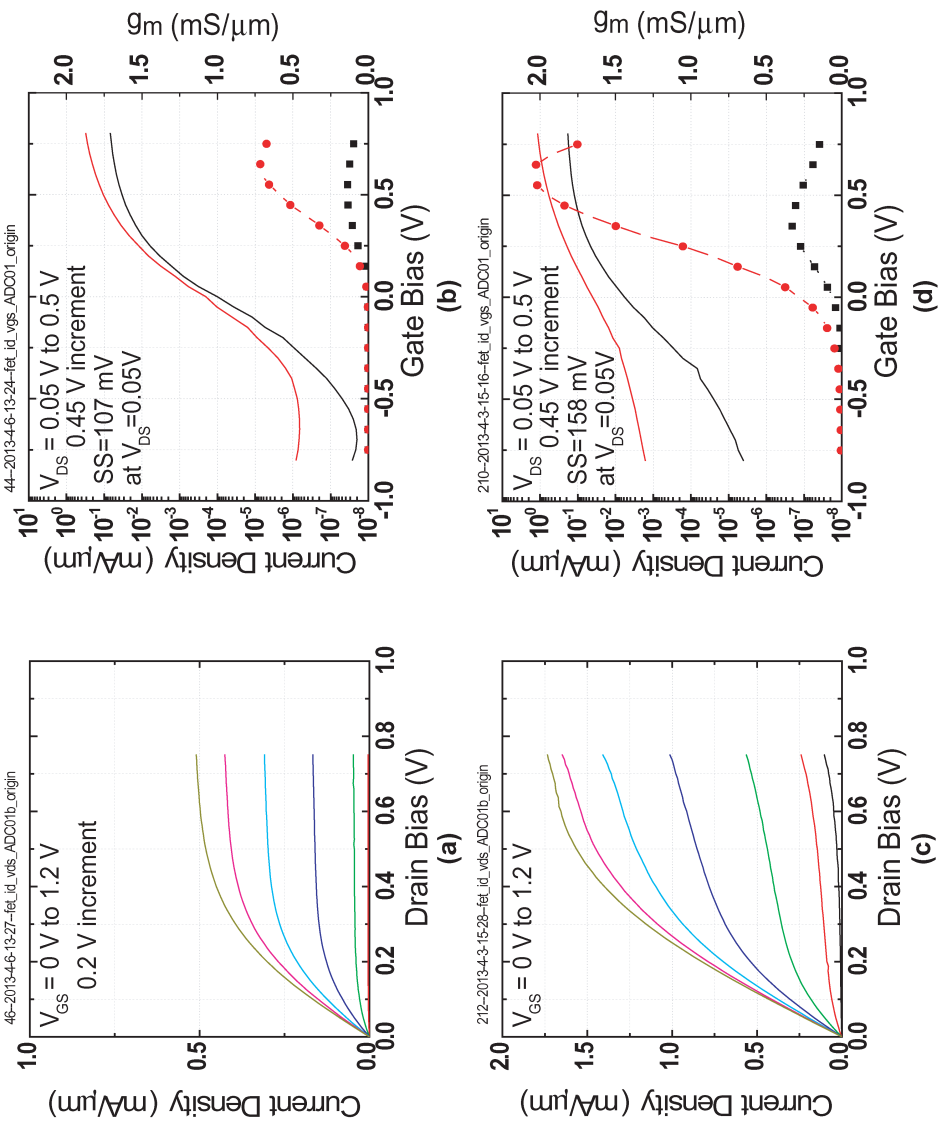


Figure 6.43: Lot C6: J_{drain}versus V_{ds} and V_{gs}. a) 494 nm L_g J_d-V_{ds} b)494 nm L_g J_d-V_{gs} c) 48 nm L_g J_d-V_{ds} d)48 nm L_g J_d-V_{gs}.

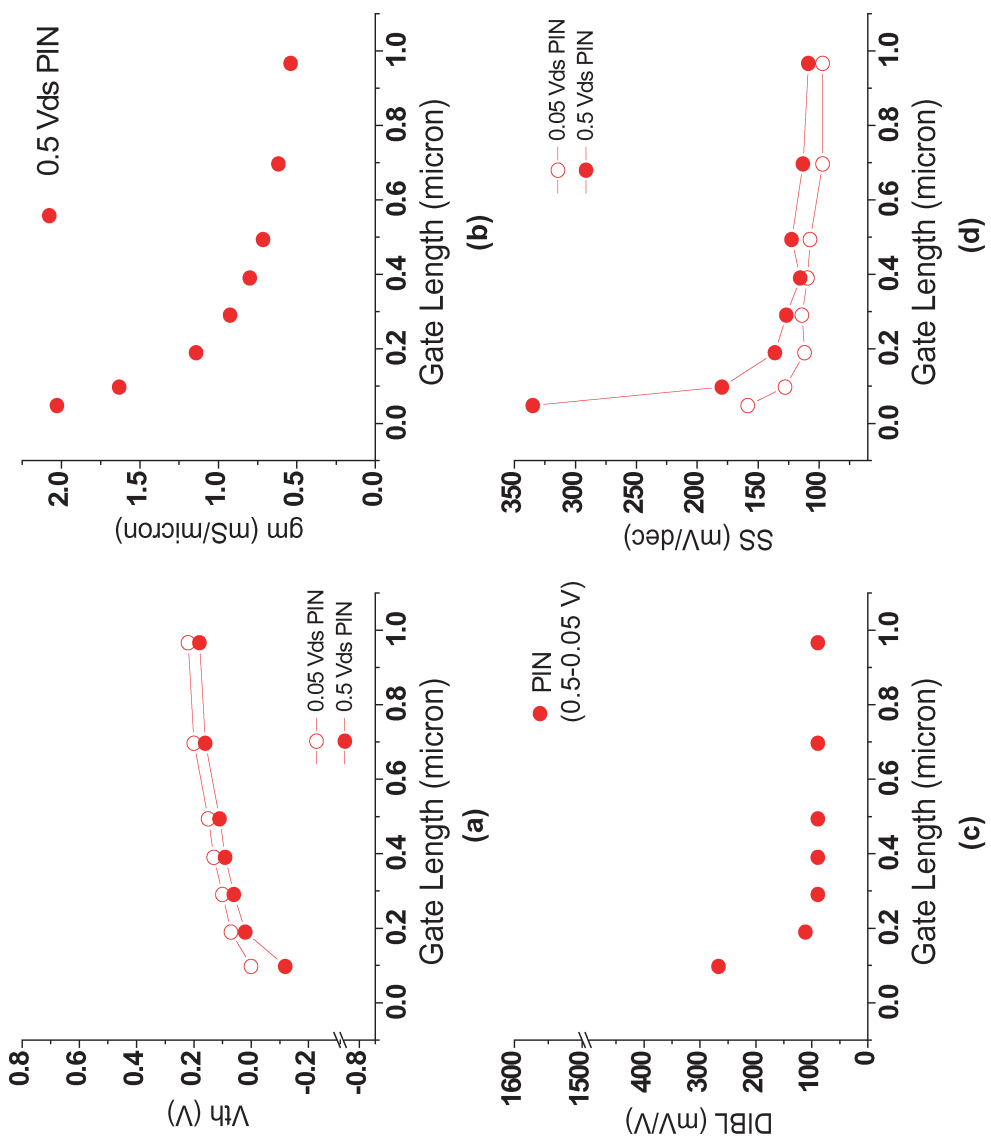


Figure 6.44: Lot C6: Figures of merit versus L_g. a) V_{th} b) g_m c) Subthreshold swing d) DIBL.

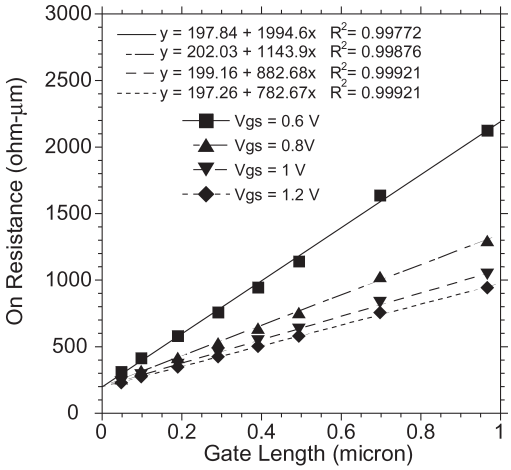


Figure 6.45: Lot C6: R_{on} versus L_g.

6.5 Gate Last: On-Wafer CV Measurements and Effective Channel Mobility

The previous sections dealt with DC IV data for various III-V MOSFET samples with varying regrowth type, gate insulator, and epitaxial design. However, this data cannot independently explain all the phenomena and trends found. Epitaxial growth can vary run-to-run, even for the sample wafer design. Cleanroom processing chambers vary as well; it is likely each ALD gate insulator deposition is different run-to-run. Another on-wafer measurement is needed to gain further insight into these measurements.

On-wafer CV measurements can reveal channel charge density as a function of gate bias. Given the low capacitance density of C_{g-ch} ($\sim$15 fF per μm^2), a relatively large-area device is required to measure an appreciable capacitance with a standard impedance analyzer and moderate ($\sim$ MHz) frequencies. Furthermore, parasitic gate overlap capacitances must be smaller than the overall measured capacitance to

be negligible. Gate-last processing (MBE or MOCVD) currently requires overlaps on the order of 200 to 400 nm of lateral gate metal along the gate width. This is to prevent gate metal misalignment in the optical photostepper. Gate lengths on the order of 20 microns are therefore required. Gate-last MBE processing was not amenable to gate lengths longer than 1 micron due to the nature of photoresist planarization. MOCVD processing is selective growth; therefore, photoresist planarization is not required to remove regrowth debris. Transistor Lots C4, C5, and C6 included large area devices (20 micron L_g, 25 micron W_{gate}), allowing their gate capacitance to be measured.

Extraction of channel charge density as a function of gate bias requires a few assumptions. First, the capacitance measured is entirely that of mobile channel charge. Interface trap response adds to the capacitance, but this charge is not mobile and does not increase device current densities. Back-barrier (InAlAs) charge could also be measured, if the semiconductor Fermi level approaches the conduction band edge of the back barrier. This would also increase measured capacitance density. Second, the gate metal source-drain overlap is negligible compared to the channel area. This ensures the measured capacitance is strictly in the channel region.

After capacitance is measured and normalized to gate area, one integrates capacitance with respect to gate voltage:

$$Q_{channel} = \frac{1}{q \int_{V_0}^{V} C_{measured}\, dV} \tag{6.5.1}$$

Mobility as a function of channel charge can also be extrapolated from the capacitance data. A key assumption is that the transistor channel is ohmic at low drain bias, and its resistivity is proportional to its mobility and charge density:

$$R_{channel} = \frac{1}{q\mu n_{sheet}} \tag{6.5.2}$$

Measurement of this resistance was taken at various gate biases with 0 to 10 mV V_{ds}. It is assumed that the channel resistance is much larger than the parasitic access resistance (due to both metal-semiconductor access resistance and semiconductor gap sheet resistance), and therefore the total measured resistance is only that of the channel. By examining Lots C4, C5, and C6 R_{on} data and comparing the y-intercept to the 20 micron gate length resistance, we can conclude assumption is valid.

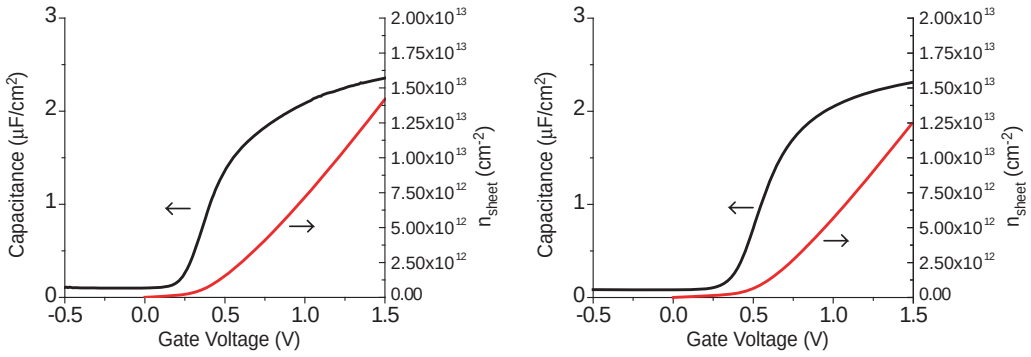
From Eqns. 6.5.1 and 6.5.2, the effective mobility is:

$$\mu_{effective} = \frac{1}{R_{channel} \int_{V_0}^{V} C_{measured}\, dV} \tag{6.5.3}$$

For all data sets, n_{sheet} integration started at 0V V_{gs}. All CV measurements were taken at 2.5 MHz.

6.5.1 CV: Lot C4 (2 cycle versus 3 cycle etching)

Figure 6.46 contains the CV and n_{sheet} curves for Lot C4. The CV curves are offset due to the threshold voltage shift from differences in channel thickness. Figure 6.47 is a plot of effective channel mobility versus sheet charge density for both samples. While the CV measurement confirmed similar sheet charge densities for both samples, the mobility for the 3 cycle etching decreased by more than 50%. This is likely due to the wavefunction proximity to the semiconductor surface, increasing electron scattering. It also explains the poor on-state performance seen in the DC



(a) 2 cycle etching

(b) 3 cycle etching

Figure 6.46: Lot C4: CV and n_{sheet} for 2 and 3 cycle channel etching.

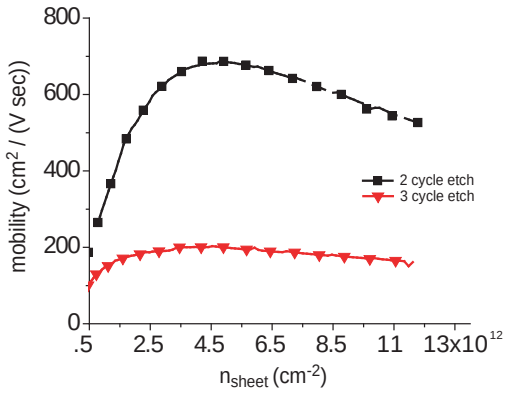


Figure 6.47: Lot C4: Effective mobility versus n_{sheet} for 2 and 3 cycle channel etching.

IV data (Figure 6.36).

6.5.2 CV: Lot C5 (Delta doping series)

Figure 6.48 shows the CV and n_{sheet} curves for Lot C5. The CV curves are offset due to the threshold voltage shift from delta doping. The maximum capacitances are as high as Lot C4, even though the same ALD recipe was run for both lots. Ellipsometry measurements of off-wafer silicon ALD witness samples confirm this

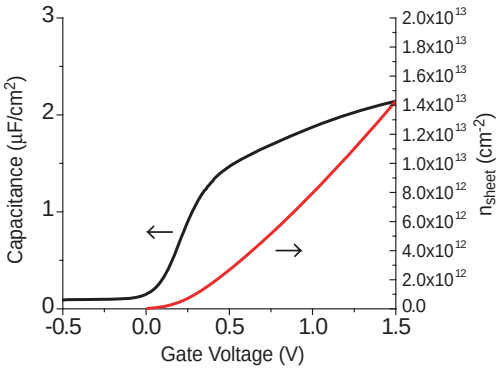
variation. Lot C4 had $\sim$ 3.6 nm HfO_2, while C5 had $\sim$ 4.2 nm HfO_2. Figure 6.49 is a plot of effective channel mobility versus sheet charge density for the three delta doping levels. The peak mobility for each sample correlates with the threshold voltage shift. This could be due to the wavefunction movement with applied gate bias. The heavier delta doping forces the wave function towards the back of the channel, away from the channel surface. Only until the channel charge density is high enough does the electron wavefunction centroid move from the back towards the front of the channel. The 50% delta doping sample in C5 had the same processing as the 2 cycle channel etching sample in C4, but the mobility decreased by about half for C5. This is could be an effect of ALD-induced process variation on channel mobility.

6.5.3 CV: Lot C6 (P-doped back barrier)

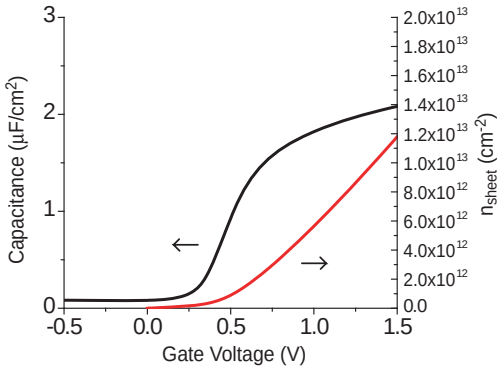
Figure 6.50 shows the CV, n_{sheet}, and effective mobility curves for Lot C6. Yet again the maximum measured capacitance is different than that seen in the other lots, and is in fact the highest out of all three lots. The threshold voltage is also more negative due to the heavy delta doping. The effective mobility is also the highest of all three lots; combined with the higher capacitance, this can explain the superior on-state DC performance.

6.5.4 CV: Data Discussion

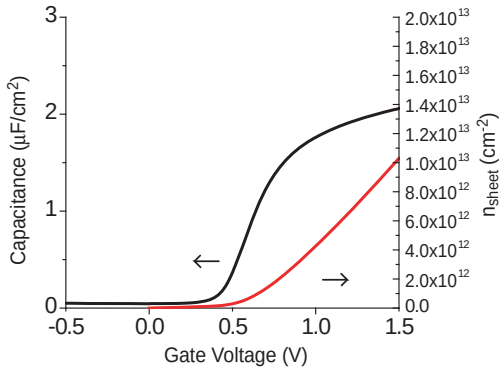
There a few discrepancies when comparing the measured capacitance data to theoretical calculations. The measured accumulation capacitance for all lots is on the order of 2 μF / cm^2. Given 4 nm HfO_2 with a relative dielectric permittivity of



(a) 100% delta doping



(b) 50% delta doping



(c) 25% delta doping

Figure 6.48: Lot C5: CV and n_{sheet} for 100, 50, and 25% delta doping concentrations.

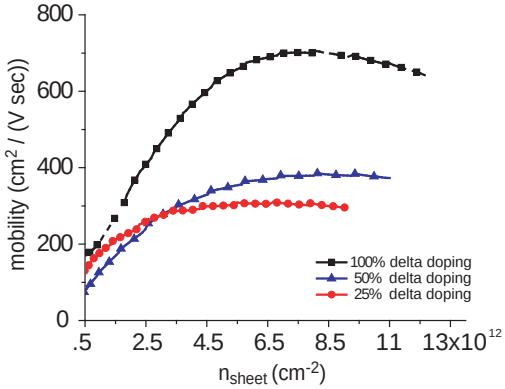
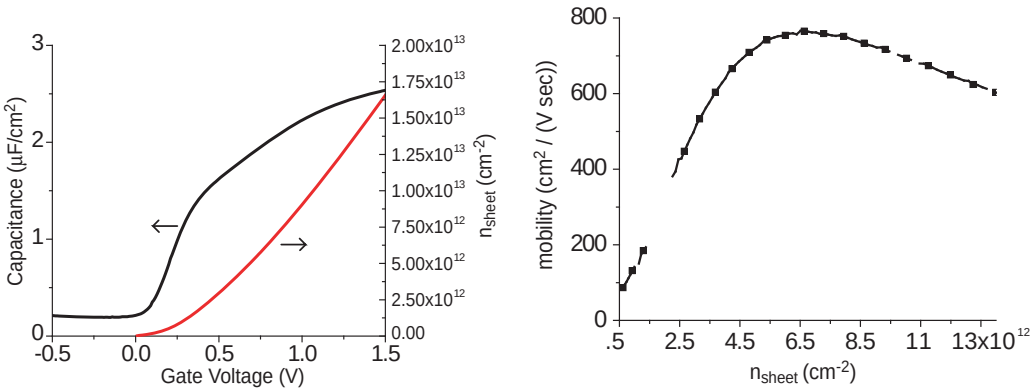


Figure 6.49: Lot C5: Effective mobility versus n_{sheet} for 100, 50, and 25% delta doping concentrations.



(a) 2 cycle etching

(b) 3 cycle etching

Figure 6.50: Lot C6: CV,n$_{sheet}$, and effective mobility for p-doped back barrier.

20, C$_{ox}$ = 4.42 μF / cm^2. The two-dimensional density of states capacitance for InGaAs, assuming m* = 0.04m$_0$ and one eigenstate, equals 2.69 μF / cm^2. Neglecting wave function depth capacitance, C$_{g-chan,max}$ = 1.67 μF per cm^2, lower than measured. This would be even lower if C$_{depth}$ were not neglected.

The extra capacitance may be due to the following: unaccounted parasitic capacitances, incorrect channel density of states capacitance, interface trap capacitance, or back barrier capacitance. Parasitic capacitance may come from needle pad geometries. This can be eliminated from the measurement by removing the pad and directly probing gate metal on top of the channel. The channel density of states capacitance is proportional to the effective mass in the channel and the number of eigenstates. Nonparabolicity and strain effects in the channel can modify m* and alter C$_{dos}$. Increased capacitance can come from a second eigenstate population near the top of the well.

Interface trap capacitance may be present at 2.5 MHz. Higher frequency measurements are therefore required to eliminate their response. However, as frequency

increases, device resistance terms (access, channel) will affect measurement capacitance due to RC charging delay. Channel resistance is high around V_{th}, and long gate length capacitance measurements will suffer at high frequencies. Therefore, shorter gate length measurements can be done at high frequencies, with a proportional increase in gate width to maintain absolute capacitance.

Back barrier capacitance requires the electron Fermi level to be near the back barrier conduction band edge. For InGaAs/InAlAs, $\Delta E_c \sim 0.5$ eV. Including quantum confinement, this will decrease, leaving less than 0.5 eV of Fermi level movement to accumulate charge in the channel. The theoretical maximum charge in the channel at E_f - E_1 is $\sim 7{\times}10^{12}$ cm^{-2} before back barrier states are populated. n_{sheet} calculations for all lot capacitance data exceed this, suggesting charge is accumulating in the back barrier. If the back barrier density of states capacitance is high enough, it will pin the Fermi level in the channel region, preventing increase in device current.

It is likely that a combination of incorrect effective mass, interface trap capacitance, and back barrier capacitance affects the measurement. Since increased capacitance equates to increased charge, the effective mobility is lowered. Therefore, the effective mobilities seen here are lower bounds on the actual mobility. Future publications will more rigorously analyze the CV data to obtain more accurate mobile channel charge densities.

Overall, the capacitance and effective mobility data can help correlate and guide future experiments to improve device performance. A few trends have emerged. The channel thickness plays a strong role in channel mobility at the 5 to 6 nm channel thickness regime. Delta doping effectively moves the wave function closer to the back barrier, away from the channel surface, providing higher effective mobilities

are consequently better on-state performance. However, higher peak mobility does not make an optimal device, since carrier densities on the order of 1 to 2×10^{12} cm^{-2} have low mobilities. This may be due to electron scattering at the InGaAs/InAlAs interface and with the delta doping in the InAlAs. Delta doping set back may improve the mobility. Reduction of the delta doping appears to hurt mobility since the wave function is not buried. Surface roughness must be improved to prevent mobility degradation. Wide bandgap channel capping layers, such as InP or InAlAs, may improve mobility by setting the wavefunction back from the surface. However, they must be kept thin, on the order of a few monolayers, to prevent EOT increase. Clearly, there is a trade-off between mobility, capacitance, and performance that must be optimized.

6.6 Gate Last: MOCVD Regrowth Discussion

MOCVD regrowth provides heavily-doped lattice-matched InGaAs source-drain regions. Due to its selective growth properties, transistor process complexity is reduced; more samples can be processed in a given time, increasing the confidence in conclusions drawn from the data. Lot C1 showed that MOCVD performance is as good as MBE for on-state, but worse for the off-state. The addition of digital channel etching improves both the on- and off-state performance by removing semiconductor damage during processing. A comparison of etched InGaAs channel thicknesses suggests surface roughness for the $\sim$ 5 nm channels dominates device performance. Back barrier delta doping improves on-state device performance, by improving channel mobility, but negatively impacts off-state performance, by increasing subthreshold swing and DIBL for short gate lengths. P-doped back bar-

riers tend to minimize off-state leakage current. Using 0.8 nm EOT HfO_2 gate dielectrics, an InGaAs channel achieved peak transconductance of 2.0 mS/micron at 0.5 V V_{ds}. With a subthreshold swing of $\sim$ 100 mV/dec, interface trap density is still 1 to 2 $\times 10^{13}$ cm^{-2} eV^{-1}. Further work must be done to improve short-channel subthreshold swing while maintaining channel mobility.

6.7 Conclusion: Gate-Last MOSFETs

This chapter has summarized and analyzed multiple experiments in gate last III-V MOSFET process flow. Transitioning from gate first to gate last immediately improved device performance, revealing III-V surface protection is not a critical step for on-state device performance. Continued process development led to moderate performance improvements, but eventually plateaued. The combination of MOCVD regrowth and digital etching allowed for continued device improvements. Improving off-state performance can have negative effects on on-state performance. Mobility measurements suggest higher mobility channels, or prevention of mobility degradation, are critical for maintaining on-state performance while improving off-state performance.

References

[1] Varistha Chobpattana, Junwoo Son, Jeremy JM Law, Roman Engel-Herbert, Cheng-Ying Huang, and Susanne Stemmer. Nitrogen-passivated dielectric/InGaAs interfaces with sub-nm equivalent oxide thickness and low interface trap densities. *Applied Physics Letters*, 102(2):022907–022907, 2013.

[2] Titta Aaltonen, Petra Alén, Mikko Ritala, and Markku Leskelä. Ruthenium thin films grown by atomic layer deposition. *Chemical Vapor Deposition*, 9(1):45–49, 2003.

[3] Jill S Becker and Roy G Gordon. Diffusion barrier properties of tungsten nitride films grown by atomic layer deposition from bis (tert-butylimido) bis (dimethylamido) tungsten and ammonia. *Applied Physics Letters*, 82(14):2239–2241, 2003.

[4] UCSB Nanofab Staff. Private communication. 2013.

[5] Greg J Burek, Yoontae Hwang, Andrew D Carter, Varistha Chobpattana, Jeremy JM Law, William J Mitchell, Brian Thibeault, Susanne Stemmer, and Mark JW Rodwell. Influence of gate metallization processes on the electrical characteristics of high-k / $In_{0.53}Ga_{0.47}As$ interfaces. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 29(4):040603–040603, 2011.

[6] Sanghoon Lee. Private communication. 2013.

[7] Viktor Ariel-Altschul, Eliezer Finkman, and Gad Bahir. Approximations for carrier density in nonparabolic semiconductors. *Electron Devices, IEEE Transactions on*, 39(6):1312–1316, 1992.

[8] U Singisetti. *$In_{0.53}Ga_{0.47}As$ MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth*. PhD thesis, UC Santa Barbara, 2009.

[9] YQ Wu, M Xu, RS Wang, O Koybasi, and PD Ye. High Performance Deep-Submicron Inversion-Mode InGaAs MOSFETs with maximum G m exceeding 1.1 mS/μm: New HBr pretreatment and channel engineering. In *Electron Devices Meeting (IEDM), 2009 IEEE International*, pages 1–4. IEEE, 2009.

[10] Han-Chung Lin, Wei-E Wang, Guy Brammertz, Marc Meuris, and Marc Heyns. Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator. *Microelectronic Engineering*, 86(7-9):1554–1557, 2009.

[11] JJ Gu, YQ Liu, YQ Wu, Robert Colby, Roy G Gordon, and Peide D Ye. First experimental demonstration of gate-all-around III–V MOSFETs by top-down approach. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 33–2. IEEE, 2011.

[12] Mikael Egard, Lars Ohlsson, B Mattias Borg, L-E Wernersson, and Erik Lind. Self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ As MOSFET with selectively regrown source and drain contact layers. In *Device Research Conference (DRC), 2011 69th Annual*, pages 1–2. IEEE, 2011.

[13] M Egard, L Ohlsson, BM Borg, F Lenrick, R Wallenberg, L-E Wernersson, and E Lind. High transconductance self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 13–2. IEEE, 2011.

[14] Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces, author=Engel-Herbert, Roman and Hwang, Yoontae and Stemmer, Susanne. *Journal of Applied Physics*, 108(12):124101–124101, 2010.

[15] John S Parker, Ashish Bhardwaj, Pietro RA Binetti, Yung-Jr Hung, and Larry A Coldren. Monolithically integrated gain-flattened ring mode-locked laser for comb-line generation. *Photonics Technology Letters, IEEE*, 24(2):131–133, 2012.

[16] Andrew D.Carter Jeremy J. M. Law Doron C. Elias Varistha Chobpattana Brian J. Thibeault William Mitchell Susanne Stemmer Arthur C. Gossard Mark J. W. Rodwell Sanghoon Lee, Cheng-Ying Huang. High Transconductance Surface Channel $In_{0.53}Ga_{0.47}As$ MOSFETs Using MBE Source-Drain Regrowth and Surface Digital Etching. In *Indium Phosphide and Related Materials (IPRM), 2013 International Conference on*. IEEE, 2013.

[17] JM Fastenau, D Lubyshev, Y Wu, C Doss, and WK Liu. Comparative studies of the epireadiness of 4in. InP substrates for molecular-beam epitaxy growth. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 23(3):1262–1266, 2005.

[18] O Ostinelli, AR Alt, R Lovblom, and CR Bolognesi. Growth and characterization of iron-doped semi-insulating InP buffer layers for Al-free GaInP/GaInAs high electron mobility transistors. *Journal of Applied Physics*, 108(11):114502–114502, 2010.

Chapter 7

Conclusions and Future Work

7.1 Summary

This dissertation has examined semiconductor MOSFET theory and experimental device results for InGaAs-based MOSFETs. It has covered MOSFET device theory for long-channel, velocity saturated, and ballistic FETs, including short channel effects and general FET scaling theory. It has examined two key process modules: source-drain regrowth and atomic layer deposition of gate insulators. Three process flows were examined: gat first MBE source-drain regrowth, gate last MBE source-drain regrowth, and gate last MOCVD source-drain regrowth. Gate-first research concluded with sub-100-nm-gate lengths, but scaled device data did not improve performance. Gate-last processing, when paired with MOCVD regrowth and digital channel etching, showed markedly better performance than any MBE regrowth FET process.

7.2 Process Improvements

This dissertation has shown the potential for gate last III-V MOS processing, but the process flow can be altered to enhance performance and better characterize the devices. IV and CV data is currently measured using needle-probeable device layouts. Needle probe measurements are adequate for DC characterization, but not for high-frequency or microwave characterization. At microwave frequencies, the interface trap response will be low, improving on-state performance. Using a network analyzer and measured S-parameters, more in-depth characterization of the FETs can be accomplished.

Gate lengths in the dry-etch SiO_xprocess scale to $\sim$ 50 nm gate lengths, with adequate sidewall roughness. The gate length can be further scaled using electron beam lithography direct-write HSQ dummy gates. This process should scale to 20 nm or less. However, scaling the gate length is only effective if short channel effects can be kept under control. Non-planar device geometries will improve gate-channel control, allowing gate length scaling to continue below 50 nm.

Gate metal is currently evaporated over the entire sample and selectively removed using photoresist liftoff processing. The sample must be removed from the ALD chamber, exposed to ambient conditions, and to photoresist; all of these pose sample contamination issues, such as water vapor and mobile ions. These will likely decrease device performance. An in-situ ALD metal, such as Ru or WN, would prevent these contamination opportunities. For non-planar device geometries, an ALD metal is critical, as standard metal evaporation does not have adequate sidewall coverage (in the case of fins), and is impossible for shadowed surfaces (in the case of gate-all-around or nanowires).

Gate-last CV data provides on wafer capacitance data and effective mobility. However, given the presence of interface states, actual channel mobility extraction is difficult. Hall mobility measurements would provide a more accurate assessment of the channel. Adding gate control to a Hall structure would allow mobility characterization as a function of channel charge, without interface trap density affecting an accurate charge density extraction.

7.3 Data Trends

A few trends have emerged from the collective transistor data set. As predicted from FET device scaling, improving C_{g-ch}, by scaling gate insulator and wavefunction depth, has improved device performance. Short gate length MOSFETs with 1 to 2 nm EOT gate insulators and 10 nm thick InGaAs channels had peak transconductance $\sim$ 1.0 mS/micron at 0.5 V_{ds}. Channel thickness scaling (Lot C2, Lot C3) showed trends of improved transconductance in the limit channel mobility is not affected. $\sim$ 0.8 nm EOT dielectrics combined with $\sim$6 nm InGaAs channels and heavy delta doping saw the best peak transconductance, 2.0 mS/micron at 0.5 V_{ds}. In this process flow, InAs/InGaAs composite channels have shown 2.5 mS/micron peak transconductance [1].

C_{depth} can be increased by decreasing the channel thickness. However, as seen in the channel scaling series, long channel performance decreases, a sign of lower mobility. Another effect of channel thickness scaling is eigenstate energy increase. ΔE_c for InGaAs/InAlAs is 0.5 eV. From Schrödinger-Poisson simulation, 6 nm InGaAs channels with HfO_2 gate dielectric raise the eigenstate at least 0.1 eV from the band edge. Further channel thickness scaling will continue to raise the state.

This will increase threshold voltage and cause the electron wavefunction to have a larger portion of its evanescent tail in the InAlAs barrier, increasing electron scattering and decreasing overall gate control. Therefore, it is important for device scaling to increase channel confinement. Larger ΔE_c is possible with lattice-matched AlAsSb, offering a theoretical 1.0 eV offset to InGaAs [2]. This would allow larger channel charge densities without sacrificing channel mobility. Another option is the use of non-planar device structures, shown in Figure 7.1. By surrounding the channel with large ΔE_c material, charge confinement is no longer a problem, and very thin channels with large C_{depth} are possible, in the limit where channel mobility does not deteriorate. Non-planar device geometries also improve short channel effects.

Scaling C_{ox} and C_{depth} are important and necessary for device scaling. However, C_{g-ch} also includes C_{dos}, the density of states capacitance. For a given material system, this is a fixed parameter. In the absence of interface trap capacitance, the electrical effective thickness capacitance, C_{EET}, is the series combination of C_{ox} and C_{depth}, which controls the electron Fermi level for C_{dos}. Given current EOT (0.8 nm) and 2 nm wave function depth in InGaAs, and one populated eigenstate, C_{g-ch} / C_{dos} = 49%. Given a 0.5 nm EOT gate insulator, 2 nm wave function depth in InGaAs, and one populated eigenstate, C_{g-ch} / C_{dos} is 55%. Further scaling of C_{ox} is not effective for improving on-state gate control, but will improve subthreshold swing if interface state density remains constant.

Interface trap density for the gate first and gate last data set is summarized in Table 7.1. While the interface state density was highest for gate first MBE regrowth, the lowest was for InAs channels with gate last MOCVD regrowth. Increasing C_{ox} correlated with improved on-state and off-state device performance, but the

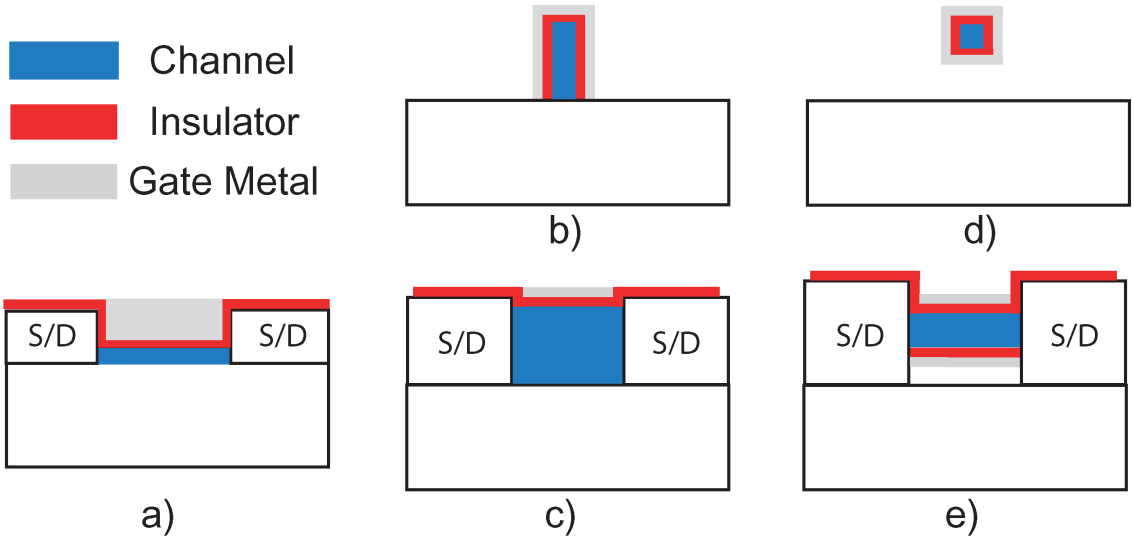


Figure 7.1: Various field effect transistor geometries. a) Planar FET, parallel to current flow b) FinFET, perpendicular to current flow c) FinFET, parallel to current flow d) Nanowire FET, perpendicular to current flow e)Nanowire FET, parallel to current flow.

absolute interface state density is still very high, $\sim 1{\times}10^{13}$ (cm^{-2} eV^{-1} for the samples measured. Channel passivation techniques need to be examined and new methods developed to further reduce the trap density. For the same EOT, lower subthreshold swings (85 mV/dec) have been seen on InAs channels [1]. In the literature, there is a correlation with improved subthreshold swing with increasing channel In content. For [3], 0.53 In content channels show 80 mV/dec with sulfur treatments, and for [4] gate-all-around has 63 mV/dec with 0.65 In content with sulfur treatments. Higher indium content channels offer lower effective mass carriers, improving electron velocity, but also a decreased density of states capacitance.

Ballistic FET limit analysis in the degenerate limit [7] reveals an optimum effective mass for a given electrical effective thickness (a combination of insulator capacitance and wave function depth). If there are too few electrons (low DOS), while they move very fast, there is not enough current. Too many electrons (high

Sample	Gate Insulator	EOT (nm)	SS (mV/dec)	D_{it} (cm^{-2} eV^{-1})
Ref. [5]	Al_2O_3	2.17	500	7.3×10^{13}
Lot A2	Al_2O_3	2.17	230	2.8×10^{13}
Lot B1	Al_2O_3+HfO_2	2.36	200	2.1×10^{13}
Lot B3	Al_2O_3+HfO_2	1.72	120	1.25×10^{13}
Lot B4	Al_2O_3+HfO_2	1.21	144	2.4×10^{13}
Lot C5	HfO_2	0.8	110	2.8×10^{13}
Lot C6	HfO_2	0.8	100	1.9×10^{13}
InAs surface [6]	HfO_2	0.8	85	1.2×10^{13}

Table 7.1: Summary of subthreshold swing and interface trap density for various FET samples.

DOS) means many electrons move slowly, therefore there is not enough current. In the ultra-thin EET limit, silicon is the semiconductor of choice. However, it is theoretically possible to engineer a higher density of states in III-Vs [7], thereby increasing C_{dos}, the limiting capacitance in C_{g-ch}. By altering the crystal orientation, two favorable eigenstates can be populated simultaneously, and therefore compete with or exceed the ballistic currents of silicon.

III-V MOSFETs are promising candidates for future integrated MOS technologies. This dissertation has examined three process flows for their fabrication. Two process modules, gate insulator deposition and source/drain regrowth, were examined and optimized for best possible device performance. From the measured data, the current generation of III-V MOSFETs require a reduction in interface trap density and improved gate-channel control for improved off-state performance. These modules and process flows can be leveraged for other III-V devices, such as HEMTs, HBTs, and photonic devices.

References

[1] Sanghoon Lee, Cheng-Ying Huang, Andrew D.Carter, Doron C. Elias , Jeremy J. M. Law, Varistha Chobpattana, Brian J. Thibeault, William Mitchell, Susanne Stemmer, Arthur C. Gossard, Mark J. W. Rodwell. Record Extrinsic Transconductance (2.45 mS/μm at $V_{DS} = 0.5V$)$InAs/In_{0.53}$GaAs Channel MOSFETs Using MOCVD Source-Drain Regrowth. In *VLSI Technology and Circuits, 2013 Symposia on*, 2013.

[2] Cheng-Ying Huang. Unpublished AlAsSb FET Results. 2013.

[3] Mikael Egard, Lars Ohlsson, B Mattias Borg, L-E Wernersson, and Erik Lind. Self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ As MOSFET with selectively regrown source and drain contact layers. In *Device Research Conference (DRC), 2011 69th Annual*, pages 1–2. IEEE, 2011.

[4] H. Wu J. Shao A. T. Neal M. J. Manfra R. G. Gordon J. J. Gu, X. W. Wang and P. D. Ye. 20-80nm Channel Length InGaAs Gate-all-around Nanowire MOSFETs with EOT=1.2nm and Lowest SS=63mV/dec. In *Electron Devices Meeting, 2001. IEDM 2012. Technical Digest. International*, 2012.

[5] U Singisetti. *$In_{0.53}Ga_{0.47}As$ MOSFETs with 5 nm channel and self-aligned source/drain by MBE regrowth*. PhD thesis, UC Santa Barbara, 2009.

[6] Sanghoon Lee. Private communication. 2013.

[7] Mark Rodwell, W Frensley, S Steiger, E Chagarov, S Lee, H Ryu, Y Tan, G Hegde, L Wang, J Law, et al. III–V FET channel designs for high current densities and thin inversion layers. In *Device Research Conference (DRC), 2010*, pages 149–152. IEEE, 2010.

Appendix A

Gate First MOSFET Process Flow

This appendix describes the gate first MBE source/drain regrowth process flow.

Process Step	Equipment	Process Step	Notes	X	Date
Sample Information			Sample Description: Wafer number(s):		
Extra Notes	N/A	N/A			
Sample Preparation					
Cleave	Wet Bench	Cleave samples according to established guidelines regarding flat orientation (check with senior Rodwell process staff)			
Extra Note Space	N/A	N/A			
Gate Stack Deposition					
Alumina Deposition	FlexAL ALD	100 cycles ADC AL2O3 300C 200d H2	Nothing in chamber, seasoning step		
		Vent loadlock, go to next step immediately			
		Clean samples in 10:1 DI: HCl at acid bench, 10 seconds			
		Immediately load samples on to private AL2O3 NO AU/NO PR carrier wafer			
		____ cycles ADC AL2O3 300C 200d H2. **Include CV square for dielectric testing.** **Include Si quarter for VASE/etch test.**	About 1.1 Angston/cycle		
		Hold samples in loadlock until next layer deposition is ready.			
Extra Note Space	N/A	N/A			
W Deposition	Sputter #1	Load sample onto private holder			

Process Step	Equipment	Process Step	Notes	X	Date
	Sputter #1	Public W, W shield, sputter clean for 15m, sputter deposit for __ m __ s @ ___ V (_____ sccm Ar)			
		While waiting for pump down, run ellipsometer on sample to confirm growth.	Ellipsometer thickness of al2o3:		
Cr Gate Deposition	Ebeam #1	Load sample onto private holder			
	Ebeam #1	Evaporate ____A Cr @ 5A/sec			
SiO2 Deposition	PECVD	Run 60m clean/pre-dep until ready			
		Deposit ____nm of SiO2			
Cr Mask Deposition	Ebeam #1	Evaporate ____A Cr @ 5A/sec			
Extra Note Space	N/A	N/A			
Gate Stack Lithography					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
EBL Resist Spin	PR Bench	Test Spin wafer 6krpm 30s			
		Apply 6% HSQ (fridge)			
		Spin 6krpm 30s			
		Softake 90C 60s			
EBL Expose	JEOL EBL	Expose Pattern	800-1000uC/cm^2 area dose 3000uC/cm^2 line dose		
	JEOL EBL	Exposure Name and Serial Number			
EBL Develop	Base Bench	Develop 25% TMAH 30s			
		1m DI Rinse			
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			

Process Step	Equipment	Process Step	Notes	X	Date
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "GATE" reticle	Login: [10,126]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK			
		Edit ADCGATE if necessary			
		Run "MAP ADCGATE/LOQUAR"	Shoot inner die first		
		Run "MAP ADCGATE/INNER,OUQUAR"	Shoot inner die second		
		Expose for ___s	Shoot .24 is looking good right now		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Extra Note Space	N/A	N/A			
Gate Stack Etch					
Cr Mask Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m Cl2/O2 condition/season (163)			
		Mount sample with Santovac oil			
		Etch __m __s (163)	Etching 20nm in 1 minute is an overetch		
	Solvent Bench	Upon release with indirect DI spray, immediately submerge in DI water			
		Carry wet, 2m Acetone, 2m Iso			
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	PE-IIA	2m O2 @ 100W 300mT (optional)			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
SiO2 Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m SF6/Ar condition/season (162)	50/5 75W Recipe		
		Mount sample with Santovac oil			
		Etch __m ___s 75W (162)			

Process Step	Equipment	Process Step	Notes	X	Date
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Cr Gate Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m Cl2/O2 condition/season (163)			
		Mount sample with Santovac oil			
		Etch m s (163)			
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
W Gate Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m SF6/Ar condition/season (162)	50/5 75W Recipe		
		Mount sample with Santovac oil			
		Etch m s 15W (162)			
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
Sidewall Dep and Etch					
PECVD Preparation	PECVD	Run 60nm clean			
	Solvent Bench	Cleave one Si quarter per process sample			
		Cleave two extra Si quarter for rate check			
		3m Acetone, 3m Iso, carry wet to dev			
		3m DI, N2 blow dry (<20PSI)			

Process Step	Equipment	Process Step	Notes	X	Date
ALD Measure and Dep	Ellipsometer	Measure 0nm wafer for native Si	Thickness: _____		
	PECVD	Deposit 100nm SiNx on two Si quarters			
	Ellipsometer	Measure 200 cycle wafers	Thickness: _____		
	PECVD	Deposit ___ nm on 1 Si 0nm wafer and 1 process wafer			
	Ellipsometer	Measure thicknesses	Thickness: _____		
RIE Etch and Measure	ICP #1	Run 20nm O2 Clean (121)	Check binder for any Rodwell specific process settings		
		5m CF4/O2 Season (134)			
		Mount sample with Santovac oil			
		Etch 100nm Si ___ m			
		Etch 100nm Si ___ m			
		Remove with water or tweezers			
	Ellipsometer	Measure thicknesses	100nm 1st Thickness: _____ 100nm 2nd Thickness: _____		
		Calculate 120% overetch for process samples			
	ICP #1	Mount sample with Santovac oil			
		Etch process samples ___ m ___ s			
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Ellipsometer	Measure thicknesses	0nm Thickness: _____, should be ~20A!		
Extra Note Space	N/A	N/A			
Al2O3 Etch and Regrowth Prep					
	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
	Develop Bench	Soak in fresh 100% AZ400K for ___ m	or less depending on Al2O3 thickness		

Process Step	Equipment	Process Step	Notes	X	Date
	UV Ozone	Run empty for 30m			
		Load FET and run for 30m			
	MBE Lab	Etch 1m HCl:DI 1:10			
		Load into MBE ASAP	Any special requests? Confirm with the Grower		
Extra Note Space	N/A	N/A	Who (re)grew it? _____		
Mo Planarization					
		Prepare process wafer, one Si quarter			
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS to Si, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR510, spin 4krpm 30s			
		Apply SPR510 to process wafer, spin 4krpm 30s			
		Softake 90C 60s			
		Postbake 110C 60s			
PR Thickess Check	Filmetrics	Measure thickness of PR on SI	Thickness: _____		
ICP Prep	ICP #1	Run 30m O2 Ash empty (306 or 309)			
PR Ashing		Run 30m O2 Ash with process wafer and Si wafer (306 or 309)			
		Measure thickness of PR on SI and extrapolate rate	Thickness: _____ Rate:_____		
	ICP #1	Run until PR ~250nm thick	Either remove wafers or just use in next etch		
Mo Etch		10m O2 clean (Recipe 121)			
		5m SF6/Ar condition/season (162)			
		Etch 2m 5/5 SF6/Ar (162)			
		Upon release with indirect DI spray, immediately submerge in DI water			
		Carry wet, 2m Acetone, 2m Iso			
		Soak in 1165 @ 80C for 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	PE-IIA	2m O2 @ 100W 300mT			
	Any Microscope	Check etch and yield			

Process Step	Equipment	Process Step	Notes	X	Date
	SEM	Check if planarization was successful, if not, repeat			
Extra Note Space	N/A	N/A			
S/D Contact Liftoff					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare AI carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply nLOF 5510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "SD-SDVIAS" reticle			
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETSD if necessary			
		Run "MAP MFETSD\LOCAL"			
		Expose for 0.35s	perhaps .27?		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 90s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Contact Metal Dep	Ebeam #4	Mount on rotating stage			
		Evaporate 200A Ti			
		Evaporate 750A Pt or Pd (diff barrier)			
		Evaporate 1500A Au			
	Solvent Bench	Liftoff in 1165 @ 80C for 1hr			
		Agitate (pipette spray)			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Any Microscope	Check liftoff and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			

Process Step	Equipment	Process Step	Notes	X	Date
Device Isolation 1					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR 510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "ISO-VIAS" reticle			
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETISO if necessary			
		Run "MAP MFETISOLOCAL"			
		Expose for 0.27s			
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Mo Etch	ICP #1	10m O2 clean (Recipe 121)			
		5m SF6/Ar condition/season (162)			
		Mount sample with Santovac oil			
		Etch 2m 5/5 SF6/Ar etch (162)			
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		Soak in 1165 @ 80C for 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	PE-IIA	2m O2 @ 100W 300mT			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
Device Isolation 2					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			

Process Step	Equipment	Process Step	Notes	X	Date
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR 510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "ISO2-PADS" reticle			
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETISO if necessary			
		Run "MAP MFETISOILOCAL"			
		Expose for 0.27s			
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Semiconductor Etch	Acid Bench	Etch 2m H3PO4:H2O2:DI 1:1:25			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
SiO2 Gate Pad Etch	HF Bench	Etch 90s Buffered HF			
		Rinse 2m DI			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Cr Gate Pad Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m Cl2/O2 condition/season (163)			
		Mount sample with Santovac oil			
		Etch 2m (163)			
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		Soak in 1165 @ 80C for 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	PE-IIA	2m O2 @ 100W 300mT			
	Any Microscope	Check etch and yield (perhaps SEM)			
	Dektak	Note Dektak Pad thickness	Thickness: _____		

Process Step	Equipment	Process Step	Notes	X	Date
Extra Note Space	N/A	N/A			
DC Device Check					
Check DC Device yield					
If successful, proceed					
S/D Post Liftoff					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare AI carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply nLOF 5510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "SD-SDVIAS" reticle			
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETSD if necessary			
		Run "MAP MFETSDVIAS/LOCAL"			
		Expose for 0.35s			
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 90s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Post Metal Dep	Ebeam #4	Mount on rotating stage			
		Evaporate 200A Ti			
		Evaporate 6000A Au			
	Solvent Bench	Liftoff in 1165 @ 80C for 1hr			
		Agitate (pipette spray)			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Any Microscope	Check liftoff and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		

Process Step	Equipment	Process Step	Notes	X	Date
Extra Note Space	N/A	N/A			
Gate Post Liftoff					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply nLOF 5510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "GATE-GVIA" reticle			
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETSD if necessary			
		Run "MAP MFETGVIA/LOCAL"			
		Expose for 0.35s	.27?		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 90s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Contact Metal Dep	Ebeam #4	Mount on rotating stage			
		Evaporate 200A Ti			
		Evaporate 8500A Au			
	Solvent Bench	Liftoff in 1165 @ 80C for 1hr			
		Agitate (pipette spray)			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Any Microscope	Check liftoff and yield			
	Dektak	Note Dektak Pad thickness	Thickness:		
Extra Note Space	N/A	N/A			
BCB Cure and Etch					
		Prepare process wafer, one Si wafer			
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			

Process Step	Equipment	Process Step	Notes	X	Date
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
	Blue Oven	Flow N2 100%			
		Confirm Program 5 is the following:			
		a) 5m ramp to 50C, 5m soak			
		b) 15m ramp to 100C, 15m soak			
		c) 15m ramp to 150C, 15m soak			
		d) 60m ramp to 250C, 50m soak			
		e) Natural cool down			
		f) Oven off			
		Leave oven empty at 25C for 20m			
	PR Bench	Test spin to confirm recipe 7 4krpm 30s			
		Apply BCB 2264 to process wafer, spin 4krpm 30s			
		Apply BCB 2264 to Si wafer, spin 4krpm 30s			
		Softbake 110C 1m			
	Filmetrics	Measure thickness of BCB on Si wafer	Thickness: _____		
BCB Cure	Blue Oven	Run Progam 5 overnight			
	Filmetrics	Measure thickness of BCB on Si wafer	Thickness: _____		
ICP Prep	ICP #1	Run 30m O2 Ash empty (306 or 309)			
		Mount sample with Santovac oil			
		Ash process wafer and Si wafer 3m CF4/O2 BCB ash (308)			
	SEM	Insepct posts with tilted holder			
	Filmetrics	Measure thickness of BCB on Si wafer	Thickness: _____		
		If posts not exposed, calculate rate, current thickness, and etch to desire thickness			
SiNx Adhesion Layer and Etch					
PECVD Preparation	PECVD	Run 60m clean/pre-dep until ready			
	Solvent Bench	Cleve one Si Wafer			
		(two will have 100nm, two will have 30nm)			
		3m Acetone, 3m Iso, carry wet to dev			
		3m DI, N2 blow dry (<20PSI)			
		Prepare Al carrier, 110C 5m			
PECVD Measure and Dep	Ellipsometer	Measure 0nm wafer	Thickness: _____		

Process Step	Equipment	Process Step	Notes	X	Date
	PECVD	Deposit 100 nm on two Si wafers			
	Ellipsometer	Measure 100nm wafer	Thickness: _____		
	PECVD	Deposit 50 nm on 1 Si 0nm wafer. 1 Si 100nm wafer, and 1 process wafer			
		Deposit 50 nm on 1 Si 0nm wafer. 1 Si 100nm wafer, and 1 process wafer			
	Ellipsometer	Measure thicknesses	150nm Thickness: _____ 50nm Thickness: _____		
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "ISO-PADS" reticle	Login: [10,126], see "Rodwell Group Processing Document" for local alignment tips		
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETADHESION if necessary			
		Run "MAP MFETADHESION/LOCAL"			
		Expose for 0.27s			
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 90s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
RIE Etch and Measure	ICP #1	Run 30nm O2 Clean (121)	Check binder for any Rodwell specific process settings		
		5m CF4/O2 Season (134)			
		Mount sample with Santovac oil			
		Etch 150nm Si 4m			
		Etch 150nm Si 5m			
		Remove with water or tweezers			
	Ellipsometer	Measure thicknesses	130nm 4m Thickness: _____ 130nm 5m Thickness: _____		

Process Step	Equipment	Process Step	Notes	X	Date
		Calculate 150% 50nm etch			
	ICP #1	Mount sample with Santovac oil			
		Etch process wafers with calcualted time and 30nm monitor piece			
		Upon release with indirect DI spray, immediately submerge in DI water			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Ellipsometer	Measure thicknesses	0nm Thickness: _____		
Extra Note Space	N/A	N/A			
Gate Post Liftoff					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply nLOF 5510, spin 4krpm 30s			
		Softake 90C 60s			
PR Expose	Autostepper	Load "PADS" reticle			
		Place wafer onto chuck (typ. 1/4 2in)			
		Run SETUP, CHUCK			
		Load sample onto stage, run AWLT			
		Edit MFETPADS if necessary			
		Run "MAP MFETPADS/LOCAL"			
		Expose for 0.35s			
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 90s with agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Contact Metal Dep	Ebeam #4	Mount on rotating stage			
		Evaporate 200A Ti			
		Evaporate 10,000A Au			
	Solvent Bench	Liftoff in 1165 @ 80C for 1hr			

Process Step	Equipment	Process Step	Notes	X	Date
		Agitate (pipette spray)			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Any Microscope	Check liftoff and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			

Appendix B

Gate Last MOSFET Process Flow

This appendix describes the gate last MBE/MOCVD source/drain regrowth process flow.

Process Step	Equipment	Process Step	Notes	X	Date
Sample Information			Sample Description: Wafer number(s): _____		
Sample Preparation					
Cleave	Wet Bench	Cleave samples according to established guidelines regarding flat orientation (check with senior Rodwell process staff)			
Extra Note Space	N/A	N/A			
Gate Stack Deposition			**1 Si wafer needed for SiO2 etch rate calibration**		
SiO2 Seasoning	PECVD	Run 60m clean/pre-dep until ready			
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	2m DI, N2 blow dry (<20PSI)			
SiO2 Deposition	PECVD	Clean ____ min, deposit _____nm of SiO2	Dummy sample? Y / N		
		Deposit _____nm of SiO2 on dummy Si	Dummy sample? Y / N		
		Deposit _____nm of SiO2 on samples	Dummy sample? Y / N		
Cr Mask Deposition	Ebeam #1	Evaporate ____A Cr @ 2A/sec	Dummy sample? Y / N		

Process Step	Equipment	Process Step	Notes	X	Date
Extra Note Space	N/A	N/A			
EBL Gate Lithography					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	2m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
EBL Resist Spin	PR Bench	Test Spin wafer 6krpm 30s			
		Apply "6%" (3:1 MIBK:HSQ) HSQ (fridge)	Do not use filter!		
		Spin 6krpm 30s			
		Softake 90C 60s			
EBL Expose	JEOL EBL	Expose Pattern	800-1000uC/cm^2 area dose 3000uC/cm^2 line dose		
	JEOL EBL	Exposure Name and Serial Number			
EBL Develop	Base Bench	Develop 25% TMAH 45 to 60 sec			
	Any Microscope	Check lithography in microscope			
Optical Gate Litho, Cr Mask Etching					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS through filter + syringe, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR955-0.9, spin ___ krpm 30s			
		Softbake 90C 60s			
PR Expose	Autostepper	Load "GATE" reticle	Login: [10,126]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK, INV			
		Edit FGLGATE necessary			

Process Step	Equipment	Process Step	Notes	X	Date
		Are you leaving blank die???			
		Run MAP FGLGATEINNER,OUTER	1urad?		
		Expose for ___s	Somewhere btwn .25-.28 is looking good right now		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Cr Mask Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m Cl2/O2 condition/season (163)			
		Mount sample with Santovac oil			
		Etch __m___s (163)	Etching 20nm in 1 minute is an overetch		
		O2 Ash 1000W ___m ___s (306)			
		Upon release with indirect DI spray, immediately submerge in DI water			
		Soak in hot 1165 @ 80C for minimum 2 hr			
		Rinse in hot 1165 for 5 min			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
SiO2 Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m SF6/Ar condition/season (162)	50/5 50W Recipe		
		Mount sample with Santovac oil			
		Etch __m ___s 50W (162)	50W is necessary for a good dummy gate taper		
		Upon release with indirect DI spray, immediately submerge in DI water			
		Soak in 1165 @ 80C for minimum 2h			

Process Step	Equipment	Process Step	Notes	X	Date
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
Cr Planarization					
		Prepare process wafer(s), one Si quarter			
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS to Si, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR955-0.9, spin ___ krpm 30s			
		Softbake 90C 60s			
		Cool sample down, 1 minute			
		Postbake 110C 60s			
PR Thickess Check	Filmetrics	Measure thickness of PR on SI	Thickness: _____		
ICP Prep	ICP #1	Run 30m O2 Ash empty (306 or 309)			
		O2 Ash Power: _____W			
PR Ashing		Run 30m O2 Ash with process wafer(s) and Si wafer (306 or 309)	Load up to 4 quarters (or equivelent)		
		Measure thickness of PR on SI and extrapolate rate	Thickness: _____ Rate: _____		

Process Step	Equipment	Process Step	Notes	X	Date
	ICP #1	Run until PR ~____nm thick (thickness determined from total stack height!)	Either remove wafers or just use in next etch		
Cr Mask Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m Cl2/O2 condition/season (163)			
		Mount sample with Santovac oil			
		Etch __m __s (163)	Etching 20nm in 1 minute is an overetch		
	Microscope	Verify that the Cr was etched			
	ICP #1	Run **1 minute** O2 Ash with process wafer(s) and Si wafer (306 or 309)	Polymerized PR removal, crucial for PR descum.		
		Upon release with indirect DI spray, immediately submerge in DI water			
		Soak in hot 1165 @ 80C for minimum 16 hr			
		Rinse in hot 1165 for 5 min			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
Regrowth Prep					
	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	UV Ozone	Run empty for 30m			
		Load FET and run for 30m			
	MBE Lab	Etch 1m HCl:DI 1:10			
		Load into MBE ASAP	Any special requests? Confirm with the Grower		

Process Step	Equipment	Process Step	Notes	X	Date
Extra Note Space	N/A	N/A	Who (re)grew it? _____		
Poly InAs Planarization					
		Prepare process wafer(s), one Si quarter			
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Oven	Prepare Al carrier, 110C 5m			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS to Si, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR510, spin 4krpm 30s			
		Apply SPR510 to process wafer, spin 4krpm 30s			
		Softbake 90C 60s			
		Postbake 110C 60s			
PR Thickess Check	Filmetrics	Measure thickness of PR on SI	Thickness: _____		
ICP Prep	ICP #1	Run 30m O2 Ash empty (306 or 309)			
PR Ashing		Run 30m O2 Ash with process wafer(s) and Si wafer (306 or 309)	Load up to 4 quarters (or equivelent)		
		O2 Ash Power: _____ W			

Process Step	Equipment	Process Step	Notes	X	Date
		Measure thickness of PR on SI and extrapolate rate	Thickness: _____ Rate:_____		
	ICP #1	Run until PR ~____nm thick (thickness determined from total stack height!)	Either remove wafers or just use in next etch		
	Any Microscope	Verify the the sio2 is exposed			
Poly Removal	Acid Bench	Mix InGaAs/InAlAs/InP wet etch: 1:1:25 H3PO4: H2O2: DI (10mL:10mL:250ml)			
		Etch sample____ m	1m appears sufficent, 2m is safer. Particulate = gate leakage!		
	Any Microscope	Verify the etch, continue etching until clear	Total etch time:		
		Soak in hot 1165 @ 80C for minimum 16 hr			
		Rinse in hot 1165 for 5 min			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
ALIGNment Open Lithography, In(Ga)As, etch, Cr Etch, ISO etch					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			

Process Step	Equipment	Process Step	Notes	X	Date
		Apply HMDS through filter + syringe, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR510, spin 4krpm 30s			
		Softbake 90C 60s			
PR Expose	Autostepper	Load "GATE" reticle	Login: [10,1,26]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK, INV			
		Edit FGLALIGN as necessary			
		Are you leaving blank die???			
		Run EXEC FGLALIGN2IGLOBAL	Global alignment (precision not required)		
		Expose for ___s	Somewhere btwn .25-.28 is looking good right now		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
In(Ga)As Etch	Acid Bench	Mix InGaAs etch (slow on InAlAs, stops on InP) 1) Mix 50 g Citric Acid (anhydrous) with 50mL DI 2) Stir on hot plate (set to 70C) until clear 3) Add 1:1 Citric/H2O2, let cool to RT			
		Etch sample__m__s	Total etch time:		
	Any Microscope	Verify the etch, continue etching until field clear.			
Cr Mask Etch	ICP #1	10m O2 clean (Recipe 121)	Check binder for any Rodwell specific process settings		
		5m Cl2/O2 condition/season (163)			
		Mount sample with Santovac oil			
		Etch__m__s (163)	Etching 20nm in 1 minute is an overetch		
	Microscope	Verify that the Cr was etched			
	ICP #1	Run 1 minute (not minutes!) O2 Ash with process wafer(s) and Si wafer (306 or 309)	Polymerized PR removal, crucial for PR descum.		

Process Step	Equipment	Process Step	Notes	X	Date
InAlAs Etch	Acid Bench	Mix InGaAs/InAlAs/InP wet etch: 1:1:25 H3PO4: H2O2: DI (10mL:10mL:250ml)			
		Etch sample ___m ____s	Total etch time:		
	Any Microscope	Verify the etch, continue etching until clear. Watch for device undercutting. Do not agressively undercut!			
SiO2 removal	HF Bench	Mix up Tergitol/HF solution: add ___ drops tergiol, add 100 or 200 mL H2O with sprayer to mix well. Add BOE to top off to 400 mL.			
		_____ sec BOE HF dip ("Buffered HF Improved")	Total etch time:		
	Any Microscope	Verify the etch, continue etching until clear. Watch for device undercutting. Do not agressively undercut!			
InAlAs Etch	Acid Bench	Mix InGaAs/InAlAs/InP wet etch: 1:1:25 H3PO4: H2O2: DI (10mL:10mL:250ml)			
		Etch sample ___m ____s	Total etch time:		
	Any Microscope	Verify the etch, continue etching until clear. Watch for device undercutting. Do not agressively undercut!			
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			

Process Step	Equipment	Process Step	Notes	X	Date
ISO2 Lithography, Partial Device Isolation, Dummy Gate Removal					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS through filter + syringe, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply SPR955-0.9, spin ___ krpm 30s			
		Softbake 90C 60s			
PR Expose	Autostepper	Load "ISO2" reticle	Login: [10,126]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK, INV			
		Edit ADCSD if necessary			
		Are you leaving blank die???			
		Run MAP FGLISO\INNER,OUTER	Align to inner die, shoot all die		
		Expose for ___ s	Somewhere btwn .25-.28 is looking good right now		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
SiO2 Etch	HF Bench	BOE Dip 30 sec	Enough to etch SiO2 dummy away		

Process Step	Equipment	Process Step	Notes	X	Date
In(Ga)As Etch	Acid Bench	Mix InGaAs etch (stops on InAlAs,InP) 1) Mix 50 g Citric Acid (anhydrous) with 50mL DI 2) Stir on hot plate (set to 70C) until clear 3) Add 5:1 Citric/H2O2, let cool to RT			
		Etch sample ___m ___s			
	Any Microscope	Verify the etch, continue etching until field clear.	Total etch time:		
InAlAs Etch	Acid Bench	Mix InGaAs/InAlAs/InP wet etch: 1:1:25 H3PO4: H2O2: DI (10mL:10mL:250ml)			
		Etch sample ___m ___s			
	Any Microscope	Verify the etch, continue etching until clear. Watch for device undercutting. Do not agressively undercut!	Total etch time:		
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
Oxide Deposition and Anneal			**Si pieces needed for ALD oxide etch rate calibration**		
Consider stepper calibration! Look at signupmonkey for last cal date. 1urad!					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			

Process Step	Equipment	Process Step	Notes	X	Date
SiO2 removal	HF Bench	Mix up Tergitol/HF solution	Recipe: add 2 drops Triton to BOE beaker. Spray H2O into sink for a few seconds. Pulse spray H2O into beaker, breaking up tertitol. ____ mL H2O. Stir with vertical teflon boat vigrously to mix Tergitol into solution. Once solution is mixed, at ____ mL of BOE. Only use vertical boat for the dummy etch!		
		____m ____ sec BOE HF dip ("Buffered HF Improved")	2 to 3 minutes is typical. Longer promotes better large feature liftoff. 3 minutes with triton solution. Triton appears to lift off chrome better. Might be longer settling time.		
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
Alumina Deposition	FlexAL ALD	___ cycles _____	**Si quarter in chamber, seasoning/TMA verification step**		
Sample Cleaning	Acid Bench	Etch surface ox. in BOE , ____m			
		Vent loadlock, go to next step immediately			
		Immediately load samples on to private AL2O3 carrier wafer			
		____ cycles _____. **Include CV square for dielectric testing. Include Si quarter for VASE/etch test.**	**About 1.1 Angstom/cycle**		
		Hold samples in loadlock until next layer deposition is ready.			
Hafina Deposition	FlexAL ALD	___ cycles _____	**Nothing in chamber, seasoning step**		
		____ cycles _____ **Include CV square for dielectric testing. Include Si quarter for VASE/etch test.**	**About 1.1 Angstom/cycle**		
Oxide Anneal RTA	RTA	Pre-anneal bake: 500C 15 minute FGA, private SiO2 carrier wafer only	**Nothing in chamber, seasoning step**		
		Sample bake: ____C ____ minute FGA, private carrier wafer			

Process Step	Equipment	Process Step	Notes	X	Date
Extra Note Space	N/A	N/A			
Gate Liftoff					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS through filter + syringe, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply nLOF-5510, spin 4krpm 30s			
		Softbake 90C 60s			
PR Expose	Autostepper	Load "LIFT" reticle	Login: [10,126]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK, INV			
		Edit FGLLIFT if necessary			
		Are you leaving blank die???			
		Run "MAP FGLLIFT/INNER,OUTER"	Align to inner die, shoot all die		
		Expose for ____s	Somewhere btwn 25- 28 is looking good right now		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Liftoff	Thermal Evap #1	Load Ni (two boats) center slot, adjust mirrors for proper deposition, check crystal			
		Evaporate ___A Ni @ ___A/sec			
		Evaporate ___A Au @ ___A/sec			
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: ____		

Process Step	Equipment	Process Step	Notes	X	Date
Extra Note Space	N/A	N/A			
Source/Drain Etch and Liftoff					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS through filter + syringe, wait 20s			
		Spin 4krpm 30s			
		Wait 1m			
		Apply nLOF-5510, spin 4krpm 30s			
		Softbake 90C 60s			
PR Expose	Autostepper	Load "SD" reticle	Login: [10,126]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK, INV			
		Edit ADCSD if necessary			
		Are you leaving blank die???			
		Run "MAP FGLSD/INNER,OUTER"	Align to inner die, shoot all die		
		Expose for ____s	Somewhere btwn .25-.28 is looking good right now		
		Run "EXEC FGLSD/BLNK"	For the blank die		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Dielectric removal	HF Bench	~____ sec BOE HF dip ("Buffered HF Improved") with dummy Si piece to verify oxide removal			
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			

Process Step	Equipment	Process Step	Notes	X	Date
		Repeat previous lithography and continue!			
Liftoff	Ebeam #1, 4 or Thermal #1	Unload all public sources, load Ti Pd and Au private sources			
		WEIGH THE PUBLIC AU!			
		Evaporate ___A Ti @ 1A / sec	Typically 5 nm evaporated behind shutter, 15 nm during sample rotation		
		Evaporate ___A Pd @ 1 to 3 A / sec	Typically 60 nm		
		Evaporate ___A Au @ 1 to 3 A / sec	Typically 100 nm		
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			
Device Test	Device Test	Device Test	**Test a few devices in the lab. If they work proceed to device isolation after ADC approval.**		
ISO2 Lithography, Full Device Isolation					
Solvent Clean	Solvent Bench	3m Acetone, 3m Iso, carry wet to dev			
	Develop Bench	3m DI, N2 blow dry (<20PSI)			
	Dehydration Bake	5m bake on 110C plate			
PR Resist Spin	PR Bench	Test Spin wafer 4krpm 30s (recipe 7)			
		Apply HMDS through filter + syringe, wait 20s			
		Spin 4krpm 30s			

Process Step	Equipment	Process Step	Notes	X	Date
		Wait 1m			
		Apply SPR510, spin 4krpm 30s			
		Softbake 90C 60s			
PR Expose	Autostepper	Load "ISO2" reticle	Login: [10,126]		
		Place wafer onto chuck			
		Run SETUP [10,1], CHUCK, INV			
		Edit FGLISO if necessary			
		Are you leaving blank die???			
		Run "MAPFGLISO/INNER,OUQUAR"	Align to inner die, shoot all die		
		Expose for ____s	Somewhere btwn .25-.28 is looking good right now		
		Postbake 110C 1m			
PR Develop	Develop Bench	Fresh AZ300MIF 60s with slight agitation			
		2m DI Rinse			
	Any Microscope	Check lithography in microscope			
Dielectric removal	HF Bench	~60 sec BOE HF dip ("Buffered HF Improved") with dummy Si piece to verify oxide removal			
III-V Removal	Acid Bench	Mix InGaAs/InAlAs/InP wet etch: 1:1:25 H3PO4: H2O2: DI (10mL:10mL:250ml)			
		Etch sample 1m			
	Any Microscope	Verify the etch, continue etching until clear. Watch for device undercutting. Do not agressively undercut!	Total etch time:		
InP Removal	Acid Bench	1:1 H2O:HCl (10nm/min quoted rate)			
		Etch sample 30 sec			
	Any Microscope	Verify the etch, continue etching until clear	Total etch time:		
		Soak in 1165 @ 80C for minimum 2h			
		2m Iso, 2m DI Rinse, N2 Dry (<20 PSI)			
	Solvent Bench	Carry wet, 2m Acetone, 2m Iso			
		2m DI Rinse			
	Any Microscope	Check etch and yield			

Process Step	Equipment	Process Step	Notes	X	Date
	Dektak	Note Dektak Pad thickness	Thickness: _____		
Extra Note Space	N/A	N/A			