University of California

Santa Barbara

High Resolution High Bandwidth $\Sigma - \Delta$ ADC in the Transferred-Substrate HBT Technology

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Doctor of Philosophy
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Shrinivasan Jaganathan

Committee in charge:

Professor Mark Rodwell, Chairperson
Professor Steve Butner
Professor Stephen Long
Professor Umesh Mishra

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The dissertation of Shrinivasan Jaganathan
is approved:

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_____

_____
Committee Chairperson

September, 2000

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Vita

- July 1, 1972: born in Kumbakonam, India.
- July, 1993: BTech, Electrical Engineering, Indian Institute of Technology, Bombay, India.
- March, 1997: M.S., Electrical and Computer Engineering, University of California, Santa Barbara.
- 1996-2000: Research Assistant, Department of Electrical and Computer Engineering, University of California, Santa Barbara.

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Abstract

High Resolution High Bandwidth $\Sigma - \Delta$ ADC
in the
Transferred-Substrate HBT Technology

by
Shrinivasan Jaganathan

The advances in semiconductor technologies are being driven by an explosive growth in the fiber-optic and telecommunication market. This has pushed the demand for high performance broadband analog and high clock-rate digital systems. In the context of radar receivers in defense applications, this translates into requirements for high signal bandwidth ($>$ 100 MHz) with high resolution ($>$ 16 bits) and signal-to-noise ratio ($>$ 98 dB). Superior circuit design techniques in a high speed device technology are required to meet these specifications. In addition to high device bandwidth (f_t and f_{max} in excess of 300 GHz), the transferred substrate process offers the significant advantages from the point of view of circuit design - low parasitic microstrip wiring environment with integral ground plane and a low thermal impedance environment for high power operation and increased packing density. In this work, a $\Sigma - \Delta$ ADC operating at a clock rate of 18 GHz with 6.2 bits of resolution at 990 MHz signal bandwidth has been demonstrated. The technology has the potential to yield flip-flops at 100 Gb/s clock rates which can translate into $\Sigma - \Delta$ ADCs operating at $>$ 50 GHz clock rates.

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3.1.1 Loop design 38

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Chapter 1

Introduction

Advances in VLSI technology are making more sophisticated radio receiver architectures practical. They enable more flexibility in design of communication receivers - even receivers that are capable of handling multiple modulation standards. An important trend in this area is to handle more of the signal processing in the digital domain. This means that the analog-to-digital (A/D) function moves "forward" in the signal chain, closer to the antenna. The ultimate goal in a radio receiver design is to directly digitize the RF signal at the output of the antenna. Further receiver functions would, then, be implemented in digital hardware or software (DSP). Trends in receiver design have progressively evolved toward this goal by incorporating digitization closer to the receive-antenna for systems at increasingly higher frequencies and bandwidths. These receivers are expected to find applications in areas such as mobile cellular, satellite and personal communication services [1].

One important consumer of digital receiver hardware is the military electronics sector. The signal processing requirements of military avionics systems are constantly increasing to counter the threats from enemies. A/D converter performance requirements form the backbone of military radar and reconnaissance applications. Current military communication radars use a bank of high-resolution, low-bandwidth ADCs along with switched filters. These are expensive on account of the high component count as well as the associated bulk. Because a small frequency band is scanned at a time, these have a large response time.

Moving the digital interface closer to the antenna results in lower costs,

smaller physical size, increased speed of response and improved overall performance [2]. However, this reduction (Fig. 1.1) in RF downconversion stages places requirements on ADC performance which are not currently met by commercial technologies.

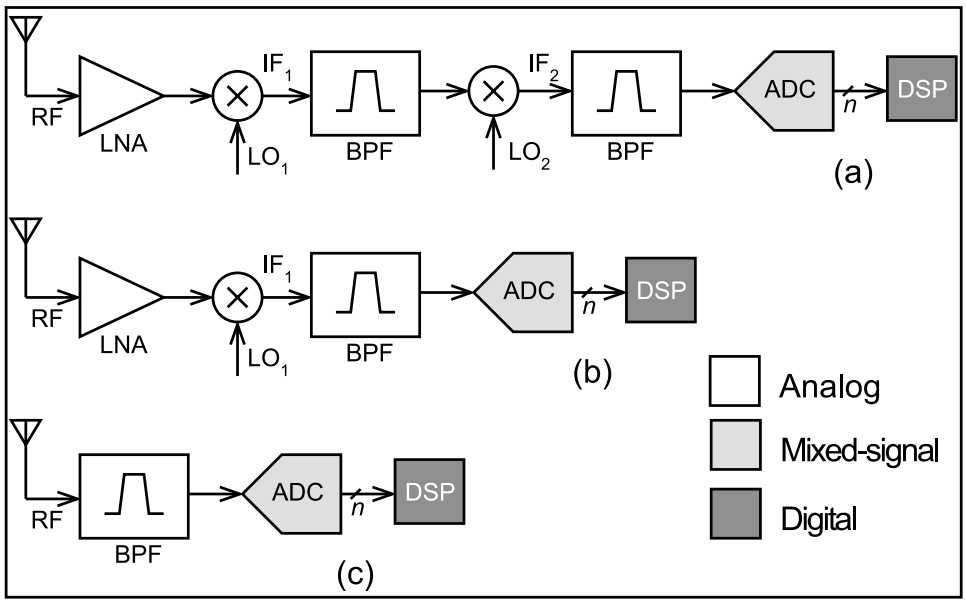

Figure 1.1: Migration of the digital interface toward the antenna in receiver systems: (a) Double Down Conversion receiver (b) Single Down Conversion Receiver (c) Direct Conversion (Software) Receiver.

1.1 ADC Fundamentals

As the name suggests, Analog-to-Digital Converters (ADC) take a continuously varying analog input and output a quantized digital n-bit output.

ADCs primarily fall into two categories: Nyquist rate converters and oversampling converters. Nyquist rate converters quantize input samples at a rate slightly above that specified by Nyquist's sampling theorem [3]. Thus, a band-limited input signal with maximum frequency component, f_{high}, is sampled every $1/f_s$ seconds, $f_s = 2f_{high}$ being the sample rate. The result is a single digital output sample from a single analog input sample. In contrast, an oversampling converter samples the input at a rate greater

than Nyquist's sampling theorem ($f'_s = n.f_{high}, n > 2$). A brief description of each kind of ADCs is presented in the following subsections.

1.1.1 Nyquist Rate ADCs

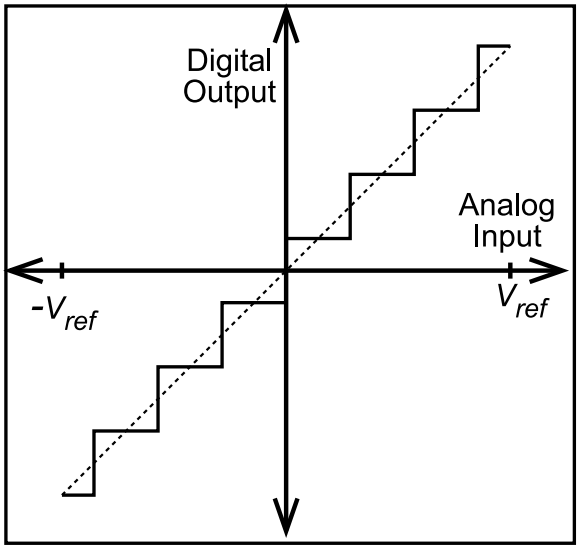

Figure 1.2: Mapping from Analog to Digital Domain.

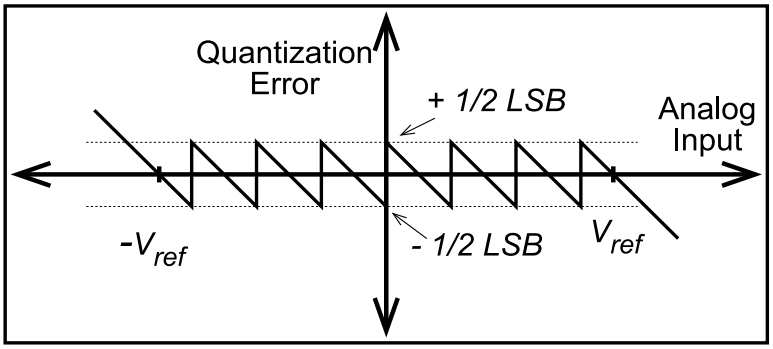

Figure 1.3: Quantization Error vs. Analog Input.

A basic Nyquist rate ADC performs a sample-by-sample mapping from the analog to the digital domain (Fig. 1.2). The analog input varies continuously from $-V_{ref}$ to $+V_{ref}$, while the digital output is quantized into 2^n

discrete levels for an n-bit converter. Quantizing the input results in error, as shown in Fig. 1.3. Ideally, for the input range of the ADC, quantization noise is bound between $\pm$ 0.5 LSB, where LSB (Least significant bit) represents the minimum analog step size. A typical implementation of a Nyquist rate ADC is the parallel version known as Flash ADC (Fig. 1.4). Other popular implementations of Nyquist rate ADCs include the Successive Approximation and the Pipelined ADCs [4]. A more detailed discussion of Nyquist rate ADCs follows in section 2.1.

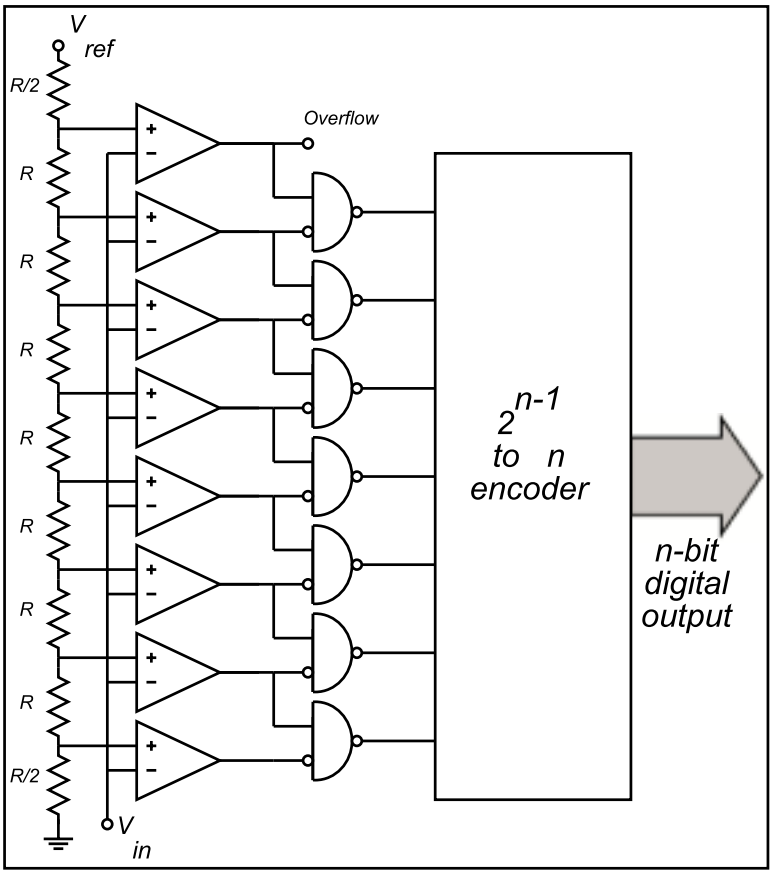

Figure 1.4: A 3-bit Flash ADC.

1.1.2 Oversampling ADCs

Sigma Delta ($\Sigma - \Delta$) ADCs are the most common type of oversampling ADCs. A generic discrete time $\Sigma - \Delta$ converter is shown in Fig. ??. In such a converter, oversampling (sampling at a rate higher than Nyquist rate) is supplemented by noise-shaping. The architecture uses a filter in a feedback loop with the aim of shaping the spectrum of quantization noise so as to maximize the signal-to-noise ratio (SNR). The loop-filter accomplishes this by providing a high-pass transfer function for the noise. The total quantization noise integrated over the entire frequency spectrum is constant. Thus, the high-pass transfer function results in the noise becoming redistributed, with noise in the signal band being suppressed and more of the noise power appearing at higher frequencies. The elevated stopband noise is of little concern since it can be rejected with digital filtering.

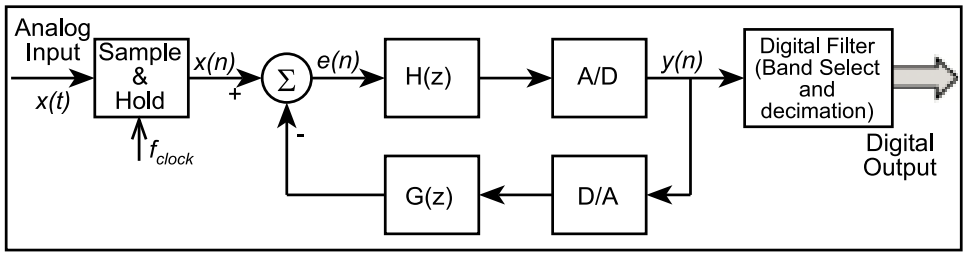

Figure 1.5: Block diagram of a generic discrete-time $\Sigma - \Delta$ ADC

$\Sigma - \Delta$ ADC is specified by two parameters: order of the converter and the oversampling ratio. The order of the converter is determined by the order of the loop filters, $H(z)$ and $G(z)$ (Fig. ??), while the oversampling ratio (OSR) is determined by the bandwidth of input signal and the clock frequency, f_{clock}. The two together determine the SNR and the effective number of bits (ENOB) resolution achievable. Noise-shaping for a $\Sigma - \Delta$ ADC with $H(z)$ as a low-pass filter is shown in Fig. 1.6. The operation of $\Sigma - \Delta$ ADCs is described in greater detail in section 2.2.

Trends in performance of ADCs suggest that $\Sigma - \Delta$ ADCs attain the highest resolution for relatively lower signal bandwidths (Fig. 1.7) compared to conventional Nyquist rate converters. Consequently, $\Sigma - \Delta$ techniques are heavily used in audio applications where the signal bandwidth is only about 20 kHz, while the resolution needed is high (up to 14 bits) [5]. Flash converters, on the other hand, find wider reach into broadcast

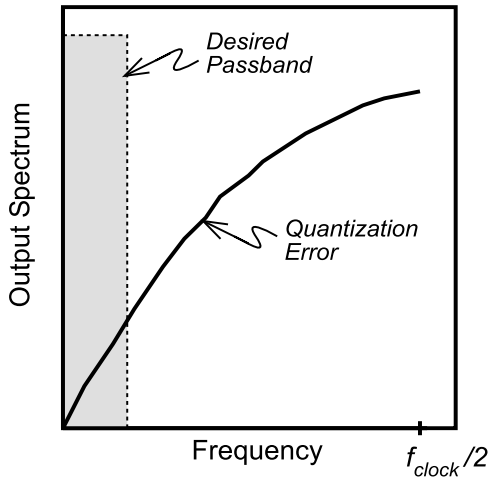

Figure 1.6: Signal passband and colored quantization error spectrum of a low-pass $\Sigma - \Delta$ ADC.

video applications where signal bandwidth is ≈ 5 MHz, but only ≈ 8 bits resolution is required.

$\Sigma - \Delta$ ADCs have several advantages over Nyquist rate designs:

- First, the accuracy of the $\Sigma - \Delta$ converters is not directly correlated to that of the components used. For Nyquist rate converters, each signal sample is quantized at the full precision or resolution of the converter. The resolution of such converters implemented on VLSI chips is limited by the technology of choice. For example, some Flash ADCs rely on matching of resistors to perform precise division of a reference voltage (Fig. 1.4). This divided reference is then compared with the input to place the input in one of the 2^N bins. Achieving N bit resolution from such converters demands the resistor values and comparator offsets to be matched to within 1 part in 2^N. For a 10 bit ADC, this would translate in a 0.1% matching in components! Thus, it is extremely difficult to attain high resolution in Nyquist rate converters without the use of techniques such as laser trimming of components.

- Second advantage is the relaxed requirement on anti-aliasing filtering. The necessity of anti-aliasing is explained in section 2.1. In fact, with sufficiently high *OSR* the spurious input tones beyond the frequency

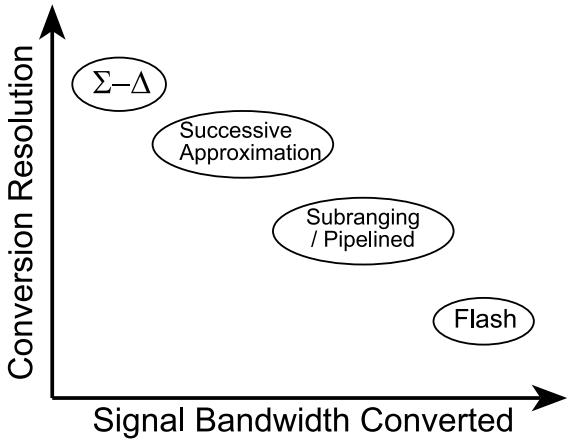

Figure 1.7: Bandwidth-resolution tradeoff in ADCs.

band of interest may be sufficiently attenuated by the signal transfer function. In such cases an anti-aliasing filter may not even be needed. On the other hand, Nyquist rate designs require an anti-aliasing filter with a very sharp cut-off. Such analog filters are very expensive and difficult to realize.

One disadvantage of $\Sigma-\Delta$ converters is the extremely small usable passband. This is so because the clock rate required for a given *OSR* increases linearly with the signal bandwidth of interest. Increasing the sampling rate translates into demand for higher transistor speeds. A second disadvantage pertains to the loop instability associated with higher order $\Sigma - \Delta$ converters. This instability is usually observed as limit cycle oscillations under some input conditions. An approach to solving these problems has been to use a multibit quantizer in the forward path along with a mulitbit digital-to-analog converter (DAC) in the feedback path. Using a multibit DAC in the feedback path has associated mismatch problems which result in a lower *SNR*.

1.2 Motivation for this work

From the discussion presented above, it is clear that $\Sigma - \Delta$ ADCs can adequately handle data conversion requirements at lower input frequencies.

However, a significant improvement in device technology is needed to translate their advantages to higher frequencies ranging from a few tens of MHz to a few GHz. This shift to higher frequencies is primarily motivated by the military avionics requirements [2] which can be broadly categorized into:

- Communications Navigation and Identification (CNI): These receivers need to provide support for high bit-rate secure data and voice communication through satellites, instrument and microwave landing systems and integrated global positioning systems (GPS) systems.

- Electronic Warfare (EW): These systems are for self-defense of navy ships. EW systems include electronic countermeasures (transmitting false radar returns) and transmitting signals to jam enemy radars. Current EW receivers are analog with multiple downconversion stages. However, future requirements on the receivers will demand converters with dynamic range in excess of 60 dB and with input signal bandwidths greater than 3 GHz. This is already pushing the receiver architecture closer to direct conversion type.

- Radar: Some of the current limitations of radar receivers that need to be addressed in future include:

  - Higher dynamic range : need higher resolution ADC
  - Higher spectral purity

  These requirements may translate in ADC performance of $\geq$ 100 dB dynamic range over instantaneous bandwidths as high as 100 MHz.

All these future requirements of the military can not be met by either current "commercial-off-the-shelf" (COTS) converters (A review of the current state of the art in ADC performance has been published by Walden [6]), or by new designs in IC technologies currently available. At the same time, an IC process capable of providing fast devices should be a good candidate for designing high speed ADCs.

Bipolar transistors are suitable for high speed circuits because of their reproducible DC characteristics, excellent control of turn-on voltage, high transconductance and high bandwidth. Wide band-gap emitters in heterojunction bipolar transistors (HBTs) enable the use of high base doping without degrading the emitter injection efficiency. This reduces the base

resistance in HBTs compared to Si bipolar transistors, while maintaining high current gain (β). The material properties of InP-based semiconductors provide attractive features for high speed devices and ICs. High electron mobility in the InGaAs base and high electron saturation velocity in the InGaAs (or InP) collector layer leads to low transit times and low access resistances. While AlGaAs/GaAs HBTs have a turn-on voltage of 1.4 V, the small bandgap of the InGaAs base sets the turn-on voltage in the InAlAs/InGaAs HBT at 0.7 V. The low turn-on voltage reduces the power consumption and allows use of smaller supply voltages.

The above reasons make HBTs in the InP material system a strong choice for high speed ICs [7], [8], [9]. However, there is the issue of scalability. While the bandwidth of HEMTs (0.1 μm HEMTS) and CMOS (0.18 μm) transistors are improved by reducing their lithographic dimensions, the bandwidth of normal mesa HBTs does not improve significantly by scaling emitter dimensions below $\sim$ 1 μm. Among several approaches, one solution to the scaling problem is the transferred substrate process [10] - a process which modifies the HBT topology so that HBT bandwidth can be improved by reducing lithographic dimensions. A detailed description of the underlying concepts and physics of the transferred substrate HBT process is available in [11], [12], [13].

The transferred substrate HBT process has continued to mature over the last few years with demonstration of relatively small (3-5 transistors) analog circuits, e.g. wideband amplifiers ([15], [16], [17]). In the last two years, digital circuits have been designed in this technology, with larger scales of integration. Examples include a 20 transistor CML and a 50 transistor ECL divider both operating at 48 GHz [18]. More recently, a 76 transistor ECL divider operating at 66 GHz has been demonstrated [19].

In this work, a $\Sigma - \Delta$ ADC with about 150 transistors has been demonstrated in the transferred substrate HBT technology. The work involved system design, design of circuit blocks, layout and fabrication. HP ADS 1.3 layout editor was used for the purpose of layout. However, the tool is not suited for design of a large IC. A rudimentary version of design rule checker (DRC) has been implemented to facilitate the layout. On the processing front, interconnect density severely limits the integration density. Another processing issue that limits the integration density is the minimum size of ground via in the Benzocyclobutene (BCB) dielectric. Layout and process changes (improvements) have been effected to account for this shortcoming.

1.3 Organization of Thesis

The main focus of this work was on circuit design. Given that the $\Sigma - \Delta$ ADC is a non-linear feedback system, attention is needed on the system level design. Chapter 2 focuses on the general theory of $\Sigma - \Delta$ ADCs with a brief description of their history. Different approaches to implementation (discrete vs. continuous time) are discussed. A section is devoted to understanding the various specifications of ADCs. The effect of various $\Sigma - \Delta$ ADC parameters (e.g. order of the system, oversampling ratio) on these specifications is analyzed.

Chapter 3 describes in detail the design of the $\Sigma - \Delta$ modulator. Both the system level design of the ADC, as well as, the design of various circuit blocks are discussed. The effect of various factors limiting the sampling rate is discussed.

Measured data and results are presented in chapter 4. A description of the measurement setup and the theory behind the measurement is also presented. An analysis of the measured data is presented in the context of measurement limitations.

Chapter 5 concludes the thesis by summarizing the results while suggesting future improvements.

Appendix A describes the process flow used in the fabrication of the ICs. A significant part of the work described in this thesis was spent in the cleanroom battling with processing issues. Some of these issues are described in Appendix B. Appendix C describes briefly the implementation of Design Rule Checking in HP ADS which allows us to identify the design rule violations in the layout in an efficient manner.

Chapter 2

$\Sigma - \Delta$ ADC: Theory and Operation

This chapter describes the theory of $\Sigma - \Delta$ ADCs. To be able to appreciate that fully, we need to review a few basic concepts from signal processing.

2.1 Nyquist Rate Conversion

Analog to digital conversion of a signal is described in terms of 2 distinct operations [5]: Uniform sampling in time, and quantization in amplitude.

2.1.1 Sampling

In the sampling process, a continuous time signal, $x(t)$ is sampled at uniformly spaced time intervals, T_s, resulting in samples, $x[n] = x[nT_s]$. For an ideal sampling, this is equivalent to multiplying the input analog signal with a train of delta functions. The output is

$$x_s(t) = x(t) \sum_{k \to -\infty}^{\infty} \delta(t - kT_s) = C_o x(t) \sum_{k \to -\infty}^{\infty} e^{jkf_s t} \tag{2.1}$$

where C_o is a constant. In the frequency domain, the Fourier transform of the sampled output is

$$X_s(f) = C_o \sum_{k \to -\infty}^{\infty} X(f - kf_s) \tag{2.2}$$

In the frequency domain, the process of sampling creates versions of signal spectrum repeated periodically at multiples of the sampling frequency $f_s = 1/T_s$.

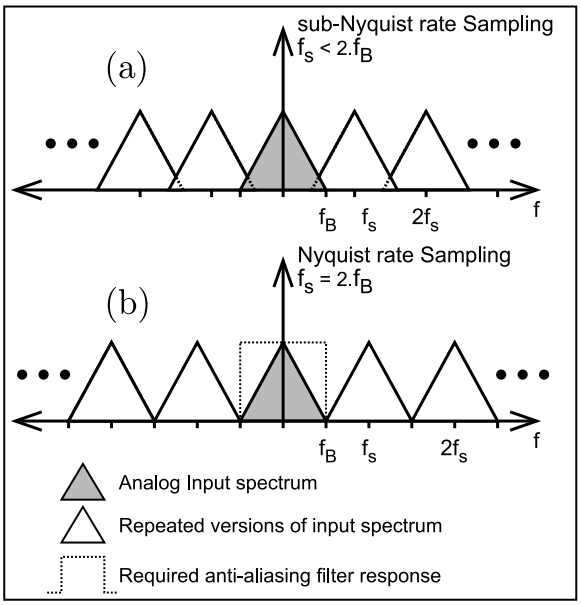

Figure 2.1: Spectrum of a band-limited input spectrum sampled at (a) below Nyquist rate; (b) Nyquist rate, showing the required anti-aliasing filter response.

The input signal is assumed to be band-limited to frequencies $|f| \leq f_B$. If the signal is sampled without violating Nyquist's sampling criterion ($f_s \geq 2f_B$), then the repeated versions of the original signal spectrum do not overlap (Fig. 2.1(b)). Therefore, the original signal can be recovered by using a filter with very sharp cut-off frequency of f_B at the output. Thus, if $f_s \geq f_B$, process of sampling is non-destructive.

If $f_s < 2f_B$, the repeated versions of the input signal spectrum overlap at the edges (Fig. 2.1(a)). Thus the high-frequency components of the input are distorted. Under this condition, the process of sampling is destructive and hence not invertible. In such cases, the input signal needs to be band-limited to half the sample-rate by using a filter with very sharp cutoff. This filter is called an anti-aliasing filter.

2.1.2 Quantization

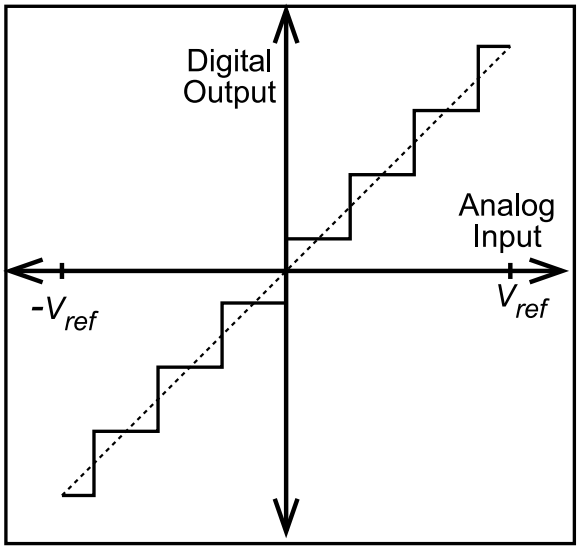

Figure 2.2: Mapping from Analog to Digital Domain.

The next process in analog to digital conversion is to quantize the amplitudes of input samples into finite set of output values. Typical transfer characteristics of a quantizer is shown in Fig. 2.2. Unlike Nyquist rate sampling, the process of quantization is not invertible, since an infinite number of input amplitudes are mapped to a finite number of output values. The quantized output values are represented by a digital code word (often referred to as Pulse Code Modulation or PCM) composed of a finite number of bits. An ADC quantizer with Q output levels is said to have a N bits of resolution where $N = log_2(Q)$. If the full-scale input of the ADC is V_{ref}, then, only input values separated by a least significant bit (LSB), $\Delta = 2V_{ref}/(Q-1)$ can be distinguished or resolved to different output levels. Fig. 2.3 shows the result of sampling and quantizing a sine wave with a 3 bit quantizer.

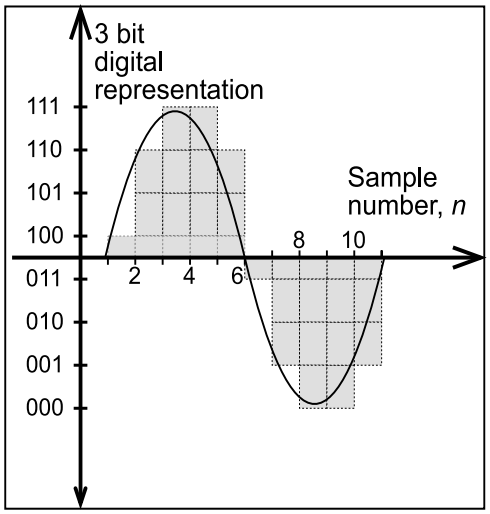

Figure 2.3: A sinusoidal signal quantized by a 3-bit ADC.

2.1.3 Performance modeling of Nyquist rate PCM converters

The quantizer embedded in an ADC is inherently a non-linear system. To estimate the *SNR* of the ADC, the variance of the quantization error generated by quantizer needs to be computed. To make the analysis simple, the quantizer is often linearized (Fig. 2.4) and modeled by a noise source $e[n]$, added to the signal $x[n]$, to produce the output quantized signal $y[n]$:

$$y[n] = x[n] + e[n] \tag{2.3}$$

Further analysis is simplified by some assumptions about the statistics of the noise process.

- The error sequence $e[n]$ is a sample sequence of a stationary random process.
- The noise sequence $e[n]$ is uncorrelated with the input sequence $x[n]$.
- The probability density function of the error process is uniformly distributed over the range of quantization error, i.e over $\pm\Delta/2$.

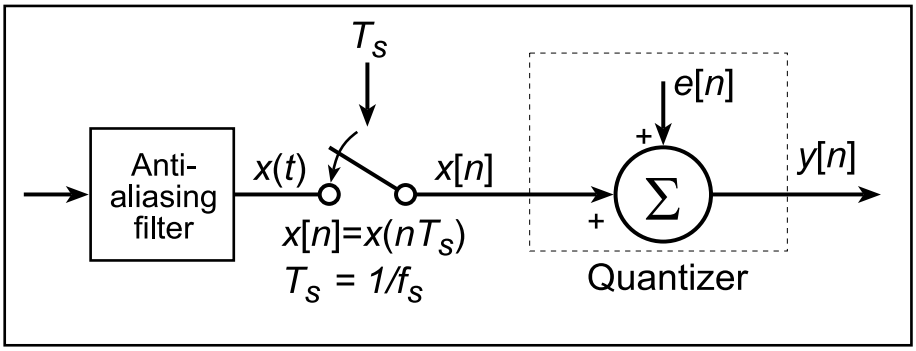

Figure 2.4: linearized model of a conventional Nyquist rate ADC.

- The random variables of the error process are uncorrelated, i.e. the error is a white noise process.

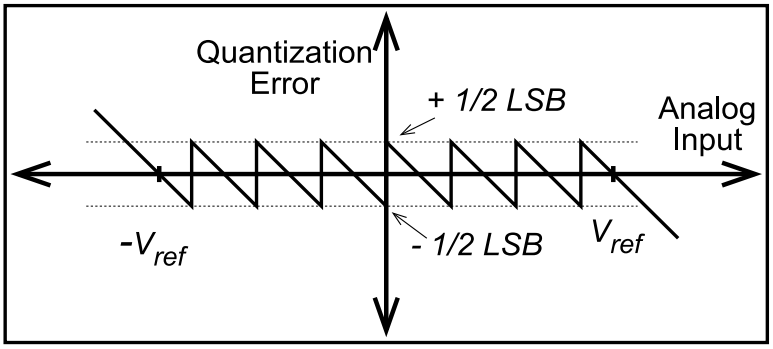

Figure 2.5: Quantization Error vs. Analog Input.

These assumptions provide a reasonable approximation to the spectrum of the quantization error when the resolution of quantizer, N is large, the input is sufficiently small to not overload the quantizer and when successive samples of the input signal are sufficiently uncorrelated. The quantizer is said to overload if the input extends beyond the maximum input range of the quantizer as a result of which, the quantization error extends beyond the range, $\pm\Delta/2$.

The variance of the quantization noise (a measure of the noise power) for an N bit quantizer is

$$\sigma_e^2 = \int_{-\Delta/2}^{\Delta/2} x^2 . \frac{1}{\Delta} . dx = \frac{\Delta^2}{12} = \frac{1}{12} \left(\frac{2V_{ref}}{2^N - 1} \right)^2 \simeq \frac{1}{12} \left(\frac{2V_{ref}}{2^N} \right)^2 \qquad (2.4)$$

If the input signal is treated as a zero mean random process with power σ_x^2, then the signal to quantization noise ratio becomes

$$SNR \ = 10 \log_{10} \left(\frac{\sigma_x^2}{\sigma_e^2} \right) = 10 \log_{10} \left(\frac{\sigma_x^2}{V_{ref}^2} \right) + 4.77 + 6.02N \quad (dB) \qquad (2.5)$$

There is ~ 6 dB improvement in SNR for every 1-bit increment in N. The maximum SNR that can be achieved corresponds to a full scale input (i.e. $\sigma_x^2 = V_{ref}^2/2$).

$$\mathrm{SNR_{max}} = \log_{10} \left(\frac{V_{ref}^2/2}{V_{ref}^2} \right) + 4.77 + 6.02N = 6.02N + 1.76 \quad (dB) \qquad (2.6)$$

In the absence of any spurious tones, the maximum SNR (Eq. 2.6) is also referred to as the dynamic range.

2.2 Oversampled PCM Conversion

The resolution obtained from Nyquist rate conversion can be increased by employing oversampling. In this method, the samples are acquired from the analog input waveform at a rate (f_{s2}) significantly higher than the Nyquist rate (f_{s1}). Each of the resulting samples is quantized by a N bit ADC. Quantization noise generated by the converter still has the variance specified by (Eq. 2.4). Since the samples are now arriving at a rate $f_{s2} > f_{s1}$, the quantization noise is distributed over a frequency range $[-f_{s2}/2, f_{s2}/2]$ (Fig. 2.6). The total quantization noise in the signal bandwidth is $2\sigma_e^2 f_B / f_{s2}$ ($< \sigma_e^2$, since $f_{s2} > 2f_B$). We define the OSR as

$$OSR \ = \frac{f_s}{2.f_B} \qquad (2.7)$$

Thus, the quantization noise in the signal bandwidth is only σ_e^2/OSR. For large values of OSR, a relatively small fraction of the total noise power

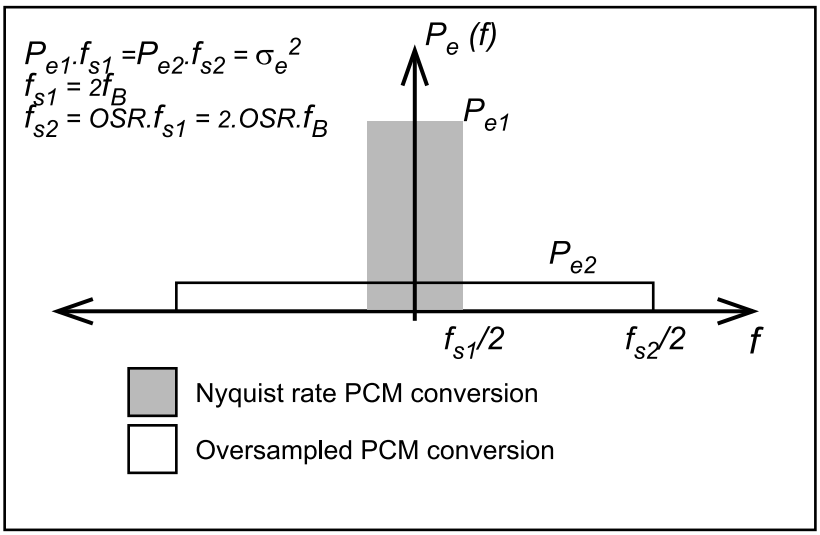

Figure 2.6: Quantization noise spectrum for Nyquist rate and oversampled PCM ADCs.

falls inside the signal bandwidth and hence contributes to the *SNR*. The noise power outside the signal bandwidth can be significantly attenuated with a digital low-pass filter following the ADC. Having rejected the out-of-band noise, the filtered samples can be down-sampled digitally to the Nyquist-rate ($2f_B$). The process of down-sampling together with the low-pass filtering constitutes the process known as decimation.

2.2.1 Performance modeling of oversampled PCM converters

Fig. **??** shows the linearized model of an oversampled PCM converter. The time domain relation between output and input is still given by Eq. 2.3. This translates in Z-domain to :

$$Y(z) = X(z) + E(z) \tag{2.8}$$

where X, Y and E are Z-transforms of input, output and the quantization error process, respectively. The white noise assumption of the noise process implies that the noise power spectral density is $P_e(f) = \sigma_e^2/f_s$. Assuming an ideal low-pass filter with cutoff frequency of f_B at the output of

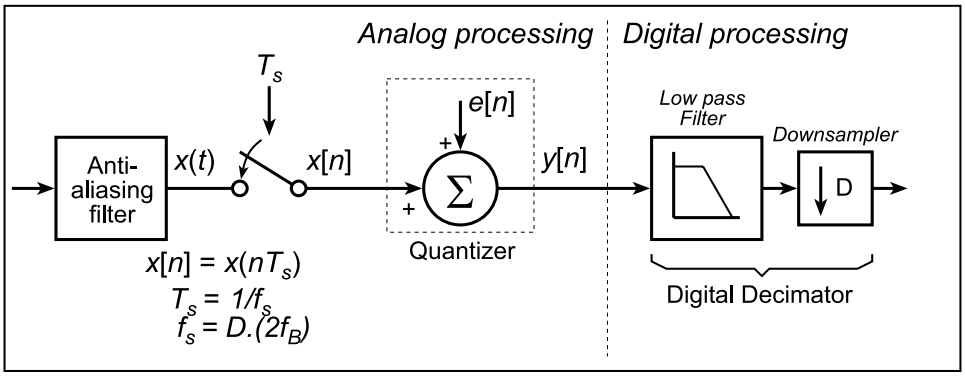

Figure 2.7: linearized model of an oversampled PCM data conversion system

quantizer, the noise power (σ_{ey}^2) at the output of the converter is

$$\sigma_{ey}^2 = \int_{-f_B}^{f_B} P_e(f)df = \sigma_e^2 \frac{2f_B}{f_s} = \frac{\sigma_e^2}{OSR} \tag{2.9}$$

Since the signal power, σ_x^2, is assumed to occur only over the signal band, it remains unchanged. The maximum achievable SNR is therefore

$$SNR = 6.02N + 1.76 + 10\log_{10}(OSR) \quad (dB) \tag{2.10}$$

Thus, a doubling of the OSR provides a 3 dB increase in SNR or a half bit improvement in resolution.

The oversampled PCM ADC can obtain a higher resolution than that of the internal quantizer at the expense of a higher sampling rate. Therefore, the oversampled PCM converter requires a less complex analog circuit to achieve the desired resolution. If the input has very little spectral content beyond $f_s/2$, only these components result in aliasing after sampling. If the anti-aliasing filter provides sufficient attenuation for the frequency components between f_B and $f_s/2$, the aliasing will not be a significant issue. Thus, by using a large OSR , a smaller stop-band roll-off is required for the anti-aliasing filter to achieve the same attenuation of aliasing components.

2.3 Performance metrics of ADCs

In general, the transfer characteristics of a quantizer differ from that shown in Fig. 2.2 because circuit imperfections move the transition points away

from desired levels. These variations in turn introduce errors in the ADC output. Performance metrics used to describe the deviation of ADC performance from that of an ideal converter fall in two categories [25]: *Static* and *Dynamic*.

Static metrics include

1. Offset: Offset is the x-intercept of the straight line that connects the end points of transfer characteristics.

2. Gain error: Deviation from unity of the slope of the ADC input-output transfer characteristics.

3. Differential non-linearity (DNL): DNL is the maximum deviation of difference between two consecutive transition points from the ideal point (1 LSB). A DNL more negative than -1 LSB means there is at least one code that can not be generated (known as a *missing code*).

4. Integral non-linearity (INL): INL is the maximum deviation, specified in bits, of the ADC input-output transfer characteristics from that of the ideal ∞-bit ADC.

Dynamic metrics include

1. Signal to noise ratio (*SNR*): *SNR* is defined as the ratio of input (output) signal power to the power of input (output) referred noise. The noise considered includes the noise generated by the circuit as well as the quantization noise, but not the power in the harmonics. For an ADC with uniform quantization levels, the *SNR* rises linearly with input power until the quantizer overloads when the *SNR* drops rapidly.

2. Signal to distortion ratio (*SDR*) or Total harmonic distortion (*THD*): *SDR* is the ratio of signal power to power in the harmonics at the output. If ADC non-linearities are described by a Taylor series, the amplitudes of spurious tones are expected to be proportional to the square or a higher power of the input signal power. Therefore, the *SDR* falls with increase in input signal power.

3. Signal to noise plus distortion ratio (*SNDR*): This parameter describes the ratio of signal power to the sum of power in all distortion components and in quantization and circuit noise. At low input power

the distortion terms are negligible and hence the *SNDR* follows *SNR*. However, as input power increases, the distortion starts becoming significant and *SNDR* follows *SDR*.

4. Dynamic range (*DR*): Dynamic range is equal to the ratio of overload level to the noise floor. The overload level is the power of input sinusoid (more than the power that achieves peak *SNDR*) that causes the *SNDR* to fall 3 dB below its peak value. The noise floor is defined as the input referred baseband noise comprising of the circuit and the quantization noise.

5. Spurious free dynamic range (*SFDR*): *SFDR* is defined as the ratio of (a) signal power to power in the strongest spectral tone when it equals the minimum detectable level and (b) minimum detectable signal power.

These dynamic measures can obtained from spectral analysis of the ADC output by performing a fast Fourier Transform, *FFT*, on the captured digital output data. The dynamic measures specify the ADC performance in the terms relevant to radio or radar receivers. Moreover, for high sample-rate ADCs, the dynamic errors may be many times larger than the static errors. Therefore, For communication and radar receivers, dynamic measures of performance are most important. In this work, we will be concentrating solely on *SNR* to evaluate ADCs.

2.4 $\Sigma - \Delta$ Analog to Digital Converter

$\Sigma - \Delta$ converters (chapter 1) operate by using oversampling in tandem with noise shaping to achieve high *SNR*. An early reference for these ADCs is Inose *et al* [21], [22] who presented the $\Sigma - \Delta$ converter as a modification of the Delta (Δ) modulator. Δ modulation (Fig. 2.8) is a digital modulation format for communication applications where the input signal is differentiated and converted into digital form before being transmitted.

$$e(t) = x(t) - \int_0^t y(\tau)d\tau \tag{2.11}$$

Thus, the transmitted signal $y[n]$ is oversampled and quantized version of the error signal $e(t)$. This modulation scheme is incapable of transmitting the DC component in the data; its dynamic range and *SNR* are

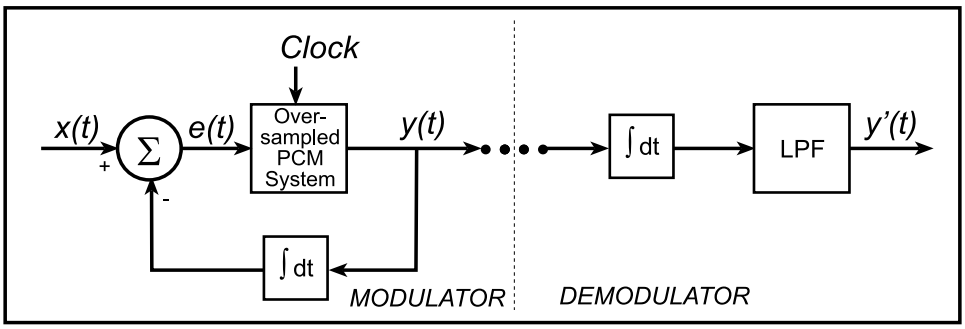

Figure 2.8: Block diagram of a Delta modulator and demodulator.

inversely proportional to the input frequency ; and the integration at the receiving end leads to accumulation errors during inevitable transmission disturbances [3]. Nevertheless, the simplicity of Delta modulation makes it very appealing compared to oversampled PCM.

Δ modulation is converted to $\Sigma - \Delta$ modulation by introducing an integrator in the signal path generating the error signal (Fig. 2.9). This particular configuration, with a single integrator in the loop, is referred to as first order modulator. Since the $\Sigma - \Delta$ ADCs were used initially as encoders in digital communication systems, the term "modulator" is often used to describe them. In this work, we will use the two terms (ADC and modulator) without any distinction.

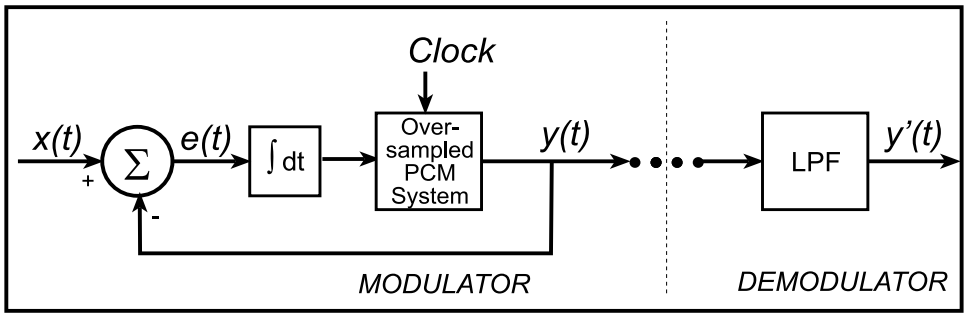

Figure 2.9: Block diagram of the initially proposed $\Sigma - \Delta$ modulator and demodulator.

2.4.1 Operation

A general description of the $\Sigma - \Delta$ modulator consists of a linear system in the forward loop path followed by a quantizer. The digital output is fed back and subtracted from the input before being processed by the linear system. A linearized model of the system is presented in Fig. 2.10.

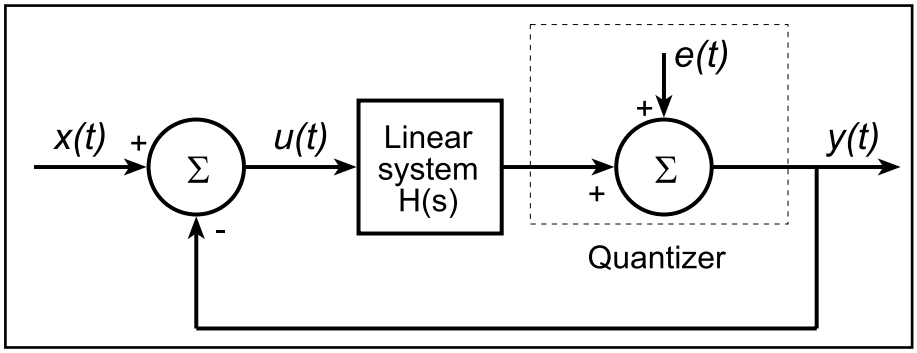

Figure 2.10: Linearized model of a general $\Sigma - \Delta$ modulator.

The Laplace transform $Y(s)$ of output $y(t)$ can be written in terms of Laplace transforms $X(s)$ and $E(s)$ of input $x(t)$ and quantization error $e(t)$, respectively, as

$$Y(s) = X(s).\frac{H(s)}{1+H(s)} + E(s).\frac{1}{1+H(s)} \tag{2.12}$$

The term $H(s)/(1+H(s))$ is the signal transfer function modulating the signal, while $1/(1+H(s))$ is the noise transfer function shaping the noise. If the linear system being used were an active low pass filter with a large passband gain, then the signal transfer function is almost unity in the signal passband, and rolls off as $H(s)$ in the stopband far away from the cutoff frequency. The noise transfer function, on the other hand, is approximately $1/H(s)$ in the filter passband, increasing to unity in the stopband. Fig. 2.11 shows this information graphically.

In general, a $\Sigma - \Delta$ modulator is characterized by 2 parameters:

- Order of the loop: The order of the filter used in the loop defines the order of the modulator loop. A first order modulator would thus have a single integrator in forward path ($H(s) = g_m/sC$). The roll-off

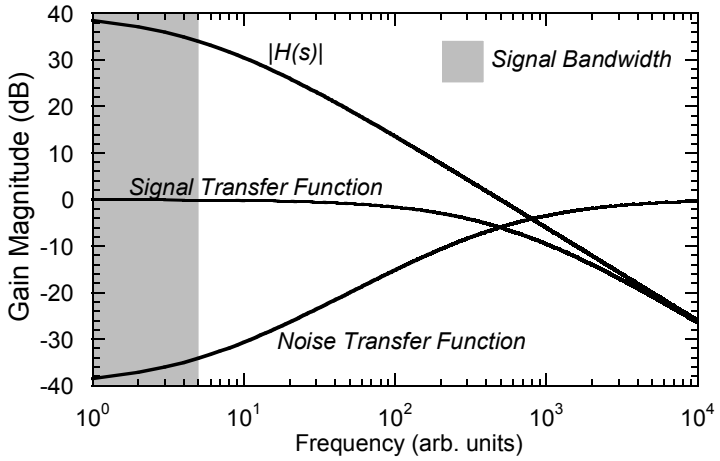

Figure 2.11: Qualitative behavior of signal and noise transfer functions for a first order low-pass filter in the forward loop of $\Sigma - \Delta$ modulator.

of the gain magnitude of the filter in the stopband is defined by the order of the filter, which in turn defines the gain magnitude of the signal and the noise transfer functions. Therefore, it is reasonable to expect higher rejection of quantization noise in the signal passband for higher order modulators. If the order of the loop is m, the modulator gains $(6m + 3)$ dB of *SNR* for every doubling of clock frequency. Equivalently, the modulator gains $(m + 0.5)$ effective number of bits (ENOB) in resolution for every octave increase in clock frequency.

- Oversampling Ratio (OSR): The oversampling ratio defines, for a given order of the loop, the extent of in-band noise rejection that can be achieved. This also defines the extent to which the rate of stopband-rolloff for anti-aliasing filter can be relaxed.

The limit to order of the loop comes from the stability constraints. A feedback loop with N integrators is unstable for N $>$ 3, due to the Bode constraints. A loop with N $>$ 3 can be stabilized by addition of (N-2) or (N-1) zeros in the loop, provided the zeros are at frequencies below the loop bandwidth.

Other technique used to improve stability is the use of a multibit quantizer. A multibit quantizer with a sufficiently large number of quantization

levels (e.g. 6 bits $\equiv$ 64 levels) has a well specified gain which doesn't vary significantly with the strength of the input to the quantizer. A loop with such a quantizer will have a well defined loop gain and hence loop bandwidth. For such systems, unconditional stability can be achieved. On the other hand, with a single bit quantizer, the quantizer gain and hence the loop bandwidth is not well specified. If the quantizer gain is defined as v_o/v_{in} (Fig. 2.12), then the quantizer gain is proportional to the inverse of the amplitude of the quantizer input. Consequently, the closed-loop poles and zeros for the system depend on the quantizer input. Thus, the loop gain and the loop bandwidth vary with the strength of the input to the quantizer. So, we can not reliably stabilize the loop with a zero just below the closed loop bandwidth, because we don't know the exact closed loop bandwidth. The stability analysis for high order (N $>$ 3) $\Sigma - \Delta$ modulators using single bit quantizers is more properly treated by non-linear system theory (beyond the scope of this thesis).

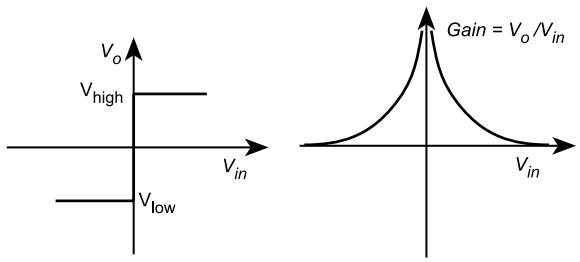

Figure 2.12: Input dependent gain for a one bit quantizer.

The *OSR* is limited primarily by the speed of technology available. With an increase in desired signal bandwidth ($>$ 100 MHz) and *SNR* ($\sim$ 90 dB), the required *OSR* is $\sim$ 128. The clock rates required to achieve these specifications is very high ($\sim$ 25 GHz). Such high clock rates can not be achieved currently in any device technology.

Loop filters may be implemented in either switched capacitor or continuous time techniques [24].

Continuous time filters use passive components (capacitors, inductors and resistors) in combination with operation amplifiers or transconductance stages. Fig. 2.13 shows a typical implementation of a filter in continuous time. The realization of such a circuit on an integrated circuit, while feasible in theory, may face severe obstacles in practice. These include

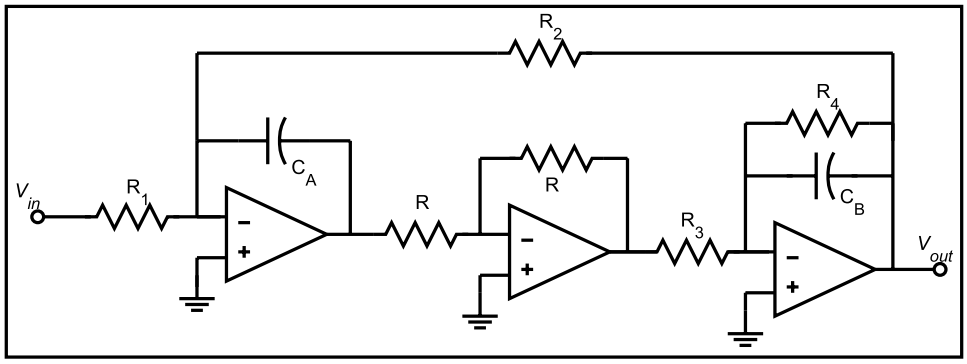

Figure 2.13: Realization of an active RC filter in continuous time.

- The required R and C values may be large. Therefore, large die area is needed.
- The circuit has a bandwidth $\leq$ (op-amp bandwidth/Q of the filter poles). The op-amp bandwidth in turn is substantially less than the transistor f_τ due to closed-loop stability requirements.

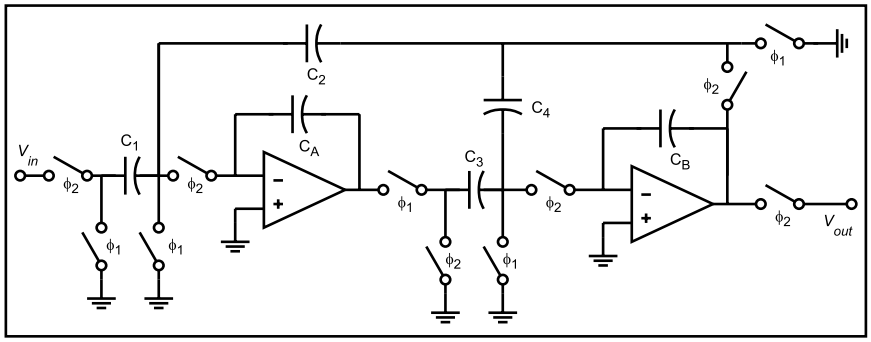

Figure 2.14: Block diagram of a second order switched capacitor filter section

Switched capacitor techniques are preferred in a technology where well matched capacitors can be obtained, but in which well matched resistors are not available. It can solve both the die-area and the resistor-matching issues. However, switched capacitor filters still suffer from the op-amp bandwidth limitations. An example of the switched capacitor filter implementation is shown in Fig. ??. The resistors, R, in a continuous time filter

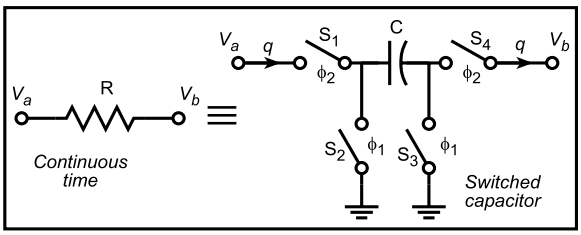

Figure 2.15: Transformation from Continuous time to switched capacitor implementation.

are replaced by a combination of a capacitor, C, and switches $S_1 - S_4$ (Fig. 2.15). The switches, operated by two phases (ϕ_1 and ϕ_2) of a clock signal, open and close periodically at a rate much faster than that of the variation of the node voltages V_a and V_b. The switches S_1 and S_4 close on phase ϕ_1 of clock while S_2 and S_3 close on the opposite phase ϕ_2 of clock. Initially, when S_2 and S_3 are closed, S_1 and S_4 are open and the capacitor C is discharged. When S_2 and S_3 open next, S_1 and S_4 close and C charges to the voltage $V_c = V_a - V_b$. This causes a charge $q = C.(V_a - V_b)$ to flow through the branch as shown in Fig. 2.15. This cycle of charging and discharging is repeated every T seconds, T being the period of the clock. Therefore, the average current through the branch is

$$i_{av} = q/T = \frac{C}{T}.(V_a - V_b) \tag{2.13}$$

If C and T are chosen such that $R = T/C$, then, $i_{av} = \frac{1}{R}.(V_a - V_b)$, which equals the average current flowing through the resistor in continuous time case. A switched capacitor filter can therefore be related to a continuous time RC-filter. Note that large equivalent resistor values can be obtained by using small capacitors. Large on-wafer time constants can thus be obtained with small valued capacitors.

2.4.2 Analysis example

Fig. ?? presents a discrete-time representation of a first order $\Sigma - \Delta$ modulator. The digital data stream would be followed by a digital decimator to obtain a digital representation at the Nyquist rate of the analog input signal. The digital output $y[n]$ is subtracted from the input $x[n]$ and the

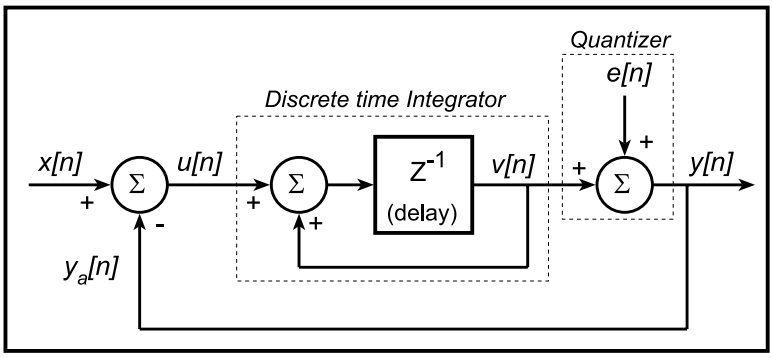

Figure 2.16: Discrete-time model of a first order $\Sigma - \Delta$ modulator

resulting error signal is filtered. In the case of a first order system, the loop filter is a discrete time integrator with transfer function $z^{-1}/(1-z^{-1})$. Recognizing that z^{-1} represents a pure delay in time of $e^{-j\omega T_s}$, we can write

$$\begin{aligned} y[i] &= v[i] + e[i] = (u[i-1] + v[i-1]) + e[i] \\ &= (x[i-1] - y[i-1] + v[i-1]) + e[i] \\ &= (x[i-1] - e[i-1]) + e[i] \\ &= x[i-1] + (e[i] - e[i-1]) \end{aligned}$$

Thus, the circuit differentiates the quantization error, making the modulator noise the first difference of quantization error, while leaving the signal unchanged except for a delay. The effective resolution of the $\Sigma - \Delta$ modulator can be determined by treating the error as white noise uncorrelated with the input signal. The spectral density of the modulation noise

$$n[i] = e[i] - e[i-1] \tag{2.14}$$

may then be expressed in terms of power spectral density $P_e(f) = {\sigma_e.}^2/f_s$ (section 2.2.1) of PCM quantizer as

$$P_n(f) = P_e(f).|(1 - e^{-j.2\pi.f/f_s})|^2 = 4.\frac{{\sigma_e.}^2}{f_s}.\sin^2\left(\frac{2\pi f}{2f_s}\right). \tag{2.15}$$

Total noise power in the signal band is

$$\sigma_n^2(f) = \int_{-f_B}^{f_B} P_n(f)df = \sigma_e^2.\frac{\pi^2}{3}\left(\frac{2f_B}{f_s}\right)^3. \tag{2.16}$$

The SNR can therefore be written as

$$SNR = 10\log_{10}(\sigma_x^2) - 10\log_{10}(\sigma_e^2) - 10\log_{10}\left(\frac{\pi^2}{3}\right) + 30\log_{10}\left(\frac{f_s}{2f_B}\right) \text{ (dB)}. \tag{2.17}$$

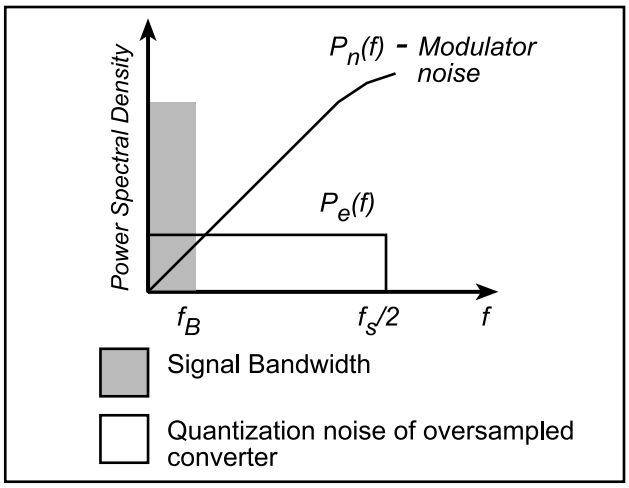

Figure 2.17: Qualitative spectral shaping of modulator noise in a $\Sigma - \Delta$ converter.

If the oversampling ratio $OSR = f_s/2f_B = 2^r$, then

$$SNR = 10\log_{10}(\sigma_x^2) - 10\log_{10}(\sigma_e^2) - 10\log_{10}\left(\frac{\pi^2}{3}\right) + 9.03r(\text{dB}). \tag{2.18}$$

For every doubling of oversampling ratio, or for every increment in the value of r, the SNR improves by 9 dB (equivalently, the resolution increases by 1.5 bits). The noise shaping of a $\Sigma - \Delta$ modulator is qualitatively shown in Fig. 2.17.

To understand the behavior of the digital output in time domain, we will again look at the first order modulator. The input to the integrator is the error signal $u[n]$ (or in continuous time $u(t)$). The integrated output $v[n]$ ($v(t)$) is quantized by the 1 bit quantizer to $y[n]$ ($y(t)$). Since there is an overall negative feedback, the integrator output must be finite at all time. Therefore, the average value of the input to the integrator, $\overline{u(t)}$, should be zero, indicating that the average value of output, $\overline{y(t)}$, is same as that of

the input $\overline{x(t)}$. Thus, the weighted average of the samples at the output tracks the input. This is shown graphically in Fig. 2.18 for a modulator using an *OSR* of 128. Thus, there are 256 output digital samples (logic **1** represented by 1V and logic **0** by -1V) in one cycle of the analog input. The zero crossing of the analog input is represented by the output frequently alternating between **1** and **0**. When the input is close to the maximum or the minimum, there is a correspondingly higher density of **1**'s or **0**'s, respectively.

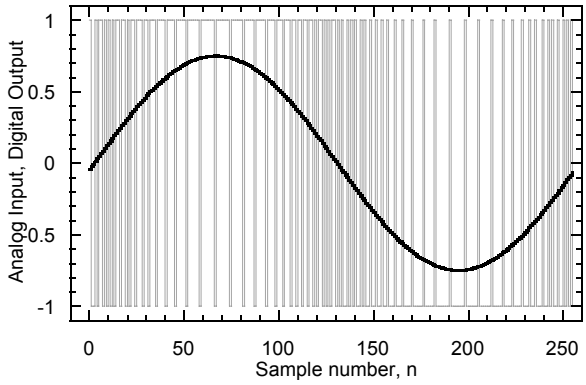

Figure 2.18: Time domain plot of analog input and corresponding digital output of an ideal first order $\Sigma - \Delta$ modulator of Fig. **??** with an *OSR* of 128.

2.4.3 $\Sigma - \Delta$ modulator using multibit quantizer

The use of multibit quantizer in $\Sigma - \Delta$ modulator can improve the stability of the non-linear feedback system. Moreover, the resolution of the $\Sigma - \Delta$ ADC also increases by the number of extra bits in the quantizer.

$$SNR_{\,multibit} = SNR_{\,single\text{-}bit} + (\text{extra \# of bits in the quantizer}) \quad (2.19)$$

The multibit quantizer in the forward path needs a multibit DAC in the feedback path. Because the multibit DAC is in the feedback path, the closed-loop $\Sigma - \Delta$ modulator resolution can be no better than the precision

of the levels in the feedback DAC. This is one of the main reasons for using a single bit quantizer in $\Sigma - \Delta$ modulators. To the extent that the two output levels of a single-bit DAC are time-invariant, the DAC introduces only constant gain and offset errors which do not reduce the *SNR* or *SFDR* of the ADC.

The multibit DAC in a $\Sigma - \Delta$ modulator must be linear to the desired number of closed-loop bits. In principle, this can be achieved if the steps between adjacent output levels of the DAC are very nearly equal in magnitude. Unfortunately, the matching precision required is of the same order as the precision desired of the overall data converter. For example, if a 3 bit quantizer and DAC are to be used in a $\Sigma - \Delta$ converter to get 16 effective number of bits at the output, the DAC will be required to have a 16 bit accuracy. Such precision is beyond the limits of present VLSI technology.

Several designers have investigated this issue and a widely accepted solution has been the use of noise-shaping DACs in the feedback path [26], [27], [28]. The noise-shaping DACs use digital signal processing techniques to redistribute the noise power due to the error resulting from DAC output-step-size mismatches. This redistribution increases the noise power outside of the passband of the $\Sigma - \Delta$ modulators. The associated hardware complexity is easily implemented in CMOS VLSI technology. It is a much more difficult task to translate these designs to compound semiconductor technologies, where the scales of integration are smaller by many orders of magnitude.

2.4.4 Bandpass $\Sigma - \Delta$ modulator

A straight forward modification of the baseband version of the $\Sigma - \Delta$ modulator is the bandpass modulator, where the low pass filter in the forward loop is replaced with a bandpass filter [5]. The large gain in the passband of the bandpass filter introduces nulls in the noise transfer function of the modulator which significantly increases the *SNR* for a signal in the passband. Regardless of the center, f_o, of the signal band, the smaller the signal band, f_B, is relative to the sampling frequency, f_s, the larger the attenuation of the in-band noise for a given filter order and the higher the resolution that can be achieved. The simplicity of implementation has made the bandpass modulator extremely attractive for use in the IF section of a radio receiver.

Fig. 2.19 shows the block diagram of a generic dual conversion receiver

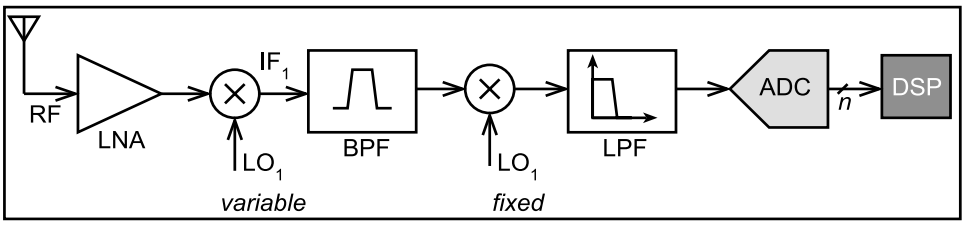

Figure 2.19: Schematic of a generic dual conversion radio receiver.

- a commonly used architecture. This architecture suffers from spurious frequency components resulting from the mixers. Rejecting these frequency components needs expensive and often complex off-chip filters. Filters are needed before mixers to reject the image components and to avoid mixer overload. Mixers have to be followed by high quality filters to reject undesired frequency component. So, it is difficult to realize the entire receiver as a single integrated circuit.

Methods of alleviating the problem include using novel IF stage design that can use on-chip filters. These filters heavily rely on achieving extremely high component matching [29]. Another solution is to eliminate the second mixer and directly digitize the IF signal output of the first mixer [30]. A bandpass $\Sigma - \Delta$ modulator accomplishes this objective. The processing of signals in digital domain is very reproducible under large temperature changes and tolerant to manufacturing variations in component values. Thus it is preferable over analog compensation mechanisms to counter the uncertainties introduced by analog components.

Having reviewed the basic issues in $\Sigma - \Delta$ modulator design, we will consider some of these issues in further detail in the next chapter. The design of a second-order continuous time modulator in transferred-substrate HBT technology will also be described.

Chapter 3

Design Methodology

In this chapter, we will consider in detail the procedure used in the design of a $\Sigma - \Delta$ ADC. The choice of technology is considered before deciding on the architecture.

The goal of this work is to achieve as high a clock frequency as allowed by the device technology. This would help the modulator handle higher signal bandwidths. Most $\Sigma - \Delta$ modulator reported in literature use CMOS based technology for implementation. The switched capacitor technique replaces resistors in a filter with capacitors and switches. It is valuable for technologies which can not implement high value resistors with high precision. A large value resistor R implemented as T/C_1 amounts to using a small capacitor value C_1. Moreover, a time constant RC in continuous time is equivalent to TC/C_1. Thus, the precision in R and C values translates to a precision in ratio of capacitors C/C_1, which is easier to achieve. Therefore, precise time constants are easy to achieve. As a result, most of the CMOS implementations of $\Sigma - \Delta$ modulator use switched capacitor architecture. In this work, the technology to be used for implementing the $\Sigma - \Delta$ modulator is the transferred-substrate HBT technology. The use of bipolar devices thus limits the design to continuous time architecture. Some of the compelling reasons are:

- switched capacitor modulators need a large number of switches. Bipolar technology does not offer good switches. So, it is very difficult to implement a switched capacitor modulator in bipolar technology.

- The transferred-substrate HBT technology has a provision for nichrome

thin-film resistors which allows implementation of large value resistors.

- The bandwidths we seek in our design are large. Therefore, large RC time constants are not required on-wafer.

There are numerous advantages associated with design in continuous time architecture [31], [24], [23], [32]:

1. A typical switched capacitor discrete time $\Sigma-\Delta$ ADC has a maximum clock rate limited by the operational amplifier (op-amp) unity-gain bandwidth. Furthermore, for a given unity gain frequency of the op-amp, f_u, the switches in a switched capacitor filter have to be clocked at a sufficiently low rate ($\sim f_u/5$) to ensure that the node voltages have enough time to settle (chapter 7 of [24]). As will be seen in section 3.1.2, the unity gain bandwidth of op-amps is limited by stability issues to a small fraction of the device f_τ. The continuous time modulator can use g_m stages which can have significantly higher bandwidth.

2. In a switched capacitor modulator, switching of large signals induces large glitches on the op-amp nodes that are intended to remain at virtual ground. This is not the case in continuous time case where the feed-through effects are minimal.

3. Although oversampling alleviates the requirements on the roll-off properties of anti-aliasing filter required at the input, it is still needed in the case of switched capacitor modulators. Candy [33] showed that there is an implicit anti-aliasing property associated with a low-pass continuous time modulator. This is because the signal is sampled at the quantizer rather than at the input to the modulator. Thus, the a low-pass continuous time modulator does not need a anti-aliasing filter at its front end. This concept has been studied in great mathematical detail and rigor by Cherry [31] and Shoaei [23].

The other issues in a $\Sigma - \Delta$ modulator design are briefly considered below:

- **Modulator order**: The SNR of an m^{th} order $\Sigma - \Delta$ modulator improves by (6m+3) dB per octave increase in OSR. Thus a high-order

modulator is desirable because of the huge increase in the converter performance obtained from a doubling of the *OSR* . At the same time, there are stability issues associated with a high-order loop (section 2.4.1) which makes only a second order modulator relevant for the design using a single-bit quantizer. Our design requires a high *SNR* over a large signal bandwidth. To keep the risks in fabrication low, we implement the modulator in a second order continuous time architecture. This gives us the option of achieving a stable operation with the least design complexity. A second order loop should give us an improvement of 15 dB in *SNR* for every doubling of the clock frequency.

- **Oversampling ratio**: The design of the $\Sigma - \Delta$ modulator using a continuous time architecture can allow us to clock the modulator as fast as allowed by the device technology. This is possible if the integrators use g_m stages with large bandwidths (rather than operational amplifiers which have their second and third open-loop poles well below the device f_τ). So far, the highest clock frequencies reported for $\Sigma - \Delta$ modulators have been 5 GHz in the InGaP/InGaAs HEMT technology [35] and 3.2 GHz in the InP HBT [36], both in continuous time architecture. Listed below are some of the factors that limit the clock frequency.

  - Excess delay in the loop.
  - Metastability and dynamic hysteresis in the quantizer.

  The effect of these factors on the modulator performance will be studied later (section 3.2). We decided to use a clock frequency of 20 GHz for our modulator. From the point of view of achieving this high clock rate, transferred substrate HBT technology is very appealing. Extremely fast transistors have been demonstrated in the transferred substrate HBT technology. Devices with f_τ and f_{max} higher than 200 GHz are routinely achieved.

- **Quantizer resolution**: At the expense of an increase in complexity, the single-bit quantizer in the modulators could be replaced with a multi-bit quantizer. As discussed in section 2.4.3, this has the advantage of improving the *SNR* of the modulator. Moreover, multibit

quantizers tend to make higher order modulators more stable. A multibit quantizer with its multiple output levels has a gain which is better defined compared to a single-bit quantizer which has only two levels (Fig. 2.12). Therefore, the input dependence of quantizer gain is reduced. As a result, the stability of the modulator does not depend on modulator input strength very strongly. The white-noise model describes the quantization noise behavior more accurately now; hence the tonal behavior in the modulator output is less likely. Non-idealities of the quantizer are suppressed by the loop gain but the DAC errors are not suppressed. To correct for these errors the error-randomization techniques such as *dynamic element matching* ([28], section 2.4.3) have to be implemented. The circuit implementation of such solutions may need up to 10,000 transistor clocked at the sample rate.

Keeping in mind the complexity of the implementation, we choose a single-bit internal quantizer for use in the modulator. A latched comparator is usually used as a single-bit quantizer in a $\Sigma - \Delta$ modulator. This work uses a master-slave flip-flop for this purpose.

These design aspects have been summarized in Table 3.1. Fig. 3.1 depicts a standard second order continuous time $\Sigma - \Delta$ modulator. The design of various circuit blocks and their effect on the circuit performance will be discussed in the following section.

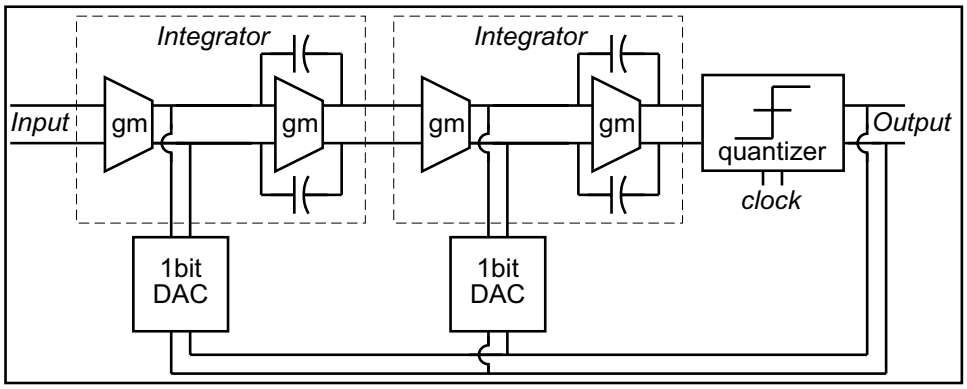

Figure 3.1: A block diagram of second-order continuous time $\Sigma - \Delta$ modulator.

Table 3.1: Advantages and disadvantages of modulator architectures [34].

Design parameters	Advantages	Disadvantages
Low order single loop single bit	• Stability is guaranteed. • Loop filter is easy to design. • Circuit implementation is easy.	• High *SNR* requires very high *OSR* . • More prone to idling tones (dithering helps).
High order single loop single bit	• High *SNR* can be achieved for modest *OSR* . • Less prone to idling tones. • Circuit implementation is still fairly easy.	• Loop filter design is difficult. • Stability is signal dependent. • Maximum input range needs to be restricted for ensuring stability.
Multibit quantizer	• High *SNR* can be achieved for fairly low *OSR* . • Stability is easier to achieve for higher order loops.	• Imperfect matching of levels in the feedback DAC results in harmonic errors translating to baseband. Techniques like dynamic element matching needed which result of transistor count of the order of 10,000. • Circuit design and implementation is more complex.

3.1 Loop design and Simulation issues

The design issues include the choice of a transfer function to be implemented by the loop-filter, design of the quantizer and the feedback DAC.

3.1.1 Loop design

The most common design procedure for $\Sigma - \Delta$ modulators is to start with a discrete time transfer function for the loop filter to be designed to obtain the best $\Sigma - \Delta$ modulator performance. This can be transformed to the continuous time domain to obtain a continuous time design. Maximum baseband attenuation of quantization noise in a second order design requires us to choose the noise transfer function in discrete time to be

$$NTF(z) = (1 - z^{-1})^2 \tag{3.1}$$

This leads to a choice of loop filter transfer function to be

$$H(z) = \frac{2z - 1}{(z - 1)^2} \tag{3.2}$$

The equivalent continuous time transfer function for the discrete time loop filter is given by [33]

$$H(s) = \frac{1 + 1.5sT_s}{s^2T_s^2} \tag{3.3}$$

where $T_s = 1/f_s$ represents the sampling time. Note that z^{-1} corresponds to a delay in time domain T_s (e^{-sT_s} in frequency domain), but $z^{-1} \neq e^{-sT_s}$. The equivalence (of Eq. 3.3) assumes that the feedback employs a non-return-to-zero (NRZ) DAC. This equivalence is established on the basis of the equivalence of the impulse responses of the two filters in time domain. *This would guarantee the output of the two filters to be the same at the sampling instants for the same inputs and the resulting discrete time and continuous time modulators will be equivalent.* The necessary math has been discussed in [31].

For a clock frequency of 20 GHz, the sampling period is 50 ps. Therefore, we need to implement the transfer function:

$$H(s) = \frac{1 + 75^{-12}s}{(2.5 \times 10^{-21}s^2)} = 3 \times 10^{10}\left(\frac{s + 1.3\overline{3} \times 10^{10}}{s^2}\right) \tag{3.4}$$

This transfer function describes two integrators with unity gain frequency of $\omega_{u,1}.\omega_{u,2} = 1/T_s^2 = 4 \times 10^{20}$ rad^2/s^2 (or, $f_{u,1}.f_{u,2} = 1.01 \times 10^{19}$ Hz^2) and a zero at $\omega_z = 1/(1.5T_s) = 1.3\overline{3} \times 10^{10}$ rad/s (or, $f_z = 2.12 \times 10^9$ Hz). The unity gain frequency is a gain factor in the loop which will decide the maximum voltage swings at different nodes in the $\Sigma - \Delta$ modulator. This factor will be adjusted to ensure that the integrators and quantizers do not overload. It has to be simultaneously ensured that this factor is sufficiently large for the quantizer metastability related errors to be minimum.

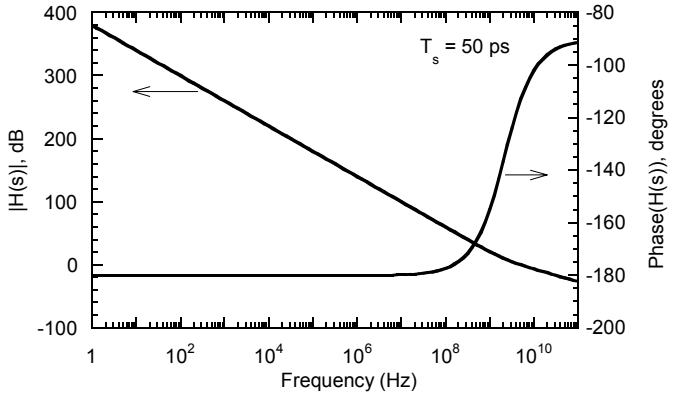

Figure 3.2: Magnitude and phase response of the ideal filter in Eq. 3.4.

High speed $\Sigma-\Delta$ modulators generally adopt a fully differential architecture. The advantages of such an architecture include significant suppression of even-harmonic distortion, a 6-dB increase in dynamic range and reduction in extraneous unwanted signals such as power supply noise and clock switching noise.

3.1.2 Choice of filter architecture

Before proceeding with the analysis of the ADC performance with a nonlinear simulator, we can make some qualitative statements about the requirements from the loop-filter.

1. The filter should have as high a dc gain as possible. The ideal filter transfer function (Eq. 3.4) requires a double pole at dc (Fig. 3.2)

requiring an infinite DC gain. With a bipolar transistor technology without pnp devices, obtaining a high DC gain is challenging.

2. Any excess delay in the loop modifies the loop transfer function from the desired value. An integrator ideally has only one pole, at DC. But, the circuit implementation results in a second pole due to parasitics inherent in the device as well as the layout. The second pole contributes some excess phase at frequencies much smaller than the location of second pole. This excess phase translates in excess loop delay. For the best ADC performance, the integrator should have $(g_m/j\omega C)$ frequency response over as high a bandwidth as possible.

Our design needs to consider architectures that minimize the impact of these issues and if possible, predict the extent of performance loss and compensate for it.

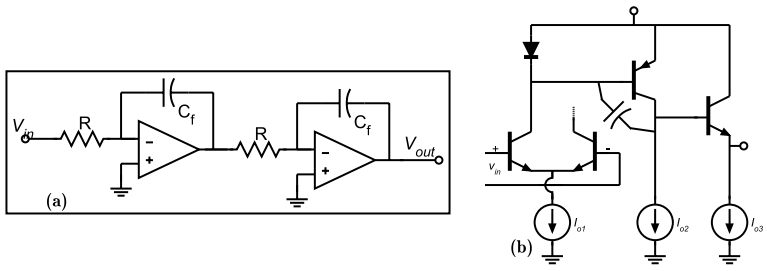

Figure 3.3: A continuous time integrator using resistors, capacitors and op-amps: (a) Block diagram, (b) A simple schematic of a bipolar op-amp.

It is possible to design an integrator using op-amps. Fig. 3.3 depicts one such circuit. The op-amp uses multi-stage transistor amplification. If the IC technology has devices with poor transconductance, and allows fabrication of precise resistor values along with good pnp transistors, this might be an attractive option. The limitation of this technique is in the low unity-gain frequency, f_u, that can be achieved for the op-amp. The op-amp will have 2^{nd} and 3^{rd} open-loop poles at frequencies somewhat below the transistor f_τ. So, loop stability requirements force the closed-loop bandwidth of the op-amp to $f_u \sim f_\tau/10$ or lower. An active filter using an op-amp is known to perform poorly for $f > f_u/5$. Thus, the usable frequency range of the integrator is limited to $f \ll f_\tau$.

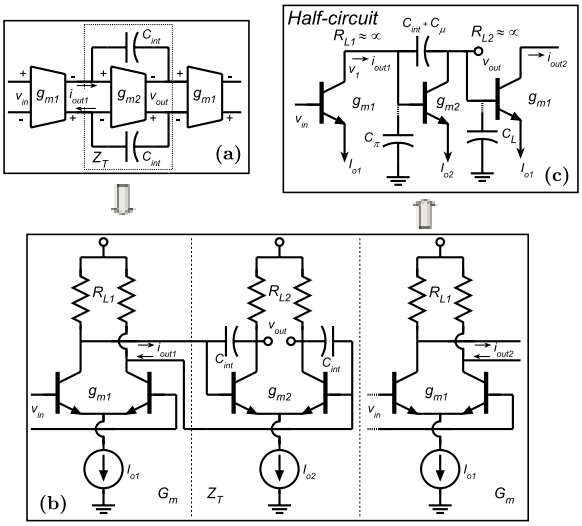

Figure 3.4: Standard implementation of the transconductance-transimpedance ($g_m - Z_T$) filter : (a) Block diagram, (b) Implementation using simple bipolar differential pair, (c) Equivalent half-circuit for analysis.

Another choice in integrator design using bipolar devices is the use of transconductance (g_m) stages as a building block. The integrators built using these devices can be usually broken into independent blocks: a transconductance stage followed by a transimpedance (Z_T) stage (Fig. 3.4(a)). A simple circuit implementation using bipolar differential pairs is shown in (Fig. 3.4(b)). For simplicity of analysis, an equivalent half-circuit is shown in part (c) of the same figure. The transistor forming the transimpedance stage has at the input a capacitance, C_π (the transistor's diffusion capacitance), from base to ground, and a load capacitance, C_L, formed by the C_π of the loading device. The base-collector capacitance, C_μ, of the device appears in parallel with the integration capacitance, C_{int}. Assuming resistive loads, $R_{L1}, R_{L2} \sim \infty$, ignoring the base resistance R_{bb} and writing $C_t = C_{int} + C_\mu$, a nodal analysis of the half-circuit yields

$$\begin{bmatrix} i_{out1}(s) \\ 0 \end{bmatrix} = \begin{bmatrix} s(C_\pi + C_f) & -sC_f \\ g_{m2} - sC_f & s(C_f + C_L) \end{bmatrix} \begin{bmatrix} v_1(s) \\ v_{out}(s) \end{bmatrix} \tag{3.5}$$

From this equation, the transimpedance can be obtained as

$$\frac{v_{out}(s)}{i_{out1}(s)} = \frac{1}{sC_f}\left(1 - \frac{sC_f}{g_{m2}}\right)\left(\frac{1}{1 + s(C_fC_\pi + C_fC_L + C_\pi C_L)/(g_{m2}C_f)}\right) \tag{3.6}$$

The overall integrator transfer function will thus have a pole at DC, a zero in the right half of s-plane at $s = g_{m2}/C_f$ and a second pole at $s = -g_{m2}C_f/(C_fC_\pi + C_fC_L + C_\pi C_L)$. In a typical circuit implementation, $C_f \gg C_\pi, C_L$, which gives the second pole location at $\sim g_{m2}/2C_\pi \sim f_\tau/2$. When R_{bb} is considered, this parasitic pole frequency will be reduced.

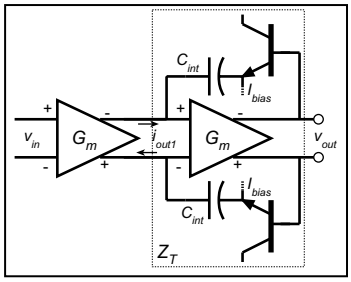

Figure 3.5: Unilateralizing the transimpedance stage in the integrator.

Use of a technology allowing only npn transistors limits the DC gain that can be achieved in the integrators. The circuit in Fig. 3.4(b) has pull-up resistors R_{L1} and R_{L2} loading each transconductance stage. Thus, this configuration achieves a high DC gain $= g_{m1}g_{m2}R_{L1}R_{L2}$. These filters suffer from lower feasible bandwidth due to the zero and the pole in the transfer function which could adversely affect the stability of the $\Sigma - \Delta$ modulator loop. The second pole contributes excess phase at higher frequencies resulting in excess delay in the loop. Several solutions have been proposed to offset the effect of right half plane zero. They include:

- Canceling the zero by placing a resistor ($R_z = 1/g_{m2}$) in series with the integrating capacitor.
- Unilateralizing the system by placing a emitter follower in the feedback path (Fig. 3.5). The emitter follower needs to be biased at $I_{bias} = g_{m2}.V_t$, where V_t is the thermal voltage.

With the zero canceled, the integrator bandwidth can be $\sim f_\tau/2$. Thus, an integrator designed using transconductance elements instead of op-amps

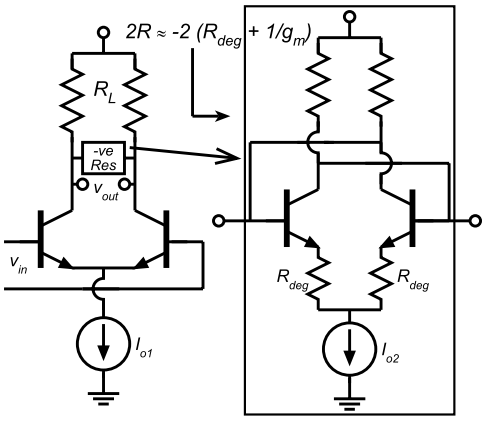

Figure 3.6: Implementation of a negative resistance element to boost the dc gain. For maximum gain, one picks $R = R_L$.

can obtain higher bandwidths. The issue of achieving a high dc gain is typically addressed by circuit design techniques such as use of a bootstrapped [36] or a negative resistance [37],[38] load. Fig. 3.6 shows a typical implementation of negative resistance load in bipolar technology. The negative resistance load helps achieve high differential gains with the use of relatively small pull-up resistors as well as low power supply voltages. However, the following issues make this technique undesirable from the point of view of implementation in transferred substrate HBT technology:

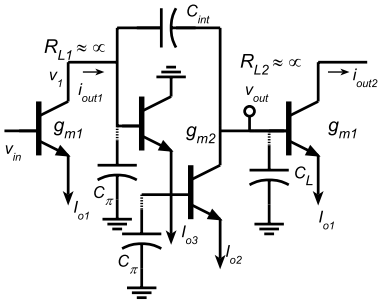

Figure 3.7: The equivalent half circuit for a g_m-Z_T integrator using darlington pairs in the g_m stages.

- The complexity of the circuit increases the transistor count in the high frequency path resulting in higher order poles due to the device

as well as the layout parasitics. These higher order poles result in an excess phase delay in the integrator, limiting the maximum clock rate possible.

- These techniques also add extra transistors. Since we are fabricating this circuit in a university process, we would like to keep the device count in the circuit low for a better circuit yield.

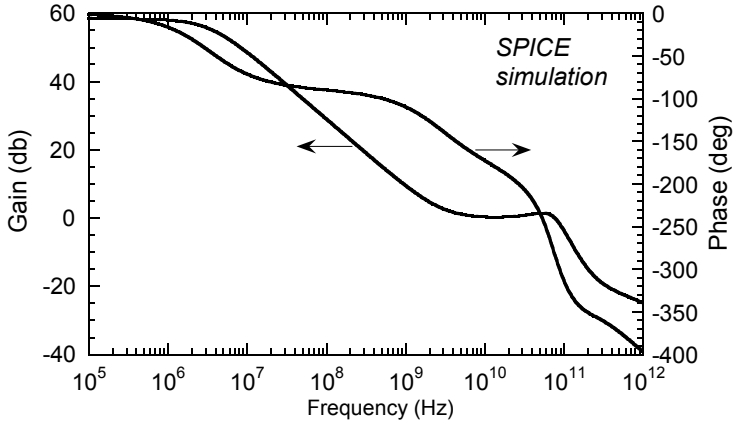

Figure 3.8: Response of the g_m-Z_T integrator employing darlington pairs simulated using SPICE.

To be able to use an integrator architecture such as shown in Fig. 3.4, we need to use darlington pairs instead of simple transistors for the differential pair. This is required to ensure proper DC levels for transistor operation as well as to provide higher input impedance for each stage. The analysis to obtain the transfer function for such a system is more involved. The equivalent half-circuit for such a circuit is shown in Fig. 3.7. Without going into the mathematical details, we can observe that the number of significant poles in this system is larger because the diffusion capacitances of transistors in the signal path can no longer be lumped together at one node. Such a design is likely to have a usable bandwidth further limited by the transistor parasitics. The SPICE simulation of the response of this circuit (Fig. 3.8) confirms the fact that this integrator has a lower usable bandwidth. The integrator response show a $g_m/j\omega C$ behavior from $\sim$ 3.2 MHz to $\sim$ 2.6 GHz. The right-half plane feedforward zero ($g_m/2\pi C_{int}$) seems to be the

primary bandwidth limiting factor. The maximum frequency to which this can be used is thus $\sim f_\tau/10$ for the device models used here.

Our design needs an integrator with the highest bandwidth allowed by the technology. Furthermore, we desire to keep the transistor count to the minimum. Any of the circuit configurations discussed so far will need a large number of transistors for implementing the integrator. Moreover, each transconductance stage needs a common-mode feedback loop (describe later in this section) which further increases the circuit complexity.

A simple integrator design was therefore selected for our design. In this work, the integrators are implemented as a transconductance element loaded by a capacitor to ground (Fig. 3.9). The loading effect of next transconductance stage is lumped with the integrating capacitor (Fig. 3.9(b)) thus allowing higher integrator bandwidth compared to the circuit configurations discussed above. To achieve a high dc gain, a very high value of pull-up resistor is used along with a large power supply voltage. The large output impedance at DC necessitates the use of a common-mode feedback circuit. The common-mode feedback (CMFB) circuit sets the common mode voltage of the output (and the integrator DC bias) at a desired value. The bandwidth of the CMFB loop should be limited to much less than the signal frequencies. This ensures that the CMFB loop does not interfere with the operation of the $\Sigma - \Delta$ modulator. The low breakdown voltage of InGaAs collector HBTs ($BV_{CEO} \approx 1.4$V), makes the transistors very fragile and sensitive to varying V_{ce}, and makes CMFB circuit particularly important for the successful operation of $\Sigma - \Delta$ modulator. The design presented here uses an off-chip operational amplifier integrator for common-mode feedback.

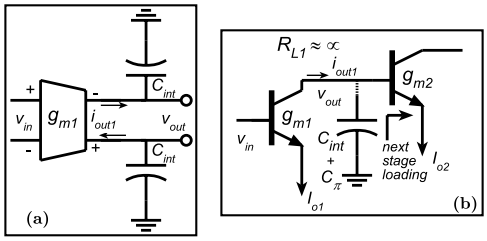

Figure 3.9: (a)The block diagram of a simple g_m-C integrator to be implemented, (b) The equivalent half circuit.

3.1.3 Simulation techniques

We analyzed the performance of the $\Sigma - \Delta$ modulator loop using MATLAB, a nonlinear simulator. A simulator such as SPICE uses an accurate description of the transistors to analyze the behavior of a circuit in time or frequency domain. In MATLAB, various $\Sigma - \Delta$ modulator components can be isolated into independent blocks with a behavioral model. Thus, while the performance indicated by MATLAB simulations do not reflect all the circuit imperfections, the simulations are significantly faster and they provide an approximation to the true $\Sigma - \Delta$ modulator response. The SIMULINK tool in MATLAB allows a graphical description of the components of the loop. The integrators can be implemented as linear blocks with the s-domain transfer function description. Slew rate limits in g_m elements as well as the maximum voltage swings at the integrator output can be modeled. The quantizer is implemented by a level-triggered D flip-flop. The delay elements suitably mimic the effect of excess component delays as well as the transmission-line wiring delays in the layout. The output digital data is analyzed in the frequency domain (by performing an FFT) to evaluate the modulator performance. The parameters for various blocks, e.g. the unity gain frequency of the integrators, transconductance of the integrators, feedback current in the DAC, location of the zero in the loop transfer function, were varied to obtain the best modulator performance.

Following the system analysis in MATLAB, the next step is the design of each circuit component in the $\Sigma - \Delta$ modulator system. This is done using the circuit simulators HP Series-IV and HP ADS. For the early phases of the project, computing difficulties prevented us from simulating the entire loop performance using a SPICE based transient simulator. The principal objective of this work was to explore and demonstrate the feasibility of a large circuit in this technology. So, the problems with transient simulation were ignored. Instead, the individual circuit blocks were designed to obtain the parameters defined by the MATLAB simulations.

3.1.4 Quantizer and feedback DAC design : Issues and suggested solutions

The MATLAB simulations of the continuous time $\Sigma - \Delta$ modulator assumed an ideal quantizer. The input is compared with a reference and an output is

generated as a logic level. The quantizer can be implemented by a very high gain amplifier. This is accomplished by using a positive feed-back circuit which is enabled by a clock [4], [39].

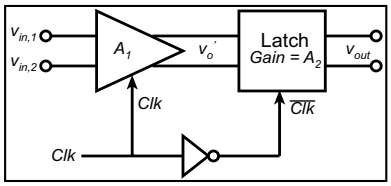

Figure 3.10: Typical latched comparator architecture.

Fig. 3.10 illustrates a typical comparator architecture often utilized in mixed-signal applications. The main components here are the preamplifier (gain = A_1) and the latch. The overall circuit has two modes of operation: tracking and latching. In the tracking mode, the a clock signal (Clk) enables the preamplifier to track and amplify the input difference. Its output is given by:

$$v_o' = A_1.(v_{in,1} - v_{in,2}) \tag{3.7}$$

During this time, the latch is disabled. In the latching mode, the preamplifier is disabled and the latch is enabled with $\overline{Clk}$ so that the changes in input no longer affect the output. At the instant the latch is enabled, the output of the preamplifier is regeneratively amplified to a logic level produced at v_{out}. Thus, this architecture defines a sampling instant at which the polarity of the difference in inputs is stored. The preamplifier has a finite bandwidth. Therefore, there is a time constant (τ_{track}) which results in a delay with which changes in input can be tracked. Similarly, the process of regeneration has an associated time constant (τ_{reg}).

Fig. 3.11 shows a latch comprising of two identical single-pole inverting amplifiers each with a small signal gain of $-A_o$ ($A_o > 0$) and a characteristic time constant of τ_o. This circuit can be described with the differential equations:

$$\begin{aligned} \tau_o \frac{dv_x}{dt} + v_x &= -A_o v_y \\ \tau_o \frac{dv_y}{dt} + v_y &= -A_o v_x \end{aligned}$$

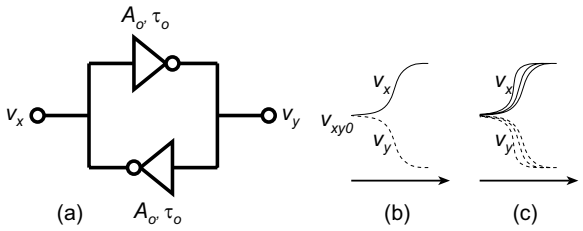

Figure 3.11: (a) A latch modeled as two back-to-back inverting amplifiers; (b) Time response of the outputs of the latch; (c) Time response for different initial differences v_{xy0} at the input.

From which we obtain

$$\tau_o \frac{d(v_x - v_y)}{dt} = -(1 - A_o)(v_x - v_y). \tag{3.8}$$

Given the initial conditions, $(v_x - v_y)|_{t=0} = v_{xy0}$,

$$v_x - v_y = v_{xy0} \exp((A_o - 1)t/\tau_o). \tag{3.9}$$

Typically, $A_o \gg 1$, which results in an exponentially increasing differential voltage at the output of the latch. The resulting regeneration time constant is $\tau_{reg} = \tau_o/(A_o - 1)$. If v_{xy1} is the logic level to be reached by $(v_x - v_y)$, then the corresponding regeneration time is

$$T_{reg} = \frac{\tau_o}{(A_o - 1)} \ln\left(\frac{v_{xy1}}{v_{xy0}}\right) \tag{3.10}$$

As show above, the time taken for the output to regenerate to the logic levels has a logarithmic dependence on the initial input voltage difference, v_{xy0}. Thus, the regeneration time is particularly sensitive to this input voltage difference when this difference is very small. The circuit implementation of a quantizer suffers from some non-idealities related to finite non-zero time for response to changes in inputs.

An example of a latched comparator using current mode logic (CML) is shown in Fig. 3.12. The tracking stage is enabled when Clock (C) is high. The input differential pair amplifies the input difference $(v_{i1} - v_{i2})$ to generate output voltages v_{o1} and v_{o2}. The equivalent circuit showing the dominant capacitances determining the tracking time-constant is shown

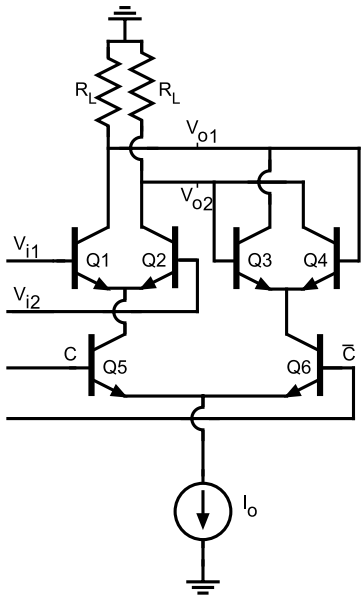

Figure 3.12: A latched comparator implemented in current mode logic.

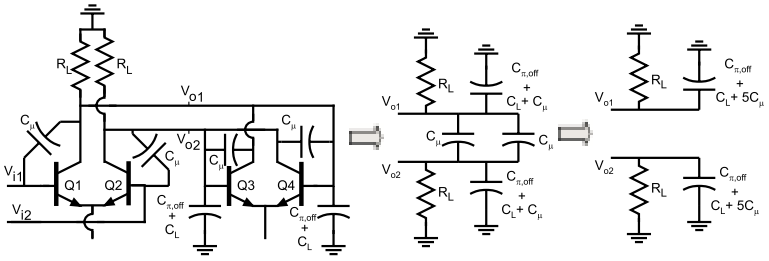

Figure 3.13: Equivalent circuit of the CML latch during tracking along with the half circuit equivalent for calculating the tracking time constant.

in Fig. 3.13. Ignoring the transistor base resistance and assuming that the input is driven from a low impedance node (as the case is in a $\Sigma - \Delta$ modulator), the tracking stage has the dominant pole in the form of $\tau_{track} = R_L.(5C_\mu + C_{\pi,off} + C_L)$. The capacitance $C_{\pi,off}$ comes from the base node of a transistor in the cross-coupled latch which is off during the tracking stage, while C_μ is the collector base capacitance of the transistor. C_L is the capacitance due to loading from the next stage. Let's assume a design with bias current $I_o = 6$ mA, load resistance, $R_L = 50\Omega$, $C_{\pi,off} = 40$ fF, $C_\mu = 10$ fF and $C_L = 100$ fF. This leads to a tracking time constant of 9.5 ps.

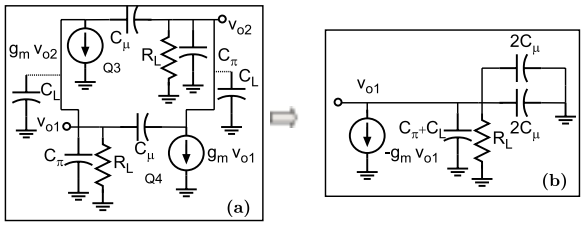

Figure 3.14: (a)Equivalent circuit of the CML latch during regeneration, (b) half circuit.

The latching stage is enabled when the clock is low ($\overline{C}$ is high). Fig. 3.14(a) shows an approximate small-signal equivalent circuit during regeneration. The cross-coupled pair regeneratively amplifies the difference $v_{o1} - v_{o2}$ to the appropriate logic levels. The equivalent half circuit obtained by taking into account the symmetry in the system is shown in Fig. 3.14(b). From this figure, the time constant associated with the process of regeneration can be written as

$$\tau_{reg} = -(-\frac{1}{g_m}||R_L)(4C_\mu + C_\pi + C_L) = \frac{(4C_\mu + C_\pi)}{g_m}\left(\frac{g_m R_L}{g_m R_L - 1}\right) \quad (3.11)$$

For $I_o = 6$ mA, $g_m = (I_o/2)(q/kT) = 120$ mS, and $C_\pi \sim 200$ fF, $\tau_{reg} \approx 3.4ps$. Thus, for the same drive current the regeneration takes place with a smaller time-constant compared to the process of tracking.

We can estimate the limits on clock frequency for correct operation of the CML latch. If the input is high at logic level **1** (300 mV) for a sufficiently long time before it changes to a small negative voltage, $V_{in} < kT/q$, the

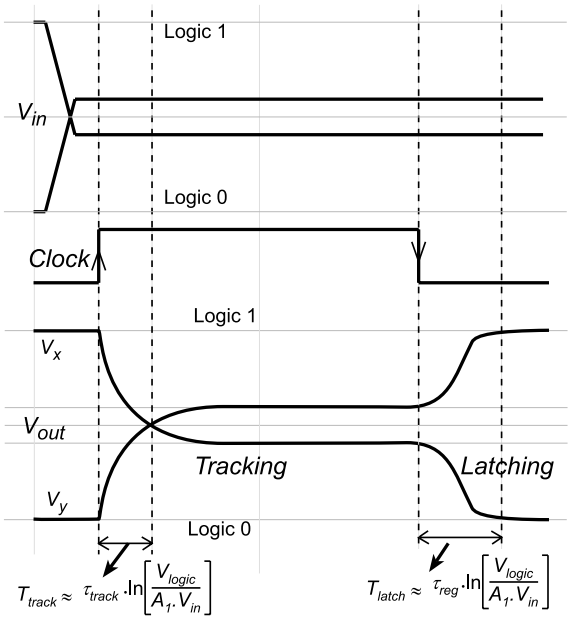

Figure 3.15: Time variation of the voltage in the comparator during tracking and latching.

preamplifier output changes in an exponential fashion. It has to amplify the input to $A_1.V_{in}$.

$$V_{out}(t) = V_{out,final} + (V_{out,initial} - V_{out,final}) \exp(-t/\tau_{track}) \tag{3.12}$$

Thus, it takes a time

$$T_{track} = -\tau_{track} \ln \left(\frac{V_{out,final}}{(V_{out,final} - V_{out,initial})} \right) \tag{3.13}$$

for the output to reach zero voltage before it starts reading the sign of the input correctly.

The waveform for the outputs of the tracking and regeneration circuits corresponding to a very small voltage at the input is shown graphically in Fig. 3.15. Consider an input changing from +300 mV to -10 mV. The output has an initial value of $V_{out,initial} = +300$ mV. With the preamplifier gain of $A_1 = g_m R_L = 6$, the output has to reach a final value of $V_{out,final} = (A_1)(-10\text{mV}) = -60$ mV. Then, $T_{track} = -7.5ps \times \ln(60/360) = 13.4$ ps. If the preamplifier is ON for less than 13.4 ps, the output of the tracking circuit is erroneous. This error is referred to as overdrive-recovery error. Since the input strength has to be increased before the preamplifier detects the change, it manifests in high speed circuit circuits as dynamic hysteresis error.

Consider now, the case when the input has been read correctly by the preamplifier and the output has reached -60 mV (asymptotically) before the regeneration is enabled. The regeneration circuit will receive a $V_{out,initial} = -60mV$ and it needs to amplify this voltage to $V_{out,final} = -300mV$. the output of the regeneration circuit will again be an exponential with the time dependence described by

$$V_{out}(t) = V_{out,initial} \exp(t/\tau_{reg}) \tag{3.14}$$

Thus, it takes a time

$$T_{reg} = \tau_{reg} \ln \left(\frac{V_{out,final}}{V_{out,initial}} \right) \tag{3.15}$$

for the output voltage to reach its final value.

In this example, $T_{reg} = 3.4ps \times \ln(300/60) = 5.5$ ps. Therefore, the limitation to the comparator speed comes from preamplifier time constant.

In a more general circuit, depending on the value of the time-constants of the preamplifier and the latch, the logic levels, the input applied and the clock frequency, the comparator could suffer from one or both the problems listed below:

- **Dynamic hysteresis**: If the time-constant, τ_{track} (Eq. 3.13) is too large, the preamplifier will need a long time to track the changes in input correctly. If the clock frequency is too high ($T_{clock} < 2.T_{track}$), the preamplifier is disabled before the input is read correctly. This results in erroneous voltage being input to the regeneration circuit leading to an incorrect comparator decision. This error is called dynamic hysteresis.

- **Metastability**: Let's assume that the tracking time constant is sufficiently small such that the input is read correctly by the preamplifier, i.e. there are no hysteresis errors. The latch needs a time T_{reg} (Eq. 3.15) to regenerate this amplified input to a logic level. For a given logic level, the time taken to regenerate the input to logic levels depends on the initial voltage at the input to the regeneration circuit (Eq. 3.15). If the clock frequency is too high ($T_{clock} < 2.T_{reg}$), the latch is disabled before the output reaches a logic level. The deviation of the output voltage from the logic levels is described as metastability error.

For a proper operation of the comparator, we need to allow enough time for overdrive recovery as well as regeneration.

In a $\Sigma-\Delta$ modulator, the output of the quantizer drives the DAC which generates a current pulse proportional to the quantizer output. Since the input to the quantizer could be arbitrarily small, the output of the quantizer may suffer from the metastability errors. The DAC needs to interpret all positive outputs as being equal to the logic **1** and all negative outputs to be logic **0**. Any non-idealities in the shape of DAC pulses results in feedback of incorrect amount of charge into the integration capacitor. This adversely affects the performance of the continuous time $\Sigma - \Delta$ modulator.

The standard implementation of a one bit DAC is in the form of a current steered differential pair (Fig. 3.36). A non-return-to-zero (NRZ) DAC outputs a current pulse of width equal to the input data bit. The total charge delivered by the DAC into the integrator equals the area under

the current pulse waveform generated by the DAC. Quantizer metastability results in the output of the comparator reaching the final voltage (logic level) in different times, depending on the strength of the quantizer input. This causes timing modulation of the edge of DAC output pulse. This is shown graphically in Fig. 3.16.

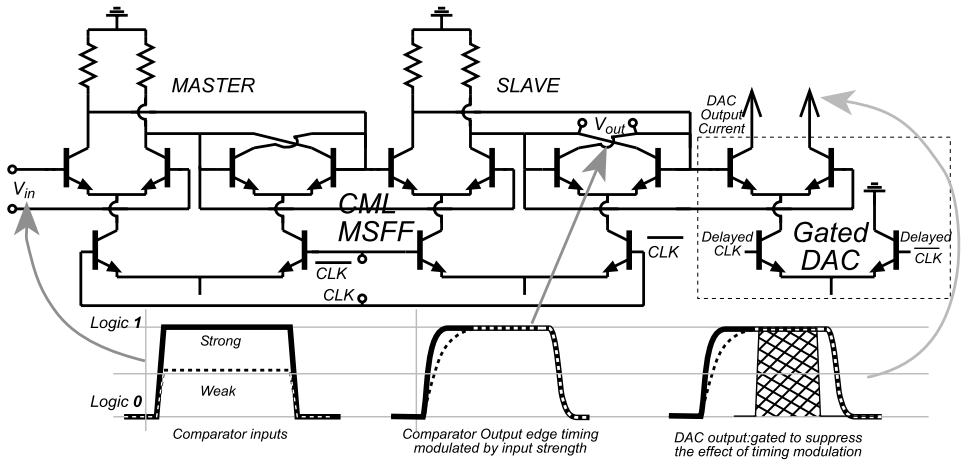

Figure 3.16: Qualitative description of comparator-metastability related issues in the context of DAC outputs.

For the clarity of discussion, a current mode logic (CML) master-slave flip-flop has been depicted. Two different possible input scenarios are described. The first corresponds to an input which switches from logic level **0** to **1** (shown by thick solid line). The second corresponds to the input changing from logic level **0** to a small positive voltage (thinner dashed line). Assuming no overload recovery errors in the comparator, the output of the master-slave flip-flop will reach logic level 1 for each of the two inputs. The time required for regeneration of the output to logic levels depends logarithmically on the initial voltage. Therefore, the time taken for the output to reach the final value is perceptibly different in the two cases. This is manifested as the timing modulation of the comparator output edge by its input. If an NRZ DAC is used, the current pulse generated by the DAC will demonstrate the same timing modulation of the edge speed. This results in feedback of different amounts of charge into the integrator for the same logic level at the output. The fact that the $\Sigma - \Delta$ modulator performance will suffer because of this imperfect feedback can be understood by a simplified

linear model of the loop. Fig. 3.17 shows the linearized $\Sigma - \Delta$ modulator with error in the DAC feedback.

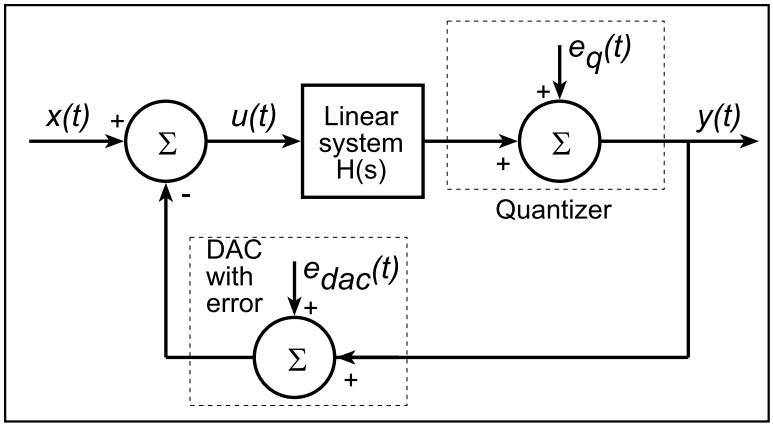

Figure 3.17: Linear model for $\Sigma - \Delta$ modulator loop with feedback error.

The quantization error is represented by $e_q(t)$ while the DAC feedback error is represented by the additive component $e_{dac}(t)$. The Laplace transform $Y(s)$ of output $y(t)$ can be written in terms of Laplace transforms $X(s)$, $E_q(s)$ and $E_{dac}(s)$ of the input $x(t)$ and the errors $e_q(t)$ and $e_{dac}(t)$ respectively, as

$$Y(s) = X(s).\frac{H(s)}{1+H(s)} + E_q(s).\frac{1}{1+H(s)} + E_{dac}(s).\frac{H(s)}{1+H(s)} \qquad (3.16)$$

The DAC feedback error is modified by the signal transfer function. Thus, it directly degrades the overall $\Sigma - \Delta$ modulator SNR . It can be observed from Fig. 3.16 that a fully balanced differential operation for the DAC does not eliminate the feedback errors due to metastability in the quantizer. The solutions commonly suggested in literature are:

- Using a preamplifier before the quantizer to ensure larger inputs to the comparator. The preamplifiers still suffer dynamic hysteresis. Further, given non-zero preamplifier output rise-times, the comparator can still receive small inputs, which can still cause metastability errors.

- Using two master-slave flip-flops to increase the degree of regeneration before the data is fed back to the DAC. This has the disadvantage of

introducing an extra clock cycle of delay which is not desirable from the point of view of modulator performance (section 3.2.2).

- Using a RTZ DAC. If this pulse is gated in the latter half of the clock period, with a delayed clock pulse, the current pulse generated by the DAC will show less impact of quantizer-output edge speed variations. This is shown qualitatively in Fig. 3.16.

Since we are fabricating the $\Sigma - \Delta$ modulator in a university cleanroom, yielding ICs with large transistor counts is a challenge. We decide to use the RTZ DAC in our design because of the lower circuit complexity and smaller transistor count.

3.2 Non-idealities in the system

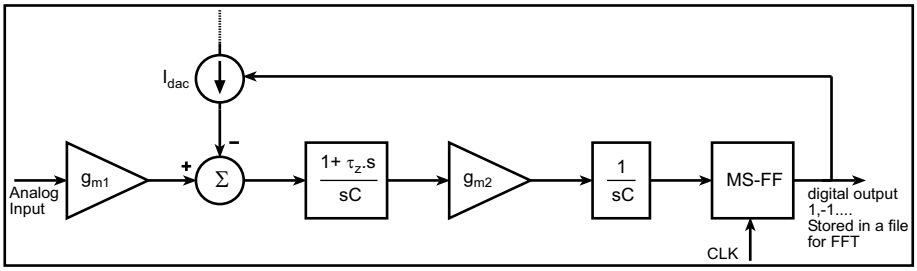

Figure 3.18: Block level description of an ideal $\Sigma - \Delta$ modulator loop in MATLAB.

The loop is initially designed by describing the various components as ideal blocks in MATLAB SIMULINK. Fig. 3.18 shows the block diagram of a second order $\Sigma - \Delta$ modulator. Suppose the digital output is $V_{out}(s)$, then the input to the quantizer can be represented as

$$\begin{aligned} V_q(s) &= (g_{m1}V_{in}(s) - I_{dac}V_{out}(s)) \left(\frac{g_{m2}(1+\tau_z s)}{s^2C^2}\right) \\ &= \frac{g_{m1}g_{m2}}{s^2C^2}(1+\tau_z s)\left(V_{in}(s) - \frac{I_{dac}}{g_{m1}}V_{out}(s)\right) \\ V_q(f) &= \left(\frac{f_u^2}{f_c^2}\right)\left(\frac{f_c^2}{f^2}\right)(1+j2\pi f\tau_z)\left(V_{in}(f) - \frac{I_{dac}}{g_{m1}}V_{out}(f)\right) \end{aligned}$$

where $f_u^2 = g_{m1}g_{m2}/(2\pi C)^2$ is the square of the effective unity gain frequency of the integrator chain. The quantizer input voltage amplitude is proportional to the square of f_u. Thus, f_u must be carefully selected. Presenting a very small input to the quantizer is likely to make the loop very sensitive to metastability errors.

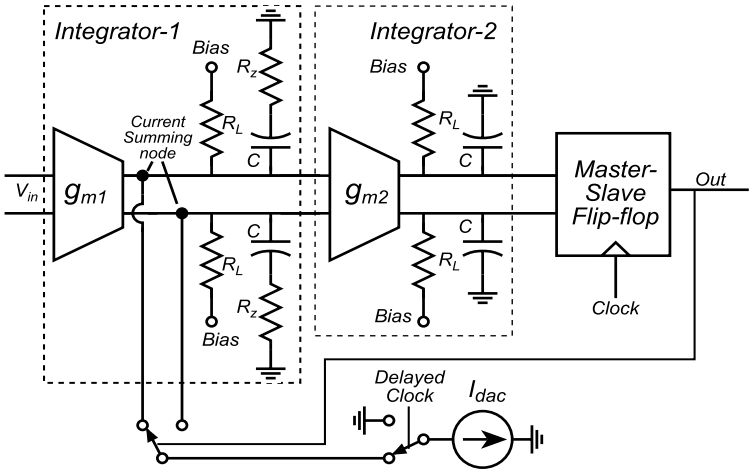

Figure 3.19: A block diagram of second-order continuous time $\Sigma - \Delta$ modulator.

Fig. 3.19 shows the simplified block diagram of the $\Sigma - \Delta$ modulator designed in this work. Assuming ideal circuit blocks, a MATLAB simulation was performed to estimate the $\Sigma - \Delta$ modulator performance. The numerical values used for the simulation were $f_{clock} = 20GHz$, $f_{in} = 78.125MHz$ (or, $OSR = 128$), $g_{m1} = 15$ mS, $g_{m2} = 65$ mS, $C = 3$ pF, average value of feedback current, $I_{dac} = 2$ ma and $\tau_z = R_z.C = 75$ ps (the zero time constant is $1.5T_s$). The integrator DC gains were set to infinity ($1/R_L = 0$). Fig. 3.20 shows the output corresponding to an input -10 dB below full-scale. The modulator achieved ~ 79 dB SNR (in 100 MHz bandwidth) suggesting that the maximum SNR that could be achieved is ~ 89 dB (in 100 MHz bandwidth) or ~ 169 dB (in 1Hz bandwidth). This is equivalent in performance to a 200 MS/s Nyquist-rate ADC with 14.5 ENOB resolution (refer to Eq. 2.6).

The performance of idealized $\Sigma - \Delta$ modulator loop can be improved by increasing the OSR, or the clock frequency. In the following subsections,

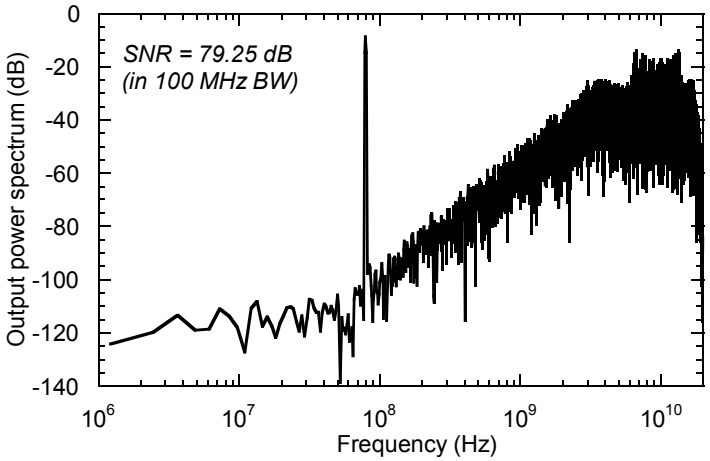

Figure 3.20: FFT of the output of an ideal second order $\Sigma - \Delta$ modulator loop for f_{clock} = 20 GHz, f_{signal} = 78.125 MHz; FFT bin = 1.22 MHz.

we will study the impact of certain non-idealities in the loop components on the loop performance. These non-idealities include:

- Finite integrator DC gain: The finite DC gain of the integrators (often referred to as *integrator leakage* in the literature) has the effect of providing only a finite suppression of quantization at lower frequencies [20], resulting in flattening of the noise floor as shown in Fig. 3.21.

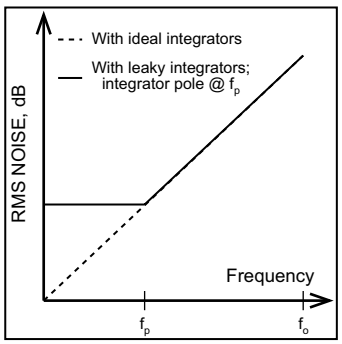

Figure 3.21: An illustration of the effect of integrator leakage on the spectral density of modulation noise.

- Excess loop delay: The excess delay in the loop comes from higher

order poles in the integrators and the DAC, and from the quantizer delays. The effect of the excess loop delay will be considered in detail in section 3.2.2.

- comparator hysteresis and metastability: As seen in previous section, the comparator errors may result in feedback errors which need more complex circuit design solutions.

The effect of the non-idealities mentioned above on modulator performance is studied in an organized fashion.

3.2.1 Finite DC gain - Integrator leakage

A high gain at lower frequencies ensures proper operation of the modulator by suppressing the baseband component of the quantization noise and redistributing it to higher frequencies. This helps in increasing the baseband *SNR* .

The effect of finite DC gain on the performance was studied by keeping the unity-gain frequency (g_m/C) of the integrators constant while changing the location of the pole. Fig. 3.22 shows the spectra of the output for pull-up resistor values (R_L) ranging from 10 Ω to 10 kΩ in increments of one decade. With the value of integration capacitor at $C = 3$ pF, the corresponding pole locations are: (1) 5.3 GHz, (2) 530 MHz, (3) 53 MHz and (4) 5.3 MHz.

It can be noted that for the case (3) and (4) where the pole location is below the signal frequency, the spectra are fairly close to that for the ideal case with infinite DC gain. However, as the pole location moves to higher frequencies as in case (1a) and (2a), the spectra become very tonal. This is predicted in [20]. A qualitative explanation is as follows: with a large integrator time constant, the quantizer input is a function of the $\Sigma - \Delta$ modulator input and of the quantization error of a large number of past samples. Thus, the quantization error becomes a complex function of the past behavior of the system and has a complex (aperiodic) behavior without spectral features. With short time constant, periodic behavior is seen in the quantization error leading to observation of tones at the output.

One of the solutions suggested in the literature to solve this problem is to add a white noise source at the input to the modulator (dither) [34]. In this case, the addition of dither at the input has no impact on the simulation

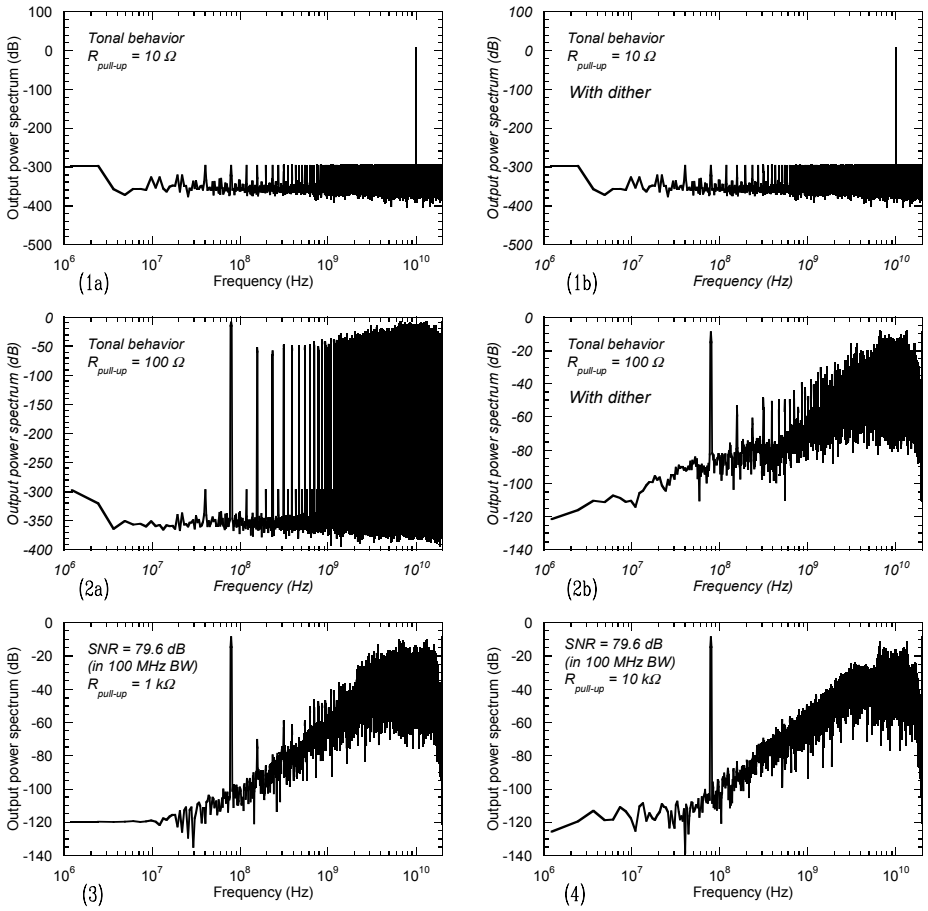

Figure 3.22: FFT of the output of a second order $\Sigma - \Delta$ modulator loop with varying integrator DC gain for f_{clock} = 20 GHz, f_{signal} = 78.125 MHz; FFT bin = 1.22 MHz. (1a - 6) R_L varies from 10 Ω - 10 kΩ. (1b) and (2b) repeat the simulation for (1a) and (2a) with dither, a white-noise source of strength -168 dBm/Hz added at the input to the modulator.

results with 10 Ω load (case 1b). However, the noise shaping is somewhat restored for the 100 Ω load (case 2b). However, the tones are not entirely suppressed.

From these simulation data, we conclude that a pull-up resistor value $R_L \geq 1$ kΩ is sufficient to give us a good $\Sigma - \Delta$ modulator performance.

3.2.2 Excess loop delay

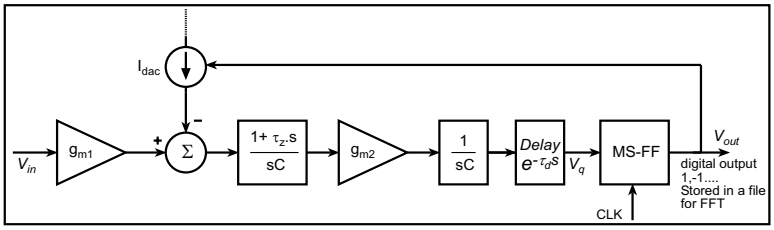

Figure 3.23: $\Sigma - \Delta$ modulator loop with excess loop delay.

Fig. 3.23 shows a $\Sigma - \Delta$ modulator loop with excess delay. Since the loop performance is characterized entirely by the time-variation of the input to the quantizer at the instant of clock-ticks, the delays in all the components can be lumped into a single delay represented by τ_d ($e^{-\tau_d s}$ in the frequency domain). Furthermore, the delay is simply a multiplying factor in the frequency domain, making its exact location in the signal chain unimportant for the purpose of determining quantizer input voltage. To understand the effect of this delay on *SNR* , we can again relate the quantizer input, $V_q(s)$ to the input, $V_{in}(s)$ and the fed-back digital output, $V_{out}(s)$.

$$V_q(s) = \frac{g_{m1}g_{m2}}{s^2C^2}\left(1+\tau_z s\right)e^{-\tau_d s}\left(V_{in}(s) - \frac{I_{dac}}{g_{m1}}V_{out}(s)\right) \tag{3.17}$$

If $\tau_d \ll T_s$, then the factor $\tau_d s \ll 1$ for all frequencies of interest. Under these conditions, we can write $e^{-\tau_d s} \approx 1/(1+s\tau_d)$. Thus, the effect of small values of excess delays is to add an extra pole to the transfer function.

$$V_q(s) = \frac{g_{m1}g_{m2}}{s^2C^2}\left(\frac{1+\tau_z s}{1+\tau_d s}\right)\left(V_{in}(s) - \frac{I_{dac}}{g_{m1}}V_{out}(s)\right) \tag{3.18}$$

The effect of the excess delay can be partially offset by introducing a zero at $\omega_z' = 1/\tau_d$. In our integrator design, it is done by simply placing a resistor in series with the integration capacitor. Fig. 3.24(a1-a15) shows the FFT of the output of the $\Sigma - \Delta$ modulator for various values of delay. The effectiveness of the compensation technique was also studied and these results are shown in Fig. 3.24(b1-b15). The results are summarized in Fig. 3.25. The *SNR* is seen to degrade from 79 dB to about 62 dB for a delay of 30 ps. The zero compensation restores the *SNR* to almost 79 dB in 100 MHz bandwidth.

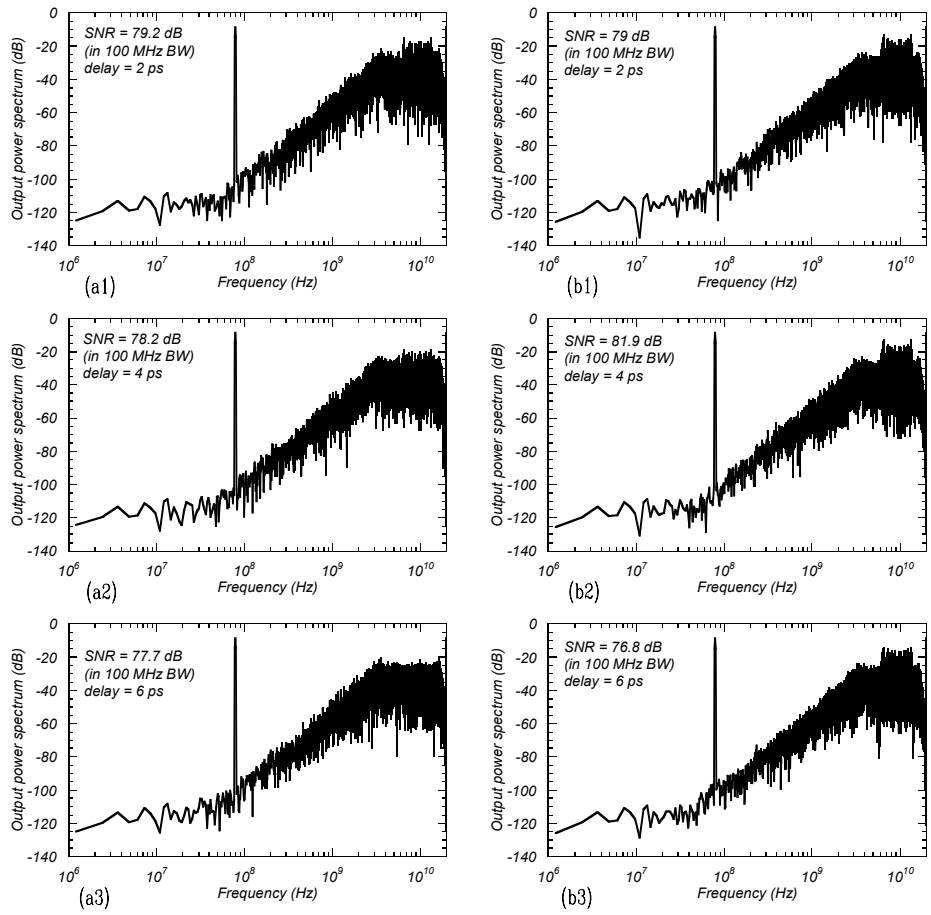

Figure 3.24: FFT of the output of a second order $\Sigma - \Delta$ modulator loop with varying excess loop delay: $f_{clock} = 20$ GHz, $f_{signal} = 78.125$ MHz; FFT bin = 1.22 MHz. (a1-a3) delay = 2, 4 and 6 ps. (b1-b3) delays compensated by using a zero in the transfer function.

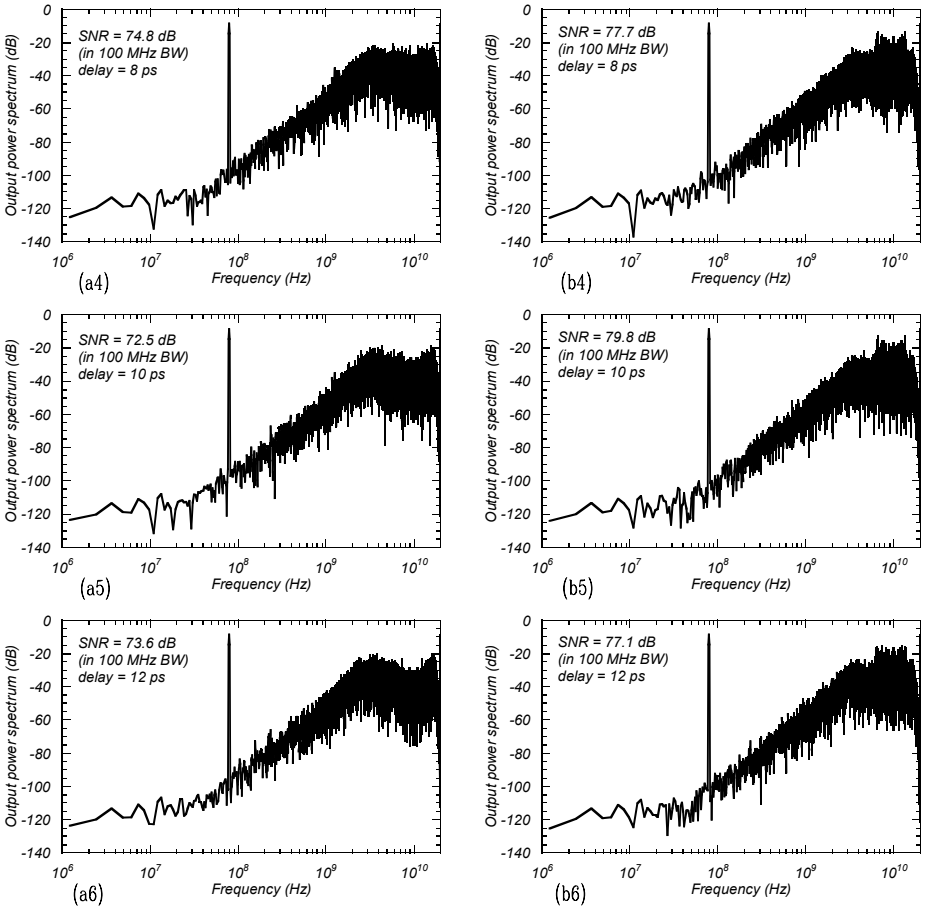

Fig. 3.24: contd. (a4-a6) delay = 8, 10 and 12 ps. (b4-b6) delays compensated by using a zero in the transfer function.

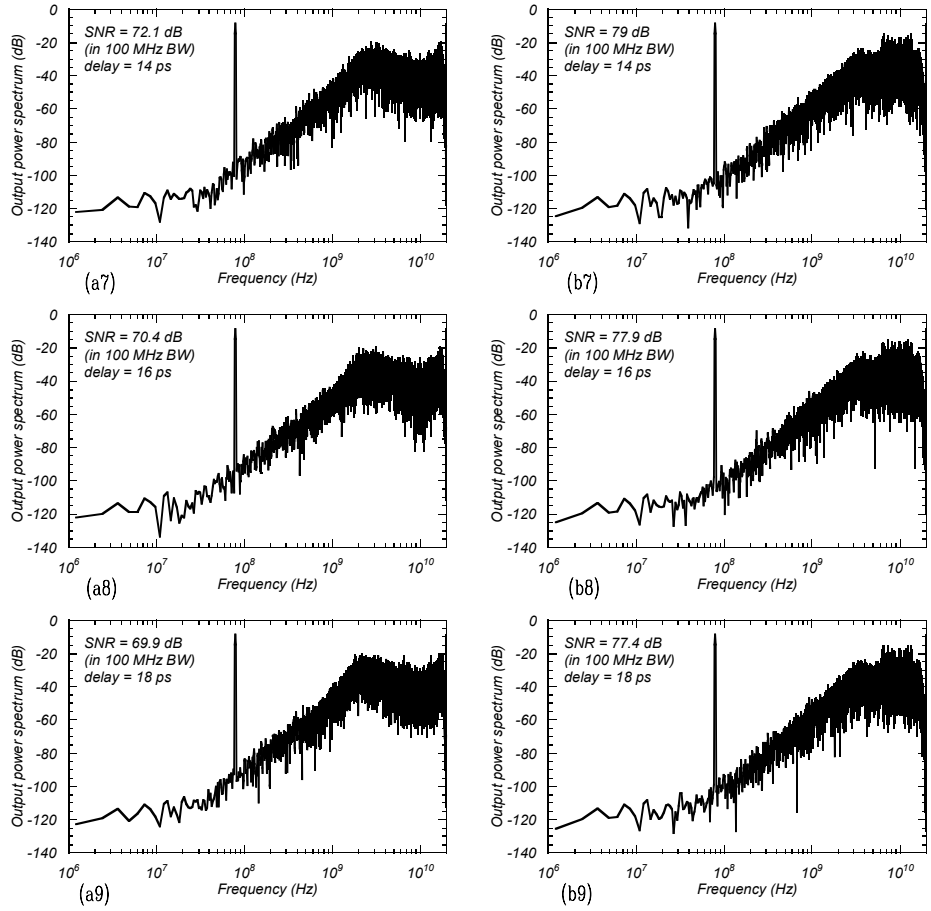

Fig. 3.24: contd. (a7-a9) delay = 14, 16 and 18 ps. (b7-b9) delays compensated by using a zero in the transfer function.

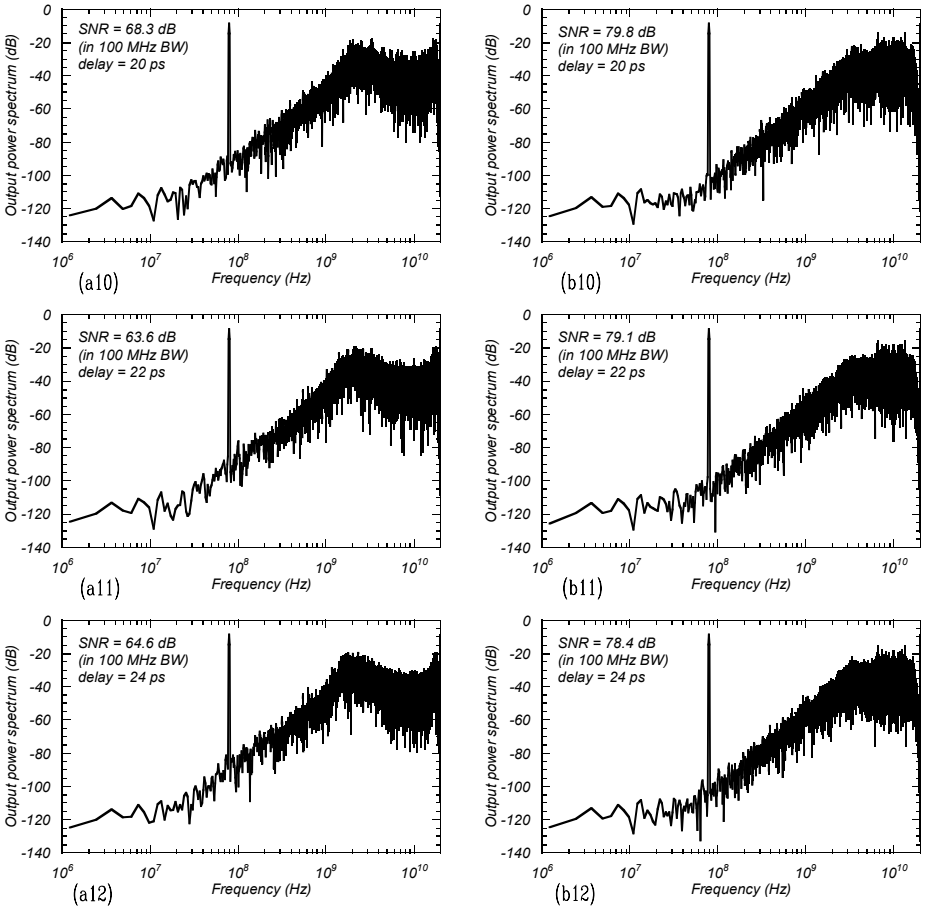

Fig. 3.24: contd. (a10-a12) delay = 20, 22 and 24 ps. (b10-b12) delays compensated by using a zero in the transfer function.

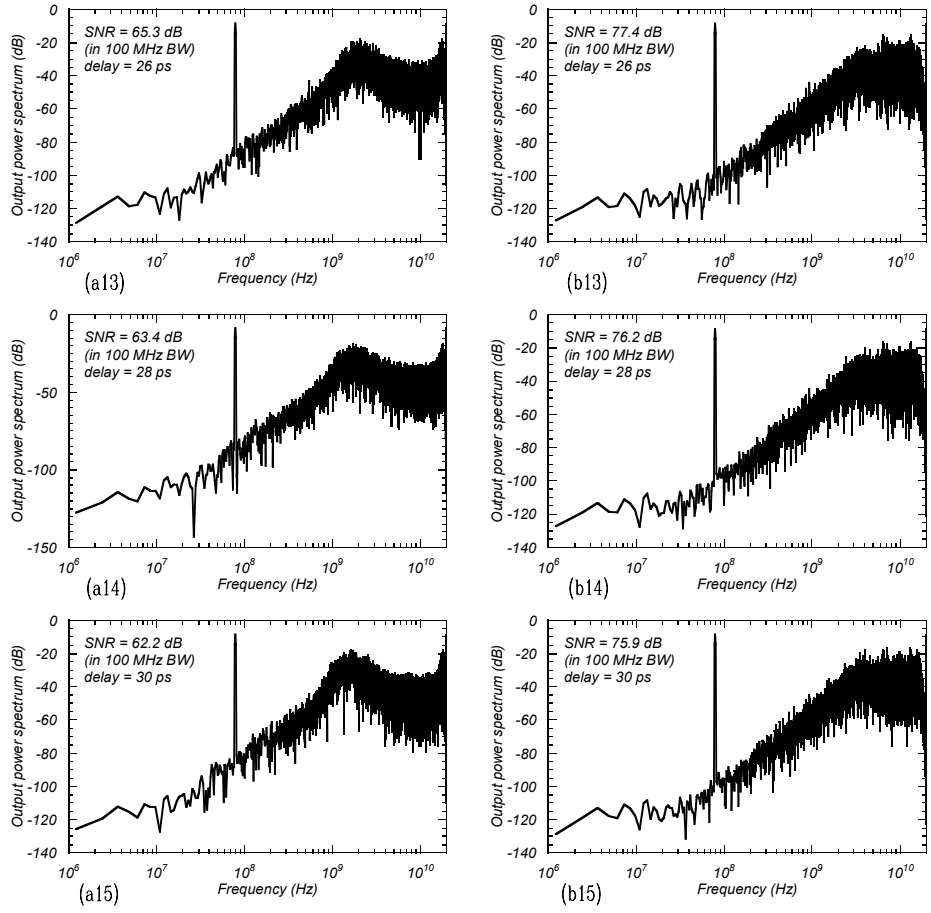

Fig. 3.24: contd. (a13-a15) delay = 26, 28 and 30 ps. (b13-b15) delays compensated by using a zero in the transfer function.

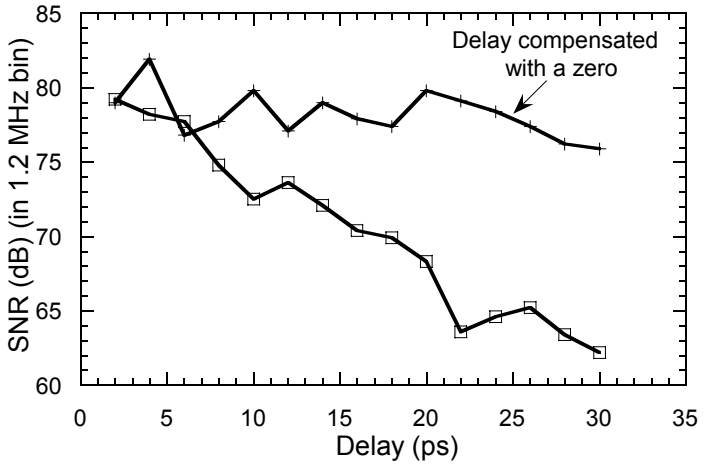

Figure 3.25: Compensation for the excess loop delay using a zero in the transfer function.

3.2.3 Quantizer hysteresis

In MATLAB, the hysteresis in quantizer is implemented as a 'relay' element placed at the input to the ideal quantizer. A hysteresis of V_H corresponds to the relay switching at $+V_H$ for the input variation from negative to positive values. The variation in input from positive to negative values results in the relay switching at $-V_H$. Thus, there is a decision ambiguity of width $2V_H$ where the quantizer output is incorrect. The effect of the variation of this decision ambiguity window on the output spectra is shown in Fig. 3.26(1-10). A 10 dB reduction in *SNR* can be noticed for a 50 mV hysteresis (100 mV window in decision ambiguity).

These MATLAB simulations provide an estimate for the factors limiting modulator performance. To derive the maximum performance from the modulator, it is essential to achieve as high an *OSR* as possible and that demands a small hysteresis/metastability error in the flip-flop, a high DC gain and large bandwidth from the integrator and small overall excess delay in the loop. These studies allowed us to fix the design values of the components at :

$$g_{m1} = 15\text{mS}$$

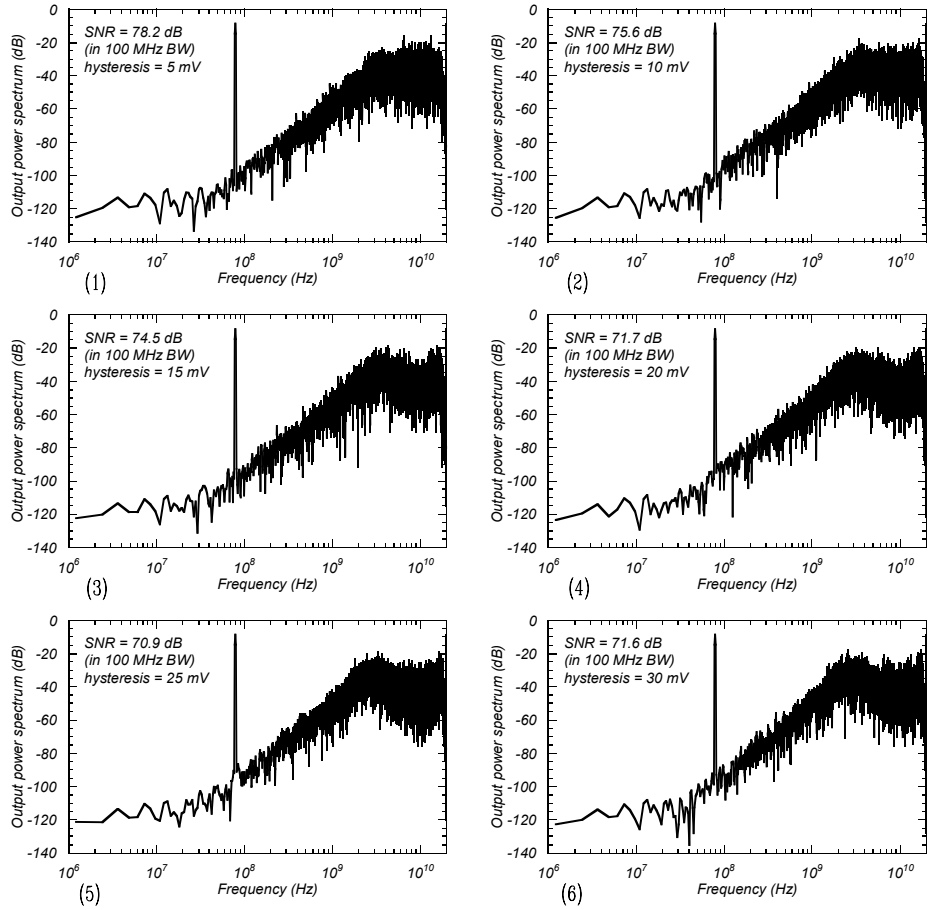

Figure 3.26: FFT of the output of a second order $\Sigma - \Delta$ modulator loop with comparator hysteresis: f_{clock} = 20 GHz, f_{signal} = 78.125 MHz; FFT bin = 1.22 MHz. (1-6) Hysteresis = 5 mV - 30 mV.

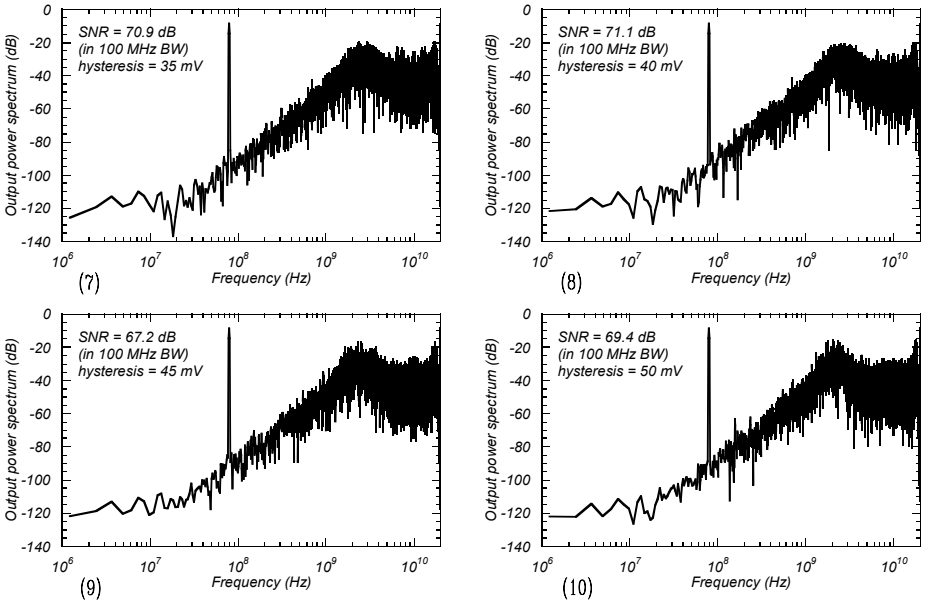

Fig. 3.26: contd. (7-10) Hysteresis = 35 mV - 50 mV.

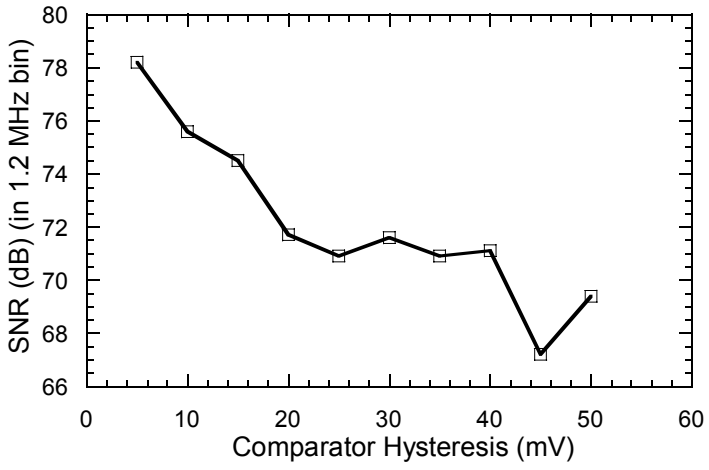

Figure 3.27: Variation of *SNR* with comparator hysteresis : Summary.

$$
\begin{aligned}
g_{m2} &= 65\text{mS} \\
C_{int1} &= 3\text{pF} \\
C_{int2} &= 3\text{pF} \\
\text{average } I_{dac} &= 2\text{mA} \\
f_{clock} &= 20\text{GHz} \\
R_L &= 1.125\text{k}\Omega
\end{aligned}
$$

3.3 SPICE design of the loop

We have already discussed the issues in the design of each component in the loop. Here we describe the actual circuit architecture used for each component.

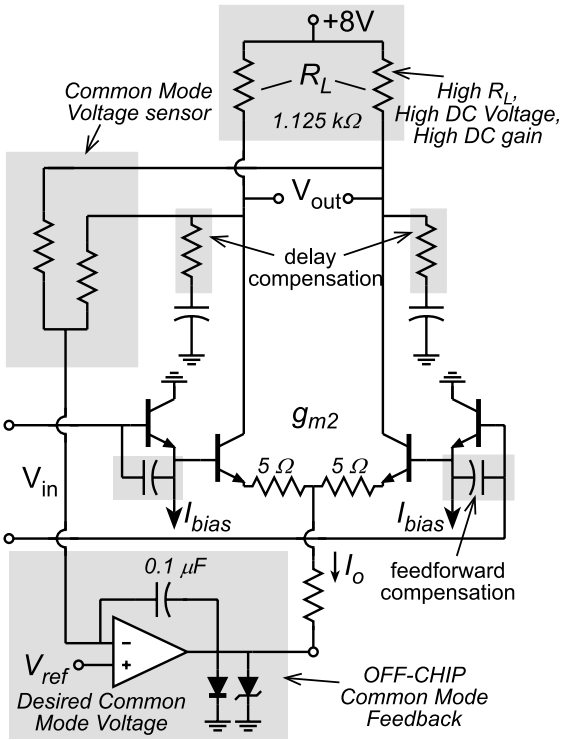

Figure 3.28: A schematic of the second integrator in the loop.

3.3.1 Integrator Design

Fig. 3.28 shows the schematic circuit of the second integrator in the loop. The circuit is simply a transconductance cell (g_{m2}) whose output is loaded by grounded capacitors. The design features a pair of high value on-chip resistors which sense the common-mode voltage at the output of the transconductance stage. For the purpose of final testing, this sensed common-mode voltage was input to an op-amp based off-chip common-mode feedback (CMFB) loop which controlled the bias current (and hence the transconductance) of the differential pair. The CMFB loop bandwidth was limited by introducing a dominant pole which ensured that the feedback did not interfere with the operation of the $\Sigma - \Delta$ modulator loop.

The transconductance stage is a differential pair driven by emitter-followers. These provide a high input impedance at DC which results in a large DC gain. At high frequencies, the integrator is driven from a low-impedance node formed by integration capacitor ($1/j\omega C_{int1}$) for the first integrator. Since the output impedance of the emitter-follower transistors ($kT/qI_E + R_{ex} + R_{bb}/\beta$) may be higher than that of the drive point at high frequencies, they are removed from signal path at high frequencies by feed-forward compensation. This is achieved by bypassing the emitter-follower transistors with a feed-forward capacitor.

The device and layout parasitics result in higher order poles which introduce excess delay in the integrator. Placing a resistor in series with the integrating capacitor introduces a zero in the transfer function and partially compensates for the effect of these delays. A 5 Ω resistor is used for degeneration to achieve the required transconductance.

In analyzing the performance of $\Sigma - \Delta$ modulator, we have considered only the quantization noise. This would be adequate if the noise-figure of the input stage was very small. The noise-figure of the other components in the loop is somewhat less important because the noise contributed by them is suppressed by the gain preceding them. This is not true for the input stage transconductance. The input stage noise directly degrades the *SNR* at the output. Fig. 3.29(a) shows a second order $\Sigma - \Delta$ modulator with noise sources e_{n1}^2 and e_{n2}^2 representing the input referred noise powers (in $V^2/\sqrt{Hz}$) for the two integrators in the loop. The effective noise at the input of the loop is $e_n^2 = e_{n1}^2 + e_{n2}^2.(sC/g_{m1})^2 = e_{n1}^2 + e_{n2}^2.(\omega/\omega_{u1})^2$, where $\omega_{u1} = g_{m1}/C$ is the unity gain frequency of the first integrator. Thus, in the signal bandwidth, $(\omega/\omega_{u1}) \ll 1$, making the noise contribution from the

second integrator less important compared to that from the first integrator.

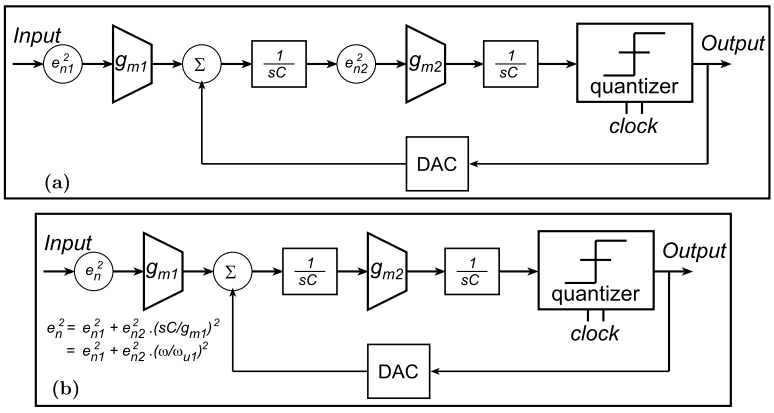

Figure 3.29: (a) Noise contribution from integrators in a second order $\Sigma-\Delta$ modulator loop. (b) Effective noise due to the integrators referred to the input of the loop.

Similarly, the linearity of the input stage impacts the dynamic range of the $\Sigma - \Delta$ modulator. Jensen [36] reported a linearized input g_m stage based on the Caprio's cell [40]. Our initial design used a Caprio's cell in the input stage. Simulations showed that the Caprio's cell resulted in $\sim$ 19 dB improvement in IP3. The simulated two-tone response of the input stage with and without the Caprio's cell is shown in Fig. 3.30. The initial fabrication attempts failed owing to the high transistor count in the $\Sigma - \Delta$ ADC circuit. Since the focus on this work was on demonstrating a working $\Sigma - \Delta$ modulator that can be yielded in a university cleanroom environment, the next generation design eliminated the Caprio's cell in favor of a differential pair with lower transistor count.

The effect of linearity of the input stage on that of the overall loop can be reduced by a careful choice of bias currents. From the optimum values for loop components, we see that the average I_{dac} is 2 mA. Therefore, the RF component in DAC current switches between $\pm$2 mA. The loop starts overloading when the signal current $I_{sig} = g_{m1}v_{in}$ equals the DAC switching current. For larger inputs, the signal current at the current summing node is larger than can be corrected for by the DAC feedback current which leads to generation of harmonic distortion from the negative-feedback loop. The input stage overloads and generates harmonic distortion when the input

voltage is sufficiently large to switch the entire bias current to one of the arms of the differential pair. Thus, if the input g_m stage is biased at $I_{bias} \gg$ 2 mA, the input stage saturates after the feedback loop overloads. This results in the IP3 of the loop being determined by the loop components rather than the input stage. In our design, resistor values were chosen so as to achieve the required transconductance at a bias current of 6 mA.

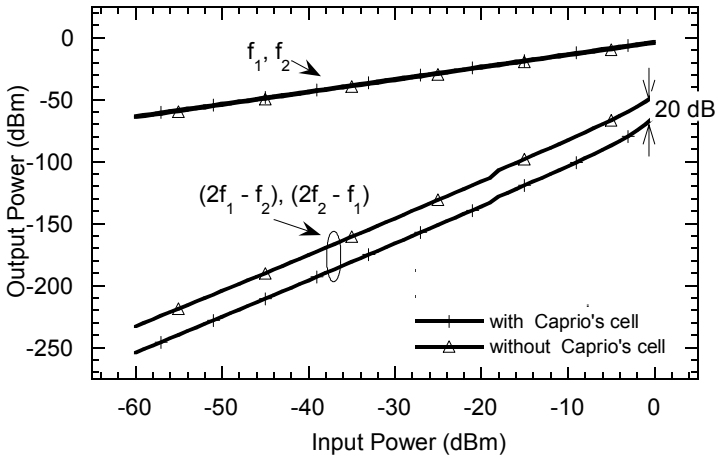

Figure 3.30: Simulated two-tone response of the input stage with and without the Caprio's cell. The simulation used $f_1 = 100\text{MHz}, f_2 = 90\text{MHz}$. Caprio's cell causes a 20 dB reduction in the third order $(2f_1 - f_2)$ components.

Fig. 3.31 shows the final circuit schematic used for the input integrator. The circuit uses the same CMFB loop described above along with the delay compensation techniques. The output nodes of this transconductance cell are the current summing node where the feedback current from the DAC is added to the current generated by the input signal ($g_{m1}v_{in}$) to create the error signal.

The response of the two integrators was simulated on SPICE and the results are plotted in Figs. 3.32 and 3.33. From the plots it is clear that the integrator have a very wide bandwidth and they show a $g_m/j\omega C$ behavior from about 40 MHz to about 100 GHz.

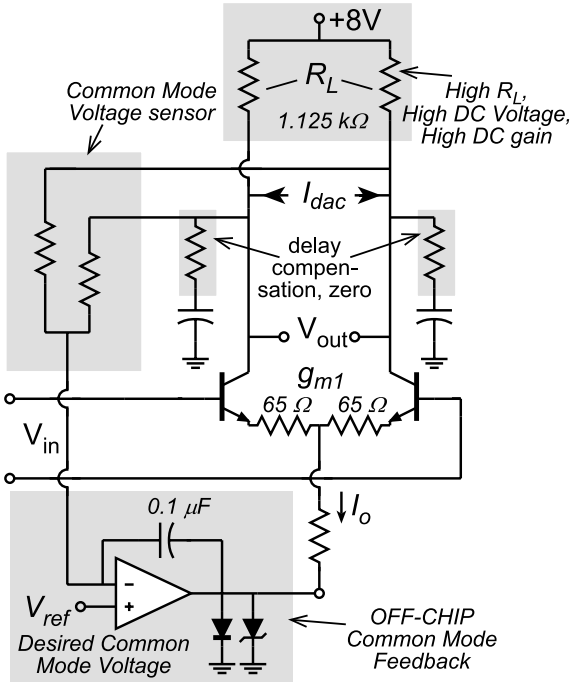

Figure 3.31: A schematic of the input stage integrator.

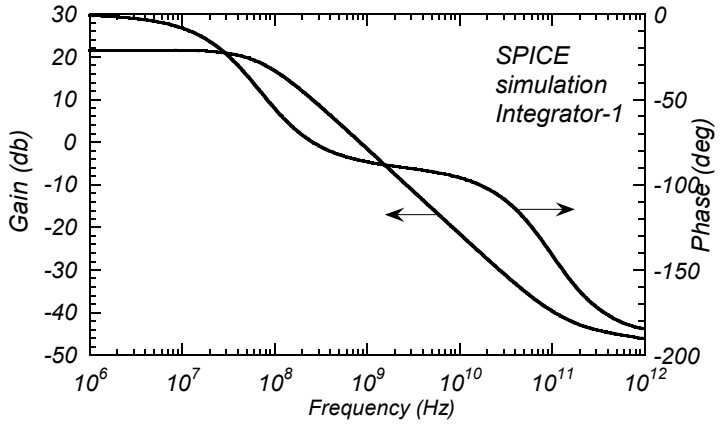

Figure 3.32: Frequency response of the input stage integrator.

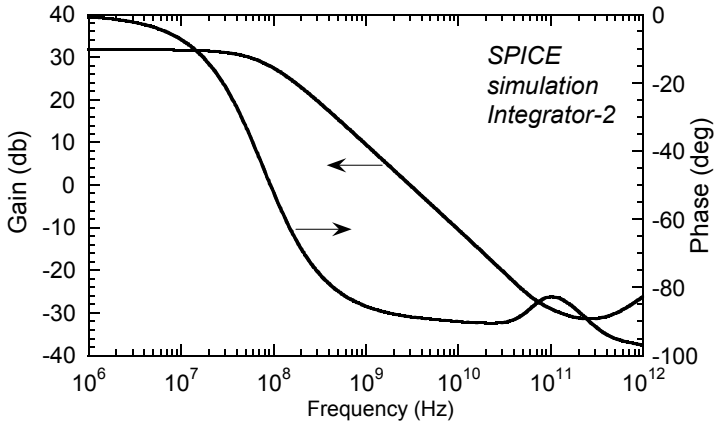

Figure 3.33: Frequency response of the second integrator in the loop.

3.3.2 Quantizer and RTZ DAC

The quantizer used in this work is an ECL master-slave flip-flop designed by Q. Lee. The basic core of the circuit has been demonstrated to operate as a divide-by-two circuit at 66 GHz [19]. The schematic of a latch which forms a part of the master-slave flip-flop is shown in Fig. 3.34. For clarity, the diodes used for protection from breakdown are not shown.

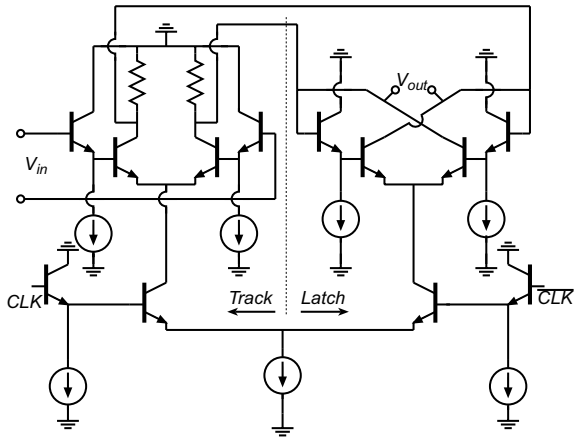

Figure 3.34: Typical ECL latch used in a master-slave flip-flop.

The latch uses a two-level series gated ECL logic. The lower level is

driven by the clock signal while the data drives the upper level. During the tracking period, the clock signal (CLK) enables linear differential stage which tracks the data. During latching period, the $\overline{\text{CLK}}$ enables the positive-feedback-connected differential pair which regenerates the data at its inputs to appropriate logic levels. In a master-slave flip-flop, two such latches are connected in cascade, with the regeneration stage of the first latch (master) and the tracking stage of the second latch (slave) enabled by the same clock phase.

As described earlier, metastability and dynamic hysteresis errors in the quantizer limit clock speed. The quantizer in a $\Sigma - \Delta$ modulator loop will receive inputs which are distributed over the entire output range of the $g_m - C$ integrator. The master-slave flip-flop used here is designed for use in digital circuits; i.e. the signals at its input switch between two logic levels. Therefore, in digital circuits, the master-slave flip-flop does not demonstrate overdrive recovery and metastability related errors very often. For use as a comparator in $\Sigma - \Delta$ modulators, the preamplifier and the regeneration stages have to be designed to have low time constants. This is essential for alleviating the effect of metastability and hysteresis errors on modulator performance.

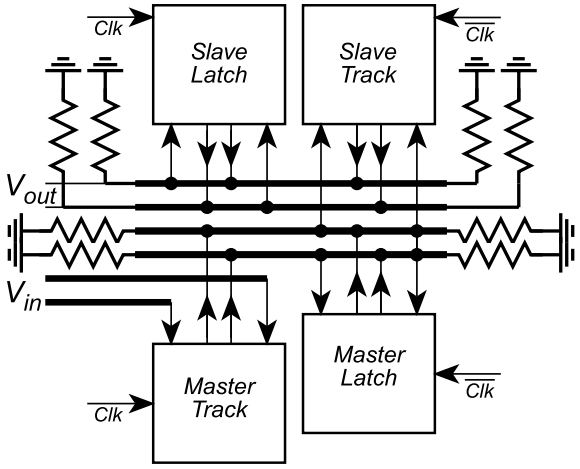

Figure 3.35: Schematic representation of the master-slave flip-flop depicting the layout symmetry.

The decision to use an existing master-slave flip-flop design for the quantizer was motivated by the following factors-

- The core of the flip-flop had already been validated by high speed operation of the divide-by-two circuit.
- The layout of the core was available. Minor modifications were needed to achieve compatible DC levels. Having an error free layout reduced the overall design effort and design-risk considerably.

A schematic of the flip-flop depicting the symmetry employed in the layout is shown in Fig. 3.35. The 'track' and the 'latch' blocks together represent the ECL clocked latch shown in Fig. 3.34. The flip-flop layout was entirely symmetric with the signals routed over transmission-line bus. The output of the track and latch blocks are brought to 90 Ω transmission lines which are terminated at either ends by a 90 Ω resistor. All signals are routed from the collector output of the differential pairs rather than from the emitter output of emitter follower due to potential instability of the latter. The emitter followers had adequate resistive damping to ensure stable operation without ringing.

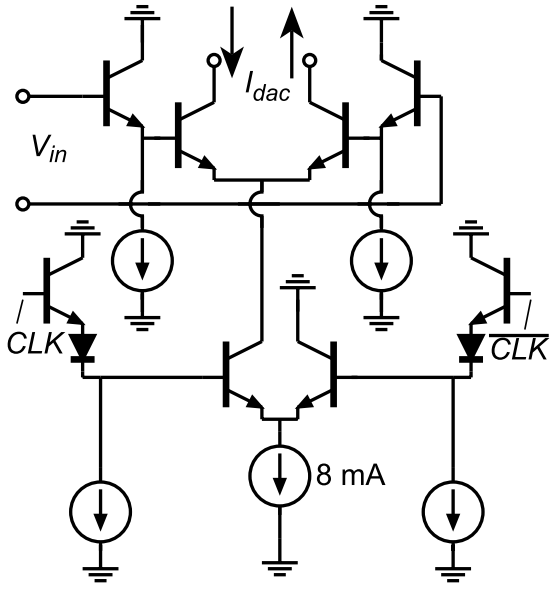

Figure 3.36: Circuit schematic of the RTZ DAC.

Fig. 3.36 shows the schematic of the DAC used in this design. To maintain clarity, the level-shift diodes used for protection from breakdown

are not shown. The DAC is a differential current steering pair. Our design requires us to provide a DC current of 2 mA from the DAC (assuming an equal density of logic **1** and logic **0** output from the quantizer). RTZ version of the DAC is obtained by gating the current in the differential pair with a clock pulse. The schematic for this configuration is shown in Fig. 3.36. The correct biasing condition requires the use of current source of 8 mA.

The clock signal to circuit is available in a single-ended form from the synthesizer. Clock buffers were used on wafer to convert the signal to differential form. The differential clock signal thus generated was further amplified to make the edges steeper and feed the flip-flop and the gated DAC. The delay in the path from the buffer to DAC was adjusted appropriately to gate the data reaching the DAC in the latter part of its period.

3.3.3 Input stage noise estimation

We now consider the input stage noise. This is important to be able to estimate the degradation in *SNR* due to the input stage noise. Fig. 3.37 depicts the significant noise sources that contribute to the noise current at the current summing node. For the purpose of this calculation, following device and circuit parameters were used:

$$\begin{aligned}
\text{device size} &= 1\mu\text{m} \times 16\mu\text{m} \\
\text{emitter contact resistance, } r_{ex} &= 4\Omega \\
\text{base contact resistance, } r_{bb} &= 15\Omega \\
\text{bias current, } I_c &= 6\text{mA} \\
\text{DC current gain, } \beta &= 50 \\
\text{emitter degeneration resistance, } R_E &= 65\Omega \\
\text{generator resistance, } R_{gen} &= 50\Omega \\
\text{device junction temperature, } T &= 75^o \text{ C} \\
\text{current source pull-down resistance, } R_{pd} &= 250\Omega \\
\text{mismatch in differential drive, } \alpha &= 20\% \\
\text{bias current for next stage, } I_c' &= 4\text{mA};
\end{aligned}$$

With a perfectly differential drive, the noise current from the pull-down resistor will split between the two transistors in the differential pair. But, since this contribution in the two branches is correlated, it effectively gets

canceled under differential operation. For this calculation, we have assumed a 20 % mismatch (the factor α) in the differential drive.

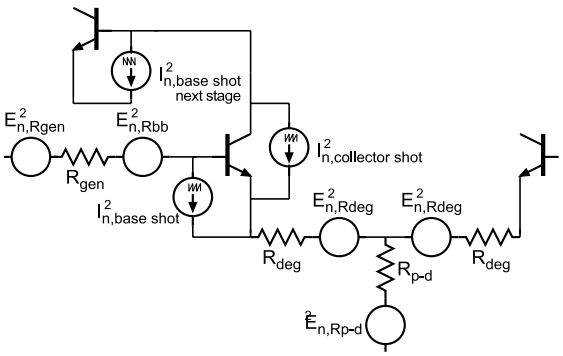

Figure 3.37: The important noise sources in the input stage contributing to the noise current at the current-summing node.

With these parameter values, the contribution from various noise sources in the input transistor to the collector noise current are evaluated below:

1. Shot noise from collector current $\rightarrow I_1^2 : I_{coll,shot}^2 = 2kT/(1/g_m + r_{ex} + R_E)^2 = 8.87 \times 10^{-24}$ A^2/Hz.

2. Shot noise from base current $\rightarrow I_2^2 : I_{base,shot}^2 = (2kTg_m/\beta)((R_{gen} + r_{bb} + r_{ex} + R_E)/(1/g_m + r_{ex} + R_E))^2 = 8.32 \times 10^{-23}$ A^2/Hz.

3. Base thermal noise $\rightarrow I_3^2 : I_{base,thermal}^2 = 4kTr_{bb}/(1/g_m + r_{ex} + R_E)^2 = 5.29 \times 10^{-23}$ A^2/Hz.

4. Thermal noise from emitter degeneration $\rightarrow I_4^2 : I_{deg,thermal}^2 = 4kTR_E/(1/g_m + r_{ex} + R_E)^2 = 2.43 \times 10^{-22}$ A^2/Hz.

5. Thermal noise from generator resistance $\rightarrow I_5^2 : I_{deg,thermal}^2 = 4kTR_{gen}/(1/g_m + r_{ex} + R_E)^2 = 1.76 \times 10^{-22}$ A^2/Hz.

6. Thermal noise from current source pull-down resistance $\rightarrow I_6^2 : I_{pd,thermal}^2 = 4kTR_{gen}\alpha^2/R_{pd} = 3.1 \times 10^{-24}$ A^2/Hz.

7. Shot noise from base current of next stage $\rightarrow I_7^2 : I_{pd,thermal}^2 = 2qI_c'/\beta = 2.56 \times 10^{-23}$ A^2/Hz.

These contributions are shown in Fig. 3.38. The total noise current at the current summing node is

$$\begin{aligned} I_{c,noise}^2 &= I_1^2 + I_2^2 + I_3^2 + I_4^2 + I_5^2 + I_6^2 + I_7^2 \\ &= 5.93 \times 10^{-23} \mathrm{A}^2/\mathrm{Hz}. \\ \text{or } I_{c,noise} &= 24.35 \mathrm{pA}/\sqrt{Hz} \end{aligned}$$

The maximum signal current at the current-summing node under "no-overload" conditions is $I_{c,signal} = 2$ mA. Thus, the maximum *SNR* at the output of the input stage is

$$SNR_{\text{ input stage}} = 20 \log_{10} \left(\frac{I_{c,signal}}{I_{c,noise}} \right) = 158.3\mathrm{dB} \text{ (in 1 Hz)} \qquad (3.19)$$

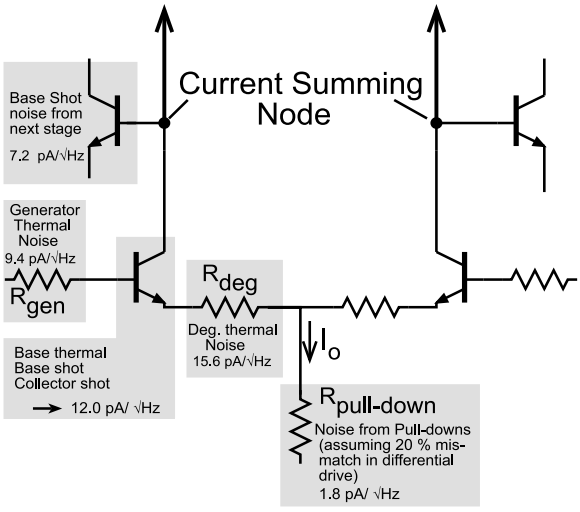

Figure 3.38: Contribution of various noise sources in the input stage to noise current at the current-summing node.

Earlier in the chapter, we evaluated the maximum *SNR* of the ideal $\Sigma - \Delta$ modulator to be about 169 dB in 1 Hz. Thus the input stage causes a 11 dB reduction in the *SNR* . The first order analysis conducted above suggests that the best performance that can be achieved from the $\Sigma - \Delta$ modulator is an *SNR* of about 158 dB (in 1 Hz) or 78 dB (in 100 MHz bandwidth). The equivalent Nyquist rate ADC will have a sample rate of 200 MS/s with 12.7 ENOB.

The complete $\Sigma - \Delta$ ADC circuit consists of 150 transistors. The circuit schematic of the complete ADC is shown in Fig. 3.39.

3.3.4 Layout of the chip

Careful layout of the circuit is required to reduce the parasitics on the critical paths by limiting wire lengths. Any parasitic capacitance on the collectors of the switching transistors in the ECL circuits deteriorates performance. There are three levels of wiring available in the transferred-substrate HBT IC process. The metal-1 and metal-2 levels are isolated by silicon nitride (SiN) which is also used for implementing MIM capacitors. Metal-2 is separated from the ground plane by the dielectric benzo-cyclo-butene (BCB) which forms the substrate for microstrip wiring. All interconnect wires on metal-1 and metal-2 can be modeled as a microstrip transmission lines. The microstrip back side ground plane eliminates ground return loop inductance by providing a continuous ground return path for high frequency signals on the IC.

The critical component in the ADC is the ECL master-slave flip-flop. As described in section 3.3.2, the master-slave flip-flop uses 90 Ω transmission lines. On a 5 μm thick BCB substrate, the corresponding interconnects are $\sim$ 4 μm wide. While there is negligible parasitic capacitance from the wires on BCB, cross-overs between metal-1 and metal-2 layers add $\sim$ 2 fF of capacitance per crossover.

The third level of interconnects is implemented on the collector layer. In this design, the cross-over capacitance has been reduced wherever possible by using the collector layer for one of the interconnects. The delayed clock for the gated DAC is obtained by using transmission line delays in the clock path between the clock-buffer and the DAC. The layout of the complete ADC occupies 1.5 μm $\times$ 1.3 μm. The cell size for repetition on wafer was chosen as 3.9 μm $\times$ 3.9 μm. This allowed inclusion of 4 repetitions of the circuit per cell leading to an estimated 60 ADC chips per quarter of a 2" wafer processed. The completed layout of the circuit is shown in Fig. 3.40.

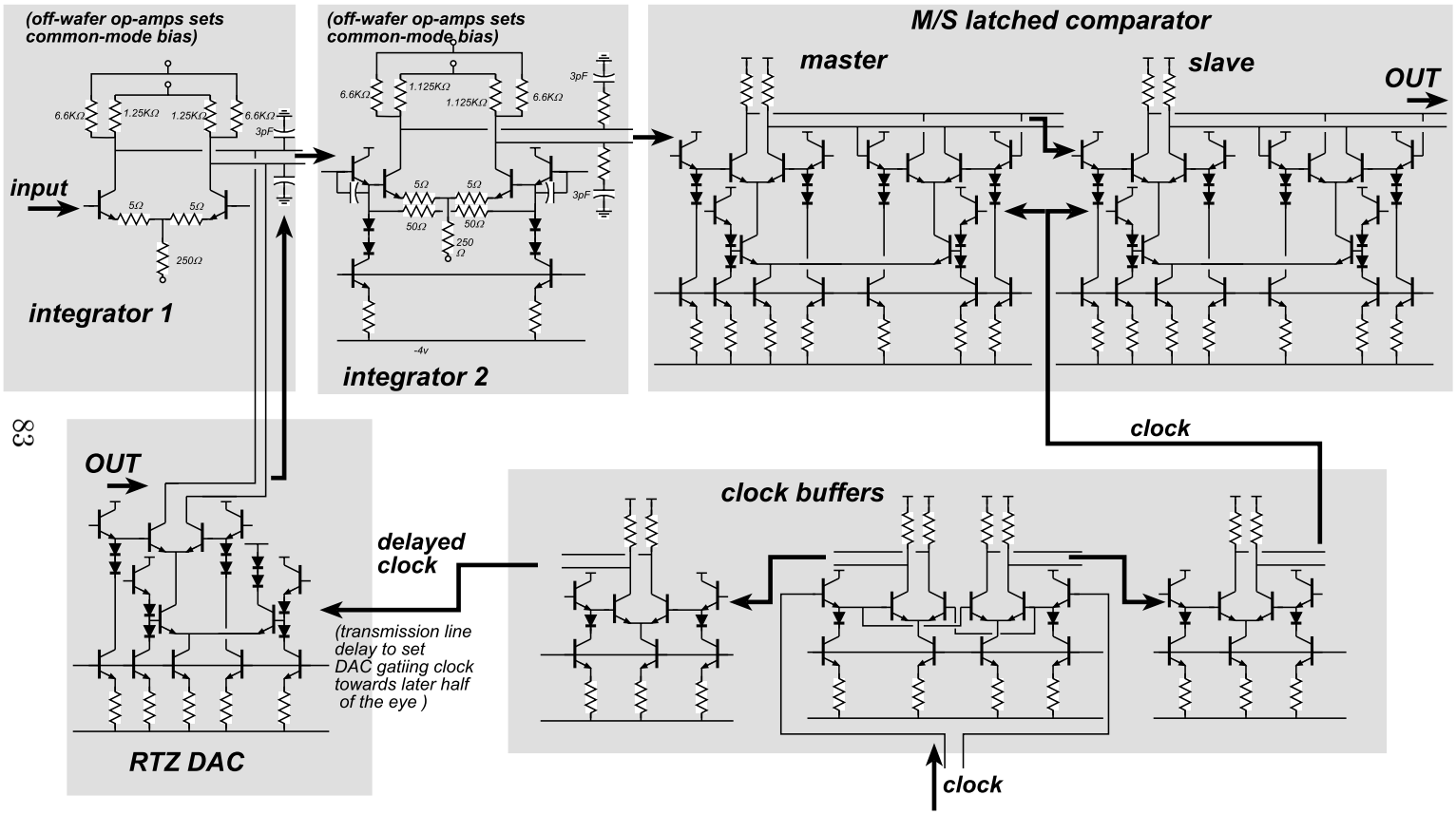

Fig. 3.39: A simplified schematic of the complete ΣΔ ADC circuit

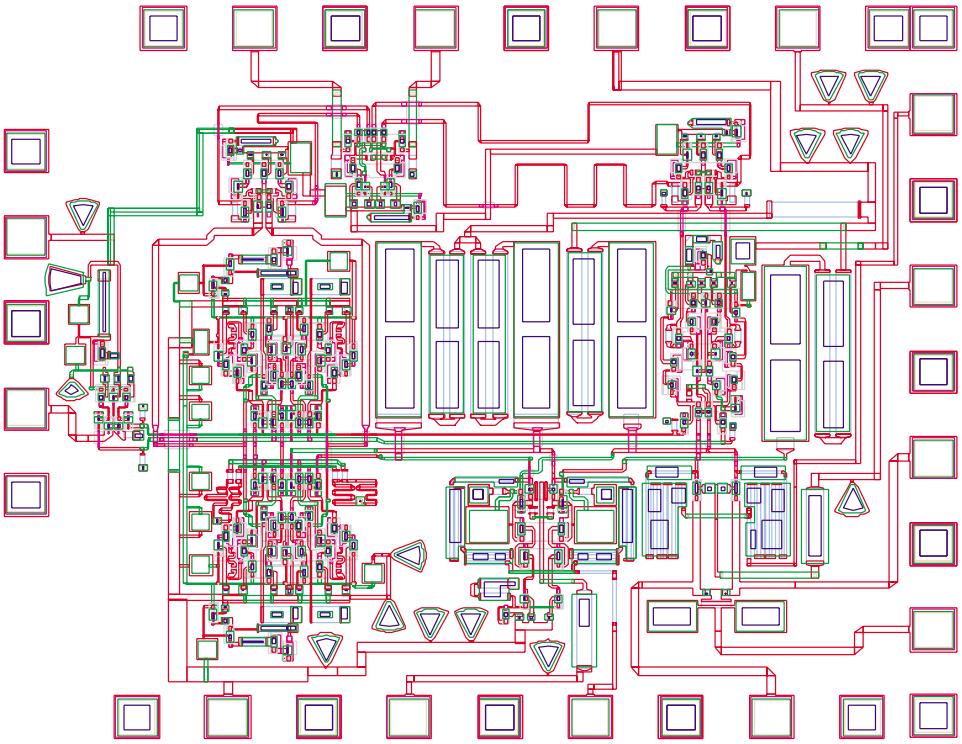

Figure 3.40: Layout of the second order $\Sigma - \Delta$ modulator IC.

Chapter 4

Measurement and Results

A successful process run yielding working $\Sigma - \Delta$ ADCs was obtained after several failed process runs. This required several process changes which are described in Appendix B. This chapter describes the measurement technique used for characterizing the ADC performance as well as the results obtained.

The wafer (ID: System A - 981116A) had an epitaxial layer structure with 300 Å thick 4×10^{19} cm^{-3} Be-doped base with 2 kT grading in band gap. The collector was a Schottky contact to lightly Si-doped 2000 Å thick layer. This wafer was chosen because it was available; a thicker 400 Å base and a thicker 300o Å collector would have given better circuit performance. The circuit components critical for high speed operation of the ADC (the master-slave flip-flop and the RTZ DAC) used devices with 0.7 μm $\times$ 12 μm emitters. Test devices with similar dimensions were characterized for DC and RF performance. Typical DC characteristics of the device are shown in Fig. 4.1. The DC characteristics demonstrate a DC current gain $\beta \geq 100$ and a breakdown voltage $BV_{CEO} \sim 1.4$ V.

The RF characteristics of the device were measured from 50 MHz to 50 GHz using HP 8510C. The measured s-parameters can be used to obtain the frequency variation of short-circuit-current-gain (h_{21}) and Mason's unilateral gain (U). Fig. 4.2 shows the RF characteristics of the 0.7 μm $\times$ 12 μm emitter device at $V_{ce} = 1$ V and emitter current density $J_E = 1.7$ kA/cm^2. A 20 dB/decade extrapolation of h_{21} and U provide the values of f_τ and f_{max} for the device as 190 GHz and 217 GHz, respectively. A significant improvement is typically observed in the value of f_{max} after a collector

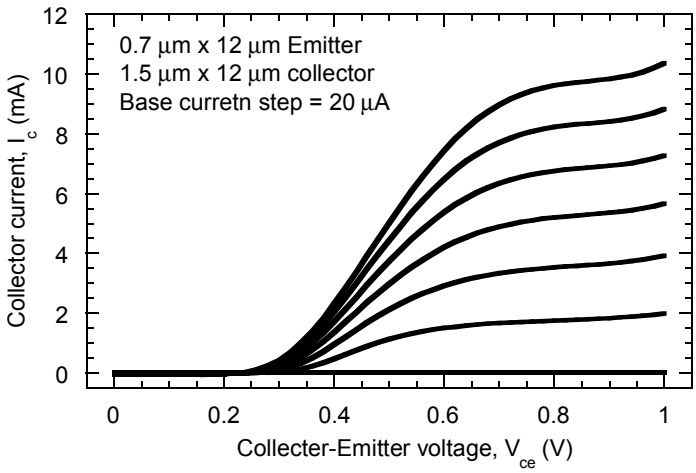

Figure 4.1: DC common emitter characteristics for a test device.

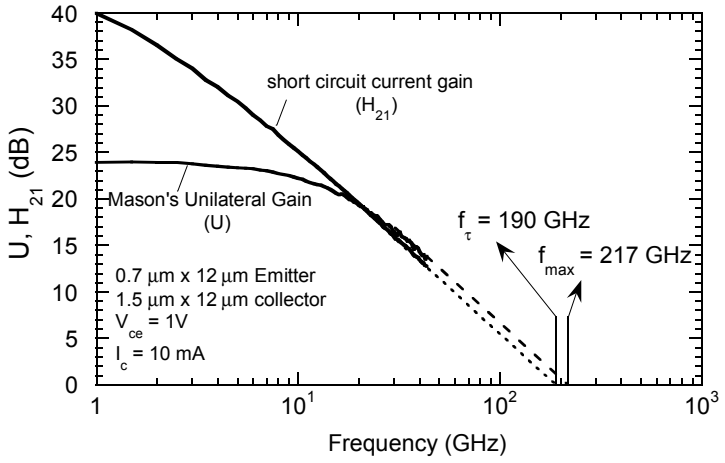

Figure 4.2: RF characteristics of a test device.

recess etch which reduces the collector-base junction overlap capacitance. Since this employs a wet etch which is likely to attack the exposed nichrome resistors, it was not done on this wafer. We intend to solve this problem by adding a Si_3N_4 layer to protect the resistors in the future process runs. The fabricated resistors yielded a sheet resistance of 42 $\Omega/\Box$ against a required value of 50 $\Omega/\Box$. The chip photograph of the completed $\Sigma - \Delta$ modulator is shown in Fig. 4.3.

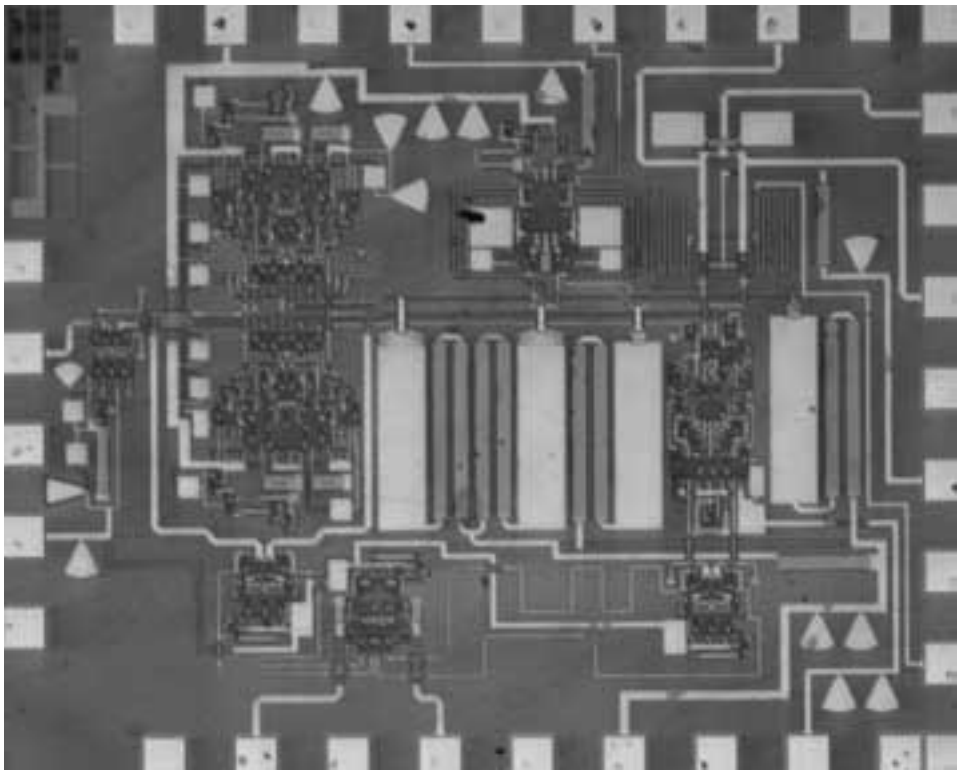

Figure 4.3: Photograph of the die for the completed $\Sigma - \Delta$ modulator IC.

4.1 ADC measurement setup

In the absence of a decimator following the modulator, a typical $\Sigma - \Delta$ ADC measurement uses a high-speed logic-analyzer to capture the output digital data stream. A Fourier transform (FFT) is employed on this cap-

tured data to obtain its spectrum. In our measurements, we clocked the $\Sigma - \Delta$ modulator at 18 GHz. Since, we do not yet have a logic analyzer sufficiently fast to capture a 18 Gbps data stream, we resorted to an analog measurement technique. This involves the use of an analog spectrum analyzer to observe the spectrum of the output. The other feature of our measurement was the use of two tones at the input that allowed us to verify that the distortion components were not dominating the output spectrum. A simplified schematic of the measurement setup is shown in Fig. 4.4.

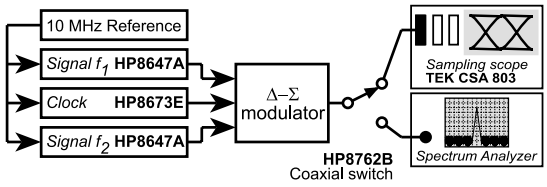

Figure 4.4: The setup used for testing the $\Sigma - \Delta$ modulator.

The two input tones are generated from HP 8647A synthesizers while the clock frequency of 18 GHz was provided by HP 8673E synthesizer. The ICs were tested by on-wafer probing using 40 GHz microwave probes from GGB Industries. The synthesizers are phase-locked to a common 10 MHz reference. As seen from the chip photograph in Fig. 4.3, the IC has 14 pads for DC bias and RF inputs. The DC bias provided through HP 33150A (0.1 MHz - 18 GHz) and Wiltron K250 (50 KHz - 40 GHz) bias tees. All RF and DC ports are terminated with 50 Ω load. A more accurate description of the measurement system is shown in Fig. 4.5. Under operating conditions the ADC dissipates $\sim$ 1.5 W.

The output of the $\Sigma - \Delta$ modulator is connected to a microwave switch (HP 8762B) enabling the data stream to be analyzed with a digital sampling oscilloscope (Tektronix CSA 803) or a spectrum analyzer (HP 8590B). The sampling oscilloscope allows the eye-pattern of the output pattern to be observed on the screen. Since in our circuit, the output of the quantizer is directly available at the output, the jitter at the transitions between **1**s and **0**s gives an estimate of the metastability in the quantizer. A representative eye-pattern obtained for the $\Sigma - \Delta$ modulator clocked at 18 GHz is shown in Fig. 4.6. The eye-pattern demonstrates a scope-limited timing jitter of 7 ps. However, for some inputs to the $\Sigma - \Delta$ modulator, the output demon-

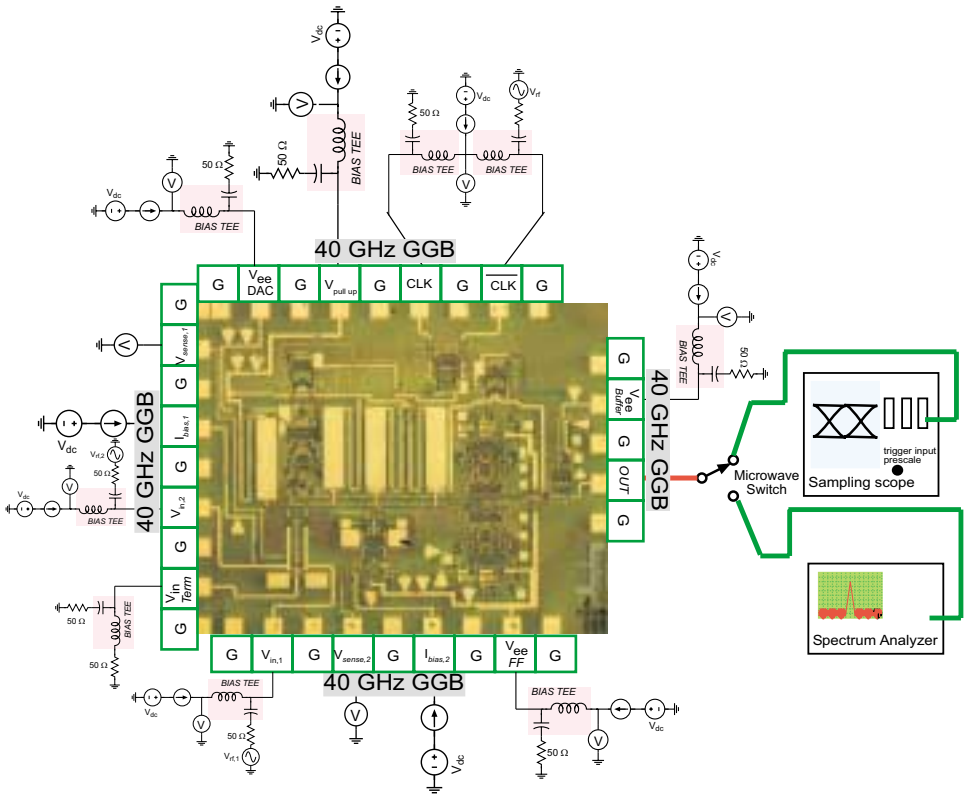

Figure 4.5: A detailed description of the setup used for testing the $\Sigma - \Delta$ modulator.

strated significant timing jitter ($\approx$ 20 ps) suggesting significant increase in metastability in the master-slave flip-flop .

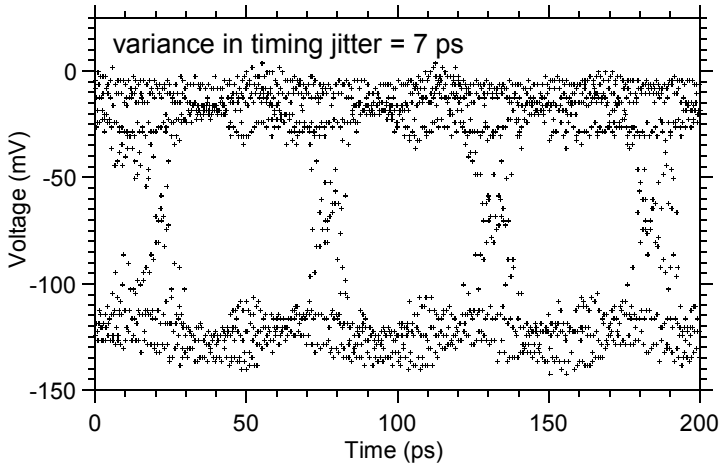

Figure 4.6: An eye-pattern of the digital output of the $\Sigma - \Delta$ modulator sampled at 18 GHz. For this measurement, the effective load at the input was the oscilloscope in parallel with the spectrum analyzer, leading to a reduced voltage swing.

All the measurements with the spectrum analyzer (HP 8590B) used a resolution bandwidth (RBW) of 10 kHz and a video bandwidth (VBW) of 10 kHz. Under these conditions, the instrument had a noise figure of $\sim$ 45 dB. This elevates the noise floor of the instrument to -128.8 dBm (= -173.8 + 45) in 1Hz. Since, this is higher than the noise floor expected from the $\Sigma - \Delta$ modulator, we used high-gain low-noise amplifiers along with switched attenuators at the input to the spectrum analyzer to obtain a low noise-figure receiver. The following section explains the technique used to estimate the *SNR* for the ADC.

4.2 Measurement Technique

Fig. 4.7 explains the setup used for measuring the signal and distortion components in the ADC output. The ADC is driven with two-tone signals from two synthesizers phase-locked to a common 10 MHz reference. Another

synthesizer phase-locked to the same 10 MHz reference generates the 18 GHz clock for sampling. The output is received by the spectrum analyzer after a 40 dB attenuation and an amplification with a high-gain low noise-figure amplifier chain (composed of 2 amplifiers ZFL 1000LN from Mini-circuits).

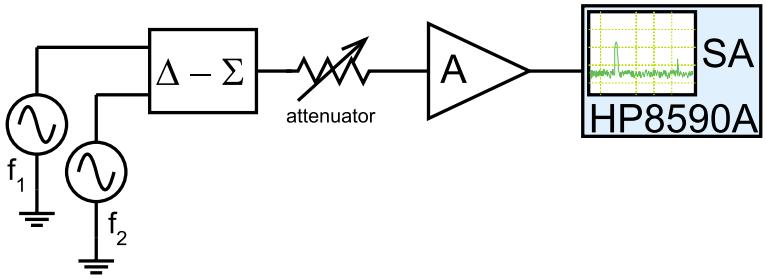

Figure 4.7: Setup used for measuring the signal and distortion components at the output of the $\Sigma - \Delta$ modulator.

Consider for example the output of the $\Sigma - \Delta$ modulator corresponding to a large input power as shown in Fig. 4.8. The raw power read by the spectrum analyzer in any of the signal tones (f_1 or f_2) is $P_{sig,raw}$ = -5.8 dBm. Taking into account the gain A of the amplifiers and the attenuation (-40 dB) of the attenuator, the corrected signal power at the output of the $\Sigma - \Delta$ modulator is $P_{sig,corr}$ = (-5.8 - A + 40) dBm = (34.2 - A) dBm.

For the measurement of the noise floor, the attenuator is removed from the path and the input signal powers are brought down sufficiently (to ensure that the amplifiers which receive higher power levels now, do not saturate). This is shown in Fig. 4.9. The setup continues to use the same amplification at the input to the spectrum analyzer.

Fig. 4.10 shows the raw output of the $\Sigma - \Delta$ modulator as measured by the spectrum analyzer when the input to the modulator is reduced by 46 dB. Ignoring the power in the signal components, we can observe the noise floor in a 40 kHz RBW is $P_{noise,raw}$ = -58 dBm. The corrected noise floor at the output of the $\Sigma - \Delta$ modulator is $P_{noise,corr}$ = (-58 + A) dBm (in 40 kHz).

With these two measurements, we can estimate the *SNR* of the modulator as

$$SNR = P_{sig,corr}\ (\text{dB}) - P_{noise,corr}\ (\text{dB}) = (34.2+58)\text{dB (in 40 kHz)} \quad (4.1)$$

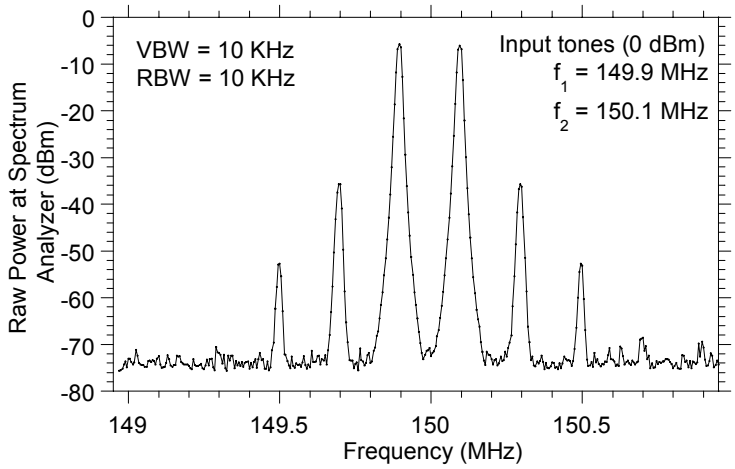

Figure 4.8: The output of the $\Sigma - \Delta$ modulator measured with the setup shown in Fig. 4.7.

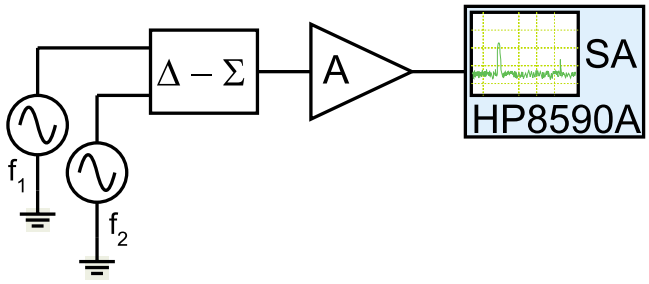

Figure 4.9: Setup used for measuring the noise-floor at the output of the $\Sigma - \Delta$ modulator.

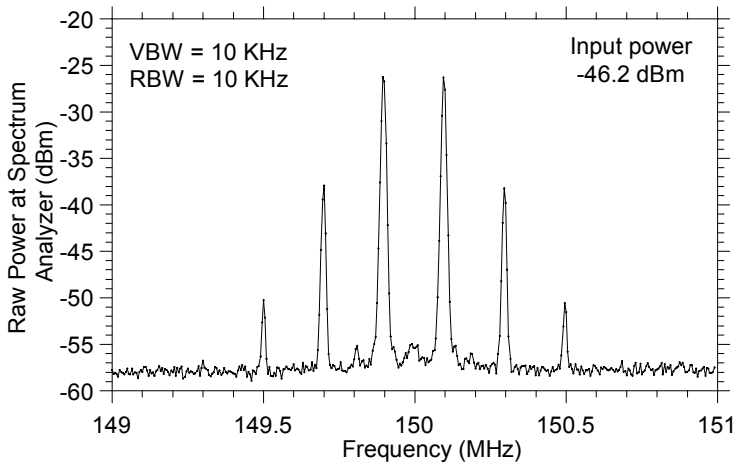

Figure 4.10: The output of the $\Sigma - \Delta$ modulator measured with the setup shown in Fig. 4.9.

$$SNR \ = 92.2\text{dB (in 40 kHz)} = 138\text{dB (in 1 Hz)} \tag{4.2}$$

This measurement technique assumes the fact that the logarithmic-amplifier in the spectrum analyzer display is precise with a 140 dB dynamic range. This assumption was independently verified by measuring the output from a calibrated noise source using the setup in Fig. 4.9. A similar measurement was performed for the signals from a known signal source using the setup in Fig. 4.7.

4.3 $\Sigma - \Delta$ ADC performance

The performance of the ADC was measured at signal frequencies of 150 MHz, 500 MHz and 990 MHz using the technique described above. The two-tone measurements were performed using frequencies separated by 0.2 MHz at each of the frequencies. The resulting third-order distortion components ($(2f_1 - f_2)$ and $(2f_2 - f_1)$) are at a further 0.2 MHz separation from each fundamental frequency component. Thus, the distortion components can be observed on the spectrum analyzer with a small frequency span. Figs. 4.11 - 4.13 show a plot of the output signal and distortion powers in one

of the two signal tones plotted along with the measured noise-floor as a function of the input signal power. Using the signal output power in only one of the two tones, the *SNR* obtained is 48 dB, 42 dB and 33 dB in 150 MHz, 500 MHz and 990 MHz bandwidths, respectively. The *SNR* obtained in the 150 MHz bandwidth is $\approx$ 25 dB lower than expected from MATLAB simulations. This is due to the fact that the $\Sigma - \Delta$ modulator does not provide any noise shaping below an input frequency of $\sim$ 1 GHz. This is clearly demonstrated in Fig. 4.14 which shows a spectrum analyzer sweep from DC to $\sim$ 3 GHz. The instrument used for this purpose was HP 70900 series spectrum analyzer.

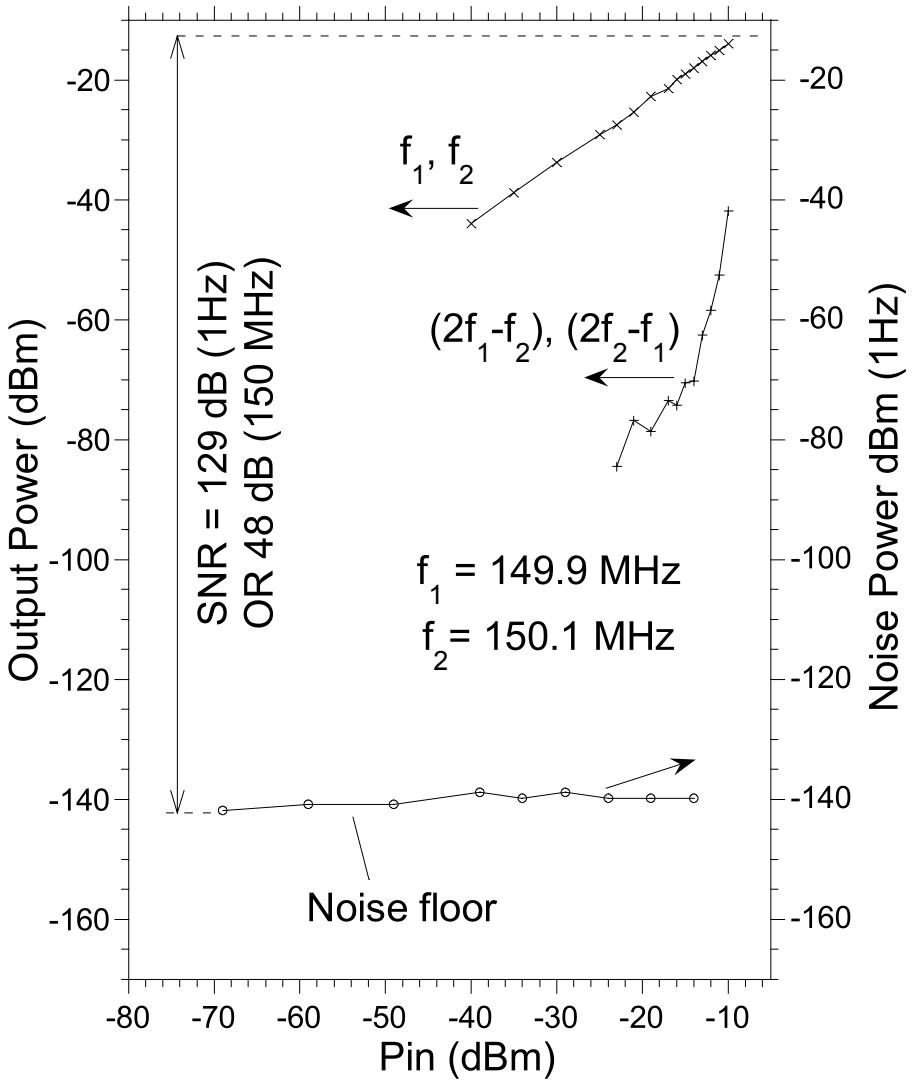

Figure 4.11: Results of the two-tone measurement at 150 MHz. The ADC can achieve 48 dB *SNR* in a 150 MHz bandwidth.

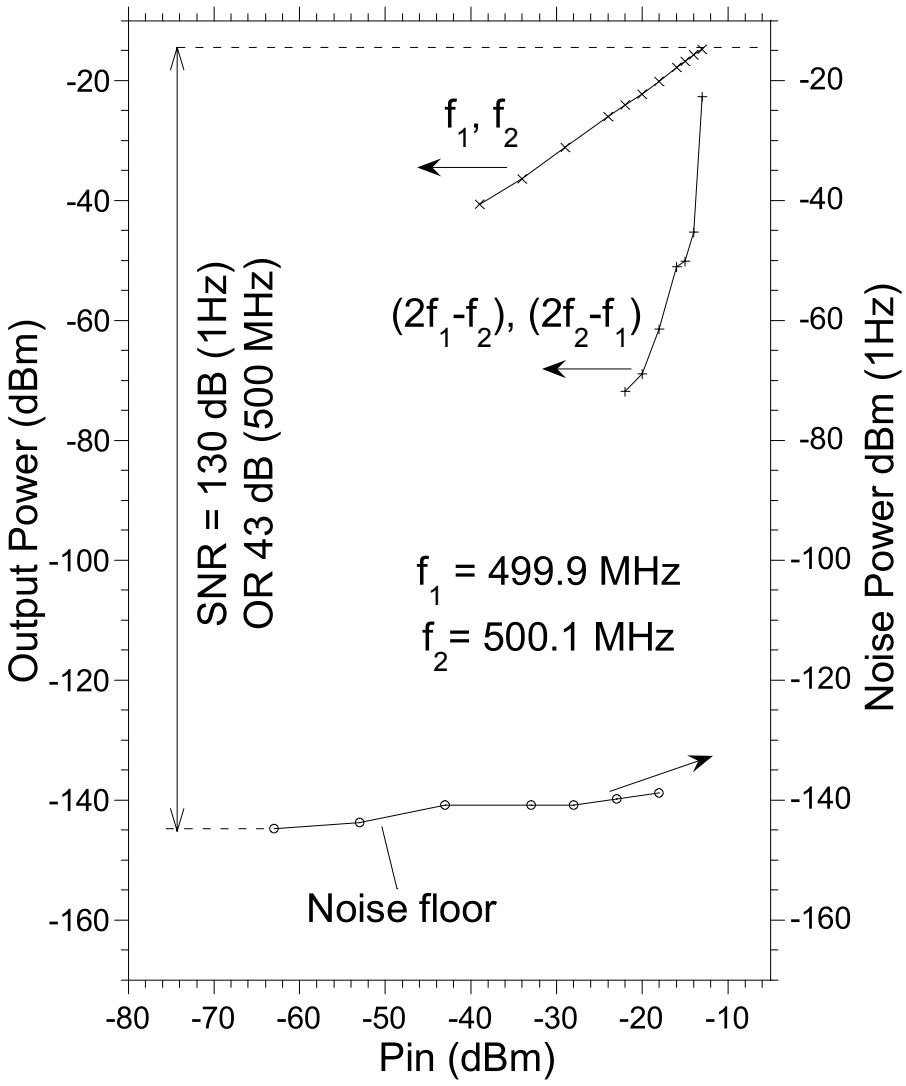

Figure 4.12: Results of the two-tone measurement at 500 MHz. The ADC can achieve 42 dB *SNR* in a 500 MHz bandwidth.

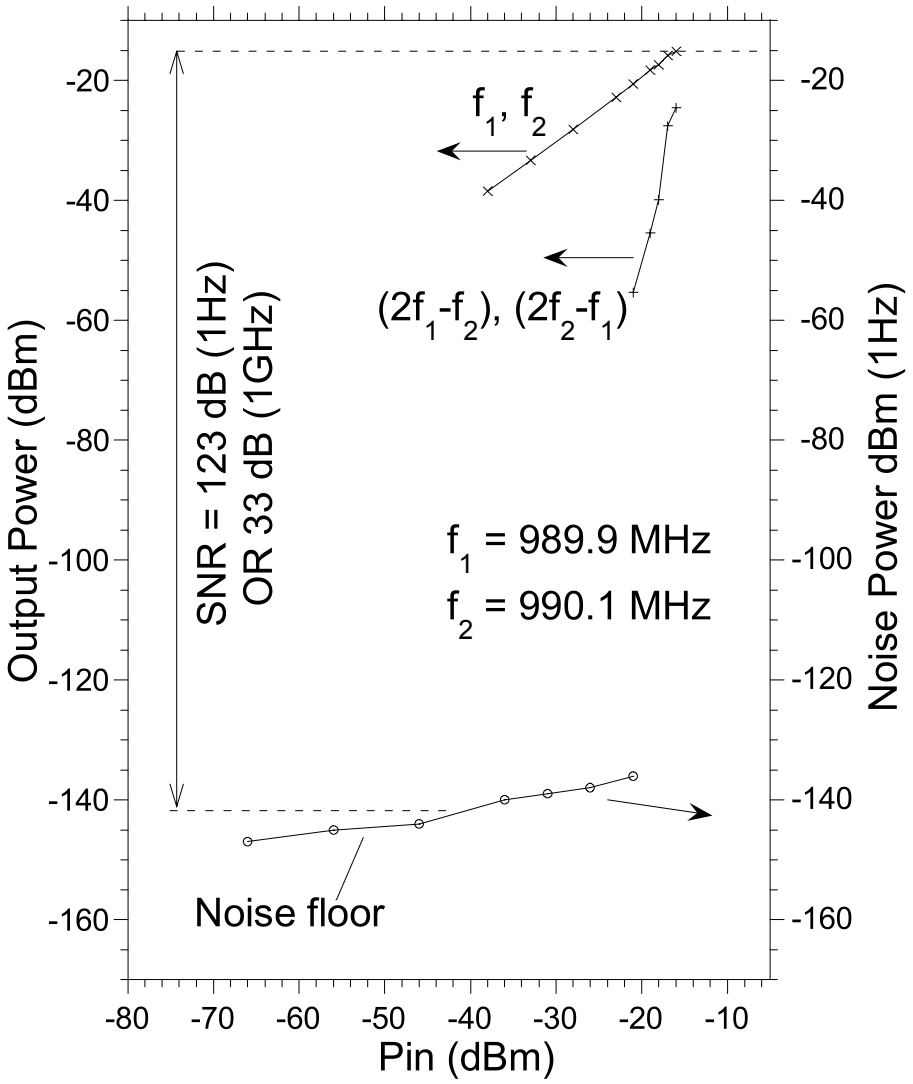

Figure 4.13: Results of the two-tone measurement at 990 MHz. The ADC can achieve $\sim$ 33 dB *SNR* in a 1 GHz bandwidth.

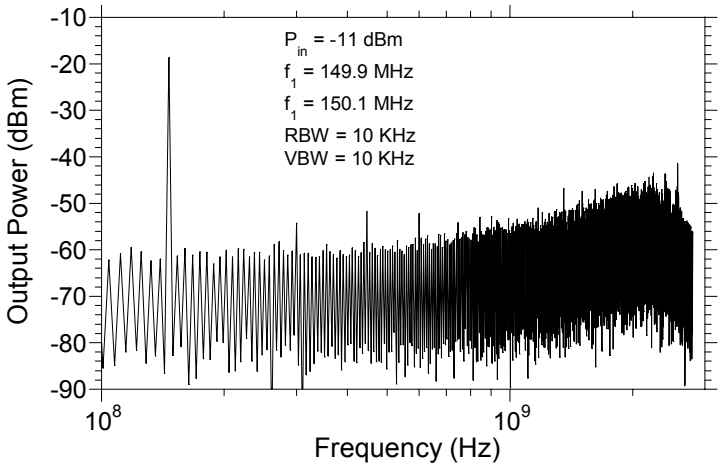

Figure 4.14: A DC - 2.8 GHz span of the $\Sigma-\Delta$ modulator output spectrum for a two-tone input at 150 MHz.

The other fact to be observed from the Figs. 4.11 - 4.13 is that the third order distortion components rise at a slope greater than 3. This is consistent with our design objective of the loop linearity being decided by the loop components rather than by the input stage. The distortion term is obtained by the contribution to $(2f_1 - f_2)$ and $(2f_2 - f_1)$ terms in the Taylor series representation of the output.

$$V_{out} = f_1(V_{in}) + f_3(V_{in}^3) + f_5(V_{in}^5) + \cdots \tag{4.3}$$

Under two-tone test conditions, the input voltage V_{in} consists of the tones f_1 and f_2. Thus the contribution to the third order distortion terms $(2f_1 - f_2)$ and $(2f_2 - f_1)$ results from $f_3(V_{in}^3)$ and higher order terms. In a simple circuit like a transconductance stage, the contribution from the third order term $f_3(V_{in}^3)$ usually dominates leading to a slope of 3 for the distortion term plotted on a logarithmic scale.

In the $\Sigma-\Delta$ modulator, if the loop gain is high, the input output transfer characteristics are close to that of an ideal limiter, with maximum input $V_{in,max} = I_{dac}/g_{m1}$. An ideal limiter must be described by a Taylor series in which the 5^{th}, 7^{th} and higher order terms are significant. The two-tone intermodulation is strongly affected by these terms and the $(2f_1 - f_2)$ and $(2f_2 - f_1)$ amplitudes are not proportional to V_{in}^p where $p > 3$.

Next we describe the method to obtain the resolution of a Nyquist rate ADC with similar performance. This will allow us to describe the $\Sigma - \Delta$ modulator performance in effective number of bits.

the term $f_3(V_{in}^3)$ In single tone testing, for a Nyquist-rate ADC, the number of bits of resolution (N) and the *SNR* are related by [4]

$$SNR(dB) = 6.02N + 1.76 \tag{4.4}$$

$$N = [SNR(dB) - 1.76]/6.02 \tag{4.5}$$

For single-tone testing, a Nyquist ADC with maximum input $\pm v_{max}$ can have a maximum single-tone input amplitude of $v_{in} = v_{max}cos(\omega_1 t)$, while for two-tone testing, the maximum input is $v_{in} = (v_{max}/2)cos(\omega_1 t) + (v_{max}/2)cos(\omega_2 t)$. Thus, the maximum signal power at ω_1 in two-tone testing is 6dB below that in single-tone testing. Under two-tone testing, a Nyquist-rate ADC has

$$\begin{aligned} SNR(dB) &= 6.02N + 1.76 - 6 \\ &= 6.02N - 4.24 \\ N &= [SNR(dB) + 4.24]/6.02 \end{aligned} \tag{4.6}$$

Thus, the 33 dB SNR (990 MHz signal) for the $\Sigma - \Delta$ ADC is equivalent in performance to a 1.98 GS/s Nyquist-rate ADC with 6.2 effective number of bits (ENOB) resolution (Eq. 4.6). The measured *SNR* with ENOB resolution is presented in Table 4.1.

Table 4.1: *SNR* and the ENOB of an equivalent Nyquist-rate ADC at different signal frequencies (obtained using Eq. 4.6).

frequency	Measured *SNR*	ENOB resolution
150 MHz	48 dB	8.7
500 MHz	42 dB	7.7
990 MHz	33 dB	6.2

4.4 SPICE simulation of the entire loop

Improvement in computing techniques and simulation software during the course of this work enabled us to setup the SPICE simulation of the entire $\Sigma - \Delta$ modulator loop. HP ADS 1.3 was used for this purpose and the simulation used a single tone input at 78.125 MHz while a clock frequency of 20 GHz was used to obtain an OSR of 128. The parasitics in the device as well as in the layout were extracted to get a reasonable approximation to the actual fabricated circuit. The *FFT* of the output is shown in Fig. 4.15. It can be noted from the figure that the $\Sigma - \Delta$ modulator loop shows a noise-floor that flattens below $\sim$ 1 GHz. This seems to verify our experimental observation. The MATLAB simulation (Fig. 4.16) of the entire loop using the layout parameters does not demonstrate this fact. The noise shaping extends all the way down to about $\sim$ 100 MHz.

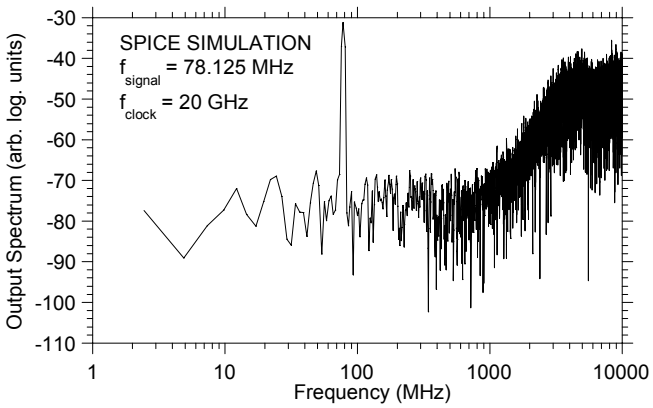

Figure 4.15: Output spectrum obtained from SPICE simulation of the complete $\Sigma - \Delta$ ADC loop using layout parameters.

Preliminary investigation of the reason for the lack of noise-shaping is currently under investigation. Though more systematic and organized approach is needed, we suspect that the metastability and dynamic hysteresis errors in the quantizer may be responsible to some extent for the lack of noise-shaping. To test this hypothesis, the SPICE simulation was idealized somewhat by placing a high gain preamplifier at the input to the quantizer. The resulting output spectrum is shown in Fig. 4.17, which demonstrates noise-shaping down to $\sim$ 300 MHz. More time and effort is needed to ensure that the translation of circuit parameters from MATLAB designs to

implementation in circuits is correct.

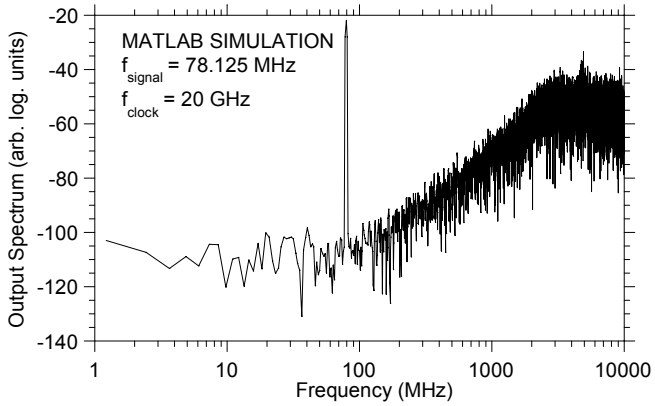

Figure 4.16: Output spectrum obtained from MATLAB simulation of the complete $\Sigma - \Delta$ ADC loop using layout parameters.

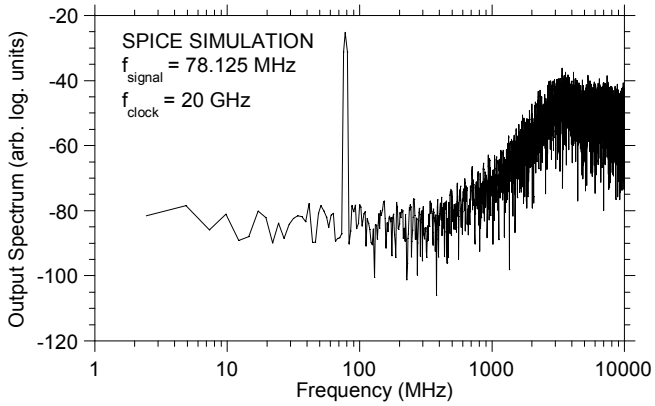

Figure 4.17: Output spectrum obtained from SPICE simulation of the complete $\Sigma - \Delta$ ADC loop using layout parameters - The ADC is somewhat idealized by introduction of a high gain preamplifier at the input to the quantizer.

Chapter 5

Conclusion

5.1 Summary of Achievements

This work has demonstrated a working $\Sigma - \Delta$ modulator IC which allows a clock rate of 18 GHz. The high clock rate allows the $\Sigma - \Delta$ modulator to achieve a good performance even at signal levels as high as 1 GHz. The ADC achieves 6.2 bits of resolution at 990 MHz, 7.7 bits at 500 MHz and 8.7 bits at 150 MHz.

The expression for the *SNR* that can be achieved with an ideal second order $\Sigma - \Delta$ modulator in terms of the *SNR* ($SNR_{Nyquist}$) of the Nyquist rate ADC using the same quantizer is (Eq. 22 of [5])

$$SNR_{ideal} = SNR_{Nyquist} - 10.\log_{10}\left(\frac{\pi^4}{5}\right) + 50.\log_{10}(OSR)(\text{ dB}) \quad (5.1)$$

A Nyquist rate ADC with 1 bit quantizer has $SNR_{Nyquist} = 7.76$ dB (Eq. 2.6). Thus, the Eq. 5.1 reduces to

$$\begin{aligned} SNR_{ideal} &= 7.76 - 10.\log_{10}\left(\frac{\pi^4}{5}\right) + 50.\log_{10}(OSR)(\text{ dB}) \\ &= -5.14 + 50.\log_{10}(OSR)(\text{ dB}) \end{aligned}$$

This can be translated to the effective number of bits of an equivalent Nyquist rate ADC by using Eq. 4.5.

$$\begin{aligned} N_{ideal} &= [-5.14 + 50.\log_{10}(OSR) - 1.76]/6.02 \\ &= [-6.9 + 50.\log_{10}(OSR)]/6.02 \end{aligned}$$

The effective number of bits resolution of the equivalent Nyquist rate ADC expected from an ideal second order $\Sigma - \Delta$ modulator is compared with the resolution obtained from the $\Sigma - \Delta$ modulator fabricated in Table 5.1.

Table 5.1: *SNR* and the ENOB of an equivalent Nyquist-rate ADC at different signal frequencies compared with the expected ideal values.

frequency	Sample rate for Nyquist rate ADC	*OSR*	ENOB resolution obtained	Ideal ENOB resolution expected
150 MHz	300 MS/s	60	8.7	13.6
500 MHz	1GS/s	18	7.7	9.3
990 MHz	1.98 GS/s	9	6.2	6.7

From the table above, it is clear that the $\Sigma - \Delta$ ADC performance obtained at lower signal bandwidths is significantly below that expected from an ideal $\Sigma - \Delta$ ADC. The performance at a signal frequency of 990 MHz is very close to that expected from an ideal converter.

From the point of view of technology development, this work demonstrates an IC with more than 100 transistors in transferred-substrate HBT process for the first time. The ability to successfully yield a 150 transistor IC should inspire confidence in future endeavors in complex IC design and fabrication. Several processing problems were encountered in the fabrication procedures. The interconnect density on Metal-2 layer severely affected the initial fabrication attempt. Another limit to device density was the minimum-size and aspect-ratio restrictions on the BCB vias for ground contacts. Process and design-rule improvements were implemented to overcome these problems (described in Appendix B).

5.2 Suggestions for future IC designs

The most significant limitation of the current devices in transferred-substrate HBT process is their low breakdown voltages. This necessitates a large num-

ber of diodes in the circuit to ensure protection from breakdown. While this reduces the yield due to the sheer transistor count in the circuit, the working circuits are slower due to the capacitance of the diodes due to the thermal-via.

There is effort currently aimed at a transition to InP collector devices in the transferred substrate HBT technology. When fully implemented, the InP based device technology has the potential of implementing more complex circuits while using fewer transistors. In the $\Sigma - \Delta$ ADC, for example, the input stage could be designed to have a more complex Caprio's cell which may significantly improve the linearity of the ADC. The elimination of diodes as breakdown protection devices with result in lower transistor count increasing the circuit yield. Another advantage of the InP collector is the better thermal conductivity of InP relative to InGaAs. The $\Sigma - \Delta$ modulator circuit designed here dissipates 1.5 W. An InP collector will improve the thermal performance of the circuit improving the reliability.

The future work in $\Sigma - \Delta$ modulator needs to develop a good SPICE simulation technique which allows prediction of the circuit performance before fabrication. This will allow analysis of the effect of quantizer metastability on the circuit performance, a factor which is difficult to simulate with MATLAB. The next generation circuit will have to take into account the noise and distortion contribution from the input stage. This will allow an ADC design with a high dynamic range as well as a high *SNR* . With improvement in process technology to favor high integration levels and incorporation of SPICE simulation tools, design of higher order modulators will become feasible.

Appendix B

Process Improvements

The following process related problems were identified during the course of this work.

- Interconnect pitch : The interconnects Metal-1 and Metal-2 are defined by a lift-off process using the photoresist AZ5214. Severe problems associated with resist adhesion were encountered. These lead to smearing of the interconnects. The problem was particularly severe in the case of fine pitched features in Metal-2 (Fig. B.1).

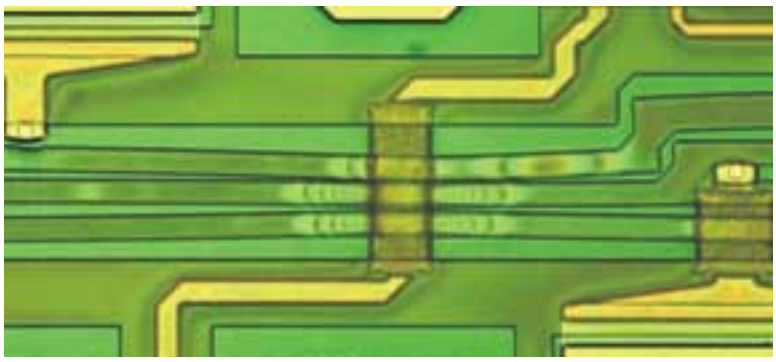

Figure B.1: Chip photograph showing the adhesion problem in the photoresist for Metal-2.

  The problem was circumvented by changing the design rules to increase the interconnect pitch. The improvement is depicted in Fig. B.2.

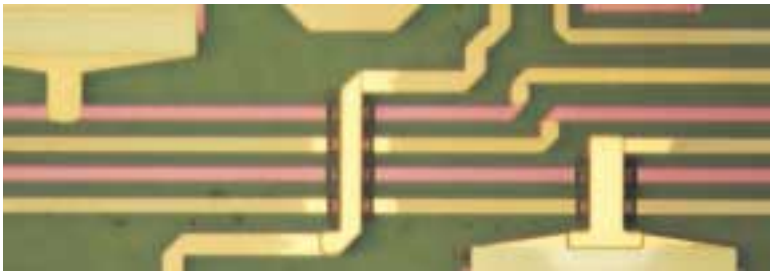

Figure B.2: Chip photograph showing the improved interconnect definition in Metal-2 layer.

- Adhesion of the nichrome resistors: The integrated circuit yield depends critically on the adhesion of nichrome resistors. The original circuit process has nichrome resistors defined on the semiconductor. The substrate removal etch exposes the resistors to HCl solution. On some occasions, the NiCr film peels off at places on the wafer even before the substrate removal (Fig. B.3). The solution to this problem is to protect the nichrome from exposure to HCl by using SiN (Fig. B.4).

- BCB via process: When this work was initiated, the ground vias in benzo-cyclo-butene (BCB) were defined by transferring the pattern from photoresist to BCB using a dry etch. This procedure sufficed to yield an integrated circuit with < 100 transistors. The main limitations of this process were the roughness left on the BCB surface at the end of the etch and the difference between the via size on the wafer from that on the mask. This problem is demonstrated in the SEM picture (Fig. B.5) of 4 μm $\times$ 4 μm BCB via.

  The problem was solved by using a low-temperature-PECVD-deposited SiN to transfer the pattern to the BCB etch. A 1:10 selectivity in SiN:BCB etch rates allows the BCB surface to remain reasonably smooth while even the smallest vias have well defined edges (Fig. B.6).

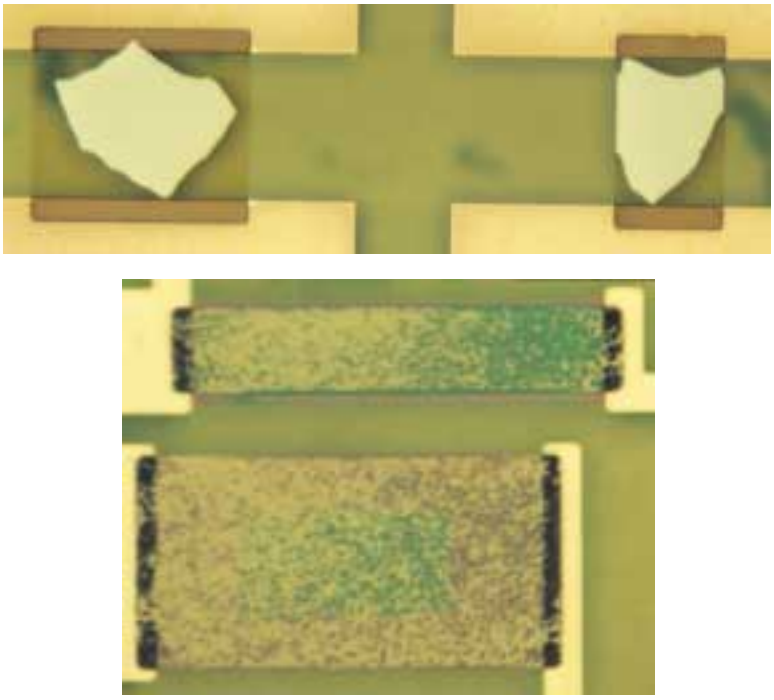

Figure B.3: Chip photograph showing the resistors with the surface showing signs of attack from HCl etch or peeling off.

Figure B.4: Chip photograph showing the resistors protected with SiN.

Figure B.5: SEM photograph showing the surface roughness and distorted via edges in BCB.

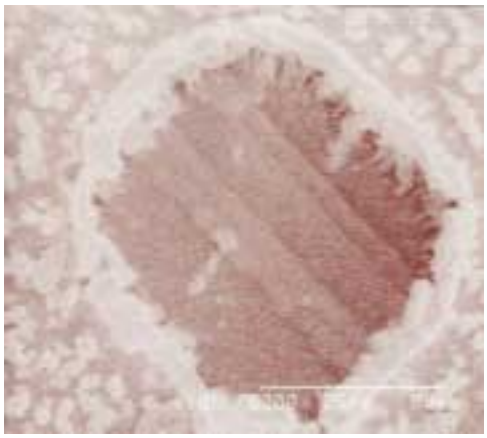

Figure B.6: SEM photograph showing the reduced surface roughness of BCB with better defined vias.

Appendix C

Device Rule Checker code

The following is the code used to implement the device rule checker (DRC) in HP ADS.

```
// declare input design layers
decl Emitter = dve_import_layer(‘‘Emitter’’);
decl BaseCont = dve_import_layer(‘‘BaseCont’’);
decl BaseMesa = dve_import_layer(‘‘BaseMesa’’);
decl PolyEtch = dve_import_layer(‘‘PolyEtch’’);
decl Resistors = dve_import_layer(‘‘Resistors’’);
decl Metal_1 = dve_import_layer(‘‘Metal-1’’);
decl SiNEtch = dve_import_layer(‘‘NitrideEtch’’);
decl Metal_2 = dve_import_layer(‘‘Metal-2’’);
decl BCBEtch = dve_import_layer(‘‘BCBetch’’);
decl Collector = dve_import_layer(‘‘Collector’’);
decl Collector_shrunk = dve_import_layer(‘‘Collector-Shrunk’’);

// declare some output layers
decl lyr_error1 = dve_export_layer(101);
decl lyr_error2 = dve_export_layer(102);
decl lyr_error3 = dve_export_layer(103);

// declare some derived layers
decl work1,work2,work3,work4,work5,work6,work7,work8,work9,work10;
//these are derived layers,
// that do not map to a real
// process layer
```

```
//------------EMITTER RULES-------------------------

//
// Emitter should be enclosed in PolyEtch
//
work1 = dve_bool_and(PolyEtch,Emitter);
work2 = dve_bool_not(Emitter,work1);
work3 = dve_bool_not(work1,Emitter);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error1 += dve_drc( all_edges(work5),
``PolyEtch does not cover emitter fully'');

lyr_error1 += dve_drc( contains(PolyEtch,Emitter) < 3,
``PolyEtch edge to emitter < 3 um'');

//
// Emitter should be enclosed in BaseCont
//
work1 = dve_bool_and(BaseCont,Emitter);
work2 = dve_bool_not(Emitter,work1);
work3 = dve_bool_not(work1,Emitter);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error2 += dve_drc( all_edges(work5),
``BaseCont does not cover emitter fully'');

lyr_error2 += dve_drc( contains(BaseCont,Emitter) < 0.5,
``BaseCont edge to emitter < 0.5 um'');

//
// Emitter should be enclosed in BaseMesa
```

```
//
work1 = dve_bool_and(BaseMesa,Emitter);
work2 = dve_bool_not(Emitter,work1);
work3 = dve_bool_not(work1,Emitter);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error3 += dve_drc( all_edges(work5),
``BaseMesa does not cover emitter fully'');

lyr_error3 += dve_drc( contains(BaseMesa,Emitter) < 0.5,
``BaseMesa edge to emitter < 0.5 um'');

//
// Emitter should be enclosed in Collector
//
work1 = dve_bool_and(Collector,Emitter);
work2 = dve_bool_not(Emitter,work1);
work3 = dve_bool_not(work1,Emitter);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error1 += dve_drc( all_edges(work5),
``Collector does not cover emitter fully'');

lyr_error1 += dve_drc( contains(Collector,Emitter) < 0.2,
``Collector edge to emitter < 0.2 um'');

//------------BASECONT RULES-------------------------
//
// BaseCont should be enclosed in BaseMesa
//
work1 = dve_bool_and(BaseMesa,BaseCont);
work2 = dve_bool_not(BaseCont,work1);
work3 = dve_bool_not(work1,BaseCont);
```

```
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error1 += dve_drc( all_edges(work5),
``BaseMesa does not cover BaseCont fully'');

//------------POLYETCH RULES-------------------------
//
// Detemining PolyEtch to BaseCont via rules :
//
// Assuming PolyEtch has an opening on BaseCont:
// Derive the overlap of BaseCont with Metal-1
// and PolyEtch.  Subtract the the overlaps (like XOR).
// AND this with Metal1 to get size of opening.

work1 = dve_bool_and(PolyEtch,BaseCont);
work2 = dve_bool_not(BaseCont, work1);

work3 = dve_bool_and(work2, Metal_1);

lyr_error1 += dve_drc( width(work3) < 4,
``PolyEtch via for BaseCont - 4 um minimum'');

work4 = dve_drc(poly_inter_layer(work2,Metal_1),
DVE_RN_INTER_SELECT, DVE_RV_ACCEPT,
DVE_RN_INTER_CODE, DVE_RV_OUTSIDE_ONLY,
DVE_RN_INTER_CODE, DVE_RV_OUTSIDE_TOUCH);
lyr_error2 += dve_drc( all_edges(work4),
``Metal_1 contact for BaseCont does not exist'');

//
// If PolyEtch has no opening on BaseCont
// find out if it encloses BaseCont completely.
//
work5 = dve_drc(poly_inter_layer(PolyEtch,BaseCont),
DVE_RN_INTER_SELECT, DVE_RV_ACCEPT,
```

```
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_ONLY,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_TOUCH);

lyr_error3 += dve_drc( all_edges(work5),
``PolyEtch via for BaseCont does not exist'');

work6 = dve_bool_and(Metal_1,Collector);
work7 = dve_bool_and(work6,PolyEtch);
lyr_error3 += dve_drc( contains(PolyEtch,work7) < 4,
``PolyEtch edge from Metal-1 and Collector crossover less than 4
um'');

work8 = dve_bool_and(Metal_2,Collector);
work9 = dve_bool_and(work6,PolyEtch);
lyr_error3 += dve_drc( contains(PolyEtch,work7) < 2,
``PolyEtch edge from Metal-2 and Collector crossover less than 2
um'');

//------------RESISTORS RULES-------------------------
//location of Resistors relative to PolyEtch
work1 = dve_bool_and(Resistors,PolyEtch);
lyr_error1 += dve_drc( width(work1) > 0,
``Resistors are sitting on Polyimide'');

lyr_error1 += dve_drc( external(Resistors,PolyEtch) < 2,
``Resistors are closer to Polyimide than 2 um'');

// Extension of Metal-1 beyond Resistor edge
lyr_error2 += dve_drc( contains(Metal_1,Resistors) < 0.5,
``Metal-1 extension from NiCr resistor edges is less than 0.5 um'',
DVE_RN_EDGE_ANGLES, DVE_RV_PARALLEL);

//Intrusion of NiCr Resistors into Metal-1
lyr_error2 += dve_drc( internal(Resistors,Metal_1) < 2,
``NiCr resistor intrusion into Metal-1 is less than 2 um'',
DVE_RN_EDGE_ANGLES, DVE_RV_PARALLEL);
```

```
//Width of Resistors
work3 = dve_bool_not(Resistors,Metal_1);
work4 = dve_drc(poly_path_length(work3) < 5,
DVE_RN_PATH_CODE, DVE_RV_BIT,
DVE_RN_PATH_LENGTH, DVE_RV_MIN_PATH);

lyr_error3 += dve_drc( all_edges(work4),
``NiCr resistor width is less than 5 um'');

//Length of Resistors
work5 = dve_bool_and(Resistors,Metal_1);
lyr_error3 += dve_drc( spacing(work5) < 4,
``NiCr Resistor length is less than 4.0 um'');

//------------METAL1 RULES-------------------------
lyr_error1 += dve_drc( width(Metal_1) < 2,
``Metal-1 width less than 2 um'');

lyr_error2 += dve_drc( gap(Metal_1) < 4,
``Metal-1 to Metal-1 spacing < 4 um'');

//------------SILICON NITRIDE RULES-------------------------
work1 = dve_bool_and(Metal_1,SiNEtch);
work2 = dve_bool_not(SiNEtch,work1);
work3 = dve_bool_not(work1,SiNEtch);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error1 += dve_drc( all_edges(work5),
``Metal-1 does not cover Niride Etch vias fully'');

work6 = dve_drc(poly_inter_layer(Metal_1,SiNEtch),
DVE_RN_INTER_SELECT, DVE_RV_ACCEPT,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_ONLY,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_TOUCH);
```

```
lyr_error1 += dve_drc( contains(work6,SiNEtch) < 1,
‘‘Nitride Etch via inclusion in Metal-1 less than 1 um’’);

lyr_error2 += dve_drc( width(SiNEtch) < 3,
‘‘Niride Etch vias smaller than 3 um’’);

work1 = dve_bool_and(Metal_2,SiNEtch);
work2 = dve_bool_not(SiNEtch,work1);
work3 = dve_bool_not(work1,SiNEtch);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error3 += dve_drc( all_edges(work5),
‘‘Metal-2 does not cover Niride Etch vias fully’’);

//------------METAL2 RULES-------------------------
lyr_error1 += dve_drc( width(Metal_2) < 2,
‘‘Metal-2 width less than 2 um’’);

lyr_error2 += dve_drc( gap(Metal_2) < 4,
‘‘Metal-2 to Metal-2 spacing < 4 um’’);

//------------BCB NITRIDE RULES--------------------------
work1 = dve_bool_and(Metal_2,BCBEtch);
work2 = dve_bool_not(BCBEtch,work1);
work3 = dve_bool_not(work1,BCBEtch);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error1 += dve_drc( all_edges(work5),
‘‘Metal-2 does not cover BCB Etch vias fully’’);

lyr_error2 += dve_drc( width(BCBEtch) < 4,
‘‘BCB Etch vias smaller than 4 um’’);
```

```
work6 = dve_drc(poly_inter_layer(Metal_2,BCBEtch),
DVE_RN_INTER_SELECT, DVE_RV_ACCEPT,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_ONLY,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_TOUCH);

lyr_error3 += dve_drc( contains(work6,BCBEtch) < 4,
``BCBEtch via inclusion in Metal-2 less than 4 um'');

//------------COLLECTOR RULES-------------------------
work1 = dve_bool_and(Collector,Emitter);
work2 = dve_bool_not(Emitter,work1);
work3 = dve_bool_not(work1,Emitter);
work4 = dve_bool_or(work2,work3);
work5 = dve_drc(poly_line_length(work4) > 0,
DVE_RN_LINE_LENGTH, DVE_RV_MIN_LINE);

lyr_error1 += dve_drc( all_edges(work5),
``Collector does not cover emitter fully'');

lyr_error1 += dve_drc( contains(Collector,Emitter) < 0.2,
``Collector edge to emitter < 0.2 um'');

work1 = dve_bool_and(Collector,PolyEtch);
work2 = dve_bool_not(Collector, work1);

work3 = dve_bool_and(work2, Metal_1);

lyr_error1 += dve_drc( width(work3) < 4,
``Collector to Metal-1 overlap - 4 um minimum'');

work4 = dve_drc(poly_inter_layer(work2,Metal_1),
DVE_RN_INTER_SELECT, DVE_RV_ACCEPT,
DVE_RN_INTER_CODE, DVE_RV_OUTSIDE_ONLY,
DVE_RN_INTER_CODE, DVE_RV_OUTSIDE_TOUCH);

lyr_error2 += dve_drc( all_edges(work4),
``Metal_1 contact for Collector does not exist'');
```

```
//
// If PolyEtch has no opening on Collector
// find out if it encloses Collector completely.
//
work5 = dve_drc(poly_inter_layer(PolyEtch,Collector),
DVE_RN_INTER_SELECT, DVE_RV_ACCEPT,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_ONLY,
DVE_RN_INTER_CODE, DVE_RV_ENCLOSE_TOUCH);

lyr_error3 += dve_drc( all_edges(work5),
``PolyEtch via for Collector does not exist'');

//work6 = dve_bool_not(Collector,Collector_shrunk);
//lyr_error3 += dve_drc( width(work6) > 0,
// ``Collector after shrinkage not present everywhere'');
```

Appendix D

Schematic and Layout of the ADC circuit blocks

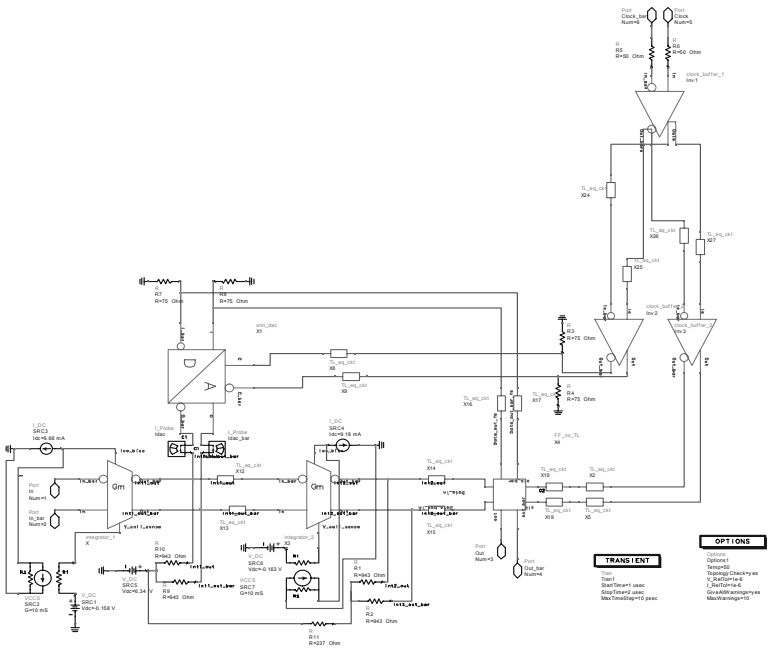

Figure D.1: Schematic of the complete ADC circuit

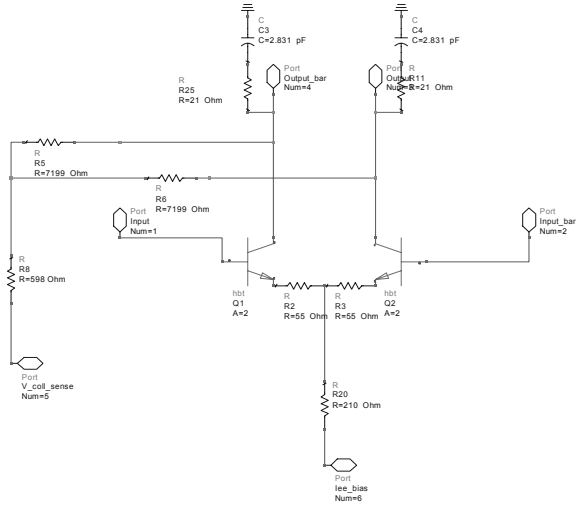

Figure D.2: Schematic of the input transconductance circuit

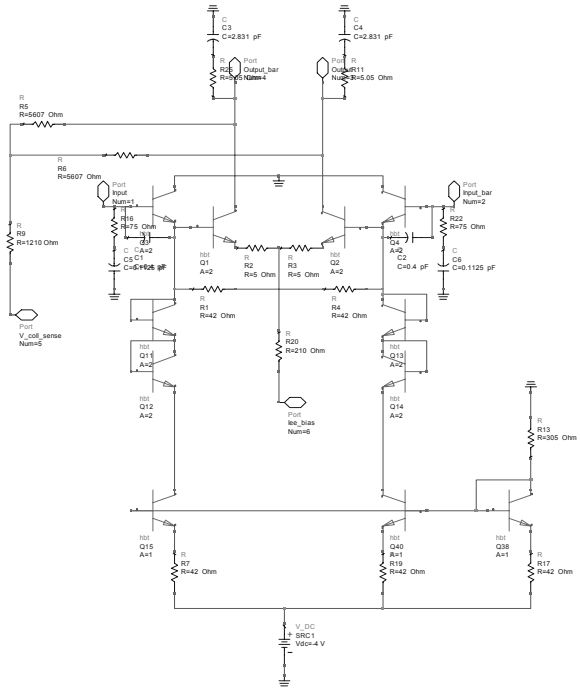

Figure D.3: Schematic of the second transconductance circuit

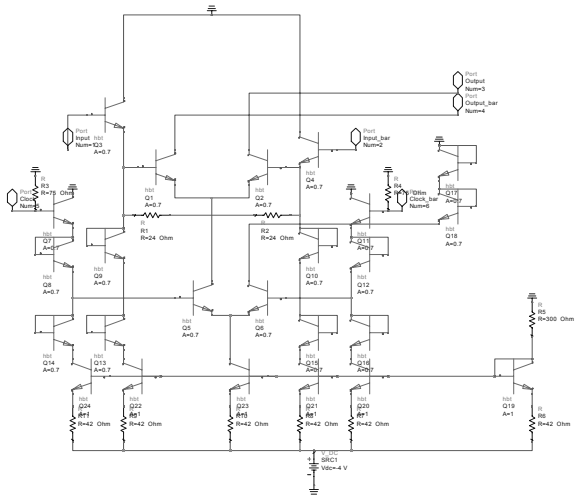

Figure D.4: Schematic of the DAC circuit

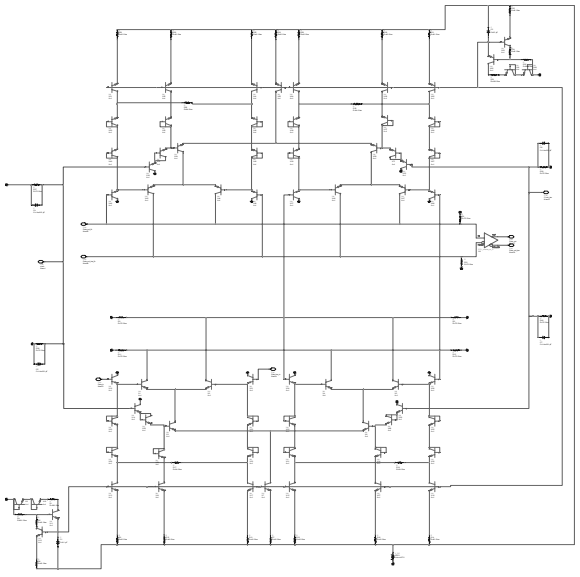

Figure D.5: Schematic of the flip-flop circuit

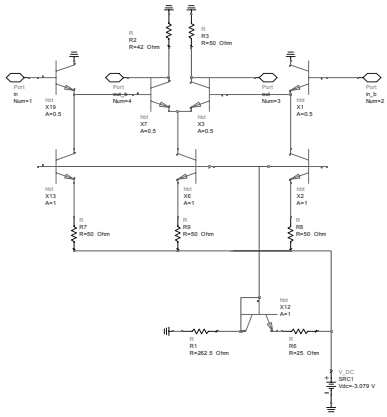

Figure D.6: Schematic of the output buffer

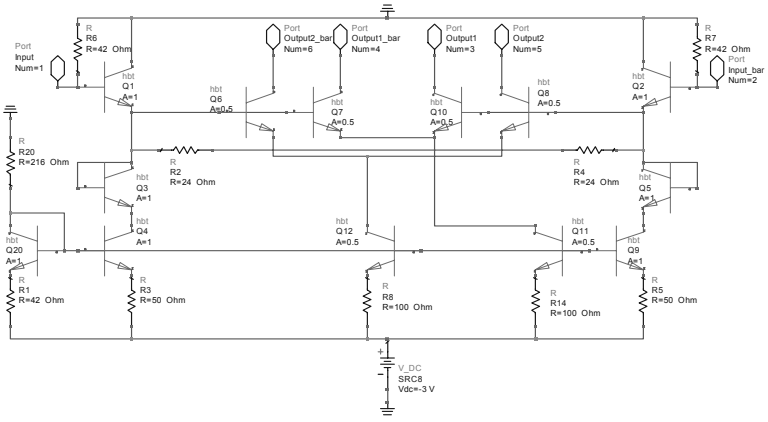

Figure D.7: Schematic of the clock buffer at the input

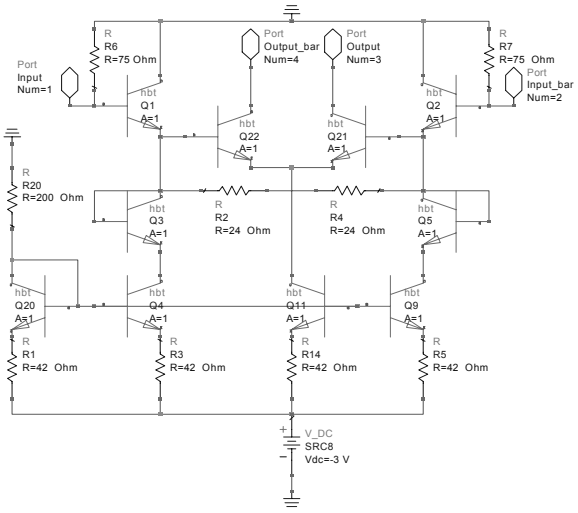

Figure D.8: Schematic of the clock buffer at the input to flip-flop and DAC

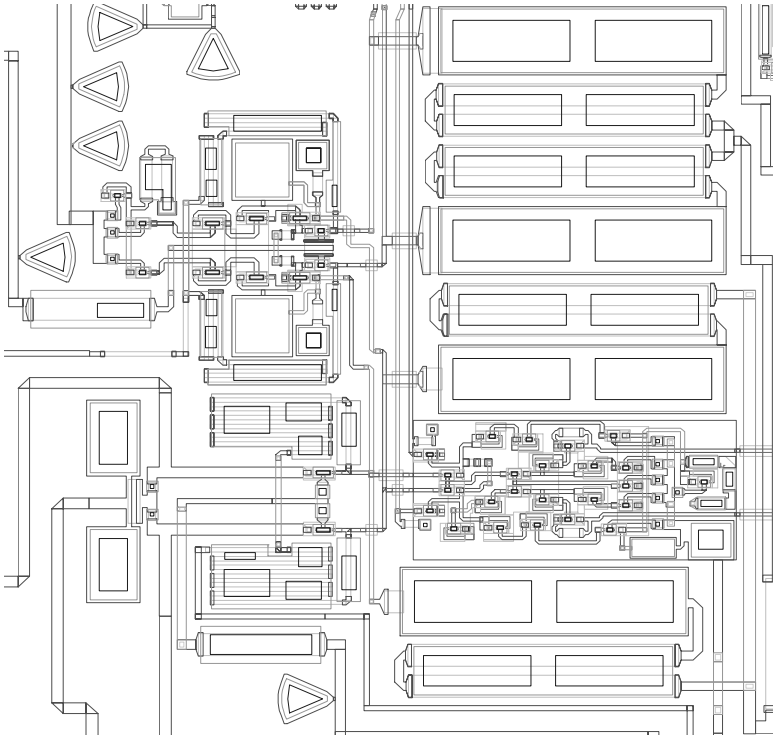

Figure D.9: Layout of a section of the ADC showing the two integrators and the DAC

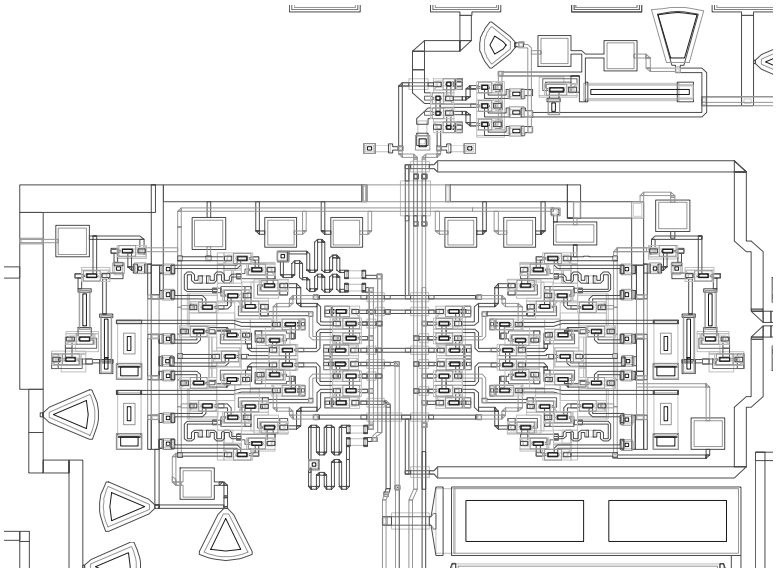

Figure D.10: Layout of a section of the ADC showing flip-flop and the output buffer

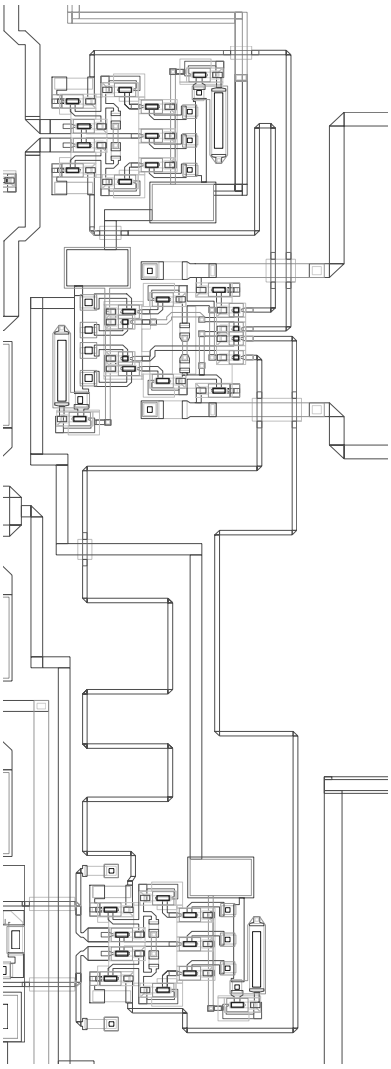

Figure D.11: Layout of a section of the ADC showing the clock buffers

Bibliography

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