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Metal Substrate Process and W-band Power Amplifier Integrated Circuits in Transferred-Substrate HBT Technology

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering
by
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March, 2000

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Acknowledgments

This work depended on the committed efforts of many others. First and foremost, my advisor, Professor Mark Rodwell had the vision and the courage to challenge the status quo of a device which did not scale. He remained committed to, and enthusiastic about, the metal substrate process even as my list of setbacks lengthened. His insight, enthusiasm, hard work, and concern for the best interests of his students will always remain an inspiration.

None of this work would have been possible without the contributions of my past and current lab-mates. Bipul Agarwal, Yoram Betser, Uddalak Bhattacharya, Shrinivasan Jaganathan, Karthikeyan Krishnamurthy, Michelle Lee, Thomas Mathew, Dino Mensa, Rajasekhar Pullela, Girish Ramesh, Madhukar Reddy, Dennis Scott, Lorene Samoska, P.K. Sundararajan, Miguel Urteaga and Yun Wei: all have helped me in too many ways to count. For your help and friendship I am grateful.

Last, but certainly not least, I am indebted to my parents, whose encouragement, love and support were unswerving.

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Abstract

Metal Substrate Process and
W-band Power Amplifier Integrated Circuits
in Transferred-Substrate HBT Technology

by
James Russell Guthrie

Record power gain and current gain bandwidths, f_{max} and f_t respectively, have been demonstrated by the transferred-substrate HBT technology developed at UCSB. Further, record gain-bandwidth baseband amplifiers and static frequency divider IC's have been demonstrated in this technology. In order to extend the high speed advantages of this technology from the demonstrated building block circuits to larger scale IC's, significant improvements in heat-sinking and packageability need to be made.

It is in the interest of enabling larger scale integrated circuits that a metal substrate HBT IC process was developed in this work. The first discrete HBTs on a copper substrate were demonstrated. Transferred substrate HBTs and simple integrated circuits were for the first time fabricated on full wafers.

In this work, integrated circuit power amplifiers were designed and fabricated which demonstrated the highest output power above 75 GHz for any HBT circuit. These MMIC power amplifiers demonstrate that the advantages of transferred substrate HBT's extend to large signal amplifiers.

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Chapter 1

Introduction

Heterojunction Bipolar Transistors had long been touted as devices that achieved high performance without fine lithographic dimensions. This "advantage" belied the corollary difficulty that HBT bandwidths did not improve with lithographic scaling. Accordingly, advancing lithography allowed HEMT bandwidths to far surpass those of HBTs.

The parasitic base resistance of a conventional double mesa HBT decreases as an emitter mesa of fixed area is made longer and narrower. However, this improved base resistance leads to little increase in device bandwidth because the total parasitic collector base capacitance is tied by the transfer length of the base ohmic technology to the area of the base mesa which increases with scaling of the emitter width. The transferred substrate HBT structure pioneered at UCSB[1] escapes this conundrum by the radical means of patterning both sides of the transistor epitaxial film. After partial processing of the devices on the native growth substrate, the epitaxial film is transferred to a surrogate substrate, and the opposite side of the film is patterned. Most results in this technology have come from devices in which the emitter was grown last, and the collector patterned last.

World record figures of merit $f_t = 275\,\mathrm{GHz}$ and $f_{\max} > 1\,\mathrm{THz}$ have been demonstrated by UCSB's transferred substrate HBT[2, 3]. Furthermore, a number of very high performance small scale integrated circuits have been demonstrated: static frequency dividers clocking to 66 GHz[4] and baseband amplifiers with gain-bandwidth products of $> 400\,\mathrm{GHz}$[5].

The above mentioned results were achieved by processing quarters of

50 mm wafers. In order successfully to fabricate larger scale integrated circuits, it is imperative that the transferred substrate process be extended to wafers of larger area. Much of the processing at UCSB occurs under conditions less than appropriate to VLSI efforts, and simple statistics suggest that circuit yield will decrease dramatically with increasing scales of integration.

When these larger scale integrated circuits are successfully fabricated, they will dissipate much larger powers, and the dissipated power density averaged over the die area will increase greatly by comparison to existing circuits. Greatly improved heat-sinking will be required.

The relevance of integrated circuits which can be tested on wafer but not packaged is somewhat limited. Successful packaging of complex high speed integrated circuits demands that the die present a continuous ground plane for bonding to the package

In this work, a process for integrating transferred substrate HBTs on a metal substrate was developed in an attempt to address the above issues relating to increasing scales of integration. This process was from the beginning developed with the goal of yielding full 50 mm wafers of HBT integrated circuits. By transferring the epitaxial material of the HBTs to a surrogate substrate composed of a highly conductive metal, the thermal resistance from the transistor junction to the far side of the substrate could be greatly reduced. Furthermore, this wholly metal substrate presents the lowest possible parasitic ground inductance between die and package.

Two schemes for fabricating transferred substrate HBT's on copper wafers were demonstrated. While discrete HBT's were successfully fabricated on a free-standing copper wafer some 200 μm thick, the difficulties of yielding integrated circuits in this scheme proved insurmountable. The second scheme involved processing integrated circuits residing on a 30 μm thick copper foil, temporarily mounted to a supporting carrier wafer. This thin foil process allowed the processing of entire 50 mm wafers. Small scale integrated circuits were successfully fabricated in this thin foil process.

As a vehicle to demonstrate the thermal advantages of the copper substrate and as part of a project that would demand an integrated array of circuits, reactively matched power amplifier circuits were designed in this work. These amplifiers were designed for operation at 94 GHz, a frequency heretofore out of reach for HBT MMICs.

To date, HEMT's have been the only viable three terminal (semiconduc-

tor) active devices for use in power amplifiers at frequencies above 70 GHz. InP based HEMT MMICs have demonstrated output powers of 430 mW at 95 GHz[6]. Only at lower frequencies did HBT's offer sufficient gain to compete with HEMT's. Millimeter-wave output powers from HBT integrated circuits have been limited to 16.2 dBm at 44 GHz[7], 13 dBm at 47 GHz[8], 4 dBm at 62.4 GHz[9] and 0.9 dBm at 108 GHz[10]. Discrete HBTs have been reported which deliver 25.6 dBm at 35 GHz[11], and 24 dBm at 44GHz[12].

While the transferred substrate HBT affords gains more comparable to those of HEMTs into the 75-110 GHz, W, band, the breakdown voltages of the current InGaAs collector device structure are lower than those attainable in HEMTs of similar bandwidth. The eventual introduction of InP collector layers to transferred substrate HBTs will significantly increase the collector breakdown voltages. As a first attempt at power amplifier design in the transferred substrate HBT technology, several integrated circuit power amplifiers were designed for the InGaAs collector device.

In the present work, reactively matched common-base power amplifier MMICs were designed and fabricated which attained non-saturated output powers of 9.7 dBm at 82.5 GHz. Also, reactively matched cascode power amplifiers were designed and fabricated. The fabricated cascode amplifiers achieved greater small signal gains and better return loss than the common-base design, and demonstrated 10 dBm output power at 75 GHz, again not saturated. A balanced pair of these cascode amplifiers delivered 10.7 dBm output power at 78 GHz. These MMICs represent the results of a first attempt to use larger, multi-finger transferred substrate HBTs in actual circuits. In particular, it should be noted that distributed combining of multiple lumped transistors was not attempted except in the balanced amplifier.

While the output powers achieved here are substantially less than the records for HEMT MMICs in this frequency range, it is worth noting that the output power per unit die area is actually more comparable. Whereas the HEMT MMIC in [6] delivered 120 mW/mm^2 of die area, the cascode amplifier here delivered 66 mW/mm^2.

Chapter 2

Substrate Engineering

Electronics for 40 GBit/sec fiber links are currently under active development at numerous companies. Future communications and radar systems will require complex ICs operating significantly above 100GHz. These and future, higher speed, generations of integrated circuits will demand very significant innovations in the design of the integrated wiring environment. In addition to producing transistors of greatly increased bandwidth, severe difficulties with interconnects, packaging and heat sinking must be addressed. The choice of wiring architecture fundamentally affects these issues and hence the performance achievable from packaged ICs. Densely integrated transmission lines and low inductance ground connections will be required which will not easily be achieved by further scaling of conventional integrated circuit structures.

2.1 Wiring Architecture

In integrated circuits operating in the 10s of GHz and above, nearly any interconnection will introduce appreciable parasitics. Where the electrical length of such interconnections exceeds some fraction of the period of signals of interest, delayed reflections from impedance discontinuities must be accounted for in the circuit design. Practically, this means that controlled impedance transmission lines are required for long interconnections. The two most prevalent geometries for the construction of transmission lines in integrated circuits are microstrip and coplanar waveguide. When designed correctly for the frequency of operation, either scheme can provide

low dispersion controlled impedance transmission lines.

Microstrip transmission lines consist of metal ribbons separated from a continuous ground plane by a slab of dielectric, as shown in figure 2.1. In many extant microwave integrated circuits, the GaAs or InP substrate has served as the dielectric layer. The characteristic impedance, Z_o, and effective permittivity $\epsilon_{\text{eff}} = (\lambda_o/\lambda)^2$ are determined by the thickness, h, and permittivity of the substrate and the width, W, of the line. For some geometries the weaker dependence of Z_o and ϵ_{eff} on the thickness of the strip metalization can not be neglected. Physical analysis of microstrip transmission lines does not lead to equations for Z_o and ϵ_{eff} that are both simple and accurate. It is worth noting however that ϵ_{eff} approaches ϵ_r for low impedance lines. The range of achievable characteristic impedances is limited in practice: resistive losses in the line tend to dominate the characteristics of lines of $Z_o > 100\Omega$, while lines of $Z_o < 20\Omega$ become too wide to be useful or even operate correctly. Line widths of greater than $\lambda/8$ must be avoided to assure single mode propagation[13]. Because the desired microstrip mode is only approximately a TEM one, it is dispersive. An empirical expression for the frequency bound below which dispersion is negligible is [14, p. 138]

$$f \approx \frac{21\text{GHz} \cdot \text{mm}}{(w + 2h)\sqrt{\epsilon_r + 1}} \tag{2.1}$$

This bound is well below the cutoff frequency of the first higher order mode of the microstrip line.

In the design of microstrip transmission lines, a compromise must be struck between line characteristics and ground connection parasitics. Because ground connections must be made by vias through the thickness of the microstrip dielectric substrate, thinner substrates result in smaller ground parasitic inductance. Against this, the strip width for a given impedance scales linearly with dielectric thickness; the narrower lines on a thinner dielectric suffer greater resistive losses. Practical microstrip geometries mandate the mechanical thinning of III-V MMIC wafers. The wafer thinning and through-wafer via etching required for microstrip integrated circuits are very costly operations.

Coplanar waveguide consists of a strip conductor centered in the gap between two semi-infinite ground planes, all atop a dielectric slab. This geometry is shown schematically in figure 2.1. The characteristic impedance

of CPW lines is a function of the ratio of the strip width W to the total width $d = W + 2s$[14, p.351]. The effective permittivity of CPW lines is simply the arithmetic mean of the permittivity of the substrate and the overlying dielectric, usually air, i.e. $\epsilon_{\text{eff}} = (\epsilon_r + 1)/2$. To avoid significant radiation, and hence be practically useful, the total width d must be scaled with frequency. Consisting as it does of three conductors, the CPW structure supports two fundamental modes: the desired CPW mode as well as a spurious slot line mode. Suppression of the slot line mode demands the periodic interconnection of the ground planes with e.g. air-bridges. Maintaining continuity of the ground planes becomes a critical issue in complex circuits.

Because all the conductors of CPW transmission lines reside on the active surface of the integrated circuit, CPW wiring promises to be a much less expensive option that microstrip wiring. Furthermore, a great advantage promised by CPW is that appropriate scaling of the transmission line dimensions for operation at frequencies as high as 300 GHz is technologically easy. In so far as adequate ground integrity can be maintained, ground return parasitics in CPW circuits can be much smaller than in microstrip: the CPW ground planes are only separated from the signal conductor by the separation s. Finally, it should be noted that in practice, CPW MMICs are typically mounted in metal packages. The additional ground plane under the die presented by the package has significant electromagnetic implications, discussed in section 2.1.3

2.1.1 Pitch of Isolated Lines

Signals on parallel homogeneous microstrip lines are coupled at all frequencies by mutual fringing capacitance. The need for isolation from line to line dictates the allowable proximity of such lines. For long runs, isolated lines are typically spaced apart by $S > 3h$[13, p.198].

Isolation between parallel CPW lines depends on the width of ground plane between them, but also on the continuity of the various separated planar ground conductors. The longitudinal ground current density distribution concentrates at the edges of the gaps in CPW (increasingly so at higher frequencies)[14, p.351], and so the characteristics of an individual transmission line are only slightly perturbed if the ground planes are each cut down to a width of $a \approx d/2$ [14, p.362]. A lower bound on center-to-

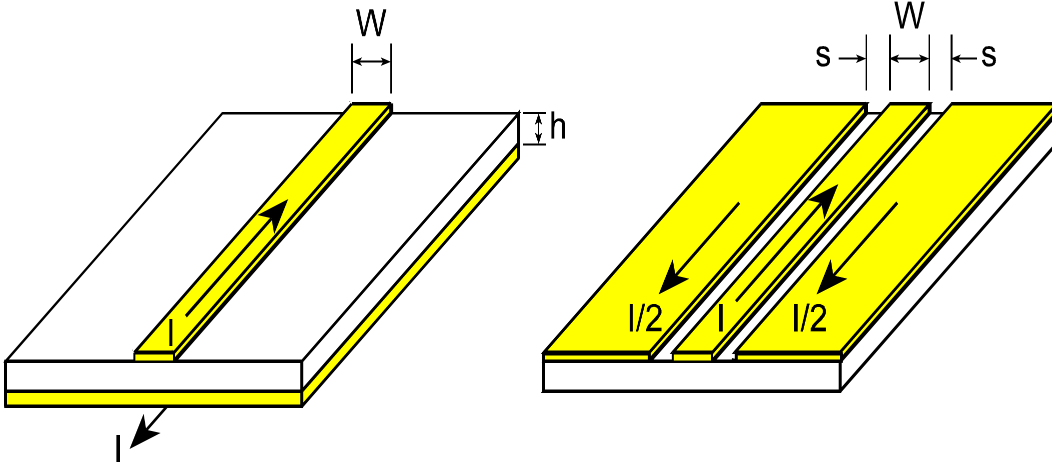


Figure 2.1: Planar transmission line geometries: a) microstrip line b) Coplanar waveguide.

center line separation for good isolation is thus $W/2 + s + d = 1.5d$. As discussed in section 2.1.3, the CPW structure inherently supports a spurious slot-line mode which must be suppressed by periodic interconnection of the ground plane segments. If the separation between or inductance of these ground stitching connections is too large, isolation between signal paths will suffer.

2.1.2 Effective Permittivity

Wiring delays can be limiting factors in the performance of delay critical circuits. The density of active devices in a given technology is constrained — if not by lithographic design rules then by limits to dissipated power density. For a fixed integration density, propagation delays will scale with $\sqrt{\epsilon_{\text{eff}}}$. Given that wiring for broadband circuits should be non-dispersive, the group velocity on transmission lines is simply $v_g = c/\sqrt{\epsilon_{\text{eff}}}$. Though semi-insulating GaAs and InP offer low enough dielectric loss to form usable transmission lines, they suffer from quite large permittivities, ϵ_r of 13 and 12.5 respectively.

2.1.3 Spurious Modes

To prevent the excitation of spurious modes, the dimensions of any transmission line must be scaled with its frequency of operation. Integrated transmission lines are no exception, and the thickness of transmission line substrates must be scaled inversely with frequency. Microstrip transmission lines inherently support the TM_0 surface wave mode for all frequencies. However, energy transfer from the microstrip mode does not occur until such frequency as the phase matching condition is reached. This condition is approximately given by the cutoff of the TE_0 surface wave mode, $f_{\mathrm{TE}_0} = c/\left(4h\sqrt{\epsilon_r - 1}\right)$[14]. Spurious surface wave modes in CPW are suppressed by the addition of a package ground plane under the substrate. The resulting structure supports a TEM parallel plate mode (between CPW and package grounds) at all frequencies which, *for ICs much smaller than* $\lambda/2$, is suppressed by peripheral grounding. For $f > c/\left(2h\sqrt{\epsilon_r}\right)$, or about 80GHz for a 0.5mm InP wafer, the spurious TE_1 parallel plate substrate mode is also supported by CPW on ground plane. CPW MMIC wafers not thinned according to operating frequency are subject to degradation by substrate mode effects. Although scaling CPW transmission lines to narrower ground plane separations can reduce the loss to spurious modes, it cannot eliminate such loss where substrate modes are allowed. Thus, any energy coupled into substrate modes from one signal path on a CPW MMIC can potentially couple back to other signal paths. Such coupling can critically affect signal isolation within real systems implemented in CPW.

As the substrate thickness of microstrip and the ground-ground separation of CPW lines are scaled down for higher frequency operation, skin effect losses are exacerbated. The surface resistance due to the skin effect varies as [14, p.111]

$$R_f = \sqrt{\omega\rho\mu/2} \tag{2.2}$$

where ρ is the resistivity, and μ the magnetic permeability — i.e. μ_o for metals of interest here. Correct scaling of the transmission line dimensions demands reducing the transverse dimensions in inverse proportion to the maximum frequency of operation. The skin effect loss per unit length, α thus varies as

$$\begin{aligned} \alpha &\propto R_f/w \\ &\propto R_f \times f \end{aligned}$$

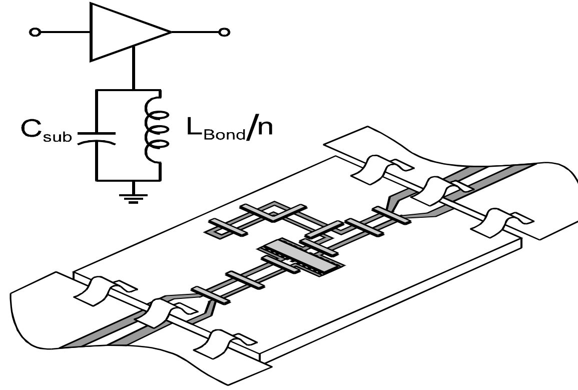


Figure 2.2: Limiting package to die ground connections to the periphery of the die introduces parasitic ground return inductance. The inductance of the n ground bond ribbons, L_{bond}/n resonates with the parallel plate substrate capacitor, C_{sub} in the ground return circuit.

$$\propto \quad f^{3/2} \tag{2.3}$$

2.2 Grounding

Ground return inductance, in particular the grounding inductance from die to package is critical to successful deployment. In wiring environments such as CPW with top-side ground planes, the die to package ground connection must be made at the periphery of the die. The inductance presented by peripheral ground wire bonds to common mode current transients scales inversely with the linear dimension of the die. For a given integration density, the currents switched in a complex IC scale with the die area. The associated $L \times dI/dt$ voltage transients can be seen to *increase* proportional to the linear dimension of the die. Problems of parasitic ground lead inductance in packaged ICs are greatly alleviated by the adoption of microstrip wiring, with its continuous backside ground plane available for soldering to the package.

Parasitic ground return inductance shared at the subcircuit level can be just as significant a problem as die-package ground inductance. While CPW wiring affords very short individual connections to the ground planes, the continuity of the ground planes suffers as circuit complexity increases,

and so it is not clear that CPW retains any ground inductance advantage in complex circuits.

The parallel ground planes of packaged CPW circuits introduce problems. Particularly on compound semiconductor wafers with their high ϵ_r, the parallel plates can represent a rather large high Q lumped capacitor. This capacitor can potentially resonate with the inductance of peripheral ground connections, as shown schematically in Fig. (2.2).

The issue of ground return loops tends to favor the use of microstrip transmission lines for complex circuit designs. Though microstrip helps to isolate ground return paths, through wafer vias themselves introduce a parasitic inductance which becomes significant at mm wave frequencies. A typical ground via through a $100 \mu m$ thick GaAs wafer might represent a 10pH inductor.

2.3 Signal I/O

Integrated circuits with either microstrip or CPW transmission line wiring require peripheral I/O connections. Wire bonding is the most established technique for effecting these connections. The fine wires used introduce significant inductance to the connection, however. The minimum inductance of a wire bond is typically on the order of 300 pH [15]. This inductance can be tuned out of controlled impedance connections by synthesizing a pi-section with capacitors at either end of the bond wire — *if* the bond wire inductance is sufficiently small and reproducible. At higher frequencies, multi-wire mesh and ribbon conductors are used to reduce the inductance of I/O connections.

A bonding technology which has long promised to deliver reproducible low inductance I/O connections is the bump bond. Bump bonds are created by fabricating metal pillars or bumps on the integrated circuit active surface and then bonding these face down to a circuit board. Where the actual bonding is effected by melting of solder bumps, surface tension of the molten metal can align the IC to the underlying metal pads. This self-aligning aspect of the solder bump bond has been important in the past, but may be less relevant with continuing improvements in automated bonding and placement equipment. Bump heights of 20–$80 \mu m$ have been demonstrated [16, 17], thus offering connections much shorter than practical bond-wires. Bump bonds with L = 10pH have been demonstrated [16]. Despite the

promise shown by bump bonding, unresolved issues of mechanical reliability and electromagnetic interaction between circuit board and integrated transmission lines remain. Also, not all bump bonding technologies allow for adequate heat sinking of active devices.

2.4 Heat Sinking

Delay sensitive circuits demand interconnects which are both physically short and characterized by high wave velocity (low ϵ_r). Minimizing interconnection delays forces integration densities up. Compounded with the high bias current density required for high speed HBTs, high power densities will arise and effective heat sinking is required.

HBTs typically reach their peak bandwidth at emitter current densities on the order of 10^5A/cm^2. Given a minimum collector-emitter bias voltage of about 1V, this implies local dissipated power densities on the order of 10^5W/cm^2. In a complex digital or mixed signal IC, the overall die power density could reach 1000W/cm^2.

We can estimate the order of magnitude of junction temperature rises using analytical expressions for heat flow in simple approximate geometries. Take for example, a $25\mu m$ grid of triple mesa HBTs each with $1 \times 6\mu m^2$ emitters, and layer structures including 300 nm InGaAs collectors and 300 nm InGaAs sub-collectors. Heat is generated in the collector by thermalization of the injected electrons. It is conventional to approximate the heat flow as spreading at 45° to the vertical.

Beneath the mesa, the heat flow from the individual device spreads initially in two dimensions, before the converging heat flux from adjacent devices results in heat flow which is essentially one dimensional. Approximating the heat flow as spherical within a cone of 45° half angle until cones from adjacent devices meet, and uniform below that, we have

$$R_{\text{th,cone}} = \frac{1}{\Theta \cdot \kappa_{\text{InP}}} \cdot (1/r_1 - 1/r_2) \qquad (2.4)$$

where $\Theta = 2\pi(1 - 1/\sqrt{2})$steradians is the solid angle of the cone, and r_1, r_2 are chosen to match the areas of the spherical surfaces to the physical areas; $\kappa_{\text{InP}} = 75\text{Wm}^{-1}\text{K}^{-1}$ has been assumed to apply in the collector layers here. Thus, for $6\mu m^2$ emitters on a $25\mu m$ grid, $r_1 = \sqrt{6\mu m^2\Theta^{-1}} \approx 1.8\mu m$, $r_2 \approx$

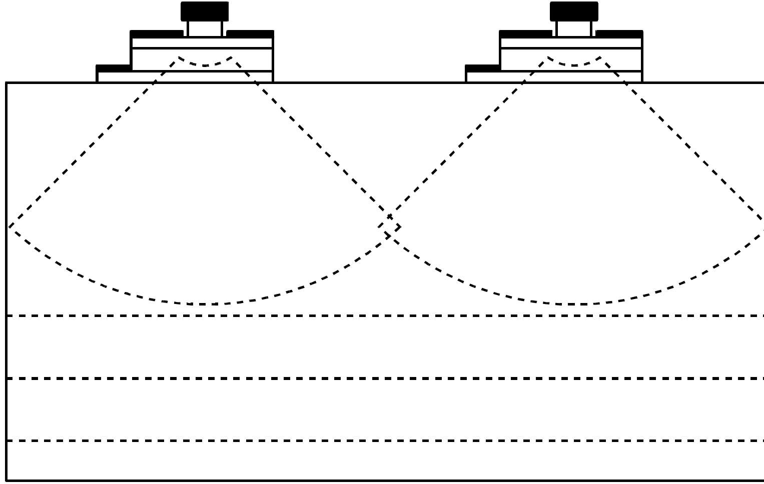


Figure 2.3: Diagram of approximate heat flow conditions assumed in calculation

$18.4\mu m$, and $R_{\text{th,cone}} \approx 3600$K/W. Assuming one-dimensional heat flow in a cross-sectional area of $625\mu m^2$ through the rest of the wafer, the thermal resistance of a 0.5mm InP wafer is $R_{\text{th,unif}} = t/(A\kappa_{\text{InP}}) \approx 10^4$K/W. For the power density of our example, the temperature will drop 22 K across the spherical flow region, and a further 60 K in the one dimensional flow region. Given that the HBT collector is composed of InGaAs, a much worse thermal conductor than InP ($\kappa_{\text{InGaAs}} \approx 5Wm^{-1}K^{-1}$) the actual temperature rise will be higher. To achieve acceptable junction temperature rises in dense integrated circuits, the thermal resistance to the package must be reduced. Thinning the InP wafer in the above example to $50\mu m$ reduces the total temperature rise from 82 K down to 25 K.

2.4.1 Wafer Back-thinning

Given the thermal and electrical issues which favor the use of thin substrates, it has long been common practice to thin GaAs and InP wafers[18, p.320]. This has generally been accomplished by temporarily mounting the semiconductor wafer to a supporting substrate and then mechanically grinding the back of the semiconductor wafer away[18, 19]. While microstrip MMICs had long been thinned to $100\mu m$, increasing operating frequencies have recently forced the widespread use of thinner wafers. Recently re-

ported MMIC amplifiers operating at 155GHz[20] and 94GHz[21] required substrate thinning to $75\mu m$ and $50\mu m$ respectively, where heat sinking and ground via inductance are the driving issues. High power HBT MMICs have been fabricated on substrates thinned to $30\mu m$ [22]. Handling and lapping of such thinned wafers is difficult, and will become more so as frequencies are increased and the wafers thinned accordingly. In so far as complex high speed IC's will require controlled impedance wiring, a wiring architecture which scales to higher frequencies more easily than conventional microstrip wiring is called for.

2.5 Scaleable Wiring Architectures

A number of approaches to the various IC substrate issues raised above have been proposed in the literature. Microstrip-like transmission lines can be fabricated by depositing dielectric and conducting layers all on the active side of a semiconductor wafer. This general concept has been demonstrated in a number of implementations[23, 24, 25].

In the "Embedded transmission line" [24, 26] architecture, strip transmission lines are permanently sandwiched between the GaAs substrate and a deposited polymer dielectric, with a continuous ground plane residing on this polymer layer opposite the GaAs. The effective dielectric constant of transmission lines is intermediate between the dielectric constant of the host semiconductor and the low k polymer; this results in faster propagation than in conventional microstrip MMICs, but may lead to undesirable synchronous coupling to surface wave modes. Global planarization of electroplated ground vias and deposited polymer dielectric is achieved with a mechanical lapping step. This architecture has the advantage that flip-chip mounting to a suitable carrier can very simply provide heat sinking, grounding, and low inductance signal connections. Furthermore, the electrical properties of the circuit are perturbed relatively little with respect to on-wafer testing when packaged. Against these advantages, ϵ_{eff} of the embedded lines is greatly increased by the presence of the GaAs wafer, and device parasitic capacitances are increased by embedding in the polymer.

Another approach to achieving very thin transmission line structures is the so-called "master–slice" technology of NTT[27, 25]. In this scheme, nearly continuous ground planes are formed in metal deposited on the wafer surface after front-end processing, leaving gaps around active and passive

devices on the wafer surface. Strip transmission lines are then formed on top of, or sandwiched between, thin deposited layers of polyimide. The ground plane on the wafer surface makes the transmission line properties independent of the underlying semiconductor. The inclusion of a second ground plane in the structure changes the transmission lines from microstrip to embedded strip geometry. The embedded strip-line geometry increases coupling of the signal line to ground compared to microstrip, and so reduces the maximum achievable impedance. While electrical vias from transistors to the topside ground plane have been demonstrated by NTT in this technology, the effectiveness of such vias as heat sinks has not been established.

If continuity between the two ground planes is sufficient, then loss to and coupling via spurious modes are virtually eliminated. Maintaining continuity between the final ground plane and the first, perforated, ground plane will however become increasingly difficult for densely integrated active devices. Ideally, thin embedded stripline supports no radiation modes, and the evanescent fields at transmission line discontinuities decay strongly. Thus, cavity resonances can not be excited by radiation from transmission line discontinuities, and so the packaged circuit performance is changed very little from that measured on wafer. Furthermore, bonding the so-called master-slice IC's wiring side down to a package can allow very low inductance bump bonded signal and ground connections. Designs with multiple ground planes isolating stacked transmission lines have been demonstrated on both GaAs and Si substrates [27].

2.6 A Substrate for Transferred Substrate IC's

A substrate technology was developed to address many of the obstacles to building medium scale integrated circuits with UCSB's transferred substrate HBT. This device structure, which demands processing of both sides of the epitaxial semiconductor film, affords some unique freedoms but also imposes restrictions on the substrate fabrication process.

Current research goals for the HBT IC process at UCSB include high speed integrated circuits of 100-3000 transistors. These include digital and mixed signal integrated circuits such as a sigma-delta ADC, the building

blocks of a very fast direct digital frequency synthesizer. These circuits demand dense routing of controlled impedance transmission lines, a high degree of isolation between signal paths as well as posing serious heat sinking problems.

2.6.1 Metal Substrate Solution

In this work, a technology was developed to address substrate issues by choosing the substrate to which the transferred substrate HBT's were transferred. By transferring the epitaxial material to a metal substrate, many advantages could be gained. This metal substrate would serve as the electrical ground plane of microstrip wiring and also provide a greatly improved heat sink. By transferring the epitaxial film of the transistors to a metallic substrate, the junction temperature rise could be greatly reduced with respect to that achievable on the native, InP, substrate. With a suitable process sequence, the dielectric of the microstrip lines could be formed in a deposition operation; the microstrip dielectric layer could then be made much thinner than the practical limits of mechanical wafer thinning schemes. Such a thin microstrip dielectric would allow ground vias to be aligned directly to the HBT, thus minimizing heat conduction by any material but metal. As in any microstrip wiring scheme, these ground vias constrain the routing of transmission lines, but this is mitigated by the small via dimensions made possible by a drastically thinned dielectric.

The essential features of this metal substrate structure are shown schematically in fig. 2.4. Individual transistor mesas represent the only remaining semiconductor. The microstrip wiring is on a layer of the thermoset polymer benzo-cyclobutene (BCB) which affords a low permittivity of $\epsilon_r = 2.7$. Heat is removed from individual transistors by metal ground vias through the BCB. Electrical isolation between such ground vias and non-grounded transistors is provided by a thin film of PECVD $\mathrm{SiN_x}$. The ratio of ground parasitic capacitance introduced to thermal conductivity provided by this MIM structure is fixed by the material properties of the $\mathrm{SiN_x}$. To mitigate the impact of the parasitic capacitance to ground introduced by the MIM heatsink structure, an emitter down configuration of the HBTs was chosen. The intrinsic base-emitter capacitance C_{BE} of a bipolar transistor is inherently much larger than the parasitic C_{CB}. Thus, parasitic capacitance to ground will tend to impact circuits less if it occurs

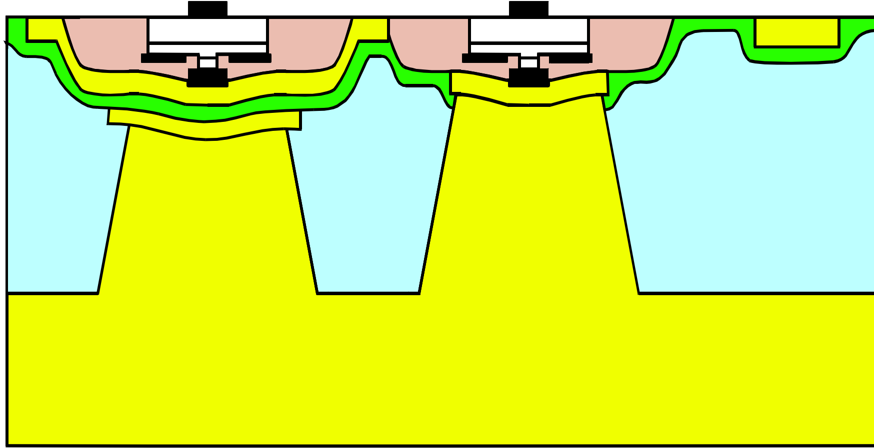


Figure 2.4: Schematic diagram of proposed metal substrate IC structure. Ground vias rise to an isolated and a grounded-emitter HBT at left and center respectively, while a microstrip line runs at right.

at the emitter node than at the collector. Furthermore, while heat is largely generated in the collector of HBTs, it is uniformity of the base-emitter junction temperature(s) which is most critical to thermal stability. For these reasons, the finished HBTs are built with their emitters facing the ground plane.

Design curves of Z_o and ϵ_{eff} for microstrip lines on $5\mu m$ of BCB are shown in figure 2.5. The transmission lines formed in this process are not, however, strictly of microstrip geometry. Because the SiN_x and BCB dielectrics are deposited over metal lines already residing on the semiconductor surface, these lines are embedded in dielectric as is illustrated in figure 2.4. The thickness of the metal lines, at approximately $0.8\mu m$, is not negligible compared to the $5\mu m$ thickness of the BCB, and the characteristic impedance of these lines will be reduced from that of microstrip lines of the same width.

Removing heat through the emitter material introduces a significant thermal resistance. Heat generated in the collector must traverse the material layers of the base and emitter before reaching the highly conductive ground via. Assuming that heat is generated uniformly through the collector space charge region, the thermal resistance from the collector to the

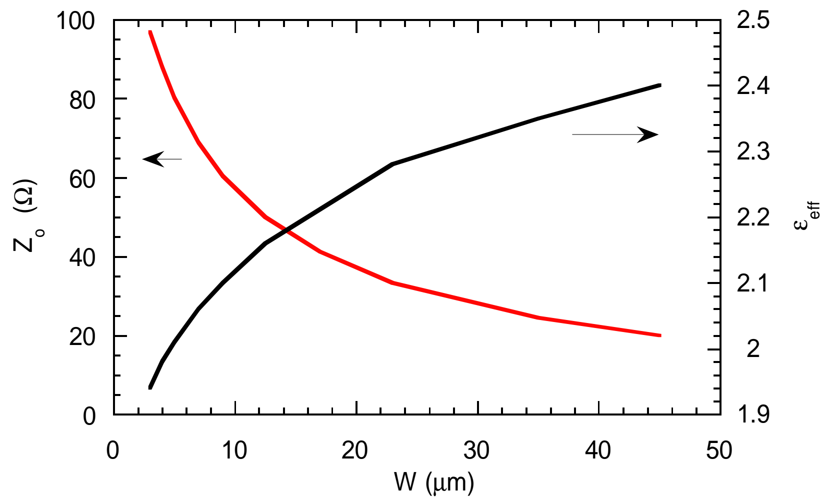


Figure 2.5: Design curves for microstrip transmission lines on $5\mu m$ of BCB, calculated with the semi-analytical models of HP EESOF Linecalc. Note that with this thin low ϵ_r dielectric, and even assuming true microstrip geometry, Z_o is sensitive to the thickness of metalization: $1\mu m$ was used here.

base of the emitter mesa can be estimated as

$$\begin{aligned} R_{th,cb} &= \int_0^{T_{col}} Q[z] \frac{dz}{\kappa_{col} L_E W_{equ}} \\ &= \frac{T_{col}}{2\kappa_{col} L_E W_{equ}} \end{aligned} \tag{2.5}$$

where $Q[z] = P \cdot z/T_{col}$ is the heat flux at z, and W_{equ} is an equivalent collector width chosen to approximate the two dimensional heat flow. For the purposes of rough estimates, W_{equ} can be taken as $(W_E+W_C)/2$. For an example transistor with $1 \times 6\mu m^2$ emitter, $2\mu m$ wide collector and $0.3\mu m$ collector thickness, $R_{th,cb} \approx 3300\text{KW}^{-1}$. Assuming that this transistor dissipates 6 mW, $\Delta T_{cb} \approx 20°C$.

The resistance of the emitter mesa

$$R_{th,emit} = \frac{T_{emit}}{\kappa_{th,emit} L_E \cdot W_E} \tag{2.6}$$

where W_E is the width of the emitter semiconductor — which in this process is less than the width of the emitter metalization. In the present work, emitters with a patterned width of $1\mu m$ were undercut to a minimum semiconductor width of $\approx 0.7\mu m$. Given that κ_{th} for InGaAs and InAlAs is $\approx 5Wm^{-1}K^{-1}$, and $T_{emit} = 0.27\mu m$, $R_{th,emit} \approx 13000KW^{-1}$ for a $1 \times 6\mu m^2$ nominal emitter size, and $\Delta T_{emit} \approx 78°C$. The adoption of InP emitters will improve $R_{th,emit}$ by the ratio of $\kappa_{InP}/\kappa_{InGaAs}$, i.e. 15:1. The thermal conductivity of polyimide is sufficiently poor that it contributes little to heat sinking. A lower bound on the resistance through the polyimide is given by assuming uniform heat flow through an area of $8 \times 8\mu m^2$ of polyimide $0.5\mu m$ thick, which yields $R_{PI} = 5 \times 10^4 KW^{-1}$.

The thermal resistance of the MIM structure can be calculated approximately using transmission-line models. Approximating the true heat flow by the currents in the thermal resistor network shown in figure 2.6,

$$R_{th,SiN} = (G_e + 2G_{spread})^{-1} \tag{2.7}$$

where G_e is approximately

$$G_e = \frac{\kappa_{SiN} L_E \cdot W_E}{t_{SiN}} \tag{2.8}$$

Material	Thermal Conductivity $Wm^{-1}K^{-1}$	Source
InP	75	
InGaAs	5	
InAlAs	5	
Si_3N_4	5–30	[28]
Au	300	
Cu	400	
Polyimide	0.15	

Table 2.1: Thermal properties of materials in the heat path. Note that the low value for Si_3N_4 refers specifically to PECVD nitride.

and G_{spread} is given by [18, p.231]

$$G_{spread} = \left(\frac{\sqrt{R_{sh} r_c}}{L_E} \coth \frac{d}{L_t} \right)^{-1} \tag{2.9}$$

and the transfer length, L_t is given by

$$L_t = \sqrt{r_c / R_{sh}} \tag{2.10}$$

$$r_c = \frac{T_{SiN}}{\kappa_{\mathrm{SiN}}} \tag{2.11}$$

$$R_{sh} = \frac{1}{t_{Au} \kappa_{Au}} \tag{2.12}$$

In the present work, a layer of Au interconnect 800 nm thick is interposed between the emitter contact metal and the $\mathrm{SiN_x}$ insulator. The $\mathrm{SiN_x}$ layer in turn is 400 nm thick. Referring to the material parameters in table 2.1, and taking κ_{SiN} to be 5 $\mathrm{Wm^{-1}K^{-1}}$, $r_c = 8 \times 10^{-8} Km^2W^{-1}$, $R_{sh} = 4167 KW^{-1}$ and $L_t = 4.4 \mu m$. For the example $1 \times 6 \mu m^2$ emitter device, and assuming that the interconnect metal overlapping the ground via measures $8 \times 8 \mu m^2$, $G_{spread} \approx (3400 KW^{-1})^{-1} = 2.9 \times 10^{-4} WK^{-1}$, $G_E \approx 7.5 \times 10^{-5} WK^{-1}$ and $R_{th,SiN} \approx 1500 KW^{-1}$. This corresponds to a $9°C$ temperature rise for 6 mW power dissipation.

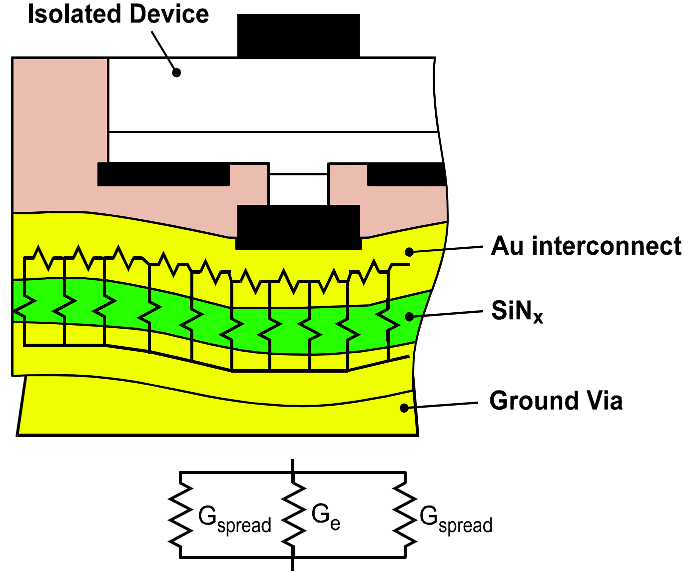


Figure 2.6: Distributed equivalent circuit model of heat flow across SiN_x dielectric to ground via.

The thermal resistance of the ground via is taken to be simply

$$R_{th,via} \approx \frac{H_{via}}{\kappa_m A_{via}} \tag{2.13}$$

which, for a Au via $5\mu m$ tall of $6 \times 6\mu m^2$ cross section is approximately $460\,\mathrm{K\,W^{-1}}$ and corresponds to a 3°C temperature rise. The temperature rise through the body of a copper substrate $30\mu m$ thick is estimated, as per the method of section 2.4, to be a further 2°C.

By replacing the InP substrate with a Cu one, and hence increasing the substrate thermal conductivity from 75 to $400\mathrm{Wm^{-1}K^{-1}}$, the proposed metal substrate technology promises to provide greatly improved heatsinking of densely integrated HBTs. However, so long as the emitter material consists of InGaAs and InAlAs, the thermal resistance incurred by heatsinking the device through the narrow emitter mesa will negate most of the advantage of the metal substrate over conventional thinned semiconductor wafers. Where the metal substrate confers an immediate advantage is by comparison to the pre-existing transferred substrate process. As discussed in section 3.2, this process involved mounting a relatively thin ground plane

to a GaAs carrier wafer with a layer of solder some $50 \mu m$ thick. An overall dissipated power density of $1000\,\mathrm{W\,cm^{-2}}$ would result in temperature rises of 12°C across the solder and 100°C across the GaAs, or 110°C more than the temperature rise estimated above for the copper substrate.

Chapter 3

Copper Substrate Process

It was shown in chapter 2 that a metal substrate would afford significant thermal and electrical advantages to HBT integrated circuits. In this chapter, a process for fabricating these metal substrate ICs is presented, and its development discussed.

The problem of producing a suitable metal substrate was approached by electroplating thick films of metal. Electroplating is often used in the fabrication of high performance ICs because it allows for much more efficient use of the source material than vacuum deposition methods. Here, electroplating was chosen because it can reliably yield metal films under less stress than any other deposition method.

In this work, two distinct metal substrate processes were developed. The first, which entailed plating a metal substrate thick enough to handle by itself, only yielded discrete transistors. In the second approach, a much thinner film of metal was deposited, and temporarily mounted to a rigid support wafer for final processing. This thin foil process yielded the first complete 50 mm wafers of transferred substrate HBTs, as well as yielding functioning HBT ICs.

3.1 Building a Metal Substrate

Various means of transferring the integrated circuits to a metal substrate were examined. These can be categorized as bonding or depositing. Mechanical issues had a large bearing on the choice made here. Although metals offer superior electrical and thermal conductivity, other properties

of many metals are not so well suited for integration in an IC process. The coefficients of thermal expansion (CTE) of most pure metals and alloys are much larger than the CTE of InP and related materials. Whereas the CTE of InP around room temperature is approx. $4.6 \times 10^{-6} K^{-1}$, those of highly conductive metals are much higher. As shown in figure 3.1, the CTE's of Ag, Cu and Au at room temperature are 19.7,16.8 and $14.2 \times 10^{-6} K^{-1}$, respectively. The refractory metals W and Mo have CTE's much closer to that of InP, but thermal conductivities significantly inferior to those of the good conductors. Likewise, common low expansion alloys such as Kovar and "Alloy 42" (42wt%Ni 58%Fe) suffer from inferior thermal conductivity: 17.3 and $10.7\text{Wm}^{-1}\text{K}^{-1}$, respectively. A number of metal matrix composite materials with adjustable expansivity have been used successfully in packaging integrated circuits. Notable among these are Cu matrices with dispersed W, and porous SiC infused with Al.

Bonding methods which can provide electrical and thermal conductivity include soldering, the use of conductor loaded adhesives, and diffusion bonding of suitable metal surfaces. Diffusion bonding of e.g. Pd coated surfaces was not considered here because of the extreme surface flatness that would be required to achieve a continuous bond between two wafers. The thermal conductivities of loaded adhesives tend to be much nearer the mediocre value of the matrix adhesive than the desirable value of whatever powdered constituent is added. Thus, the thermal conductivity of a typical Ag loaded epoxy is only $1.66\text{Wm}^{-1}\text{K}^{-1}$[29]. A number of solders are markedly more conductive: pure In and 80 wt% In 15% Pb 5% Ag have thermal conductivities of 86 and $43\text{Wm}^{-1}\text{K}^{-1}$, respectively [30]. Solders are sufficiently poor thermal conductors that only a thin layer could be tolerated within the thermal budget

In the context of the transferred substrate HBT process, soldering to a metal substrate would be not be without difficulties. In such a scheme, the partially processed wafer would be capped with a thin metal ground plane, and this last would be soldered to a suitable metal substrate. Severe practical issues of planarity arise in joining two wafers with a thin continuous layer of solder. Furthermore, thermo-mechanical issues greatly constrain the choice of metal substrate. Bonding would occur before removal of the InP substrate, and so the sandwich of InP-solder-metal would be joined rigidly as the solder cooled down from its melting temperature. Large mismatches between the CTE's of the InP and the metal selected would lead

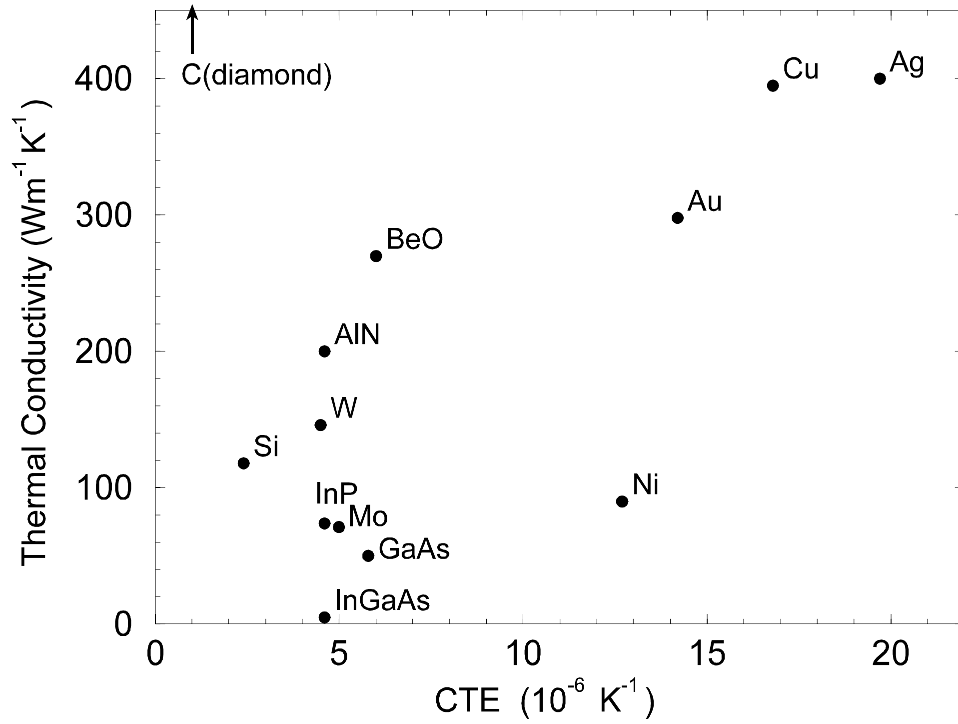


Figure 3.1: Coefficient of thermal expansion and thermal conductivity of pure materials.

to the wafer sandwich bowing substantially. In the practical case of a metal having a larger CTE than the InP, this last would be under net biaxial compression upon cooling. In the bowed, bimetallic disk, configuration the free surface of the InP would tend to be under tension, which would create the risk of crack initiation. Thus, metal substrates for bonding need to be well expansion matched to the semiconductor. Tungsten or Cu/W composites are indicated, but neither of these proved to be readily available in wafer form.

Having decided against bonding the partially processed wafer to a monolithic metal substrate, it remained to devise some way to deposit a suitable substrate. The vacuum deposition methods used to deposit thin films in integrated circuit processing tend to yield materials under very significant stress. This intrinsic stress is only partly attributable to temperature excursions and the CTE mismatch between the metal deposited and the substrate. Reported film stress values range from 50 MPa for sputtered Au[31] to $1GPa$ for sputtered W[32]. Electroplating is generally acknowledged to be the deposition method which affords the lowest stress films. Film stresses of 1 MPa are routinely achieved in plated Cu[33, 197]. It should be noted that film stresses in metal films are subject to significant hysteresis with temperature cycling[31]. Significant recrystallization of plated metal films at temperatures far below normal annealing temperatures – even at room temperature – is a well known phenomenon[34].

Electroplating cannot be used to deposit films of pure metals which are expansion matched to the semiconductors of interest. Whereas the refractory metals W and Mo, which are nearly expansion matched with InP, can be deposited by sputtering or evaporation, they have not been electroplated[33]. The additional complexities involved in the plating of alloys were judged unacceptable for this work. Likewise, the technology of forming metal matrix composites by occlusion of foreign particles in a plated film [35, 36], long established in the coating of gas turbine parts and the fabrication of diamond tipped tools, was not considered here.

Realizing that metals which can be plated are not expansion matched, it remained to choose a metal from among the good conductors based on other criteria. The two metals for which low stress plating chemistries are very well established are nickel, from nickel sulfamate solutions, and copper, from copper sulfate solutions. Copper, being by far the better conductor of these two, was chosen to form the bulk of the plated substrate.

3.2 Solder Bonded Process

In parallel to the development of the metal substrate process, a provisional process was developed [37, 38]. This partial wafer process relies upon a solder bond to mount the IC structure to a carrier wafer. While this solder bonded process did not afford all the advantages of the proposed metallic substrate, it has been this process which has yielded most device and circuit results to date.

Elements of the integrated circuit process common to both the solder bonded process and the copper substrate one will be described here, as will the solder bonding operation itself. Device formation begins with the patterning and definition of emitter contact stripes. The emitter metalization is in turn used as the mask for a self-aligned emitter mesa etch. The emitter mesa is etched in a combination dry and wet etch sequence. To date, the dry etching has been by $CH_4/H_2/Ar$ RIE etching, and is stopped within the InAlAs emitter layer with the aid of laser interferometry. Material damage is removed, etch depth controlled, and the emitter metal undercut in a multi step selective/non-selective wet etch sequence.

Self-aligned base ohmic contacts are formed by lifting off Ti/Pt/Au metalization which breaks at the emitter base undercut. Devices are isolated into mesas by a non-selective dry etch in Cl_2 plasma, controlled by visible laser interferometry. The mesas are passivated and planarized with polyimide which is etched back with O_2 RIE and then patterned in an O_2 plasma etch.

NiCr thin-film resistors are patterned by lift-off. An underlayer of Si evaporated along with the NiCr serves to protect the resistors from the subsequent InP removal etch. Next, the first level of interconnect metal is deposited by evaporation and patterned by lift-off. In this step, the wafer is mounted at an angle on a rotating mount to assure coverage of topographic steps. Silicon nitride is deposited by PECVD and contact vias are etched in this layer. The Si_3N_x film serves the purposes of dielectric for MIM capacitors and insulation between the first and second interconnect metalization. Also, the Si_3N_x conducts heat from emitters which are not electrically grounded. A second level of interconnect metal is deposited in the same manner as the first. Benzo-cyclobutene resin is deposited by spin coating, and cured in a nitrogen purged programmable oven. Vias are patterned in the cured BCB film by RIE etching with a thick photoresist

mask. A continuous conducting layer is applied to the wafer by DC magnetron sputtering of Ti and Au. Some $5\mu m$ of Au are then built up by electroplating in a commercially prepared $Na_3Au(SO_3)_2$ solution.

The metalized HBT wafer and a carrier are soldered together under air. To date, GaAs wafers have been used as carriers. Lumps of solder are melted on the heated carrier piece, and the molten solder spread manually. Once the surface of the carrier is visibly covered with solder, any excess is removed. The wafer is then placed active side down to the solder. In an effort to form a continuous solder bond free of voids and oxide layers, the wafer is then manually "scrubbed" across the solder coated carrier. Given that the plated Au ground plane tends to be rough and non-planar, the possibility of voids is very real. The carrier and native wafer are squeezed together with controlled force before the sandwich is cooled to room temperature.

Continuity of the solder bond depends critically on craft and determination in the "scrubbing" operation. As it stands, the solder bonding scheme offers little hope of scaling to full 50mm wafers. It is already difficult to apply sufficient shear forces to scrub two samples of quarter (50mm diameter) wafer size. Furthermore, many finished quarter wafers show clear evidence of numerous large voids in the bond. This can be seen under dark-field or quasi-dark-field optical microscopy such as provided by stereo microscopes with nearly coaxial illumination.

This solder bonding scheme suffers from poor control and reproducibility. Particularly after removing "excess" solder from the carrier, the quantity of solder in the bond is not controlled. In figure 3.2, a sawed and polished cross-section of a solder bonded wafer reveals that the solder thickness is sometimes quite large. Solder thicknesses of $\approx 50\mu m$ are not conducive to good heat sinking. Furthermore, the sometimes substantial thickness of solder allow quantities of this solder to dissolve in the substrate removal etchant; it is not known how the variable concentrations of solder constituents in the etch solution affect the final collector surface.

3.3 Plating Copper Substrates

Two approaches to integrating transferred substrate HBT's on a Cu substrate were demonstrated in this work. The first consisted of plating sufficient thickness of Cu to handle the metal wafer by itself through final

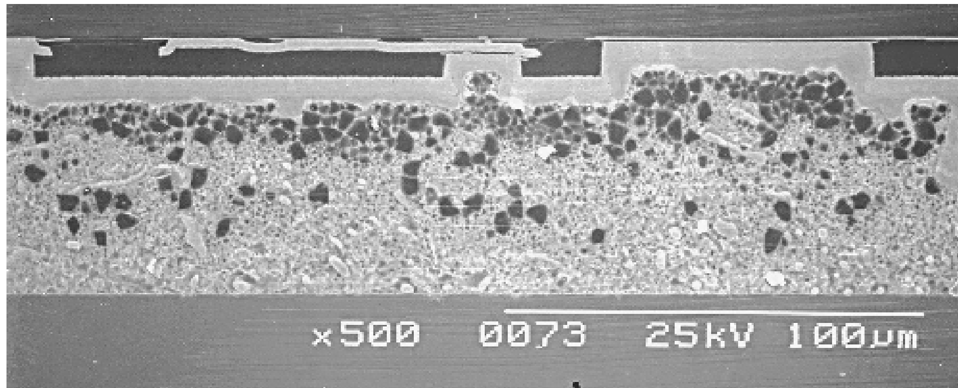


Figure 3.2: SEM image of sawed and polished solder bonded wafer. Dark lumps are artifacts of the polishing process.

processing. This approach was attempted first because it seemed to be the simplest route to demonstrating on-wafer measurements of integrated circuits, and it promised to avoid some thermal mismatch problems. If the InP could be removed without the InP/Cu sandwich undergoing any temperature excursions, then there would be little opportunity for cracks to initiate in the semiconductor due to thermal mismatch stresses. After InP removal, only single device sized mesas of semiconductor would remain, and the strain energy developed in these mesas by unavoidable temperature excursions would hopefully not be sufficient to cause damage. At first, quarter wafers were processed in this way, and later whole wafers.

Later, it proved necessary to reduce the thickness of metal plated below that which would allow practical handling of an entire wafer. In order to complete the processing after metal deposition, it was therefore necessary to mount the wafer temporarily to a support substrate.

In both cases, electroplated Cu formed the bulk of the plated metal thickness. It was decided, however, to form the initial thickness of the ground plane out of plated Au to avoid metallurgical problems at the interface with the underlying thin film metalization. Copper and Au are a notorious diffusion couple[34, p.90], inter-diffusing appreciably at room temperature. This interdiffusion leads to degradation of the properties of the metals, but worse can lead to the formation of a plane of voids[34, p.95]. To preclude interdiffusion, barrier layers of Ni were plated between Au and Cu layers. Copper etches very readily in the HCl solution used

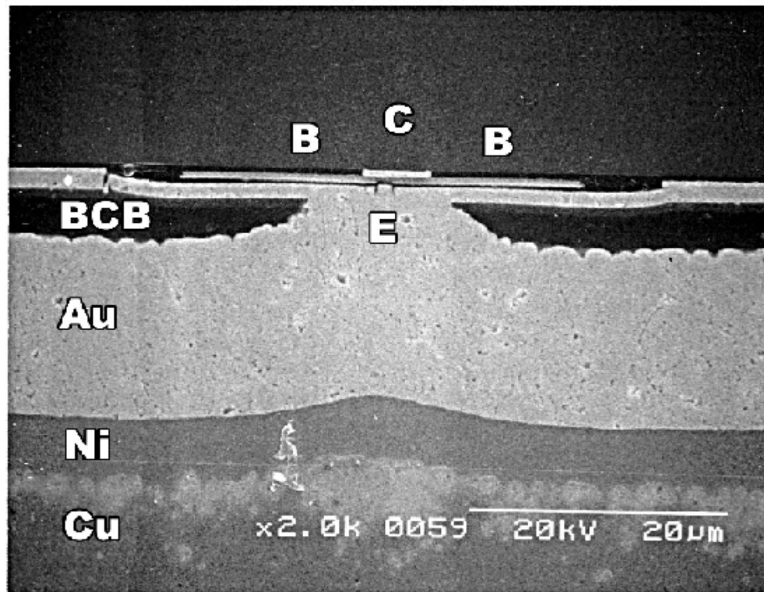


Figure 3.3: Cross-sectional SEM of test wafer. Thicknesses of Au, Ni, not representative of those finally used.

to remove the InP substrate, and so the plated Cu was encapsulated with further layers of Ni and Au.

3.4 Free-Standing Metal Wafers

Handling of a free-standing metal wafer demanded a deposit of Cu hundreds of microns thick. In order to plate metal films on the order of $2 \rightarrow 400\mu m$ thick, some innovative plating fixtures were required. Achieving a planar metal wafer required some investigation of film stress issues, and led to the unconventional choice of a Cu plating solution free of commercial additives. The final photolithography step, to define the collectors, had to be performed on the free-standing metal wafer. In order to make metal wafers hold down to aligner vacuum chucks, it proved necessary to lap the plated surface.

3.4.1 Plating Fixtures

Plating an unusually thick layer of metal required special attention to be paid to the electrical contacts through which plating current was applied to the wafer. These contacts needed to be isolated from the plating solution, else they would be welded permanently to the wafer by the growing deposit. Furthermore, the distribution of plated metal had to be controlled. The back and edges of the wafer had to be protected from potential attack by the corrosive plating solution and from encroachment of the plated film. Given that only contact lithography was available during the development of the full-thickness Cu process, it was imperative that the plated metal not extend around the edges of the InP wafer. Although photoresist could in principle be used to protect the back and edges of the wafer, coating resist on the back of the wafer without damage to the front of the wafer presented practical obstacles.

To control the gross distribution of plated metal, and to isolate the contacts, a front-surface sealing fixture was designed (see Appendix B). One o-ring is compressed against the front of the wafer, while a second o-ring creates an enclosed, dry, volume within which the electrical connections to the seed layer could be made. This fixture was fabricated in PVDF, a fairly inert plastic with stiffness and cold-flow properties superior to PTFE. A noteworthy tradeoff in the design of the quarter wafer sealing fixture was between fluid flow and stiffness of the bolt-ring that squeezes the two o-rings. In the fabricated quarter wafer fixture, the opening through which the wafer is exposed to the plating solution is almost as deep as it is far across, and this impacted the uniformity of fluid flow past the wafer. The deep recess created by the quarter wafer plating fixture restricted the choice of plating chemistry and presented some other challenges.

3.4.2 Plating Solutions

Throughout this work, Au was plated from a commercial solution of sodium gold sulfite and proprietary additives. Nickel diffusion barriers were plated from a commercial solution of Ni sulfamate. Cu was plated from a variety of different $CuSO_4$,H_2SO_4 solutions, some commercial with organic additives, and some without any additives at all.

A common insoluble anode was used to plate from the Au, Ni, and Cu solutions. This choice simplified the transport of the wafer from one

Compound	Molecular (atomic) weight	Density $g \cdot cm^{-3}$	Species Plated
$CuSO_4 \cdot 5(H_2O)$	249.68		
$CuSO_4$	159.60		Cu^{2+}
H_2SO_4	98.08		
$Na_3Au(SO_3)_2$	196.97		Au^{1+}
Ni Sulfamate	58.69		Ni^{2+}
Cu	63.55	8.92	
Ni	58.69	8.90	
Au	196.97	19.31	

Table 3.1: Molecular weights of compounds and metals, and charged species relevant to plating here.

solution, through rinsing baths, to the next solution in the metal stack with minimum exposure to air. The insoluble anode and wafer holding fixture were together bolted to a plastic frame which suspended them from the rim of the beaker in use. While the use of insoluble anodes is commonplace in Au plating from $Na_3Au(S0_3)_2$ solutions, it is less common practice in the plating of Ni and Cu. In any electroplating reaction, the use of an insoluble anode leads to depletion of the metal ion and acidification of the plating solution in proportion to the charge plated. Here, the properties of Ni films were judged not to be critical, and the solution chemistry allowed to drift. The $CuSO_4$ solution was discarded and replaced frequently to compensate for depletion of Cu^{2+} ions.

A $300\mu m$ layer of Cu on a $500\mu m$ InP wafer represents a bimetallic disk. The large expansivity mismatch between these materials mandates very small thermal budgets for any processing which follows the Cu deposition. For this reason, the Au and Ni plating conditions were adjusted to work at room temperature.

Initial attempts to plate Au in the fixture under established conditions but reduced temperature led to unusable, powdery deposits. Smooth surfaces were only achieved, at practical current densities and at room temperature, with the use of a pump to circulate the plating solution. A small diaphragm pump was used to force the solution through a filter capsule and out of a nozzle immersed in the solution and directed against the wafer.

Successful plating of Ni at room temperature as opposed to the recommended operating temperature of 50°C proved to be a matter of establishing a suitable current density. The limited agitation provided by a stirrer bar in the beaker proved adequate. Attempts to plate Cu from commercial solutions designed for low-stress, fine-grained deposits were met with terrible non-uniformity.

The $CuSO_4$ solution without additives used here was based on textbook practice for low stress copper plating [33, p. 186][39]. This solution consisted of 0.8 mole $CuSO_4 \cdot 5(H_2O)$ and 45 ml of concentrated H_2SO_4 per liter of solution.

Initial attempts to plate Cu from a commercial solution, Techni-Copper FB from Technic Inc., were abandoned when thick deposits proved to be under significantly more stress than deposits from a $CuSO_4$,H_2SO_4 solution without additives. Later, a different commercial solution, "UBAC R-1" from Enthone-OMI, which was designed to deposit thick low stress Cu, was acquired. The pump and nozzle circulation which had led to acceptable coverage and roughness of plated Au in the deeply recessed fixture did not achieve acceptable results with this latter Cu solution. Test samples plated displayed spectacular undulating surfaces. The large thicknesses of Cu plated put a great premium on uniformity of deposit thickness. Beyond this, however, the Cu solution had been designed for conditions of much more vigorous agitation than had the Au solution, and seemed to suffer more from the nonuniform flow in the quarter wafer fixture.

3.4.3 Film Stress

The major problems in developing a copper plating process revolved around the need to do lithography on the final wafer. Early on, it became apparent that the stresses in thick plated films could be more than enough to make the wafer too non-planar for contact lithography. Later, it was found that stresses in the metal film impacted the wet selective etch used to remove the InP growth substrate. Later still, it was recognized that roughness and non-uniformity of the back surface of the metal were critical issues for vacuum chucking of the wafer on exposure tools.

Throughout this work, qualitative comparisons of film stress were made by measuring the bowing of plated wafers. For lack of a dedicated instrument, the Dektak profilometer was used, often taking maximum length

traces – i.e. 30mm long. Traces were taken on the semiconductor side of plated wafers because the semiconductor surface was generally smoother, and because doing so reduced sensitivity of the bowing measurement to thickness variations in the deposit. The stress in plated Cu films was consistently tensile, and so the wafers showed no propensity to rock under the profilometer stylus when measured from the semiconductor side. For full wafers, with their circular symmetry, analytical generalizations of the Stoney equation[40] can be used to calculate quantitative values of stress in thick deposited films from the measured bowing[41, 42].

As an alternative to the use of organic additives, which is almost universal in commercial practice, alternating current plating was investigated. Some conditions of alternating current did lead to desirable modifications of both the gross distribution of Cu and of the surface roughness. However, these improvements were not sufficient by themselves to enable final processing of the wafers, and were accompanied by some increase in the film stress with respect to direct current plating. Furthermore, it proved quite difficult to reproduce some results of the alternating current plating trials.

Initial attempts to scale the metal substrate process to full wafers concentrated on the thick Cu plating. Some progress was made in modifying the stress of Cu deposits by compensating intrinsic stress with thermo-mechanical stress. By plating the Cu at reduced temperature, then warming the Cu/InP sandwich, the thermal expansion mismatch leads to a stress σ_{Cu}

$$\langle \sigma_{\mathrm{Cu}} \rangle \propto \mathrm{Y}_{\mathrm{Cu}} \Delta \mathrm{T} \cdot (\alpha_{\mathrm{InP}} - \alpha_{\mathrm{Cu}}) \tag{3.1}$$

where the brackets indicate an average over the Cu layer, Y_{Cu} is the biaxial modulus of Cu, and $\alpha_{\mathrm{InP}}, \alpha_{\mathrm{Cu}}$ are the respective expansivities. Any change in the intrinsic stress in the Cu due to lower temperature deposition turned out to be less significant than this thermo-mechanical stress, and wafers plated at reduced temperature were bowed less. Although alternating current plating (with pumping and filtration) resulted in markedly better surface roughness at 7°C, it seemed also to result in higher stress.

3.4.4 Lapping

Before discrete transistors were demonstrated free-standing Cu wafers, several otherwise successful runs had been lost to difficulties at the collector lithography stage. Roughness and non-planarity of the final plated surface

prevented vacuum chucking on the contact aligner. An o-ring vacuum chuck for the contact aligner was designed which could hold these wafers down, but this only changed the nature of the alignment problem rather than solving it. Faced with the inability to align collector lithography to the plated wafers, it proved necessary mechanically to lap the surface of the thick plated Cu before the wafers would hold down to the vacuum chuck. Initial attempts to plate $400\mu m$ of Cu had led to wafers which were too severely bowed to lap, and the thickness of Cu had to be reduced to $200\mu m$.

As noted above, the Cu/InP sandwich suffers from very bad thermal expansion mismatch. This precludes mounting of the Cu plated wafer by normal means to a stainless steel block for lapping. In common practice for laboratory III-V wafer lapping and back-thinning operations, the wafer to be lapped is adhered to a massive block with melted wax, and the assembly then cooled to room temperature before lapping proceeds. For practical waxes, temperatures of $75 - 120°C$ are used in this mounting operation. Bowing of the Cu/InP sandwiches under $50°C$ temperature excursions is visible to the naked eye. Even if such a bowed wafer could be mounted with wax, doing so would not help to achieve a plane parallel metal film. Vacuum chucking of the wafers for lapping was attempted; for this specific application, better chuck face design, and higher "soft" vacuum than present in the contact aligner were possible. Even so, the shear forces produced in lapping trial wafers exceeded the holding force of the vacuum chuck, and lapping could not be completed.

A temporary mounting method which allowed adequate lapping of the Cu wafer consisted of mounting the InP with epoxy to an improvised fixture. An epoxy with poor chemical resistance was chosen, and the mixing ratio intentionally altered from that recommended, in order to allow removal of the epoxy after lapping. Devcon "Five Minute Epoxy" served fairly well here, and could be removed in methylene chloride. In order to speed the process of dissolving the epoxy, a grooved lapping fixture was required. A segment of a steel file, ground flat, plated with Ni and then lapped, served this purpose. In order to maintain the chemical inertness of a final layer of Au, the lapping was performed between Cu plating and the final Ni and Au layers.

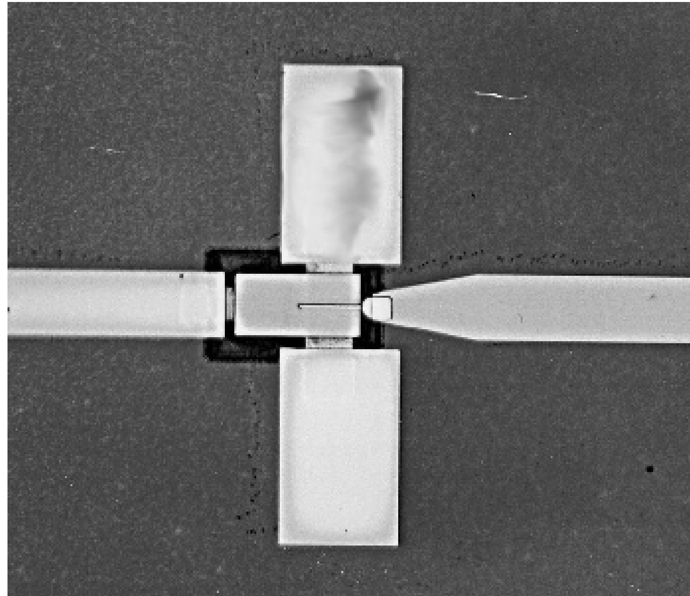


Figure 3.4: Microphotograph of HBT on free-standing Cu wafer.

3.4.5 Results

Discrete devices were fabricated on $200\mu m$ thick Cu quarter wafers using the epoxy mounted lapping scheme. A photomicrograph of one such device, which demonstrated $f_t = 110\text{GHz}$ and $f_{\max} = 200\text{GHz}$, is shown in figure 3.4. Alignment of the collector lithography was still problematic. Consequently, DC yield of devices was quite poor, and RF performance hampered by misalignment between collector and emitter. Even with the reduced thickness of plated Cu, the wafers were still bowed when mounted to the lapping fixture. Lapping smoothed the plated surface, but the Cu wafers were not planar after removal of the InP. The plating scheme used resulted in very large grained metal with a correspondingly low yield stress, and the Cu wafers were prone to bending inelastically in normal handling.

3.4.6 Discussion

A final layer of plated Au had been relied upon to protect the Ni and Cu from attack in the 9N HCl solution used to remove the InP substrate. Good adhesion of this Au layer was never achieved. While Au is routinely

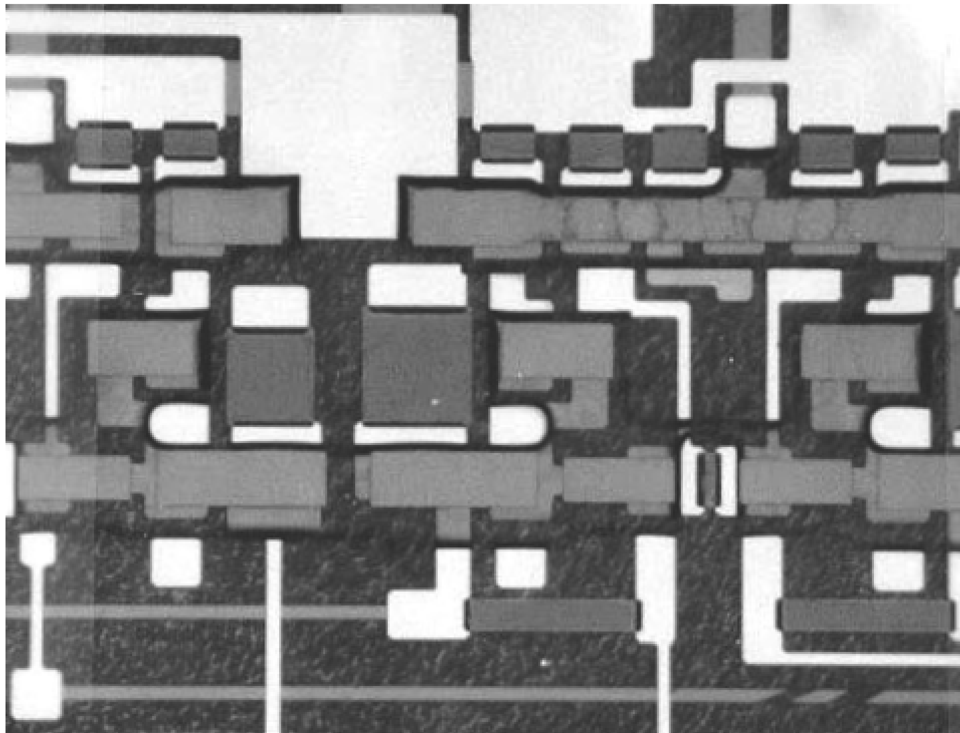


Figure 3.5: Microphotograph of integrated open circuits on free-standing Cu wafer. Process failed at collector lithography stage

plated on Ni surfaces in industry, it is commonly deposited from cyanide solutions. Nickel forms a passive oxide quite readily, and does so very quickly in alkaline solutions such as the $Na_3Au(S0_3)_2$ solution used here. Although immersing the Ni plated wafer in the Au solution with the current source already connected helped,adhesion was still poor. The inadequate adhesion of this Au protective layer, and the lack of Au at the edges of the plated area, contributed to metal ion contamination of the HCl etchant. This contamination manifested itself in colouring the etchant yellow–green, and in quickly decelerating the InP etch rate. Better adhesion of the gold layer might have been achieved by using vacuum deposition methods to deposit a suitable sticking layer and thin gold seed layer.

3.5 Thin Foil Process

3.5.1 Development/Method

Attempting to plate a metal layer thick enough to handle at wafer size presented such great difficulties that another route was attempted. The thickness of metal needed to handle individual dice would be much less, and plating this much might present fewer obstacles. Final lithography and processing of the thin metal wafer would demand mounting it to a temporary "carrier" substrate. Practically, this means that the wafer must be mounted before removal of the InP growth substrate. Thus, the means used to mount the wafer to its carrier must be compatible with the substrate removal etchant, the chemicals and temperatures of a resist cycle and with acetone used to lift off the collector metalization.

For the thin foil process, metal film thicknesses were set at $2\mu m$ for the initial Au layer, $1\mu m$ for the Ni diffusion barrier, $30\mu m$ for the plated Cu, and $1\mu m$ for a final Ni capping layer. Given the difficulties, noted above, with Au plating on Ni, a final layer of Au was not used here, but rather the wax used for temporary mounting was relied upon for protection.

Intrinsic stress and thermal mismatch stress were much smaller concerns in plating the relatively thin foil of metal. For this reason, the Au and Ni were plated at 50 –60°C to obtain better quality deposits. Also, the stress in Cu deposited at room temperature was tolerable. For the purposes of the initial demonstrations, simple DC current plating at 5.6 mA/cm^2 from a $CuSO_4$,H_2SO_4 solution without additives was used.

Waxes have long been used for temporary mounting operations in III-V wafer processing. A wax which was found to have convenient solvent solubility and insolubility was Apiezon W "black" wax. This material is soluble in toluene (as well as in chlorinated solvents which are increasingly unavailable), and not soluble in acetone. The suspended fine carbon black powder which gives the wax its black color does not serve any purpose in this application. Black wax softens appreciably at $85°C$, i.e. at temperatures below those encountered in the photoresist cycle.

A uniform, thin, film of this wax was here applied to the plated metal surface of the HBT wafer, and to the carrier wafer, by spin casting. Toluene proved overly volatile as a casting solvent, so mesitylene was substituted. This latter provides similar solvent action, but a significantly higher boiling point, and hence slower drying.

The flats of the (inverted) HBT wafer and the carrier wafers were aligned together on a jig then heated on a hotplate. This sandwich was then clamped under low vacuum in a fixture which made use of a flexible diaphragm to apply some two times atmospheric pressure to a stainless steel mandrel which pressed the sandwich to an anvil. The sandwich was heated to above the flow temperature of the wax while clamped in this manner.

Less evidence of metal dissolution was seen during substrate removal etching of Cu foil wafers. This improvement was attributed to the plated Cu and Ni being largely encapsulated in wax. After the substrate etch, wafers were baked on a hotplate, to drive off water, and photoresist applied. Where a delay intervened between the substrate etch and resist application, the wafer was cleaned on the spinner chuck with acetone and isopropanol dispensed from wash-bottles. At the expense of generating some solvent mist at the resist bench, this avoided potential wax contamination of solvent cleaning glassware.

The thin foil process described above yielded discrete transistors and simple integrated circuits (see section 5.1) on full wafers C and D. A photograph of wafer C, a full 50 mm wafer processed in this manner, is shown in figure 3.6. A problem which plagued these full wafers and the subsequent wafer E was that many NiCr thin film resistors deposited with evaporated Si underlayers were etched away in the substrate removal etch. In order to address this yield problem with the resistors, an additional process step was developed. PECVD SiO_2 was deposited over the entire wafer to a thickness of 4000 Å and patterned, with a buffered HF wet etch, into areas

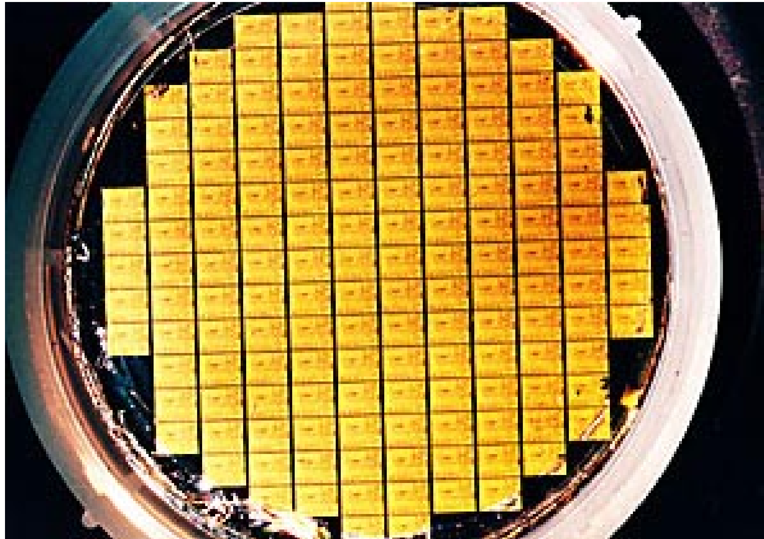


Figure 3.6: Photo of full 50mm wafer of transferred substrate HBT's, IC's. Each stepper field contains multiple discrete devices and integrated circuits, not intended for dicing.

extending some $3\mu m$ beyond the edges of the NiCr which was subsequently evaporated. The adhesion problems which had been associated with evaporated Si underlayers were circumvented by depositing the NiCr directly on the underlying silicon dioxide. While the resistor yield was greatly improved by this new process step, the measured sheet resistance of the NiCr was increased dramatically. Inspection of the oxide and NiCr under DIC/Nomarski microscopy suggested that the deposited oxide surface was extremely rough – rougher than the dry-etched InAlAs surface beneath it. It is believed that excessive roughness of the oxide broke the continuity of the NiCr film and so increased its apparent resistivity.

3.5.2 Discussion

The o-ring front surface sealing fixtures developed here were not entirely successful. While fluid flow was not impeded so badly by the full wafer fixture, other problems remained. The sealing was imperfect, particularly when the fixture was immersed in heated solutions. Leakage into and out of the dry space in the fixture provided a source of contamination to subse-

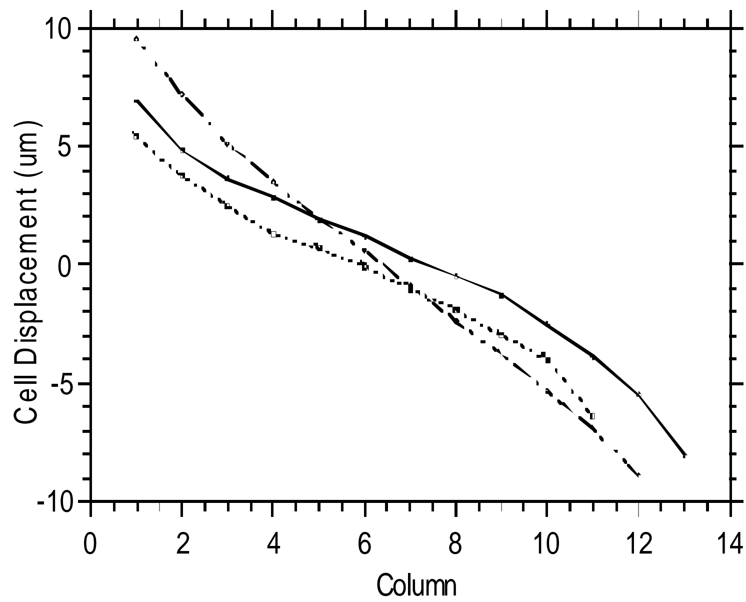


Figure 3.7: Wafer shrinkage on three separate foil wafers, measured using stepper as measuring microscope. Cell width was 3.5 mm; wafer shrinkage $\approx 0.03\%$.

quent plating solutions. Also, excess plating tended to occur at the o-ring seal to the wafer, leaving a raised lip of metal. Replacement of the o-ring after each used helped slightly. This raised lip impacted wax bonding, and would be an impediment to efforts to mount a thin foil wafer to e.g. a probe-station wafer chuck. An enhancement of the plating rate at edges would be expected regardless of how these edges are defined, however, and mechanical planarization may be necessary in any event. Such mechanical planarization would have the additional potential benefit of yielding a smoother surface for die bonding to a metal submount.

The wax mounting procedure used in the full wafer process demonstrated here is far from adequate. The InP wafer could be seen routinely to have broken in the vacuum clamping fixture. While this did not separate the ground plane into multiple pieces, it did impact both the substrate etch, and the collector lithography step. Manual alignment on the stepper revealed that distinct regions, presumably corresponding to the separate pieces of the broken InP wafer, of the foil wafer were translated and rotated with respect to one another.

In the absence of a highly planar metal surface, application of the mounting wax by spin casting is inappropriate. Wax solutions can not be relied upon to planarize much topography. In particular, spin-cast wax will not planarize over the edge of the plated metal, or the raised lip of metal noted above. The perimeter of the wafer which is not plated with a ground plane has been left unsupported after the substrate etch, and tends to break up and shed particles.

There is a tradeoff between a wax melting temperature high enough to allow the lithography cycle and low enough to allow successful mounting of the wafer. The Apiezon W wax arguably errs on the side of too low a melting point. It was found that the collector lithography photoresist bake led to substantial changes in the planarity of the wafer sandwich. Whereas the silicon carrier wafer would hold down on the stepper vacuum chuck before the photoresist bake, it would not do so immediately afterwards. After a delay of about three hours, the silicon carrier repeatably flattened enough to hold down on the chuck. It is surmised that the bowing of the sandwich by thermal mismatch stress integrated from the wax softening temperature down to room temperature leads to cold flowing of the wax bond layer in this interval. Two approaches to this difficulty which might be pursued in future are 1) to develop a reduced temperature photoresist

bake process or 2) to bond the sandwich with a higher temperature wax which does not soften during the photoresist cycle. Of course, the latter option may present equal difficulties with bowing of the sandwich at the mounting stage.

The problems inherent to bonding a bimetallic disk to a support wafer with a thermoplastic might best be avoided entirely. Epoxies are capable of forming a strong bond at room temperature. An epoxy able to withstand immersion in the substrate etch and the whole collector lithography process is not particularly likely to be easily removed however. A process which might be made to work would be to coat the HBT wafer with a release layer after plating. This layer could even be a higher melting point wax. Rather than bond the wafer to a carrier at elevated temperature, though, what is suggested here is to bond the release layer to a carrier with a room-temperature curing epoxy. After final processing, the release layer could be dissolved away, and the epoxy coated carrier wafer discarded.

In the context of the thin foil process, the advantages of Cu may be outweighed by the complications introduced by its use. Intrinsic stress is certainly less of a problem in the thin foil than in a full thickness metal wafer. The plated copper layer had to be separated from underlying Au metalization by a diffusion barrier, and the Cu furthermore had to be protected from the InP removal etch. Plating a relatively thick layer of Au alone would eliminate the multiple step plating procedure, and any reduction in the yield stress of the foil might be acceptable. The yield stress of plated Cu films may be as low as 70 MPa[39], while the yield stress of plated Au is on the order of 30 MPa[31].

Insofar as the goal of any integrated circuit technology is to yield packaged functioning systems, some means to dice the processed wafers is needed. From this point of view, the practical relevance of IC's on a $200\mu m$ thick Cu substrate is quite limited: conventional dicing saws do not handle thick metals well. The thin foil process described above has more promise of allowing dicing. Indeed, temporary wax mounting of the wafer does not demand that the ground plane be continuous. Plating the ground plane only in discrete areas separated by photoresist filled scribe streets could essentially define the dicing of the wafer lithographically.

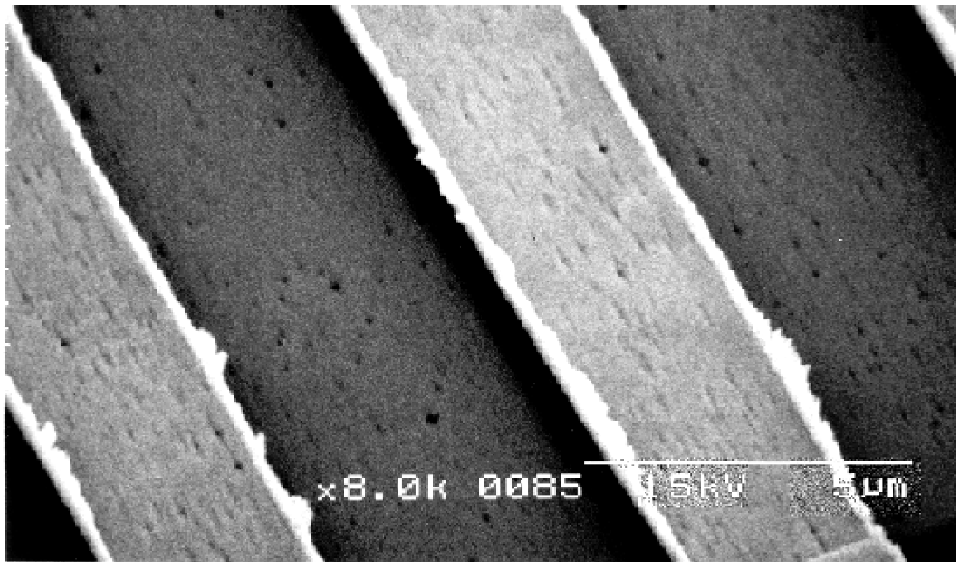


Figure 3.8: SEM showing pitting of collector semiconductor. Pits are replicated in the Collector metalization stripes running diagonally across image. Note that the resolution of image is exceptional for clean room SEM.

Chapter 4

Microwave Bipolar Power Transistors

In the present work, large area multi-finger transistors were implemented for the first time in the transferred substrate HBT technology. Millimeter wave large-signal amplifiers based upon these devices will be presented in chapter 5.

In this chapter, some background to the design of microwave power transistors is developed in section 4.1, and the power transistors designed here are presented in section 4.2. Small and large signal models for HBTs are presented in sections 4.6.1 and 4.3 respectively. In the former section, a method for the extraction of model parameters from measurements of actual devices is explained. In section 4.6.2 a small signal model of transistors from the wafer which yielded the power amplifier results of chapter 5 is extracted in this way.

4.1 Microwave Power Transistors

Power amplifiers are designed to maximize the power delivered from a given device, subject to some constraints on linearity. Power amplifiers operating at the highest frequencies are biased in class A. The power delivered by such an amplifier is

$$P = \frac{1}{8}\Delta V \times \Delta I \tag{4.1}$$

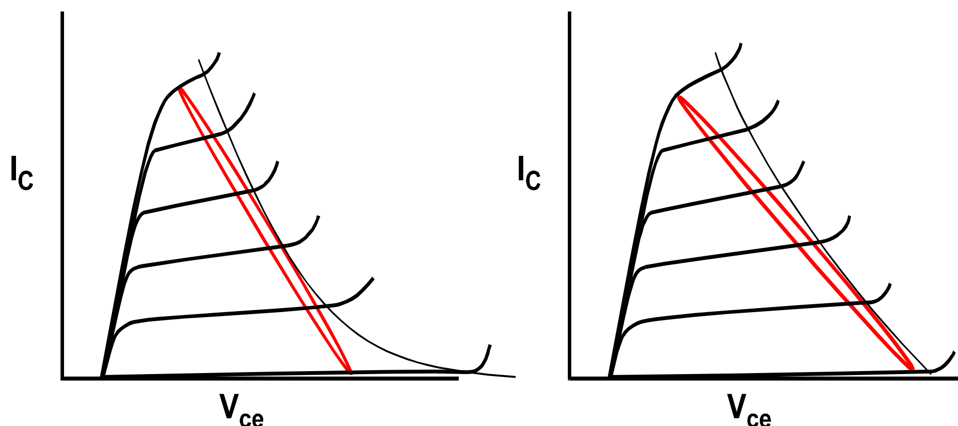


Figure 4.1: Sketches of allowable large signal dynamic load lines for two hypothetical devices. The breakdown voltage BV_{ceo} of the device in the left graph is substantially higher, but the output power obtained from that on the right is higher.

The maximum power output of the amplifier is achieved when the load line traversed is such that ΔI and ΔV correspond to physical limitations of the device. Thus the current excursion is from 0 to $I_{\max}$ and the voltage excursion is usually from the relevant "knee" voltage to the zero-current breakdown voltage. For an HBT, $I_{\max}$ may be set by electrostatics (i.e. the onset of the Kirk effect) or by limitations on dissipated power density. In most bipolar transistors, the relevant "knee" voltage is determined by the edge of the saturation region.

Operating with V_{ce} below the zero-current breakdown voltage is not necessarily sufficient. Where the breakdown voltage is a strong function of current density, the constraint relevant for nearly linear operation should be that the load line not enter the breakdown region. As sketched in figure 4.1, a device with lower BV_{ceo} may deliver more power than one with higher breakdown voltage but adverse breakdown contour.

At frequencies close to the bandwidth of the transistor, the concept of a dynamic load line should be examined closely. At such frequencies, the displacement currents in the collector base capacitor can approach the magnitude of currents due to injected carriers. Nonetheless, the power amplifier circuit is designed according to the dynamic load line in the electron current $I_{C,\text{cond}}$ voltage V_{ce} plane. The physical limits on current density in the de-

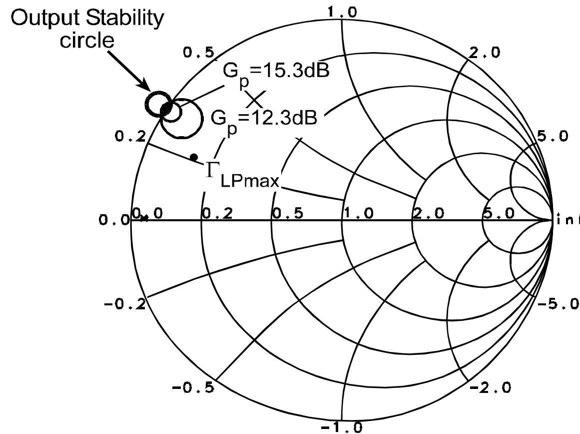


Figure 4.2: Operating power gain circles and load reflection coefficient for maximum power output, $\Gamma_{\mathrm{L,Pmax}}$ for a nominal device model of a $4 \cdot (1 \times 25\mu m^2)$ emitter HBT in common base configuration.

vice apply to electron current. Furthermore it is the electron current which confers power gain in the transistor.

Note that the load impedance yielding the maximum saturated output power, $\Gamma_{\mathrm{L,Pmax}}$ does not in general correspond to the load for maximum small signal gain. This is illustrated in figure 4.2 where operating power gain circles and the large signal load for a nominal device model (see section 4.3) are compared.

4.1.1 Large Devices

RF power transistors, be they bipolar or field effect, are built as multi-finger structures. Breakdown voltages are determined by material parameters; for a given device structure increases in output power can only be had by increasing the output current. Permissible current densities in HBTs are limited by electrostatics, or by junction temperature rise. Practical device design maintains a constant periphery to area ratio as the junction area is increased. Practical large area bipolars consist of multiple emitter fingers.

The layout of multi-finger devices becomes quite critical at mm wave frequencies. Dissipated power density must be traded off against wiring parasitics and delays in choosing the spacing of fingers. Particularly in a scaleable bipolar device, an explicit tradeoff must be made between overall

power density and individual finger performance. HBT's have long been said to have the advantage over HEMT's in power density because current flows vertically in an HBT through an area much greater than the channel cross-section of a HEMT of similar overall size. This advantage rested on the fact that HBT's had never been scaleable devices. Transferred substrate processing has provided a route to aggressive lithographic scaling of HBT's which does not require significant improvements to the base ohmic contact technology. For a fixed base contact technology, the ratio of emitter area to base contact area of the transferred substrate HBT decreases when the emitters are scaled to narrower widths in order to improve high speed performance — and so bandwidth will tend to come at the expense of power density.

Multiple fingers of large transistors are combined at several levels. The interconnection of multiple fingers in parallel by wiring of negligible electrical length will here be referred to as "lumped" combining, whereas interconnection of sub elements of a larger transistor by wiring which is explicitly phase-matched will be referred to as "distributed combining."

The degree to which transistor area may be combined at the lumped level is limited either by wiring delays or by constraints on impedance transformation. A common rule of thumb pertaining to the lumped combining of fingers is that the delay between fingers of the device should not exceed one eighth the signal period[22]. At 100 GHz and assuming $\epsilon_{\text{eff}} = 2.2$, this limits the dimension of the lumped structures to $\approx 260\mu m$. Paralleling increasing junction areas reduces the impedance looking into the transistor terminals. Once the resistance looking into the transistor ports becomes comparable to resistive losses in the associated reactive matching network, further paralleling leads to diminishing returns[43, p364].

Still larger junction areas are achieved by distributed combining. In the archetypal corporate power combining scheme, the outputs of of transistor elements are combined by a binary tree of networks with appropriate impedance transformation properties e.g. Wilkinson combiners. While the output powers which can be achieved by corporate power combining either on or off chip are significant (see e.g. [44]), the overall impedance transformation achievable in this way decreases with increasing frequency. Given a minimum allowable impedance Z_{min} presented to the (combined) transis-

tor(s),

$$P_{max} = \frac{(\Delta V)^2}{Z_{min}} \tag{4.2}$$

and in the usual regime where BV $\propto T_c$ and $f_t \propto (T_c)^{-1}$, $P_{max} Z_{min} f^2$ is a constant for a given collector material.

Perhaps the single most salient feature of the design of power bipolar transistors is the need to consider thermal stability. The diode equation dependence of collector current density on base emitter voltage

$$J_C = J_s \left(\exp\left[\frac{q \cdot V_{be}}{nk_B T}\right] - 1 \right) \approx K \exp\left[\frac{q \cdot V_{be} - nE_g(T)}{nk_B T}\right] \tag{4.3}$$

is a crucial liability of the bipolar transistor. Where transistor junctions are connected in parallel, i.e. with a common value of V_{be}, any junction with a higher temperature will draw a disproportionate share of the total current – and so get hotter still. The current distribution between emitter fingers, and indeed within any one finger, is stabilized with respect to perturbations of the local temperature by emitter resistance. The minimum value of ballast resistance required to assure thermal stability in an HBT was derived by Gao et al[45]. Neglecting any temperature dependence of the ballast resistor's value, the minimum total emitter resistance for thermally stable operation was shown to be

$$R_{E,min} = -\frac{\partial V_{BE'}}{\partial T} \cdot \frac{dT_j}{dI_e} - \frac{nk_B T_j}{qI_e} \tag{4.4}$$

where $V_{BE'}$ is the internal base emitter voltage. The derivative $\partial V_{BE}/\partial T$ amounts to approximately $-0.95\,\mathrm{mV\,K^{-1}}$[46]. Assuming a constant thermal resistance from junction to case,Θ, $T_j = T_c + \Theta I_c V ce$ and $dT_j/dI_e = V_{ce}\Theta$ giving

$$R_{E,min} \approx (0.95\,\mathrm{mV/K}) V_{ce}\Theta - \frac{nk_B(T_c + \Theta I_e V_{ce})}{qI_e} \tag{4.5}$$

It is usually necessary to provide emitter degenerating resistance in excess of the emitter contact resistance, to assure thermally stable operation. This excess emitter resistance, commonly referred to as "ballast" or balance resistance, degrades RF performance of the transistor[47]. The emitter contact resistance may be increased intentionally to implement this balancing resistance in devices specialized for power amplification alone [22], but this

solution is not generally acceptable where a common layer structure is used for small signal and power transistors. In this latter case, external resistors must be connected to each emitter finger individually.

While the RF effect of the ballast resistors can in principle be reduced by bypassing $R_{ballast}$ with a capacitor, the capacitance C_{byp} required to have much impact at the operating frequency f,

$$C_{byp} > (2\pi R f)^{-1} \tag{4.6}$$

is not often practically realizable.

4.1.2 High Speed Under High Bias

A severe trade off in the design of millimeter wave power transistors is between device breakdown voltage and bandwidth. Carrier times-of-flight and hence current delays are of course strongly linked to the distances traversed. Increases in breakdown voltage attained by increasing the thickness of depletion regions by ΔT will come at the expense of transit times which increase at least linearly with ΔT. The familiar figure of merit $F_{br} \cdot v_{sat}$ for semiconductors, which gives rise to a limiting product PZf^2 for each material[47], may not strictly apply for highly scaled devices. The saturation velocity v_{sat} pertains to thick layers. Injected electrons may traverse very thin collectors without gaining enough energy to scatter into higher energy conduction band valleys and so to be slowed to v_{sat}. Also, for thin layers of semiconductor, the bulk value of breakdown field F_{br} does not necessarily apply. Impact ionization can only take place when hot carriers gain more energy than E_g, and so the bulk value of breakdown field may be exceeded in thin layers, provided that $q \cdot V_{CE} < E_{g,col}$.

Common emitter breakdown voltages in InGaAs collectors HBTs are very strongly related to injected current density. In the lightly doped collector structure used, the electric field at the collector end of the collector-base space charge region is increased by band-bending due to injected electron densities $n \gg N_d^+$, as illustrated in figure 4.3. This field redistribution leads to increased impact ionization rates. Also, the collector temperature rises with increasing power dissipation. The electron impact ionization coefficients in InGaAs are noteworthy for rising with increasing temperature[48]. Also, the bandgap of InGaAs is such that carrier generation rates in the

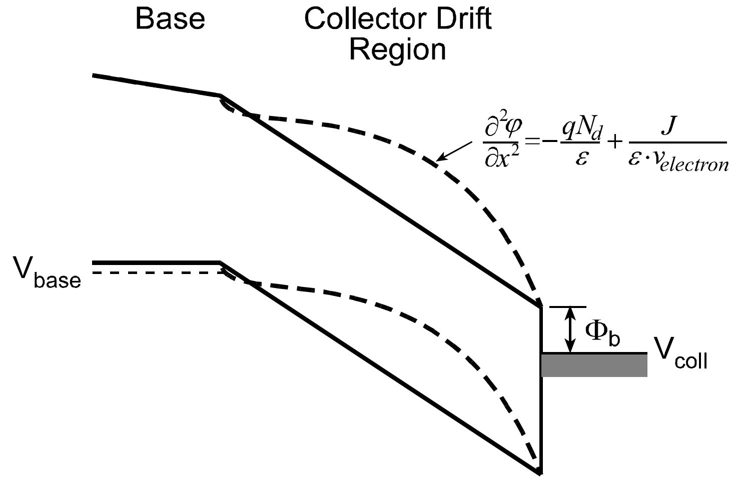


Figure 4.3: Schematic band diagram illustrating field enhancement at Schottky contact under high injection.

collector space charge region rise to significant levels with moderate temperature rises. This leads to output characteristics with poor output conductance, and hastens the onset of common emitter breakdown.

The bandwidth of an HBT is by no means independent of operating temperature. Carrier scattering rates increase with temperature, and consequently f_t is seen to decrease with increasing temperature[46]. Even where breakdown phenomena do not limit the allowable dissipated power density, the need to retain device bandwidth may do so.

4.1.3 Measuring Power Transistors

Characterization of power transistors is a significant problem in itself. Practical transistors are not unilateral amplifiers. High performance transistors are often potentially unstable over broad bandwidths, and can oscillate when presented with some impedances– even purely resistive impedances. Microwave wafer probes and broad band bias tees can present a controlled impedance to the device under test over a very broad bandwidth, but below the low frequency cutoff of the bias tee, this impedance is uncontrolled. This fact has implications for DC and RF testing of power devices: it may not be possible to suppress device oscillation with the use of controlled impedance on wafer microwave probes and off-wafer termination. Some form of inte-

grated matching and stabilizing network is required for RF testing of any device which is either not stable under 50Ω termination or unstable at low frequencies when terminated with bias tees.

In any event, the signal to noise ratio of RF measurements is degraded by the large reflection coefficients of large area devices. Whereas at frequencies below 50 GHz, the available network analyzer offers adjustable source power levels, the same is not true of the available 75–110 GHz network analyzer. This latter test set, and the newly acquired 140-220 GHz test set are designed to operate with the signal sources heavily saturated. The signal levels involved may be sufficient to over-drive small devices, but the signal to noise ratio of measurements on large area devices without reactive matching will be low.

4.2 Multi-Finger Designs

Most power HBT's in the literature have been designed in the so-called "herring-bone" configuration[49] in which two rows of emitter fingers straddle a signal feed. This configuration is required in part to make ohmic contacts to the sub-collector of double mesa HBT's in close proximity to the emitter base junction. Given that the emitter and collector are accessed from opposite sides of the semiconductor film in the transferred substrate HBT, and that a metal contact runs the length of the collector, there is less incentive to use a herring-bone layout. Since the objective here was to build transistors which would develop moderate powers at the very high frequencies where the performance of the transferred substrate HBT is exceptional, unusually compact layouts were chosen. In all of the designs in this work, a merged base mesa was used; this saves the space needed for etching an isolating gap and, more importantly, greatly simplifies the wiring.

Common emitter devices with four and eight emitter fingers, each one $1\times25\mu m^2$ and aligned to a collector finger of $2\times29\mu m^2$ were designed. Each emitter finger was connected to a ballast resistor with wiring in metal one. The four finger common emitter device was designed specifically for the amplifiers described in chapter 5, and the layout of this device is shown in figure 4.4. The area of overlap between metal one and metal two serving to heatsink each finger of this device across the Si_3N_4 layer was $4\times27\mu m^2$. This four finger device is heatsunk by two ground vias, each $19\times16\mu m^2$ in area. Following the approximate calculations of section 2.6.1, the components

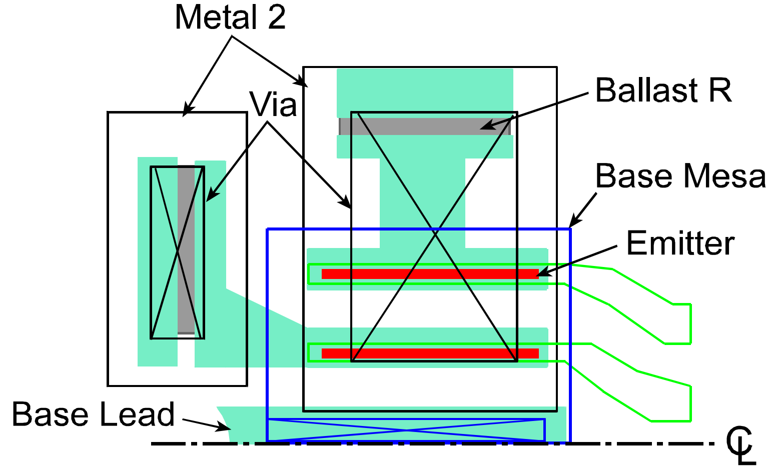


Figure 4.4: Diagram showing layout of two multi-finger transistors of a cascode cell, with emitter ballast resistors, and separate connection to each emitter finger of common base device.

of the thermal resistance of this multi-finger transistor are estimated to be: $R_{emit} = 550\text{KW}^{-1}$; $R_{SiN_x} = 205\text{KW}^{-1}$; $R_{via} = 27.5\text{KW}^{-1}$; $R_{subst} = 11.5\text{KW}^{-1}$. When this device is operated at 1.5 V V_{CE} and 50 mA I_C, the corresponding temperature rises are 41° C across the emitter mesa, 15° C through the Si_3N_4 and a further 3° C through the metal substrate. While the thermal resistance of the via and that through the body of a $30\mu m$ Cu substrate are slightly increased by the dense layout, the total thermal resistance of the transistor is totally dominated by components within the semiconductor and SiN_x.

The layout of a four finger grounded base transistor used in the amplifier discussed in section 5.3 is shown in figure 4.5. By virtue of the thin deposited microstrip dielectric process, the ground via overlaps much of the device mesa, and three contacts between the base metalization and the via are located between the emitters. As above $R_{emit} = 550\text{KW}^{-1}$. Heat is removed from the emitters through the SiN_x over a total area of $4(4 \times 18\mu m^2) = 288\mu m^2$, giving rise to $R_{SiN_x} \approx 290\text{KW}^{-1}$. The thermal resistance of the via is approximately $17\,\text{KW}^{-1}$, and the resistance through the Cu substrate an additional $34\,\text{KW}^{-1}$. If this device is operated at $I_C = 50$ mA and $V_{CB} = 2\,\text{V}$, the temperature rises are 74° C across the emitter mesa, 39° C

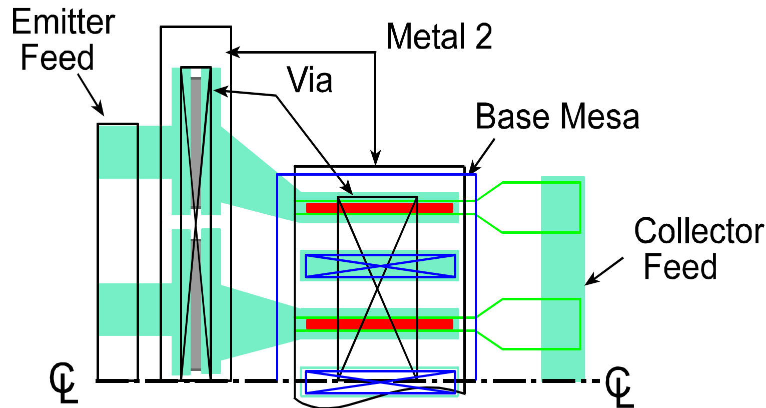


Figure 4.5: Diagram showing layout of common base power transistor with emitter ballast resistors

across the Si_3N_4, 2° C in the via and 5° C through the body of the substrate.

While the emitter mesa thermal resistance dominates the total for the above devices with InAlAs/InGaAs emitters, this situation will change with the introduction of InP emitters. Under the consequent 15 times reduction in Θ_{emit}, $\Theta_{\mathrm{SiN_x}}$ will dominate the thermal resistance of these devices. In the case of common emitter devices, the (heat) conducting area of SiN_x can be increased somewhat without severe performance penalty. On the other hand, for a common base device the capacitance to ground introduced by the ground via, which heat sinks the emitters and emitter ballast resistors across the SiN_x layer, is a significant parasitic. Considering that the introduction of epitaxial InP layers to the HBT structure will greatly increase the breakdown voltages and hence the feasible power dissipation of transistors, the thermal resistance of the SiN_x layer will be a major issue. Clearly, dielectric materials with superior ratios $\kappa_{th} : \epsilon_r$ to that of SiN_x would be desirable here, but such materials may not be available at UCSB in the near term.

Ballast resistors with a nominal value of 5Ω were connected to each $1 \times 25 \mu m^2$ emitter in the above multi-finger designs. This value was arrived at in part with reference to other mm-wave power HBT's in the literature, and in part because it represented a practical minimum value given the limitations of interconnect patterning and the 50Ω/□ sheet resistance NiCr process. In fact, the 5Ω ballast resistors were implemented with a

contact separation already less than the recommended minimum of $4\mu m$; smaller value resistors implemented with the $50\Omega/\square$ NiCr would necessarily consume more area.

4.3 Large Signal Modelling

Measurements of transistors in non-linear operation enable the design of highest performance power amplifiers. For microwave transistors, the relevant measurements are so-called load-pull measurements, in which the transistor performance is measured under large signal drive and a wide range of load impedances. Load pull measurements were not made of the devices used in the present work because no practical measurement system existed in the frequency range of interest. Passive load-pull systems using mechanical tuners can not synthesize very high reflection loads because of losses in the tuners. For on-wafer measurements at high frequencies, the losses in microwave probes further severely limit the range of impedances available to passive load-pull. Active load-pull systems at W band remain prohibitively expensive.

In the absence of large-signal measurements, the approximate device modelling technique of parasitic absorption was used in the present work. The basic principle of this technique is to separate the parasitic elements of the device model from a fictitious "intrinsic" device. By designing a matching network to load this "intrinsic" device with the desired load resistance, $\Gamma_{L,Pmax}$ of the actual device can be approached[50, p 336].

The parasitic absorption model used in design work herein was synthesized from a small signal device model extracted from network analyzer measurements. The parasitic capacitances C_{cbi} and C_{cbx} were removed from the "intrinsic device, along with R_{ex} and R_{bb} as shown in figure 4.6.

The large signal model synthesized in this way is clearly only approximate. The SPICE Gummel Poon "intrinsic" device should model the large signal electron current, exclusive of breakdown, fairly well. However, the composite model does not reproduce any of the bias sensitivity of C_{cb} observed in actual devices. Note in particular that the values of C_{cbi} inferred from measurements of transferred substrate HBTs biased for peak $f_{\max}$ will be significantly less than those pertaining under class A bias for power amplifiers.

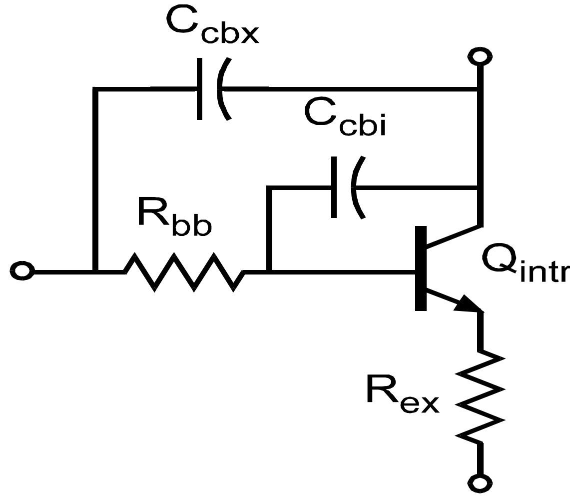


Figure 4.6: Schematic diagram of parasitic absorption approximate large signal model of HBT. The transistor labeled Q_{intr} is implemented with a SPICE Gummel-Poon BJT model with R_{bb},C_{cb} and R_{ex} set to zero.

4.4 Device Results

In this and subsequent sections, transistors from a solder bonded quarter wafer, which will be referred to as wafer G, are presented. This particular wafer is discussed in detail because it is on this wafer that power amplifiers were successfully fabricated. While the same mask set was used to process wafer E and wafer F in the thin foil copper substrate process, no working circuits were obtained from these wafers. Essentially all of the NiCr thin film resistors from wafer E were destroyed in the substrate removal etch. While the PECVD SiO_2 layer added to protect resistors on wafer F served its purpose, transistors on this wafer suffered from gross collector base leakage currents.

The HBT epitaxial layer structure of wafer G is given in table 4.1.

4.5 DC Characterization

Common emitter devices with four emitter fingers each $1 \times 25\mu m^2$ and four $2 \times 29\mu m^2$ collector fingers were fabricated and tested on wafer G. The DC characteristics of one such transistor, with resistors of nominally

Description	Material	Thickness (Å)	Doping (cm^{-3})
n+ Emitter Cap	InGaAs	1000	10^{19} Si
Grade		200	10^{19} Si
n+ spacer	InAlAs	700	10^{19} Si
Emitter	InAlAs	500	8×10^{17} Si
Digital Alloy	33 Åperiod	233	8×10^{17} Si
linear grade		66	2×10^{18} Be
Graded bandgap Base	$In_{0.455}Ga_{0.545}As \rightarrow In_{0.53}Ga_{0.47}As$	400	5×10^{19} Be
Collector	InGaAs	400	10^{16} Si
n+ Delta Dope	InGaAs	50	10^{18} Si
n- Collector	InGaAs	2550	10^{16} Si
Growth Buffer	InAlAs	2500	UID

Table 4.1: Epitaxial layer structure of wafer G. InGaAs and InAlAs here refer to the compositions lattice matched to InP, i.e. $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$.

5Ω degenerating each emitter finger, are shown in figure 4.8[1]. Whereas $BV_{ceo} > 2.8$V, the breakdown voltage drops to $V_{ce} \approx 1.3$V at high currents. Transistors of identical geometry but without any external ballast resistors were seen to fail catastrophically for $V_{ce} = 1.2$V and $I_C > 50$mA.

Discrete common base transistors with a single $1 \times 25\mu m^2$ emitter, $2 \times 29\mu m^2$ collector finger were included on the mask set. The DC common base characteristics, shown in figure 4.9, of one such device on wafer G exhibit a strong dependence of breakdown voltage on current density. A breakdown voltage BV_{cbo} of > 6V drops to < 1.5V at currents over 14 mA. Even as the collector base junction temperature rises with dissipated power, the peak electric field in the collector increases due to compensation of the ionized donors in the collector by injected electrons. Catastrophic failure of the device tends to coincide with the first clear sign of breakdown in

[1]Curve-tracer-like foldback measurements are easily made on the HP 4145 semiconductor parameter analyzer by connecting an appropriate resistor in series between the "source-measure-unit" output and the DUT, then measuring the collector voltage applied to the DUT with one of the voltage monitor inputs.

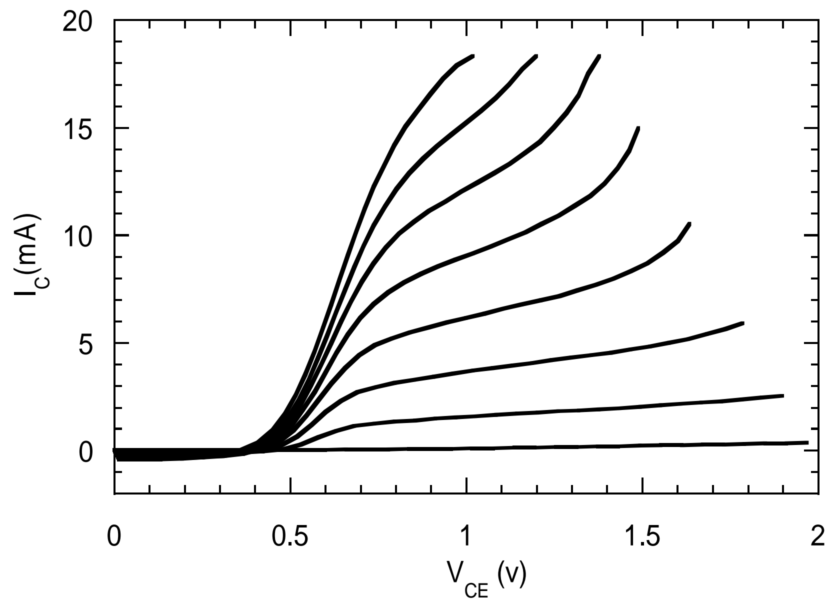


Figure 4.7: Common emitter characteristics of device with a single $1 \times 25 \mu m^2$ emitter finger, and corresponding $2 \times 29 \mu m^2$ collector.

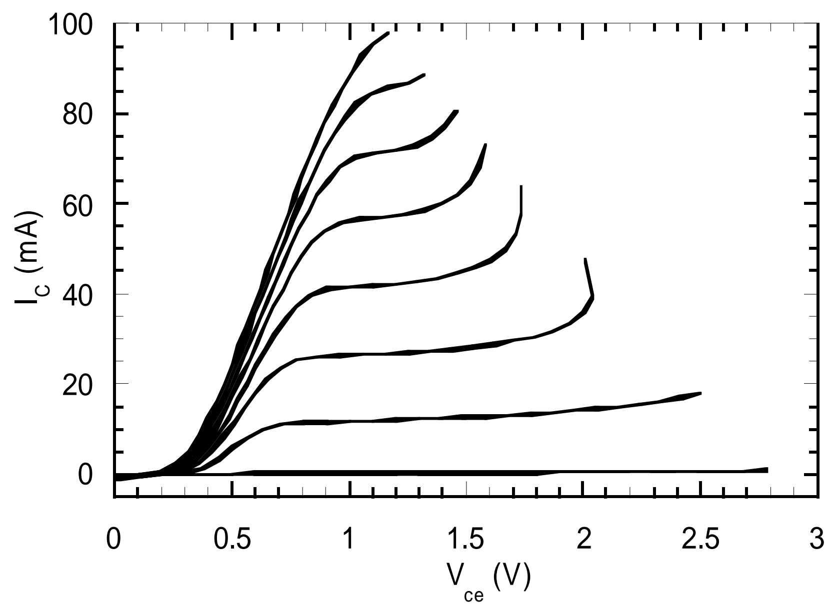


Figure 4.8: Common emitter characteristics of four finger device with four emitter fingers each $1 \times 25\mu m^2$ and four corresponding $2 \times 29\mu m^2$ collector fingers. Base current steps of $400\mu A$.

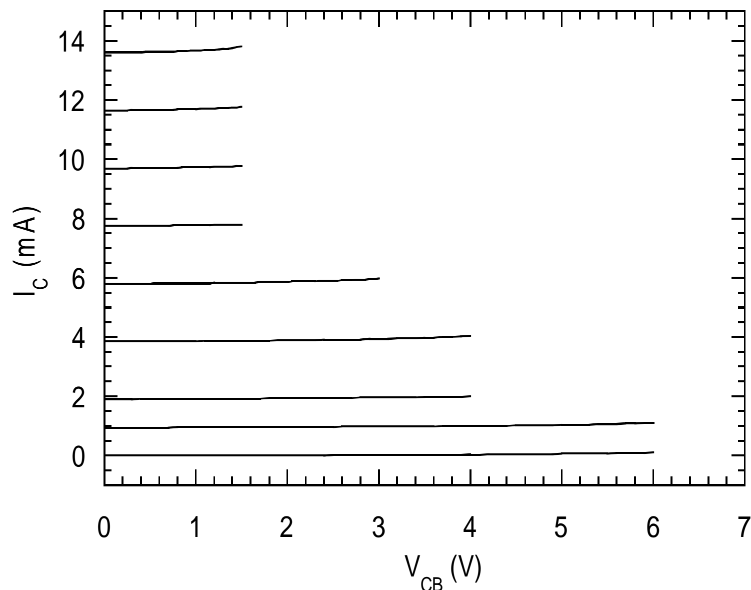


Figure 4.9: Common Base characteristics of $1 \times 25\mu m^2$ emitter, $2 \times 29\mu m^2$ collector common base device.

the I_C V_{CB} characteristic, even when external series resistors are included in the collector circuit; this may be because the reverse biased Schottky collector presents ≈ 0 contact resistance, and so does not serve to stabilize the current distribution throughout the collector area.

4.6 Small Signal Characterization

The W-band network analyzer measurements of discrete devices were calibrated with on-wafer line-reflect-line (LRL) standards[51], with the reference planes offset by $293\mu m$ from the probe pads. The long offset has been shown[52] dramatically to improve the accuracy of measurements of S_{12} of high f_{max} devices. This calibration methodology does however refer all measured quantities to the characteristic impedance of the transmission lines on wafer, which impedance is not exactly 50Ω. S parameters in the

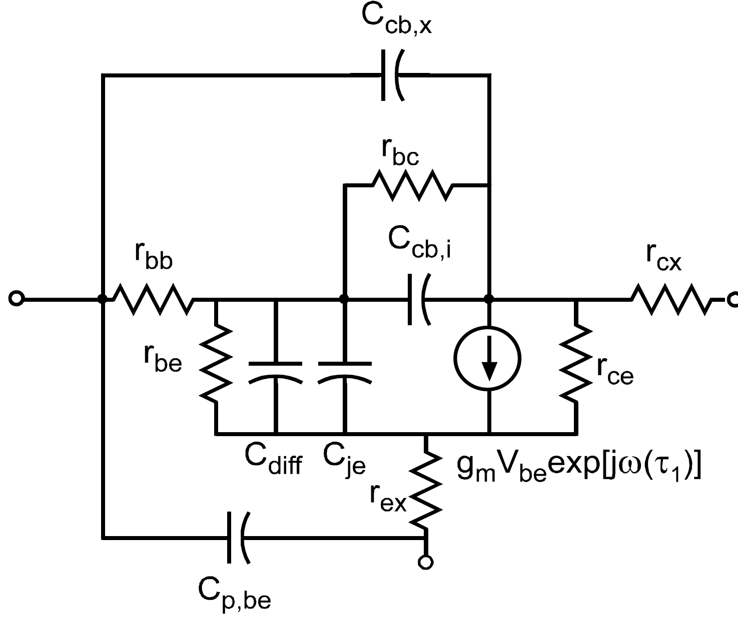


Figure 4.10: Hybrid Pi model of HBT

following are nonetheless referred to 50Ω reference impedance.

4.6.1 Small signal model

Small signal characteristics of HBTs are modelled here with a hybrid pi equivalent circuit. The parameter extraction procedure follows from analysis of this equivalent circuit, which is shown in figure 4.10.

The extrinsic emitter resistance is extracted from measured values of Y_{21} at low frequency. Inspecting the equivalent circuit, and neglecting R_{cx}, Y_{21} at DC is given by

$$Y_{21}|_{f=0} = \left(\frac{1}{g_m} + (1 + 1/\beta)R_{ex} + \frac{r_{bb}}{\beta}\right) \tag{4.7}$$

If $r_{bb} \ll \beta(R_{ex} + 1/g_m)$, then $Y_{21} \approx (1/g_m + R_{ex})^{-1}$. This equation holds for $f \ll f_\beta = (2\pi R_\pi(C_\pi + C_{cbi}))^{-1}$. Since

$$g_m = \frac{qI_c}{nk_BT} \tag{4.8}$$

a linear regression of Y_{21}^{-1} vs. I_c^{-1} yields an intercept of R_{ex} and a slope of nk_BT/q – under the assumption that the junction temperature is the same at all bias points measured.

Measurement of H_{21} at $f \ll f_\beta$ yields the dynamic current gain β. Knowing β, we can calculate $R_{be} = \beta/g_m$. Some care must be exercised in making low frequency measurements that small devices are not over-driven. For internal voltages $v_{be} > kT/q$, device operation cannot be approximated as linear. Network analyzers can readily supply enough source power at low frequencies to overdrive small devices in this way.

Neglecting r_{cx}, Y_{12} of the hybrid pi model is

$$Y_{12} \approx \left(\frac{1}{r_{cb}} + \omega^2 C_{cbi}^2 r_{bb}\right) + j\omega\left(C_{cbx} + C_{cbi}\right) \tag{4.9}$$

The total collector base capacitance $C_{cb,tot} = C_{cbx} + C_{cbi}$ can be extracted from a linear regression of $\mathrm{Im}\left[Y_{12}\right]$ vs. frequency.

Again neglecting r_{cx}, the current gain cutoff frequency of the hybrid pi model is given by

$$\frac{1}{2\pi f_\tau} = \tau_f + r_{ex}\left(C_{cb} + C_{\mathrm{p,be}}\right) + \frac{nk_BT}{qI_e} \cdot \left(C_{cb} + C_{je} + C_{\mathrm{p,be}}\right) \tag{4.10}$$

f_τ is computed from measurements over a range of emitter current densities. Extrapolating $1/f_\tau$ vs. $1/I_e$ to zero inverse current, yields an intercept $\tau_f + r_{ex}\left(C_{cb,tot} + C_{\mathrm{be,ild}}\right)$ and slope $nk_BT/q \cdot \left(C_{cb,tot} + C_{je} + C_{\mathrm{be,ild}}\right)$. Given an estimate for $C_{\mathrm{be,ild}}$, the transit time τ_f and base-emitter junction capacitance C_{je} are determined from this linear regression. Although the junction temperature is necessarily higher at the higher bias points, and the collector space charge transit time is sensitive to current density in high performance HBT's, the linear regression often fits measured data quite well.

The base parasitic resistance R_{bb} is extracted by fitting the hybrid pi model to measured Y_{11}. For a highly simplified hybrid pi model – neglecting C_{cbx}, r_{ex} and r_{cx} –

$$Y_{11} = \frac{1}{r_{be} + r_{bb}} \cdot \frac{1 + j\omega r_{be}(C_{je} + C_{diff} + C_{cbi})}{1 + j\omega\frac{r_{bb}r_{be}}{r_{be}+r_{bb}}(C_{je} + C_{diff} + C_{cbi})} \tag{4.11}$$

assuming $r_{be} \gg r_{bb}$, and noting that the zero then dominates at low frequencies, leads to the approximate relation

$$\mathrm{Re}\left[Y_{11}\right] \approx \frac{1}{r_{be}} + \omega^2 r_{bb}\left(C_{je} + C_{diff}\right)^2 \tag{4.12}$$

r_{bb} of the equivalent circuit model is adjusted to fit Y_{11} over a range of frequencies.

It remains to apportion the total collector base capacitance between C_{cbi} and C_{cbx}. In the present work, this was done by adjusting the distribution to fit Mason's unilateral gain of the model to that computed from measurements.

4.6.2 Common Emitter Devices

Single finger devices with geometry representative of each finger in the power devices were measured. Because these single finger devices have no extrinsic degeneration in the emitter lead, it is somewhat easier to isolate the intrinsic parameters. Several devices with nominal (written) emitter and collector dimensions of $1 \times 25\mu m^2$ and $2 \times 29\mu m^2$, respectively, were included on the mask. The following discussion pertains to one such device from wafer G. Small signal gains for this device, biased at $V_{CE} = 1.2$V and $I_C = 19.8$mA, are shown in figure 4.11. The value of f_{max} extrapolated at 20dB per decade from Mason's unilateral gain U is 320 GHz and the value of f_t extrapolated from H_{21} is 170 GHz. Figures 4.12 and 4.13 show the variation of f_t and f_{max} with bias. The effect of C_{cb} cancelation by injected electrons in the collector space charge region[53, 54, 52] can be seen in the former figure. Even as f_t decreases for $V_{ce} > 0.95$V, f_{max} increases significantly as V_{ce} is increased to 1.25 V. This Schottky contacted collector HBT only enters the active mode of operation when the entire collector layer is depleted.

A small signal model for this device, when biased at $I_C = 19.8$mA was extracted according to the procedure of section 4.6.1. Extrapolation of the values at 2 GHz of $\mathrm{Re}\,[Y_{21}]$ vs $1/I_C$ yields a value of 2.7Ω for r_{ex} and 30 mV for nk_BT/q. The value of $|H_{21}|$ at 1 GHz is 34 dB, giving $\beta \approx 51$, and hence $r_{be} = 77\Omega$.

Extrapolation of the transit time to infinite collector current yields a value of $\tau_f + r_{ex}(C_{cb,tot} + C_{p,be}) = 0.62$psec and $nk_BT/q \cdot (C_{cb} + C_{je} + C_{\mathrm{p,be}}) =$ 5.9psec · mA. The slope gives $(C_{cb} + C_{je} + C_{\mathrm{p,be}}) = 197$fF. Geometrical calculations give $C_{\mathrm{p,be}} \approx 10$fF, and so we have $\tau_f = 0.51$psec and $C_{\mathrm{diff}} = g_m \tau_f \approx 340fF$.

Fitting Y_{11} of the equivalent circuit model to measurements at low frequencies, and fitting S_{11} at high frequencies yields $r_{bb} = 11\Omega$. The base

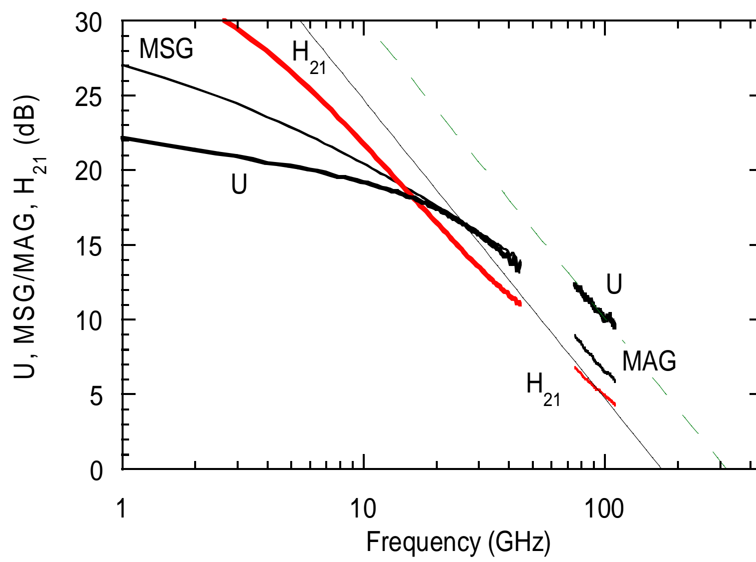


Figure 4.11: Small signal gains computed from network analyzer measurement of $1 \times 25\mu m^2$ emitter, $2 \times 29\mu m^2$ collector device.

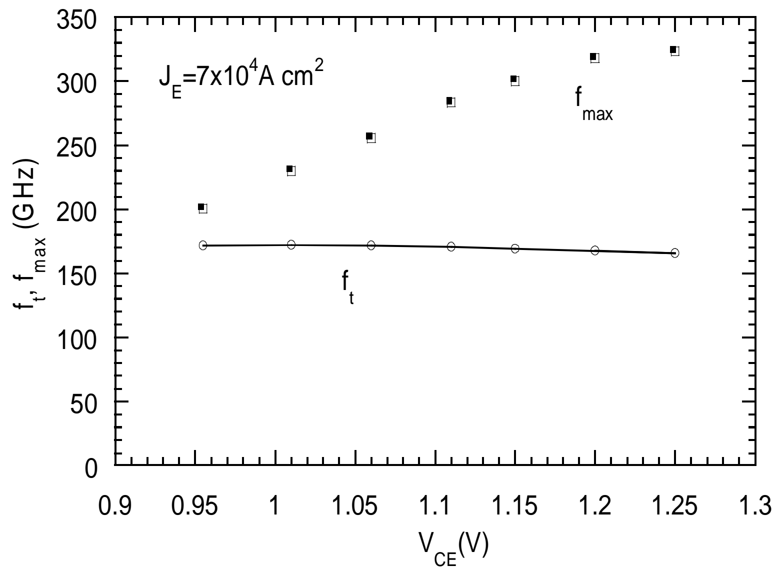


Figure 4.12: Cutoff frequencies, f_t, $f_{\max}$ as a function of Collector bias voltage V_{CE} for $1 \times 25\mu m^2$ emitter, $2 \times 29\mu m^2$ collector device.

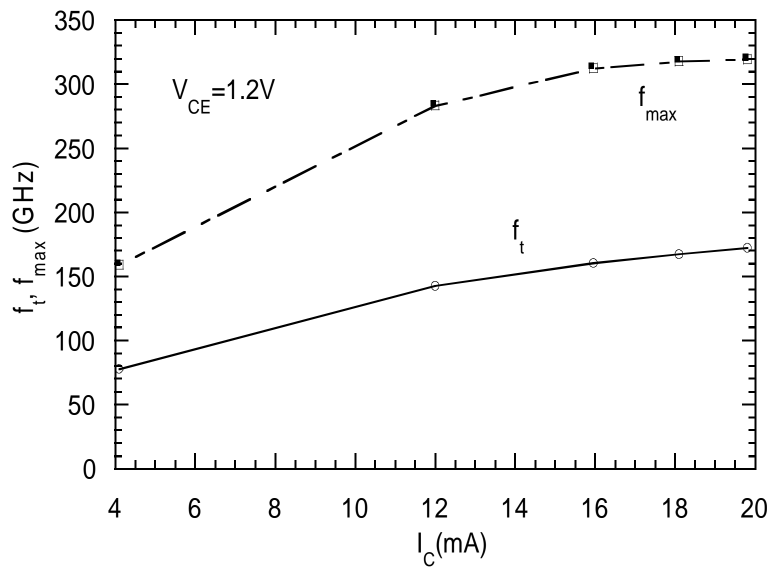


Figure 4.13: Cutoff frequencies as a function of collector current, I_C in $1 \times 25\mu m^2$ emitter, $2 \times 29\mu m^2$ collector device.

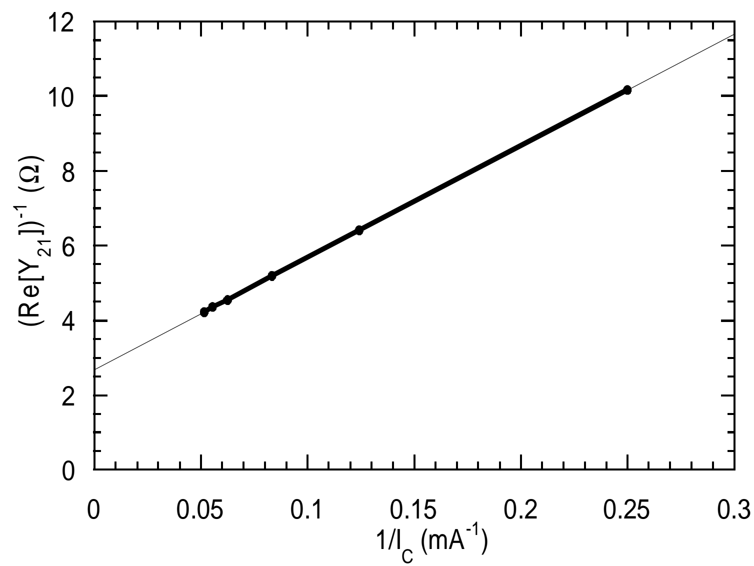


Figure 4.14: Extrinsic transconductance, from $|\mathrm{Y}_{21}|$ below f_β, vs. I_C. Extrapolating to infinite current yields a value of 2.7Ω for R_{ex}

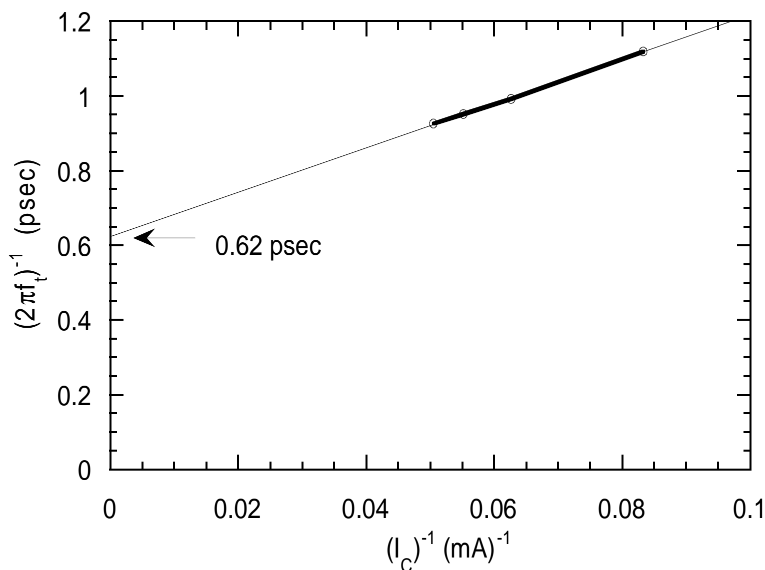


Figure 4.15: Transit time vs. inverse collector current. Extrapolation to $1/I_C = 0$ yields $\tau_f + r_{ex}(C_{cb,tot} + C_{p,be}) = 0.62$psec.

collector capacitance distribution was here picked to fit U and H_{21}.

The small signal equivalent circuit model extracted from measurements of this device is shown in figure 4.16. Note that a parasitic collector resistance r_{cx} has been added here, and other elements adjusted slightly to give a better fit to measured data. The output resistance r_{ce} is notably small for an HBT with a degenerately doped base. It is improbable that this output conductance results from the Early effect in such devices, and parasitic surface conduction is suspected. The S parameters of the equivalent circuit model are compared to measurement in figure 4.17.

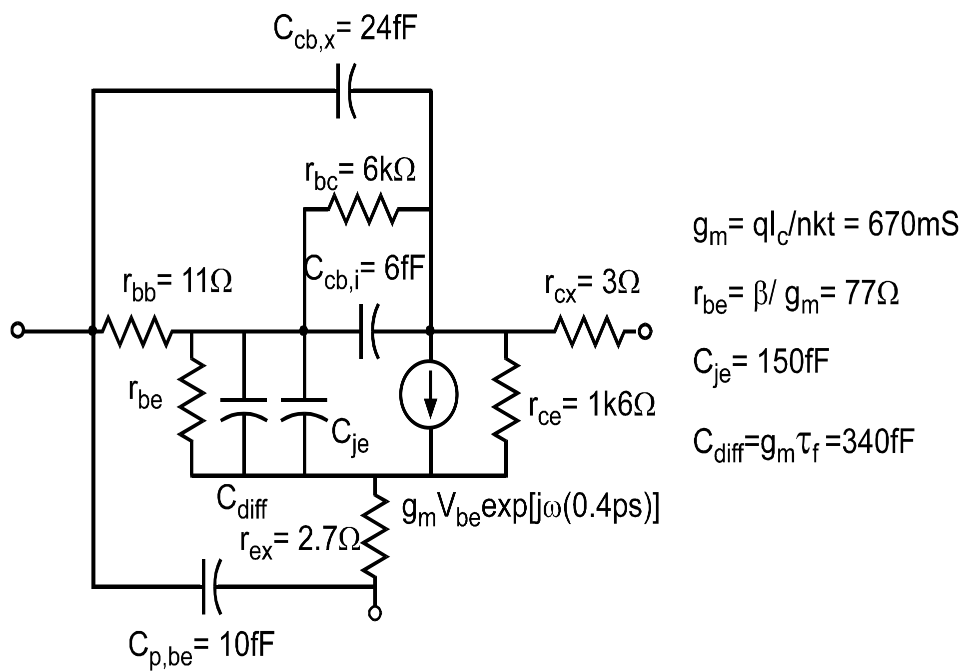


Figure 4.16: Small signal equivalent circuit extracted from measurement of "E" type transistor

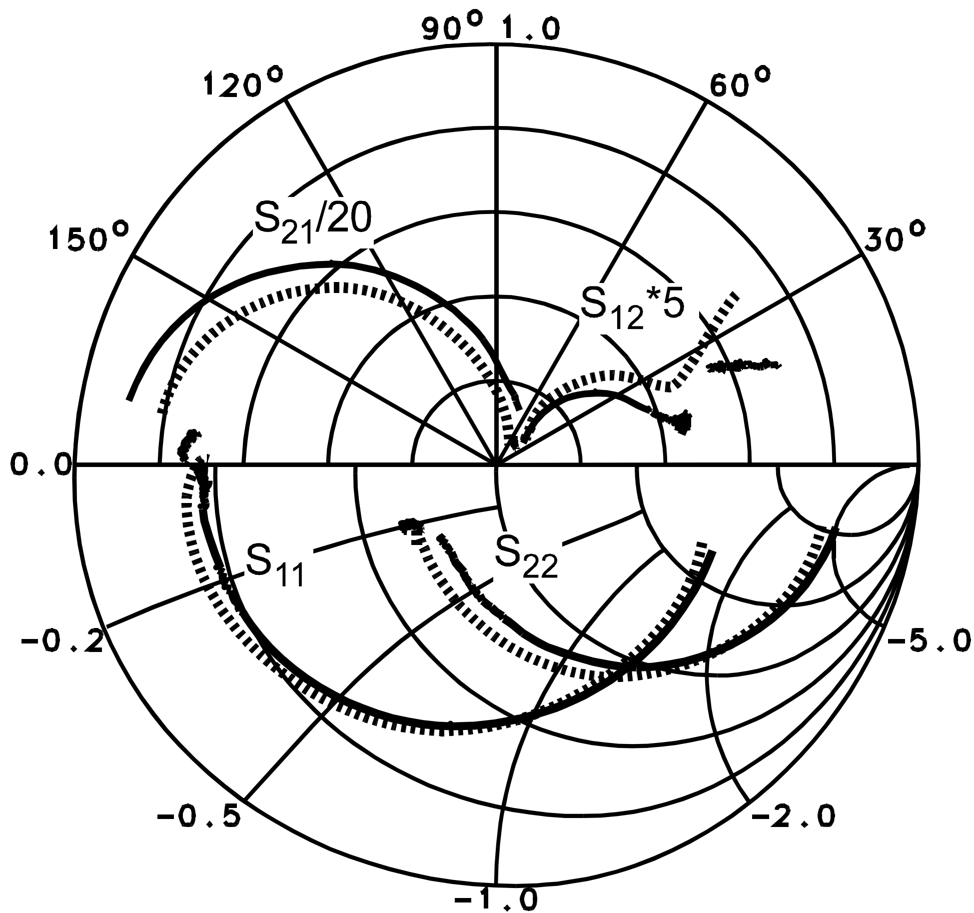


Figure 4.17: S parameters of equivalent circuit model from 0.5 to 110 GHz (heavy dotted lines) vs. measured values from 0.5 to 40 and from 75 to 110 GHz. Upper half of unit circle shows S_{21}, S_{12} with the indicated scaling. S_{11}, S_{22} are plotted in the reflection coefficient plane. The reflection coefficient contours of constant resistance and constant reactance, referred to $50\,\Omega$ i.e. the Smith chart, are shown in the bottom half of the unit circle.

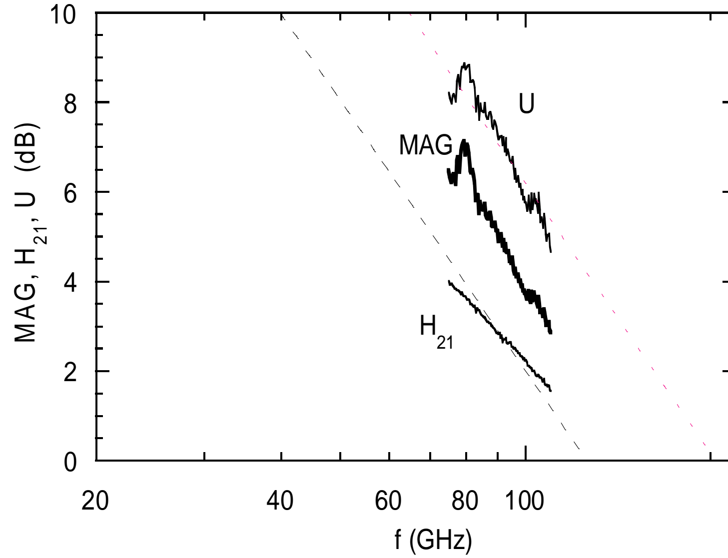


Figure 4.18: RF characteristic gains of $4 \cdot (1 \times 25\mu m^2)$ emitter area common emitter device with emitter ballasting.

4.6.3 Multi-Finger Devices

RF measurements were made of the four finger common emitter transistor described in section 4.5. The characteristic gains U, H_{21} and MAG of such a four finger device, biased at $I_C = 51$mA and $V_{CE} = 1.31$V, are shown in figure 4.18.

One of the omissions from the mask set used here was of any test structure to allow DC measurements of the ballast resistors. As noted earlier, these resistors were designed with contact separations less than the prudent design rule. Also, the ballast resistors are located in close proximity to the substantial topography of the HBT mesas which will perturb the thickness of the interconnect metal patterning photoresist. Given that a short length separation will magnify the absolute variations of the decidedly variable interconnect lithography process, the actual ballast resistance could be quite different than the designed.

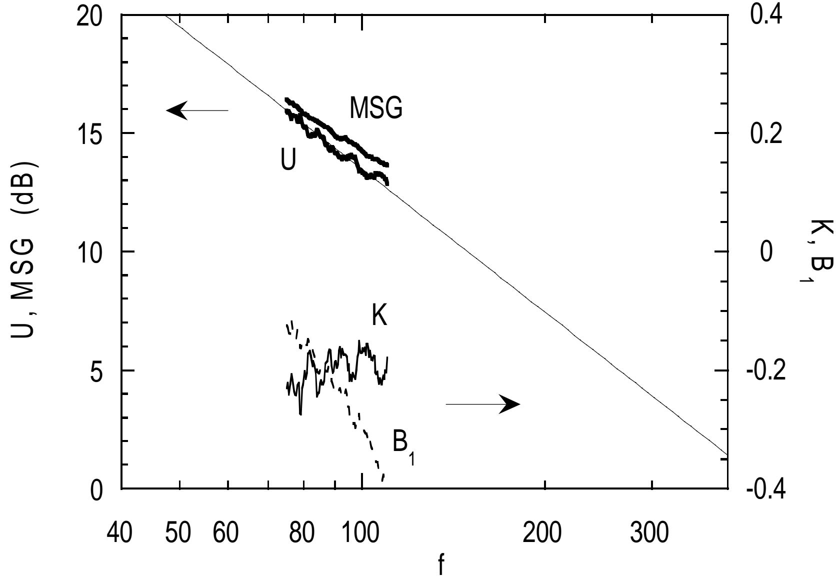


Figure 4.19: Characteristic gains MSG, U, stability factor K and stability measure B_1 of single finger common base device computed from network analyzer measurements. Extrapolating U at 20dB/decade suggest a value of 470 GHz for $f_{\max}$.

4.6.4 Common Base Devices

Common base devices with a single $1 \times 25\mu m^2$ emitter and $2 \times 29\mu m^2$ collector were measured. For many bias conditions, these devices exhibit potential instability over all of W-band. The characteristic gains of such a device, biased at $I_C = 19$ mA and $V_{CB} = 0.37$ V are shown in figure 4.19, while S_{11}, S_{22} and output stability circles at the same bias point are shown in figure 4.20. Note that, although S_{22} is outside the Smith chart over the whole band, the output stability circles indicate that device operation is stable under $50\,\Omega$ loading. The magnitude of S_{11} is less than unity for 50Ω output termination, showing that the output stability circles enclose the load impedances which would result in instability.

The characteristic gains U and MSG/MAG, of a $8 \cdot (1 \times 25\mu m^2)$ emitter

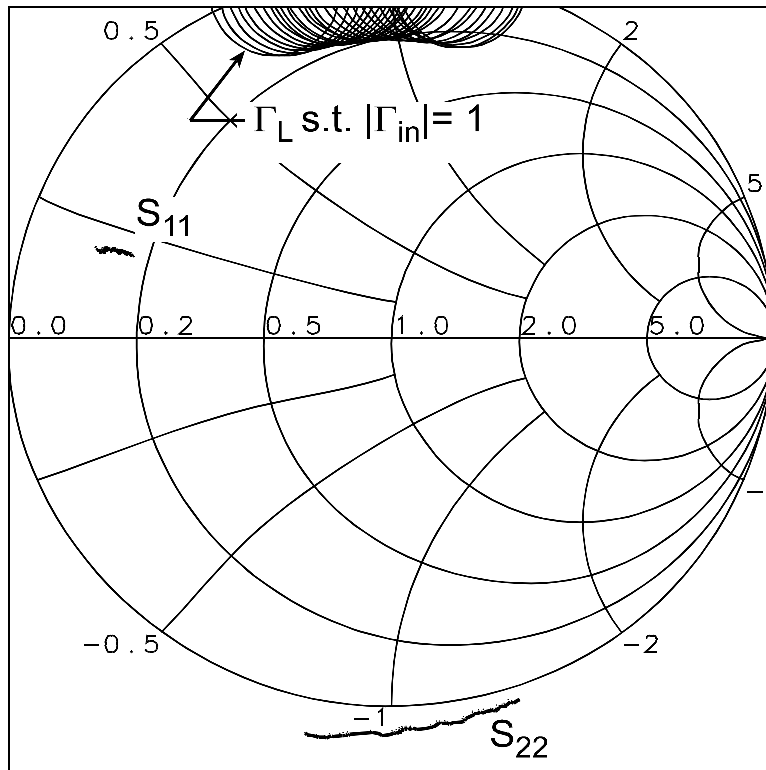


Figure 4.20: Reflection coefficients, S_{11}, S_{22} and output stability circles of common base transistor

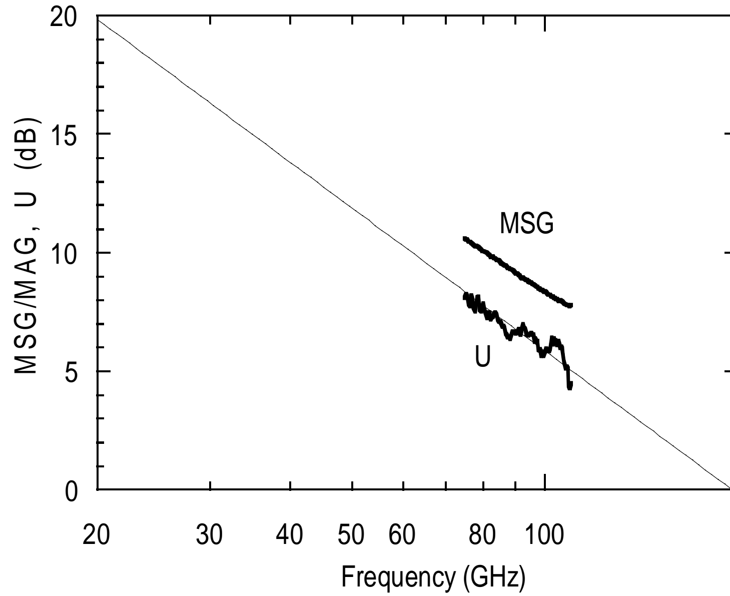


Figure 4.21: RF characteristic gains U, MSG, of $8 \cdot (1 \times 25\mu m^2)$ emitter $8 \cdot (2 \times 29\mu m^2)$ collector common base device

$8 \cdot (2 \times 29\mu m^2)$ collector common base device with emitter ballasting resistors, and biased at $I_C = 67\text{mA}$, $V_{CB} = .74\text{V}$, are shown in figure 4.21. $f_{\max}$, extrapolated at 20 dB per decade from U is 195 GHz. Rollett's stability factor K and the stability measure B_1 computed from the same measurements showed the operation of this device to be potentially unstable over the whole of W band: $K < 1$ and $B_1 < 0$. Nonetheless, the expected 10 dB per decade slope is not seen in the computed MSG. The calibrated measurement of S_{22} falls outside of the Smith chart over the whole 75–110 GHz band. Note that the maximum stable gain did not rise when the device was biased at higher collector current densities, but that U increased slightly in magnitude and significantly in noise.

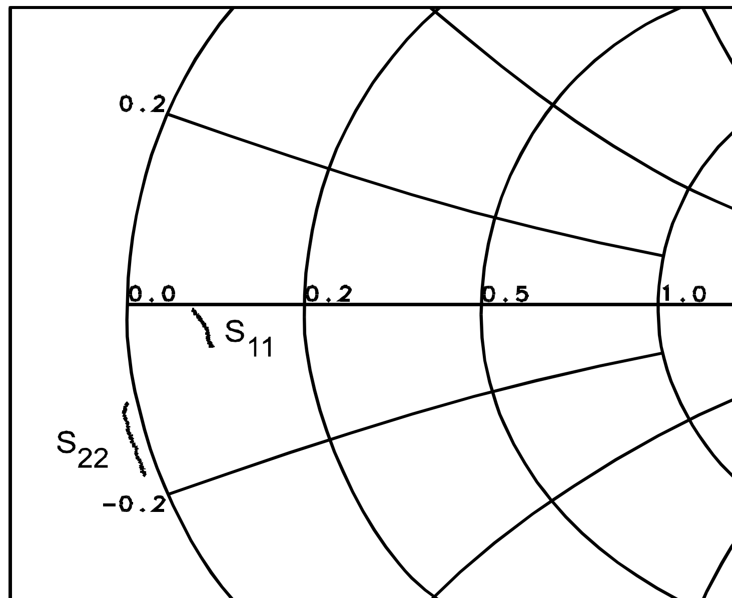


Figure 4.22: S_{11} and S_{22} of eight finger CB device with frequency swept from 75 to 110 GHz. Network analyzer data with this calibration suggest that S_{22} fell outside of Smith chart over whole band.

Chapter 5

Integrated Circuits

A number of integrated circuits were designed in the present work. The initial goal was to demonstrate the integration of a complete circuit in the metal substrate process. The first circuits so demonstrated were simple resistive feedback small signal amplifiers. Having demonstrated that integrated circuits could be built, a demonstration of the benefits of the metal substrate was desired. Power amplifiers represent relatively simple circuits which dissipate significant amounts of power, and so were chosen as a vehicle to showcase the metal substrate. As discussed in section 4.4, unresolved process problems prevented the successful fabrication of power amplifier circuits in the copper substrate process in this work. For this reason, the results of circuits fabricated on a solder bonded quarter wafer referred to herein as wafer G, are presented here.

For the purposes of computer circuit design work, the SPICE BJT model was used, with a parameter set extracted by S. Jaganathan from device measurements. The parameters of this model, with the emitter area normalized to $8\mu m^2$, are given in table 5.1.

5.1 First IC's on Cu Substrate

The first circuits fabricated successfully in the metal substrate process were Darlington resistive feedback amplifiers. Existing Darlington feedback amplifier designs[37, 55] were modified for this mask set. Small value resistors were inserted in series with the DC bias probe pads, in order to damp bias network resonances which had been observed in prior designs[55]. These

Parameter	Value	
I_s	5	pA
β_f	50	
n_f	1	
V_{Af}	8	V
I_{se}	50	pA
n_e	1.67	
I_{sc}	5	nA
n_c	1	
R_b	20	Ω
R_e	6.6	Ω
C_{je}	18	fF
τ_f	0.34	psec
C_{jc}	8.2	fF
V_{jc}	0.7	V
M_{jc}	0.33	
X_{cjc}	0.2	
T_{nom}	78	°C
E_g	1.11	eV
X_{ti}	35	

Table 5.1: SPICE BJT model parameters for a $1 \times 8\mu m^2$ emitter, $2 \times 10\mu m^2$ transferred substrate HBT.

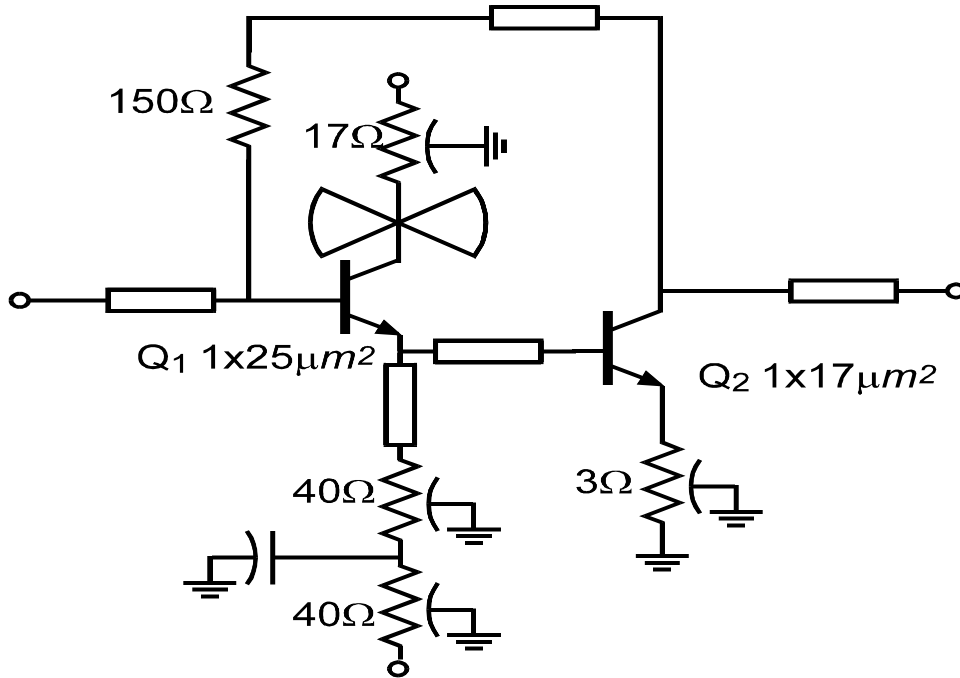


Figure 5.1: Darlington resistive feedback amplifier circuit schematic.

observed resonances occurred with a frequency spacing of some $4GHz$, implying a resonator length of $3.8\text{cm}/\sqrt{\epsilon_r}$. It is surmised that these resonances were a manifestation of reflections at the external bias tee from a low performance termination.

The feedback resistance used here is somewhat less than is indicated to achieve 50Ω input and output impedances at DC. By increasing the return losses at DC in this way return losses at frequencies above the resonance seen in S_{11} were improved. As shown in figure 5.2 the Darlington feedback amplifier showed 9 dB of insertion gain with a 3 dB bandwidth of 90 GHz in simulations.

Measured small signal characteristics of the Darlington feedback amplifier, as fabricated on wafer D are shown in figure 5.4. The amplifier exhibited insertion gain of 9.5 dB from 0 to $>$ 50 GHz, with an interpolated 3dB bandwidth of 60 GHz. The input return loss rose to -2dB at 50 GHz.

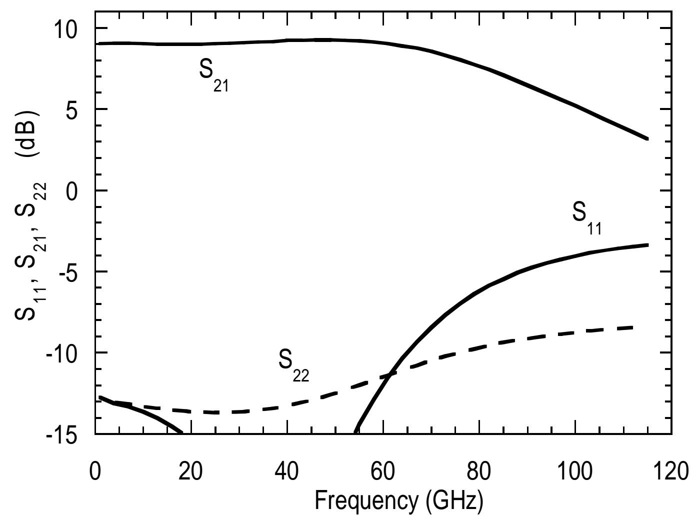


Figure 5.2: Simulated small signal performance of Darlington feedback amplifier

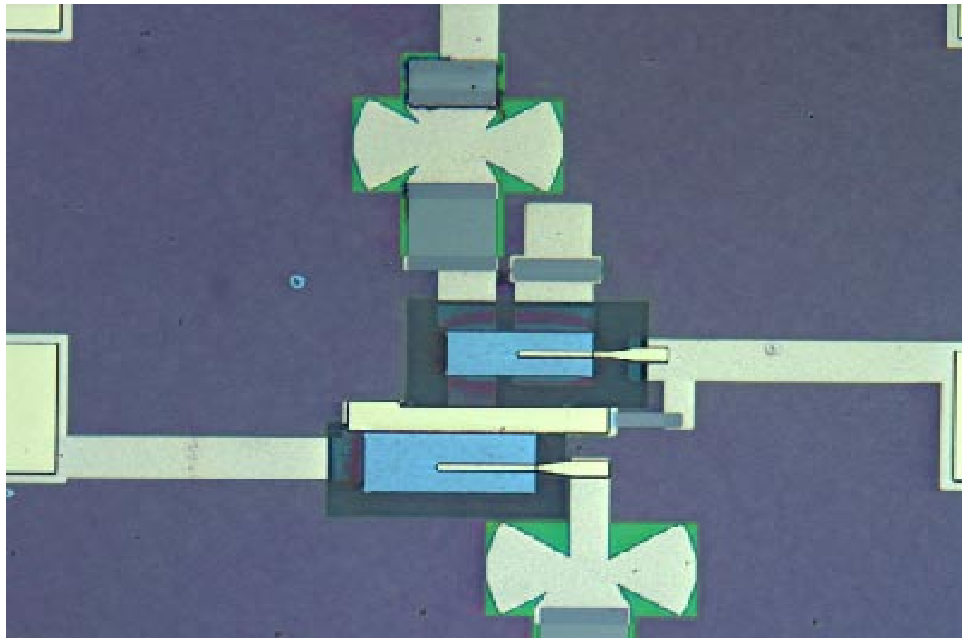


Figure 5.3: Die photo of Darlington resistive feedback amplifier on 50mm Cu wafer.

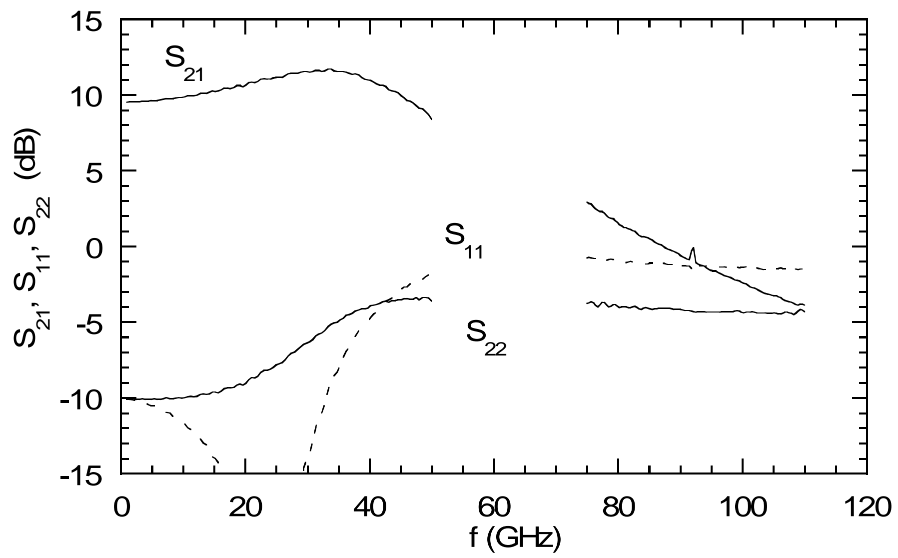


Figure 5.4: RF characteristics of Darlington feedback amplifier, measured on wafer

5.2 Power Amplifiers in Small Signal Technology

While the Cu substrate is well suited to the development of amplifier MMICs with large dissipated power densities, the present device is less so. The InGaAs collector of HBTs presently available in the transferred substrate HBT process leads to low breakdown voltages, while the InGaAs/InAlAs emitter contributes rather large thermal resistance. As shown in chapter 4 the common emitter breakdown voltage BV_{CEO} in these devices is only ≈ 2.8V, while the common base breakdown voltage BV_{CBO} is about 6V. The eventual introduction of MBE grown InP will improve the breakdown voltage by $3\times$ to $5\times$ and greatly improve device heatsinking. These improvements should come at little price in device RF performance for low bias voltages[56]. Collector transit times are however expected to be larger in an InP collector device when large collector bias voltages are applied, because scattering of electrons into the conduction band satellite valleys will increase.

Conventional schemes for monolithic integrated power combining involve substantial losses, particularly at the high frequencies where the performance of these HBTs is exceptional. It should also be reiterated that the choice of a microstrip dielectric thickness of $5\mu m$ was driven by other circuit goals for the technology, and does not necessarily represent the best tradeoff between via parasitics and transmission line skin loss for reactively matched amplifiers.

Within the constraints of the present technology, a number of reactively matched large signal amplifiers were designed, in part to showcase the metal substrate technology, in part to investigate the large signal behaviour of the TS-HBT. To maximize the permissible voltage swing, common base output stages were used. Amplifiers were here designed for loading corresponding to 2 V peak-to-peak voltage swing and current density swing of 10^5 A cm^{-2} referred to the masked emitter dimension. The design and results of a common base, a cascode, and a balanced power amplifier are presented in sections 5.3, 5.4 and 5.5.

5.2.1 Phased Array Project

In order to demonstrate greater output powers, and the heatsinking advantages of the copper substrate, a less typical approach to power combining was pursued. At mm-wave frequencies where the devices performance is exceptional, monolithically integrated antennas begin to become feasible. With integrated antennas radiating in a phased array, the output power of numerous low output impedance amplifiers could be combined in free space. A design project was embarked upon to build such an array operating at 94GHz, a frequency of technological relevance because of a dip in atmospheric absorption.

In order to reduce the array pitch to a reasonable value, broadband antenna designs could not be considered. Instead, narrow band dipole antennas were designed by our collaborators at Caltech. Complementary signals are needed to drive dipole radiators. Two approaches to developing the complementary power outputs were pursued. One consists of a differential power amplifier, while the other approach consists of generating balanced signals with a small signal active balun, and amplifying each phase of the signal with a single-ended power amplifier. The latter architecture is illustrated schematically in figure 5.5. The use of single-ended power amplifiers simplifies testing of high risk building block circuits. A differential power amplifier design is presented in section 5.8, while the active balun design is presented in section 5.7. The cascode power amplifier designed for use with active baluns in the array is presented in section 5.4

5.2.2 On the Design of Reactively Matched MMICs

Epitaxially grown III-V wafers constitute an exceedingly expensive substrate for microwave circuits. Even so, integrating very large areas of transmission line matching networks on the same IC with a few high performance transistors is sometimes the best way to achieve performance goals. Clearly the cost of a MMIC amplifier is tied to the area of the entire die as opposed to the much smaller area consumed by active devices.

To maximize the chances of yielding working amplifiers in the presence of significant process variability, it is advisable to avoid very narrow band reactive matched designs. In the present process, the specific capacitance of the SiN_x MIM capacitors is quite variable, and some variability is also seen in the thickness of the BCB transmission line dielectric. Some care in pro-

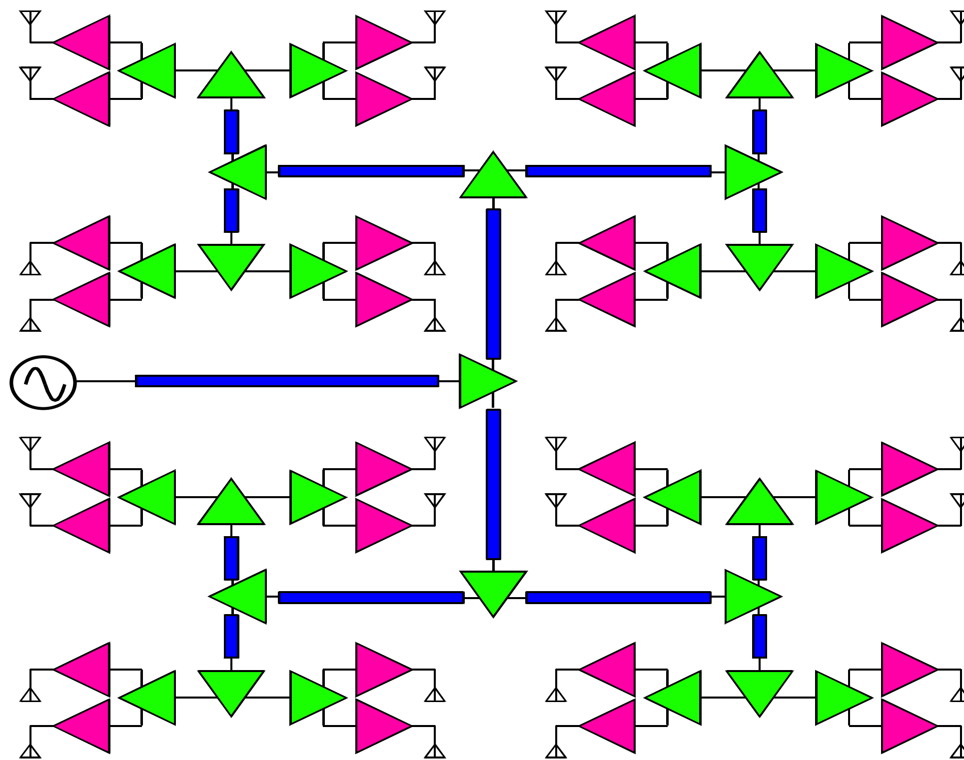


Figure 5.5: Schematic diagram of proposed 94 GHz phased array. The input signal is distributed by a transmission line H tree with gain provided by active baluns at each branching. Single ended power amplifiers drive integrated monopole radiators.

cessing is required to achieve reproducible emitter etch undercut and hence A_E related parasitics. The collector feedback capacitance C_{cbi} is highly bias dependant, while R_{bb} and $C_{cb,x}$ vary from run to run. Given that the transistor parasitics are quite variable, it is not sufficient to design narrow band input and output matching networks that track one another with variations in the passive elements: variations in the transistor parasitics will cause the resonant frequencies of any such networks to diverge.

The fundamental limitations on the gain and bandwidth achievable by reactive matching networks were derived by Fano[50, 43]. No lossless matching network can achieve a broadband match exceeding

$$\int_0^\infty \ln\left|\frac{1}{\Gamma}\right| d\omega = \pi \cdot \frac{\omega_o}{Q_1} \tag{5.1}$$

for shunt RC and series RL circuits, where $Q_1 = R/X_c, X_L/R$ respectively, or

$$\int_0^\infty \omega^{-2} \ln\left|\frac{1}{\Gamma}\right| d\omega = \pi \cdot (\omega_o Q_1)^{-1} \tag{5.2}$$

for series RC and shunt RL circuits where $Q_1 = X_c/R, R/X_L$ respectively.

For a power amplifier design in a highly variable process, we would like to achieve an acceptable input reflection coefficient over as wide a bandwidth as possible. Ideally, a constant magnitude of reflection coefficient $|\Gamma|$ can be achieved within a band from ω_a to ω_b such that

$$|\Gamma| = \exp\left[-\pi \frac{Q_2}{Q_1}\right] \tag{5.3}$$

where

$$Q_2 = \frac{\omega_o}{\omega_b - \omega_a} \tag{5.4}$$

Practically, equation 5.3 only serves as a guideline for evaluating actual matching networks.

The design constraint on the output matching network of a power amplifier is perhaps less obvious, in so far as this network is designed to achieve a specific $\Gamma_L = \Gamma_{L,Pmax}$ as opposed to a small magnitude of Γ_L at the design frequency.

Matching networks in power amplifier MMICs are generally designed using microstrip elements to implement all the reactive elements. In the interest of yield, it is often preferable to synthesize the matching networks

from transmission line stubs: the delay of a microstrip line segment is relatively insensitive to variations in line width and dielectric (wafer) thickness. Furthermore, by relying only on microstrip elements to implement the key components of the matching network, process tolerances on MIM dielectrics can remain relaxed. Against these advantages, microstrip matching networks tend to consume large areas of the die. The expense in area of microstrip matching networks is actually exacerbated by the use in this work of very low permittivity microstrip dielectric; fractional wavelength structures are $\sqrt{\epsilon_{\mathrm{InP}}/\epsilon_{\mathrm{BCB}}} \approx 2.2$ times longer.

In the present work, the objective was to demonstrate the achievable performance, as opposed to yielding large numbers of acceptable IC's. In this context, the design strategy taken was to compromise reproducibility in favor of compact die size and to include versions of the basic circuit with intentional detunings to allow for some process variation. Here, MIM capacitors were used in many reactive matching networks. Where $\lambda/4$ line segments were used, they were meandered tightly, taking advantage of the reduced line pitch allowed by very thin microstrip. Although quarter wave structures can be constructed from lumped element synthetic transmission lines, this strategy is rarely employed in MMIC designs at V band and above and was avoided here. It was decided that the benefit in reduced die size would not justify the cost of greatly increased variability in tuning.

5.2.3 Special Passive Elements

In the present work, transistors with relaxed lithographic dimensions were used. In the power amplifier designs, each finger had nominal emitter and collector dimensions of $1 \times 25 \mu\mathrm{m}^2$ and $2 \times 29 \mu\mathrm{m}^2$, respectively. The common emitter and common base devices in the single-ended cascode each consisted of four such fingers.

In designing the cascode amplifier, a larger base bypass capacitor was found necessary than could be modeled with EESOF's built in radial stub model. For this reason, the characteristics of MIM capacitors with planar dimensions in excess of the range of validity of EESOF's model was calculated numerically using the HP Momentum method of moments field solver. Roughly 0.5 pF could be obtained from an MIM radial stub capacitor with a self-resonance frequency of approximately 250 GHz. For the purposes of circuit simulation, the lumped element equivalent circuit show in figure 5.6,

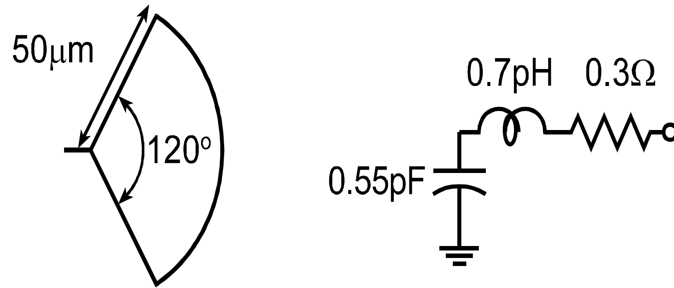


Figure 5.6: Diagram and equivalent circuit of large MIM radial stub capacitor.

with self resonance and Q fitted to the numerical calculations, was used. This same large capacitor design was reused as a bypass capacitor to provide an AC ground termination of shunted inductive line segments.

As noted in section 2.6.1, the transmission lines in this process are only approximately of microstrip geometry. Particularly for high impedance lines, the additional capacitance due to the embedding of the line in dielectric was anticipated to reduce the characteristic impedance achieved. Measurements of a test structure, calibrated with on wafer LRL standards, are shown in figure 5.8.

5.2.4 Large Signal Measurements

In order to measure W-band power amplifiers, a high power signal source was required. Here, active frequency multipliers were used to generate drive signals at six times the frequency of a microwave synthesized source. This signal source and a W-band waveguide power sensor were coupled to the IC's under test with waveguide coupled wafer probes and a 60 cm length of WR-10 waveguide. Waveguide and probe losses were extracted by measuring signal throughput first without wafer probes and then with 50Ω on-wafer through lines (whose insertion loss was known from network analyzer measurements).

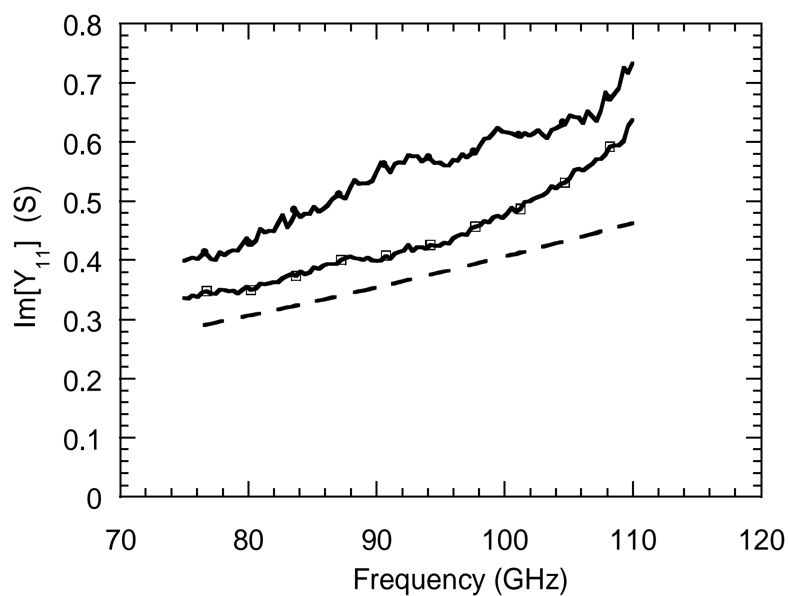


Figure 5.7: Susceptance of large radial stub MIM capacitor. Calculated susceptance of equivalent circuit shown in dashed curve at bottom. Measured susceptance from wafer F (open squares) and wafer G (filled circles) shown for comparison.

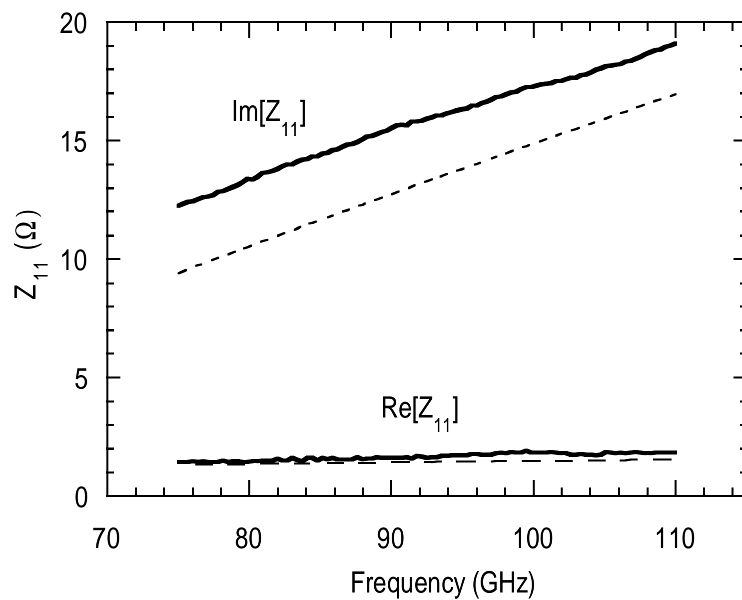


Figure 5.8: Reactance of a high impedance transmission line shunted to large bypass capacitor. Measured (solid lines) values are compared to calculated (dashed lines).

5.3 Common Base Amplifiers

Common base power amplifiers were designed with a four $1 \times 25\mu m^2$ finger device. Very low inductance ground connections to the common base device could be made by landing multiple ground vias between the emitter mesas. Given that the emitter pitch was already constrained by the need for ballasting resistors, these multiple vias did not further increase the pitch. A schematic diagram of this common base amplifier design is shown in figure 5.9. Thermal stability was improved by degenerating each emitter finger with a 5Ω ballast resistor. The input matching network consists of a two section LC low-pass prototype. The capacitors are implemented as MIM radial stubs, which saves die area but ties the tuning to the SiN as well as the BCB film thickness. The output matching network was designed to transform from a 50Ω interface impedance to a 20Ω large signal load line for the device. The output capacitance of the transistor resonates with an inductive line section, shunted to AC ground by a .5pF MIM radial stub capacitor, and a quarter wave $Z_o = 33\Omega$ line transforms the resulting impedance. Broad band stability is attained through a quarter wave line shunted to a parallel RC network on the input.

The input matching network was designed to provide a fairly broad band match to the transistor by maintaining small circuit node Q's, Q_n where[43, p125].

$$Q_n = \frac{|X|}{R} = \frac{|B|}{G} \tag{5.5}$$

Referring to figure 5.10 where transmission line elements have been replaced by single pi-section equivalent networks, we can easily calculate nodal Q's. The nominal model of the four finger transistor with emitter ballasting (and output tuning network) presents an input impedance of $(3.5 + j1.4)\Omega$ and hence $Q_{in} = 0.4$ at 94 GHz. This is transformed to $Z = (3.5 + j6.8)\Omega$, $Q_1 = 1.9$ by the first series inductor, $Y = (60 - j68)$mS , $Q = 1.1$ by the first shunt capacitor and $Z = (7.3 + j13.6)\Omega$ by the second series inductor. The final shunt capacitor transforms to $Y = (31 + j9.3)$mS, and we see that the highest nodal Q in the network is only 1.9. This input tuning network can also be viewed as a length of synthetic transmission line. Examining S_{11} of the complete amplifier on the Smith chart (see figure 5.11), we see that a higher impedance synthetic transmission line, by encircling the center of the chart would have yielded a somewhat better input match over most of

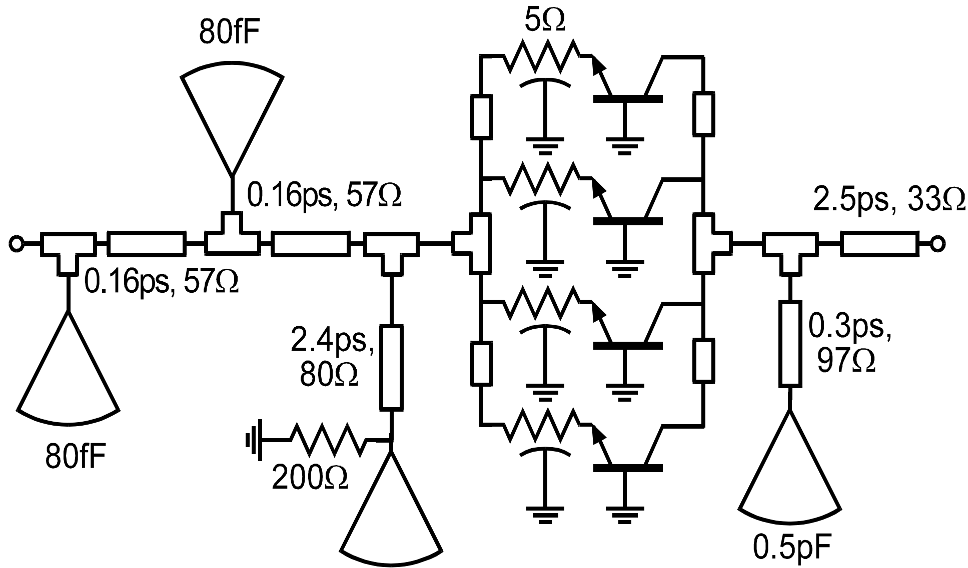


Figure 5.9: Schematic diagram of common base power amplifier design.

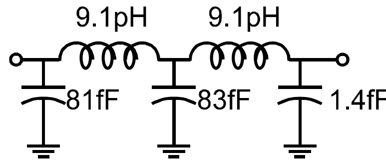


Figure 5.10: Lumped element circuit equivalent to microstrip input matching network of the common base amplifier.

the band.

While either a shunt or series inductor could be used to resonate with the capacitive output admittance of the transistor, the former was chosen to give a broadband small signal gain peak. A shunt inductor with $B_{L,p} \approx -B_{C,o}$ transforms the output admittance $Y = (2.2+j68)$mS of the transistor directly to a point much more central on the Smith chart than does a series inductor with $X_{L,s} = -X_{C,o}$.

Small signal measurements of the fabricated common base amplifiers revealed large discrepancies between the designed and actual performance. Most obvious is that the measured gain peak was at or somewhat below 75GHz as opposed to the design value of 94GHz. Under class A bias condi-

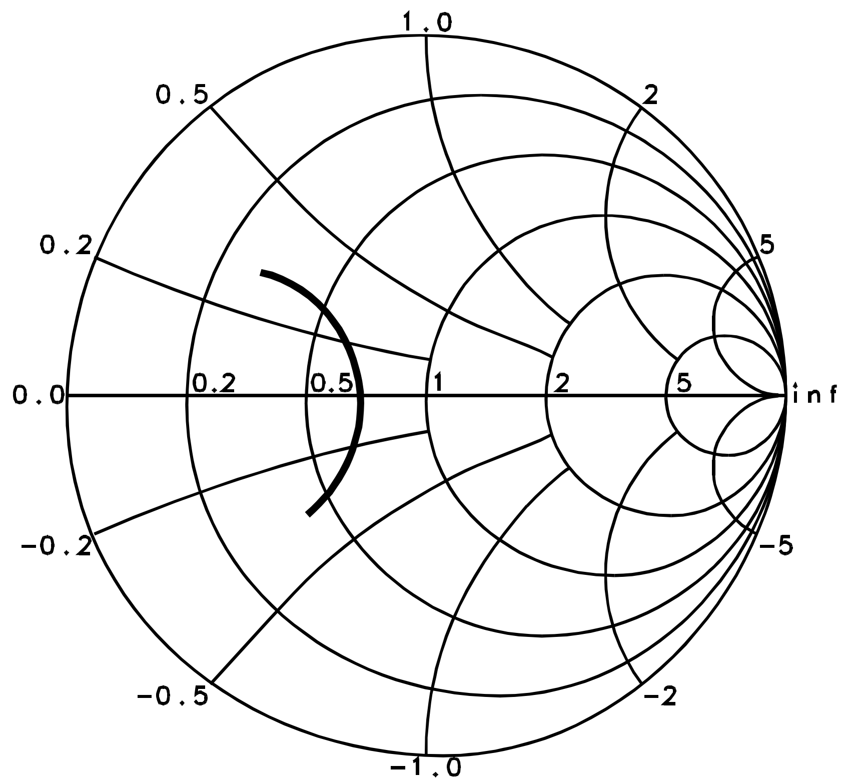


Figure 5.11: Input return loss, S_{11}, of common base amplifier simulated from 75 to 110 GHz.

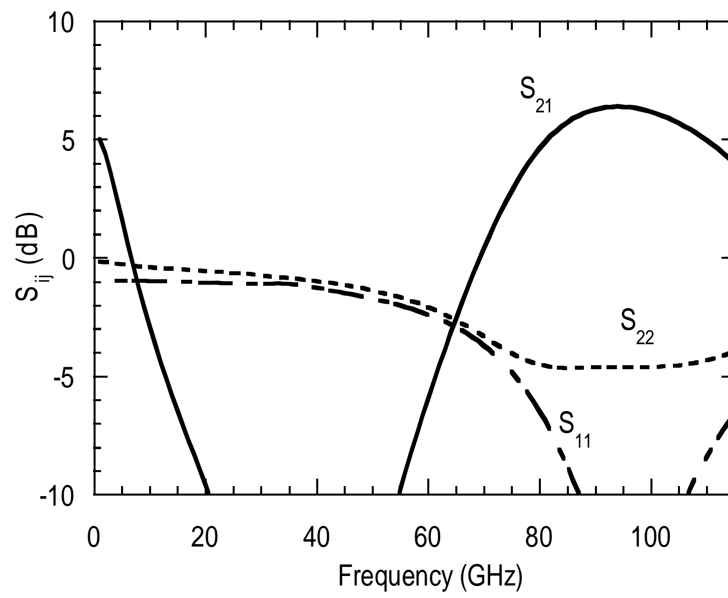


Figure 5.12: Simulated linear characteristics of the common base power amplifier.

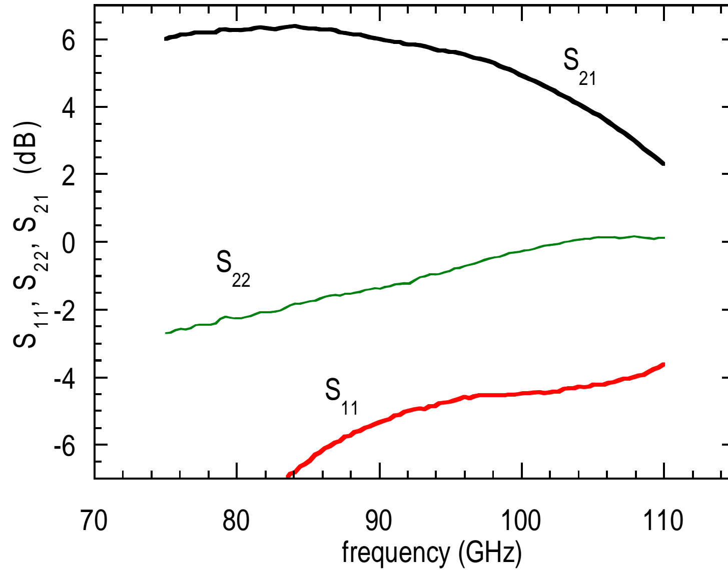


Figure 5.13: Small signal characteristics of common base power amplifier.

tions, the output return loss magnitude was negative for frequencies above 100 GHz. Computation of Rollett's stability factor K and the stability measure B_1 from the measured S parameter data confirmed that the amplifiers were potentially unstable for frequencies greater than 81 GHz.

When biased for maximum power output, the common base amplifier showed 5.3 dB of gain small signal, and 9.7 dBm output power at 82.5 GHz under 0.8 dB of gain compression. It was not possible to saturate the common base amplifiers' output power with the available W band source.

Measurements of MIM test structures on wafer G which revealed that the specific capacitance of the SiN_x was some 40% higher than anticipated. Informed by this data, the common base amplifier was re-simulated. Increasing the SiN_x specific capacitance lowered the resonance in S_{11} down to some 85 GHz, but did not reproduce the very poor output return loss, nor the instability seen in measurements. While increasing the value of C_{cbx} by some 10 fF per collector finger in simulation better reproduced the

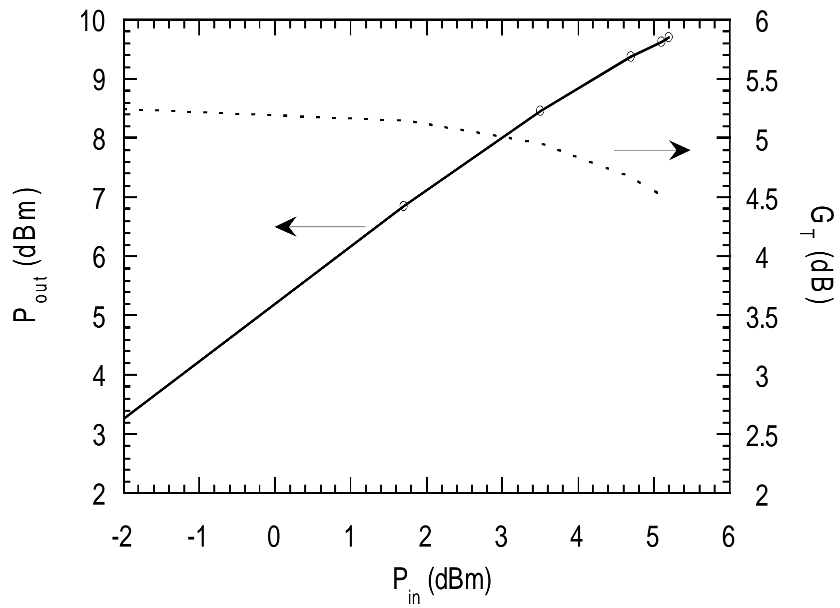


Figure 5.14: Output power saturation characteristic of the common base power amplifier at 82.5 GHz.

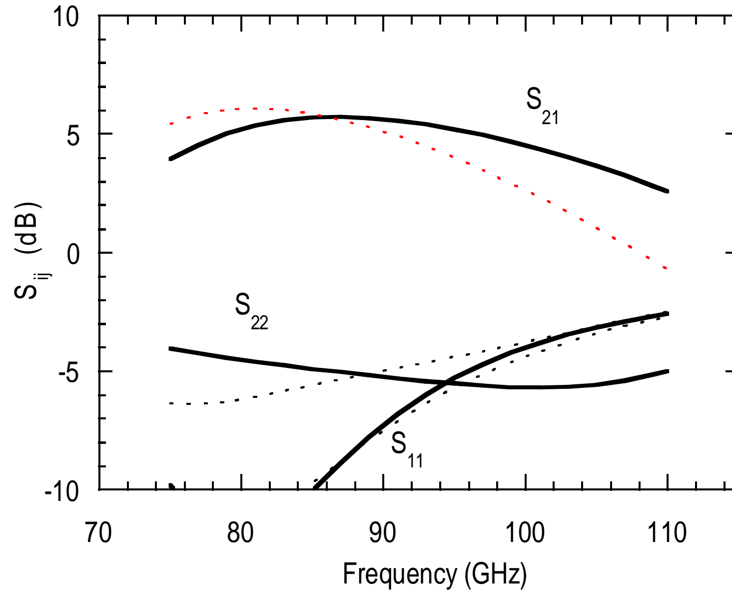


Figure 5.15: Small signal characteristics of common base power amplifier re-simulated with increased SiN_x specific capacitance. Solid lines: nominal device model; dashed lines excess C_{cbx}.

measured S_{22}, it did not result in potential instabilility. It is surmised that ground via parasitic inductance was significant in the actual amplifiers.

5.4 Cascode Power Amplifiers

Cascode power amplifiers were designed for 94 GHz operation. The cascode topology offers significantly higher gain than single transistors, and when configured correctly allows for improved thermal stability. On the other hand, cascode amplifiers in a low breakdown device technology suffer from significantly reduced power added efficiency as compared to single transistor cells. A schematic diagram of the cascode power amplifier is shown in figure 5.16. The thermally stable configuration of the multi-finger cascode [57, 58] was used to assure thermally stable operation: each emitter finger

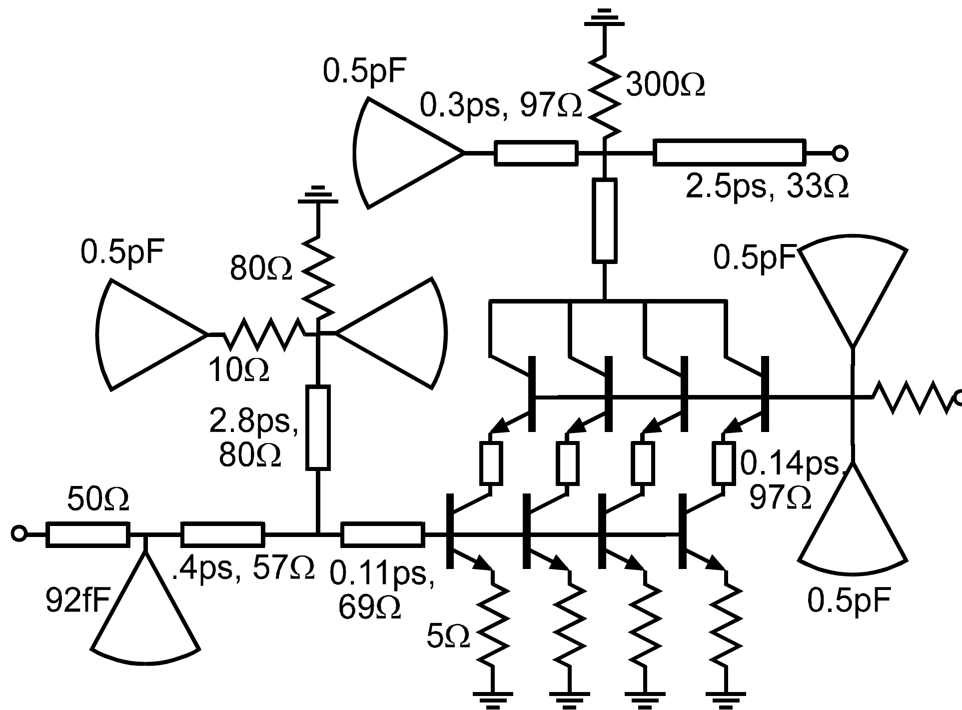


Figure 5.16: Cascode power amplifier circuit schematic. N.B. that radial stub capacitors are designed for implementation as MIM structures.

of the common base device separately to one collector finger of the common emitter device. In this way a fixed, common, value of V_{be} is not presented to the different emitter fingers of the common base device, which may be different temperatures in normal operation.

Large signal output matching to 50Ω was accomplished with a shunt inductor to a large MIM radial stub, along with a quarter wave transformer. While the simulated S_{22} of the amplifier is unusually low for a power amplifier (see figure 5.18), the output match is actually detuned from the small signal simultaneous complex conjugate match condition. Figure 5.19 shows that the reflection coefficient presented by the output matching network to the common base transistor is well outside the 3 dB penalty operating gain circle for the underlying cascoded transistors.

The input matching network consisted of an MIM radial stub capacitor and a section of high impedance line. Broadband stability was assured by

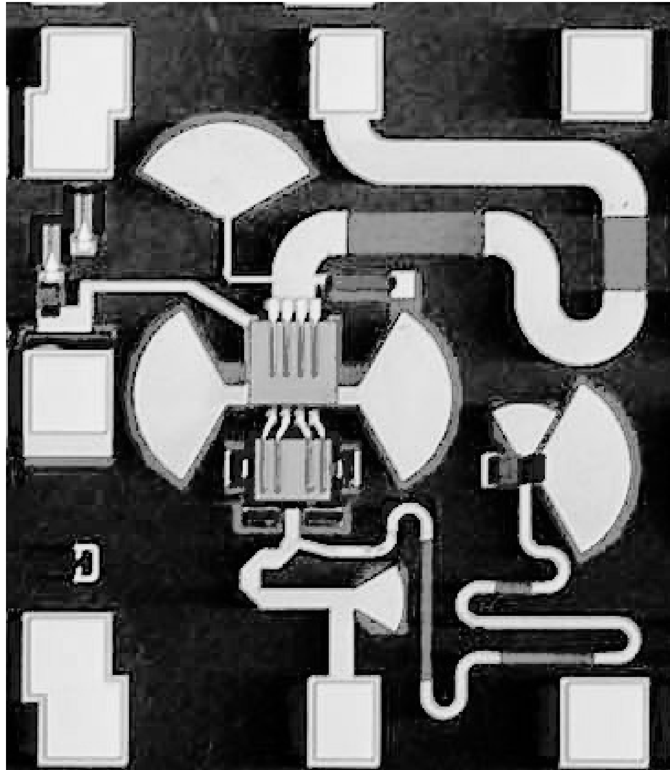


Figure 5.17: Cascode power amplifier die photo.

means of a quarter wave shunt stub terminated in an RC bypass network on the input and a resistor shunting the collector to ground on the output. The input stub bypass terminating network consisted of two MIM radial stubs in parallel with a resistor to ground. The smaller of the two radial stub capacitors was connected directly to the quarter wave line, while the larger was connected in series with a resistor of nominally 5Ω to reduce the Q of the low frequency L-C resonator formed by the inductive line and large capacitor.While the large radial stub was necessary to provide adequate shunt susceptance at lower frequencies, this series resistor was found necessary to suppress the low frequency LC resonance. Transmission lines in the input, output, and quarter wave stub networks were meandered tightly, taking advantage of the very thin microstrip substrate. The total die area is $0.42 \times 0.36\mathrm{mm}^2$.

The amplifiers were tested on wafer with waveguide coupled microcoax

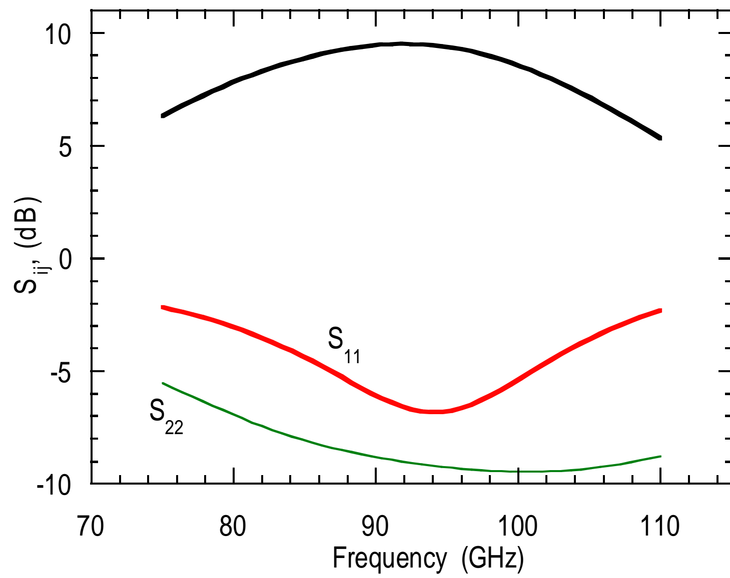


Figure 5.18: Simulated small signal performance of 94GHz cascode power amplifier design.

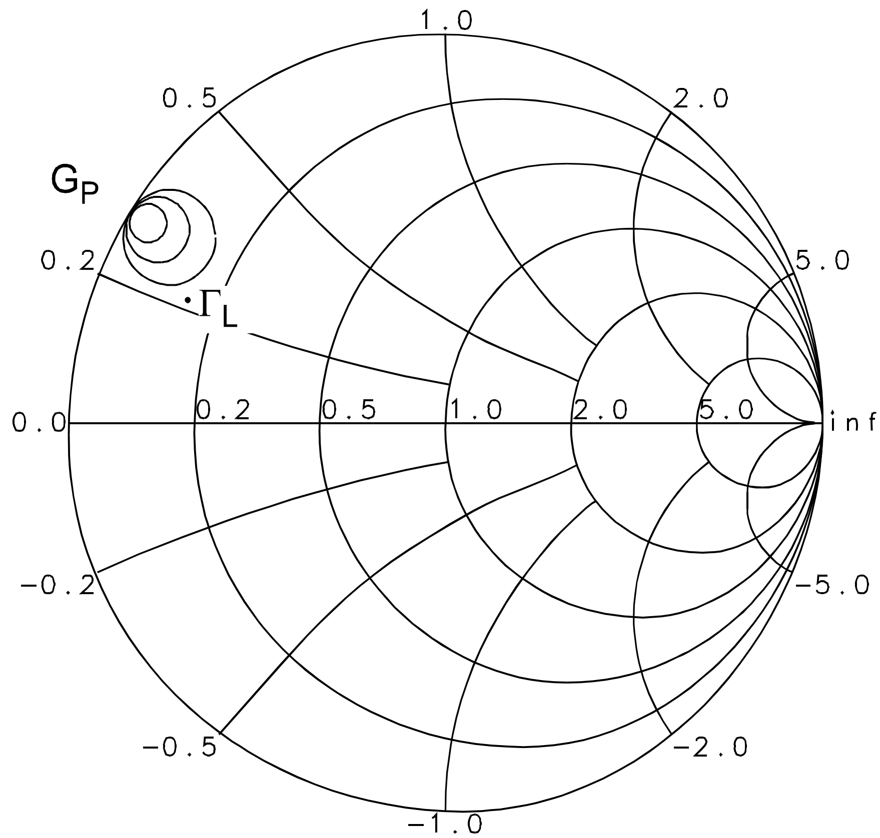


Figure 5.19: Simulated matching conditions at 94 GHz. Operating gain circles at 1,2, and 3 dB penalty from simultaneous complex conjugate match condition for cascoded transistors, and reflection coefficient looking into output matching network of amplifier.

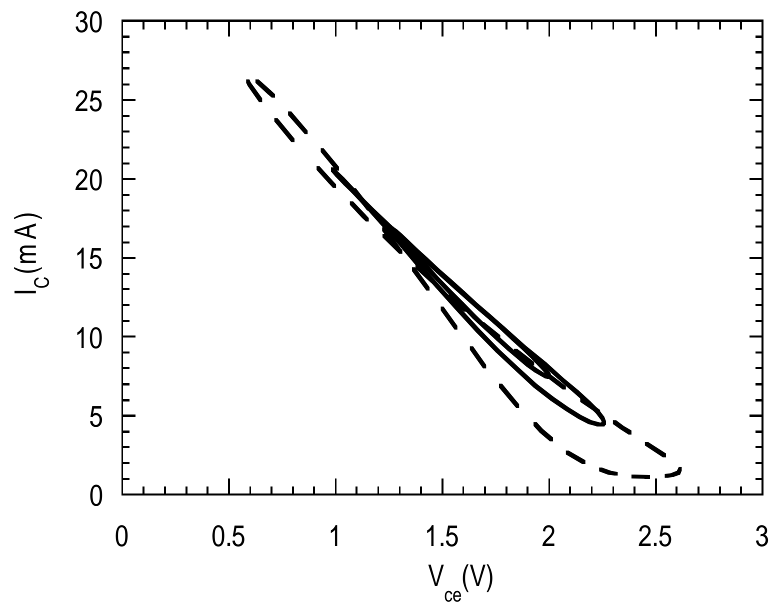


Figure 5.20: Dynamic load lines of one finger of common base "intrinsic" device for 94 GHz cascode power amplifier design driven with input powers of -5, 0 and +5 dBm.

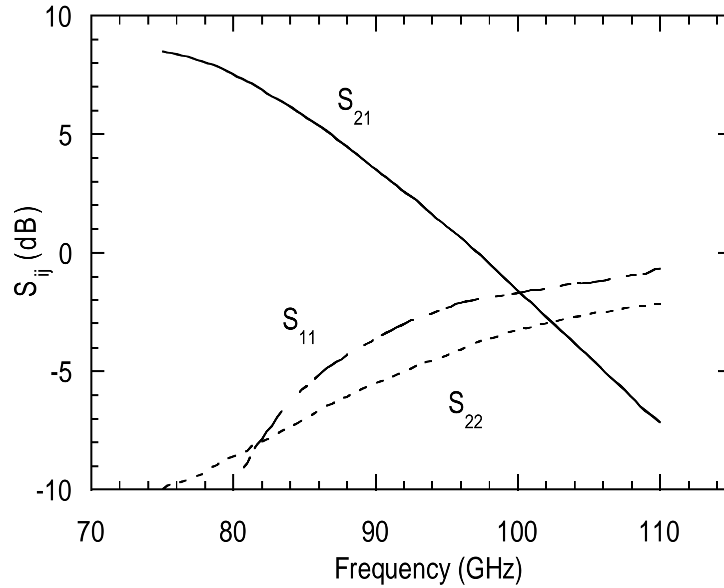


Figure 5.21: Measured cascode power amplifier small signal characteristics.

wafer probes. Small signal measurements were made on an HP 8510 network analyzer, calibrated with a commercial LRM substrate. It is worth noting that the cascodes showed significant bias sensitivity of I_C to V_{cc}: i.e. worse output conductance than a common base device. This is taken to be indicative of thermal coupling between the common base and the common emitter devices.

The cascode amplifier exhibited 8.5 dB of insertion gain at 75GHz, with input and output return losses of greater than 10 dB at that frequency, when biased for peak gain. When biased for peak output power, the amplifier exhibited 7.5 dB of insertion gain and 1dB of gain compression at 9.4 dBm output power. The maximum output power attained, 10dBm, was limited by the available signal source and not by saturation of the amplifier, which could only be driven to 1.7 dB of gain compression.

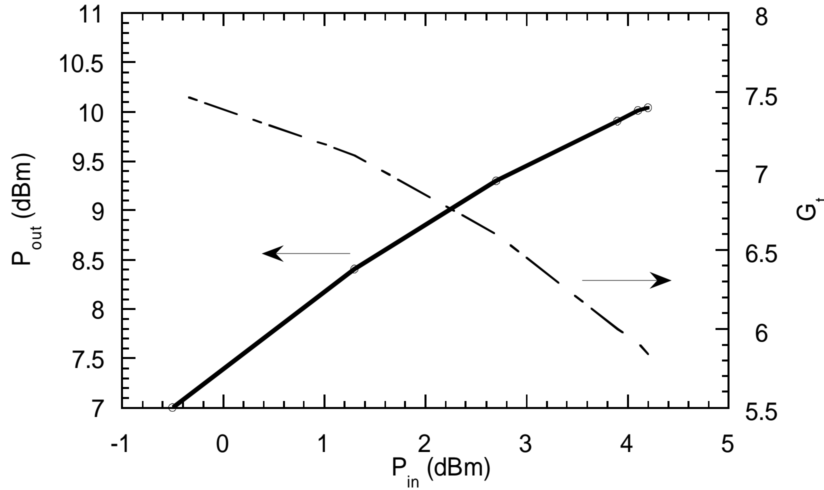


Figure 5.22: Measured power output and gain saturation characteristic of cascode power amplifier at 75GHz.

5.5 Wilkinson Balanced Amplifier

A composite power amplifier consisting of a balanced pair of the above cascode amplifiers was designed. Whereas common practice in the design of MMIC balanced amplifiers is to use Lange couplers to implement the indicated 90° hybrid networks[50], the present design makes use of Wilkinson dividers and quarter wave delay lines. The thin deposited microstrip dielectric of the present technology is by design ill-suited to the construction of edge coupled structures such as the Lange coupler. While 90° hybrid structures as compact as Lange couplers could be produced in process through the use of overlapping floating line coupling structures[14, p. 262], this possibility was not pursued here. The Wilkinson divider network was designed to match the 50Ω source impedance to the inputs of the two, 50Ω, amplifiers. The impedance of lines in the Wilkinson combiner on the other hand was chosen to effect the impedance transformation from the 50Ω external loading to the desired large signal load-line of the power amplifiers. Accordingly the quarter wave delay line in the output is a low impedance line. A schematic diagram of the balanced power amplifier design is shown

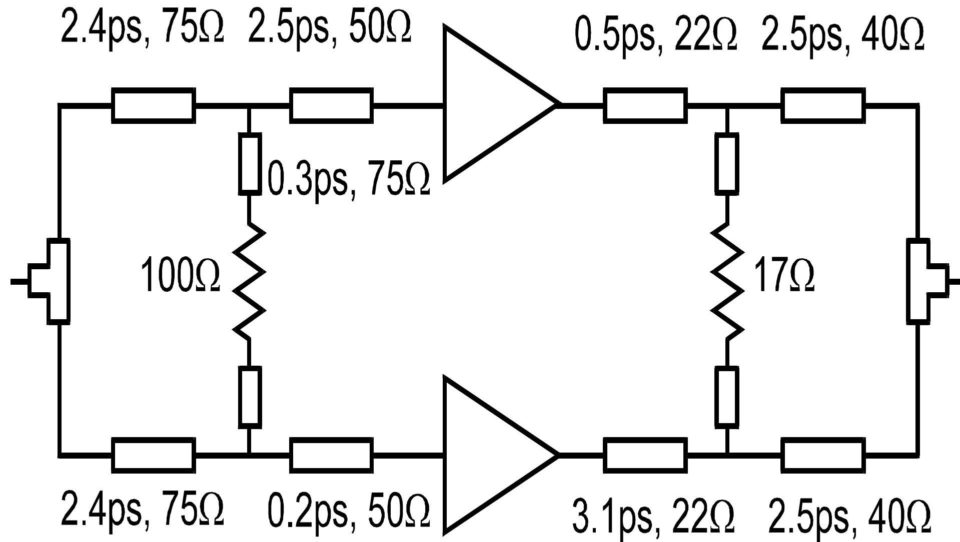


Figure 5.23: Schematic of balanced amplifier design with Wilkinson divider and combiner, along with quarter wave delay lines.

in figure 5.23.

Measured small signal characteristics of the balanced power amplifier are shown in figure 5.25. Both S_{11} and S_{22} show minima below -15 dB centered at approximately 98 GHz, demonstrating that the passive elements of the balanced topology are effective at the design frequency. The transducer gain of the balanced amplifier is however, rolling off from 75 GHz, as did that of the individual cascode amplifiers. The Wilkinson balanced amplifier exhibited 7.9 dB of gain at 78 GHz under small signal drive, and delivered 10.7 dBm output power under 1 dB of compression at the same frequency.

5.6 45GHz Cascode Power Amplifier

The low breakdown voltages of the available devices lead to power performance which is less competitive at lower frequencies. However, there were a variety of reasons to design some power amplifier circuits at lower frequencies. The source power available below 50 GHz was significantly higher than that at W-band, and so the output power of amplifiers of similar device area could be saturated.

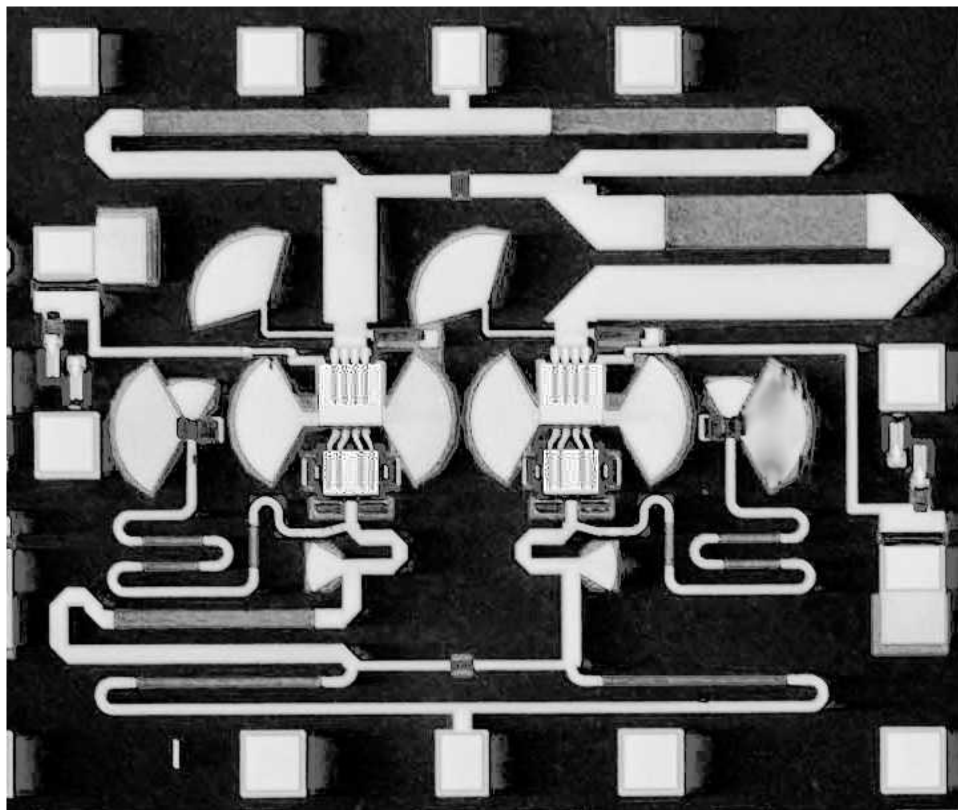


Figure 5.24: Die Photo of Wilkinson balanced cascode power amplifiers.

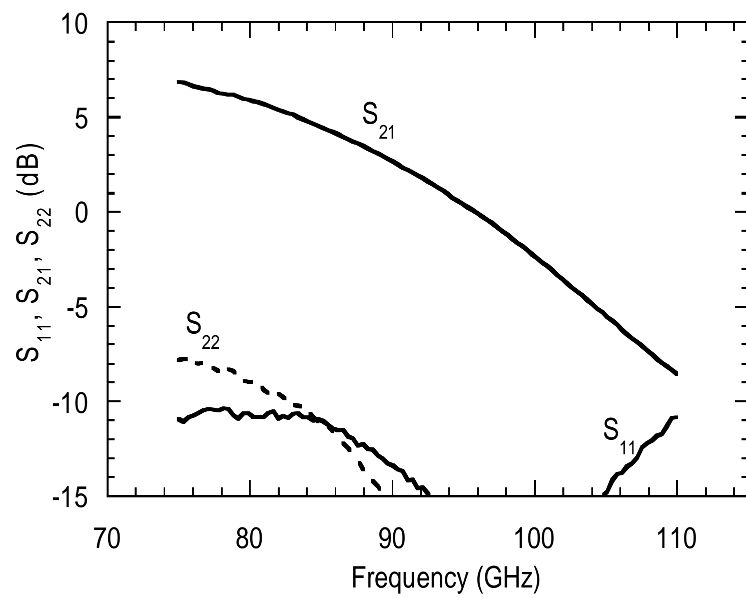


Figure 5.25: Small signal characteristics of the Wilkinson balanced power amplifier.

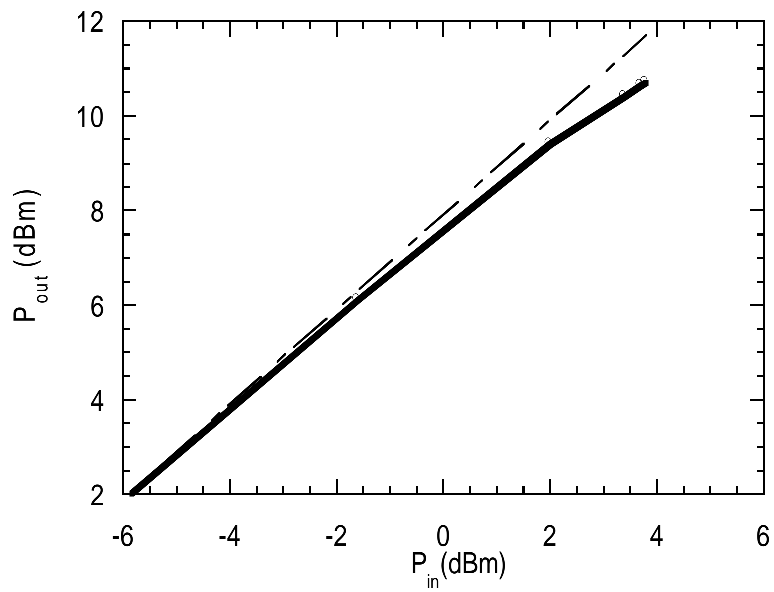


Figure 5.26: Output power saturation characteristic at 78GHz of the Wilkinson balanced power amplifier.

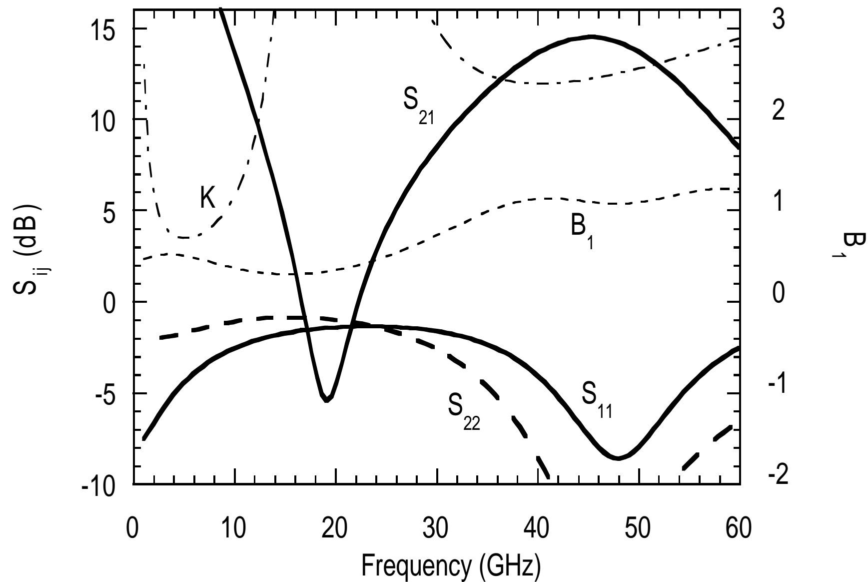


Figure 5.27: Simulated small signal characteristics of the 45GHz power amplifier. Rollett's stability factor, K and the stability factor B_1 demonstrate broad-band stability of the design.

The basic cascode power amplifier designed for 94GHz operation was retuned for a large signal match at 45GHz. At this frequency, a shunt inductive network on the output yielded the desired load impedance, and reasonable freedom from looping in the dynamic load line. In order to maintain a compact die size, broadband unconditional stability was sacrificed. While Rollett's stability factor, K for the amplifier drops slightly below unity in magnitude between 2 and 9 GHz, the incursion of the output stability circles into the Smith chart is quite small.

Small signal measurements of the amplifier MMIC, with no de-embedding of signal pad parasitic, are shown in figure5.29 An active frequency doubler module provided ample power to saturate the fabricated amplifiers from 28 to 40 GHz. The saturated output power peaked at +15.1 dBm at 40 GHz with an associated gain of 6.1 dB. While significant modification

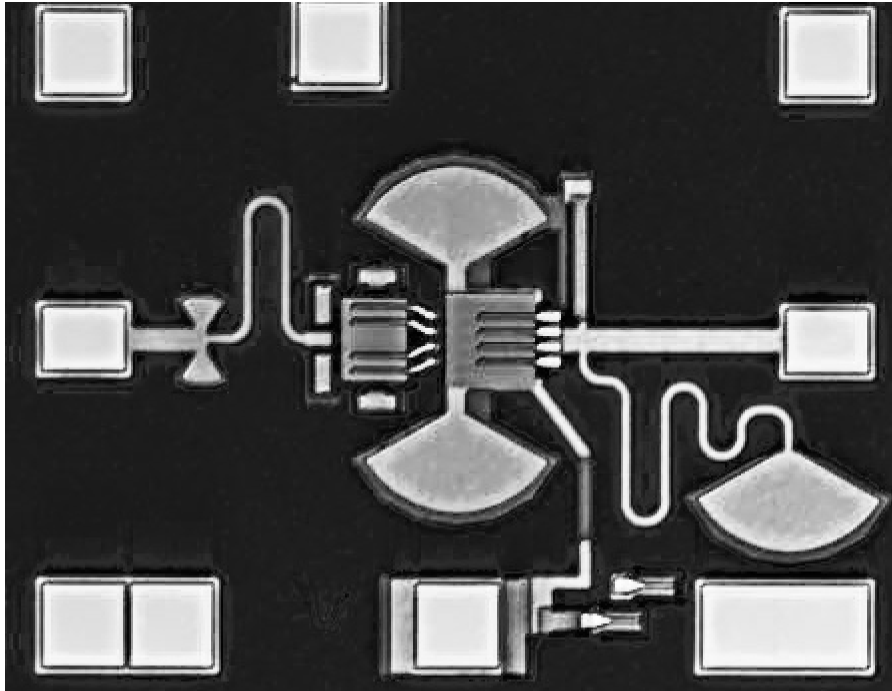


Figure 5.28: Die photo of 45 GHz cascode power amplifier.

of the bias point by self bias effects was observed at the higher drive levels, bias measurements were not recorded, and so no calculation of power added efficiency can be made. It should be noted that input drive levels above +13 dBm resulted in degradation of the amplifiers.

5.7 Active Balun

Active baluns can provide broader bandwidth and smaller die size than passive structures. Adequate common mode rejection ratio is difficult to achieve with differential pairs at high frequency. An active balun configuration which is well known in microwave design is the common-source/common-gate pair. The inverting and the non-inverting device share a common input node in this topology, and so many of the parasitics are common to both signal paths. It is fairly straightforward to achieve adequate magnitude and phase balance between the complementary outputs over a narrow

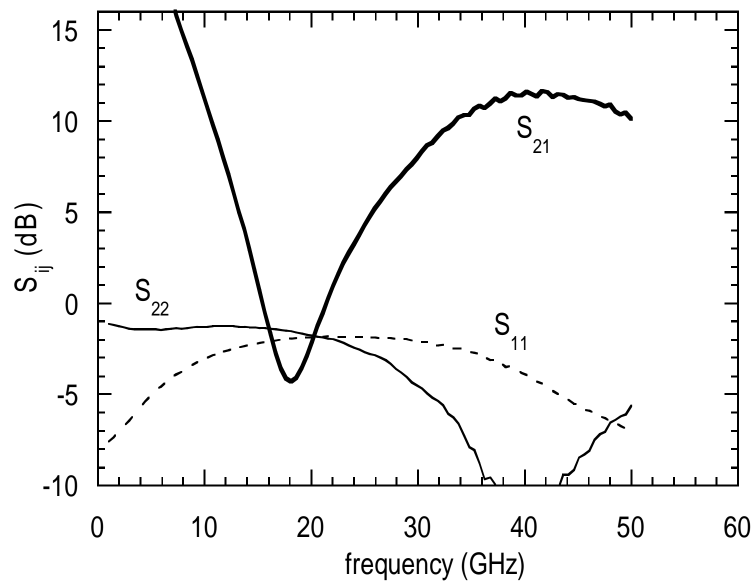


Figure 5.29: Measured S-parameters of the fabricated 45GHz power amplifier. $V_{cc} = 3.x$V, $I_c = 6x$ mA.

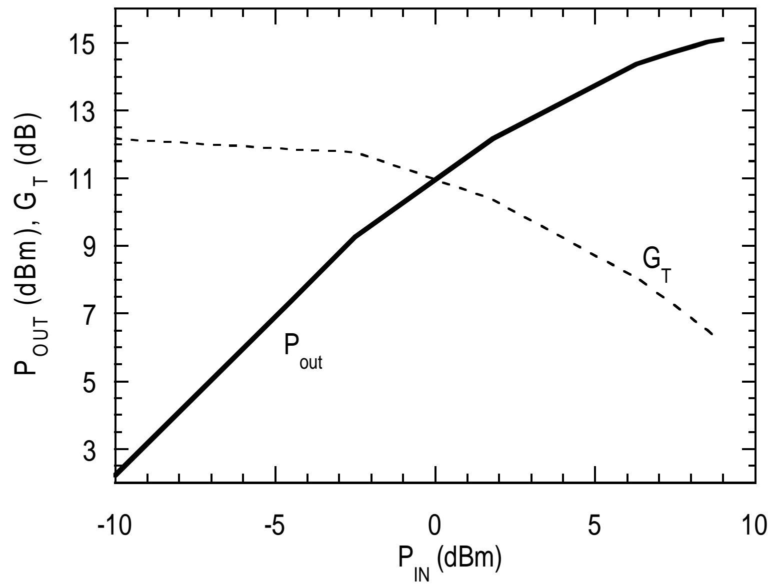


Figure 5.30: Measured power output characteristic at 40 GHz. $V_{cc} = 2.65V$, $I_c = 62$ mA $P_{1dB} = +\,7.4$ dBm, $P_{sat} = +15.1$ dBm.

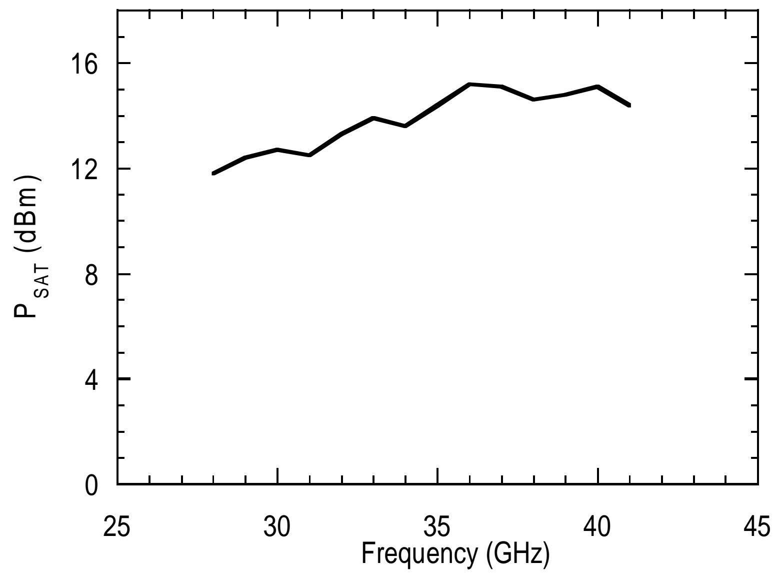


Figure 5.31: Measured frequency dependence of saturated output power.

bandwidth with this topology.

In the present design, current mirrors are used to bias the two devices at the same current, while AC coupling is used to achieve a common output DC bias. Simulated small signal performance of the balun is shown in figure 5.33. While the amplitude balance is better than 1 dB between 40 and 120GHz, the phase error with respect to 180° ranges from 25° to −7° over the same frequency range.

The active baluns were layed out in several different configurations. To facilitate testing with the probe configuration of the W-band network analyzer balun dies in several configurations were designed. Thus, two dies with complementary outputs available were designed: one with the inverting, one the non-inverting output signal pad in line with the input pad. Also, these two layouts were repeated with that output port not in line with the input resistively terminated on wafer. A die photo of one such balun with the non-inverting output terminated on-wafer is shown in figure 5.34. A layout error in the extra mask level defining the resistor protecting dielectric prevented biasing of the fabricated baluns.

5.8 Differential f_t Doubler Cascode Power Amplifiers

While differential pairs do not provide very good common mode rejection at high frequencies, differential operation does allow some flexibility in the design of reactive tuning networks. In particular, advantage can be taken of the virtual ground between the outputs when designing a reactive matching network.

A modified differential cascode topology sometimes used in high frequency power amplifiers is the Tektronix deflection coil driver circuit, which implements the differential pair of common emitter devices as a differential f_t doubler.[59] A version of this topology is shown in figure 5.35, where each common base transistor has been divided in two, and each separate emitter finger connected to the collector of one device of the differential f_t doubler. This is simply an extension of the thermally stable cascode topology[57, 58] to the case of the Tektronix differential cascode. Note that finite values of base bias resistor reduce the common mode rejection ratio attainable from this circuit, even given ideal current sources biasing each differential pair.

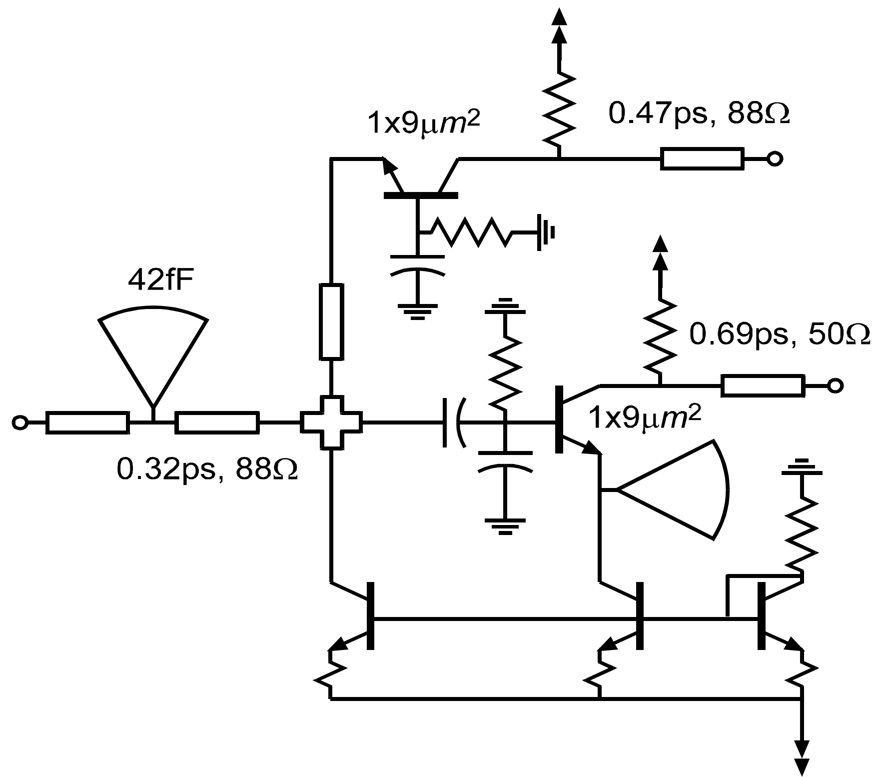


Figure 5.32: Schematic diagram of active balun IC.

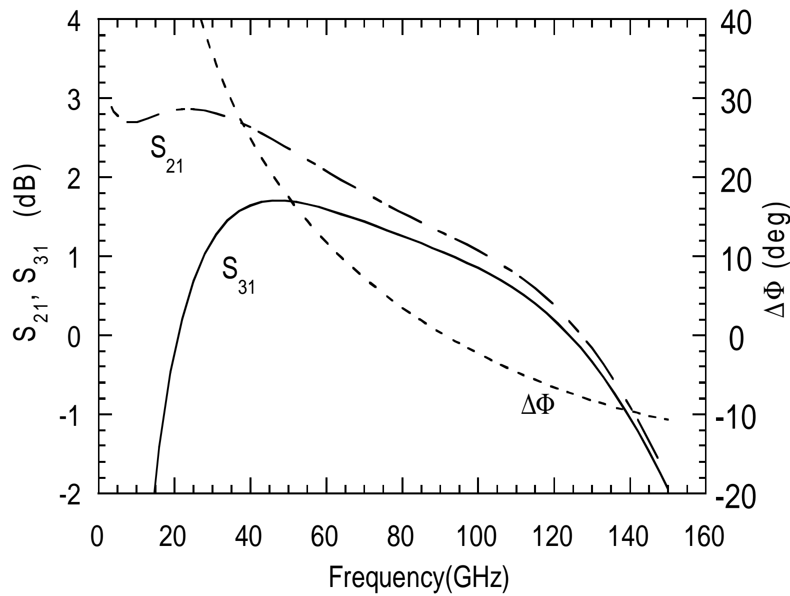


Figure 5.33: Simulated small signal performance of the active balun. Port two here is the non-inverting output, while port three is the inverting output. S_{i1} here refers to the insertion gain of the balun with respect to directly connecting port i to the signal source. The phase balance measure $\Delta\Phi$ is the discrepancy from the desired 180° relationship.

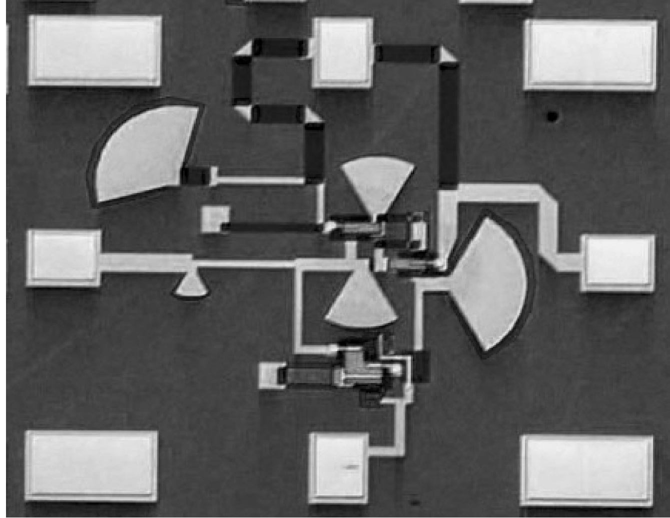


Figure 5.34: Die photo of active balun in fabrication.

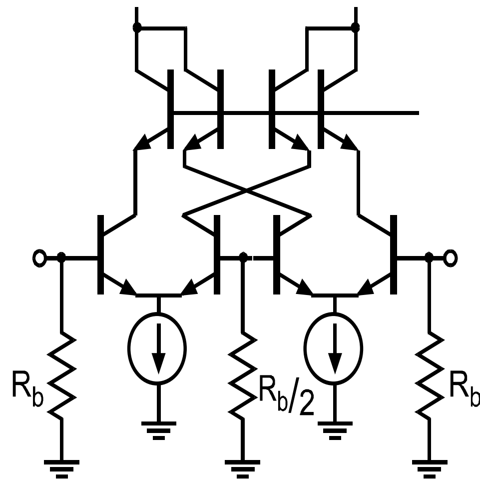


Figure 5.35: Schematic diagram of Tektronix differential cascode deflection amp topology with segmented common base transistors.

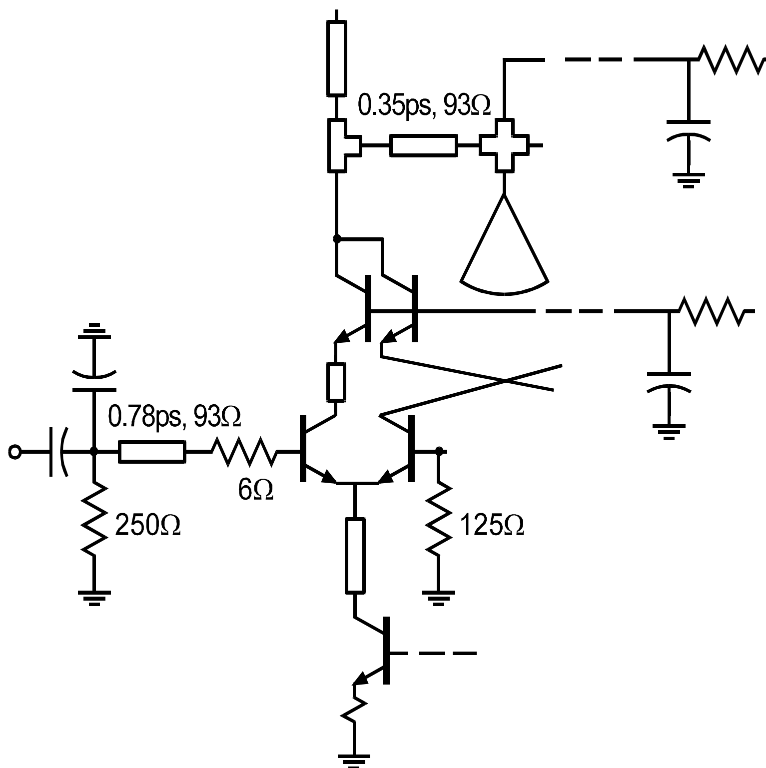


Figure 5.36: Detailed schematic of half-circuit of reactively matched differential cascode f_t doubler power amplifier.

A reactively matched power amplifier for the 94 GHz phased array project was designed around this differential cascode f_t doubler (DCFD) topology. The output device consists of two $1 \times 25\mu m^2$ emitter, $2 \times 29\mu m^2$ collector fingers in each half circuit. The output reactive match consists of inductive line segments shunted to a virtual ground point. Given that the common mode rejection ratio of the DCFD is inherently rather poor, the virtual ground point is capacitively bypassed to ground with an MIM radial stub.

Measured small signal characteristics of a DCFD amplifier from wafer G are shown in figure 5.38. Several departures of the realized circuit elements from design values on this wafer were noted above. The fabricated DCFD amplifiers were further compromised by a layout error in the termination network for the unused output; the resistor terminating the unused output

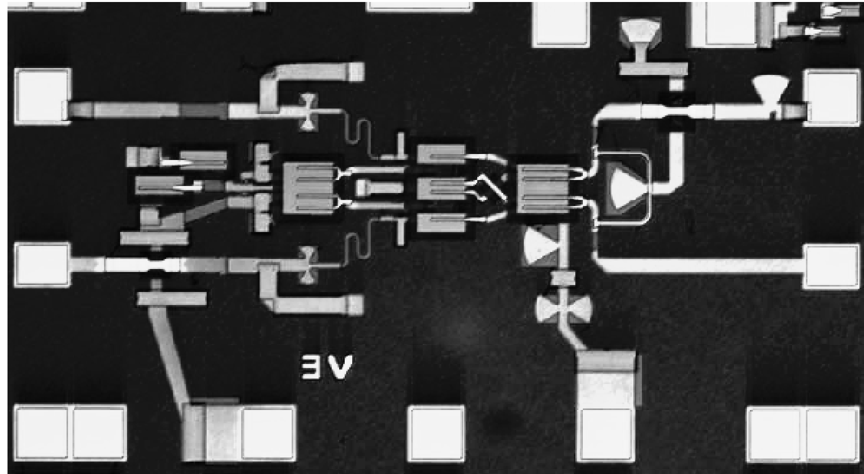


Figure 5.37: Die photo of differential cascode f_t doubler large signal amplifier.

was DC coupled to V_{CC} by a short across a series capacitor, and this resistor consistently fused when the amplifier was biased.

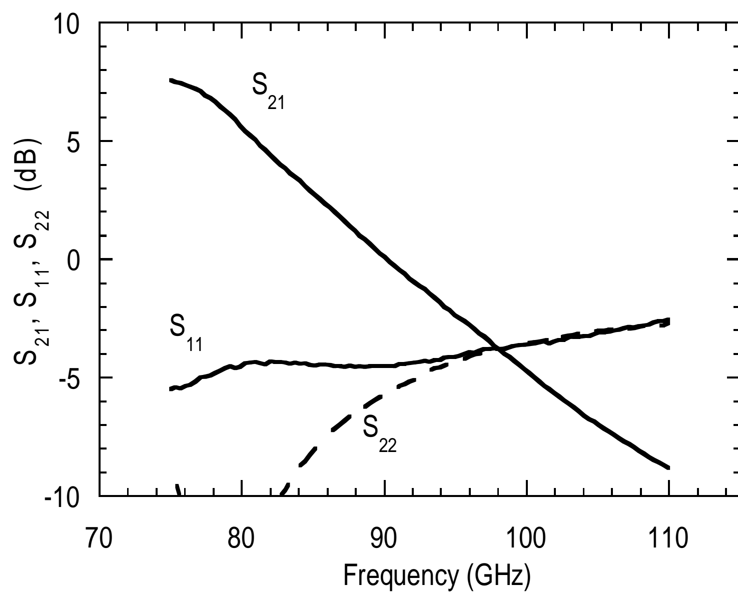


Figure 5.38: Small signal measurements of fabricated differential cascode amplifier.

5.9 Discussion

Some initial large signal amplifiers in the present small signal device technology were presented. Due to limitations of the available signal source, the output power of the W-band amplifiers could not be saturated. This difficulty had been anticipated, and two stage power amplifiers included on the mask set, but a layout error prevented biasing of these two stage amplifiers. Although the W-band amplifiers could not be driven to saturation, the output powers that were attained represent records for HBT integrated circuits in this frequency range. Furthermore, by virtue of the tight meandering of transmission lines allowed by the thin microstrip dielectric, the power amplifier MMICs were quite compact, and attained power densities referred to the die area quite competitive with the best HEMT MMICs in the literature.

While the power amplifiers in this work were designed for implementation in the Cu substrate process, the results presented here were from a wafer processed in the solder bonded process. The advantages of a metal substrate will be more important once InP emitters with better thermal conductivity, and InP collectors with higher potential power dissipation, are introduced. With the introduction of InP collectors, the maximum power load line will of course shift to larger resistances, and some redesign will be required of the reactively matched amplifiers of this work.

A serious error in the design of reactively matched amplifiers presented here was in not allowing for the process variability of deposited SiN_x. Such bracketing of tuning networks as was included in the mask set pertained to the output tuning networks, whereas the most significant actual variation seen was in the SiN_x capacitors which affected only the input tuning networks. In future, reactively matched circuit designs in this process should allow for substantial variations in any MIM capacitors used. Also, the measurement of SiN_x layers deposited on witness wafers immediately before or concurrently with the first half deposition on the real wafer, would allow greater repeatability of MIM capacitors.

Chapter 6

Conclusion

6.1 Achievements

In this work, a metal substrate process was developed which allowed, for the first time, entire 50 mm wafers of integrated circuits to be fabricated with transferred substrate HBTs. High performance HBTs and simple integrated circuits fabricated in this process were demonstrated. While this metal substrate technology promises eventually to provide improved heat sinking of the active devices, the immediate benefits are the ability to process entire wafers and the availability of the ground conductor at the back surface of the finished structure. This back-side ground contact promises to allow successful packaging of complex very high speed integrated circuits. The heat sinking provided by the metal substrate is already superior to that of the prior, solder bonded process for integrated circuits with sustained large dissipated power densities.

Large signal amplifiers were designed and fabricated as part of this work. The fabricated amplifiers demonstrated the highest output power to date from any bipolar integrated circuit at frequencies above 70 GHz. A reactively matched cascode power amplifier delivered 10 dBm of output power under 1.7 dB of gain compression at 75 GHz. An integrated balanced pair of these amplifiers delivered 10.7 dBm of output power under 1 dB of gain compression at 78 GHz. A reactively matched common base power amplifier delivered 9.7 dBm of output power at 82.5 GHz with an associated gain of 4.5 dB under only 0.8 dB of gain compression. With modest revisions, these circuit designs will yield similar output powers at 94 GHz.

6.2 Future Work

Future generations of high speed integrated circuits will demand significant innovations in interconnect and packaging architectures. The metal substrate technology demonstrated in this work constitutes an effective approach to integrating transmission lines, ground vias and active devices appropriate to 100+ GHz electronics within the context of the transferred substrate HBT device structure. For less esoteric device structures not requiring access to both sides of an epitaxial film, simpler deposited strip or microstrip-like transmission line architectures will suffice.

The metal substrate process does not itself address the dominant contributor to device thermal resistance in the present InGaAs/InAlAs device structure. The very low thermal conductivities of these disordered ternary semiconductors, and the fact that heat is removed from the transferred-substrate HBT through the emitter mesa, lead to the largest temperature rises being internal to the transistor. With the adoption of InP emitters and collectors, the thermal conductivity within the transistor will improve considerably, and junction temperatures of devices decrease.

Problems remain with the plated substrate process, in particular at the stages of temporary mounting and demounting of the wafer, and with the substrate removal etch. To date, the mounting operation has consistently damaged the HBT wafer while it still resides on the InP substrate. The combination of enhanced plating rate at the edges of the wafer and a wax mounting procedure which could not provide sufficient planarization impacted lithographic alignment at the collector stage. It is suggested that these two problems might best be addressed by mechanically planarizing the plated ground plane prior to wax bonding, and further, by using a temporary mounting procedure which provides ample planarization. This last might consist of either mounting the ground plane down to a carrier wafer with bulk, molten wax, or by mounting the ground-plane with a suitable release layer coating to the carrier wafer with epoxy at room temperature.

Demounting of finished wafers was not attempted in this work, but some experiments were performed on test wafers. Because of the thin wax layers used, infiltration of suitable solvents to the center of the sandwich took many hours. Immersing the wax bonded sandwich in a suitable solvent heated (with appropriate safety precautions) to the melting temperature of the wax would greatly accelerate this procedure. Cutting arrays of grooves

into the surface of the carrier wafer with a dicing saw prior to mounting might facilitate timely demounting by allowing faster diffusion of the solvent.

Excess collector-base leakage currents were observed in many devices processed in the metal substrate process. Such poor junction characteristics have also been seen in some wafers processed in the solder-bonded, partial wafer, process. It is hypothesized that this issue may be process related, and asserted that shorter test process sequences would greatly facilitate understanding of the problem. As an initial avenue of investigation, the correlation or lack thereof between excess junction leakage and the appearance of pitting of the collector semiconductor surface might be established. The concentration of chloride ions and of undissociated HCl in the substrate etch while the InGaAs collector material is exposed may both be important, and both are potentially sensitive to the quantity of dissolved solder or other metal contamination in the etch.

In summary, a process was developed to extend the transferred substrate HBT technology to full wafers. This technology will enable packaging of very high speed integrated circuits. Together with the imminent introduction of InP layers to the device structure, the metal substrate process will greatly improve heat-sinking of integrated circuits with very high dissipated power density. The first large signal amplifier results in this device technology were demonstrated.

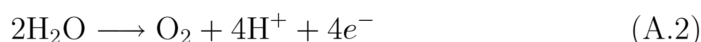
Appendix A

Electroplating

The electroplating process consists of electrolytic reduction of metal ions at a cathode and oxidation of an anode. For many metals and plating solutions it is common practice to use an anode of the metal to be deposited. This anode dissolves with the passage of current through the electrolytic cell, in the reaction

$$M \longrightarrow M^{z+} + ze^- \quad (A.1)$$

where M represents the metal involved, and z the charge state of its ions in solution. The use of such a soluble anode maintains the concentration of metal ions in solution even as these ions are reduced at the cathode. Where an insoluble anode is used, electrolysis of water constitutes the anode reaction[60, p. 517]:



$$2H_2O \longrightarrow O_2 + 4H^+ + 4e^- \quad (A.2)$$

the hydrogen ions on the right hand side of this equation lead to the acidification of the plating solution with continued current flow.

At the cathode, both deposition of the metal, in the reaction

$$M^{z+} + ze^- \longrightarrow M \quad (A.3)$$

and evolution of hydrogen, in the reaction

$$2e^- + 2H_2O \longrightarrow H_2 + 2OH^- \quad (A.4)$$

occur. The relative importance of these reactions varies with the metal and solution involved. In the plating of copper from $CuSO_4$ solutions at

useful current densities, almost no hydrogen is evolved and so the *cathode efficiency* is said to be near 100% [33, p. 185]. Likewise, cathode efficiencies are high in the deposition of Au from $Na_3Au(SO_3)_2$ solutions. The cathode efficiency of Ni deposition from nickel sulfamate solutions can be much lower.

The activation potential η_a, that is the potential across the space charge region (electrical double layer) at an electrode is given by the Tafel equation[61, 33]:

$$\eta_a \approx \frac{2RT}{zF} \ln \left[\frac{j}{j_o} \right] \tag{A.5}$$

where R is the gas constant, F is Faraday's constant (the charge in one mole of electrons), z is the charge state of the species depositing, and j_o is the exchange current density. In addition to this activation potential, a further *concentration* potential is associated with the depletion of ions from the solution near the space charge region [33, p.17]

$$\eta_{\text{conc}} = \frac{RT}{zF} \ln \left[\frac{C_c}{C_o} \right] \tag{A.6}$$

where C_c is the concentration of the metal ion at the edge of the space charge region and C_o is its bulk concentration.

The roughness of the metal surface deposited on the cathode inherently tends to increase with continued deposition. Transport of the metal ions across the region of liquid depleted of them to the cathode is by diffusion. The ionic current density is given by the diffusion equation

$$J_c = -D\nabla C \tag{A.7}$$

where D the diffusivity of the ion in the liquid. Note that, for a uniform cathode potential, J_C will be enhanced at high points of the cathode. The ion diffusivity increases with temperature. The thickness of the diffusion layer in the liquid is a strong function of mass transport conditions: i.e. agitation. For given solution, temperature and agitation conditions, increasing the current density will eventually lead to the cathode increasing in roughness with deposition time. This represents an instability of the surface in the sense that any perturbation from smoothness increases with time. In cases of extreme surface instability, the deposited metal surface evolves into treed dendrites.

The traditional solution to the problem of surface instability in commercial practice is to add certain carefully selected organic species to the plating solution which tend to inhibit deposition of the metal. Precisely because the inhibitors deposit preferentially on peaks of the cathode surface, metal deposition there is decreased the most. The surface concentrations of inhibitor molecules required to stabilize surfaces are very low and greater depletion depths for the additives than the metal ions are desirable. Because the concentrations of additives in the plating solution are therefore very low, agitation is required to achieve transport of the additives that is uniform in the time average. Careful plating cell design is required to achieve uniform deposit thickness when plating from solutions with additives[62].

A.0.1 Epitaxy

Some component of epitaxial growth occurs in electroplating of metals. The epitaxial growth of grains at the surface of the cathode can itself contribute to roughening of the surface. This phenomenon is particularly evident in the plating of Cu from $CuSO_4$ solutions Most technological applications of electroplated metal demand films which are both smooth and fine-grained In order to achieve fine grained films, further additives, often organic, are included in commercial plating solutions. Very low concentrations — on the order of 1ppm by volume — of such grain refining additives or "brighteners" can be effective in Cu and Ni plating [34, p.208]. Many organic compounds turn out to have some inhibiting or grain refining effect, and this makes electroplating solutions notoriously sensitive to any organic contamination: 1–10 mg of impurity per liter of solution can have serious consequences [33, p.191].

A.0.2 Alternating Current Plating: Diffusion Limited Etching

Whereas diffusion limited deposition suffers from inherent instability, diffusion limited etching tends to make surfaces smoother. Electroplating from many electrolytes is a reversible electrochemical reaction. Copper plating from solutions of $CuSO_4$ and H_2SO_4, for instance, is reversible. For these reversible chemistries, judicious choice of alternating current waveforms can be used to stabilize deposit surfaces. By choosing an etching current density

significantly larger than the plating current density, the etching current distribution can readily be made less uniform than the plating current density distribution, while still maintaining an average “forward” current.

Electrochemical etching is complicated by the presence of grain boundaries. Practical deposits, and soluble anodes, consist of polycrystalline metals, and etching rates are almost always enhanced at grain boundaries. This enhanced etching leads to grains becoming detached from the anode. Filtration is required to prevent repeated or continuous etching operations from filling the plating cell with suspended grains of metal. Such grains of metal can become attached to the plated film on the cathode and severely impact surface roughness. It is in particular worth noting that where alternating current is used to electroplate in a cell with an insoluble anode, it would be wise not to plate metal on this insoluble anode during the cathode etching cycle but rather to provide a secondary cathode.

A.0.3 Interrupted Current

Deposits can sometimes be improved by plating with interrupted DC current. With duty cycles less than 100%, the peak current density increases above the average current density. High current densities favor nucleation of new grains over growth of existing ones. Where the surface mobility of adatoms is sufficiently low, and the room-temperature recrystallization sufficiently slow, plating at low duty cycles can be used to form particularly fine grained deposits. The period of zero current itself improves the quality of deposit in the case of nickel plating. The deposition potential of nickel from common electrolytes is high, and so the rate of electrolysis of water competes with the deposition of nickel. It has been found that periodic interruptions of the plating current reduce the entrapment of hydrogen in plated nickel and also reduce the compressive stress in the deposit[63].

Appendix B

Mechanical Drawings

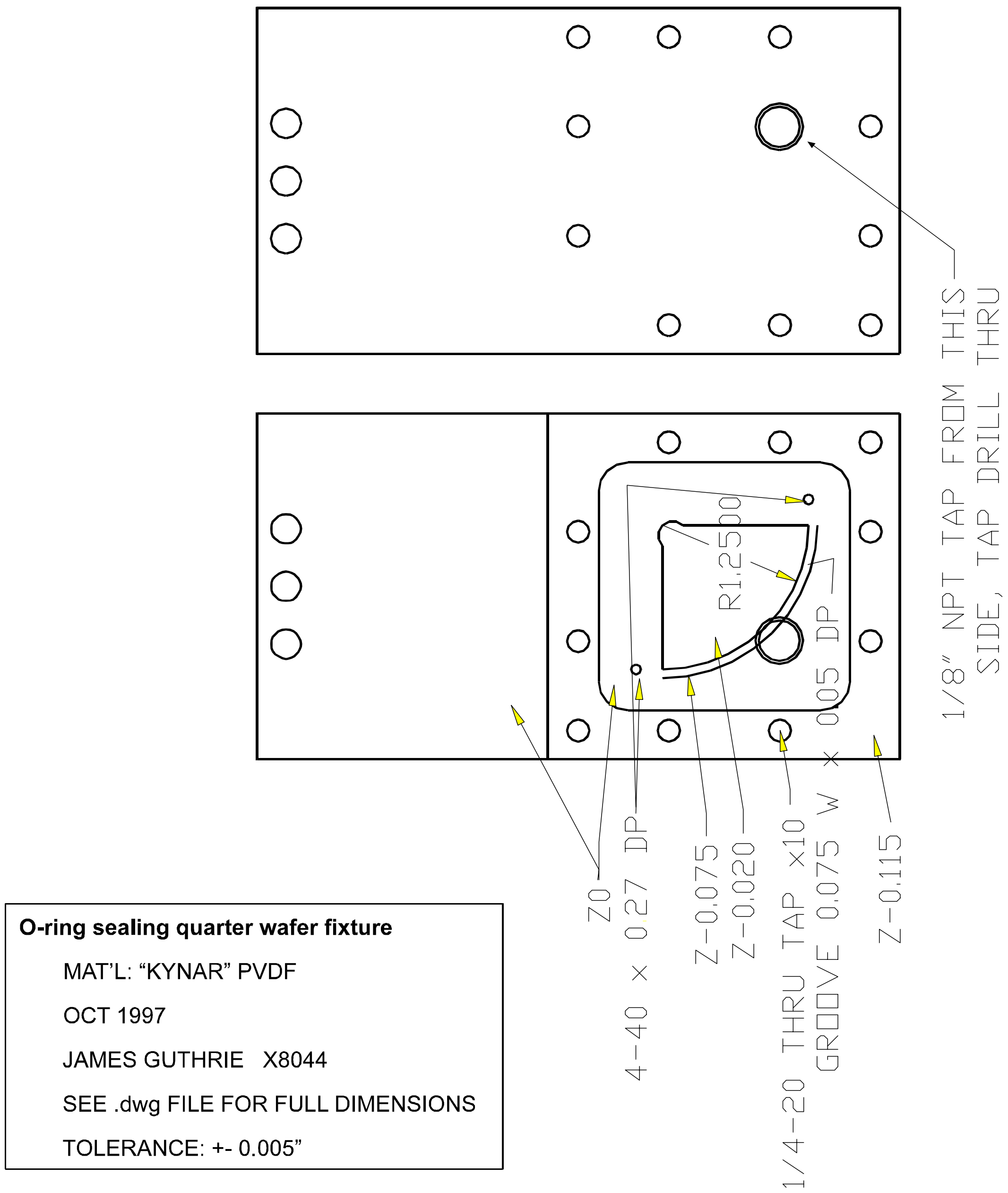


Figure B.1: Quarter wafer o-ring sealing plating fixture, mounting block. Wafer is held in place, and electrical contacts are made with two of the smaller Be-Cu spring finger contacts stocked by J. Whaley.

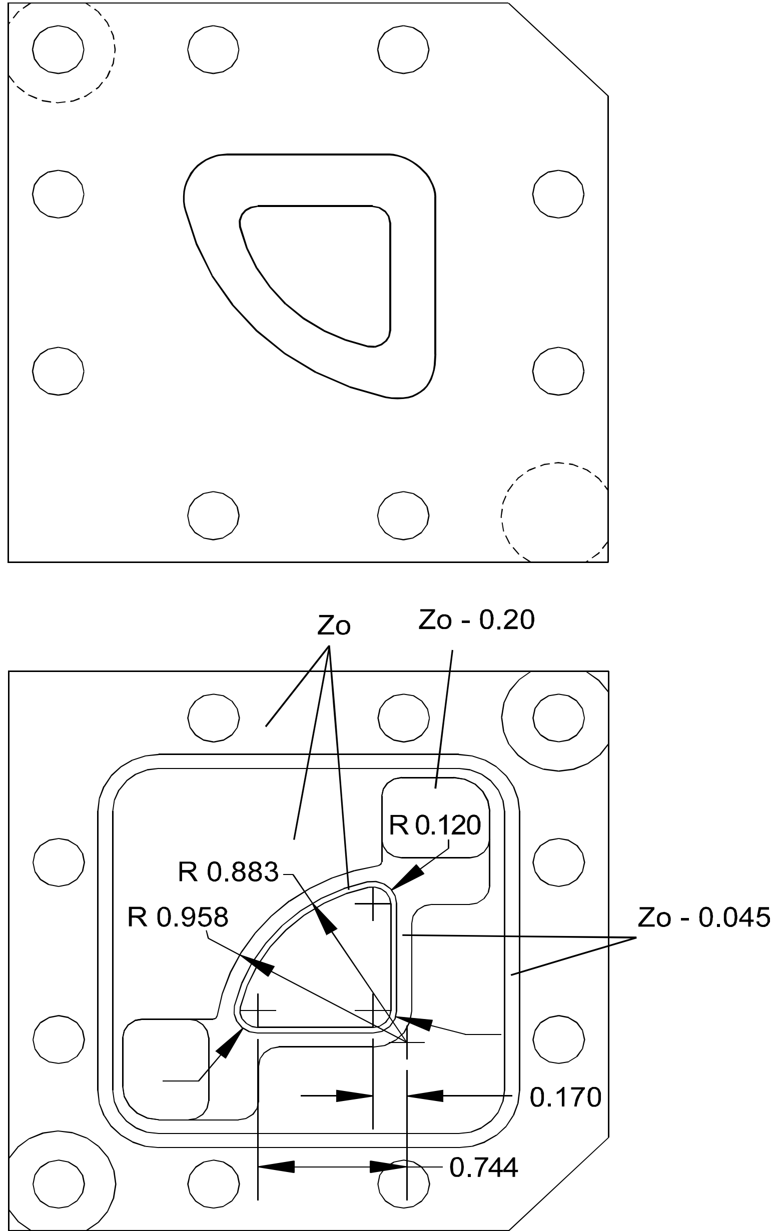


Figure B.2: Quarter wafer o-ring sealing plating fixture, bolt ring. Inner groove accepts 2-020 size o-ring, while outer accpets size -034.

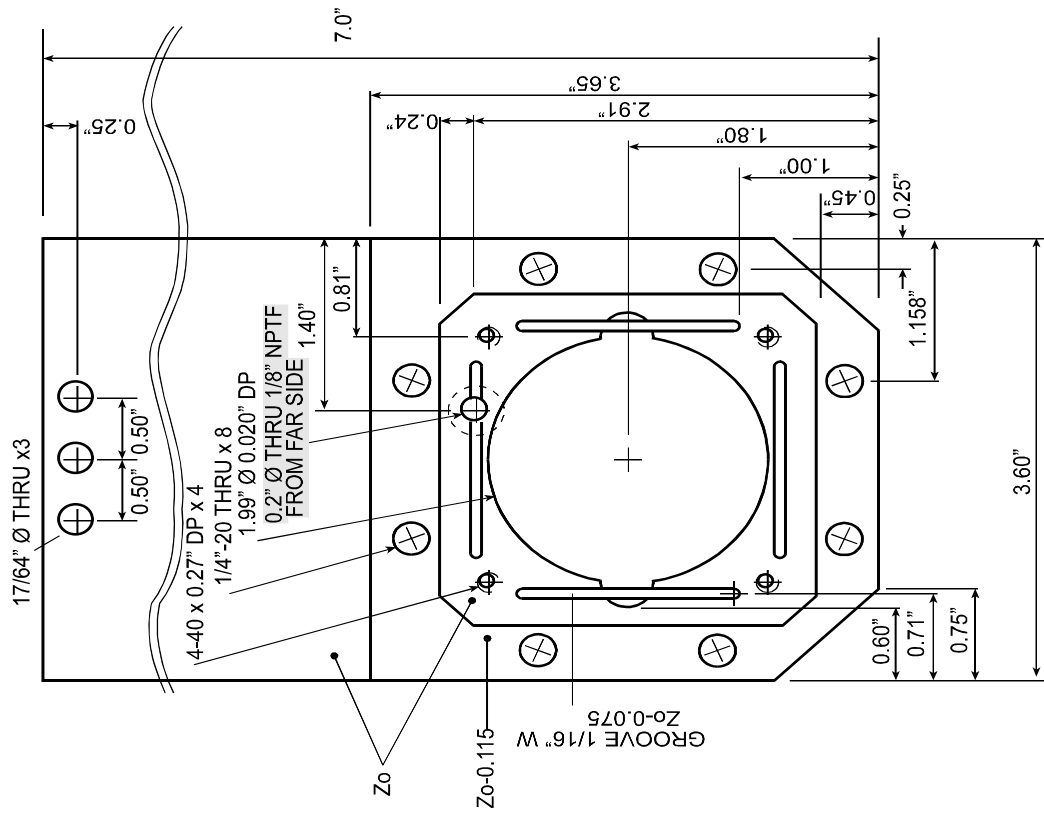
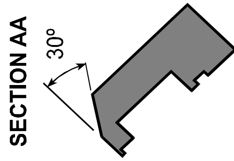


Figure B.3: Full wafer o-ring sealing plating fixture. N.B. that recess dimensions have to be increased to acommodate 50.8 mm diameter wafers.

TWO INCH WAFER PLATING FIXTURE RING
MAT'L: 1/2" KYNAR SHEET
MATERIAL BURRS BADLY
DO NOT CLEAN WITH ACETONE
JAMES GUTHRIE X8044
NOV 18, 1997



BEVEL 0.28" DP ?

TOP

3.60"
3/4"
0.25" R
0.25" R
Zo - 0.2
Zo
3.60"
1.158"
0.25"
0.45"
0.55"
0.62"
2.45"
A
A
17/64" Ø THRU x8 CHAMFERED FAR SIDE
GROOVE 0.045" DP 0.075" WIDE
GLAND 0.045" DP FOR -031 O-RING (e.g. 1.737 ID ?)
LIP 0.03" RADIALLY FROM THRU HOLE TO GLAND

BOTTOM

Figure B.4:

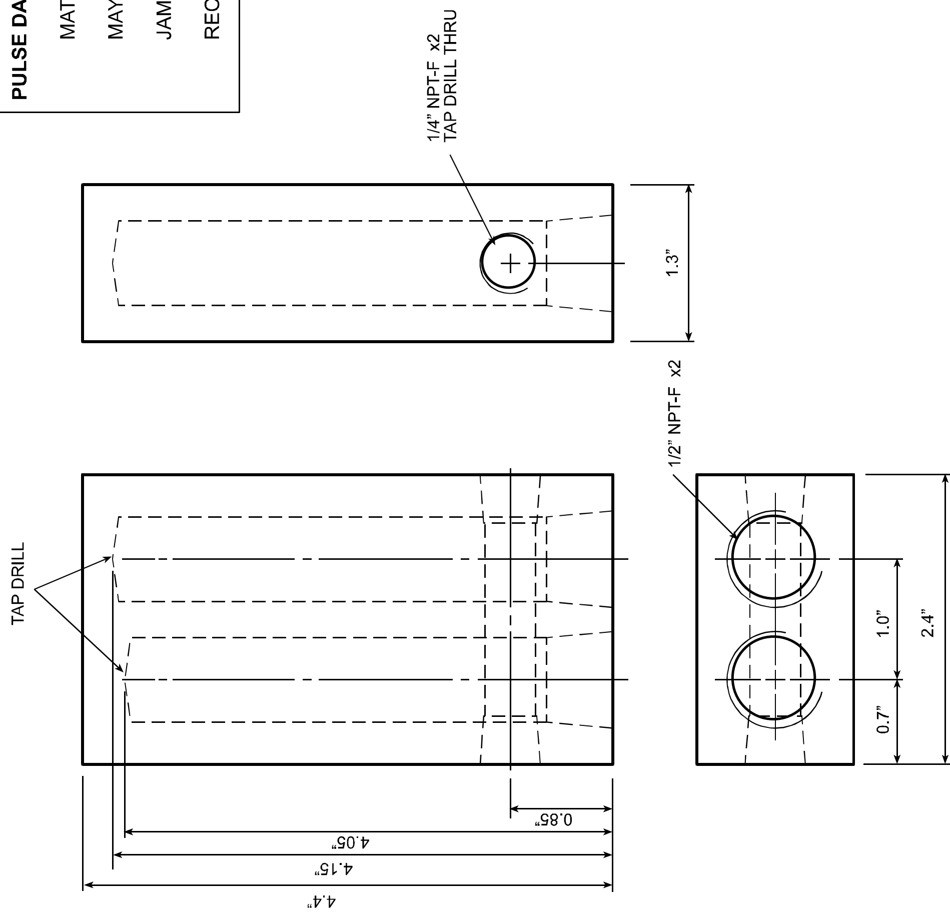


Figure B.5: A simple surge dampener used to reduce the pressure surges in plating solution circulated by a diaphragm pump. The air cavities of this simple design tend to fill over a period of about eight hours of use.

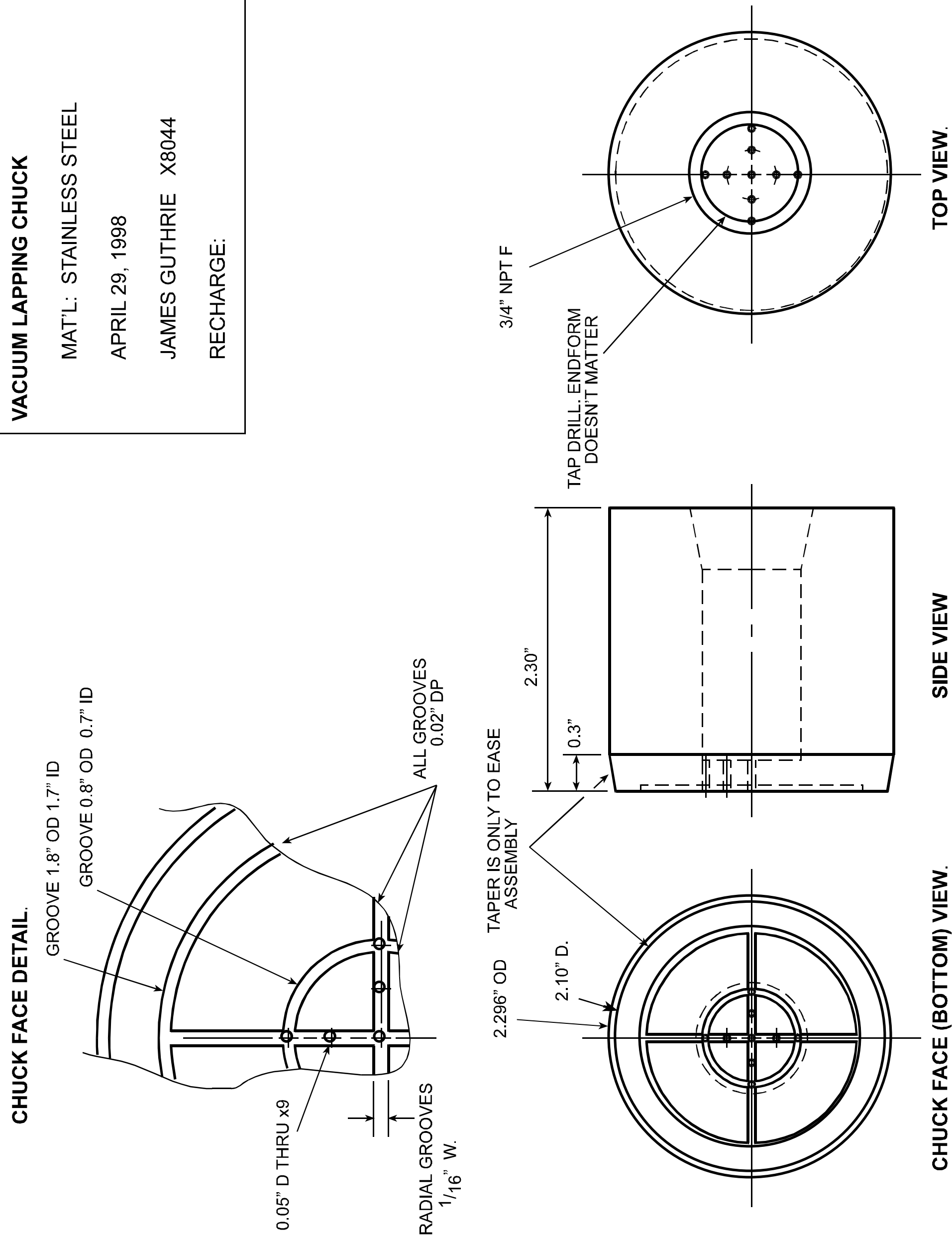


Figure B.6: A vacuum chuck fixture for the lapping of full wafers. N.B. that a straight bore and mating o-ring fitting were used in place of the pipe thread in the actual fixture.

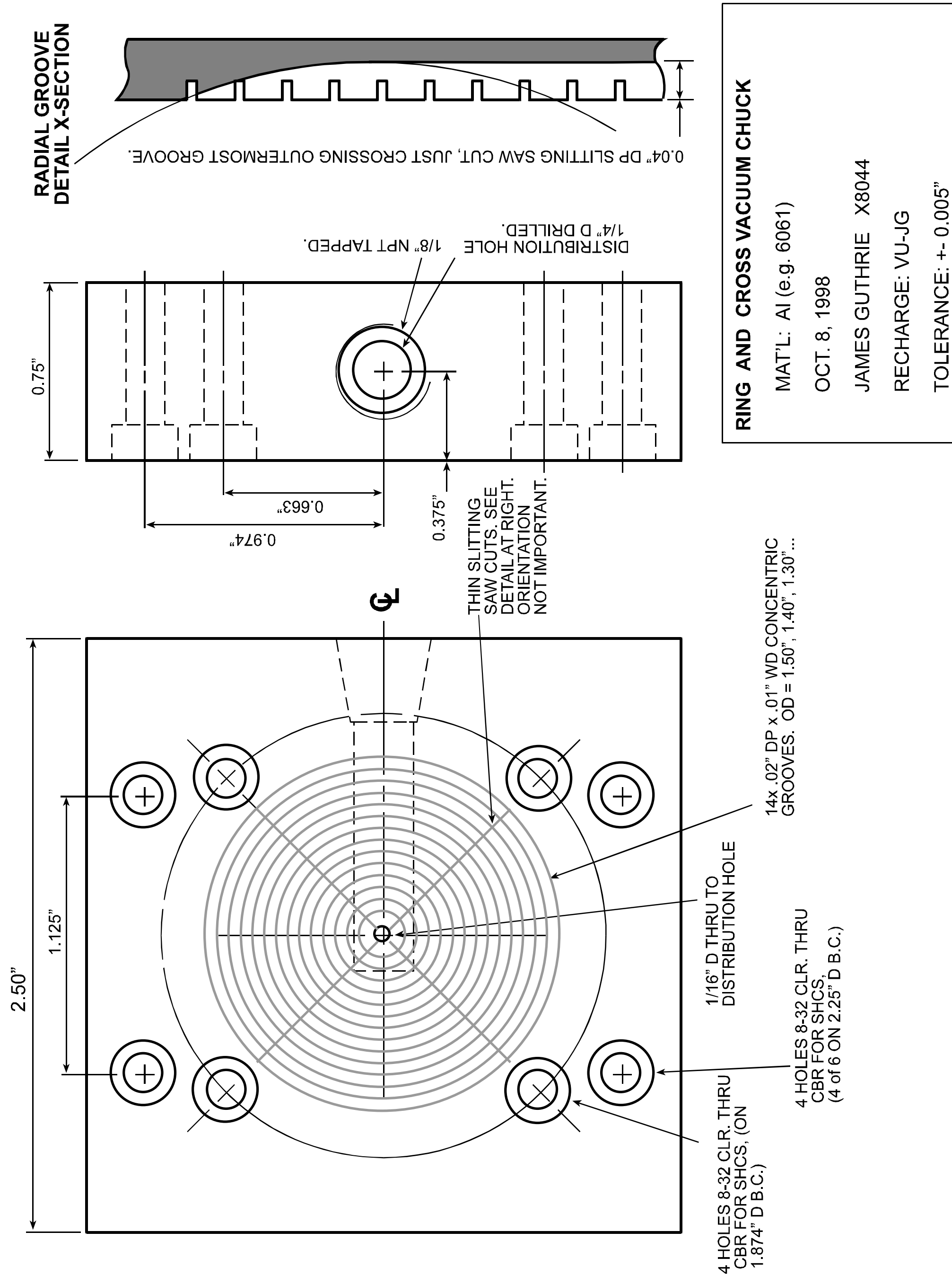


Figure B.7: Vacuum chuck to hold thin plated wafer.

Appendix C

Process Recipe

C.1 Summary

Step	Mask	Systems used
Emitters	Emitter	Stepper, Evaporator
Emitter Etch		RIE-2, PE-IIA
Base Contact	BCon	Stepper, Evaporator
Sinter		RTA
Mesa Isolation	Mesa	Stepper, RIE-5
Polyimide		Blue M oven
PI etchback		RIE-1
PI pattern	PIetch	Stepper, PE-IIA
Resistor Protect	ResPro	Stepper, PE-IIA, PECVD
Resistors	Resistors	PECVD, Stepper, Evaporator
Metal 1	M1	Stepper, Evaporator
Nitride Dep		PECVD
Nitride Via	SiN	Stepper, RIE-3
Metal 2	M2	Stepper, Evaporator
Apply BCB		Blue M oven
BCB via etch	BCB	Stepper, Evaporator, RIE-3
Ground Plane		Sputter, Plating Fixtures
Wax Mounting		Vacuum bonder, hotplate
Substrate Etch		Etch Bench
Collector	Col	Stepper, Evaporator
Recess Etch		

C.2 Emitter Litho

SPR 950 CEM Process

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

1. Dehydration bake: 3 minutes on 120°C hotplate
2. **Warning For full wafers, you must install one of the flat surface spinner chucks.** These are the chucks with the bare stainless steel surface marked by a spiral groove and intersecting radial grooves. The 2" o-ring chucks apply significant bending forces to the wafer — enough to break III-V wafers. Use our private chuck, or soak the public chuck in Shipley "1165" to remove any PMGI residue left by other users.
3. Wafer on spinner chuck with vacuum, blow with N_2
4. Apply SPR 950 with syringe and filter to cover wafer
5. Spin at 2.5 krpm for 30 sec.
6. Soft Bake, $90°C$, 60 sec. on hotplate
7. set spinner to 4kRPM
8. Wafer on spinner chuck with vacuum, blow with N_2
9. Apply ACEM 3651s with syringe and filter to cover wafer
10. Spin at 4kRPM for 30". **Do Not Bake.**

C **Exposure**

1. This step writes the alignment targets for all subsequent steps. Align the mask to the stepper platten carefully. Align the emitters perpendicular to the wafer major flat: for masks to date, this has meant seating the wafer major flat against the pins on the stepper paddle chuck.
2. Use exposure time of 2.4" on the stepper.
3. Focus: **total** focus of 44 has worked for many months. Focus array on Michelle's 2.25 inch Si wafer can also be used. In the latter case, use a total focus of Si focus − system focus +40. The free 2.25 inch Si wafers are somewhat suspect though, in that these wafers are near the minimum allowable thickness for the stepper.
4. For latent image focus arrays, use 2.5" exposure.

D **Post Exposure Bake** bake at $100°C$ for 2 min. 10 sec.

E **Development**

1. Immerse in DI in Develop DI rinse beaker for 30 sec.
2. Immerse in MF701 developper (TMAH developper beaker) for 2 min 20 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2
5. Inspect under microscope with yellow filter. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure/ focus array.

F **Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency
3. Run for 15 seconds

G **Surface Preparation**

1. Mix HCl oxide etch. To 200ml of DI add 20ml HCl.
2. Dip for 15 seconds.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2

H **Metal Evaporation**

1. Mount wafer to E-Beam sample holder, being careful that the sample hangs with its surface perpendicular to the evaporator source.
2. Make sure the crystal monitor reads < 9; change if necessary.
3. Pump down to at least 1×10^{-6} Torr.
4. Deposit material:

Material	Thick	Rate	Vernier
Ti	200	2-3	1.65
Pt	425	1.5	1.90
Au	8000	~15	1.55
Si	650	4	1.65

I **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

J **Inspect** Inspect pattern under microscope. Measure metal thickness of broad features with Dektak.

C.3 Emitter Mesa Etch

Base Emitter Etch

A **Surface Preparation**

1. Photoresist plasma descum, 300 mTorr of O_2, low frequency, 100 W, 30 sec.
2. Surface dip, dilute NH_4OH (1:10), 15 sec.
3. Rinse in DI for 3 min and blow dry.

B **Dry Etch**

1. Clean both plates, and shield of RIE2 with ISO-soaked wipes.
2. Turn laser on now to let it warm up.
3. O_2 plasma clean, 20 sccm, 125 mTorr, 500V bias, 30 min.
4. Precoat chamber, ($CH_4/H_2/Ar$, 4/20/10 sccm, 125 mTorr, 300V bias, 20 min).
5. Load wafer: press down on chamber lid as you turn on the roughing pump. Align laser monitor. Pump down to mid 10^{-6} Torr.
6. Set up Chart recorder. Low pass filter the output of power monitor box, using e.g. the blue BNC box from RIE 1.
7. Etch, $CH_4/H_2/Ar$, 4/20/10 sccm, 75 mTorr, 500 V bias until slope of laser monitor plot changes.
8. Increase pressure to 110 mTorr.
9. Continue to etch until desired stop point reached (determined from the laser monitor output plot) $3/2 \cdot \Delta T$.
10. Remove polymer, (O_2, 50 sccm, 125 mTorr, 200 V bias for a quarter of etch time).

C **Si Removal**

1. 300 mTorr CF_4, low frequency, 100 W, 90 sec.
2. Inspect under microscope for remaining Si.
3. Repeat in steps of 30 sec until all Si is gone.
4. Remove samples, clean chamber for 10 minutes with O_2, low frequency, 300 W, 300 mTorr.
5. Plasma descum, 300 mTorr of O_2, low frequency, 100 W, 15 sec.

D **Selective Etch for InAlAs (A+B etch)**

1. Surface dip, dilute NH_4OH (1:10), 10 sec.
2. Rinse in running DI for 3 min and blow dry.
3. Mix solution B - HCl:H_2O :: 4:1. 125 mL total in HCl beaker. Use HCl graduated cylinder.
4. Mix solution A - HBr:Acetic acid :: 1:1. 125 mL total in A+B beaker. Use Solution A cylinder.

5. Mix solution A:B :: 1:1, stirring at 300 rpm.
6. Stop stirring, etch for 13 sec.
7. Rinse in DI for 3 min and blow dry.

E **Non-Selective Etch**

1. Mix etchant as follows: 55 ml of 1 M citric acid in 220 ml DI. Mix well. Add 5 ml hydrogen peroxide. Mix well. Add 1 ml phosphoric acid. Mix well.
2. Stirring at 200 rpm etch for 25 sec by suspending the wafer vertically in a holder.
3. Rinse in DI for 3 min and blow dry.
4. Proceed directly to base contact lithography.

C.4 Base Contacts

5214 Process

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

1. Dehydration bake: 3 minutes on 120°C hotplate
2. Wafer on spinner chuck with vacuum, blow with N_2
3. Apply AZ 5214 with syringe and filter to cover wafer

4. Spin at 6 krpm for 30 sec.
5. Soft Bake, 95°C, 60 sec.

C **Exposure**

1. Use exposure time of 0.35 seconds on the stepper.
2. As of October 1998, **Total** focus of +18 is fairly consistently the result of latent image focus array test on stepper.
3. For latent image focus arrays, use ???? exposure.

D **Post Exposure Bake** bake at 105°C for 60 seconds.

E **Flood Expose** Expose the entire wafer for 30 seconds at 7.5mW/cm^2 on Karl Suss mask aligner. Make sure that i-line filter is not in use.

F **Development**

1. Mix AZ 400K : DI 1:5.5
2. Immerse wafer in developper for 40 seconds
3. Rinse in running DI water for 3 min.
4. Blow dry with N2
5. Inspect under microscope. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array. More to the point, if you see too much undercut, then you need more (patterned) exposure.

G **Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency
3. Run for 15 seconds

H **Surface Preparation**

1. Mix HCl oxide etch. HCl:DI 1::10
2. Dip for 20 seconds.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2

I **Metal Evaporation**

1. Charge the small tungsten cylinder "bazooka" Au source less than half full. Very little Au is deposited in this step, and any metal left over will tend to crack the cylinder as it contracts in cooling from the melting point of Au.
2. Mount wafer to E-Beam sample holder.
3. Make sure the crystal monitor reads < 9; change if necessary.
4. Pump down to at least 10^{-6} Torr.
5. Deposit material:

Material	Thick	Rate	Vernier
Ti	200	2-3	1.65
Pt	425	1.5	1.90
Au	800	~15	1.55

J **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

K **Sinter**

1. Remove external, dummy thermocouple, and install internal thermocouple as necessary. Clamp quartz tube to door. Red lead goes to TC lead that is attracted to magnets.
2. Run RTP from command line of PC, as necessary. Password is "BOB".
3. Under Runs, choose program "300/1' "
4. Wait till temperature drops back down to 100°C before unloading your wafer.

C.5 Mesa Isolation

Chlorine RIE

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale while your head is under the hood.

1. Wafer on spinner chuck with vacuum, blow with N_2
2. Apply SPR 518 with syringe and filter to cover wafer
3. Spin at 3 kRPM for 30 sec.
4. Soft Bake, $90°C$, 60 sec. on hotplate

C **Exposure**

1. Use exposure time of 1.1" on the stepper.
2. For latent image focus arrays, use ???? exposure.

D **Post Exposure Bake** bake at $110°C$ for 60 seconds.

E **Development**

1. Immerse in MF701 developper (TMAH developper beaker) for 90 seconds.
2. Rinse in running DI water for 3 min.
3. Blow dry with N2

4. Inspect under microscope with yellow filter. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array.

F **Post Exposure**

1. **Do Not Forget This Step** Flood expose 2 minutes under Karl Suss, 7.5mW/cm^2.
2. O_2 plasma descum 300mT 100W 20 seconds.

G **Hardbake** 20 minutes in 120°C oven in Petri dish without cover.

H **Pre-clean RIE 5**

1. Select a 4" Si wafer. Scrub with iso-wet swabs.
2. Load wafer, transfer into chamber of RIE 5.
3. Run the "LeeGan" Cl_2 clean program.
4. Unload Si carrier wafer, watching spot on laser monitor to identify the spurious window reflection.

I **Chlorine Etch**

1. Place your wafer on precleaned 4" Si wafer, and load system.
2. Pump down to 2.5×10^{-6} Torr
3. Set up laser monitor. Chart recorder scales of $\approx$ 500mV and 1min/cm.
4. Etch under Manual control.
5. Cl_2 flow = 20.0sccm
6. chamber pressure 5.0 mTorr
7. Power = 150 W (this is what is controlled). Voltage is usually 150-175 V
8. Etch 15 seconds into the InAlAs buffer. Usually six minutes 15 seconds total for 300nm collector, 1/4 wafer.

J **Strip Resist**

1. Immerse wafer in developper for 3 minutes.
2. Rinse in running DI for 3 minutes.
3. Blow dry with N_2 gun.

K **Under-characterized "optional" Ash Step**

1. O_2 plasma photoresist ash in Technic: 300mT, 100W, 30 seconds
2. Inspect and remediate: Inspect under optical microscope, and subject wafer to further O_2 ashing as indicated

C.6 Polyimide planarization

Polyimide Process

A **Warm Polyimide** Take our polyimide, Dupont Pyralin PI-2556 out of the resist refrigerator.

B **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M $\Omega\cdot$cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

C **Mix Adhesion promoter Explanation** Amino-silane adhesion promoters in weak solutions are said to be prone to polymerization — creating particles. You must mix the adhesion promoter fresh every time.

1. Add 1mL of VM-651 adhesion promoter with a disposable pipette to 200mL of DI. Stir with and then discard the pipette.
2. **Polyimide Application**
3. Dehydration bake: 3 minutes on 120°C hotplate
4. Chuck wafer on spinner.
5. Blow off with N_2 gun.
6. Apply adhesion promoter mixture with a pipette to cover the wafer.
7. Wait for 20 seconds.

8. Spin at 3kRPM for 60 seconds.
9. Blow off with N_2 gun.
10. Bake for 3 minutes on hotplate at 120°C.
11. Chuck wafer on spinner.
12. Blow off with N_2 gun.
13. Apply Pyralin PI 2556 polyimide to cover wafer with syringe and $1\mu m$ filter.
14. Spin at 2.5 kRPM for 30 seconds.
15. Line bottom of Petri dish with aluminum foil, then return wafer to the dish.
16. Bake polyimide in the Blue M oven in petri dish without cover. Turn N_2 flow up to 100scfh on rotameter beside oven. Run program 3:
    (a) $90°C$ for 60 min.
    (b) ramp to $150°C$ over 15 min.
    (c) hold at $150°C$ for 60 min.
    (d) ramp to $230°C$ over 20 min.
    (e) hold at $230°C$ for 60 min
    (f) cool down naturally. Wait until temperature reaches $170°C$.

D **Photoresist Application**

1. Cool down at least 5 min.
2. Chuck wafer on spinner with vacuum, blow with N2
3. Apply AZ P4330-RS with syringe and filter to cover wafer
4. Spin at 5 krpm for 30 sec.
5. Soft Bake, $90°C$, 30 min. in petri dish without cover

E **Hardbake**

1. Hardbake photoresist at $120°C$ for 30 min

F O_2 **R.I.E. Etch**

1. Load system according to instructions. Four small dots of mung, spread thin with swabs should suffice to hold a full 2" wafer. Set wafer down on these spots, and gently press it down by its edges, moving around the wafer with plastic tweezers or swab handle. Check its adhesion by pushing on its edge (i.e. trying to shear the wafer with respect to Cathode).

2. Pump down to at least 5×10^{-6} Torr
3. Set up laser monitor:
   (a) the reflection from sample, as opposed to those from various window surfaces, is generally the one closest to gowning room. Reflections off the windows are visibly double spots.
   (b) Set up chart recorder for 1 hour and $\approx 1V$ full scale
4. Turn off Ion Gauge
5. Turn on chiller and circulator.
6. Etch Conditions:
   (a) O_2 flow rate 7.0 sccm
   (b) chamber pressure $10mT$
   (c) $P = 60W$ (this is what is controlled)
   (d) Voltage $350V$ — Voltage and pressure determine etch characteristics
7. Etch for 18.5 cycles
8. Remove mung. If holding wafer in hand, use tight latex "solvent" gloves.
9. Emitters should be exposed at this stage. Check on Dektak.
10. : remedial action:
    (a) Clean off mung.
    (b) Plasma etch in steps of 2 minutes.
    (c) 300mT of O_2, 200W at low frequency.

G **PI patterning**

H **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale while your head is under the hood.

1. Wafer on spinner chuck with vacuum, blow with N_2
2. Apply SPR 518 with syringe and filter to cover wafer
3. Spin at 3 kRPM for 30 sec.
4. Soft Bake, $90°C$, 60 sec. on hotplate

I **Exposure**

1. Use exposure time of 1.1" on the stepper. Total focus of 12−system. Do not use DFAS at this stage.

2. For latent image focus arrays, use ???? exposure.

J **Post Exposure Bake** bake at 110°C for 60 seconds.

K **Development**

1. Immerse in MF701 developper (TMAH developper beaker) for 90 seconds.
2. Rinse in running DI water for 3 min.
3. Blow dry with N2
4. Inspect under microscope with yellow filter. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array.

L **Post Exposure Do Not Forget This Step** Flood expose 2 minutes under Karl Suss, 7.5mW/cm^2.

M **Hardbake** 20 minutes in 120°C oven in Petri dish without cover.

N **Plasma Etch**

1. load wafer in Technics PE IIA
2. Etch 300mT O_2 100W 28 minutes

O **Strip Resist**

1. Immerse wafer in MF 701 developper for 2 minutes.
2. Rinse in running DI for 3 minutes.
3. Blow dry with N_2 gun.

C.7 Resistors

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.

2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Polyimide Reflow Bake** Bake wafer on 250°C hotplate for 10 minutes. Where the resistor patterning follows polyimide patterning directly, the dehydration bake for the resistor patterning step and the bake to reflow the polyimide are combined.

C **Deposit Underlayer of** SiO_2

1. Run 30clnSiO program on PECVD.
2. Mix HCl surface dip. To 200 mL of DI add 20 mL of HCl.
3. Dip wafer in HCl solution for 20 seconds.
4. Rinse in running DI for 3 minutes.
5. Blow dry with N_2.
6. Load wafer in PECVD and pump to low vacuum.
7. Deposit first layer of SiO_2 with SiO20 program.
8. Immerse wafer in ISO for one minute at solvent bench. Squirt with iso.
9. Blow dry with N_2.
10. Load wafer in PECVD again, and deposit remainder of oxide film with SiO20 program.

D **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

1. Oxide coated wafer must be primed with HMDS.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 518A with syringe and filter to cover wafer
4. Spin at 4 kRPM for 30 sec.
5. Soft Bake, $90°C$, 60 sec.

E **Exposure**

1. Expose with RESPRO mask plate for 0.9 seconds with focus offset of 38.

2. Post exposure bake: 110° C for 60 seconds.
3. Develop 90 sec. in MF701 (TMAH developer beaker).
4. Rinse 3 minutes in running DI.
5. Blow dry with N_2.
6. Oxygen plasma descum 20 seconds on PE-IIA
7. Hardbake: 20 minutes in 120° C oven.
8. Mix oxide etchant mix buffered HF:DI::1:10
9. Etch oxide for 3.5 minutes
10. Rinse in running DI for 3 minutes.
11. Blow dry with N_2.
12. Inspect for any remaining oxide.
13. Strip resist with acetone in lift-off beaker.
14. Oxygen plasma descum 30 seconds in PE-IIA.

F **Spin Clean**

1. Apply vacuum to hold wafer to spinner chuck.
2. Prepare yourself with a wash bottle of acetone and a wash bottle of isopropanol.
3. Set the spinner speed and time for the following application step.
4. start the spinner, and irrigate the spinning wafer with acetone, then iso, acetone again, and a final iso rinse, not letting the wafer dry in between solvents. No dehydration bake is required.

G **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

H **Photoresist Application**

1. Wafer on spinner chuck with vacuum, blow with N_2
2. Apply AZ 5214 with syringe and filter to cover wafer
3. Spin at 6 krpm for 30 sec.
4. Soft Bake, $95°C$, 60 sec.

I **Exposure**

1. Use exposure time of 0.35 seconds on the stepper.

2. As of October 1998, **Total** focus of +18 is fairly consistently the result of latent image focus array test on stepper.
3. For latent image focus arrays, use ???? exposure.

J **Post Exposure Bake** bake at $105°C$ for 60 seconds.

K **Flood Expose** Expose the entire wafer for 30 seconds at 7.5mW/cm^2 on Karl Suss mask aligner. Make sure that i-line filter is not in use.

L **Development**

1. Mix AZ 400K : DI 1:5.5
2. Immerse wafer in developer for 40 seconds
3. Rinse in running DI water for 3 min.
4. Blow dry with N2
5. Inspect under microscope. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array.

M **Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency
3. **Run for 45 seconds**

N **Surface Preparation**

1. Mix HCl oxide etch. HCl:DI 1::10
2. Dip for 20 seconds.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2

O **Metal Evaporation Caveat:** there is evidence to suggest that evaporated Si is ineffective as a sticking layer. If you are going to rely on Si to perform this function, be careful to proceed quickly from the surface preparation dip to evacuating the evaporator. **N.B. that effective sheet resistance of NiCr on PECVD oxide has to be characterized. In the past, very high apparent resistivities have been seen — possibly due to roughness of the oxide film.**

1. Mount wafer to E-Beam sample holder.

2. Make sure the crystal monitor reads < 17; change if necessary.
3. Pump down to at least 1×10^{-6} Torr.
4. Deposit material:

Material	Thick	Rate	Vernier
NiCr	550	1	1.70

P **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

C.8 Metal 1

Thick 5214 Process

A **Solvent Cleaning**

Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

1. Dehydration bake: 3 minutes on 120°C hotplate
2. Wafer on spinner chuck with vacuum, blow with N_2
3. Apply AZ 5214 with syringe and filter to cover wafer
4. Spin at 4 krpm for 30 sec.
5. Soft Bake, 95°C, 3 minutes.

C **Exposure**

1. Use exposure time of 0.42 seconds on the stepper.
2. As of October 1998, **Total** focus of +18 is fairly consistently the result of latent image focus array test on stepper.
3. For latent image focus arrays, use ???? exposure.

D **Post Exposure Bake** bake at 105°C for 3 minutes.

E **Flood Expose** Expose the entire wafer for 30 seconds at 7.5mW/cm^2 on Karl Suss mask aligner. Make sure that i-line filter is not in use.

F **Development**

1. Mix AZ 400K : DI 1:5.5
2. Immerse wafer in developper for 55 seconds
3. Rinse in running DI water for 3 min.
4. Blow dry with N2
5. Inspect under microscope. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array.

G **Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency
3. Run for 15 seconds

H **Surface Preparation**

1. Mix HCl oxide etch. HCl:DI 1::10
2. Dip for 20 seconds.

3. Rinse in running DI for 3 min.
4. Blow dry with N_2

I **Metal Evaporation**

1. Mount wafer to rotating E-Beam sample holder. We have a special mounting disk for full wafers.
2. Adjust boom in its clamp to yield angle of $\approx 35°$ to horizontal, and verify that power supply connections rotate motor correctly.
3. Make sure the crystal monitor reads < 9; change if necessary.
4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:[thicknesses WRT tooling factor of 140]

Material	Thick.	Rate	Vernier
Ti	200	2-3	1.65
Au	9500	12	1.70
Ti	100	2-3	1.70

J **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

C.9 SiN Capacitors

SiN Deposition and Pattern Clean a witness wafer — e.g. quarter of GaAs monitor wafer — to track the nitride deposition rate.

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **PECVD SiN Deposition Split** the desired thickness of SiN into two deposition steps. Rinsing and squirting the wafer with ISO in between depositions is reputed to reduce the density of full thicknes pin-holes. Also, pin-holes in the second layer will hopefully not be correlated to those in the first layer.

1. Scrub the PECVD chamber with Iso wet wipes. This has in the past been done while the platten is at 250°C, wearing solvent gloves and not lingering.
2. Plasma cleaning. Run 60ClnSiN program.
3. Deposit first portion of SiN on wafer and witness.
4. Immerse wafer in ISO for one minute. Squirt with iso.
5. Blow dry with N_2.
6. Load wafer in PECVD again, and pump to low vacuum. Measure thickness of nitride film on witness wafer, and adjust second deposition length to achieve desired final thickness.
7. Deposit second portion of SiN.

C **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale while your head is under the hood.

1. Wafer on spinner chuck with vacuum, blow with N_2
2. Apply SPR 518 with syringe and filter to cover wafer
3. Spin at 4 kRPM for 30 sec.
4. Soft Bake, $90°C$, 60 sec. on hotplate

D **Exposure**

1. Use exposure time of 0.9" on the stepper.
2. For latent image focus arrays, use ???? exposure.

E **Post Exposure Bake** bake at 110°C for 60 seconds.

F **Development**

1. Immerse in MF701 developper (TMAH developper beaker) for 90 seconds.
2. Rinse in running DI water for 3 min.
3. Blow dry with N2
4. Inspect under microscope with yellow filter. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array.

G **Photoresist Descum**

1. Ash in PE-IIA
2. 300 mTorr O_2 100W, 20 seconds

H **Post Exposure Do Not Forget This Step** Flood expose 2 minutes under Karl Suss, 7.5mW/cm^2.

I **Hardbake** 20 minutes in 120°C oven in Petri dish without cover.

J **Pre-clean RIE 3**

1. Vent system. Scrub both electrodes and the glass cylinder with ISO wet wipes.
2. Clean chamber with 20 minute O_2 etch.
   (a) 20.0 sccm O_2
   (b) 50 mTorr chamber pressure
   (c) Set RF supply for constant voltage of 500V.
3. Etch the Nitride:
   (a) 5.0 sccm SF_6 3.0 sccm O_2 10.0 sccm Ar
   (b) Chamber pressure = 20 mTorr
   (c) Constant voltage of 250V.
   (d) Etch for 5 minutes.
4. Inspect under microscope. This etch also removes the Ti layer from the top of metal 1.

K **Strip Resist**

1. Immerse wafer in acetone in a liftoff beaker for 5 minutes.
2. Rinse with methanol and isopropanol wash bottles, collecting the solvents in large flat beaker.
3. Rinse in running DI for 3 minutes.
4. Blow dry with N_2 gun.
5. Ash in PE-IIA
6. 300 mTorr O_2 100W, 30 seconds

C.10 Metal 2

Thick 5214 Process

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M $\Omega\cdot$cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

1. Dehydration bake: 3 minutes on 120°C hotplate
2. Wafer on spinner chuck with vacuum, blow with N_2
3. Apply AZ 5214 with syringe and filter to cover wafer
4. Spin at 4 krpm for 30 sec.
5. Soft Bake, $95°C$, 3 minutes.

C **Exposure**

1. Use exposure time of 0.42 seconds on the stepper.
2. As of October 1998, **Total** focus of +18 is fairly consistently the result of latent image focus array test on stepper.
3. For latent image focus arrays, use ???? exposure.

D **Post Exposure Bake** bake at $105°C$ for 3 minutes.

E **Flood Expose** Expose the entire wafer for 30 seconds at 7.5mW/cm^2 on Karl Suss mask aligner. Make sure that i-line filter is not in use.

F **Development**

1. Mix AZ 400K : DI 1:5.5
2. Immerse wafer in developper for 55 seconds
3. Rinse in running DI water for 3 min.
4. Blow dry with N2
5. Inspect under microscope. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure array.

G **Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency
3. Run for 15 seconds

H **Surface Preparation**

1. Mix HCl oxide etch. HCl:DI 1::10
2. Dip for 20 seconds.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2

I **Metal Evaporation**

1. Mount wafer to rotating E-Beam sample holder. We have a special mounting disk for full wafers.
2. Adjust boom in its clamp to yield angle of $\approx 35°$ to horizontal, and verify that power supply connections rotate motor correctly.
3. Make sure the crystal monitor reads < 9; change if necessary.

4. Pump down to at least 1×10^{-6} Torr.
5. Deposit material:[thicknesses WRT tooling factor of 140]

Material	Thick.	Rate	Vernier
Ti	200	2-3	1.65
Au	9500	12	1.70
Ti	100	2-3	1.70

J **Liftoff**

1. Suspend in beaker of ACE. Squirt bottle spray may be used to peel off metal film.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
3. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.
4. Rinse in METH then ISO with squirt bottle.
5. Rinse in running DI water for 3 min.
6. Blow dry with N_2.

C.11 BCB planarization

Thin BCB Process

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Adhesion Promoter**

1. Dehydration bake: 3 minutes on 120°C hotplate
2. Chuck wafer on spinner with vacuum
3. Play over wafer with N_2 gun.
4. Apply adhesion promoter AP8000 to cover wafer.
5. Spin at 3krpm for 60 seconds
6. Wait for 1 minute
7. Play over wafer with N_2 gun.

C **BCB Application Safety Note:** The casting solvent for Cyclotene BCB is fairly noxious. More importantly, the photoresist casting solvents present at the spinner bench are very harmful. Never inhale with your head under the hood.
N.B. Syringes with black "rubber" plunger tips will contaminate BCB. The silicone lubricant used in such syringes destroys the resin.

1. Apply Cyclotene 3022-57 to cover wafer from **HSW syringe or eye dropper**. BCB reacts with the silicone lubricants in syringes with rubber plunger tips. Fill the syringe by dipping the tip into the small bottle of BCB, and pulling up on the plunger.
2. Spin at 3kRPM for 30 seconds. This gives a total cured film thickness of about $7.5\mu m$
3. line the bottom of Petri dish with aluminum foil to prevent the wafer from sticking to dish

D **Clean-up and or Rework** *Uncured* BCB is soluble in toluene

1. clean off tweezers, bench-top, spinner chuck etc. with toluene soaked swabs. Toluene is not good for chuck o-rings.
2. If necessary, remove BCB film from wafer in beaker of toluene.

E **Cure**
Warning BCB is prone to rapid oxidation in air at temperatures above $150°C$. It must be cured under N_2 ambient. Use only the Blue-M nitrogen purged oven (by the deep UV exposer).

1. load wafer, in Petri dish without cover, in the Blue M oven. Close door carefully.

2. Flow 100SCFH of N_2 (this will max the rotameter out).

3. Use program P2 in the oven controllers non-volatile memory.
   (a) 100° C for 30 min.
   (b) ramp at 4° C per min. to 210° C.
   (c) hold at 210° C for 20 min.
   (d) ramp at 2° C per min. to 250° C.
   (e) hold at 250° C for 60 min.
   (f) ramp at 2° C per min. to 210° C.
   (g) ramp at 4° C per min. to 80° C.
4. Remove from oven when temperature drops below 80°C.

F **Photoresist Application for Flakey Nickel Mask Process**

1. Wafer on spinner chuck with vacuum. Blow with N_2.
2. Apply 5214 EIR resist with syringe and filter to cover wafer.
3. Spin at 6kRPM for 30 seconds.
4. Hot plate bake at $95°C$ 60 seconds.

G **Photoresist Application for Nickel-less Process**

1. Chuck wafer on spinner. Blow with N_2.
2. Draw SJR 5740 into syringe with polyethylene needle from small bottle.
3. Dispense resist to cover wafer.
4. Spin at 5.5kRPM for 30 seconds. Faster acceleration seems to be better than slow.
5. Hot plate bake at 100°C for 5 minutes.

H **Expose SJR 5740 resist**

1. Use Dark Field BCB etch reticle.
2. Exposure: 1.95 seconds
3. Total focus of -20.
4. Develop 10 minutes in MF 453.
5. Hard bake 30 minutes in 120°C oven.

I **Etch BCB**

1. Scrub the glass cylinder, top and bottom electrodes with iso wet wipes. If the top electrode is flaking, scrub it with an iso wet Scotch-brite pad.
2. Preclean etch chamber 20 sccm O_2, 50 mTorr chamber pressure self bias of 500V for 30 minutes.
3. Etch the BCB.
   (a) Pump down to mid 10^{-6} Torr range.
   (b) Turn on the etch cooling water chiller, and open up the etch cooling valve to let water circulate under cathode.
   (c) 6.0 sccm SF_6 10.0 sccm O_2.
   (d) Chamber pressure = 50 mTorr
   (e) Constant self-bias voltage of 350V.
   (f) Etch for 18 minutes then inspect under microscope. With longer exposure, Au surfaces get visibly rougher. Gold on top of transistor mesas will obviously be exposed before interconnect on field between mesas.
   (g) Clean etch chamber again, then finish up with at least a 30 second BCB etch before loading sample in sputter system.

C.12 Copper Plating

Copper Plating Process

A **Solvent Cleaning**

Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.

Check the resistivity of the DI water. It should be > 17 M $\Omega\cdot$cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Preheat Plating Solutions**

1. Preheat Technic Technigold 25E solution in beaker on hotplate at $75°C$ and stirring at 200RPM. Allow a minimum of one hour for the solution temperature to equilibrate.
2. Preheat Technic Nickel S Sulfamate solution on hotplate at $65°C$ and stirring at 200RPM. The boric acid buffer in this solution sometimes precipitates out at the bottom of bottle at room temperature. If it has done so, you will need to preheat the Nickel solution in its bottle until everything is dissolved.

C **Loading Plating Fixture**

1. Cleanliness is essential. Get a fresh pair of latex “solvent” gloves and wear them to handle anything that will be immersed in the plating solutions. Don’t touch the faucets, your nose, the stepper stages or anything else that is dirty with them.
2. Loosen off the finger clip bolts. Use the titanium hex key from the Cu plating box, and don’t loose it.
3. Seat the inner o-ring in the ring part of fixture. It often helps to stretch this like a rubber band before attempting to seat it.
4. Place your wafer in the recess of the fixture, and swing the finger clips into place. Tighten the bolts with the Ti hex key.
5. Push a couple of the opaque white Teflon hex head bolts through the sealing ring, then lower it into place over your wafer. Start all eight bolts. Tighten the bolt circle uniformly. Once the first bolt comes into contact with the sealing ring, work your way around the bolt circle, tightening each bolt by not more than 1/4 turn at a time before proceeding to the next bolt.

D **Assemble Electrodes, Lid**

E **Plate Inital Au Layer** 8mA for 60 minutes.

F **Plate Ni Diffusion barrier Safety Note: Under No circumstances should either the Nickel Sulfamate solution or the Copper Sulfate solution be taken to the Cyanide bench.** Coldren’s students (among others?) still stock and use cyanide compounds at that bench. Cyanide compounds react with acids to liberate lethal Hydrogen Cyanide gas. Even if taking acids to the cyanide bench doesn’t kill anyone, it should get you expelled from the cleanroom.

Plate Ni 40mA 20 minutes on hotplate at $65°C$.

G **Strip Nickel Oxides Explanation:** Ni surfaces oxidize very readily. If the Ni surface has been allowed to dry in air, then it can be assumed to have oxidized, and this extra oxide strip step should be followed. N.B. that Ni passivates especially quickly in alkaline solutions such as our Na Au Sulfite plating solution.

1. Prepare 3.5N H_2SO_4 solution. To 9 parts DI, add 1 part H_2SO_4.
2. Allow to cool. Give the sulfuric acid solution at least 30 minutes to cool down after mixing.
3. Transfer dilute acid to Nalgene bottle and cap it. Carry it back to the back developper bench
4. Prepare three large beakers to accept assembled plating fixture: one filled with the sulfuric acid solution, and two with DI.
5. Immerse assembled plating fixture (with wafer!) in H_2SO_4 solution for 20 seconds. Pull it out and immerse in first rinse beaker quickly. Agitate it for several seconds, then immerse in second rinse beaker.

H **Mix Cu Solution**

1. To 800mL of $CuSO_4$ solution from Enthone, add 45 mL of H_2SO_4.
2. Add DI water to bring total to 1L

I **Plate Cu**

1. Carefully drop magnetic stirrer bar into a clean empty 2L beaker.
2. Pour $CuSO_4$ solution into the beaker.
3. Immerse fixturing, and place the beaker atop a stirrer.
4. Stirring at $\approx$ 200RPM room temperature.
5. 80 mA for 3 hours 20 minutes for $\approx 30\mu m$ of Cu.

J **Plate Ni** 40 mA 25 minutes $65°C$

K **Unload Wafer** Once again, cleanliness is important. Wear clean latex gloves, and don't touch plating fixturing with them after having touched your nose, the faucets, or anything else in the clean room that you didn't just personally clean. The edge of the metal plated on the wafer often gets caught on the o-ring. Remove the bolt ring carefully, as the wafer may be stuck to the o-ring, and you could be pulling the wafer up away from the spring finger contacts.

C.13 Wax Mounting

Wax Mounting

A **Solvent Cleaning**
Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.
Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Preheat the Alignment Jig**

1. Clean any visible wax off the stainless steel jig with toluene soaked wipes.
2. Place the clean jig on a programmable hot-plate at $90°C$

C **Spin Coat Wax**

1. Chuck wafer on spinner with vacuum, blow with N_2
2. Apply wax solution to cover wafer with syringe and $1.0\mu m$ "prefilter".
3. Spin at 3 krpm for 30 sec.
4. Repeat with Si carrier wafer

D **Bake out casting solvent**
Bake each wafer for minimum 3 minutes at $90°C$ on hotplate.

E **Pre-mounting**

1. Place the silicon wafer, wax up, on the preheated jig, and press its flat against the two pins.
2. Carefully lower your HBT wafer, wax side down into place atop the carrier wafer. Try to line the flats of the two wafers up against the pins.

F **Vacuum Bonding**

G **Demounting**

1. Black wax is soluble in toluene, mesitylene, tetrachloro-ethylene, methylene chloride, TCA, TCE, and the terpene solvent with the trade name Opticlear. This last is far and away the least hazardous. Don't be alarmed by the pungent citrus odour that it emits.
2. If soaking alone is used, expect it to take a period of days for the solvent to reach to the center of the wafer.
3. Heating organic solvents always entails some hazzards. Tetrachloro-ethylene (a.k.a. "perchloro-ethylene") has the distinct advantage of not being flammable, against which it attacks the liver and nervous system. Most "solvent" gloves are **not** recommended for use with tetrachloro-ethylene.

C.14 Substrate removal

Substrate removal etch liberates poisonous phosphine gas. Leave appropriate warning notes on the bench.

A **Mix Etchant**

1. Use HCl InP etch beaker and stirrer bar, HCl and DI cylinders.
2. To 1 part DI water, add 3 parts HCl. Mix well.

B **Etching Explanation** 3:1 HCl : H_2O hydrolizes InP extremely fast. While it will etch {100} planes at $\approx 7\mu m/min$, it will barely etch {111}In planes at all. If anything initially present on the InP surface patterns the etch, you could be left with permanent ridges which are virtually impossible to remove by wet etching.

1. Place the bonded/transferred piece in a basket with the back of the InP wafer facing up.
2. **Hydrolysis of InP generates bubbles of Phosphine,** PH_3, **which is extremely toxic. Leave a clear note on the bench warning others that the bubbles are highly toxic.** A quick check with hydride sensing tape from the MOCVD lab demonstrates that phosphine is produced.

3. Check for {111} ridges. It may be a good idea to remove the sample from etch after 20 minutes, rinse in DI for 3 minutes, and inspect either visually or under optical microscope. The InP surface left by the HCl etch is usually quite rough, and appears faceted under the microscope. {111} ridges are, however recognizable by their sheer size and height (you might go cross-eyed at the stereo microscope).
4. Remedying {111} ridges: if they are caught early, then ridges might be eliminated by scratching with scriber tool to reveal non {111} planes, and returning to etch. This is not very hopeful though, and it may be better to 1) write the sample, or that part of it with ridges, off or 2) learn about mechanical lapping, and lap down to a planar InP surface.
5. Remix etch. The HCl etch should, in any event, be remixed after 30 minutes of etching time. The etch rate slows down drastically as HCl evaporates and is consumed. Total etch time to remove InP substrate is $\approx$ 40–70 minutes.
6. Stop after InGaAs etch stop plane has been reached. Small streams of bubbles at this point may indicate that a crystal defect has allowed the etch to reach underlying InAlAs.

C.15 Collector

SPR 950 CEM Process

A **Solvent Clean**

Do not use regular imersion solvent clean for wax mounted wafers. Instead, clean wafer on the spinner chuck.

1. **Warning** For full wafers, you must install one of the flat surface chucks. These are the chucks with the bare stainless steel surface marked by a spiral groove and intersecting radial grooves. The 2" o-ring chucks apply significant bending forces to the wafer — enough to break III-V wafers. Use our private chuck, or soak the public chuck in Shipley "1165" to remove any PMGI residue left by other users.
2. Apply vacuum to hold wafer sandwich to wafer chuck
3. Prepare yourself with a wash bottle of acetone and a wash bottle of isopropanol.
4. Set the spinner speed and time for the following application step.

5. start the spinner, and irrigate the spinning wafer with acetone, then iso, acetone again, and a final iso rinse, not letting the wafer dry in between solvents. No dehydration bake is required.

B **Photoresist Application** Safety Note: The vapors from photoresist are extremely harmful. Never inhale with your head under the hood.

1. Dehydration bake: 3 minutes on 120°C hotplate
2. Wafer on spinner chuck with vacuum, blow with N_2
3. Apply SPR 950-0.8 with syringe and filter to cover wafer
4. Spin at 6.0 krpm for 30 sec.
5. Soft Bake, 90° C, 60 sec. on hotplate
6. Wafer on spinner chuck with vacuum, blow with N_2
7. Apply ACEM 3651s with syringe and filter to cover wafer
8. Spin at 6kRPM for 30". **Do Not Bake.**

C **Exposure**

1. Measure the post transfer cell size. In global alignment mode, step across central row, noting offset required to align each cell **under the right microscope objective.** Stepping along an entire column of a 2" wafer will exceed the allowable stage travel; this should be avoided.
2. Edit job file to reflect indicated cell size.
3. Use exposure time of 1.66" on the stepper.
4. Focus: **total** focus of 44 has worked for many months. Focus array on Michelle's 2.25 inch Si wafer can also be used. In the latter case, use a total focus of Si focus − system focus +40. The free 2.25 inch Si wafers are somewhat suspect though, in that these wafers are near the minimum allowable thickness for the stepper.

D **Post Exposure Bake** bake at $100°C$ for 2 min. 10 sec.

E **Development**

1. Immerse in DI in Develop DI rinse beaker for 30 sec.
2. Immerse in MF701 developer (TMAH developer beaker) for 2 min 20 sec.
3. Rinse in running DI water for 3 min.

4. Blow dry with N2
5. Inspect under microscope with yellow filter. If some photoresist remains develop in steps of 5 sec. Might be time to do an exposure/ focus array.

F **Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency
3. Run for 15 seconds

G **Surface Preparation**

1. Mix HF oxide etch. To 200ml of DI add 10ml HF.
2. Dip for 30 seconds.
3. Rinse in running DI for 3 min.
4. Blow dry with N_2

H **Metal Evaporation**

1. Mount wafer to E-Beam sample holder, being careful that the sample hangs with its surface perpendicular to the evaporator source.
2. Make sure the crystal monitor reads < 9; change if necessary.
3. Pump down to at least 1×10^{-6} Torr.
4. Deposit material:

Material	Thick	Rate	Vernier
Ti	200	2-3	1.65
Pt	425	1.5	1.90
Au	4000	$\sim$15	1.55

I **Liftoff**

1. Use dedicated glassware for liftoff on wax-mounted wafers.
2. Suspend wafer in beaker of ACE. Wash bottle spray may be used to peel off metal film.
3. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil. DO NOT LET ACE DRY ON WAFER.
4. Only as a last resort: Beaker of ACE in ultrasonic. Ultrasonic will weaken your wafer and it might not survive further process steps.

5. Rinse in METH then ISO with wash bottles.
6. Rinse in running DI water for 3 min.
7. Blow dry with N_2.

C.16 Patterned Plating

SJR5740 Process

Explanation: Dispensing and spinning the resist in air saturated with the resist casting solvent changes the spinning process, because the resist is not drying as it spins. This should eliminate any problems associated with the crests of spreading waves drying, and it also reduces the edge bead. Against this, using a watch glass to cover the spinner will often lead to particles dropping on the wafer.

A **Solvent Cleaning**

Cleanliness Caution: Virtually everything in the clean room is dirty. Change your gloves before getting near your wafer.

Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.

Check the resistivity of the DI water. It should be > 17 M Ω·cm.

1. Cold ACE 3 min.
2. Hot MET 3 min.
3. Hot ISO 3 min.
4. Running DI 2 min.
5. Blow dry with N_2

B **Prepare the spinner**

1. Set the spinner acceleration to $\approx$ 5kRPM/sec with the trim-pot on the box under the bench.
2. Set the deceleration around middle of range.
3. Set the spinner to 900RPM, 10 seconds (not including deceleration time)
4. Clean the large watch glass.

5. Install the appropriate wafer chuck. Do not use any chuck with top surface o-rings for 2" wafers. You must use the cross-and-spiral grooved flat surface chucks for 2" wafers. The public flat surface chucks are often covered in resist and PMGI, and need to be soaked in NMP (Shipley 1165 stripper) at room temperature before use.

C **Dispense photoresist**

1. draw ≈ 5 mL of resist into a syringe with polyethylene "needle" tip.
2. Dispense 1 – 2 mL of resist into the bottom of the spinner bowl. Cover the bowl with the watch glass. Because the exhaust lines of the spinners are not connected to any ventilation system, this will suffice to saturate the air under the watch glass with casting solvent.
3. Lift watch glass up only long enough to place wafer on the spinner chuck. Recover with watch glass.
4. Blow wafer with N_2 gun. Recover.
5. Lift watch glass, and quickly dispense resist to cover the wafer. Again, recover the spinner bowl.
6. Start the spin cycle. Start a stop watch at this time.

D **Wait and Bake**

1. One minute after beginning the spin, remove the watch glass. Excessive time under solvent saturated ambient, on spinners which tend not to be level, leads to the resist flowing too much.
2. Wait a further five minutes before placing wafer on the hotplate. This "resting" period is to allow much of the casting solvent to evaporate gradually and avoid blistering problems in the hot-plate bake. Resting on the bench may be preferable to resting on the chuck, depending on which is more level.
3. Bake 12 minutes on 105°C hotplate.
4. Wait for a minimum of 15 minutes before exposing the wafer. Photoresist must be allowed to reabsorb water from the air between softbake and exposure.

E **Expose**

1. 16 seconds exposure, focus offset ≈ -10.
2. Fill two beakers with MF453 developer. Develop for a total of 30 minutes, changing wafer from one beaker to the second, fresh beaker after 15 minutes.

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