University of California
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Ultra-Broadband, Efficient, Microwave Power Amplifiers in Gallium Nitride HEMT Technology

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philosophy
in
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by
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June, 2000

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Abstract

Ultra-Broadband, Efficient, Microwave Power Amplifiers
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Karthikeyan Krishnamurthy

Wide bandwidth power amplifiers are key components in phased-array radars and instrumentation. Obtaining a combination of high power, decade (10:1) bandwidth and high power-added-efficiency (PAE) requires both advanced semiconductor devices and improved microwave circuit design techniques. AlGaN / GaN HEMTs have high $f_\tau V_{br}$ products, and can provide high output power at microwave frequencies. Efficient broadband circuits that operate over high percentage of transistor's f_τ are required. Simple lumped broad-band amplifiers have gain-bandwidth products limited by the transistor current-gain cut-off frequency, f_τ. Distributed amplifiers are limited by the power-gain cut-off frequency, f_{max}, but have poor efficiency due to the drain-line reverse wave.

To obtain efficient wideband amplification over bandwidths of ~40% of the transistor's f_τ, two competing topologies have been developed. The cascode-delay-matched traveling wave amplifier is a distributed amplifier topology capable of obtaining gain-bandwidths limited by f_{max}, with efficiencies up to the class-A theoretical limit of 50%. The f_τ-doubler feedback power amplifier is a lumped amplifier topology which in addition to obtaining similar bandwidths and efficiencies, has a much lower output reflection coefficient, and uses a smaller die area. To further improve bandwidth and efficiency high f_τ - high V_{br} cascode cells (or dual gate devices) and broadband class-AB push-pull stages are proposed which could be incorporated into either circuits.

Scale-models were fabricated in a GaAs MESFET technology to verify the circuit concepts. f_τ-doubler feedback power amplifiers using AlGaN / GaN HEMTs achieved ~10 dB gain, 1 - 8.0 GHz bandwidth amplifiers with ~5.12 W output power and up to 23% PAE. GaAs MESFET - GaN HEMT cascode-delay-matched distributed power amplifiers achieved 1 - 10 GHz bandwidth with 10 dB small signal gain and $>$ 1 W output power. With device scaling and improved thermal performance these circuits are capable of providing 10's of Watts over 2 - 20 GHz with up to 40% PAE.

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Chapter 1

Introduction

THIS work describes the design and fabrication of ultra-broadband, efficient high power microwave amplifiers in AlGaN / GaN HEMT technology.

1.1 Objective

The Office of Naval Research (ONR) requires ultra-broadband, efficient, linear solid-state high power microwave amplifiers to replace the currently employed traveling-wave tubes in Naval radar systems. Output powers on the order of 10's of Watts over a 2-20 GHz bandwidth is required with power-added-efficiencies (PAE) of 40% or higher, low noise figure $\leq$ 3 dB and high linearity with >28 dB suppression of spurious output.

Obtaining a combination of high power and decade (10:1) bandwidth requires both advanced semiconductor devices and improved microwave circuit design techniques. Since reactively-matched microwave power amplifier topologies do not obtain high gain and high efficiencies over multi-octave bandwidths, new power amplifier topologies are required to obtain high efficiency and frequency-independent high gain over broad bandwidths. Since low loss impedance transformation over a broad 10:1 bandwidth are hard to realize for large transformation ratios, the power amplifier must drive loads of 25-50Ω nominal impedance. Without broadband transformers, GaAs / InP based transistors in standard broadband power amplifier circuits can hardly provide 1 W over a decade bandwidth due to their limited breakdown voltage (V_{br} ~20 V). High device breakdown voltages are consequently re-

quired for obtaining high output power. Thus wideband power amplifiers demand wide-bandwidth (high f_τ), high-power (high V_{br})transistors. The combination of high power and high bandwidth is best addressed with wide-bandgap semiconductor materials like Gallium Nitride (GaN) [1, 2]. In this work amplifiers were implemented using AlGaN / GaN power HEMTs. AlGaN / GaN HEMTs have high $f_\tau V_{br}$ product, and can provide high powers at these frequencies.

As it is fundamentally difficult for high breakdown microwave power transistors to obtain high unity current-gain cutoff frequency (f_τ), the circuit topologies employed must provide high amplifier performance over a high percentage of the transistor's bandwidth. As standard broadband power amplifier topologies obtain bandwidths of only ~20% of f_τ alternative efficient broadband power amplifier topologies are needed.

1.2 In this work

To obtain efficient wideband amplification over bandwidths of ~40% of the transistor's f_τ, two competing topologies have been developed.

The cascode-delay-matched traveling wave amplifier is a distributed amplifier topology capable of obtaining bandwidths limited by the transistor power gain cut-off frequency, f_{max}. The drain-line in a traditional traveling wave amplifier (TWA) is eliminated, and efficiencies up to the class-A theoretical limit of 50% is achieved by suppressing the reverse-wave. The delay matching is done between the common-source (CS) and common-gate devices (CG) of a cascode cell. Unlike the tapered drain-line distributed amplifier this topology does not require high impedance lines and so is physically realizable for higher powers.

The f_τ-doubler feedback power amplifier is a lumped amplifier topology which in addition to obtaining similar bandwidths and efficiencies, has a much lower output reflection coefficient, and uses a smaller die area.

To further improve bandwidth, *slow-fast* cascode cells are proposed which could be incorporated into either of the proposed circuits. This configuration uses a *fast* transistor (having a high f_τ and consequentially low device V_{br}) for the CS device, and a *slow* transistor (having a high device V_{br} and consequentially low f_τ) for the CG device, in a cascode cell. This could be realized in a monolithic form using dual-gate devices having small and large gate lengths for the first and second gates respectively or in a

hybrid multi-chip module (MCM) form using two different device technologies (eg. InP PHEMT for the common-source device and GaN HEMT for the common-gate devices). Since the bandwidth is limited primarily by the CS device and the output power by the CG device the overall power and bandwidth are improved.

To further improve the efficiency, two kinds of broadband class-AB push-pull stages have been analyzed. A modified Marchand balun architecture, employing even mode termination for a true class-AB operation of the device, is capable of providing efficiencies up to the theoretical class-B limit of 78.5% and a 5:1 bandwidth.

While final power amplifier designs have used GaN HEMT devices, the GaN technology was relatively immature to allow circuit fabrication in the early phase of this research. So the first-generation of microwave power amplifiers were fabricated in GaAs MESFET technology to verify the circuit concepts. Scale-model Microwave Monolithic Integrated Circuits (MMICs) of the f_τ-doubler feedback power amplifier were implemented in a commercial GaAs MESFET process. A bandwidth of 0.2 - 6 GHz with 12 dB gain, over 23 dBm output power, and more than 25 % PAE was obtained in a GaAs MESFET technology offering 18 GHz f_τ and 12 V breakdown. These circuits have a bandwidth of 33% of f_τ and a gain-bandwidth product of $\sim 1.3{\cdot}f_\tau$, with efficiencies more than what traditional distributed power amplifiers have achieved.

Two generations of f_τ-doubler feedback power amplifier were designed, fabricated and tested in AlGaN / GaN HEMT technology. The first generation of circuits yielded ~11 dB gain, 0.2 - 7.5 GHz bandwidth amplifiers with ~1.5 W output power (limited by the large DC - RF dispersion) and up to 15% PAE. The second generation of circuits achieved ~10 dB gain, 1 - 8.0 GHz bandwidth amplifiers with ~5.1 W output power and up to 23% PAE.

Scale-model hybrids of the cascode-delay-matched TWAs were implemented using commercially available packaged GaAs MESFETs. Bandwidth up to 25% of f_τ with ~15 dB gain and 30±5 % power-added-efficiency was achieved. Hybrid MCM were fabricated in GaAs / GaN technology using GaAs MESFETs for the CS device and AlGaN / GaN HEMTs for the CG device in the cascode cell. These circuits achieved 1 - 10 GHz bandwidth with 11 dB small signal gain and >1 W output power. These were the first circuits to incorporate GaAs and GaN devices into a single hybrid

and represent the largest gain-bandwidth obtained using GaN HEMTs.

1.3 Motivation

High power broadband amplifiers are one of the key components in phased-array radar applications [3]. Present day U.S. Navy ships and aircraft have numerous antennas and receivers, each operating at different frequency bands, performing unique functions in the radar, electronic warfare (EW), and communication bands. The Office of Naval Research (ONR) formed the Advanced Multifunction RF Systems (AMRFS) program whose goal is to integrate these individual RF systems into a single multifunction, programmable system (fig. 1.1).

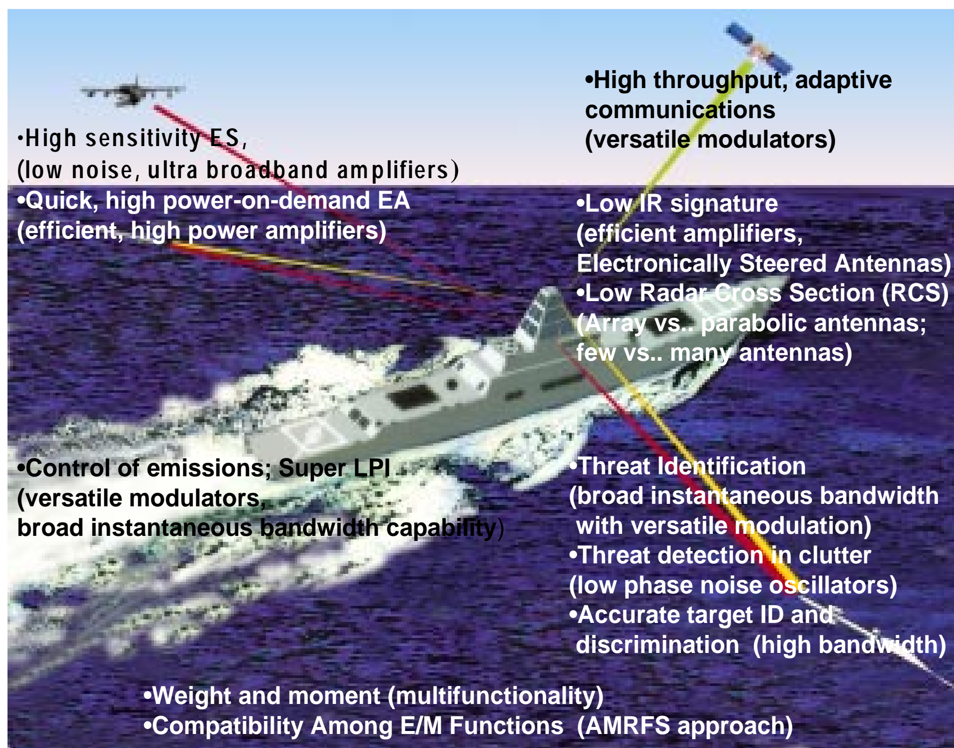

Figure 1.1: Multitude of RF functions expected from AMRFS approach.

The key requirements for the AMRF system are summarized below:

- A single ultra broadband system that could cover electronic warfare (EW), communications and electronic surveillance frequency bands. High bandwidth is also required for accurate target identification and discrimination.

- Ultra low phase noise system for increased threat detection in clutter environment and high sensitivity electronic surveillance.

- Efficient high power amplifiers that can provide quick, high power-on-demand electronic attack.

- Low radar cross section (RCS) that will leave reduced signature (chance of being detected) and hence improved survivability.

- Efficient amplifiers and electronically steered antennas for low IR signature.

- Multifunctional systems for reduced weight and volume saving critical real-estate on ships and aircrafts.

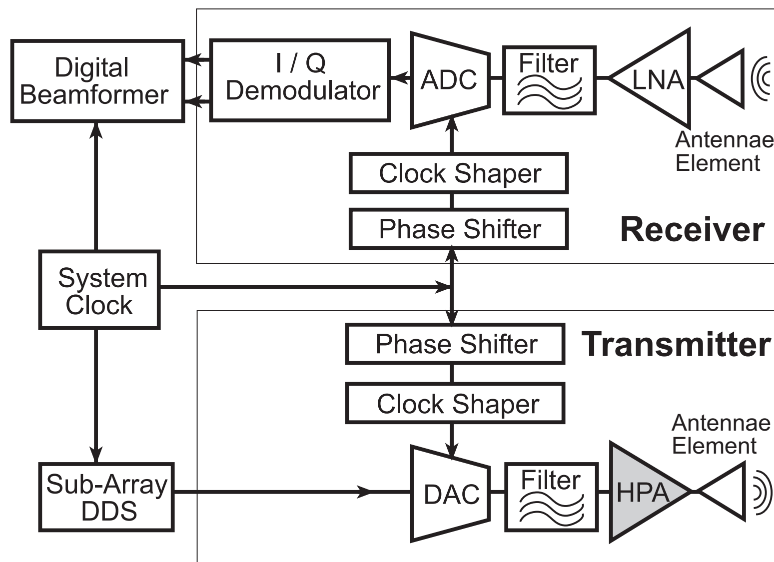

Figure 1.2: Block diagram of a multifunction RF system.

Fig. 1.2 shows the block diagram of the components in a digital phased array radar in a multifunction system. Performance requirements for the various elements are listed below :

1. Antennae element (array architecture requirements) : Broadband, low-profile, efficient, dual-polarized radiating elements are required for low-signature phased array antennas suitable for the 1 - 25 GHz band. Wideband separate transmit and receive phased array architectures to provide multiple simultaneous receive and transmit beams. Full phase and amplitude control at each element, radiating assembly, and array level to accommodate various true time delay concepts. High polarization integrity for any polarization at all scan angles is also required.

2. Filters (transmit/receive isolation requirements) : Broadband, tunable, precision, low-loss bandpass filters; channelized filters; and notch filters that provide high transmit-to-receive isolation are required. Filters with improved cutoff properties are needed to reduce out-of-band noise. To be able to transmit and receive simultaneously requires that the transmit signal level is +65 dBm and the receive sensitivity is -130 dBm, resulting 195 dB isolation between transmit and receive.

3. Solid State Modules and Components : High power, linear, wideband amplifiers; low noise amplifiers; phase shifter, attenuator, switch, amplifier networks for separate transmit and receive modules are required. These modules must exhibit a wide bandwidth ($\sim$10 - 20 GHz), high power ($\geq$ 10W at X-band), low noise figure ($\leq$ 3 dB), and high linearity ($\sim$28 dB below rated power). Since the size, output power and efficiency of these modules are highly dependent on the characteristics of the high power amplifier, a PAE of at least 40% is desired.

4. Direct Digital Synthesis (DDS) : DDS will be used for the implementation of true time delay beam forming, and complex signal generation with arbitrary waveform generators. DDS and arbitrary waveform generators may be used for synthesizing radar and communications waveforms. The minimum acceptable digital to analog converter (DAC) performance is 12 bits of -60 dBc spur free dynamic range with 1 GHz of bandwidth.

5. Analog to Digital (A/D) Converters (ADC): ADCs are used to digitize the received waveforms for further processing. The goal of the ADC is to ultimately produce digital receivers with reduced size and weight. For EW applications, 12 bits of spur-free dynamic range with 400 - 500 MHz of bandwidth is required. For radar and communications, at least 20 bits of spur-free dynamic range with 20 MHz of bandwidth is required.

6. Digital beamformer (true time delay) : True time delay beamsteering provides wideband simultaneous operation of multiple signals in a phased-array AMRFS antenna. A combination of time delay and phaseshifting could also be used. The beamformer should be capable of providing time delay at a subarray level such that instantaneous bandwidths of 1.5 GHz is supported across the full operating frequency band. Finally, the overall system throughput delay needs to be kept small.

As is apparent, to achieve the goals of the AMRFS program, a multitude of critical enabling technologies have to be developed. Various components of the AMRFS system are in development at UCSB and in numerous universities and research labs in the U.S. This work deals only with the solid-state power amplifier circuits and modules required for the AMRFS. This thesis presents an overview of the key issues in designing a broadband solid-state module, the status of the technologies required, the first demonstration of the circuits proposed, and estimates its potential in the near future.

Though most of this work on decade bandwidth high power amplifiers is intended only for military applications, some of the circuit concepts developed are applicable to amplifiers with few octave bandwidths that have a potential for use in commercial wireless and instrumentation applications [4]. In fact in the last year, resistive feedback Darlington power amplifiers similar to once described in chapter 5 are commercially available [5], and are intended for use as drivers for optical fiber networks and CATV amplifiers.

1.4 Thesis organization

Chapter 2 reviews the basics of power amplifier design and presents the additional limitations especially in designing broadband power amplifiers.

These limitations are on the choice of load-line, class of operation, gain - bandwidth product, power - frequency product, and choice of device technology. Chapter 3 deals with the basic circuit topologies used in RF / microwave power amplifiers and the limitations of these circuits in terms of the bandwidth, and efficiency they can obtain. Chapter 4 presents an overview of the processing steps involved in fabrication of GaN HEMTs and AlN substrates and in the assembly of the power amplifiers. D.C. and RF test device results from the various GaN HEMT circuit process runs are also discussed. Detailed process flows are presented in Appendix A, B and C.

Theory of operation of f_τ-multiplier power amplifiers is presented in Chapter 5 along with design, simulation and measurement results from GaAs MESFET and GaN HEMT f_τ-doubler power amplifiers. Chapter 6 talks about the design of cascode-delay-matched distributed amplifiers and presents measured results from GaAs MESFET and GaN HEMT power amplifiers. Chapter 7 discusses techniques for achieving further improvements in bandwidth, output power and efficiency. The output capacitance has a fundamental limitation on the efficiency bandwidth in broadband power amplifiers. The cause of this limitations is analyzed along with solutions that include minimizing the output capacitance and using optimal output networks to absorb the capacitance over broad bandwidth. Additional improvement in power bandwidth using small - large gate length dual-gate cascodes and high f_τ - high V_{br} common source - common gate cascode pairs are discussed. Broadband push-pull class-AB designs that could further improve the efficiency are analyzed. Chapter 8 concludes the thesis, listing the achievements and suggestions for future work.

Chapter 2

Limitations on wide bandwidth power amplifier designs

HIGH power solid state microwave amplifiers usually operate over ∼10% or lesser bandwidth. As the output power is increased the amplifier bandwidth decreases for a given device technology. The requirement of both high power and a decade bandwidth requires that fundamental limitations associated with both the circuit architectures and device technology be addressed. This chapter addresses these basic limitations in designing efficient broadband high power amplifiers.

2.1 Definition of broadband power amplifier

Before we look at the practical limitations on broadband power amplifiers, we would define the term explicitly to include a class of amplifiers for which these limitations hold. Power amplifiers could be classified into two broad categories namely, broadband and narrowband power amplifiers depending on the bandwidth over which they can provide constant output power. The distinction between the two has become increasingly unclear with the development of highly tuned narrowband amplifiers, which have a bandwidth of less than 1% around the center frequency (for example 400 MHz bandwidth around 40 GHz). This had lead to claims of power amplifiers with ∼ 10% bandwidth as relatively broadband power amplifiers. Since in this work we are looking at power amplifiers with a bandwidth of a decade or more, we shall use the term *broadband amplifiers* to refer to amplifiers

having at least a bandwidth of two octaves (4:1 or 120%), but more in the range of a decade (10:1 or 164%) or so. Having made this distinction we could highlight the circuit and device limitations associated with designing such broadband power amplifiers.

2.2 Limitations on the class of operation

We will first look at the classes of operation that are best suited for use in broadband power amplifiers. Transistor power amplifiers could be divided into a number of classes determined by one or more of the following criterion [6]:

1. where the device is biased
2. what load-line the device sees
3. whether the active device is operated as a amplifier or a switch

Though the number of classes in existence [7] is far too many to be described here in detail, we will see that most of the classes other than class-A, and push-pull configurations of class-AB/B are unsuitable for use in broadband power amplifiers.

2.2.1 Class-A

Fig. 2.1 shows the circuit schematic of a simple class-A power amplifier. For narrowband applications, a tuning network might be added at the output to terminate the harmonics created due to the variation in device transconductance. In this class of power amplifiers the device is biased normally-on, at about half the peak-peak output current and half the peak-peak output voltage (fig. 2.2).

The load-line in class-A operation is linear at low frequencies and primarily determined by the load resistance (R_L). To obtain the maximum power from the device, the load-line is chosen so that the device operates between the maximum allowed drain to source voltage (the breakdown voltage, V_{br}) at one extreme and the maximum allowed drain current (the saturation current, I_{DSS}) at the other extreme [8]. This requires that the

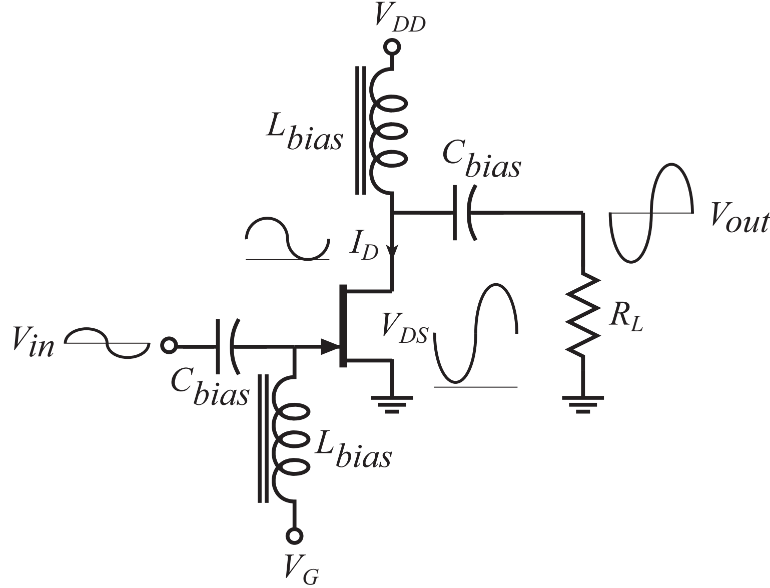

Figure 2.1: Circuit schematic of a simple class-A power amplifier.

optimum load resistance $R_{L,opt}$ be,

$$R_{L,opt} = \frac{(V_{br} - V_k)}{I_{DSS}} \ . \tag{2.1}$$

This ensures that device provides the maximum output power obtainable, given by

$$P_{out,max} \leq \frac{(V_{br} - V_k)I_{DSS}}{8} \equiv \frac{(V_{br} - V_k)^2}{8R_{L,opt}} \ . \tag{2.2}$$

Choosing this load-line minimizes the total device periphery (and hence the die area) required for a given RF output power. As will be seen in chapter 3 this also provides the best bandwidth. Larger device periphery results in larger device input and output capacitances which degrade the bandwidth. Oversizing is done if the device on-resistance in the linear region (R_{on}) is large (i.e. V_k/V_{br} is large). Then by operating at $I_{d,max} < I_{DSS}$, the $I_d^2 R_{on}$ losses are reduced and the efficiency is improved. However this is achieved at the cost of reduced bandwidth.

The maximum output power obtainable is roughly half the DC power, which means that the theoretical maximum drain efficiency (ratio of the

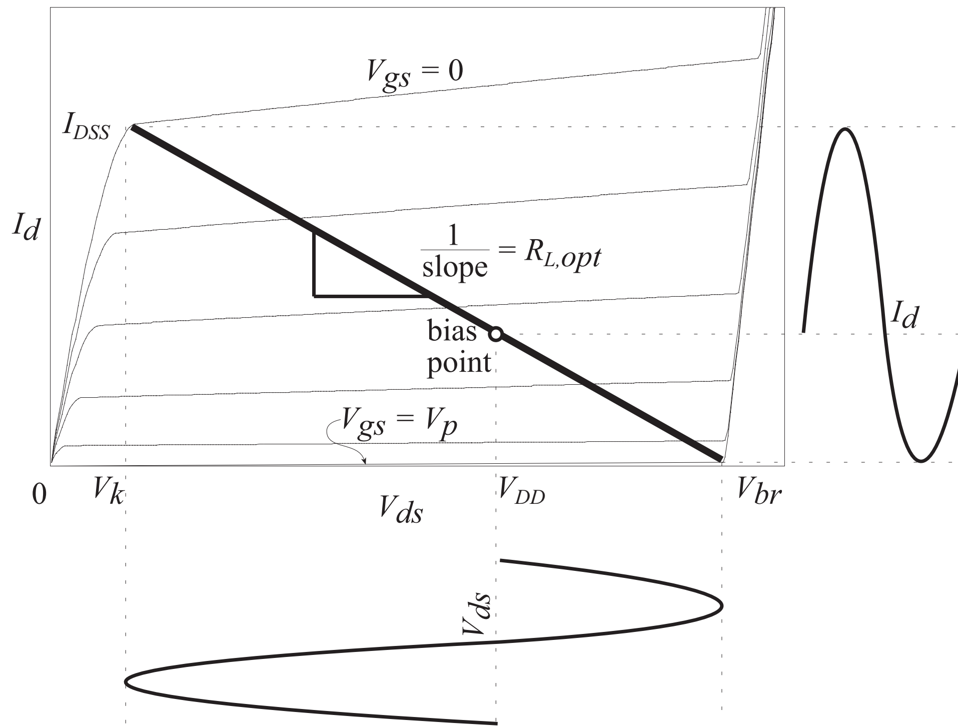

Figure 2.2: Optimum load-line for class-A operation.

output RF power to the DC power) is 50%. Since the device is normally on, a constant DC power of nearly twice the peak RF output power is dissipated at all times. This might degrade the performance of high power amplifiers with time. But the advantages of class-A operation include broadband operation and high linearity.

2.2.2 Tuned Class-AB/B

In class-AB (class-B) amplifiers the device is biased close to pinch-off (at pinch-off) so that the device operates as a amplifier for half the cycle and remains cut-off for the other half of the cycle [8]. In tuned class-AB/B amplifiers sinusoidal output swings are obtained using a resonator at the output (fig. 2.3) tuned to the fundamental frequency. The drain voltage and current waveforms are sinusoidal and half-sinusoidal respectively and the drain is biased at roughly half the peak-peak RF output voltage swing

(fig. 2.4). It is apparent that for the same device periphery as the class-A case the optimum load is now a factor of 2 lesser, but the net fundamental output power is the same. Since the device is off when the voltage across it is high, lower D.C. consumption and hence higher efficiency up to 78.6% is expected. However, this configuration is inherently narrowband because the series (parallel) resonator that is designed to be a short (open) at a fundamental frequency acts close to a open (short) at the second harmonic, and so even bandwidths of 2:1 are hard to realize.

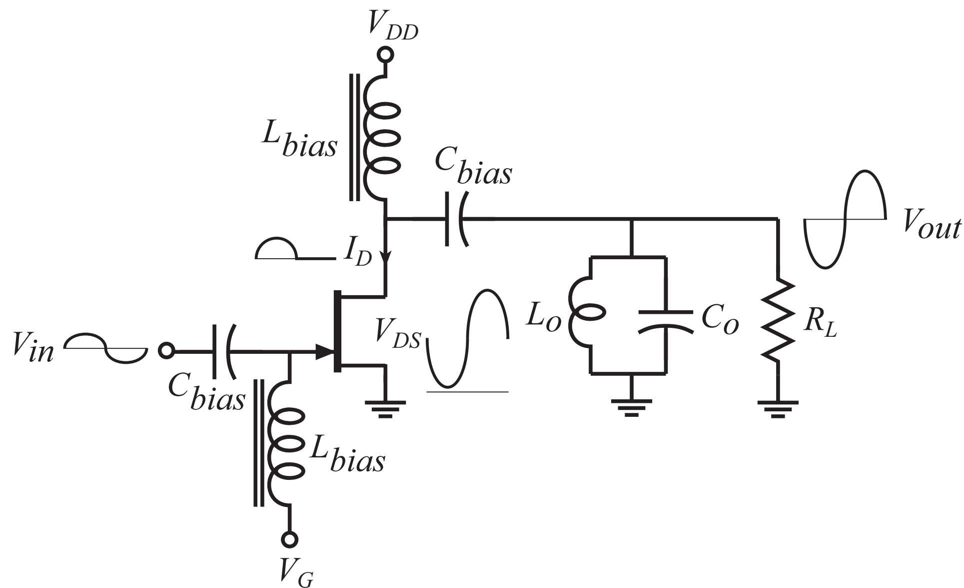

Figure 2.3: Circuit schematic of a simple class-B tuned power amplifier.

2.2.3 Push-pull Class-AB/B

In push-pull class-AB/B configuration sinusoidal output swings are obtained using two devices, each operating for half the cycle and combining the output currents. This configuration could be made relatively broadband but requires broadband transformers or complementary devices. Since complementary devices and magnetic materials are unavailable at microwave frequencies, 180° hybrid couplers (baluns) have to be used instead of transformers. As in the class-A case a filter could be used at the output to

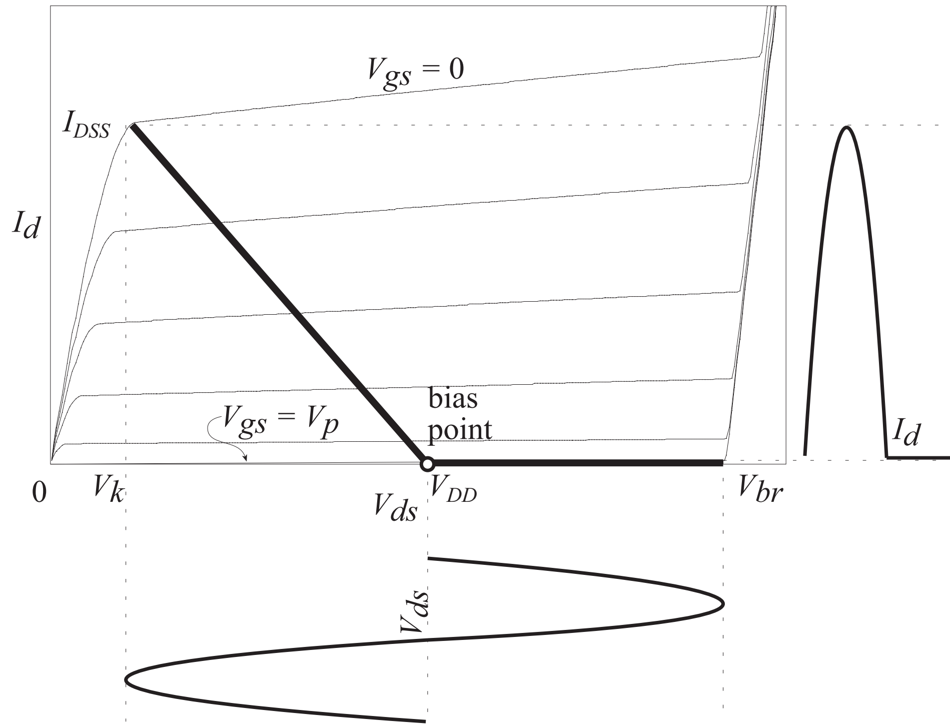

Figure 2.4: Device bias point and load-line for class-B operation.

terminate the harmonics in narrowband applications. In push-pull power amplifiers the two devices have half the periphery as class-A case with the optimum load $R_{L,opt}$ chosen to provide a half sinusoidal peak current swing of $I_{DSS}/2$ and a sinusoidal peak-peak voltage swing of $(V_{br} - V_k)$ for each device (fig. 2.5). Since the peak-peak current swing is I_{DSS}, the value of $R_{L,opt}$ and the peak output power are same as in the class-A case.

Broadband class-B push-pull amplifiers using transformers (fig. 2.6) require proper connection of the transformers to provide class-B waveforms. At the input the two primary and secondary windings are connected in series (*series - series transformer*) to create equal amplitude 180° out of phase voltages for the two devices. At microwave frequencies this could be realized using 180°-hybrids or baluns.

Such a balun (or a *series - series transformer*) provides a high impedance (open) termination for even mode signals and is not suitable for the output. At the output we have 180° out of phase sinusoidal voltage waveforms from

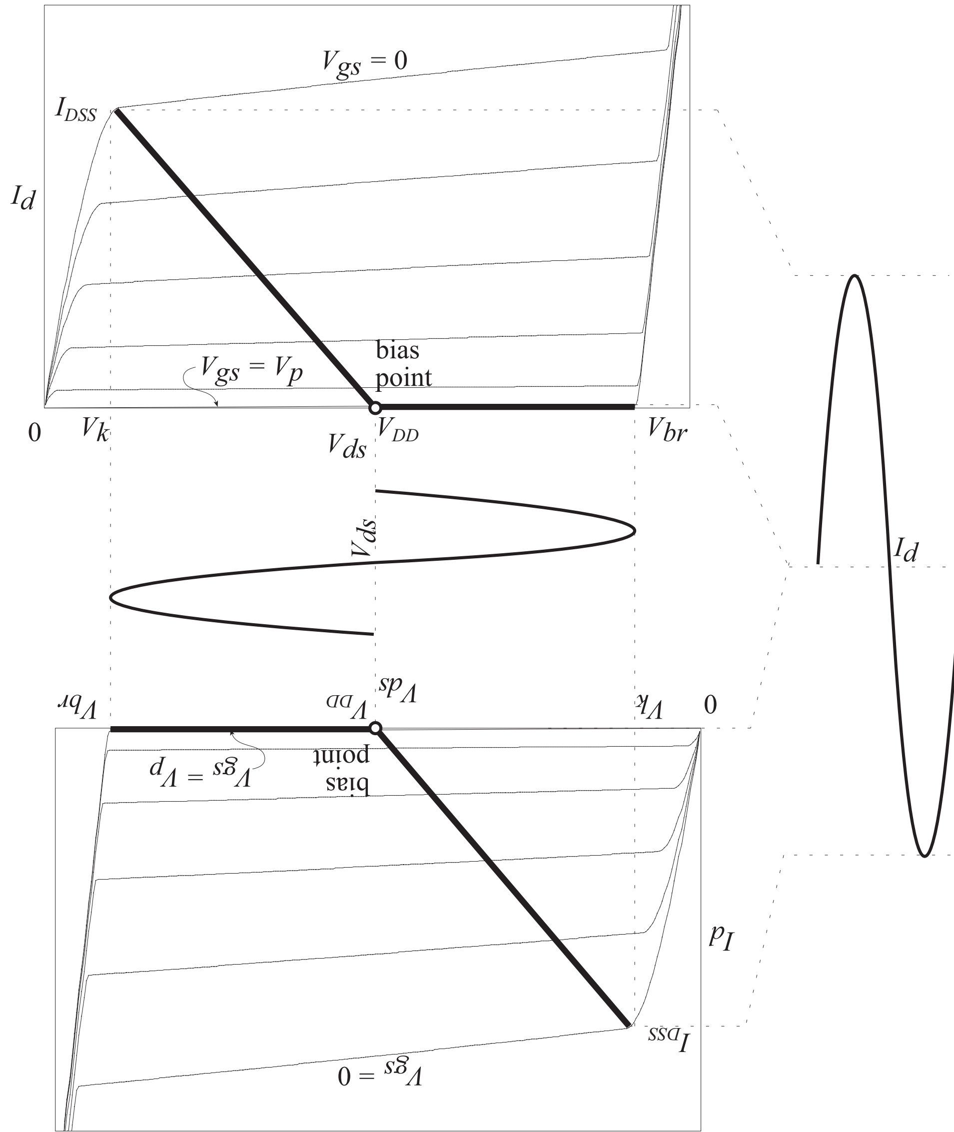

Figure 2.5: Optimum load-line for push-pull class-B operation.

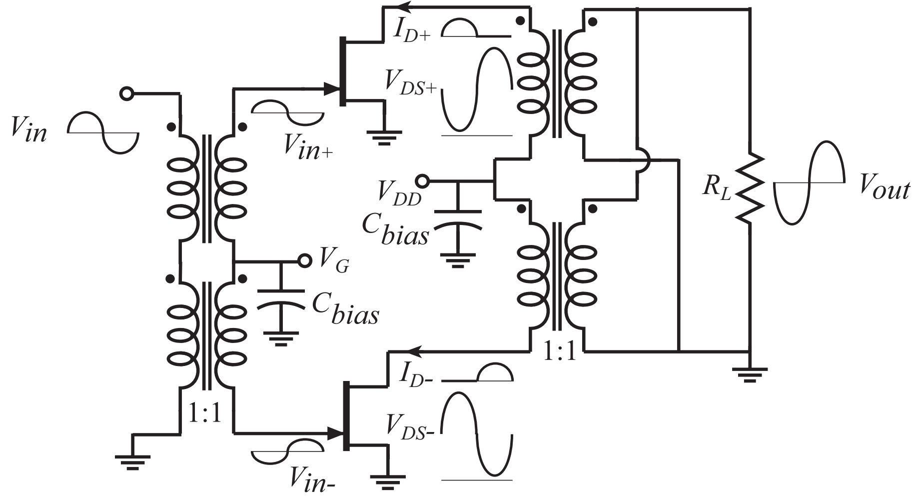

Figure 2.6: Circuit schematic of a class-B push-pull power amplifier using transformers.

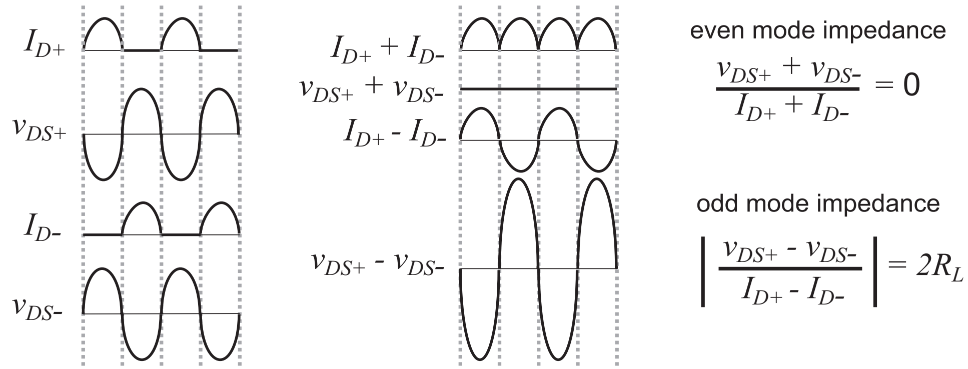

Figure 2.7: Even and odd mode impedances required for class-B push-pull operation.

the two devices, but the current waveforms have to be out of phase half sinusoids for a true class-AB/B operation. This requires a 0 Ω impedance (short) termination for the even mode (symmetric) drain current (fig. 2.7). This is achieved using transformers by connecting the primary windings in series and the secondary windings in shunt (*series - shunt transformer*) (fig. 2.6). However, there is no equivalent balun at microwave frequencies for such a transformer connection.

A *series - shunt transformer* could be realized using a *series - series transformer* with a separate even mode termination which shorts the symmetric drain currents (fig. 2.8). The load impedance is now four times larger in the absence of 2:1 transformers at the output. Using this equivalence a microwave class-B balun could be realized using a 180°-hybrid along with a even mode termination. However for broadband operation we require that both the balun and the even mode termination be broadband. Chapter 7 discusses ways of implementing them for two octaves of bandwidth.

As in the tuned class-B case, higher efficiency up to 78.6% is obtained due to reduced D.C. consumption. Thus, using the same total device periphery and the same load, considerably higher efficiency is obtained in class-AB,B push-pull power amplifiers than in class-A power amplifiers. However the bandwidth may be limited by the transformer performance. The peak output power obtainable from class-AB / class-B stage is similar to the class-A case but with a higher drain efficiency. Also due to the negligible or zero dissipation with no input drive, the thermal performance of the device is usually better than in the class-A case.

2.2.4 Other classes

Class-C amplifiers are similar to the class-B tuned power amplifier with the device biased deep into cut-off region, so that the conduction angle for a sinusoidal waveform is less than 180°. Higher efficiencies are obtained by lowering the conduction angle, up to a theoretical limit of 100% with 0° conduction angle. Class-D,E are switched mode power amplifiers, where the device is operated as a switch. The load networks are chosen to minimize the current and voltage waveform overlap across the device, resulting in higher efficiency. But, again as in the case of class-B tuned power amplifiers, these classes as well as other classes like F, G, H etc. use a resonator at the output to obtain the fundamental power and are of no significance in broadband

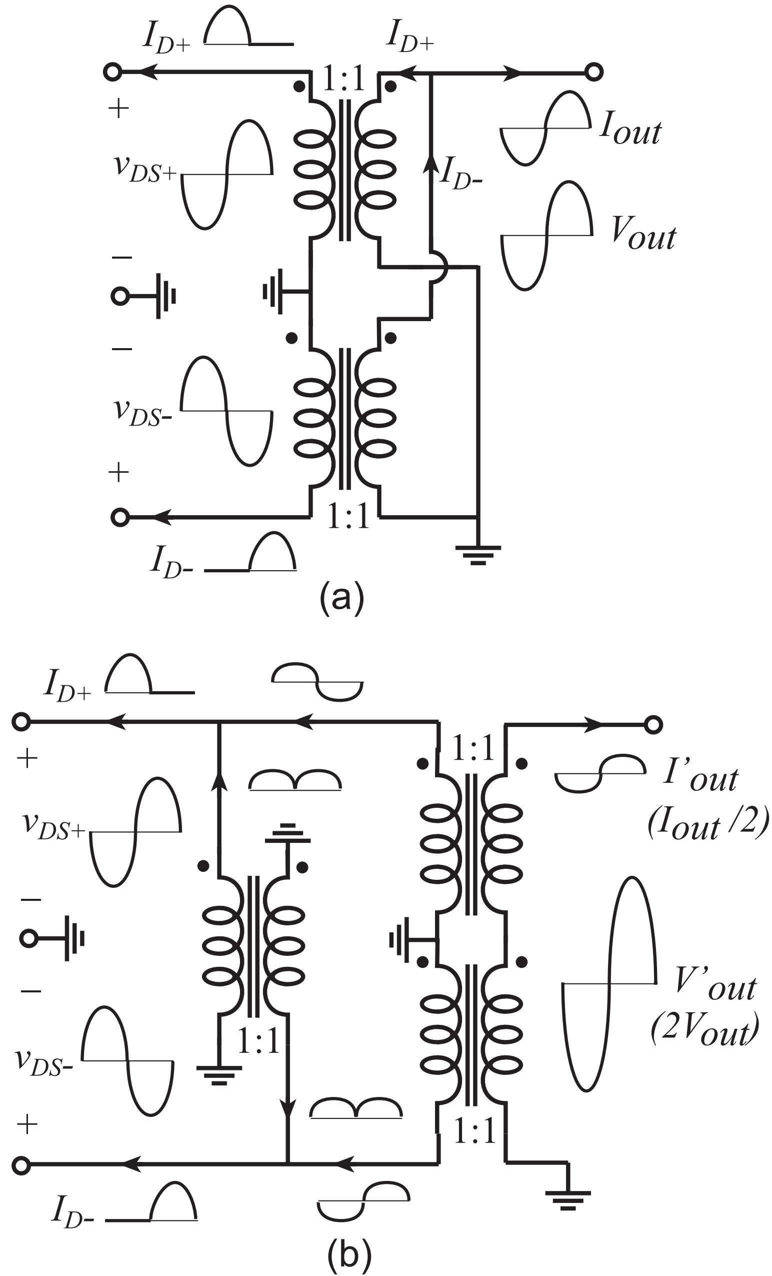

Figure 2.8: Transformer configuration for true class-B push-pull operation: (a) series - shunt connection and (b) series - series connection with even mode termination.

amplifiers.

With these limitation only class-A and push-pull class-AB,B are suited for broadband operation. This sets a theoretical limit of 78.6% on the drain efficiency one can achieve over broad bandwidths. However most decade bandwidth amplifiers in literature operate in class-A mode and have typically 15% efficiency, the reasons for which will be explained in chapter 3. In most of this work we have limited ourselves to class-A power amplifiers, though a few push-pull class-AB designs were analyzed and are discussed in chapter 7.

2.3 Limitation on load impedance

The second limitation, called the load impedance limit, limits the range of load resistance that can be used in broadband amplifiers. As we had seen earlier in this chapter the maximum output power (eq. 2.2) varies roughly as the square of the breakdown voltage ($(V_{br} - V_k)^2 \sim V_{br}^2$) and inversely as the optimum load resistance, $R_{L,opt}$. Thus for obtaining higher power we require higher breakdown voltage and lower load impedance. Limitations on the breakdown voltage will be discussed in the next section. But for a given device technology and hence a given V_{br}, higher power could be obtained by using smaller $R_{L,opt}$. This could be done by scaling the total device periphery and hence the net I_{DSS} (eq. 2.1). But, this implies that we need a impedance transformation network at the output to transform $Z_o = 50\Omega$, the nominal system / antennae impedance to $R_{L,opt}$. This is where broad bandwidth imposes a restriction on the smallest $R_{L,opt}$ one can use, and hence the largest power one can obtain.

In narrowband microwave power amplifiers, there is a minimum feasible load resistance (typically 5Ω) set by realizability and loss issues in transmission-line impedance transformation networks. In broadband microwave power amplifiers, the limit is more severe. Impedance-transformation networks effective over a 2-20 GHz bandwidth are not compatible with monolithic fabrication. To be feasible at all, such broadband transformers must be fabricated off-wafer. Even then, such off-wafer broadband impedance-transformation networks will be very large, as it will involve multiple sections of quarter-wave lines at the center frequency. Such long lines are invariably lossy. It should be noted here that a 3 dB loss in a 2:1 impedance transformation network means that any power gained due to the

smaller $R_{L,opt}$ is lost in the output network and hence there is no significant improvement in the net output power while the efficiency is a factor of 2 lesser.

Classically, broadband load tuning in RF power amplifiers is performed by ferrite-loaded transformers, but these are not presently available at the frequencies of interest. Hence, the amplifier must have typically a $R_{L,opt} = Z_o = 50\Omega$ load impedance for a decade bandwidth and could be transformed down to 25Ω for two octaves of bandwidth with acceptable losses in impedance transformation. The maximum output power is then given by,

$$P_{out,max} \leq \frac{(V_{br} - V_k)^2}{8Z_o} \ , \tag{2.3}$$

and the net device periphery (W) is chosen to provide a total saturated drain current (I_{DSS}) decided by,

$$I_{DSS} = \frac{(V_{br} - V_k)}{Z_o} \ . \tag{2.4}$$

The table 2.1 gives the typical broadband power one could expect from various device technologies and the device periphery needed, based on the above limitations.

Table 2.1: Typical power obtainable from various device technologies driving a $Z_o = 50\Omega$ load.

device technology	typical V_{br} (V)	typical V_k (V)	typical I_{DSS} (mA/mm)	device periphery (mm)	typical $P_{out,max}$ (W)
* GaAs MESFET [9]	12	1	300	0.75	0.3
§InP PHEMT [10]	12	1	500	0.45	0.3
†GaN HEMT	50	5	500	1.8	5.0
‡GaN HEMT	200	5	1000	4.0	100

* Triquint, § HRL, † UCSB current, ‡ UCSB projected

2.4 Power-frequency limit

The third limitation called the power-frequency (pf^2) limit relates to the inherent limit on the breakdown voltage a high frequency device technology can achieve. This limits the output power one can obtain from a given device technology especially over broad bandwidths. The pf^2 limit, well-known in microwave power transistor design, imposes particularly severe performance limits on broadband microwave power amplifiers.

In high frequency transistors, whether HEMT or HBT, there is a high-field drift region separating the control region (the HEMT channel, the HBT base) from the output terminal. In HEMTs it is the extension of the gate depletion region laterally towards the drain contact, while in a HBT this drift region is the collector depletion layer. If the length of this region is D_{drift}, and the semiconductor breakdown electric field is E_{max}, then the transistor breakdown voltage is,

$$V_{br} = E_{max} D_{drift} \ . \tag{2.5}$$

This drift layer introduces space-charge transit time. If the electron velocity is v_{sat}, then the space charge transit time ($\tau_{transit}$) is

$$\tau_{transit} = \frac{D_{drift}}{2 v_{sat}} \ , \tag{2.6}$$

and (ignoring all other transit delays) the unity current-gain cutoff frequency is

$$f_\tau \leq \frac{v_{sat}}{\pi D_{drift}} \ . \tag{2.7}$$

Combining eq. 2.5 and 2.7, we get

$$f_\tau V_{br} \leq \frac{E_{max} v_{sat}}{\pi} \ , \tag{2.8}$$

which is purely dependent on the material parameters. So, the transistor f_τ and V_{br} have to be traded against each other, with extended drift regions giving high breakdown voltages but low f_τ and thin drift regions giving low breakdown voltages but high f_τ [11]. A tradeoff between breakdown voltage and current-gain cutoff frequency does not fundamentally mean that high-frequency devices must be low-power devices. As was mentioned in the last section high power could be obtained over narrow bandwidths at

high frequencies by transforming to low $R_{L,opt}$. But for a broadband power amplifier with $R_{L,opt} = Z_o$ we have from eq. 2.3 and 2.8,

$$P_{out} \approx \frac{V_{br}^2}{8Z_o} \leq \frac{(E_{max}v_{sat})^2}{8\pi^2 Z_o f_\tau^2} \ . \tag{2.9}$$

On rearranging the terms we get,

$$P_{out} f_\tau^2 \leq \frac{(E_{max}v_{sat})^2}{8\pi^2 Z_o} \ . \tag{2.10}$$

2.5 Limitation on bandwidth

The fourth limitation is a consequence of the pf^2 limit, the loadline limit and the limitations with the input tuning network. Since the current-gain cutoff frequency varies inversely with breakdown (eq. 2.8), a high-power broadband amplifier must use low-f_τ power transistors. Also large device peripheries are required, as determined by eq. 2.4, to match a $Z_o = 50\Omega$ loadline. Consequently, the transistor has a large input capacitance (C_{gs}), given by

$$C_{gs} = \frac{G_m}{2\pi f_\tau} \ , \tag{2.11}$$

where G_m is the device intrinsic large signal transconductance, given by

$$G_m = \frac{I_{DSS}}{V_p} \ . \tag{2.12}$$

Difficulties with the design of broadband input matching networks then limit the amplifier bandwidth. As the input capacitance is directly proportional to G_m one possible way of increasing bandwidth is to decrease the device extrinsic transconductance ($G_{m,ext}$) and hence the gain by using either capacitive or resistive degeneration. Though these two techniques offer one degree of freedom to trade-off gain for bandwidth, and is frequently used in broadband power amplifiers, it will be seen in chapter 3 that they do not provide any improvement in gain bandwidth product, which is still limited by f_τ.

2.6 Limitation on gain

The need for high gain in power amplifiers will become apparent once we understand the overall efficiency specifications of the amplifier. We will first define the efficiencies typically used for quantifying power amplifier performance :

1. *Drain efficiency* ($DE\%$) or D.C. to RF conversion efficiency is defined as the ratio of R.F. output power (P_{out}) to the D.C. power drawn from the drain supply ($P_{DC,D}$)expressed as a percentage ;

$$DE\% = \frac{P_{out}}{P_{DC,D}} \cdot 100\% \; . \tag{2.13}$$

   Drain efficiency represents what fraction of the D.C. power is converted into R.F. output power.

2. *Power Added Efficiency* ($PAE\%$) is defined as the ratio of the difference in the R.F. output to input power, to the total D.C. power drawn from all bias supplies (P_{DC}).

$$PAE\% = \frac{P_{out} - P_{in}}{P_{DC}} \cdot 100\% \equiv \frac{P_{out}}{P_{DC}} \left(1 - \frac{1}{G}\right) \cdot 100\% \; , \tag{2.14}$$

   where P_{in} is the RF input power, and G is the power gain. As PAE also accounts for the input R.F. drive power required for the amplifier it is representative of how the power amplifier output stage is going to impact the overall system efficiency.

In short, a low PAE due to a high input drive (low power gain) would imply, efficiency of the driver stage is also going to significantly affect the overall efficiency. So at least a power gain of 10 (10 dB) is required to obtain high PAE (say up to 45% for the class-A case). This ensures that the system efficiency is primarily determined by the efficiency of the output stage and the driver stages does not significantly affect the overall efficiency.

2.7 Implications on device technology and circuits

Having understood the limitations on decade bandwidth high power amplifiers, the following implications on the choice of circuits and device technol-

ogy are apparent :

1. circuits must operate in class-A mode.
2. push-pull class - AB/B operation is feasible in the presence of efficient broadband transformer or complementary devices.
3. designs must be for a $Z_o = 50\Omega$ load for a decade bandwidth and at least 25 Ω for a bandwidth of two octaves.
4. designs must be for at least 10 dB gain to ensure high PAE.
5. circuits must have bandwidths up to a high fraction of the device f_τ for high bandwidth.
6. circuits must use a device technology with high $f_\tau V_{br}$ product.

All these implications have been addressed in this work. Though all the circuit results are from class-A operation, the feasibility of implementing efficient broadband transformers (baluns) and quasi-complementary stages at microwave frequencies for efficient class-AB operation is addressed. Circuits that obtain bandwidth up to high fractions of f_τ have been developed and were designed for 10 dB gain while driving 25 or 50 Ω load. Circuits were fabricated in a high $f_\tau V_{br}$ GaN / AlGaN HEMT technology, and further improvements using high f_τ - high V_{br} *fast-slow* cascodes using two device technologies or using dual-gate devices with small and large gate lengths for the two gates are in progress.

Chapter 3

Wideband power amplifier basics

THIS chapter examines conventional microwave amplifier topologies in literature and evaluates their performance in terms of the bandwidth, output power and efficiencies they can achieve. This will provide sufficient motivation to explore alternate topologies to obtain high power over broad bandwidth with high power added efficiency. Since the circuit gain-bandwidth performance will be compared in terms of the device figures of merits, the current gain cut-off frequency f_τ and the power gain cut-off frequency f_{max}, these are defined here for reference. Also defined is the large signal power gain for a loadline match, which is more relevant to power amplifiers.

3.1 Transistor figures of merit

Using the simplified A.C. model (fig. 3.1(a)) for the transistor, short circuit current gain is defined as the current gain of the device when the output is short circuited and the input is driven using a current source (fig. 3.1(b)). Short circuit current gain is given by,

$$H_{21} = \frac{I_{out}}{I_{in}} = \frac{G_m}{j2\pi f C_{gs}} \equiv \frac{f_\tau}{jf} \ , \tag{3.1}$$

where

$$f_\tau = \frac{G_m}{2\pi C_{gs}} \ , \tag{3.2}$$

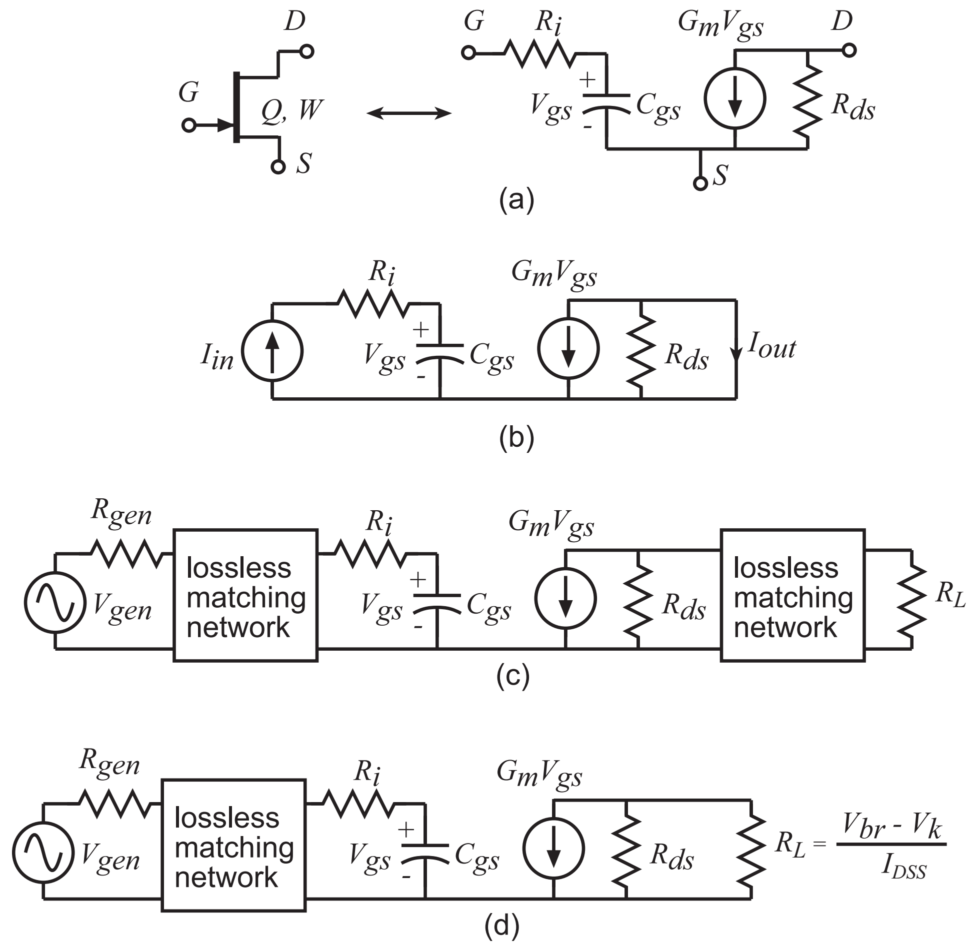

Figure 3.1: (a)Simplified A.C. π-model for the transistor used in this analysis, (b) definition of short circuit current gain and (c) definition of maximum available power gain (d) definition of large signal power gain for loadline match.

is the frequency at which the current gain becomes unity, also called the unity current gain cut-off frequency.

The transistor provides the maximum power gain when both the input and output are conjugate matched to the generator and load impedance respectively (fig. 3.1(c)). This maximum available power gain (MAG) is given by,

$$MAG = \frac{P_{load}}{P_{av,gen}} = \frac{G_m^2 R_{ds}}{16\pi^2 f^2 C_{gs}^2 R_i} \equiv \left(\frac{f_{\max}}{f}\right)^2 , \tag{3.3}$$

where

$$f_{\max} = \frac{f_\tau}{2\sqrt{R_i/R_{ds}}} , \tag{3.4}$$

is the frequency at which the power gain becomes unity, also called the power gain cut-off frequency.

In power amplifiers a loadline match is usually provided at the output (eq. 2.1) as in fig. 3.1(d), rather than a match for the maximum power gain as in fig. 3.1(c). The large signal power gain (LSG) is then given by (for the case $R_L \gg R_{ds}$),

$$LSG = \frac{P_{load}}{P_{av,gen}} = \left(\frac{V_{br} - V_k}{V_p}\right) \frac{G_m}{4\pi^2 f^2 C_{gs}^2 R_i} \equiv \left(\frac{f_{lsg}}{f}\right)^2 , \tag{3.5}$$

where

$$f_{lsg} = \sqrt{\frac{V_{br} - V_k}{I_{DSS}}} \frac{f_\tau}{\sqrt{R_i}} . \tag{3.6}$$

Here the large signal power gain cut-off frequency (f_{lsg}) is the frequency at which the power gain becomes unity for a loadline match.

With the transistor parameters scaling with the device periphery (W) as $I_{DSS} \propto W$, $C_{gs} \propto W$, $G_m \propto W$, $R_i \propto 1/W$ and $R_{ds} \propto 1/W$, f_τ, f_{max} and f_{lsg} are independent of the device periphery.

3.2 Common source amplifier

In an elementary common source power amplifier without input tuning (fig. 3.2(a)), the net device periphery W is chosen to provide a total saturated current I_{DSS}, determined by the loadline constraint (eq. 2.4).

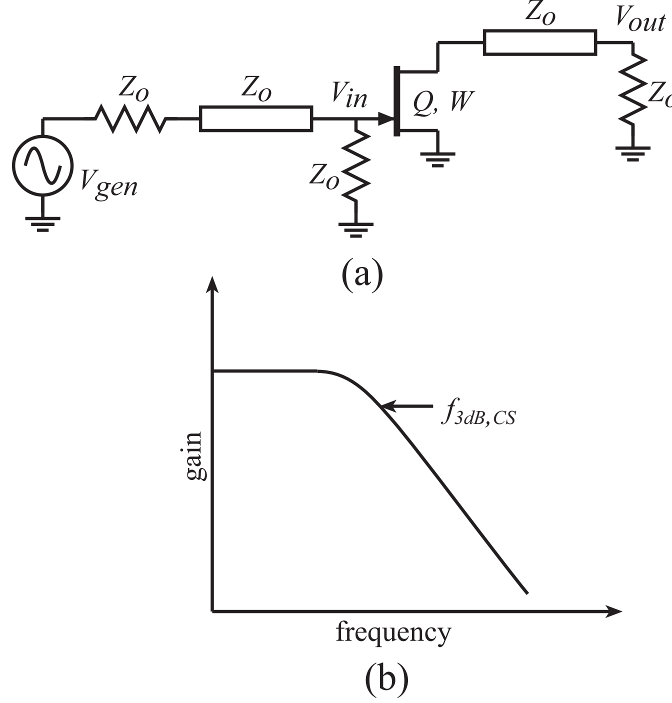

Figure 3.2: (a) A.C. circuit schematic and (b) typical frequency response of a common source amplifier without input tuning.

Assuming the simplified π-model (fig. 3.1) for the transistor the amplifier has a fixed mid-band voltage gain and transducer power gain of,

$$\begin{aligned} S_{21,CS} &= G_m Z_o \ , \\ G_{T,CS} &= \left(\frac{V_{br}-V_k}{V_p}\right)^2 \ , \end{aligned} \tag{3.7}$$

respectively, and an input capacitance (C_{gs}) limited bandwidth (fig. 3.2(b)) of

$$f_{3dB,CS} = \frac{1}{2\pi(Z_o/2+R_i)C_{gs}} \ . \tag{3.8}$$

This limits the gain-bandwidth product to,

$$S_{21,CS}f_{3dB,CS} = \frac{G_m Z_o}{\pi(Z_o+2R_i)C_{gs}} \simeq \frac{G_m}{\pi C_{gs}} \equiv 2f_\tau \ . \tag{3.9}$$

The gain-bandwidth product is greater than f_τ because of the loadline match done without the output termination. Adding an output termination of Z_o for a better output reflection coefficient will decrease the gain and efficiency by a factor of 2 and will limit the gain-bandwidth to f_τ. Though the gain-bandwidth is $2f_\tau$ in this case, any series cascade of stages will still have a gain-bandwidth limit of f_τ. As seen in fig. 3.3 this improvement in gain-bandwidth because of the mis-match between stages could be used only once in an amplifier cascade.

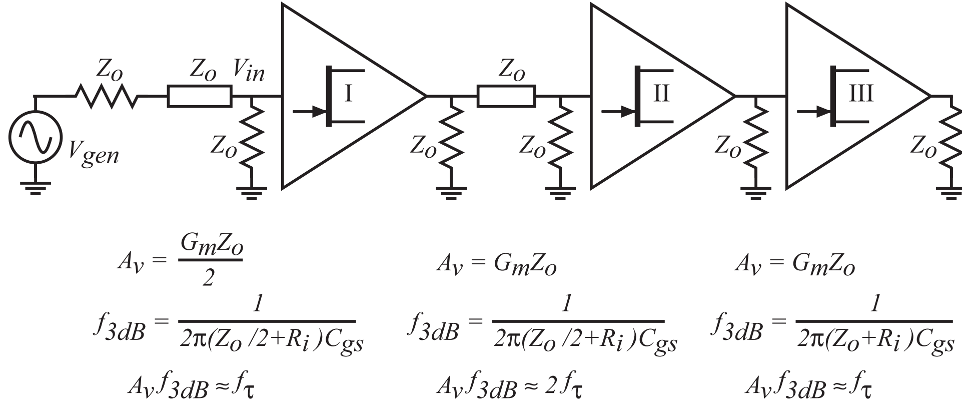

Figure 3.3: Gain-bandwidth product in a series cascade of stages with (I) both input and output matched, (II) only the input matched and (III) both input and output mismatched.

The 3 dB bandwidth (f_{3dB}) corresponds to a 50% drop in output power (25% class-A theoretical efficiency) and so over-estimates the usable range of operation in power amplifiers. A more appropriate figure of merit for power amplifiers would be the 1 dB bandwidth associated with 20% drop in output power (40% class-A efficiency). For the case of a single pole roll-off we have $f_{1dB} \sim f_{3dB}/2$.

The gain and bandwidth are individually constrained in a common source power amplifier as well as the rest of the amplifiers discussed below. So capacitive [12] or resistive degeneration is essential in all broadband power amplifiers to trade-off gain for bandwidth, while maintaining a constant gain-bandwidth product.

In the case of capacitive degeneration (fig. 3.4(a)) of value C_{div}, the extrinsic transconductance, net input capacitance, gate resistance, mid-

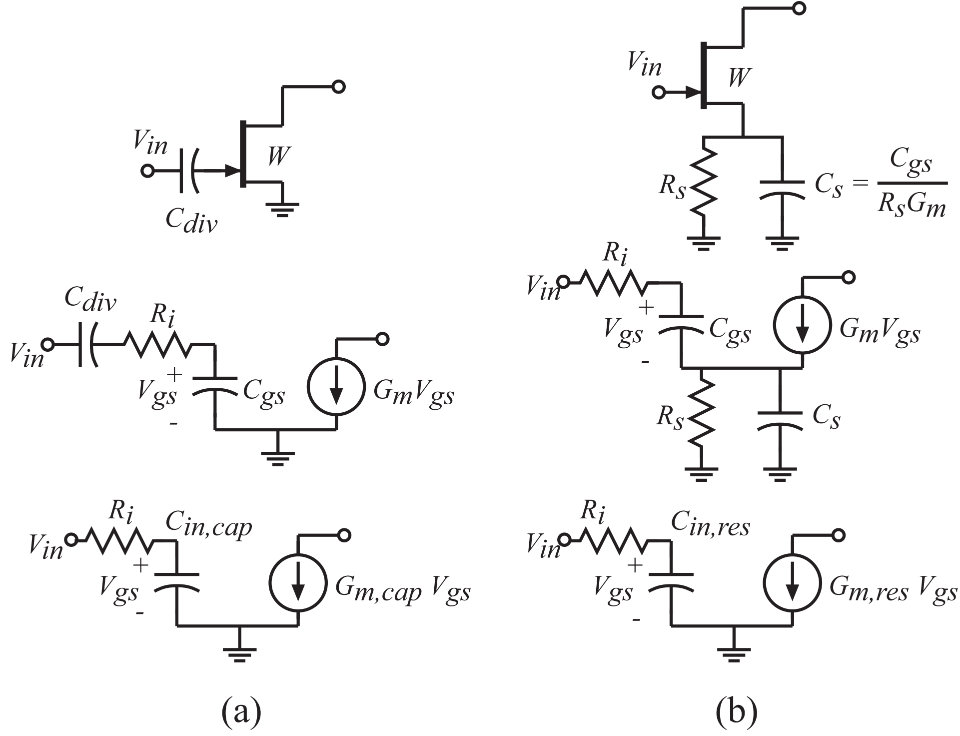

Figure 3.4: A.C. circuit schematic of (a) capacitive and (b) resistive degeneration.

band gain and the 3 dB bandwidth are respectively,

$$
\begin{aligned}
G_{m,cap} &= G_m \frac{C_{div}}{C_{div} + C_{gs}} \ , \\
C_{in,cap} &= \frac{C_{div} C_{gs}}{C_{div} + C_{gs}} \ , \\
R_{i,cap} &= R_i \ , \\
S_{21,cap} &= G_m Z_o \frac{C_{div}}{C_{div} + C_{gs}} \ , \\
f_{3dB,cap} &= \frac{1}{2\pi (Z_o/2 + R_i) C_{in,cap}} \ .
\end{aligned}
\tag{3.10}
$$

Capacitive degeneration introduces a lower cut-off frequency depending on the degeneration value and so cannot be used if operation up to D.C. is desired.

For the case of resistive degeneration (fig. 3.4(b)) of value R_s in shunt with $C_s = C_{gs}/G_m R_s$, the extrinsic transconductance, net input capacitance, gate resistance, mid-band gain and the 3 dB bandwidth are respectively,

$$\begin{aligned} G_{m,res} &= \frac{G_m}{1+G_m R_s} , \\ C_{in,res} &= \frac{C_{gs}}{1+G_m R_s} , \\ R_{i,res} &= R_i , \\ S_{21,res} &= G_m Z_o \frac{1}{1+G_m R_s} , \\ f_{3dB,res} &= \frac{1+G_m R_s}{2\pi(Z_o/2+R_i)C_{gs}} . \end{aligned} \tag{3.11}$$

Thus both configurations provide improved bandwidth at the cost of gain, and the gain-bandwidth product is still limited by $2f_\tau$ under the assumed model of fig. 3.1. As was mentioned in chapter 2 to obtain high PAE we need a power gain of at least 10 dB. This means that S_{21} should be at least 10 dB (> 3.2), which limits the 3 dB bandwidth to $\sim 2f_\tau/3$ and the 1 dB bandwidth to $\sim f_\tau/3$ for any of the above configurations. Once all transistor parasitics are modeled there is a further drop in bandwidth to below 25% of f_τ for a 10 dB gain. Combining eq. 2.10 and 3.9 we can rewrite the expression for the relationship between output power, gain and bandwidth as,

$$P_{out} f_{3dB}^2 \leq \frac{(E_{max} v_{sat})^2}{8\pi^2 S_{21}^2 Z_o} . \tag{3.12}$$

3.3 Reactively matched amplifier

A reactively-matched power amplifier (fig. 3.5) provides efficient coupling to the device over a narrow bandwidth. The inductor, $L = 1/(4\pi^2 f_o^2 C_{gs})$ resonates with C_{gs} at the design frequency f_o and the low-loss broadband impedance transformer provides an input match to Z_o. As in the earlier case, the device periphery is chosen to provide a loadline match at the output. The mid-band voltage gain and transducer power gain are then

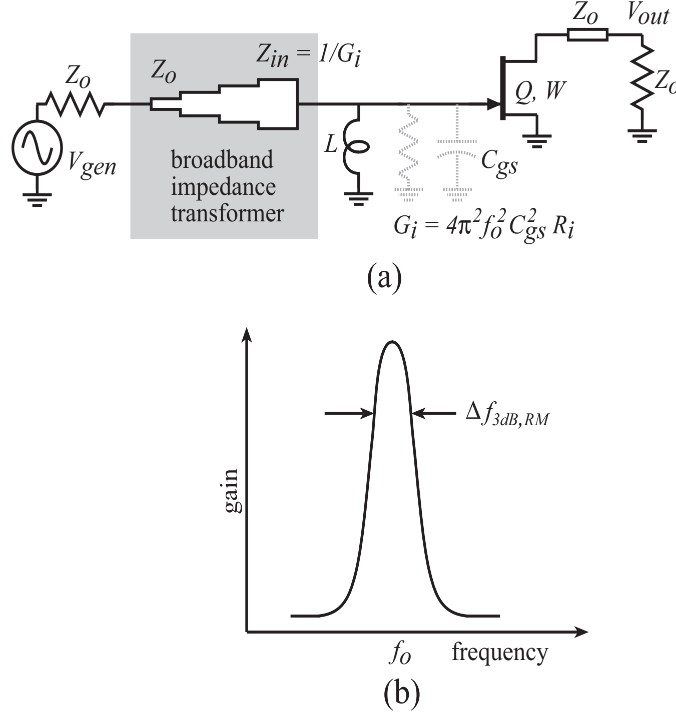

Figure 3.5: (a) A.C. circuit schematic and (b) typical frequency response of a reactively matched common source amplifier

given by,

$$
\begin{aligned}
S_{21,RM} &= \frac{G_m Z_o}{2\pi f_o C_{gs}\sqrt{R_i Z_o}} \; , \\
G_{T,RM} &= \frac{(V_{br} - V_k)\, I_{DSS}}{V_p^2} \frac{1}{4\pi^2 f_o^2 C_{gs}^2 R_i} \; ,
\end{aligned}
\tag{3.13}
$$

respectively, and the bandwidth that could be obtained for design frequencies $f_o \ll 1/(2\pi R_i C_{gs})$, is limited by,

$$
\begin{aligned}
Q \equiv \frac{f_o}{\Delta f_{3dB,RM}} &\equiv \frac{1}{2\pi f_o C R} = \frac{1}{4\pi f_o R_i C_{gs}} \; , \\
\Delta f_{3dB,RM} &= 4\pi f_o^2 R_i C_{gs} \; .
\end{aligned}
\tag{3.14}
$$

This is the Bode-Fano limit [13], which limits the bandwidth over which the input reflection coefficient (Γ_{in}) is small,

$$\int_0^{+\infty} \frac{1}{\omega^2} \ln\left(\frac{1}{\|\Gamma_{in}\|}\right) d\omega \le \pi R_i C_{gs} \ . \tag{3.15}$$

3.4 Lossy matched amplifier

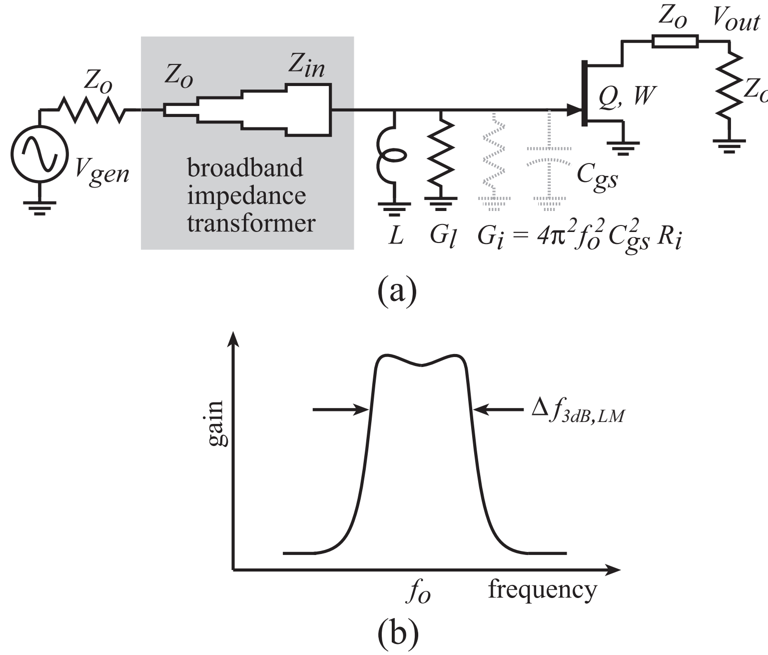

Figure 3.6: (a) A.C. circuit schematic and (b) typical frequency response of a lossy matched common source amplifier.

In the lossy matched power amplifier (fig. 3.6) [14, 15] the shunt inductance (L) resonates with C_{gs} at the center frequency f_o. The shunt conductance G_l along with the broadband impedance transformer provides the input match to Z_o. For design frequencies $f_o \ll 1/(2\pi R_i C_{gs})$, the impedance transformer should transform Z_o to Z_{in} given by,

$$\begin{aligned} Z_{in} &= \frac{1}{G_l + G_i} \ , \\ G_i &= 4\pi^2 f_o^2 C_{gs}^2 R_i \ . \end{aligned} \tag{3.16}$$

The mid-band voltage gain and transducer power gain are then given by,

$$\begin{aligned} S_{21,LM} &= \frac{G_m Z_o}{2\pi f_o C_{gs}\sqrt{Z_{in} Z_o}} \ , \\ G_{T,LM} &= \frac{(V_{br} - V_k)\, I_{DSS}}{V_p^2} \frac{1}{4\pi^2 f_o^2 C_{gs}^2 Z_{in}} \ , \end{aligned} \tag{3.17}$$

respectively. The amplifier bandwidth is improved (compared to the reactively matched amplifier),

$$\begin{aligned} Q \equiv \frac{f_o}{\Delta f_{3dB,LM}} &\equiv \frac{2\pi f_o C}{G} = \pi f_o Z_{in} C_{gs} \ , \\ \Delta f_{3dB,LM} &= \frac{1}{\pi C_{gs} Z_{in}} \ , \end{aligned} \tag{3.18}$$

at the cost of reduced gain. Thus G_l could be varied to trade-off gain for bandwidth in addition to using degeneration.

3.5 Bridge-tee matched amplifier

Bridge-tee matching [16, 17] uses a lossy all-pass matching network (fig. 3.7) to provide good input reflection coefficient and flat gain. The element values for obtaining input match over wide bandwidth are given by,

$$\begin{aligned} L_1 &= (Z_o - R_i) Z_o C_{gs}/2 \ , \\ L_2 &= (Z_o + R_i) Z_o C_{gs}/2 \ , \\ C_1 &= (1 - R_i^2/Z_o^2) C_{gs}/4 \ . \end{aligned} \tag{3.19}$$

The mid-band voltage gain and transducer power gain are same as the common source case (eq. 3.7), but the amplifier exhibits a gain peaking and the gain falls to the low frequency value at

$$\Delta f_{BT} = \frac{1}{\pi Z_o C_{gs}} \sqrt{\frac{(1 - 3(R_i/Z_o))}{(1 - (R_i/Z_o))\,(1 - (R_i/Z_o)^2)}} \simeq \frac{1}{\pi Z_o C_{gs}} \ , \tag{3.20}$$

for $R_i \ll Z_o$. Note that the -3 dB bandwidth is somewhat larger than Δf_{BT} (exact expressions for f_{3dB} are intractable).

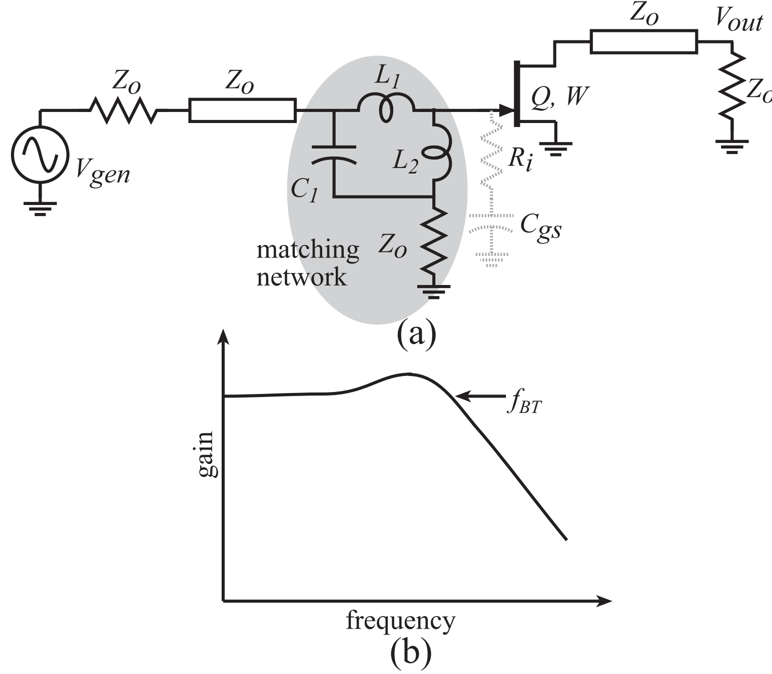

Figure 3.7: (a) A.C. circuit schematic and (b) typical frequency response of a bridge-tee lossy matched amplifier.

3.6 Resistive feedback amplifier

Resistive feedback power amplifier [15, 18, 19] uses a drain to source feedback resistance (fig. 3.8) of value,

$$R_f = Z_o(1 - A_v) \ , \tag{3.21}$$

to match the input and output to Z_o. The loadline constraint for the resistive feedback case is,

$$I_{DSS} = \frac{(V_{br} - V_k)}{Z_o}\left(1 + \frac{1}{A_v}\right) \ . \tag{3.22}$$

In the absence of degeneration, the mid-band voltage gain (A_v) is fixed and given by,

$$A_v = (1 - G_m Z_o) \cong \frac{(V_{br} - V_k)}{V_p} \ . \tag{3.23}$$

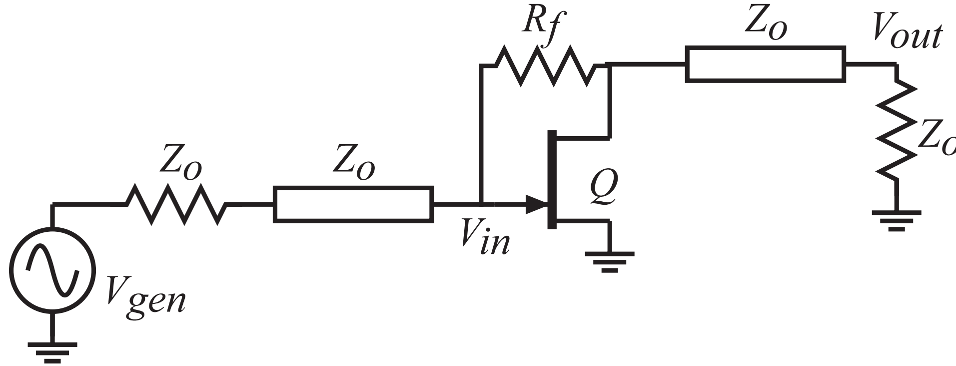

Figure 3.8: A.C. circuit schematic of a resistive feedback amplifier.

In the presence of degeneration, the degenerated value of G_m (eq. 3.10 or 3.11) should be used in the above equations.

The bandwidth and gain-bandwidth products are similar to the common source case (eq. 3.8 and 3.9). Unlike the other amplifiers considered above, resistive feedback amplifiers provide good output reflection coefficients while providing close to class-A limited efficiencies (for high gain designs).

3.7 Distributed amplifier

Unlike the frequency selective impedance matching circuits considered earlier, that provide efficient coupling to a device over narrow bandwidths, distributed circuits [12, 20, 21, 22] allows efficient coupling to a group of devices over broad bandwidths. Distributed or traveling-wave amplifiers (TWAs) (fig. 3.9) obtain high bandwidth by absorbing the transistor input capacitances (C_{gs}) into a synthetic input (gate) transmission line. This input synthetic line introduces relative delays between the drive voltages of the various transistors within the TWA. A similar synthetic output (drain) transmission line provides compensating delays in the output circuit, so that A.C. drain currents of the individual transistors add in-phase at the load.

While the transistor output capacitance (C_{ds}) is also absorbed into the output synthetic line, HEMTs typically have $C_{ds} \ll C_{gs}$, and the high bandwidths (fig. 3.10) observed with TWAs results from incorporation

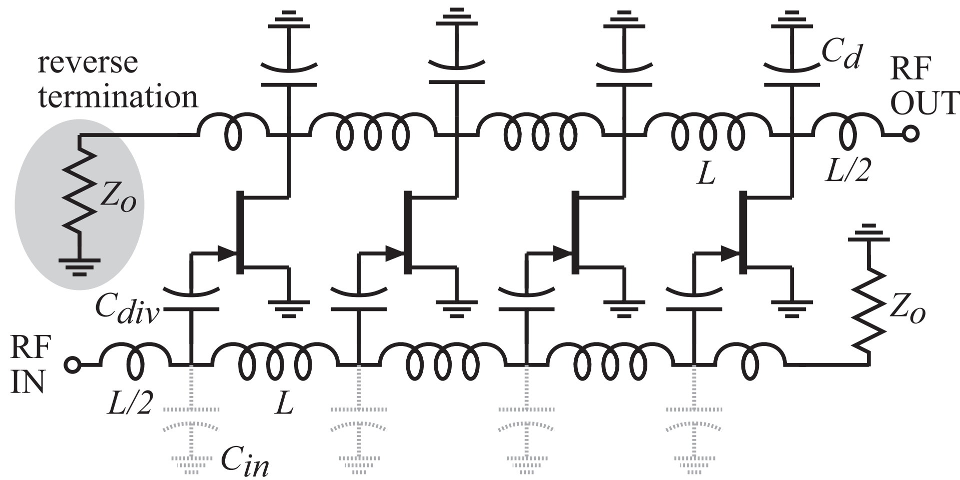

Figure 3.9: A.C. circuit schematic of a distributed amplifier.

of C_{gs} into the input synthetic line. The output synthetic line is present primarily for delay equalization.

In TWAs with synthetic output transmission lines, the A.C. drain current of each transistor contributes equally to forward and reverse waves on the output line. At low frequencies, the lengths of the delay lines are negligible and each device is matched to its optimum load. However due to the reverse termination which consumes half the output power, efficiency is limited to 25% in class-A operation. At higher frequencies where the line delays are significant the reverse waves do not add up in phase. So the power lost in the reverse termination is smaller [23]. However the loadlines seen by the devices are far from optimum due to the same reason, resulting in lesser output power and efficiency. Reported monolithic power TWAs typically have 10-15% PAE. Though modifications to this topology like the tapered-drain-line TWA [22] have been suggested that can provide theoretical class-A efficiency approaching 50%, they are difficult to realize in monolithic form especially for high powers. This and improved distributed architectures for high power, like the cascode-delay-matched distributed amplifiers are the topic of discussion in chapter 6.

Thus to obtain high output power over broad bandwidths we must de-

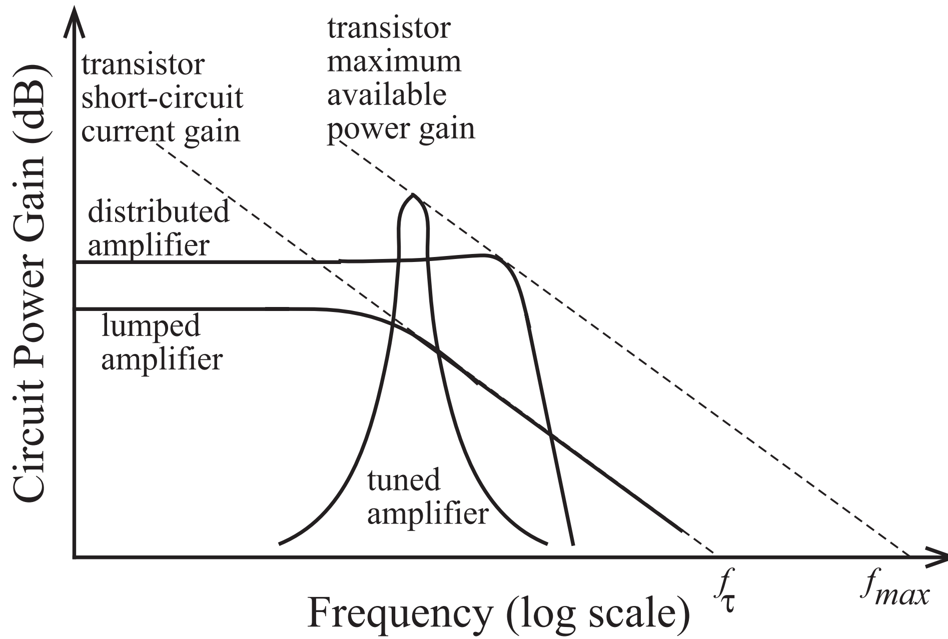

Figure 3.10: Typical frequency response of a distributed amplifier compared to lumped amplifiers.

velop power amplifiers whose bandwidth is not limited by f_τ, in a high $f_\tau V_{br}$ material system like GaN. In chapters 4 we will look at the materials and processing aspects of the GaN /AlGaN HEMT technology and present device results from the wafers used for the circuit runs. In chapter 5 and 6, we present alternate lumped and distributed broadband power amplifier topologies whose bandwidth are not limited by the device f_τ and can provide efficiencies up to the class-A limit.

Chapter 4

Processing and device results

ALGAN / GAN HEMTs used in this work were grown by Metal Organic Chemical Vapor Deposition (MOCVD) on C - plane sapphire substrate. Due to the poor thermal conductivity of the sapphire substrate, large periphery devices were flip chip bonded on to a AlN carrier wafer [25, 26]. The AlN substrate acts as a thermal carrier providing a low impedance thermal path for efficient heat sinking.

The circuit process consists of six mask steps for the GaN wafer and six mask steps for the AlN substrates. An i - line stepper lithography (365 nm wavelength) capable of producing 0.5 μm features was used for both processes. The sapphire wafer contains the active devices and one level of interconnect. The AlN substrate contains all the passive elements including resistors, Si_3N_4 capacitors, inductors realized using high impedance lines and controlled impedance coplanar waveguide (CPW) transmission lines. Au bond pads, 2.5 μm in thickness were evaporated on both the sapphire and AlN substrates for the flip chip bonding. The GaN and AlN wafers are then diced and bonded together. The details for the GaN / AlGaN HEMTs and AlN substrate processes are presented in this chapter along with the D.C. and R.F. test device data from the different process runs used for circuit fabrication. Appendix A presents a summary of the process steps. Detailed GaN and AlN substrate process flows are available in appendix B and C respectively.

4.1 GaN HEMT process

The sapphire substrate process consists of six mask steps. They include the standard four mask process step for the GaN HEMTs consisting of the source and drain ohmic contacts, gate pad isolation, gate finger Schottky contacts and mesa isolation of the devices. An interconnect metal layer and an evaporated bond pad layer were added for the circuit process.

4.1.1 Growth

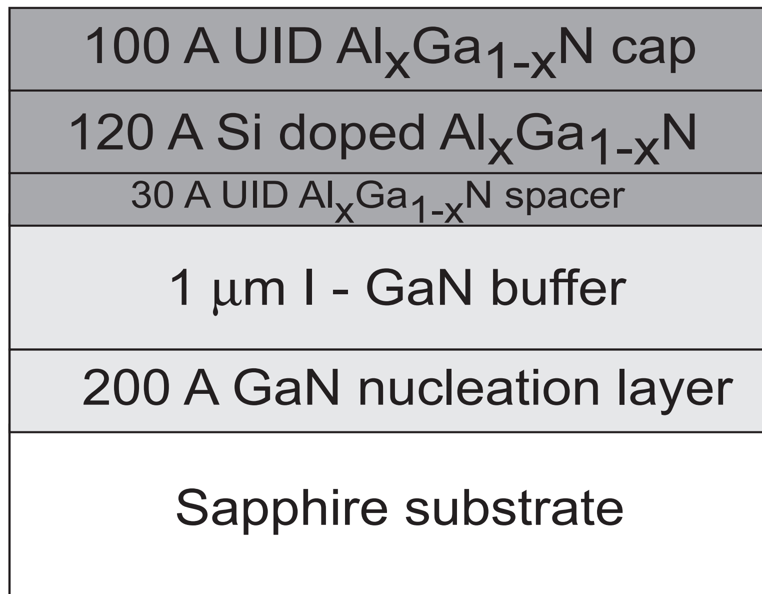

Figure 4.1: Typical layer structure of an AlGaN / GaN HEMT wafer.

Fig. 4.1 shows a typical layer structure of an AlGaN / GaN HEMT wafer. The growth starts with a 200 Å GaN nucleation layer on a C-plane sapphire substrate. This is followed by a 1.4 μm thick insulating GaN buffer grown under low pressure, or a bilayer I-GaN consisting of 1 μm low pressure I-GaN and 1 μm atmospheric pressure I-GaN as the device buffer layer. The $Al_{0.15}Ga_{0.85}N$ gate structure consists of a 30 Å spacer, a 150 Å Si-doped charge layer (n = 3 $\times$ 10^{18} cm^{-3}) and a 120 Å unintentionally doped cap. The background doping in a UID $Al_{0.15}Ga_{0.85}N$ is $\sim$ 1 $\times$ 10^{18}

cm^{-3}. Higher Al content up to 35 % in the AlGaN layer is known to improve device performance [27] and is used in some of the growths. The improved performance is due to the larger bandgap and the increased conduction band discontinuity (ΔE_c) resulting in larger breakdown field and better carrier confinement, allowing high mobilities and large carrier densities.

4.1.2 Ohmic contacts

The fabrication starts with the formation of ohmic contacts by depositing Ti/Al/Ni/Au of thickness 200/2000/550/500 Å respectively. Standard e-beam evaporation and lift-off process was used for all metalization in the GaN wafer. Ti is known to form TiN on annealing, resulting in N deficiency in GaN, which is equivalent to n-type doping. The n$^+$-GaN interface along with the conductive TiN forms excellent ohmic contacts. The Au layer is for better conductivity and for preventing oxidation of the Al, while the Ni is for reducing the Au/Al mixing. Usual precautionary measures during GaN processing, like avoiding KOH based developers (which are known to etch AlGaN slowly) were followed.

Reactive Ion Etching (RIE) with Cl_2 for 15 seconds at 6 Å/s, is used to damage the ohmic region prior to metal evaporation. The AlGaN layer is thinned to ∼100 Å as previous study have shown the reaction depth of Ti on GaN to be about 150 Å. The reaction depth on AlGaN is expected to be similar or lesser. A surface cleaning with $NH_4OH : H_2O$ of 1 : 10 is used to lower the specific ohmic resistance further.

After evaporation and lift-off the wafer is annealed at 875 °C for 25 seconds in a Rapid Thermal Annealer (RTA). At these temperatures the RTA has occasionally shown random temperature fluctuations of up to 20 ° which severely degrades the ohmic contacts (fig. 4.2). Also additional precaution is necessary while loading the wafer into the chamber, as the sapphire substrate slides freely on smooth Si wafer on which it is loaded. Contact resistances ∼ 0.47 Ω-mm (fig. 4.3) were measured using Transmission Line Measurements (TLM) patterns on the best wafers.

4.1.3 Gate pad isolation

SiO_2 is then used to isolate the gate contact pad and eliminate any extra substrate capacitance. RIE with Cl_2 for 40 seconds at 20 Å/s is used to

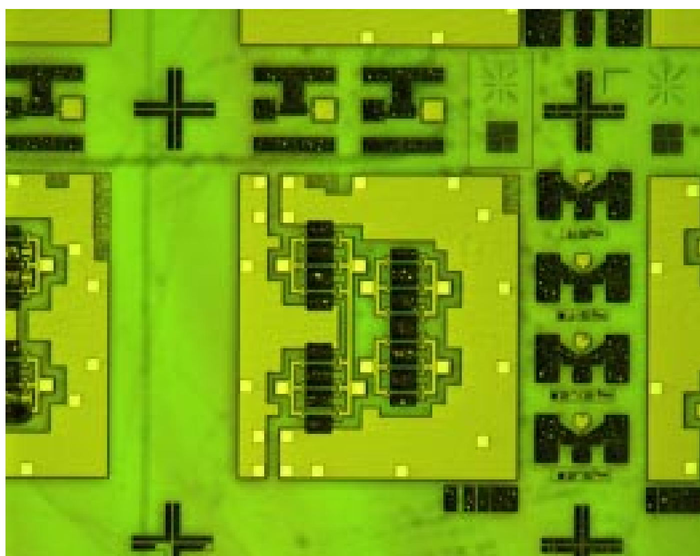

Figure 4.2: Micrograph of a bad source and drain ohmic anneal due to temperature instabilities in the RTA.

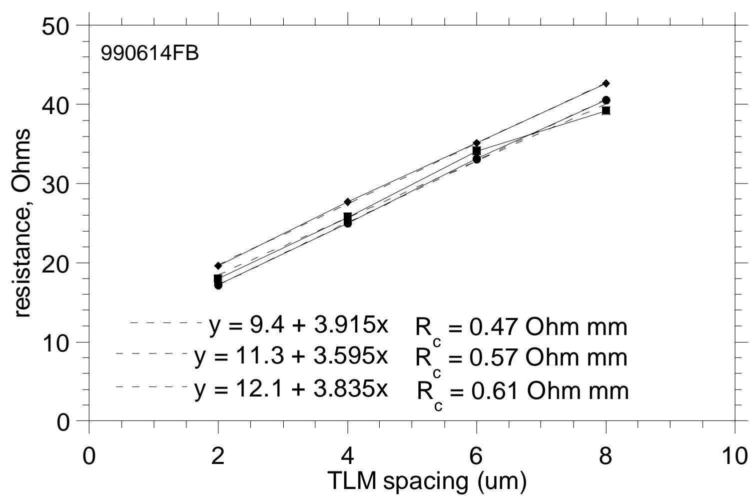

Figure 4.3: Typical contact resistances obtained from TLM measurements (wafer # 990614FB).

etch the GaN cap and AlGaN layers. SiO_2 is evaporated to fill the etched regions so that the gate fingers run over down from the gate contact pad. A slow rate of evaporation (2 - 3 Å/s) is preferred, as the oxide has been observed to peel off after higher rates of evaporation.

4.1.4 Schottky gates

The third and most critical step in the process is the gate finger metalization step. In the circuit process the gate fingers and the gate interconnect metal were split on to separate layers. This enhances the lift-off of large periphery multi-finger devices (fig. 4.4), especially the dual gate devices which will have interdigitated fingers (fig. 4.5) accessed from either side of the active layer.

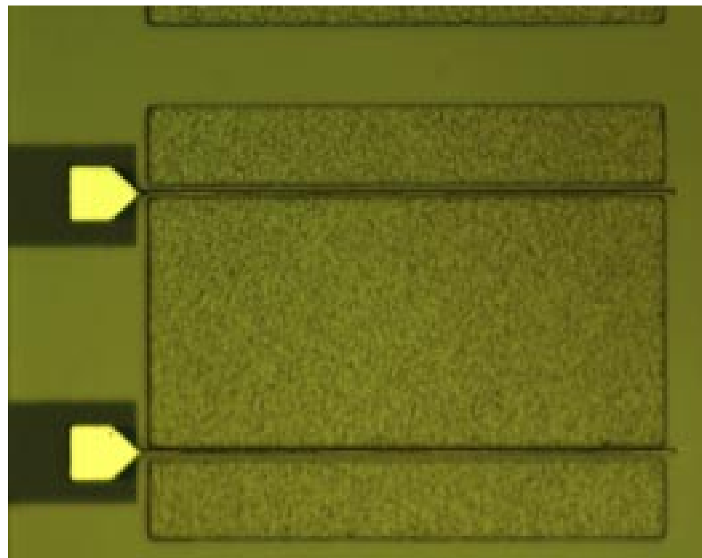

Figure 4.4: Micrograph of gate fingers in large periphery GaN HEMT devices.

A bi-layer resist process with SPR 950-0.8 and Contrast Enhancement Material layer, capable of defining 0.5 μm features on plane substrates with the i - line stepper, is used. However consistent high yielding large periphery devices typically have 0.7 $\sim$ 1 μm periphery. This is because the gate fingers

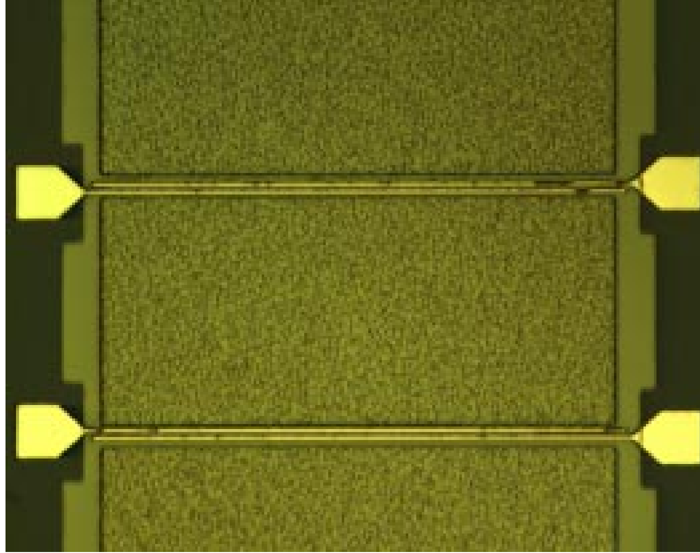

Figure 4.5: Micrograph of a 0.7 μm gate length fingers in large periphery dual-gate devices.

are being defined between the source and drain pads which are $\sim$ 3000 Å thick. Also the high temperature annealing of the ohmic contacts leaves jagged source and drain edges making the alignment harder. Gate recess is not done as RIE introduces damage to the surface and reduces breakdown voltages.

GaN shows low extent of barrier pinning by surface traps, and exhibits Schottky behavior with different metals which generally follows work function difference. With reported electron affinity of $\sim$4.2 eV, Al ($\Phi \sim 4.2$ eV) always forms a natural ohmic contact on clean n-GaN surfaces. Au, Pt and Ni ($\Phi = 5 \sim 5.5$ eV) has relatively high Schottky barriers of 0.8 $\sim$ 1.1 eV on n-GaN and are potential candidates for gate metal on GaN and AlGaN. A surface cleaning with NH_4OH : H_2O of 1 : 10 was used to remove the thin layer of surface insulator believed to exist. Ni/Au/Ni of thickness 200/4000/500 Å is used for the gate fingers. The first layer of Ni is to improve the adhesion of Au. Since Ti forms TiN which is ohmic it is essential that the Ni source be contamination free. It is advisable to have a separate Ni source for the gate finger evaporation. The Au thickness is

chosen to be able to carry the R.F. gate current at high frequencies. The second Ni layer acts as a etch mask for the mesa isolation step.

4.1.5 Mesa isolation

Cl_2 RIE is again used to dry etch GaN and AlGaN surfaces to isolate the device mesas. A 2 μm thick layer of hard baked SPR 518-A protects the active area during the etch. The etch rates have been previously observed to depend on the DC-bias than on the Cl_2 pressure, indicating the etching is highly energy driven. Etching is done for $3 \sim 4$ minutes at the rate of 20 Å/s. This is followed by a wet etch using a HNO_3 based Ni etchant to remove the Ni on top of the gate finger access pad. This step was not used in the first process run. Yield of the large periphery devices was low in that run due to large number of open gates. This is attributed to poor ohmic contact between the interconnect metal layer and the gate finger access pad, due to the oxidation of Ni on top of the gate fingers.

4.1.6 Interconnects

One layer of interconnect was added to the GaN HEMT process which serves the following purposes:

- to provide a continuous ground plane around the active devices. This helps in maintaining ground plane continuity between the input and output on the AlN substrate. Since it is not possible to use air-bridges on AlN underneath the bonded GaN die, this interconnect layer was used for ground plane cross-over about the signal and bias connections (fig. 4.6).

- as was mentioned earlier, connections between individual gate fingers was moved to this layer to facilitate easy lift-off of interdigitated fingers in large periphery dual-gate devices (fig. 4.6.(c)).

- to connect the drains together. Some circuits have only the sources flip-chip bonded to minimize drain to source capacitance. In these circuits the drains are connected together using this interconnect layer and then flip bonded using a single bond pad (fig. 4.6.(a,b)).

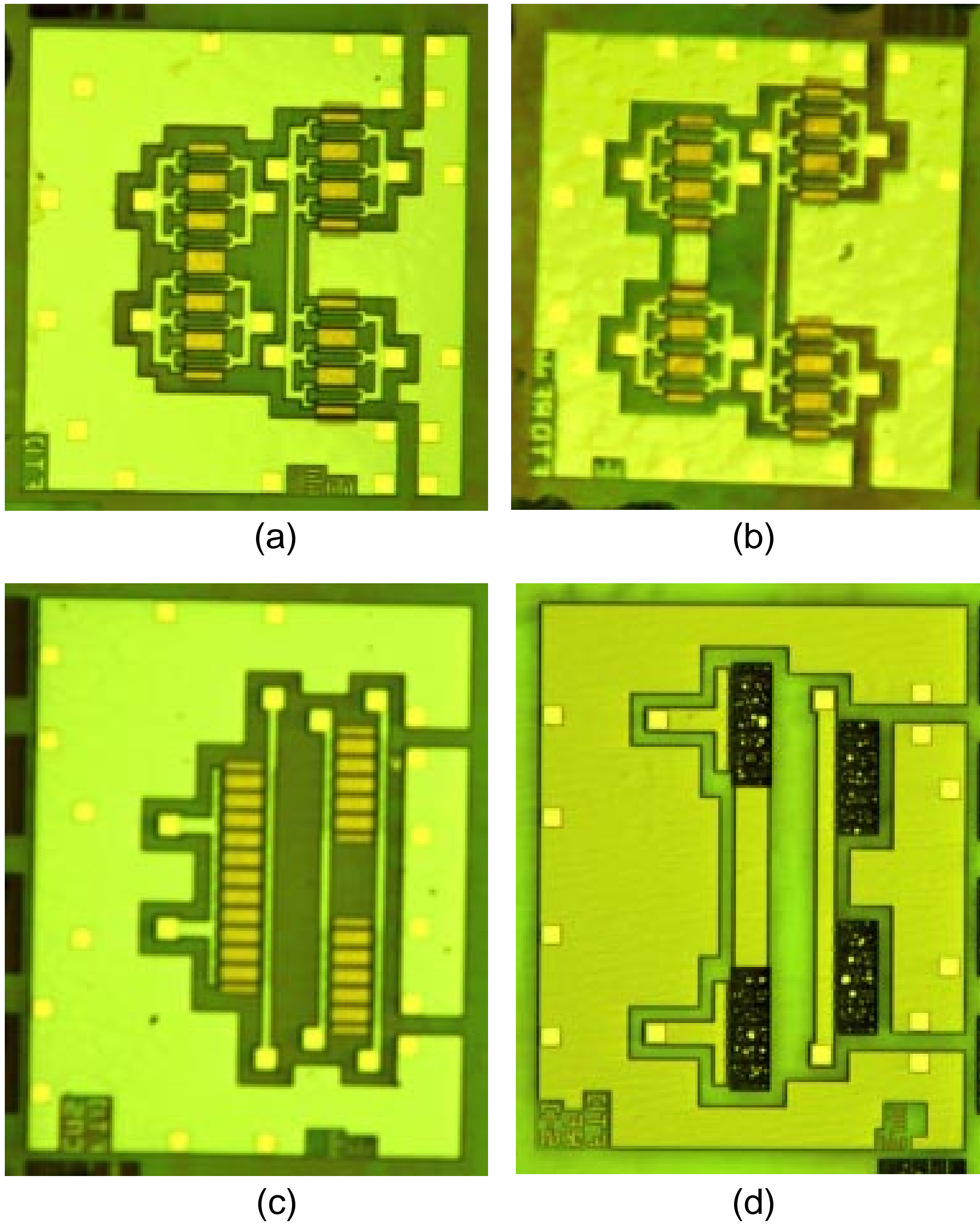

Figure 4.6: Micrograph of the GaN HEMT dice for (a) f_τ-doubler, (b) resistive feedback f_τ-doubler, (c) resistive feedback f_τ-doubler with source and drain bonds, and (d) dual-gate cascode f_τ-doubler power amplifiers.

Ti/Au/Ti of 200/4000/100 Å thickness was used for metalization. The thickness and width were decided based on a peak D.C. current density of 5 mA/μm^2 set by the electro-migration limits of Au. After the lift-off the transistors were tested for D.C. and R.F. performance before proceeding to the next mask step.

4.1.7 Bond pad metalization

A bi-layer resist process is used to evaporate and lift-off 2.5 μm thick metal bond pads. Electro-plating was tried in the first run to deposit thick metal, but was subsequently discontinued due to uneven surface morphology with the electro-plated Au. 2.5 μm thick deep-UV sensitive PMGI-SF15 resist is first spun and baked. Lithography using 1 μm thick SPR 950-0.8 is then done. This is followed by deep - UV exposure and development of PMGI to obtain 3.5 μm thick resist pattern with a lift-off profile. Evaporation is done with the wafer kept at a distance of 31.5 cm from the source (by lowering the wafer mount) to increase the evaporation rate. Lift-off of the top resist layer is followed by exposure and development of PMGI underneath.

4.1.8 Dicing

The wafer is then protected with photoresist and bonded to a Si carrier before dicing. A brown bonding wax is used to provide better adhesion compared to the crystalbond - 509 mounting wax. For die sizes of $\sim$ 1 mm $\times$ 1 mm crystalbond - 509 mounting wax was found to be insufficient for holding the dice on the carrier substrate. Bonding to the Si substrate should be done with caution to prevent the resist from being over baked during the bonding. Also sufficient pressure must be applied during bonding to remove any air bubbles in the molten wax that could lead to dice peeling off during dicing. Once diced the dies are individually cleaned in ultrasonic to remove the saw dust deposited during the dicing. The dice then flip chip bonded as described in page 52.

4.2 AlN substrate process

The AlN substrate process consists of six mask steps. This includes nichrome resistors, two layers of interconnect metals, metal-insulator-metal (MIM)

capacitors, bond pad metal and air-bridges.

4.2.1 Resistors

Nichrome resistors of sheet resistivity ~50 Ω/□ are obtained by evaporating ~ 475 Å of NiCr. Since the source is prone to spitting evaporation must be done with caution. The sheet resistivity was found to vary depending on how long the source has been used and the surface morphology of the substrate. So calibration using a test substrate was found necessary especially with new sources. Oxygen plasma descum during further processing could also change the resistivity due to the Ni getting oxidized on the surface. So the second generation circuits used a Si_3N_4 protective coating over the resistors. The resistors were contacted using Metal - 1 interconnect layer. Burn in tests of resistors showed peak D.C. current density capability of 4 ~ 5 mA/μm and peak power densities up to ~ 1.2 mW/μm^2. The resistors in circuits were designed for a peak current density of 1 mA/μm.

4.2.2 Metal - 1

First interconnect metal layer (Metal - 1) was deposited by evaporation and lift-off of Ti/Au/Ti of thickness 200/10000/100 Å respectively. The two layers of Ti are used for better adhesion of Au to the substrate and of the photoresist in the later process steps to Au. Evaporation must be done with caution to avoid spitting as surface roughness could cause shorts in MIM capacitors to be deposited in the next step. The resistors are tested for their sheet resistivity after this step.

4.2.3 Capacitors

Si_3N_4 for capacitors is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD). The process is done in two steps of 2500 Å and 1500 Å with surface cleaning and orientation change in between, to prevent the formation of any through pin holes in the nitride. This is immediately followed by photolithography and RIE using SF_6 to etch the nitride from everywhere except where capacitors are required. As was mentioned earlier in the second generation circuits Si_3N_4 was used for protecting the NiCr resistors. Also it was used as a protective covering for the signal conduc-

tors underneath the air-bridges to prevent accidental shorting of any fallen bridges during dicing and die handling.

4000 Å thick nitride is expected to give a capacitance per unit area of 0.128 fF/μm^2. However in some of the process runs up to a 75% higher capacitances was obtained. This is attributed to the poor quality of the nitride deposited by PECVD during that period. The system was subsequently overhauled and recalibrated.

4.2.4 Metal - 2

Second interconnect metal layer (Metal - 2) is used for the top metal in MIM capacitors. Additionally sections of signal lines and ground planes in the CPW layout were deposited in the metal - 2 step (fig. 4.7). This split of interconnects and ground planes between metal - 1 and 2 was done to ensure that there are no enclosed features in either mask steps, which could lead to lift-off failure. Again Ti/Au/Ti of thickness 200/10000/100 Å respectively was used. The wafer is mounted on a rotating chuck, set at an angle of 30° with respect to the source, to get a step coverage of metal - 2 over the 4000 Å thick Si_3N_4. The capacitors are tested for shorts after this step. Typical capacitor breakdown voltages are in excess of 100 V (fig. 4.8) and so they could be used for bias decoupling in the resistive feedback network, as well as a shunt element in the output matching networks.

4.2.5 Bond pad metalization

A bi-layer resist process similar to the GaN bond pad metalization is used to evaporate and lift-off 2.5 μm thick metal bond pads. The same mask is also used to define the post layer for the air-bridges. Earlier process runs used separate mask steps for the bond pads and for the air-bridge posts (total of seven mask steps). The process described here is the newer six mask step process. 2.5 μm thick deep-UV sensitive PMGI-SF15 resist is first spun and baked. Lithography using 1 μm thick SPR 950-0.8 is then done to define bond pads as well as air-bridge posts. This is followed by deep - UV exposure and development of PMGI to obtain 3.5 μm thick resist pattern with a lift-off profile. Evaporation is done with the wafer kept at a distance of 31.5 cm from the source (by lowering the wafer mount) to increase the evaporation rate. Lift-off is performed in acetone which removes SPR 950-

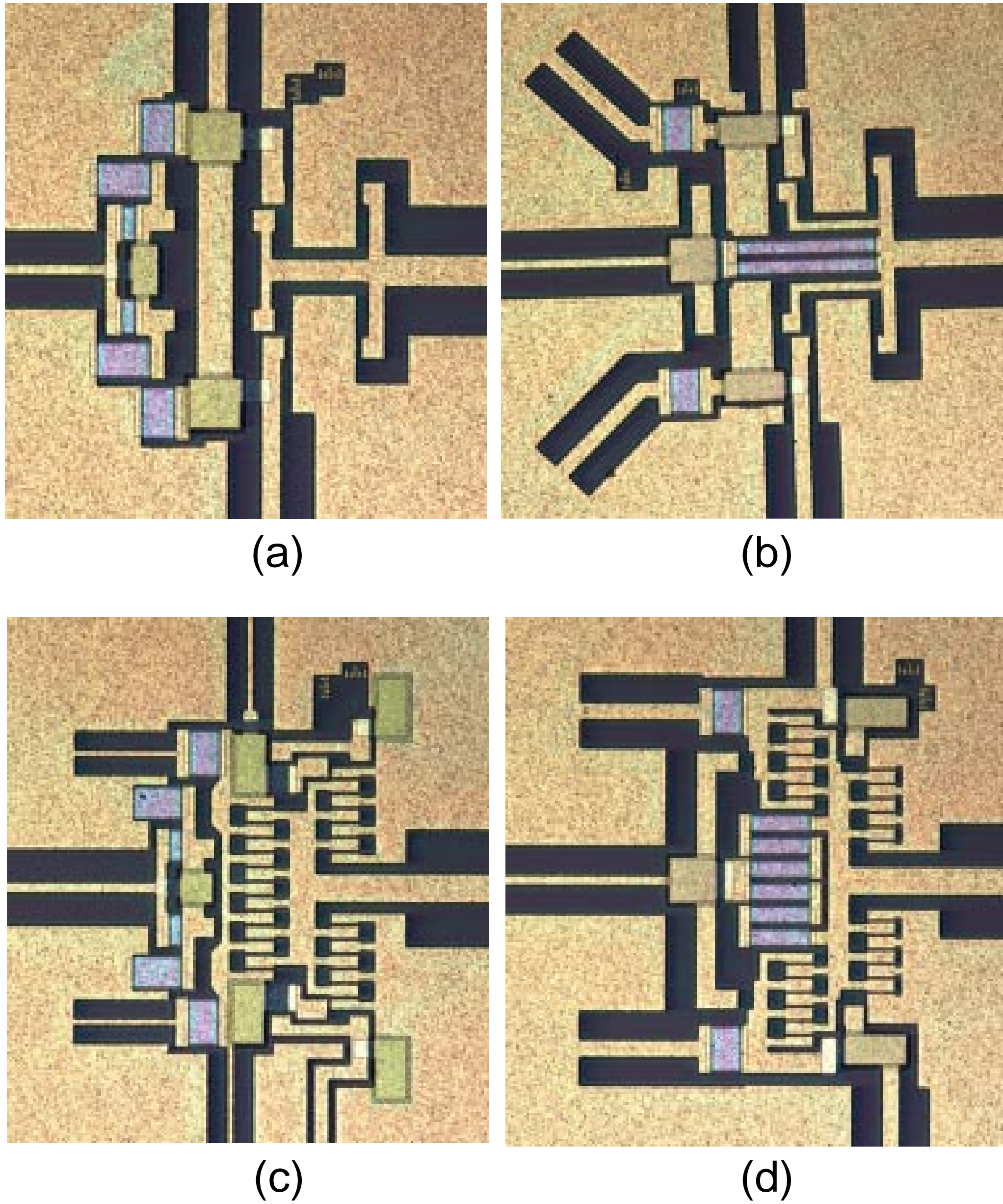

Figure 4.7: Micrograph of the AlN substrate dice for (a) f_τ-doubler, (b) resistive feedback f_τ-doubler, (c) resistive feedback f_τ-doubler with source and drain bonds, and (d) dual-gate cascode f_τ-doubler power amplifiers.

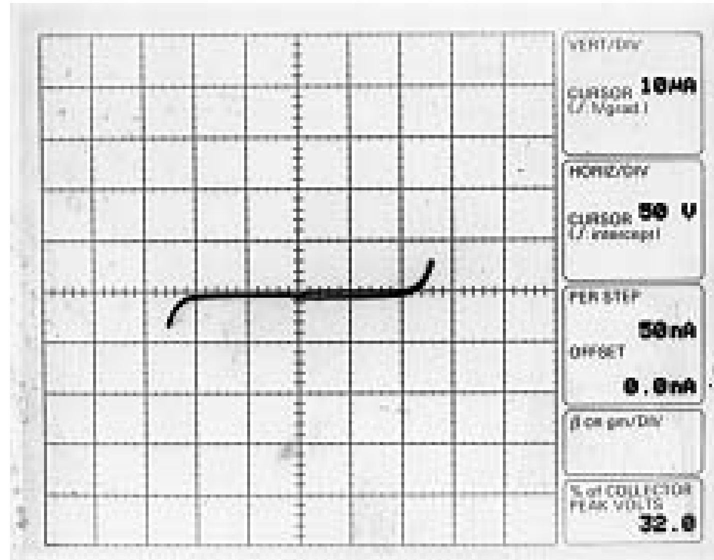

Figure 4.8: Measured breakdown voltages in excess of 100 V for 4000 Å thick Si_3N_4 MIM capacitors.

0.8 leaving behind PMGI which is impervious to acetone. The PMGI layer is used for the next air-bridge mask step.

4.2.6 Plated air-bridges

After a 5 second etch in a diluted Au etchant to roughen the surface of the posts, a flash layer of Ti/Au/Ti of thickness 300/1000/100 Å is evaporated using angle rotated evaporation to obtain step coverage over the side walls of the PMGI. This is followed by photolithography to define the air-bridges and Au plating to a thickness of 3 μm. The top layer of resist is removed in acetone, and the flash layers of Ti/Au/Ti is etched in buffered HF and Au etchants. The bottom PMGI layer is retained until dicing is completed to provide stability to the air-bridges while dicing.

4.2.7 Dicing

The wafer is then protected with photoresist and bonded to a Si carrier using crystalbond - 509 mounting wax before dicing. Bonding to the Si

substrate should be done with caution to prevent the resist from being over baked during the bonding. Once diced the dies are individually cleaned in acetone to remove the top photoresist layer and in warm 1165 to remove the bottom PMGI layer.

4.2.8 Flip chip bonding

Circuits and large periphery devices are flip chip bonded [28] before testing. The GaN and AlN dice to be bonded are thoroughly cleaned to remove any dirt accumulated during dicing. Calibration of the flip chip bonder is done first to align the top and bottom camera probes. The dice are vacuum held on the top and bottom chucks and visual alignment is done using the camera probes and alignment marks on the dice. Since the optimum bonding temperature and pressure depends on the number and cross-sectional area of the bond pads, a few test runs are performed first with bad dies. Typically a pressure of 3000 g / 0.25 mm^2 total bond pad area, at a temperature of 250 ° works well. Automatic bonding sequence is initiated to complete the bonding. The bonded die is visually checked under a microscope for alignment (the sapphire substrate being transparent) and planarity of the bonding, followed by a D.C. testing to verify connectivity. R.F. testing is done after bonding the AlN substrate to a Cu heat sink using silver epoxy. The Cu heat sink is further mechanically mounted on to the probe station during testing.

4.3 Device D.C. and R.F. measurements

D.C. and R.F. measurements are performed on the test devices without flip chip bonding. Since the test devices are measured on-wafer, smaller periphery is used to avoid thermally limited performance. 150 μm periphery (fig. 4.9) is chosen based on the power limiting capability of the curve tracer. Gate lengths of 0.4 - 1.0 μm mask dimensions were used for the test devices.

The typical mask dimensions for the large periphery devices in the circuits were gate to source separation of $L_{gs} = 0.7$ μm, gate length of $L_g = 0.5$ μm and drain to gate separation of $L_{gd} = 1.5$ μm. The layout of the device including the separation between the gate fingers and the total device periphery per unit area were chosen based on extensive thermal modeling of flip chip bonded devices, done by others [29].

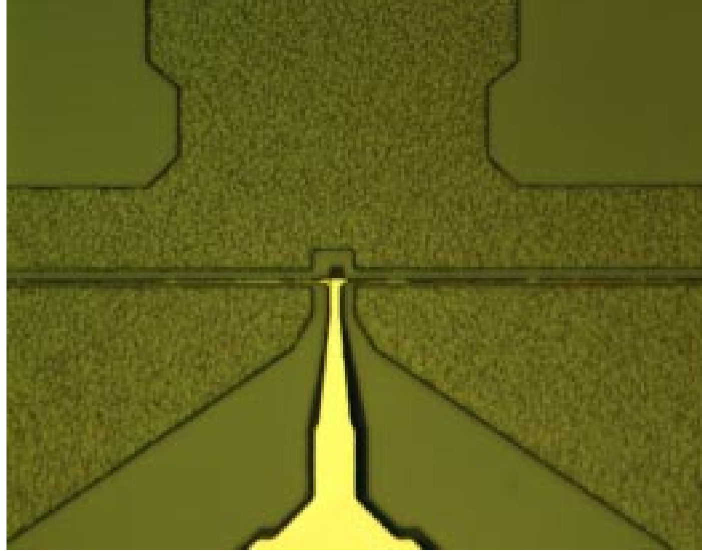

Figure 4.9: Micrograph of a 0.5 μm gate length x 150 μm wide test device.

Fig. 4.10 shows a typical D.C. I-V plot from a good wafer. Peak currents of up to 875 mA/mm (at V_{gs} = 1 V) have been obtained with V_p = -5 V and V_k = 6 V and breakdown voltages greater than 75 V with measured leakage currents <6 mA/mm at V_{ds} = 50 V. The negative resistance on the I-V curve is attributed to the self heating due to the poor thermal conductivity of the sapphire substrate.

Microwave power measurements were performed at 8 GHz with an automated load pull system. The input match was optimized to maximize the delivered power and the output to maximize the output power. Although the breakdown voltages are greater than 75 V, a compromised class-AB D.C. bias with V_{ds} = 25 V and I_d = 25 mA was used to avoid thermal degradation. In the best wafer, maximum output power of 27.7 dBm was obtained at an input power of 15.5 dBm, translating to a power density of 3.92 W/mm with 36 % PAE (fig. 4.11). The linear small signal linear gain was 17 dB. Device performance is thermally limited and degrades at higher biases.

Five GaN process runs for the circuits were carried out to completion. Table 4.1 on page 56 lists the typical D.C. and best R.F. power performance

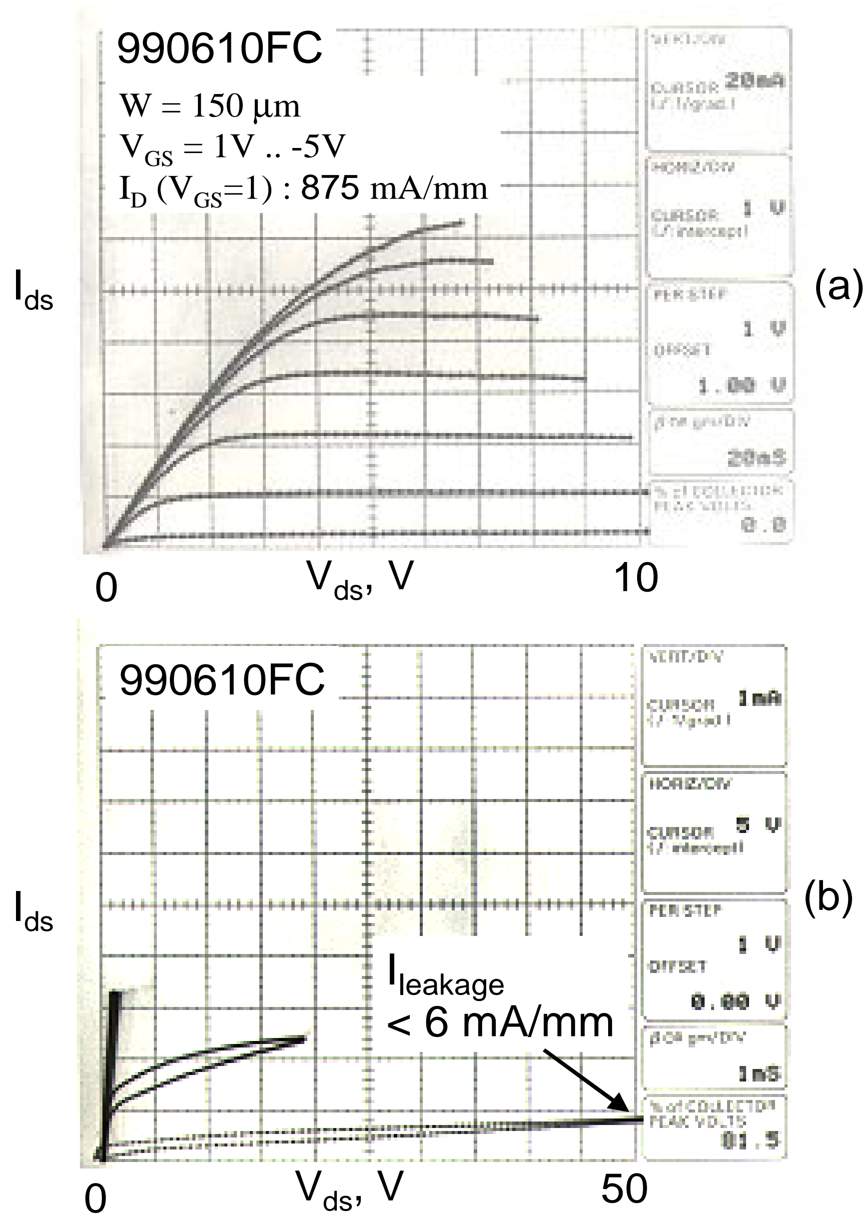

Figure 4.10: Typical D.C. I-V plot for a 150 μm periphery device (wafer # 990610FC) showing (a) peak saturation current and (b) leakage current.

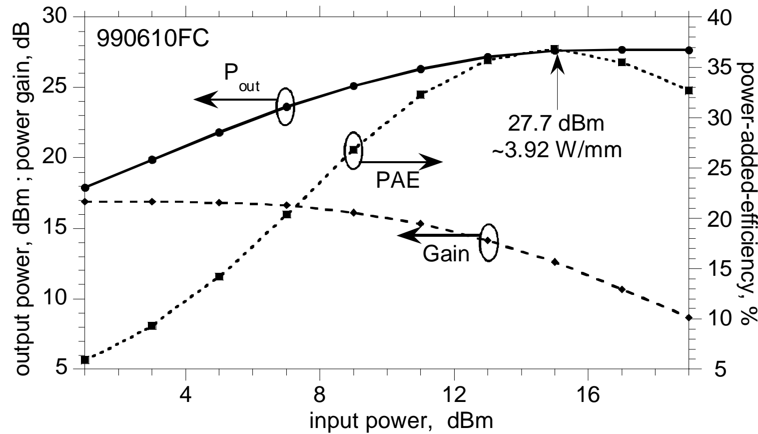

Figure 4.11: R.F. power performance of a 150 μm periphery device (wafer # 990610FC).

of the test devices in the various process runs, and details of the circuits bonded and tested. The power performance from the initial runs were poor inspite of good D.C. performance in some cases. This has been attributed to strong D.C. to R.F. dispersion in those wafers, possibly due to the presence of surface traps [30]. Various causes for this have been reported in literature including growth related and process related issues, and is still a intense topic of research. However, this work does not intend to address that problem. Oxygen plasma descum has been suggested to degrade the R.F. performance, and the additional process steps for the circuit process could have worsened the performance. In the later runs minimum descum time was used to minimize this degradation.

The circuit results presented in the next two chapters are from wafers #981216FD and #990614FA. The device yield in wafer #981216FD was poor due to the oxidation of Ni between the gate finger metalization and interconnect metal, leading to open gates at places. This oxide breaks down on applying 8 $\sim$ 10 V, and the circuits were bonded and tested after that. First generation f_τ-doubler circuit results presented are from this wafer.

Table 4.1: D.C. and R.F. power performance of the test devices in the completed process runs, and details of the circuits bonded and tested

wafer #	I_{max} (mA/mm)	P_{out} (W/mm)	comments	circuits tested
981216FD	650	2.59	low device yield : open gates, dispersion, leakage	f_τ doublers
990616FB	370	–	poor ohmics : RTA instabilities	–
990614FB	875	1	high dispersion	–
990614FA	900	2.54	dispersion, low circuit yield : SiO_2 peeling off	f_τ doublers
990610FC	830	3.92	good wafer	f_τ doublers CDM TWAs

The later process runs used a Ni etch step to alleviate this problem. Also substantial leakage currents up to 100 mA/mm at 50 V V_{ds} (fig. 4.12) was observed in this run further degrading the power performance of the circuits.

Due to temperature instabilities and the wafer sliding within the RTA, the ohmic contacts were poor in wafer #990616FB as is seen in the linear region of the device I-V (fig. 4.13). The drain saturation currents were too small to warrant power measurements or bonding circuits.

Wafer #990614FB exhibited good D.C. characteristics with 875 mA/mm peak current but peak R.F. output power of only 1 W/mm at 15% PAE and 12 dB small signal gain (fig. 4.14) indicate significant dispersion.

Wafer #990614FA had excellent D.C. characteristics with 900 mA/mm peak current and average R.F. performance with up to 2.54 W/mm output power at 33% PAE and 19 dB small signal gain (fig. 4.15). However the yield was low due to the gate pad oxide peeling off at places. f_τ-doubler circuits were bonded and tested using devices from this run.

Wafer #990610FC had good D.C. characteristics with 830 mA/mm peak

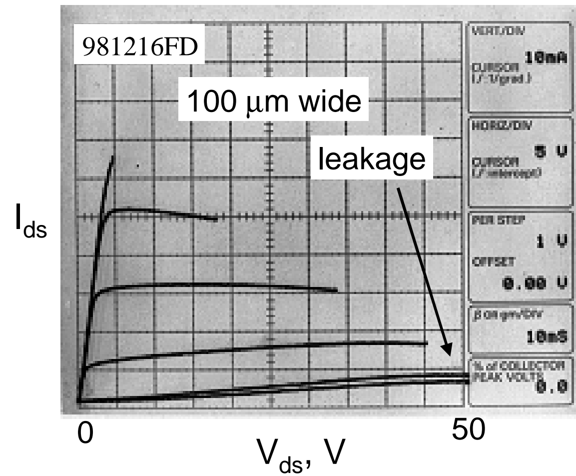

Figure 4.12: Leakage currents measured in a 100 μm wide device (wafer # 981216FD).

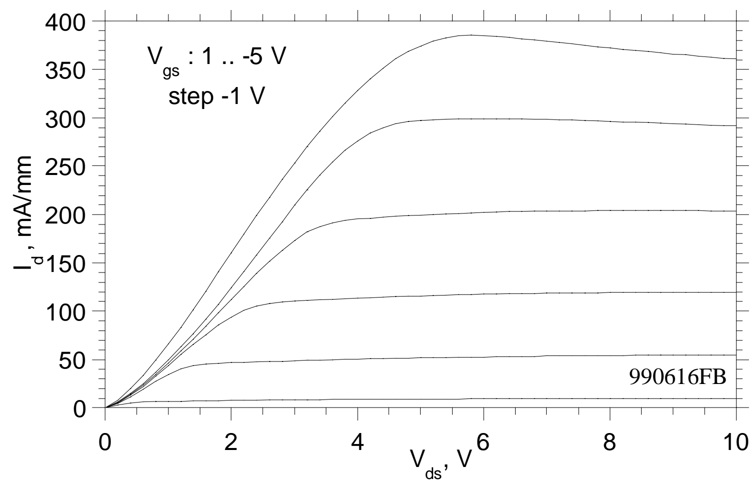

Figure 4.13: Typical D.C. I-V plot for a 150 μm periphery device (wafer # 990616FB).

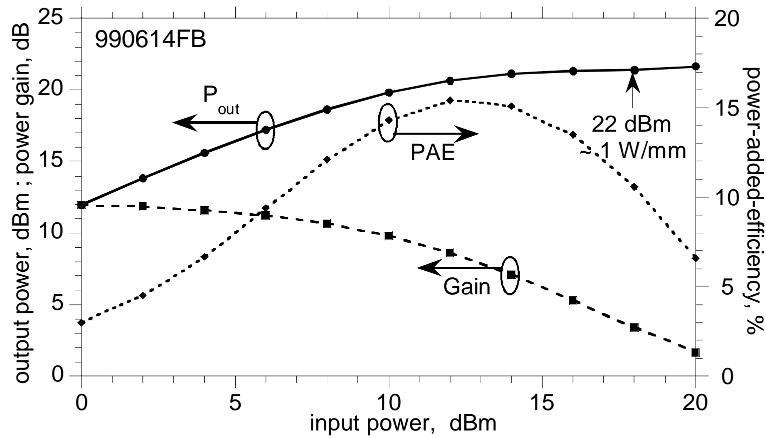

Figure 4.14: R.F. power performance of a 150 μm periphery device (wafer # 990614FB).

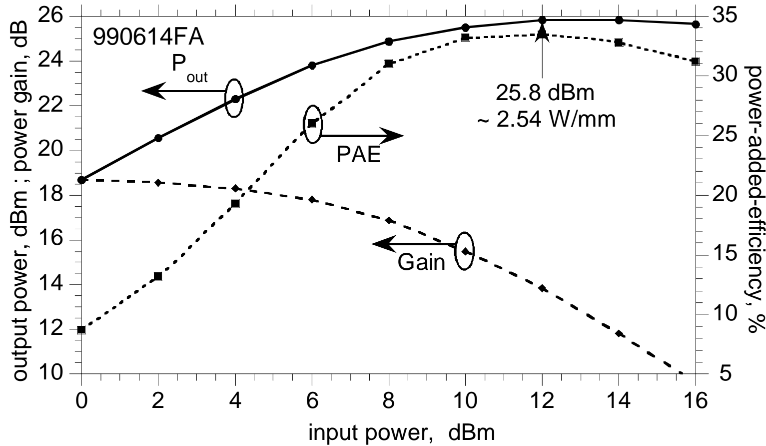

Figure 4.15: R.F. power performance of a 150 μm periphery device (wafer # 990614FA).

current and < 6mA/mm leakage at 50 V V_{ds}, (fig. 4.10) and excellent R.F. performance with up to 3.92 W/mm output power at 36% PAE and 17 dB small signal gain (fig. 4.11). The results from the second generation of f_τ-doubler circuits and cascode-delay-matched distributed power amplifiers presented in chapters 5 and 6 are from this process run.

Chapter 5

f_T-multiplier power amplifiers

IN chapter 3 we saw that simple lumped broadband amplifiers have gain-bandwidth products limited by the transistor current-gain cut-off frequency, f_τ . We also saw that distributed amplifiers could provide gain-bandwidth products up to the power-gain cutoff frequency, f_{max} [21], [22] but have poor efficiency and occupies large die areas.

In this chapter we look at an alternative lumped broad-band power amplifier based on the f_τ- doubler topology [36]. f_τ- doubler small-signal amplifiers have shown gain-bandwidth products approaching twice the transistor f_τ [37, 38]. As a power amplifier f_τ- doubler circuits can provide higher efficiency and smaller die area than conventional distributed amplifiers. Results from f_τ-doubler power amplifiers in GaAs MESFET technology [39, 40] and from GaN HEMT technology [41] are presented.

f_τ-doubler resistive feedback power amplifier MMICs in a GaAs MESFET technology offering 18 GHz f_τ and 12 V breakdown achieved, 0.2 - 6 GHz bandwidth, 12 dB gain, over 23 dBm output power, and more than 25 % power-added-efficiency. These circuits have gain-bandwidth products of $\sim 1.3 \cdot f_\tau$ and are more efficient than distributed power amplifiers.

First generation of GaN based f_τ-doubler broad-band power amplifiers yielded, ∼11 dB gain, 0.2 - 7.5 GHz bandwidth amplifiers with ∼1.5 W output power and up to 15% PAE. The poor RF output power is attributed to the strong DC-RF dispersion observed in that wafer. Second generation of circuits achieved ∼10 dB small signal gain, 1 - 8.0 GHz bandwidth amplifiers with 5.12 W peak output power and up to 23% PAE. With better devices, improved thermal heat sinking, and better modeling significantly

improved performance could be achieved from these circuits.

5.1 Darlington power amplifiers

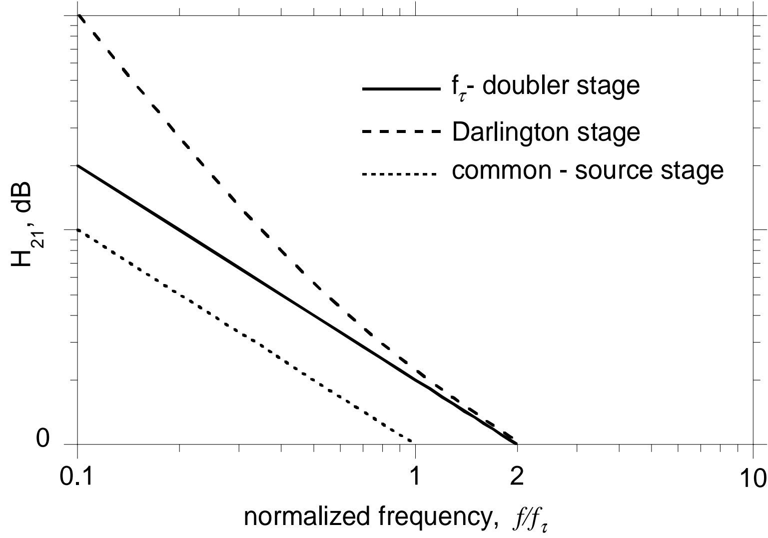

Figure 5.1: Short circuit current gain H_{21} for common-source, Darlington and f_τ-doubler configurations.

In chapter 3 we saw that a simple broadband common-source power amplifier without input tuning has a gain bandwidth product of f_τ (eq. 3.9 on page 28). This is because the short circuit current gain of a common-source configuration, using a simplified FET model of fig. 3.1 on page 26, is

$$H_{21,CS} = \left(\frac{G_m}{\omega C_{gs}}\right) \equiv \left(\frac{f_\tau}{jf}\right) , \tag{5.1}$$

and reaches unity at f_τ (fig. 5.1). As was seen in chapter 3 capacitive [12] or resistive degeneration provides higher bandwidth at lower gain with constant gain-bandwidth product. To obtain sufficiently high PAE (up to 40%), gains > 10 dB are required, limiting bandwidth to $f_{3dB} < f_\tau/3$. With other parasitics considered, bandwidth falls significantly below $f_\tau/3$.

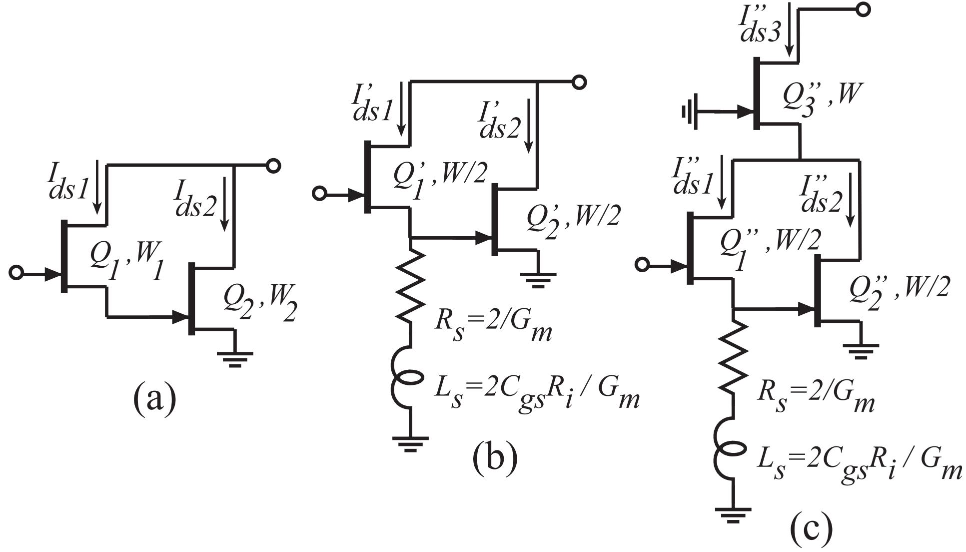

Figure 5.2: A.C. schematics of (a) basic Darlington, (b) f_τ-doubler configurations and (c) cascode f_τ-doubler configurations.

Darlington amplifiers have higher bandwidth [42] than common-source amplifiers but provide lesser efficiency. If the drain of the common-drain device is connected to the amplifier output (fig. 5.2(a)), then the current gain

$$H_{21,Darlington} = \frac{(1 + j2f/f_\tau)}{(jf/f_\tau)^2} , \tag{5.2}$$

is twice that of a common-source stage at high frequencies (fig. 5.1), reaching unity at $2f_\tau$. The peak output power obtainable from a Darlington stage is

$$P_{out,Darlington} \leq \frac{(V_{br} - V_k - V_p)^2}{8Z_o} \equiv \frac{V_{o,p-p}}{8Z_o} , \tag{5.3}$$

slightly less than the common-source case (eq. 2.3 on page 20) because the peak - peak output voltage, $V_{o,p-p}$ is now reduced by the pinch-off voltage, V_p. Of greater importance for efficiency is the ratio of the A.C. currents of the two devices. This ratio is independent of device sizing and is frequency-dependent, given by

$$\frac{I_{ds1}}{I_{ds2}} = \frac{(jf/f_\tau)}{(1 + jf/f_\tau)} . \tag{5.4}$$

At low frequencies, transistor Q_2 provides the entire A.C. output current. Thus, a Darlington amplifier designed for the same power level as the common-source power amplifier must have $I_{DSS2} = V_{o,p-p}/Z_o$ or $W_2 = W$, the same periphery as the device in the common-source case. At high frequencies (of the order of f_τ) the A.C. output current is provided equally by Q_1 and Q_2. Thus, we must have $I_{DSS1} = V_{o,p-p}/2Z_o$ or $W_1 = W/2$. Thus, in the Darlington power amplifier, the total device periphery and the net bias current are a factor of 1.5 higher than in a common-source power amplifier designed for the same A.C. output current. D.C. power consumption is a factor of 1.5 higher and the PAE is impaired. Improved bandwidth is obtained at the cost of lower PAE. Potential instability due to negative input resistance

$$Z_{in,Darlington} = R_{i1} + R_{i2} - \frac{G_{m1}}{\omega^2 C_{gs1} C_{gs2}} + \frac{1}{j\omega}\left(\frac{1 + G_{m1}R_{i2}}{C_{gs1}} + \frac{1}{C_{gs2}}\right) , \quad (5.5)$$

is a further limitation of Darlington.

5.2 f_τ-doubler power amplifiers

The f_τ-doubler power amplifier (fig. 5.2(b)) is a modified Darlington stage where suitable source loading of Q_1' splits the input voltage equally between Q_1' and Q_2', so that $I_{ds1}' = I_{ds2}'$ at all frequencies. The source loading consists of a resistor, $R_s = 2/G_m$ in series with an inductor, $L_s = 2C_{gs}R_i/G_m$. Published f_τ-doubler amplifiers [37, 38] have not incorporated this inductor. L_s is required to obtain equal input voltage division between Q_1' and Q_2' for frequencies $f \sim 1/2\pi R_i C_{gs}$; the L_s/R_s time constant being set equal to the $R_i C_{gs}$ time constant.

With this source loading Q_1' and Q_2' carry equal A.C. drain current for all frequencies. Thus, for the two devices to reach saturation simultaneously, we require that $I_{DSS1}' = I_{DSS2}' = V_{o,p-p}/2Z_o$. Hence the two devices should have half the periphery of a common-source stage of equal output power (i.e. $W/2$). The two devices, Q_1' and Q_2', have marginally different loadlines given by $(2Z_o + 2/G_m)$ and $2Z_o$ respectively. This is due to the extra source loading seen by Q_1', which limits the peak-peak V_{ds} of Q_1' and Q_2' to $(V_{br} - V_k)$ and $(V_{br} - V_k - V_p)$ respectively (fig. 5.3). This does not significantly affect the output power provided that $Z_o \gg 1/G_m$ or $(V_{br} - V_k) \gg V_p$. As in the

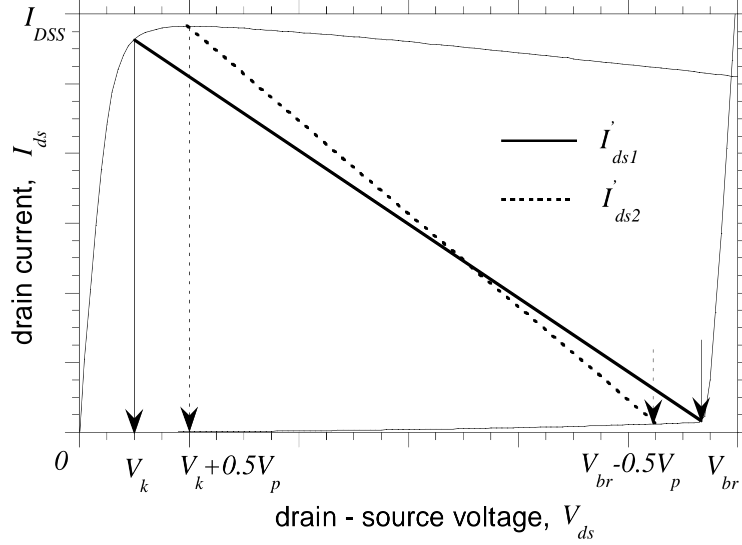

Figure 5.3: Load-lines seen by the two devices in a f_τ-doubler power amplifier, super-imposed on the device $I_{ds} - V_{ds}$ plot.

case of the Darlington amplifier, the peak output power

$$P_{out,f_\tau-doubler} \leq \frac{(V_{br} - V_k - V_p)(V_{br} - V_k - V_p/2)}{8Z_o} , \tag{5.6}$$

is slightly smaller than common-source power amplifier. DC power consumption is similar to the common-source case provided that D.C. power dissipation in the source resistance is eliminated by grounding the source of $Q_1^{'}$ for D.C. using a RF choke. The current gain of the f_τ-doubler stage

$$H_{21,f_\tau-doubler} = \left(\frac{2f_\tau}{jf}\right) , \tag{5.7}$$

has a single pole and is unity at $2f_\tau$ (fig. 5.1). Thus bandwidth is improved without significant loss in efficiency. Stability is also improved as the input impedance of the f_τ-doubler

$$Z_{in,f_\tau-doubler} = R_{i1} + R_{i2} + \frac{1}{j\omega}\left(\frac{1}{C_{gs1}} + \frac{1}{C_{gs2}}\right) , \tag{5.8}$$

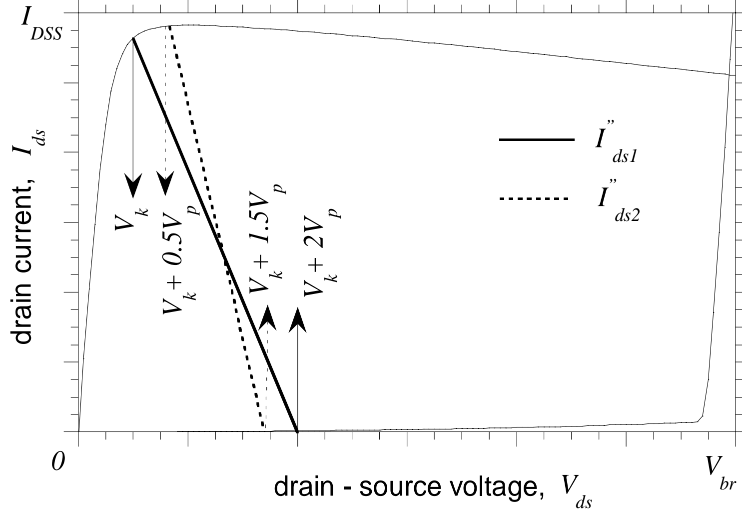

Figure 5.4: Load-lines seen by the two devices, Q_1'' and Q_2'' in a cascode f_τ-doubler power amplifier, super-imposed on the device $I_{ds} - V_{ds}$ plot.

no longer has a negative resistance.

Because the f_τ-doubler topology alleviates the bandwidth limitation due to C_{gs}, the parasitic C_{gd} and C_{ds} may then become significant. Addition of a common-gate stage to form a cascode f_τ-doubler (fig. 5.2 (c)) reduces the effect of C_{gd} substantially. In this case, since the f_τ-doubler is driving a low input impedance common-gate stage, the two devices Q_1'' and Q_2'' drive widely different loads of $4/G_m$ and $2/G_m$ respectively (fig. 5.4). However the power dissipated in Q_1'' and Q_2'' is a small fraction of the net output power as in the case of a cascode (common-source - common-gate) amplifier.

For all the configurations considered above, the capacitances C_{gd} and C_{ds} load the amplifier output. The device A.C. loadline then deviates at high frequencies from that required for peak PAE [43]. We will see in chapter 7 that inductive networks could be used to partially compensate for the effect of C_{gd} and C_{ds} on output loading, improving the efficiency. These networks are effective over a bandwidth of at most $f_{out} = I_{DSS}/2\pi C_{ds} V_{br}$.

5.3 GaAs MESFET f_T-doubler power amplifiers

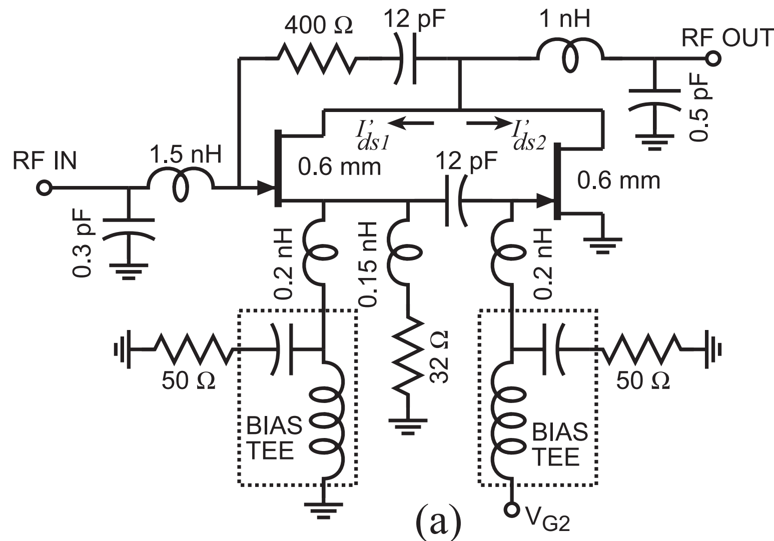

Figure 5.5: Complete schematic of GaAs f_T-doubler resistive feedback power amplifier.

Scale model GaAs MESFET f_T-doubler power amplifiers ICs were fabricated using the Triquint Semiconductor, Inc., TQTRx process to verify the circuit concept. TQTRx is a 0.6 μm MESFET process which has enhancement and depletion mode MESFETs with three layer gold interconnect on a low-ϵ dielectric substrate [9]. Nichrome resistors, MIM capacitors and high-Q spiral inductors are also available. Circuits were simulated using TOM2 large signal MESFET models.

Fig. 5.5 shows the circuit diagram of the f_T-doubler power amplifier. Resistive feedback was used to match the input and output impedances to 50 Ω without significant loss of efficiency. Broad-band π-sections at the input and output improve matching. High Q spiral inductors were obtained by using two layers of metalization. External bias tees were used to independently bias the two devices. The source of the first device was grounded for D.C. through a bias tee. This also facilitates monitoring the device bias currents. The source loading was split into three parallel sections, with the

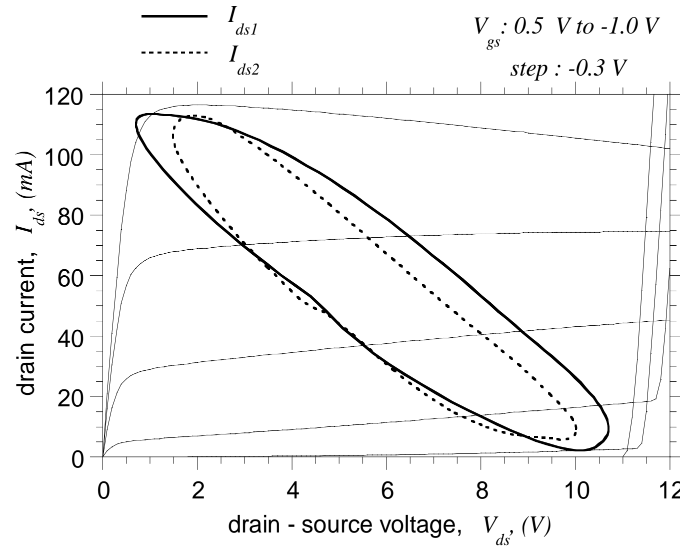

Figure 5.6: Simulated load-lines of the devices in GaAs f_T-doubler resistive feedback power amplifier (frequency = 3 GHz), super-imposed on the simulated device $I_{ds} - V_{ds}$ plot.

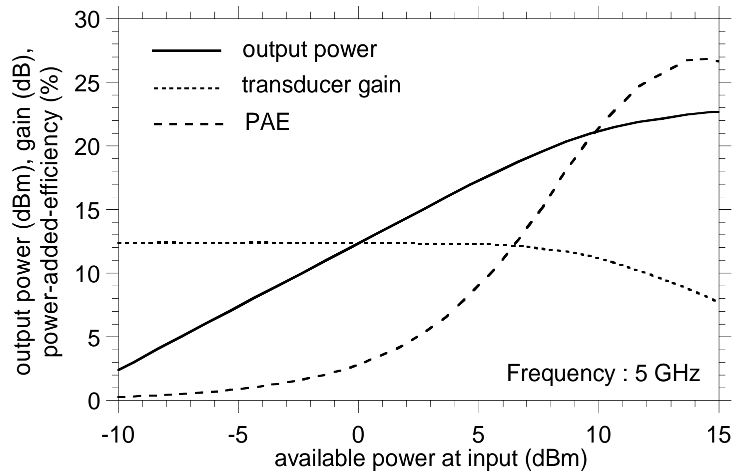

Figure 5.7: Power performance of the GaAs f_T-doubler power amplifier at 5 GHz.

bias tee's 50 Ω A.C. ports providing part of the RF termination.

The simulated load-line for the two devices (fig. 5.6) at 3 GHz shows a nearly equal current division. The capacitive current seen in the load-line is due to the device parasitic capacitance at the drain. Measured power performance (output power, transducer power gain and PAE) at 5 GHz, (fig. 5.7) shows a peak output power of 23 dBm with 27% PAE.

Figure 5.8: Complete schematic of the GaAs cascode f_τ-doubler resistive feedback power amplifier.

Fig. 5.8 shows the circuit diagram of the cascode f_τ-doubler power amplifier. A secondary RC feedback network, effective at high frequency, provides unconditional stability.

Fig. 5.9 shows the simulated load-line for the three devices at 3 GHz. Measured power performance at 6 GHz (fig. 5.10) shows a peak output power of 23 dBm with 26% PAE.

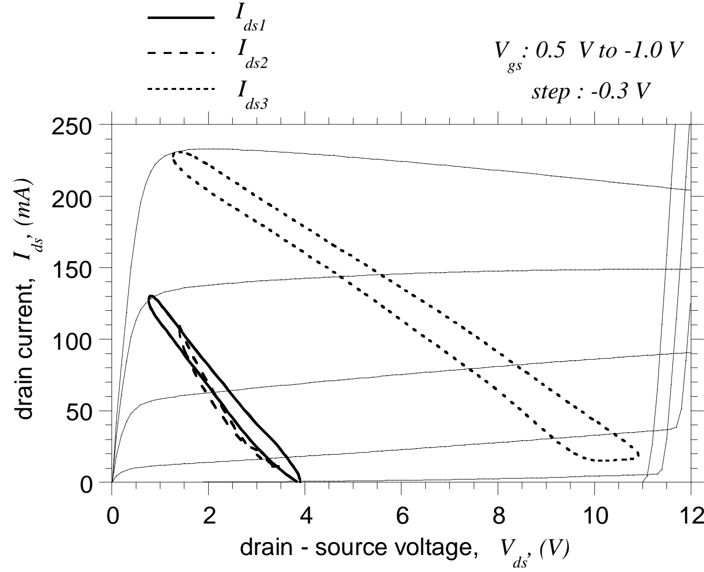

Figure 5.9: Simulated load-lines of the devices in the GaAs cascode f_T-doubler resistive feedback power amplifier (frequency = 3 GHz), superimposed on the simulated device $I_{ds} - V_{ds}$ plot.

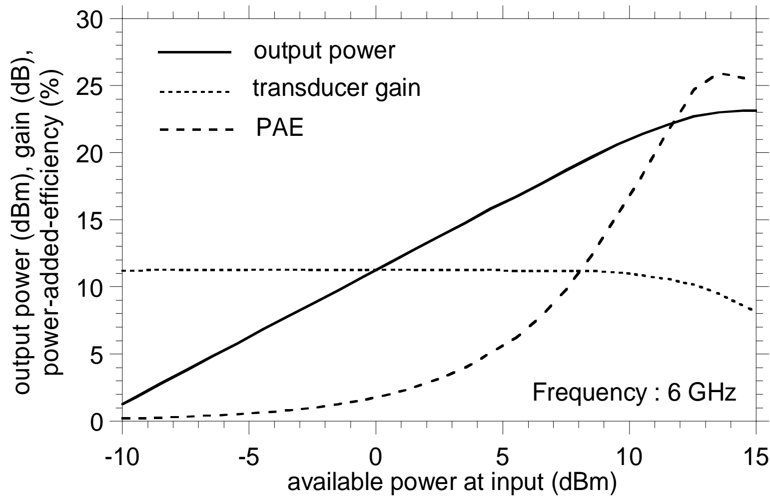

Figure 5.10: Power performance of the GaAs cascode f_T-doubler at 6 GHz.

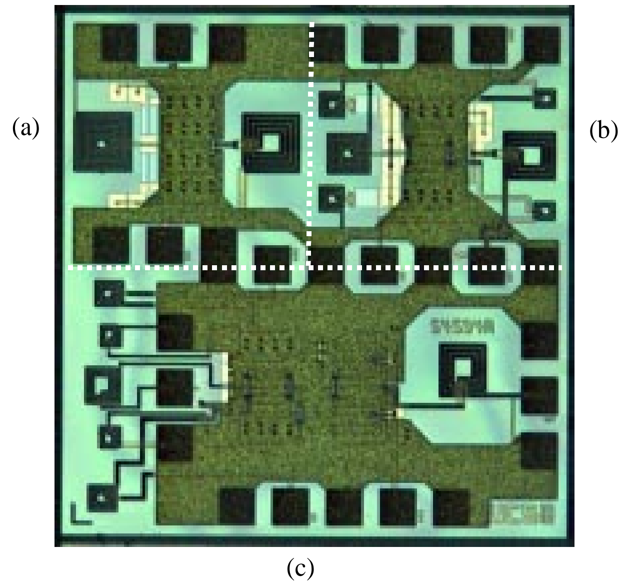

Figure 5.11: Chip photograph of the GaAs (a) common-source , (b) f_τ-doubler and (c) cascode f_τ-doubler power amplifiers.

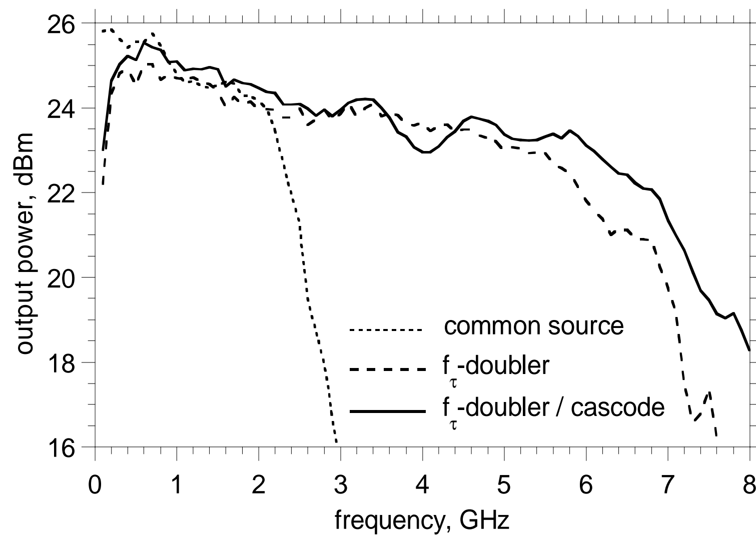

Figure 5.12: Measured output power of the GaAs MESFET amplifiers as a function of frequency.

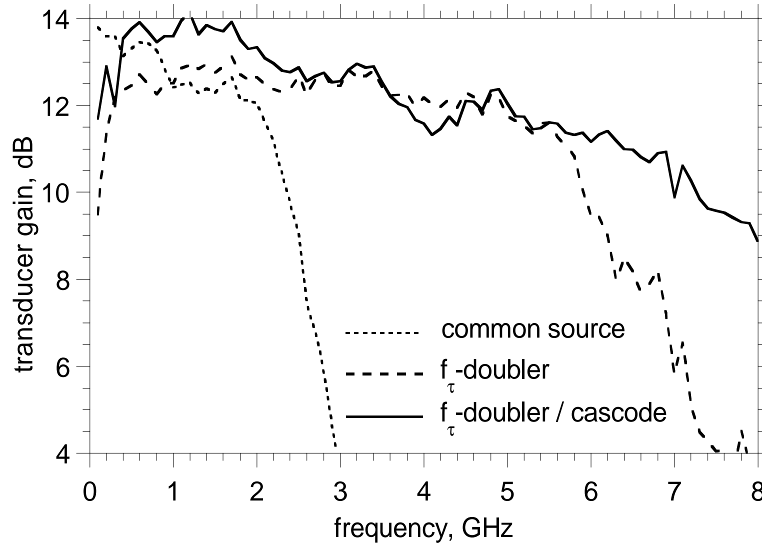

Figure 5.13: Measured transducer gain of the GaAs MESFET amplifiers as a function of frequency.

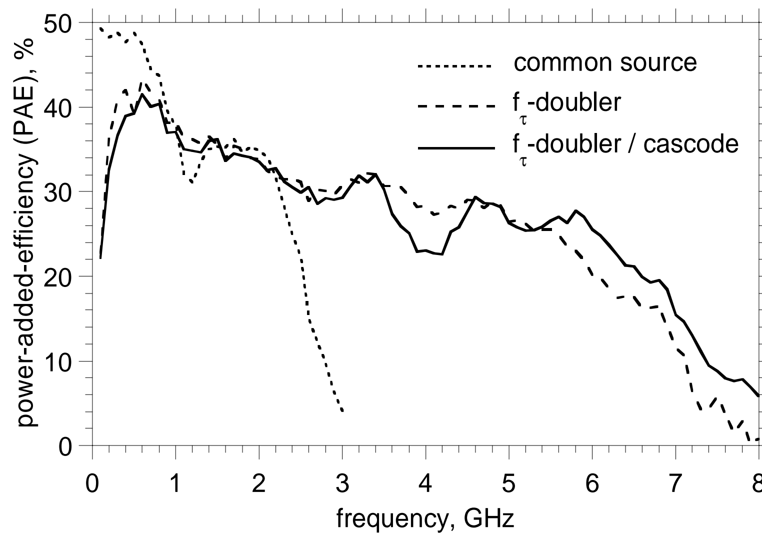

Figure 5.14: Measured power-added-efficiency of the GaAs MESFET amplifiers as a function of frequency.

Common-source power amplifiers were also fabricated for comparison. The die area (fig. 5.11) for the common-source , f_τ-doubler and cascode f_τ-doubler amplifiers are 0.64 mm $\times$ 0.66 mm, 0.7 mm $\times$ 0.7 mm and 1.36 mm $\times$ 0.75 mm respectively. The f_τ-doubler occupies similar die area as the common-source power amplifiers. f_τ-doubler power amplifiers using dual-gate FETs should provide similar performance as cascode f_τ-doubler power amplifiers without the excess die area.

Fig. 5.12, 5.13, 5.14 compares the power performance of the three circuits measured over 0.1 - 8 GHz . The common-source PA provides > 24 dBm output power over 2 GHz bandwidth with $> 30\%$ PAE. The f_τ-doubler PA and the cascode f_τ-doubler PA provide > 23 dBm output power over 0.2 - 5 GHz and 0.2 - 6 GHz bandwidth respectively with $> 25\%$ PAE. The roll-off in the output power and PAE is attributed to the FET output capacitance of 0.27 pF/mm resulting in an output pole at $\sim$ 10 GHz. Circuits with multi-section LC filters at the output should provide improved PAE at the upper band-edge and were incorporated in later GaN based designs.

Compared to this commercial Darlington resistive feedback amplifiers [5] are available for 13 dBm output power, with 9 dB gain over D.C. - 6 GHz bandwidth in SiGe HBT technology featuring 1 μm emitters and offering 50 GHz f_τ. Higher powers up to 19 dBm at 30% PAE are available, with 13 dB gain and D.C. - 3.5 GHz bandwidth [44] in SiGe HBT technology with 65 GHz f_τ.

Two generations of f_τ-doubler power amplifiers were fabricated in GaN / AlGaN HEMT technology. The process details and the device performance were presented in chapter 4. Details of circuit designs and measurement results are described here.

5.4 First generation GaN HEMT f_τ-doubler power amplifiers

The first generation circuits were designed using a simplified device model shown in fig. 5.15 for a 0.5 μm gate length device. A total device periphery of $W = 2.4$ mm was used to drive up to 1 A current into a 50Ω load, to obtain 6 W output power.

The single gate f_τ-doubler power amplifier (fig. 5.16) uses resistive feed-

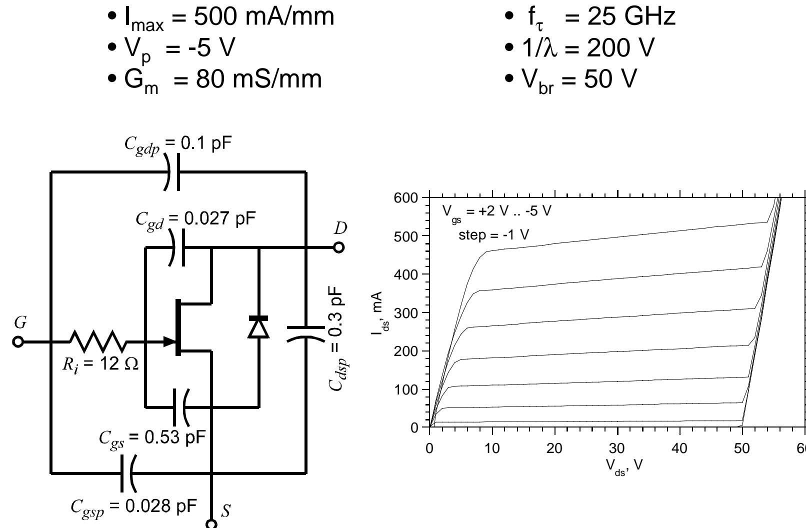

Figure 5.15: Large signal model of a 0.5 μm gate length 1 mm periphery device used for simulations.

back to match the input and output to 50Ω. Versions of this circuit having only the sources of the FETs bonded to AlN were included to minimize C_{ds} and improve efficiency at higher frequencies (chapter 7).

The dual-gate cascode f_τ-doubler power amplifier (fig. 5.17) uses capacitive division [12] to decrease gain and improve bandwidth. This design uses a resistive divider as a lossy input matching network. The divider also provides a low impedance path for the gate bias preventing bias shifts at high RF drive.

Biasing and π-section matching networks were implemented similar to the GaAs MESFET designs. Inductances were implemented using a 90 Ω CPW transmission line at the input and using a 75 Ω line at the output to accomodate the higher current capacity at the output. Transmission lines were designed to carry a peak D.C. current density less than 5 mA/μm^2 to eliminate electro-migration problems. The nichrome resistors were designed for a sheet resistivity of 50 Ω/□ and a peak current density less than 1 mA/μm. Simulations predicted 10 dB gain and 0.2 - 10 GHz bandwidth

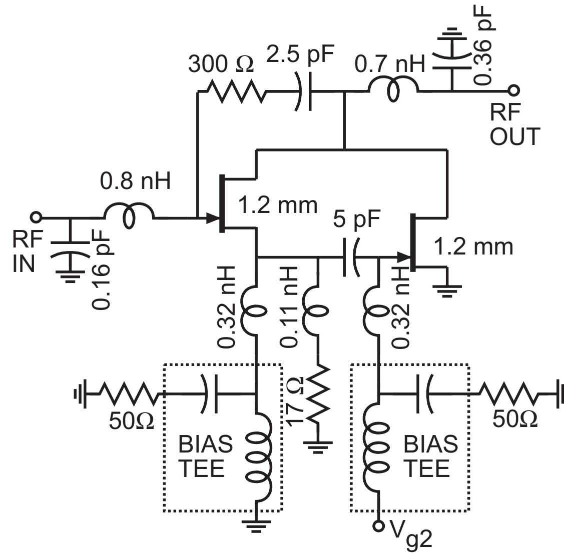

Figure 5.16: Complete schematic of GaN f_τ-doubler resistive feedback power amplifier.

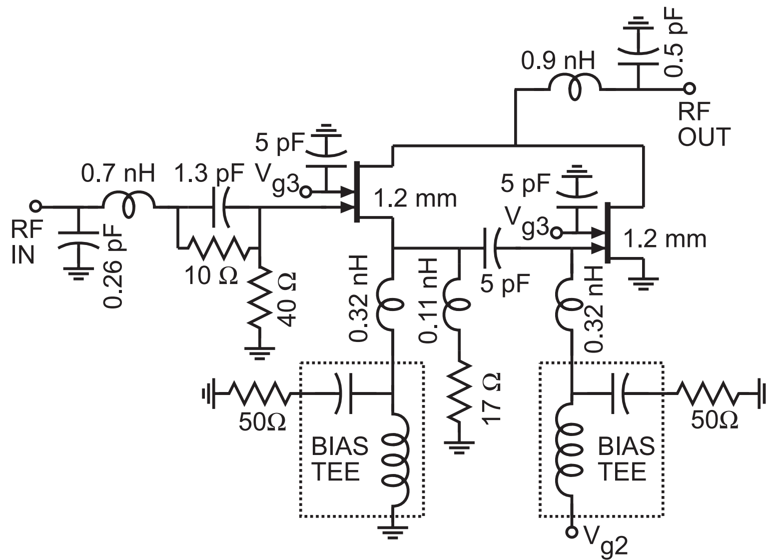

Figure 5.17: Complete schematic of GaN dual-gate cascode f_τ-doubler power amplifier.

for the source only bonded circuits.

The circuit lay-out was done in a CPW wiring environment using air-bridges to shunt ground planes. The GaN die with the bump-bonds provides a second plane of wiring for cross-overs underneath the bonded die. GaN HEMTs with 0.7 - 1 μm gate-length were fabricated on baseline material grown by MOCVD on C-plane sapphire. As was elaborated in chapter 4 the devices were flip-chip bonded to 10 mil thick AlN substrates (fig. 5.18) which has the passive components (NiCr resistors, Si_3N_4 capacitors), CPW interconnects, and provides a low resistance thermal path for efficient heat-sinking. The GaN die (fig. 5.18) size is 1.1 mm $\times$ 1.2 mm for source only bonded circuits and 1.1 mm $\times$ 1.45 mm for the circuits with both source and drain bonds. The AlN die sizes were 4.25 mm $\times$ 3.0 mm for all circuits. The AlN substrates were bonded to a copper block using silver epoxy. The copper block was further mechanically attached to the probe station to provide a good thermal path.

Power measurements were done in a 50Ω system (fig. 5.19) without any external tuning. The input network consists of a synthesizer, directional coupler and a bias tee. The directional coupler was used to determine the input power to the amplifier. An amplifier was included at the input when higher input drives were required in the second generation circuits. The output network consists of a bias tee, attenuators, directional coupler and power meter. The directional coupler was connected to a spectrum analyzer to detect the presence of any oscillations and harmonic content in the output. Losses in the external networks were calibrated to measure the output power accurately. Additional bias tees were used to individually bias the two devices for maximum output power. The synthesizer, power meters and ammeters were controlled using a PC interface which sweeps the input power and frequency and records the output power and D.C. bias currents. Two port small signal measurements were done using HP8510B network analyzer.

Measured small signal scattering parameters of the resistive feedback power amplifiers (fig. 5.20) shows $\sim$11 dB small-signal gain with 0.2 - 7.5 GHz bandwidth. The amplifier provides $>$ 1 W output power over 1 - 7.5 GHz with $>$ 12% PAE (fig. 5.21). At 6 GHz the peak output power and peak PAE are 1.8 W and 22.5% respectively (fig. 5.22).

The dual-gate cascode power amplifier provide $\sim$11 dB small-signal gain with 0.2 - 7 GHz bandwidth (fig. 5.23) and $>$ 1 W output power over 1 -

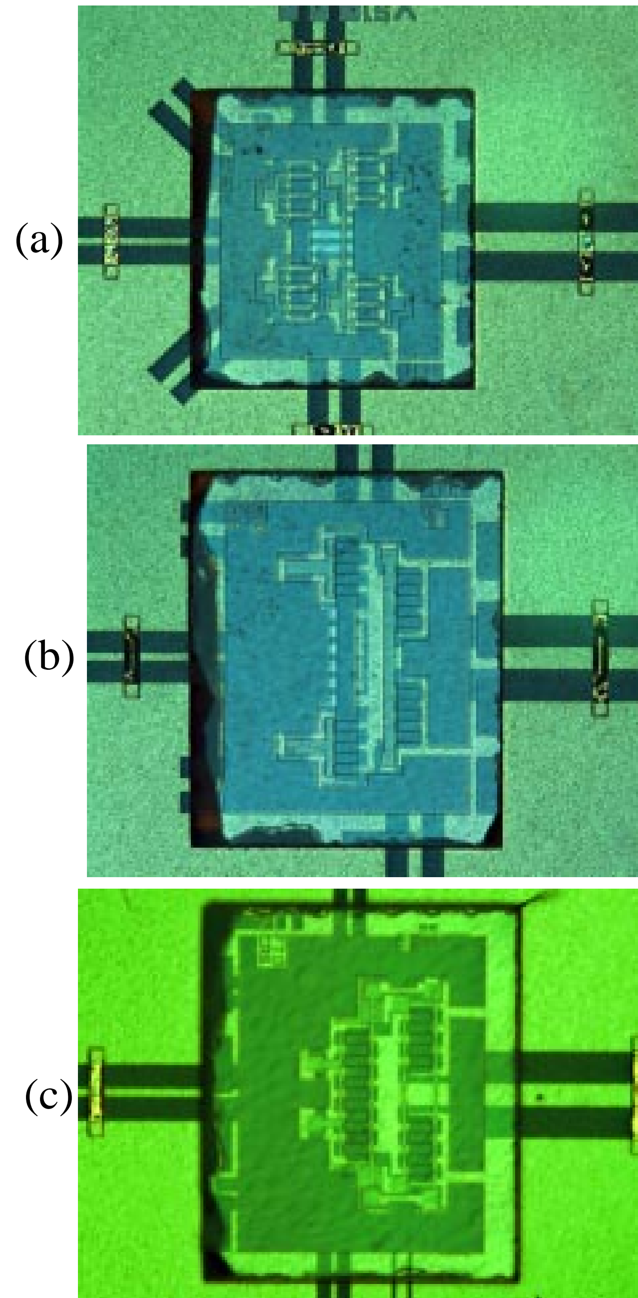

Figure 5.18: Die photograph of GaN (a) f_τ-doubler resistive feedback power amplifier with source bonds only (b) f_τ-doubler resistive feedback power amplifier with source and drain bonds and (c) dual - gate cascode f_τ-doubler power amplifier.

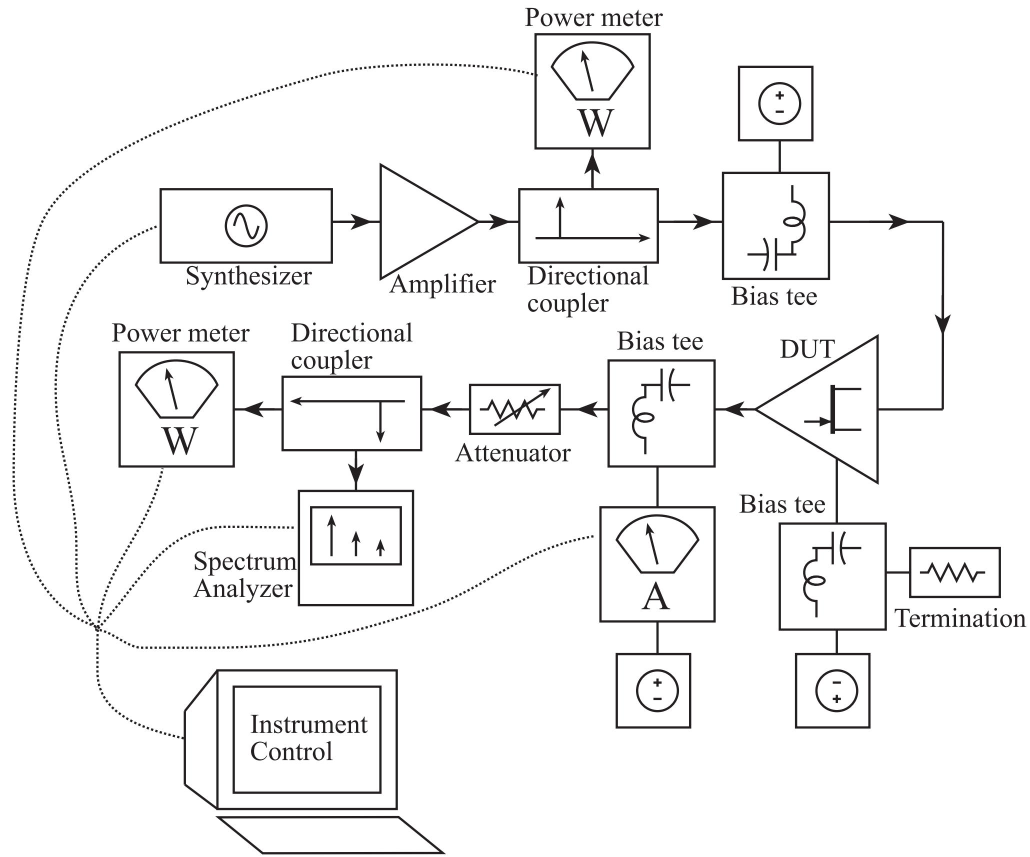

Figure 5.19: Schematic of the test setup used for power measurements.

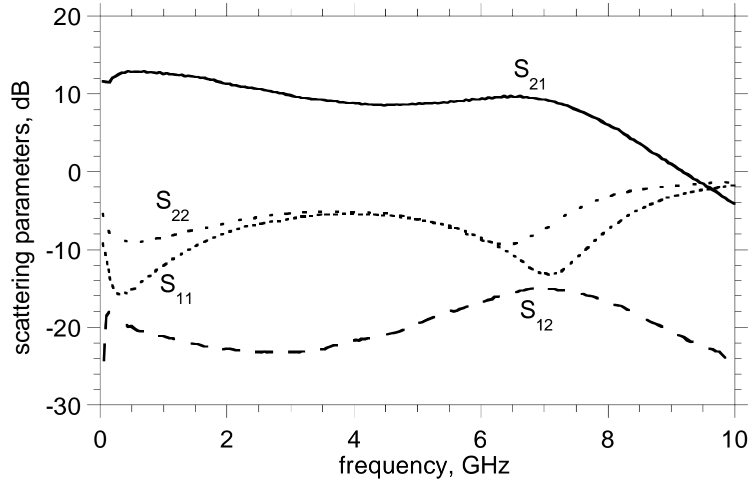

Figure 5.20: Small-signal performance of GaN f_τ-doubler resistive feedback power amplifier.

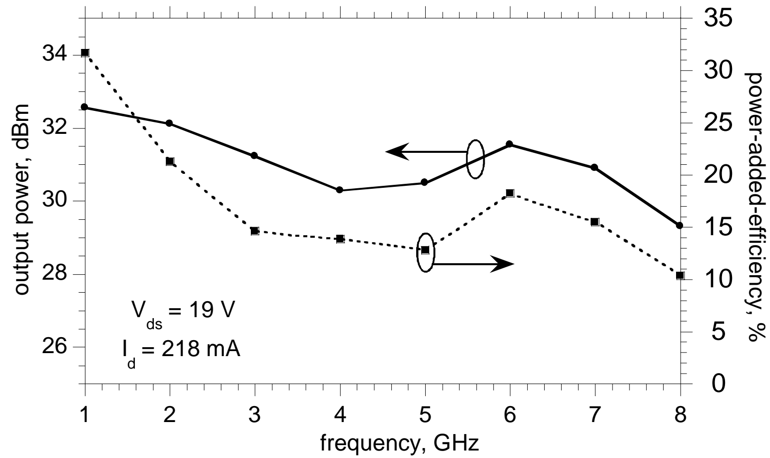

Figure 5.21: Power performance of GaN f_τ-doubler resistive feedback power amplifier from 1 - 8 GHz with 25 dBm available power at input.

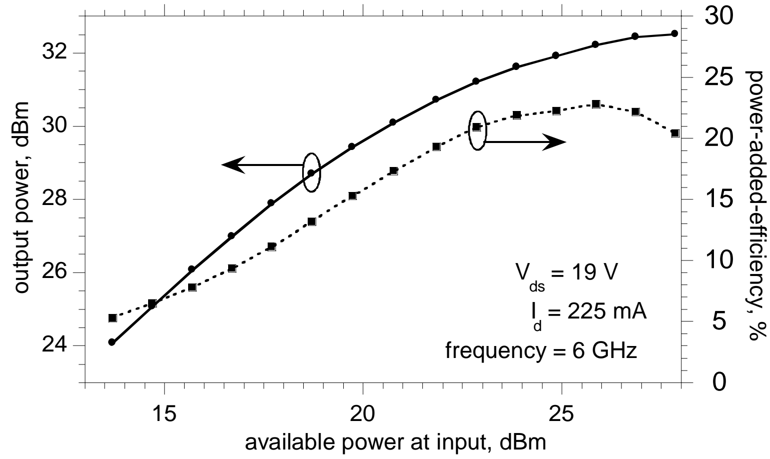

Figure 5.22: Power performance of GaN f_T-doubler resistive feedback power amplifier at 6 GHz.

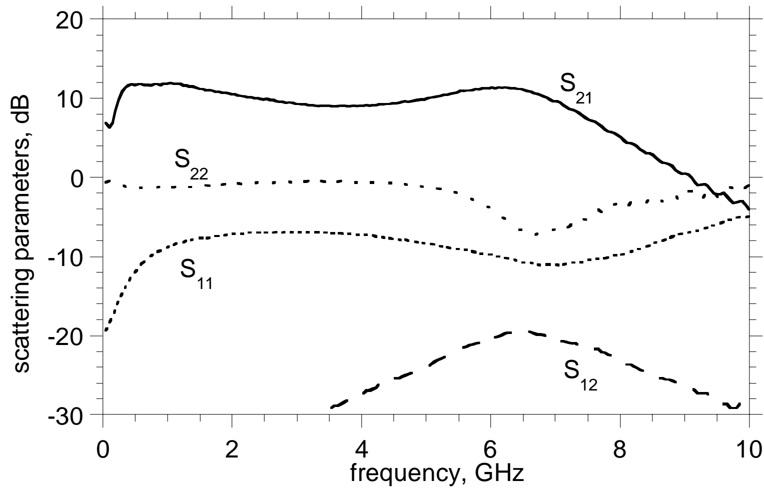

Figure 5.23: Small-signal performance of GaN dual-gate cascode f_T-doubler power amplifier.

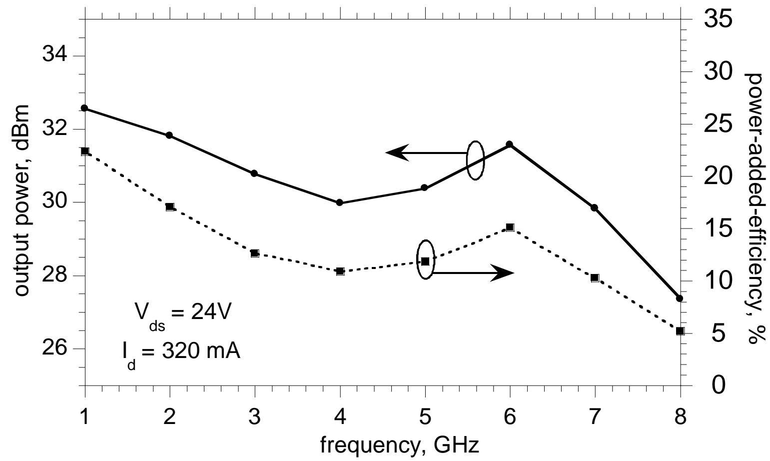

Figure 5.24: Power performance of GaN dual-gate cascode f_τ-doubler power amplifier from 1 - 8 GHz.

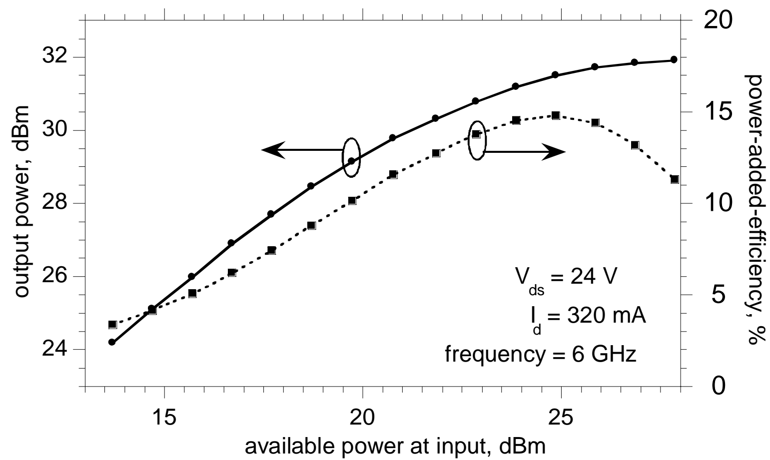

Figure 5.25: Power performance of GaN dual-gate cascode f_τ-doubler power amplifier at 6 GHz.

7.0 GHz with > 10% PAE (fig. 5.24). At 6 GHz the peak output power and peak PAE are 1.5 W and 15% respectively (fig. 5.25).

The bandwidth, matching, output power and PAE obtained were poorer than what was predicted from simulations. This is attributed to various processing and device issues detailed earlier in chapter 4 and summarized here :

- strong D.C. to RF dispersion observed for the GaN HEMTs (wafer #981216FD) severely degrades the RF output power and efficiency expected from the circuits.

- substantial leakage currents at high voltages (chapter 4, page 4.12) prevents complete cut-off of the channel at high voltages, decreasing the allowed RF current swing.

- to have good yield of large periphery devices, gate lengths of 0.75 μm were obtained on wafer compared to 0.5μm mask dimension. This leads to a larger C_{gs}) and smaller f_τ (15 GHz instead of 25 GHz), decreasing the bandwidth.

- larger C_{gd} (0.15 pF/mm instead of 0.1 pF/mm) than estimated during design decreases bandwidth further and also affects the matching.

- larger capacitance per unit area for the deposited Si_3N_4 than what was estimated resulted in the broadband matching sections at the input and output being mistuned.

This difference between the measured and simulated performance was more severe for the source only bonded circuits, which exhibited a gradual roll-off in gain starting from 1 GHz. Simulations were repeated with extracted data for the devices and passives and compared with the measured results. A comparison of the S-parameter data for the f_τ-doubler resistive feedback power amplifier with source bonds only (fig. 5.26, 5.27) shows a close correlation.

To verify the presence of D.C. to RF dispersion in the devices and to verify if the device is operating along the optimum loadline, voltage waveform measurements were performed. Measurements were done at 2 GHz in order to preserve the harmonic content of the waveform, so that saturation could be observed. Also the effects of output capacitance could be

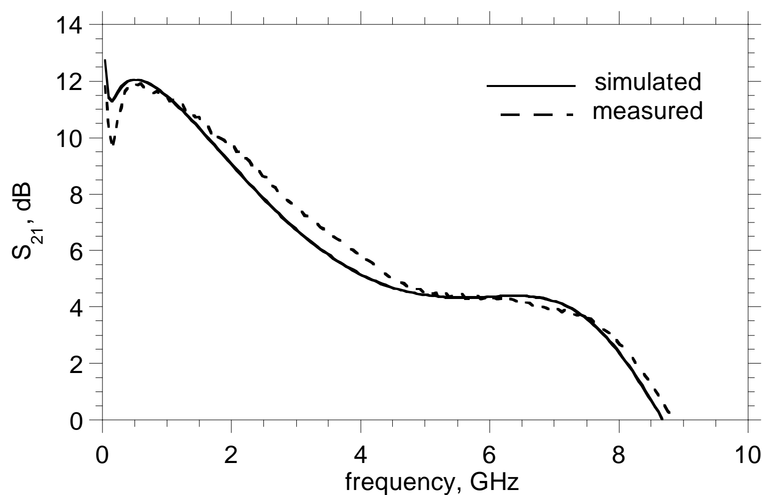

Figure 5.26: Comparison of simulated and measured S_{21} for the GaN f_τ-doubler resistive feedback power amplifier with source bonds only.

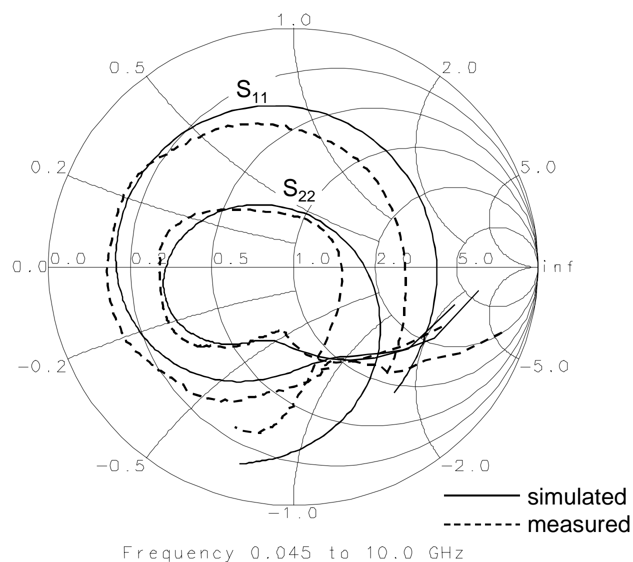

Figure 5.27: Comparison of simulated and measured S_{11} and S_{22} for the GaN f_τ-doubler resistive feedback power amplifier with source bonds only.

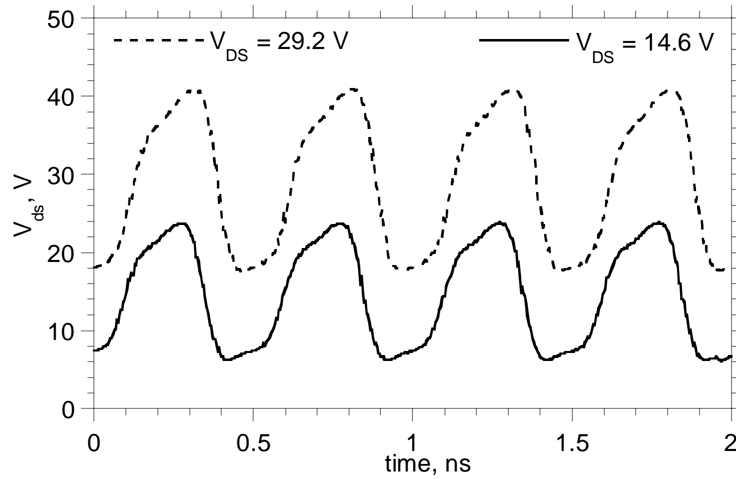

Figure 5.28: Reconstructed voltage waveform across the devices in a GaN f_T-doubler resistive feedback power amplifier for various drain bias voltages.

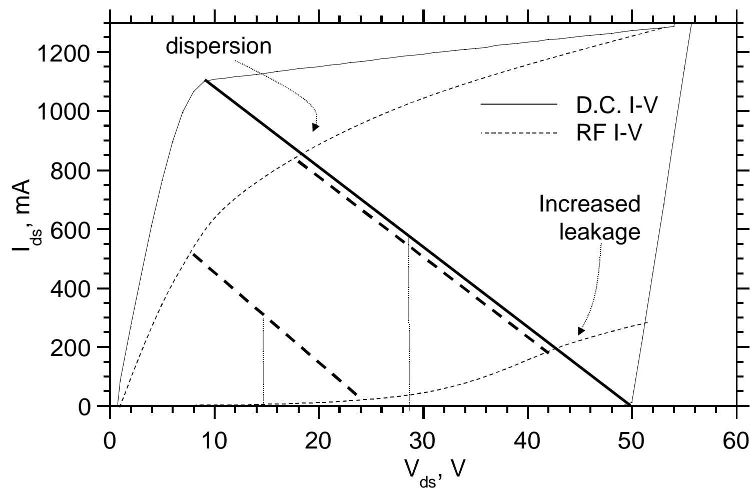

Figure 5.29: Reconstructed RF I-V for the device shows severe D.C. to RF dispersion and leakage current limiting the peak output power.

neglected at these frequencies. Since the loadline is fixed and nearly linear, knowing the bias voltage and the RF voltage saturation limits, we could reconstruct the voltage across the device (fig. 5.28). This is done by increasing the input drive at each bias till the voltage starts saturating. The reconstructed voltages now represent the peak swings limited by device pinch-off (or breakdown) at one extreme and the saturation current (or device linear region) at the other extreme. Repeating this procedure at varying drain bias we could reconstruct the device RF I-V (fig. 5.29) curves corresponding to saturation and pinch-off. The measured peak output power of 1.5 W correlates with what is expected from the RF I-V curve.

5.5 Second generation GaN HEMT f_τ-doubler power amplifiers

The final simulations of the second generation circuits were performed using a more realistic large periphery device model shown in fig. 5.30 for a 0.5 μm gate length dual gate device. The circuits were designed for a 25 Ω load to make use of the larger currents available from the devices, and to operate them at lower voltages. So a broadband impedance transformation from 50 to 25 Ω was done at the output using four quarter-wave line sections. Also with the lower f_τ, larger G_m and considerably larger C_{gs} observed in the earlier process runs, similar impedance transformation was required at the input to improve the upper cut-off frequency.

Dual-gate cascode resistive feedback f_τ-doubler power amplifier (fig. 5.31) were designed for 10 dB gain, 2 - 9 GHz bandwidth and 6 W output power (fig. 5.32) Biasing and π-section matching networks were implemented similar to the earlier designs.

The circuits were layed out, processed and bonded similar to the earlier run. The GaN and AlN die sizes are 1.4 mm × 1.4 mm and 7.25 mm × 2.2 mm respectively (fig. 5.33). The gate lengths were close to 0.75 μm due to lithographic limitations. Power measurements were performed after optimizing the bias for peak output power. Measured output power is $>$ 3 W over 2 - 8 GHz with 25 dBm (0.32 W) available power at the input (fig. 5.34). Saturated output power is $>$ 4.4 W over 2 - 8 GHz (fig. 5.35). At 6 GHz the peak output power and peak PAE are 5.12 W and 21 % respectively with 12 dB small signal gain (fig. 5.36).

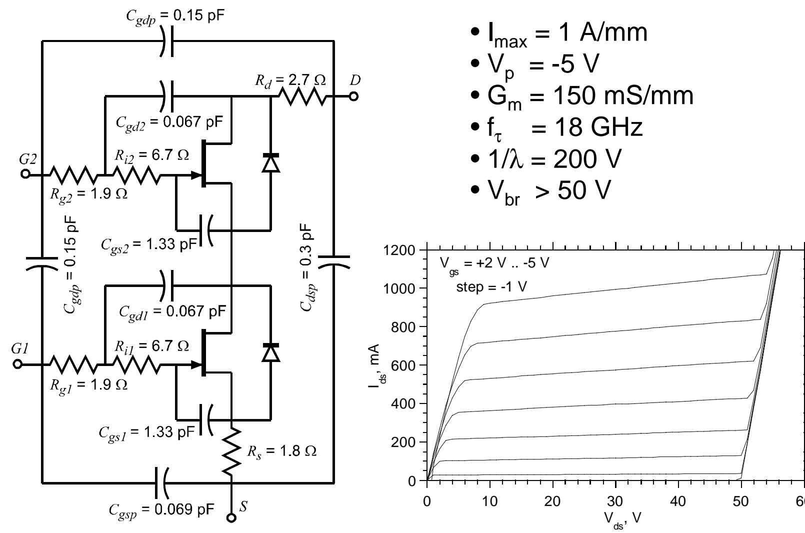

Figure 5.30: Large signal model of a 0.5 μm gate length 1 mm periphery dual-gate device used for simulations.

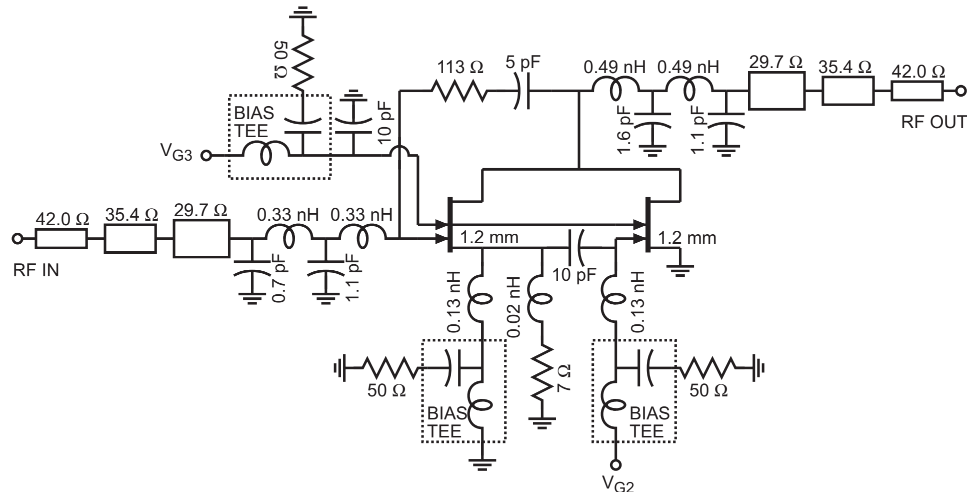

Figure 5.31: Complete schematic of GaN dual-gate cascode f_τ-doubler resistive feedback power amplifier.

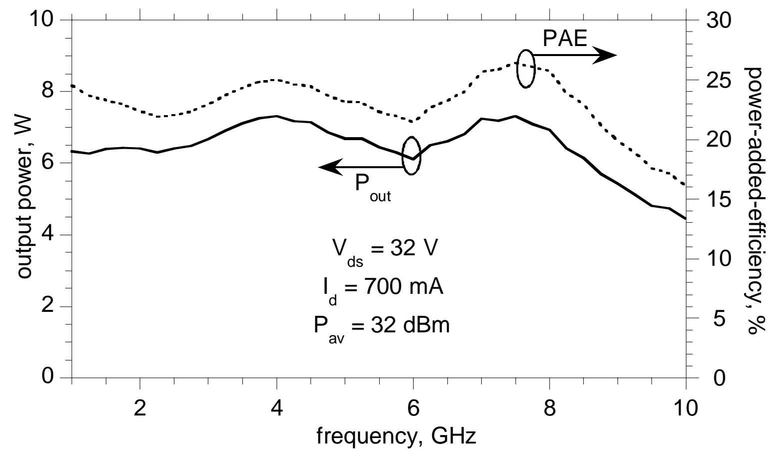

Figure 5.32: Simulated performance of GaN dual-gate cascode f_T-doubler resistive feedback power amplifier from 1 - 10 GHz.

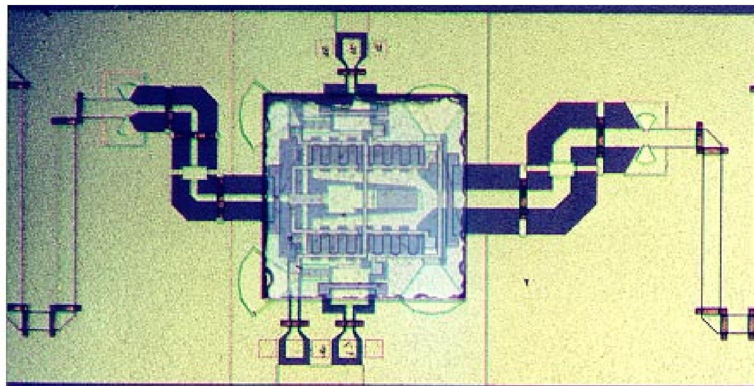

Figure 5.33: Die photograph of GaN dual-gate cascode f_T-doubler resistive feedback power amplifier.

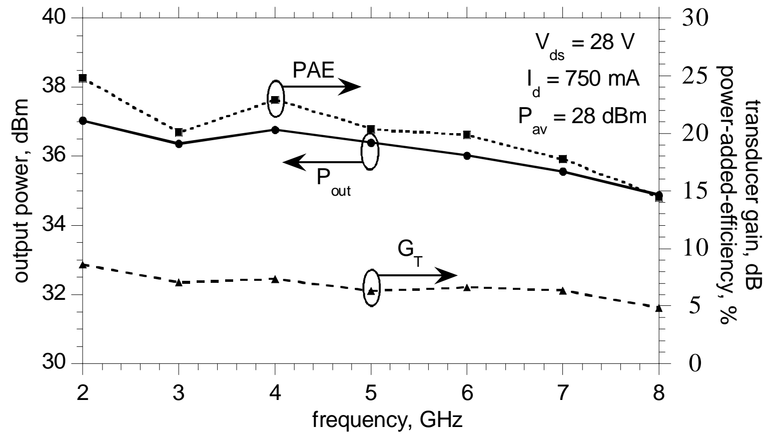

Figure 5.34: Power performance of GaN dual-gate cascode f_τ-doubler resistive feedback power amplifier from 2 - 8 GHz (P_{av} = 28dBm).

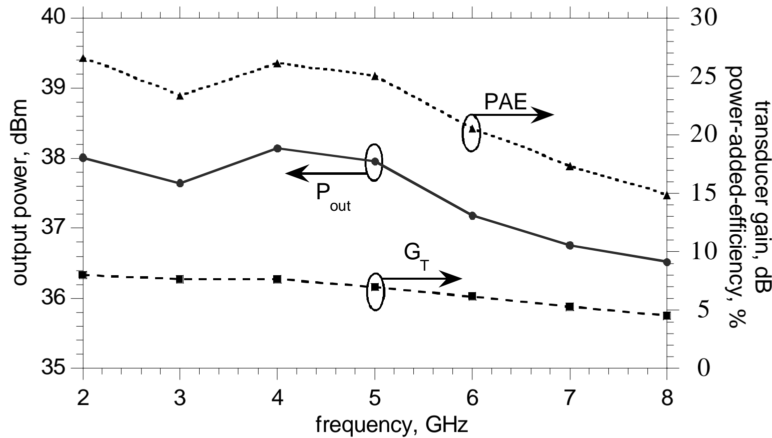

Figure 5.35: Saturated power performance of GaN dual-gate cascode f_τ-doubler resistive feedback power amplifier from 2 - 8 GHz.

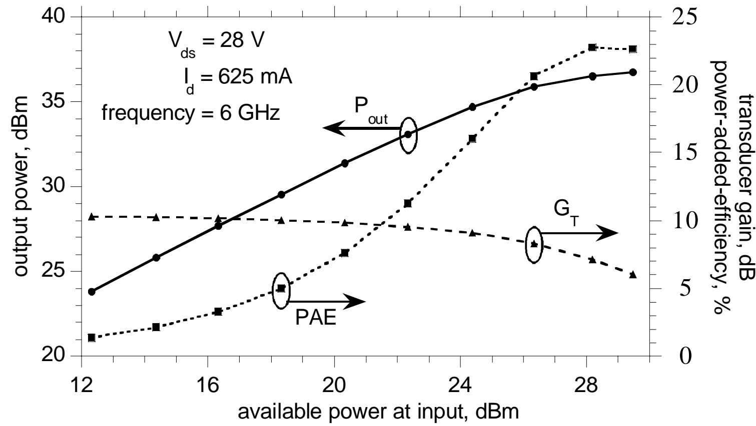

Figure 5.36: Power performance of GaN dual-gate cascode f_T-doubler resistive feedback power amplifier at 6 GHz.

Thus the f_T-doubler topology is an alternative to the distributed amplifiers in realizing wide-band power amplifiers in a smaller die area. Experimental circuits in a GaAs MESFET technology offering 18 GHz f_T and 12 V breakdown, has achieved 0.2 - 6 GHz bandwidth, $\sim$ 12 dB gain, $>$ 23 dBm output power and 25% power-added-efficiency. The bandwidth is 33% of f_T and the gain-bandwidth product is 1.3 $\cdot f_T$. Two generations of circuits were fabricated using GaN / AlGaN HEMTs technology offering a typical f_T of 15 GHz and peak voltage operation up to 50 V. Output power $>$ 37 dBm and bandwidth up to 8 GHz were achieved with 10 dB gain. The efficiency at higher frequencies can be improved further by using improved broadband output networks.

Chapter 6

Cascode-delay-matched distributed power amplifiers

DISTRIBUTED circuits have been traditionally used in wide range of applications like traveling wave amplifiers [45, 46, 47], microwave traveling wave tubes [48], traveling wave photodetectors [49], traveling wave electrooptic modulators [50], nonlinear transmission line based sampling circuits [51], paraphase amplifiers [52] and level-shifters [53]. This chapter discusses the application of distributed circuits in microwave power amplification to provide broadband, high power, high efficiency amplifiers. The basic design equations for a conventional reverse terminated distributed power amplifier is presented first. Disadvantages of this topology in power amplifiers and suggested solutions are discussed next. Cascode-delay-matched traveling-wave power amplifiers (CDMTWA) are introduced which overcomes most of the problems including poor efficiency, uneven drive, and MMIC realizability. Results from GaAs MESFET scale model hybrid and GaAs MESFET / GaN HEMT CDMTWA are presented.

6.1 Distributed power amplifiers

Distributed or traveling-wave amplifier (TWA) (fig. 6.1(a)) is a broadband circuit whose gain-bandwidth product is limited by f_{max} [54, 22]. In chapter 3 (page 36) the basic operation of a distributed amplifier was explained. Here design equations for a distributed power amplifier are derived.

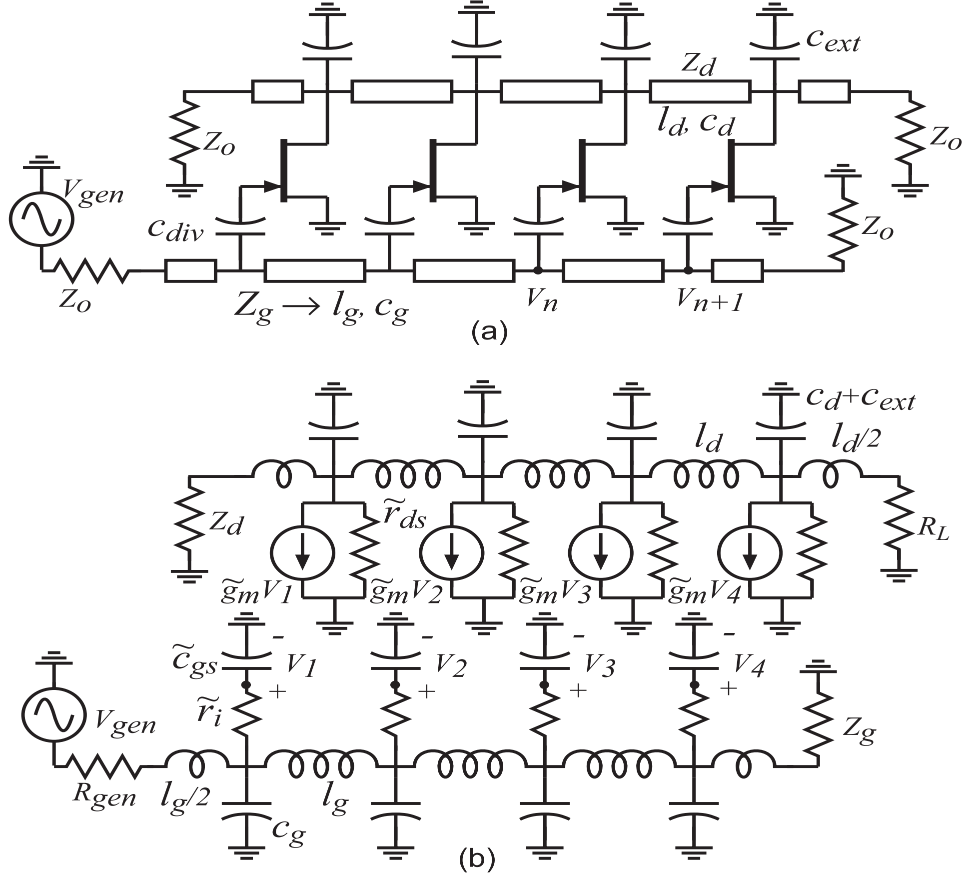

Figure 6.1: (a) A.C. circuit schematic and (b) equivalent circuit model of a TWA.

6.1.1 Distributed power amplifier design equations

The total device periphery (W) in a power TWA is chosen to meet the loadline criterion given by

$$I_{DSS} = \frac{2(V_{br} - V_k)}{Z_o} \ , \tag{6.1}$$

for a doubly terminated drain line (fig. 6.1(a)). Using the simplified A.C. model of fig. 3.1 (page 26) for the transistor, the individual devices in a TWA with N cells will have a periphery $w = W/N$, a transconductance $g_m = G_m/N$, a gate capacitance $c_{gs} = C_{gs}/N$, a gate resistance $r_i = NR_i$

and an output resistance $r_{ds} = NR_{ds}$.

As in the case of the common source power amplifier of chapter 3 (page 27), capacitive or resistive degeneration is essential to obtain additional degree of freedom in designing for a specified gain and bandwidth. Adding a external series capacitance of $c_{div} = C_{div}/N$ to each gate input would increase the bandwidth by a factor $1/M \equiv 1 + (C_{gs}/C_{div})$ and decrease the voltage gain by the same factor. A resistive degeneration of $r_s = NR_s$ in parallel with $c_s = C_{gs}/NR_sG_m$ added to each source would increase the bandwidth by a factor $1/M = (1 + G_mR_s)$ and decrease the gain by the same factor. The equivalent circuit element values shown in fig. 6.1(b) and used in rest of the analysis refers to the degenerated elemental values as given by,

$$\begin{aligned}
\tilde{g}_m &= \frac{\tilde{G}_m}{N} = \frac{M}{N} G_m \ , \\
\tilde{c}_{gs} &= \frac{\tilde{C}_{gs}}{N} = \frac{M}{N} C_{gs} \ , \\
\tilde{r}_i &= N\tilde{R}_i = NR_i \ , \\
\tilde{r}_{ds} &= N\tilde{R}_{ds} = NR_{ds} \ , \\
&\quad \text{(capacitive degeneration)} \\
&= N\tilde{R}_{ds} = \frac{N}{M} R_{ds} \ , \\
&\quad \text{(resistive degeneration)} \ . \qquad (6.2)
\end{aligned}$$

To determine the bandwidth of the TWA, delays in the gate and drain transmission line must be included in the analysis. Wave propagation in a synthetic line with series inductance l and shunt capacitance c can be expressed as,

$$\begin{aligned}
V_{n+1} &= V_n e^{-(\alpha + j\beta)} \ , \\
\cosh(\alpha + j\beta) &= 1 + \frac{\omega^2 lc}{2} \ , \qquad (6.3)
\end{aligned}$$

where α is the attenuation per line section and β is the phase constant. The synthetic line is characterized by a cut-off frequency (called Bragg frequency), which for a lossless line ($\alpha = 0$) is,

$$f_{Bragg} = \frac{1}{\pi\sqrt{lc}} \ . \qquad (6.4)$$

At frequencies well below, f_{Bragg}, the lossless line has a characteristic impedance of $\sqrt{l/c}$ and delay per section of $\sqrt{lc}$.

In a TWA periodic loading of the gate transmission line (fig. 6.1(b)) of impedance $Z_g = \sqrt{l_g c_g}$, by the transistors' input impedances forms a synthetic gate transmission line with Bragg frequency

$$f_{Bragg,g} = \frac{1}{\pi\sqrt{l_g(c_g + \tilde{c}_{gs})}} \ . \tag{6.5}$$

For frequencies $f \ll f_{Bragg,g}$ the synthetic line is matched to Z_o and the characteristic impedance and loaded phase delay per line section are given by,

$$\begin{aligned} Z_o &= \sqrt{l_g/(c_g + \tilde{c}_{gs})} \ , \\ \tau_g &= \sqrt{l_g(c_g + \tilde{c}_{gs})} \ , \end{aligned} \tag{6.6}$$

respectively. The gate resistance $\tilde{r}_i$ in series with $\tilde{c}_{gs}$ introduces a frequency dependent attenuation per line section of

$$\alpha_g = 4\pi^2 f^2 \tilde{c}_{gs}^2 \tilde{r}_i Z_o/2 \ , \tag{6.7}$$

for $f \ll f_{Bragg,g}$.

Similarly periodic loading of the drain transmission line of impedance $Z_d = \sqrt{l_d c_d}$, by the transistors' output impedances and the external capacitance c_{ext}, forms a synthetic drain transmission line with Bragg frequency

$$f_{Bragg,d} = \frac{1}{\pi\sqrt{l_d(c_d + c_{ext})}} \ . \tag{6.8}$$

For frequencies $f \ll f_{Bragg,d}$ the drain line is matched to Z_o and the characteristic impedance and loaded phase delay per line section are given by,

$$\begin{aligned} Z_o &= \sqrt{l_d/(c_d + c_{ext})} \ , \\ \tau_d &= \sqrt{l_d(c_d + c_{ext})} \ , \end{aligned} \tag{6.9}$$

respectively. The periodic shunt loading of the drain line due to the transistors output conductance introduces an attenuation per line section of

$$\alpha_d = Z_o/2\tilde{r}_{ds} \ . \tag{6.10}$$

The amplifier gain is calculated by adding the contribution from each (n^{th}) transistor in the TWA. For a TWA with N transistors, the gain is,

$$\frac{V_{out}}{V_{in}} = \left(\frac{-\tilde{g}_m Z_o}{2}\right) \times \sum_{n=1}^{N} e^{[-(n-1/2)(\alpha_g+j\beta_g)-(N-n+1/2)(\alpha_d+j\beta_d)]} . \tag{6.11}$$

At low frequencies where the transmission line delays are small, the TWA is equivalent to the common source power amplifier of chapter 3 (page 27) but with a dummy termination at the output. The low frequency voltage gain and transducer power gain are fixed and given by,

$$\begin{aligned} |S_{21}| &= \frac{N\tilde{g}_m Z_o}{2} = M\frac{G_m Z_o}{2} , \\ G_T &= \left(\frac{MG_m Z_o}{2}\right)^2 = M^2\left(\frac{V_{br}-V_k}{V_p}\right)^2 , \end{aligned} \tag{6.12}$$

respectively. Thus for a given net periphery, gain is independent of the number of cells and could be varied only by degeneration.

Limitations on the TWA bandwidth arise due to several reasons enumerated below:

- delay mismatch between the gate and drain lines ($\Delta\tau = \tau_g - \tau_d$) : The limitation due to the delay mismatch is analyzed by setting the losses to zero ($\alpha_g = \alpha_d = 0$). The gain expression (eq. 6.11) then simplifies to,

$$\begin{aligned} \left\|\frac{V_{out}}{V_{in}}\right\| &= \left(\frac{\tilde{g}_m Z_o}{2}\right) \times \left\|\sum_{n=1}^{N} e^{[-j(n-1)2\pi f\Delta\tau]}\right\| \\ &= \left(\frac{\tilde{g}_m Z_o}{2}\right) \times \left\|\frac{1-e^{-j2\pi fN\Delta\tau}}{1-e^{-j2\pi f\Delta\tau}}\right\| \\ &= \left(\frac{\tilde{g}_m Z_o}{2}\right) \times \left\|\frac{e^{j\pi fN\Delta\tau}-e^{-j\pi fN\Delta\tau}}{e^{j\pi f\Delta\tau}-e^{-j\pi f\Delta\tau}}\right\| \\ &= \left(\frac{\tilde{g}_m Z_o}{2}\right) \times \left[\frac{\sin(\pi fN\Delta\tau)}{\sin(\pi f\Delta\tau)}\right] \\ &\simeq \left(\frac{N\tilde{g}_m Z_o}{2}\right) \times \left[1-\frac{(N2\pi f\Delta\tau)^2}{24}\right] , \end{aligned} \tag{6.13}$$

  where higher order terms of $f\Delta\tau$ are ignored in the last approximation. The gain decreases at high frequencies ($N2\pi f\Delta\tau \sim 1$) because

the transistor outputs do not add in phase. So it is essential to design the gate and drain lines with $\Delta\tau = 0$ or $\tau_g = \tau_d$ to eliminate the bandwidth limits arising from delay mismatch. This is done by selecting $Z_d = Z_g$ and $c_{ext} = \tilde{c}_{gs}$. For strong coupling between two propagating waves the phase mismatch $\Delta\theta$ must be small at all frequencies of interest, or $\Delta\theta = N2\pi f\Delta\tau < \pi$.

- gate-line attenuation : The input voltage of the Nth transistor is attenuated by $e^{-(N-1/2)\alpha_g}$. To keep the loss in the gate drive of the Nth transistor within 1 dB we require,

$$\begin{aligned} N\alpha_g &\equiv N \cdot 4\pi^2 f_{high}^2 \tilde{c}_{gs}^2 \tilde{r}_i Z_o/2 \leq 1/8 \ , \\ f_{high} &\simeq \frac{1}{M}\frac{1}{4\pi C_{gs}\sqrt{R_i Z_o}} \ . \end{aligned} \tag{6.14}$$

Thus for a given net periphery, the gate line attenuation limited bandwidth is independent of the number of cells and could be varied only by degeneration.

- drain-line attenuation: The output of the first transistor is attenuated by $e^{-(N-1/2)\alpha_d}$ before it reaches the output. To keep the attenuation in the drain line within 1 dB we require,

$$\begin{aligned} N\alpha_d &\equiv \frac{Z_o}{2\tilde{r}_{ds}} \leq 1/8 \ , \\ \frac{Z_o}{R_{ds}} &\leq 1/4 \ , \text{(capacitive degeneration)} \\ M\frac{Z_o}{R_{ds}} &\leq 1/4 \ , \text{(resistive degeneration)} \ . \end{aligned} \tag{6.15}$$

Thus for a given net periphery, the drain line attenuation is independent of the number of cells. This is where resistive degeneration is advantageous compared to capacitive division as it decreases the drain line losses. Also dual-gate or cascode (common source - common gate) devices can significantly decrease the output conductance and minimize the drain line losses [55, 56].

- gate and drain line Bragg frequencies : The TWA gain drops rapidly for $f > f_{Bragg,g}$ or $f > f_{Bragg,d}$. Selecting $\tau_g = \tau_d$, and $Z_d = Z_g \simeq$

$\sqrt{l_g/\tilde{c}_{gs}}$, the gate and drain Bragg frequencies are given by,

$$f_{Bragg,g} = f_{Bragg,d} \simeq \frac{2}{\pi Z_o \tilde{c}_{gs}} \equiv \frac{N}{M} \frac{2}{\pi Z_o C_{gs}} \ . \tag{6.16}$$

Thus the Bragg frequencies can be increased arbitrarily by using a large number cells or by using larger degeneration.

Combining eq. 6.12 and 6.14 , the TWA large signal gain-bandwidth product could be determined to be,

$$|S_{21}| f_{high} = \left(\frac{M G_m Z_o}{2}\right) \left(\frac{1}{4\pi M C_{gs} \sqrt{R_i Z_o}}\right) = \frac{f_\tau}{4\sqrt{R_i/Z_o}} \ . \tag{6.17}$$

6.1.2 Distributed power amplifier design procedure

The design procedure for power TWA are different from small signal TWA [57, 58]. The design equations for a power TWA are first summarized below (for the case $\tau_g = \tau_d$ and $Z_d = Z_g$) :

$$\begin{aligned}
I_{DSS} &= \frac{2(V_{br} - V_k)}{Z_o} \ , \\
|S_{21}| &= M \frac{G_m Z_o}{2} \ , \\
G_T &= M^2 \left(\frac{V_{br} - V_k}{V_p}\right)^2 \ , \\
f_{high} &\simeq \frac{1}{M} \frac{1}{4\pi C_{gs} \sqrt{R_i Z_o}} \ , \\
f_{Bragg,g} = f_{Bragg,d} &= \frac{N}{M} \frac{2}{\pi Z_o C_{gs}} \ , \\
\frac{Z_o}{R_{ds}} &\leq 1/4 \ , \text{(capacitive degeneration)} \ , \\
M \frac{Z_o}{R_{ds}} &\leq 1/4 \ , \text{(resistive degeneration)} \ .
\end{aligned} \tag{6.18}$$

The net device periphery is first chosen based on the loadline constraint. As seen from the above design equations the number of cells changes only the Bragg frequency. Assuming no degeneration ($M = 1$), N is chosen so that

the Bragg frequency is a little larger than the gate line cut-off frequency f_{high}. Degeneration ratio (M) is chosen to trade off gain for bandwidth. The type of degeneration is decided based on how dominant the drain line losses are, the lower cut-off frequency specification. Dual-gate or cascode cells might be required if the drain line attenuation is significant.

6.1.2 f_τ-multiplier cells in distributed power amplifiers

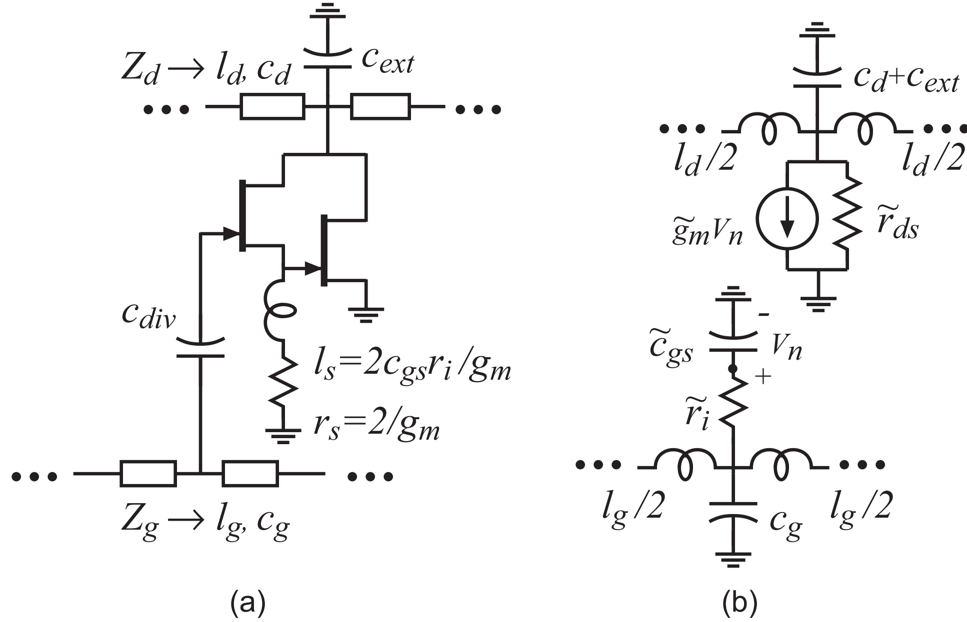

Figure 6.2: (a) A.C. circuit schematic and (b) equivalent circuit model of a TWA with f_τ-doubler cells.

If each cell of the TWA is replaced by a f_τ-multiplier consisting of P devices, each of periphery w/P then the equivalent device elements are given by,

$$\begin{aligned}
\tilde{g}_m &= \frac{\tilde{G}_m}{N} = \frac{M}{NP} G_m \ , \\
\tilde{c}_{gs} &= \frac{\tilde{C}_{gs}}{N} = \frac{M}{NP^2} C_{gs} \ , \\
\tilde{r}_i &= N\tilde{R}_i = NP^2 R_i \ ,
\end{aligned}$$

$$\begin{aligned}\tilde{r}_{ds} &= N\tilde{R}_{ds} = NR_{ds} \text{ , (capacitive degeneration)} \\ &= N\tilde{R}_{ds} = \frac{N}{M}R_{ds} \text{ , (resistive degeneration) .} \end{aligned} \quad (6.19)$$

Substituting these back in the design equations eq. 6.12, 6.14, 6.16 and 6.15, we get a new set of design equations for a distributed power amplifier with f_τ-multiplier cells (for the case $\tau_g = \tau_d$ and $Z_d = Z_g$) :

$$\begin{aligned} I_{DSS} &= \frac{2(V_{br} - V_k)}{Z_o} \text{ ,} \\ |S_{21}| &= \frac{M}{P}\frac{G_m Z_o}{2} \text{ ,} \\ G_T &= \left(\frac{M}{P}\right)^2 \left(\frac{V_{br} - V_k}{V_p}\right)^2 \text{ ,} \\ f_{high} &\simeq \frac{P}{M}\frac{1}{4\pi C_{gs}\sqrt{R_i Z_o}} \text{ ,} \\ f_{Bragg,g} = f_{Bragg,d} &= \frac{NP^2}{M}\frac{2}{\pi Z_o C_{gs}} \text{ ,} \\ \frac{Z_o}{R_{ds}} &\leq 1/4 \text{ , (capacitive degeneration) ,} \\ M\frac{Z_o}{R_{ds}} &\leq 1/4 \text{ , (resistive degeneration) ,} \\ |S_{21}|f_{high} &= \frac{f_\tau}{4\sqrt{R_i/Z_o}} \text{ .} \end{aligned} \quad (6.20)$$

Thus the f_τ-multiplier cells improves the gate line attenuation limited bandwidth at the cost of gain without any change in the drain line losses or gain-bandwidth product. This trade off is identical to what could be achieved using degeneration. Though the f_τ-multiplier increases the Bragg frequency by a factor of P^2, it could have been achieved by increasing the number of cells. For example, a f_τ-doubler power TWA $(M = 1, P = 2, N)$ would have similar performance as a capacitive division power TWA using 50% capacitive division and twice the number of cells $(M = 0.5, P = 1, 2N)$.

6.1.3 Device loadline in distributed power amplifiers

To obtain the maximum output power from a TWA it is essential that each device sees the optimum loadline at its output and an equal input drive

over the entire bandwidth. However it was seen that the drive levels at the gate of each device is different at high frequencies because of the frequency dependent gate line attenuation. This leads to the device farther away from the input not operating at its peak output when the first device is optimally driven. So there is a drop in efficiency at the higher frequency end. This loss in efficiency could be improved by using one of the following three techniques :

1. capacitive tapering along the gate line [12] : By suitably tapering the capacitive division value along the gate line the drive levels at each gate could be equalized at one frequency. This is usually done at the highest frequency of interest (where the mismatch is maximum) for the best performance. Varying capacitive degeneration however leads to phase differences for the signals passing through the different FET's. Phase correction should be done by using corresponding line lengths in the drain section. (fig. 6.3)

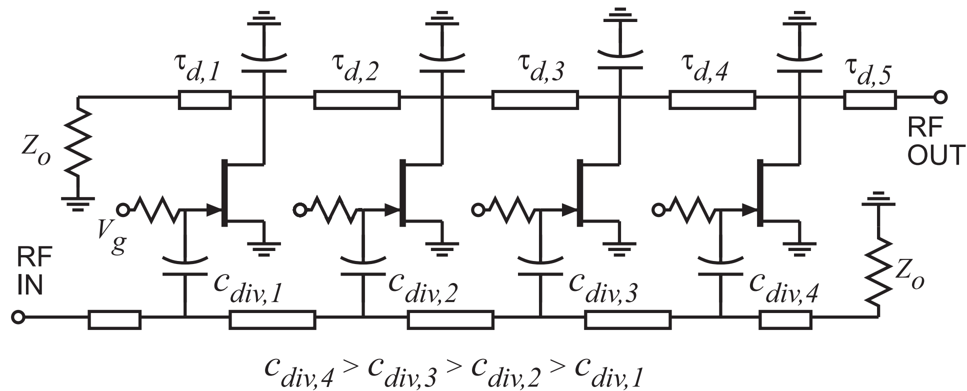

Figure 6.3: A.C. circuit schematic of a TWA using capacitive degeneration.

2. gate line tapering [59] : By suitably tapering the gate line so that each line section is matched to the impedance of the loaded lossy line. Again the drives could be equalized at one frequency only. As in the earlier case phase correction in the drain line is essential. (fig. 6.4)

3. independent biasing of stages : The stages could be A.C. coupled with each stage individually biased at its optimum bias point corresponding

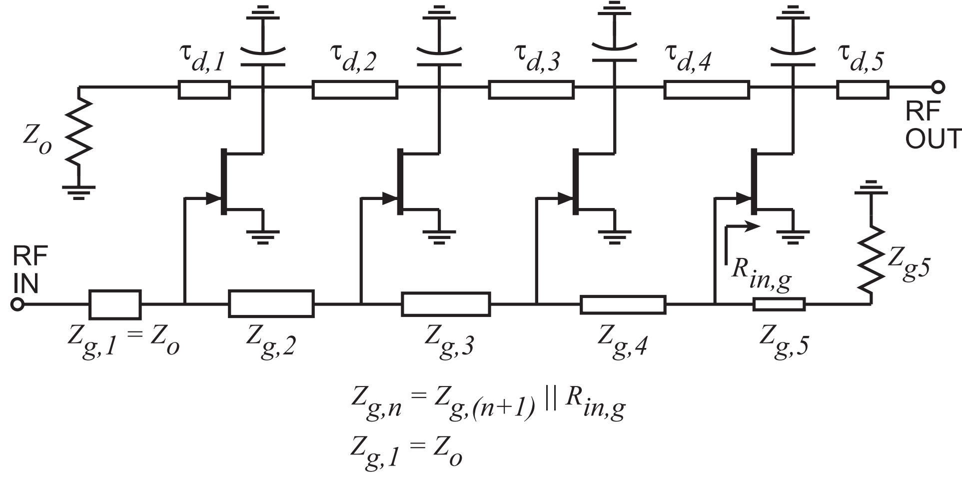

Figure 6.4: A.C. circuit schematic of a TWA using tapered gate line ($Z_{g,n}$ refers to the loaded line impedance).

to its peak output voltage swing. The output voltage swings are frequency dependent, so the optimization is usually done at midband.

Even with these modifications breakdown of devices due to unequal loading is a serious concern which severely limits their use near their peak output power.

The output power and efficiency is also limited by the attenuation in the drain line. Using dual-gate or cascode devices can significantly increase the output conductance of the device [55, 56] to improve output power and efficiency.

Though all the techniques discussed above try to improve efficiency by equalizing the device drives, efficiency is still limited to 25% due to the reverse termination (chapter 3, page 36). In the quest for higher efficiencies, numerous variations have been explored in the past including

1. distributed power amplifier using a Wilkinson combiner [60].
2. tapered drain line distributed amplifier [61].
3. distributed power amplifier using corporate power combiner [62, 63].
4. Class-B push-pull distributed amplifier using a distributed paraphase converter [64].

Some of these topologies trade-off bandwidth (case 1) for higher efficiency. Here we look at tapered-drain-line distributed amplifier which is the topology used in most commercial broadband power amplifier MMICs [65, 66].

6.2 Tapered-drain-line distributed amplifiers

The tapered-drain-line TWA [22] eliminates the drain-line reverse wave by suitable tapering of the drain line, and has theoretical class-A efficiency approaching 50%. Considering the four stage design of fig. 6.5, in the absence of the reverse termination all the current from the first device (i_d) flows in the forward direction into the line with characteristic impedance $Z_{d,1}$. By choosing $Z_{d,2} = Z_{d,1}/2$, one third of the current ($-i_d/3$) is reflected back at the junction of $Z_{d,1}$ and $Z_{d,2}$. The current flowing from the second device splits as ($i_d/3$) in the reverse wave and ($2i_d/3$) in the forward wave. Thus the reverse current cancels with the reflected current eliminating the reverse wave. For this to occur at every drain line section the drain line impedances should be $4Z_o$, $4Z_o/2$, $4Z_o/3$ and Z_o.

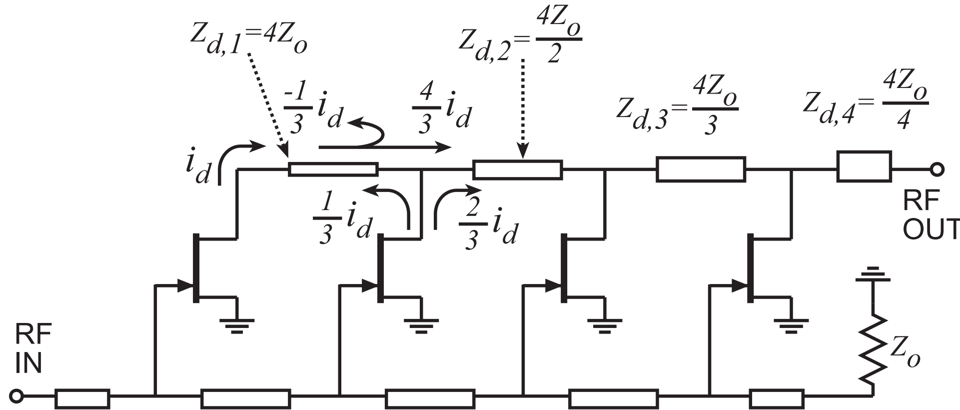

Figure 6.5: A.C. circuit schematic of a 4 cell tapered-drain-line TWA.

In general a TWA with N cells and load Z_o requires output line sections of impedance up to NZ_o. A 4-cell TWA with 50Ω loading requires 200Ω impedance lines which are difficult to realize in monolithic form. On III-V substrates, such transmission-lines have only a few μm width, resulting in high skin-effect losses and very low current-carrying capability (with ∼

5 mA/μm^2 electro migration limit). So partial tapering of the drain-line impedance is commonly used to reduce the required line impedances below NZ_o [55, 61] at the expense of lower efficiency. PAE is usually below 20% [66].

6.3 Cascode-delay-matched distributed amplifiers

Cascode-delay-matched traveling-wave amplifier (CDMTWA) [67] is a distributed amplifier having no output synthetic transmission line. The drain-line reverse wave is eliminated, and class-A efficiencies can approach 50%. Delay equalization is instead provided by impedance-matched line sections (fig. 6.6) between the common-source (CS) and common-gate (CG) devices within a cascode cell, where high impedance lines are not required. The equalizing line sections have delay increments of $\tau_s = \tau_g$, the loaded delay per section of the gate line (eq. 6.6).

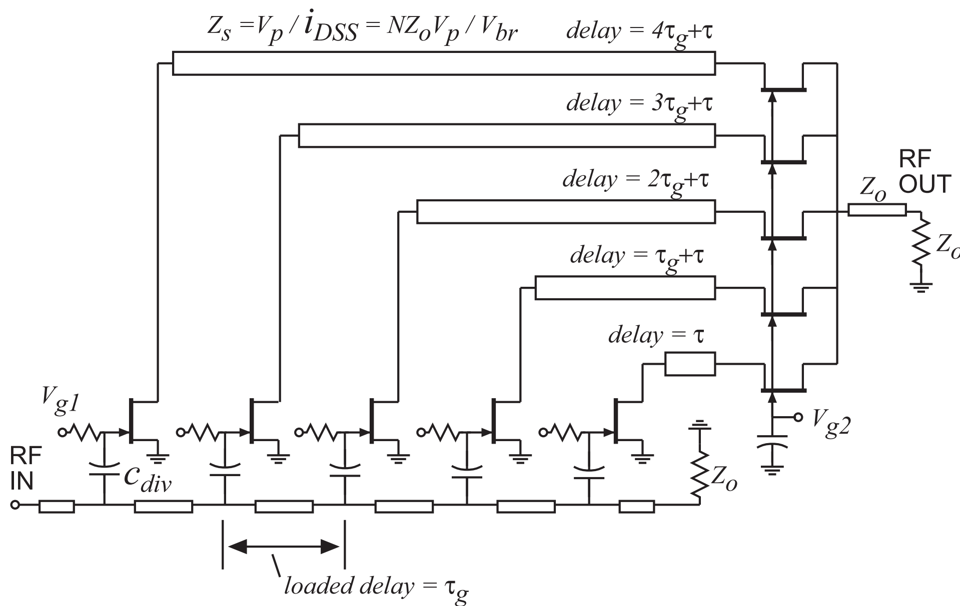

Figure 6.6: A.C. circuit schematic of a cascode-delay-matched power TWA.

In the absence of the reverse termination, the total device periphery is

selected to meet the load line $I_{DSS} = (V_{br} - V_k)/Z_o$. So each CG device in a N stage CDMTWA has a maximum current capability of $i_{DSS} = I_{DSS}/N$, and a large signal input impedance of

$$Z_{in,s} = \frac{V_p}{i_{DSS}} = \frac{NZ_oV_p}{(V_{br} - V_k)} \ . \tag{6.21}$$

To avoid resonances, the equalizing delay lines must be terminated in their characteristic impedance, $Z_s = Z_{in,s}$. Comparing this with NZ_o in the case of the tapered-drain-line TWA, the line impedance is lowered by a factor $(V_p/(V_{br} - V_k))$. For both GaAs MESFETs and GaN HEMTs used in this work this factor is ∼10. Hence in a 4-cell TWA driving a 50Ω load the equalizing lines must have 20Ω characteristic impedance. 20Ω impedance lines are readily realized on MMICs and could be designed to carry several amperes of current. Other circuit design details including gate line Bragg frequency, gate line attenuation limits and capacitive degeneration are similar to earlier TWA analysis.

This architecture could be further thought of as a tapered-drain line TWA with a broadband impedance transformation at the output. As was discussed in the last section the biggest disadvantage with the tapered-drain line TWA is the realizability of high impedance drain lines when designed for a 50Ω load. It is a perfectly feasible topology for lower impedance loads. The CG stage in a CDMTWA acts as a broadband active transformer with an impedance transformation ration of $(V_p/(V_{br} - V_k))$, and a bandwidth of f_τ. By connecting the equipotential nodes of a CDMTWA that are matched in phase and amplitude (fig. 6.7), we arrive at the tapered-drain line TWA driving a broadband active transformer.

Thus the cascode-delay-matched TWA is a transadmittance - transimpedance pair consisting of a tapered drain-line distributed transadmittance stage driving a low input impedance common-gate transimpedance stage. Successive cascading of transadmittance and transimpedance stages, results in strong impedance mismatching between stages. This principle of impedance mismatching is frequently used in high speed circuit architectures [68, 69] to realize high gain - broadband systems. Impedance mismatching makes the intermediate nodes low impedance in nature, thereby minimizing the RC charging times and improving the bandwidth.

Besides the higher efficiency the CDMTWA has other advantages. In a cascode cell most of the output voltage swing appears across the CG

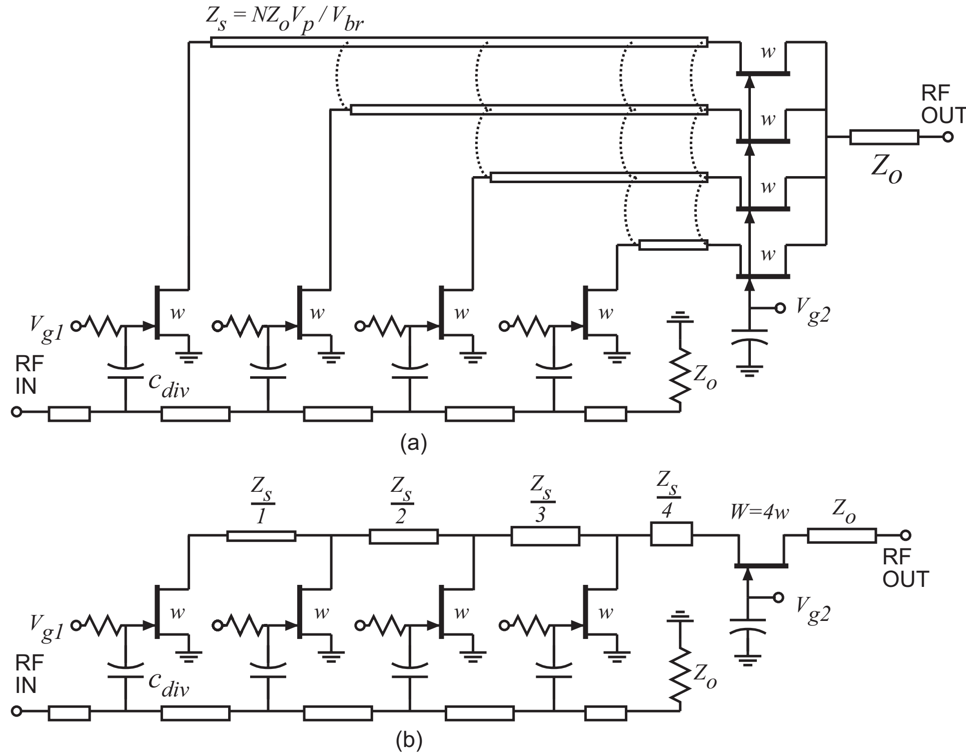

Figure 6.7: A.C. circuit schematic of a cascode-delay-matched TWA (a) as a tapered-drain line TWA with a common gate output stage (b).

device. The CS device drives the gate-source junction of the CG device and has a peak-peak V_{ds} swing of V_p, while the CG device has a peak-peak swing of $(V_{br} - V_k)$. This allows the use of low breakdown and possibly high f_τ devices for the CS distributed stage and a high breakdown device for the CG stage. Also since the inputs to the CG devices are phase and amplitude matched, and the drains are connected together (fig. 6.6), it could as well be a single lumped large periphery device. So the problems in power TWAs due to mismatch in load are eliminated. However unlike the uniform drain line TWA the output capacitances cannot be absorbed into a synthetic drain line. Effects of the output capacitance on bandwidth and efficiency is an issue (as with the f_τ-doubler circuits) and will be analyzed in detail in chapter 7.

6.4 GaAs MESFET CDM distributed power amplifiers

As a first demonstration, a 3 stage hybrid CDMTWA was constructed using discrete L-band packaged GaAs FETs (Fujitsu FSU01LG) mounted on a 20-mil duroid microstrip substrate (fig 6.8). 24 dBm of output power was expected with 4 GHz bandwidth.

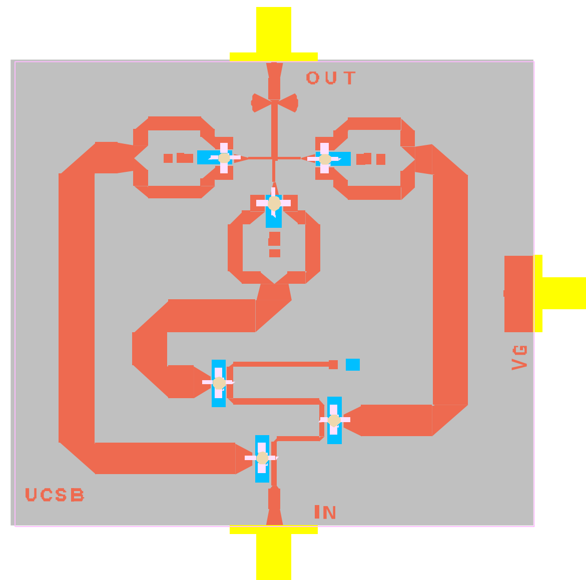

Figure 6.8: Scale model cascode-delay-matched TWA using discrete GaAs MESFETs.

Measured small-signal gain is $>$ 10 dB with 3.5 GHz bandwidth and input reflection coefficient $<$ -10 dB (fig. 6.9).

Fig. 6.10 shows output power and PAE for 10 dBm input. The output power is $>$ 23 dBm and the PAE is 30$\pm$5 % between 0.2 - 2.5 GHz. Fig. 6.11 shows PAE at frequencies of 0.5, 1.5 and 2.5 GHz. The peak PAE at these frequencies are 44%, 36% and 28% respectively. The roll-off in the output power and PAE is attributed to the FET output capacitance C_{ds} . Circuits with improved output broad-band matching should provide improved PAE at the upper band-edge. Performance is also limited by parasitics arising from hand assembly.

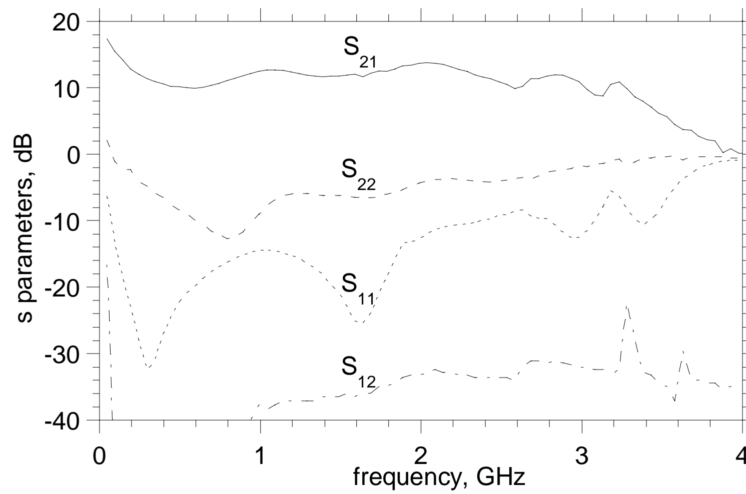

Figure 6.9: Measured small-signal S-parameters.

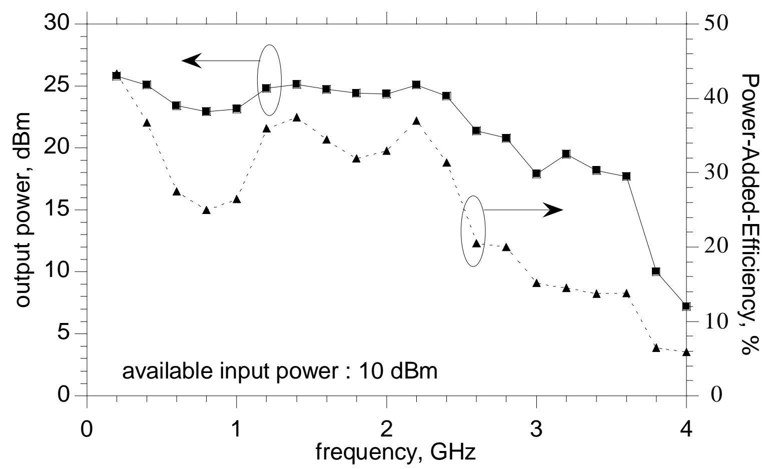

Figure 6.10: Measured PAE and output power vs. frequency at 10 dBm available input power.

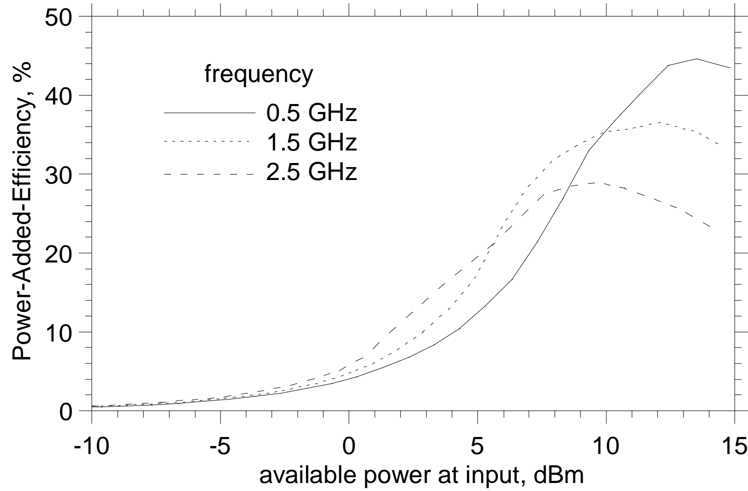

Figure 6.11: Measured PAE vs. input power at 0.5, 1.5 and 2.5 GHz.

6.5 GaAs MESFET / GaN HEMT CDM distributed power amplifiers

Initial designs of CDMTWA were done using GaN HEMTs for the CS and CG devices. However due to the immaturity of the device technology, poor yield and gross non-uniformity of the devices within a wafer, building distributed circuits that require larger die area, uniform devices and accurate models seemed a nightmare. Even though the CG device is a lumped large periphery device with similar die area as the f_τ-doubler circuits, the distributed nature of the CS stage either requires separate dice for each device or a large die containing all devices. Due to the limitations of dicing and handling dice < 1 mm^2 area, separate dice for the CS devices would imply at least 4 mm^2 area for a 4 cell CS stage. If all the CS devices are in a single die then the minimum size limitation is set by the separation required between adjacent high impedance CPW gate lines. These issues combined with the problems of device non-uniformity within a wafer heightened the risks of yielding larger circuits.

So a low risk approach was instead taken that uses GaAs MESFETs from

a commercial process for the CS device and GaN HEMTs for the CG device. As was mentioned earlier in the chapter, high power CDMTWA requires high breakdown devices for the CG stage and lower breakdown ($> V_p$ of the CG device) is sufficient for the CS devices. Using GaAs MESFETs ($V_{br} =$ 12 V) from Triquint's TQTRx process also meant that the distributed CS stage could be accurately designed and modeled, and any variation in the GaN HEMT performance would only affect the lumped CG stage.

Flip-chip bonding approach allows the incorporation of different materials technologies in the same circuit. Since Triquint's design guidelines [9] do not allow any bond pads for flip chip bonding, three-layer metalization available in their process was used to define the bond pads. Separate drain, source and gate bond pads were defined and were located as close to the device as allowed by the design rules (fig. 6.12).

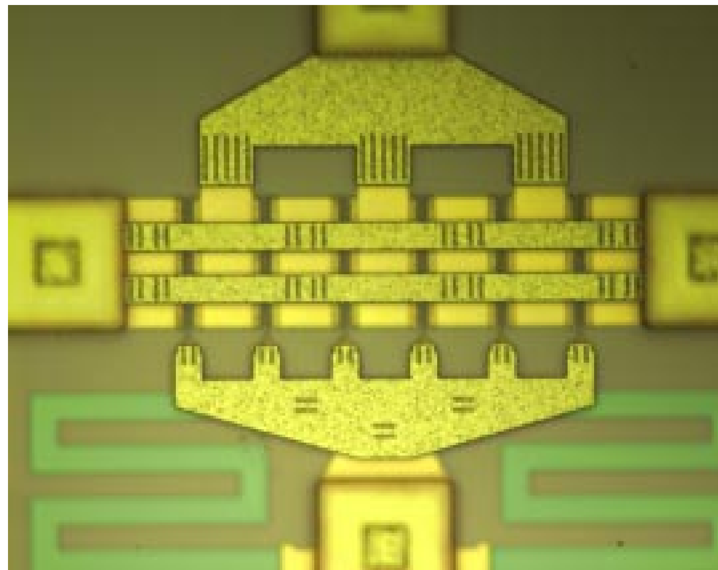

Figure 6.12: Micrograph of the GaAs MESFET used to flip-chip bond to AlN.

A 10 cell distributed stage with a total device periphery of 3 mm for the GaAs MESFET was chosen to provide 1 A current swing. The gate line impedance of 90 Ω was used, with a gate line Bragg frequency of 13 GHz. 50 % capacitive division was used to get an overall gain of 12 dB and a bandwidth of 12 GHz. Interstage delay matching was done using 60 Ω lines

to match to the input impedance of the CG device. The interstage delays were set equal to the loaded delays of the gate line. To partially absorb the parasitics of the lumped CG device, inductive networks were used at its source and drain. Multiple designs were made for a 50 Ω load and for a 25 Ω load using a four stage impedance transformation network.

The GaAs die has the MESFETs, biasing resistors and capacitive division capacitors. The GaN die contains only the HEMTs. All CPW transmission lines, matching networks and additional bias and termination resistors and capacitors are on the AlN substrate (fig. 6.13). Air-bridges are used for connecting ground planes in the CPW layout. For regions under the bonded dice, metalization on the die along with the bump bonds are used as cross-overs.

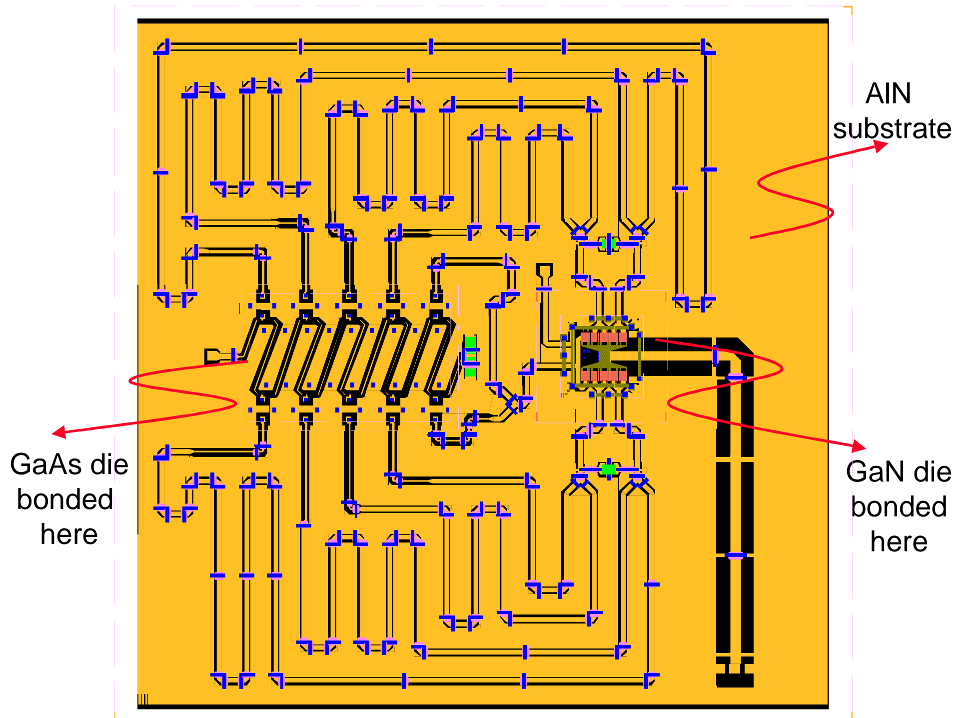

Figure 6.13: Layout of GaAs MESFET / GaN HEMT CDM TWA showing the gate line and interstage delay matching networks.

The die area for the GaN HEMT, GaAs MESFET and AlN dice are 1.38 mm × 1.38 mm, 2.29 mm × 1.53 mm and 7.75 mm × 7.50 mm respectively.

The GaAs dice were milled to 7 mils at Triquint. The GaAs die is flip chip bonded to the AlN substrate before bonding the GaN die (fig. 6.14). Small signal and power measurements are done using the same setup mentioned in chapter 5 on page 78.

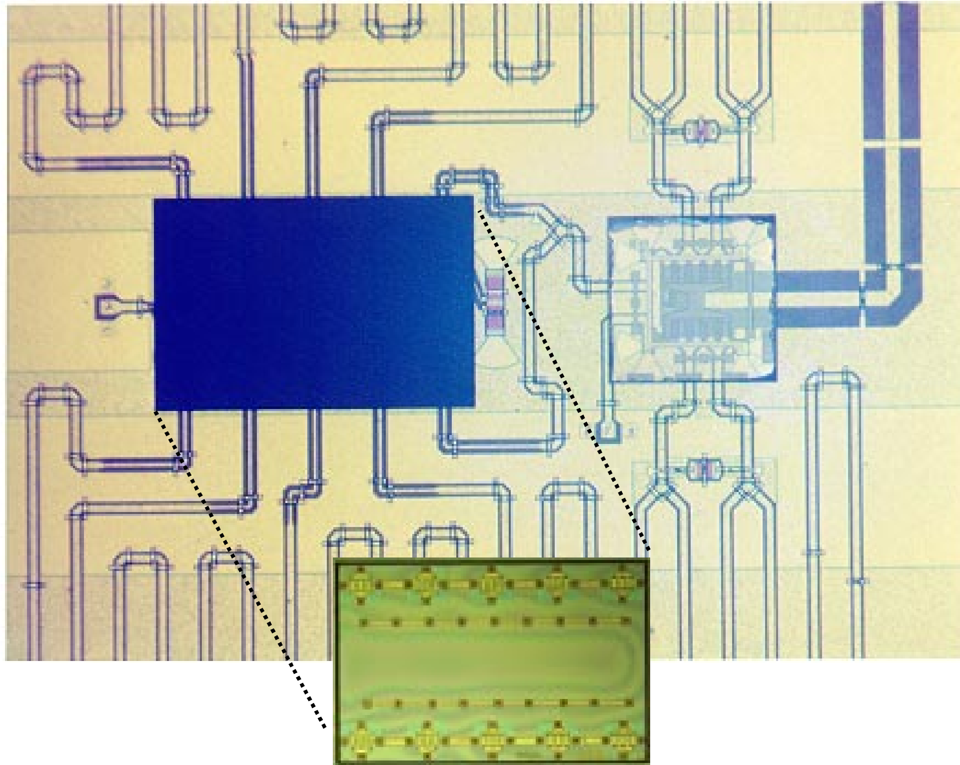

Figure 6.14: Die photograph of GaAs MESFET / GaN HEMT CDM TWA with a 50 Ω load (GaAs MESFET die shown as inset).

Measured small signal scattering parameters of the CDMTWA with 50 Ω load (fig. 6.15) shows $\sim$ 11 dB small-signal gain over 1 - 9 GHz bandwidth with input reflection coefficient lesser than -10 dB, at a drain bias of 15 V. However as the drain bias was increased beyond 19 V breakdown in the GaAs MESFETs was observed. For 5 - 6 W operation the cascodes have to be biased at $\sim$ 30 V bias. At a reduced drain bias of 19 V, output power $>$ 28 dBm have been measured over 2 - 8 GHz with a flat gain of 11 dB and $>$ 10% PAE (fig. 6.16). At 8 GHz the peak output power and peak PAE

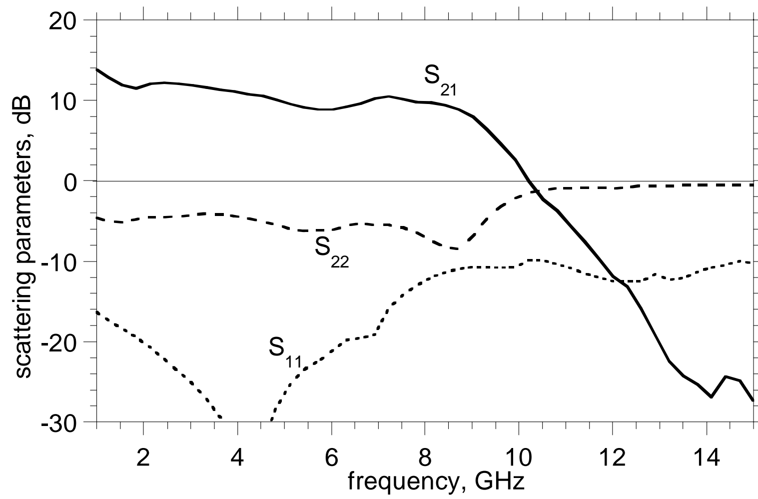

Figure 6.15: Small-signal performance of GaAs MESFET / GaN HEMT CDM TWA with a 50 Ω load.

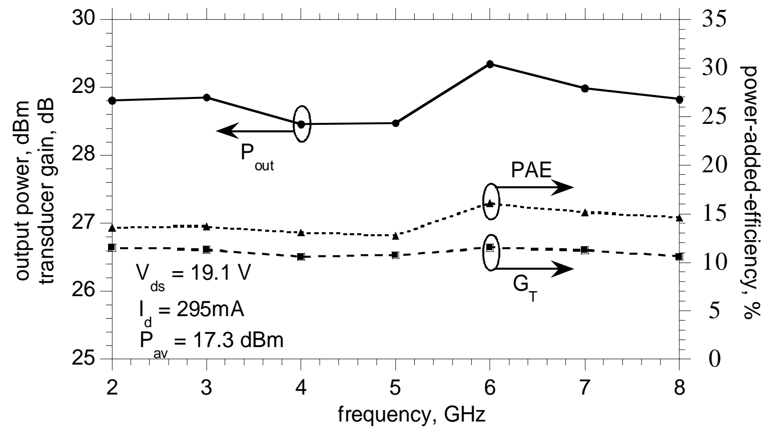

Figure 6.16: Power performance of GaAs MESFET / GaN HEMT CDM TWA with a 50 Ω load from 2 - 8 GHz.

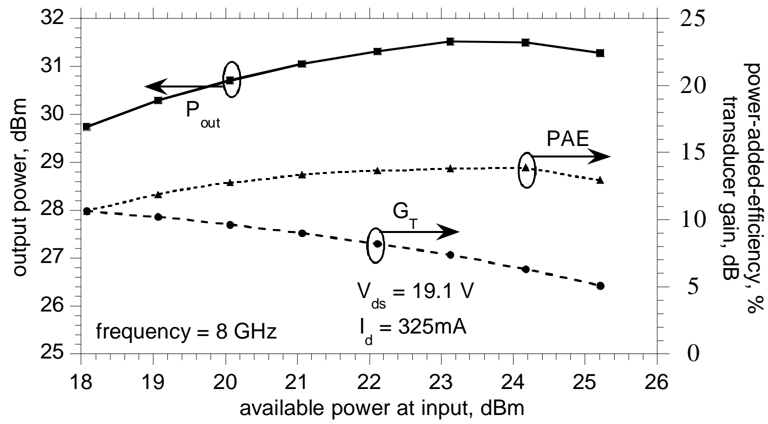

Figure 6.17: Power performance of GaAs MESFET / GaN HEMT CDM TWA with a 50 Ω load at 8 GHz.

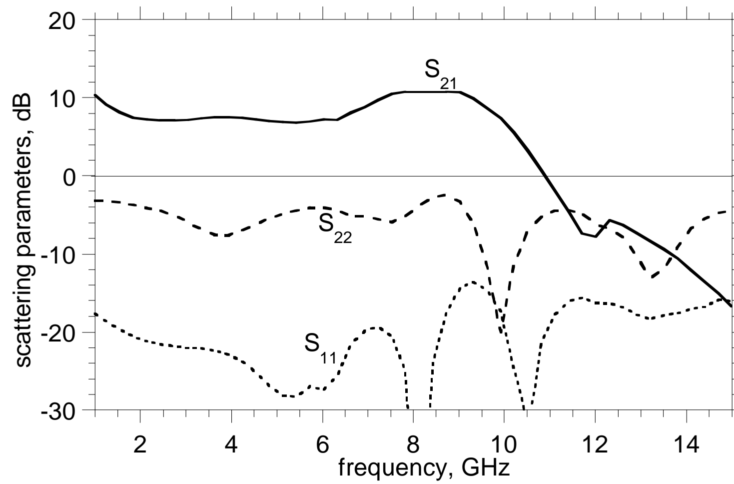

Figure 6.18: Small-signal performance of GaAs MESFET / GaN HEMT CDM TWA with a 25 Ω load.

are 1.35 W and 14% respectively (fig. 6.17). The circuits with 25 Ω load had a slightly higher bandwidth of 10 GHz with 8 - 11 dB small signal gain (fig. 6.18).

Though these output powers are far less than what is expected at higher bias voltages, they correlate well with 1.6 W maximum power expected from 25 V swings at these bias. The cause of the GaAs MESFET failure at higher bias could be due to two reasons. The MESFETs dice are thinned to 7 mils and are designed for being heat sunk from the back of the die. Though the flip chip bonding approach provides a low inductance electrical contact to the devices, it does not provide a good thermal path as the design rules do not allow bonds on top of the devices. There is also a potential breakdown problem if there is uneven voltage distribution from what is expected in an ideal cascode pair. Any leakage current from the CG device could increase the voltage drop across the CS device. There could also be potential problems of oscillations with CG devices, though in this case no signs of oscillations were observed during any of the measurements.

The cascode-delay-matched distributed amplifier topology is a physically realizable distributed amplifier capable of providing class-A limited efficiency. This topology is suitable for efficient high power broad-band MMIC amplifiers. An experimental hybrid in a GaAs MESFET technology achieved gain-bandwidth product of $1.4f_\tau$, with 30±5 % power-added-efficiency. GaAs MESFET / GaN HEMT CDMTWA using GaAs MESFETs for the CS device and GaN HEMTs for the CG device achieved 1 - 10 GHz bandwidth with 11 dB small signal gain and $>$ 1 W output power. These were the first circuits to incorporate GaAs and GaN devices into a single hybrid and represent the largest gain-bandwidth obtained using GaN HEMTs. Further improvements in bandwidth, power and efficiency are feasible using techniques described in the next chapter.

Chapter 7

Further improvements in bandwidth, power and efficiency

THOUGH the circuit techniques presented in the chapters 5 and 6 are capable of providing efficient broadband high power amplifiers they do not meet the ONR's goal of 10's of Watts of power over 2 - 20 GHz. Further improvements at both the device level and circuit level are essential to improve the performance of the circuits.

Three key improvements are discussed in this chapter which could be used in conjunction with the circuits discussed in the earlier chapters. These include

1. Broadband output network designs for effective C_{ds} absorption over broad bandwidths. This should improve efficiencies especially at high frequencies where $C_{ds}Z_o$ time constant starts dominating.

2. Dual - Gate and *slow-fast* cascode designs for improving output power and bandwidth available from a given material technology.

3. Broadband push-pull class-AB designs for improving efficiency beyond the class-A limits.

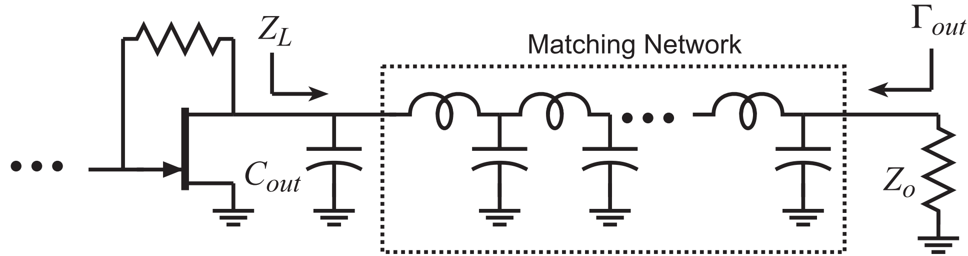

Figure 7.1: π-section output matching networks for broad-band power amplifiers.

7.1 Broadband output networks for C_{ds} absorption

In all amplifier configurations considered earlier, the device parasitic capacitances C_{gd} and C_{ds} load the amplifier output. In narrowband power amplifiers the net output capacitance (C_{out}) is tuned out using an inductive element, so as to provide the optimum load to the device at the frequency of interest. Except for the losses in the inductors one could obtain the maximum available power from the device at one frequency. However in broadband designs it is not feasible to tune C_{out} over all frequencies of interest. So broadband π-sections (fig. 7.1) are used to partially absorb C_{out} and improve matching. In small signal amplifiers, these networks are designed to minimize the magnitude of the output reflection coefficient (Γ_{out}), over the bandwidth of interest.

In power amplifiers however, the matching network has to be designed to improve output power and PAE at the upper band-edge. In the absence of the matching network, the load-line deviates from R_L with increasing frequency due to C_{out}. This deviation could be easily understood by assuming a linear model for the device output, consisting of a current source that swings from 0 to I_{DSS}, in shunt with a capacitor C_{out}. The allowed voltage swing is assumed to be between 0 (V_k neglected) and V_{br} to further simplify the analysis. The low frequency optimum load for such a device is $Z_o = V_{br}/I_{DSS}$. At higher frequencies the intrinsic device sees the combination of C_{out} and Z_o as the load and the loadline is no longer resistive (fig.

7.2(a)). Here f_{out} is the output pole frequency given by,

$$f_{out} = \frac{1}{2\pi C_{out}(V_{br}/I_{DSS})} \ . \tag{7.1}$$

This is the frequency at which the output power and PAE falls to 50% of their mid-band values, in the absence of any output matching network. As is seen in fig. 7.2(a), linear operation is limited by the peak available current swing I_{DSS} at high frequencies.

In the presence of a lossless matching network (fig. 7.1), linear operation could be limited either by the peak available current swing I_{DSS} or by the peak available voltage swing V_{br}. In general if $Z_L(f)$ is the load seen by the intrinsic device, then if $|Z_L(f)| < Z_o$ linear operation is limited by I_{DSS} and if $|Z_L(f)| > Z_o$ linear operation is limited by V_{br} [43].

The maximum linear power is calculated for either case as follows :

1. $|Z_L(f)| < Z_o$
   Since the loadline is current limited, imagining the load as a series impedance, the maximum linear power ($P_{out}(f)$) can be expressed as

   $$P_{out}(f) = \frac{I_{DSS}^2 \mathrm{Re}\{Z_L(f)\}}{8} \tag{7.2}$$

   The maximum linear power is now lesser than the low frequency case ($P_{out} = I_{DSS}^2/Z_o$), by a factor

   $$\frac{P_{out}(f)}{P_{out}} = \frac{\mathrm{Re}\{Z_L(f)\}}{Z_o} \ . \tag{7.3}$$

2. $|Z_L(f)| > Z_o$
   Since the loadline is now voltage limited, imagining the load as a shunt admittance, ($P_{out}(f)$) can be expressed as

   $$P_{out}(f) = \frac{V_{br}^2 \mathrm{Re}\{Y_L(f)\}}{8} \tag{7.4}$$

   The maximum linear power is now lesser than the low frequency case, by a factor

   $$\frac{P_{out}(f)}{P_{out}} = \mathrm{Re}\{Y_L(f)\} Z_o \ . \tag{7.5}$$

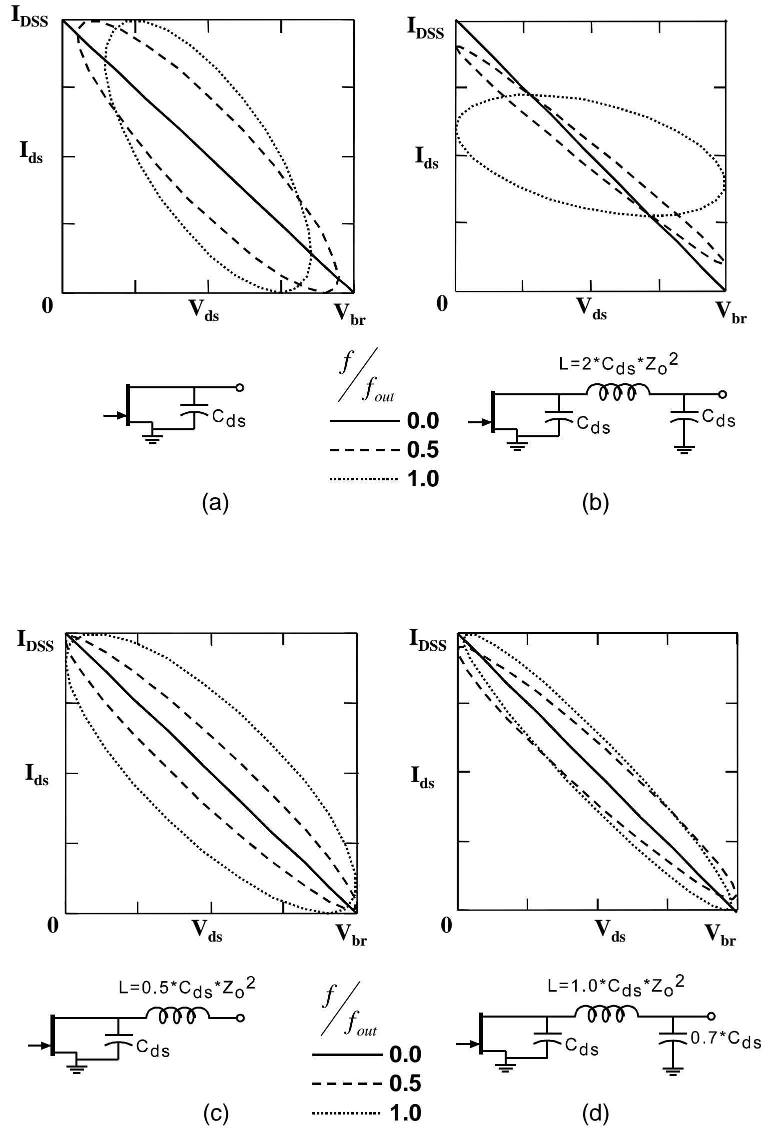

Figure 7.2: Variation of load-line with frequency for (a) no matching network, (b) small signal π network, (c) L - section and (d) optimum large signal π network compensation.

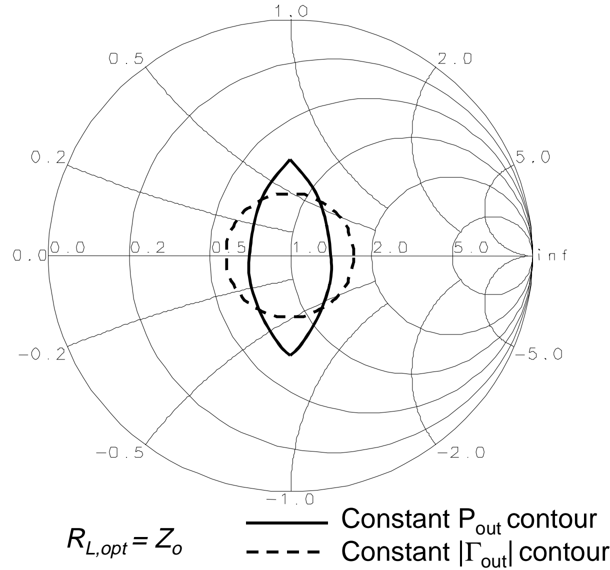

Figure 7.3: Design consideration for output matching networks in small signal and power amplifiers.

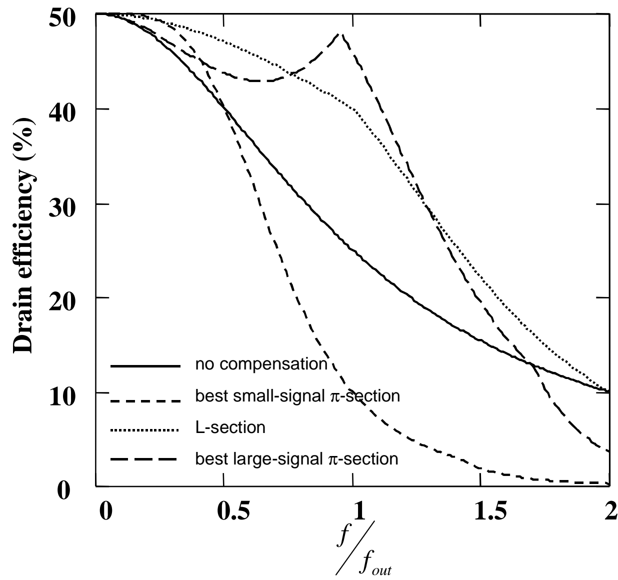

Figure 7.4: Theoretical maximum drain efficiency obtainable with various matching networks.

So to obtain the maximum output power the matching networks have to be designed to minimize both Im$\{Z_L(f)\}$ and Im$\{Y_L(f)\}$ over the bandwidth, as against minimizing $|\Gamma_{out}|$ in small signal designs. Fig. 7.3 shows the difference between the two designs. The constant $|\Gamma_{out}|$ contours are circles about the center of the Smith chart unlike the constant output power contours for a non optimum load.

Fig. 7.2 shows the variation of loadline with frequency for various output networks. The best output networks (c),(d) maintains an almost Z_o load by shifting between the current limited case and voltage limited case. Comparing the drain efficiency corresponding to the maximum linear power for each case, fig. 7.4 shows that a three section matching network (d) could theoretically obtain more than 40% drain efficiency up to f_{out}. Further improvement could be obtained by increasing the number of sections in the matching network. A similar analysis for feedback circuits designed for a voltage gain of four, is shown in fig. 7.5 and 7.6.

With these improved broadband matching sections one could obtain high efficiencies up to f_{out}. For the GaN HEMTs in common source configuration most of the output capacitance contribution comes from C_{ds}. The drain to source capacitance for flip chip bonded devices is nearly doubled, as AlN has similar dielectric constant as GaN ($\epsilon_{r,AlN} = 8.9$, $\epsilon_{r,GaN} = 10.4$). Using *Tranline* [72, 73] C_{ds} for devices which have both source and drain bonded and for devices having only the source bonded (fig. 7.7) were estimated to be 0.3 pF/mm and 0.1 pF/mm respectively. Using these values f_{out} is calculated to be 16 GHz and 5.3 GHz respectively, for the two cases.

So, the flip-chip bonding technique needs to be re-examined especially when higher bandwidths are required. GaN HEMTs grown on SiC substrates having superior thermal conductivity will allow the fabrication of true MMICs without the need for flip-chip bonding. In such circuits bandwidth should be primarily limited by the input pole.

7.2 Dual-gate and *slow-fast* cascode designs

To achieve high power over bandwidths of 2 - 20 GHz significant improvements at the device level is required. Output power density of 5 $\sim$6 W/mm at 10 GHz have been demonstrated on SiC substrates [74]. Devices with $f_\tau \sim 50$ GHz and with f_{max} of 105 GHz have also been achieved by scaling gate-length $L_g \sim 0.25$ m [75, 76]. However, as L_g is reduced to obtain a

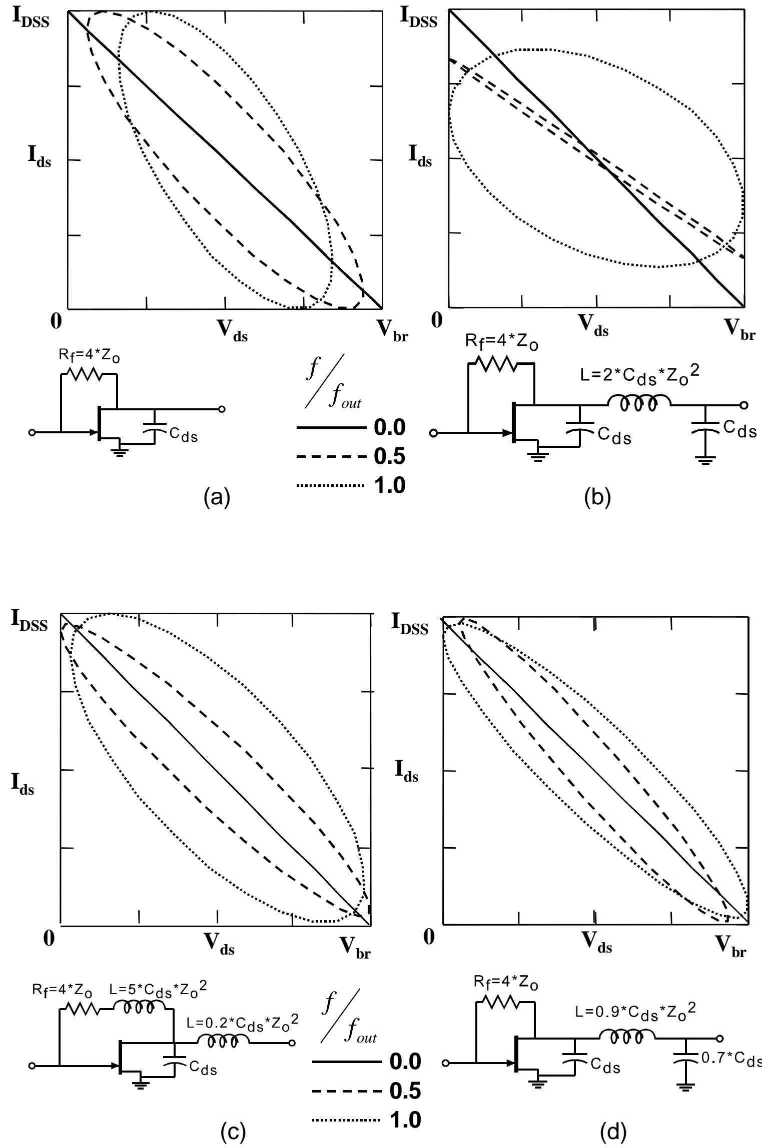

Figure 7.5: Variation of load-line with frequency for resistive feedback circuits with (a) no matching network, (b) small signal π network, (c) T - network and (d) optimum large signal π network compensation.

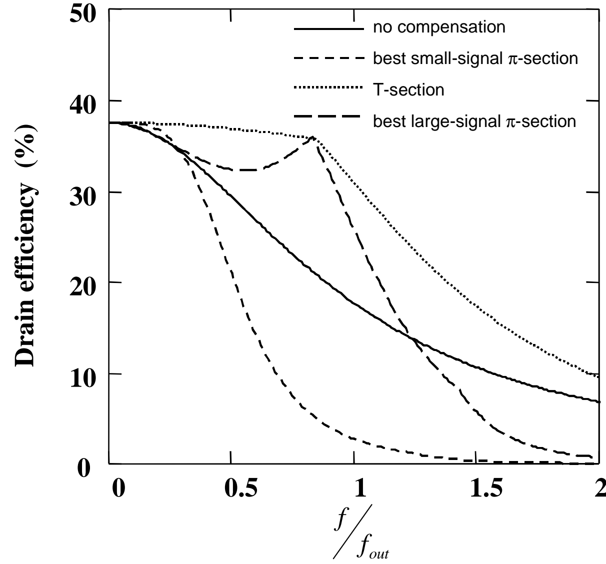

Figure 7.6: Theoretical maximum drain efficiency obtainable with various matching networks in resistive feedback amplifiers designed for a voltage gain of 4.

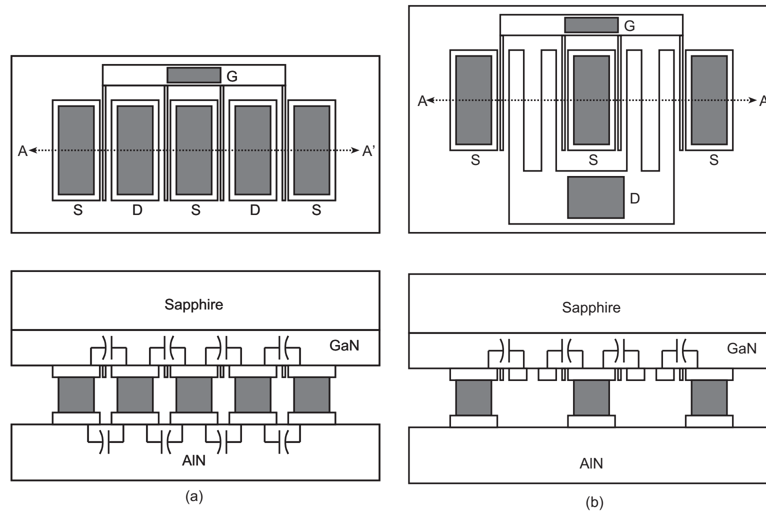

Figure 7.7: Output capacitance in flip chip bonded devices (a) with source and drain bonded and (b) with the source only bonded.

higher f_τ, the breakdown voltage decreases. As was mentioned in chapter 2, (page 21) the product of f_τ and V_{br} can be written as $E_{max}v_{sat}/\pi$ (eq. 2.8), a constant for a given technology, where E_{max} and v_{sat} are breakdown field and electron velocity respectively [11]. Increased f_τ is obtained at the expense of V_{br}, and high power levels are obtained at the expense of amplifier bandwidth.

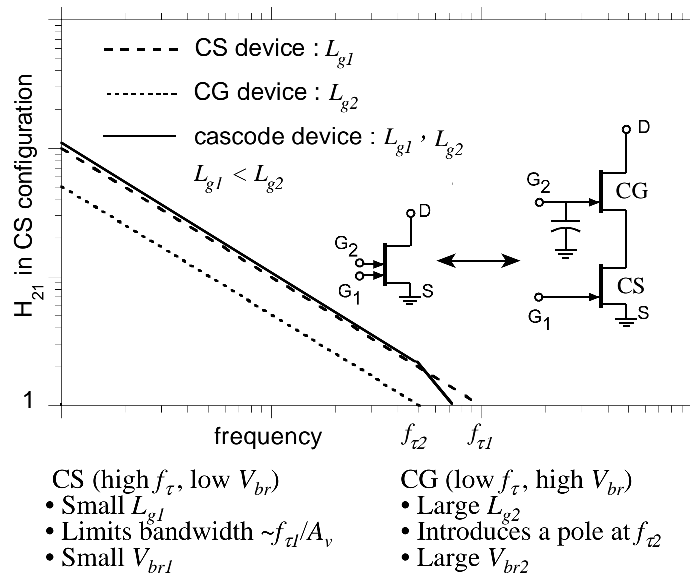

Figure 7.8: Dual-gate device design for high power broadband amplifiers.

A dual-gate device is electrically equivalent to a common-source (CS) / common-gate (CG) cascode pair [77] (fig. 7.8). The current gain $H_{21}(jf)$ for a single-gate and a cascode device are f_τ/jf and $(f_{\tau 1}/jf)(1+jf/f_{\tau 2})^{-1}$ respectively, where $f_{\tau 1}$ and $f_{\tau 2}$ are the current gain cut-off frequencies of the CS and CG devices respectively. For $f < f_{\tau 2}$, H_{21} for a cascode is similar to a single-gate device with cut-off frequency $f_{\tau 1}$. So the gain-bandwidth product of the cascode is $\sim f_{\tau 1}$ for bandwidths $< f_{\tau 2}$. Hence the stage bandwidth in a cascode is determined primarily by the CS device [78]. Breakdown voltage in contrast is determined by the CG device as the applied V_{ds} of a CS device is small. Thus a dual-gate device designed with the CS device having short L_g for high f_τ, and the CG device having larger L_g for high V_{br} can provide simultaneous high f_τ and V_{br} required for high

power broadband applications. This does not violate the Johnson limit, but just splits the bandwidth and breakdown requirements between the CS and CG devices.

Dual-gate AlGaN / GaN HEMTs with gate-lengths of 0.16 μm and 0.35 μm for the first and second gates respectively, have been developed using e-beam lithography. These devices have achieved $f_\tau > 60$ GHz with $V_{br} > 100$ V, compared to < 50 V breakdown and similar f_τ for 0.16 μm single gate devices [79]. Output power densities up to 3.5 W/mm at 8.2 GHz have been achieved. MMIC f_τ-doubler power amplifier circuits using dual-gate GaN HEMTs on SiC are in development and are expected to achieve 2 - 20 GHz bandwidth.

Using a similar approach we could also realize CS - CG cascode pairs that use different device technologies for the two devices. The CS device could be a high f_τ InP PHEMT with 10 V breakdown driving a high breakdown low f_τ AlGaN / GaN HEMT. Such *slow-fast* hybrids used in either of the lumped or distributed circuits should be capable of achieving higher power-frequency products.

7.3 Push-pull class - AB designs

To improve efficiency further class - AB push - pull designs were analyzed. Since complementary devices are not available, for class - AB designs using baluns (fig. 7.9) to be feasible over broad bandwidths the following three key components are required :

1. efficient, broadband, high power amplifiers : either CDMTWA or f_τ-doubler power amplifiers could be used.

2. broadband low loss balun : baluns with bandwidths of 4:1 have been reported at microwave frequencies. However, losses need to be minimized. Most broadband microwave balun use the *Marchand* balun architecture [81, 82, 83], which has been used here.

3. broadband second-harmonic termination : again bandwidths of 4:1 have been reported using coupled spiral inductor transformers [84].

Losses in a microstrip Marchand balun (fig. 7.10) can be minimized by using a low ϵ_r dielectric substrate [85] with maximum thickness (limited by

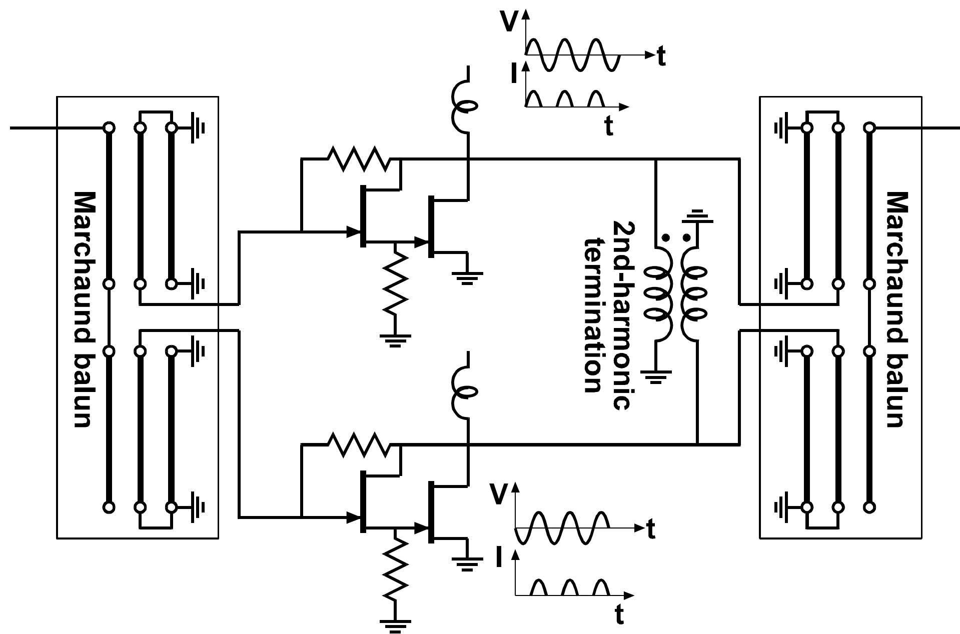

Figure 7.9: Schematic of a microwave class - AB push pull power amplifier.

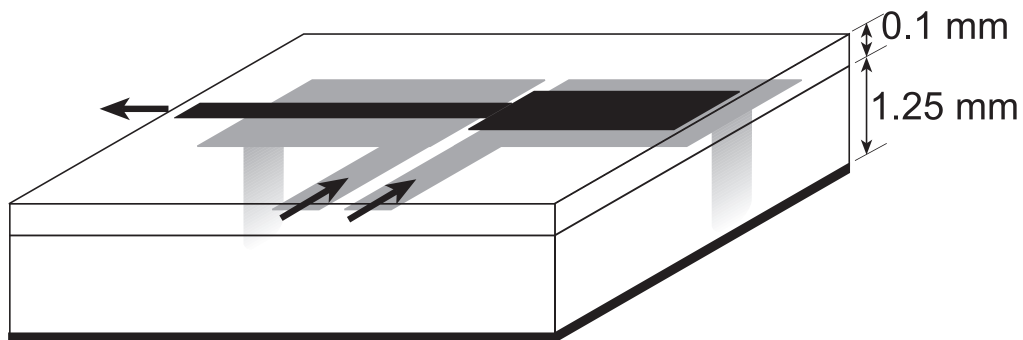

Figure 7.10: Schematic of a Marchand balun on duroid substrate.

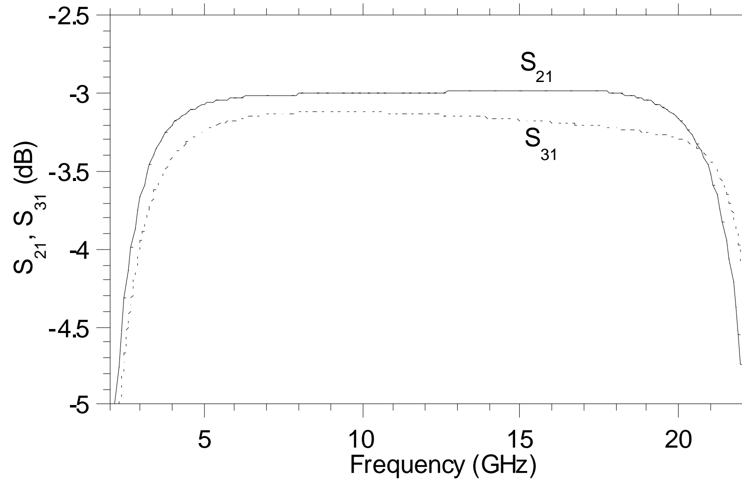

Figure 7.11: Simulated loss of a Marchand balun on duroid substrate (coupling loss = -3 dB, rest is insertion loss).

$\lambda/8$). Simulations have predicted $\sim$ 0.3 dB insertion loss (fig. 7.11) over 4 - 20 GHz bandwidth.

As was seen in chapter 2 (fig. 2.8), to provide true class-AB loadlines, broadband harmonic terminations are required to short the even mode signals. However tuners cannot provide two octaves of bandwidth and ferrites are not available at microwave frequencies. Planar coupled spiral inductors have been used to obtain 5 - 20 GHz transformers with $\sim$1.5 dB loss [84]. Again, implementation on thick low ϵ_r dielectric substrates will minimize the losses.

With these improvements, f_τ-doubler and CDMTWA power amplifiers should be capable of achieving output power beyond 10 W, with 2 - 20 GHz bandwidth and > 50 % PAE.

Chapter 8

Conclusion

8.1 Achievements

IN this work a comprehensive study of circuit topologies for broadband, efficient, high power microwave amplifiers was done. Two circuit configurations have been developed, which are capable of providing class-A limited efficiencies over bandwidths of up to 40% of the transistor's f_τ while providing 10 dB gain.

The f_τ-doubler resistive feedback power amplifier is a lumped amplifier topology which uses a Darlington pair with suitable shunt loading on the input device, to provide equal A.C. current division between the two devices up to frequencies of the order of f_τ. This ensures loadline matching for either device at all frequencies of interest. Additionally the shunt loading provides a gain-bandwidth product of $2f_\tau$ with a single pole roll-off for the short-circuit current gain. This improves the bandwidth and stability of the power amplifiers. Resistive feedback along with the broadband matching sections provide input and output matching over broad bandwidths. These circuits are capable of obtaining similar bandwidths as distributed amplifiers in a smaller die area.

The cascode-delay-matched traveling wave amplifier is a distributed amplifier topology capable of obtaining efficiencies up to the class-A theoretical limit of 50%, with bandwidths limited by the transistor power gain cut-off frequency, f_{max}. The reverse-wave in a traditional traveling wave amplifier is suppressed by eliminating the drain line. The delay matching is instead done between the common-source and common-gate devices

of a cascode cell. This could also be thought of as a tapered drain-line distributed transadmittance stage driving a low input impedance common-gate transimpedance stage. This strong impedance mismatch between the transadmittance and transimpedance stages is frequently used in high speed circuit architectures to realize high gain broadband systems. In the cascode-delay matched traveling wave amplifier the common gate transimpedance stage minimizes the line impedances required for the tapered drain-line distributed input stage. This makes them physically realizable for higher powers by overcoming electro-migration problems.

GaN / AlGaN HEMT microwave power amplifiers using either circuit topologies were designed, fabricated and tested. The first-generation power amplifiers were designed in a GaAs MESFET technology to verify the circuit concepts, since GaN HEMT technology was relatively immature to allow circuit fabrication in the early phases of this research. Scale-model f_τ-doubler feedback power amplifier MMICs were implemented in a commercial GaAs MESFET process. A bandwidth of 0.2 - 6 GHz with 12 dB gain, over 23 dBm output power, and more than 25 % PAE was obtained using devices offering 18 GHz f_τ and 12 V breakdown. These circuits have a bandwidth of 33% of f_τ and a gain-bandwidth product of $\sim 1.3{\cdot}f_\tau$, with efficiencies more than what traditional distributed power amplifiers have achieved. Scale-model hybrids of the cascode-delay-matched TWAs were implemented using commercially available discrete L-band GaAs MESFETs. Bandwidth up to 25% of f_τ with ∼15 dB gain and 30±5 % power-added-efficiency was achieved.

Two generations of f_τ-doubler feedback power amplifier were designed, fabricated and tested in 0.7 μm gate-length GaN HEMT technology. The first generation of circuits yielded ∼11 dB gain, 0.2 - 7.5 GHz bandwidth amplifiers with ∼1.5 W output power (limited by the large DC - RF dispersion) and up to 15% PAE. The second generation of circuits achieved ∼10 dB small signal gain, 1 - 8.0 GHz bandwidth amplifiers with up to ∼5.12 W output power and up to 23% PAE. Cascode-delay-matched distributed power amplifiers were fabricated in GaAs MESFET / GaN HEMT technology using GaAs MESFETs for the CS device and GaN HEMTs for the CG device in the cascode cell. These circuits achieved 1 - 10 GHz bandwidth with 11 dB small signal gain and up to 1 W output power. These were the first circuits to incorporate GaAs and GaN devices into a single hybrid and represent the largest gain-bandwidth obtained using GaN HEMTs.

8.2 Future Work

To meet ONR's requirements of ultra-broadband, efficient, linear solid-state high power microwave amplifiers with 10's of Watts over a 2-20 GHz bandwidth, with 40% or higher PAE, low noise figure ≤ 3 dB and high linearity, improvements at both the device level and circuit level are essential.

Improvements in bandwidth and output power could be obtained by using *slow-fast* cascode cells in either of the proposed circuits. This configuration uses a *fast* transistor (having a high f_τ and consequentially low device V_{br}) for the CS device, and a *slow* transistor (having a high device V_{br} and consequentially low f_τ) for the CG device, in a cascode cell. Monolithic form using dual-gate devices having small and large gate lengths for the first and second gates respectively or a hybrid multi-chip module (MCM) implementation using two different device technologies (eg. InP PHEMT for the common-source device and GaN HEMT for the common-gate devices) are feasible. Since the bandwidth is limited primarily by the CS device and the output power by the CG device the overall power and bandwidth could be improved. This requires device scaling to deep sub-micron gate lengths using e-beam lithography, work on which is in progress and the initial results look promising, with f_τ of 60 GHz obtained with 0.2 μm - 0.4 μm dual-gate devices.

Improvements in efficiency could be obtained using broadband class-AB push-pull stages. A modified Marchand balun architecture, employing even mode termination for a true class-AB operation of the device, is capable of providing efficiencies up to the theoretical class-B limit of 78.5% and a 5:1 bandwidth. Initial studies on feasibility of such a balun have been performed. These designs are capable of meeting ONR's demands of efficient, high power 4 - 20 GHz systems. Higher powers up to 100's of Watts should be feasible by using low-loss power combiners that combines power from class-AB push-pull stages using either of the two circuit topologies.

As with any developing technology reliability is a key issue that will delay the deployment of these designs in their intended systems, in the near future. Wafer uniformity is a serious concern, as the peak output power density and maximum current varies a by factor of three or more within wafer, in most of the processed wafers. Methods of efficient heat-sinking of GaN HEMTs on sapphire substrates have to be re-examined. Though flip chip bonding has proven adequate at lesser powers, with the power from the

devices increasing rapidly in the last few years thermal issues have limited operation at higher biases, at higher power levels and in continuous operation. SiC substrates will certainly improve thermal performance and would make MMIC implementations feasible. This should improve bandwidth further by lowering C_{ds} and should improve power by allowing operation at higher drain voltages. Also issues of linearity and noise would have to be addressed in the future generation designs.

Appendix A

Process flow summary

GaN HEMT Process		
Step	Mask	Systems used
1. Source / drain ohmics	sourcedrain	Stepper, PE-IIA, RIE-5, E-beam evaporator, RTA
2. Gate pad isolation	gatepad	Stepper, PE-IIA, RIE-5, E-beam evaporator
3. Gate finger Schottky	gatefinger	Stepper, PE-IIA, E-beam evaporator
4. Mesa isolation	mesa	Stepper, PE-IIA, RIE-5
5. Interconnect metal	metal0	Stepper, PE-IIA, E-beam evaporator
6. Bond pad metal	bondpad	Stepper, Deep UV, PE-IIA, E-beam evaporator
7. Dicing		Disco dicing saw
8. Bonding		Flip chip bonder

AlN Substrate Process		
Step	Mask	Systems used
1. Resistors	nichrome	Stepper, PE-IIA, E-beam evaporator
2. Metal - 1	metal1	Stepper, PE-IIA, E-beam evaporator
3. Capacitors	nitride	Stepper, PE-IIA, PECVD, RIE-3
4. Metal - 2	metal2	Stepper, PE-IIA, E-beam evaporator
5. Bond pad / post metal	post	Stepper, Deep UV, PE-IIA, E-beam evaporator
6. Air-bridge metal	airbridge	Stepper, Deep UV, PE-IIA, E-beam evaporator
7. Dicing		Disco dicing saw
8. Bonding		Flip chip bonder

Appendix B

Detailed GaN HEMT process flow

B.0 Focus Check With 2" Si Wafer

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Set spinner for 4 krpm for 2 minutes.
3. Get 2" Si wafer from dry box (in old toluene petri dish).
4. Start wafer spinning, then squirt with acetone.
5. Don't let it dry, squirt with ISO, then ACE and ISO again.
6. Put on 200°C hot plate for 5 minutes.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 1 minute. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Use "Smartset Array" mask plate, run job as follows: "FOCUS SFOC2\FOC", note down the best focus number returned by computer.

B.1 Source Drain Ohmic Contacts (mask layer 1, sourcedrain, dark field)

A Solvent Cleaning

Warning: Sapphire being transparent, observe the marks on the wafer to identify the top surface of the wafer where the epi layer is grown.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot ISO 3 minutes, ultrasonic 30 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
Warning: It is advisable to do an expo at the first mask level to find the optimum focus and exposure. The conditions mentioned here will vary with wafer thickness, lamp intensity and photoresist life.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 1 minute. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Expose for 1.4 seconds, set focus offset to -18.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 3 minutes (over develop if necessary to remove photoresist scum).
4. Rinse in running D.I., 3 minutes.

D Oxygen Plasma Descum of Photoresist

Warning: Oxygen plasma descum damages the surface, increasing DC - RF dispersion. Minimum descum time is recommended.

1. chamber pressure = 300mT of O_2.
2. Power = 100W at low frequency.
3. Run for 10 seconds.

E RIE Etch of GaN Cap Layer

1. Load Si wafer to be used in RIE #5.
2. Run LeeGAN or GaNCLN program to clean the Si wafer.
3. Unload Si wafer and place GaN wafer to be etched on top of it.
4. Etch conditions: (etch rate : 6 Å/seconds.)
   (a) Cl_2 flow rate = 10.0 sccm.
   (b) chamber pressure = 5.0 mTorr.
   (c) P = 60 W (this is controlled).
   (d) Voltage should be ∼ 150 V.
5. Etch for 15 seconds. (leave 100 - 160Å of cap layer)

F Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of NH_4OH : H_2O :: 1 : 10.
2. Dip in dilute NH_4OH for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

G Evaporation

1. Place wafer on E-Beam mount. Level it.
2. Put in a new crystal if the crystal monitor reads more than 10.
3. Pump down to below $1 \cdot 10^{-6}$ torr.
4. Deposit material:

Warning: Use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting.
Warning: Ni is prone to spitting and needs to be evaporated with care.

Material	Thickness($\mathring{A}$)	Dep. Rate ($\mathring{A}$/s)	Approx. Vernier
Ti	200	1-2	1.55
Al	2000	5	1.45
Ni	550	2	1.55
Au	500	2-3	1.50

H Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. Squirt with ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone.
4. Rinse with ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of metal.

I Annealing

1. Make sure the thermocouple is seated properly on the Si wafer inside the RTA.
2. Make sure that the leads of the thermocouple are connected correctly and it reads the room temperature in steady state.
3. Test run the GN880 program 2-3 times preferably with a test wafer.
   Warning: The RTA is known to have shown random temperature fluctuations at high temperatures, and so the test run is a must. A 10°C lower temperature could result in poor ohmics and a 20°C higher temperature could char the substrate.
4. Load the wafer into the chamber very slowly.
   Warning: Sapphire substrate is known to slide freely on smooth Si wafer. So use a rough Si wafer (with dicing marks) or restrict the sapphire substrate's motion by placing a circular piece of a used thermocouple wire around it.

5. RTA for 25 seconds at 875°C using the program GN 880.
6. Unload the wafer very slowly to prevent it from sliding.

J Test Ohmic Contacts

1. Check for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.
3. Use 4 probe measurement set up to test the TLM patterns.

B.2 SiO_2 Isolation of Gate Pad (mask layer 2, gatepad, dark field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot ISO 3 minutes, ultrasonic 30 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 1 minute. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Expose for 1.4 seconds, set focus offset to -18.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 3 minutes (over develop if necessary to remove photoresist scum).
4. Rinse in running D.I., 3 minutes.

D Oxygen Plasma Descum of Photoresist

Warning: Oxygen plasma descum damages the surface, increasing DC - RF dispersion. Minimum descum time is recommended.

1. chamber pressure = 300mT of O_2.
2. Power = 100W at low frequency.
3. Run for 10 seconds.

E RIE Etch of GaN Cap / AlGaN Layer

1. Load Si wafer to be used in RIE #5.
2. Run LeeGAN or GaNCLN program to clean the Si wafer.

3. Unload Si wafer and place GaN wafer to be etched on top of it.
4. Etch conditions: (etch rate : 20 Å/seconds)
   (a) Cl_2 flow rate = 10.0 sccm.
   (b) chamber pressure = 5.0 mTorr.
   (c) P = 200 W (this is controlled).
   (d) Voltage should be $\sim$ 400 V.
5. Etch for 40 seconds. (etch $\sim$ 800 Å)

F Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O :: 1 : 10.
2. Dip in dilute HCl for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2

G Evaporation

1. Place wafer on E-Beam mount. Level it.
2. Put in a new crystal if the crystal monitor reads more than 15.
3. Pump down to below $1.5 \cdot 10^{-6}$ torr.
4. Deposit material:

Warning: SiO_2 evaporates at high rates at the beginning of the evaporation. In the past SiO_2 have known to peel off from places and is attributed to high rates of evaporation. Keep the shutter closed for 2-3 minutes after the SiO_2 is melted, to allow the evaporation rate to stabilize, and then open the shutter.

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
SiO_2	1200	2-3	1.50

H Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until SiO_2 comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. Squirt with ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone.
4. Rinse with ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of SiO_2.

B.3 Gate Finger Metalization (mask layer 3, gatefinger, dark field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.

3. Hot ISO 3 minutes, ultrasonic 30 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
Warning: This being the critical mask level, it is advisable to do an expo to find the optimum focus and exposure. Any mis-alignment due to stepper error could be determined from the expo and corrected during the actual exposure.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 1 minute. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Expose for 3.5 seconds, set focus offset to -18.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 3 minutes (over develop if necessary to remove photoresist scum).
4. Rinse in running D.I., 3 minutes.

D Oxygen Plasma Descum of Photoresist

Warning: Oxygen plasma descum damages the surface, increasing DC - RF dispersion. Minimum descum time is recommended.

1. chamber pressure = 300mT of O_2.
2. Power = 100W at low frequency.
3. Run for 10 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$.
2. Dip in dilute NH_4OH for 20 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

F Evaporation

1. Place wafer on E-Beam mount. Level it.
2. Put in a new crystal if the crystal monitor reads more than 10.
3. Pump down to below $1 \cdot 10^{-6}$ torr.
4. Deposit material:

Warning: Ni is prone to spitting and needs to be evaporated with care. Ti contamination in Ni is an issue as the contacts might exhibit ohmic behavior in the presence of Ti. Have a separate Ni source for gate finger evaporation.
Warning: Use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting.

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
Ni	200	1-2	1.50
Au	4000	5	1.55
Ni	500	2	1.55

G Liftoff
Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. Squirt with ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone.
4. Rinse with ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of metal.

H Test Schottky Contacts

1. Check for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.
3. Use 2 probe measurement set up to test gate - source Schottky.

B.4 Mesa Isolation (mask layer 4, mesa, clear field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 10 seconds.
3. Hot ISO 3 minutes, ultrasonic 10 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 518-A with syringe and filter to cover wafer.
4. Spin at 4.0 krpm for 30 seconds.
5. Hot Plate Bake, 90°C, 1 minute.
6. Expose for 1.4 seconds, set focus offset to -18.

7. Hot Plate Bake, 110°C, 1 minute.

C Development

1. Develop in full beaker of MF-701 for 1 minutes, 30 seconds. (over develop if necessary to remove photoresist scum)
2. Rinse in running DI water for 3 minutes.
3. Blow dry with N_2.
4. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 seconds longer.

D Oxygen Plasma Descum of Photoresist and Hardbake.

1. 300mT of O_2.
2. power = 100W at low frequency.
3. run for 10 seconds.
4. Hardbake photoresist at 120°C for 20 minutes.

E Mesa Isolation Etch

1. Load Si wafer to be used in RIE #5.
2. Run LeeGAN or GaNCLN program to clean the Si wafer.
3. Unload Si wafer and place GaN wafer to be etched on top of it.
4. Etch conditions: (etch rate : 20 Å/seconds)
   (a) Cl_2 flow rate = 10.0 sccm.
   (b) chamber pressure = 5.0 mTorr.
   (c) P = 200 W (this is controlled).
   (d) Voltage should be $\sim$ 400 V.
5. Etch for 3 minutes. (for $\sim$ 3600 Å)

F Oxygen Plasma Descum of Photoresist and Hardbake.

1. 300mT of O_2.
2. power = 100W at low frequency.
3. run for 10 seconds.

G Etch Ni on Top of Gate Contacts.

1. Rinse in running DI water for 3 minutes. to remove scum left during the RIE etch.
2. Blow dry with N_2.
3. Warm Ni etchant to 60°C with stirring at 300 rpm.
4. Etch for 30 seconds after all Ni has disappeared (total etch time of 2 minutes for 550 Å).
5. Look for shiny golden surface on top of the gate contacts under the microscope.

H Resist Strip

1. Remove photoresist with acetone in liftoff beaker for 3 minutes.
2. Rinse by spraying with ISO.
3. Rinse in running DI water for 3 minutes.
4. Blow dry with N_2.

I Test Transistors

1. Check for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.
3. Use 3 probe measurement set up to test the FETs.

B.5 Gate Contact and Interconnect Metalization (mask layer 5, metal0, dark field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 10 seconds.
3. Hot ISO 3 minutes, ultrasonic 10 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 1 minute. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Expose for 1.4 seconds, set focus offset to -18.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 3 minutes. (over develop if necessary to remove photoresist scum)
4. Rinse in running D.I., 3 minutes.

D Oxygen Plasma Descum of Photoresist

Warning: Oxygen plasma descum damages the surface, increasing DC - RF dispersion. Minimum descum time is recommended.

1. chamber pressure = 300mT of O_2.
2. Power = 100W at low frequency.
3. Run for 10 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of $NH_4OH : H_2O :: 1 : 10$.
2. Dip in dilute NH_4OH for 15 seconds.

3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

F Evaporation

1. Place wafer on E-Beam mount. Level it.
2. Put in a new crystal if the crystal monitor reads more than 10.
3. Pump down to below $1.5 \cdot 10^{-6}$ torr.
4. Deposit material:

Warning: Use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting.

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
Ti	200	1-2	1.55
Au	4000	5	1.50
Ti	100	1-2	1.55

G Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. Squirt with ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone.
4. Rinse with ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of metal.

H Test Transistors

1. Check for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.
3. Use 3 probe measurement set up to test the FETs.

B.6 Bond Pad Metalization (mask layer 5, bondpad, dark field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 10 seconds.
3. Hot ISO 3 minutes, ultrasonic 10 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply PMGI - SF15 with syringe and dropper to cover wafer.
4. Spin at 3.5 krpm for 30 seconds.
5. Bake, 200 C, 2 minutes. on hot plate.
6. Remove SF15 threads from the corners using a clean razor.
7. Apply SPR 950-0.8 with syringe and filter to cover wafer.
8. Spin at 2.5 krpm for 30 seconds.
9. Soft Bake, 90 C, 1 minute. on hot plate.
10. Apply CEM 365 with syringe and filter to cover wafer.
11. Spin at 4 krpm for 30 seconds.
12. Expose for 1.4 seconds, set focus offset to -18.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 3 minutes. (over develop if necessary to remove photoresist scum)
4. Rinse in running D.I., 3 minutes
5. Blow dry with N_2.
6. Expose in deep - UV for 200 seconds.
7. Develop in SAL 101 for 1 minute.
8. Rinse in running D.I., 3 minutes.
9. Blow dry with N_2.
10. Observe under microscope for resist fringes.
11. Expose in deep - UV for 200 seconds.
12. Develop in SAL 101 for 30 seconds.
13. Rinse in running D.I., 3 minutes.
14. Blow dry with N_2.
15. Observe under microscope. Repeat 200 seconds deep - UV exposure and 30 second SAL 101 development if resist fringes are visible.

D Oxygen Plasma Descum of Photoresist

Warning: Oxygen plasma descum damages the surface, increasing DC - RF dispersion. Minimum descum time is recommended.

1. chamber pressure = 300mT of O_2
2. Power = 100W at low frequency.
3. Run for 10 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O :: 1 : 8.
2. Dip in dilute HCl for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2

F Evaporation

1. Place wafer on E-Beam mount. Lower boom by 7.5 cm. (31.5 cm from source). Level it. At this height, for a crystal monitor reading of 1.75 μm the actual thickness was calibrated to be 2.5 μm.
2. Always use a new crystal for bond pad evaporation.
3. Pump down to below $1.5 \cdot 10^{-6}$ torr.
4. Deposit material:

Warning: Use the small crucible for Au - be sure to fill it completely. If charge is less Au might run out before the desired thickness is reached. Do not let it overflow, then it might spill out of the crucible while melting.
Warning: As the evaporation rate for Au is high, and the boom is lowered the chances of spitting is high. Be on a constant look out during the evaporation.

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
Ti	200	1-2	1.55
Au	17500	20	1.65
	(crystal reading)		

G Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. Squirt with ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone.
4. Rinse with ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Expose in deep - UV for 200 seconds.
8. Develop in SAL 101 for 1 minute.
9. Rinse in running DI water for 3 minutes.
10. Blow dry with N_2.
11. Observe under microscope for resist fringes.
12. Expose in deep - UV for 200 seconds.
13. Develop in SAL 101 for 30 seconds.
14. Rinse in running DI water for 3 minutes.
15. Blow dry with N_2.
16. Check under microscope, then Dektak thickness of metal.

H Test transistors

1. Check for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.
3. Use 3 probe measurement set up to test the FETs.

B.7 Dicing GaN wafer (no mask required)

A Solvent Cleaning GaN Wafer

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 10 seconds.
3. Hot ISO 3 minutes, ultrasonic 10 seconds.
4. Running DI 3 minutes.
5. Blow dry with N_2.
6. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Protection of Top Surface

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
Warning: It is advisable to do an expo at the first mask level to find the optimum focus and exposure. The conditions mentioned here will vary with wafer thickness, lamp intensity and photoresist life.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ 4330 with syringe and filter to cover wafer.
4. Spin at 6.0 krpm for 30 seconds.
5. Soft Bake, 90°C, 30 minutes in petri dish without cover.

C Solvent Cleaning Carrier 2" Si Wafer

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot METH 3 minutes, ultrasonic 30 seconds.
4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

D Bonding to Carrier Wafer

Warning: If the die sizes are < 2 mm $\times$ 2 mm, brown bonding XX wax is preferred as it provides better adhesion compared to the crystalbond-509 mounting wax.
Warning: The melting point of the wax are high enough (150°C for brown wax and 120°C for crystalbond-509 mounting wax) to degrade the resist on the wafer. So the bonding should be done immediately after removing the carrier wafer from the hot plate, before the wax starts hardening. Hard baking the resist would make it impossible to remove the resist scum from the individual dice.
Warning: Any air bubbles under the bonded wafer would cause dice to fall off from the carrier substrate while dicing.

1. Place the carrier wafer on the hot plate at the melting point of the wax used.
2. Use the wax stick and apply a thin layer of wax evenly over wafer.
3. Remove wafer from the hot plate, once wax melts.
4. Place the GaN wafer immediately over the melted wax, and apply pressure evenly to remove any air bubbles underneath the wafer.
5. If the wax hardens before getting a even bonding, place the carrier substrate with the GaN wafer on the hot plate at 120°C for 5 - 10 seconds and repeat the procedure.

6. Measure the thickness with a micrometer to verify if the bonding is planar. if the substrate is not planar with the carrier the saw may be damaged while dicing.

E Setting up the Dicing Saw

Warning: Always leave the compressed air on the saw, even while the saw is off. If the spindle is turned without the compressed air on, it can be severely damaged.

Warning: If you need to stop the saw in an emergency, press the *EM STOP* button

1. Turn on the power to the monitor, CCTV camera box and the dicing saw.
2. Turn on the water to the saw.
3. For 0.1 - 0.5 mm thick sapphire substrates, thermocarbon resin-bonded blade model 2.050-8B-54RU7-3 is recommended with feed rate of 0.7 mm/second or lesser. If a different blade is in use or if it is worn out, change the blade following the procedure mentioned in the dicing room.
4. Do a *SET UP* of the saw to set the Z axis reference. It should be done at the beginning of every session and after changing blades. It should be done without any wafer on the chuck.
   (a) blow off any water on the chuck.
   (b) turn on the spindle by pressing *[SPINDLE]*.
   (c) turn on vacuum by pressing *[VACUUM]*.
   (d) press *[SET UP]*
   (e) the spindle lowers until the chuck is detected, then it resets and the *"SET UP"* indicator will light.
5. Select metric units by pressing *INCH/MM*, till the *"MM"* indicator lights.
6. Set the length the saw cuts along x - axis
   (a) press *SHIFT* until the *"CUT-STRK"* indicator lights.
   (b) enter *1* then *W* for round substrates.
   (c) enter the cut stroke distance in mm and press *W*.
   (d) the entered values will be indicated under *"BLOCK"* and *"DATA"*
7. Set the cut speed for the saw
   (a) press *SHIFT* until the *"CUT-SPD"* indicator lights.
   (b) enter *1* then *W* for 0.5 mm/second cut speed.
   (c) the entered values will be indicated under *"DATA"*
8. Set y index, the distance the saw steps in y - axis after each cut along x - axis.
   (a) press *SHIFT* until the *"Y-IND"* indicator lights and *"1"* is displayed under *"BLOCK"*.
   (b) enter y index in mm and press *W*.
   (c) the entered values will be indicated under *"DATA"*
   (d) press *SHIFT* until *"2"* is displayed under *"BLOCK"*.
   (e) enter the second y index parameter used by the saw after it rotates by 90° once the cuts along the x - axis are done in fully automatic operation.
   (f) the entered values will be indicated under *"DATA"*

9. Set z index, the distance from the bottom of the saw blade to the chuck surface during a cut, or the amount left uncut. Typically this is selected to dice through the wafer and 0.1 mm into the carrier Si substrate.
   (a) press *SHIFT* until the *"Z-IND"* indicator lights and *"1"* is indicated under *"BLOCK"*.
   (b) enter z index in mm and press *W*.
   (c) the entered values will be indicated under *"DATA"*
10. Set z back clearance, the distance from the bottom of the saw blade to the chuck when the chuck is repositioning for another cut. Typically this is sum of sample thickness, carrier Si substrate thickness and 5 mm safety margin.
   (a) press *SHIFT* until the *"Z-IND"* indicator lights and *"7"* is indicated under *"BLOCK"*.
   (b) enter the z back clearance in mm and press *W*.
   (c) the entered values will be indicated under *"DATA"*
11. Set blade compensation, the amount by which z index decreases after each cut to account for blade wear. Typically this is 0.01 mm for sapphire substrates.
   (a) press *SHIFT* until the *"Z-IND"* indicator lights and *"8"* is indicated under *"BLOCK"*.
   (b) enter the blade compensation in mm and press *W*.
   (c) the entered values will be indicated under *"DATA"*
12. Set Φ index, the angle in degrees the chuck will rotate before beginning the cut along the original y - axis. Typically this is 90°.
   (a) press *SHIFT* until the *"Φ-IND"* indicator lights and *"1"* is indicated under *"BLOCK"*.
   (b) enter the Φ index in degrees and press *W*.
   (c) the entered values will be indicated under *"DATA"*
13. Set the cut number, the number of cuts after which the saw will stop. This is important only in fully automated production environment, and is set to 9999 here.
   (a) press *SHIFT* until the *"CUT-NO"* indicator lights and *"3"* is indicated under *"BLOCK"*.
   (b) enter *9999* and press *W*.
   (c) the entered values will be indicated under *"DATA"*
14. Reset cut count, the number of cuts made on the current blade, while changing blades.
   (a) press *SHIFT* until the *"CUT-#"* indicator lights and *"1"* is indicated under *"BLOCK"*.
   (b) press *[C/E]* and then press *W* if you have changed blades.
   (c) the entered values will be indicated under *"DATA"*

F Wafer Mounting and Aligning

1. Place the wafer on the center of the chuck.
2. Turn on the vacuum using the *[VACUUM]* key. The vacuum gauge on the front of the saw should be in the green range. If it is not check for dirt on the chuck or back of the Si wafer.

3. Turn on the microscope illuminator using the *[ILLUMINATION]* key.
4. While indexing the chuck using the ← and → keys, align the wafer to the cut indicating cursors on the monitor.
5. Rotationally align the wafer using the ↩ and ↪ keys.
6. Align the wafer in the y axis using the ↗ and ↙ keys.
7. After aligning, make sure the last keys pressed were the green ↪ and ↗ keys. This sets the Φ and y axis reference points.
8. Verify the y index using the *[INDEX]* key.

G Dicing the wafer

1. New resin bonded blades must be "dressed" before use to remove any irregularities in the outer diameter and expose the diamond grit for cutting. Blade dressing is done by making several cuts across a Si wafer [86].
2. Move the chuck along y axis by pressing the *[INDEX]* and ↗ (or ↙) keys, to bring the exposed Si carrier underneath the blade. Press *[SPINDLE]*, *[SEMI AUTO]* and ↗ to begin the cut. Once the saw starts cutting press *[SEMI AUTO]* again to stop the saw after a single cut. Verify the alignment and make adjustments if necessary. Repeat the procedure two more times on the Si wafer.
   Warning: The water stream from the nozzle should be aimed at the interface between the saw and the substrate. Reposition the nozzle if necessary with a pair of pliers. Adjust the water flow with the needle valve on the flow meter.
3. Focus the optics using the silver knob on top of the optical housing. While looking through the eyepiece, align the optics to the cut using the silver knob located at the front of the housing. Align the cursors on the monitor to the cut using the *X1* and *X2* knobs on the CCTV interface box.
4. Move the chuck along y axis by pressing the *[INDEX]* and ↗ (or ↙) keys, to bring the sapphire substrate underneath the spindle. Verify the alignment on the monitor and begin dicing by pressing the *[SEMI AUTO]* and ↗ keys.
5. Stop after the last cut, by pressing *[SEMI AUTO]* before the last cut along the x axis starts. Rotate the wafer by 90°, by pressing *[INDEX]* and ↪ keys.
6. Align the wafer and begin dicing by pressing the *[SEMI AUTO]* and ↗ keys. Stop after the last cut, by pressing *[SEMI AUTO]* before the last cut starts. Stop the spindle by pressing *[SPINDLE]*.
7. Blow dry the wafer and chuck and remove the wafer after turning off the vacuum.
8. Turn off the saw, monitor, CCTV interface box, water flow and the lights before leaving.

H Die Removal and Cleaning

Warning: Do not let ACE dry on wafer.

1. Dice bonded with crystalbond-509 are removed using ACE, and those bonded with brown XX wax are removed in hot METH.
2. Keep the dice immersed in ACE to remove the photoresist.
3. Cold ACE 3 minutes, ultrasonic 30 seconds.

4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Verify under microscope to check if the dice are cleared of all dust deposited during dicing. Repeat the cleaning procedure using longer ultrasonic if necessary.

B.8 Bonding GaN wafer (no mask required)

A Solvent Cleaning GaN die

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 10 seconds.
3. Hot METH 3 minutes, ultrasonic 10 seconds.
4. Hot ISO 3 minutes, ultrasonic 10 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Flip Chip Bonding

1. Calibrate the bonder using the calibration substrates. Follow the instructions in the manual to get a good xy and collimeter alignment between the top and bottom camera probes.
2. Select upper chuck based on the die size (smaller die sits on the upper chuck). Clean off with ISO soaked wipes. Switch Pedestal VAC switch on front down to remove or place chuck, then switch it back up.
3. Always do few test runs with bad dice before using the best ones. Place GaN die on upper chuck, AlN die on lower chuck.
4. Hit UP VAC, LO VAC.
5. Do a xy and collimeter alignment of the two dice using the alignment marks.
6. Turn z micrometer on side of bonder to ~ 5.
7. Hit *RISER* to move the lower chuck up.
8. Move the lower chuck closer to the top chuck using the stage micrometer.
9. Set up the automatic bonding program. The optimum pressure and temperature for bonding will depend on the total cross-sectional area of the bonds. So a few test runs are recommended. For a 0.25 mm^2 total bond pad cross-section a pressure of 3000 g at a temperature of 250°C (both chucks) for 1 minute works well.
10. Begin automatic bonding sequence.
11. Once the bonding is finished, bring the riser down, unlock the clamp and remove the bonded dice.
12. Observe through the microscope (through the transparent sapphire substrate) to check alignment and planarity of the bonds.
13. Measure the D.C. I-V curves to check for shorts and to verify if all the pads are bonded.

Appendix C

Detailed AlN substrate process flow

C.0 Focus Check With 2” Si Wafer

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Set spinner for 4 krpm for 2 minutes.
3. Get 2” Si wafer from dry box (in old toluene petri dish).
4. Start wafer spinning, then squirt with acetone.
5. Don’t let it dry, squirt with ISO, then ACE and ISO again.
6. Put on 200°C hot plate for 5 minutes.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 1 minute. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Use “Smartset Array” mask plate, run job as follows: “FOCUS SFOC2\FOC”, note down the best focus number returned by computer.

C.1 Resistors(mask layer 1, nichrome, dark field)

A Solvent Cleaning

Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot METH 3 minutes, ultrasonic 30 seconds.
4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on 2" o-ring spinner chuck with vacuum, blow with N_2.
3. Apply SPR 950-0.8 with syringe and filter to cover wafer.
4. Spin at 2.5 krpm for 30 seconds.
5. Soft Bake, 90°C, 2 minutes. on hot plate.
6. Apply CEM with syringe and filter to cover wafer.
7. Spin at 4 krpm for 30 seconds.
8. Expose for 1.5 seconds, set focus offset to -20.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 2 minutes 20 seconds.
4. Rinse in running D.I., 3 minutes.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 seconds longer.

D Oxygen Plasma Descum of Photoresist

1. chamber pressure = 300mT of O_2.
2. Power = 100W at low frequency.
3. Run for 20 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O :: 1 : 10.
2. Dip in dilute HCl for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2

F Evaporation

1. Place wafer on E-Beam mount. Level it.
2. Put in a new crystal if the crystal monitor reads more than 15.
3. Pump down to below $1 \cdot 10^{-6}$ torr.
4. Deposit material:

Warning: NiCr is prone to spitting and needs to be evaporated with care. Move the beam over the source, keeping it focused, to get a more uniform Ni to Cr ratio.

Material	Thickness(Å)	Dep. Rate (Å/s)	Approx. Vernier
NiCr	475	1	1.75

G Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of nichrome.

C.2 Metal 1 (mask layer 2, metal1, clear field)

A Solvent Cleaning

Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot METH 3 minutes, ultrasonic 30 seconds.
4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply EIR 5214 with syringe and filter to cover wafer.
4. Spin at 4 krpm for 30 seconds.
5. Hot Plate Bake, 95°C, 2 minutes.
6. Expose for 0.4 seconds, set focus offset to -20.
7. Hot Plate Bake, 105°C, 2 minutes.
8. Flood Expose at 7.5 mW/cm2 for 30 seconds using Karl Suzs aligner.

C Development

1. Develop in two 300 ml beakers of AZ 400K : DI :: 1:5.5.
2. Develop for 40 seconds.
3. Rinse in running DI water for 3 minutes.

4. Blow dry with N_2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 seconds longer.

D Oxygen Plasma Descum of Photoresist

1. chamber pressure = 300mT of O_2.
2. power = 100W at low frequency.
3. run for 15 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O :: 1 : 10.
2. Dip in dilute HCl for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

F Evaporation

1. Place wafer on E-Beam mount. Level it.
2. Put in a new crystal if the monitor reads more than 8.
3. Pump down to below $1.5 \cdot 10^{-6}$ torr.
4. Deposit material:

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
Ti	200	2-3	1.65
Au	10000	15	1.5
Ti	100	2-3	1.65

Warning: Use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting.
Warning: It is very important to avoid spitting at this step as poor surface morphology of metal 1 can lead to shorts in Si_3N_4capacitor.

G Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of metal.

H Test Resistors

1. Check for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.

3. Use 4 probe measurement set up to measure the NiCr resistors and calculate the sheet resistance.
4. Do a burn in test to find the peak current carrying capacity of the resistors.

C.3 Capacitors (mask layer 3, nitride, clear field)

A Solvent Cleaning

1. Wipe lower electrode, housing of PECVD with ISO soaked wipes. Careful, HOT!
2. Run 60CLNSiN program.
   Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.
3. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
4. Cold ACE 3 minutes, ultrasonic 30 seconds.
5. Hot METH 3 minutes, ultrasonic 30 seconds.
6. Hot ISO 3 minutes, ultrasonic 30 seconds.
7. Running DI 3 minutes.
8. Blow dry with N_2.

B Silicon Nitride Deposition

1. Load wafer in PECVD, and run SiN25. Note down the wafer orientation.
2. Unload the wafer and rinse with ISO for 1 minute.
3. Load wafer in PECVD, rotate 90° from previous orientation and run SiN15.
4. Unload the wafer and let it cool for 5 minutes.

C Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Wafer on spinner chuck with vacuum, blow with N_2.
2. Apply SPR 518-A with syringe and filter to cover wafer.
3. Spin at 4 krpm for 30 seconds.
4. Hot Plate Bake, 90°C, 2 minutes.
5. Expose for 1.4 seconds, set focus offset to -20.
6. Hot Plate Bake, 110°C, 2 minutes.

D Development

1. Develop in full beaker of MF-701 for 1 minute. 30 seconds.
2. Rinse in running DI water for 3 minutes.
3. Blow dry with N_2.
4. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 seconds longer.

E Oxygen Plasma Descum of Photoresist

1. chamber pressure = 300mT of O_2.
2. power = 100W at low frequency.

3. run for 20 seconds.
4. Hardbake photoresist at 120°C for 20 minutes.

F Silicon Nitride Etch

1. Clean system with ISO and clean wipes.
2. O_2 clean of system as follows:
   (a) O_2 flow rate = 20.0 sccm.
   (b) chamber pressure = 10.0 mTorr.
   (c) Voltage=500 V.
   (d) Minimize reflected power by tuning.
3. Load sample, pump down to at least $1 \cdot 10^{-5}$ torr.
4. Etch conditions:
   (a) SF_6,O_2,Ar flow rate = 5.0, 3.0, 10.0 sccm.
   (b) chamber pressure = 20.0 mTorr.
   (c) Voltage=250 V.
   (d) Minimize reflected power by tuning.
   (e) Etch for 5 minutes.
5. Look under microscope. Etch in 1 minute increments if necessary.

G Resist strip

1. Remove photoresist with acetone in liftoff beaker for 3 minutes.
2. Rinse by spraying with METH and ISO.
3. Rinse in running DI water for 3 minutes.
4. Blow dry with N_2.

H Oxygen Plasma Photoresist Removal (optional, at your discretion)

1. chamber pressure = 300mT of O_2.
2. power = 100W at low frequency.
3. run for 30 seconds.
4. examine under microscope to ensure photoresist removal.

C.4 Metal 2 (mask layer 4, metal2, clear field)

A Solvent Cleaning

Safety Note: Keep hot solvents well under the splash guards. Always keep tweezers or some other boiling surface in a heated solvent to provide a boiling surface and prevent eruptions.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot METH 3 minutes, ultrasonic 30 seconds.
4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply EIR 5214 with syringe and filter to cover wafer.
4. Spin at 4 krpm for 30 seconds.
5. Hot Plate Bake, 95°C, 2 minutes.
6. Expose for 1.5 seconds, set focus offset to -20.
7. Hot Plate Bake, 105°C, 2 minutes.
8. Flood Expose at 7.5 mW/cm2 for 30 seconds.

C Development

1. Develop in two 300 ml beakers of AZ 400K : DI :: 1:5.5.
2. Develop for 40 seconds.
3. Rinse in running DI water for 3 minutes.
4. Blow dry with N_2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 seconds longer.

D Oxygen Plasma Descum of Photoresist

1. chamber pressure = 300mT of O_2.
2. power = 100W at low frequency.
3. run for 15 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O :: 1 : 10.
2. Dip in dilute HCl for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

F Evaporation

1. Use the circular 2 " chuck with the motor for rotation.
2. Place wafer on E-Beam mount for angle of about 30° and connect the motor leads.
3. Put in a new crystal if the monitor reads more than 8.
4. Pump down to below $1.5 \cdot 10^{-6}$ torr.
5. Deposit material: do not forget to rotate the chuck.

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
Ti	200	2-3	1.65
Au	10000	15	1.5
Ti	100	2-3	1.65

Warning: Use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting.

G Liftoff

Warning: Do not let ACE dry on wafer!

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle).
5. Rinse in running DI water for 3 minutes.
6. Blow dry with N_2.
7. Check under microscope, then Dektak thickness of metal.

H Test Capacitors

1. Check the probes for continuity before using the probe station. The wires leading to the probes are known to frequently break within the insulation.
2. Use new probes if necessary.
3. Use 2 probe measurement set up to measure the capacitor breakdown voltage and to check for shorts.

C.5 Bond Pad and Post Metalization (mask layer 5, post, dark field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot METH 3 minutes, ultrasonic 30 seconds.
4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Application and Exposure
Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply PMGI - SF15 with syringe and dropper to cover wafer.
4. Spin at 3.5 krpm for 30 seconds.
5. Bake, 200 C, 2 minutes. on hot plate.
6. Remove SF15 threads from the corners using a clean razor.
7. Apply SPR 950-0.8 with syringe and filter to cover wafer.
8. Spin at 2.5 krpm for 30 seconds.
9. Soft Bake, 90 C, 1 minute. on hot plate.
10. Apply CEM 365 with syringe and filter to cover wafer.
11. Spin at 4 krpm for 30 seconds.
12. Expose for 1.4 seconds, set focus offset to -18.

C Development

1. Post Bake, 100°C, 2 minutes, 10 seconds.
2. Rinse in running D.I., 30 seconds.
3. Develop in MF-701 for 3 minutes. (over develop if necessary to remove photoresist scum)
4. Rinse in running D.I., 3 minutes
5. Blow dry with N_2.
6. Expose in deep - UV for 200 seconds.
7. Develop in SAL 101 for 1 minute.
8. Rinse in running D.I., 3 minutes.
9. Blow dry with N_2.
10. Observe under microscope for resist fringes.
11. Expose in deep - UV for 200 seconds.
12. Develop in SAL 101 for 30 seconds.
13. Rinse in running D.I., 3 minutes.
14. Blow dry with N_2.
15. Observe under microscope. Repeat 200 seconds deep - UV exposure and 30 second SAL 101 development if resist fringes are visible.

D Oxygen Plasma Descum of Photoresist

1. chamber pressure = 300mT of O_2
2. Power = 100W at low frequency.
3. Run for 10 seconds.

E Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O :: 1 : 8.
2. Dip in dilute HCl for 15 seconds.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2

F Evaporation

1. Place wafer on E-Beam mount. Lower boom by 7.5 cm. (31.5 cm from source). Level it. At this height, for a crystal monitor reading of 1.75 μm the actual thickness was calibrated to be 2.5 μm.
2. Always use a new crystal for bond pad evaporation.
3. Pump down to below $1.5 \cdot 10^{-6}$ torr.
4. Deposit material:

Material	Thickness($\AA$)	Dep. Rate ($\AA$/s)	Approx. Vernier
Ti	200	1-2	1.55
Au	17500 (crystal reading)	20	1.65

Warning: Use the small crucible for Au - be sure to fill it completely. If charge is less Au might run out before the desired thickness is reached. Do not let it overflow, then it might spill out of the crucible while melting.
Warning: As the evaporation rate for Au is high, and the boom is lowered the chances of spitting is high. Be on a constant look out during the evaporation.

G Liftoff

Warning: Do not let ACE dry on wafer!
Warning: Do not leave the wafer soaking in ACE overnight, as ACE degrades the PMGI beneath the resist over prolonged exposure. The PMGI layer is required for air bridge mask step.

1. Soak wafer in beaker of ACE until metal comes loose, minimum time recommended.
2. Squirt with ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone.
3. Rinse with ISO (squirt bottle).
4. Rinse in running DI water for 3 minutes.
5. Blow dry with N_2.
6. Check under microscope, then Dektak thickness of metal.

Note: If the PMGI surface has cracks, remove it completely following the steps below. Then redo the post lithography and development as above. Reflow the new PMGI around the previously evaporated post and bond pad metal by heating it to 200°C for 2 minutes. Proceed with the next mask step.

1. Expose in deep - UV for 200 seconds.
2. Develop in SAL 101 for 1 minute.
3. Rinse in running DI water for 3 minutes.
4. Blow dry with N_2.
5. Observe under microscope for resist fringes.
6. Expose in deep - UV for 200 seconds.
7. Develop in SAL 101 for 30 seconds.
8. Rinse in running DI water for 3 minutes.
9. Blow dry with N_2.
10. Check under microscope, then Dektak thickness of metal.

C.6 Air Bridge Metalization (mask layer 6, airbridge, dark field)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes.
3. Cold METH 3 minutes.
4. Cold ISO 3 minutes.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Surface Preparation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases. Wear face shield at all times while at acid hood.

1. Mix $KI_2/I_2/H_2O : H_2O :: 1 : 5$
2. Etch for 5 seconds.
3. Rinse in DI for 3 minutes.

4. Blow dry with N_2.
5. Mix a dilute solution of HCl : H_2O :: 1 : 10.
6. Dip in dilute HCl for 15 seconds.
7. Rinse in DI for 3 minutes.
8. Blow dry with N_2.

C Evaporate Flash layer

1. Use the circular 2 " chuck with the motor for rotation.
2. Place wafer on E-Beam mount for angle of about 30° and connect the motor leads.
3. Put in a new crystal if the monitor reads more than 8.
4. Pump down to below $1.5 \cdot 10^{-6}$ torr.
5. Deposit material: do not forget to rotate the chuck.

Material	Thickness($\mathring{A}$)	Dep. Rate ($\mathring{A}$/s)	Approx. Vernier
Ti	300	2-3	1.65
Au	1000	10	1.45
Ti	100	2-3	1.65

Warning: Use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting.

D Photoresist Application and Exposure

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Immediately take wafer from the e-beam evaporator to the photoresist bench.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ P4330-RS with syringe and filter to cover wafer.
4. Spin at 6 krpm for 30 seconds.
5. Soft Bake, 90°C, 30 minutes in petri dish without cover.
6. Cool down after soft bake, 10 minutes.
7. Expose for 1.4 seconds, set focus offset to -20.

E Development

1. Develop in two 300 ml beakers of AZ 400K : DI :: 1 : 4.
2. Develop for 120 seconds.
3. Rinse in running DI water for 3 minutes.
4. Blow dry with N_2.
5. Observe under microscope. If there is some photoresist scum in the post holes develop for 10 - 20 seconds longer.
6. Flood expose for 2 minutes using the Karl Suzs aligner.

F Oxygen Plasma Descum and Hard Bake of Photoresist

1. chamber pressure = 300mT of O_2.
2. power = 100W at low frequency.
3. run for 15 seconds.
4. post bake at 120°C for 30 minutes in petri dish without cover.

G Plating Preparation

1. Clean beaker, anode, cathode and magnet with ISO and DI water.
2. Rinse in DI for 3 minutes.
3. Heat 800 ml of plating solution in beaker with short stirrer bar to 55°C.

H Titanium Etch

1. Dektak photoresist and record initial thickness.
2. Use a swab with ACE to remove the photoresist on four corners of the substrate. This is used to make electrical contact.
3. Mix HF : DI H_2O :: 1 : 20.
4. Etch top layer of Ti for $\sim$ 25 seconds (10 seconds after surface appears golden).
5. Rinse in DI for 3 minutes.

I Gold Plating

1. The plating rate depends on the size of the wafer, number of air bridges on it and the age of the plating solution. Start with a plating current of 2 mA for a 2" square substrate ($\sim$ 2.2 μm/hour for a new solution).
2. Plate for 15 minutes with stirrer bar set to 300 rpm and temperature at 55°C.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.
5. Dektak the photoresist and calculate how much the depth has changed.
6. Adjust the current to get a plating rate of 2 μm/hour.
7. Repeat steps above to keep close track of the plating rate
8. Plate until the top of the air bridges are even with the photoresist, for a total thickness of 3 μm.

J Top Photoresist Layer Removal

1. Develop in two 300 ml beakers of AZ 400K : DI :: 1 : 1.
2. Develop for 60 seconds in the first beaker.
3. Develop for 30 seconds in the second beaker.
4. Rinse in running DI water for 3 minutes.
5. Blow dry with N_2.
6. Observe under microscope. If there is some photoresist scum in the post holes develop for 10 - 20 seconds longer.

K Oxygen Plasma Descum of Photoresist

1. chamber pressure = 300mT of O_2.
2. power = 200W at low frequency.
3. run for 1 minute.

L Etch First Titanium Layer

1. Use HF : DI H_2O :: 1 : 20 from before.
2. Etch top layer of Ti for $\sim$ 30 seconds with moderate agitation (10 seconds after surface appears golden).
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

M Etch Gold Layer

1. Mix new etchant $KI_2/I_2/H_2O : H_2O :: 1 : 5$
2. Etch initially for 5 seconds using stirrer bar.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.
5. Inspect under microscope.
6. If some gold is left, etch further for 5 seconds.
7. Repeat the above steps if necessary.
8. Rinse in DI for 3 minutes.
9. Blow dry with N_2.

N Etch Bottom Titanium Layer

1. Use HF : DI H_2O :: 1 : 20 from before.
2. Etch top layer of Ti for $\sim$ 30 seconds with moderate agitation (10 seconds after surface appears golden).
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.

Safety Note: Leave the PMGI layer underneath as a protection for air bridges while dicing. It could be removed after dicing the wafer.

C.7 Dicing AlN wafer (no mask required)

A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes, ultrasonic 10 seconds.
3. Hot METH 3 minutes, ultrasonic 10 seconds.
4. Hot ISO 3 minutes, ultrasonic 10 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Photoresist Protection of Top Surface

Safety Note: The vapors from photoresist are extremely harmful. Never breathe if you put your head under the hood.
Warning: It is advisable to do an expo at the first mask level to find the optimum focus and exposure. The conditions mentioned here will vary with wafer thickness, lamp intensity and photoresist life.

1. Cool down after dehydration, 5 minutes.
2. Wafer on spinner chuck with vacuum, blow with N_2.
3. Apply AZ 4330 with syringe and filter to cover wafer.
4. Spin at 6.0 krpm for 30 seconds.
5. Soft Bake, 90°C, 30 minutes in petri dish without cover.

C Setting up the Dicing Saw

Warning: Always leave the compressed air on the saw, even while the saw is off. If the spindle is turned without the compressed air on, it can be severely damaged.
Warning: If you need to stop the saw in an emergency, press the *EM STOP* button

1. Turn on the power to the monitor, CCTV camera box and the dicing saw.
2. Turn on the water to the saw.
3. For 0.1 - 0.5 mm thick AlN substrates, thermocarbon resin-bonded blade model 2.050-4B-22RU7-3 is recommended with feed rate of 1 mm/second or lesser. If a different blade is in use or if it is worn out, change the blade following the procedure mentioned in the dicing room.
4. Do a *SET UP* of the saw to set the Z axis reference. It should be done at the beginning of every session and after changing blades. It should be done without any wafer on the chuck.
   (a) blow off any water on the chuck.
   (b) turn on the spindle by pressing *[SPINDLE]*.
   (c) turn on vacuum by pressing *[VACUUM]*.
   (d) press *[SET UP]*
   (e) the spindle lowers until the chuck is detected, then it resets and the *"SET UP"* indicator will light.
5. Select metric units by pressing *INCH/MM*, till the *"MM"* indicator lights.
6. Set the length the saw cuts along x - axis
   (a) press *SHIFT* until the *"CUT-STRK"* indicator lights.
   (b) enter *1* then *W* for round substrates.
   (c) enter the cut stroke distance in mm and press *W*.
   (d) the entered values will be indicated under *"BLOCK"* and *"DATA"*
7. Set the cut speed for the saw
   (a) press *SHIFT* until the *"CUT-SPD"* indicator lights.
   (b) enter *1* then *W* for 0.5 mm/second cut speed.
   (c) the entered values will be indicated under *"DATA"*
8. Set y index, the distance the saw steps in y - axis after each cut along x - axis.
   (a) press *SHIFT* until the *"Y-IND"* indicator lights and *"1"* is displayed under *"BLOCK"*.
   (b) enter y index in mm and press *W*.
   (c) the entered values will be indicated under *"DATA"*
   (d) press *SHIFT* until *"2"* is displayed under *"BLOCK"*.
   (e) enter the second y index parameter used by the saw after it rotates by 90° once the cuts along the x - axis are done in fully automatic operation.
   (f) the entered values will be indicated under *"DATA"*
9. Set z index, the distance from the bottom of the saw blade to the chuck surface during a cut, or the amount left uncut. Leave about 0.1 mm of the AlN substrate uncut.
   (a) press *SHIFT* until the *"Z-IND"* indicator lights and *"1"* is indicated under *"BLOCK"*.
   (b) enter z index in mm and press *W*.
   (c) the entered values will be indicated under *"DATA"*
10. Set z back clearance, the distance from the bottom of the saw blade to the chuck when the chuck is repositioning for another cut. Choose this to be the sum of sample thickness and 5 mm safety margin.

(a) press *SHIFT* until the *"Z-IND"* indicator lights and *"7"* is indicated under *"BLOCK"*.
(b) enter the z back clearance in mm and press *W*.
(c) the entered values will be indicated under *"DATA"*

11. Set blade compensation, the amount by which z index decreases after each cut to account for blade wear. Typically this is 0.005 mm for AlN substrates.
    (a) press *SHIFT* until the *"Z-IND"* indicator lights and *"8"* is indicated under *"BLOCK"*.
    (b) enter the blade compensation in mm and press *W*.
    (c) the entered values will be indicated under *"DATA"*
12. Set Φ index, the angle in degrees the chuck will rotate before beginning the cut along the original y - axis. Typically this is 90°.
    (a) press *SHIFT* until the *"Φ-IND"* indicator lights and *"1"* is indicated under *"BLOCK"*.
    (b) enter the Φ index in degrees and press *W*.
    (c) the entered values will be indicated under *"DATA"*
13. Set the cut number, the number of cuts after which the saw will stop. This is important only in fully automated production environment, and is set to 9999 here.
    (a) press *SHIFT* until the *"CUT-NO"* indicator lights and *"3"* is indicated under *"BLOCK"*.
    (b) enter *9999* and press *W*.
    (c) the entered values will be indicated under *"DATA"*
14. Reset cut count, the number of cuts made on the current blade, while changing blades.
    (a) press *SHIFT* until the *"CUT-#"* indicator lights and *"1"* is indicated under *"BLOCK"*.
    (b) press *[C/E]* and then press *W* if you have changed blades.
    (c) the entered values will be indicated under *"DATA"*

D Wafer Mounting and Aligning

1. Place the wafer on the center of the chuck.
2. Turn on the vacuum using the *[VACUUM]* key. The vacuum gauge on the front of the saw should be in the green range. If it is not check for dirt on the chuck or back of the AlN substrate.
3. Turn on the microscope illuminator using the *[ILLUMINATION]* key.
4. While indexing the chuck using the $\leftarrow$ and $\rightarrow$ keys, align the wafer to the cut indicating cursors on the monitor.
5. Rotationally align the wafer using the $\hookleftarrow$ and $\hookrightarrow$ keys.
6. Align the wafer in the y axis using the $\nearrow$ and $\swarrow$ keys.
7. After aligning, make sure the last keys pressed were the green $\hookrightarrow$ and $\nearrow$ keys. This sets the Φ and y axis reference points.
8. Verify the y index using the *[INDEX]* key.

E Dicing the wafer

1. New resin bonded blades must be "dressed" before use to remove any irregularities in the outer diameter and expose the diamond grit for cutting. Blade dressing is done by making several cuts across a Si wafer [86].

2. Move the chuck along y axis by pressing the *[INDEX]* and ↗ (or ↙) keys, to bring the AlN substrate corner dies underneath the blade. Press *[SPINDLE]*, *[SEMI AUTO]* and ↗ to begin the cut. Once the saw starts cutting press *[SEMI AUTO]* again to stop the saw after a single cut. Verify the alignment and make adjustments if necessary.
   Warning: The water stream from the nozzle should be aimed at the interface between the saw and the substrate. Reposition the nozzle if necessary with a pair of pliers. Adjust the water flow with the needle valve on the flow meter.
3. Focus the optics using the silver knob on top of the optical housing. While looking through the eyepiece, align the optics to the cut using the silver knob located at the front of the housing. Align the cursors on the monitor to the cut using the *X1* and *X2* knobs on the CCTV interface box.
4. Move the chuck along y axis by pressing the *[INDEX]* and ↗ (or ↙) keys. Verify the alignment on the monitor and begin dicing by pressing the *[SEMI AUTO]* and ↗ keys.
5. Stop after the last cut, by pressing *[SEMI AUTO]* before the last cut along the x axis starts. Rotate the wafer by 90°, by pressing *[INDEX]* and ↪ keys.
6. Align the wafer and begin dicing by pressing the *[SEMI AUTO]* and ↗ keys. Stop after the last cut, by pressing *[SEMI AUTO]* before the last cut starts. Stop the spindle by pressing *[SPINDLE]*.
7. Blow dry the wafer and chuck and remove the wafer after turning off the vacuum.
8. Turn off the saw, monitor, CCTV interface box, water flow and the lights before leaving.

F Photoresist Removal

Warning: Do not let ACE dry on wafer.

1. Keep the substrate immersed in ACE to remove the photoresist.
2. Cold ACE 3 minutes, ultrasonic 30 seconds.
3. Hot METH 3 minutes, ultrasonic 30 seconds.
4. Hot ISO 3 minutes, ultrasonic 30 seconds.
5. Running DI 3 minutes.
6. Blow dry with N_2.

G Remove Bottom PMGI layer

1. Warm 1165 in a hot plate at 80°C for 10 minutes.
2. Immerse wafer in 1165 for 2 minutes with moderate agitation.
3. Rinse in DI for 3 minutes.
4. Blow dry with N_2.
5. Verify under microscope to check if the AlN substrate is cleared of all dust deposited during dicing. Repeat the cleaning procedure if necessary.

H Die Removal and Cleaning

1. Apply pressure on the dicing streets using a sharp tweezer or a scribe to break the substrate into individual dice.
2. Cold ACE 3 minutes.

3. Hot METH 3 minutes.
4. Hot ISO 3 minutes.
5. Running DI 3 minutes.
6. Blow dry with N_2.

C.8 Bonding AlN wafer (no mask required)

A Solvent Cleaning GaN and AlN dice

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.
2. Cold ACE 3 minutes.
3. Hot METH 3 minutes.
4. Hot ISO 3 minutes.
5. Running DI 3 minutes.
6. Blow dry with N_2.
7. Dehydration bake, 120°C, 30 minutes in petri dish without cover.

B Flip Chip Bonding

1. Calibrate the bonder using the calibration substrates. Follow the instructions in the manual to get a good xy and collimeter alignment between the top and bottom camera probes.
2. Select upper chuck based on the die size (smaller die sits on the upper chuck). Clean off with ISO soaked wipes. Switch Pedestal VAC switch on front down to remove or place chuck, then switch it back up.
3. Always do few test runs with bad dice before using the best ones. Place GaN die on upper chuck, AlN die on lower chuck.
4. Hit UP VAC, LO VAC.
5. Do a xy and collimeter alignment of the two dice using the alignment marks.
6. Turn z micrometer on side of bonder to ~ 5.
7. Hit *RISER* to move the lower chuck up.
8. Move the lower chuck closer to the top chuck using the stage micrometer.
9. Set up the automatic bonding program. The optimum pressure and temperature for bonding will depend on the total cross-sectional area of the bonds. So a few test runs are recommended. For a 0.25 mm^2 total bond pad cross-section a pressure of 3000 g at a temperature of 250°C (both chucks) for 1 minute works well.
10. Begin automatic bonding sequence.
11. Once the bonding is finished, bring the riser down, unlock the clamp and remove the bonded dice.
12. Observe through the microscope (through the transparent sapphire substrate) to check alignment and planarity of the bonds.
13. Measure the D.C. I-V curves to check for shorts and to verify if all the pads are bonded.

C Bonding AlN die to Cu heat-sink

1. Apply thin layer of silver epoxy on the 2" Cu block. Spread evenly with a sharp razor blade edge.

2. Place the AlN die (with the GaN die bonded to it) on top of the Cu block and slide it applying a little pressure.
3. Cure the epoxy at 170°C for 30 seconds using a hot plate
4. The bonded die is ready for on wafer testing.

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