University of California

Santa Barbara

# Ultra-high Bandwidth Heterojunction Bipolar Transistors and Millimeter-wave Digital Integrated Circuits

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering
by
Qinghung Lee

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June, 1999

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# Vita

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# Publications

1. Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie and M. J. W. Rodwell, "Submicron Transferred-Substrate Heterojunction Bipolar Transistors" , *to be published in IEEE Electron Device Letters*, August, 1999.

2. Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, S. Jaganathan, T. Mathew, S. Krishnan, S. Ceran and M. J. W. Rodwell, "Submicron Transferred-Substrate Heterojunction Bipolar Transistors with greater than 800 GHz $f_{max}$" , *presented in the 1999 IEEE Conference on InP and Related Materials, Switzerland, May*

3. Q. Lee, D. Mensa, J. Guthrie, S. Jaganathan, T. Mathew, S. Krishnan, S. Ceran and M. J. W. Rodwell, "66 GHz Static Frequency Divider in Transferred-substrate HBT Technology" , *to be presented at the 1999 IEEE MTT Symposium RFIC, CA, June*

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# Abstract


Ultra-high Bandwidth Heterojunction Bipolar
Transistors and
Millimeter-wave Digital Integrated Circuits

by
Qinghung Lee

Heterojunction bipolar transistors have applications in medium-scale integrated circuits operating at GHz frequencies. Target applications include microwave frequency direct digital synthesis, fiber-optic transmission chipsets and analog-digital converters. In these applications, both the transistor current gain cut-off frequency $f_\tau$, and the power gain cut-off frequency $f_{max}$ must be considerably higher than the signal frequencies involved. To permit clock rates exceeding 100 GHz, transistors with bandwidths of several hundred GHz are required. Obtaining high transistor bandwidth requires both vertical and lateral device scaling. The substrate transfer process has yielded scalable heterojunction bipolar transistors with submicron emitter-base and collector-base junctions, minimizing RC parasitics and increasing $f_{max}$ to 820 GHz. The high $f_{max}$ results from the scaling of HBT junction widths, from elimination of collector series resistance through the use of a Schottky collector contact, and from partial screening of the collector-base capacitance by the collector space charge. The process also provides a microstrip wiring environment on a low dielectric constant substrate. A static frequency divider fabricated from ECL flipflops with 76 transistor has demonstrated at 66 GHz clock frequency. The technology has the potential to yield ICs at 100 Gb/s clock rates.

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# Chapter 1

# Introduction

In the growing market of high bandwidth communication networks, there are increasing demands for high performance circuits that include microwave frequency direct digital synthesis[1], fiber-optic transmission chip-sets[2], [3], [4], [5] and analog-digital converters [6], [7] at GHz frequencies. The motivation for high circuit bandwidth varies with the application.

A typical fiber-optic communication system configuration is shown in figure 1.1. At the transmitter, a multiplexer (MUX) combines parallel input channels of low bit-rate data into one high bit-rate data stream. This high-speed electrical signal is amplified by a laser driver , and drives a laser diode, allowing the signal to be transmitted through the fiber. At the receiver, a photodiode converts the optical signal back to photocurrent. A transimpedance preamplifier transforms the photocurrent detected by the photodiode into a voltage signal. Then a main-amplifier amplifies the signal to a level regulated by an AGC loop. Decision circuits then regenerate the transmitted data in time and in amplitude. A clock recovery circuit extracts the clock from the data, as required by the data decision and demultiplexer (DEMUX) circuits. The recovered data is demultiplexed into parallel low bit-rate data channels. Improving the bandwidth of these electronic components will directly enable increased time division multiplexed (TDM) transmission rates. The transmission capacity can be further increased by wavelength division multiplexing (WDM).

Delta-sigma ADCs are a second emerging application for HBTs. These provide the high resolution required in radio receivers. Delta-sigma analog-to-digital converters (figure 1.2) modulate the analog input into single-bit

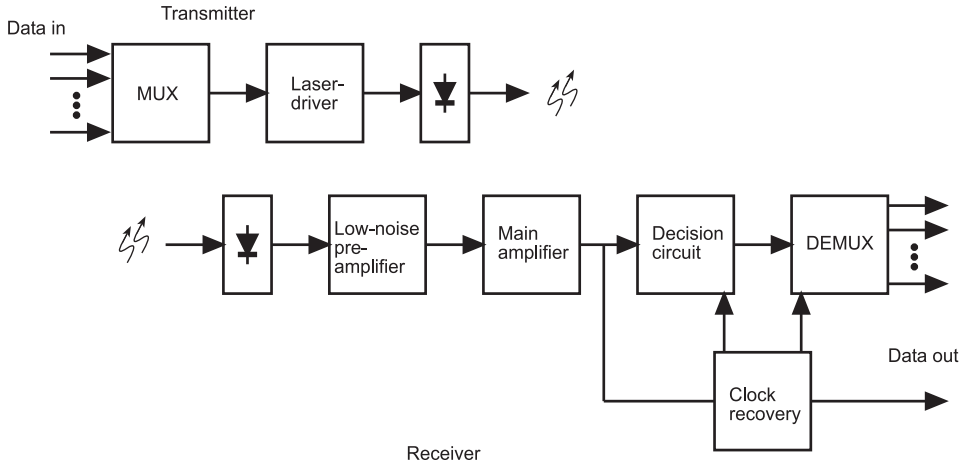



Figure 1.1: Basic transmitter and receiver configuration for a typical fiber-optical system.

words whose time-average value accurately represents the input. The conversion frequency is much higher than the necessary minimum-Nyquist rate. This oversampling spreads the quantization noise over a wide bandwidth. Placing the converter in a feedback loop with frequency-dependent gain shapes the quantization noise, so that most of the noise power is moved outside the bandwidth of interest. In this way higher sampling speed provides higher resolution. For over-sampled ($\Delta$-$\Sigma$) analog-to-digital converters, in-band quantization noise power decreases in proportion to the $5^{th}$ power of the oversampling ratio for $2^{nd}$-order modulators. Very high speed IC technologies offer the potential of $\Delta$-$\Sigma$ ADCs with clock frequencies in the 10's GHz, providing high dynamic range, -and large instantaneous bandwidth-over radio-frequencies and lower microwave frequencies.

Direct digital synthesis (DSS) can provide accurate, fast hopping, low phase noise and broad band generation of modulated sinusoidal signals. A DDS (figure 1.3) consists of three parts: a phase accumulator, a sine function read-only memory (ROM) look up table, and a digital-to-analog converter (DAC). Since frequency is the rate of phase change, the common phase increment word which is added to the phase accumulator each clock period determines the output frequency. A ROM look up table is used to convert the phase values to the sinusoidal amplitude value. The final step is to convert the digital amplitude data to an analog voltage. In direct

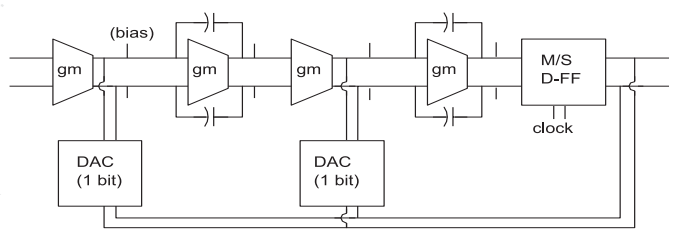



Figure 1.2: Block diagram of Delta-sigma A/D converter.

digital frequency synthesis (DDS), increases in logic IC rates and DAC bandwidths will result in increased synthesizer bandwidth. Used in radar transmitters, modulation bandwidths can then be increased and frequency agility improved.

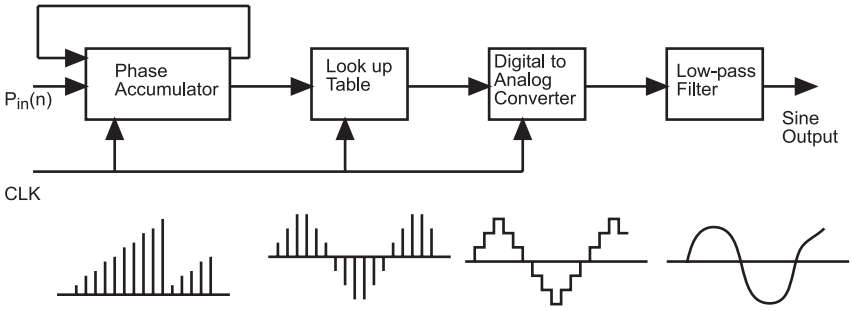



Figure 1.3: Block diagram of Direct Digital Synthesis.

A 100 GHz clock rate IC technology would permit significant advances in the performance of such signal conversion ICs. To permit clock rate exceeding 100 GHz, both the transistor current gain cutoff frequency $f_\tau$, and the power gain cutoff frequency $f_{max}$ must be considerably higher than the signal frequencies involved. HBTs with bandwidths of several hundred GHz are needed. Other issues in interconnects, packaging, and thermal design also must be addressed. Wiring parasitics must be minimized. Efficient heat sinking is essential. Good effective grounding is also vital.

Competing technologies for 100 GHz ICs include deep submicron SiGe bipolar transistors[8], InP/InGaAs[9] or InAlAs/InGaAs HBTs[10], and In-

AlAs/InGaAs HEMTs[11]. 0.1 $\mu$m InAlAs/InGaAs HEMTs have extremely high bandwidth (200-300 GHz $f_\tau$[12], 300-500 GHz $f_{max}$[13]) and had been used in applications above 40 GHz. Yet, the precision (0.1 $\mu$m) in photolithography and gate recess etch have limited the scale of integration of HEMT ICs [11]. Si/SiGe HBTs offer $\sim$ 100 GHz $f_\tau$ and $f_{max}$ with very high yield. Further, $\sim 10^6$ A/cm$^2$ current density in Si bipolar minimizes the emitter charging time, resulting in clock frequencies that are a higher fraction of $f_\tau$ than now obtained with III-V devices[8].

Heterojunction bipolar transistors have several advantages over Si-based and HEMTs technology, such as bandwidth, high transconductance per unit area and per unit current, high power density, high output resistance, low 1/f noise, a semi-insulating substrate, excellent linearity and threshold matching, etc. To win this competition, III-V HBT IC technology must offer transistor bandwidth equal to -or better than- HEMTs, and 3-5 times that of Si. The technology must also offer other features needed for high speed ICs, including low parasitic interconnects.

This thesis concentrates on developing a deep submicron transferred-substrate HBT IC process which can offer very high transistor bandwidth, low wiring capacitance, and low wiring inductance. A scalable HBT is developed which can be scaled to achieve high bandwidths for high-speed applications. Typically, HBTs are not scalable devices. The transferred-substrate process renders the HBT scalable and achieves record bandwidths. The wiring parasitics in this technology are minimized by using the low $\epsilon_r$ wiring dielectrics. Deep submicron transferred-substrate HBT fabricated by e-beam lithography with record device bandwidth (820 GHz $f_{max}$) have been demonstrated. The transferred-substrate HBT IC process using optical projection lithography has been developed and digital circuits consisting of 76 transistors in this technology with record clock-rate (66 GHz) have also been demonstrated.

# Chapter 2

# Submicron Lateral Scaling of Transferred-substrate HBTs

Progressive improvement in device bandwidths are needed to meet the demand for integrated circuits clocking at high frequencies. The scaling of device dimensions is essential for achieving large device bandwidth and a large integration level. Improvement in device bandwidth requires the scaling of devices, ie. lateral scaling by reducing the lithographic dimensions accompanied by vertical scaling by thinning the semiconductor epitaxial layer thickness. The dimensions of transistors in different semiconductor technologies have been progressively reduced over the past 30 years. This device scaling increased the packing density, reduced parasitic RC elements, and resulted in greatly increased device bandwidth. Clock rates of CMOS VLSI microprocessors have increased by a factor of 10 in the past decade, and should surpass 1 GHz as the gate lengths approach 0.1 $\mu$m.

Scaling has also been exploited to great success with III-V high-electron mobility-field-effect transistors (HEMTs). HEMTs fabricated with 0.1 $\mu$m gate lengths obtained a power gain cutoff frequency ($f_{max}$) of 450 GHz [13] and a current cutoff frequency ($f_\tau$) of 370 GHz [12]. Two results of 600 GHz $f_{max}$ have also been reported. The superior bandwidths of HEMTs is a result of the rapid improvement in HEMT bandwidth with deep submicron scaling.

Given the successful deep submicron scaling of MOSFETs and HEMTs, it is remarkable that both heterojunction bipolar transistors (HBTs) are typically fabricated at junction dimensions of 1-2 $\mu$m. Scaling emitter di-

mensions below $\sim$ 1 $\mu$m does not improve the device bandwidth of HBTs significantly. A HBT with smaller emitter width does not generally have a higher bandwidth. Figure 2.1 shows $f_{max}$ versus emitter dimension for some HBT technologies reported in the literature. It can be seen that there is no strong correlation between $f_{max}$ and emitter width except for the UCSB transferred-substrate HBT technology. Therefore, HBTs are not fabricated with deep submicron dimensions except to minimize bias current for the low power operation.

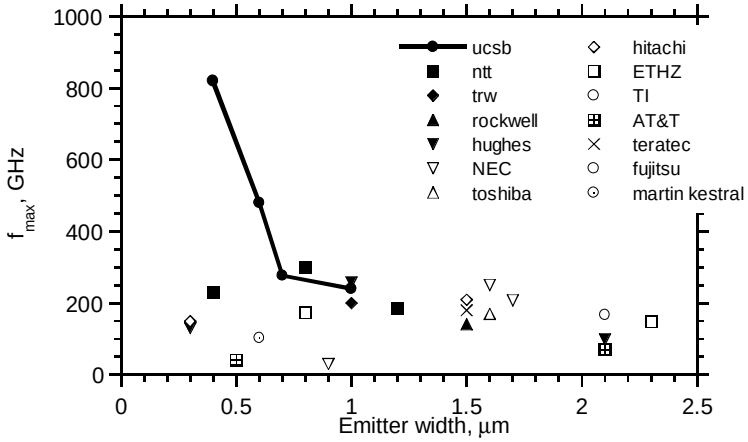



Figure 2.1: Comparison of $f_{max}$ and emitter dimensions for some HBTs in the literature.

Let us first review the factors which generally determine semiconductor device bandwidth. In all semiconductor devices, carriers drift in a depleted semiconductor layer. Semiconductor parasitics, such as the bulk semiconductor resistance, Ohmic contact resistance, lateral contact access resistance and the depletion layer capacitance, etc, will add RC charging time-constants to the diffusion/depletion transit time. These in combination determine the device bandwidth.

HEMTs and MOSFETs are lateral-transport devices, with the electron flux parallel to the plane of the wafer. Decreasing the lithographic dimensions, e.g. the gate length, reduces both transit times and device parasitics and consequently, a higher bandwidth results. To maintain low output con-

ductance, as the lateral dimensions are reduced, the vertical dimensions must be proportionally scaled. On the other hand, HBTs and RTDs are vertical transport devices, with the carrier transit times controlled by epitaxial layer thickness. In vertical transport devices, there are parasitic RC time-constants whose magnitude is strongly controlled by the widths of the semiconductor junctions. With the correct device structure, reducing the lateral dimension of the contact structures reduces the parasitic RC charging times, reducing vertical dimensions of the epitaxial layer reduces the transit time, and the transistor bandwidth increases rapidly with scaling.

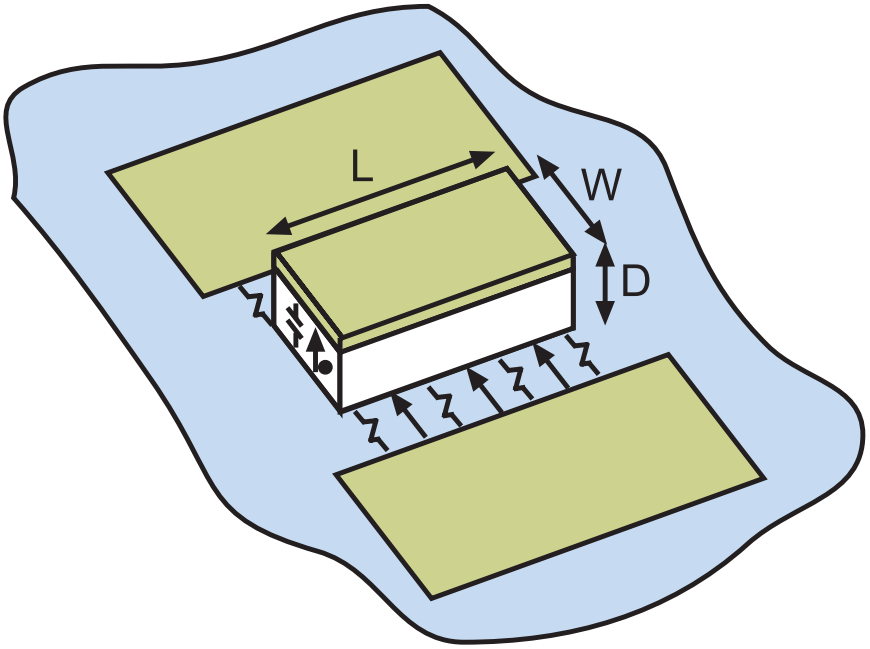
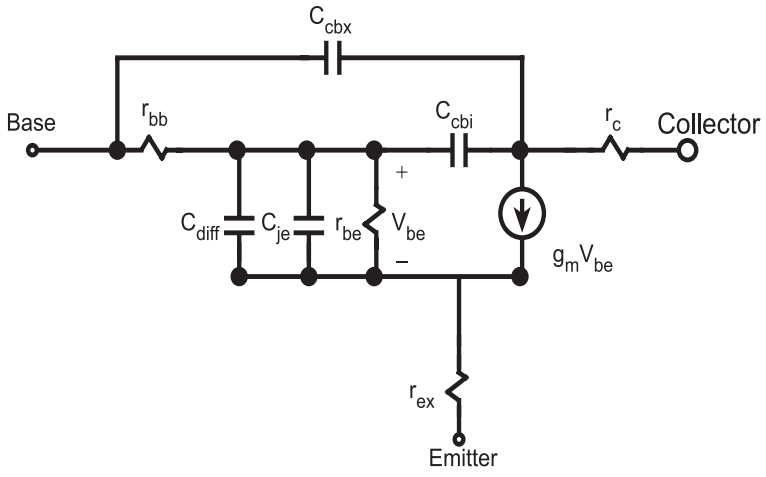



Figure 2.2: Scaling a Schottky diode.

The Schottky diode serves as a simple example (figure 2.2)of device scaling. Carrier transit time through the depletion region of a Schottky diode is proportional to the thickness (D) of the depletion region ($\tau_{transit} \propto D/v_{electron}$). Therefore, the bandwidth of the device with thick depletion layer is limited by the carrier transit time. Vertical scaling of the depletion region will reduce the carrier transit time, hence improve the device bandwidth; but this thinning of the depletion layer thickness D increases the depletion capacitance C ($C \propto WL/D$, where W is the semiconduc-

tor junction width, and L is the junction stripe length). Given the series resistance of the Ohmic contacts (R $\propto$ 1/L), the RC time constant is $\propto$ W/D. Therefore, extreme vertical scaling of the semiconductor layer will result in a device whose bandwidth is limited by the resistance-capacitance (RC) time-constant. Lateral scaling can be used in such a situation to reduce the RC time-constant. A Schottky contact with narrower width will have a lower capacitance, a lower spreading resistance, and an unchanged ohmic contact resistance. The RC time-constant is thus reduced. In vertical transport devices, transit times are reduced by deep submicron scaling of the semiconductor epitaxial layer thicknesses and RC time-constants are reduced by deep submicron scaling of the transverse junction dimensions.




| | |
|---|---|
| $r_{bb}$ base resistance | $C_{je}$ emitter-base junction capacitance |
| $r_c$ collector resistance | $C_{diff}$ emitter-base diffusion capacitance $g_m\tau_f$ |
| $r_{ex}$ emitter contact resistance | $\tau_f$ forward transit time $\tau_b + \tau_c$ |
| $r_{be} = \beta/g_m$ | $C_{cbi}$ intrinsic collector-base capacitance |
| $g_m = qI_c/kT$ | $C_{cbx}$ extrinsic collector-base capacitance |

Figure 2.3: Hybrid-$\pi$ model for an HBT.

As with most devices, the bandwidth of HBTs is determined by the combination of transit times and RC charging times. The RC time-constants are controlled by the HBT's lateral dimensions. We now briefly consider

the factors limiting the HBT bandwidth. A much more detailed analysis will be considered in chapter 3. Figure 2.3 shows a simplified small signal equivalent circuit model for an HBT. The expression for the short circuit current gain cutoff frequency $f_\tau$ is:

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{KT}{qI_c}\,(C_{je} + C_{cb}) + (r_{ex} + r_c)C_{cb}, \tag{2.1}$$

where $\tau_b$ is the base transit time, $\tau_c$ is the collector transit time, KT/q is the thermal voltage, $I_c$ is the collector current, $C_{je}$ is the emitter-base junction capacitance, $C_{cb}$ is the collector-base capacitance, $r_{ex}$ is the emitter contact resistance, and $r_c$ is the collector contact resistance. At a given current density, all terms except $(r_{ex} + r_c)C_{cb}$ in the above equation are independent of the lateral dimensions. The base and collector transit times can be reduced by vertically thinning the base and collector layers. Therefore, $f_\tau$ can be improved by vertical scaling of the epitaxial layer. Since $r_{ex}$ is inversely proportional to the emitter width, and $C_{cb}$ is proportional to the collector width, $r_{ex}C_{cb}$ is reduced by reducing the ratio of emitter to collector junction width.

The power gain cutoff frequency $f_{max}$ is another important figure-of-merit of high-frequency HBT performance. $F_{max}$ is the frequency at which the maximum available power gain $G_{max}$, and Mason's unilateral power gain U [14] are both unity. $f_{max}$ not only depends on $f_\tau$, but also on the base-resistance-collector-base-capacitance time constant as

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi r_{bb} C_{cbi}}}, \tag{2.2}$$

where $r_{bb}$ is the base resistance and $C_{cbi}$ is the fraction of the collector-base capacitance charged through $r_{bb}$. Power gain is available only at frequencies below $f_{max}$, no matter how large the value of $f_\tau$. Therefore, to improve device bandwidth, both $f_\tau$ and the $r_{bb}C_{cb}$ time-constant should be improved. The extrinsic collector-base capacitance has little effect on $f_{max}$, but it does affect the performance of many high speed circuits, and should also be minimized.

We now consider factors determining the $r_{bb}C_{cb}$ time-constants for an HBT. Figure 2.4 shows the schematic cross-section of a standard triple-mesa HBT. The base resistance $r_{bb}$ has three components. These are the contact resistance from the base ohmic contact, the sheet resistance from the gap between the emitter mesa and base ohmic contact, and the spreading

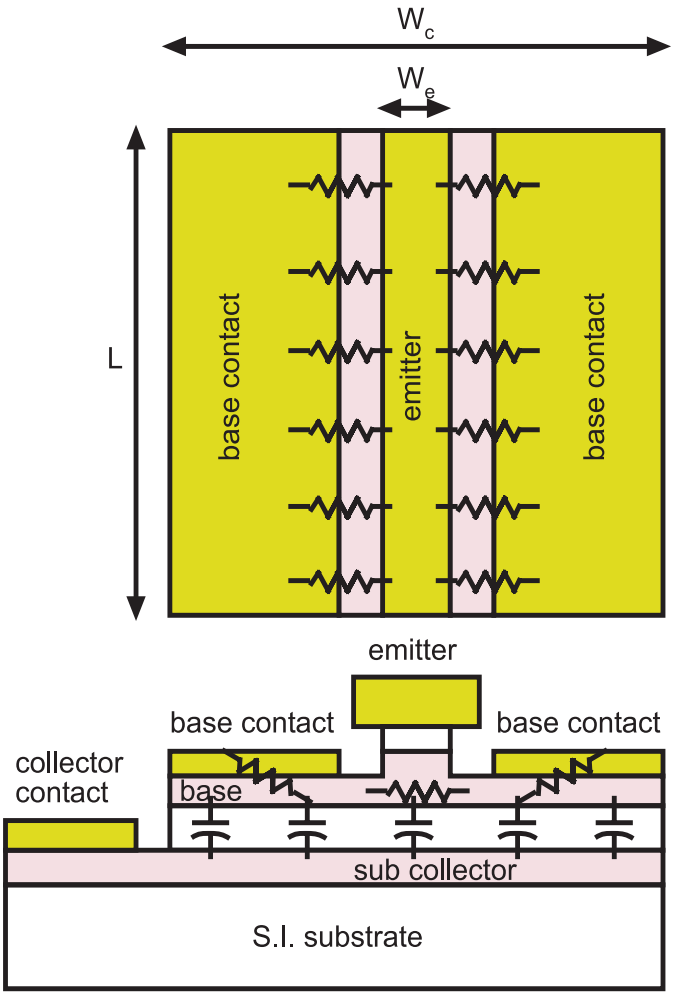



Figure 2.4: Schematic cross-section of a standard triple-mesa HBT.

resistance of the base layer underneath the emitter mesa. When the base ohmic is much larger than the contact transfer length $L_T$ ($= \sqrt{\rho_{bc}/\rho_{bs}}$), the contact resistance $R_{contact}$ is equal to $\sqrt{\rho_{bc}\rho_{bs}}/2L$, where $\rho_{bc}$ is the specific contact resistance per unit area of the metal-semiconductor interface (units of $\Omega$-cm$^2$), $\rho_{bs}$ is the base sheet resistivity (units of $\Omega/\Box$) and L is the emitter stripe length (units of $\mu$m). The gap resistance $R_{gap}$ is equal to $\rho_{bs}W_{gap}/2L$ where $W_{gap}$ is the separation between the emitter mesa and the base ohmic contact. For the standard self-aligned HBT process, $W_{gap} \leq 0.1$ $\mu$m, and $R_{gap}$ is fairly small and independent of the emitter width. The spreading resistance $R_{spread}$ is given by $\rho_{bs}W_e/12L$ where $W_e$ is the emitter width. Note that $R_{spread}$ is proportional to the emitter width $W_e$, but the $R_{gap}$ and $R_{contact}$ are independent of $W_e$. Therefore, for very narrow-emitter devices, the base resistance is dominated by the $R_{contact}$ and $R_{gap}$ and is only weakly dependent upon $W_e$. The minimum base resistance for a given stripe length, is set by the base contact resistance. The total collector-base capacitance $C_{cb}$ is proportional to $W_c$. The collector junction is defined in the same step as the base ohmic contacts, setting a minimum collector junction width equal to two base ohmic contact transfer lengths plus the emitter width, $W_c = 2L_T + W_e$. We then have $C_{cb} = \epsilon LW_c/T_c$, where $T_c$ is the thickness of the collector depletion region. Hence, the minimum collector-base capacitance is set by the minimum base contact size, and is independent of $W_e$. For narrow emitters, the base-collector time constant is

$$r_{bb}C_{cb} = W_e(2L_T)\cdot\frac{\epsilon}{T_c}\,\frac{\rho_{bs}}{12} + (2L_T)\cdot\frac{\epsilon}{T_c}\,\frac{\sqrt{\rho_{bc}\rho_{bs}}}{2}\ . \qquad (2.3)$$

Therefore, the $R_{bb}C_{cb}$ time-constant is very weakly dependent on $W_e$ for very narrow emitters. Hence lateral scaling of the emitter width below $\sim$ 1 $\mu$m does not significantly improve the device bandwidth of triple-mesa HBTs (figure 2.1).

To render the HBT scalable, significant changes must be made to the device structure. As discussed above, in the case of normal triple-mesa HBTs, the transfer length of the base ohmic contact sets a minimum size for the collector-base junction, regardless of lithographic limits. The parasitics ($r_{bb}C_{cb}$) associated with the HBT collector-base junction are therefore not addressed by scaling.

We have developed HBTs fabricated in a substrate transfer process. This transferred-substrate process allows one to lithographically define both

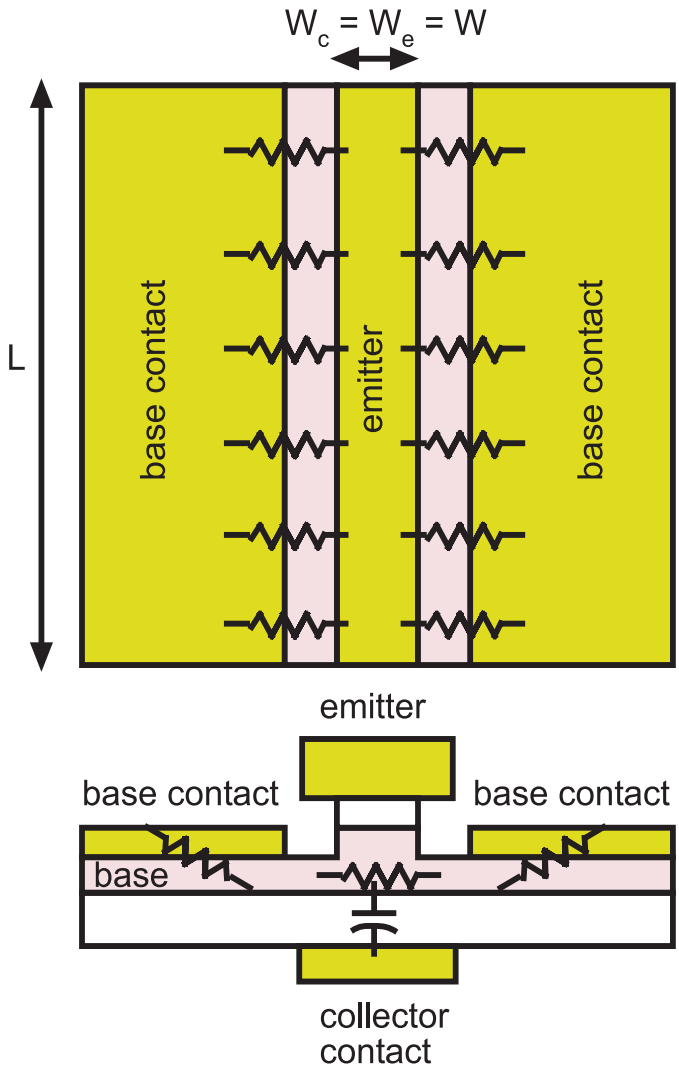



Figure 2.5: Schematic cross-section of a transferred-substrate HBT.

narrow emitter and collector stripes aligned to each other on opposite sides of the base epitaxial layer[15]. The collector-base capacitance $C_{cb}$ is proportional to the collector stripe width $W_c$ which can be determined by the lithography, independent of the base-mesa width. $r_{bb}C_{cb}$ becomes proportional to the process minimum feature size, and $f_{max}$ increases rapidly with scaling. Figure 2.5 shows a schematic cross-section of a transferred-substrate HBT. In transferred-substrate HBTs, the emitter and collector stripe widths are nearly equal ($W_e = W_c = W$), and the base-collector time constant is

$$r_{bb}C_{cb} = W^2 \cdot \frac{\epsilon}{T_c}\,\frac{\rho_{bs}}{12} + W \cdot \frac{\epsilon}{T_c}\,\frac{\sqrt{\rho_{bc}\rho_{bs}}}{2}\ . \tag{2.4}$$

The first term arises from the base spreading resistance and scales as $W^2$; the second term from the base ohmic contact resistance and scales as W. The $R_{bb}C_{cb}$ time-constant reduces rapidly with deep submicron scaling. Consequently, the power gain cutoff frequency $f_{max}$ ($\propto 1/\sqrt{W_e}$) rapidly improves with deep submicron scaling of the device for the transferred-substrate HBTs (figure 2.1). Bandwidth is improved simply because the collector junction width is proportional to the emitter junction width.

A comparison of $f_{max}$ obtained by the transferred-substrate HBT technology and the standard triple-mesa HBT technology is shown in figure 2.6. This figure was calculated using [28] the more accurate $f_{max}$ theory at chapter 3, using typical material parameters for InAlAs/InGaAs HBTs. It is observed that the transistor bandwidth dramatically increased for deep submicron emitter junction width in the transferred-substrate HBT technology.

In the transferred-substrate HBT technology, lateral scaling provides a secondary benefit of slightly improving $f_\tau$. Rewriting the expression for $f_\tau$ below:

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{KT}{qI_c}\,C_{je} + (\frac{KT}{qI_c} + r_{ex} + r_c)C_{cb}. \tag{2.5}$$

Collector resistance $r_c$ is eliminated in transferred-substrate HBTs through the use of the Schottky collectors. Further, $C_{cb}$ is low for a highly scaled collector, so $f_\tau$ at lower current density is improved due to $C_{cb}(kT/qI_e)$, and peak $f_\tau$ is improved due to lower $C_{cb}r_{ex}$.

In a given technology, except in oscillators, reactively-tuned amplifiers and distributed amplifiers where $f_{max}$ is the only determinant of the circuit bandwidth, both $f_\tau$ and $f_{max}$ are very important for circuit performance. Application to combined microwave/analog/digital circuits places a set of

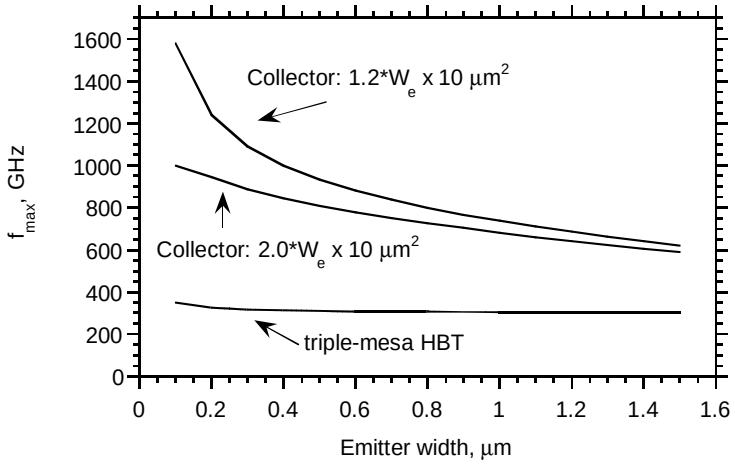



Figure 2.6: Comparison of the projected $f_{max}$ of the transferred-substrate HBT to the triple-mesa HBT.

demands on transistors. The requirements are summarized in Table 2.1.

For most applications, high $f_\tau$, as well as high $f_{max}$ is needed. Low collector capacitance and low base resistance are essential. To obtain usable devices, vertical scaling of the epitaxial layer thickness must accompany the lithographic scaling. Devices with $f_{max} \ll f_\tau$, obtained by thinning the epitaxial layers without lateral lithographic scaling will show circuit bandwidth limited by $r_{bb}$ and $C_{cb}$. Devices with $f_{max} \gg f_\tau$ (e.g. devices with relatively thick epitaxial layers and significant lateral lithographic scaling) will show circuit bandwidth limited by $(\tau_b + \tau_c)$. Reduction of $(\tau_b + \tau_c)$ is obtained by thinning the epitaxial layers, which unfortunately increases $r_{bb}C_{cb}$. The transferred-substrate HBT technology allows for the subsequent reduction of $r_{bb}C_{cb}$. A device with both high $f_\tau$ and $f_{max}$ is thus feasible.

Several approaches have been reported for reducing the collector-base capacitance of HBTs, and thereby improving $f_{max}$ and extrinsic collector capacitance $C_{cbx}$. One approach is the reduction of the width of the base mesa [16]. This relies on improvements in base contact technology because a narrow base mesa results in a smaller base ohmic contact area. The base contact width must be at least one transfer length if the contact resistance is to be kept small. In contrast, the transferred-substrate technique pro-

| Parameters | Digital | Analog | Microwave Power |
|---|---|---|---|
| $f_\tau$ | very high | very high | very high |
| $f_{max}$ | high | very high | very high |
| $r_{bb}$ | very low | low | very low |
| $C_{cb}$ | low | very low | low |
| $C_{be}$ | very low | low | low |
| $\beta$ | 20 | 10-30 | 10-20 |
| $V_{be}$ control | medium | good | low |
| Yield | very high | high | low |

Table 2.1: Requirements for HBT technology in different applications.

vides independent control of the base and collector contact widths. There have been other approaches to make the collector contact width independent of the size of the base contact, such as selective etching to undercut the collector [17], and collector isolation implantation [18]. However, in almost all cases, the scalability and controllability of these approaches has not been demonstrated and only moderate (10-30 %) increases in $f_{max}$ have been obtained. Transferred-substrate HBTs can be scaled to deep submicron dimensions with the use of powerful fine-line lithography for fabricating narrow emitter and collector stripes precisely. This leads to dramatic improvements in device bandwidth.

An interesting further advantage of the transferred-substrate HBT is the possibility of accommodating a Schottky collector. The important parasitics resistance $r_c$ in small area devices is due to the collector metal contact and semiconductor junction. Since the resistance of an ohmic contact, figure 2.7a, scales with its area, at small enough dimensions it may dominate over other resistances that scale with the contact perimeter. Therefore, a Schottky collector can be used instead of the $n^+$ doped semiconductor layer in the collector, figure 2.7b, so the $r_c$ is eliminated.

There are several issues regarding the deep submicron scaling of the transferred-substrate HBTs that need to be addressed.

Electron-beam and optical-stepper lithography tools are needed to define the deep submicron emitter and collector contact stripes.

To minimize the parasitic base resistance, a self-aligned emitter-base

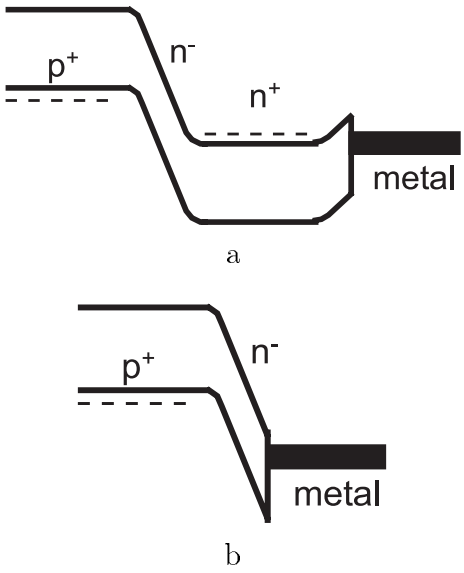



Figure 2.7: (a) Ohmic semiconductor-metal collector contact. (b) Schottky semiconductor-metal collector contact.

process in which the device features are defined by the same photoresist pattern is wanted. Therefore, precise dimensional control of the emitter/base mesa formation is essential. A dry etch technique is required to enable a reproducible, high yield, and size controllable deep submicron process technology. There are three basic approaches to self-aligned processing of HBTs. In the first, the emitter contact metalization is used as the dry etch mask for exposing the base, the dry-etch step is followed by wet chemical etch for damage layer removal and undercut emitter for the subsequent base metal lift-off. In the second self-aligned process, a dielectric dummy emitter is used as a etching mask to produce the undercut. After base metalization, the emitter contact is then deposited after removal of the initial dielectric layer. The third approach is to establish the emitter/base separation by using a sidewall spacer layer, comprised of either $SiO_2$ or $Si_3N_4$. The third process is a more controlled technique for $< 0.1$ $\mu$m emitter width device. In this work, the first approach is used, i.e. a very controlled 3-step combined reactive-ion dry and wet chemical etch.

Another important issue is that the collector has to be precisely aligned to the emitter and has to cover the emitter. To eliminate the excess

collector-base capacitance, the collector width must be as narrow as the emitter width plus the alignment tolerance. The effect of misalignment is to increase the average transit time of electrons from the emitter to the collector and thus reduce $f_\tau$ at given current density. Also, in the regions where there is no collector contact and hence no electric field to attract the electrons, the electrons tend to move under diffusive low-field transport. Hence, $f_{max}$ reduces drastically for misalignment devices. Ultimately, the collector scaling is limited by the lithographic tools' alignment tolerance.

The early work on AlGaAs/GaAs HBTs showed that lateral scaling results in a significant reduction in current gain. The physical origin is that electrons diffuse isotropically. When a bias is applied, an electron concentration gradient exits between the emitter/base and base/collector junctions (vertically), and also between the emitter/base junction and base ohmic contact (laterally). Therefore, electrons diffuse both vertically and laterally within the base. The recombination current between the exposed surface is then given by $J_{rec} = qnv_s$ where n is the concentration of electrons at the surface and $v_s$ is the surface recombination velocity. The calculation of the DC current gain involves solving the 2-dimensional diffusion equation in the base, where the boundary conditions are $J = qnv_{sat}$ at the collector-base junction and $J = nqv_s$ at the exposed surfaces of the base. Generally, as the aspect ratio of the emitter width to base thickness is decreased, the DC current gain will degrade. Therefore, a low surface recombination velocity is necessary to improve current gain. The recombination velocity of electrons on exposed surface of InGaAs base is known to be fairly low ($10^3$ cm/s compared to $10^6$ cm/s for GaAs). Another approach to increase the current gain is to vertically scale the base layer thickness, i.e. use a thinner base. For a fixed base thickness, a larger vertical velocity through the base can improve the lateral diffusion because the electrons spread laterally to a lesser extent and hence, the lateral recombination is reduced. This can be done by bandgap grading in the base to introduce a built-in electric field. Hence, for deep submicron lateral scaling, vertical scaling and bandgap engineering are needed to improve $f_\tau$ and the DC current gain.

In summary, the scaled transferred-substrate HBTs have the potential to out perform other competitive technologies by providing very high bandwidth devices. Other features of the technology important to high speed ICs, include low capacitance, low inductance wiring environment, and in addition, a copper substrate for heat sinking for dense circuits, are the

subject of J. Guthrie's thesis.

# Chapter 3

# $F_{max}$ in Transferred-substrate HBTs

## 3.1 Calculation of $f_{max}$ in Transferred-substrate HBTs

Power gain cutoff frequency $f_{max}$ is very important figure of merit for high frequency transistors performance. $f_{max}$ is the frequency at which the maximum available power gain $G_{max}$ or Mason's unilateral power gain U is unity. Power gain is available only at frequencies below $f_{max}$. For heterojunction bipolar transistors, $f_{max}$ is usually estimated by $f_{max} = \sqrt{f_\tau/(8\pi R_{bb} C_{cbi})}$. However, the equivalent circuit models of the real HBT device structures are usually more complicated than the simple hybrid-$\pi$ model used to derive the above relationship. In the simple hybrid-$\pi$ model, the base resistance and collector-base junction capacitance are treated as single, lumped elements, the distributed nature of the base resistance and the collector-base capacitance is ignored. Considering the distributed nature of these device parasitics, M. Vaidyanathan and D. Pulfrey [28] have derived an expression for the maximum oscillation frequency $f_{max}$ for the normal-mesa HBTs. The derivation is based on a general-form equivalent circuit that uses a network to represent the distributed nature of the base resistance and the collector-base capacitance, and also takes into account the parasitic emitter and collector resistance. While there remain simplifying assumptions in [28] which restrict the generality of the derivation of $f_{max}$, [28] provides a more

complete description than the simple 2-base-resistor model.

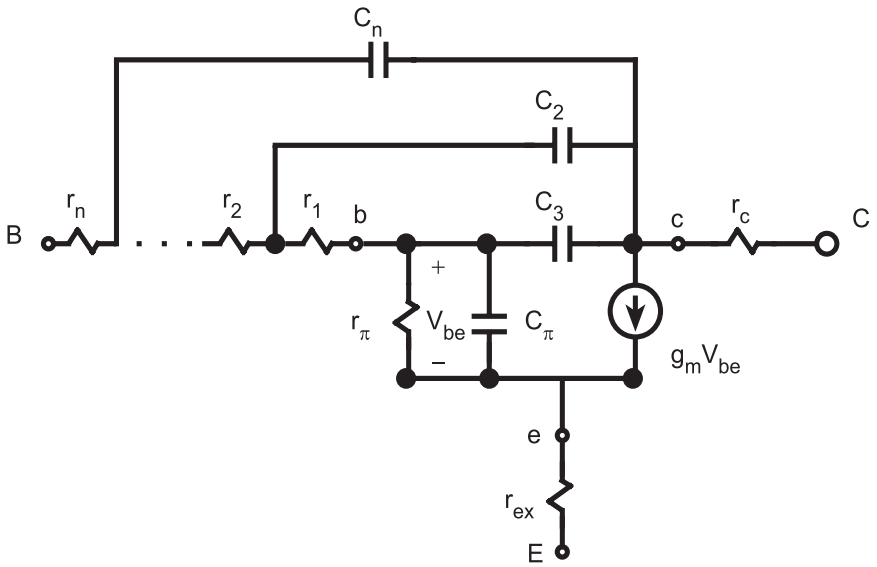



Figure 3.1: Equivalent circuit of a microwave HBT.

At high frequencies, the HBTs are modeled by the hybrid-$\pi$ circuits as shown in figure 3.1, the base resistance and the collector-base capacitance being represented as a distributed network: $r_1$, $r_2$, ..., $r_n$ and $C_1$, $C_2$,..., $C_n$. the total base resistance $r_{bb} = \Sigma_{j=1}^{n} r_j$ and the total collector-base capacitance $C_{cb} = \Sigma_{j=1}^{n} C_j$. The parasitic emitter resistance $r_{ex}$ and parasitic collector resistance $r_c$ are included in the circuit as well. Based on this equivalent circuit, by making reasonable assumptions regarding the relative sizes of the element values and the frequency range of interest [28], obtains the expression below for the extrapolated $f_{max}$:

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi(RC)_{eff}}}, \tag{3.1}$$

with $(RC)_{eff}$ given by the following:

$$(RC)_{eff} = (r_{bb}C_{cb})_{eff} + (\omega_T r_{ex} C_{cb})(r_\lambda C_{cb} - \Lambda) + (\omega_T r_c C_{cb})(r_{ex} + \frac{1}{g_m})C_{cb}, \tag{3.2}$$

where $(r_{bb}C_{cb})_{eff}$ is an effective base-collector time constant given by:

$$(r_{bb}C_{cb})_{eff} = r_{bb}C_{cb} - \Lambda, \tag{3.3}$$

where $r_{bb}$ is the total base resistance, $C_{cb}$ is the total collector-base junction capacitance, and $\Lambda$ is given by:

$$\Lambda = r_1(C_2 + C_3 + \cdots + C_n) + r_2(C_3 + C_4 + \cdots + C_n) + \cdots + r_{n-1}C_n. \tag{3.4}$$

Assumptions used in the derivation and a detailed calculation can be found in [28].

Given this expression, based on the exact physical structure of the HBT of interest, the best values for the elements $r_1$, $r_2$, ..., $r_n$ and $C_1$, $C_2$,..., $C_n$ can be chosen.

Now the above model is applied to the Schottky-collector transferred-substrate HBTs, the collector resistance $r_c$ is eliminated because of the Schottky collector contact. Further, assume that

$$\omega_T \ll \frac{1}{(r_{ex})C_{cb}} \tag{3.5}$$

where $\omega_T$ is the extrapolated, common-emitter, unity-current-gain frequency. Eq.( 3.5) is generally true for the transferred-substrate HBTs because of the small collector-base capacitance $C_{cb}$, therefore, the very high $f_{max}/f_\tau$ ratio. Hence, to a very good approximation, the $(RC)_{eff}$ can be simplified to

$$(RC)_{eff} = (r_{bb}C_{cb})_{eff} + (\omega_T r_c C_{cb})(r_{ex} + \frac{1}{g_m})C_{cb}, \tag{3.6}$$

because $r_c = 0$, the above equation can be further simplified to

$$(RC)_{eff} = (r_{bb}C_{cb})_{eff} = r_{bb}C_{cb} - \Lambda. \tag{3.7}$$

To find the appropriate values for $r_1$, $C_1$, etc, the device structures of the transferred-substrate HBTs must be examined. Figure 3.2 shows a schematic cross section of a transferred-substrate HBT structure, with the components of base resistance and base-collector capacitance labeled. First, the device with $W_c > W_E$ is considered. The case when $W_c = W_E$ will be discussed later. The base-collector junction structure is divided into four parts: an " intrinsic region " directly under the emitter junction

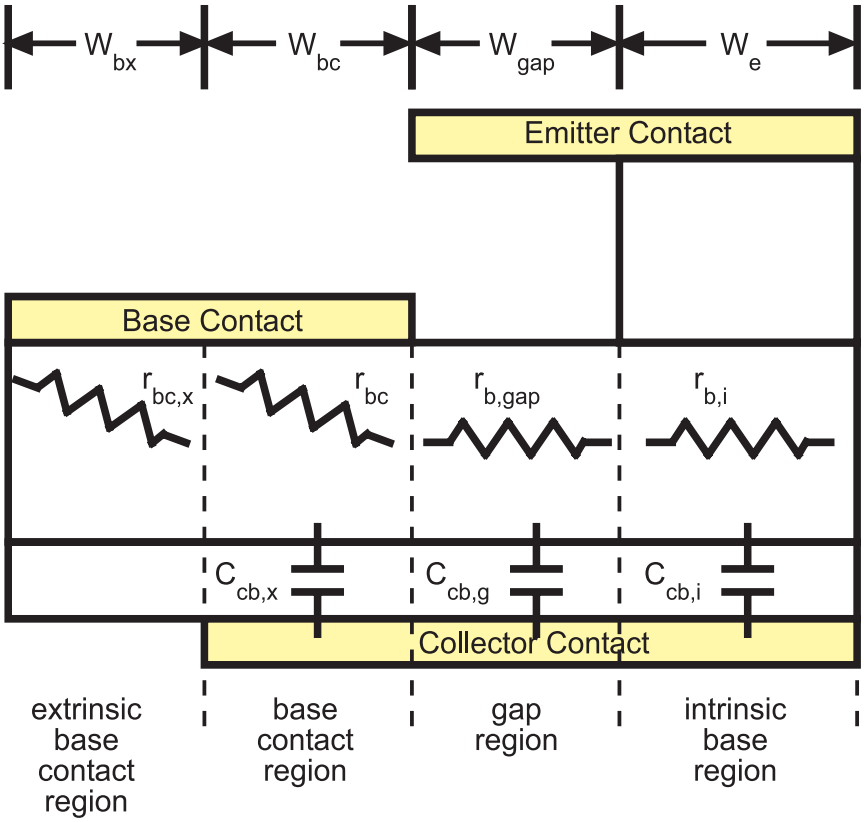
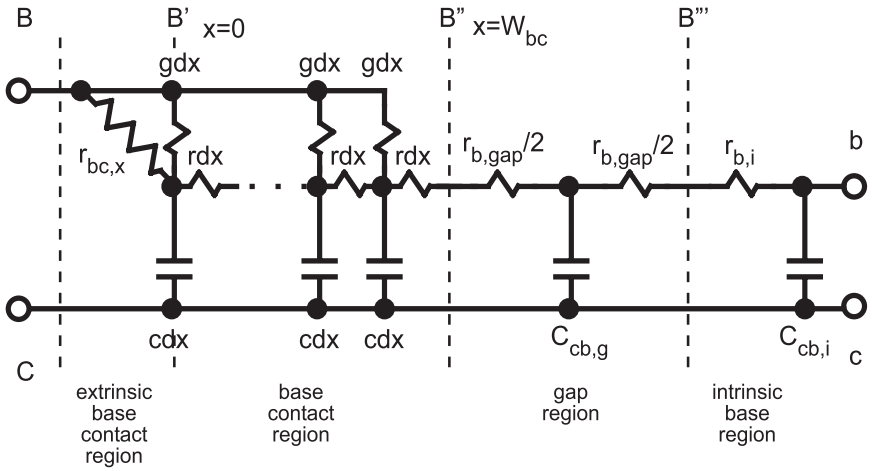



Figure 3.2: Schematic cross-section of a transferred-substrate HBT structure.

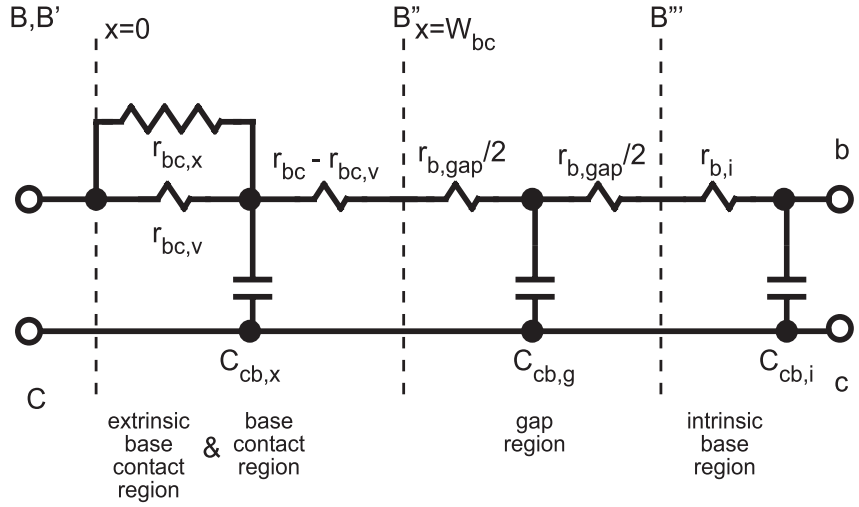
area; a " gap region " between the emitter mesa and base contacts; a " base-contact region ", which is the overlap between the base contact and collector contact; and the rest of the base contact region is called the " extrinsic base contact region ". The components of the base resistance are as follows: $r_{bc}$ is the base contact resistance, given by $r_{bc} = (\rho_{sb} L_T / 2L_{stripe})$, where $\rho_{sb}$ is the base sheet resistance ($\Omega/\Box$), $L_{stripe}$ is the length of the base contact perpendicular to the base current flow, and $L_T = \sqrt{\rho_v/\rho_{sb}}$ is so called "transfer length", where the $\rho_v$ is the vertical tunneling resistance of the base contact ($\Omega$-$\mu m^2$). $r_{b,gap} = \rho_{sb} W_{gap} / 2L_{stripe}$ is the gap resistance, where $W_{gap}$ is the separation between the emitter mesa and base Ohmic contact. $r_{b,i} = \rho_{sb} W_E / 12 L_{stripe}$ is the intrinsic base spreading resistance, where $W_e$ is the length of the base under the emitter. The components of collector-base junction capacitance shown in figure 3.2 are as follows: $C_{cb,x} = C_0 W_{bc} L_{stripe}$, $C_{cb,g} = C_0 W_{gap} L_{stripe}$, and $C_{cb,i} = C_0 W_e L_{stripe}$, where $C_0$ is the depletion capacitance per unit area for the collector-base junction: $C_0 = \epsilon_r \epsilon_0 / T_c$.

Figure 3.3 shows the distributed RC network for the base-collector junction structure described above. The region between B and B" is modeled as a distributed RC network and is part of a larger network that represents the base-collector junction structure as shown in figure 3.3. The region between B and B" is represented by distributing $C_{cb,x}$ over the distributed components of the vertical and horizontal base resistance. $\delta G = L_{stripe} \delta W / \rho_v$, $\delta R = \rho_{sb} \delta W / L_{stripe}$, and $\delta c = \epsilon L_{stripe} \delta W / T_c$. In [28], it is shown that at the frequencies of interest that the network in figure 3.3a can be reduced to that in figure 3.3b, where the circuit between B' and B" in figure 3.3a is replaced by the simple T circuit with the components $r_{bc,v}$, and $r_{bc}$ - $r_{bc,v}$, and $C_{cb,x}$. $r_{bc,v} = \rho_v / 2 W_{bc} L_{stripe}$, is the purely vertical part of the base contact resistance. This is proved next. In Figure 3.3a, the RC network between B' and B" can be treated as a two-port network with port 1 defined as between B' and C and port 2 defined as between B" and C. Assuming the boundary condition i(x=0)=0, one can solve the equation between x=0 and x=$W_{bc}$ (ie, the region between B' and B") to obtain the two-port open-circuit impedance (Z) parameters:

$$z_{11} = r_{bc,v} - \frac{j}{\omega C_{cb,x}}, \tag{3.8}$$




(a)




(b)

Figure 3.3: (a)Base-collector electrical network for a transferred-substrate HBT structure. (b) Reduced base-collector electrical network for a transferred-substrate HBT structure.

$$z_{21} = -\frac{j}{\omega C_{cb,x}}, \tag{3.9}$$

$$z_{12} = -\frac{j}{\omega C_{cb,x}}, \tag{3.10}$$

$$z_{22} = \frac{(R_{sh,b}/L_{stripe})coth(W_{bc}\Gamma)}{\Gamma} - \frac{r_{bc,v}}{1 + j\omega r_{bc,v} C_{cb,x}} - \frac{j}{\omega C_{cb,x}} \tag{3.11}$$

where $\Gamma = \sqrt{\delta r(\delta g + j\omega\delta C)} = (1/\mathrm{L}_T)\sqrt{1 + j\omega r_{bc,x} C_{cb,x}}$. At frequencies of interest, the expression for $z_{22}$ can be simplified to:

$$z_{22} \approx r_{bc} - r_{bc,v} - \frac{j}{\omega C_{cb,x}}. \tag{3.12}$$

In figure 3.3b, the T circuit $r_{bc,v}$, ($r_{bc}$ - $r_{bc,v}$) and $C_{cb,x}$ has the same values of $z_{11}$, $z_{21}$, $z_{12}$ as in ( 3.8)-( 3.10), and $z_{22}$ as in ( 3.12).

$F_{max}$ now can be calculated. Comparing figure 3.3b with figure 3.1, this establishes Pulfrey's relationship that n=3 and $r_1 = (r_{b,gap}/2 + r_{b,i})$, $r_2 = (r_{bc}$ - $r_{cv} + r_{b,gap}/2)$ and $r_3 = r_{bc,x}//r_{cv}$. Further, $C_1 = C_{cb,i}$, $C_2 = C_{cb,g}$, and $C_3 = C_{cb,x}$. Hence, for the transferred-substrate HBTs, the maximum oscillation frequency $f_{max}$ was obtained as follows:

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi(RC)_{eff}}}, \tag{3.13}$$

with

$$(RC)_{eff} = r_{bb} C_{cb,i} + (r_{cb,t} + \frac{r_{b,gap}}{2}) C_{cb,g} + r_3 C_{cb,x}, \tag{3.14}$$

where

$$r_{bb} = r_{b,i} + r_{b,gap} + r_{cb,t}, \tag{3.15}$$

$$r_{cb,t} = r_{cb} - r_{cb,v} + r_3 \tag{3.16}$$

$$r_3 = \frac{r_{bc,s} r_{cv}}{r_{bc,x} + r_{cv}} \tag{3.17}$$

We now consider the second case, when the collector width $W_c$ and emitter width $W_E$ are equal. The network between B' and B" does not exist. The base-collector network is much simpler, and the $r_3 = r_{cb}$ and $r_2 = r_{b,gap}/2$. The maximum oscillation frequency $f_{max}$ was obtained as follows:

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi(RC)_{eff}}}, \tag{3.18}$$

with

$$(RC)_{eff} = r_{bb}C_{cb,i} + \frac{r_{b,gap}}{2}C_{cb,g}, \tag{3.19}$$

It is noted that $r_{b,i}$ is proportional to the emitter width $W_e$, but that $r_{b,gap}$ and $r_{cb}$ are independent of $W_e$. Table 3.1 lists the value of these resistance with different emitter sizes. From table 1, it is seen that for very narrow-emitter devices (less than $1\mu$m), the total base resistance is dominated by $r_{cb}$ and is only weakly dependent upon $W_e$.

| $W_e$ ($\mu$m) 6$\mu$m-base | $r_{b,i}$ ($\Omega$) $\propto W_e$ | $r_{b,gap}$ ($\Omega$) independent of $W_e$ | $r_3$ ($\Omega$) independent of $W_e$ | $r_{bb}$ ($\Omega$) |
|---|---|---|---|---|
| 0.3 | 1.67 | 2.5 | 14.4 | 18.57 |
| 0.5 | 3.33 | 2.5 | 14.4 | 20.23 |
| 1.0 | 6.67 | 2.5 | 14.4 | 23.57 |
| 2.0 | 15.0 | 2.5 | 14.4 | 31.90 |

Table 3.1: Base resistance with different emitter sizes, assuming 6 $\mu$m emitter length, base mesa width = 6$\mu$m, 0.05 $\mu$m undercut, $\rho_{sb}$ = 600 $\Omega/\Box$, $\rho_v$ = 5 x $10^{-7}$ $\Omega$cm$^2$ and $L_T$ = 0.288 $\mu$m.

For the transferred-substrate HBTs, the collector-base capacitance $c_{cb}$ is proportional to $W_e$. Hence, to get a scalable HBTs with very high bandwidth, transferred-substrate HBT structure is the right approach.

The simple and systematically derived expression of $f_{max}$ discussed here should be very useful in the design of modern HBTs with optimized $f_{max}$ values.

## 3.2 Collector-base Capacitance $C_{cb}$ Cancelation

The intrinsic collector-base capacitance $C_{cbi}$ of the transferred-substrate InGaAs/InAlAs HBTs were measured as a function of collector current and collector-emitter voltage. The experimental results were considerably smaller than the expected dielectric capacitance, leading to unexpected high values of $f_{max}$. The modulation of electron velocity in the collector depletion region by the collector-base voltage accounts for the reduction of $C_{cbi}$ and will be discussed below. The following discussion also relates the change in $C_{cbi}$ to the variation of the collector transit time $\tau_c$ with collector-base voltage.

The collector region has a geometry similar to a parallel plate capacitor. In the presence of zero current, the intrinsic base-collector capacitance is given by:

$$C_{cbi} = \frac{\epsilon A_E}{T_C} \tag{3.20}$$

where $A_E$ is the emitter area, $\epsilon$ is the dielectric constant, and $T_C$ is the thickness of the collector depletion region. Eq. ( 3.20), however, is not very reliable for high performance HBTs. At high collector current and high emitter-collector voltage, the intrinsic collector-base capacitance $C_{cb,i}$ can be substantially lower than the parallel-plate dielectric capacitance value. This effect is very important for proper modeling of the small-dimension transistors with very high values of $f_{max}$. The underlying physics of the reduction of $C_{cbi}$ is the modulation of the electron space-charge in the collector by the collector-base voltage at high collector current. In III/V materials such as InP and InGaAs, electron velocity is electric field dependent and decreases with applied field. While not well-known, this effect has been analyzed and measured by several groups [24], [25], [26]. Y. Betser et al. [24] have developed a model of $C_{cb}$ reduction with an arbitrary electron velocity profile and doping profiles in the collector.

The collector-base capacitance has two components: the extrinsic and intrinsic capacitance. The intrinsic differential collector-base capacitance is defined as:

$$C_{cbi} = \frac{dQ_{ci}}{dV_{bc}} \Bigg| \; I_e = constant \quad , \tag{3.21}$$

where the positive charge in the intrinsic collector depletion region is

$$Q_{ci} = qA_e \int_0^{W_{sc}} (N_D(x) - n(x))dx, \tag{3.22}$$

where $N_D(x)$ is the donor distribution in the collector, and the electron concentration in the collector is given by

$$n(x) = \frac{I_C}{qA_e v(x)} \tag{3.23}$$

where v(x) is the electron space-charge velocity profile in the collector. We consider only transistors under forward-active bias with fully depleted collectors. Combining Eqs.( 3.21)-( 3.23), the intrinsic differential collector-base capacitance is given by:

$$\begin{aligned} C_{cbi} &= \frac{\epsilon A_e}{W_{sc}} - \tau_c \frac{dI_c}{dV_{bc}} \Big|_{W_{sc}} - I_c \frac{d\tau_c}{dV_{bc}} \Big|_{W_{sc}} \\ &= \frac{\epsilon A_e}{T_c} - \tau_c \frac{dI_c}{dV_{bc}} \Big|_{T_c} - I_c \frac{d\tau_c}{dV_{bc}} \Big|_{T_c} , \end{aligned} \tag{3.24}$$

where $\tau_c$ is the collector transit time. The first term of Eq.( 3.24) accounts for the conventional parallel-plate capacitance due to the space-charge variation at the depletion edges. The second term accounts for the Early effects by considering the change in $I_c$ modulated by $V_{bc}$. For HBTs biased in the forward-active region, this term is negligible. The third term originates from the response of the collector space-charge to the modulation of the $V_{cb}$, ie. the average velocity modulated by the collector electric field. The electron velocity decreases as the collector-base voltage increases, hence collector transit time increases with $V_{cb}$. Therefore the third term in Eq.( 3.24) reduces the overall $C_{cbi}$.

Now let's take a look at what determines the collector transit time $\tau_c$. While an electron is in the base, its charge is screened by holes, so no collector current flows. When the electron enters the depleted collector, however, it images charge on the quasi-neutral base and the undepleted collector. Figure 3.4 illustrates the electrostatic-induced excess charge at the depletion edges, which is caused by an electron traversing the depletion region. Because of the electrical symmetry in figure 3.4, the induced charges

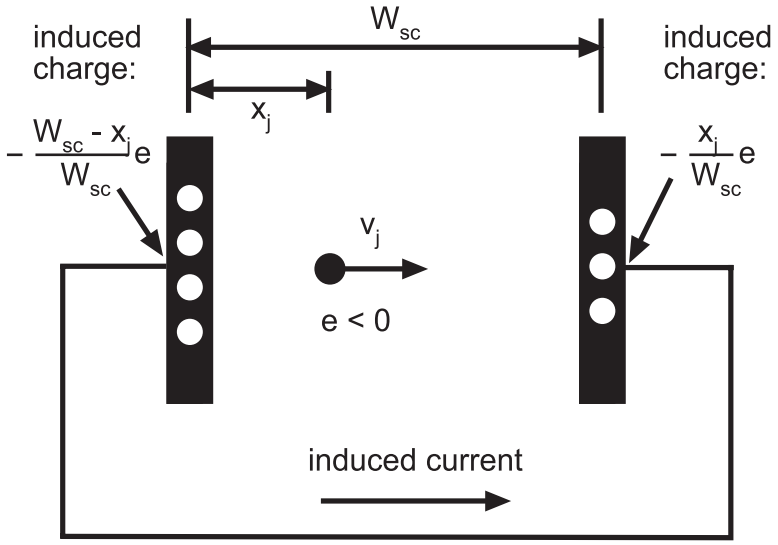



Figure 3.4: Model for the collector depletion region. The left electrode corresponds to the base edge of the depletion region and the right one to the collector edge.

at the base and collector edges of depletion region are given by -($W_{sc}$ - $x_j$)e/$W_{sc}$, and -$x_j$e/$W_{sc}$, respectively. While it traverses the collector space-charge region, electron current flux j induces a collector current given by:

$$i_{cj}(t) = \frac{-qv_{zj}(t)}{W_{sc}} \tag{3.25}$$

where $W_{sc}$ is the width of the collector space-charge region, and $v_{zj}$(t) is the z-directed velocity of electron j at time t. Hence with a position-dependent weighting as shown in figure 3.4[29], the total hole charge in the base induced by the collector space-charge is given by:

$$Q_{bc} = \int_0^{W_{sc}} \frac{I_c}{v(x)} \left(1 - \frac{x}{W_{sc}}\right) dx. \tag{3.26}$$

Therefore, the collector transit time $\tau_c$ is

$$\tau_c = \frac{\partial Q_{bc}}{\partial I_c} = \int_0^{W_{sc}} \frac{\partial}{\partial I_c} \frac{I_c}{v(x)} \left(1 - \frac{x}{W_{sc}}\right) dx. \tag{3.27}$$

How does $\tau_c$ change with bias? We can examine two different cases. In the first case, $V_{cb}$ is held constant, while increasing collector current $I_c$. In

the second case, collector current $I_c$ is held constant, while increasing the base-collector voltage $V_{cb}$.

Case 1: figure 3.5 shows electric field profiles in the collector space-charge region in low and high collector current. We can see that at low collector current density case, the distribution of the electric field in the depletion layer of the collector is mainly determined by the profiles of the impurities and applied voltage, the electric field is maximum on the base side of the depletion layer, the electron velocity overshoots its steady-state value until intervalley scattering occurs. In this case the electron velocity overshoot effect exits only over a narrow region near the base collector interface. On the other hand, increasing the collector current density reduces the electric field on the base side of the depletion region and increases the width of the overshoot region. This is accompanied by an increase of the effective electron velocity in the collector depletion layer, leading to a reduction of the collector transit time.

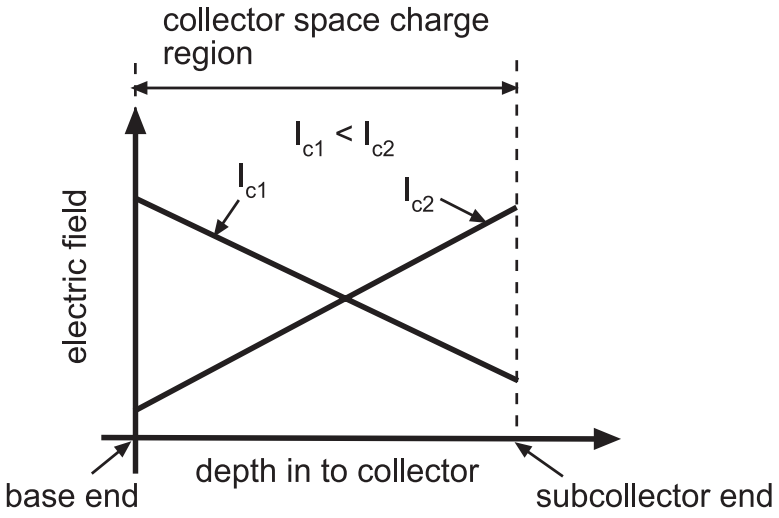



Figure 3.5: Electric field profiles in the collector space charge region for low and high collector current.

Case 2: Increasing the applied base-collector voltage $V_{cb}$ leads to increase of the collector transit time, resulting from the increased electron transition from the Γ-valley to upper L, X-valleys – that is, due to the resultant decrease in overshoot effect region under the high collector base voltage.

The reduction in $C_{cbi}$ can be predicted by Eq.( 3.24) if the variation of the collector transit time with collector-emitter voltage can be obtained. $1/(2\pi f_\tau)$ is equal to $\tau_b + \tau_c + C_{je}r_e + C_{cb}(r_e + r_{ex})$. At constant emitter current $I_e$, the base transit time $\tau_b$, and the emitter charging time $r_e C_{je}$ do not vary with $V_{cb}$, the contribution of $C_{cb}(r_e + r_{ex})$ is fairly small, hence is ignored in the derivation, therefore, we have obtained the following relation:

$$\frac{\partial \tau_c}{\partial V_{cb}} \Bigg|_{I_e} \approx \frac{\partial(\frac{1}{2\pi f_\tau})}{\partial V_{cb}} \Bigg|_{I_e} \tag{3.28}$$

Figure 3.6 plots the measured $1/(2\pi f_\tau)$ versus $V_{cb}$ for different emitter currents. By linear fitting to the measured data, $\partial\tau_c/\partial V_{cb}$ is obtained for different emitter currents. As expected, $\partial\tau_c/\partial V_{cb}$ is smaller for higher current. For $I_e = 5.0$ mA, $\partial\tau_c/\partial V_{cb} = 0.15$ ps/V, this predicts a $\sim 0.6$ fF reduction from 1 mA $I_c$ to 5 mA $I_c$. Compared with the measured total $C_{cb}$ from $Y_{12}$ (figure 3.7), which the reduction between 1 mA $I_c$ to 5 mA $I_c$ is 0.75 fF, this is a fairly good prediction.

The question arises as to whether the theory is corrected. There are two experimental tests. First, we can directly measure $C_{cb}$ from $Y_{12}$. The reduction in the intrinsic collector-base capacitance predicted by eq.( 3.24) has been observed in standard HBTs[24], [25]. We have fabricated transferred-substrate HBTs with 0.4 x 6 $\mu m^2$ emitters and 1.1 x 10 $\mu m^2$ collectors. The total collector-base capacitance $C_{cb}$ is extracted from microwave measurements by plotting the imaginary part of the admittance parameter $Y_{12}$ versus frequency. Figure 3.7 shows the total collector-base capacitance versus emitter current at $V_{ce} = 1.16$ Volts. A substantial reduction of the capacitance can be obtained at high emitter current densities up to the threshold of the Kirk effect. The variation of $C_{cb}$ between 1-5 mA is 0.75 fF (figure 3.7). From figure 3.6, a reduction of $\Delta C = (\partial\tau_c/\partial V_{cb})I_c = 0.6$ fF is expected. This is a reasonable agreement.

Second, to investigate the change in the intrinsic collector-base junction capacitance $C_{cbi}$ very approximately, we also plot $f_\tau/(8\pi r_{bb} f_{max}^2) = C_{cbi,estimated}$ values versus emitter current in figure 3.8 which are derived by modifying the following well-known relationship between $f_\tau$ and $f_{max}$:

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi r_{bb} C_{cb}}}, \tag{3.29}$$

where $r_{bb}$ is the base resistance. Again, the reduction of $C_{cb}$ with bias is clear, and of magnitude consistent with figure 3.6 and figure 3.7.

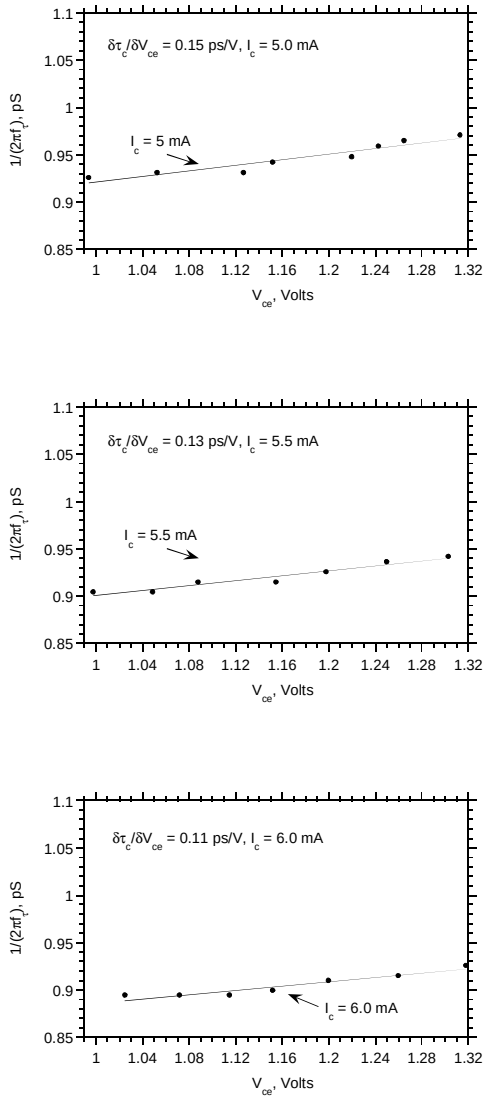



Figure 3.6: $1/(2\pi f_\tau)$ vs. $V_{cb}$ for emitter currents of (a) 5.0 mA, (b) 5.5 mA and (c) 6.0 mA. The solid lines are the best linear fits to the measured data.

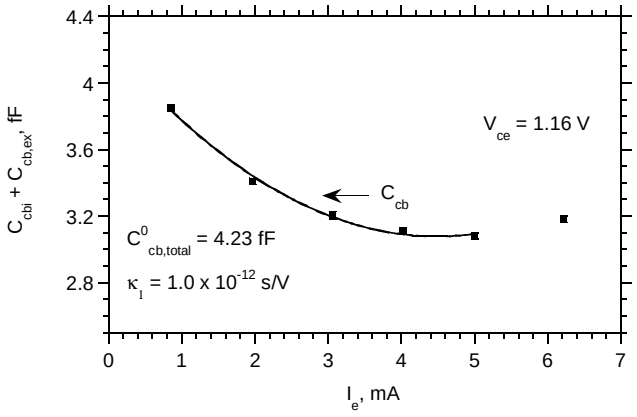



Figure 3.7: Collector-base capacitance extracted from Y-parameter vs. emitter current.

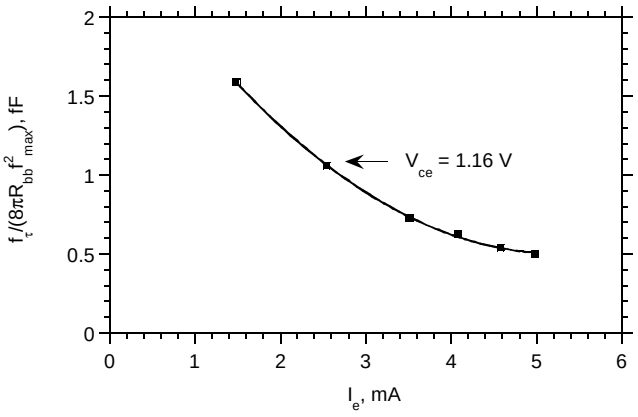



Figure 3.8: Collector-base capacitance extracted from $f_\tau$, $f_{max}$ and $R_{bb}$ vs. emitter current.

We can get some interesting observations by investigating figure 3.7 in more details. As shown in figure 3.7, the data can be fitted with a polynomial which is $C_{cb}$ = 4.37 - 0.73$I_e$ + 0.144$I_e^2$. In the following discussion, it will be shown that from this polynomial, we can find out the electric field dependence of collector electron velocity quantitatively. The electron under high field in $In_{0.53}Ga_{0.47}As$ has a negative differential mobility. The reciprocal of the velocity of the electron in $In_{0.53}Ga_{0.47}As$ has an approximate linear relation with the electric field of interest. Thus, one can approximate the inverse of the high-electric-field electron velocity in $In_{0.53}Ga_{0.47}As$ by the linear relation:

$$\frac{1}{v(E)} = \kappa_0 + \kappa_1 E, \tag{3.30}$$

where E is the electric field.

Camnitz et. al[25] have used this velocity-field relation to calculate the collector transit time,

$$\tau_c = \frac{1}{J_c}\frac{kT_jC_e}{qA_e} - J_c\frac{\kappa_1 W_c^2}{12\epsilon v(E_{avg})} + \cdots \tag{3.31}$$

and the intrinsic collector-base capacitance:

$$\frac{C_{cbi}}{A_e} = \frac{\epsilon}{T_c} - \frac{\partial Q_{bc}}{\partial V_{cb}} = \frac{\epsilon}{T_c} - \frac{\kappa_1 J_c}{2}\left[1 - \frac{\kappa_1 J_c T_c}{6\epsilon}\right], \tag{3.32}$$

the detailed derivation of Eq.( 3.31) & ( 3.32) can be found in [25]. Comparing Eq.( 3.32) to the polynomial obtained by figure 3.7, we find that $\kappa_1$ = 1.0 x $10^{-12}$ sec/V. It should be noted that while the parabolic data of figure 3.7 has two free parameters, Camnitz's theory (eq. 3.32) provides a single degree of freedom,$\kappa_1$. The correlation of theory vs. experiment is therefore strong.

To summarize, the base-collector capacitance is very important in determining the transistor's output impedance, reverse isolation characteristics and the power gain cutoff frequency $f_{max}$. Because of the modulation of the electron-space-charge velocity by the base-collector voltage at high current density, the intrinsic collector-base capacitance can be considerably lower than the dielectric capacitance value. This capacitance cancelation effect could greatly increase the overall performance of HBTs, but in the normal-mesa HBT designs, the large value of extrinsic collector-base capacitance would withhold the potential improvements. In transferred-substrate HBT

technology, which allow us to lithographically define both narrow emitter and collector stripes aligned to each other on the opposite sides of the base epitaxial layer, this will substantially reduce or eliminate the extrinsic collector-base capacitance, therefore, the full benefit of the collector capacitance cancelation effect can be achieved.

# Chapter 4

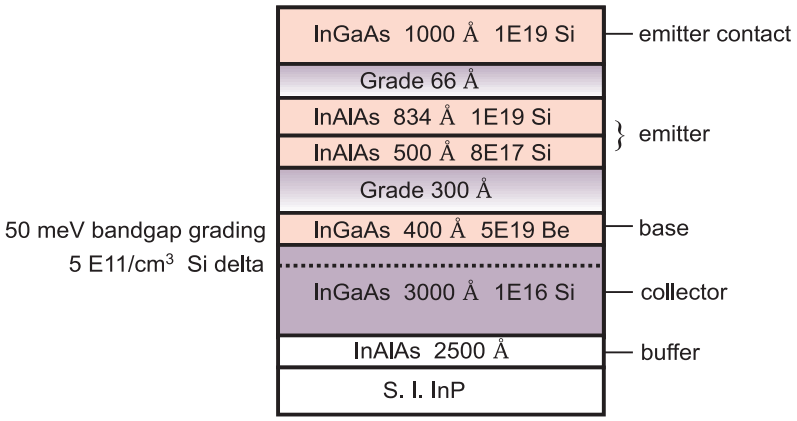
# Growth and Fabrication

This chapter will describe in detail the important stages of development of the submicron transferred-substrate HBT technology in the InAlAs/InGaAs material system. The fabrication of deep submicron transferred-substrate HBTs and integrate circuit was challenging. Extensive experiments and multiple wafer runs were done in developing the fabrication process. The results from every process development experiment are not presented here in detail; the final process is presented briefly. The detail process flow is included in the appendix.

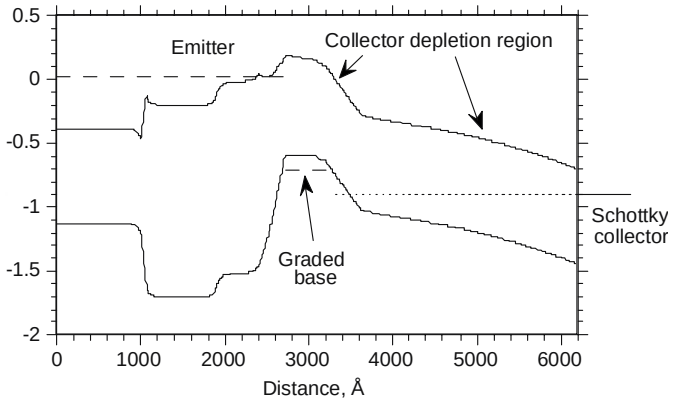
## 4.1 Growth

Figure 4.1 shows the epitaxial layer structure for a typical transferred-substrate HBT[19]. The InGaAs/InAlAs material was chosen. InP-based HBTs have several advantages over the GaAs-based HBTs including higher electron mobility, higher peak electron velocities and saturated electron velocities, three orders of magnitude lower surface recombination velocity, larger thermal conductivity and lower base-emitter turn-on voltage. Combined with the scalability of the transferred-substrate HBT technology, the InGaAs/InAlAs HBT is ideal for very high speed and low-power circuit applications. The HBT epitaxial layer structure (figure 4.1) is grown by molecular beam epitaxy, lattice matched to a Fe-doped semi-insulating InP substrate (by D. Mensa).

The InGaAs base used in this work is 400-500 Å thick, and is Be-doped at 5 x $10^{19}/cm^3$. To reduce the base transit time, the base has kT-2kT




(a)




(b)

Figure 4.1: (a) MBE layer structure and (b) Band diagram under forward bias.

bandgap grading. By increasing the Ga cell temperature progressively during growth of the base layer, the Ga:In ratio is gradually increased, introducing 30-50 meV bandgap gradient across the base. More bandgap grading would improve the base transit time, but too much grading can cause excessive strain and growth defects in the semiconductor layers due to lattice mismatch. Also, on InGaAs layer with too high a Ga content may act more like GaAs with its higher surface recombination velocity, degrading the current gain of the deep submicron device. A thin base also improves the base transit time, but at the cost of increased base sheet resistance. Also a low and uniform base resistance necessitates a more precise and uniform emitter/base etch. Very thin base layers may be completely removed during the emitter/base etch. Further, out-diffusion of the Be dopant from the heavily doped base layer, results in a lower bound on the base thickness. For these reasons, thickness below 400 Å were not attempted.

The InGaAs emitter contact cap is $N^+$ doped with Si at 1 x $10^{19}/cm^3$, and is 1000 Å thick. The InAlAs emitter is 1350 Å thick. The first 500 Å is doped with Si at 8 x $10^{17}/cm^3$ and the remainder is Si-doped at 1 x $10^{19}/cm^3$. The InAlAs emitter is graded in 300 Å to the InGaAs base, and in 66 Å to the InGaAs emitter cap.

The InGaAs collector is 3000 Å thick, and is Si-doped at 1 x $10^{16}/cm^3$. A collector $N^+$ pulse-doped layer is placed 400 Å from the base to delay the onset of the base push-out [20] at higher collector current densities. Devices for this work use Schottky collector contacts. The Schottky-collector device has a zero collector series resistance. The 0.2 V barrier present in the Schottky-collector device increases the $V_{ce}$ required to suppress base push-out at high collector current densities. The Schottky-collector devices are used for the emitter-coupled-logic (ECL), where the operating $V_{ce}$ is high. Thinner collectors will improve the collector transit time and the Kirk effect threshold. But thin collectors increase the base-collector capacitance, hence degrade $f_{max}$. Breakdown voltage is worse in thin collectors because of the increased electric field.

The band diagram associated with the layer structure of figure 4.1a under forward bias is shown in figure 4.1b. The biasing conditions are: emitter-base voltage $V_{be}$ = 0.7 V, emitter-collector voltage $V_{ce}$ = 0.9 V, and an emitter current density of 1 x $10^5$ $A/cm^2$. Collector current density is assumed to be the same as the emitter current density, which is the case for the narrow collector device. The pulse-doped layer causes significantly

band-bending in the collector, as shown in the band diagram, resulting in increased current density at the onset of the Kirk effect.

## 4.2 Fabrication

The transferred-substrate HBT fabrication process are shown in figures 4.2, and 4.3 sequentially. First, the Ti/Pt/Au/Si ($\sim$1 $\mu$m) emitter contacts are defined by electron-beam or optical projection lithography at submicron linewidths. The emitter mesa formation is done by reactive ion etching with subsequent selective (acetic/HBr/HCl) and nonselective citric based wet etches. $\sim$ 1000 Å self-aligned Ti/Pt/Au base metal is then deposited and sintered at 300°C for a minute. Active base mesa formation is done by a $Cl_2$/Ar RIE dry etch with photoresist mask. Next, the device is passivated and planarized with polyimide in an $O_2$ RIE dry etch with photoresist as a mask. After planarization, polyimide is reflowed at 250°C for 10 minutes to round its edges for subsequent metal step coverage. Thin film NiCr (475 Å) is evaporated to form resistors with 50 $\Omega/\Box$ sheet resistivity. Then the first level of interconnect metal M1 ($\sim$1 $\mu$m) is evaporated at an angle with wafer rotation to get enough step coverage at the mesa and polyimide edges(figure 4.2a,b).

SiN dielectric is then deposited over the entire wafer by the PECVD at 250°C to form an insulating layer and the dielectric for the MIM capacitors. The SiN is patterned by the $SF_6/O_2$/Ar dry RIE etch with photoresist mask. Then the second level of the interconnection metal M2 is evaporated at the same manner as the M1. At this point, all passive elements like resistors and capacitors are formed.

The substrate transfer process starts with $\sim$5 $\mu$m Benzocyclobutene (BCB, $\epsilon_r = 2.7$) deposition. Thermal vias on the emitters and resistors and ground vias are done by $SF_6/O_2$ dry RIE etch using 100 Å Ni as the etching mask. Then the vias are filled with thick Au by eletroplating. This electroplated Au also forms ground planes (figure 4.2c). Next, the wafer is bonded to a GaAs transfer-substrate using Indium solder, and the InP host substrate is removed in HCl. $\sim$ 5000 Å Ti/Pt/Au Schottky collector metal is then deposited. This metal could be used as the third level of interconnect metal, M3. An isotropic collector recess etch to 0.05 $\mu$m depth forms collector-base junctions with a tapered profile, reducing collector-base junction capacitance $C_{cb}$ while maintaining latitude for emitter-collector

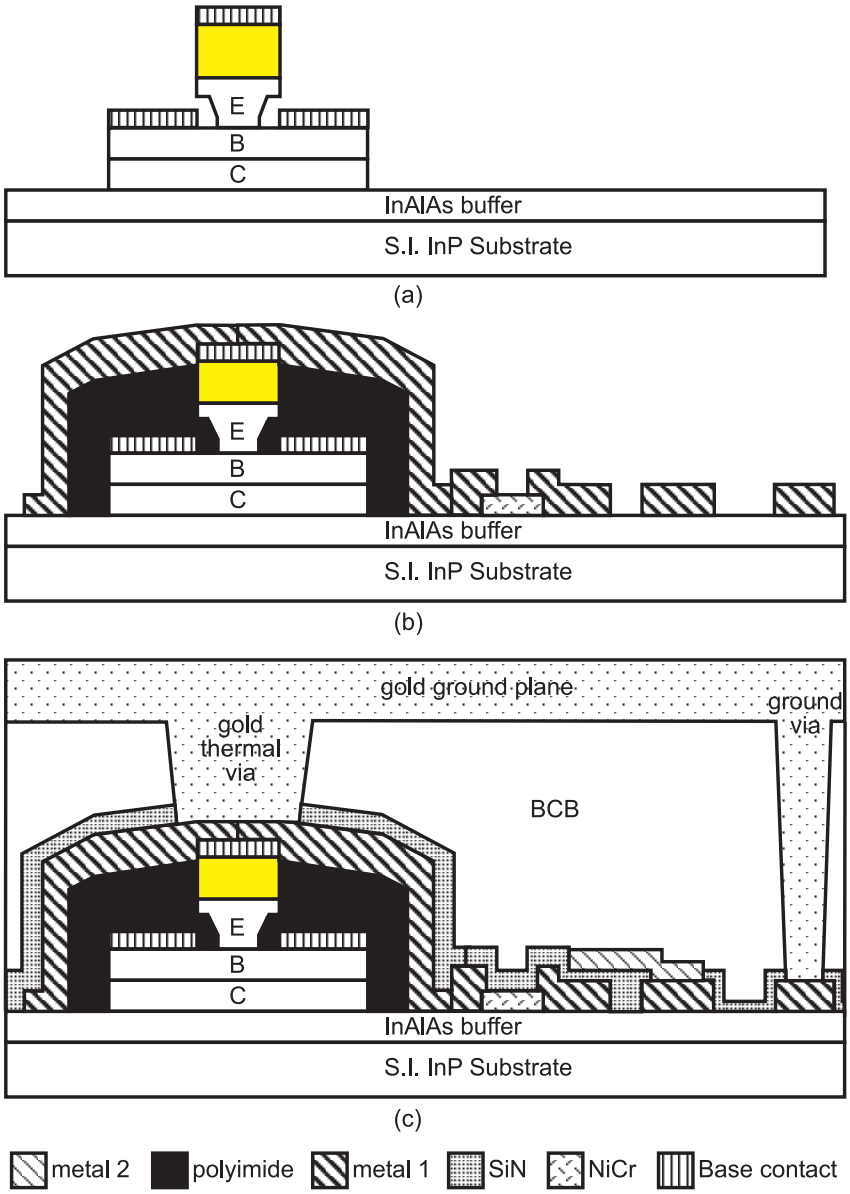



Figure 4.2: Fabrication process for the transferred-substrate HBTs.

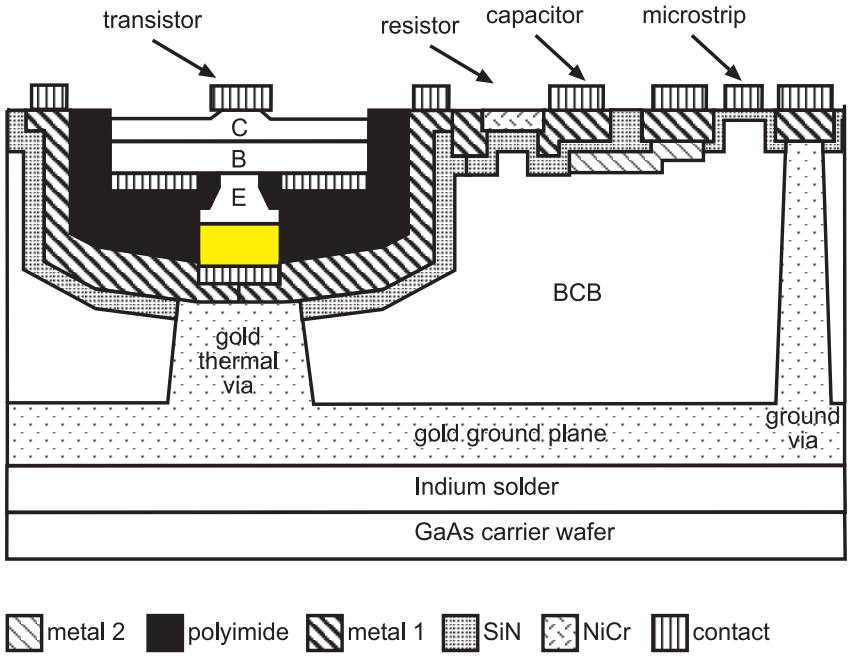



Figure 4.3: Fabrication process for the transferred-substrate HBTs.

misalignment. This completes the fabrication process (figure 4.3).

The following subsections contain a detail description of steps for the deep submicron device fabrication which differ from the standard transferred-substrate HBT process[40], [41]. This includes the problems encountered in process development and their solutions.

## 4.3 Emitter Definition

The emitter contact structure requires a large (height/width) aspect ratio so that it can be planarized and interconnects to the emitter fabricated. A large aspect ratio requires a tall metal structure and hence, a tall photoresist profile. Emitters were fabricated both using e-beam and optical projection lithography.

The electron-beam lithography process development was done at JPL on a JEOL JBX 5DII e-beam lithography system. The process uses a bilayer resist consisting of PMMA495K ($\sim$ 8000 Å) and PMMA950 ($\sim$ 1200 Å). After exposure, the sample is dipped in one to three mixture of MIBK and

IPA for 60 s, followed by one to one mixture of MIBK and IPA spray for 45 s. This development undercuts the top PMMA layer. This is the desired photoresist profile for the metal liftoff. A 0.3 $\mu$m wide, 0.8 $\mu$m tall emitter SEM is shown in figure 4.4a.

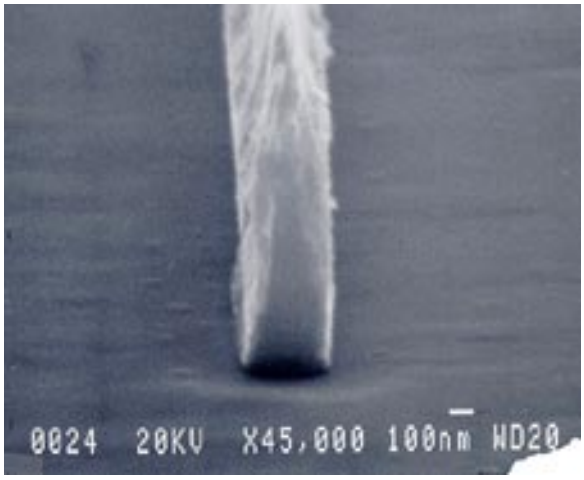
The UCSB optical projection lithography tool is also capable of defining submicron (0.5 $\mu$m) dimension. A bilayer photoresist process is developed (figure 4.5). The bottom $\sim$ 9000 Å SPR-950 photoresist is i-line sensitive and has very fine resolution, but it gives a perfectly vertical side-wall, which is not desired for the emitter metal lift-off. A 4000 Å contrast enhancement material (CEM) is spun on top of the SPR-950 resist. After exposure, a post exposure bake will harden the interface between the nonexposed CEM and SPR-950 resist (figure 4.5a), then the water soluble CEM is removed by DI water rinse. After development, the overhanging profile of the photoresist which is desired for the metal liftoff is thus obtained (figure 4.5b). With this process, minimum feature size of 0.4 $\mu$m wide 1 $\mu$m tall emitter lines (figure 4.4b)is obtained, which is beyond the lithography tool specification (0.7 $\mu$m). The top opening of the SPR-950 resist is not only affected by the exposure time, but is also sensitive to the post exposure bake time and hot plate temperature. 0.4 $\mu$m lines can be obtained consistently from run to run.

## 4.4 Emitter Base Etch

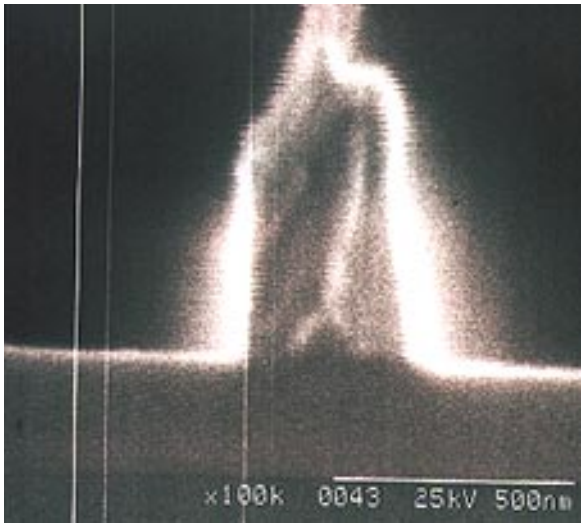
To obtain high bandwidth with transferred-substrate HBTs, emitter dimensions must be scaled. To fabricate $\sim$ 0.1 $\mu$m device and to achieve reasonable scale of integration of integrated circuits it is necessary to develop a dimensionally well-controlled, high yield, dry etch, self-aligned processing technology instead of the low-resolution wet-etching techniques.

Much of the III-V HBT industry still uses wet-etching techniques to form the emitter/base junction. There are two problems. First, the etch may not stop exactly on the base, consequently, the over etched base will increase the base sheet resistance, hence, increase $r_{bb}$. Second, since wet etching tends to be isotropic, the large etch undercutting of the mask makes it unsuitable for deep submicron emitter/base junction formation. Variability in the etch makes it unsuitable for the integrated circuit process.

Dry etching has more anisotropic pattern transfer and better dimensional control. A combined of dry and wet etch emitter mesa process is

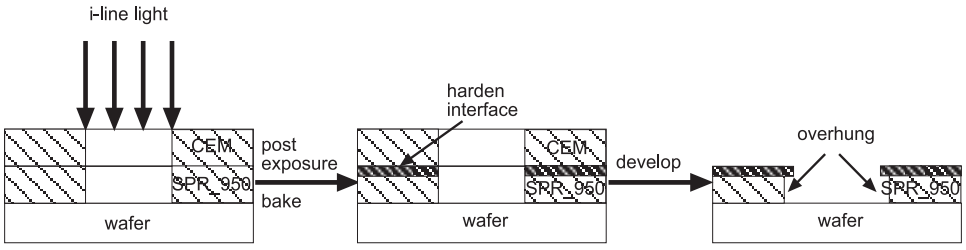



(a)

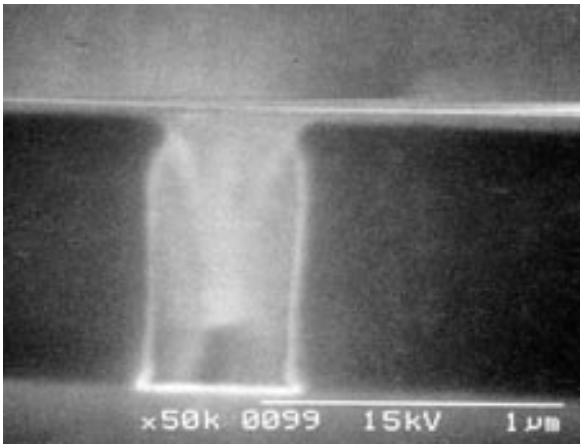



(b)

Figure 4.4: (a) 0.3 $\mu$m emitter contact defined by electron-beam lithography, and (b) 0.4 $\mu$m emitter contact defined by optical projection lithography.




(a)




(b)

Figure 4.5: (a) Optical projection lift-off process, and (b) SEM of the lift-off photoresist profile.

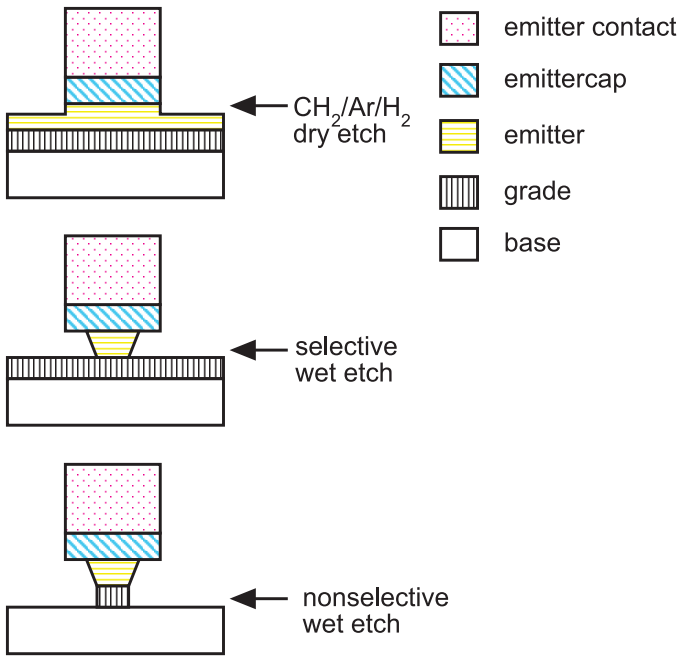
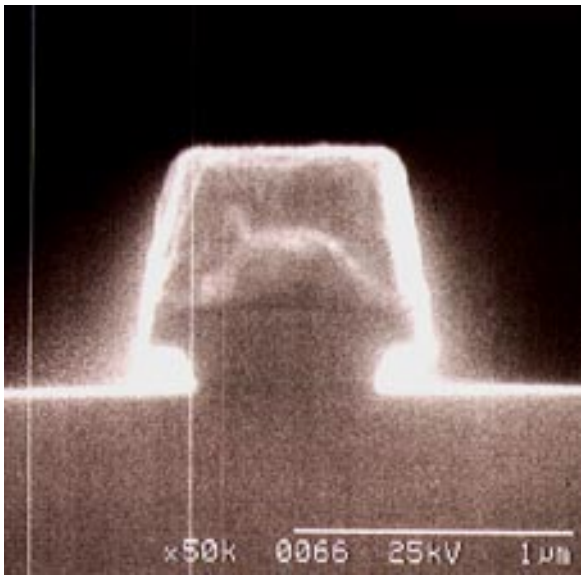



Figure 4.6: Emitter mesa process for the transferred-substrate HBTs.

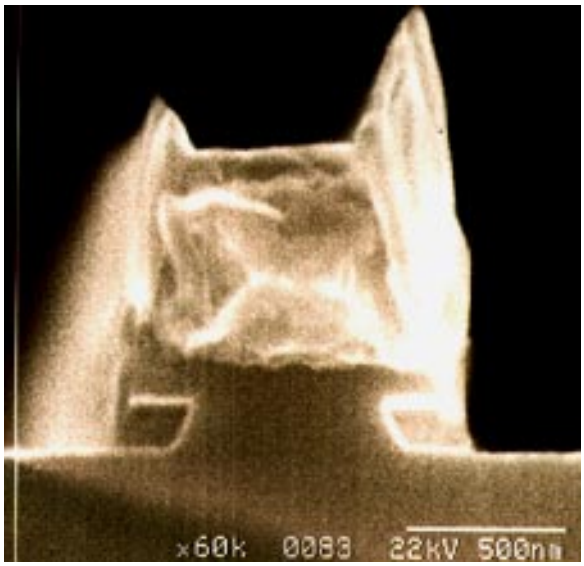
developed (figure 4.6). 1 $\mu$m thick Ti/Pt/Au/Si is lifted off during the definition of the emitter contact. 500 Å Si is used as masking material due to its good edge resolution and high durability through the dry etch process [42]. The Si protects the emitter contact metal from sputtering during the high self-bias dry etching of the emitter. A combination of $CH_4/H_2/Ar$ gasses is used to dry etch through the 1000 Å InGaAs cap layer and partially through the InAlAs emitter. In situ endpoint determination is necessary for etch depth control. Laser reflectometry is used here for monitoring progress throughout the etch. The reflected light intensity profile is an unique signature dependent on the layer structure of the etching material[42]. The dry etching end-point is reproducible from run to run due to this technique. After the dry etching, the remaining Si on the emitter contact is removed by $CF_4$ plasma.

The InAlAs emitter is then etched through by a wet chemical etch (acetic/HBr/HCl) with a large selectivity with respect to the $p^+$ InGaAs base. A slight undercut of InAlAs emitter, under the InGaAs cap is obtained to allow for the break in the self aligned base metal lift-off. The etch is timed depending upon the amount of the undercut desired. Deep undercuts increase the emitter-base gap resistance, decreasing $f_{max}$, and are undesirable. The undercut for the $> 1$ $\mu$m device dimension is less than 0.2 $\mu$m, as shown in SEM micrograph in figure 4.7. Since this etch is selective on the basis of Al versus Ga content of the material, it stops abruptly at some point in the graded emitter/base junction where the Ga content becomes sufficiently high. Because the $\sim$ 1350 Å InAlAs emitter is partially etched during the RIE etch, the vertical distance etched by the selective wet etch is less than the desired lateral undercut, the over-etching therefore occurs in the vertical direction. This over-etching will remove the nonuniformity caused by the edge of the wafer etching faster than the center during the dry etch. An uniform surface very close to the $p^+$ InGaAs base is thus exposed. Next, a short, timed, slow etching rate and non selective citric based wet etch is performed to reach the base.

The wet chemical etching involves oxidation or reduction of the semiconductor surface and removal of a soluble reaction product. The etching rate may therefore be limited by the diffusion of the active etchant elements to the surface or by the diffusing away of the soluble product. The etch rate of the diffusion-controlled etches is sensitive to the agitation of the wafer or etching solution, but insensitive to the etching solution temperature. The




(a)




(b)

Figure 4.7: Emitter mesa profile of (a) emitter stripe perpendicular to major flat, and (b) emitter stripe parallel to the major flat.

other type of etch is the reaction-limited etch in which the chemical reaction at the semiconductor surface is the rate-limiting step. For III-V material systems that consist of at least two different sublattices, the reaction-limited etch usually etches the different orientations at different etching rates, hence the etch is anisotropic (figure 4.7). As shown in figure 4.7, the etch rate is higher for the $(0\bar{1}1)$ crystal directions than for $(0\bar{1}\bar{1})$ direction. Because of this, the emitter is written perpendicular to the major flat of the wafer, which avoids the lack of undercut in the $(0\bar{1}\bar{1})$ direction. This makes the self-aligned structure possible with minimum over etching. For deep submicron small-aspect ratio (or square) emitters, the hexagonal emitter shape is prefered for ease of metal liftoff [21]. Reaction-limited etches are generally insensitive to agitation, but are highly sensitive to the solution temperature. Figure 4.8 shows the selective wet etching rate versus temperature of the solution. Depending on the applications, the solution may either heated or cooled to obtain controlled etch rates. For deep submicron emitters, the solution is cooled to 10°C to obtain highly reproducible $< 0.05$ $\mu$m undercut (figure 4.9).

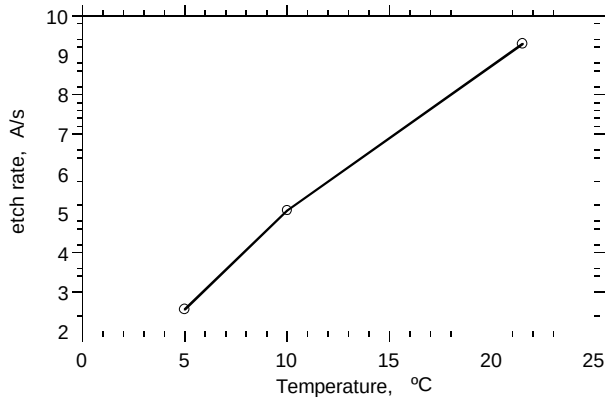



Figure 4.8: Etch rate of the selective wet etch versus temperature.

In summary, the combined reactive-ion and wet chemical etches used to form the emitter mesa has several advantages over complete wet etch process. The dry etch provides a vertical side-wall, and the follow-up wet-etches remove damage and nonuniformity in the semiconductor left from the

dry etch process. The selective wet etch stops accurately close to the thin InGaAs base, which helps avoid over-etching into the base. A controlled undercut of the emitter mesa is possible. Figure 4.9 shows the SEM of a 0.3 $\mu$m emitter/base junction.

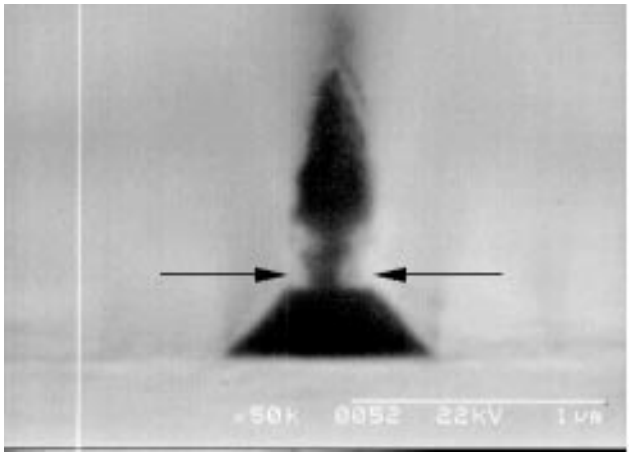



Figure 4.9: SEM of 0.3 $\mu$m emitter/base junction.

We have observed that deep submicron emitters often have anomalously high emitter resistance. The HCl in the selective wet etchant is suspected to attack the emitter contact metal Ti layer, therefore increasing the extrinsic emitter resistance $r_{ex}$. As the emitter is scaled to deep submicron dimension, this problem will be worse. Here, a new emitter-mesa etch process is proposed (figure 4.10) , in which the emitter contact metal is protected by a SiN spacer. After the dry etch of the emitter by the same way as described above, a thin layer of $Si_3N_4$ is deposited on the whole wafer. Then, a low pressure and high bias voltage dry etch can etch back to leave a uniform sidewall of SiN. Then a light selective wet etch is performed for the same purpose as discussed in the above paragraph. The self-aligned base contact can then be evaporated. This process may also provide better dimension control for the deep submicron emitter mesas.

## 4.5 Bonding

The wafer bonding steps involves transferring the processed layers from the InP host substrate to a GaAs carrier wafer. Collector definition is done

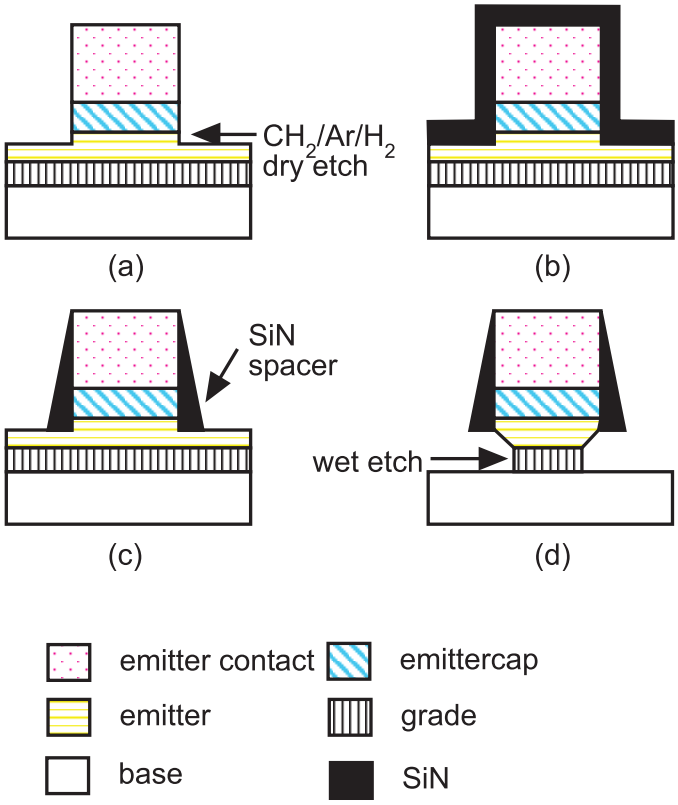
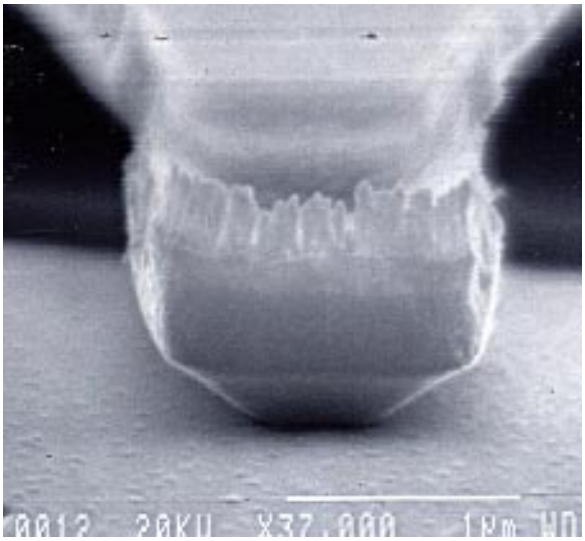



Figure 4.10: Improved emitter mesa etch for deep submicron dimension.

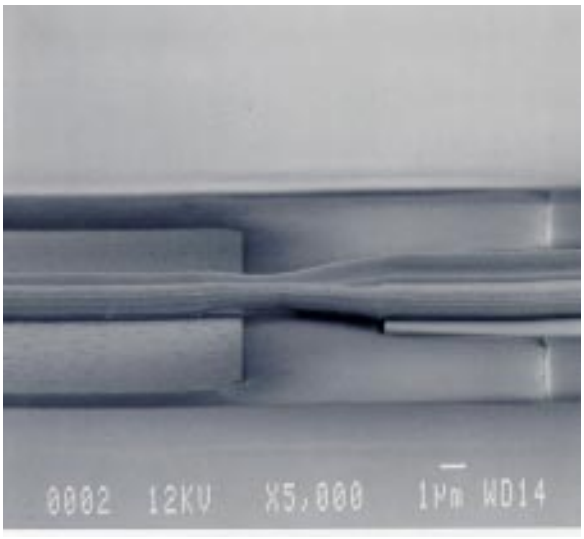
after the substrate transfer. Therefore, this requires the transferred wafer be smooth, and unshrunk. The transferred wafer must the collector definition process. After experimenting with a variety of bonding materials, a $In_{0.8}Ag_{0.1}Pb_{0.1}$ solder (melting point $\sim 140^{\circ}C$) was chosen. This step is performed in a flip-chip bonder at $180^{\circ}C$ and under less than 1000 gm pressure in order to ensure solder thickness uniformity. The GaAs carrier wafer is sputtered with a thin layer of Ti/Au to improve the adhesion and wettability of the solder. For the wafers where the collectors are to be defined by the ebeam lithography, a higher melting point ($\sim 190^{\circ}C$) solder ($In_{0.6}Pb_{0.4}$) is used. This is because the wafer has to survive a $170^{\circ}C$ resist bake during the collector definition. Since this solder has less indium content, its wettability is poor. Ultimately, the copper substrate process developed by J. Guthrie will solve these problems.

## 4.6 Collector Definition

After substrate removal, collectors are defined by e-beam lithography. The process developed at JPL creates the airbridged submicron Schottky-collector in a single lithography and metalization step. The reason for the airbridge collector is that the base mesa isolation etch is etched into the InAlAs buffer layer, hence, there is a step of $\sim 1000$ Å between the InGaAs semiconductor and collector contact pads. The airbridge collector can prevent a break in the collector metal at the step, and can also reduce the extrinsic collector-base capacitance. The process uses a trilayer resist consisting of PMMA/COPMMA/PMMA similar to a standard T-gate e-beam lithography process. Multiple scans are done at different electron doses to expose the footprint and the side-beams of the T-gate separately. The airbridges are formed by limiting the areas where the footprint penetrates the bottom resist layer. The collector then contacts the semiconductor only at places where all the three layers of resist were developed away, the remainder of the structure becoming an airbridge. Figure 4.11 shows the SEM of the collector finger and the collector airbridge.




(a)




(b)

Figure 4.11: SEM of (a) 0.4 $\mu$m collector stripe, and (b) airbridged collector.

## 4.7 Collector Alignment

Emitter/collector alignment is critical. HBTs with misaligned collectors have poor DC and RF characteristics. After substrate transfer, a 3 x 3 $mm^2$ cell will shrink 1 $\mu$m in both vertical and lateral directions due to accumulated stress from the stacked up layers of BCB, electroplated Au and solder. The lithography tool alignment tolerance is also a limiting factor of the accurate emitter/collector alignment. Therefore, to obtain working devices and circuits, a staggered alignment of collector to emitter is used - collector are deliberately and successively misaligned on the mask from the emitter in steps, which depends on the alignment tolerance of the optical lithography tool used. For the optical contact lithography, the step of 0.5 $\mu$m and a maximum of 1.5 $\mu$m on either side are used due to the 1-2 $\mu$m alignment tolerance. For the optical projection lithography, a step of 0.3 $\mu$m and a maximum of 0.6 $\mu$m on either side are used due to the 0.5 $\mu$m alignment tolerance. This ensures that at least one HBT in the array of each cell has emitter and collector well aligned to each other. The other repetitions of the same device or circuit will be misaligned and will thus have poor characteristics. As a result, the yield of the whole wafer is not very high. By using the optical projection lithography, the real cell size on the carrier wafer can be measured and input to the computer setup, hence the effect of wafer shrinkage only impacts one cell. Therefore, the yield is much higher for the stepper than the contact lithography. For the electron beam lithography (0.1 $\mu$m alignment tolerance), local alignment marks are added to each individual transistor. This improves the emitter/collector alignment, but is not suitable for integrated circuit applications.

To obtain higher scales of integration, the emitter/collector alignment problems have to be addressed. First, we should try to reduce the wafer shrinkage. This wafer shrinkage is suspected to be caused by the BCB stress built up during curing. A low-stress curing profile may result in less stress, hence less wafer shrinkage. Secondly, a low stress copper-plated substrate may also improve the wafer shrinkage. Third, devices with short stripes are prefered over the long devices in the layout because the effect of the E/C misalignment due to wafer rotation is less severe for the shorter device as shown in figure 4.12. The improved lithography tool alignment tolerance definitely helps.

The transferred-substrate HBT IC fabrication process has been devel-

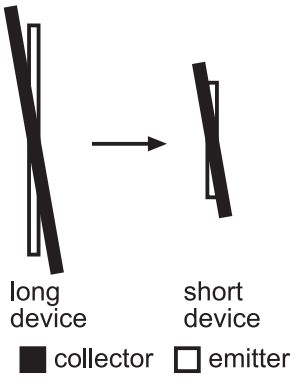



Figure 4.12: Comparison of the misalignment due to wafer rotation for a short and long devices.

oped. In next few chapters, the results of the transferred-substrate HBT technology will be shown and discussed.

# Chapter 5

# Through-Reflect-Line on-wafer Calibration

## 5.1 Introduction

In a microwave wafer probing system, the wafer probes utilize open air fixtures which result in leakage and coupling errors that are not modeled or accounted for in the 12-term error models. Consequently, when isolation measurements ($S_{12}$) are performed, errors in $S_{12}$ are unavoidable. If accurate microwave measurements are to be expected, it is necessary to minimize these leakage and coupling errors.

Transferred-substrate heterojunction bipolar transistors have very small base collector capacitance $C_{cb}$[19], [22]. When RF gains are measured under common-emitter configuration, this small $C_{cb}$ corresponds to the small $S_{12}$. A major problem encountered when making accurate RF power gain measurements of transferred-substrate HBTs is the need to minimize the effects of microwave probe-probe coupling on $S_{12}$ measurements. This is a particularly serious problem for W-band (75-110 GHz) measurements (figure 5.1). In order to minimize probe-probe coupling, the HBTs have to be separated from the probe pads by some length of on-wafer transmission lines. Then, losses of these lines have to be de-embedded in determining the accurate RF gain of the devices. On wafer calibration standards are used to de-embed the transistor S-parameters. The standard THROUGH-REFLECT-LINE (TRL) technique [23] is used, with microstrip through line, extended lines for 20-50 GHz and 75-110 GHz calibration, and offset shorts and opens for

the reflect standards and for verification.

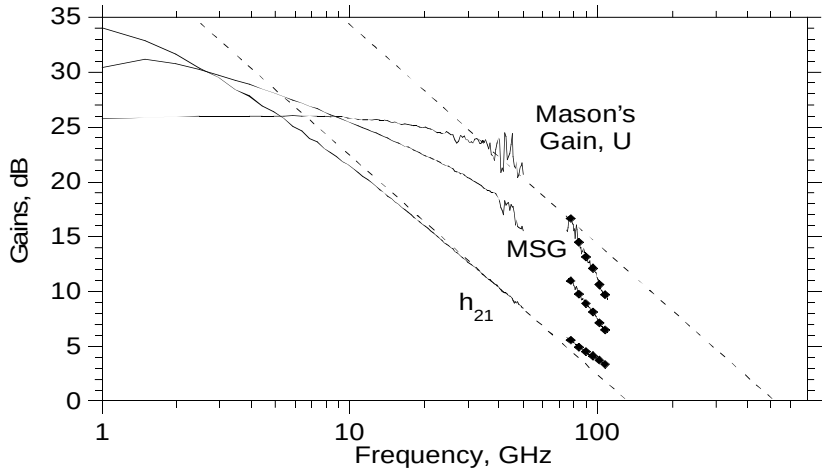



Figure 5.1: Corrupted gain plots for 0-50 and 75-110 GHz measurements.

## 5.2 Line-Reflect-Line Calibration Theory

At microwave frequencies, system effects such as leakage, test port mismatch, phase shift in cables and reflections from cables will affect the measured data. These amplitude/phase contributions of cabling(etc.) between the instrument and the device under test are repeatable and can be measured by the network analyzer. This process is called " calibration ". The calibration is done using standard devices with known characteristics. The system effects are determined as the difference between the measured and known responses of the standards. Once characterized, these errors can be mathematically related by solving a signal flow graph. The 12-term error model, shown in figure 5.2, includes all the significant system errors for the 2-port case.

Through-reflect-line is an approach to the 2-port calibration that relies on transmission lines. Rather than a set of discrete impedance standards, these are the simplest elements to realize on wafer, especially for very high frequency (>100 GHz) measurements. TRL stands for the three basic steps

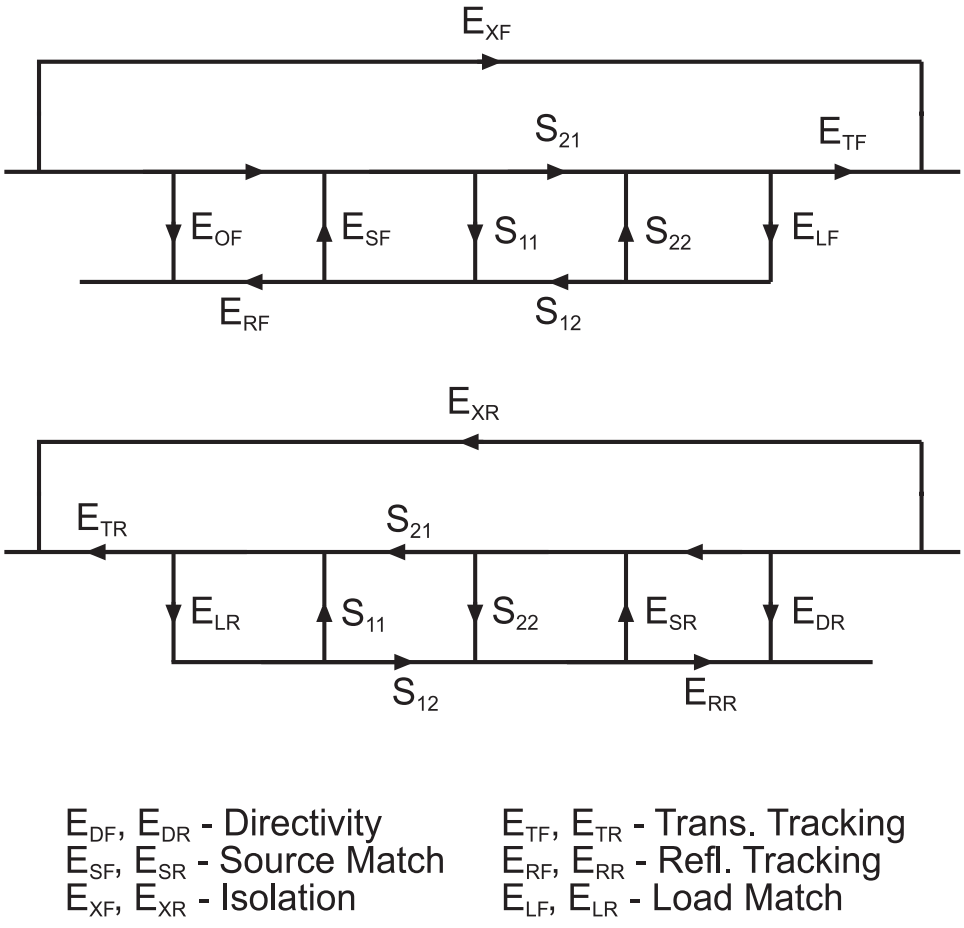



Figure 5.2: Two-port 12-term error model

in the calibration process. THROUGH is to connect port 1 and port 2 directly or with a short length of transmission line. REFLECT is to connect identical one-port high reflection coefficient devices to each port. LINE is to insert a short length of transmission line between port 1 and 2 (different line lengths are required for the THROUGH and the LINE). A total of 16 measurements are required to quantify the twelve unknowns.

Figure 5.3 shows the block diagram for a simplified 2-port measurement system. Eight of the error terms are represented by the two 2-port error networks in the figure. These errors are characterized using the basic TRL calibration and are shown in figure 5.4a. To solve for these eight unknown error terms, eight linearly independent equations are required.

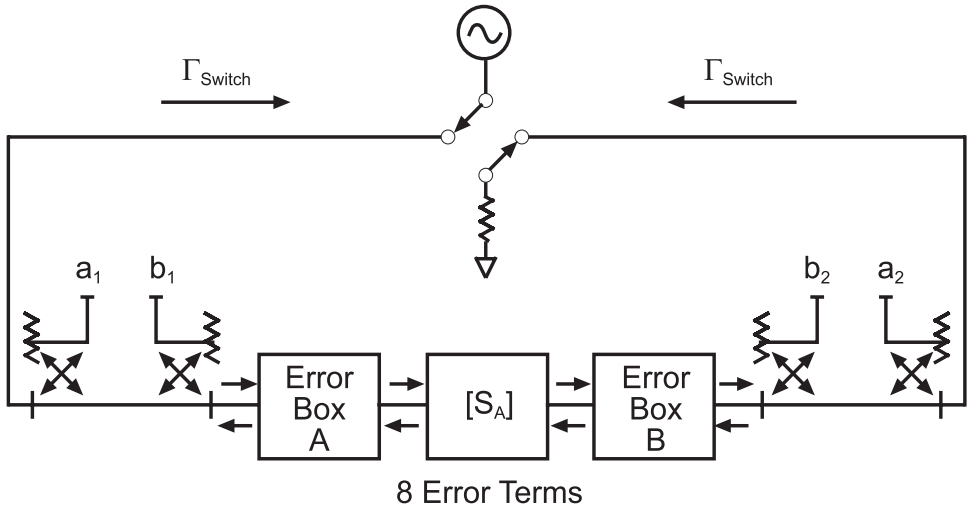
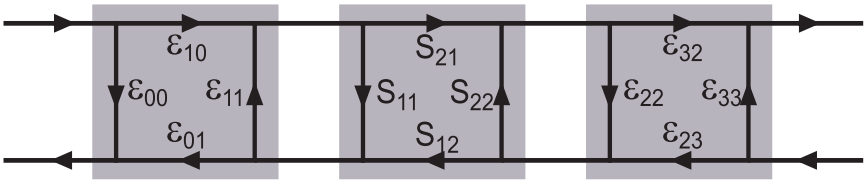



Figure 5.3: Block diagram for a two-port error-corrected measurement system.

The basic TRL calibration process is shown in figure 5.4b. In the THROUGH step, the test ports are connected with a short transmission line and then transmission frequency response and port match are measured in both directions (four measurements). For the REFLECT step, the same highly reflective device (typically a short or open circuits) is connected to each test port and its reflection coefficient is measured (two measurements). In the LINE step, a different length of transmission line is inserted and again frequency response and port match are measured in each direction (four measurements).



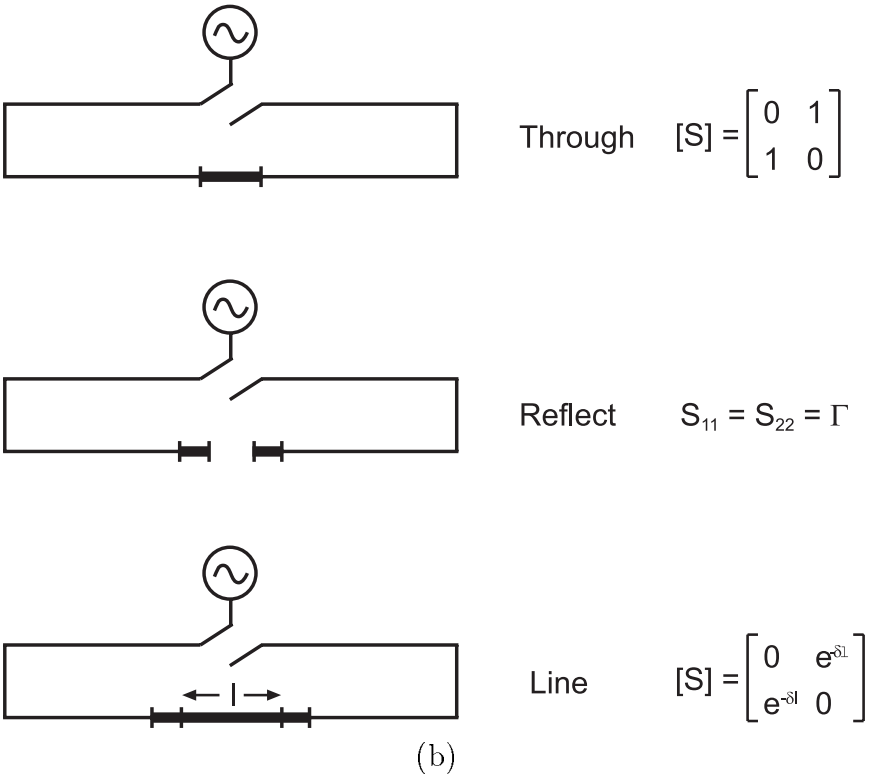

$\varepsilon_{10}\varepsilon_{01}=E_{RF}$ $\varepsilon_{23}\varepsilon_{33}=E_{RR}$

$\varepsilon_{00}=E_{DF}$ $\varepsilon_{33}=E_{DR}$

$\varepsilon_{11}=E_{SF}, E_{LR}$ $\varepsilon_{22}=E_{SR}, E_{LF}$

$\varepsilon_{10}\varepsilon_{32}=E_{TF}$ $\varepsilon_{01}\varepsilon_{23}=E_{TR}$

(a)




(b)

Figure 5.4: (a) 8-term TRL error model. (b)TRL procedure.

We have obtained ten equations from the 10 measurements. But the TRL error model shown in figure 5.4a, has only eight unknowns. Hence, two constants defining the calibration devices can also be obtained from the measurements. In the TRL solution, the complex reflection coefficient of the REFLECT standard and the propagation constant of the LINE are determined. This is significant because now these characteristics need not to be specified during the calibration. The calibration accuracy is not compromised even though these characteristics are unknown.

Up to now the solution for the error model assumes a perfectly balanced test system. The $\epsilon_{11}$ and $\epsilon_{22}$ terms represent both source and load match. However, in any switching test set, these terms are not equal. The RF switch, shown in figure 5.3, presents a different terminating impedance as its position is changed between port 1 and port 2. By measuring the ratio of the incident signals ($a_1$ and $a_2$) during the THROUGH and LINE steps, the impedance of the switch can be measured, and can be used to modify $\epsilon_{11}$ and $\epsilon_{22}$. $\epsilon_{11}$ is modified to produce forward source match ($E_{sf}$) and reverse load match ($E_{lr}$). $\epsilon_{22}$ is modified to produce reverse source match ($E_{sr}$) and forward load match ($E_{lf}$). This provides the additional corrections for this unbalanced test set.

Now, all the twelve terms of the 2-port error model are determined. Also, the reflection coefficient of the REFLECT standard and the transmission response of the LINE can be measured directly.

## 5.3 LRL implementation

To implement the TRL calibration method, we have to select and build a set of appropriate standards that meet the basic requirements of the TRL technique. Table 5.1 lists the detail requirements of the TRL calibration standards.

The HBT devices are characterized by HP8510 on-wafer network analysis from 0 to 50 GHz and from 75 to 110 GHz using (GGB Inc.) waveguide-coupled microwave wafer probes. Given the physical line length, line metal thickness, and the relative permittivity and thickness of the dielectric substrate, we can model on-wafer microstrip line by using commercial simulators such as LineCalc. On a 5$\mu$m BCB ($\epsilon_r = 2.7$) substrate, the characteristic impedance $Z_0$ of a 12.5 $\mu$m wide, 1.0 $\mu$m thick Au line is 50 $\Omega$ and the propagation velocity of the line is $2.04 \times 10^8$ m/s. Because of the

| Standard | Requirements |
|---|---|
| Reflect | Reflection Coefficient $\Gamma$ magnitude need not be known.<br>Phase of $\Gamma$ must be known within $\pm$ 1/4 wavelength.<br>Must be the same $\Gamma$ on both ports. |
| Zero Length Trough | $S_{21}$ and $S_{12}$ are defined equal to 1 at 0 degrees (typically used to set the reference plane).<br>$S_{11}$ and $S_{22}$ are defined equal to zero. |
| Non-Zero Length Through | Characteristic impedance $Z_0$ of the Through and Line must be the same.<br>Attenuation of the Through need not be known. |
| Line | $Z_0$ of the Line establishes the reference impedance after error correction is applied.<br>Insertion phase of the Line must never be the same as that of the Through(zero or non-zero length).<br>Optimal Line length is 1/4 wavelength or 90 degree relative to the Through at center frequency.<br>Usable bandwidth of a single Through/Line pair is 8:1 (frequency span/start frequency).<br>Multiple Through/Line pairs ($Z_0$ assumed identical) can be used to extend bandwidth to the extent transmission lines are realizable.<br>Attenuation of the Line need not be Known.<br>Insertion phase or electrical length need only be specified within 1/4 wavelength. |

Table 5.1: Requirements for TRL calibration standards.

probe-probe coupling we mentioned before, the HBTs are separated from the probing pads by a 230-$\mu$m-length, 12.5-$\mu$m-width, on-wafer microstrip lines. A 460 $\mu$m long 12.5 $\mu$m wide microstrip line connecting the input and output probe pads serves as a non-zero through line. The delay of the Through line is specified as zero, so the reference plane will be established in the middle of the Through Line, hence the device under test interface. The most simple Reflect standard would be an open circuit. This is done by separating probe pads the same amount as the real device, and connect a 12.5 $\mu$m wide 230 $\mu$m long microstrip line to each probe port. A short circuit could also be used, and could be made very similar structure to the opens except being ground at the ends of both transmission lines.

The Line standard requires the same characteristic impedance as the Through but a different length. So the LINE standard is also 12.5 $\mu$m wide. The insertion phase difference between the Through and LINE must be between (20 and 160 degrees) $\pm$ n $\times$ 180 degrees. Measurement uncertainty will increase significantly when insertion phase is near 0 or an integer multiple of 180 degrees. The optimal LINE length is 1/4 wavelength or 90 degree relative to the Through in the middle of desired frequency span. However, the insertion phase of the 1/4 wavelength LINE will vary with frequency. For 75-110 GHz measurement, center frequency is chosen to be the geometric mean frequency:

$$f = \sqrt{f_{start} \times f_{stop}} = \sqrt{75 \times 110} GHz = 91 GHz \tag{5.1}$$

length of the line with 1/4 wavelength at 91 GHz is given by

$$\frac{1}{4}\ \lambda_{91} = \frac{v}{4f} = \frac{2.04 \times 10^8 ms^{-1}}{4 \times 91 \times 10^9 s^{-1}} = 560 \mu m \tag{5.2}$$

The total length of the LINE for 75-110 GHz calibration is given by 460 $\mu$m + 560 $\mu$m = 1020 $\mu$m. To determine whether this LINE meets the conditions of acceptable insertion phase for the whole desired frequency range (75 GHz to 110 GHz), the following expression can be used:

$$Phase(degrees) = \frac{360 \times f \times l}{v} \tag{5.3}$$

At 75 GHz Phase = 74 degrees
At 110 GHz Phase = 109 degrees

The LINE does meet the recommended insertion phase requirements (20 and 160 degrees). Using equation (1), (2) and (3), the same calculation can be done for the 20-60 GHz band and 17-51 GHz band. The center frequency for those bands are 40 and 34 GHz, the insertion line length is 1275 and 1500 $\mu$m, see table 5.2:

| band (GHz) | center frequency (GHz) | insertion length ($\mu$m) | Phase at $f_{start}$ (degrees) | Phase $f_{stop}$ (degrees) |
|---|---|---|---|---|
| 20-60 | 34 | 1500 | 53 | 159 |
| 27-60 | 40 | 1275 | 61 | 135 |
| 75-110 | 91 | 560 | 74 | 109 |

Table 5.2: multiple lines for LINE standard for different frequency span.

Figure 5.5 shows the schematic layout of the LRL on-wafer calibration standards.

## 5.4 Calibration Verification

Now that we have the appropriate standards, they must be defined mathematically and entered into the calibration kit registers of the HP8510.

Once the calibration standards has been defined in the HP8510 cal kit, the calibration can be performed. After the error correction is applied, we need to check the calibration performance, i.e., verify the calibration. The probes are landed on the Line that we used as a cal standard. $S_{11}$ and $S_{22}$ should be less than -50 dB over the full frequency span. Figure 5.6 shows the open, short and through measurements in Smith chart from 75 to 110 GHz. Figure 5.7a shows the $S_{11}$ and $S_{22}$ of an offset open circuit, and figure 5.7b shows the $S_{11}$ and $S_{22}$ of an offset short circuit. Another way for verifying the calibration is to measure the reflection from a long open circuited line. The 20-60 GHz (1960$\mu$m) line can be used. The phase should be linear with frequency with no visible ripple or glitches. The magnitude should be monotonically decreasing with frequency due to line losses. This should be true over the full frequency span. Figure 5.8 shows the magnitude and

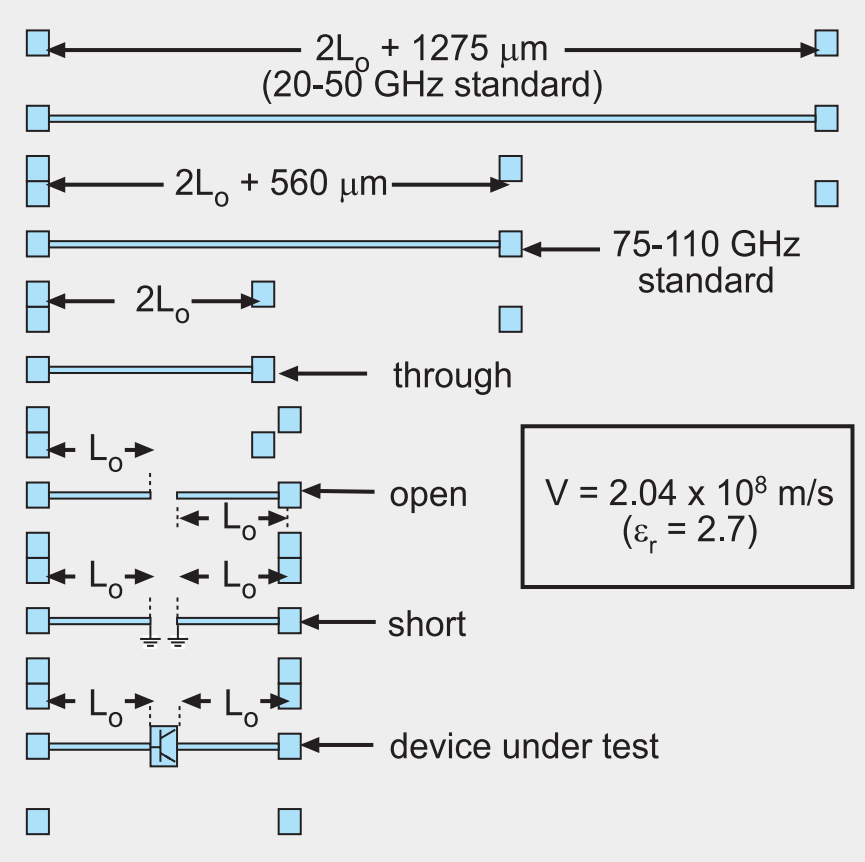



Figure 5.5: Layout of the on-wafer calibration standards.

phase of port 1 and port 2 of the open line for 75-110 GHz band. Now the HP8510 is setup to make RF measurement of the offset DUT.

Figure 5.10 shows the example measurement of a transferred-substrate HBT using the on-wafer LRL calibration.

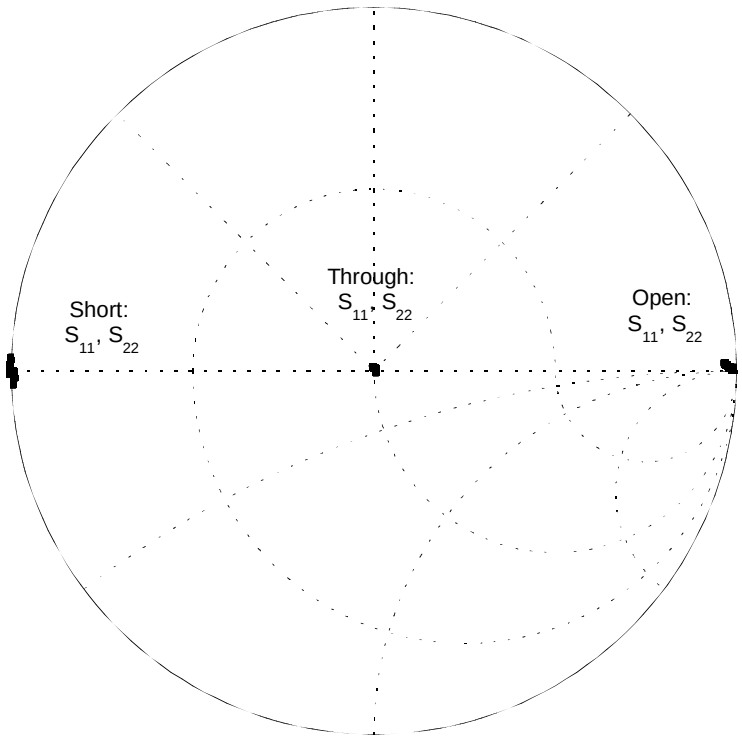
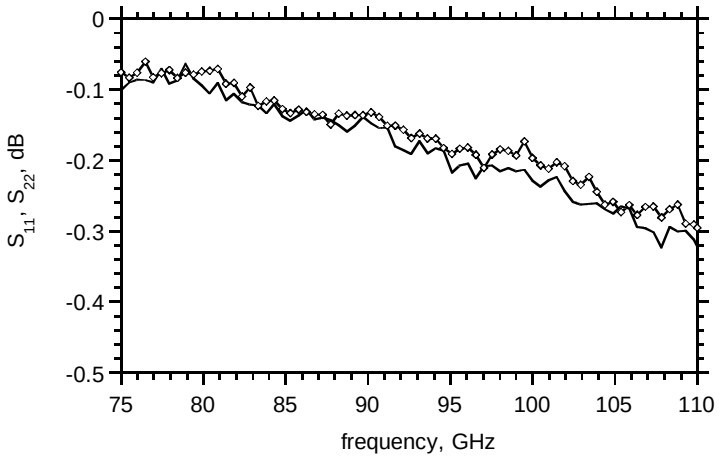
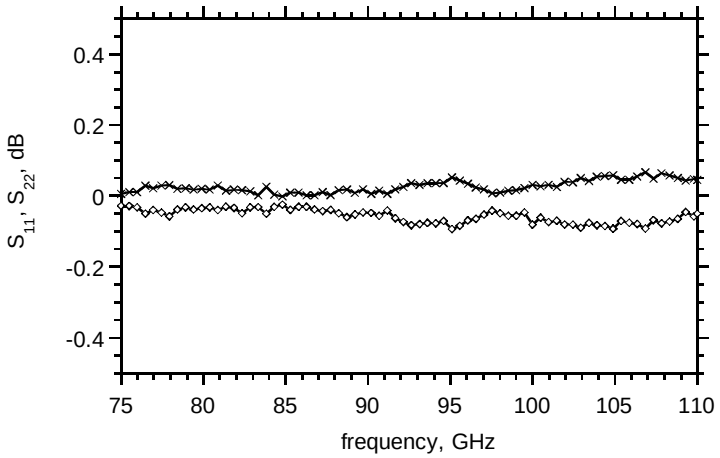



Figure 5.6: $S_{11}$, $S_{22}$ of the open, short, and through on smith chart after apply calibration.

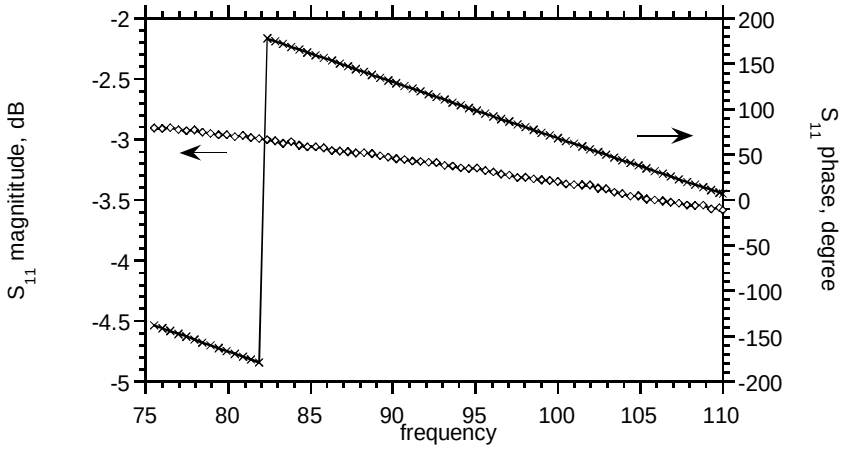



(a)

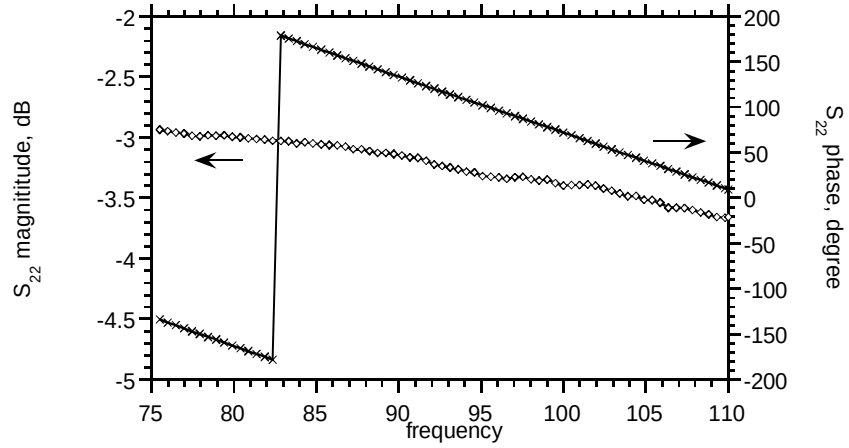



(b)

Figure 5.7: (a) $S_{11}$, $S_{22}$ measurements of open circuit after calibration. (b) $S_{11}$, $S_{22}$ measurements of short circuit after calibration.




(a)




(b)

Figure 5.8: (a) $S_{11}$ measurement of open line circuit after calibration. (b) $S_{22}$ measurement of open line circuit after calibration.

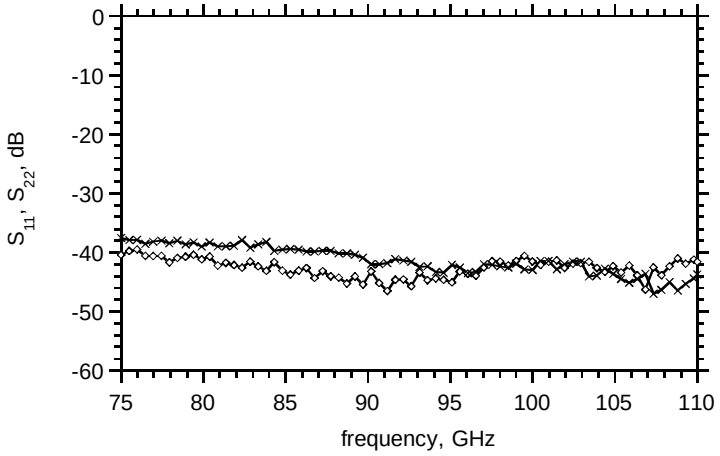



Figure 5.9: $S_{11}$, $S_{22}$ measurements of through line after calibration.

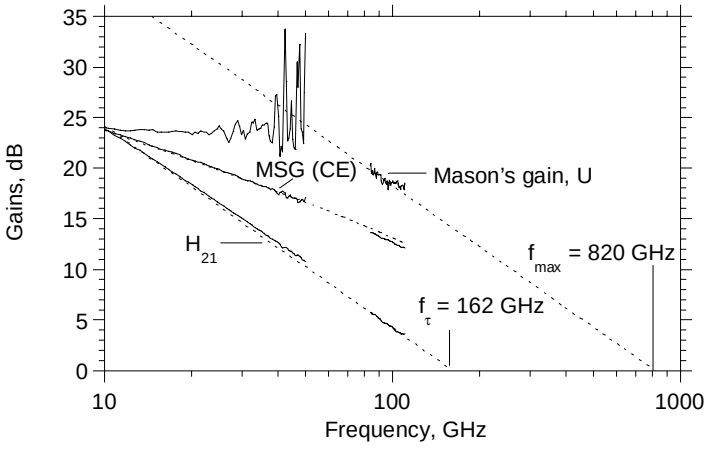



Figure 5.10: Example measurement of a transferred-substrate HBT using the LRL on-wafer calibration standards.

# Chapter 6

# Results

A variety of devices were fabricated in the transferred-substrate HBT technology with different emitter and collector widths and lengths. For process development and process control, test structures like TLM patterns were also fabricated and measured. Both DC and RF measurements were done and device parameters extracted based on these measurements.

## 6.1 Base Resistance

TLM test patterns were used to determine the base layer sheet and contact resistivity. Based on this measured data, the base resistance $r_{bb}$ of a HBT was estimated. Two kinds of TLM structures were used, and are shown in figure 6.1.

The measured resistance of the normal base TLM structure consists of contact resistance between base contact and semiconductor and sheet resistance from the etched base layer. Contact resistance depends on the doping in the base, the metal used for contact, and the processing conditions, and so it varies from run to run. Sheet resistance depends mainly on the base doping, and thickness of the etched base layer which in turn depends on the emitter mesa etch. As a consequence, the base sheet resistance also varies from run to run.

A modified TLM structure (figure 6.1b) is used to determine the extent to which the base region is etched during the emitter mesa etch. The modified TLMs have the emitter and the total base layer in the spacings that separate the TLM contact pads. Therefore, the measured sheet resistance in

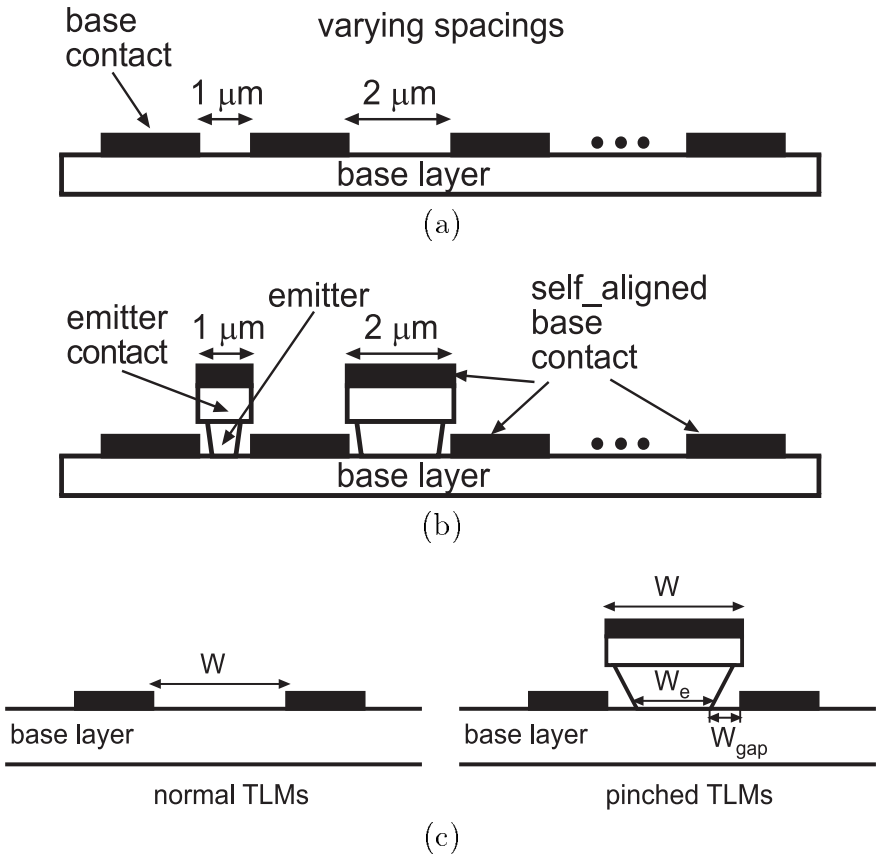



Figure 6.1: (a) normal base TLM (b) modified base TLM with emitters (c)some definitions .

these TLMs should depend on the as-grown base thickness and doping. The measured resistance consists of contact resistance (same as normal TLMs), gap sheet resistance and as-grown base sheet resistance under the emitter.

The terminal resistance for the normal TLMs is given by:

$$R_{normal} = 2\sqrt{\rho_{bc}\rho_{bs}}/L + \rho_{bs}W/L, \tag{6.1}$$

where $\rho_{bc}$ is the specific contact resistance per unit area of the metal-semiconductor interface (units of $\Omega$-cm$^2$), $\rho_{bs}$ is the base sheet resistivity (units of $\Omega/\square$, W is the gap width and L is the length of the gap. By plotting measured resistance versus gap width, $\rho_{bc}$ and $\rho_{bs}$ can be obtained.

The terminal resistance for the modified TLMs is given by:

$$R_{pinched} = 2\sqrt{\rho_{bc}\rho_{bs}}/L + 2\rho_{bs}W_{gap}/L + \rho_{bs,e}W_e/L, \tag{6.2}$$

where $W_{gap}$ is the separation between the emitter mesa and the base contact, $W_e$ is the width of the emitter mesa and the $\rho_{bs,e}$ is the sheet resistivity of the un-etched base layer under the emitter. And $W = W_e + 2W_{gap}$. $W_{gap}$ does not change with the emitter width W, hence, by plotting the measured resistance versus emitter width W, $\rho_{bs,e}$ can be determined. The ratio of the $\rho_{bs}/\rho_{bs,e}$ gives the extent to which the base layer has been etched.

Figure 6.2 shows the measured normal and pinched TLM data from a wafer with a 500 Å base. With eq. ( 6.1), ( 6.2), it is found that $\rho_{bs} = 629$ $\Omega/\square$, $\rho_{bs,e} = 540$ $\Omega/\square$, $\rho_{bc} = 8.8$ x $10^{-7}$ $\Omega$-cm$^2$, and $W_{gap} = 0.05$ $\mu$m. From $\rho_{bs,e}/\rho_{bs}$, the etched base thickness is estimated to be 500 Å x 540/629 = 429 Å. Hence, the base has been over etched by 70 Å, which is about the same as measured by B. Agarwal for a 400 Å thick base [40].

## 6.2 DC measurements

DC characterization includes DC common-emitter characteristics and Gummel plots. These were measured by a semiconductor parameter analyzer using microwave probes and bias-T to prevent microwave device oscillating during DC measurements. Results from four different wafers A, B, C, D and E are presented here. The materials and processes used in these five runs are not identical. The important differences of the layer structure and process between these four runs are shown in table 6.1.

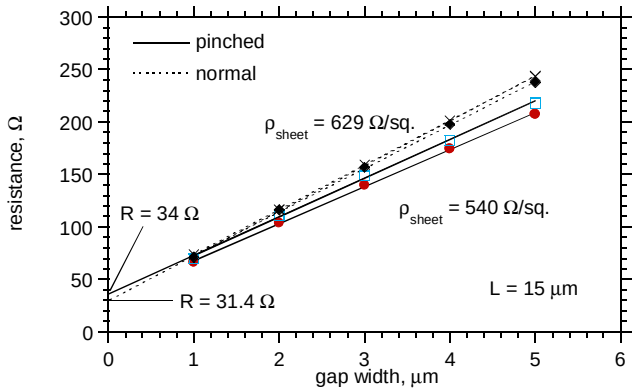



Figure 6.2: Normal and pinched TLM measurements across a quarter of a 2-inch wafer with 500 Å thick base doped at 5 x $10^{19}/cm^2$.

| | base thickness (Å) | base grading (meV) | emitter definition | selective-etch undercut ($\mu$m) | emitter length ($\mu$m) |
|---|---|---|---|---|---|
| A | 500 | 25 | contact | 0.15 | 25 |
| B | 500 | 25 | e-beam | 0.05 | 25 |
| C | 400 | 50 | e-beam | 0.05 | 6 |
| D | 400 | 50 | stepper | 0.05 | 12 |
| E | 400 | 50 | e-beam | 0.05 | 6 |

Table 6.1: Layer structure and process parameters for four different runs.

The Gummel plot of a typical transferred-substrate HBT is shown in figure 6.3. The collector current ideality factor $n_c$ is close to 1. The base current ideality factor $n_b$ is 1.2.

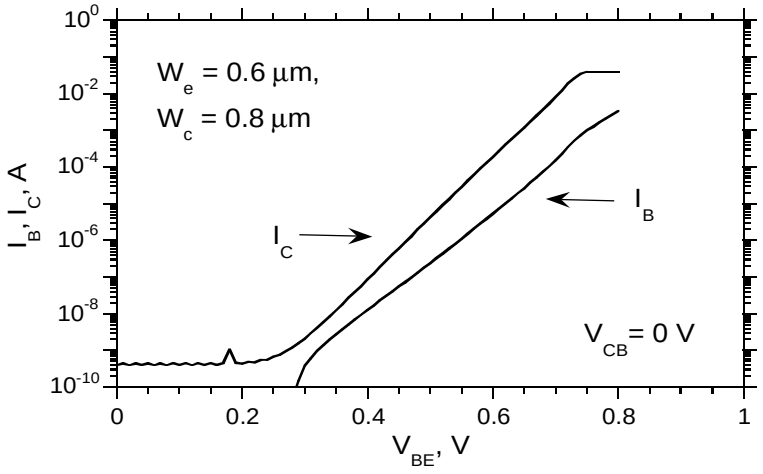



Figure 6.3: Gummel plots of transferred-substrate HBTs with 0.6 x 25 $\mu$m$^2$ emitters and 0.8 x 29 $\mu$m$^2$ collectors.

For a transistor common-emitter characteristics, the small signal current gain $\beta$, the saturation voltage at high current density and the breakdown voltage are the important features. What affects these characteristics will be discussed below.

DC current gain $\beta$ is influenced by leakage and the electron transit time through the base. Therefore, for devices with the same emitter stripe length, same emitter width, same separation between the emitter mesa and same base contact, the base layer thickness, the velocity at which electrons tranverse the base and the emitter/collector alignment will determine the small signal DC current gain $\beta$. A thin and graded base will improve $\beta$. Precise emitter/collector alignment is also observed to improve $\beta$. The narrower the emitter, the lower the current is gain $\beta$. Reducing the emitter undercut also degrades $\beta$.

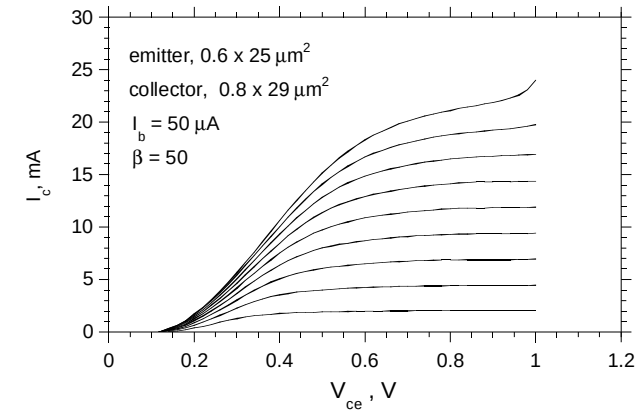
DC common-emitter characteristics of HBTs from wafer A are shown in figure 6.4. On this wafer, devices with nominal contact-aligner-defined emitter dimensions of 1 x 25 $\mu$m$^2$ and with nominal collector dimensions of 1 x 29 $\mu$m$^2$ (narrow collector) and 2 x 29 $\mu$m$^2$ (wide collector) were fabricated. The actual emitter/base junction width is 0.7 $\mu$m, and collector/base

junction widths are 0.8 and 1.8 $\mu$m. The small signal current gain at DC, $\beta$, for the narrow collector is 50, and for the wide collector is 56.

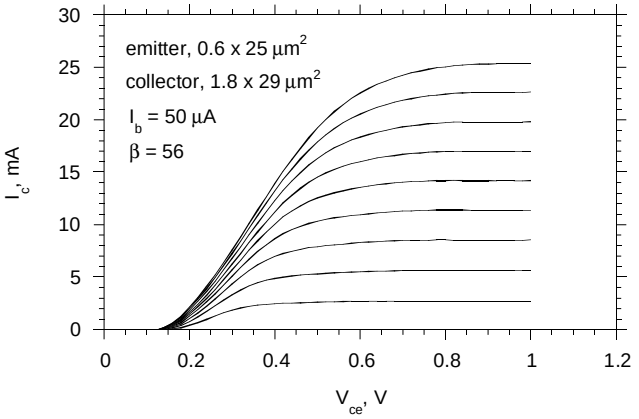
DC common-emitter characteristics of HBTs from wafer B are shown in figure 6.5. On this wafer, devices with nominal e-beam-defined emitter dimensions of 0.3 x 25 $\mu m^2$ and with nominal collector dimensions of 0.5 x 29 $\mu m^2$ (narrow collector) and 0.7 x 29 $\mu m^2$ (wide collector) were fabricated. Devices with nominal emitter dimensions of 0.5 x 25 $\mu m^2$ and with nominal collector dimensions of 0.7 x 29 $\mu m^2$ (narrow collector) and 1.1 x 29 $\mu m^2$ (wide collector) were also fabricated. The actual emitter/base junction widths are 0.2 $\mu$m and 0.4 $\mu$m, and collector/base junction widths are 0.5, 0.7 and 1.1 $\mu$m. The small signal current gain at DC, $\beta$, for the device with a 0.3 $\mu$m emitter and a 0.7 $\mu$m collector is 15, for the device with a 0.5 $\mu$m emitter and a 0.7 $\mu$m collector is 25, and for the device with a 0.5 $\mu$m emitter and a 1.1 $\mu$m collector is 32.

DC common-emitter characteristics of HBTs from wafer C are shown in figure 6.6. On this wafer, devices with nominal ebeam-defined emitter dimensions of 0.3 x 6 $\mu m^2$ and with nominal collector dimensions of 0.5 x 10 $\mu m^2$ (narrow collector) and 0.7 x 10 $\mu m^2$ (wide collector) were fabricated; and devices with nominal emitter dimensions of 0.5 x 6 $\mu m^2$ and nominal collector dimensions of 0.7 x 10 $\mu m^2$ (narrow collector) and 1.1 x 10 $\mu m^2$ (wide collector) were also fabricated. The actual emitter/base junction width are 0.2 $\mu$m and 0.4 $\mu$m, and collector/base junction widths are 0.5, 0.7 $\mu$m and 1.1 $\mu$m. The small signal current gain at DC, $\beta$, for the device with 0.3 $\mu$m emitter and 0.5 $\mu$m collector is 24, for the device with 0.3 $\mu$m emitter and 0.7 $\mu$m collector is 42.

Comparing wafers A and B, the following observations are made: both wafers have the same base thickness and grading; devices with wider emitter (0.6 $\mu$m on A vs. 0.3 & 0.5 $\mu$m on B) have higher $\beta$ (50 vs. 14 & 32); devices with same emitter width but wider collector (collector of 0.5 $\mu$m vs. 0.7 $\mu$m for a 0.3$\mu$m emitter) have higher $\beta$ (25 vs. 15). This is due some way to the collector not fully covering the emitter. Comparing wafers B and C, the following observation are made: both wafers are written by e-beam lithography and have similar device dimensions; devices with the similar emitter/collector dimensions on wafer C have significantly higher $\beta$ than those on wafer B, this is because of two reasons: one is that wafer C has thinner base (400 Å on C vs. 500 Å on B) and higher bandgap grading (50 meV for C vs. 25 meV for B). The device-by-device alignment done in the

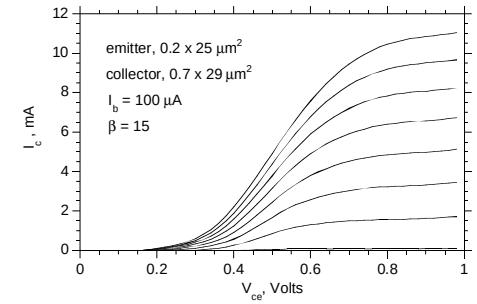



(a)

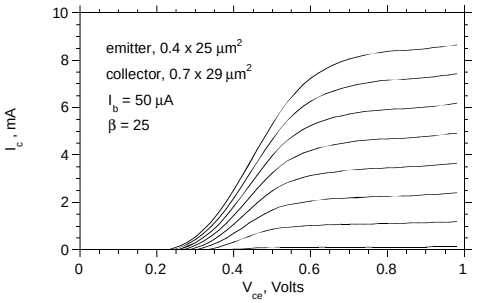



(b)

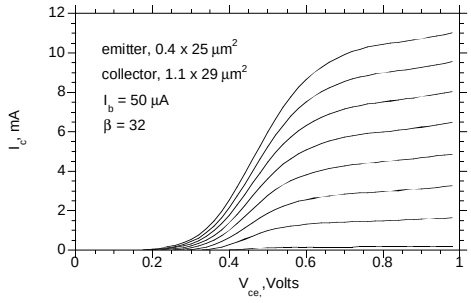
Figure 6.4: DC common-emitter characteristics of devices on wafer A with 0.7 x 25 $\mu$m$^2$ emitters and (a) 0.8 x 29 $\mu$m$^2$ collectors and (b) 1.8 x 29 $\mu$m$^2$ collectors.




(a)

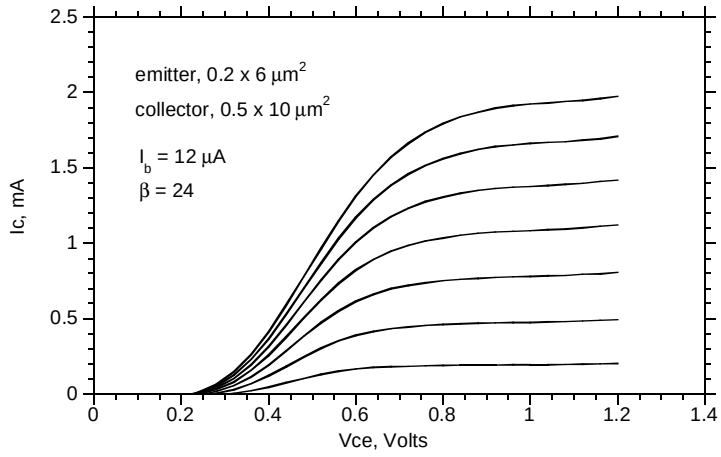



(b)

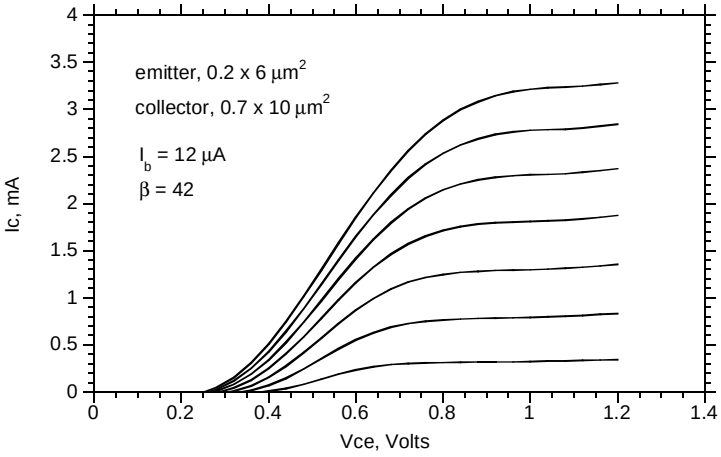



(c)

Figure 6.5: DC common-emitter characteristics of devices on wafer B with (a) 0.3 x 25 $\mu$m$^2$ emitters and 0.8 x 29 $\mu$m$^2$ collectors, (b) 0.5 x 25 $\mu$m$^2$ emitters and 0.7 x 29 $\mu$m$^2$ collectors and 0.5 x 25 $\mu$m$^2$ emitters and 1.1 x 29 $\mu$m$^2$ collectors.




(a)




(b)

Figure 6.6: DC common-emitter characteristics of devices on wafer C with 0.3 x 6 $\mu$m$^2$ emitters and (a) 0.5 x 10 $\mu$m$^2$ collectors and (b) 0.7 x 6 $\mu$m$^2$ collectors.

case of wafer C as compared to a cell-by-cell alignment for wafer B offers additional improvement in $\beta$.

The slope in the linear part of the common-emitter characteristics and the saturation voltage $V_{ce,sat}$ are also important device DC characteristics. They are determined by field collapse in the collector depletion region, and influenced by the lateral electron spreading within the collector. At a collector current density $J_c$, the potential $\phi(x)$ in the collector at a distance x from the base, is related to the current flowing through the collector space charge region by Poisson's equation as

$$\frac{\partial^2 \phi(x)}{\partial x^2} = \frac{J_c/v_{sat} - qN_d}{\epsilon} \tag{6.3}$$

where $v_{sat}$ is the electron velocity, and $N_d$ is the collector doping. calculating the total potential drop across the collector, the following relation are obtained:

$$V_{cb} + \phi = T_c^2 \frac{J_c/v_{sat} - qN_d}{2\epsilon} \tag{6.4}$$

and

$$\Delta V_{cb} = \Delta J_c \frac{T_c^2}{2\epsilon v_{sat}} \tag{6.5}$$

where $T_c$ is the collector thickness, and $\phi$ is the emitter-base junction built-in potential. From eq.( 6.4), it is shown that the electrostatic field in the collector is screened by the electron space charge in the collector. At high current density, narrow-collector devices show significantly larger collector-emitter saturation voltages ($V_{ce,sat}$) due to this screening effect. In devices with wider collectors, there is significant lateral spreading of the electrons at high current densities, and hence leading to less space charge screening in the collector and lower saturation voltage $V_{ce,sat}$. Lateral current confinement in narrow-collector devices causes increased $V_{ec,sat}$ and decreased on-set current density of Kirk effects, resulting in reduced peak $f_\tau$. Eq.( 6.5) shows the changes in voltage and current density across the collector space charge region are linearly related. The proportionality constant (space charge resistance) $R_{sc} = \Delta V_{cb}/\Delta I_c = T_c^2/(2\epsilon A_e v_{sat})$ determines the slope in the linear region of the common-emitter characteristics. Table 6.2 shows the calculated $R_{sc}$ of different device sizes form wafer A, B and C.

| | wafer ID | emitter-width ($\mu$m) | collector-area ($\mu$m$^2$) | current-gain $\beta$ | $R_{sc}$ ($\Omega$) |
|---|---|---|---|---|---|
| 1 | A | 0.6 | 29 | 50 | 20 |
| 2 | A | 0.6 | 58 | 56 | 15 |
| 3 | B | 0.3 | 20.3 | 15 | 35.2 |
| 4 | B | 0.5 | 20.3 | 25 | 37.3 |
| 5 | B | 0.5 | 31.9 | 32 | 28 |
| 3 | C | 0.3 | 5.0 | 24 | 220 |
| 4 | C | 0.3 | 7.0 | 42 | 145 |

Table 6.2: Current gain and space-charge resistance $R_{sc}$ for different device sizes from different wafers.

$R_{sc}$ deceases with larger width collectors because the electrons can spread laterally in the collector, reducing the collector current density, hence leading to an increase in the effective area of $A_c$ that determines the space charge resistance.

The collector recess etch also affects transistor DC characteristics. Without collector recess etching, the electrons spread laterally in the collector to regions where there is no collector contact. When the electrons spread into regions of lower field (outside the collector contact), higher vertical field has to be applied for the electrons to reach the collector contact. Therefore, the saturation voltage $V_{ce,sat}$ increases. After collector recess etching, the electrons are confined to the area under the collector contact. $V_{ce,sat}$ is reduced, and collector current density at the Kirk effect threshold decreased.

The common-emitter breakdown voltage $BV_{CEO}$ is $\sim 3$ V, and decreases as the bias current is increased, reaching $\sim$ 1.5 V at 1-2 x $10^5$ A/cm$^2$. The breakdown voltage is low due to the narrow-bandgap InGaAs collector material. InP collectors with a InGaAs/InAlAs linear grade would provide much higher breakdown voltage. This is essential for further scaling of the transferred-substrate HBTs both vertically and laterally.

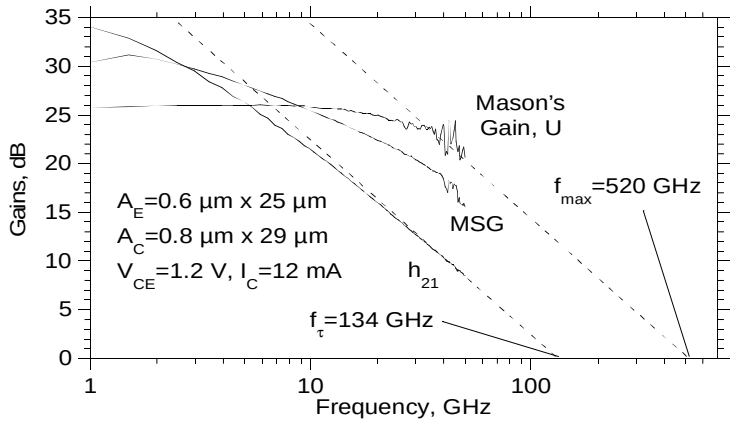
## 6.3 RF measurements

The devices were characterized by HP8510 on-wafer network analysis from 0 to 50 GHz and 75-110 GHz using (GGB Inc.) waveguide-coupled microwave wafer probes. Short circuit current gain $h_{21}$ is defined as the small signal current gain of the device with the output shorted. The unilateral gain U (Mason's gain)[14] is the power gain when a device with a lossless reactive feedback network connects between input and output designed to make $S_{12}$ for the overall device equal to zero, and then subsequently providing impedance matches at the device input and output with lossless networks. To the extent that the transistor is modeled by a hybrid-$\pi$ model, $H_{21}$ and U vary as -20 dB/decade. U is independent of the transistor configuration (common-base vs. common-emitter) and independent of pad inductive and capacitive parasitics. Thus, $h_{21}$ and U are used to extrapolate the short circuit current gain cutoff frequency $f_\tau$ and the power gain cutoff frequency $f_{max}$.

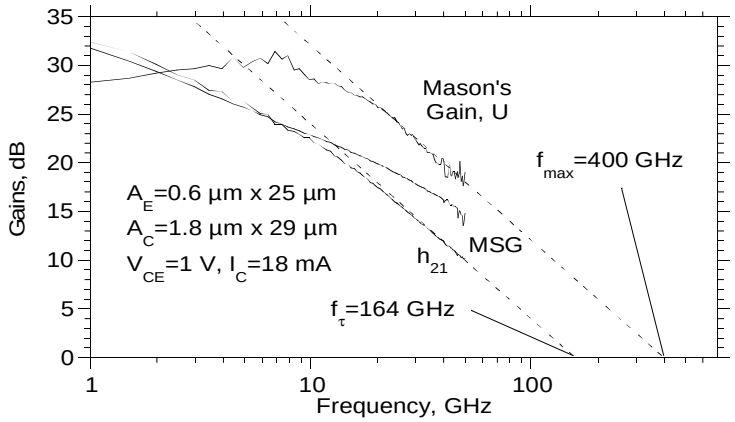
### 6.3.1 Wafer A: Optical Contact lithography

Figure 6.7 shows the $h_{21}$, $G_{max}$ and U for devices from wafer A. This wafer had a 500 Å base with 25 meV bandgap grading and a 2700 Å thick collector. The devices were characterized by on-wafer analysis to 50 GHz. Pad parasitics on these devices, fabricated with thick BCB ($\simeq$ 10 $\mu$m), is small enough to be neglected. Biasing at $V_{ce}$ = 1.2 volts and $I_c$ = 12 mA, devices with 0.6 x 25 $\mu m^2$ emitters and 0.8 x 29 $\mu m^2$ collectors obtained 8.6 dB current gain and 20.6 dB unilateral power gain at 50 GHz (figure 6.7a). Extrapolating at -20 dB/decade, the current gain cut-off frequency $f_\tau$ is 134 GHz and the power gain cutoff frequency $f_{max}$ is 520 GHz. Biasing at $V_{ce}$ = 1.1 volts and $I_c$ = 24 mA, devices with 0.6 x 25 $\mu m^2$ emitters and 1.8 x 29 $\mu m^2$ collectors obtained 10.0 dB current gain and 18.0 dB unilateral power gain at 50 GHz (figure 6.7a). Extrapolating at -20 dB/decade, the current gain cut-off frequency $f_\tau$ is 164 GHz and the power gain cutoff frequency $f_{max}$ is 400 GHz. RF measurements are at the limits of reliability for a 50 GHz instrument. W-band measurements are to determine device $f_{max}$ above $\sim$ 400 GHz.

Figure 6.8 shows the variation of $f_\tau$ and $f_{max}$ with bias. $f_\tau$ is similar for both the devices. At low bias currents, $f_\tau$ is dominated by the emitter

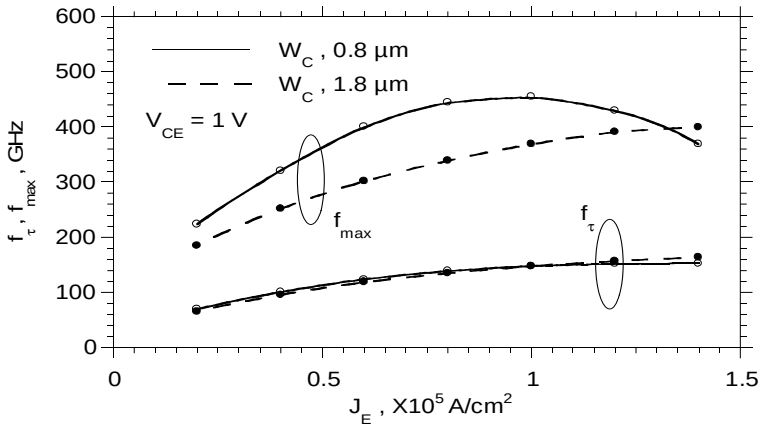



(a)

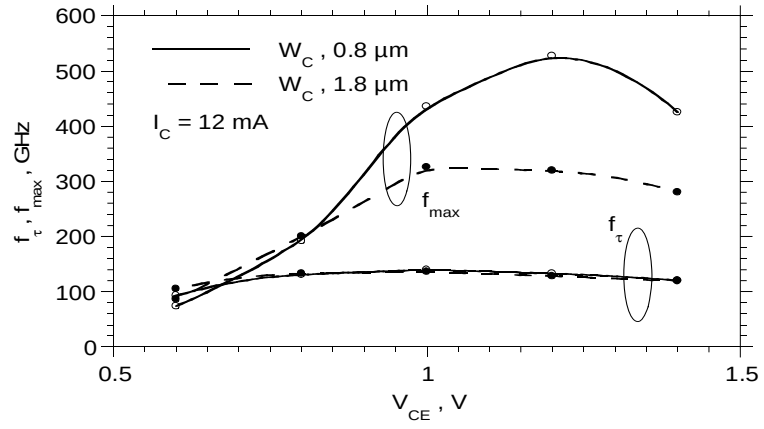



(b)

Figure 6.7: Gains of (a) 0.6 x 25 $\mu$m$^2$ emitter and 0.8 x 29 $\mu$m$^2$ collector HBT, and (b) 0.6 x 25 $\mu$m$^2$ emitter and 1.8 x 29 $\mu$m$^2$ collector HBT from wafer A. Theoretical -20 dB/dec. ($H_{21}$ and U) and -10 dB/dec. (MSG) gain slopes are indicated.




(a)




(b)

Figure 6.8: Variation of $f_\tau$ and $f_{max}$ with (a) emitter current density and (b) collector-emitter voltage for devices from wafer A.

charging time $(kT/qI_e)C_{je}$. As the bias current increases, $f_\tau$ increases due to the reduced emitter charging time. The leveling off of $f_\tau$ at high currents is due to the base push out (Kirk-effect). The on-set current of Kirk effect is lower for the devices with narrow-collectors than those with wide-collectors.

Chapter 3 will show that the intrinsic $C_{cbi}$ reduces with bias current by the relation

$$\frac{C_{cbi}}{A_e} = \frac{\epsilon}{T_c} - J_c \frac{\partial \tau_c}{\partial V_{cb}} \tag{6.6}$$

The reduction of $C_{cbi}$ is more pronounced for devices with narrow collectors than those with wide collectors because of the smaller collector current density in the wider collectors due to the electron spreading more in the wide collectors. Therefore, $f_{max}$ is higher for the narrow-collector devices. $f_{max}$ decreases at low bias current due to two reasons. First, $f_\tau$ is lower at lower bias current. Second, the reduction of $C_{cbi}$ is less for a lower collector current. At very high collector currents, the base pushes out, thus increasing $C_{cb}$, hence decreasing $f_{max}$. Variations of $f_\tau$ and $f_{max}$ with collector-emitter voltage $V_{ce}$ for collector current $I_c$ = 12 mA are shown in figure 6.8b. At low currents and low $V_{ce}$, the collector-base junction is partially depleted. $C_{cb}$ is high due to the undepleted collectors, hence $f_\tau$ and $f_{max}$ are low. With very high $V_{ce}$, electrons in the collectors gain enough energy to transfer to the satellite valley, where the electron velocity is lower. Hence $f_\tau$ and $f_{max}$ decrease with increasing $V_{ce}$ beyond 1.1 V.

### 6.3.2 First Generation E-beam Lithography Devices

Figure 6.9 shows the $h_{21}$, $G_{max}$ and U for devices from wafer B. This wafer has an identical layer structure to wafer A. The emitter and collector are defined by e-beam lithography. W-band gain measurements of 0.4 x 25 $\mu m^2$ emitter/1.0 x 29 $\mu m^2$ collector devices indicated 500 GHz $f_{max}$ and 152 GHz $f_\tau$. As discussed in chapter 4, to avoid measurement errors (in $S_{12}$, hence U) arising from microwave probe-probe coupling, the HBTs are separated from the probe pads by 400-$\mu$m-length on-wafer microstrip lines. Unfortunately, on-wafer LRL calibration standards were not available, and line losses could not be extracted in determining the 500 GHz $f_{max}$; an estimated correction for these leads to an estimated $\sim$ 600 GHz $f_{max}$. The relatively low $f_\tau$ compared to wafer A results from base push out at lower current densities, in turn caused by the emitter/collector misalignment. The

relatively low $f_{max}$ compared to wafer A results from line loss in reference lines and emitter/collector misalignment.

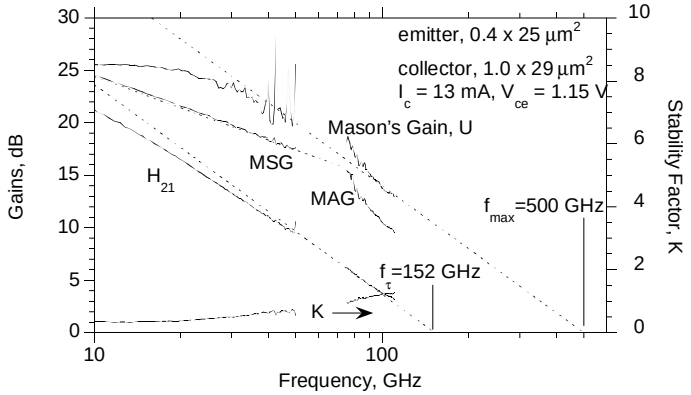



Figure 6.9: Gains of 0.4 x 25 $\mu$m$^2$ emitter and 1.0 x 29 $\mu$m$^2$ collector HBT on wafer B. Theoretical -20 dB/dec. ($H_{21}$ and U) and -10 dB/dec. (MSG) gain slopes are indicated.

### 6.3.3 Second Generation E-beam Lithography Devices

Figure 6.10 shows the $h_{21}$, $G_{max}$ and U for devices from wafer C. This wafer had a 400 Å base with 50 meV bandgap grading and a 2700 Å thick collector. The emitters are defined by e-beam lithography. Further, the collectors are aligned to the emitters device-by-device using e-beam lithography. Again, the HBTs are separated from the probe pads by 230-$\mu$m-length on-wafer microstrip lines here. On wafer LRL calibration standards were used to de-embed the transistor S-parameters. Biasing at $V_{ce} = 1.2$ volts and $I_c = 5.0$ mA, devices with 0.4 $\mu$m emitter and 1.1 $\mu$m collector widths showed 3.2 dB current gain and 17.5 dB unilateral power gain at 110 GHz. Extrapolating at -20 dB/decade, the current gain cut-off frequency $f_\tau$ is 162 GHz and the power gain cut-off frequency $f_{max}$ is a record 820 GHz. The common-emitter and common-base maximum stable gains are 12.2 dB and 16.0 dB at 110 GHz.

The $f_\tau$ is higher than wafer A and B because of the thinner, graded base and better emitter/collector alignment. The $f_{max}$ is higher than wafer A

as a result of scaling of HBT junction widths and from partial screening of the collector-base capacitance by the collector space charge. Normalizing to the emitter junction area $A_e$ to correct for differing device sizes, devices from wafer A exhibited $R_{bb}A_e = 72\ \Omega - \mu m^2$ and $C_{cbi}/A_e = 0.42$ fF/$\mu m^2$[19] vs $R_{bb}A_e = 58\ \Omega - \mu m^2$ and $C_{cbi}/A_e = 0.17$ fF/$\mu m^2$ (will be discussed later) for devices from wafer C. The reduction in $R_{bb}A_e$ results from scaling, while the reduction in $C_{cbi}/A_e$ results from the reduction of $C_{cbi}$ through the differential space-charge effect[24], [25] under the combined conditions of high current density and high collector-emitter bias voltage. In comparing the devices from wafer C with those from wafer B, the high $f_{max}$ results from the better emitter/collector alignment, shorter emitter/collector lengths which allow devices to be biased much harder, leading to larger $C_{cbi}$ reduction, and more accurate RF gain measurements due to the on-wafer LRL calibration.

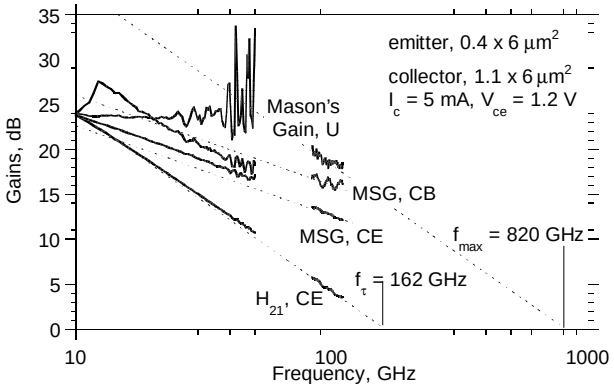



Figure 6.10: Gains of 0.4 x 6 $\mu m^2$ emitter and 1.1 x 10 $\mu m^2$ collector HBT on wafer C. Theoretical -20 dB/dec. ($H_{21}$ and U) and -10 dB/dec. (MSG) gain slopes are indicated.

Figure 6.11 shows the variation of $f_\tau$ and $f_{max}$ with bias for wafer C. At low $V_{ce}$, the collector is partially depleted leading to increased $C_{cb}$ and decreased $f_{max}$ as with the other devices. At high $V_{ce}$, $f_\tau$ and $f_{max}$ decrease as before. The measured $f_\tau$ vs. $V_{ce}$ indicates $\partial\tau_c/\partial V_{ce} \cong 0.15$ ps/Volt, predicting 0.75 fF reduction in $C_{cbi}$ at $I_c = 5$mA. In order to make this $C_{cbi}$ reduction more significant, a collector width close to emitter width is preferred due to the better collector space charge confinement in the narrow

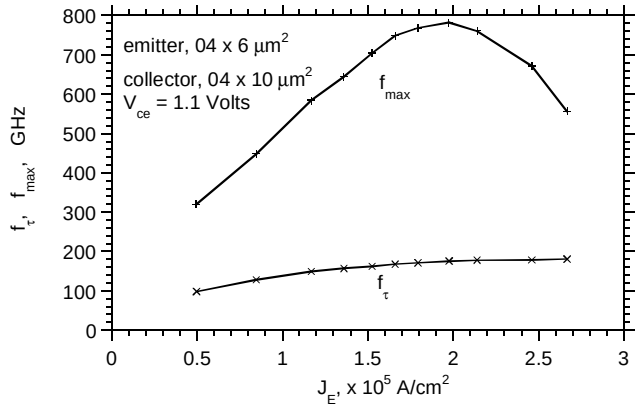
collectors. The shorter length device is preferred because it can be biased more uniformly and consequently a higher current density can be applied before reaching the on-set current of the Kirk effect (1 x $10^5$ A/cm$^2$ for devices with 0.6 x 25 $\mu$m$^2$ emitter, vs. 2 x $10^5$ A/cm$^2$ for devices with 0.4 x 6 $\mu$m$^2$ emitter).

### 6.3.4 Third Generation E-beam lithography Devices

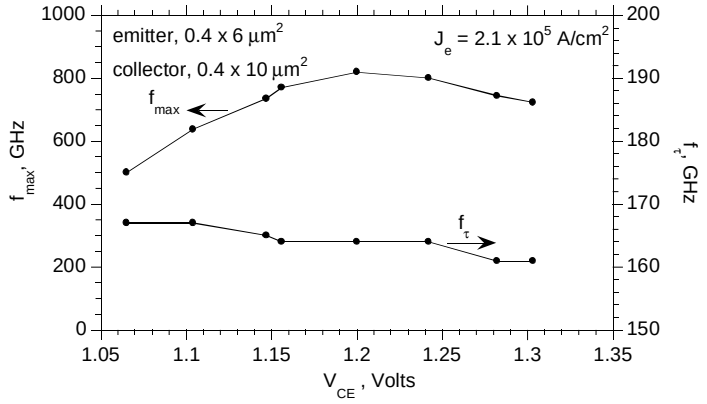
Figure 6.12 shows the $h_{21}$, $G_{max}$ and U for devices from wafer E. This wafer had identical layer structure and process as wafer C. Improved e-beam lithography leads to narrower and more reproducible collector widths. Biasing at $V_{ce}$ = 1.2 volts and $I_c$ = 6.0 mA, devices with nominal 0.4 $\mu$m emitter and nominal 1.1 $\mu$m collector widths showed 5.2 dB current gain and 19.6 dB unilateral power gain at 110 GHz. Extrapolating at -20 dB/decade, the current gain cut-off frequency $f_\tau$ is 204 GHz and the power gain cut-off frequency $f_{max}$ is a record 1080 GHz. The common-emitter maximum stable gains are 14.2 dB at 110 GHz. The $f_\tau$ is higher than wafer C because of better emitter/collector alignment. Because of the poor line width controllability of collector ebeam writing, the collector linewidth in wafer E is narrower than expected($C_{cb}$ extracted from $Im(Y_{12})$ is 3.2 fF for wafer C, 2.2 fF for wafer E). Hence, the $f_{max}$ in wafer E results from narrower collector-base junction widths and better emitter/collector alignment. The measurement is beyond the instrument reliability. A wider bandwidth network analyzer (140 GHz-220 GHz) is needed to perform more accurate RF gain measurements and verify the results of wafer E.

Figure 6.13 shows the variation of $f_\tau$ and $f_{max}$ with bias.

Figure 6.14 shows the results of lateral scaling in the transferred-substrate HBTs. Shown in the figure is the variation of $f_\tau$ and $f_{max}$ with emitter current density for two different devices. The first one has 0.6 x 25 $\mu$m$^2$ emitter and 1.8 x 29 $\mu$m$^2$ collector. The second one has 0.4 x 6 $\mu$m$^2$ emitter and 1.1 x 10 $\mu$m$^2$ collector. These two devices are from different wafers, and thus have slightly different parameters, but the general scaling trend can be clearly observed. Scaling improves $f_{max}$ by a large amount. It is expected that with further deep submicron scaling of emitter and collector dimensions, and with improved emitter/collector registration, a power gain cutoff frequency well in excess of 1000 GHz can be obtained.




(a)




(b)

Figure 6.11: Variation of $f_\tau$ and $f_{max}$ with (a) emitter current density and (b) collector-emitter voltage for devices from wafer C.

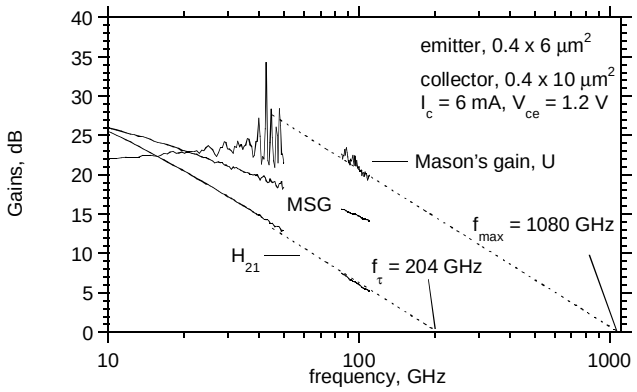
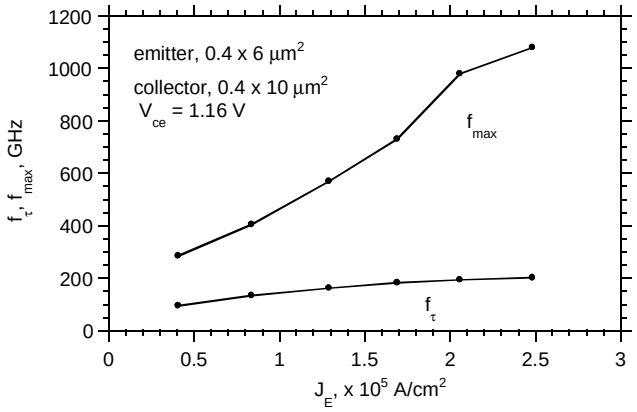


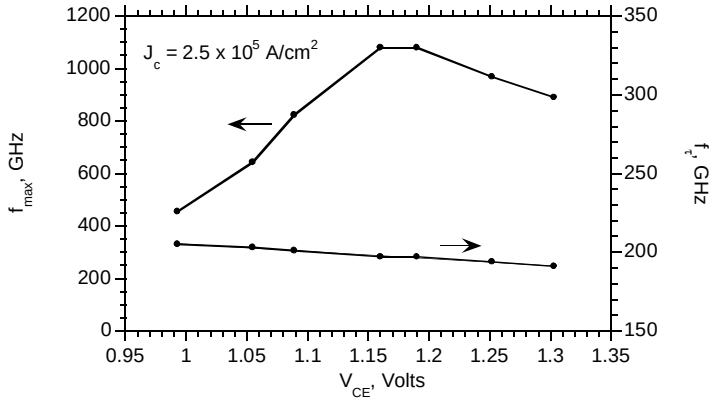

Figure 6.12: Gains of nominal 0.4 x 6 $\mu$m$^2$ emitter and nominal 1.1 x 10 $\mu$m$^2$ collector HBT on wafer E. Theoretical -20 dB/dec. ($H_{21}$ and U) and -10 dB/dec. (MSG) gain slopes are indicated.

### 6.3.5 Optical Projection Lithography (Stepper) Defined Transferred-substrate HBTs

Submicron devices fabricated with e-beam lithography have shown superb rf performance. E-beam lithography, though, is not suitable for integrated circuits. This is because e-beam writing is quite time-consuming and very hard to set-up for big circuits. Optical projection lithography (stepper) offers very high yield of minimum feature size of 0.5 $\mu$m, hence it is the tool for integrated circuits. Figure 6.15 shows the $h_{21}$, $G_{max}$ and U for devices from wafer D. On this wafer, both emitter and collector are defined by the stepper. This wafer has the identical layer structure as wafer C. Similarly to C, the network analyzer is calibrated by the on-wafer LRL calibration standards. Devices with 0.4 x 6 $\mu$m$^2$ emitter and 1.1 x 10 $\mu$m$^2$ collector exhibit extrapolated current gain cutoff frequency $f_\tau$ of 147 GHz and power gain cutoff frequency $f_{max}$ of 805 GHz. The slightly lower $f_\tau$ than devices from wafer C is due to less precise emitter/collector alignment. With these high bandwidth transistors, integrated circuits operating up to 100 GHz should be feasible.




(a)




(b)

Figure 6.13: Variation of $f_\tau$ and $f_{max}$ with (a) emitter current density and (b) collector-emitter voltage for devices from wafer E.

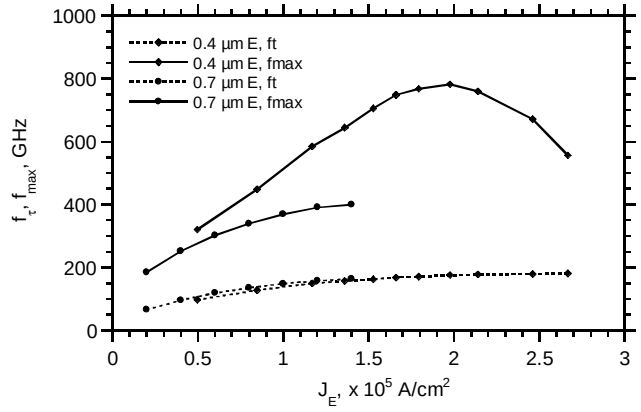



Figure 6.14: Variation of $f_\tau$ and $f_{max}$ with $J_e$ for devices with different geometry.

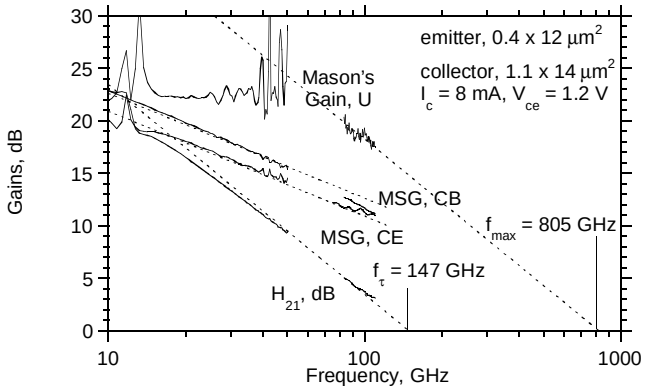



Figure 6.15: Gains of 0.4 x 6 $\mu$m$^2$ emitter and 1.1 x 10 $\mu$m$^2$ collector HBT fabricated by stepper. Theoretical -20 dB/dec. ($H_{21}$ and U) and -10 dB/dec. (MSG) gain slopes are indicated.

## 6.4 Hybrid-$\pi$ Models of Transferred-substrate HBTs

Small-signal hybrid-$\pi$ models of transferred-substrate HBTs from wafer C were developed. Figure 6.16 shows a small-signal model for a device from wafer C with a 0.4 x 6 $\mu m^2$ emitter and a 0.4 x 10 $\mu m^2$ collector biased at $I_c$ = 5 mA and $V_{ce}$ = 1.2 V. Base resistance $R_{bb}$ consists of spreading resistance, contact resistance and base-emitter gap resistance. The measured base sheet resistance is 600 $\Omega/\Box$ and the specific contact resistance is 50 $\Omega$-$\mu m^2$. With these parameters, we calculate a 24 $\Omega$ base resistance. $R_{ex}$ is given by the intercept of the curve of $Re\{Y_{21}\}$ vs. $1/I_c$ and is found to be 15 $\Omega$. By plotting $1/2\pi f_\tau$ versus $1/J_e$, it is determined that the sum of the base and collector transit times ($\tau_b$ + $\tau_c$) is 0.59 ps, and the sum of the collector-base and base-emitter depletion capacitances ($C_{cb}$ + $C_{be,depl}$) is 39 fF. $R_{cb}$ and the total $C_{cb}$ are extracted by plotting the real and imaginary part of the admittance parameter $Y_{12}$ versus frequency. $R_{cb}$ represents the variation of collector-base leakage with bias, likely due to impact ionization. Base-width modulation in HBTs is negligible, hence $R_{ce}$ is large. $C_{be,poly}$ is a calculated metal-polyimide-metal overlap capacitance between the emitter and base metalizations. The 3.2 fF sum of $C_{cbi}$ and $C_{cbx}$ is of the magnitude expected from the combination of ($\epsilon A_c/T_c$) 1.5 fF collector junction capacitance and ($\sim$ 10 $\mu$m x 150 fF/mm) metal-metal fringing capacitance between the base ohmic metal and the transmission line contacting the collector. Inclusive of the differential space-charge effect [24], [25], observed earlier in MESFETs [26], $C_{cbi} = \epsilon A_E/T_c$ - $I_c \partial\tau_c/\partial V_{ce}$, where $T_c$ is collector thickness and $\partial\tau_c/\partial V_{ce}$ is the variation in collector transit time with bias. The measured $f_\tau$ vs. $V_{ce}$ (figure 4) indicates $\partial\tau_c/\partial V_{ce} \cong$ 0.05 - 0.15 ps/Volt, predicting $C_{cbi} \cong$ 0.13 fF - 0.63 fF at $I_c$ = 5 mA. $C_{cbi}$ = 0.4 fF is determined by fitting to the measured unilateral gain. This is 2.2:1 smaller than the expected zero-current capacitance ($\epsilon A_E/T_c$ = 0.88 fF). The measured S-parameters (figure 6.17), $h_{21}$ and U (figure 6.18) show good correlation to that of the hybrid-$\pi$ model.

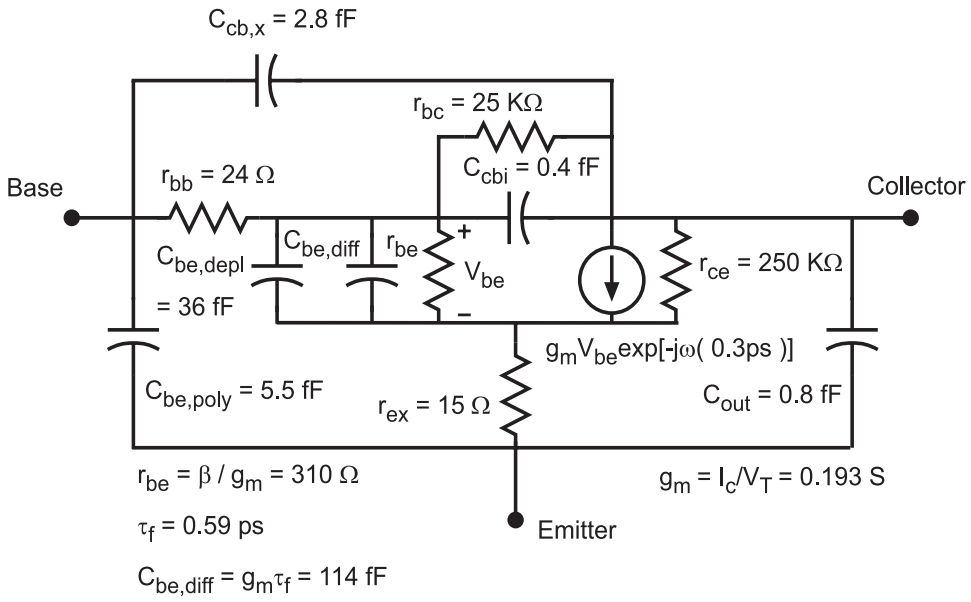



Figure 6.16: Device equivalent circuit model for device with 0.4 x 6 $\mu$m$^2$ emitter and 1.1 x 10 $\mu$m$^2$ collector at $V_{ce} = 1.2$ V and $I_c = 5$ mA.

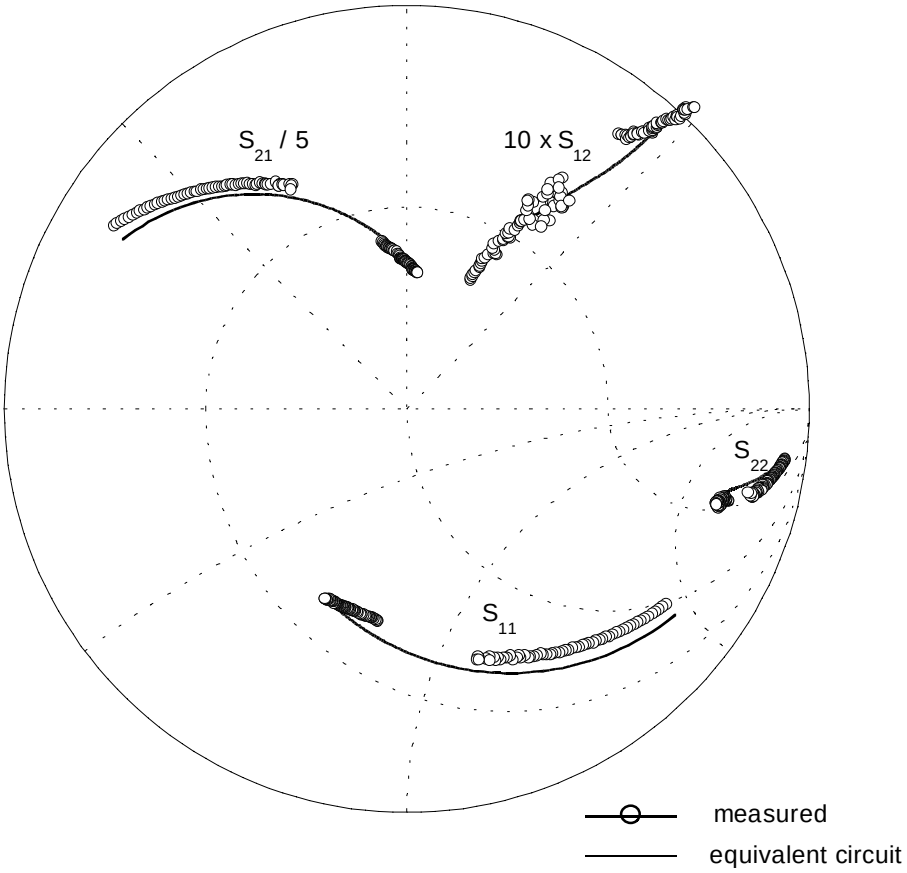



Figure 6.17: Measured device S-parameters (10-50 & 75-110 GHz) at $V_{ce}$ = 1.2 V and $I_c$ = 5 mA. The solid line represents S-parameters of the equivalent circuit model.

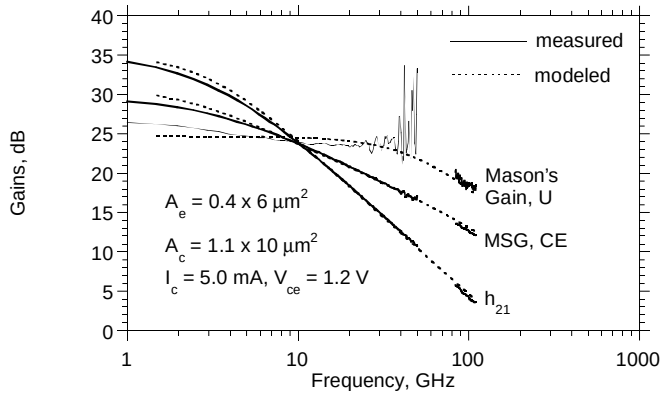



Figure 6.18: Comparison of measured and hybrid-$\pi$ modeled RF gains of devices from wafer C.

Devices with 164 GHz $f_\tau$ and 820 GHz$_{max}$ have been obtained by the transferred-substrate HBT technology. The $f_{max}/f_\tau$ ratio is $\sim 5$, which is very large. With the exception of reactively-tuned circuits, for which $f_{max}$ is the sole determinate of circuit bandwidth, circuit design generally requires both high $f_\tau$ and $f_{max}$. Examining significant terms in $1/2\pi f_\tau$, with 400 Å thick and 50 meV bandgap grading base, $\tau_b + \tau_c$ is small at 0.6 ps, while the Schottky collector eliminates $R_c C_{cb}$. At peak $f_\tau$ bias, $(C_{je} + C_{cb})/g_m \simeq 0.1$ ps. Presently $R_{ex}C_{cb} \simeq 0.1$ ps, and has significant impact upon $f_\tau$. To obtain $> 500$ GHz both $f_\tau$ and $f_{max}$, device has to be scaled into deep submicron dimensions laterally, base bandgap grading must be increased, the collector thinned, and InAs emitter Ohmic contact layers employed.

Transferred-substrate HBT technology has demonstrated a record current gain cutoff frequency $f_\tau$ of 252 GHz[27] and a record power gain cutoff frequency $f_{max}$ of 820 GHz. Indid, data of $> 1$ THz $f_{max}$ has been obtained, but needs to be confirmed. To demonstrate the viability of this technology as a reasonable scale IC technology, integrated circuits need to be designed and fabricated in this technology.

# Chapter 7

# Integrated Circuits

Applications for HBTs include microwave frequency direct digital synthesis, fiber-optic transmission chip-sets and analog-digital converters. Master-slave flip-flops are critical functional elements in a variety of these digital and microwave systems. The flipflop is a regenerative memory element similar to a latch, with a trigger pulse (clock) to control the change of states. In sequential logic circuits, flipflops are necessary to avoid race conditions and resynchronization. Therefore, the flipflop is a fundamental building block for digital machines. Maximum clock frequencies of master-slave flip-flops are readily determined by configuring the circuit as a 2:1 static frequency divider. These circuits are often used as benchmarks to evaluate the speed of a digital technology [36].

In this chapter, a static frequency divider designed and fabricated in the transferred-substrate HBT process is discussed. The maximum clock frequency is limited by the test set-up. Other key element circuits for fiber-optic communication system, such as selector, demultiplexer (DEMUX), phase-lock-loop (PLL), and voltage-controlled-oscillator (VCO) were also designed and fabricated in the transferred-substrate HBT technology and will also be discussed in this chapter.

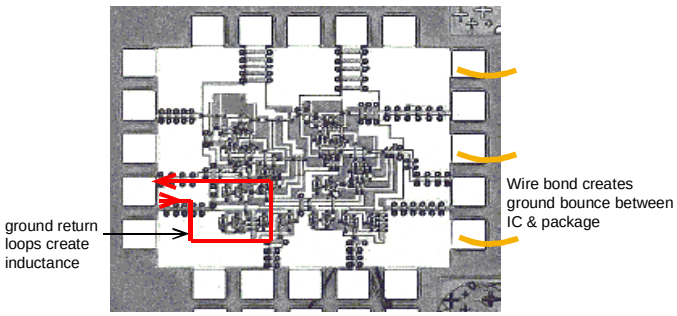
## 7.1 Key Features of the Transferred-substrate IC process

To permit clock rate exceeding 100 GHz, significant issues in transistor design, interconnects, packaging, and thermal design must be addressed. The transistor current gain cutoff frequency $f_\tau$ and power gain cutoff frequency $f_{max}$ must be of the order of several hundred GHz. Devices with 250 GHz $f_\tau$[27] and 820 GHz $f_{max}$[22] have been obtained in the transferred-substrate HBT technology.

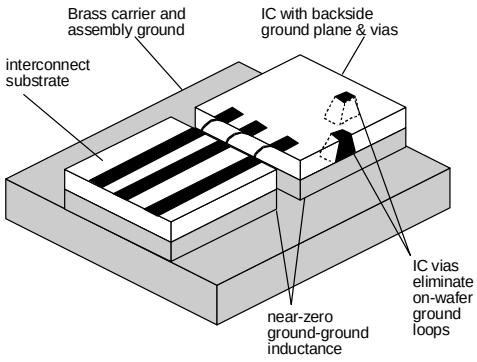
But high transistor bandwidths alone are insufficient for high frequency ICs. Wiring parasitics and delays must be minimized. The interconnects must have small capacitance and inductance per unit length, and the wire lengths. This leads to small transistor-transistor spacings. Given that fast HBTs operate at $\sim 10^5$ A/cm$^2$ current density, efficient heat sinking is then vital. This is provided in the transferred-substrate HBT process by gold electroplated thermal vias. Heat sinking will be improved further by utilizing the plated-copper substrate developed by J. Guthrie.

Even with short interconnects, wiring capacitance is a severe issue (figure 7.1). In the transferred-substrate process, the interconnects are fabricated on BCB with a dielectric constant $\epsilon_r$ of 2.7, much smaller than that of semiconductors ($\epsilon_r \sim 13$). To provide predictable performance, interconnects of more than a few ps length must have controlled characteristics. It is equally important to provide good ground plane. To prevent circuit-circuit interaction through ground-circuit common-lead inductance (" ground loop "), an IC technology that can provide an integral ground plane for ground-return connection is preferred. Similarly, to prevent circuit-circuit interaction between the IC's input and output lines, common-lead inductance between the IC and package ground systems must be made very small. The transferred-substrate IC technology provides a ground connection on the connection on the IC back surface (figure 7.1). IC to package ground inductance is eliminated.

With the high bandwidth transistors, the low parasitics microstrip wiring environment, and copper plated metal substrate, clocked 100 GHz digital ICs should be feasible.




(a)




(b)

Figure 7.1: Wiring in (a) triple-mesa HBT IC technology: ground loops & wire bonds degrade circuit & packaged IC performance, and (b) transferred-substrate HBT technology: microstrip IC wiring to eliminate ground bounce noise and vias & ground plane are provided.

## 7.2 ECL Gate Delay, a Method of Time Constant Analysis (MOTC)

The Master-slave D-flipflop consists of series gated emitter-coupled-logic (ECL) gates whose switching speed depends on a variety of circuit and device parameters including the logic swing, load resistance, peak operating current density, transistor bandwidth, device parasitics and area ratios of the different transistors, etc. An analytic expression is needed to give insight into the dependence of dominant time constants in the propagation delay on the various circuit and device parameters.

ECL is a bipolar logic family that exhibits the shortest propagation delay time of any the commercially available digital ICs. This is accomplished by biasing the transistors so that they do not go into saturation, and thus the time delay required to dissipate excess stored charge in the base is eliminated. These circuits also require the most power to operate.

A basic ECL gate is shown in figure 7.2. Emitter followers at the output provide voltage level shifters, so that the emitter-collector voltage $V_{ce}$ for the switching transistors is in the range of 1.1 V to 1.4 V. The rf performance of HBTs used in the ECL logic peaks for this bias. The emitter followers also produce a low resistance at the input nodes of subsequent stages, which reduces the time constants of these nodes and thus improves the drive capability.

To calculate the time constant of the ECL gate, the equivalent circuit model has to be constructed first and all the active and passive elements of the ECL gates have to be linearized[30], [31]. The non-linear emitter/base diode resistance ($r_D$), a large signal version of $r_e$, and diffusion capacitance ($C_D$) of the HBT are linearized by averaging them over a period of the time during which the transistor is in the process of being turning on/off.

Figure 7.3 shows the equivalent circuit of the ECL gate. The transistor without device parasitics is represented by the hybrid-$\pi$ model (figure 7.3a). The HBT and its parasitics and other circuit elements of the logic gate is shown in figure 7.3b.

The source resistance in figure 7.3, $r_{e5} + r_{ex5}$, represents the effective output resistance from the previous stage assuming a fan-out of one. Since in the switching circuit, when input is at logic 1 (or 0), the output is at logic 0 (or 1), thus the large signal output voltage swing of the logic gate is equal to the input voltage swing, hence, the large signal transconductance

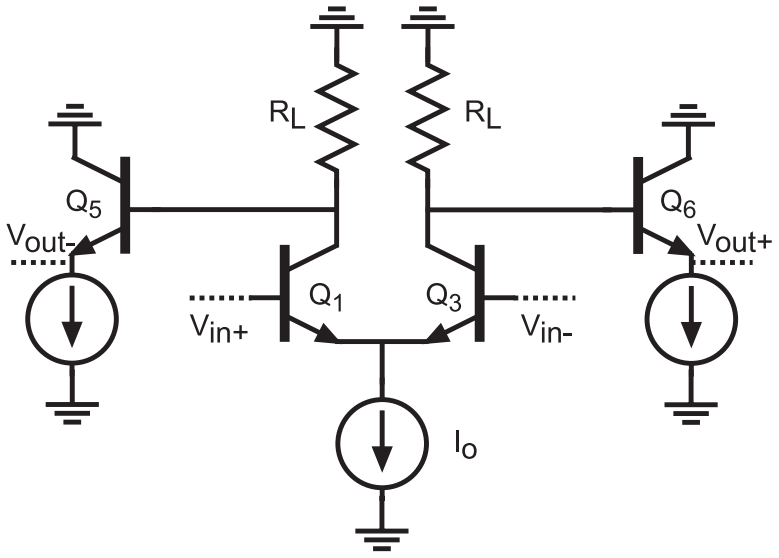



Figure 7.2: Basic ECL gate

of the devices can be linearized as:

$$G_m = \frac{1}{R_L} \ . \tag{7.1}$$

The average diffusion capacitance $C_D$ is the ratio of the charge injected to the base ($I_o \tau_f$) to the change in the voltage across the capacitacne.

$$C_D = \frac{I_o \tau_f}{\Delta V} = \frac{\tau_f}{R_L} \ , \tag{7.2}$$

where $\tau_f$ is the forward transit time of the device. For the fully depleted Shottky collector, it is a good approximation that the base-collector capacitance does not change with transistor bias.

The method of time constant analysis (MOTC) is used to estimate the gate propagation delay $\tau_d$, which is the time from the 50% point in the low-high transition of the input pulse waveform to the 50% point in the high-low transition of the output pulse waveform[33], [32]. If the circuit is assumed can be described by a single time constant $a_1$, the propagation delay time is given by $a_1 \ln(2)$. The MOTC method is performed by calculating the time-constant associated with each capacitor in the network, provided that

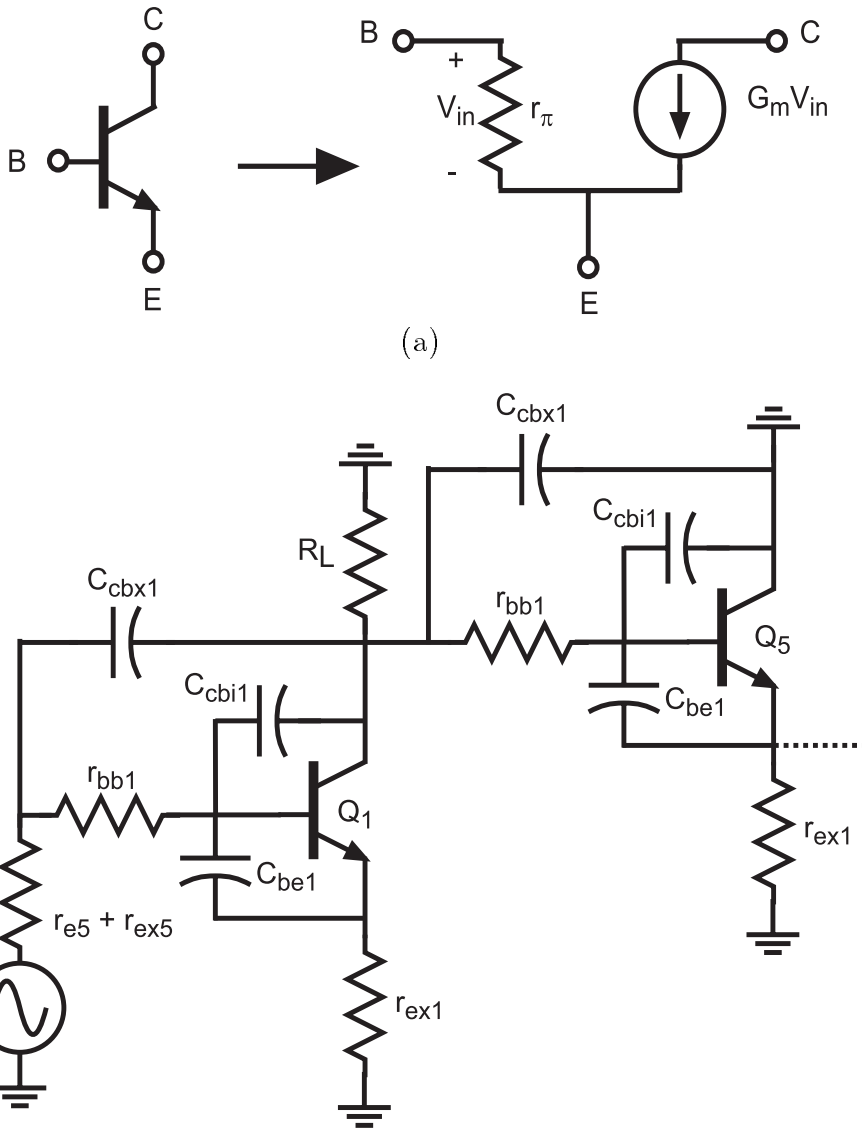



Figure 7.3: (a) Hybrid-$\pi$ model of HBTs without parasitics, (b) ECL equivalent circuit diagram.

all other capacitors have been removed from the circuit. The time-constant of the circuit is the sum of the time constants associated with individual capacitors.

The resulting ECL propagation delay consists of two terms - $\tau_{sw}$ is the delay associated with the switching transistor and $\tau_{ef}$ is the delay associated with the emitter follower.

$$\begin{aligned}\tau_{sw} &= (r_{e5} + r_{ex5} + r_{bb1} + r_{ex1})C_{be1} + [2(r_{e5} + r_{ex5} + r_{bb1}) + R_L]\, C_{cbi1} + \\ &\quad [2(r_{e5} + r_{ex5}) + R_L]\, C_{cbx1}, \end{aligned} \tag{7.3}$$

and

$$\tau_{ef} = r_{e5}C_{be5} + (r_{bb1} + R_L)C_{cbi5} + R_L C_{cbx5}, \tag{7.4}$$

where $\mathrm{C}_{be1} = \mathrm{C}_{je1on} + \mathrm{C}_{D1} = \mathrm{C}_{je1on} + \tau_f/\mathrm{R}_L$ and $\mathrm{C}_{be5} = \mathrm{C}_{je5on} + g_{m5}\tau_f$. The net time constant $\mathrm{a}_1$ of the ECL gate is given by the sum of $\tau_{sw} + \tau_{ef}$. And the ECL gate propagation delay $\tau_d = \mathrm{a}_1 \ln(2)$.

Eq.( 7.3), ( 7.4) can be rearranged to show its dependence on device dimensions. To ease the analysis, $\mathrm{Q}_1$ and $\mathrm{Q}_5$ are assumed to have the same size and be biased at the same current density $\mathrm{J}_e$. All elements's dependence on device dimensions are shown in figure 7.4. Hence, eq. ( 7.3), ( 7.4) can be rewritten as

$$\begin{aligned}\tau_{sw} &= (\frac{V_T}{J_c} + 2r^0_{ex})(C^0_{je} + \frac{\tau_f J_c}{\Delta V}) + \left[2(\frac{V_T}{J_c} + 2r^0_{ex}) + \frac{\Delta V}{J_c}\right] C^0_{cb} + \\ &\quad r^0_{bb}(C^0_{je} + \frac{\tau_f J_c}{\Delta V} + C^0_{cbi})W_e, \end{aligned} \tag{7.5}$$

and

$$\tau_{ef} = \frac{V_T}{J_c}\,(C^0_{je} + \frac{\tau_f J_c}{\Delta V}) + \frac{\Delta V}{J_c}\, C^0_{cb} + r^0_{bb}C^0_{cbi}, \tag{7.6}$$

where $\mathrm{C}^0_{cb} = \mathrm{C}^0_{cbi} + \mathrm{C}^0_{cbx}$.

As is shown in eq. ( 7.5), ( 7.6), at a fixed emitter current density $\mathrm{J}_e$, and a fixed voltage swing $\Delta$V, the delay due to base contact resistance is $\propto \mathrm{W}_e$, hence the associated RC time-constants will decrease as the emitter/collector widths decrease. Therefore, the submicron lateral scaling emitter/collector dimensions does reduce the total ECL gate propagation delay. Also $\tau_d$ can be improved by reducing the forward transit time by vertical scaling the epitaxial layers.

For the ECL designs in this work, the voltage swing $\Delta\mathrm{V} = 360$ mV and $\mathrm{R}_L = 45\ \Omega$. The devices are biased at 1 x $10^5$ A/cm$^2$. To determine the

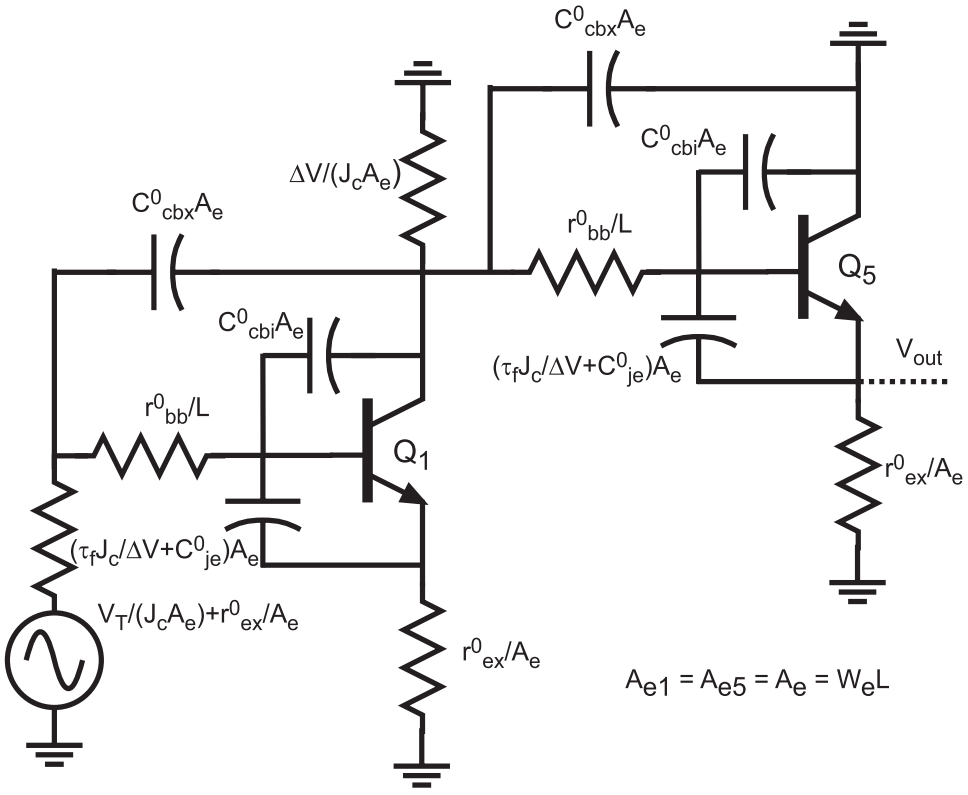



Figure 7.4: ECL equivalent circuit with area dependence indicated.

total gate delay, devices with 1 x 8 $\mu m^2$ emitters and 2 x 12 $\mu m^2$ collectors are used in the following calculations. And the same device sizes are used in $Q_1$ and $Q_5$. The hybrid-$\pi$ parameters for the devices are listed in table 7.1.

| Device parameters | $C_{je,off}$ (fF) | $C_{je,on}$ (fF) | $C_{cbi}$ (fF) | $C_{cbx}$ (fF) | $r_{bb}$ ($\Omega$) | $r_{ex}$ $\Omega$) | $\tau_f$ (ps) |
|---|---|---|---|---|---|---|---|
| 1 x 8 $\mu m^2$ emitter 2 x 12 $\mu m^2$ collector | 20 | 40 | 2 | 6 | 30 | 5 | 0.5 |

Table 7.1: Devices parameters of the transferred-substrate HBTs.

The ECL gate propagation delay $\tau_d$ for the circuit described above is found to be $\sim 2.67$ ps. For the same emitter area, $A_e$, changing the transistors from 1 x 8 $\mu m^2$ to 0.67 x 12 $\mu m^2$ emitters results in a 15 % improvement in the ECL gate propagation delay (from 2.67 ps to 2.27 ps).

Optimum ratio of areas ($A_1/A_5$) for minimum gate delay can be calculated from the time-constant expression if different areas are assumed for the two transistors. This was discussed in [30]. For this work, the two transistors are chosen to have identical sizes for the simplicity of the layout.

## 7.3 ECL Static Frequency Divider: Circuit Design and Layout

Figure 7.5 and 7.6 show the circuit diagram and chip photo of the ECL 2:1 static frequency divider. The divider consists of the circuit core-an ECL master-slave D-flipflop with inverting output connected back to data input, a clock buffer-an emitter follower stage, and an output buffer-an ECL inverter for driving matched 50-$\Omega$ transmission lines.

Current mirrors are used to provide biasing. Emitter degeneration resistors of 40 $\Omega$ are used. The purpose of the emitter resistors is twofold. First, the matching between the reference current and the output current can be greatly improved by the emitter degeneration. Second, the use of emitter degeneration increases the output resistance of the current source. These emitter resistors dissipate considerable amount of heat, hence, thermal vias

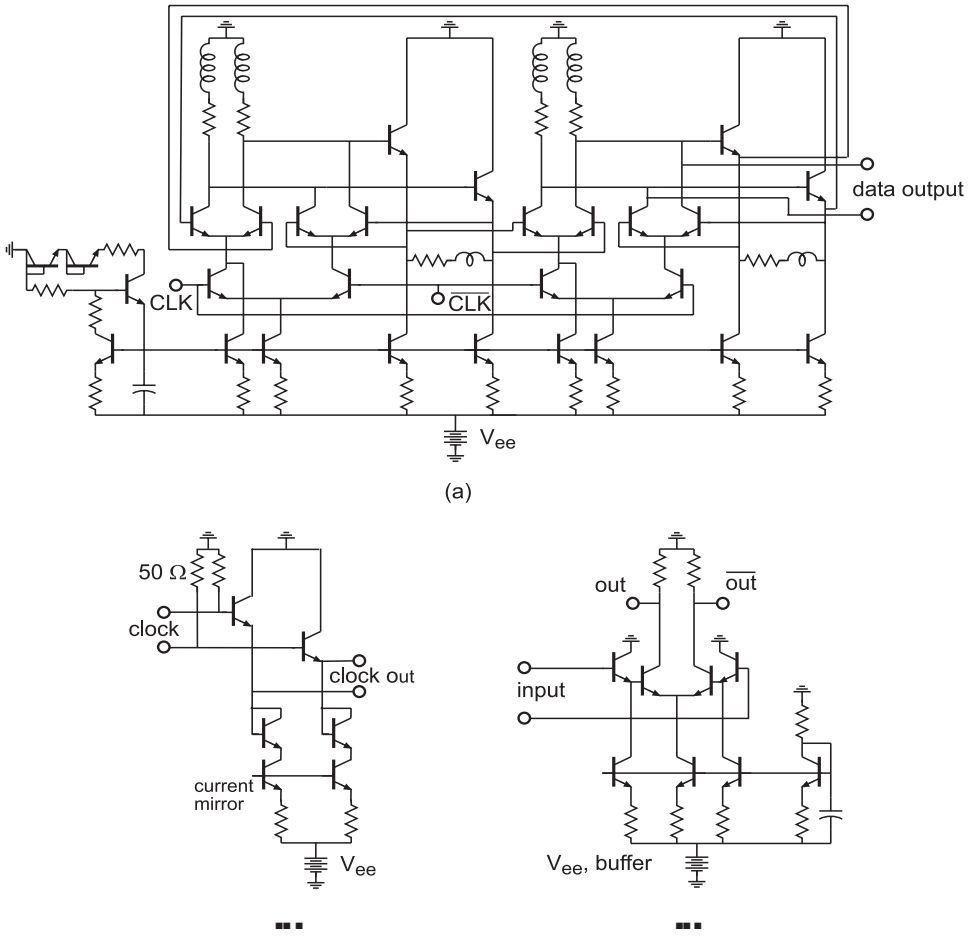



Figure 7.5: Circuit diagram of the ECL 2:1 static frequency divider. (a) Master-slave D-flipflop 2:1 static divider core. (b) Clock buffer. (c) Data output buffer.

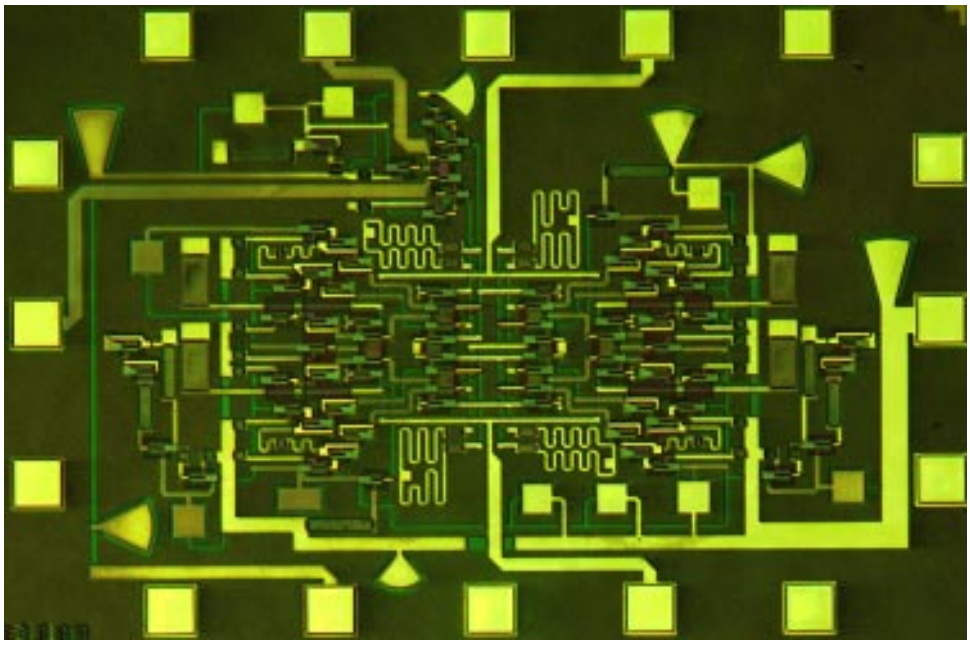


Figure 7.6: IC photograph.

are provided on the degeneration resistors of the current sources. The parasitic capacitance from the via on these resistors does not degrade the overall circuit performance. Bypass capacitors with total capacitance of $\sim$ 1 pF are distributed between the $V_{ee}$ power bus and the bases of the current source transistors. This is to stabilize the voltage between the base and DC power line $V_{ee}$. There are also distributed bypass capacitors between $V_{ee}$ power bus and ground. The bypass capacitors have been designed to have self resonance frequencies much beyond the frequency of interests.

A differential voltage swing of 640 mV and a load resistance $R_L$ of 45 $\Omega$ are chosen. For this $\Delta V$ and $R_L$, the current is 8 mA. For minimum gate delay, it is desirable to operate the transistors at the optimum current density calculated by Pullela[41] from the propagation delay analysis. Kirk effect and breakdown however limit the peak current density to 2 x $10^5$ A/cm$^2$, hence devices with 0.7 x 12 $\mu$m$^2$ emitters and 1.5 x 14 $\mu$m$^2$ collectors are used. A thermal via is provided on each transistor and this introduces a parasitic emitter to ground capacitance of the order of 20 fF. This capacitance arises from the overlap of interconnect metal 1 (M1) to

the ground interconnect metal 2 (M2) through the 5000 Å thick SiN. Hence the model for the HBT used in the SPICE simulations has been modified to an "intrinsic" Spice model (figure 7.7a) plus the parasitic capacitance (figure 7.7b).

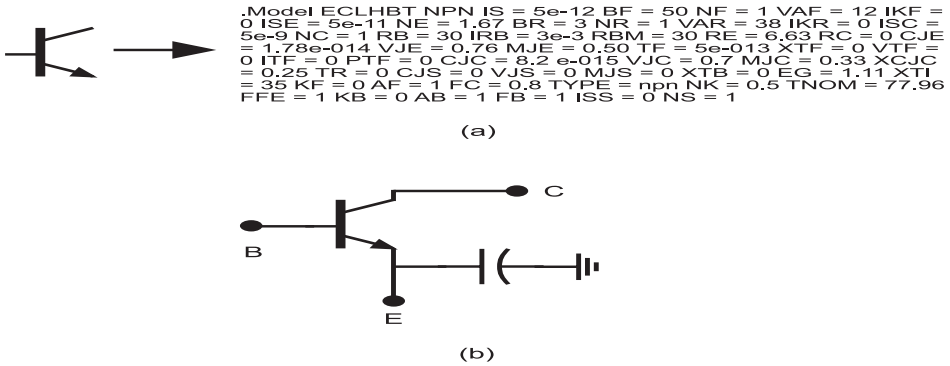



Figure 7.7: (a) Spice model of "intrinsic" HBT.(b)Modified HBT Spice model.

Figure 7.8 shows the key circuit design and layout features. A "keep-alive" current (1/6 of the on-state current) is applied to the input stage of each D-latch. This current keeps the input switching pair weakly biased during the latching phase, reducing the latch-load transition time, and hence the propagation delay. Interconnect delay is a serious issue. The switching signal path is a short, doubly-terminated 90 Ω transmission-line bus, located at the center of the IC. The IC periphery is devoted to biasing current mirrors. The 90 Ω bus termination resistors use a small amount of series inductive peaking. The inductors are implemented with microstrip transmission lines. For a BCB thickness of 5 $\mu$m and a line width of 3 $\mu$m,

$Z_0$ is 98 Ω and the velocity is 117 $\mu$m/ps. A 130-$\mu$m long line of 3 $\mu$m width has an inductance of 0.05 nH. The 90 Ω pull-up resistors do not require the thermal via because the current density is within the current capacity of the NiCr resistors.

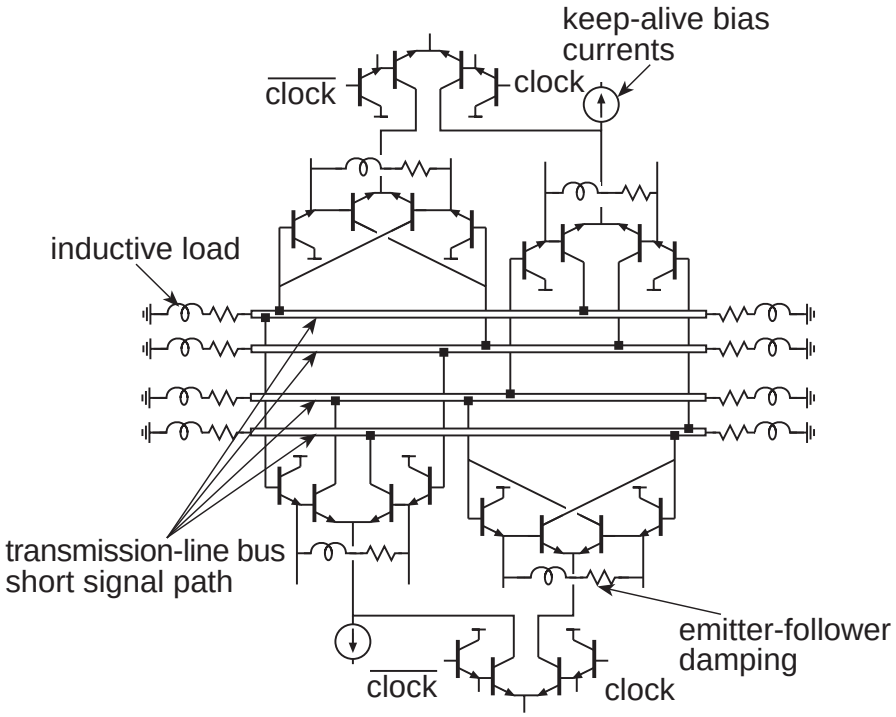



Figure 7.8: Key features of design and physical layout.

Ringing is a inherit problem of the emitter followers. Hence, it has to be carefully considered during circuit design. At the circuit input, the negative real part of the emitter follower's input impedance, together with the input capacitance, and the driving source impedance, can cause severe ringing or oscillation. A series connected resistor and inductor combination between the emitter nodes of the emitter followers provides damping, thus preventing emitter follower ringing.

A dc reference voltage $V_{rf}$ of -1.0 V is applied to one of the two differential clock inputs through a 40 GHz wafer probe with the bias-T. The other differential clock input is driven by a sinusoidal clock signal. The clock signal, first goes to the core circuit through a 50 Ω transmission line,

then splits into two 100 Ω lines, reaches the clock inputs of the two latches symmetrically, then is terminated by 100 Ω resistors. These termination resistors consume a considerable amount of power due to their large resistance and current through them, and so require thermal vias to conduct the heat away from the resistors. The thermal vias will result in significant parasitic capacitance, which is the input capacitance, and hence will degrade the circuit performance. In this design, the problem is improved by increasing the resistor width and using a relatively small thermal via.

The output buffer reduces the effect of the pad and external parasitics on the performance of the critical core circuits. In this design, output buffers are implemented with a differential ECL inverter, providing better match for transmission lines. In future, an output with more than one stage of ECL inverter buffering should give better decoupling.

The Tektronix 40 GHz sampling head provides one of the 50Ω load resistance terminations for the output buffer stage. The second output pad is terminated in a 50Ω load through a 40 GHz wafer probe. The circuit is fabricated with 0.7 $\mu$m x 12 $\mu$m emitter and 1.5 $\mu$m x 14$\mu$m collector HBTs, operating at a current density of 2.0 x $10^5$ A/$cm^2$. The overall chip area is 1.0 x 0.4 mm, and contains 76 transistors.

Simulation (HP-EESOF) predicts a maximum 105 GHz clock frequency (figure 7.14) without the layout parasitics. Given the influence of wiring parasitics on high-speed logic operation, circuits were simulated with all significant interconnects modeled as microstrip transmission lines. Simulations (HP-EESOF) predict a maximum 95 GHz clock frequency (figure 7.9).

## 7.4 ECL Static Frequency Divider Results

The 2:1 divider were tested on-wafer using commercial micro-coaxial probes. One of the two differential clock inputs is terminated in 50 Ω. A 67 GHz micro-coaxial wafer probe connects the second differential clock input pad to a sinusoidal clock signal source through an 18-50 GHz bias tee. The clock input is driven single-ended with a 2-20 GHz synthesizer followed by a 50-75 GHz frequency multiplier. Divide-by-2 operation is observed up to the maximum available clock frequency of 66 GHz using the current test setup (figure 7.10). Figure 5 shows the output waveform of this circuit driven at 66 GHz. The output waveform is small due to the output probe and cable losses. The clock input is small due to the input probe and

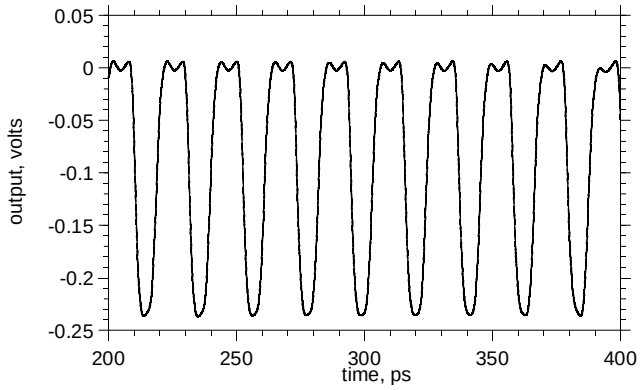



Figure 7.9: Simulated output of ECL divider for 95 GHz clock input.

cable and bias tee losses. The clock input is also driven single-ended with a 2-20 GHz synthesizer to verify the dividers operate correctly at very low clock input frequencies. Divide-by-2 operation is observed at 2 GHz which is the lowest available frequency from this synthesizer. Due to the lack of the power meter for all frequency ranges, and using different frequency multipliers for different frequency ranges, the input clock power level could not be accurately determined.

The flip-flop dissipates 812 mW from a -5V supply, and the output buffer dissipates 38 mW from a -2V supply. Given the peak clock frequency of 95 GHz predicted from SPICE simulation, which takes into account all significant device and interconnect parasitics, we believe that the circuit performance is currently limited by the measurement setup, in particular high frequency losses of the probe, bias tee, and cable connecting to the clock input.

## 7.5 Another ECL Static Frequency Divider Design

Another version of ECL master-slave D-flipflop static frequency divider was also designed. A block diagram of this divider is shown in figure 7.12. The circuit consists of two novel D-latches (ND) which will be discussed next

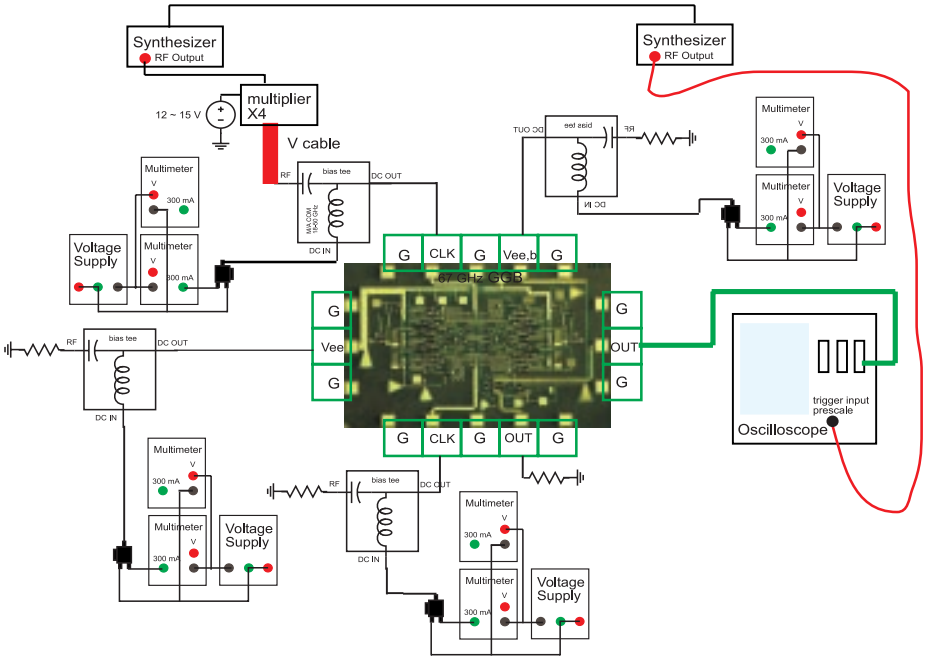



Figure 7.10: Divider test setup.

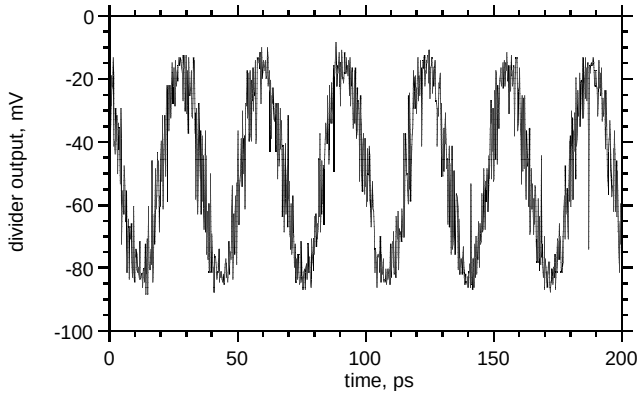



Figure 7.11: 33 GHz output waveform of ECL divider for 66 GHz clock input.

and a conventional D-latch (CD) that was used in the previous design. The novel D-latch is very similar to the conventional latch except an additional switching pair is inserted to between the load stage and the latch stage (figure 7.13). When the clock level is high, the additional switching pair become diodes whose resistance is smaller than the load resistance $R_L$, and hence the loading stage has lower effective resistance leading to a reduced output voltage swing and improved load stage switching time. This reduces the overall propagation delay. When the clock_bar goes high, this pair is off, and has no effect on the circuit. The conventional D-latch is used to restore the logic levels and is outside the feedback loop. Simulation (HP-EESOF) predicts a maximum 140 GHz clock frequency (figure 7.14) without the layout parasitics. At $\sim$ 100 GHz, the previous divider design has shown that the circuit bandwidth was reduced by layout parasitics. Hence, this version of divider has not been laid out due to absence of significant improvement given the presence of layout parasitics.

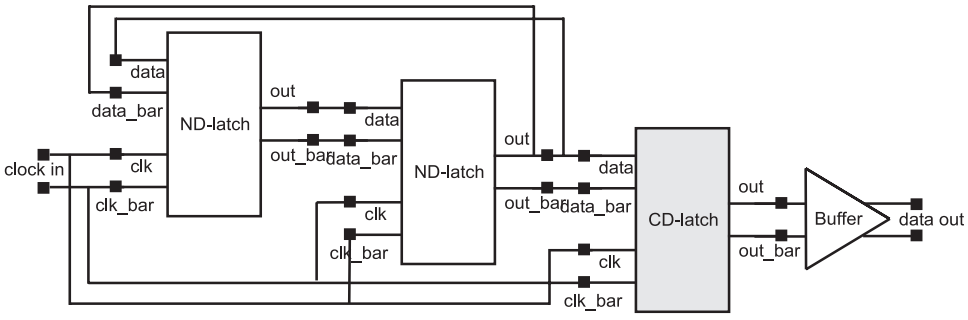



Figure 7.12: Block diagram of novel ECL frequency divider.

## 7.6 Other Circuit Built in Transferred-substrate HBT Technology

Other circuits have also been designed and fabricated to demonstrate the transferred-substrate HBT technology. These includes digital phase-lock-loops (PLLs), W-band voltage-control-oscillators (VCOs), 1:2 demultiplexers (DEMUXs) and selectors. These circuits have not been tested yet.

A block diagram of the digital PLL system is shown in figure 7.15. The elements of the system are a phase detector, a loop filter, and a VCO.

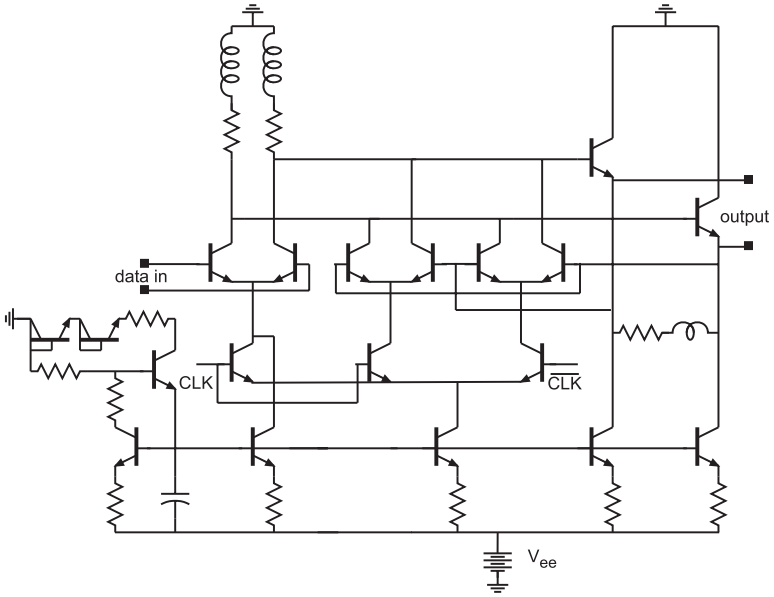



Figure 7.13: Schematic of novel D-latch.

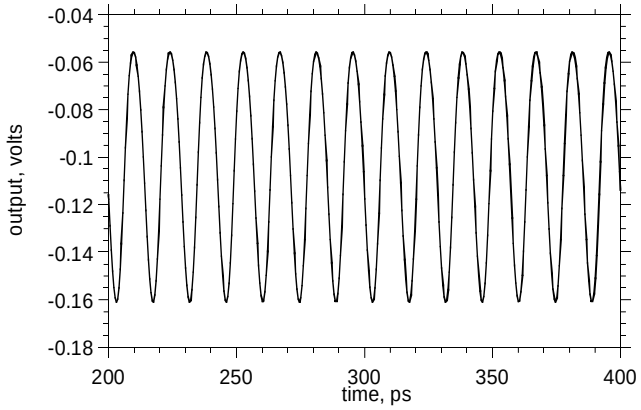



Figure 7.14: Simulated output of the novel ECL divider for 140 GHz clock input.

The phase detector is a master-slave D-flipflop, sampling the output data with frequency $f_{VCO}$ from the VCO at the rising edges of the input data with frequency $f_{in}$. When the loop is locked on an incoming periodic signal ($f_{in}$), the VCO frequency $f_{VCO}$ is exactly equal to $f_{in}$. Figure 7.16 shows the circuit diagram of the loop filter. No design optimization has been done for the best loop performance. The VCO, as shown in figure 7.17, is the emitter-coupled RC multivibrator in which the charging current in the capacitor is varied in response to the control input. The frequency of the oscillator $f = I/(4CV_{be,on})$, where I is controlled by the output of the loop filter. In addition to being controlled by the output of the loop filter, an externally DC voltage tuning is designed, this coarse tuning is designed to increase the loop lock range. This design contains $\sim$ 100 transistors. The chip photo is shown in figure 7.18.

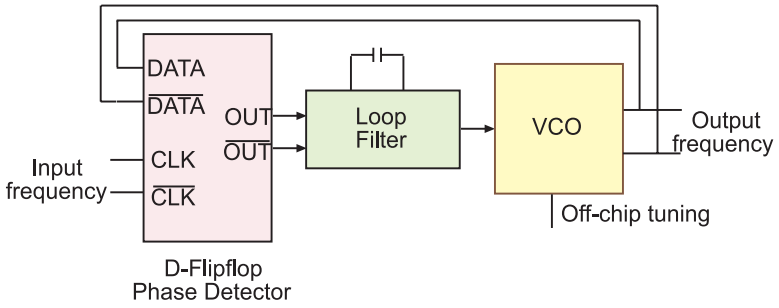



Figure 7.15: Block diagram of digital PLL.

Figure 7.19 shows the chip photos of a W-band VCO, a multiplexer (selector), 1:2 demultiplexer. Transistor count in the DEMUX is up to 120 HBTs.

A digital technology building block with record high clock rate has been demonstrated here. A wide variety of analog ICs in transferred-substrate HBT technology have also been demonstrated[40], [35]. With highly scaled lithographic and epitaxial dimensions, giving both high $f_\tau$ and $f_{max}$, improved interconnect technology, and improved circuit design, 300 GHz analog and 100 GHz digital ICs should be feasible. With improved substrate transfer process and better MBE growth, reasonable large scaled ICs integration should be feasible.

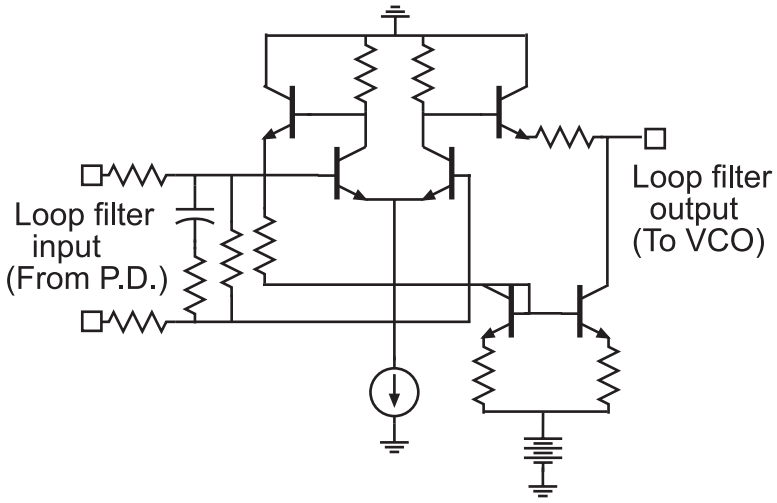



Figure 7.16: Schematic of the loop filter.

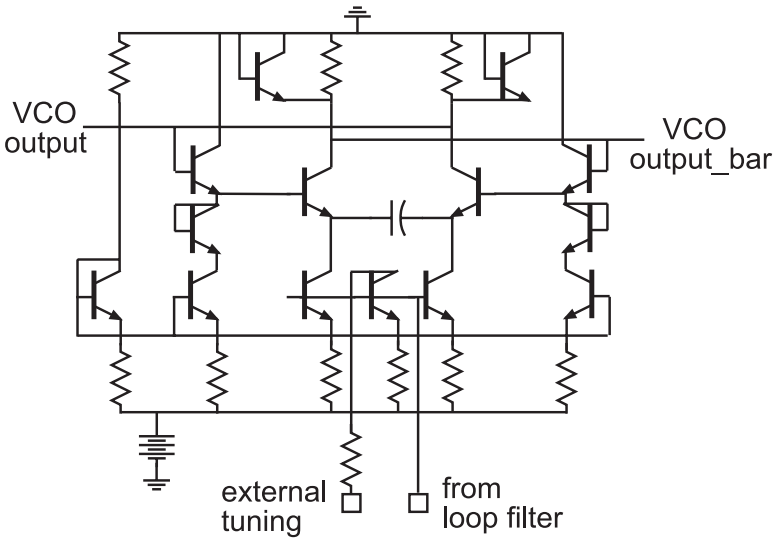



Figure 7.17: Schematic of the VCO.

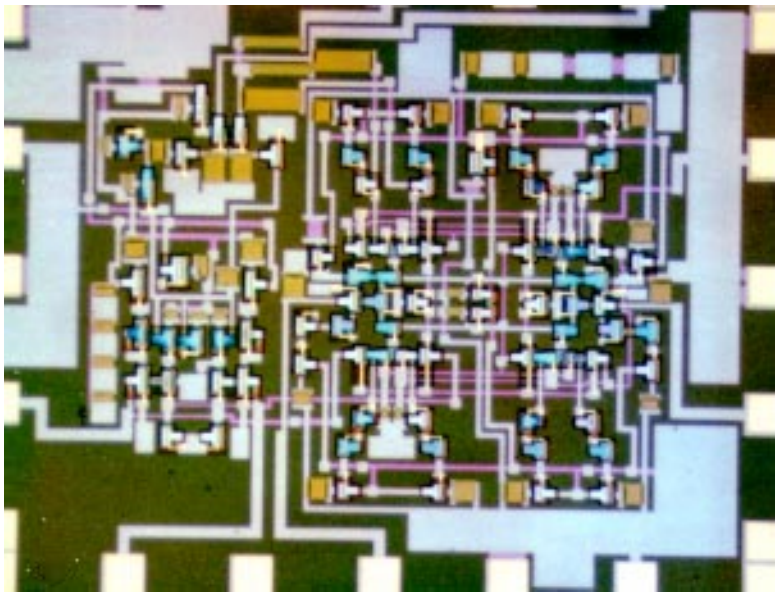


Figure 7.18: Chip photo of a digital PLL.

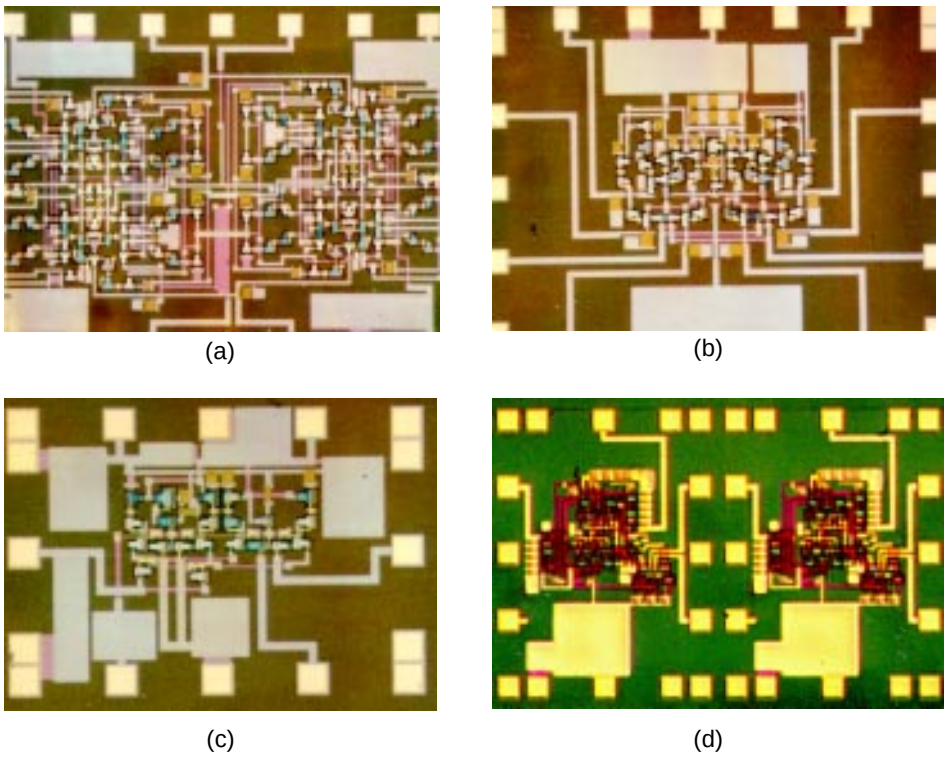



Figure 7.19: Chip photo of (a) W-band VCO, (b) MUX, and (c) 1:2 DE-MUX.

# Chapter 8

# Conclusions

## 8.1 Achievements

Deep submicron InGaAs/AlInAs transferred-substrate HBTs were fabricated. A fabrication process for deep submicron devices was developed. This includes the definition of the deep submicron emitters/collectors, 3-step controlled etch process of submicron emitter mesa, bonding process of the host wafer to the carrier wafer, and emitter/collector alignment. Using substrate-transfer process, HBTs were fabricated with deep submicron emitter/base and collector/base junctions on opposing sides of the base epitaxial layer. The reduced emitter and collector widths progressively reduce $R_{bb}C_{cb}$, hence $f_{max}$ increases drastically.

Transferred-substrate HBTs with ultra-high bandwidth have been demonstrated. Record power gain cutoff frequency $f_{max}$ of 820 GHz has been obtained for HBTs fabricated using e-beam lithography, with 0.4 x 6 $\mu m^2$ emitters and 1.0 x 10 $\mu m^2$ collectors; the current gain cutoff frequency $f_\tau$ is 162 GHz. The high $f_{max}$ results from the scaling of HBT junction widths, from the elimination of collector series resistance through the use of a Schottky collector contact, and from partial screening of the collector-base capacitance by the collector space charge. The large $f_{max}/f_\tau$ ratio allows subsequent thinning the base and collector epitaxial films to improve the current gain cutoff frequency $f_\tau$ at the expense of $f_{max}$, and high values of both $f_\tau$ and $f_{max}$ are thus obtained.

The devices also show encouraging DC characteristics. Devices with 0.2 x 6 $\mu m^2$ emitter and 0.5 x 10 $\mu m^2$ collector exhibit DC current gain $\beta = 24$,

while devices with 0.2 x 6 $\mu m^2$ emitter and 0.7 x 10 $\mu m^2$ collector exhibit DC current gain $\beta = 42$. Devices with small dimensions (0.2 $\mu$ emitter) fabricated in this work showed poor RF characteristics, approximately 400 GHz $f_{max}$. This is due to emitter/collector alignment difficulties, and under-exposure during the collector definition using electron-beam lithography that lead to much narrower collectors than intended.

The effect of the collector space charge on the intrinsic collector-base capacitance $C_{cbi}$ was investigated. It has been observed that the reduction in $C_{cbi}$, hence the improvement in $f_{max}$ through the differential space-charge effect, under combined conditions of high current density and high collector-emitter bias voltage, can be significant for devices with deep submicron emitter and collector.

The devices were characterized using DC-50 GHz and W-band (75-110 GHz) network analyzers. A very reliable calibration procedure is used. The extended reference planes are used to separate the microwave probes to avoid measurement error (in $S_{12}$, hence U) arising from the probe-probe coupling (worse for W-band). The on-wafer Line-reflect-line calibration standards were fabricated and used to de-embed the transistor S-parameters. The 820 GHz $f_{max}$ is reaching the limit of reliability for the 75-110 GHz network analyzer, for RF characterization of devices with higher bandwidth, wider-bandwidth instruments have to be used.

Due to the difficulties with electron-beam exposure during critical dimension definition, especially collector lithography, the yields of devices with deep submicron dimension in this work were low, in the range of 50 %. In other process runs using optical projection lithography, yields above 70 % were obtained for 76-transistor ICs.

Various ICs have been built in the transferred-substrate HBT process. These includes W-band VCOs, DEMUXs, MUXs and PLLs. An integration level of 120 transistors has been achieved. Efficient heat sinking of heat generators (transistors and resistors) provided by this technology has permitted high packing density and, hence shorter wire lengths. Microstrip interconnects fabricated on 5$\mu$m thick BCB provide a low capacitance and low loss wiring environment. The backside ground plane provided by this process, eliminates the IC to package ground inductance and provides effective grounding with very small via inductance.

In the early work [40], [41], the fabrication process used for the ICs employed a Karl Suss contact mask aligner for lithography. This lithography

tool has limitations on fine line capabilities (1 $\mu$m minimum feature size), and on the alignment tolerance. Hence, circuits could not be built using scaled HBTs with higher bandwidth, and "staggering" technique had to be employed to get some circuits and devices aligned, thus wasting wafer area and limiting the scales of integration. And it also causes process failure when hard contact mode is needed for fine line-width lithography. The problems are solved by using the 0.5 $\mu$m resolution GCA projection lithography system (stepper). It is a non-contact high resolution (0.5 $\mu$m) lithography tool with small alignment tolerance. This allows the rapid increase in the scales of integration. The fabrication process using stepper has been developed.

For HBTs fabricated using the optical-projection lithography, with identical MBE material (400Å InGaAs base with 50 meV grading, 3000 Å collector thickness), an $f_{max}$ of 805 GHz has been achieved in devices with 0.4 x 6 $\mu m^2$ emitters and 1.0 x 10 $\mu m^2$ collectors; the $f_\tau$ is 147 GHz. Emitter coupled logic 2:1 static frequency dividers were designed and fabricated using the stepper in the transferred-substrate HBT technology. The circuit consists of 76 transistors. A record 66 GHz divide by 2 operation is observed. Given the peak clock frequency of 95 GHz predicted from SPICE simulation, which takes into account all significant device and interconnect parasitics, it is clear that the circuit performance is currently limited by the test setup. With higher frequency instrumentation, improved circuit layout, and low parasitics interconnects, clocked 100 GHz digital ICs should be feasible.

## 8.2 Future Work

It is shown in this work that the bandwidth of transferred-substrate HBTs improves significantly by deep submicron lateral scaling. The primary requirement for further deep submicron scaling is the need for a powerful lithography tool for precise high resolution reproducible emitter/collector definition and precise emitter/collector alignment, a reliable high resolution emitter mesa formation process, and a wider bandwidth network analyzer avaliable for RF measurements.

Another issue with deep submicron scaling which needs to be addressed is emitter resistance $r_{ex}$. In current HBT dimensions, the emitter resistance $r_{ex}$ does not appear to be very important for the transistor $f_{max}$, but has

serious impact on $f_\tau$ as the collector is thinned below 3000 $\mathring{A}$. As the transistor lateral dimension decrease, $r_{ex}$ may soon become a limiting factor. Emitter resistance reduces the current cutoff frequency $f_\tau$ due to $r_{ex}C_{cb}$ time constant, degrades differential voltage gain at switching point of the differential pair, reduces noise margin, speed, and voltage swing. $r_{ex}$ has to be improved in deep submicron transferred-substrate HBT technology. InAs emitter Ohmic contact layers could be employed for this purpose, and the contact must be protected during the etch used for emitter mesa formation.

Maintaining DC current gain $\beta$ is also an important issue in deep submicron scaling. Lower electron transit time is desired. Thinner base and higher base bandgap grading are necessary.

Devices should be laid out with short stripe lengths. This relaxes the emitter/collector alignment precision comparing with those of longer stripes. Also the shorter device can be biased at much higher current density than longer devices, this leads to, higher bandwidth, faster gate delay, etc. As the emitter/collector widths scale, the base mesa width has to be scaled accordingly to the limit of the transfer length. This extrinsic emitter-base capacitance must be minimized.

The breakdown voltage at high current density has to be improved. From the digital circuit point of view, higher breakdown will permit multiple emitter followers in ECL gates (like $E^2CL$ in SiGe). Therefore, the switching transistor can be biased at much higher $V_{cb}$, hence suppressing the base push-out and thereby delaying the on-set current of the Kirk effect. A larger current density results in larger $C_{cbi}$ reduction, and reduced gate propagation delay. The higher breakdown will also allow more circuit design freedom for more complex digital circuits which involves multiple circuit stages. The InP collector can be employed to improve the transistor breakdown. Substrate removal process has to be developed for the InP collectors.

The ECL gate propagation delay analysis shows that to improve the gate propagation delay, $\tau_f$, $r_{bb}$, and $C_{cb}r_{ex}$ time-constant have to be reduced. Transferred-substrate technology provides the advantage of thinning the base and collector epitaxial films to reduce $\tau_f$, hence increase $f_\tau$ without excessive sacrifices in $C_{cb}r_{ex}$ time-constant and $f_{max}$. The aggressive lateral scaling of lithographic dimensions accompanied by vertical scaling of the epitaxial layers will offer both very high $f_\tau$ and $f_{max}$ to meet 100 GHz circuit

requirement.

It is important to reduce base resistance because it directly affects transistor bandwidth and digital gate propagation delays. Using a $CBr_4$ doping source, $> 10^{20}/cm^3$ carbon base doping is feasible, improving by 3:1 both the base sheet and base contact resistance. This will allow to further thinning the base and collector epitaxial films to reduce $\tau_f$, and hence to improve $f_\tau$ without excessive sacrifices in $r_{bb}$ and $r_{bb}C_{cb}$ time-constants. As the diffusion coefficient of carbon is orders of magnitude less than that of beryllium, greater control of the base doping profile, hence the actual base thickness can be obtained. The extrinsic base regions can also be regrown with highly-doped wide bandgap material graded to a low-bandgap material for metal contact. The wide-bandgap material will improve electron confinement in the base thus increasing the current gain and the heavily doping will reduce the base resistance. With improved alignment, 0.1 $\mu$m emitter and collector dimensions should be feasible. These enhancements should results in a transistor with 500 GHz $f_\tau$ and 2-3 THz $f_{max}$.

At 100 GHz, the circuit performance is also limited by the wiring parasitics. Circuit layout has to be very carefully done. New techniques for clock distribution and power bus distribution have to be developed. Optimum partitioning of a high speed circuit may depend on thermal and crosstalk consideration. The layout is preferred to be done with high symmetry if possible. The critical signal paths have to be kept short. And accurate line modeling is a must. The cross-over between the critical signal paths have to be minimized. The load resistance $R_L$ and the impedance of the transmission lines $Z_0$ should be selected and laid out so that reflections are eliminated. Input and output buffer designs are essential to reduce the effect of the pad and external parasitics on the performance of core circuits.

In summary, HBTs and digital integrated circuits with record performance have been fabricated in the transferred-substrate HBT technology. Using substrate transfer processes, HBTs of high values of both $f_\tau$ ($> 500$ GHz) and $f_{max}$ ($> 1000$ GHz) can be obtained by highly scaled lithographic and epitaxial dimensions. With further scaling and improved circuit design, 100 GHZ digital ICs should be feasible.

# Appendix A

# Process Flow

## A.1 Focus check with 2" Si wafer

### A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be $> 17$ MΩ.
2. Set spinner for 4 krpm for 2 minutes.
3. Get 2" Si wafer from drybox (in old toluene petri dish)
4. Start wafer spinning, then squirt with acetone.
5. Don't let it dry, squirt with ISO, then ACE and ISO again.
6. Put on 200°C hot plate for 5 minutes.

### B Photoresist Application and Exposure

1. Cool down after dehydration, 5 min
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply SPR 950-0.8 with syringe and filter to cover wafer
4. Spin at 2.5 krpm for 30 sec
5. Soft Bake, 90°C, 1 min. on hot plate
6. Apply CEM with syringe and filter to cover wafer
7. Spin at 4 krpm for 30 sec
8. Use "Smartset Array" mask plate, run job as follows: "FOCUS SFOC2\FOC", note down the best focus number returned by computer.

### Align emitters perpendicular to the major flat of the wafer

## A.2 Emitter Contacts (Mask Layer 1)

### A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be $> 17$ MΩ.
2. Cold ACE 5 min.
3. Hot METH 5 min.
4. Hot ISO 5 min.
5. Running DI 5 min.
6. Blow dry with N2
7. Dehydration bake, 120°C, 30 min in petri dish without cover

### B Photoresist Application and Exposure

1. Cool down after dehydration, 5 min
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply SPR 950-0.8 with syringe and filter to cover wafer
4. Spin at 2.5 krpm for 30 sec
5. Soft Bake, 90°C, 1 min. on hot plate
6. Apply CEM with syringe and filter to cover wafer
7. Spin at 4 krpm for 30 sec
8. Expose for 2.4 seconds, set focus to Si wafer focus + 40 - system focus.

### C Development

1. Post Bake, 100°C, 2 min, 10 sec
2. Rinse in running D.I., 30 sec.
3. Develop in MF-701 for 2 min, 20 sec
4. Rinse in running D.I., 3 min

### D Oxygen Plasma Descum of Photoresist

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

### E Evaporation

1. Mix a dilute solution of HCl : H2O :: 1 : 10

2. Dip in dilute HCl for 15 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer on E-Beam mount. Level it.
6. Put in a new crystal. A new crystal should always be used for emitters.
7. Pump down to below 1 x 10-6 torr
8. Deposit material:

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Ti | 200 | 1-2 | 1.65 |
| Pt | 500 | 1 | 1.85 |
| Au | 8000 | 15 | 1.5 |
| Si | 500 | 2-3 | 1.6 |

(use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting)

**F Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–**

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle)
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope, then Dektak thickness of metal.

### A.3 Base Contact etch (no mask required)

**A Oxygen Plasma Descum**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

**B Surface Prep**

1. Mix a dilute solution of NH4OH : H2O :: 1 : 10
2. Dip in dilute NH4OH for 10 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2.

**C Dry Etch**

1. Clean both chucks and shield with ISO. Turn laser on now.
2. O2 plasma clean (20sccm @ 125 mT, 500V bias for 20 min)
3. Precoat chamber (M/H/A 4/20/10 sccm @ 125 mT, 300V bias for 20 min)
4. Load wafer and align laser monitor, then pump down to low E-6 torr.
5. Etch (M/H/A 4/20/10 sccm @ 75 mT, 500V bias) until slope changes.
6. Increase pressure to 110mT. Etch until desired stop point reached.
7. Remove polymer (O2 50 sccm @ 125 mT, 200V bias for a quarter of etch time).
8. Vent chamber and remove sample.

**D Si removal**

1. 300mT of CF4
2. power = 100W at low frequency.
3. run for 1 minute per 500A Si.
4. Check that Si has been removed with optical microscope.
5. Remove samples, clean chamber for 10 minutes with O2 (300W, 300mT)
6. Replace samples and do standard descum (O2 @ 100W, 300mT for 15 sec)

**E Selective etch**

1. Mix a dilute solution of NH4OH : H2O :: 1 : 10
2. Dip in dilute NH4OH for 10 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2.
5. Mix Solution B - HCL:H20 :: 4:1 in HCL beaker (plastic) with Soln B.
6. Mix Solution A - HBr:glacial acetic :: 1:1 in Soln A beaker with stirrer bar. Mix well.
7. Mix Solution A & B 1:1 by adding Soln B then Soln A to A+B beaker. Mix well
8. Put the A+B beaker in the ice, wait till 10°C.
9. NO stirring, etch for 22 seconds (in water after 22 seconds).
10. Rinse in DI for 3 min.
11. Blow dry with N2.

**F Nonselective etch**

1. Mix etchant as follows: 55ml of 1M citric acid in 220ml DI. Mix well. Add 5ml peroxide. Mix well. Add 1ml phosphoric acid. Mix well.
2. Stirring at 200 rpm etch for 25 seconds by suspending the wafer in a basket.
3. Rinse in DI for 3 min.
4. Blow dry with N2.

## A.4 Base Contact (Mask Layer 2)

**A Dehydration bake, 120°C, 30 min. in petri dish without cover**

**B Photoresist Application and Exposure**

1. Cool down after dehydration, 5 min.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply EIR 5214 with syringe and filter to cover wafer
4. Spin at 6 krpm for 30 sec.
5. Hot Plate Bake, 95°C, 1 min.
6. Expose for 0.32 sec., focus of 24 - system focus

7. Hot Plate Bake, 105°C, 1min.
8. Flood Expose at 7.5 mW/cm2 for 30 sec.

**C Development**

1. AZ 400K : DI :: 1:5.5.
2. Develop for 40 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

**D Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

**E Evaporation**

1. Mix a dilute solution of HCl : H2O :: 1 : 10
2. Dip in dilute HCl for 15 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer on E-Beam mount. Level it.
6. Put in a new crystal. A new crystal should always be used for emitters.
7. Pump down to below 1 x 10-6 torr
8. Deposit material:

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Ti | 200 | 1-2 | 1.65 |
| Pt | 500 | 1 | 1.85 |
| Au | 800 | 15 | 1.5 |

**F Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–**

1. Soak wafer in beaker of ACE until metal comes loose.

2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle)
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope, then Dektak thickness of metal.

**G RTA for 60 seconds at 300°C. Run a test program first.**

## A.5 Isolation (Mask Layer 3)

### A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be ¿ 17MW.
2. Cold ACE 3 min.
3. Hot METH 3 min.
4. Hot ISO 3 min.
5. Running DI 3 min.
6. Blow dry with N2
7. Dehydration bake, 120°C, 30 min. in petri dish without cover

### B Photoresist Application and Exposure

1. Cool down after dehydration, 5 min.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply SPR 518-A with syringe and filter to cover wafer
4. Spin at 4.0 krpm for 30 sec.
5. Hot Plate Bake, 90°C, 1 minute
6. Expose for 0.8 sec, focus of 20 - system focus
7. Hot Plate Bake, 110°C, 1 minute

### C Development

1. Develop in full beaker of MF-701 for 1 min, 30 seconds

2. Rinse in running DI water for 3 min.
3. Blow dry with N2.
4. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

**D Oxygen Plasma Descum of Photoresist and Hardbake.**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 20 seconds.
4. Hardbake photoresist at 120C for 20 min.

**E Isolation Etch**

1. Load Si wafer to be used in RIE #5
2. Run LeeGAN or GaNCLN
3. Set up laser monitor, try to center laser on Si wafer
4. Etch conditions:
   (a) Cl2 flow rate = 20.0 sccm
   (b) chamber pressure = 5.0 mTorr
   (c) P=150W (this is controlled)
   (d) Voltage should be 150-175 V
5. Etch until 30 seconds after slope change. (6 min., 30 sec. For 3 kA collector).

**F Resist strip**

1. Remove photoresist with acetone in liftoff beaker for 3 minutes.
2. Rinse by spraying with METH and ISO.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.

**G Oxygen Plasma Photoresist Removal (optional, at your discretion)**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 30 seconds.

4. examine under microscope to ensure photoresist removal.

**H Characterization of process so far.**

1. Dektak etch depth, measure TLMs.

## A.6 Poly Planarize (Mask Layer 4)

### A Solvent Cleaning

1. Get Poly out of refrigerator, warm up!!
2. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
3. Cold ACE 5 min.
4. Hot METH 5 min.
5. Hot ISO 5 min.
6. Running DI 5 min.
7. Blow dry with N2
8. Dehydration bake, 120°C, 30 min. in petri dish without cover

### B Poly Spin & Cure

1. Mix adhesion promoter in designated beaker (1 mL of VM-651 from bottle using plastic dropper, 200 mL of D.I.). Stir then get new dropper.
2. Wafer on spinner chuck with vacuum, blow with N2.
3. Apply adhesion promoter to cover wafer.
4. Let it sit on the wafer for 20 seconds.
5. Spin at 3.0 krpm for 60 sec.
6. Hot plate bake, 125°C, 3 minutes.
7. Apply DuPont Ployimide to cover wafer with syringe and 1 um filter.
8. Let sit on wafer for 20 seconds.
9. Spin at 2.5 krpm for 30 sec (to give 1.8um film).
10. Hard bake polyimide in programmable oven as follows in petri dish without cover, and with the base of the petri dish covered with aluminum foil.
    (a) hold at 90°C for 60 min.

(b) ramp at 4°C per min. to 150°C.
(c) hold at 150°C for 60 min.
(d) ramp at 4°C per min. to 230°C.
(e) hold at 230°C for 60 min.
(f) ramp at 4°C per min. to 170°C.

**C Photoresist Application and Exposure**

1. Remove from oven when below 90°C.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply AZ 4330 with syringe and filter to cover wafer
4. Spin at 5.0 krpm for 30 sec.
5. Soft Bake, 90°C, 30 min. in petri dish without cover
6. Hard Bake, 120°C, 30 min. in petri dish without cover

**D Polyimide Etchback**

1. Load RIE#1 according to instructions
2. Pump down to low E-6.
3. Set up laser monitor
   (a) Look for diffraction pattern to identify beam. Laser signal should be about 500mV. Use outermost spot of laser beam.
   (b) Set up chart recorder for 1 hour and ~700mV.
4. Etch conditions:
   (a) O2 flow rate 7.0 sccm.
   (b) chamber pressure = 10 mTorr
   (c) P=60W (control this watching Heathkit)
   (d) Voltage should be around 350 V
5. Etch for 18 cycles.

**E Check**

1. Put in SEM and look at 1um emitter fingers to see if they are clear.
2. If not, etch two minutes in PEII-A at 100W, 300 mT then SEM again.

**F Clean Up** Remove mung from backside with ISO soaked Q-tip

**G Photoresist Application and Exposure**

1. Wafer on spinner chuck with vacuum, blow with N2
2. Apply SPR 518-A with syringe and filter to cover wafer
3. Spin at 3.0 krpm for 30 sec.
4. Hot Plate Bake, 90°C, 1 minute
5. Expose for 1.1 sec, focus of 12 - system focus. Must use global alignment.
6. Hot Plate Bake, 110°C, 1 minute

**H Development**

1. Develop in MF-701 for 1 min, 30 seconds
2. Rinse in running D.I. for 3 minutes
3. Flood Expose at 7.5 mW/cm2 for 2 minutes.
4. Hard Bake, 120°C, 30 min. in petri dish without cover

**I Etch Poly** Poly etch for 30 minutes, PEII-A, 300 mT O2, 100 W

**J Resist strip**

1. Remove resist in MF-701, 2 minutes.
2. Rinse in running D.I. for 3 minutes
3. Blow dry with N2.
4. Inspect under microscope.

**K Reflow Bake** Hot plate bake, 250°C, 10 minutes to reflow polyimide and complete the cure.

### A.7 NiCr Resistors (Mask Layer 5)

**A Solvent Cleaning**

1. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
2. Cold ACE 5 min.
3. Hot METH 5 min.
4. Hot ISO 5 min.
5. Running DI 5 min.
6. Blow dry with N2
7. Dehydration bake, 120°C, 30 min. in petri dish without cover

## B Photoresist Application and Exposure

1. Cool down after dehydration, 5 min.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply EIR 5214 with syringe and filter to cover wafer
4. Spin at 6 krpm for 30 sec.
5. Hot Plate Bake, 95°C, 1 min.
6. Expose for 0.32 sec, focus of 18 - system focus.
7. Hot Plate Bake, 105°C, 1 min.
8. Flood Expose at 7.5 mW/cm2 for 30 sec.

## C Development

1. AZ 400K : DI :: 1:5.5.
2. Develop for 40 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

## D Oxygen Plasma Descum of Photoresist

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

## E Evaporation

1. Mix a dilute solution of HCl : H2O :: 1 : 10
2. Dip in dilute HCl for 15 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer on E-Beam mount. Level it.
6. Put in a new crystal. A new crystal should always be used for emitters.
7. Pump down to below 1 x 10-6 torr
8. Deposit material:

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Si | 200 | 2-3 | 1.65 |
| NiCr | 475 | 1 | 1.75 |

**F Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–**

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle)
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope, then Dektak thickness of metal.

## A.8 Pad Metal (Mask Layer 6)

**A Solvent Cleaning**

1. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
2. Cold ACE 5 min.
3. Hot METH 5 min.
4. Hot ISO 5 min.
5. Running DI 5 min.
6. Blow dry with N2
7. Dehydration bake, 120°C, 30 min. in petri dish without cover

**B Photoresist Application and Exposure**

1. Cool down after dehydration, 5 min.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply EIR 5214 with syringe and filter to cover wafer
4. Spin at 4 krpm for 30 sec.

5. Hot Plate Bake, 95°C, 1 min.
6. Expose for 0.42 sec, focus of 18 - system focus.
7. Hot Plate Bake, 105°C, 1 min.
8. Flood Expose at 7.5 mW/cm2 for 30 sec.

**C Development**

1. AZ 400K : DI :: 1:5.5.
2. Develop for 55 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

**D Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

**E Evaporation**

1. Mix a dilute solution of HCl : H2O :: 1 : 10
2. Dip in dilute HCl for 15 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer on E-Beam mount for angle of about 30 and rotation.
6. Put in a new crystal.
7. Pump down to below 1 x 10-6 torr
8. Deposit material:

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Ti | 200 | 2-3 | 1.65 |
| Au | 9500 | 15 | 1.5 |
| Ti | 100 | 2-3 | 1.65 |

### F Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle)
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope, then Dektak thickness of metal.

## A.9 SiN Etch (Mask Layer 7)

### A Solvent Cleaning

1. Wipe lower electrode, housing of PECVD with ISO soaked wipes. Careful, HOT!
2. Run 60CLNSiN.
3. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
4. Cold ACE 3 min.
5. Hot METH 3 min.
6. Hot ISO 3 min.
7. Running DI 3 min.
8. Blow dry with N2

### B SiN Deposition, PR application

1. Load wafer in PECVD, run SiN30. Remember orientation.
2. Unload, rinse with ISO beaker with ISO (of course) for 1 minute.
3. Load wafer in PECVD, rotate $90^\circ$ from previous orientation, run SiN20.
4. Unload, let wafer cool for 5 minutes.
5. Wafer on spinner chuck with vacuum, blow with N2
6. Apply SPR 518-A with syringe and filter to cover wafer

7. Spin at 4 krpm for 30 sec.
8. Hot Plate Bake, 90°C, 1 min.
9. Expose for 0.9 sec, focus of 20 - system focus.
10. Hot Plate Bake, 110°C, 1 min.

**C Development**

1. Develop in full beaker of MF-701 for 1 min. 30 seconds
2. Rinse in running DI water for 3 min.
3. Blow dry with N2.
4. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

**D Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 20 seconds
4. Hardbake photoresist at 120°C for 20 min.

**E SF6, O2, Ar RIE3**

1. Clean system with ISO and clean wipes.
2. O2 clean of system as follows:
   (a) O2 flow rate = 20.0 sccm
   (b) chamber pressure = 10.0 mTorr
   (c) Voltage=500 V
   (d) Minimize reflected power by tuning
3. Load sample, pump down to at least 1 x 10-5 torr.
4. Etch conditions:
   (a) SF6,O2,Ar flow rate = 5.0, 3.0, 10.0 sccm
   (b) chamber pressure = 20.0 mTorr
   (c) Voltage=250 V
   (d) Minimize reflected power by tuning
   (e) Etch for 5 minutes
5. Look under microscope. Etch in 1 min. increments if necessary.

### F Resist strip

1. Remove photoresist with acetone in liftoff beaker for 3 minutes.
2. Rinse by spraying with METH and ISO.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.

### G Oxygen Plasma Photoresist Removal (optional, at your discretion)

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 30 seconds.
4. examine under microscope to ensure photoresist removal.

## A.10 Metal 2 (Mask Layer 8)

### A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
2. Cold ACE 5 min.
3. Hot METH 5 min.
4. Hot ISO 5 min.
5. Running DI 5 min.
6. Blow dry with N2
7. Dehydration bake, 120°C, 30 min. in petri dish without cover

### B Photoresist Application and Exposure

1. Cool down after dehydration, 5 min.
2. Wafer on spinner chuck with vacuum, blow with N2
3. Apply EIR 5214 with syringe and filter to cover wafer
4. Spin at 4 krpm for 30 sec.
5. Hot Plate Bake, 95°C, 1 min.
6. Expose for 0.42 sec, focus of 18 - system focus.
7. Hot Plate Bake, 105°C, 1 min.
8. Flood Expose at 7.5 mW/cm2 for 30 sec.

**C Development**

1. AZ 400K : DI :: 1:5.5.
2. Develop for 55 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

**D Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

**E Evaporation**

1. Mix a dilute solution of HCl : H2O :: 1 : 10
2. Dip in dilute HCl for 15 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer on E-Beam mount for angle of about 30 and rotation.
6. Put in a new crystal.
7. Pump down to below 1 x 10-6 torr
8. Deposit material:

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Ti | 200 | 2-3 | 1.65 |
| Au | 9500 | 15 | 1.5 |
| Ti | 100 | 2-3 | 1.65 |

**F Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–**

1. Soak wafer in beaker of ACE until metal comes loose.
2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.

3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle)
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope, then Dektak thickness of metal.

## A.11 BCB (Mask Layer 9)

### A Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be $> 17M\Omega$.
2. Cold ACE 3 min.
3. Hot METH 3 min.
4. Hot ISO 3 min.
5. Running DI 3 min.
6. Blow dry with N2
7. Dehydration bake, 120°C, 30 min. in petri dish without cover

### B BCB Spin & Cure

1. Turn N2 flow up to maximum (100 scfh) in BlueM oven.
2. Wafer on spinner chuck with vacuum, blow with N2.
3. Apply adhesion promoter AP-8000 with dropper to cover wafer.
4. Spin at 4.0 krpm for 30 sec.
5. Blow dry with N2.
6. Set spinner for 3000 RPM.
7. Apply BCB 57, spin at 3.0 krpm for 30 sec,.
8. Cure BCB in BlueM oven (Prog 2) in petri dish without cover, and with the base of the petri dish covered with aluminum foil.

### C Photoresist Application and Exposure

1. Remove from oven when below 90°C.

2. Cool down after dehydration, 5 min.
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply EIR 5214 with syringe and filter to cover wafer
5. Spin at 6 krpm for 30 sec.
6. Hot Plate Bake, 95°C, 1 min.
7. Expose for 0.32 sec, focus of 18 - system focus.
8. Hot Plate Bake, 105°C, 1 min.
9. Flood Expose at 7.5 mW/cm2 for 30 sec.

**D Development**

1. AZ 400K : DI :: 1:5.5.
2. Develop for 44 sec.
3. Rinse in running DI water for 3 min.
4. Blow dry with N2.
5. Observe under microscope. If there is a suspicion that some photoresist is remaining may go back into developer for 5 - 10 secs longer.

**E Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

**F Evaporation**

1. Place wafer on E-Beam mount.
2. Put in a new crystal in the crystal monitor if reading > 10.
3. Pump down to below 1 x 10-6 torr
4. Deposit material:

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Ni | 100 | 1.5 | 1.5 |

**G Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–**

1. Soak wafer in beaker of ACE until metal comes loose.

2. Prop wafer up in beaker and squirt the whole wafer REAL HARD with acetone. Do this for 10 minutes or so, occasionally dunking the wafer back into the beaker of acetone.
3. ACE squirt bottle (a final rinse).
4. Rinse with METH then ISO (squirt bottle).
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope.

**H BCB etch**

1. Clean RIE#3 with ISO and clean wipes.
2. O2 clean of system as follows:
   (a) O2 flow rate = 20.0 sccm
   (b) chamber pressure = 50.0 mTorr
   (c) Voltage=500 V
   (d) Minimize reflected power by tuning
   (e) Etch for 30 minutes
3. Load sample, pump down to at least 1 x 10-5 torr.
4. Etch conditions:
   (a) SF6,O2 flow rate = 6.0, 10.0 sccm
   (b) chamber pressure = 50.0 mTorr
   (c) Voltage=350 V
   (d) Minimize reflected power by tuning
   (e) Etch for 11.5 minutes
5. Look under microscope. Small vias may already be clear. Large vias still brownish.
6. Repeat O2 clean as in (2), for at least 10 minutes.
7. Etch Ni in Ni etchant @ 60C with stirring @ 300rpm for 30 seconds after all Ni has disappeared (total etch time 45 secs - 1 min for 150 A Ni)..
8. Back into RIE#3 for blanket etch.
   (a) SF6,O2 flow rate = 6.0, 10.0 sccm
   (b) chamber pressure = 50.0 mTorr
   (c) Voltage=350 V

(d) Minimize reflected power by tuning

(e) Etch for 8 minutes

### A.12 Flip

**A Solvent clean and dehydration bake carrier wafer. Load it in sputter machine with the real wafer. Pump down to 1.5 E-6 torr.**

1. Flow 25 sccm Ar, sputter Ti, 10mT, 0.1KW, 5min.
2. Flow 25 sccm Ar, sputter Au, 10mT, 0.2KW, 10 min.
3. Let sources cool for 10 min.
4. Vent and Unload.

**B Backside SiN deposition(SIN10). Put the wafer upside down on a clean Si wafer.**

**C Au plating @ 5mA, 2.5 hours. Make sure no wires can get shorted or contact each other.**

**D Bonding**

1. Get our chuck, clean off with ISO soaked wipes. Switch Pedestal VAC switch on front down to remove or place chuck, then switch it back up.
2. Place InP wafer on upper chuck, GaAs wafer on lower chuck.
3. Hit UP VAC, LO VAC.
4. Set upper and lower temperatures to 220°C.
5. Spread solder on InP wafer.
6. Release LO VAC, get GaAs wafer and place face down on InP wafer.
7. Wet surfaces with In0.4Pb0.6 by dragging GaAs wafer around on InP wafer. After some time, check that GaAs and gold plated surfaces are completely covered with In. Then wet surfaces some more.
8. Remove excess InPb with Q-tip, then move to lower chuck.
9. Turn micrometer on side of bonder to ∼5.
10. Turn top piece over, hit clamp (watch from side) then riser.

11. Wafer should be separated from top chuck by small gap now. Apply 400 grams or so of pressure by slowly turning micrometer.
12. Set upper and lower chuck temperatures to 100°C.
13. When chucks reach 50°C, hit riser, then clamp, then turn top piece over.
14. Get wafers, clean up flip-chip bonder.

**E SiN Removal**

1. Remove SiN by immersing in BHF until SiN disappears.
2. 3 minute DI rinse.

**F InP Substrate Removal**

1. Mix HCl:DI 3:1 in junk beaker.
2. Dip for 25 minutes or so. If there was polyimide on back of wafer, dip for 2-3 minutes, then try to scrape off polyimide. Repeat until polyimide is gone.
3. Mix another solution in InP etch beaker. Finish off the etch in that beaker.
4. Rinse in DI for 3 minutes.

**G Clean Up**

1. Test some base-emitter diodes.
2. Clean up edges of wafer with blade.
3. Dip for 30 seconds in 3:1 HCl:DI, then 3 minute DI rinse.

### A.13 Collector

**A No Solvent Clean.** Dehydration bake 120°C, 30 minutes.

**B Collector Lithography**

1. Configure collector job for mirror image, different alignment mark coordinates.
2. Cool down after dehydration, 5 min
3. Wafer on spinner chuck with vacuum, blow with N2
4. Apply SPR 950-0.8 with syringe and filter to cover wafer
5. Spin at 6.0 krpm for 30 sec

6. Soft Bake, 90°C, 1 min. on hot plate
7. Apply CEM with syringe and filter to cover wafer
8. Spin at 6 krpm for 30 sec
9. Refigure cell size, average step size over 3rd row for X, and over the 4th column for Y.
10. Enter new cell size into job.
11. Focus offset of +54, (change system focus to 20 or so in order to get this)
12. Expo time of 1.66 seconds

**C Development**

1. Post Bake, 100°C, 2 min, 10 sec
2. Rinse in running D.I., 30 sec.
3. Develop in MF-701 for 1 min, 30 sec
4. Rinse in running D.I., 3 min

**D Oxygen Plasma Descum of Photoresist**

1. 300mT of O2
2. power = 100W at low frequency.
3. run for 15 seconds

**E Evaporation**

1. Mix a dilute solution of HF : H2O :: 1 : 20
2. Dip in dilute HF for 30 sec.
3. Rinse in DI for 3 min.
4. Blow dry with N2
5. Place wafer on E-Beam mount. Level it.
6. Put in a new crystal.
7. Pump down to below 1 x 10-6 torr
8. Deposit material: (use the small crucible for Au - be sure to load the right amount of charge. If charge is less Au might run out before the desired thickness is reached and if it is more then it might spill out of the crucible while melting)

**F Liftoff –>> DO NOT LET ACE DRY ON WAFER! <<–**

1. Soak wafer in beaker of ACE until metal comes loose.

| Material | Thickness($\AA$) | Dep. Rate ($\AA$/sec) | Approx. Vernier |
|---|---|---|---|
| Ti | 200 | 1-2 | 1.65 |
| Pt | 400 | 1 | 1.85 |
| Au | 4000 | 15 | 1.5 |

2. If the liftoff is stubborn, leave the wafer soaking in ACE overnight. Because ACE evaporates quickly, seal the top of the beaker with foil.
3. ACE squirt bottle. Do not squirt except at edges of wafer and only with wafer immersed in acetone. Do not squirt hard.
4. Rinse with METH then ISO (squirt bottle)
5. Rinse in running DI water for 3 min.
6. Blow dry with N2.
7. Check under microscope, then Dektak thickness of metal.

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