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Santa Barbara

Scaling Mesa InP DHBTs to Record Bandwidths

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by

Evan Lobisser

Committee in charge:

Professor Mark Rodwell, *Chairman*

Professor John Bowers

Professor Umesh Mishra

Professor Chris Palmstrøm

September 2011

The dissertation of
Evan Lobisser is approved:

Professor John Bowers

Professor Umesh Mishra

Professor Chris Palmstrøm

Professor Mark Rodwell, *Committee Chairman*

August 2011

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Evan Lobisser
August 2011

Curriculum Vitæ
Evan Lobisser

Research Interests

High-speed electronic device and circuit design, nanoscale semiconductor fabrication techniques, novel semiconductor materials, scientific policy and pedagogy.

Education

2011	Ph.D. in Electrical and Computer Engineering University of Calfornia, Santa Barbara, CA
2008	M.S. in Electrical and Computer Engineering University of Calfornia, Santa Barbara, CA
2006	B.S. in Electrical and Computer Engineering Oregon State University, OR

Experience

2006–2011	Graduate Student Researcher University of Calfornia, Santa Barbara, CA
2005–2006	Undergraduate Researcher Oregon State University, OR
2005	Undergraduate Intern Hewlett-Packard Corporation, OR

Publications

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Abstract

Scaling Mesa InP DHBTs to Record Bandwidths

Evan Lobisser

Indium phosphide heterojunction bipolar transistors are able to achieve higher bandwidths at a given feature size than transistors in the Silicon material system for a given feature size. Indium phosphide bipolar transistors demonstrate higher breakdown voltages at a given bandwidth than both Si bipolars and field effect transistors in the InP material system. The high bandwidth of InP HBTs results from both intrinsic material parameters and bandgap engineering through epitaxial growth. The electron mobility in the InGaAs base and saturation velocity in the InP collector are both approximately three times higher than their counterparts in the SiGe material system. Resistance of the base can be made very low due to the large offset in the valence band between the InP emitter and the InGaAs base, which allows the base to be doped on the order of 10^{20} cm^{-3} with negligible reduction in emitter injection efficiency.

This thesis deals with type-I, NPN dual-heterojunction bipolar transistors. The emitters are InP, and the base is InGaAs. There is a thin (~10 nm) n-type InGaAs "setback" region, followed by a chirped superlattice InGaAs/InAlAs grade to the InP collector. The setback, grade, and collector are all lightly doped n-type. The emitter and collector are contacted through thin (~5 nm) heavily doped n-type InGaAs layers to reduce contact resistivity.

The primary focus of this work is increasing the bandwidth of InP HBTs through the proportional scaling of the device dimensions, both layer thicknesses and junction areas, as well as the reduction of the contact resistivities associated with the

transistor. Essentially, all RC time constants and transit times must be reduced by a factor of two to double a transistor's bandwidth. Chapter 2 describes in detail the scaling laws and design principles for high frequency bipolar transistor design. A low-stress, blanket sputter deposited composite emitter metal process was developed. Refractory metal base contacts were investigated with UCSB grown epitaxial material and the fabrication of transmission line model structures. Electron beam lithography processes were developed and employed for both emitter and base layers. Epitaxial designs were scaled and revised, and grown by a commercial vendor. These process developments are detailed in Chapter 3.

Transistor electrical characteristics were measured using a semiconductor parameter analyzer at DC and network analyzers for RF measurements at frequencies up to 220 GHz. Both on- and off-wafer network analyzer calibration structures were designed and fabricated, and the calibration techniques were compared. New structures for transmission line model measurements of contact resistivity have been designed and used in the measurement of new ohmic contact processes. Measurement techniques are detailed in Chapter 4.

Two transistor results are presented in Chapter 5. For each device, epitaxial designs are presented, and band diagrams, both without current flow and under peak bias conditions are shown. The processes used to fabricate each transistor are detailed. For the first result, referred to as DHBT 43, $f_\tau = 360$ GHz and $f_{max} > 800$ GHz was obtained with 200 nm wide emitter-base junctions and 150 nm thick collectors. For the second result, referred to as DHBT 60, $f_\tau = 530$ GHz and $f_{max} = 750$ GHz was obtained with 150 nm wide emitter-base junctions and 70 nm thick collectors. Both transistors feature a refractory emitter contact, and the second result uses electron-beam lithography to narrow the emitter-base and

base-collector junction widths. DC measurements of common-emitter I-V curves and Gummel plots are used to extract device parameters like breakdown voltage, current gain, and base and collector ideality constants. On-wafer TLM structures are used to extract device base and collector resistance. S-parameter measurements at RF frequencies are used to extract cutoff frequencies f_τ and f_{max}, as well as device parameters necessary to generate hybrid-π equivalent circuit models of the devices. These measurements and device results are detailed in Chapter 5.

Chapter 6 summarizes the progress and results of this work, and identifies the critical challenges and limits to further device scaling. Fabrication processes are proposed for the next generation of InP bipolar transistors.

Professor Mark Rodwell
Dissertation Committee Chair

For Mr. Hocken

Contents

Acknowledgements **iv**

Curriculum Vitæ **vi**

Abstract **x**

Figures **xvii**

Tables **xx**

1 Introduction **1**
References . . . 4

2 InP Bipolar Transistor Design **6**
2.1 Geometrical Design Principles . . . 6
2.1.1 Emitter Dimensional Dependencies . . . 7
2.1.2 Base-Collector Dimensional Dependencies . . . 8
2.2 Collector Design . . . 11
2.2.1 Kirk Effect . . . 11
2.2.2 Maximum Collector Doping . . . 13
2.3 High-frequency Behavior . . . 17
2.3.1 Base Transit Time . . . 17
2.3.2 Collector Transit Time . . . 18
2.3.3 Junction Delay Terms . . . 20
2.4 High-frequency Figures of Merit . . . 21
2.5 Small-signal Device Model . . . 26
2.6 HBT Scaling Principles . . . 28
2.7 Challenges and Limits of Device Scaling . . . 32
2.8 Conclusions . . . 34
References . . . 35

3 Fabrication Processes **37**
3.1 HBT Process Overview . . . 38
3.2 Emitter Process Development . . . 42
3.2.1 Emitter Contact Deposition . . . 43
3.2.2 Emitter Lithography . . . 45
3.2.3 Emitter Etch Mask . . . 46
3.2.4 Emitter Sidewalls and Low-stress Materials . . . 47
3.2.5 Vertical Emitter Contact Etch Profile . . . 51
3.2.6 Controllable Emitter Semiconductor Etch . . . 52
3.3 Base Process Development . . . 57
3.3.1 Electron-beam Lithography for the Base . . . 59
3.3.2 Refractory Base Contacts . . . 60
3.4 Transistor Back-end Processes . . . 61
3.4.1 Surface Preparation . . . 63
3.4.2 Base Post . . . 63
3.4.3 Photoresist Removal . . . 64
3.4.4 BCB Cure . . . 65
3.5 Transmission-line Model Structures . . . 66
3.6 Conclusions . . . 69
References . . . 70

4 Device Measurement **72**
4.1 Coplanar Pad Transistors . . . 72
4.1.1 Off-wafer Calibration . . . 73
4.1.2 Calibration Verification . . . 76
4.1.3 Pad Parasitic Removal . . . 78
4.1.4 Isolated versus Shared Ground Plane . . . 81
4.2 Microstrip Transmission Line Transistors . . . 83
4.2.1 Transmission Line Fabrication . . . 83
4.2.2 Thru-Reflect-Line Calibration . . . 86
4.2.3 Calibration Verification . . . 87
4.3 TLM Measurement . . . 90
4.3.1 TLM Extraction Procedure . . . 90
4.3.2 Pad Geometries . . . 92
4.3.3 Error Analysis . . . 93
4.4 Conclusions . . . 95
References . . . 96

5 HBT Results **98**
5.1 DHBT 43 . . . 98
5.1.1 Epitaxial Design . . . 99
5.1.2 Process Flow . . . 101
5.1.3 DC Characteristics . . . 103
5.1.4 RF Data . . . 103
5.1.5 Conclusions . . . 108
5.2 DHBT 60 . . . 110
5.2.1 Epitaxial Design . . . 110
5.2.2 Process Flow . . . 111
5.2.3 DC Characteristics . . . 115
5.2.4 RF Data . . . 115
5.2.5 Conclusions . . . 121
References . . . 123

6 Conclusion **124**
6.1 Summary . . . 124
6.1.1 Design Principles . . . 124
6.1.2 Fabrication Techniques . . . 126
6.1.3 Results . . . 127
6.2 Future Work . . . 127
6.2.1 Shorter Emitter Contact . . . 128
6.2.2 Refractory Base Contacts . . . 131
6.2.3 Regrown Base . . . 132
6.3 Conclusion . . . 133
References . . . 135

A Small-signal Parameter Extraction **137**

B Current HBT Process Flow **144**

Figures

2.1 Diagrams of mesa HBT structure 7
2.2 Angled SEM image of complete mesa HBT 8
2.3 Electric field in the collector with varying J_c 12
2.4 Collector electric field with highest N_c maintaining full depletion . 14
2.5 Collector band diagrams at different dopings 15
2.6 Collector electrostatics 15
2.7 Base-collector region with and without δ-doping 16
2.8 Modeled collector velocity in InP 20
2.9 Bipolar transistor with output short-circuited 22
2.10 Hybrid-π HBT model with distributed base-collector RC network . 23
2.11 Circuit used to determine Mason's Unilateral Gain 24
2.12 Distributed RC network in the base-collector junction 25
2.13 Hybrid-π small-signal model of HBT with parasitic resistances and capacitances 27
2.14 Measured (dotted) and modeled (solid) HBT S-parameters 28

3.1 Emitter contact deposition and etch 39
3.2 Emitter sidewall formation and mesa etch 39
3.3 Sputtered base process flow 40
3.4 Lifted off posts 41
3.5 Finished transistor with microstrip ground plane and ground posts 42
3.6 Emitter contact adhesion loss 44
3.7 Optically and electron-beam defined emitter caps 45
3.8 Emitter with Cr and SiO_x Cap 46
3.9 Variation in BCB height requires tall emitters 48
3.10 Dual emitter sidewalls are visible in TEM cross section 49
3.11 Stress and sheet resistance in sputtered W as pressure is varied . . 50
3.12 Smooth and columnar W 51
3.13 Emitter metal etch profiles 53
3.14 Transistor with emitter contact removed, exposing undercut of emitter semiconductor 54
3.15 Hybrid dry/wet emitter semiconductor etch 55

3.16 Hybrid dry and wet etch of the emitter semiconductor, with controllable undercut 56
3.17 W/$Ti_{0.1}W_{0.9}$ emitter contact enables thin emitter semiconductor layers 58
3.18 UV-6 photoresist spun around emitter structure 60
3.19 Contact resistivity vs. active carrier concentration with ex-situ W p-type contacts 62
3.20 Cross-section of photoresist and LOL after exposure and development 64
3.21 Metal attacked by photoresist removers 65
3.22 Mount for BCB cure 66
3.23 Cross-section of TLM pad structure 68
3.24 Top view of TLM pad structure formed through metal liftoff and wet etch 69

4.1 Schematic of GSG coplanar transistor pad structure 74
4.2 Two-part calibration to move reference plane to transistor terminals 74
4.3 Calibration standards for LRRM calibration (Open optional) 76
4.4 Calibration verification for off-wafer LRRM calibration 77
4.5 Calibration verification for off-wafer LRRM calibration (Smith chart) 77
4.6 Equivalent circuit for transistor and pad parasitics 78
4.7 Coplanar Calibration Structures 80
4.8 Shared and isolated coplanar pads 82
4.9 Gain for shared and isolated coplanar pads 82
4.10 Microstrip transmission line pad layout and fabrication 84
4.11 Transistor surrounded by microstrip ground plane and posts 85
4.12 Calibration verification on “Thru” standard 89
4.13 Transmission line model of planar Ohmic contact 90
4.14 Resistance plot for TLM extraction 91
4.15 Four-point TLM pad structure 93
4.16 Measured TLM data and calculated uncertainty 94

5.1 Band diagram for DHBT 43 100
5.2 SEM cross-section of DHBT 43 102
5.3 Angled SEM of DHBT 43 emitter after wet etch 102
5.4 DHBT 43 Common-Emitter Curves 104
5.5 DHBT 43 Gummel Plot 105
5.6 DHBT 43 gains, with extrapolated cutoff frequencies 106
5.7 DHBT 43 f_τ and f_{max} vary with current and collector-base voltage 107
5.8 Variation of C_{cb} with current and collector-base voltage 108
5.9 Equivalent circuit and S-parameters for DHBT 43 109
5.10 Band diagram for DHBT 60 112

5.11 DHBT 60 after emitter and base fabrication 114
5.12 TEM cross-section of emitter and base of DHBT 60 114
5.13 DHBT 60 Common-Emitter Curves 116
5.14 DHBT 60 Gummel Plot 117
5.15 DHBT 60 gains, with extrapolated cutoff frequencies 118
5.16 Cutoff frequency and collector-base capacitance dependence on bias 119
5.17 Equivalent circuit and S-parameters for DHBT 60 120
5.18 Base contact interface for DHBT 60 122

6.1 Angled SEM of electron-beam lithography defined emitter 126
6.2 Emitter and base fabricated through electron-beam lithography . . 127
6.3 Minimum emitter feature size 129
6.4 Proposed process flow for short emitter 130
6.5 Proposed process flow for short emitter 132
6.6 Regrown extrinsic base 133
6.7 Modeled τ_b and f_τ for DHBT 60 with varying base thickness 134

A.1 Standard small-signal model of a bipolar transistor 138
A.2 Hybrid-π small-signal model of HBT with parasitic resistances and capacitances 138
A.3 High current densities are used to extract R_{ex} and g_m 140
A.4 τ_{ec} vs. $\frac{1}{I_c}$ plot demonstrating current-induced velocity overshoot . . 141

Tables

2.1 HBT Scaling Laws 31
2.2 HBT Scaling Roadmap 33

3.1 N-type contacts to InGaAs 44
3.2 P-type contacts to InGaAs 61

5.1 DHBT 43 Epitaxial Design 100
5.2 DHBT 43 Contacts 103
5.3 DHBT 60 Epitaxial Design 112

6.1 Necessary reductions to double HBT bandwidth 125
6.2 Critical parameters of DHBT 43 and DHBT 60 128

Chapter 1

Introduction

Heterojunction bipolar transistors fabricated in the Indium phosphide material system are able to achieve higher bandwidths than Silicon germanium bipolar transistors or Silicon-based field-effect transistors at a given lithographic feature size. At a given bandwidth, InP HBTs demonstrate higher breakdown voltages than Si-based bipolars or InP-based FETs.

InP HBTs derive their superior high frequency performance from the high electron mobility in the InGaAs base and the high electron saturation velocity of the InP collector. Both are about three times higher in the InP/InGaAs material system than in the SiGe material system [1, 2]. The superior breakdown is due to the approximately 0.5 eV offset in valence band energies between the InP emitter and InGaAs base [3]. This large energy barrier at the emitter-base heterojunction allows the base to be doped in the 10^{20} cm^{-3} range to reduce base resistance while maintaining high emitter injection efficiency.

Increases in InP HBT RF performance are obtained through aggressive scaling of epitaxial layer thicknesses, lithographic feature widths, and contact resistivities for both n- and p-type contacts [4]. InP double heterojunction bipolar transistors fabricated in a triple mesa process with emitter mesa widths less than 250 nm

have demonstrated power gain cutoffs in excess of 1.0 THz [5, 6]. The superior RF performance of InP-based transistors to Si-based transistors makes them compelling options for building Terahertz monolithic integrated circuits, and InP-based HBTs offer higher breakdown voltages at a given f_τ than InGaAs-based HEMT devices, making them an advantageous platform on which to build TMICs. Mesa HBT processes at quarter-micron or larger emitter widths have been used to design few-transistor integrated circuits demonstrating record high frequency performance, including dynamic logic dividers, fundamental oscillators, and amplifiers operating in excess of 300 GHz [7, 8, 9].

The transistors described in this work are fabricated in a triple-mesa structure: collector, base, and emitter semiconductor layers are grown sequentially by solid-source molecular beam epitaxy, and the semiconductor layers are electrically isolated from each other through suquential mesa etches after electrical contacts to each layer are formed. During transistor operation, current flows vertically through the structures, perpendicular to the direction of epitaxial growth. Reducing the thickness of the base and collector semiconductor layers reduces the transit time for electrons across these layers, τ_b and τ_c. Thinning these layers will increase the short-circuit current gain cutoff frequency $f_\tau \sim (2\pi(\tau_b + \tau_c))^{-1}$. To realize performance gains in integrated circuits, RC time constants associated with the transistors must also be reduced as the devices are scaled epitaxially to maintain high power gain cutoff frequency, f_{max}. The emitter and base resistances, which include terms associated with the contact metal resistances, metal-semiconductor interfacial resistances, and bulk semiconductor resistances, are the most critical resistances with respect to high bandwidth performance. The capacitance associated with the base-collector mesa, C_{cb}, is the dominant capacitance to be scaled.

Chapter 2 of this thesis describes the theory of mesa HBT performance and outlines design rules and scaling laws for developing THz frequency, balanced f_τ and f_{max} transistors, and chapter 3 details the extensive process techniques developed iteratively through several generations of the UCSB InP mesa DHBT platform. In this work, emitter mesa widths were narrowed from 250 nm to less than 100 nm through the development of sputtered refractory metal emitter contacts, defined through electron-beam lithography and inductively coupled plasma dry etches. Sufficient device yield was maintained as device dimensions were reduced by minimizing the stress in the sputtered emitter metal film, and forming SiN_x sidewalls through plasma-enhanced chemical vapor deposition and anisotropic dry etch processes to chemically protect and mechanically anchor the emitter metal contact in place.

Substantial reductions in emitter and base contact resistivities have been achieved through the investigation of both sputtered and evaporated metal contacts, surface preparation techniques prior to metal deposition, and very high doping of the semiconductor layers: $\sim 5 \times 10^{19}$ cm^{-3} for n-type semiconductor, and $\sim 1 \times 10^{20}$ cm^{-3} for p-type semiconductor. Ohmic contact resistivities ρ_c of less than 2.0 $\Omega \cdot \mu m^2$ have been demonstrated on both n- and p-type InGaAs using the refractory metals Mo and W, respectively. Refractory metals are a good candidate for highly scaled HBTs due to their stability at the high temperatures and high current densities seen in a transistor under operation.

Chapter 4 describes the measurement technqiues used to extract the contact resistivities of refractory metal contacts to both n- and p-type InGaAs from transmission-line-model experiments, as well as the DC and RF measurement procedures used for HBT measurements. Several RF calibration methods are explained and compared, and the techniques used to extract f_τ and f_{max} from measured data are detailed.

Chapter 5 covers InP HBTs fabricated at UCSB. First, a 200 nm wide emitter result with $f_\tau = 360$ GHz and $f_{max} > 800$ GHz, on an epitaxial design with base thickness $T_b = 30$ nm and collector thickness $T_c = 150$ nm. This was the first reported InP HBT with sub-quarter-micron emitter widths, and they were enabled by a dual SiN_x sidewall process. Experiments in low-resistance, *ex-situ*, p-type contacts are also explored which are critical to further device improvement. Second, a 150 nm wide emitter result used electron-beam lithography to define both emitter and base contacts. In addition to narrowing the junctions, layer thicknesses were thinned to $T_b = 25$ nm and $T_c = 70$ nm. This device demonstrated $f_\tau = 530$ GHz and $f_{max} = 750$ GHz.

Chapter 6 summarizes the results and conclusions of this work, and proposes several process flows which may enable further device scaling and further increases in bipolar transistor bandwidth.

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Chapter 2

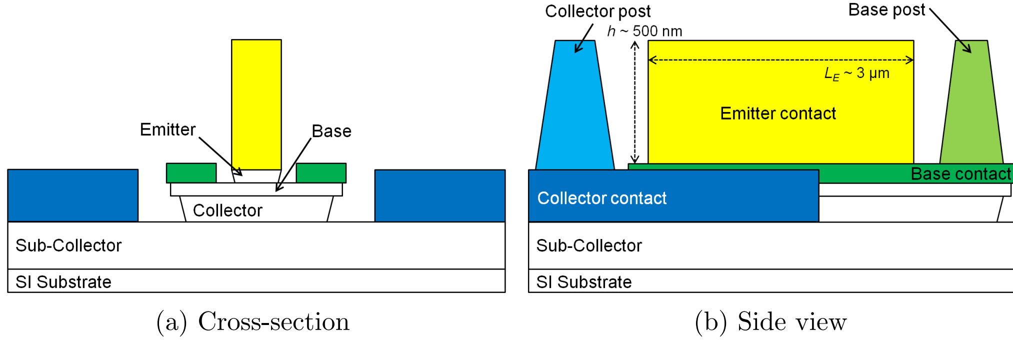
InP Bipolar Transistor Design

This chapter describes the design principles developed for mesa double heterojunction bipolar transistors constructed at UCSB in the past five years. The mesa structure and pertinent device dimensions are illustrated. Carrier transit delays, resistances, and capacitances are derived, largely from the physical geometry of this mesa DHBT structure. Transistor RF figures of merit f_τ and f_{max} are developed, based on these physical transit delays and RC time constants.

The figures of merit f_τ and f_{max}, as well as the geometrical dependence of the underlying transit times, resistances, and capacitances on device dimensions, motivates the development of scaling laws prescribing how best to increase device bandwidth. Finally, based upon these scaling laws, a roadmap for InP HBT RF performance is presented, and critical scaling challenges are described.

2.1 Geometrical Design Principles

The mesa HBTs described in this work are grown epitaxially upon each other, from the collector, to the base, to the emitter. Contacts are formed to the emitter, and then an etch is performed to define the emitter mesa. The process is repeated



(a) Cross-section (b) Side view

Figure 2.1: Diagrams of mesa HBT structure

to define base and collector contacts and isolate the base and collector mesas, as shown in Figs. 2.1 and 2.2. The fabrication process is described in extensive detail in Chapter 3.

2.1.1 Emitter Dimensional Dependencies

Because the emitter semiconductor is the top-most layer of epitaxy, the emitter contact can be formed directly on top of the active region of the emitter semiconductor. Current flows vertically through this contact into the semiconductor, giving an emitter contact resistivity of

$$\rho_e = R_{ex} A_e \tag{2.1.1}$$

where R_{ex} is the extrinsic emitter resistance, encompassing the metal resistance of the emitter contact, resistance at the emitter metal-semiconductor interface, and resistance in the bulk and at the heterointerface of the emitter semiconductor. The contact defines the emitter junction area $A_e = W_e \cdot L_e$, where W_e and L_e are the emitter width and length, respectively. The area of the emitter mesa and the

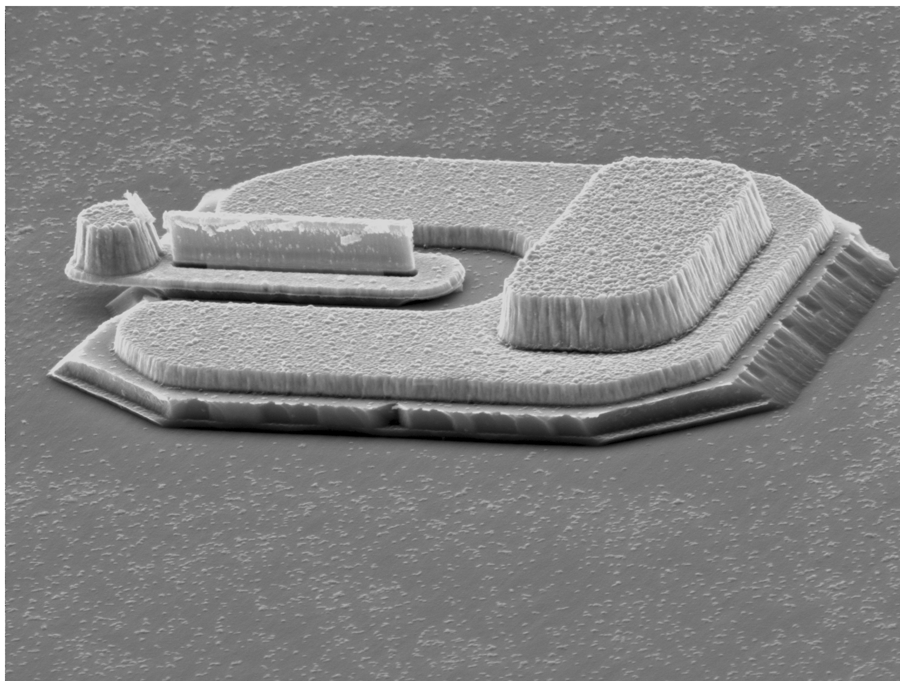


Figure 2.2: Angled SEM image of complete mesa HBT

emitter-base depletion thickness T_{eb} determine the depletion-layer capacitance of the emitter junction.

$$C_{je} = \frac{\epsilon A_e}{T_{eb}} \tag{2.1.2}$$

2.1.2 Base-Collector Dimensional Dependencies

A two-sided base contact is deposited self-aligned to the emitter mesa. The total width of the base mesa is the sum of these components, $W_b = 2W_{b,cont} + 2W_{b,gap} + W_e$. As with the emitter-base depletion capacitance, the collector-base capacitance C_{cb} is essentially a parallel plate capacitor:

$$C_{cb} = \frac{\epsilon A_c}{T_c} \tag{2.1.3}$$

where $A_c \sim W_b \cdot L_e$ is the area of the collector mesa and T_c is the thickness of the base-collector depletion region. In the devices described in this work, this depletion region is effectively the thickness of the lightly doped portion of the collector, which is designed so the collector is fully depleted under the full range of operational biases.

Because the base contact is deposited adjacent to the emitter and the active area of the device, current flowing through the base terminal flows both vertically through the metal-semiconductor interface and laterally under the base contact, laterally through the gap between the emitter and base contact, and under the emitter mesa. The total base resistance is composed of three terms: $R_{b,cont}$, the base contact resistance, $R_{b,gap}$, the resistance in the semiconductor in the emitter-base gap, and $R_{b,spread}$, the spreading resistance in the semiconductor beneath the emitter. The base contact resistance has the form

$$R_{b,cont} = \frac{\sqrt{\rho_c \rho_s}}{2L_e} \coth \frac{W_b}{L_T} \tag{2.1.4}$$

where ρ_c and ρ_s are the specific contact and sheet resistivities for the base, with units of $\Omega \cdot \mu m^2$ and $\Omega/\Box$, and the transfer length $L_T \equiv \sqrt{\frac{\rho_c}{\rho_s}}$. The factor of 2 in the denominator arises from the two-sided nature of the base contact, and the hyperbolic cotangent involving the base contact width and base transfer length is derived from modeling the planar base contact using transmission line techniques [1]. For typical HBT base designs, the base contact resistance can be approximated using the first two terms of the Laurent Series Expansion $\coth(x) \approx \frac{1}{x} + \frac{1}{3}x$

$$R_{b,cont} \approx \frac{\rho_c}{2L_e W_{b,cont}} + \rho_s \frac{W_{b,cont}}{6L_e} \tag{2.1.5}$$

The semiconductor region in the gap between the emitter-base contacts contributes a resistance

$$R_{b,gap} = \rho_s \frac{W_{b,gap}}{2L_e} \tag{2.1.6}$$

and the spreading resistance term under the emitter has a resistance

$$R_{b,spread} = \rho_s \frac{W_e}{12L_e} \tag{2.1.7}$$

where the factor of 12 in the denominator comes from, via symmetry, an effective stripe length of $2L_e$, a contact width of $\frac{W_e}{2}$, and an additional factor of 3 because of the two-dimensional current spreading under the emitter. Combining Eqs. 2.1.5, 2.1.6, and 2.1.7 results in an overall expression for base resistance

$$R_{bb} \approx \frac{\rho_c}{2L_e W_{b,cont}} + \rho_s \frac{W_{b,cont}}{6L_e} + \rho_s \frac{W_{b,gap}}{2L_e} + \rho_s \frac{W_e}{12L_e} \tag{2.1.8}$$

The contact resistance associated with the collector contact has the same general form as Eq. 2.1.8, however for the collector $W_c \gg L_T$, so $\coth \frac{W_c}{L_T} \approx 1$. Therefore, the collector resistance can be written as

$$R_c = \frac{\rho_s}{2L_e} \left(L_T + W_{c,gap} + W_b \right) \tag{2.1.9}$$

where ρ_s and L_T refer to the sheet resistance and transfer length of the heavily doped n-type sub-collector region, and $W_{c,gap}$ and W_b refer to the spacing between the collector contact and the collector mesa, and the collector mesa width, respectively.

2.2 Collector Design

There are two main constraints on the doping of the drift collector. Collectors too highly doped will not be fully depleted at low V_{cb} biases, leading to an increase in C_{cb}. Even if fully depleted, higher collector doping will increase the curvature of the conduction band in the collector, leading to earlier onset of $\Gamma - L$ scattering [2]. Conversely, if the collector doping is made too low, so is the threshold current density J_c at which "Kirk effect" occurs: the screening of background doping by mobile charge, creating a current-blocking barrier in the conduction band and increasing τ_c.

2.2.1 Kirk Effect

Since electrons in the collector travel at some finite velocity, assumed to be a constant v_{eff}, the electron density in the collector depletion region is

$$n_c = \frac{J_c}{qv_{eff}} \tag{2.2.1}$$

This electron density serves to screen out the background ionized donor doping in the collector. This screening affects the slope of the electric field and curvature of the potential in the collector region according to Poisson's equation

$$-\frac{d^2\phi}{dx^2} = \frac{d\mathcal{E}}{dx} = \frac{1}{\epsilon}\left(qN_c - \frac{J_c}{v_{eff}}\right) \tag{2.2.2}$$

where N_c is the collector doping. As J_c increases, so does n_c, and the net charge in the collector $N_c - n_c$ will decrease. According to Eq. 2.2.2, this will decrease and eventually invert the slope of the electric field in the collector, as shown in Fig. 2.3.

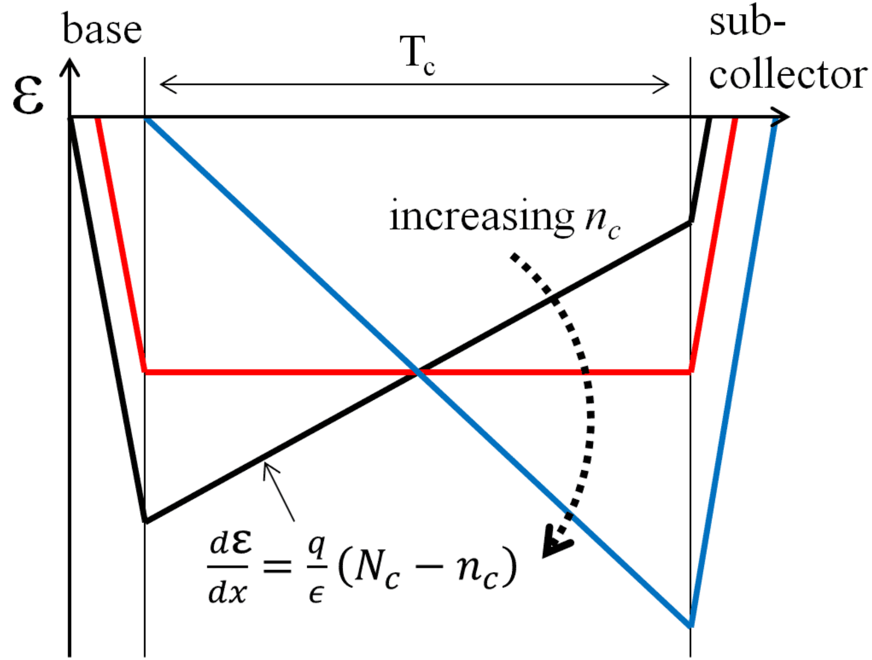


Figure 2.3: Electric field in the collector with varying J_c

Since the doping in the base and sub-collector regions is $\sim$ 100 times higher than in the collector, the areas under these portions of the graph can be neglected, and the total area under the electric field curve in the collector will stay constant with changing J_c, as it represents the sum of the applied bias and built-in potential $V_{CB} + V_{bi}$.

The triangular shaped electric field in Fig. 2.3 represents the onset of the Kirk effect, and corresponds to a current density of

$$J_{Kirk} = \frac{2\epsilon v_{eff}}{T_c^2}(V_{CB} + V_{bi}) + qv_{eff}N_c \tag{2.2.3}$$

For $J_c > J_{Kirk}$, the electric field near the base-collector interface will become positive. In a homojunction device, this creates a well in the collector valence band into which holes from the base are swept, effectively widening the base and increasing

τ_b [3]. In a heterojunction device, where there is a valence band barrier preventing holes from moving into the collecotr, there is still an increase in transit time. The inverted electric field at the interface causes a hump in the conduction band at the base-collector interface, forming a barrier to electron flow and increasing the stored charge in the base.

2.2.2 Maximum Collector Doping

The higher N_c is, the higher J_c before Kirk effect occurs. However, because digital logic IC design is easier with devices having the collector fully depleted at $V_{CB} = 0$, there is an upper limit set on collector doping. The critical doping occurs when the electric field in the collector goes to zero at the interface with the sub-collector, as shown in Fig. 2.4. Neglecting the area under the electric field curve in the heavily doped base region, the maximum allowable collector doping is

$$N_{c,max} = \frac{2\epsilon V_{bi}}{qT_c^2} \tag{2.2.4}$$

and the Kirk threshold current from Eq. 2.2.3 becomes

$$J_{Kirk} = \frac{4\epsilon v_{eff}}{T_c^2} \left(V_{CB} + V_{bi}\right) \tag{2.2.5}$$

twice as high as it would be in an undoped collector.

Depending on the doping in the collector N_c, and the ratio of emitter width W_e to collector thickness T_c, J_c may induce self-heating related RF performance degradation before J_{Kirk} is reached [4]. Independent of design constraints imposed by digital logic circuits, in these cases doping the collector more highly will reduce

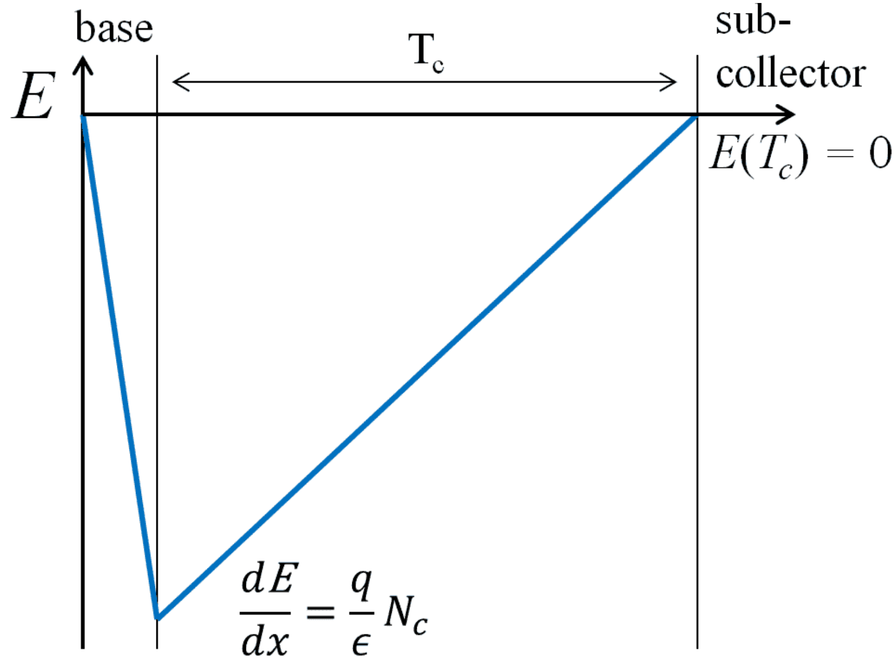
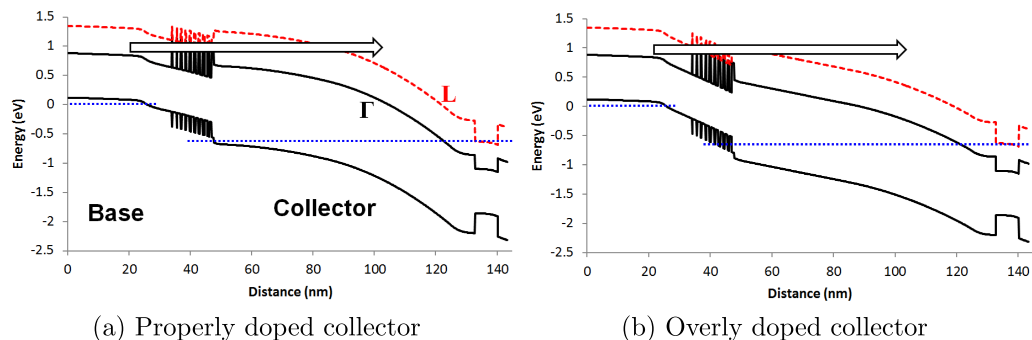


Figure 2.4: Collector electric field with highest N_c maintaining full depletion

the curvature in the collector conduction band at a given bias V_{CB} and current density J_c, as shown in Fig 2.5. This causes electrons to scatter from the Γ- to L-valley after traveling a shorter distance through the collector, increasing τ_c and reducing the maximum bandwidth of the transistor.

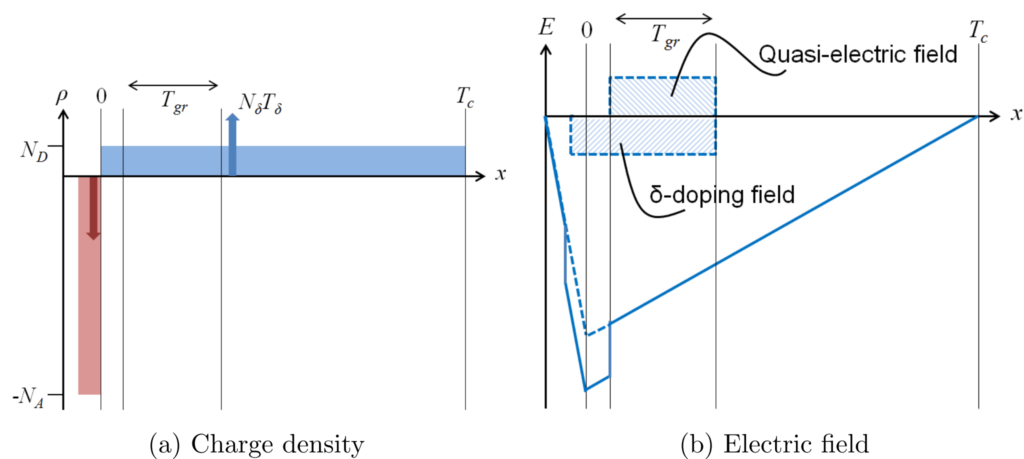
The HBTs described in this work feature an InGaAs base and InP collector — what is referred to as a Type-I HBT. The collector design incorporates an InGaAs setback region between the base, and an InGaAs/InAlAs chirped superlattice grade to remove the conduction band discontinuity between the InGaAs and InP portions of the collector [5]. To compensate for the quasi-electric field [6] induced by the graded region, a heavily doped region $\sim$ 3 nm in width, a "δ-doping," is used to induce an additional dipole field between the base and δ-doping to restore a continuous curvature to the graded region, as shown in Figs. 2.6 and 2.7.



(a) Properly doped collector

(b) Overly doped collector

Figure 2.5: Band diagrams for (a) properly doped and (b) overly doped collectors, comparing electron trajectories and relative distances traversed before $\Gamma-\mathrm{L}$ scattering occurs



(a) Charge density

(b) Electric field

Figure 2.6: Collector electrostatics

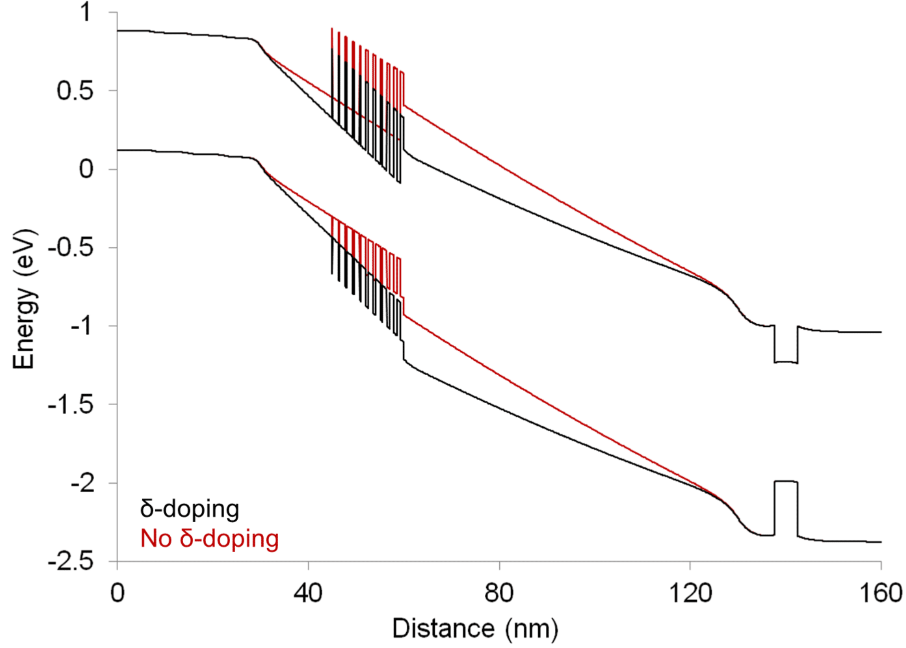


Figure 2.7: Base-collector region with and without δ-doping

The graded region creates a quasi-electric field of magnitude $\frac{\Delta E_c}{qT_{gr}}$, where T_{gr} is the length of the grade from InGaAs to InP. To remove the effect of this quasi-electric field, the δ-doping must have magnitude

$$N_\delta T_\delta = \frac{\epsilon \Delta E_c}{q^2 T_{gr}} \tag{2.2.6}$$

where $N_\delta T_\delta$ is the product of the δ-doping concentration N_δ and the thickness of the δ-doping layer, T_δ, and ΔE_c is the conduction band offset between InP and lattice-matched InGaAs, ~ 0.26 eV.

This additional dipole between the base and δ-doping modifies the total potential in the depleted collector, and therefore modifies the maximum collector doping to

maintain full depletion, Eq. 2.2.4.

$$N_{c,max} = \frac{2}{T_c^2}\left[\frac{\epsilon V_{bi}}{q} - N_\delta T_\delta \left(T_{sb} + T_{gr}\right)\right] \tag{2.2.7}$$

where T_{sb} is the thickness of the setback region before the grade. The dipole field reduces the maximum collector doping by as much as 2/3 in some designs [7].

2.3 High-frequency Behavior

For an HBT in active mode, when the emitter current is modulated by some amount ΔI_e, the collector current responds after some non-zero time delay representing the stored charge in different elements of the transistor. In general, to calculate the delays in the transistor, delay terms can be written as the modulated charge stored in an element divided by the modulated current through it, $\frac{\Delta Q}{\Delta I}$. The delays in a bipolar transistor are the base and collector transit times, τ_b and τ_c, and the emitter-base and base-collector junction charging times, τ_{eb} and τ_{bc}.

2.3.1 Base Transit Time

Electron transit times across the base and collector are a substantial portion of the delays determining total device bandwidth. To determine the base transit time, the collector current I_c in an active-mode transistor can be thought of as the excess electrons stored in the base, ΔQ_b, diffusing across to the collector every τ_b seconds, where

$$\tau_b = \frac{\Delta Q_b}{I_c} \tag{2.3.1}$$

is the base transit time. Using Shockley boundary conditions to derive ΔQ_b and I_c leads to an expression for base transit time of

$$\tau_b = \frac{T_b^2}{2D_n} \tag{2.3.2}$$

The Shockley boundary conditions imply infinite carrier velocity at the collector side of the base. Taking into account the finite exit velocity v_{sat} changes the shape of ΔQ_b from triangular to trapezoidal, and the additional charge stored in the base is reflected in the modified expression for τ_b [8, 9].

$$\tau_b = \frac{T_b^2}{2D_n} + \frac{T_b}{v_{sat}} \tag{2.3.3}$$

The HBTs described in this work employ a doping grade in the base which induces a quasi-electric field and decreases base transit time [10]. For a doping variation of about 5×10^{19} cm^{-3}, a a change in conduction band energy of $\Delta E_c \sim$ 50 meV is induced. For a linear variation in ΔE_c, the base transit time can be expressed as

$$\tau_b = \frac{T_b^2}{2D_n}\left(\frac{kT}{\Delta E_c}\right)\left[1 - \frac{kT}{\Delta E_c}\left(1 - e^{\frac{-\Delta E_c}{kT}}\right)\right] + \frac{T_b}{v_{sat}}\left(\frac{kT}{\Delta E_c}\right)\left(1 - e^{\frac{-\Delta E_c}{kT}}\right) \tag{2.3.4}$$

which leads to a $\sim$ 50% decrease in transit time.

2.3.2 Collector Transit Time

Excess electrons in the depleted collector induce imaged positive charge at both the base and sub-collector sides of the collector. The collector transit time is deter-

mined by the ratio of induced incremental base charge to the incremental increase in current through the collector [9, 11].

$$\tau_c = \int_0^{T_c} \frac{1}{v(x)} \left(1 - \frac{x}{T_c}\right) dx \equiv \frac{T_c}{2v_{eff}} \tag{2.3.5}$$

Charge closer to the base side of the collector induces more charge on the base side of the depletion region than it does when it is closer to the collector side, hence τ_c is essentially an average weighted by distance from the quasi-neutral base of the local electron velocity in the collector. This works out fortuitously for the InP material system, as electrons exiting the base first enter the Γ-valley of the InP collector, which has a saturation velocity $\sim 4.5 \times 10^7$ cm/s. In a properly designed collector, the electrons will traverse about 2/3 of the length of the collector before scattering to the L-valley, which has a higher effective mass and a saturation velocity approximately one-third of that in the Γ-valley. By modeling the collector velocity as a two-step profile as in Fig. 2.8, where the region before scattering has $v_\Gamma \sim 3 \times v_L$, and the point of scattering T_s occurs about two-thirds of the way through the collector, Eq. 2.3.5 can be re-written as a two-part integral

$$\tau_c = \int_0^{T_s} \frac{1}{v_\Gamma} \left(1 - \frac{x}{T_c}\right) dx + \int_{T_s}^{T_c} \frac{1}{v_L} \left(1 - \frac{x}{T_c}\right) dx \tag{2.3.6}$$

and solved to give

$$\tau_c = \frac{1}{T_c} \left[\frac{2T_s T_c - T_s^2}{2v_\Gamma} + \frac{(T_c - T_s)^2}{2v_L} \right] \tag{2.3.7}$$

For the assumed values of v_Γ, v_L, and T_s stated above, $v_{eff} = \frac{11}{27} v_L \approx 3.6 \times 10^7$ cm/s. Extracted experimental values for $v_{sat} \sim 3 \times 10^7$ cm/s, higher than the saturated drift velocity of the collector.

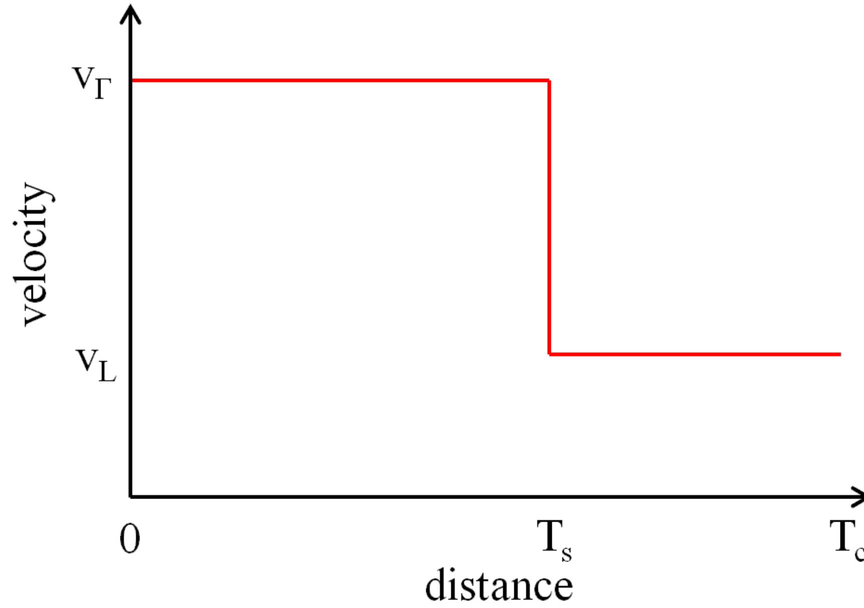


Figure 2.8: Modeled collector velocity in InP

2.3.3 Junction Delay Terms

In the emitter-base junction, a change in emitter current ΔI_e induces a change in stored charge ΔQ_{be}. The delay term associated with the junction is then

$$\tau_{eb} = \frac{\Delta Q_{be}}{\Delta I_e} = C_{je}\frac{\Delta V_{be}}{\Delta I_e} \cong C_{je}\frac{\Delta V_{be}}{\Delta I_c} \tag{2.3.8}$$

where C_{je} is the emitter-base junction capacitance and $\frac{\Delta V_{be}}{\Delta I_c}$ can be rewritten as

$$\left(\frac{V_{be}}{I_c}\right)^{-1} = g_m = \frac{1}{r_e} \cong \frac{qI_c}{\eta k_B T} \tag{2.3.9}$$

where η is the emitter ideality factor, typically between 1-2, and k_B is the Boltzmann constant. Therefore, Eq. 2.3.8 can be re-written as

$$\tau_{be} = \left(\frac{\eta k_B T}{q I_c}\right) C_{je} \tag{2.3.10}$$

Similar analysis can be employed in the collector-base junction. Under forward active DC bias, there is an AC short between the emitter and collector terminals. Therefore, an incremental change in ΔV_{be} leads to an incremental change in I_c, and therefore ΔV_{cb}

$$\Delta V_{cb} = \Delta V_{be} + \Delta I_c \left(R_{ex} + R_c\right) \tag{2.3.11}$$

Using a similarly defined delay term to Eq. 2.3.8,

$$\tau_{bc} = \frac{C_{cb}\Delta V_{cb}}{\Delta I_c} = \frac{C_{cb}}{\Delta I_c}\left(\Delta V_{be} + \Delta I_c \left(R_{ex} + R_c\right)\right) = \left(\frac{\eta k_B T}{q I_c} + R_{ex} + R_c\right) C_{cb} \tag{2.3.12}$$

The total delay term associated with electrons moving across the transistor is found by summing the previous transit times and delay terms.

$$\tau_{ec} = \tau_{be} + \tau_b + \tau_{bc} + \tau_c \tag{2.3.13}$$

2.4 High-frequency Figures of Merit

For a bipolar transistor with the output terminal short-circuited, as shown in Fig. 2.9, the frequency past which the current gain becomes less than unity is defined as the short-circuit current gain cutoff frequency f_τ. The current gain for

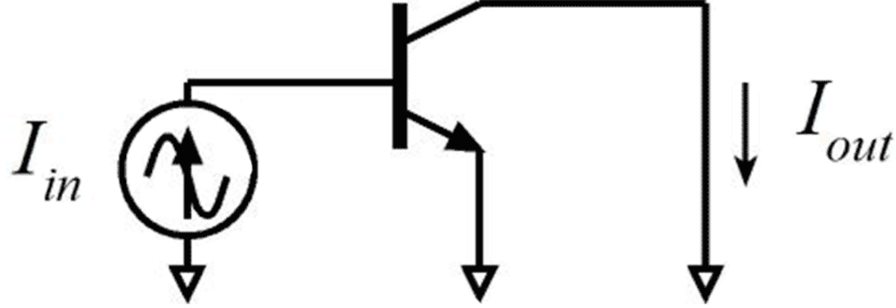


Figure 2.9: Bipolar transistor with output short-circuited

the circuit in Fig. 2.9 is found to have the form

$$\beta(j\omega) = \frac{\beta_0}{1 + j\beta_0\left(\frac{\omega}{\omega_\tau}\right)} \tag{2.4.1}$$

where $\beta_0 \cong \frac{I_c}{I_b}$ is the DC current gain, and $\omega_\tau \equiv 2\pi f_\tau$. At low frequencies, $\beta \approx \beta_0$. For frequencies $\omega \sim \omega_\tau$, $\beta \approx \frac{\omega_\tau}{j\omega}$, a single-pole roll off which reaches unity gain at ω_τ. From nodal analysis of Fig. 2.9 [9]

$$\frac{1}{\omega_\tau} = \frac{1}{2\pi f_\tau} = \tau_{ec} = \tau_b + \tau_c + \left(\frac{\eta k_B T}{qI_c}\right) C_{je} + \left(\frac{\eta k_B T}{qI_c} + R_{ex} + R_c\right) C_{cb} \tag{2.4.2}$$

While f_τ is a useful metric since it is directly dependent on intrinsic material parameters like carrier velocity and lifetimes, in actual amplifier designs, voltage (and therefore power) gain can be achieved at higher frequencies than f_τ. The maximum frequency of oscillation, f_{max}, is defined as the frequency beyond which power gain in a device is less than 1. This frequency is found where either Mason's Unilateral Gain, U, or Maximum Available Gain goes to 0 dB. In practice, U is preferred since it follows a single-pole roll off at 20 dB/dec. MAG/MSG has varying

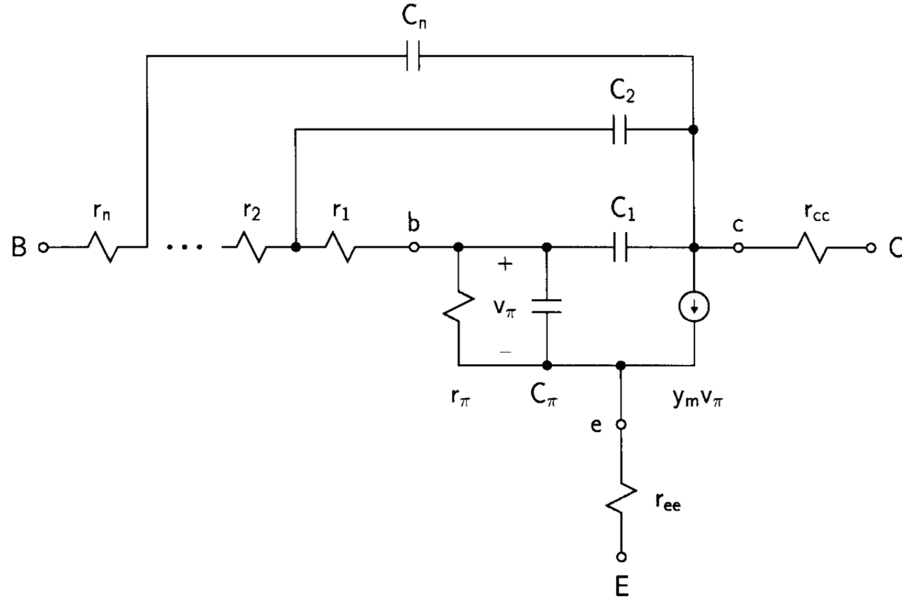


Figure 2.10: Hybrid-π HBT model with distributed base-collector RC network

slope, and cannot be used to extrapolate f_{max}. U also has the advantage of being independent from the lossless networks in which the transistor is embedded [12].

Amplifiers deliver the most gain to a conjugately matched load, so f_{max} is determined from the power gain for a small-signal model with conjugately matched load. In addition, to determine unilateral gain, the feedback between output and input is nulled, as shown in Fig. 2.11.

For the devices described in this work, the distributed nature of the base resistance R_{bb} and collector-base capacitance C_{cb} requires a more sophisticated equivalent circuit model, and analysis, as shown in Fig. 2.10 [13]. The maximum frequency of oscillation is found to have the form

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi\left(R_{bb}C_{cb}\right)_{eff}}} \tag{2.4.3}$$

where $\left(R_{bb}C_{cb}\right)_{eff}$ is an effective charging time some fraction of the full $R_{bb}C_{cb}$

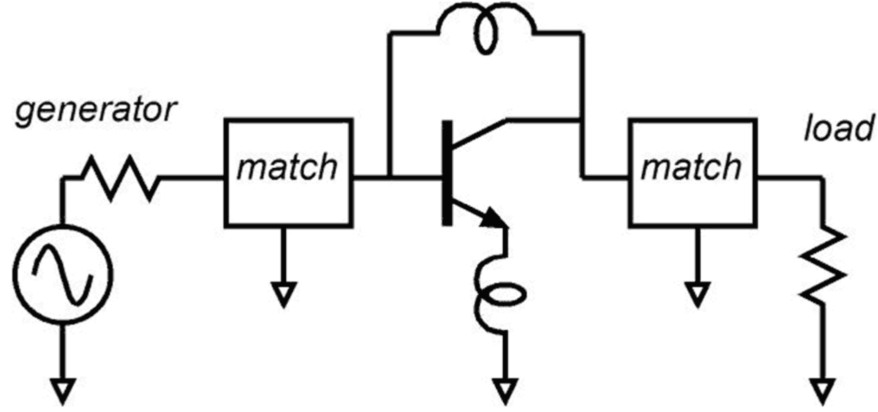


Figure 2.11: Circuit used to determine Mason's Unilateral Gain

product, based on the particular portions of C_{cb} which charge through certain components of R_{bb}.

For the mesa HBTs described in this work, the general model from [13] can be well approximated by breaking the base resistance into four parts and collector-base capacitance into three distinct components [14]. For the resistance, these are $R_{b,cont}$, the base contact resistance; $R_{b,spread,cont}$, the spreading resistance under the contact; $R_{b,gap}$, the resistance in the semiconductor gap between the base and emitter contacts; and $R_{b,spread}$, the spreading resistance in the semiconductor region under the emitter. For the capacitance, these are $C_{cb,e}$, the capacitance under the emitter region; $C_{cb,gap}$, the capacitance under the emitter-base gap; and $C_{cb,cont}$, the capacitance under the base contact. $C_{cb,e}$ is charged through a resistance $R_{b,spread} + R_{b,gap} + R_{b,spread,cont} + R_{b_cont}$, $C_{cb,gap}$ is charged through $\frac{R_{b,gap}}{2} + R_{b,spread,cont} + R_{b,cont}$, and $C_{cb,cont}$ is charged through $R_{b,cont}$, as shown in Fig. 2.12.

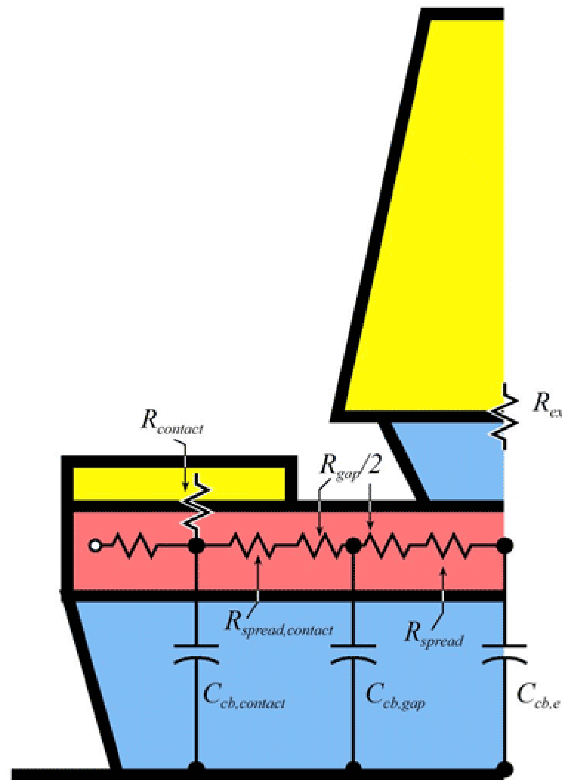


Figure 2.12: Distributed RC network in the base-collector junction

2.5 Small-signal Device Model

A hybrid-π small-signal model for a bipolar transistor is shown in Fig. 2.13. At the core of this model for an HBT in common-emitter biasing is a two-port network, with a voltage-dependent current source modeling the collector current. For accurate representation of measured high-frequency transistor behavior, parasitic capacitances C_{cb} and C_{je} are included, as well as the fictitious capacitance C_{diff}, modeling charge storage in the base.

$$C_{diff} \equiv \frac{dQ_b}{dV_{be}} = \frac{dQ_b}{dI_c}\frac{dI_c}{dV_{be}} = (\tau_b + \tau_c)\, g_m \tag{2.5.1}$$

The model also includes base-collector resistance R_{cb} and emitter-base resistance R_{be}. R_{cb} has unclear physical correspondence, but fits measured Y_{21} data.

$$R_{be} = \frac{\beta}{g_m} \tag{2.5.2}$$

To compactly model the distributed nature of $R_{bb}C_{cb}$ in the base-collector junction, C_{cb} is split into intrinsic and extrinsic components, $C_{cb,i}$ and $C_{cb,ex}$, the division of which is chosen to obtain good agreement between measured f_{max} and modeled f_{max} where $(R_{bb}C_{cb})_{eff} = R_{bb}C_{cb,i}$. It is important to note $C_{cb,i}$ does not correspond to some physical portion of the collector-base capacitance, but is instead a term defined by the distributed network of resistances and capacitances shown in Fig. 2.12.

The process of creating a hybrid-π model for a particular transistor involves incorporating measured on-wafer TLMs, theoretical values from literature, and fitting to measured S-parameter data. This is discussed in more depth in Appendix A. Good agreement between measured and modeled S-parameters verifies the quality

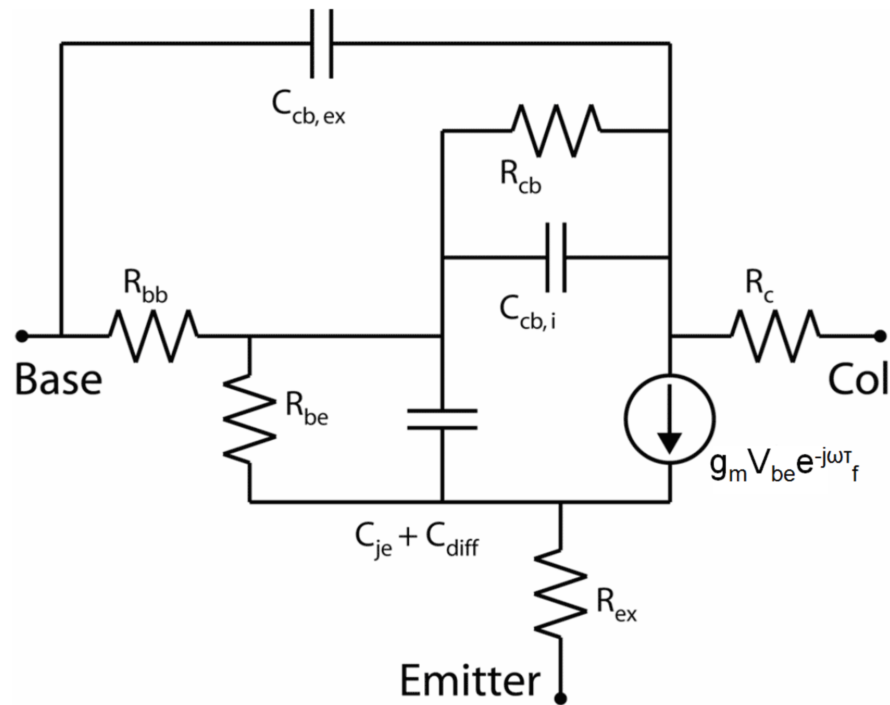


Figure 2.13: Hybrid-π small-signal model of HBT with parasitic resistances and capacitances

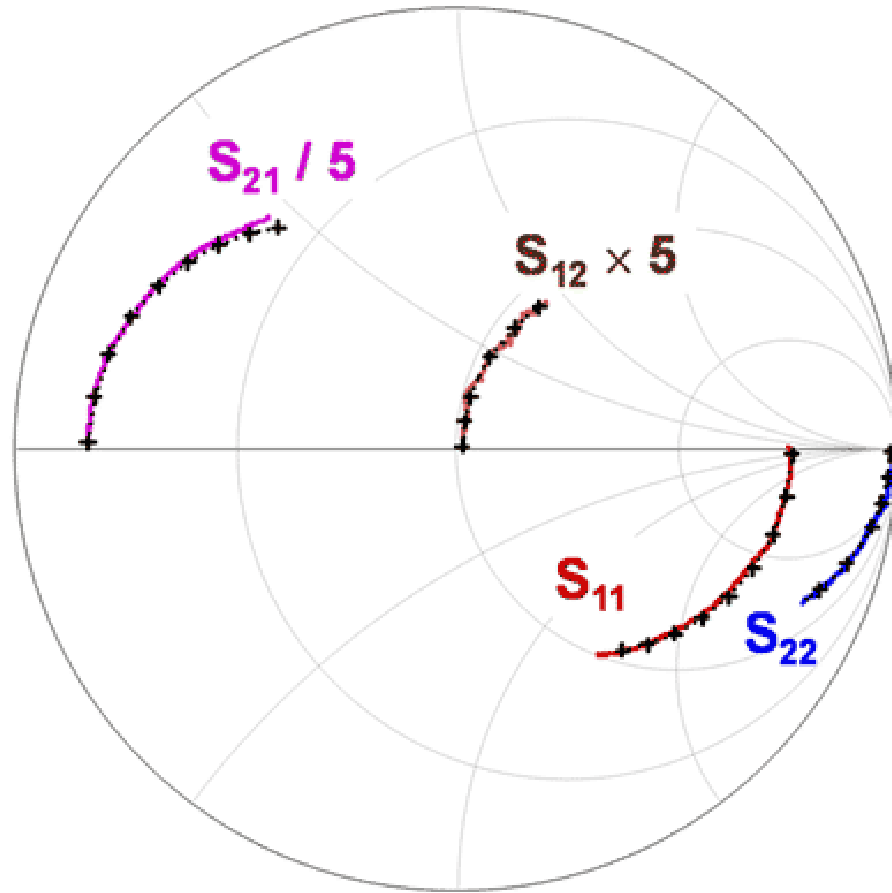


Figure 2.14: Measured (dotted) and modeled (solid) HBT S-parameters

of the measured data and identifies areas where process improvement or control may be necessary on future transistor fabrication runs.

2.6 HBT Scaling Principles

From the analyses in Secs. 2.1 and 2.3, sets of design principles can be developed to scale InP bipolar transistors for increased bandwidth while maintaining proportional f_τ and f_{max}. Fundamentally, to effect a $\gamma : 1$ increase in transistor bandwidth, all

the transit times and RC delays in the device must be scaled by $\gamma^{-1} : 1$.

For the base transit time τ_b, Eq. 2.3.4 shows scaling the base thickness T_b by a factor of $\gamma^{-\frac{1}{2}} : 1$ will modify τ_b by the necessary $\gamma^{-1} : 1$ factor. Eq. 2.3.5 shows τ_c depends directly on collector thickness T_c, so T_c must be reduced by a factor of $\gamma^{-1} : 1$ for the necessary transit time decrease.

Scaling T_b by $\gamma^{-1} : 1$ has the effect of increasing C_{cb} by $\gamma : 1$ for a given junction area. Simultaneously scaling the junction area A_c by a factor of $\gamma^{-2} : 1$ will result in the overall change in capacitance of $\gamma^{-1} : 1$, as desired. From Eq. 2.1.8, the $R_{b,cont}$ term of the base resistance is inversely proportional to junction area. Since the junction area is scaled by $\gamma^{-2} : 1$, the base contact resistivity ρ_c must also be scaled by $\gamma^{-2} : 1$ to maintain constant resistance as the device is scaled. Likewise for the emitter junction, to maintain constant extrinsic emitter resistance R_{ex} as the junction area is reduced, emitter contact resistivity ρ_c must also scale as $\gamma^{-2} : 1$.

When scaling junction capacitance by reducing junction area, either the contact width or length may be scaled. However, thermal constraints make reducing junction widths preferable to junction lengths. Treating the heat flow for a single transistor on a thick substrate of InP as cylindrical at distances $r \sim L_e$ and spherical at $r \gg L_e$, the following expression for junction temperature rise can be derived [15].

$$\Delta T \approx \frac{P}{\pi K_{InP} L_e} \ln \frac{L_e}{W_e} + \frac{P}{\pi K_{InP} L_e} \tag{2.6.1}$$

where ΔT is the temperature rise in the transistor, P is the power dissipated, and K_{InP} is a material parameter, the thermal conductivity of the InP substrate. The temperature rise is inversely proportional to device length L_e, but has a weaker inverse logarithmic dependence on W_e.

The devices pursued in this work employ junction scaling solely in the junction width of $\gamma^{-2} : 1$, while maintaining constant $L_e \propto \gamma^0 : 1$. This is an intermediate approach between scaling L_e and W_e both $\gamma^{-1} : 1$, which is the least difficult to implement lithographically, but sees a $\gamma : 1$ increase in junction temperature rise from one scaling generation to the next, and maintaining $\Delta T \propto \gamma^0 : 1$, which requires scaling W_e approximately by $\gamma^{-3} : 1$, a standard difficult to implement in process development for fabrication [16]. Another advantage of aggressively scaling W_e is the other terms in Eq. 2.1.8 are proportional to $\frac{W_e}{L_e}$, so reductions in the gap and spreading terms of R_{bb} can be realized.

As the junction area A_e is scaled $\gamma^{-2} : 1$ while current I_e is maintained constant, the emitter current density $J_e \equiv \frac{I_e}{A_e}$ scales as $\gamma^2 : 1$. Since T_c is also being scaled $\gamma^{-1} : 1$, and, from Eq. 2.2.5, $J_{Kirk} \propto \frac{1}{T_c^2}$, the current density can be increased at this rate without pushing the device into a regime higher than the Kirk limit. Ever higher current densities, and therefore higher power densities, do however necessitate thermally stable contacts and interfaces.

Since the base mesa width, and therefore, emitter width, W_e must be scaled proportionally to $\gamma^{-2} : 1$, the depletion capacitance portion of C_{je}, from Eq. 2.1.2, will also scale by the same factor. In addition to this depletion capacitance, which can be reduced by thickening the emitter-base depletion region, there is an additional capacitance associated with the junction that arises from charge storage, as well as a quasi-Fermi level drops in the depletion region [14, 17]

$$\Delta E_{fn} \equiv \int_{T_{eb}} \frac{J_e}{\mu(x)\, n(x)} dx \tag{2.6.2}$$

where T_{eb} is the emitter-base depletion region thickness, J_e is the emitter current

Design Parameter	**Scaling Law**
Collector Depletion Layer Thickness T_c	$\gamma^{-1}:1$
Base Thickness T_b	$\gamma^{-\frac{1}{2}}:1$
Emitter-base junction width W_e	$\gamma^{-2}:1$
Base-collector junction width W_b	$\gamma^{-2}:1$
Emitter access resistivity $\rho_{c,e}$	$\gamma^{-2}:1$
Base contact resistivity resistivity $\rho_{c,b}$	$\gamma^{-2}:1$
Emitter current density J_e	$\gamma^{2}:1$
Emitter length L_e	$\gamma:0$

Table 2.1: HBT Scaling Laws

density, and μ and n are the position-dependent carrier mobility and density in the region. For HBTs with 15 nm of lightly (2×10^{18} cm^{-3}) doped n-type emitter InP on a p$^+$ base doped at 9×10^{19} cm^{-3}, the voltage drop in the depletion region reduces g_m to about 80% of its ideal value, or increases the emitter ideality factor η to ~ 1.2 [17]. The emitter-base junction delay term r_eC_{je} can be written as

$$r_eC_{je} = \left(\frac{k_BT}{qI_c}\right)\left(\frac{\epsilon A_e}{T_{eb}}\right) + \frac{\Gamma T_{eb}T_b}{D_n}\int_0^1 \frac{n\left(\zeta T_{eb}\right)}{n\left(T_{eb}\right)}\zeta^2 d\zeta \tag{2.6.3}$$

where the first term represents the depletion capacitance, and the second term represents the charge storage in the depletion region. In the charge storage term, Γ is a term related to the band gap grading in the base, similar to the modifying factor in Eq. 2.3.4, and ζ is a normalized position variable $\zeta \equiv \frac{x}{T_{eb}}$. From Eq. 2.6.3, it is evident there are competing constraints upon T_{eb}: the depletion capacitance is minimized by making T_{eb} as large as possible, whereas the charge storage term is minimized by reducing T_{eb}. C_{je} is minimized for devices reported in this work with $T_{eb} \approx 15$ nm. Maximizing the current density J_e and reducing the junction area A_e will reduce the delay associated with both portions of C_{je}.

2.7 Challenges and Limits of Device Scaling

As outlined in Sec. 2.6 and Tab. 2.1, increasing a bipolar transistor's bandwidth requires proportional scaling of layer thicknesses, junction widths, and contact resistivities. Of these three tasks, reducing layer thicknesses is comparatively the easiest. The thinnest base and collector layers discussed in this work are 25 nm and 70 nm, respectively. Thinning these layers involves redesigning the base doping grade, collector background and δ-doping, as well as new base-collector grade designs of different lattice period and overall thinner length [18],but semiconductor layers of this order of thickness or even substantially thinner pose little challenge for modern epitaxial growth techniques.

More difficult is the required reduction in junction area, as it requires a quadratic (versus linear in layer thickness) reduction to double device bandwidth, and involves many sophisticated fabrication techniques to reliably produce narrow features with high yield. Transistors described in this work have emitter junctions as narrow as 128 nm, with base contacts of comparable widths and $\sim$ 50 nm misalignment between the two layers. The techniques necessary to produce these features include e-beam lithography and advanced i-line optical lithography, self aligned structures like dielectric sidewalls, formed through blanket deposition and anisotropic dry etch, and low-stress metal deposition techniques. The details of these processes and their development form a large portion of the innovation in this thesis, and are discussed in detail in Ch. 3.

Both n- and p-type contact resistivities of less than 5 $\Omega \cdot \mu m^2$ are presented in transistors in this work, and n-[19] and p-type [20, 21] contact resistivities of $\rho_c <\sim 2\,\Omega{\cdot}\mu m^2$ have been demonstrated in contact experiments using transmission-

Emitter Width W_e (nm)	256	128	64	32
Emitter Access Res. $\rho_{c,e}$ $(\Omega \cdot \mu m^2)$	8	4	2	1
Base Contact width $W_{b,cont}$ (nm)	175	120	60	30
Base Contact Res. $\rho_{c,b}$ $(\Omega \cdot \mu m^2)$	10	5	2.5	1.25
Base Thickness T_b (Å)	250	212	180	150
Collector Thickness T_c (nm)	106	75	53	38
Collector Current Density J_c $\left(\frac{mA}{\mu m^2}\right)$	9	18	36	72
f_τ (GHz)	520	730	1000	1400
f_{max} (GHz)	850	1300	2000	2800

Table 2.2: HBT Scaling Roadmap

line-model structures. If these contacts can be incorporated into a transistor process they are sufficient for simultaneous f_τ and f_{max} above 1.0 THz. Ohmic contact development of both in-situ (contact metal deposited on semiconductor cleaned and grown in MBE without breaking vacuum) and ex-situ (metal deposited after semiconductor has been exposed to air) are discussed, with resistivity reductions accomplished primarily by heavily doping semiconductor layers with active carriers and removing oxides from the surface immediately before contact deposition. A survey of these methods is provided in Secs. 3.2.1 and 3.3.2. The extraction of very low contact resistivities, particularly for p-type contacts since the sheet resistance of p-type InGaAs is typically much higher than that of n-type InGaAs, is non-trivial, and analysis of transmission-line model structures is discussed in more detail in 4.3.

Based on the design rules outlined in Tab. 2.1, a roadmap of transistor designs based on emitter contact width can be developed, as shown in Tab. 2.2. Symmetric increase in both f_τ and f_{max} is maintained from one scaling generation to the next by proportional scaling of all transit times and RC time constants. The results described in this work straddle the 256 and 128 nm emitter nodes, and process development for sub-100 nm devices is discussed.

2.8 Conclusions

This chapter details the design principles used to incrementally improve InP DHBT designs to achieve greater bandwidths. Key resistances and capacitances in the transistor are identified and described in terms of geometric principles and material constants. The resistances most important to device performance are the resistances associated with the emitter and base contacts, including metal resistance, contact resistivity, and interfacial metal-semiconductor resistances. The capacitances most influential to device bandwidth are the capacitances associated with the emitter-base and base-collector junctions. To a first order, these capacitances have the form of a parallel plate capacitance, although the modulation of stored charge in these junctions also has a non-negligible effect.

Transit times associated with electrons traversing the base and collector semiconductor regions are developed using electron transport theory. Proper design of the collector thickness, doping, and setback and pulse doping regions is discussed in order to minimize collector transit time by maximizing collector current density and delaying Γ-L scattering.

A hybrid-π equivalent circuit model for a bipolar transistor is presented, with high frequency parasitic capacitances included. Elements of the hybrid-π circuit can be tuned to achieve good agreement between measured S-parameters and those modeled by the equivalent circuit. These modeled elements can be used to estimate junction areas.

Using the developed relationships for resistances, capacitances, and transit times, a series of scaling laws is developed. In order to effect a $\gamma : 1$ increase in bandwidth, all transit delays and RC time constants in the transistor must be reduced by

$\gamma : 1$. This is accomplished through the reduction of layer thickness and junction areas. Finally, a roadmap for balanced scaling of bipolar transistors is presented, necessitating the process details described in Chapter 3.

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Chapter 3

Fabrication Processes

The important geometrical and material dependencies of the transit times, resistances, and capacitances associated with bipolar transistors were laid out in Ch. 2. In summary, semiconductor layers need to be thinned by epitaxial growth, junction widths need to be reduced by advanced lithographic and processing techniques, and contact resistivities to both emitter and base must be reduced through doping and surface preparation. This chapter will describe the extensive work carried out in the latter two of these areas.

At the time this work began in June 2007, the state-of-the-art for UCSB's HBT process was transistors with $\sim$ 250 nm wide emitter junctions, defined by optical lithography. The highest f_{max} reported at the time was 780 GHz, with a traditional lifted-off emitter contact and wet-etched emitter semiconductor [1, 2]. Processes developed to scale the emitter contact width, namely blanket-deposited and dry-etched emitter contacts and dry-etched emitter semiconductor mesas, had been developed, but minimum emitter junction widths demonstrated in this process were still nominally a quarter micron wide, and the transistors demonstrated simultaneous $f_\tau/f_{max} \approx 560/560$ GHz [3].

This chapter will further detail the extensive process work in forming narrower

emitter and base junctions than those at the 250 nm node, while maintaining low contact resistance and high device yield.

3.1 HBT Process Overview

The UCSB HBT processes developed consist of ten or eleven lithographic patterns, although this is a poor metric for gauging the complexity of the fabrication process. Many blanket and self-aligned process steps are performed at the emitter and base lithography steps. The design of the emitter and base patterns written by the e-beam lithography system, and the alignment between the two layers, requires careful layout and planning.

The process starts with surface cleaning and blanket deposition of emitter contacts and metal stack. Lithography to define the emitter pattern is performed, and Cl_2/O_2 and SF_6/Ar inductively coupled plasma dry etches are used to transfer the photoresist pattern to a Cr etch mask and to etch the emitter contact. Once the emitter metal has been etched, a sidewall is formed by blanket plasma-enhanced chemical vapor deposition of Si_xN_y and ICP etch using a CF_4/O_2 chemistry. The semiconductor under the emitter is then etched with either a hybrid-dry/wet-etch or all-wet-etch process, stopping at the surface of the base semiconductor.

Two different base processes have been demonstrated: a blanket-sputtered, dry-etched base contact as well as a lifted-off base contact. For the lift-off process, lithography is performed, opening a window in the photoresist around each emitter. The surface is cleaned with dilute HCl, and either Pd/Ti/Pd/Au or Pt/Ti/Pd/Au metal contacts are e-beam evaporated. For the sputtered contacts, a process similar to the emitter formation is followed: surface preparation, Pd/W metal deposition,

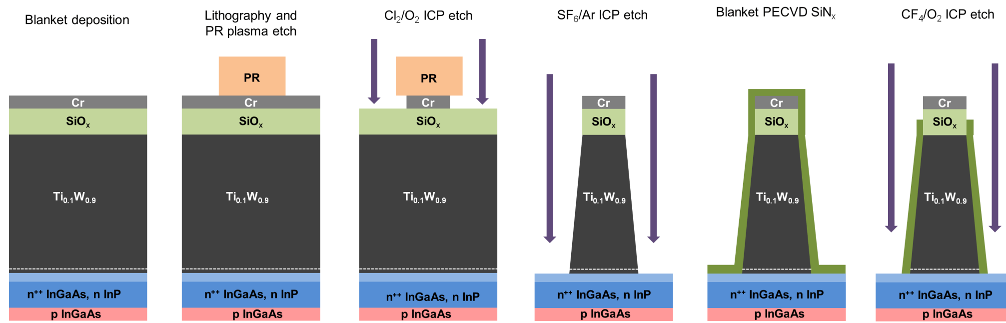


Figure 3.1: Emitter contact deposition and etch

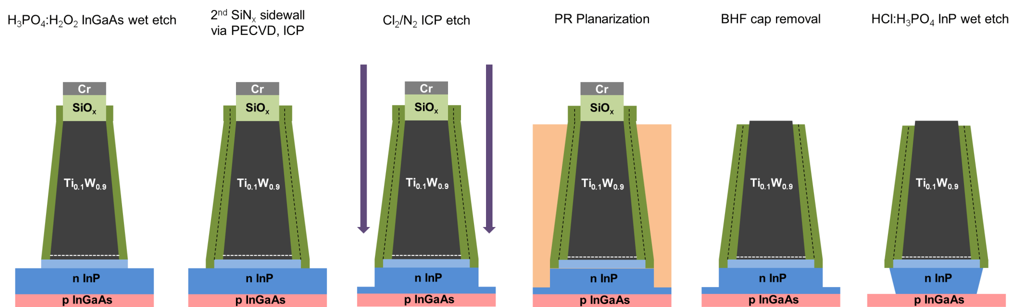


Figure 3.2: Emitter sidewall formation and mesa etch

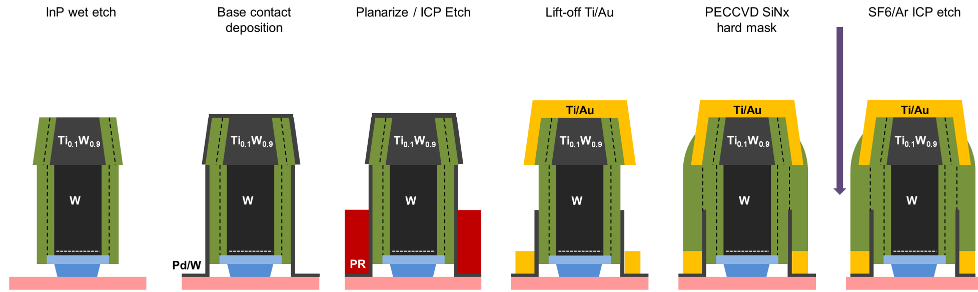
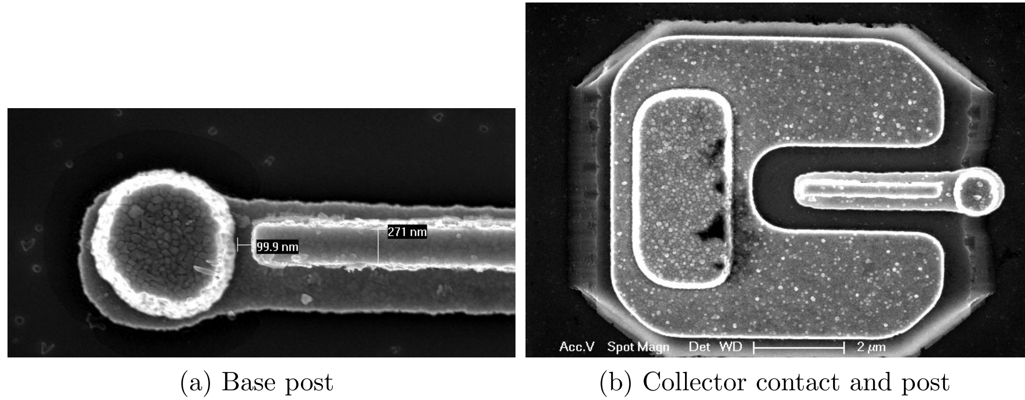


Figure 3.3: Sputtered base process flow

lithography and etch.

After base contact formation, a metal base post is lifted off at the end of the base contact to bring the base's electrical connection to the same height as that of the emitter. Base mesa lithography is performed, leaving a photoresist mask to protect the semiconductor of the emitter mesa while the base, grade, and drift collector are wet etched. This wet etch stops at the highly doped $In_{0.53}Ga_{0.47}As$ cap of the sub-collector.

Depending on which mask set is employed, the following two steps switch positions. The collector contact is formed through optical lithography, surface cleaning with dilute HCl, and liftoff of an e-beam evaporated Ti/Pd/Au metal stack. The transistor is then isolated by covering the entire structure with a photoresist mask and wet etching into the semi-insulating InP substrate. If there are no microstrip transmission line probe pads for the device, the collector contact is deposited prior to isolation etch, to minimize damage and contamination of the surface which could increase contact resistivity. If the mask set contains microstrip pads, the isolation etch is performed first, and the collector contact lithography is used to form two different structures: both collector contacts and ground planes for the transmission lines, deposited in the field on the semi-insulating material, are formed at the



(a) Base post (b) Collector contact and post

Figure 3.4: Lift off of (a) base post and (b) collector contact and post

same time. Increase in R_c due to these additional processing steps before contact deposition has been negligible in actual devices, due to both the high doping of the sub-collector and the large area of the collector contact.

After collector contact formation, a collector post is lifted off, similarly to the base post, bringing the emitter, base, and collector contacts to the same height.

At this point, the transistors have been fabricated, and are ready for encapsulation and passivation, and deposition of metal contacts. The sample is cleaned in dilute HCl and immediately coated with the spin-on dielectric benzocyclobutene. It is placed in an oven with an N_2 atmosphere, and is slowly brought from room temperature to 250 °C, where it is cured for an hour and then passively cooled. Once the BCB is hard baked on the sample, it is about 4 μm thick. It is then progessively ashed in a CF_4/O_2 plasma ash until the tops of the emitters, base posts, and collector posts are just above the BCB surface, but all other device features are covered. Because the emitter and base are self aligned, it is critical the tops of the emitters are exposed but the base contact is still covered, to prevent emitter-base shorts when the metal pads used to contact the emitter terminal are deposited on

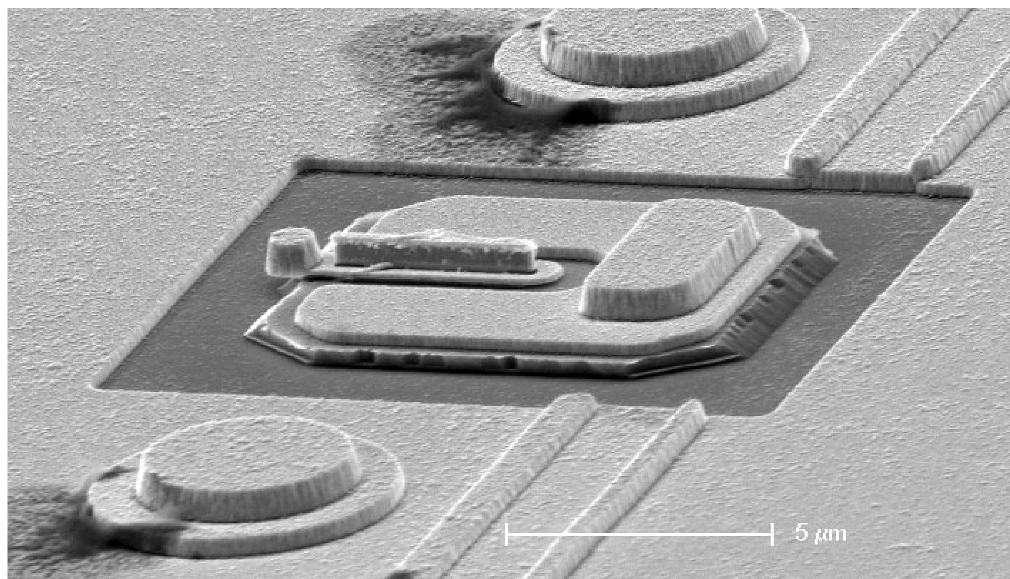


Figure 3.5: Finished transistor with microstrip ground plane and ground posts

top of the structures.

A layer of Si_xN_y is blanket deposited by PECVD on top of the sample, and a contact via lithography is performed, which opens up windows in the photoresist around each post. The Si_xN_y in the windows is dry etched using a CF_4/O_2 ICP etch, and the photoresist is removed. Finally, 1 μm Ti/Au/Ti contact pads are formed through liftoff and e-beam evaporation on top of the Si_xN_y, which acts as an adhesion layer for the pads, and device fabrication is complete.

3.2 Emitter Process Development

As the narrowest feature in the triple-mesa bipolar process, the emitter contact has the strictest requirements on junction dimensions, sustainable current densities, contact resistivities, and device yield. Because of this, a substantial amount of process development in this work has gone into developing narrow, low resistivity,

thermally stable contacts with high yield.

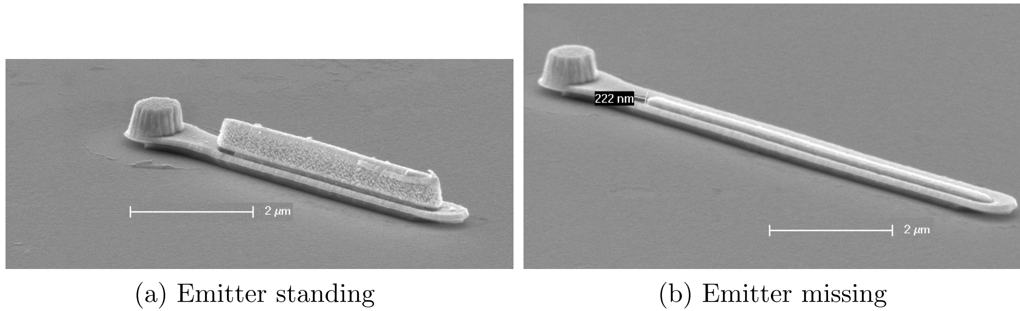
3.2.1 Emitter Contact Deposition

As bipolar transistors are scaled $\gamma : 1$ for increased RF performance, the required current density increases $\gamma^2 : 1$. For the devices described in this work, a HBT with emitter width $W_e = 64$ nm requires emitter current density $J_e = 36\ \frac{mA}{\mu m^2}$, as shown in Tabs. 2.1 and 2.2. These high current densities require contacts that are thermally stable and resist electromigration, making refractory metals such as W, Mo, and Ir, with melting points of $\sim$ 2700-3700 K, good candidates. The emitter contact resistivity required for a 64 nm HBT is less than 2.0 $\Omega \cdot \mu m^2$. We have found, irrespective of surface cleaning techniques, if the emitter semiconductor is exposed to photoresist prior to contact deposition, as in a lift-off process, the contact resistivity will be higher than this required value. Furthermore, liftoff is difficult with refractory metals due to the high temperatures at which they are evaporated, which often damages the photoresist. In addition to being thermally stable and low resistivity, the HBT emitter contacts used here must be formed in a process which can define sub-200 nm features, making lift-off defined by optical lithography, and optical lithographic definition of the contact pattern in any way, difficult.

The emitter contact processes investigated in this work were blanket-deposited $Ti_{0.1}W_{0.9}$, and Mo. $Ti_{0.1}W_{0.9}$ was sputter deposited due to the difficulty of reproducibly evaporating an alloy of two metals with such dramatically different melting points. Mo was e-beam evaporated, both *in-situ*, i.e. on epitaxially grown semiconductor without breaking vacuum, and *ex-situ*, deposited after breaking vacuum. Initial surface preparation techniques involving varying lengths of oxidation by UV-

Material	Deposition	*In/ex-situ*	Doping (10^{19} cm^{-3})	ρ_c ($\Omega \cdot \mu m^2$)
$Ti_{0.1}W_{0.9}$	Sputter	*Ex-situ*	5.0	1.82 ± 0.34
Mo	Evaporated	*Ex-situ*	5.0	1.5 ± 1.0
Mo	Evaporated	*In-situ*	6.0	1.1 ± 0.6

Table 3.1: N-type contacts to InGaAs

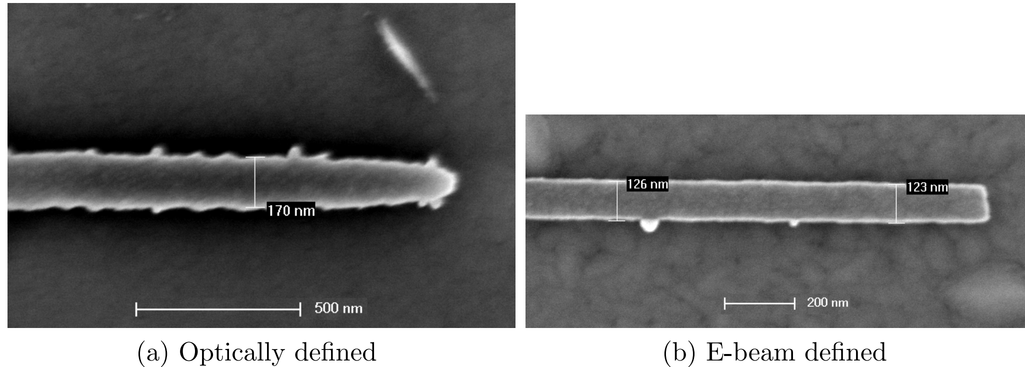


(a) Emitter standing (b) Emitter missing

Figure 3.6: Transistors after base post with (a) emitter intact and (b) emitter fallen off

O_3 and dips of varying length in either 1:10 HCl:H_2O or NH_4OH were analyzed. Contact resitivity strongly depends on semiconductor doping. *In-situ* contacts were deposited with an e-beam evaporator attached to the MBE growth chamber, and *in-situ* contacts with and without surface cleaning by H radicals under ultrahigh vacuum were also explored. The lowest reported contact resistivites, as determined through TLM experiments independent of actual transistor fabrication, are shown in Tab. 3.1 [4, 5, 6].

Transistors have been fabricated with sputtered W, sputtered $Ti_{0.1}W_{0.9}$, and evaporated Mo, both *in-* and *ex-situ*, as the emitter contact metal. The current process uses a 20 nm layer of *ex-situ* Mo topped by sputtered W and $Ti_{0.1}W_{0.9}$, which provides a medium between ease of fabrication and sufficiently low contact resistivity for the current device dimension. For smaller devices, *in-situ* deposition or further development may be required.



(a) Optically defined (b) E-beam defined

Figure 3.7: Emitter caps defined by (a) optical lithography and (b) e-beam lithography

3.2.2 Emitter Lithography

Emitter contacts in this work were defined either through optical i-line lithography or electron-beam lithography. E-beam lithography has the advantage of being able to uniformly and reproducibly write < 100 nm features, but the set up of mask files, system calibration, and write time is extensive. Optical lithography, while much easier to calibrate and faster to expose, is performed in the UCSB cleanroom using an i-line, or 365.4 nm wavelength source, which limits the minimum width of features to $\sim$ the wavelength of the source. To reduce the size of optically written emitters, after exposure and development using SPR-510 photoresist, the resist can be etched for several minutes in an O_2 plasma etcher. This isotropically etches the resist, making the resist features thinner, shorter, and narrower. This ashing process is limited by excessive thinning of the resist and undesired effect of pitting and notching the photoresist profile, making the edges non-uniform, as shown in Fig. 3.7a.

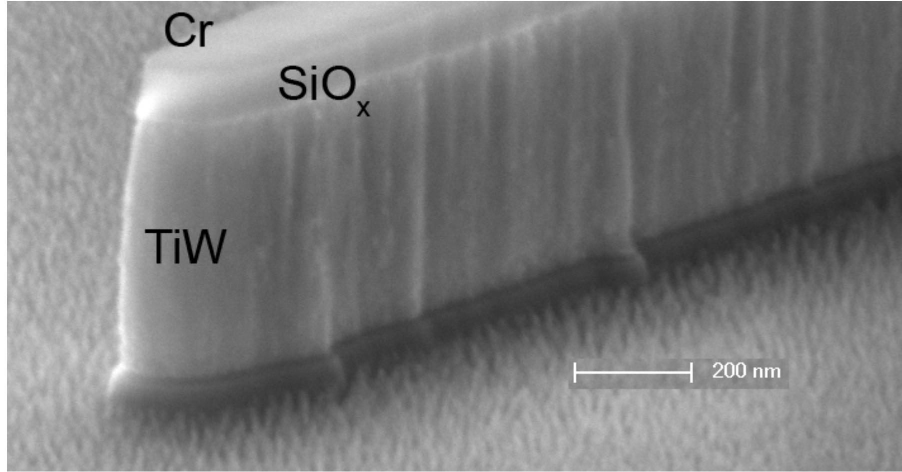


Figure 3.8: Emitter with Cr and SiO_x Cap

3.2.3 Emitter Etch Mask

In moving from lifted off emitter contacts to blanket-deposited emitter metal, a new process for defining the emitter pattern with lithography was developed. On top of the blanket sputtered emitter metal stack described in Sec. 3.2.5, 100 nm of SiO_x is deposited by PECVD at 250 °C. On top of this, 40 nm of Cr is e-beam evaporated. Lithography using positive photoresist, either optical or electron-beam lithography, is performed, leaving the resist in the pattern of the emitters, and the field to be etched clear. The Cr layer is then dry-etched using a sufficiently low-power Cl_2/O_2 ICP etch such that the Cr in the field can be completely removed without sputtering away the photoresist mask. Due to damage and chemical interaction with the dry etch plasma, the photoresist becomes difficult to remove with chemical processes like developer or photoresist strippers like 1165 or AZ-300T. After etching, the photoresist is removed by soaking in 1165 heated to 80 °C followed by a descum in a O_2 plasma etcher.

Once the emitter etch mask is formed, the exposed SiO_x in the field is removed

along with the $Ti_{0.1}W_{0.9}$ in the next ICP dry etch. The Cr etch mask and SiO_x layer beneath it are left in place through the rest of the emitter formation, prior to the final wet etch to the base surface. At this point, the entire sample is coated in photoresist ~ 1.6 μm thick – much thicker than the emitter height to ensure good planarity of the resist. The resist is then ashed back in an O_2 plasma etcher until it is about 200 nm shorter than the emitters. Next, the sample is placed in buffered HF to etch the SiO_x layer away, thereby lifting off the Cr etch mask. Finally, the ashed photoresist is removed through soak in photoresist stripper and a brief O_2 descum. The SiO_x layer and planarization process are necessary to remove the Cr etch mask because after the Cr is subjected to SF_6 plasma etches, its chemical composition changes, and it becomes both very electrically resistive and un-etchable with either standard Cr wet etch or dry etch chemistries.

3.2.4 Emitter Sidewalls and Low-stress Materials

The height of the emitter metal contacts used in this work are about 500 nm. This height is set by the need to establish a sufficient height difference between the emitter contact and base contact such that variation in the height of the spun on low-κ dielectric benzocyclobutene, used for back-end planarization, does not create an emitter-base short when metal contacts are deposited on the sample. Typical emitter contact dimensions used are 200 nm wide, 3 μm long, and 500 nm high – a high aspect ratio design where the emitter is essentially a thin sail shape. This design is mechanically unstable. When this is coupled with the use of refractory metals as the contact material, which are unreactive with the semiconductor surface compared to contacts with Ti or Pd at the interface, emitter contact yield drops through

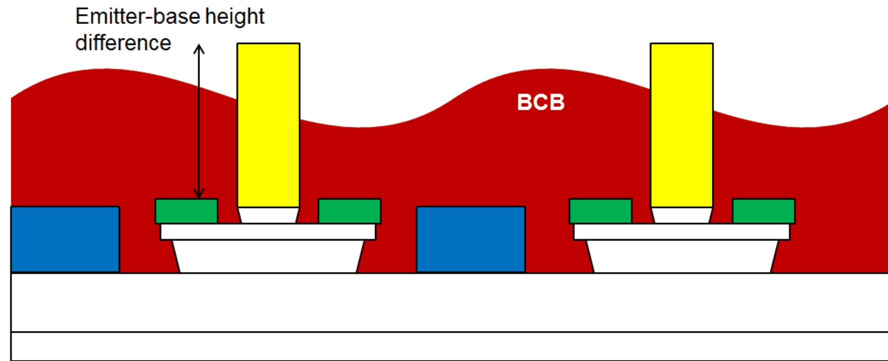


Figure 3.9: Variation in BCB height requires tall emitters

successive processing steps due to the emitters losing adhesion to the semiconductor surface.

A Si_xN_y sidewall process was developed to mechanically anchor the emitter in place, and to protect the emitter metal-semiconductor interface from being etched and damaged in subsequent fabrication steps. To form a sidewall, 30 nm of Si_xN_y is blanket deposited by plasma-enhanced chemical vapor deposition at 250 °Con the entire sample. The field is then etched using a low-power CF_4/O_2 inductively coupled plasma etch, calibrated to provide a 20% over-etch. This ICP etch is very anisotropic, and removes the Si_xN_y from all horizontal surfaces on the sample while reducing the thickness of the Si_xN_y on vertical surfaces by ∼20%, as verfied by transmission electron microscopy imaging.

In addition to using dielectric sidewalls to protect and anchor the emitter, a recipe for depositing low-stress sputtered metal films was developed. Stress in blanket metal films is measured using a stress measurement tool which measures the radius of curvature for a 2 in diameter Si wafer, before and after metal film deposition. Before actively working to reduce film stress, emitter contacts were typically sputtered $Ti_{0.1}W_{0.9}$ deposited with an Ar pressure of 20 mT. On Si test wafers,

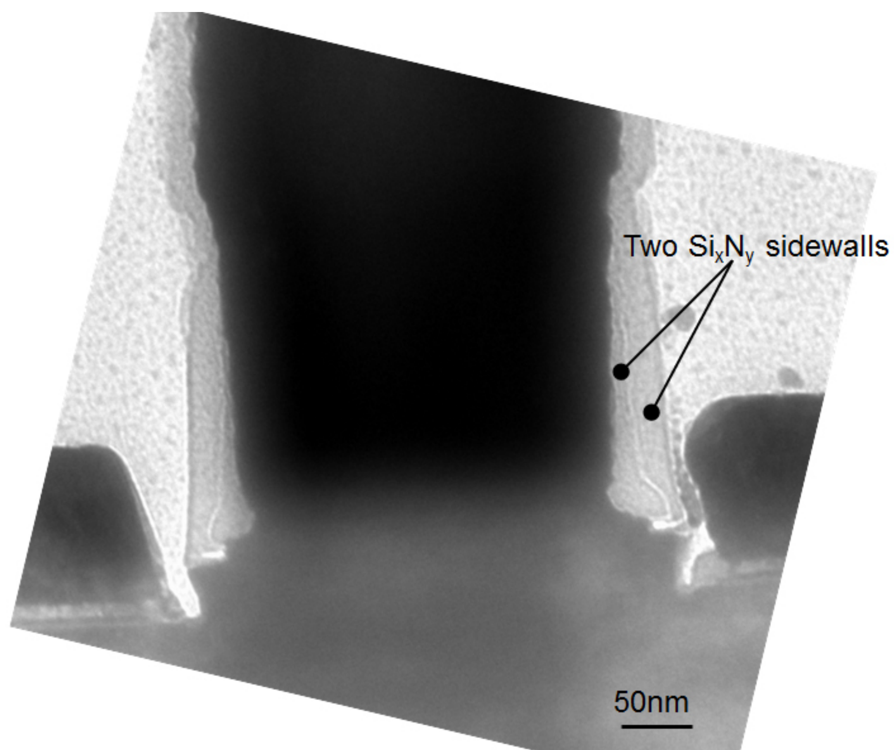


Figure 3.10: Dual emitter sidewalls are visible in TEM cross section

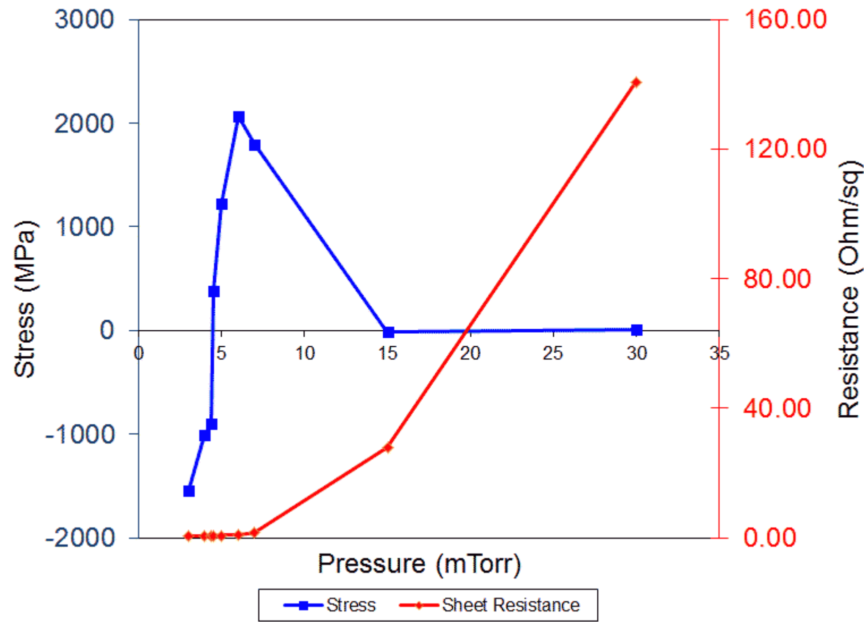
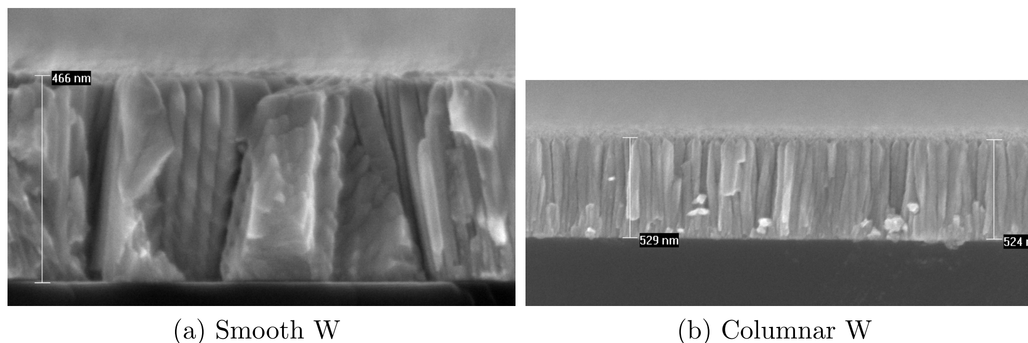


Figure 3.11: Stress and sheet resistance in sputtered W as pressure is varied

this would lead to stress in the $Ti_{0.1}W_{0.9}$ film of ∼1 GPa. A series of experiments varying pressure during deposition were conducted. As shown in Fig. 3.11, film stress is strongly dependent on pressure during deposition. At both low and high pressures, the stress goes to approximately zero, however, two different phenomena are responsible for these two different zero-stress states. In the lower pressure state, the film has the desirable qualities of having both low stress and low sheet resistance. In the high pressure state, the film is no longer a continuous film of metal, but instead forms vertical columns. This manifests itself in SEM imaging of the film cross-section or by dramatic increase in film sheet resistance. The pressure necessary to achieve the low resistance, zero stress state changes substantially from one deposition to the next, requiring lengthy calibrations immediately prior to deposition.



(a) Smooth W (b) Columnar W

Figure 3.12: Sputtered W deposited at two different conditions, leading to either (a) smooth or (b) columnar deposition

By decreasing the Ar pressure during $Ti_{0.1}W_{0.9}$ sputter deposition, the stress in the film was able to be approximately halved. By introducing a bilayer emitter stack of about 200 nm of W and 300 nm of $Ti_{0.1}W_{0.9}$, stress-free films were able to be developed on Si test wafers. Typically, one or two iterations of the W/$Ti_{0.1}W_{0.9}$ stack would be necessary, with slight adjustments to the pressures during deposition, to achieve stress less than 100 MPa in the test wafers. By using these lower stress films, emitter yield was dramatically increased. Using a bilayer emitter metal stack also had advantages in forming a vertical emitter profile, allowing the emitter semiconductor to be thinned.

3.2.5 Vertical Emitter Contact Etch Profile

Because the emitter contact height is constrained to be approximately 500 nm or taller, developing a vertical profile to the emitter contact is critical, for two reasons. First, the contact width is defined lithographically at the top of the contact — the more vertical the slopes of the contact, the more reliably narrow emitter-base junctions can be formed at the bottom of the contact. Second, a vertical contact facilitates the lift-off of the self-aligned base contact — a contact broader at the

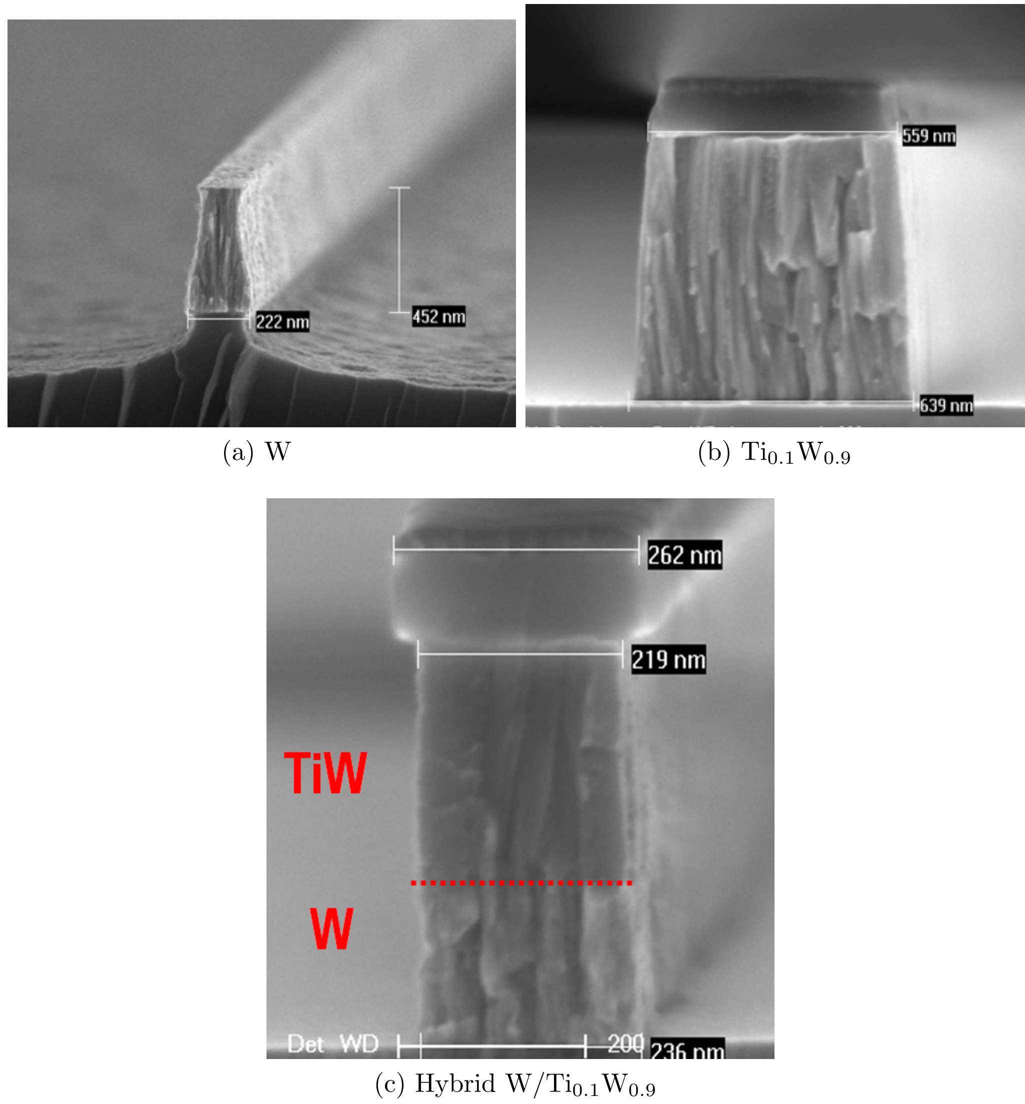
bottom than the top risks emitter-base metal shorts if a continuous film of base metal covers the entire emitter contact.

Metal contacts are blanket sputtered, and an etch mask of electron-beam evaporated Cr is deposited on top of it. The Cr is patterned through lithography, either optical or electron-beam, and dry etched in a low power Cl_2/O_2 ICP etch. The emitter contact metal, whether W, $Ti_{0.1}W_{0.9}$, or Mo, is also etched via ICP etch, using an SF_6/Ar etch chemistry. The profile slope of the contact depends on both metal species and etch conditions like power and pressure. In general, the higher the accelerating power during the etch, the more physical sputtering occurs in the etch, and the contact tends to be vertical or trapezoidal in cross-section. At low powers, chemical etching becomes more dominant, and the metal contact may take an hourglass or inverted triangle cross-sectional shape. $Ti_{0.1}W_{0.9}$ is a special case, due to its 10% Ti content by weight. Ti reacts with F from the plasma to form an unetchable compound on the sides of the emitter metal, making the contact broaden towards the bottom.

A second benefit to the $W/Ti_{0.1}W_{0.9}$ emitter metal stack developed for stress compensation is it allows a near-vertical emitter to be formed, with a small lip at the W-$Ti_{0.1}W_{0.9}$ interface, which facilitates base contact liftoff. This emitter is etched by using a high-power etch for the $Ti_{0.1}W_{0.9}$ layer, and a lower power etch for the W, which provides some undercut beneath the $Ti_{0.1}W_{0.9}$.

3.2.6 Controllable Emitter Semiconductor Etch

As the emitter contact width scales, etching the emitter semiconductor below it becomes more difficult. For devices at the quarter-micron or larger node, typical



(a) W

(b) $Ti_{0.1}W_{0.9}$

(c) Hybrid $W/Ti_{0.1}W_{0.9}$

Figure 3.13: Etch profile of (a) W, (b) $Ti_{0.1}W_{0.9}$, and (c) hybrid $W/Ti_{0.1}W_{0.9}$ emitter metal

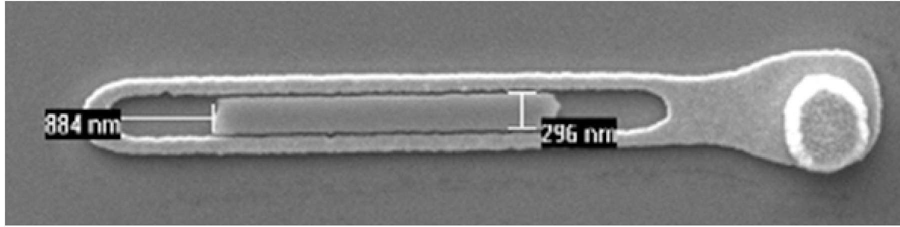
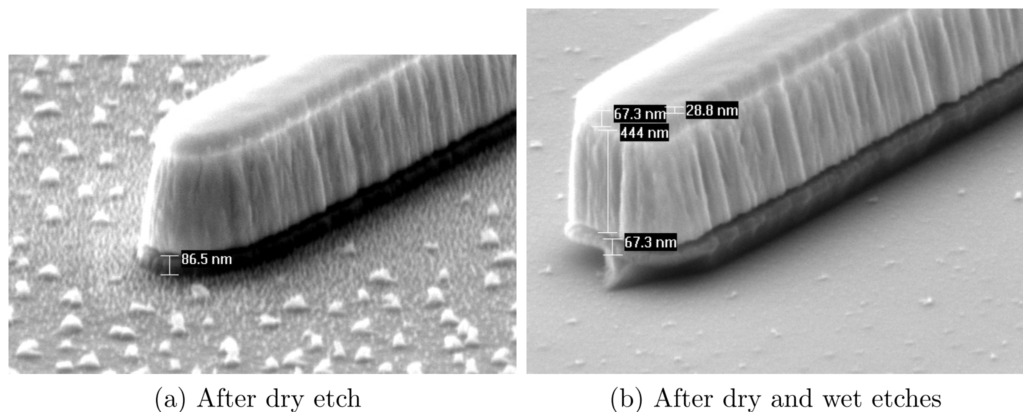


Figure 3.14: Transistor with emitter contact removed, exposing undercut of emitter semiconductor

emitter epitaxial designs consisted of $\sim$ 35 nm of heavily doped InGaAs, to make good n-type contacts, followed by $\sim$ 130 nm of InP of doping varying from $\sim 4\times10^{19}$ cm^{-3} to $\sim 8\times10^{17}$ cm^{-3} near the emitter-base junction to form the depletion region. After lift-off of the emitter contact, the semiconductor below would be wet etched, using a H_3PO_4:H_2O_2:H_2O 1:1:25 solution to etch the InGaAs, and a HCl:H_3PO_4 1:4 solution to etch the InP. These wet etches are isotropic: they etch laterally at least as much as they etch downward. In some crystallographic directions, they etch even more quickly laterally than vertically. The wet etch process does not scale for narrow emitters: the emitter-base junction size becomes uncontrollable, the emitter-base gap and gap resistance increase, and the semiconductor may be entirely etched away underneath the emitter contact.

To develop a controllable emitter etch, a hybrid dry and wet etch was developed. After forming the emitter contact, the semiconductor surface is cleaned with an NH_4OH solution and transferred immediately to the load-lock of an ICP etch tool. The emitter is etched by a low-power Cl_2/N_2 etch performed with the sample on a chuck at 200 °C. The Cl_2/N_2 etch has low selectivity between the InGaAs and InP, the etch is timed to etch through the entirety of the InGaAs emitter cap, and $\sim$ 70 nm of the emitter InP. After the etch, a short etch with Ar is used to clean the surface of $InCl_x$ compounds formed as a byproduct of the etch. As soon as



(a) After dry etch (b) After dry and wet etches

Figure 3.15: Hybrid dry/wet emitter semiconductor etch

the sample is removed from the low-pressure etch chamber, it is immediately rinsed in H_2O to further remove any etch byproducts remaining on the sample surface. The combination of the Ar sputter and H_2O rinse has been empirically found to be necessary to ensure the ability to uniformly wet etch the remainder of the emitter semiconductor.

The emitter dry etch etches the semiconductor with negligible undercut underneath the emitter contact. However, it is not selective between InGaAs and InP, making it infeasible to stop the etch precisely at the surface of the base. Furthermore, even the low-power etch causes damage to, and roughness of, the surface. For these reasons, the emitter etch is finished with the typical $HCl:H_3PO_4$ wet etch from the conventional process, albeit for a shorter time. By wet etching the bottom $\sim$ 50 nm of the emitter semiconductor, the damage and roughness from the dry etch is removed, and the etch stops on the epitaxial surface of the base, as is necessary for base contact deposition. The reduced duration and depth of the etch allow it to work with emitter widths at the 128 nm node.

While the hybrid dry and wet etch process allowed devices to be scaled below

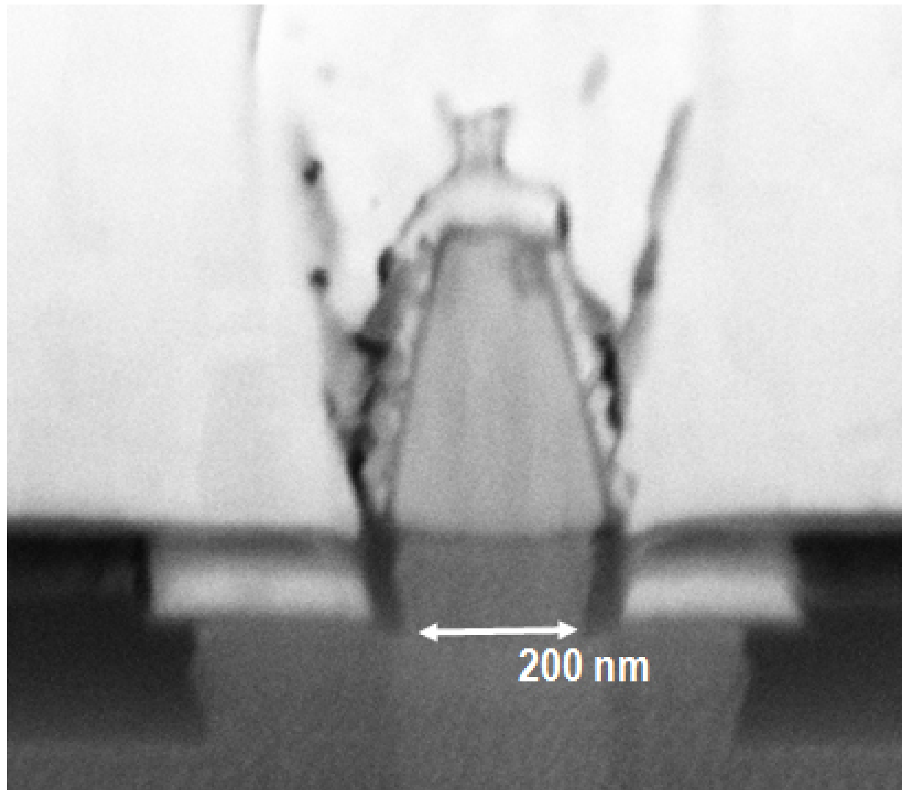


Figure 3.16: Hybrid dry and wet etch of the emitter semiconductor, with controllable undercut

256 nm while maintaining high yield, it added significant process complexity to the emitter fabrication process. When the two-layer W/$Ti_{0.1}W_{0.9}$
metal process described in Sec. 3.2.5 was developed, an ancillary benefit was the fact the emitter semiconductor was no longer constrained to be thicker than the base contact. Previously, the undercut at the emitter contact-emitter semiconductor interface was used to prevent the self-aligned base metal from forming a continuous layer over the emitter contact, the undercut at the W-$Ti_{0.1}W_{0.9}$ interface in the contact now served the same purpose. The emitter semiconductor was thinned from $\sim$ 160 nm to a 10 nm InGaAs cap and a 35 nm InP layer in future designs. These thin layers have the advantage of being entirely wet etchable even at sub-100 nm device dimensions, with controllable undercut.

3.3 Base Process Development

As device widths are narrowed and epitaxial layers are thinned, the base contact process requires modification. To minimize base resistance, the base contact should be two-sided, i.e. on both sides of the emitter, and each side should be about a transfer length $L_T \equiv \sqrt{\frac{\rho_c}{R_{sh}}}$ wide. Any narrower, and base resistance R_{bb} increases due to current not having sufficient width to spread under the base contact. Any wider, and C_{cb}, which is proportional to base width W_b, will increase. Either effect increases $\tau_{cb} = R_{bb}C_{cb,i}$ and reduces f_{max}. For typical base dopings and layer thicknesses, this leads to the proper base contact width to be 1-1.5 $\times$ the emitter width. As emitters are scaled below 100 nm through electron-beam lithography, the base may also need to be defined through e-beam lithography – not because the total base mesa width of $\sim$ 500 nm is too narrow to be optically defined, but because the

Figure 3.17: $W/Ti_{0.1}W_{0.9}$ emitter contact enables thin emitter semiconductor layers

maximum tolerable misalignment between the base and emitter layers becomes $<$ 50 nm when each side of the base contact is on the order of 100 nm wide. In addition to strict alignment tolerances for the base contact, as the base semiconductor is thinned, thermally stable contacts to the base are required to minimize how deep into the semiconductor the metal sinks, which can increase the base resistance.

3.3.1 Electron-beam Lithography for the Base

An e-beam lithography process for the base using UV-6 photoresist has been developed. After spinning this resist, its thickness in the field is $\sim$ 200 nm. The height of the emitter contact and emitter mesa is about 3 times taller than this, leading to a sloping resist profile around the features, as shown in Fig. 3.18. Since the areas being patterned and developed are immediately in the vicinity of the emitter, this thickening of the resist must be taken into account when calculating the necessary electron dose to be delivered during exposure. Windows as small as 200 nm wide can be opened in this photoresist by e-beam lithography, sufficiently narrow to form the base contacts for HBTs with 64 nm emitters.

In addition to developing a photoresist process, good alignment between the emitter and base layers must be insured. This can be helped by coating the photoresist in the commercial polymer aquaSAVE, which forms a conductive layer on top of the photoresist to minimize charging from the electron beam. Frequent system calibrations and placement of many alignment marks within each die are also critical.

Similarly to the base contact layer, the base mesa pattern, designed to protect the emitter-base semiconductor junction during the wet etch of the base-collector

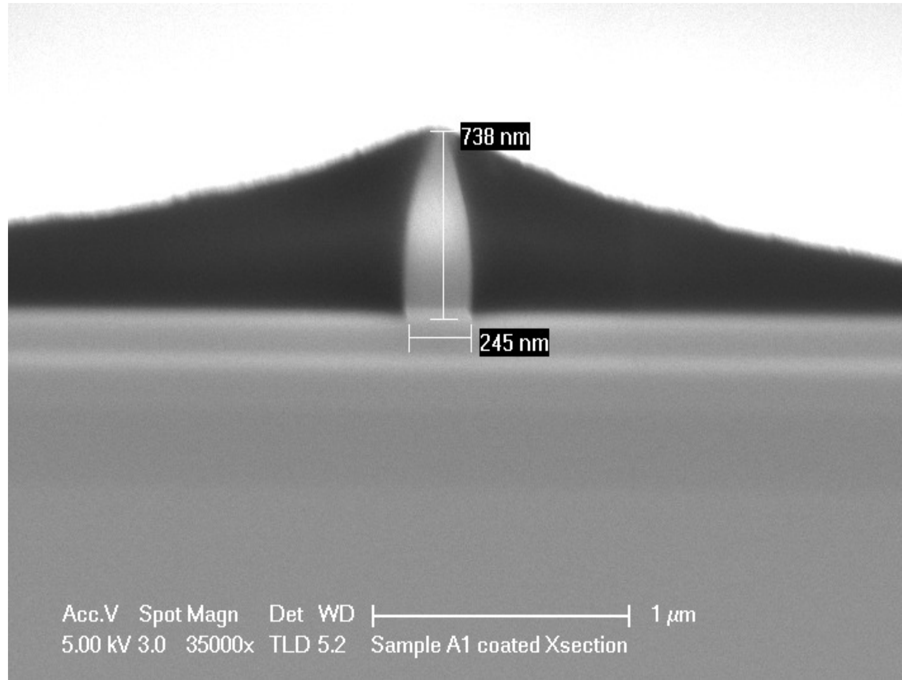


Figure 3.18: UV-6 photoresist spun around emitter structure

junction, can be defined with electron-beam lithography to improve alignment of this layer. Processes using a thicker version of the mAN-2400 resist used for the emitter write are used for this layer.

3.3.2 Refractory Base Contacts

Similar to the work done in n-type Ohmic contact research, a series of transmission line model experiments were carried out on 100 nm thick p-InGaAs, and p-type contacts using refractory metals deposited both *in-situ* and *ex-situ* were formed. Ir and Mo contacts were prepared *in-situ*, and Mo and W contacts were prepared *ex-situ* [7, 8, 9]. The surface preparation for all samples involved oxidation by UV-O_3 and cleaning with HCl:H_2O 1:10 immediately before placing under vacuum for deposition. No hydrogen cleans were used on *in-situ* contacts, due to the tendency

Material	*In/ex-situ*	Doping (10^{20} cm $^{-3}$)	ρ_c ($\Omega \cdot \mu m^2$)	ρ_c post-anneal
Ir	*In-situ*	1.5	1.0 ± 0.6	1.2 ± 0.7
Ir	*Ex-situ*	1.5	1.5 ± 0.9	1.8 ± 0.9
Mo	*In-situ*	1.1	2.0 ± 0.8	2.5 ± 0.9
W	*Ex-situ*	1.6	0.55 ± 0.69	1.90 ± 1.19

Table 3.2: P-type contacts to InGaAs

of H radicals to passivate the base doping. Brief exploratory experiments with sputtered contacts for the base yielded non-Ohmic behavior, possibly due to the sputtering process creating n-type defects in the semiconductor. Like in the n-type experiments described in Sec. 3.2.1, strong dependence on sample doping was seen. Unlike the n-type contacts, significant increases in contact resistivity are seen after annealing the TLM structures at 250 °C for 1 hr in a N_2 environment identical to the bake used to cure BCB in the transistor back-end process.

There is a very strong dependence for contact resistivity on the active carrier concentration in the material. For the ex-situ W p-type contacts listed in Tab. 3.2, record low contact resistivities were developed at dopings in excess of 1×10^{20} cm^{-}3. For lower dopings, the contact resistivity increases as shown in Fig. 3.19.

3.4 Transistor Back-end Processes

Substantial effort has been put into developing new emitter and base process techniques. The back-end (post-base contact) processes are similar to those described in previous works [1]; for components less critical to obtaining high f_τ and f_{max}, like collector contact size and deposition methods, the same processes have been maintained out of simplicity. Many changes to the back-end processing have been done to increase reproducibility and reliability.

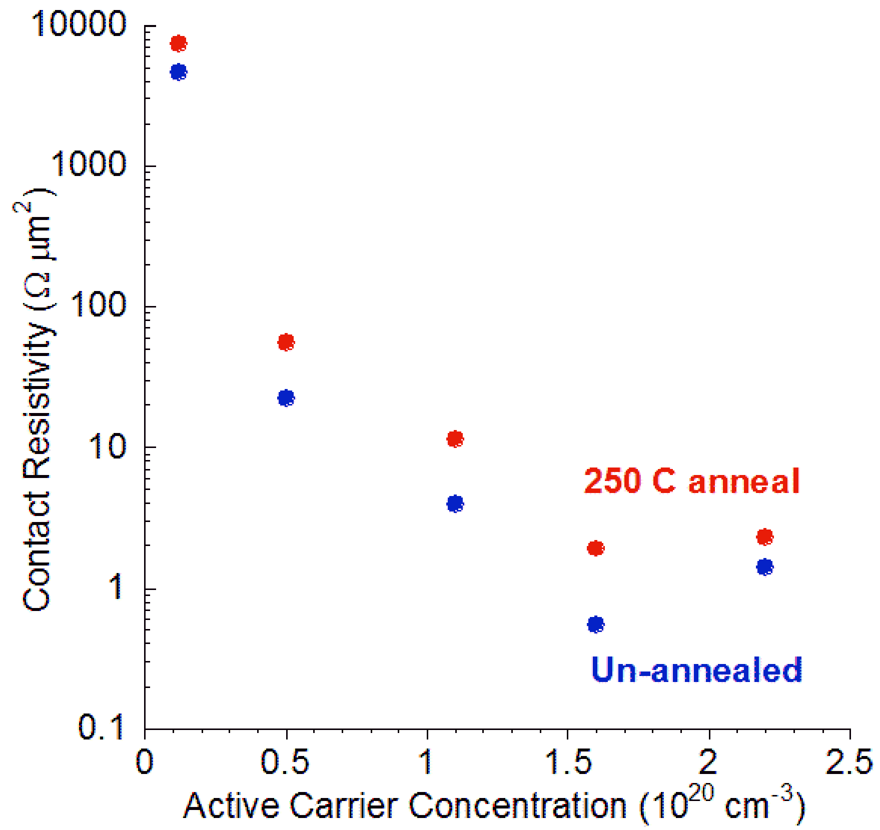


Figure 3.19: Contact resistivity vs. active carrier concentration with ex-situ W p-type contacts

3.4.1 Surface Preparation

Results for both n- and p-type contacts have shown lower contact resistivities with 1:10 $HCl:H_2O$ soaks prior to contact deposition compared to NH_4OH soaks. Before all metal depositions, be it contacts or posts, an $HCl:H_2O$ soak is used instead of NH_4OH. UV-O_3 has been found to be unnecessary before contact post depositions.

3.4.2 Base Post

The size and alignment of the base post are critical: if the post is wider than the base contact, or misaligned to extend over the edge of the contact, the base mesa area will increase, and therefore so will base-collector capacitance C_{cb}. However, electron-beam lithography is difficult to use for the base post, since it must match the emitter in height, requiring a liftoff of $\sim$ 500 nm. In addition, the thick ($\sim 2\mu$m) negative optical resists used for the collector contact and post layers cannot be used for the base post layer, as the posts are 800 nm $\times$ 800 nm, too small to be resolved in the thick photoresist. To assist in the liftoff of these small features in thinner photoresist, a bilayer lithographic process is used, incorporating a layer of LOL 1000 beneath the photoresist. The LOL is not photosensitive, so exposure times remain the same as without it, but a longer develop is used. This longer develop does not significantly change the size of the opening at the top of the resist, but does dissolve the LOL beneath the resist, creating an inverted-T shaped structure as shown in Fig. 3.20. This bilayer process facilitates the liftoff of the base post in two ways: it makes the overall photoresist higher, creating a larger gap at the top between metal and photoresist, and provides more space at the bottom of the photoresist opening – both these increased resist areas allow photoresist stripper to move in

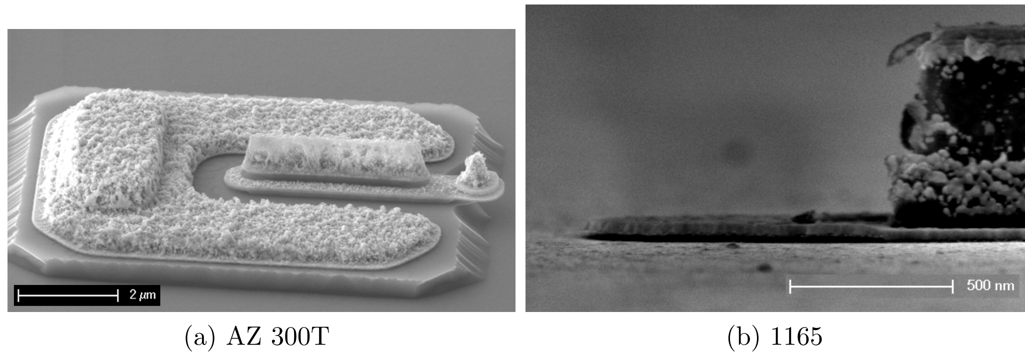
Figure 3.20: Cross-section of photoresist and LOL after exposure and development

more quickly and remove the photoresist.

In previous results, the base post metal stack had the same Pd/Ti/Pd/Au layers as in the contact, with a thicker Au layer. This was done to avoid potential diffusion of Ti diffusing into the semiconductor in case of post-contact misalignment so severe that some post material would be deposited directly on the base semiconductor surface. Deposited Pd or Pt on top of the Au of the base contact did not adhere well, and many posts peeled off during the lift off process for the post. Due to reduction in the lithographic misalignment, current processes rarely see base posts not deposited entirely on base contact, and the aggressive wet etches of the semiconductor beneath the post are probably sufficient to prevent shorts due to gross post misalignment. Because of this, Ti/Au posts have recently been used, increasing the metal-metal adhesion and post yield to $\sim$ 100%.

3.4.3 Photoresist Removal

Several proprietary photoresist strippers are available in the UCSB nanofab, the most commonly used being Shipley Microposit Remover 1165 and AZ 300T Photoresist Stripper. AZ 300T has been previously demonstrated to attack metal contacts, including Au, when samples were placed in it for extended periods of time.



(a) AZ 300T (b) 1165

Figure 3.21: Metal being attacked by (a) 300T and (b) 1165 (at the interface)

Even 1165, while lacking the alkalinity of 300T, has been demonstrated to attack refractory metals like W and Mo when samples are placed in 80 °C 1165 for more than 1 hr. To minimize the amount of time samples spend in stripper, techniques like LOL 1000 bilayers are used in conjunction with vertical and upside down sample mounts to facilitate quicker liftoff. AZ 300T is no longer used at any point in HBT processing. 1165 is heated to 80 °C in a water bath, and samples are placed in the hot stripper for as brief a duration as possible to remove photoresist or induce metal liftoff.

3.4.4 BCB Cure

As one of the final steps in the back-end process, the sample is coated in a low-κ dielectric called benzocyclobutene, which serves to passivate the device and form a planar surface upon which the metal probe pads are deposited. The BCB is spun on as a liquid, and hardens in a 1 hr cure at 250 °C. During the cure, it is important the sample is both level, to insure uniform BCB thickness, and not in contact with other surfaces at the edges of the sample, so the BCB at the edges does not bond the sample to its holder as it cures. Previously, bent Al weighing dishes had been

Figure 3.22: Mount for BCB cure

used to mount samples for the cure, but these were difficult to manually reshape each time. To replace these, an Al mount 3 inches in diameter with many small pins of equal height protruding from it was designed and machined. The sample rests on these pins during the cure.

3.5 Transmission-line Model Structures

Contact resistivity experiments are carried out by fabricating transmission-line model structures on UCSB grown epitaxy. The semiconductor layers are grown by solid-source MBE on semi-insulating InP substrates with (100) orientation. A 100 nm undoped $In_{0.52}Al_{0.48}As$ buffer layer is grown first, then a 100 nm layer of $In_{0.53}Ga_{0.47}As$. For n-type experiments, the samples are doped with Si, and for

p-type, the dopant is C, from a CBr_4 source. Peak active carrier concentrations for n-type layers are $\sim 6 \times 10^{19}$ cm^{-3}, and hole concentrations in excess of 2×10^{20} cm^{-3} have been realized.

Before deposition, the sample surface may be prepared in several different ways, as described in Secs. 3.2.1 and 3.3.2 — typically an oxidation of the surface with UV-O_3, followed by a dilute HCl rinse to remove all oxides from the surface. XPS analysis of sample surfaces before and after UV-O_3 show a reduction in C on the sample surface, indicating the UV-O_3 treatment may remove hydrocarbon compounds from the semiconductor surface, while at the same time promoting oxide growth. XPS analysis before UV-O_3 and after dilute HCl dip show comparable oxygen levels, indicating the HCl removes oxides formed by the UV-O_3, whereas NH_4OH dips do not reduce the oxygen concentration on the surface as completely [4].

Contact metal is deposited via either e-beam evaporation or sputter deposition. 20 nm of refractory metal is deposited. Mo films of 10 nm were previously explored, but the contact resistivity was found to increase after thermal stress or after several weeks' time. Mo and other refractory films have a somewhat columnar structure when deposited, and very thin films may have gaps where the semiconductor surface is exposed. 20 nm films show greater stability over time, and are the standard process used in TLM experiments [10].

On top of the blanket deposited refractory metal, contacts of 20 nm Ti, 500 nm Au, and 40 nm Ni are lifted off using photoresist patterned by i-line stepper lithography. The Ti serves as an adhesion layer, the thick Au layer reduces the metal resistance associated with the pads, and the Ni is an etch mask. The refractory metal in the field is etched using a low-power SF_6/Ar ICP etch. Finally, a second layer of

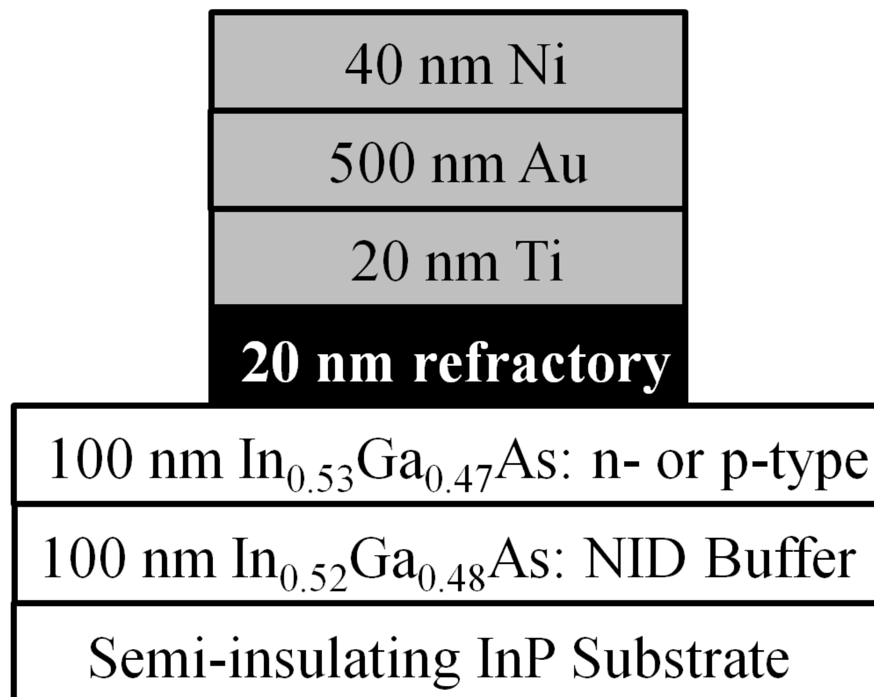


Figure 3.23: Cross-section of TLM pad structure

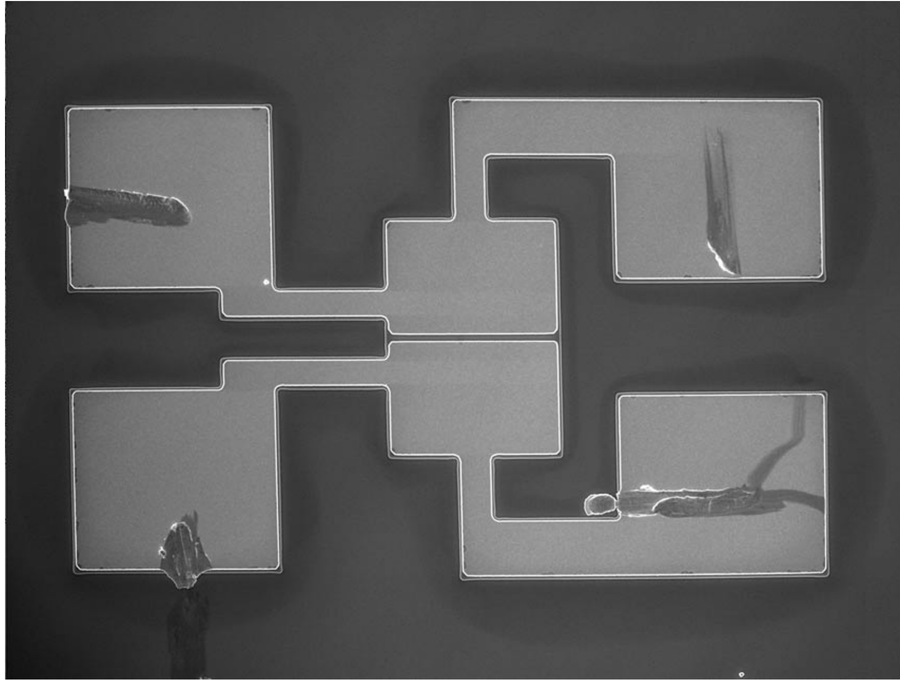


Figure 3.24: Top view of TLM pad structure formed through metal liftoff and wet etch

photoresist is placed over the gap, and the field is wet etched down to the undoped InAlAs layer, isolating the TLM structures. The completed structures have the form shown in Fig. 3.24, where the dark field is the semiconductor substrate and the light colored area is lifted off metal pads. Resistance is measured across the gap between the two pads.

3.6 Conclusions

In this section the fabrication process flows for forming InP mesa HBTs and transmission-line model structures are presented. For TLM processing, the key issues are developing processes to accurately extract very low contact resistivities. This largely depends on the design of the TLM structures and proper measurement technique,

but critical fabrication techniques include defining narrow gaps for more accurate contact resistivity extraction and depositing thick Au contact layers to reduce the influence of metal resistance on the measurement.

For the bipolar transistors, record bandwidths are achieved through epitaxial and lateral scaling of the devices. The lateral scaling is achieved through the development of sophisticated process techniques emphasizing sub-100 nm feature formation and alignment. Techniques like plasma dry etches, blanket deposition of metals and dielectrics, and e-beam lithography have proved critical to scaling devices. In general, as junctions narrow, devices become more high aspect ratio, and device reliability and yield become lower. This can be mitigated at least partially by developing more complex calibration and verification processes: e.g. doing etch rate tests or dummy sputters to calibrate sputtered film stress, or conducting two-part dry etches and inspecting the sample via electron microscopy before completing the dry etch. For future scaling, processes that reduce the aspect ratio, like shortening contact height and thinning device epitaxy, are desirable.

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Chapter 4

Device Measurement

Both the DC and RF measurement techniques used for the devices fabricated in this work will be described in this chapter. Transmission Line Model structures, used to extract contact resistivity and sheet resistance of ohmic contacts, are analyzed using four-point voltage and current measurements with a Semiconductor Parameter Analyzers. For HBTs, the Semiconductor Parameter Analyzer is used to obtain Common-Emitter and Gummel plots, and is also used to provide DC bias during RF measurement. Transistor high-frequency performance is measured with two-port S-parameter measurements on a Network Analyzer. The HBTs described in this work are contacted by one of two styles of pads – either a lumped element coplanar structure, or a microstrip transmission line contact. The calibration and measurement procedure followed depends on which type of transistor structure is being analyzed.

4.1 Coplanar Pad Transistors

The majority of transistor measurements in this work were made on devices in lumped pad structures with coplanar signal and ground, patterned in a Ground-

Signal-Ground layout. The pads are formed through 1 μm thick metal liftoff after transistors are formed and passivated in benzocyclobutene. The total pad width is 250 μm, and they support probes of pitch 75 μm – 150 μm.

4.1.1 Off-wafer Calibration

For any network analyzer system, there are intrinsic and systematic errors in measurement that arise from hardware imperfections in the network analyzer, the frequency dependent behavior of cables, probes, and the non-ideality of on-wafer structures. For two-port measurements a general network analyzer model with eight error terms has been established [1]. These errors are determined through one of many calibration processes. Essentially, all calibrations are conducted by measuring S-parameters for a chosen set of structures, from which the error terms can be calculated.

For transistors in the coplanar pad structure, a two-part calibration is used to bring the reference plane of measurement to the device under test. First, an off-wafer, Line-Reflect-Reflect-Match calibration using commercially available Impedance Standard Substrates from Cascade Microtech is conducted, bringing the reference plane to the tips of the probes. This removes the phase shift and dissipative losses associated with the network analyzer, cabling, and probes. Second, an on-wafer calibration takes into account the errors associated with the pad structures.

The LRRM calibration method was developed as an improvement to the Short-Open-Line-Thru and Line-Reflect-Match calibration techniques. It is supported in Cascade Microtech's WinCal software. LRRM has a couple advantages over these other calibration methods: SOLT requires precisely defined calibration structures,

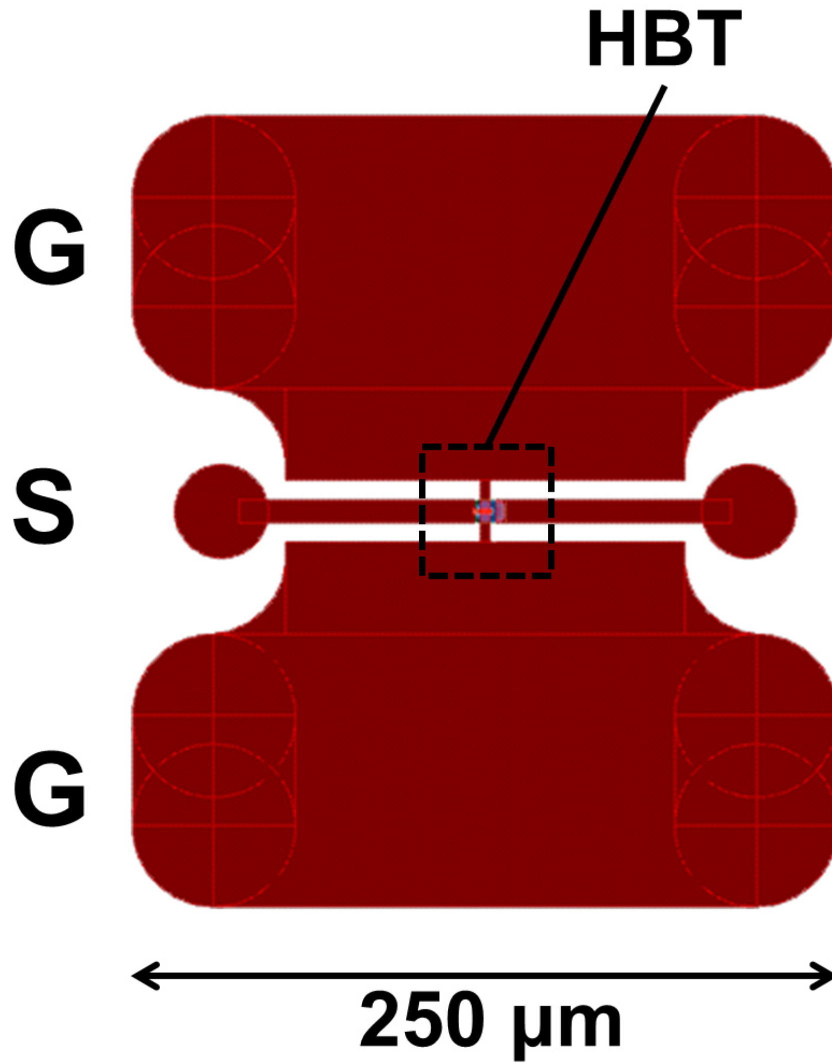


Figure 4.1: Schematic of GSG coplanar transistor pad structure

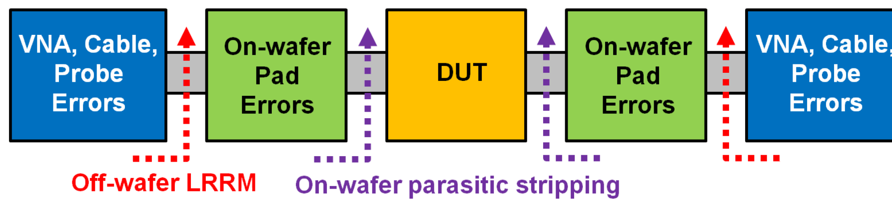


Figure 4.2: Two-part calibration to move reference plane to transistor terminals

and is several times more sensitive to probe placement reproducibility than LRRM [2]. LRRM requires a one-port "match" measurement instead of two-port, like LRM, which reduces errors due to probe structural variation or placement between the two probes [3]. LRRM calibrations require only a precisely defined resistance for the "match" standard and a known "thru" delay. The "open" and "short" standards need to only be electrically different than each other, unlike in the SOLT calibration method [4, 5].

Two GSG probes are connected to the network analyzer using semi-rigid coaxial cable. Measurements are carried out with the sample sitting on a thick ($\sim$ 2 cm) ferrite block to minimize resonances. The four calibration structures on the Impedance Standard Substrate are measured first. Two-port measurements are made on two different reflect standards: nominally a "short" and an "open." Typically, the "short" calibration structures are thin metalized strips electrically connecting the ground and signal pins of each probe, and the open is measured by lifting the probes >250 μm in the air above the ISS. Two-port measurements are carried out on the line standard as well, which is usually a short ($\sim$ 200 μm) coplanar waveguide transmission line. One-port S-parameters are measured for a matched load. On Cascade ISSs, these are 50 Ω resistors, laser-trimmed after deposition to achieve the desired DC resistance within 0.3 Ω.

The off-wafer calibration has the advantage of relying on commercially fabricated calibration standards, which saves space in each transistor die, and eliminates any error due to process variation in the fabrication of the calibration standards. A single calibration can be used from $<$ 1 GHz – 100 GHz, unlike the on-wafer Thru-Reflect-Line method described below in Sec. 4.2.2. This is useful for device parameter extraction and equivalent circuit modeling. However, because the cal-

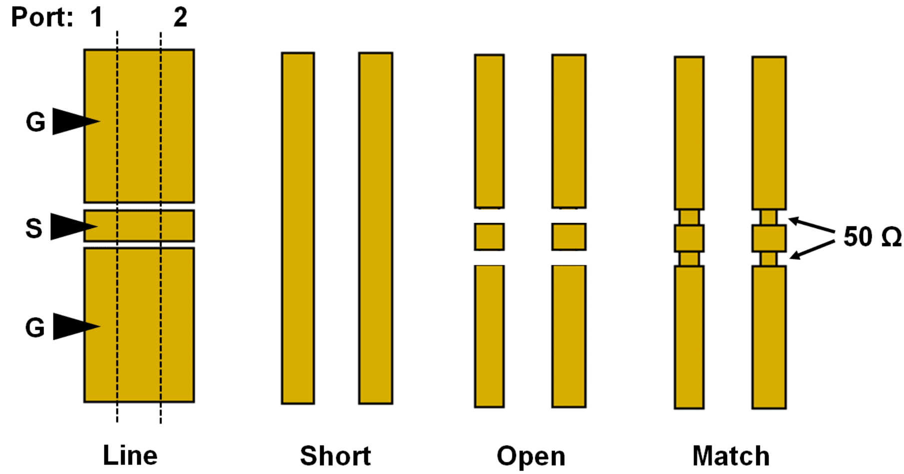
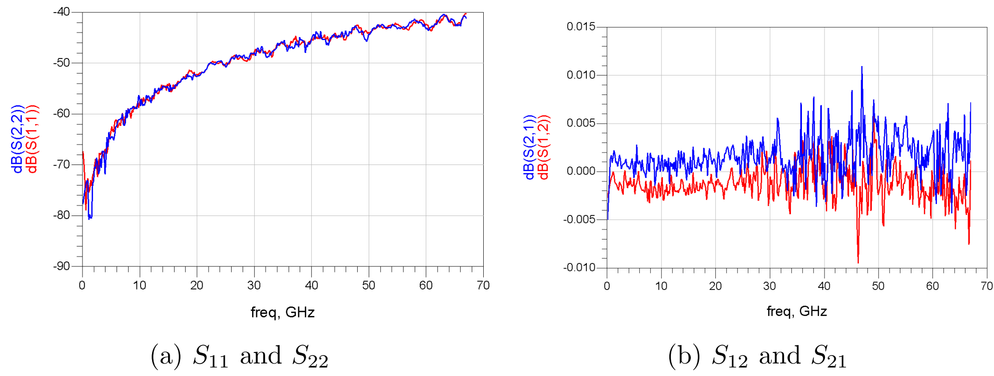


Figure 4.3: Calibration standards for LRRM calibration (Open optional)

ibration substrate and the structures on it are very different than the on-wafer structures, errors in the calibration start becoming substantial above $\sim$ 75 GHz, at which point other, on-wafer, calibration techniques become better options.

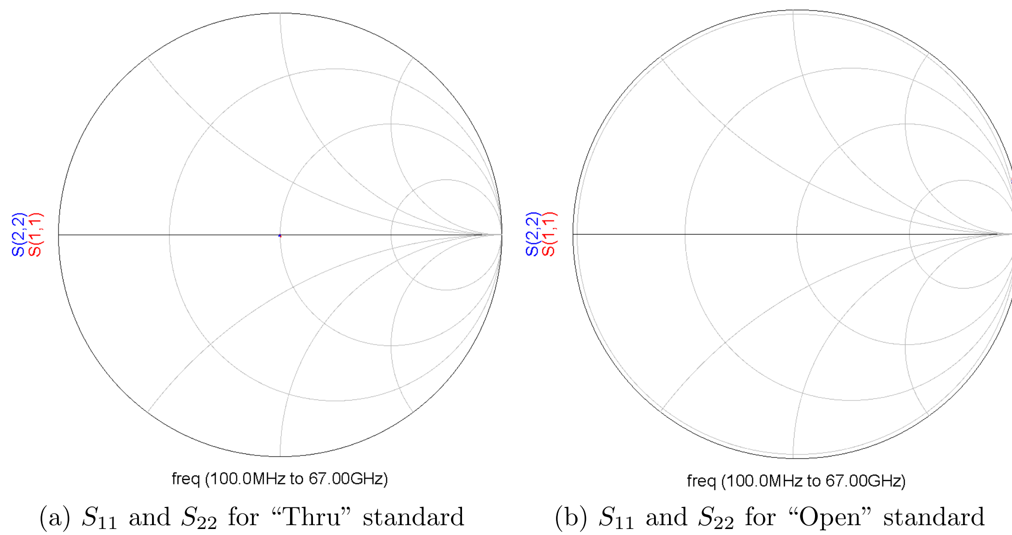
4.1.2 Calibration Verification

After performing the calibration, it is verified by re-measuring the calibration standards, and comparing measured data to their ideal counterparts' S-parameter behavior. In a LRRM calibration, typically the "line" is measured last, so the calibration can first be verified on the "line" without lifting the probes. It is then measured after lifting and replacing the probes, as are the two "reflect" and "match" standards. Typically when using a commercial ISS at low frequency ($<$ 75 GHz), the calibration verification looks very clean, as shown in Figs. 4.4 and 4.5. However because the calibration is conducted off-wafer, above $\sim$ 75 GHz, actual measured data can be noisy.



(a) S_{11} and S_{22} (b) S_{12} and S_{21}

Figure 4.4: Calibration verification on "Thru" standard for (a) reflected and (b) transmitted power



(a) S_{11} and S_{22} for "Thru" standard (b) S_{11} and S_{22} for "Open" standard

Figure 4.5: Calibration verification in Smith chart representations of reflected power for the (a) "Thru" and (b) "Open" calibration standards

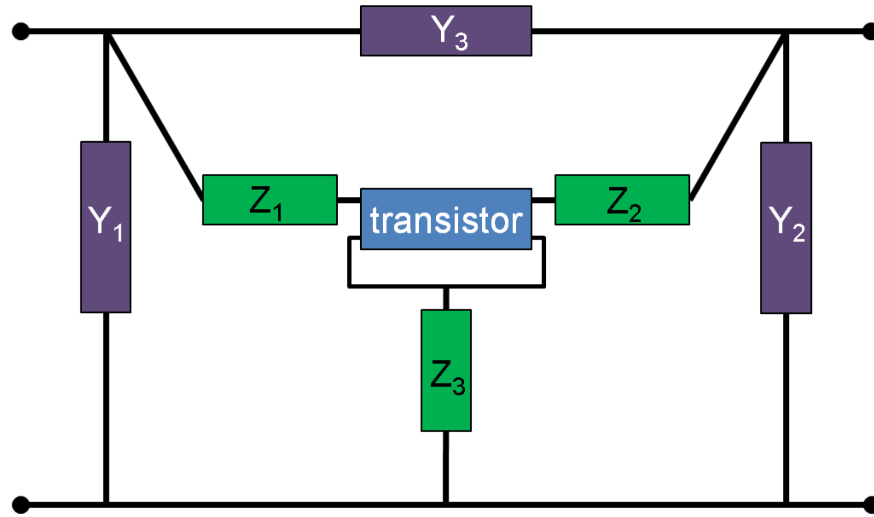


Figure 4.6: Equivalent circuit for transistor and pad parasitics

4.1.3 Pad Parasitic Removal

While the off-wafer LRRM calibration brings the reference plane to the probe tips, the actual transistor is still embedded in a pad structure much larger than the device itself, as shown in Fig. 4.1. These pads add both series and parallel resistances and reactances to the measured transistor data, as shown in Fig. 4.6. These terms are stripped off after S-parameter measurement using measurements of on-wafer dummy pad structures. On each die of a HBT sample, several dummy "open" and short" pad structures are also formed. The "open" is identical to the actual pads used to contact a transistor, albeit with the transistor removed — instead of being connected to the base and collector posts of a transistor, the ends of the two signal lines are not electrically connected to anything. The "short" standard simply connects the two signal lines to each other, and to the ground plane.

An equivalent circuit model of the "open" pad consists of the parallel parasitic elements from the pad structure, while the equivalent circuit model of the "short"

pad consists of both the parallel and series elements shown in Fig. 4.6. Actual device characteristics are obtained by first measuring S-parameter data for a transistor structure as well as the two dummy structures, and then converting from S- to Y-parameters. Through nodal analysis of the two-port network, the parallel parasitic elements can be simply subtracted off the measured data.

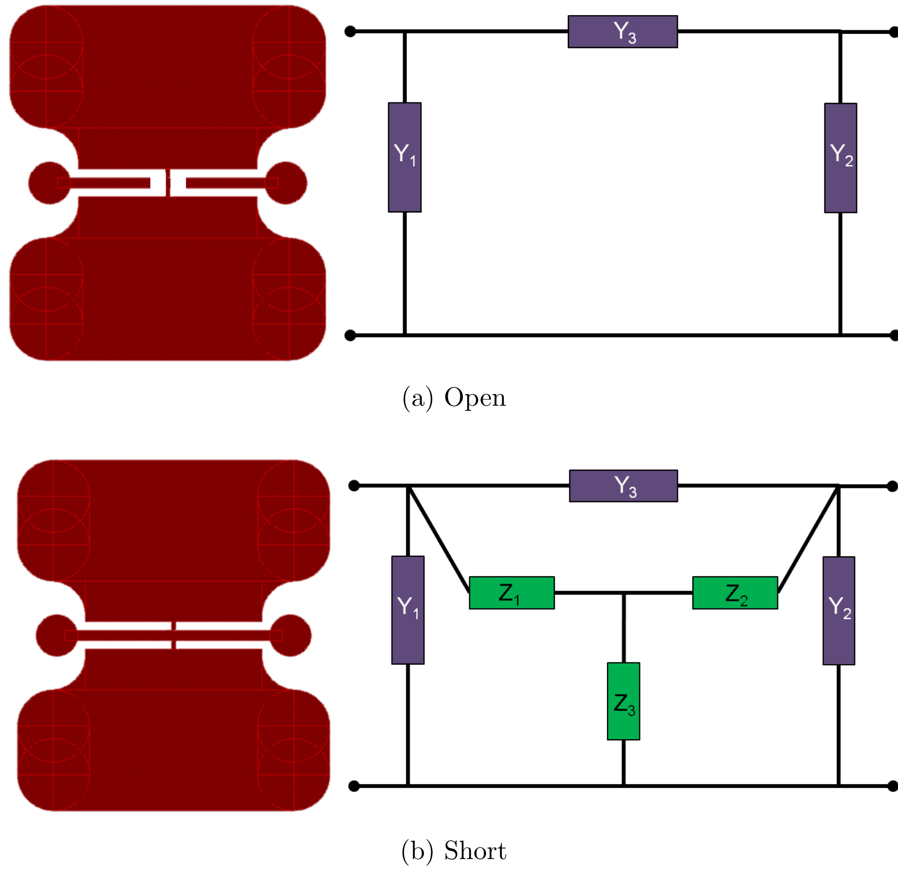
$$Y'_{trans} = Y_{meas} - Y_{open} \tag{4.1.1}$$

where Y_{meas} and Y_{open} are measured two-port Y parameters of the form $Y = \left(\begin{smallmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{smallmatrix}\right)$, and Y'_{trans} are the calculated Y parameters describing the transistor and the series parasitic elements within which it is embedded. For many devices, this step of the pad stripping may be sufficient to obtain accurate transistor data, however, for the devices described in this work, with low input impedance and high transconductance, the series impedances of the equivalent circuit are comparable, and must be extracted as well [6].

The series impedances in the device are most naturally considered as Z-parameters, and can be calculated by the difference in the measurements for the two dummy pad structures.

$$(Y_{series})^{-1} \equiv \begin{pmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{pmatrix} = (Y_{short} - Y_{open})^{-1} \tag{4.1.2}$$

where the Z-terms are described in Fig. 4.6, and Y_{short} are the measured Y parameters for the dummy "short" structure. Using both Eqs. 4.1.1 and 4.1.2, the



(a) Open

(b) Short

Figure 4.7: Pad layouts and equivalent circuits for (a) Open and (b) Short calibration structures

transistor Y parameters can be determined.

$$Y_{trans} = \left((Y'_{trans})^{-1} - (Y_{series})^{-1} \right)^{-1} = \left((Y_{meas} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \right)^{-1} \tag{4.1.3}$$

One disadvantage to the pad parasitic stripping is there is no rigorous calibration verification that can be conducted. Each die contains two or more copies of each dummy "open" and "short" structure, and these are measured immediately before and immediately after a transistor measurement, and are compared against each other for consistency and to increase the confidence in the calibration. Proper pad

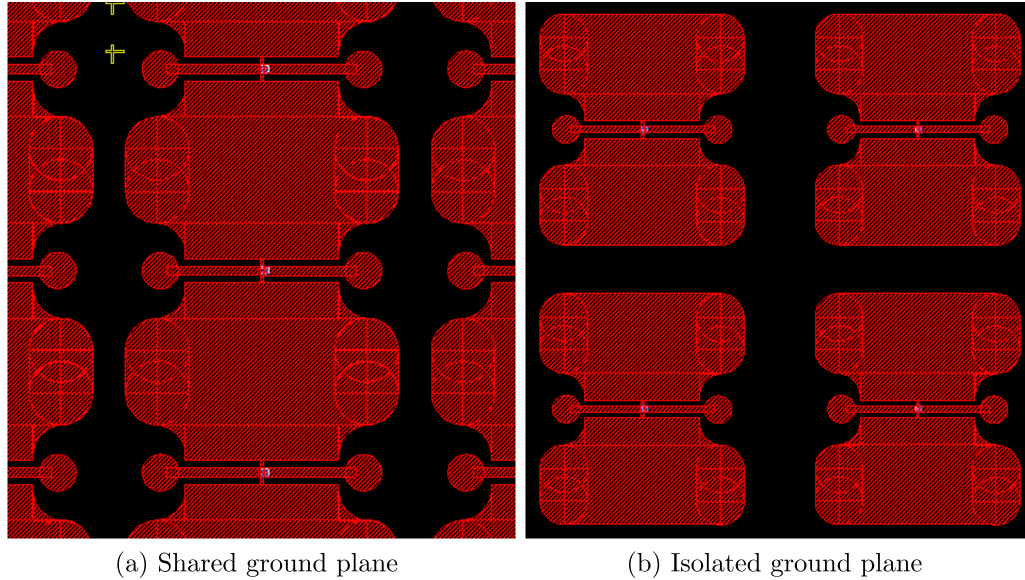
parasitic removal is paramount for accurate estimation of f_{max}. While, by definition, Mason's Unilateral Gain, and therefore, f_{max}, are invariant for any reactive network within which an active device is embedded [7], the series impedances in actual transistor measurements have real part on the order of 900 mΩ at 67 GHz [8]. These dissipative elements reduce extrapolated f_{max} by almost 50%.

4.1.4 Isolated versus Shared Ground Plane

To maximize the number of transistors in each die, the coplanar pad structures have been implemented in a "shared ground plane" arrangement of columns, as well as individually isolated devices, as shown in Fig. 4.8. In the shared ground plane devices, the "open" and "short" standards are also embedded in the column of devices to replicate the pad environment seen by an actual device. Comparison of embedded and de-embedded RF data for these devices shows substantial difference between the two structures: Mason's Unilateral Gain is substantially noisier in the shared ground plane structures, as shown in Fig. 4.9. This is likely due to parallel plate resonances associated with each type of structure, proportional to

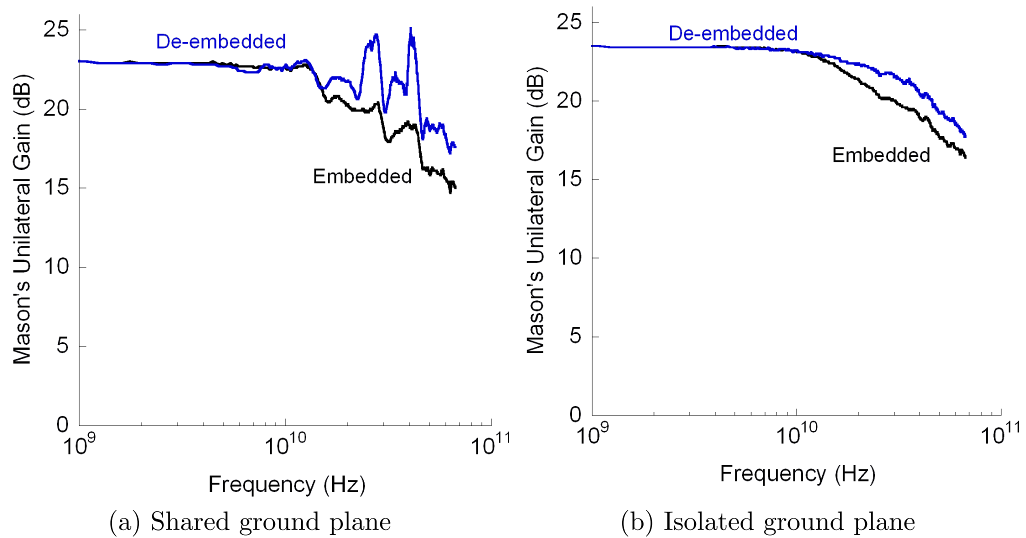
$$f_{res} \sim \frac{c}{2nL} \tag{4.1.4}$$

where c is the speed of electromagnetic wave propagation in the pad media, $n = 1, 2, 3, \ldots$ is an integer multiplier, and L is the dimensional length of the structure. For the isolated pad structures, $L \sim 100\mu$m, and for the shared pad structures, $L \sim 1$ mm. The much smaller physical dimensions of the isolated pads push the resonances associated with them above the frequency band of measurement.



(a) Shared ground plane (b) Isolated ground plane

Figure 4.8: Comparison of coplanar pad structures with (a) shared and (b) isolated ground planes



(a) Shared ground plane (b) Isolated ground plane

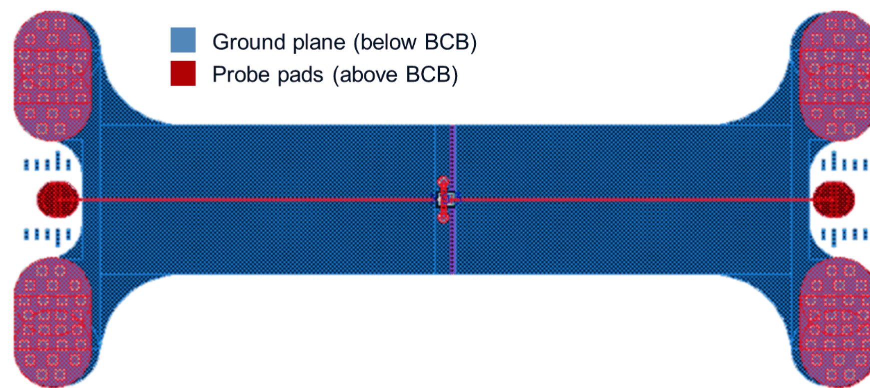
Figure 4.9: Comparison of Mason's Unilateral Gain for coplanar pad structures with (a) shared and (b) isolated ground planes

4.2 Microstrip Transmission Line Transistors

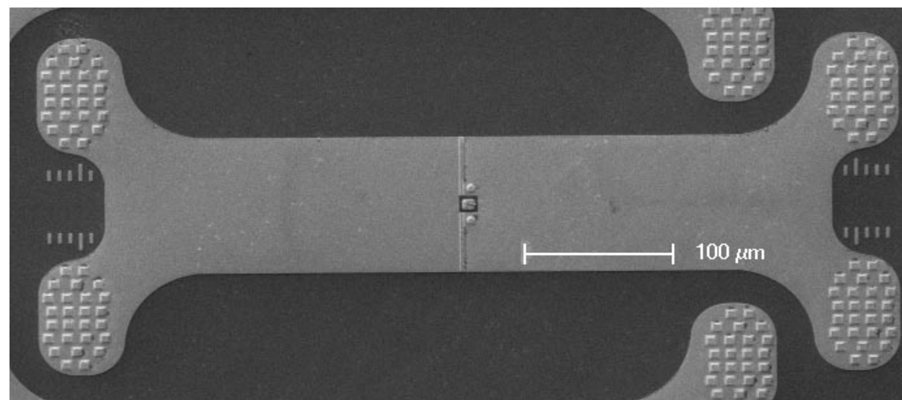
The second type of pad structures used on UCSB HBTs are microstrip transmission line structures. Like the coplanar structures, the microstrip lines are designed in a Ground-Signal-Ground configuration, supporting the same range of probe pitches. The microstrip transmission lines are twice as long as the coplanar signal lines, at 500 μm. They are designed using a two-dimensional E&M simulator to have a characteristic impedance of $Z_0 = 50\Omega$ characteristic impedance. Because of these characteristics, the microstrip lines have a more well defined reference plane at the transistor posts, and can be treated more rigorously as transmission lines than the coplanar structures. A one-step, on-wafer calibration can be used to bring the reference plane of measurement to the device. Since the calibration is performed on-wafer, it is usable to higher frequencies than the off-wafer calibration, although the lines themselves are much more sensitive to process variation than commercial standards.

4.2.1 Transmission Line Fabrication

The microstrip transmission line contacts are formed through several fabrication steps. The pattern used for the collector contact liftoff contains both collector contacts, as well as microstrip ground planes surrounding each transistor mesa. The device isolation etch is performed prior to collector deposition. The collector contacts are deposited on top of the device mesas, while the microstrip ground planes are simultaneously deposited in the field, which has been etched down to the semi-insulating substrate. While it would be preferable to form completely continuous ground planes surrounding the actual devices, lift-off processes fail for



(a) Pad layout



(b) Fabricated pads

Figure 4.10: Microstrip transmission line pads in (a) design and (b) fabrication (prior to Metal 1 deposition)

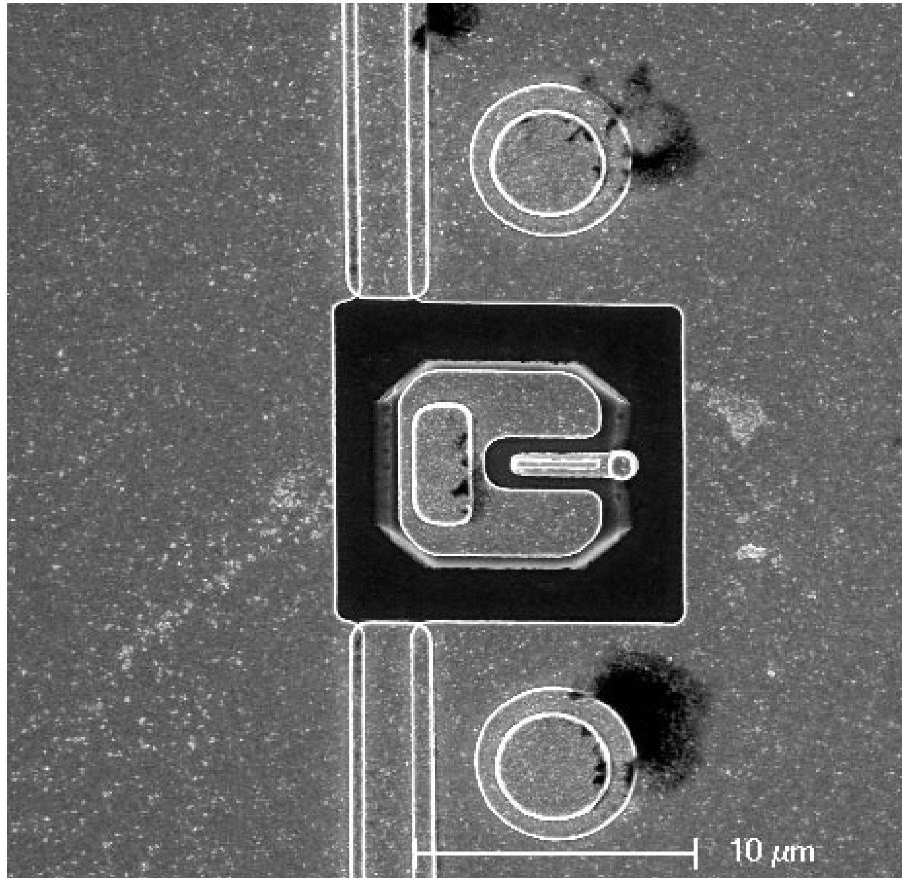


Figure 4.11: Transistor surrounded by microstrip ground plane and posts

fully enclosed holes. For this reason, the ground planes are lifted off with a break across their width, perpendicular to the signal line. This gap is covered with a second ground post lift off, thick enough to come to the same height as the collector contact. Finally, during the collector post liftoff, collector posts are deposited on top of the collector contacts as well as on the ground posts, bringing both the collector terminal and ground plane into electrical contact with the metal 1 patterns deposited after BCB planarization.

4.2.2 Thru-Reflect-Line Calibration

The on-wafer calibration performed with the microstrip transmission line style contacts described in this work is called a "Thru-Reflect-Line" calibration, after the three calibration standards that are required: a "thru" line of zero electrical length, a "reflect," and a "line" of some non-zero length. TRL calibration has two advantages over SOLT or LRRM calibration: it requires only three calibration standards instead of four, reducing the space on each die necessary for calibration structures. Further, none of the calibration structures need to be precisely defined, like the reflects in SOLT, or the "match" standard in LRRM. The "thru" is defined to be a line of zero electrical length, the "reflect" standard is required only to have nonzero reflection, and the "line" standard's length does not need to be known prior to calibration, provided it is not exactly a half-wavelength longer than the "thru".

By measuring these three standards, three separate sets of two-port S-parameters are obtained, and from these the error terms associated with entire cascading system of network analyzer, cables, probes, and on-wafer pads can be determined [9]. While the dimensions and properties of the TRL standards do not need to be precisely known prior to calibration, they must be consistent and reproducible: the characteristic impedance and dissipation of all lines should be the same, and for each "reflect" standard, the reflection coefficient should be identical when measured from either port. Lithographic variation in feature dimension, as well as variation in the thickness of the spin-on dielectric between signal and ground plane, will reduce the quality of the calibration.

Each transistor die contains four different microstrip transmission line structures. Each transistor is contacted on one side by a 250 μm microstrip line con-

nected to the base post, and a mirror image of the line on the other side connected to the collector post. The "thru" standard is these two microstrip lines directly connected together to form a single 500 μm line. The TRL algorithm defines the reference plane as the midpoint of this structure. Several different "line" structures are included on the die to cover a range of frequencies from 1 to 500 GHz. Each line length is designed around a certain frequency at which it is exactly a quarter wavelength, and it can be used to calibrate over a frequency range where its phase difference with the "thru" ranges from 20° to 160° [10]. The "open" consists of the two end pieces, separated by an additional section of ground plane, with no signal line, while the "short" connects the signal lines from each end piece to the ground plane through post structures. Because the quality of the calibration depends on the identical behavior of the "reflect" at both ports, the "short" standard, with its fabricated ground post, has been found to give more reproducible calibrations than either the on-wafer "open" standard or a reflect measured by lifting the probes above the sample, due to the variations in radiative behavior of these "open" structures.

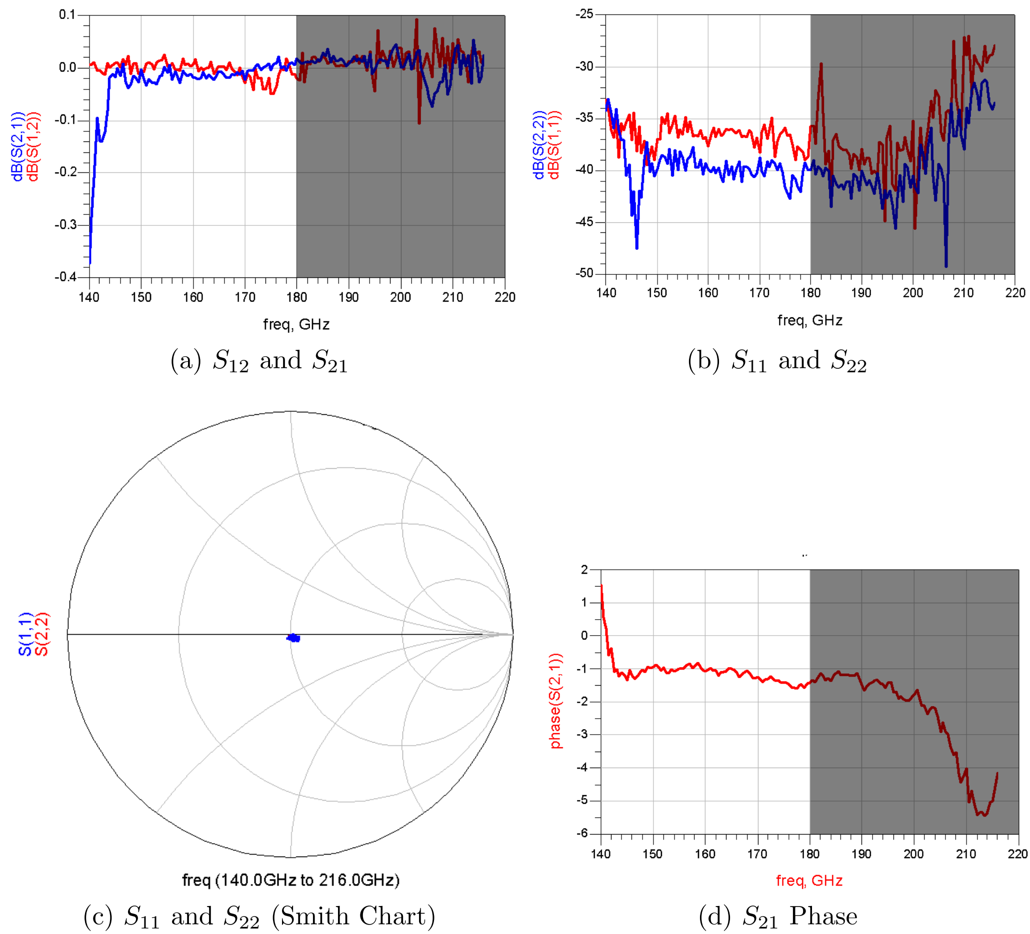
4.2.3 Calibration Verification

After performing the calibration, it needs to be verified by re-measuring the calibration standards, and seeing if they behave as their ideal counterparts should. In a Thru-Reflect-Line calibration, typically the "thru" is measured last, so the calibration can first be verified on the "thru" without lifting the probes. It is then measured after lifting and replacing the probes, as are the "line" and "reflect" standards. As the frequency range of measurement increases, the amount of error due to probe placement, seen as a phase shift in the "thru," increases. This has made

clean measurements in the WR-03 band (220-325 GHz) difficult to obtain.

The quality of calibration obtained from these microstrip calibration standards is limited by their high resistance. The microstrip line process implemented for these transistors was designed so it could be fabricated without any additional process steps beyond those required for the coplanar pad structure fabrication. Because of this, the thickness of the microstrip dielectric is tied to the overall transistor height, at $\sim$ 800 nm. To obtain transmission lines with characteristic impedance of 50 Ω on this thin dielectric, a comparatively thin line 1.7 μm wide must be used. Previous transistor results utilized a more complex back-end process and inverted microstrip lines with $\sim$ 3 μm of dielectric between ground plane and signal line, allowing for wider, less dissipative lines [11]. Similar processes could again be employed to achieve better high-frequency calibrations.

A calibration verification on the "thru" standard in the WR-05 band (140-220 GHz) is shown in Fig. 4.12. An ideal "thru" will show 0 dB for S_{12} and S_{21} at all frequencies — all energy flowing into one port will flow out the other. The reflectance terms, S_{11} and S_{22}, should be infinitely low in the ideal case, as no energy is reflected back. Typically, $S_{xx} < -35$ dB and $|S_{xy}| < 0.1$ dB is the standard necessary for a good calibration. In Fig. 4.12, the quality of the calibration above $\sim$180 GHz is insufficient to extract reliable device data from measurements. This is indicated in the increase in noise above this frequency in the Gain vs. Frequency plots, but also clearly in the Phase vs. Frequency plot of S_{21}, which sharply deviates above 180 GHz. When plotted on a Smith Chart, S_{xx} should ideally be a pinpoint dot in the center of the chart.



(a) S_{12} and S_{21}

(b) S_{11} and S_{22}

(c) S_{11} and S_{22} (Smith Chart)

(d) S_{21} Phase

Figure 4.12: Calibration verification on "Thru" standard of (a) and (c) transmitted power, (b) reflected power, and (d) phase

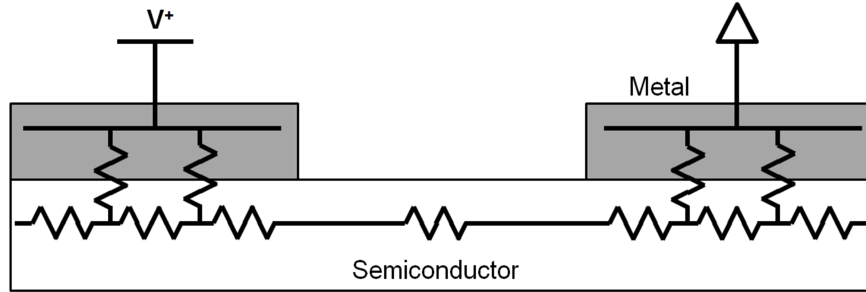


Figure 4.13: Transmission line model of planar Ohmic contact

4.3 TLM Measurement

The Transmission Line Model for Ohmic contacts is called such because a planar metal contact to semiconductor can be modeled as a two-dimensional array of resistances. Solving for the voltages and currents at different nodes of the array leads to solutions similar to in form to the solutions for the transmission line equations, albeit without reactive elements since all measurements are at DC [12].

4.3.1 TLM Extraction Procedure

Each TLM structure consists of two metal pads, separated by a gap, deposited on the semiconductor surface. Resistance is measured for several different gap spacings. Each measured resistance can be broken into two parts, with the form

$$R_T = \frac{R_{sh,gap} d_{gap}}{W} + 2R_c \tag{4.3.1}$$

where the first term is the resistance associated with the gap between the two pads, and $R_{sh,gap}$ is the sheet resistance of the semiconductor in the gap. The R_c in the second term is the contact resistance, which includes bulk metal contact resistance, the interfacial resistance between metal and semiconductor, and the spreading re-

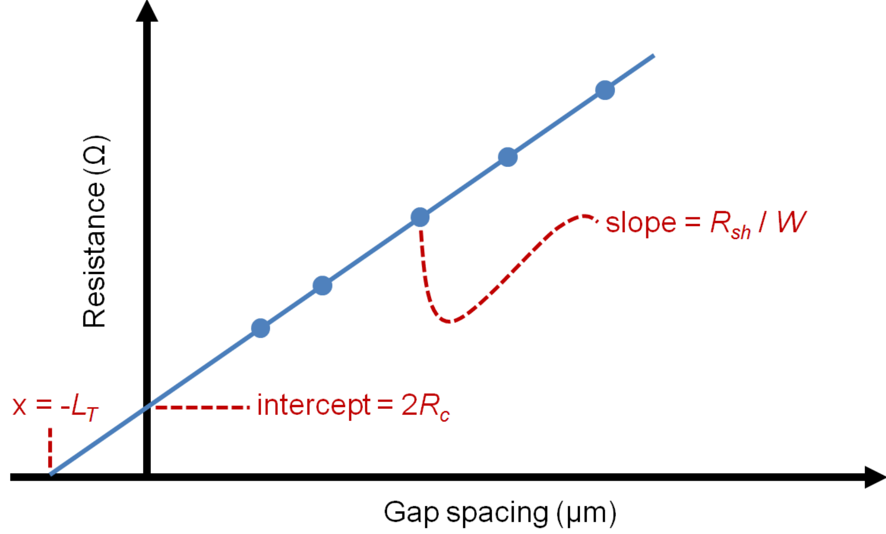


Figure 4.14: Resistance plot for TLM extraction

sistance under the contact. From the TLM analysis, the contact resistance has the form

$$R_c = \frac{\sqrt{\rho_c R_{sh,cont}}}{W} \coth\left(\sqrt{\frac{R_{sh,cont}}{\rho_c}} L_{cont}\right) \tag{4.3.2}$$

where L_{cont} is the length of the contact, and the other term in the hyperbolic cotangent is defined as the transfer length $L_T \equiv \sqrt{\frac{\rho_c}{R_{sh,cont}}}$. For the structures used in these TLM experiments, $L_{cont} \gg L_T$. Using the approximation $\coth x \sim 1$ for $x > 2$, Eq. 4.3.2 can be reduced to

$$R_c = \frac{\sqrt{\rho_c R_{sh,cont}}}{W} = \frac{R_{sh,cont} L_T}{W} \tag{4.3.3}$$

For a single TLM extraction, several resistance measurements are made on structures with varying gap spacing d_{gap} and constant contact width W. When the total resistances R_T are plotted vs. gap spacing d_{gap}, a linear plot is formed, as shown in Fig. 4.14. From this plot, the intercept is $2R_c$, and the slope is $\frac{R_sh,gap}{W}$.

By assuming $R_{sh,gap} = R_{sh,cont} \equiv R_{sh}$, the contact resistivity ρ_c can be solved for.

$$\rho_c = \frac{R_c^2 W^2}{R_{sh}} \tag{4.3.4}$$

In fact, assuming $R_{sh,gap} = R_{sh,cont}$ is not entirely valid, and is a source of error in the TLM extraction. The sheet resistance in the gap and under the contact may be different due to surface depletion or process etch damage. For standalone TLM experiments, this is mitigated by using 100 nm thick epitaxial material – several times thicker than actual emitter or base contact layers. For base contact TLM test structures on HBT wafers, both "pinched" and "non-pinched" TLM structures are fabricated. "Pinched" structures use a dummy emitter structure to form the gap between the TLM contacts, protecting the semiconductor in the gap from surface damage and leaving the HBT epitaxial layers intact [13].

4.3.2 Pad Geometries

A TLM pad structure is shown in Fig. 4.15. Resistances are measured using a four-point technique, where current is sourced through the top and bottom pads and voltage is measured at the two pads on the right side, close to the gap region, so that voltage drops along the contact do not affect the measurement. This configuration of current source and voltage sense pads was chosen so extraction gives a pessimistic value for contact resistivity when the metal resistance is non-negligible. Historically, metal resistance of the pads in TLM measurements has been neglected, but because the contact resistivities reported here are so low, it can have a noticeable effect. The metal resistance was accounted for by modifying Fig. 4.13 such that there are additional lateral resistances in the metal contact, above the semi-

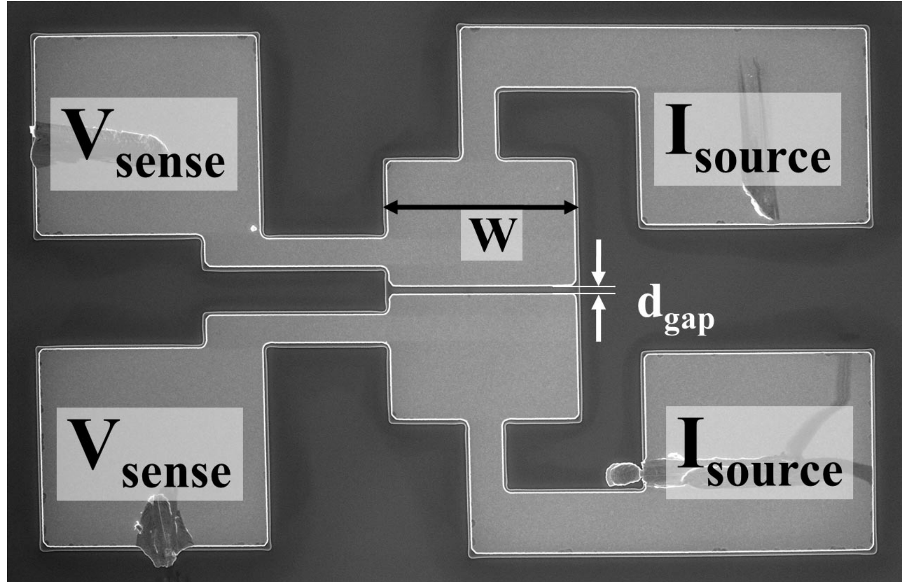


Figure 4.15: Four-point TLM pad structure

conductor resistances, and solving the TLM equations under this condition with numerical finite-element analysis for different pad geometries [14]. Previously used pad geometries effectively subtracted the metal resistance from the contact resistivity term. The effect of the metal resistance, whether additive or subtractive, is reduced to less than a 5 % change in extracted contact resistivity by the 500 nm Au pad layer employed in the TLM metal stack.

4.3.3 Error Analysis

Uncertainty in either the measured resistances or measured gap spacings for each TLM structure lead to uncertainty in the extracted R_{sh} and ρ_c. Errors in resistance measurements come from probe placement and the intrinsic accuracy of the semiconductor parameter analyzer used to make resistance measurements. These are estimated from both re-measuring resistances to see the variation in measured

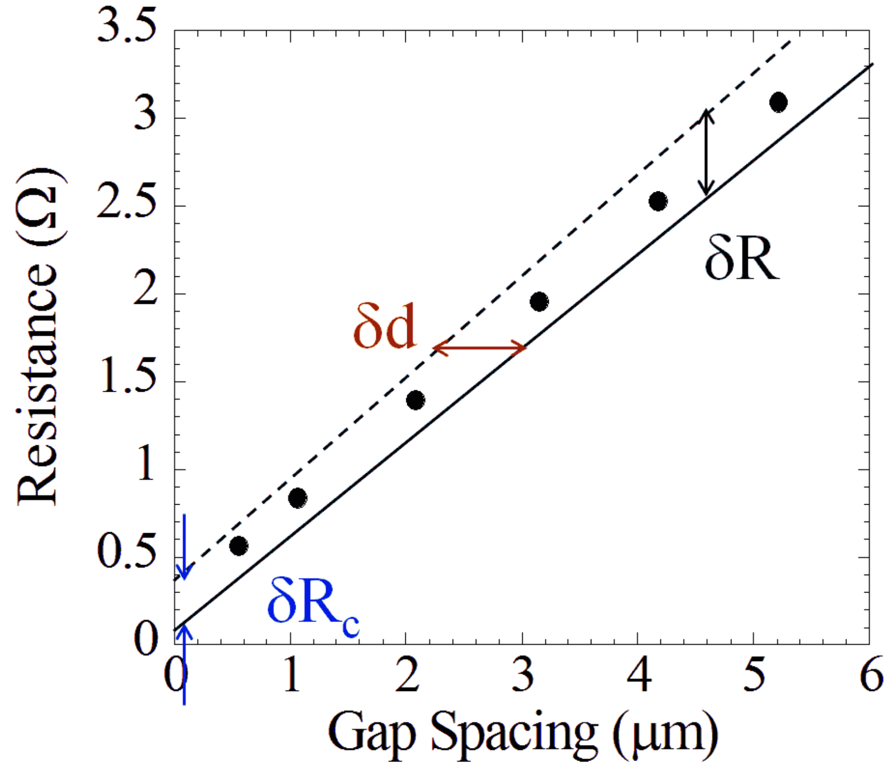


Figure 4.16: Measured TLM data and calculated uncertainty

resistance, as well as the specified accuracy of the tool to be 50 mΩ. Errors in gap spacing measurement come from variation in the profile of the contact as defined by the dry etch, as well as the accuracy of the SEM for measuring gap spacings. This is estimated to be 20 nm. While the errors in both the x- and y-coordinates of each measurement may be random, the largest errors in extracted R_{sh} and ρ_c come from systematic errors of one extreme or the other. Least-squares fits to both the smallest slope / highest intercept and steepest slope / lowest intercept of the resistance vs. gap spacing plot are used to calculate error in R_{sh} and ρ_c.

TLM error can be reduced by making each structure as uniform as possible. Wide TLM structures ($W = 25$ nm) provide more accurate extraction than narrower ones, as the undercut in the semiconductor due to the isolation etch is proportionally

smaller. Making the layers of dry-etched contact metal thin reduces the error in gap measurements due to dry etch undercut or etch variation. Particularly for p-type contacts, where bulk resistivities of the semiconductor is $\sim 2 \times 10^{-3}$ Ω·cm, the gap resistance can make up 95% of the total measured resistance, making small variation in gap length have dramatic effects on extracted intercept, and therefore ρ_c. This can be mitigated in future experiments by using e-beam lithography to define very narrow TLM gaps. For n-type semiconductor, bulk resistivities are $\sim$ 15 times lower than in p-type, so the contact resistivity extraction is more well conditioned.

4.4 Conclusions

For both the extraction of record low contact resistivities from transmission line model experiments and of record bandwidths from transistor S-parameter measurements, calibration and measurement technique are critical. This chapter describes the procedures used in both cases. For transistors, accurate measurements depend on properly biasing the transistor with DC voltages and currents, and obtaining good calibrations at RF frequencies with the vector network analyzer used to conduct RF measurements. Transistors are biased using a semiconductor parameter analyzer to precisely set the base current and collector-emitter voltage.

Several calibration methods have been used, and the quality of the calibrations verified by remeasuring calibration standards after computing error terms and sending them to the network analyzer. Both on- and off-wafer calibration techniques have been tried. On-wafer Thru-Reflect-Line calibrations using microstrip line pad structures are compared with off-wafer calibrations and a pad stripping technique to de-embed the parasitics associated with coplanar waveguide style pads. While

on-wafer calibrations are usable up to ~ 180 GHz, they require more complex fabrication processes and take up substantially more space than the off-wafer calibration standards. Particularly at low frequencies, where wavelengths are long, "Line" standards for on-wafer calibration are cumbersome to measure. Improvements in the pad topology for coplanar style contacts has allowed off-wafer calibrations to be used for measurements to 67 GHz with sufficiently low noise to confidently extract f_{max} on the order of 1 THz.

New four-point measurement pad structures have been developed for TLM measurements. Previously used designs had given overly optimistic results for extracted contact resistivity when the metal resistance of the pads was measured. After analysis in circuit simulator software, new pad designs were implemented which have a term proportional to pad metal resistance added to the extracted contact resistivity. By depositing 500 nm Au pads, the metal resistance can be made negligible, allowing accurate extraction of contact resistivities less than $2\ \Omega \cdot \mu\text{m}^2$.

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Chapter 5

HBT Results

Two fabricated transistor results are presented and analyzed in this chapter. For convenience, the devices are referred to by the design number for their epitaxial growth. DHBT 43 featured a 30 nm base and 150 nm collector [1], while DHBT 60 was thinned to a 25 nm base and 70 nm collector. Emitter junctions in DHBT 43 were 200 nm wide, and these were thinned to 100 nm in DHBT 60, although peak RF performance was obtained with 150 nm junctions. Epitaxial designs, process flows, and DC and RF characteristics are presented for both transistors.

5.1 DHBT 43

DHBT 43 was an incremental improvement to the first refractory emitter process developed at UCSB [2]. Because that result was limited in part by the relatively wide emitter junctions being formed through optical lithography at that time, established epitaxial material with a thicker collector was chosen to yield devices with higher power gain cutoff frequency, f_{max} [3].

5.1.1 Epitaxial Design

The layer structure for DHBT 43 is shown in Tab. 5.1. This material was grown on 4" InP substrates by IQE, Inc. The topmost layer of DHBT 43 is a heavily doped, In-rich InGaAs layer. The high doping and narrow bandgap of this layer are beneficial for low resistance emitter contacts. There is a thin alloy grade from In-rich to InGaAs lattice matched to InP. There is a thicker InP emitter region, some heavily doped and some lightly doped. The lightly doped region serves to define the emitter depletion width, and the InP serves as a barrier for hole injection from base to emitter.

The base is p-type InGaAs, heavily doped so low resistance base contacts can be formed. There is a doping grade causing $\sim$ 50 meV of conduction band drop across the base, decreasing the base transit time. The high doping in the base causes the bandgap of the InGaAs to shrink, so the base layer alloy composition is not specified beyond the constraint it should be lattice matched to the material at the collector interface.

The collector is 150 nm thick, including the InGaAs setback, grade region, and pulse doping to restore the electric field altered by the graded region's quasi-electric field. The grade is a chirped superlattice of $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ with a period of 15 Å. The side towards the base starts with a period of 13.5 Å InGaAs and 1.5 Å InAlAs, and the InAlAs portion increases in width monotonically to $\sim$ 50 % of the period width. There are 16 periods, for a total grade thickness of 24 nm. The grade has the same background doping as the reset of the collector.

The sub-collector has a thin layer of InGaAs, upon which collector contacts are deposited. Below the sub-collector is semi-insulating InP substrate.

Thickness (Å)	**Material**	**Doping (cm^{-3})**	**Description**
100	$In_{0.85}Ga_{0.15}As$	5×10^{19} : Si	Emitter cap
150	$In_xGa_{1-x}As$	$> 4 \times 10^{19}$: Si	Em. cap grade
200	$In_{0.53}Ga_{0.47}As$	4×10^{19} : Si	Emitter
800	InP	3×10^{19} : Si	Emitter
100	InP	8×10^{17} : Si	Emitter
400	InP	5×10^{17} : Si	Emitter
300	$In_xGa_{1-x}As$	7–4 $\times 10^{19}$: C	Base
150	$In_{0.53}Ga_{0.47}As$	3.5×10^{16} : Si	Setback
240	InGaAs / InAlAs	3.5×10^{16} : Si	BC Grade
30	InP	3.5×10^{18} : Si	Pulse doping
1080	InP	3.5×10^{16} : Si	Collector
50	InP	1×10^{19} : Si	Sub-collector
65	$In_{0.53}Ga_{0.47}As$	2×10^{19} : Si	Sub-collector
3000	InP	2×10^{19} : Si	Sub-collector
Substrate	Semi-insulating InP	—	—

Table 5.1: DHBT 43 Epitaxial Design

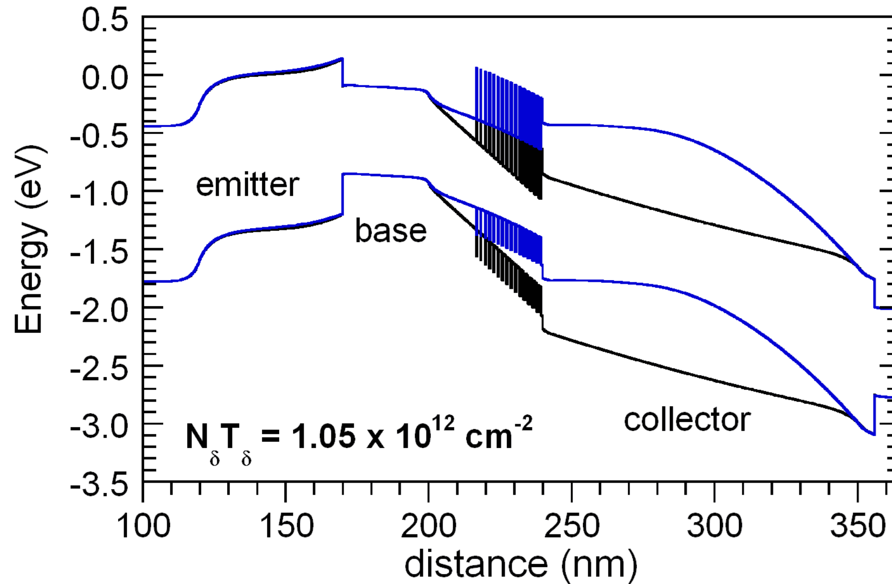


Figure 5.1: Band diagram for DHBT 43 with V_{be} = 1.0 V and V_{cb} = 0.6 V, with J_e = 0 (black) and 10 mA/μm^2 (blue)

5.1.2 Process Flow

The process flow for the emitter formation of DHBT 43 is shown in Figs. 3.1 and 3.2. To summarize, the process began with a blanket deposition of sputtered $Ti_{0.1}W_{0.9}$, PECVD SiO_x, and Electron-beam evaporated Cr. Optical lithography was used to pattern the emitter photomask, and ICP dry etches were used to form the emitter contact. A hybrid dry etch/wet etch process is used to etch the emitter semiconductor and provide a controllable amount of undercut under the emitter contact. This hybrid etch became necessary as emitter widths were narrowed from > 250 nm to 200 nm, while emitter epitaxial thickness remained ~ 150 nm — the isotropic wet etches previously used began to severely undercut the emitter mesa to the point of structual failure. Two Si_xN_y sidewalls are formed through PECVD deposition and ICP etch, one at the metal/semiconductor emitter interface and one at the emitter InGaAs/InP interface. This combination of sidewalls was found empirically to increase emitter yield, where either one by itself was insufficient in this task. Fig. 5.2 shows the cross-sectional profile of the sputtered $Ti_{0.1}W_{0.9}$ emitter and the emitter semiconductor.

The base contact mask is defined through optical lithography and lift-off of Pd/Ti/Pd/Au, ~ 100 nm thick. The height of the emitter semiconductor mesa, and its undercut under the emitter contact, forms the break in the emitter profile to allow the self-aligned base contact. The base mesa and collector mesa are defined through optical lithography and selective wet etch, and the transistor is planarized and passivated with BCB.

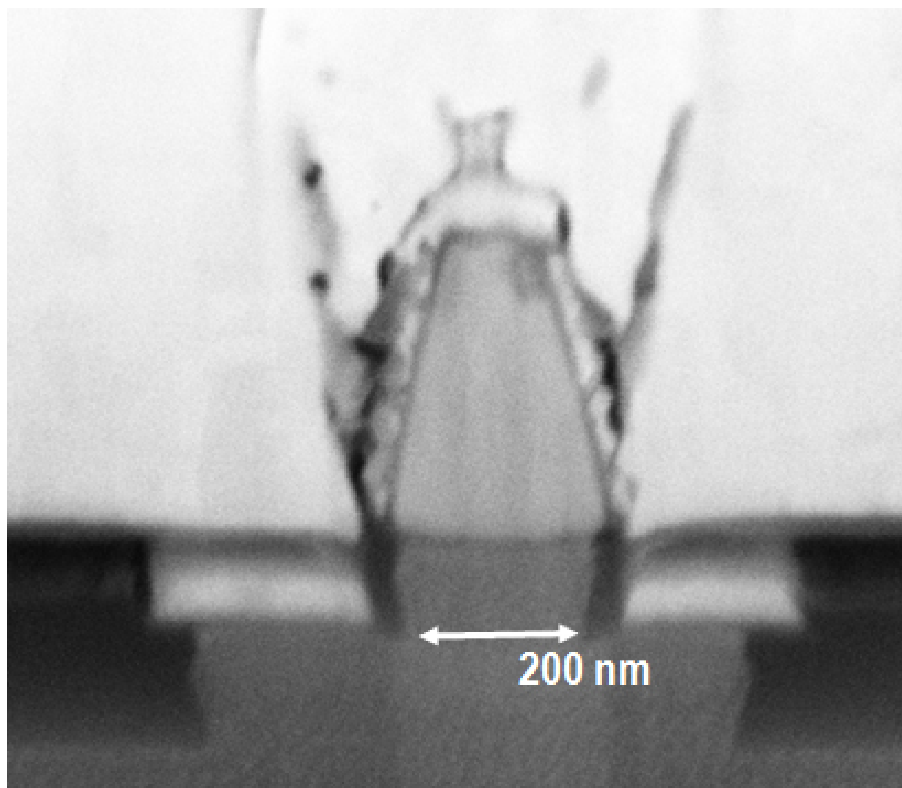


Figure 5.2: SEM cross-section of DHBT 43

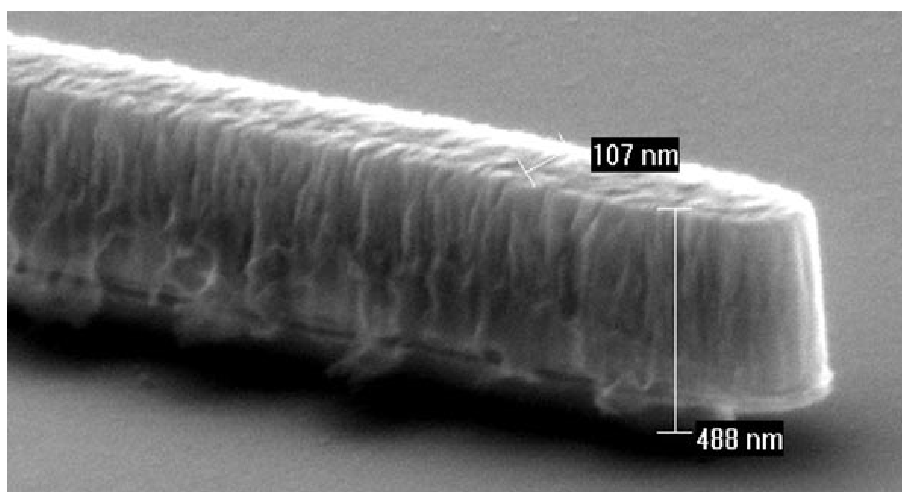


Figure 5.3: Angled SEM of DHBT 43 emitter after wet etch

Layer	Contact Resistivity ($\Omega \cdot \mu m^2$)	Sheet Resistance ($\Omega/\square$)
Emitter	9	—
Base	7	660
Collector	23	10

Table 5.2: DHBT 43 Contacts

5.1.3 DC Characteristics

Base and collector contact resistivities and sheet resistances were measured using a series of four-point resistance measurements on on-wafer TLM structures. Extrinsic emitter resistance was extracted from RF measurements of Y_{21} at different collector current biases. These contact parameters are shown in Tab. 5.2. The contact resistivity for the collector was much higher than what is obtainable with lifted off Ti/Pd/Au contacts due to photoresist scum left on the collector semiconductor surface from a step prior to collector contact deposition. The scum was removed through brief O_2 ashing at 150 °C, but some damage to the surface occurred.

Common-emitter I-V curves and Gummel plots were measured, as shown in Figs. 5.4 and 5.5. From the common-emitter curves, current gain $\beta \cong 20$ for 200 nm wide devices, and $\beta \cong 30$ for 300 nm wide devices. The common-emitter breakdown voltage for these devices was $VB_{ceo} = 4.34V$, defined at the voltage where emitter current density $J_e = 1$ kA/μm^2. Ideality constants for the base and collector currents are extracted to be $\eta_b = 1.67$ and $\eta_c = 1.19$, respectively.

5.1.4 RF Data

RF measurements were taken on an Agilent E8361A Parameter Network Analyzer from 0.1 to 67 GHz at a variety of DC bias points. Measured S-parameter data were converted into H_{21} and U plots, from which f_τ and f_{max} were extracted,

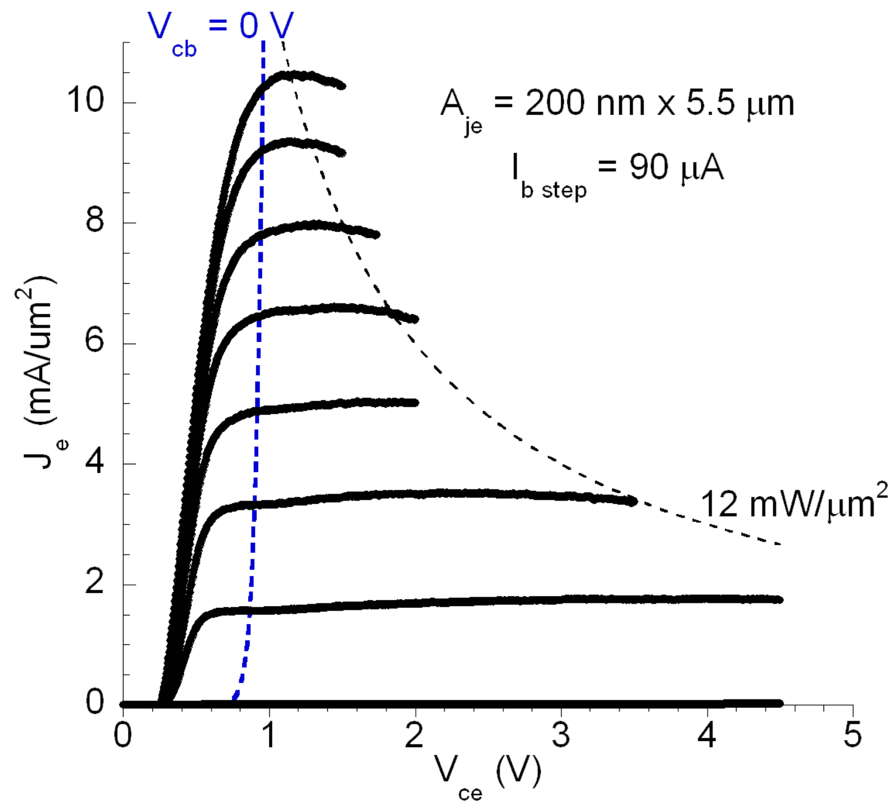


Figure 5.4: DHBT 43 Common-Emitter Curves

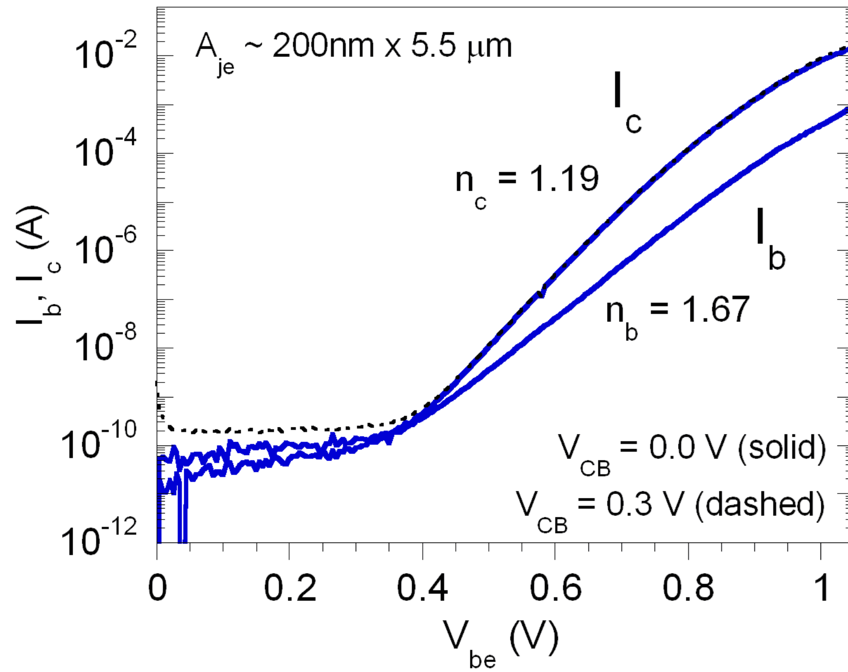


Figure 5.5: DHBT 43 Gummel Plot

as shown in Fig. 5.6. Collector-base capacitance C_{cb}, as well as other equivalent circuit parameters, were extracted to form an equivalent circuit model, as shown in Figs. 5.8 and 5.9a. Good agreement between the measured S-parameters and the simulated parameters from the equivalent circuit indicate a good understanding of the physical transistor structure. Base-collector capacitance C_{cb} is comparable to that for transistors fabricated on the same epitaxial material with lifted off emitter contacts [3], as is expected. Increases in f_{max} in the sputtered contact result are largely due to the reduction in R_{bb}.

f_τ and f_{max} were extrapolated from single-pole fits to measured H_{21} and U data. In addition, f_τ was calculated using the Gummel method, and found to agree with single-pole extraction [4]. By examining the expression for U in terms of Y-parameters, the source of the noise, peaks, and dips in the U curve can be traced

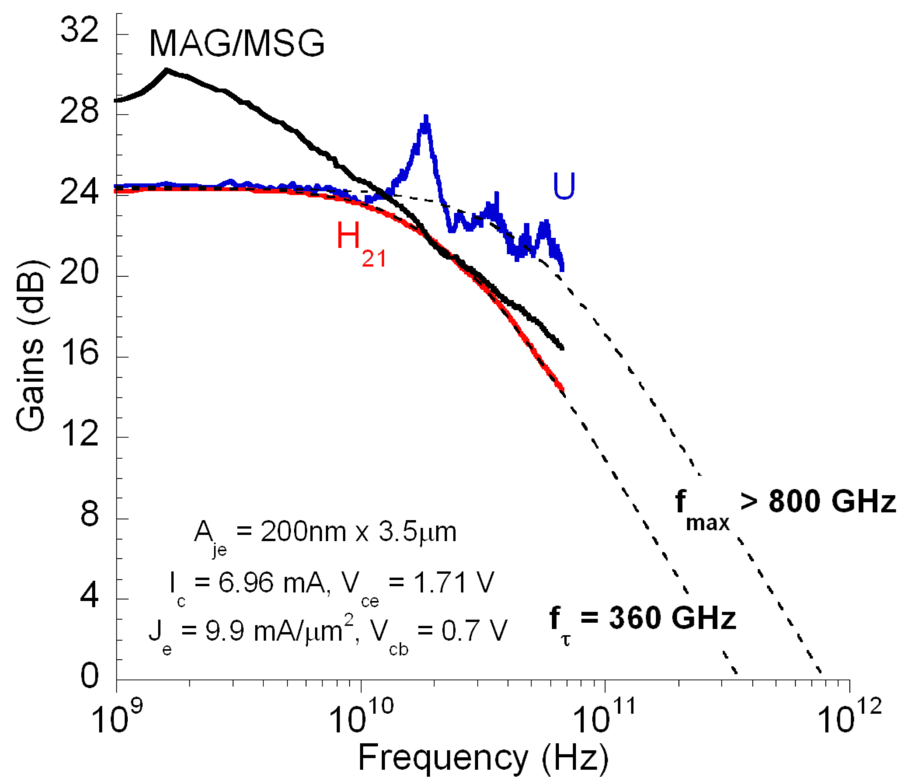
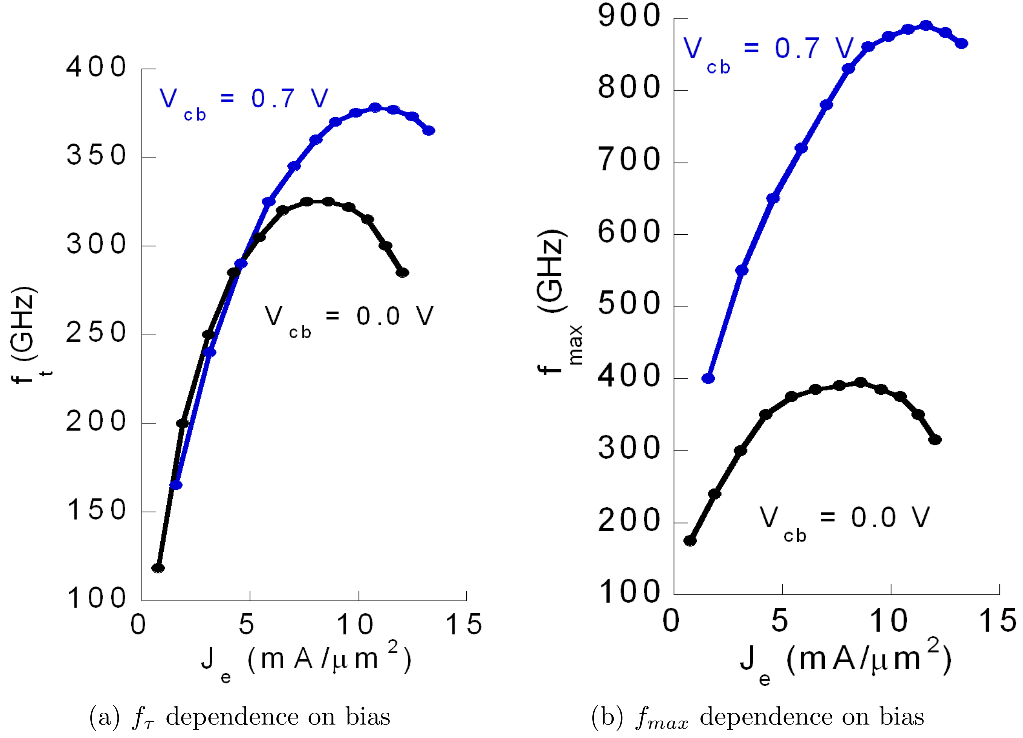


Figure 5.6: DHBT 43 gains, with extrapolated cutoff frequencies



(a) f_τ dependence on bias

(b) f_{max} dependence on bias

Figure 5.7: Variation of (a) f_τ and (b) f_{max} with collector current I_c and collector-base capacitance C_{cb} for DHBT 43

back to the denominator of Eq. 5.1.1. The difference of the two products is often small, making the U equation somewhat ill-conditioned and very sensitive to small variations in the Y-parameters. This necessitates higher frequency measurements or alternate pad structures for more reliable f_{max} extraction in the THz regime. For this result, fits for f_{max} between 800 GHz and 900 GHz seem most accurate, but it cannot be determined with high confidence based on these data alone.

$$U = \frac{\|Z_{12} - Z_{21}\|^2}{4\left(\Re\{Z_{11}\}\Re\{Z_{22}\} - \Re\{Z_{21}\}\Re\{Z_{12}\}\right)} \tag{5.1.1}$$

At first, f_τ increases with increasing I_c as the transconductance g_m increases, and charge screening in the collector depletion region decreases collector transit

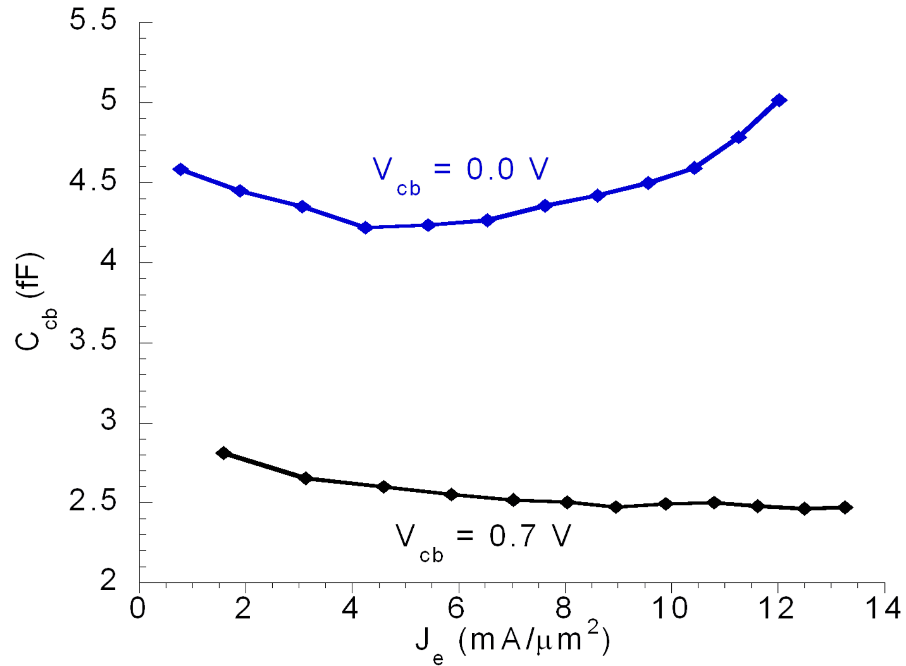


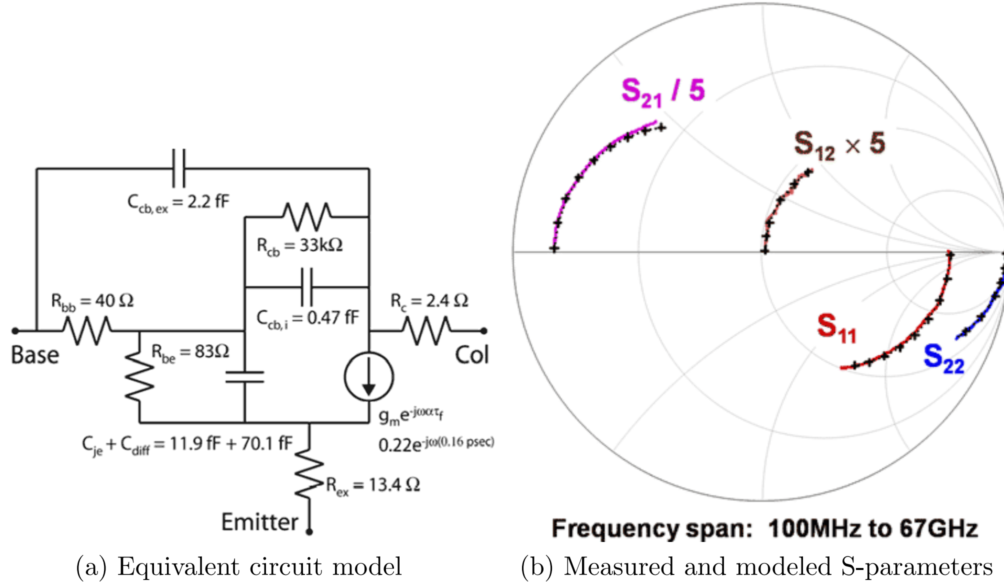
Figure 5.8: Variation of C_{cb} with current and collector-base voltage

time τ_c. Eventually, the transistor reaches the Kirk effect regime, where the charge screening in the collector creates a barrier for electron flow, and begins to increase base-collector capacitance C_{cb}. Power gain cutoff f_{max} is proportional to $\sqrt{f_\tau}$, so follows similar trends.

C_{cb} initially decreases with increasing current, but then begins to rise again as the Kirk limit is reached. Kirk onset is pushed to higher current densities as the collector-base voltage increases, and overall C_{cb} curves decrease with increasing V_{cb}.

5.1.5 Conclusions

At the time of its publication, DHBT 43 represented the highest f_{max} reported in an InP mesa HBT, although the $f_\tau = 360$ GHz was below the state-of-the-art. This was achieved largely through reductions in emitter size by switching from



(a) Equivalent circuit model (b) Measured and modeled S-parameters

Figure 5.9: (a) Equivalent circuit model and (b) measured and modeled S-parameters for DHBT 43, at bias point corresponding to peak f_τ and f_{max}

lifted off contacts, and using epitaxial material with a comparatively thick collector. However, device yield was very low in this result, despite the use of two sidewalls to protect the emitter and mechanically anchor it in place. Emitters were narrowed by switching to a positive resist process and using O_2 plasma etches to reduce the size of the photoresist features, but the technique was not scalable below ~ 200 nm features due to plasma damage to the photoresist. While sputtered W on n-type TLMs had shown contact resistivities $> 2\ \Omega \cdot \mu\text{m}^2$ [5], the contact resistivities extracted from the DHBT 43 transistors were substantially higher.

These problems were addressed in future fabrications. Device yield was increased by developing a bilayer $W/Ti_{0.1}W_{0.9}$emitter metal stack that was much lower stress. E-beam lithography was used to further scale the emitter, and then the base, contact dimensions. The emitter semiconductor layers were redesigned and thinned to minimize depletion capacitance C_{je} and reduce resistive drops in the emitter-

base depletion region. These modifications have been implemented in the transistor design that followed.

5.2 DHBT 60

DHBT 60 was designed with a 25 nm base and 70 nm collector, designed for higher f_τ while maintaining high f_{max} through lithographic scaling of the emitter and base mesas. Electron-beam lithography was used for both emitter and base, as in previous record results on 100 nm collector epitaxial material [6]. Base contacts were lifted off, but an interfacial Pt layer instead of Pd was used, as Pt has been seen to demonstrate greater thermal stability and lower resistance contacts after the 250 °C anneal required for the BCB cure [7]. No transmission-line microstrip pad environments were fabricated due to concerns about the resistive losses in the existing designs; instead coplanar pad structures, both with individually isolated transistors and columns of devices sharing ground planes, were used.

5.2.1 Epitaxial Design

Compared to the epitaxial design of DHBT 43, the design of DHBT 60 has been thinned and simplified. The epitaxial design is presented in Tab. 5.3 and Fig. 5.10. For comparison, the entire epitaxial design for DHBT 60 is $\sim$ 150 nm thick, whereas just the emitter design for DHBT 43 is 160 nm. Minimal difference in contact resistivity between InAs and InGaAs n-type contacts has been demonstrated, so a single layer of lattice-matched InGaAs is all that is used as the contact layer. The InP of the emitter is thinned and more heavily doped, as well. The base thickness has been decreased from 30 nm to 25 nm, and the doping at the top of the base has

been increased to 1.0×10^{20} cm^{-3}. This higher doping is intended to improve the base contact resistivity and sheet resistance, but also has the effect of increasing recombination and reducing current gain β as well.

The setback region, InGaAs/InAlAs grade, and collector region have been thinned to 70 nm in total. To maintain breakdown, the ratio of narrow-bandgap ternary and wide-bandgap InP has been roughly maintained, as the collector thickness has been reduced from 150 nm to 70 nm, the grade thinned from 24 nm to 12 nm. The period of the chirped superlattice is the same as in DHBT 43, 15 Å, but the number of periods has been reduced to 7.

The collector doping has been increased as proscribed by Eq. 2.2.4. The InGaAs sub-collector has been more heavily doped, in an effort to reduce collector contact resistivity, and a thin InGaAs etch stop has been added after the InP sub-collector. Previously, device passivation was done by wet etching $\sim$ 400 nm of InP, so the etch would end up well into the semi-insulating substrate. Due to variability in etch rate, this could be unreliable, and adding an etch stop layer allows a very brief InGaAs wet etch followed by a shorter InP wet etch to reach the appropriate depth in the substrate.

5.2.2 Process Flow

The emitter stack has been refined since the results of DHBT 43. The surface is cleaned with dilute HCl, then an interfacial layer of Mo was E-beam evaporated on the sample. A series of calibrations were carried out on dummy wafers, then a low stress bilayer W/$Ti_{0.1}W_{0.9}$ stack 500 nm tall was sputtered on top of the Mo. PECVD SiO_x and Cr were deposited as in the DHBT 43 process. Lithography

Thickness (Å)	Material	Doping (cm^{-3})	Description
100	$In_{0.53}Ga_{0.47}As$	8×10^{19} : Si	Emitter cap
150	InP	5×10^{19} : Si	Emitter
150	InP	2×10^{18} : Si	Emitter
250	$In_xGa_{1-x}As$	1.0–4 $\times 10^{20}$: C	Base
95	$In_{0.53}Ga_{0.47}As$	1×10^{17} : Si	Setback
120	InGaAs / InAlAs	1×10^{17} : Si	BC Grade
30	InP	5×10^{18} : Si	Pulse doping
455	InP	1×10^{17} : Si	Collector
50	$In_{0.53}Ga_{0.47}As$	4×10^{19} : Si	Sub-collector
3000	InP	1×10^{19} : Si	Sub-collector
35	$In_{0.53}Ga_{0.47}As$	undoped	Etch stop
Substrate	Semi-insulating InP	—	—

Table 5.3: DHBT 60 Epitaxial Design

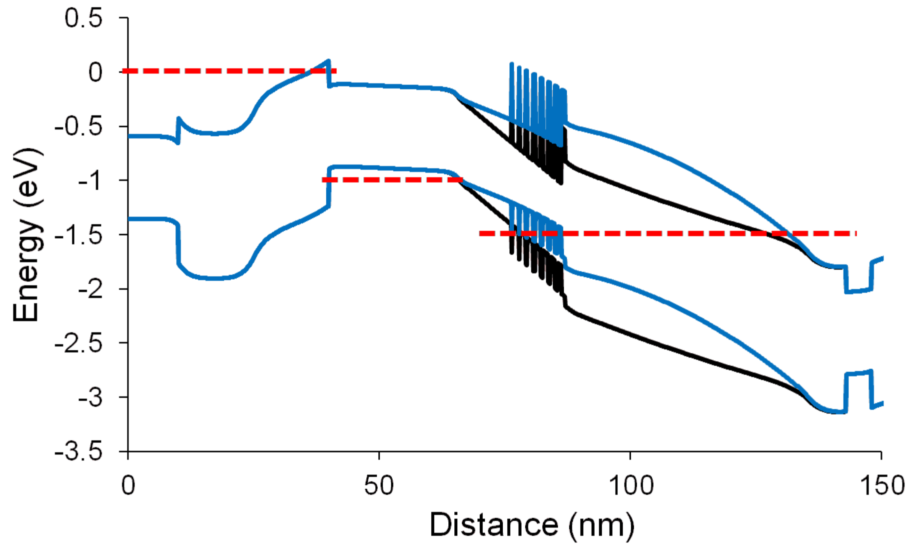


Figure 5.10: Band diagram for DHBT 60 with $V_{be} = 1.0$ V and $V_{cb} = 0.5$ V, with $J_e = 0$ (black) and 27 mA/μm^2 (blue)

for the emitter was performed using electron-beam lithography to draw features as narrow as 75 nm.

The emitter contact was formed through dry etches similar to those used in DHBT 43. Again, two Si_xN_y sidewalls are formed. Because the emitter semiconductor has been thinned, an all-wet etch process is now feasible to etch the emitter semiconductor. Because the sidewalls increase the size of the pre-etch mesa, even junctions as narrow as 75 nm may be formed via wet etch, although dry etching metal contacts that narrow is still a process which needs further development for good yield.

The base contact was formed through liftoff, using electron-beam lithography. While the narrowest features drawn for the base are $\sim$ 600 nm wide, the misalignment to the emitters must be 50 nm or less. It is for this critical alignment, not feature size, that e-beam lithography is needed for the base contact formation. As shown in Fig. 5.12, peak RF bandwidth is achieved in devices with $\sim$ 150 nm wide emitter and base contacts. The emitter-base misalignment has been reduced to $<$ 20 nm, and the wet etch used to define the base mesa and undercut the contact forms a collector-base junction $\sim$ 450 nm wide. E-beam lithography is also used for the base mesa mask, but optical lithography remains for the base post, due to the $\sim$ 450 nm height of the posts lifting off. The posts have been changed to Ti/Pd/Au instead of the same metal layers as the base, to increase metal-to-metal adhesion between base contact and base post.

After the base mesa formation, back-end processing is essentially the same as that in DHBT 43.

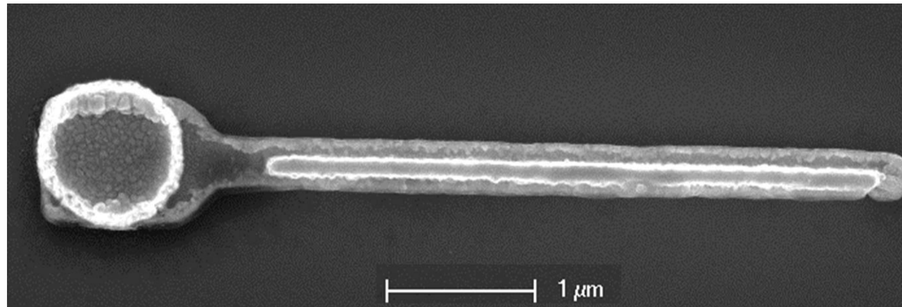


Figure 5.11: DHBT 60 after emitter and base fabrication

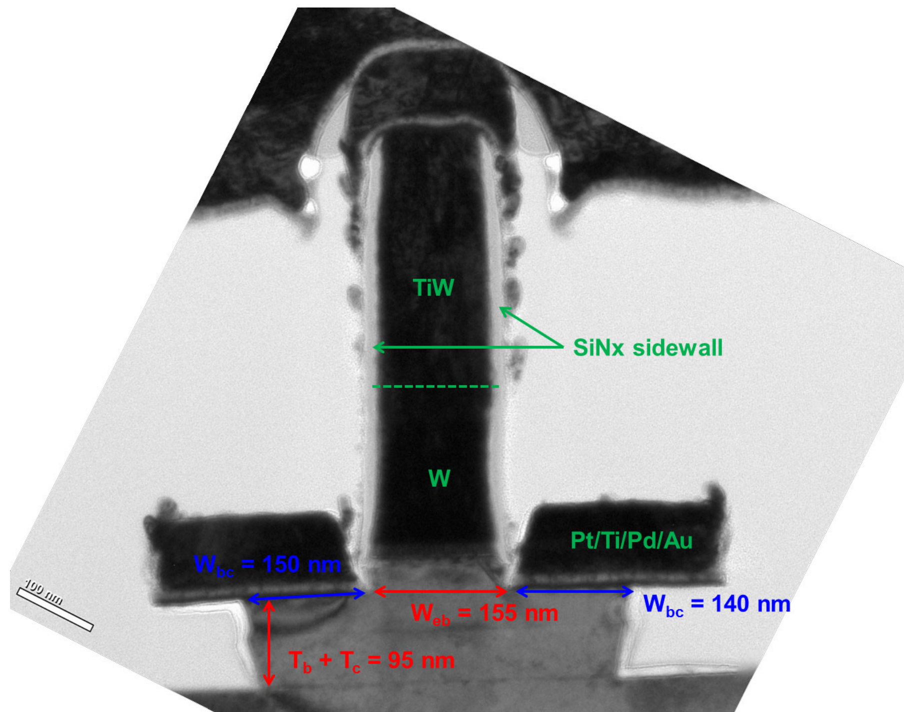


Figure 5.12: TEM cross-section of emitter and base of DHBT 60

5.2.3 DC Characteristics

Transistor common-emitter curves for DHBT 60 are shown in Fig. 5.13 for a 150 nm wide device. Many transistors in the DHBT 60 run showed instability when operated at collector-emitter voltage $V_{ce} > 1.2$ V, so these curves were deliberately truncated before reaching device failure. Nevertheless, these transistors operate easily at power densities of 25 mW/μm^2, double that seen in DHBT 43. This is accomplished by narrowing the emitter-base junction, which increases J_e for the same current, and thinning the collector, which pushes higher the current density at which Kirk effect occurs. Peak RF performance was obtained at a current density of 27 mA/μm^2 and power density of 40 mW/μm^2. Common-emitter breakdown voltage VB_{ceo} is 2.44 V, defined as the point at which $J_e = 150\ \mu$A/μm^2.

Gummel plot extractions show a peak current gain $\beta = 14$ for a 150 nm device. Base and collector ideality factors were $\eta_b = 2.72$ and $\eta_c = 1.25$, respectively. The high base ideality factor may be due to both the higher doping in this base design and damage at the emitter-base interface, which is also supported by the high base resistance R_{bb} seen in Fig. 5.17a.

Base TLMs were unmeasurable on DHBT 60 due to design errors in the base mask set. From on-wafer collector TLMs, contact resistivity was measured to be $\rho_c = 12\ \Omega \cdot \mu\text{m}^2$, and sheet resistance was $R_{sh} = 14.3\ \Omega/\Box$.

5.2.4 RF Data

RF gains were measured on an Agilent network analyzer from 0.1 to 67 GHz. The same two-step off-wafer calibration and parasitic pad stripping used in the DHBT 43 RF measurements was used here as well. The gain measurements are shown

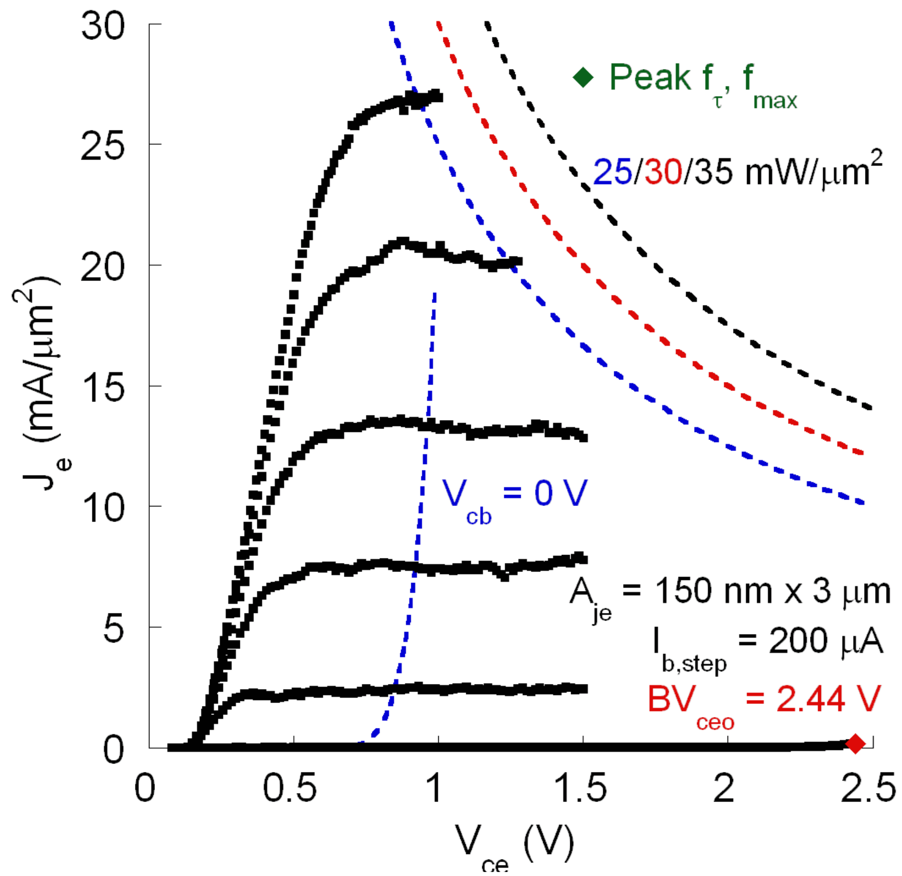


Figure 5.13: DHBT 60 Common-Emitter Curves

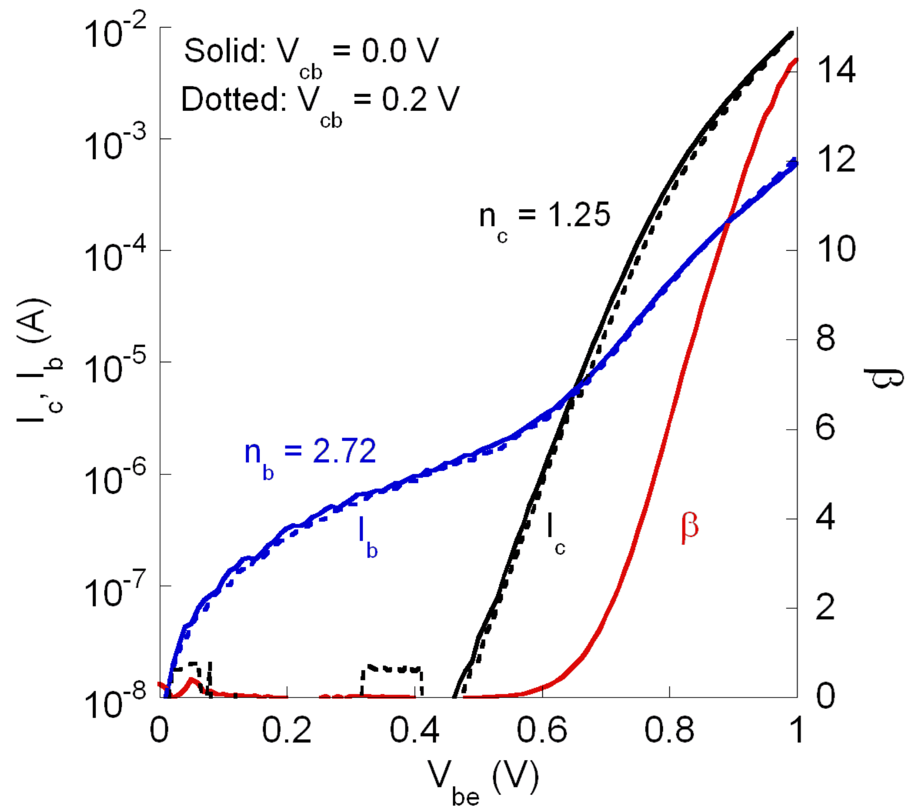


Figure 5.14: DHBT 60 Gummel Plot

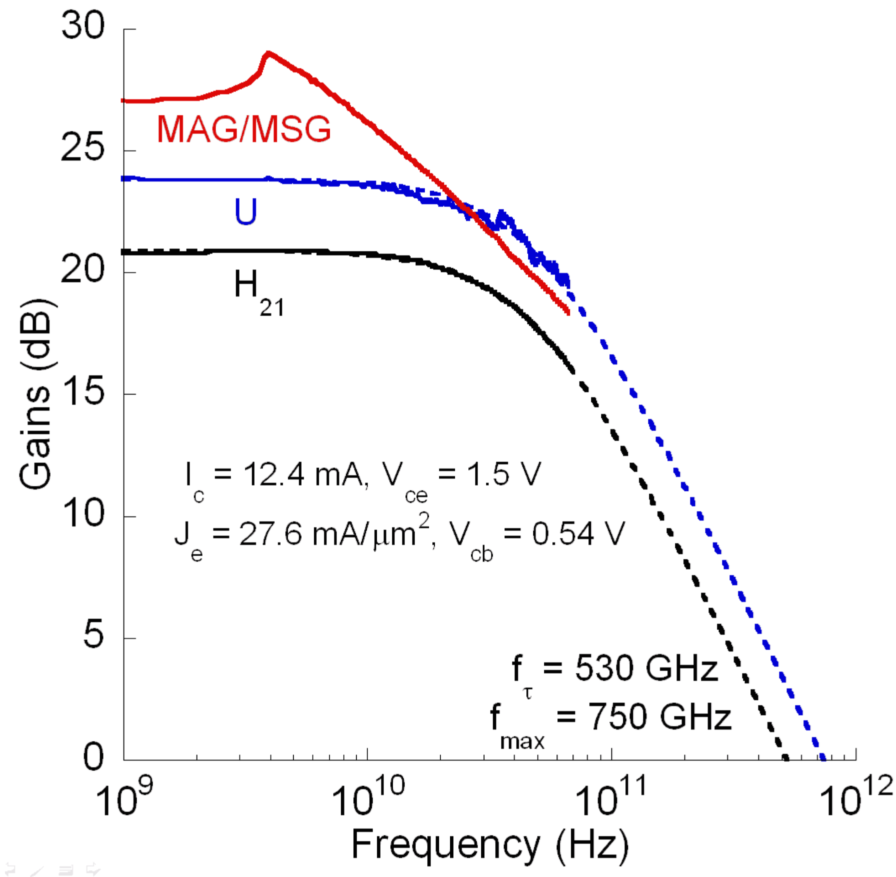


Figure 5.15: DHBT 60 gains, with extrapolated cutoff frequencies

in Fig. 5.15, with single-pole extrapolated f_τ = 530 GHz and f_{max} = 750 GHz. Mason's Unilateral Gain U curves are substantially less noisy than those of Fig. 5.6, likely due to the use of isolated ground plane coplanar structures instead of shared ground plane structures. While f_{max} is not as high as in DHBT 60 as in DHBT 43, the confidence of the extraction is much higher due to the quality of the data.

The dependence of f_τ, f_{max}, and C_{cb} are shown in Fig. 5.16. These devices were not limited by Kirk effect, as they fail at current densities below where f_τ and f_{max} begin to decrease and C_{cb} begins to increase.

The equivalent circuit model for DHBT 60 at peak RF bias, as well as the

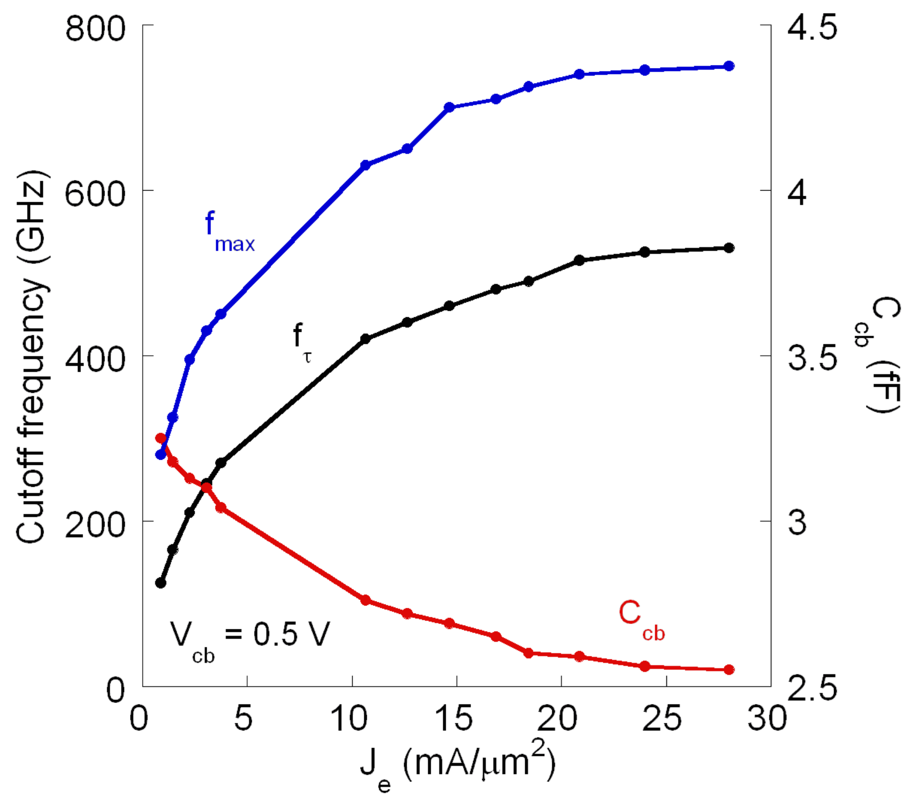
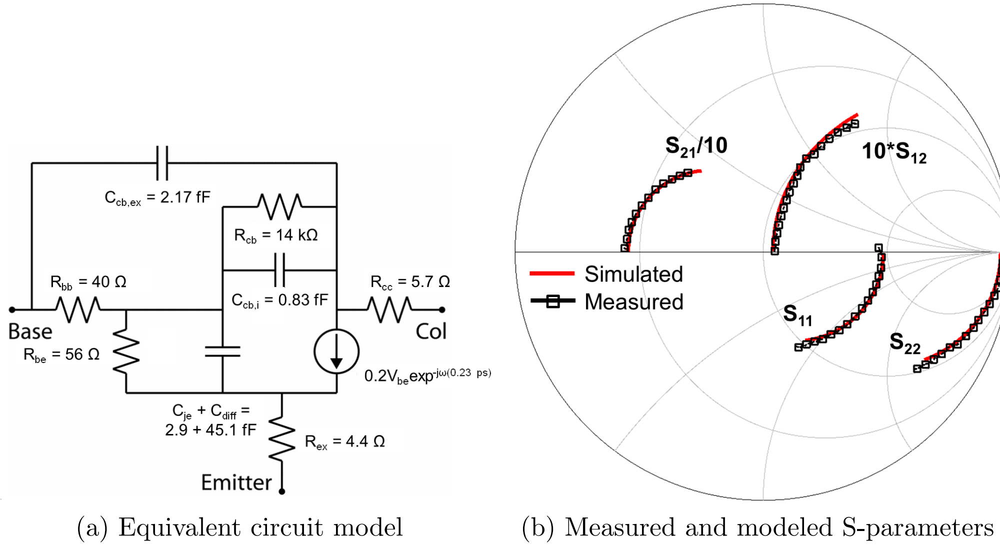


Figure 5.16: Cutoff frequency and collector-base capacitance dependence on bias



(a) Equivalent circuit model (b) Measured and modeled S-parameters

Figure 5.17: (a) Equivalent circuit model and (b) Smith chart representation of measured and modeled S-parameters for DHBT 60, at bias point corresponding to peak f_τ and f_{max}

measured and modeled S-parameters, are shown in Fig. 5.17. Several comparisons to DHBT 43 can be made. Extrinsic emitter resistance R_{ex} has been halved despite the emitter contact area being reduced in size, which demonstrates the superiority of the HCl surface clean and evaporated Mo contact over sputtered W, as well as the benefits of the redesigned emitter semiconductor layer. Base-collector capacitance C_{cb} is roughly the same as in 43, despite collector thickness T_c being reduced to less than half of what it was. This was accomplished by using electron-beam lithography for the base, which allowed the size of the mesa to be made substantially smaller. Base resistance R_{bb} was higher than expected, at 40 Ω. Base contacts formed through the same lift off process have previously shown $R_{bb} < 30\Omega$, even with larger emitter-base misalignments [6]. Device f_{max} would be higher if base resistance R_{bb} was not higher than expected.

5.2.5 Conclusions

In moving from DHBT 43 to DHBT 60, the emitter process for contact deposition, etch, and sidewall formation were made more robust, yielding sub-100 nm emitter devices. The use of e-beam lithography to define the emitter and base resulted in smaller junction areas, and the epitaxial design was thinned to reduce transit time. f_τ was increased $\sim$ 40% while f_{max} was reduced by only $\sim$ 8%. From RF extraction and hybrid-π equivalent circuit model generation, it is evident total transit time τ_{ec} in the transistor is dominated by transit delays in the base and collector. Extracted $\tau_f = \tau_b + \tau_c \approx 230$ fs. The term associated with the emitter-base junction charging time, $\frac{\eta k_B T}{q I_c} C_{je} \approx 15$ fs, and the base-collector junction charging time $\left(\frac{\eta k_B T}{q I_c} + R_{ex} + R_c\right) C_{cb} \approx 45$ fs. To create further increases in f_τ, the base and collector layers must be thinned to reduce τ_b and τ_c. Possible techniques by which to reduce base thickness without dramatically reducing f_{max} are considered in Sec. 6.2.3. The extracted ideality factor of $\eta = 2.4$ is higher than previously seen. Modeled f_τ increases by $\sim$ 10 % when η is reduced to 1.7, a value seen in previous results [6].

f_{max} for a bipolar transistor is proportional to $\sqrt{f_\tau}$ and inversely proportional to $\tau_{cb} = R_{bb} C_{cb,i}$. For this transistor, both the low f_τ and high R_{bb} caused a reduction in f_{max}. C_{cb} was sufficiently small due to a well-aligned base mesa process. Modeled f_{max} depends strongly on R_{bb}: a modeled $f_{max} \sim 1.2$ THz would be obtainable with the given $f_\tau = 530$ GHz and $R_b b = 27\Omega$, the value seen in previous THz f_{max} results [6]. One possible cause for this unexpectedly high R_{bb} is faults in the design or growth of the base epitaxy. A new base design was employed in this result, where T_b was thinned from 30 to 25 nm, and the peak doping at the emitter side of the

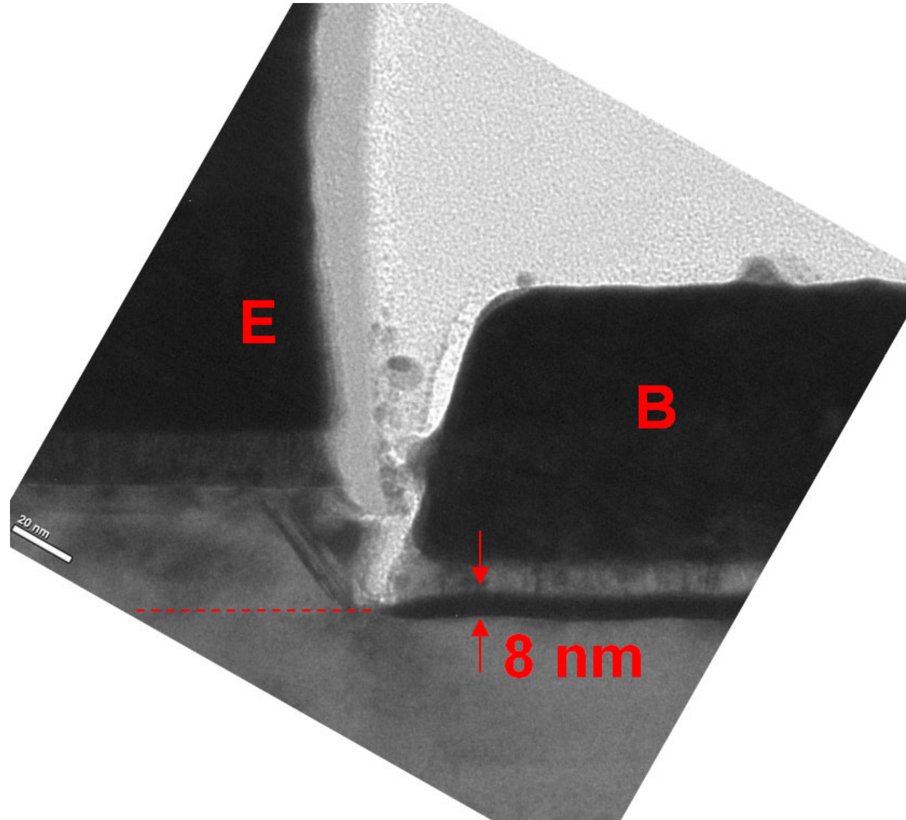


Figure 5.18: Base contact interface for DHBT 60

base was increased from 9×10^{19} cm^{-3} to 1.0×10^{20} cm^{-3}. Residual photoresist scum on the surface after base lithography could also have increased the contact resistivity, and therefore, R_{bb}, but base TLM measurements would be necessary to determine if this were the case. Finally, even if the base epitaxy was grown correctly, the base contact appears to diffuse or react with $\sim 5nm$ of the base semiconductor. The interfacial Pt layer of the base contact is deposited 2.5 nm thick, but TEM cross-sections show this layer to be $\sim$ 8 nm after device measurement, as shown in Fig. 5.18. Possible solutions to this reactive base contact problem are discussed in Secs. 6.2.2 and 6.2.3.

References

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Chapter 6

Conclusion

6.1 Summary

In this work, we have presented the relevant equations describing the resistances, capacitances, and transit delays in bipolar transistors. We have used those equations to enumerate a set of design principles for proportionally reducing those elements to increase the frequencies of operation of mesa InP dual heterojunction bipolar transistors. We have identified the dominant challenges, and developed several advanced fabrication processes to enable incremental transistor performance. We presented here two type-I, triple-mesa, InP/InGaAs DHBT results, from their epitaxial design, fabrication processes, electrical measurement methodologies, and DC and RF data.

6.1.1 Design Principles

To double the bandwidth of an electronic device, all the transit delays and RC time constants in the device must be halved. For bipolar transistors, where the direction of current flow is perpendicular to the direction of epitaxial growth of the

Design Parameter	Scaling Law
Depletion layer thicknesses	2:1
Junction widths	4:1
Junction lengths	1:1
Contact resistivities	4:1
Current density	4:1

Table 6.1: Necessary reductions to double HBT bandwidth

material, the transit delays can be reduced by thinning the semiconductor layers. Since the layers are 10 – 100 nm thick, molecular beam epitaxy can easily grow layers substantially thinner than this, so transit delays are comparatively easy to reduce. However, if the only device scaling comes through reduction of vertical layer thickness, the parallel plate capacitance associated with the collector-base junction (C_{cb}) will increase, as will the base resistance (R_{bb}) due to the increase in sheet resistance of the base layer. To reduce the junction capacitances, the areas of the emitter-base and collector-base junctions must be scaled more rapidly than the layer thicknesses. This leads to an increase in contact resistances $\left(R_c = \frac{\rho_c}{A}\right)$ associated with the emitter, base, and collector. These can be reduced by developing low-resistance contact processes like heavily doping the semiconductor cap layers, surface cleans to remove contaminants and surface oxides, and choice of thermally stable, low resistance contact metals.

Reductions in contact resistivity are the most difficult of the three challenges to scale, so the method of least aggressive scaling for contact resistivity is chosen. To summarize Tab. 2.1, Tab. 6.1 is presented. In this model, transit delays and capacitances are reduced by a factor of 2, and currents and resistances remain constant, as device bandwidth is doubled. As discussed in Sec. 2.6, junction area is scaled solely in junction widths to reduce device thermal resistance.

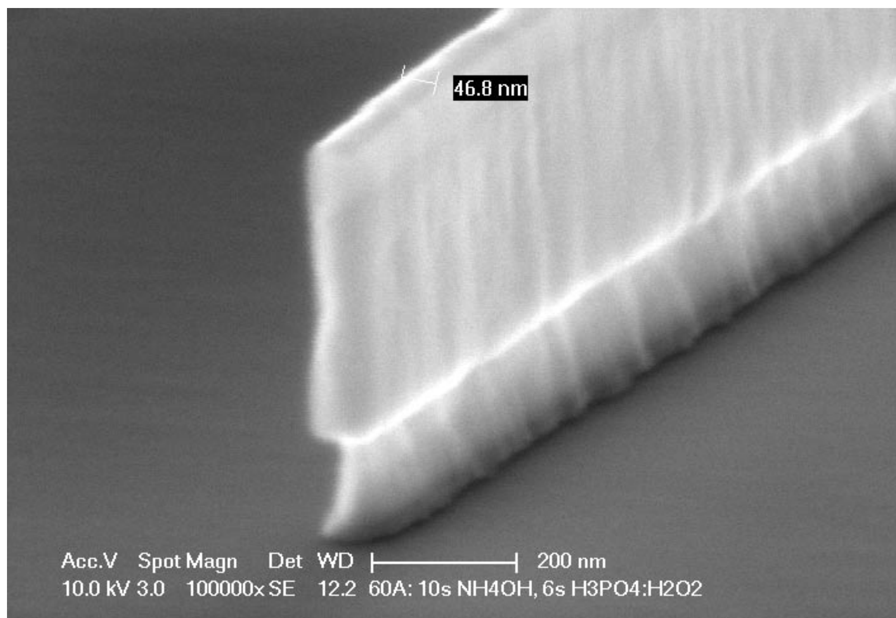


Figure 6.1: Angled SEM of electron-beam lithography defined emitter

6.1.2 Fabrication Techniques

Substantial work has gone into developing new fabrication techniques to enable these transistors, as detailed in Ch. 3. Chief among these techniques are inductively coupled plasma etches, electron-beam lithography, and refractory metal deposition through evaporation or sputtering. ICP dry etches are used to form high aspect ratio features by exploiting the anisotropic nature of the etch. Electron-beam lithograph is used to define narrower emitter features than can be achieved through optical lithographic techniques, and to align base contacts to emitter contacts more precisely than possible with the optical lithography tools presently available at UCSB. Refractory metal contacts provide low resistance and thermal stability at the high current densities needed to achieve record RF performance.

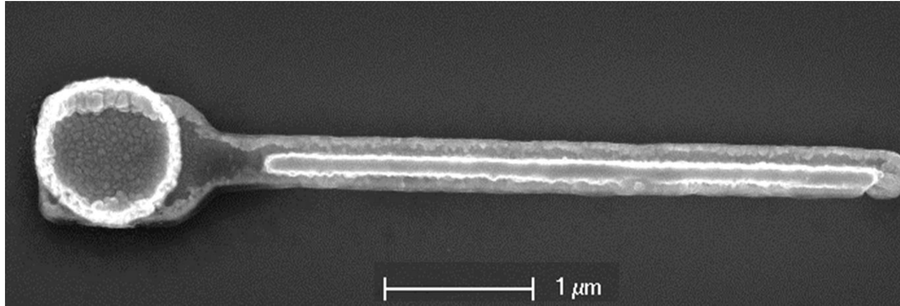


Figure 6.2: Emitter and base fabricated through electron-beam lithography

6.1.3 Results

Two transistor results were presented here, DHBT 43 and DHBT 60. Both devices employ blanket deposited refractory emitter contacts and lifted-off base contacts. The DHBT 43 epitaxial material was designed for high f_{max}, while the design for DHBT 60 was for a more balanced f_τ and f_{max}, achieved through thinner base and collector while scaling junction areas. Both devices were characterized with network analyzers using a two-part calibration and pad stripping with coplanar pad structures. Isolated pads in DHBT 60 offered a substantial improvement in data quality over the data for DHBT 43. Tab 6.2 compares the important parameters of the two devices.

6.2 Future Work

Further scaling of InP bipolar transistors for increases in RF performance will require further process developments to yield emitter and base contacts of less than 100 nm width, and base contacts with less than 25 nm of misalignment. As emitter and base contact stripes become narrower, and contact resistivities lower, the metal resistance associated with these contacts becomes non-negligible. Further, as the

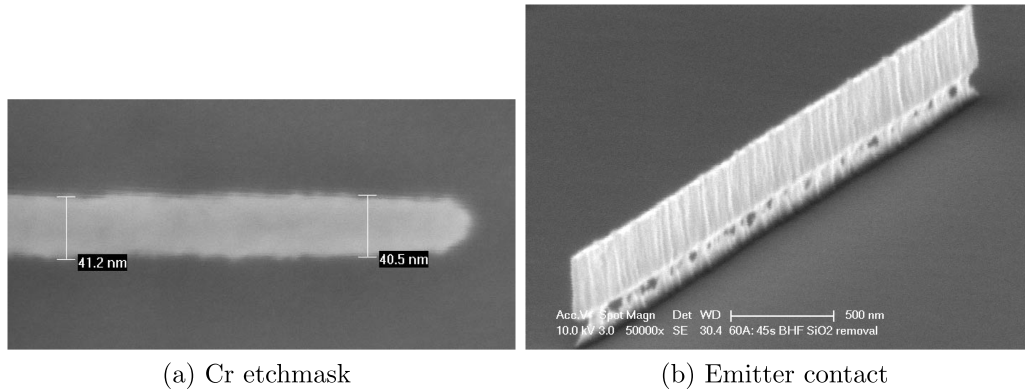
—	DHBT 43	DHBT 60
Emitter mesa width (nm)	200	150
Base thickness (nm)	30	25
Collector thickness (nm)	150	70
Emitter $\rho_{ex}(\Omega \cdot \mu m^2)$	9	2
Base resistance (Ω)	49	40
Collector $\rho_c(\Omega \cdot \mu m^2)$	23.0	12.0
Collector $R_{sh}(\Omega/\square)$	10.0	14.3
Current gain	21	14
Common-emitter breakdown (V)	4.93	2.44
Base ideality factor	1.67	2.72
Collector ideality factor	1.19	1.25
Peak current density (mA/μm^2)	10	27
Peak power density (mW/μm^2)	17	40
Collector-base capacitance (fF)	2.2 + 0.47	2.17 + 0.83
f_τ (GHz)	380	530
f_{max} (GHz)	> 800	750

Table 6.2: Critical parameters of DHBT 43 and DHBT 60

emitter and base are narrowed, the processing involved with these layers becomes more cumbersome and time-consuming. To practically test epitaxial designs and process modifications in an academic research setting, steps to simplify back-end processing and expedite device fabrication is important. Several potential processes and epitaxial designs for future devices will be proposed here. By its nature, this section is more speculative and open-ended than previous sections of this thesis.

6.2.1 Shorter Emitter Contact

Currently, the height of the emitter metal contact is 500 nm, and this height defines the height of the base and collector posts, as well. The emitter height is needed to account for variation across a wafer in the thickness of spun-on benzocyclobutene in the transistor back-end. To prevent metal contacts from shorting emitter and



(a) Cr etchmask (b) Emitter contact

Figure 6.3: Narrowest emitter (a) etchmasks and (b) contacts

base, the BCB must be ashed back below the height of the emitter, but above the base contact.

Electron-beam lithography processes have been developed to define emitter etch masks as narrow as 50 nm, but the dry etch processes used to define the full emitter contact are not anisotropic enough to prevent undercut during the etch which destroys the emitter contact. Furthermore, the metal resistance associated with a 500 nm sputtered $W/Ti_{0.1}W_{0.9}$ emitter is $\sim 0.5\ \Omega \cdot \mu\text{m}^2$, a substantial part of the $\sim 3\ \Omega \cdot \mu\text{m}^2$ extrinsic emitter resistance.

A possible solution to these emitter problems would be to do a two-part emitter contact, similar to T-gates used in many FET devices [1]. A short, $\sim$ 100 nm tall emitter could be formed through established sputter and dry etch processes as narrow as 25 nm [2]. The emitter semiconductor could be etched and base contact formed as in current processes, at which point a preliminary BCB planarization could be done, exposing the tops of the emitter. BCB thickness should be more uniform across the sample at this point in the process, due to the lack of large back-end features and the feature height variation of only $\sim$ 150 nm. On top of this

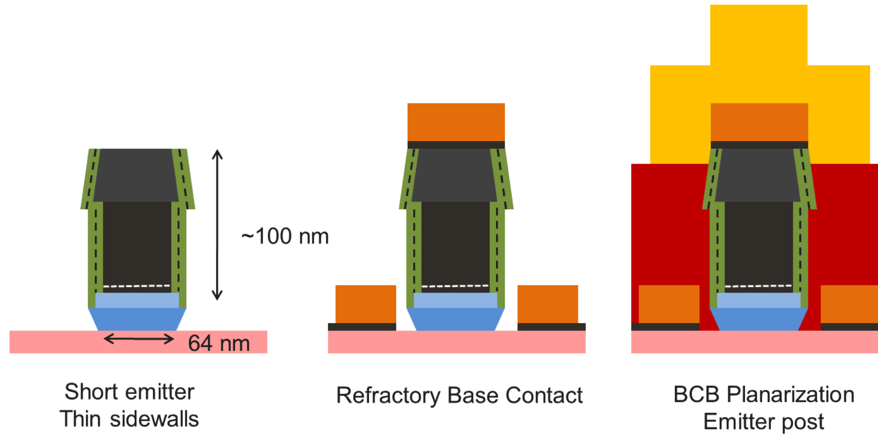


Figure 6.4: Proposed process flow for short emitter

BCB, thicker, wider Au emitter posts could be lifted off to give sufficient emitter height for the second BCB planarization in the back-end process. This would reduce both total emitter metal resistance and mitigates stress and dry etch issues with the refractory portion of the emitter. The success of this process hinges on the ability to planarize the initial BCB layer to a tolerance within $\sim$ 50 nm. Another option would be to surround the initial emitter with a thick ($\sim$ 100 nm) dielectric sidewall on which to deposit the emitter post, although care would be needed to insure this would not interfere with the base post formation, nor damage the semiconductor of the emitter mesa or the gap region between emitter and base contacts.

A consequence of switching to the short emitter would be to make traditional microstrip transmission line pads unusable. Because the dielectric height would become very thin, the signal lines of the microstrip would have to be very narrow to make 50 Ω transmission lines. Coplanar pads, or inverted microstrip lines would be necessary, as used previously [3]. Au electroplating techniques are being developed at UCSB to expedite this more involved back-end process.

6.2.2 Refractory Base Contacts

Ex-situ W contacts to p-type have been demonstrated with contact resistivity $< 1\ \Omega\cdot\mu\text{m}^2$ [4]. These contacts are desirable both for their low contact resistivity and their low diffusivity into the base semiconductor, allowing thinner base epitaxial layers. Preliminary processes in forming base contacts with refractory metals have been developed [5], although these used an interfacial Pd layer which complicated etching of the contact and removed the benefit of thermal stability provided by a refractory contact at the interface.

There are several possible ways to incorporate refractory contacts into a base contact. The simplest, i.e. the one with the least amount of changes from the current process, would be to lift-off a W/Ti/Au base contact instead of Pt/Ti/Pd/Au. W lift-off processes with optical photoresist have been developed [6], but it is not known if the high electron currents needed to electron-beam evaporate W would create x-ray damage to the electron-beam lithography photoresist needed for the base contact. Another disadvantage of this process is exposing the surface of the base semiconductor to photoresist prior to contact deposition would increase the contact resistivity of the contact by $\sim 100\ \%$.

A second potential contact process would be to form the emitter, then blanket evaporate a thin W layer on the base semiconductor surface. On top of this layer, a Ti/Au base contact pad could be lifted off, and this pad could be masked using the base mesa lithographic step. At this point, the thin W in the field could be dry etched away using a low-power etch, while the emitter and base contact are protected by base mesa photoresist.

While electron-beam lithography can be used to achieve alignment with ~ 25 nm

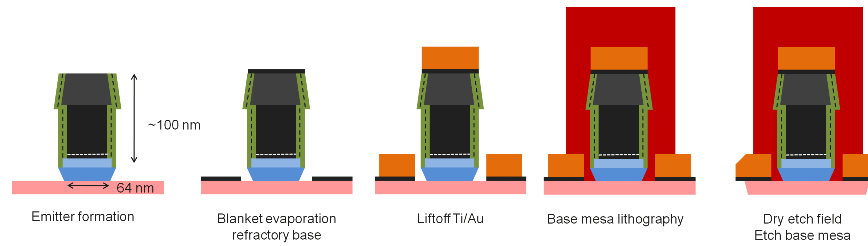


Figure 6.5: Proposed process flow for short emitter

of misalignment between emitter and base, it may not be sufficient for alignment to emitters at the 64 nm emitter node. To achieve near-perfect base-to-emitter alignment, the base contact metal could be blanket deposited, and an etch mask for the base formed by a thick (on the order of the emitter width in thickness) dielectric sidewall around the emitter. The refractory base metal could then be dry etched by ICP. Challenges with this process include incorporating the base post and dealing with the large metal resistance associated with the thin refractory base metal, since no base contact Au layer could be easily deposited and dry etched in this process. This process may be advantageous if a thick sidewall is pursued for the short emitter process described in Sec. 6.2.1.

6.2.3 Regrown Base

For high-frequency performance, the base needs to be as thin as possible. However, the portion of the base where the contacts are deposited needs to be thick enough so deposited contacts will not sink through the base, and so the sheet resistance of the base semiconductor will not be excessively high. These competing requirements for the base can be decoupled by ordering epitaxial material with base layers 10 or 15 nm thick, forming the emitter mesa above this thin base layer, and using molecular-beam epitaxy or metal-organic chemical vapor deposition to regrow thicker, heavily

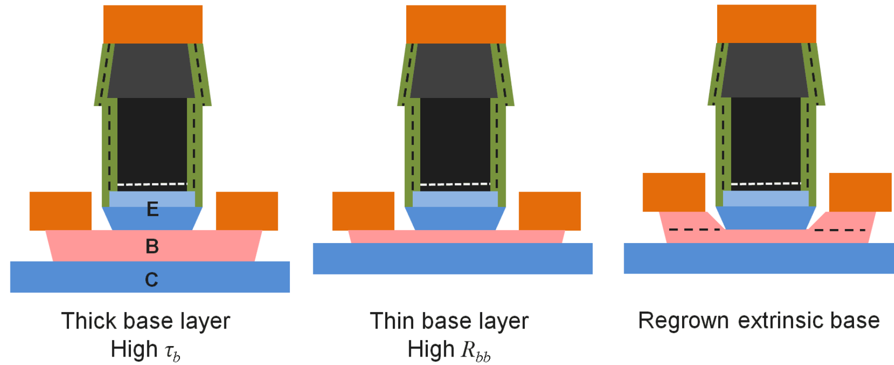


Figure 6.6: Regrown extrinsic base

doped p-type InGaAs outside the intrinsic region of the base upon which contacts can be deposited. Both n-type MOCVD and MBE have been demonstrated in III-V FET processes [8, 7]. MOCVD has the advantage of being less directional and naturally filling in around high aspect ratio features, although the regrowth is less selectively preferential to the semiconductor surface than MBE regrowth. Achieving sufficiently high dopings ($\sim 1 \times 10^{20}$) may be difficult with MOCVD. Achieving close fill-in of regrowth around emitter features and avoiding passivation of base doping by in-situ H cleaning are two issues associated with MBE regrowth. Either process likely involves significant material studies and experiments in process integration, but could provide substantial benefit — reducing the base thickness from 25 to 15 nm halves the base transit time, and for a transistor similar to DHBT 60, would increase f_τ by $\sim$ 100 GHz, as shown in Fig. 6.7.

6.3 Conclusion

The focus of this thesis has been the scaling of InP heterojunction bipolar transistors to set new records in bandwidth. The InP and InGaAs material systems are a

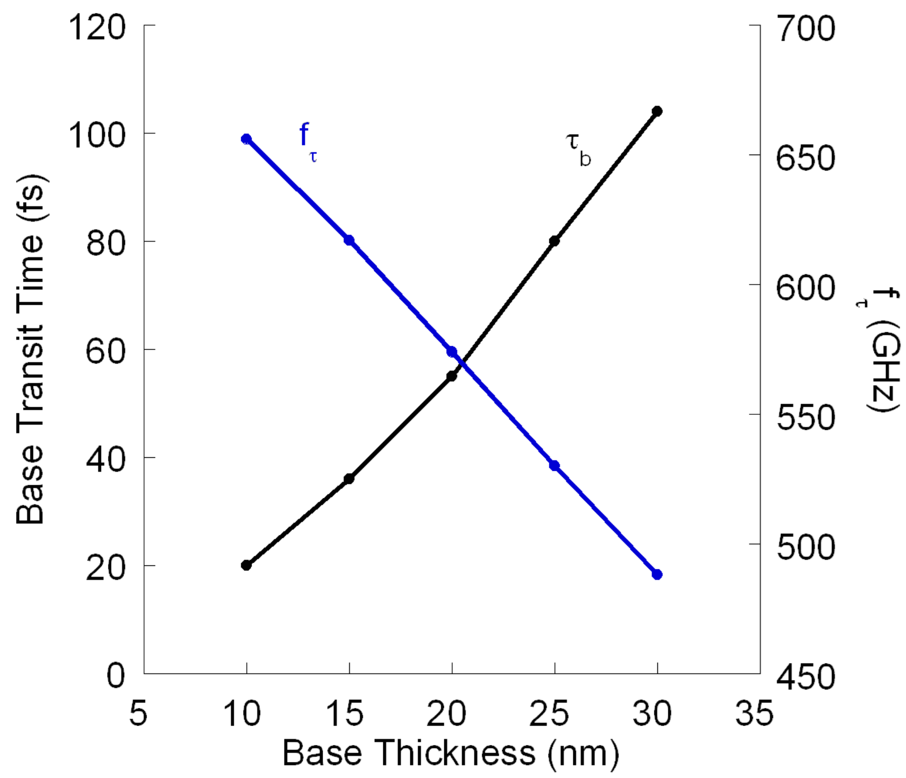


Figure 6.7: Modeled τ_b and f_τ for DHBT 60 with varying base thickness

natural system in which to develop high frequency devices due to the high electron mobility in InGaAs and the high electron saturation velocity in InP. Because current flow in a mesa bipolar transistor is vertical, i.e. perpendicular to the direction of epitaxial growth, very thin devices, can be made by growing thin semiconductor layers through molecular beam epitaxy. As semiconductor layers are thinned, so are the transit times for carriers across these layers. In addition to reducing transit delays, RC time constants associated with the transistor must also be reduced to increase bandwidth. Fortuitously, both n- and p-type contacts to heavily doped InGaAs of less than 2 $\Omega \cdot \mu m^2$ have been developed. Capacitances are minimized through lateral scaling through sophisticated process techniques.

Two transistor results are detailed here, from epitaxial design, to fabrication processes, to measurement techniques, and to DC and RF data. The first result featured a 200 nm wide emitter mesa, and a 150 nm thick collector, leading to f_τ = 360 GHz and $f_{max} >$ 800 GHz. The second result features an emitter mesa narrowed to 150 nm and the collector thinned to 70 nm, resulting in f_τ = 530 GHz and f_{max} = 750 GHz. The methods used to improve these transistors from the first result to the second are described, and, finally, several designs are proposed for future scaling and future improvement of InP HBT bandwidths.

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Appendix A

Small-signal Parameter Extraction

By first considering a simple two-port model for a bipolar transistor, analagous to the small-signal circuit shown in Fig. A.1, admittance parameters can be determined for the circuit.

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{A.1}$$

To evaluate a given admittance parameter Y_{ij}, nodal analysis can be carried out on the small-signal circuit with the appropriate voltage source shorted.

$$Y_{ij} = \left. \frac{I_i}{V_j} \right|_{V \neq j = 0} \tag{A.2}$$

As more complex parasitic terms are added, the resulting perturbations are incorporated in the Y-parameters, but can be truncated to second-order in frequency to maintain simplicity of the model while still giving a good fit to measured data. Eventually, a full hybrid-π model with all parasitic junction resistances and capacitances can be formed, as shown in Fig. A.2

The relationships for base and collector contact resistances R_{bb} and R_c are given in Sec. 2.1.2. The relationships for emitter-base diffusion capacitance C_{diff} and

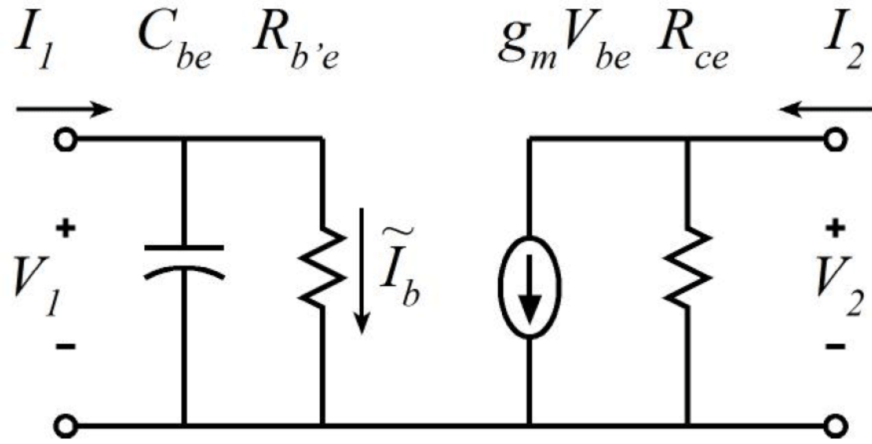

Figure A.1: Standard small-signal model of a bipolar transistor

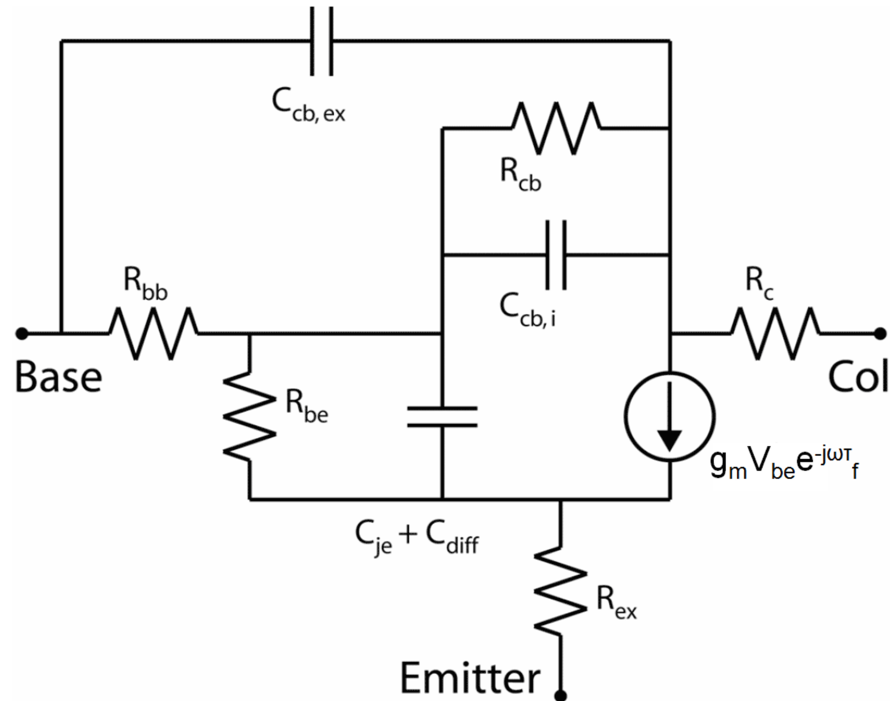

Figure A.2: Hybrid-π small-signal model of HBT with parasitic resistances and capacitances

emitter-base resistance R_{be} below were defined in Sec. 2.5.

$$R_{bb} \approx \frac{\rho_c}{2L_e W_{b,cont}} + \rho_s \frac{W_{b,cont}}{6L_e} + \rho_s \frac{W_{b,gap}}{2L_e} + \rho_s \frac{W_e}{12L_e} \tag{A.3}$$

$$R_c \approx \frac{\rho_s}{2L_e} \left(L_T + W_{c,gap} + W_b\right) \tag{A.4}$$

In each equation, ρ_c, ρ_s, and L_T refer to the values for the respective semiconductor layer.

$$C_{diff} = g_m \left(\tau_b + \tau_c\right) \tag{A.5}$$

$$R_{be} = \frac{\beta}{g_m} \tag{A.6}$$

The following relationships can be derived from analysis of the two-port hybrid-π model:

$$\Re\left\{Y_{11}\right\} = \frac{1}{R_{be}} + \omega^2 \left(C_{je} + Cdiff\right) R_{bb} \tag{A.7}$$

$$\Im\left\{Y_{11}\right\} = \omega C_{be} \tag{A.8}$$

$$\Re\left\{Y_{12}\right\} = \frac{1}{R_{cb}} + \omega^2 \left(C_{be} + C_{cb,i}\right) C_{cb,i} R_{bb} \tag{A.9}$$

$$\Im\left\{Y_{12}\right\} = \omega C_{cb} \tag{A.10}$$

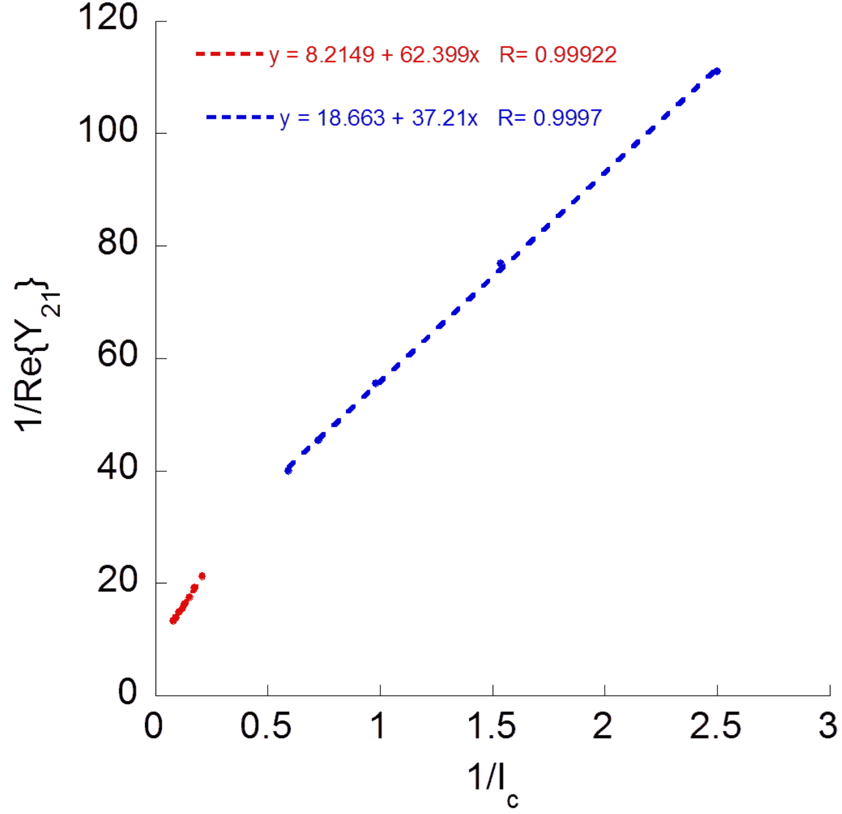

Figure A.3: High current densities are used to extract R_{ex} and g_m

$$\frac{1}{\Re\{Y_{21}\}} = R_{ex} + \frac{R_{bb}}{\beta} + \frac{\eta k_B T}{q I_e} \tag{A.11}$$

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + (R_{ex} + R_c) C_{cb} + \left(\frac{\eta k_B T}{q I_c}\right)(C_{je} + C_{cb}) \tag{A.12}$$

Using the equations above, the components in the small-signal hybrid-π model shown in Fig. A.2 can be methodically determined.

1. Measure $\Re\{Y_{21}\}$ at as wide a range of I_c biases as possible. Pick low-frequency (e.g. $\sim$ 1 GHz) point at which to select Y_{21} value at each bias point. Plot

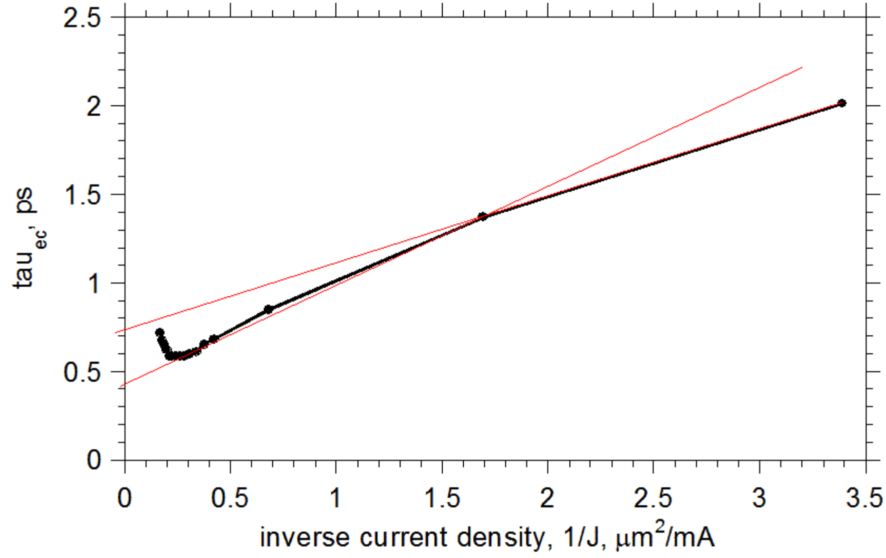

Figure A.4: τ_{ec} vs. $\frac{1}{I_c}$ plot demonstrating current-induced velocity overshoot

$\frac{1}{Y_{21}}$ vs $\frac{1}{I_c}$ for high current densities (close to where peak RF performance was obtained) and make a linear fit to these data. From Eq. A.11, the quantity $R_{ex} + \frac{R_{bb}}{\beta}$ is the intercept, and η can be extracted from the slope, assuming $\frac{k_B T}{q} \sim 0.026$ V. Low current densities will give spuriously high R_{ex} and low g_m values, as shown in Fig. A.3.

2. DC current gain β can be calculated at a given bias point from $\frac{I_c}{I_b}$.

3. Transconductance g_m at a given bias point can be calculated using $g_m \equiv \frac{qI_c}{\eta k_B T}$, with known I_c, and the slope from step 1.

4. R_{be} can now be calculated using Eq. A.6.

5. Measure $\Re\{Y_{12}\}$ at a particular bias point. Extract R_{cb}, since at low frequencies, $\Re\{Y_{12}\} \approx R_{cb}$.

6. Plot $\frac{\Im\{Y_{12}\}}{2\pi f}$ at a particular bias point. Extract C_{cb} from a low-frequency point

on this graph.

7. Measure on-wafer TLM structures for the base and collector. Extract ρ_c from the intercept and ρ_s from the TLM measurements, and use the base and collector contact geometries to determine R_{bb} and R_c, using Eqs. A.3 and eq:rccapp.

8. Estimate R_{ex} by subtracting off the extracted $\frac{R_{bb}}{\beta}$ term.

9. Measure h_{21} at as wide a range of I_c biases as possible, especially low currents ~ 2 mA, where current modulation in the collector is negligible (See Fig. A.4 for a typical τ_{ec} plot, with a lower extracted $\tau_b + \tau_c$ at higher I_c, due to enhanced velocity overshoot). Extract f_τ from these h_{21} plots, and make a new plot of $\frac{1}{2\pi f_\tau}$ vs. $\frac{1}{I_c}$.

   From Eq. A.12, the intercept of that plot will be $\tau_b + \tau_c + (R_{ex} + R_c)\, C_{cb}$, and the values of R_{ex}, R_c, and C_{cb} are known from the previous steps, so $\tau_f \equiv \tau_b + \tau_c$ can be extracted.

   Again from Eq. A.12, the slope of the graph will be $\frac{\eta k_B T}{q} (C_{je} + C_{cb})$. $\frac{\eta k_B T}{q}$ is known from the extraction in step 1 and C_{cb} is known from step 6, so C_{je} can be extracted.

10. Fictional capacitance C_{diff} can now be calculated using extracted τ_f and g_m and Eq. A.5.

11. All the extracted parameters thus far should be added to a “tunable” hybrid-π model of the device in ADS, and the remaining parameters will be tuned in a particular order to obtain good agreement between modeled and measured RF data.

12. Fine-tune R_{be} to adjust the DC value of $\Re\{Y_{11}\}$ and R_{bb} to adjust the curvature of $\Re\{Y_{11}\}$ to fit the measured data.

13. After adjusting R_{bb}, recalculate and re-adjust R_{ex} with the new amount of R_{bb} subtracted off. Iteratively re-adjust g_m and R_{be} as well until good agreement between measured and modeled S- and Y-parameters and h_{21} is obtained.

14. By definition, Mason's Unilateral Gain only depends on the intrinsic portion of the base-collector capacitance, $C_{cb,i}$. Eq. A.9 shows $\Re\{Y_{12}\}$ depends quadratically on $C_{cb,i}$, so tune this value while monitoring the curvature of $\Re\{Y_{12}\}$ and U, while maintaining constant total $C_{cb} = C_{cb,i} + C_{cb,ex}$.

15. Tune τ_c and C_{BCB} in the hybrid-π model to get good agreement between $\Im\{Y_{21}\}$ and $\Im\{Y_{22}\}$.

Appendix B

Current HBT Process Flow

This appendix describes the state of the DHBT mesa process flow with lifted off base contacts, as of July 2011. Further updates may be found on the Rodwell Group Wiki.

Sample Preparation

- Cleave 4 in wafer into pieces, at least 1.0 in^2. MBE faceplates requires samples with sides nominally of length 1.0, 1.2, or 1.4 in. The number 2 cassette for the JEOL electron-beam writer has windows 25 $\times$ 45 mm; at least one side of the sample must be larger than one of the window dimensions to hold the sample in place.

- If not obvious from the sample shape, make light marks with a scribe on the back of the sample indicating the direction of the major flat (the one below the serial number on IQE wafers).

Emitter Surface Preparation

- Perform standard solvent clean on sample: 3 m each Acetone, Isopropyl Alcohol, and lightly flowing DI H_2O.

- Place sample in 115 °C oven for 10 min to dehydration bake.
- Turn on UV-O_3 oven and let it run empty for 15 m. Load sample and run in UV-O_3 for 10 m.
- At the acid bench, prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.
- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O.
- *Immediately* load sample in E-Beam #1 evaporator.

Emitter Mo Evaporation

- Load Mo in pocket #1 and pump down with sample holder but no sample in the chamber. Pump down to 1.0e-6 T.
- Dummy evaporate 20 nm of Mo at 0.5 Å/s. This should be done *prior* to the sample surface preparation above, so the chamber can be vented and the sample immediately transferred to it and pumped down after HCl:H_2O soak.
- When base pressure reaches 1.0e-6 T, deposit 20 nm Mo on sample at 0.5 Å/s.

Note: If possible, the next 3 steps should be performed in immediate succession. If not, a standard solvent clean and dehydration bake should be performed prior to the next deposition.

Emitter W/$Ti_{0.1}W_{0.9}$ Calibration and Deposition

Prior to depositing the emitter metal on the actual sample, one or more calibration runs may be necessary to find the right pressures for the W and $Ti_{0.1}W_{0.9}$ depositions

to reduce the stress in the sample below ~ 150 MPa — a value empirically found to be sufficiently low to promote good emitter yield.

Note: $Ti_{0.1}W_{0.9}$ source is 10% Ti by *weight*, not atomic composition.

- Remove public Ti (pocket #1) and Cr (pocket #4) from the Sputter #1 tool.
- Load public W source in pocket #1 and private $Ti_{0.1}W_{0.9}$ source in pocket #4, along with their Cu shims, annular cathodes, and appropriate shieldings.
- Measure initial wafter curvature in Tencor Stress Measurement tool, then load dummy Si wafer and pump down to 5.0e-7 T, using LN_2 in the cold trap.
- Dummy sputter (shutter closed) W for 15 m, at 25 sccm Ar, 200W, and whatever the most recent good pressure is (as of this publication, 21 mT). Open the shutter, and deposit on the dummy for 8 min.
- Vent, and measure the stress after deposition. Cleave the wafer in half, and take a cross-sectional SEM to verify the film thickness is ~ 250 nm.
- If the stress (corrected for actual film thickness) is greater than 150 MPa, repeat the W deposition calibration on a fresh Si wafer. Adjust the pressure during deposition by 0.5 mT, increasing the pressure makes the film more tensile. Adjust the deposition time linearly to make the film thicker.
- Once the W film has been calibrated, deposit a join W/$Ti_{0.1}W_{0.9}$ stack on a Si wafer, again measuring the wafer curvature before loading in the chamber. Deposit at 5.0e-7 T, with W and $Ti_{0.1}W_{0.9}$ sources in the same pockets as described above. Do the low-stress W deposition, then dummy sputter the

$Ti_{0.1}W_{0.9}$ source for 15 m at 25 sccm Ar, 200W, and the most recent good pressure (17 mT). Open the shutter and deposit on the sample for 23 min.

- Vent, measure total metal stack stress, and cleave the wafer to conduct cross-sectional SEM. If stress is more than 150 MPa, redo $W/Ti_{0.1}W_{0.9}$ deposition, incrementing deposition time and rate as necessary.
- Once a stable $W/Ti_{0.1}W_{0.9}$ recipe has been established, load the actual InP sample(s) and deposit it on the surface.

Note: If sputter calibration has been performed recently, it may be possible to skip the standalone W and deposition rate calibrations, and start from the joint $W/Ti_{0.1}W_{0.9}$ calibration. If that doesn't appear to converge after several iterations, it may be necessary to start over with the W-only deposition.

Sacrificial SiO_x Deposition

- Vent PlasmaTherm PECVD chamber. Wipe inside walls with Iso-soaked paper wipe. Pump chamber and run standard 30 m SiO_x clean.
- Vent chamber and load sample in center of chamber. Pump down.
- Run standard 1000 Å SiO_x deposition.

Cr Etch Mask Deposition

- Vent E-beam Evaporator #1 and load Cr in pocket #3. Load sample.
- Pump down to 3e-6 T.
- Deposit 40 nm of Cr at 1–3 Å/s.

Emitter Lithography

- Clean sample with standard solvent clean and dehydration bake.
- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Nudge sample with tweezers at edge to verify vacuum is holding it in place. Step on foot pedal to test spin (with no photoresist on the sample). As soon as the chuck starts spinning, step on foot pedal again to stop the chuck. If the sample feels loose or the trial spin gives a vacuum error, remove the sample and replace it. Cleaning the back of the sample and cleaning or replacing the spinner chuck may be necessary.
- Use pipette to place drops of HMDS coating the sample surface. Let sit for 20 s, then spin with standard 30 s 4000 rpm recipe (#7). Wait 60 s before applying next photoresist layer.
- Cut end off a clean pipette and attach it to the end of a syringe. Withdraw enough ma-N 2403 to half fill the pipette stem, and then pull the syringe back to bring all the photoresist into the syringe. Remove the pipette end from the syringe, and attach a 0.2 μm filter.
- Push the photoresist through the filter, covering the sample uniformly in droplets.
- Spin for 30 s at 4000 rpm (recipe #7). If any large spots or solid particulates in the resist appear near the center of the sample, strip the photoresist in 80 °C 1165 for 15 m, followed by a 5 m O_2 descum at 300 mT and 100 W in the PE-II plasma etcher (O_2 only). Redo the photoresist application.
- Softbake at 90 °C for 90 s.

- Return sample to spinner chuck, again verifying vacuum is solidly holding the sample in place.
- Apply aquaSAVE using pipette, taking care to make sure edges of the sample are fully covered with drops.
- Spin sample for 30s at 3000 rpm (recipe #6).
- Softbake at 95 °C for 15s.
- Load the sample in the #2/2E cassette for the E-Beam writer. Turn the casette upside down on the table, so the handle is on the left side, and the 2E holder is in the upper left corner. Place the sample in the holder so the major flat of the wafer is parallel to the bottom of the casette, and perpendicular to the holder. Nudge the sample until it is centered vertically in the 2E window.
- Load casette in the E-Beam writer, and perform necessary calibrations and exposure.
- After exposure, rinse in DI H_2O for 1 m to remove aquaSAVE.
- Develop in beaker of AZ 300MIF for 35 s with gentle agitation every 10 s, then rinse in DI H_2O for 2 m.
- Verify lithography came out as expected under optical microscope.

Emitter Cr Etch

- Put the Panasonic ICP #1 into 'CONT' mode.
- Take a reasonably shiny looking 6 in Si carrier wafer from the "Cl_2/O_2" section of the Rodwell ICP carrier wafer box. Clean it with acetone from a spray

bottle, then wipe dry with a non-shedding wipe. Repeat with isopropyl alcohol from a spray bottle, and dry the wafer with the N_2 gun.

- Load the wafer in one of the ICP's cassettes, and run the standard O_2 clean (recipe # 121) for 10 m.

- Clean a second wafer from the "Cl_2/O_2" portion of the box identically to the first.

- Using the dropper in the bottle, place a dewdrop sized droplet of Santovac oil in the center of the wafer. Place the sample on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Load the wafer in the other ICP casette and run a Cl_2/O_2 etch with 26/4 sccm of gas flow, 1 Pa pressure, and 400/15 W of source and bias power, for 2:30.

- When the sample returns from the etcher, the surface should look uniformly indigo, indicating all the Cr in the field has been etched away to expose the SiO_x below. Immediately transfer the sample to a beaker of DI H_2O, and take it to the developer benches to rinse for 2 m.

- Transfer the sample to a beaker of 1165, pre-heated in the 80 °C bath in the E-Beam lithography bay. Leave the sample and beaker of 1165 in the bath for 30 m, then transfer the sample to isopropyl and then DI H_2O rinse for 3 m each.

- Descum the sample for 1 m in the O_2 only PE-II asher at 300 mT and 100 W.

- Inspect the Cr etch mask with top-down SEM – verify the field and features are clear of photoresist scum or Cr particles, the stitching offsets within features are ∼10 nm or less, and record the actual widths of the emitters after the etch. If the etch is unsatisfactory in any way, redo the Cl_2/O_2 etch on the entire sample, redeposit a new Cr layer through E-Beam evaporation, and redo the lithography and etch.

Emitter Contact Dry Etch

- Put the Panasonic ICP #1 into 'CONT' mode.
- Take a reasonably shiny looking 6 in Si carrier wafer from the "SF_6/Ar" section of the Rodwell ICP carrier wafer box. Clean it with acetone from a spray bottle, then wipe dry with a non-shedding wipe. Repeat with isopropyl alcohol from a spray bottle, and dry the wafer with the N_2 gun.
- Load the wafer in one of the ICP's cassettes, and run the standard O_2 clean (recipe # 121) for 10 m. If the plasma does not look dim and white during the O_2 clean, the chamber has not been fully cleaned, and a longer O_2 clean is necessary.
- Clean a second wafer from the "SF_6/Ar" portion of the box identically to the first.
- Load the wafer in the other cassette, and run a 3 m SF_6/Ar condition step at 25/5 sccm, 1 Pa, and 600/150 W power (recipe # 162). The plasma should look light blue.
- When the first wafer is returned from the system, place a dewdrop sized droplet of Santovac oil in the center of the wafer. Place the sample on top of

this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Run the same 3 m, high-power SF_6/Ar etch on the wafer with the sample. When it returns, the sample should be ~75% silvery, with the metal not entirely etched from the field except at the sample edges. If this is not the case, repeat the high-powered etch in 15 s increments until this is the case.

- Run a 1:30 SF_6/Ar etch at 5/5 sccm, 0.5 Pa, and 600/15 W power (recipe #173) to clear the field of the remaining W. The sample should return with a uniform blue surface, indicating the metal has been removed. If not, change the bias power from 15 W to 50 W, and re-run the etch for an additional 30 s.

- Immediately rinse the sample, while still attached to the carrier wafer, with H_2O from a spray bottle. If the surface is *not* hydrophobic, i.e. water does not bead up, dry the sample with the N_2 gun and redo the 50 W etch for an additional 15 s. If the surface is hydrophobic, use a wooden swab to push the sample off the carrier wafer.

- Transfer the sample to a beaker of DI H_2O, and rinse for 2 m at the developer bench. Follow with a standard solvent clean, and dry with N_2 at <20 psi.

- Inspect the device in angled SEM. Check device yield for full range of emitter widths, verify emitter profile is near vertical, and inspect field for etch completion.

Note: The given SF_6/Ar recipes above and CF_4/O_2 recipes below are frequently altered by other users. Make sure to verify *all* settings — source and bias powers,

gas flow rates, pressure, and duration of etch. Frequently, low-pressure recipes such as #134 will have a higher pressure during the ignition stage. This is normal, but double-check the pressure drops to the proper value during the etch step.

First Sidewall Formation

- Vent PlasmaTherm PECVD chamber. Wipe inside walls with Iso-soaked paper wipe. Pump chamber and run standard 30 m Si_xN_y clean.
- Vent chamber and load 2 in Si wafer in center of chamber. Place glass slides above and to the left of the wafer to hold it in place. Pump down.
- Run standard 1000 Å Si_xN_y deposition. Even if other dummy samples with Si_xN_y are available for calibration, this step *must* be done to properly condition the chamber for the real deposition.
- At the acid bench, prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.
- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O.
- Dry sample with N_2 gun at >20 psi, immediately transfer to open PECVD chamber, remove dummy wafer, and pump down.
- Run standard 300 Å Si_xN_y deposition.
- Cleave the dummy Si wafer in half. Measure the film thickness at 3 points across one of the half wafers using Brian Thibeault's standard Si_xN_y-on-Si recipes for the Woolam Spectroscopic Ellipsometer.

- Put the Panasonic ICP #1 into 'CONT' mode.

- Take a reasonably shiny looking 6 in Si carrier wafer from the "CF_4/O_2" section of the Rodwell ICP carrier wafer box. Clean it with acetone from a spray bottle, then wipe dry with a non-shedding wipe. Repeat with isopropyl alcohol from a spray bottle, and dry the wafer with the N_2 gun.

- Load the wafer in one of the ICP's cassettes, and run the standard O_2 clean (recipe # 121) for 10 m.

- Clean a second wafer from the "CF_4/O_2" portion of the box identically to the first.

- Load the wafer in the other cassette, and run a 5m CF_4/O_2 ICP etch with 20/5 sccm gas flow, 1 Pa pressure, and 500/100 W powers to condition the chamber (recipe #138).

- When the first wafer is returned from the system, place a dewdrop sized droplet of Santovac oil in the center of the wafer. Place the dummy Si sample on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Run a 4 m CF_4/O_2 etch with 20/2 sccm, 0.3 Pa, and 25/15 W powers on the wafer with the Si dummy (recipe #134). No plasma will be visible in the chamber during this etch.

- When the dummy sample is returned, rinse with DI H_2O and remove from the carrier wafer with wooden swabs. Return to the Ellipsometer and re-measure

the film thickness at the same three points. Calculate an average etch rate based on the before- and after-etch thicknesses.

- Place a dewdrop sized droplet of Santovac oil in the center of the clean carrier wafer. Place the HBT on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Based on the calculated etch rate, run the low-powered CF_4/O_2 etch for long enough to etch 360 nm of Si_xN_y (20% overetch) on the carrier wafer with the HBT sample.

- Immediately rinse the sample, while still attached to the carrier wafer, with H_2O from a spray bottle. Gently remove the sample from the wafer with a wooden swab, and transfer the sample to a beaker of DI H_2O, and rinse for 2 m at the developer bench. Follow with a standard solvent clean, and dry with N_2 at $<$20 psi.

- Inspect the device in angled SEM. Check device yield for full range of emitter widths, and verify field is clear.

Emitter InGaAs Wet Etch

- Measure and record stack height at several different points on the sample using the DEKTAK Profilometer.

- At the acid bench, prepare a beaker of 200 mL DI H_2O and 20 mL of NH_4OH, as well as a beaker of 250 mL H_2O, 10 mL H_3PO_4 and 10 mL H_2O_2. Add stirrers to the 1:1:25 H_3PO_4:H_2O_2:H_2O beaker, and place on a *room temperature hot plate* set to stir at $\sim$ 250 rpm.

- Gently agitate the $NH_4OH{:}H_2O$ beaker by hand for several seconds. Place the sample in the $NH_4OH{:}H_2O$ for 10 s, and immediately rinse under DI H_2O for another 10 s. Dry with N_2 at $<$20 psi.

- Move InGaAs etchant from hot plate to bench. Dip sample in etchant for 5-7 s, and remove from etchant as soon as the sample has uniformly changed color. Rinse under DI H_2O for 2 m. Dry with N_2 at $<$20 psi.

- Inspect under optical microscope to make sure field looks uniform. Measure stack heigh using Profilometer. The height difference should correspond to thickness of emitter InGaAs layer.

Note: The etch rate for 1:1:25 $H_3PO_4{:}H_2O_2{:}H_2O$ is $\sim$ 120-160 nm/min. Scale the etch appropriately based on the InGaAs cap thickness, but always inspect visually during etching.

Cr Etch Mask Removal

- Perform a standard solvent clean and dehydration bake on the sample.

- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Nudge sample with tweezers at edge to verify vacuum is holding it in place. Step on foot pedal to test spin (with no photoresist on the sample). As soon as the chuck starts spinning, step on foot pedal again to stop the chuck. If the sample feels loose or the trial spin gives a vacuum error, remove the sample and replace it. Cleaning the back of the sample and cleaning or replacing the spinner chuck may be necessary.

- Apply SPR 955CM-1.8 photoresist to the sample with a pipette, ensuring the entire sample is uniformly covered with droplets.

- Spin the photoresist at 4000 rpm for 30 s (recipe #7).
- Soft-bake the sample for 60 s on the 90 °C hotplate.
- Use Nanometrics Reflectometer with recipe #10 and a dielectric constant of 1.6 to veriy the photoresist thickness. It should be $\sim$ 1.6 μm.
- Run the "O_2 Only" PE-II Plasma Etcher empty for 5 m at 300 mT and 300 W. Reduce the power down to 200 W.
- Vent the PE-II, load the sample, and pump down. Ash the photoresist for 8 m at 300 mT and 200 W.
- Remove the sample and re-measure the photoresist thickness at several points using the Nanometrics. Calculate an average etch rate based on the before- and after-etch thickness measurements.
- Based on the calculated etch rate, ash the sample in the PE-II at 300 mT and 200 W for an additional amount of time, until the photoresist height is $\sim$ 2000 Å below the emitter stack height measured via profilometer after wet etching. This may require a couple iterations of ashing and thickness measurement.
- Hard-bake the sample for 60 s on the 110 °C hotplate.
- Soak the sample in buffered HF for 55 s. Immediately transfer to a DI H_2O rinse for 2 m. Dry with N_2 at $<$20 psi.
- Transfer sample to 1165 in 80 °C bath for 30 m.
- Perform standard solvent clean.

- Descum the sample for 30s in the "O_2 Only" PE-II asher at 300 mT and 100 W.
- Inspect with angled SEM. Check that field and emitters are free of photoresist scum, and that Cr caps have been lifted off from all emitter widths and have not fallen back on the emitters themselves.

Second Sidewall Formation

Note: The second sidewall deposition and etch procedures are identical to the first.

- Vent PlasmaTherm PECVD chamber. Wipe inside walls with Iso-soaked paper wipe. Pump chamber and run standard 30 m Si_xN_y clean.
- Vent chamber and load 2 in Si wafer in center of chamber. Place glass slides above and to the left of the wafer to hold it in place. Pump down.
- Run standard 1000 Å Si_xN_y deposition. Even if other dummy samples with Si_xN_y are available for calibration, this step *must* be done to properly condition the chamber for the real deposition.
- At the acid bench, prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.
- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O.
- Dry sample with N_2 gun at >20 psi, immediately transfer to open PECVD chamber, remove dummy wafer, and pump down.

- Run standard 300 Å Si_xN_y deposition.
- Cleave the dummy Si wafer in half. Measure the film thickness at 3 points across one of the half wafers using Brian Thibeault's standard Si_xN_y-on-Si recipes for the Woolam Spectroscopic Ellipsometer.
- Put the Panasonic ICP #1 into 'CONT' mode.
- Take a reasonably shiny looking 6 in Si carrier wafer from the "CF_4/O_2" section of the Rodwell ICP carrier wafer box. Clean it with acetone from a spray bottle, then wipe dry with a non-shedding wipe. Repeat with isopropyl alcohol from a spray bottle, and dry the wafer with the N_2 gun.
- Load the wafer in one of the ICP's cassettes, and run the standard O_2 clean (recipe # 121) for 10 m.
- Clean a second wafer from the "CF_4/O_2" portion of the box identically to the first.
- Load the wafer in the other cassette, and run a 5m CF_4/O_2 ICP etch with 20/5 sccm gas flow, 1 Pa pressure, and 500/100 W powers to condition the chamber (recipe #138).
- When the first wafer is returned from the system, place a dewdrop sized droplet of Santovac oil in the center of the wafer. Place the dummy Si sample on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.
- Run a 4 m CF_4/O_2 etch with 20/2 sccm, 0.3 Pa, and 25/15 W powers on the wafer with the Si dummy (recipe #134). No plasma will be visible in the

chamber during this etch.

- When the dummy sample is returned, rinse with DI H_2O and remove from the carrier wafer with wooden swabs. Return to the Ellipsometer and re-measure the film thickness at the same three points. Calculate an average etch rate based on the before- and after-etch thicknesses.

- Place a dewdrop sized droplet of Santovac oil in the center of the clean carrier wafer. Place the HBT on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Based on the calculated etch rate, run the low-powered CF_4/O_2 etch for long enough to etch 360 nm of Si_xN_y (20% overetch) on the carrier wafer with the HBT sample.

- Immediately rinse the sample, while still attached to the carrier wafer, with H_2O from a spray bottle. Gently remove the sample from the wafer with a wooden swab, and transfer the sample to a beaker of DI H_2O, and rinse for 2 m at the developer bench. Follow with a standard solvent clean, and dry with N_2 at $<$20 psi.

- Inspect the device in angled SEM. Check device yield for full range of emitter widths, and verify field is clear.

Emitter InP Etch

- Measure and record stack height at several different points on the sample using the DEKTAK Profilometer.

- At the acid bench, prepare a beaker of 200 mL DI H_2O and 20 mL of NH_4OH, as well as a beaker of 200 mL H3PO_4 and 50 mL. Add stirrers to the 4:1 H_3PO_4:HCl beaker, and place on a *room temperature hot plate* set to stir at $\sim$ 250 rpm.

- Gently agitate the NH_4OH:H_2O beaker by hand for several seconds. Place the sample in the NH_4OH:H_2O for 10 s, and immediately rinse under DI H_2O for another 10 s. Dry with N_2 at $<$20 psi.

- Move InP etchant from hot plate to bench. Dip sample in etchant for $\sim$10 s, and remove from etchant about 2 s after the sample has uniformly changed color. The surface should become covered in bubbles that slowly rise away from it during the etch. Rinse under DI H_2O for 2 m. Dry with N_2 at $<$20 psi.

- Inspect under optical microscope to make sure field looks uniform. Measure stack heigh using Profilometer. The height difference should correspond to thickness of emitter InP layer.

Due to the sensitivity of the base semiconductor to surface oxides and contaminants, and the delicacy of the chemically amplified UV-6 photoresist, it is best if the emitter InP wet etch, base lithography, and base contact liftoff are done in immediate succession.

Base Contact Lithography

- Remove UV-6 from fridge and allow to warm up for at least 1 hr prior to opening the bottle.

- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Nudge sample with tweezers at edge to verify vacuum is holding it in place. Step on foot pedal to test spin (with no photoresist on the sample).
- Use pipette to place drops of HMDS coating the sample surface. Let sit for 20 s, then spin with standard 30 s 4000 rpm recipe (#7). Wait 60 s before applying next layer of photoresist.
- Apply UV-6 to the surface of the sample with a pipette, insuring full sample coverage and no bubbles. Spin photoresist at 3000 rpm for 60 s.
- Pre-bake the sample for 60 s on the 115 °C hotplate.
- Return sample to spinner chuck, again verifying vacuum is solidly holding the sample in place.
- Apply aquaSAVE using pipette, taking care to make sure edges of the sample are fully covered with drops.
- Spin sample for 30s at 3000 rpm (recipe #6).
- Softbake at 95 °C for 15s.
- Load the sample in the #2/2E cassette for the E-Beam writer as precisely in the same place as it was for the emitter write as possible. Move the cassette, still facedown, to the glass jig and perform the necessary manual rotational corrections.
- Load casette in the E-Beam writer, and perform necessary calibrations, alignments, and exposure.

- After exposure, rinse in DI H_2O for 1 m to remove aquaSAVE.
- Postbake for 120 s on the 115 °C hotplate.
- Develop in a beaker of AZ 300MIF for 70 s, with gentle agitation every 10 s, then rinse in Di H_2O for 2 m and dry with N_2 gun at <20 psi.
- Verify lithography came out as expected under optical microscope.
- Inspect sample under optical microscope for alignment, focus checkers.

Base Contact Liftoff

- Prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.
- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O.
- *Immediately* load sample in E-Beam #4 evaporator, with long axis of emitters in the direction of rotation. Mask the edges of the sample with Al foil, taped down with Kapton tape, to facilitate the liftoff. Also load private Pt, Ti, Pd, and Au sources, and pump the system down.
- Pump until system reaches $<2 \times 10^{-6}$ T.
- After the ramp/soak cycle for each source deposition, switch to manual mode, with the shutter also manually closed, and soak for an additional 2 m at 4-5% higher power than during the deposition itself.
- Deposit 25 Å Pt at 0.2 Å/s.

- Deposit 170 Å Ti at 1.0 Å/s.
- Deposit 170 Å Pd at 1.0 Å/s.
- Deposit 650 Å Au at 1.0 Å/s.
- At least 30 m before end of deposition, heat up beaker of 1165 in the 80 °C bath. After metal deposition, vent the chamber and transfer the sample to the 1165 beaker in the bath, using a sample holder that orients the sample facedown in the beaker.
- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 10 m. If metal has not lifted off after 30 m, leave it for an additional 30 m, continuing to agitate. Try to *gently* peel any edges of the metal film away from the sample with carbon-tipped tweezers.
- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at <20 psi.
- Inspect with top-down SEM to verify base contact dimension and alignment, and emitter yield. Inspect with angled SEM to verify emitter height and break in lifted off base metal.

Base Post Lithography

- Measure the heights of the emitter and base contact DEKTAK pads with the DEKTAK Profilometer on several different die across the sample.
- Perform the standard solvent clean and dehydration bake on the sample.

- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.
- Use pipette to place drops of LOL 1000 coating the sample surface. Spin with standard 30 s 4000 rpm recipe (#7).
- Place on hotplate at 180 °C for 3 m.
- Remove sample and let cool for $\sim$ 1 m. Return sample to spinner chuck and verify the vacuum is holding it in place.
- Use pipette to cover sample uniformly in nLOF 5510.
- Program spinner recipe #0 to do 40 s at 1800 rpm, with an acceleration of 350 rpm/s. Spin the photoresist.
- Soft-bake on 90 °C hotplate for 60 s.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- Expose using Base Post mask in the GCA AutoStepper for 0.23 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.
- Post-bake for 60 s on 110 °C hotplate.
- Develop for 1:45 in beaker of AZ 300 MIF, with no agitation. Rinse in DI H_2O for 2 m.

- Inspect under optical microscope. Offset between base post verniers and emitter verniers should be <500 nm. Adjust focus slightly to confirm LOL has undercut underneath the opening in the nLOF, which should look like a lighter, fuzzy ring around the well defined opening in the top of the resist. If resist is unsatisfactory or misaligned by more than 100 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Base Post Liftoff

- Prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.

- Remove HCl:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O.

- *Immediately* load sample in E-Beam #4 evaporator, with long axis of emitters in the direction of rotation. Mask the edges of the sample with Al foil, taped down with Kapton tape, to facilitate the liftoff. Also load private Ti, and Au sources, and pump the system down.

- Pump until system reaches $<2 \times 10^{-6}$ T.

- After the ramp/soak cycle for each source deposition, switch to manual mode, with the shutter also manually closed, and soak for an additional 2 m at 4-5% higher power than during the deposition itself.

- Deposit 100 Å Ti at 1.0 Å/s.

- Deposit 500 Å Au at 1.0 Å/s, then ramp up to 2.0 Å/s to deposit another 500 Å (1000 Å total), then up to 4 Å/s for the remainder of the post height. The total post height should be the difference between the heights of the emitter and base contact DEKTAK measurements, typically about 4500 Å.

- At least 30 m before end of deposition, heat up beaker of 1165 in the 80 °C bath. After metal deposition, vent the chamber and transfer the sample to the 1165 beaker in the bath, using a sample holder that orients the sample facedown in the beaker.

- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 10 m. If metal has not lifted off after 30 m, leave it for an additional 30 m, continuing to agitate. Do not attempt to peel the film off with tweezers, as this may pull the base posts off as well.

- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at $<$20 psi.

- Inspect with top-down SEM to verify base post dimension and alignment, and emitter yield. Inspect with angled SEM to verify base post is appropriate height.

Base Mesa Lithography

- Perform the standard solvent clean and dehydration bake on the sample.

- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping

on the foot pedal.

- Use pipette to place drops of HMDS coating the sample surface. Let sit for 20 s, then spin with standard 30 s 4000 rpm recipe (#7). Wait 60 s before applying next layer of photoresist.
- Cut end off a clean pipette and attach it to the end of a syringe. Withdraw enough ma-N 2410 to half fill the pipette stem, and then pull the syringe back to bring all the photoresist into the syringe. Remove the pipette end from the syringe, and attach a 0.2 μm filter.
- Push the photoresist through the filter, covering the sample uniformly in droplets.
- Program spinner recipe #0 to do 60 s at 3000 rpm, with an acceleration of 450 rpm/s. Spin the photoresist. If any large spots or solid particulates in the resist appear near the center of the sample, strip the photoresist in 80 °C 1165 for 15 m. Redo the photoresist application.
- Softbake at 90 °C for 90 s.
- Return sample to spinner chuck, again verifying vacuum is solidly holding the sample in place.
- Apply aquaSAVE using pipette, taking care to make sure edges of the sample are fully covered with drops.
- Spin sample for 30s at 3000 rpm (recipe #6).
- Softbake at 90 °C for 2:30.

- Load the sample in the #2/2E cassette for the E-Beam writer as precisely in the same place as it was for the emitter write as possible. Move the cassette, still facedown, to the glass jig and perform the necessary manual rotational corrections.

- Load casette in the E-Beam writer, and perform necessary calibrations, alignments, and exposure.

- After exposure, rinse in DI H_2O for 1 m to remove aquaSAVE.

- Develop in beaker of AZ 300MIF for 2:15 with gentle agitation every 10 s, then rinse in DI H_2O for 2 m.

- Inspect sample under optical microscope for alignment, focus checkers. Check field for scum left from the UV-6 liftoff. If there is scum, descum in the "O_2 Only" PE-II asher for 30s at 300 mT and 100 W. Recheck the field for scum, and repeat for another 30 s if necessary.

Base Mesa Etch

- At the acid bench, prepare three beakers. One with 200 mL H_2O and 20 mL of NH_4OH used for surface preparation, an InGaAs etchant comprised of 250 mL H_2O and 10 mL each of H_3PO_4 and H_2O_2, and an InP etchant of 200 mL H_3PO_4 and 50 mL of HCl. Place the 1:1:25 H_3PO_4:H_2O_2:H_2O InGaAs etchant on a *room temperature* hot plate set to stir at $\sim$ 250 rpm. Prepare a beaker of 1156 and place it in the hot bath at 80 °C.

- Gently agitate the NH_4OH beaker by hand for several seconds. Place the sample in the NH_4OH:H_2O for 10 s, and immediately rinse under DI HH_2O for another 10 s. Dry with N_2 at $<$20 psi.

- Move InGaAs etchant from hot plate to bench. Etch sample in beaker for about 5 s after the color change is complete, or /*sim* 35 s for 250 Åbase + 180 Ågrade. Rinse under DI H_2O for 2 m. Dry with N_2 at <20 psi. This etch will go through the base, setback region, and base-collector grade.

- Place the InP etchant on the stir plate, and briefly inspect sample under optical microscope to verify the field looks smooth and without variation.

- Return to the acid bench, and move the InP etchant from the hotplate to the bench. Dip the sample in the beaker for 10 s after the color change is complete, and the gas byproduct bubbles begin to dissipate. This is /*sim* 35 s for 100 nm collector designs. Immediately transfer the sample to a DI H_2O rinse for 2 m, and dry with N_2 at <20 psi. This etch will go through the InP drift collector, stopping at the sub-collector surface.

- inspect sample under optical microscope to verify the field looks smooth and without variation.

- Transfer the sample to the beaker of 1165 in the hot bath for 15 m, agitating gently with a pipette every few minutes. Clean with isopropyl and DI H_2O for 3 m each, and dry with N_2 at <20 psi.

- Inspect with angled SEM to observe mesa undercut and etch completion, as well as to verify all photoresist has been removed.

Note: The process flow described here uses microstrip transmission line probes to the device, where the microstrip signal line is deposited at the end of the process, on top of BCB, and the ground plane is deposited concurrently with collector metal, in the field after isolation. For this to work, the device isolation is performed before

collector contact deposition, so one metal liftoff can define both collector contact and ground plane. For coplanar waveguide style or inverted microstrip probes, without the ground plane below the signal line, this is not necessary, and it is recommended to do the steps in the order collector contact, device isolation, collector post, to minimize any contamination that occurs at the sub-collector surface before contact deposition. Because the collector contact is so large in area, slightly higher collector ρ_c has minimal effect on device performance.

Device Isolation Lithography

- Perform the standard solvent clean and dehydration bake on the sample.
- Remove sample and let cool for ~ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.
- Use pipette to cover sample uniformly in SPR-510.
- Spin the photoresist at 4000 rpm for 30 s (recipe #7).
- Soft-bake the sample for 60 s on the 90 °C hotplate.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- Expose using Device Isolation mask in the GCA AutoStepper for 0.27 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.
- Post-bake the sample for 60 s on the 110 °C hotplate.

- Develop for 60 s in beaker of AZ 300 MIF, with no agitation. Rinse in DI H_2O for 2 m.
- Inspect under optical microscope. Offset between device isolation verniers and emitter verniers should be <150 nm. If resist is misaligned by more than 150 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Device Isolation Etch

- At the acid bench, prepare three beakers. One with 200 mL H_2O and 20 mL of NH_4OH used for surface preparation, an InGaAs etchant comprised of 250 mL H_2O and 10 mL each of H_3PO_4 and H_2O_2, and an InP etchant of 200 mL H_3PO_4 and 50 mL of HCl. Place the 1:1:25 H_3PO_4:H_2O_2:H_2O InGaAs etchant on a *room temperature* hot plate set to stir at $\sim$ 250 rpm. Prepare a beaker of 1156 and place it in the hot bath at 80 °C.
- Gently agitate the NH_4OH beaker by hand for several seconds. Place the sample in the NH_4OH:H_2O for 10 s, and immediately rinse under DI HH_2O for another 10 s. Dry with N_2 at <20 psi.
- Move InGaAs etchant from hot plate to bench. Etch sample in beaker for 15 s. The InGaAs sub-collector cap is too thin to notice a color change during etching. Rinse under DI H_2O for 2 m. Dry with N_2 at <20 psi.
- Place the InP etchant on the stir plate, and briefly inspect sample under optical microscope to verify the field looks smooth and without variation.

- Return to the acid bench, and move the InP etchant from the hotplate to the bench, and the InGaAs etchant back to the hotplate. Dip the sample in the beaker for $\sim$ 15 s after the color change is complete, and the gas byproduct bubbles begin to dissipate. This is $/sim$ 50 s for 300 nm sub-collector designs. Immediately transfer the sample to a DI H_2O rinse for 2 m, and dry with N_2 at $<$20 psi. This etch will go through the InP sub-collector, stopping at a thin InGaAs etch stop.

- inspect sample under optical microscope to verify the field looks smooth and without variation.

- Measure and record the Device Isolation DEKTAK pad heights at several points on the sample.

- Return to the acid bench and swap the InGaAs and InP etchant beakers from hotplate to benchtop. Etch the sample for 10 s in the InGaAs etchant. Again, the InGaAs etch stop layer is too thin to notice any color change. Immediately transfer the sample to a DI H_2O rinse for 2 m, and dry with N_2 at $<$20 psi.

- Move the InP etchant from the hotplate to the bench. Etch the sample for 15 s. Immediately transfer the sample to a DI H_2O rinse for 2 m, and dry with N_2 at $<$20 psi.

- Re-measure the same Device Isolation DEKTAK pads, and record the height difference before and after the second InP etch. If it is not $\sim$100 nm, repeat the InP etch in 5 s increments until a depth of 100 nm is reached.

- Transfer the sample to the beaker of 1165 in the hot bath for 15 m, agitating

gently with a pipette every few minutes. Clean with isopropyl and DI H_2O for 3 m each, and dry with N_2 at <20 psi.

- Inspect with angled SEM to observe mesa undercut and etch completion, as well as to verify all photoresist has been removed.

Collector Contact Lithography

- Perform the standard solvent clean and dehydration bake on the sample.
- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.
- Use pipette to cover sample uniformly in nLOF 2020.
- Spin the photoresist for 30 s at 3500 rpm (recipe #6).
- Soft-bake on 110 °C hotplate for 60 s.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- Expose using Collector Contact mask in the GCA AutoStepper for 0.16 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.
- Post-bake for 60 s on 115 °C hotplate.
- Develop for 120 s in beaker of AZ 300 MIF, with gentle agitation every 30 s. Rinse in DI H_2O for 2 m.

- Inspect under optical microscope. Offset between collector contact verniers and emitter verniers should be <200 nm. If resist is misaligned by more than 200 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Collector Contact Liftoff

- Prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.

- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O. Dry with N_2 at <20 psi.

- *Immediately* load sample in E-Beam #4 evaporator, with long axis of emitters in the direction of rotation. Also load private Ti, Pd, and Au sources, and pump the system down.

- Pump until system reaches $<2 \times 10^{-6}$ T.

- After the ramp/soak cycle for each source deposition, switch to manual mode, with the shutter also manually closed, and soak for an additional 2 m at 4-5% higher power than during the deposition itself.

- Deposit 200 Å Ti at 1.0 Å/s.

- Deposit 200 Å Pd at 1.0 Å/s.

- Deposit 300 Å Au at 1.0 Å/s, then ramp up to 2.0 Å/s to deposit another 200 Å (500 Å total), then up to 3 Å/s to deposit another 500 Å (1000 Å total), then 4-5 Å/s to deposit another 1500 Å (2500 Å total).

- At least 30 m before end of deposition, heat up beaker of 1165 in the 80 °C bath. After metal deposition, vent the chamber and transfer the sample to the 1165 beaker in the bath, using a sample holder that orients the sample facedown in the beaker.

- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 10 m. If metal has not lifted off after 30 m, leave it for an additional 30 m, continuing to agitate. Try to gently peel metal film back with Carbon tipped tweezers.

- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at <20 psi.

- Inspect with top-down SEM to verify collector contact dimension and alignment, and emitter yield. Inspect with angled SEM to verify collector contact is appropriate height.

Ground Post Lithography

- Perform the standard solvent clean and dehydration bake on the sample.

- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.

- Use pipette to cover sample uniformly in nLOF 2020.

- Spin the photoresist for 30 s at 3500 rpm (recipe #6).
- Soft-bake on 110 °C hotplate for 60 s.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- If any pass shift was needed in the collector contact layer, incorporate it into this layer as well.
- Expose using Ground Post mask in the GCA AutoStepper for 0.16 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.
- Post-bake for 60 s on 115 °C hotplate.
- Develop for 120 s in beaker of AZ 300 MIF, with gentle agitation every 30 s. Rinse in DI H_2O for 2 m.
- Inspect under optical microscope. Offset between ground post verniers and emitter verniers should be $<$200 nm. If resist is misaligned by more than 200 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Ground Post Liftoff

- Use the DEKTAK Profilometer to measure and record the heights of several Device Isolation DEKTAK pads across the sample.
- Prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.

- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O. Dry with N_2 at <20 psi.
- *Immediately* load sample in E-Beam #4 evaporator, with long axis of emitters in the direction of rotation. Also load private Ti, Pd, and Au sources, and pump the system down.
- Pump until system reaches $<2 \times 10^{-6}$ T.
- After the ramp/soak cycle for each source deposition, switch to manual mode, with the shutter also manually closed, and soak for an additional 2 m at 4-5% higher power than during the deposition itself.
- Deposit 200 Å Ti at 1.0 Å/s.
- Deposit 200 Å Pd at 1.0 Å/s.
- Deposit 300 Å Au at 1.0 Å/s, then ramp up to 2.0 Å/s to deposit another 200 Å (500 Å total), then up to 3 Å/s to deposit another 500 Å (1000 Å total), then 4-5 Å/s to deposit the remainder of the post height. The post should be the same height as the Device Isolation mesa, typically about 4000 Å.
- At least 30 m before end of deposition, heat up beaker of 1165 in the 80 °C bath. After metal deposition, vent the chamber and transfer the sample to the 1165 beaker in the bath, using a sample holder that orients the sample facedown in the beaker.
- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 10 m. If metal has not lifted off after 30 m, leave it for an additional

30 m, continuing to agitate. Try to gently peel metal film back with Carbon tipped tweezers.

- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at $<$20 psi.
- Inspect with top-down SEM to verify ground post dimension and alignment, and emitter yield. Inspect with angled SEM to verify ground post are appropriate height.

Collector Post Lithography

- Perform the standard solvent clean and dehydration bake on the sample.
- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.
- Use pipette to cover sample uniformly in nLOF 2020.
- Spin the photoresist for 30 s at 3500 rpm (recipe #6).
- Soft-bake on 110 °C hotplate for 60 s.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- If any pass shift was needed in the collector contact layer, incorporate it into this layer as well.
- Expose using Collector Post mask in the GCA AutoStepper for 0.16 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.

- Post-bake for 60 s on 115 °C hotplate.
- Develop for 120 s in beaker of AZ 300 MIF, with gentle agitation every 30 s. Rinse in DI H_2O for 2 m.
- Inspect under optical microscope. Offset between collector post verniers and emitter verniers should be $<$200 nm. If resist is misaligned by more than 200 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Collector Post Liftoff

- Use the DEKTAK Profilometer to measure and record the heights of several Emitter, Collector Contact, and Device Isolation DEKTAK pads across the sample.
- Prepare a beaker with 200 mL DI H_2O, and add 20 mL of HCl. Place on *room temperature* stirrer plate at 250 rpm.
- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Immediately rinse for 10 s under DI H_2O. Dry with N_2 at $<$20 psi.
- *Immediately* load sample in E-Beam #4 evaporator, with long axis of emitters in the direction of rotation. Also load private Ti and Au sources, and pump the system down.
- Pump until system reaches $<2 \times 10^{-6}$ T.

- After the ramp/soak cycle for each source deposition, switch to manual mode, with the shutter also manually closed, and soak for an additional 2 m at 4-5% higher power than during the deposition itself.

- Deposit 200 Å Ti at 1.0 Å/s.

- Deposit 300 Å Au at 1.0 Å/s, then ramp up to 2.0 Å/s to deposit another 200 Å (500 Å total), then up to 3 Å/s to deposit another 500 Å (1000 Å total), then 4-5 Å/s to deposit the remainder of the post height. The post should rise 50 nm above the emitter and base post, to facilitate planarization since their large size will create a slight wave in the BCB. The total post height can be calculated the heights of the DEKTAK pads measured prior to deposition: Emitter – 1400 Å – Device Isolation – Collector Contact + 500 Å.

- At least 30 m before end of deposition, heat up beaker of 1165 in the 80 °C bath. After metal deposition, vent the chamber and transfer the sample to the 1165 beaker in the bath, using a sample holder that orients the sample facedown in the beaker.

- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 10 m. If metal has not lifted off after 30 m, leave it for an additional 30 m, continuing to agitate. Try to gently peel metal film back with Carbon tipped tweezers.

- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at <20 psi.

- Inspect with top-down SEM to verify collector post dimension and alignment,

and emitter yield. Inspect with angled SEM to verify collector posts are appropriate height.

BCB Passivation

- Perform standard solvent clean and dehydration bake on the sample.
- Run the UV-O_3 reactor empty for 20 m. Load sample, and run for 10 m.
- Load the BCB sample mount in the Blue Oven, and turn on 100 % N_2flow. The Blue Oven must be at 25 °C and the N_2 must flow for 20 m before loading the sample.
- At the acid bench, pour 250 mL of NH_4OH into a beaker. Dip the sample for 10 s, and dry with N_2 at <20 psi, no DI H_2O rinse.
- *Immediately* move to the photoresist bench. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal. Use pipette to coat sample surface with Benzocyclobutene 3022-35. Let BCB sit on sample surface for 30 s.
- Program spinner recipe #0 to do 30 s at 1500 rpm, with an acceleration of 150 rpm/s. Spin the BCB.
- Place the sample on the center of the BCB sample mount, and close the Blue Oven door.
- Program recipe #5 to do the following four-step recipe: 5 m ramp to 50 °C, 5 m soak. 15 m ramp to 100 °C, 15 m soak. 15 m ramp to 150 °C, 15 m soak. 60 m rise to 250 °C, 60 m soak. Natural cooldown. Run recipe, allow 6-8 hrs

for cycle to complete and return to room temperature. *Do not* remove sample until oven temperature is at 25 °Cor lower.

- Use Nanometrics Reflectometer with recipe #10 and a dielectric constant of 1.6 to veriy the BCB thickness. It should be $\sim 4\ \mu$m.
- Verify the temperature of the Panasonic ICP ashing chamber is 50 °C.
- Take a reasonably shiny looking 6 in Si carrier wafer from the "CF_4/O_2" section of the Rodwell ICP carrier wafer box. Clean it with acetone from a spray bottle, then wipe dry with a non-shedding wipe. Repeat with isopropyl alcohol from a spray bottle, and dry the wafer with the N_2 gun.
- Load the wafer in one of the ICP's cassettes, and run a 10 m CF_4/O_2 ash with 50/200 sccm, 40 Pa, and 1000 W (recipe #308).
- Clean a second wafer from the "CF_4/O_2" portion of the box identically to the first. Place a dewdrop sized droplet of Santovac oil in the center of the wafer. Place the sample on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.
- Load the wafer in an ICP cassette and run a 4 m CF_4/O_2 ash with the same parameter as the chamber condition.
- When the wafer is returned, immediately rinse the sample, while still attached to the carrier wafer, with H_2O from a spray bottle. Gently remove the sample from the wafer with a wooden swab, and transfer the sample to a beaker of DI H_2O, and rinse for 2 m at the developer bench. Follow with a standard solvent clean, and dry with N_2 at $<$20 psi.

- Measure the thickness of the BCB using the Nanometrics. Calculate an etch rate from the measurement before etching, although this should only be used as a rough estimate. Total BCB height will be $\sim 1\ \mu$m when posts begin to poke through.

- Inspect the device in the SEM using the 20 deg holder, at 2 kV accelerating voltage to minimize charging. Check if emitters and posts are through the BCB — they will appear bright and come sharply into focus, while the field is darker and blurry. Check both edge and center die, as well as transistors in both CPW and microstrip style pads, as significant variation can occur.

- If posts are not yet exposed, repeat ashing in 1-2 m increments, based on the thickness and etch rate calculated from the Nanometrics measurement. After each etch, repeat the cleaning, reflectometery measurement, and SEM inspection.

Contact Via Deposition

- Vent PlasmaTherm PECVD chamber. Wipe inside walls with Iso-soaked paper wipe. Pump chamber and run standard 30 m Si_xN_y clean.

- Vent chamber and load 2 in Si wafer in center of chamber. Place glass slides above and to the left of the wafer to hold it in place. Pump down.

- Run standard 1500 Å Si_xN_y deposition. Even if other dummy samples with Si_xN_y are available for calibration, this step *must* be done to properly condition the chamber for the real deposition.

- At the acid bench, prepare a beaker with 200 mL DI H_2O, and add 20 mL of NH_4OH. Place on *room temperature* stirrer plate at 250 rpm.

- Remove $NH_4OH:H_2O$ solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating.
- Dry sample with N_2 gun at >20 psi, immediately transfer to open PECVD chamber, remove dummy wafer, and pump down.
- Run standard 1000 Å Si_xN_y deposition.

Contact Via Lithography

- Perform the standard solvent clean and dehydration bake on the sample.
- Remove sample and let cool for ∼ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.
- Use pipette to cover sample uniformly in SPR-510.
- Spin the photoresist at 4000 rpm for 30 s (recipe #7).
- Soft-bake the sample for 60 s on the 90 °C hotplate.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- If a pass shift was necessary for the Device Isolation layer, incorporate the same pass shift into this exposure.
- Expose using Contact Via mask in the GCA AutoStepper for 0.27 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.
- Post-bake the sample for 60 s on the 110 °C hotplate.

- Develop for 60 s in beaker of AZ 300 MIF, with no agitation. Rinse in DI H_2O for 2 m.
- Inspect under optical microscope. Offset between Contact Via verniers and emitter verniers should be <100 nm. If resist is misaligned by more than 150 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Contact Via Etch

- At least 30 m before end of etch, heat up beaker of 1165 in the 80 °C bath.
- Cleave the dummy Si wafer in half. Measure the film thickness at 3 points across one of the half wafers using Brian Thibeault's standard Si_xN_y-on-Si recipes for the Woolam Spectroscopic Ellipsometer.
- Put the Panasonic ICP #1 into 'CONT' mode.
- Take a reasonably shiny looking 6 in Si carrier wafer from the "CF_4/O_2" section of the Rodwell ICP carrier wafer box. Clean it with acetone from a spray bottle, then wipe dry with a non-shedding wipe. Repeat with isopropyl alcohol from a spray bottle, and dry the wafer with the N_2 gun.
- Load the wafer in one of the ICP's cassettes, and run the standard O_2 clean (recipe # 121) for 10 m.
- Clean a second wafer from the "CF_4/O_2" portion of the box identically to the first.

- Load the wafer in the other cassette, and run a 5m CF_4/O_2 ICP etch with 20/5 sccm gas flow, 1 Pa pressure, and 500/100 W powers to condition the chamber (recipe #138).

- When the first wafer is returned from the system, place a dewdrop sized droplet of Santovac oil in the center of the wafer. Place the dummy Si sample on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Run a 12 m CF_4/O_2 etch with 20/2 sccm, 0.3 Pa, and 25/15 W powers on the wafer with the Si dummy (recipe #134). No plasma will be visible in the chamber during this etch.

- When the dummy sample is returned, rinse with DI H_2O and remove from the carrier wafer with wooden swabs. Return to the Ellipsometer and re-measure the film thickness at the same three points. Calculate an average etch rate based on the before- and after-etch thicknesses.

- Place a dewdrop sized droplet of Santovac oil in the center of the clean carrier wafer. Place the HBT on top of this, and use two wooden swabs to press on opposite corners of the sample to bring it flush with the sample surface.

- Based on the calculated etch rate, run the low-powered CF_4/O_2 etch for long enough to etch 1200 nm of Si_xN_y (20% overetch) on the carrier wafer with the HBT sample. The low-power Si_xN_yetch is very selective to BCB.

- Immediately rinse the sample, while still attached to the carrier wafer, with H_2O from a spray bottle. Gently remove the sample from the wafer with a

wooden swab, and transfer the sample to a beaker of DI H_2O, and rinse for 2 m at the developer bench. Follow with a standard solvent clean, and dry with N_2 at $<$20 psi.

- Inspect the device in the SEM with the 20 or 45 deg mount, at 2 kV. Make sure all posts and emitters across wafer are exposed, and appear clear and bright. If not, repeat CF_4/O_2 etching in 1 m increments.
- Flood expose for $\sim$ 30 s in the UV Flood Exposure.
- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 15 m.
- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at $<$20 psi.
- Inspect under optical microscope. If photoresist scum remains on the sample, perform O_2 descum in the "O_2 Only" PE-II in increments of 1 m.

Note: Double check *all* ICP etch recipe parameters before running them, as other users frequently change them.

Metal 1 Lithography

- Perform the standard solvent clean and dehydration bake on the sample.
- Remove sample and let cool for $\sim$ 1 m. Place sample on spinner chuck and turn vacuum on. Test sample vacuum integrity with tweezers and by stepping on the foot pedal.
- Use pipette to cover sample uniformly in nLOF 2020.

- Spin the photoresist for 30 s at 3500 rpm (recipe #6).
- Soft-bake on 110 °C hotplate for 60 s.
- Load sample in stepper using 76.2 mm, 635 μm chuck.
- If any pass shift was needed in the collector contact or post layer, incorporate it into this layer as well.
- Expose using Metal 1 mask in the GCA AutoStepper for 0.16 s. Expose all die with die-by-die local alignment. Do another mapping pass based off the internal die and expose an outer ring of die to enable liftoff to occur there.
- Post-bake for 60 s on 115 °C hotplate.
- Develop for 120 s in beaker of AZ 300 MIF, with gentle agitation every 30 s. Rinse in DI H_2O for 2 m.
- Inspect under optical microscope. Offset between Metal 1 verniers and emitter verniers should be <100 nm. If resist is misaligned by more than 100 nm, write down the offset, and strip the photoresist for 30 m in 1165, followed by 3 m in isopropyl and a 3 m DI H_2O rinse. Then redo lithography after incorporating a pass shift into the file for the exposure.

Metal 1 Liftoff

- Turn on UV-O_3 oven and let it run empty for 15 m. Load sample and run in UV-O_3 for 10 m.
- Prepare a beaker with 200 mL DI H_2O, and add 20 mL of NH_4OH. Place on *room temperature* stirrer plate at 250 rpm.

- Remove HCL:H_2O solution from the hot plate, and place on acid bench. Dip sample in solution for 10 s, gently agitating. Dry with N_2 at <20 psi.
- *Immediately* load sample in E-Beam #4 evaporator, with long axis of emitters in the direction of rotation. Also load private Ti, and Au sources, and pump the system down.
- Pump until system reaches $<2 \times 10^{-6}$ T.
- After the ramp/soak cycle for each source deposition, switch to manual mode, with the shutter also manually closed, and soak for an additional 2 m at 4-5% higher power than during the deposition itself.
- Deposit 100 Å Ti at 1.0 Å/s.
- Deposit 100 Å Au at 1.0 Å/s, then ramp up to 2.0 Å/s to deposit another 200 Å (300 Å total), then up to 3 Å/s to deposit another 200 Å (500 Å total), then 4 Å/s to deposit another 500 Å(1000 Åtotal), and finally to 5 Å/s to deposit another 9000 Å(10,000 Åtotal).
- Deposit 100 Å Ti at 1.0 Å/s.
- At least 30 m before end of deposition, heat up beaker of 1165 in the 80 °C bath. After metal deposition, vent the chamber and transfer the sample to the 1165 beaker in the bath, using a sample holder that orients the sample facedown in the beaker.
- Leave sample in 1165, in the heated bath, for 30 m. Agitate with pipette every 10 m. If metal has not lifted off after 30 m, leave it for an additional

30 m, continuing to agitate. Try to gently peel metal film back with Carbon tipped tweezers.

- Transfer sample to beaker of isopropyl for 3 m, then 3 m of running DI H_2O. Dry with N_2 at $<$20 psi.
- Inspect with top-down SEM to verify metal dimension and alignment, and emitter yield. Inspect with angled SEM to verify collector posts are appropriate height.