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High-Speed Digital ICs in Transferred-Substrate HBT Technology

A Dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

Thomas Mathew

Committee in charge:

Professor Stephen I. Long, Chair

Professor Mark J. W. Rodwell

Professor Umesh K. Mishra

Professor Steve E. Butner

August 2001

The dissertation of Thomas Mathew is approved.

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Mark J. W. Rodwell

_____

Umesh K. Mishra

_____

Steve E. Butner

_____

Stephen I. Long, Committee Chair

August 2001

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VITA OF Thomas Mathew
August 2001

EDUCATION

Doctor of Philosophy (Ph.D) in Electrical and Computer Engineering, University of California, Santa Barbara, 2001 (Expected).

Master of Technology (M.Tech), Electrical and Electronics Engineering, Indian Institute of Technology, Mumbai (Bombay), India, 1996.

Bachelor of Technology (B.Tech), Electronics Engineering, Regional Engineering College, Calicut, Kerala, India, 1992.

PROFESSIONAL EMPLOYMENT

1998-2001: Graduate researcher, Department of Electrical and Computer Engineering, University of California, Santa Barbara.

Fall 1997: Teaching Assistant, Department of Electrical and Computer Engineering, University of California, Santa Barbara.

1996-1997: Research Assistant, Department of Electrical and Electronics Engineering, Indian Institute of Technology, Mumbai (Bombay), India

PUBLICATIONS

1) T. Mathew, S. Jagannathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M. Rodwell and S. Long, "2-Bit Adder Carry and Sum Logic Circuits Clocking at 19 GHz Clock frequency in Transferred Substrate HBT Technology" *IEEE Conference on Indium Phosphide and Related Materials*, May 2001.

2) T. Mathew, H-J. Kim, D. Scott, S. Jagannathan, S. Krishnan, Y.Wei, M. Urteaga, S. Long and M. J. W. Rodwell, "75 GHz static frequency divider using InAlAs/InGaAs HBTs", *IEE Electronics Letters*, Vol. 37, No. 11, May 2001

3) T. Mathew, S. Jagannathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M. Rodwell and S. Long, "2 bit adder: Carry and sum logic circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT technology", Accepted by *IEE Electronics Letters*, August, 2001.

4) T. Mathew, H-J. Kim, D. Scott, S. Jagannathan, S. Krishnan, Y.Wei, M. Urteaga, S. Long and M. J. W. Rodwell, "75 GHz static frequency divider in InAlAs/InGaAs transferred-substrate HBT technology", post deadline submission, *IEEE Conference on Indium Phosphide and Related Materials*, May 2001.

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6) M. Urteaga, D.Scott, T. Mathew, S. Krishnan, Y. Wei, and M. J. W. Rodwell, "185 GHz Monolithic Amplifier in InGaAs/InAlAs Transferred-Substrate HBT Technology", *IEEE MTT-S International Microwave Symposium*, May, 2001

7) S. Jagannathan, D. Mensa, T. Mathew, Y. Betser, S. Krishnan, Y.Wei, D. Scott, M. Urteaga, M.Rodwell, "An 18GHz continuous time $\Sigma-\Delta$ modulator implemented in InP transferred-substrate HBT Technology", *IEEE GaAs IC Symposium*, Nov. 2000.

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ABSTRACT

High-Speed Digital ICs in Transferred-Substrate HBT technology

by

Thomas Mathew

One of the key electronic component needed for next generation naval radars is the direct digital frequency synthesis (DDFS) block, that is used for signal generation. A key building block in a DDFS system is the phase accumulator (adder-accumulator). The maximum clock rate (f_{ck}) of the various building blocks in a DDFS system determines its frequency resolution and tuning range. The frequency tuning range of the DDFS system is from DC to ~ ($f_{ck}/3$) and the frequency resolution is given by $\Delta f = f_{ck}/2^N$, where N is the bit length of the phase-accumulator word.

This work presents the design techniques used to improve the clock rate of a 2-bit adder-accumulator circuit, which is used as the building block in an 8-bit pipelined adder accumulator. The first generation design used a wired OR/AND approach in the carry logic (AND-OR) circuit to increase the clock rate. The carry and sum logic circuit of the 2-bit adder was fabricated and tested. Measurements indicated a maximum clock rate of 8 GHz for the carry logic circuit and 14 GHz for the sum logic circuit. The second generation design used a new single 3-level series-gated logic gate that performed the AND-OR operation needed to realize the carry

logic of a full adder. This carry logic circuit was then merged with the latches to realize a merged AND-OR-Latch circuit. Simulations indicated that this 4-level series-gated structure was 1.8:1 faster when compared to the wired-OR/AND approach. The carry and sum logic of the second-generation 2-bit adder designs were fabricated and tested. Measurements indicated a maximum clock rate of 19 GHz for the carry logic circuit and 24 GHz for the sum logic circuit. A 75 GHz ECL static frequency divider was also fabricated as part of this work.

Attempts to extend a technology, which demonstrated circuits having tens of transistors, to realize circuits having hundreds of transistors, brings forth a new set of failure mechanisms. This work also presents the test structures designed to identify the various failure mechanisms and the statistical data collected from these structures.

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Chapter 1

Introduction

Heterojunction bipolar transistor (HBT) based integrated circuits (ICs) are finding applications in commercial, military, and satellite communication systems. The commercial applications are mainly driven by CATV, wireless and fiber-optic communication systems while the military applications include electronics for naval radars and military communication systems. The demands placed by these applications have led to the development and commercial production of a number of HBT technologies. Current HBT technologies in commercial production include GaAs and InP based HBTs. Also significant progress has been made in Silicon-Germanium (SiGe) HBT technology, enhancing the frequency range of operation of Si bipolar transistor technology. The potential uses of these technologies in high-speed applications depend on their microwave (RF) as well as logic speed performance. Current gain cut-off frequency (f_t) and power gain cut-off frequency (f_{max}) are the two common figures of merit used to evaluate the analog/RF performance of an HBT technology.

Shown in Fig. 1.1 are the f_t, f_{max} of different HBT technologies. AlGaAs/GaAs HBTs have lower cut-off frequencies [1] compared to InP or SiGe

HBTs and find applications in ICs operating around 10 - 20 GHz. Advances in SiGe technology over the last few years have resulted in commercial production of SiGe transistors with f_t and f_{max} over 100 GHz [2]. InGaP/GaAs HBTs have demonstrated peak f_t and f_{max} of 150 GHz and 260 GHz respectively [3]. Commercial InP HBTs have reported f_t and f_{max} close to 200 GHz [4] and the transferred substrate HBT technology has demonstrated simultaneous f_t and f_{max} close to 300 GHz [5].

The Master-slave latch (Flip-flop) is a key building block used in digital circuits. The maximum clocking rate of the Master-slave flip-flop is most easily evaluated by configuring it as a static frequency divider. This is achieved by feeding the inverted output back as the input. The maximum clock rate of static frequency divider (SFD) operation is used to compare the logic speed of different semiconductor technologies. The best reported SFD clock rates are in HBT technologies and are shown in Table 1.1.

Static frequency divider operation has been measured up to 30 GHz [8] in Si Bipolar transistor technology and up to 34.8 GHz [9] in AlGaAs/GaAs HBT technology. Hitachi has reported a 67 GHz frequency divider in SiGe technology [10]. In InP based HBTs, Hughes research labs (HRL) has reported a 72.8 GHz divider [11]. The highest reported clock rate to date for SFD is 75 GHz, realized in InAlAs/InGaAs transferred-substrate HBT (TSHBT) technology [12]. The power dissipation of the dividers is shown in Table 1.1.

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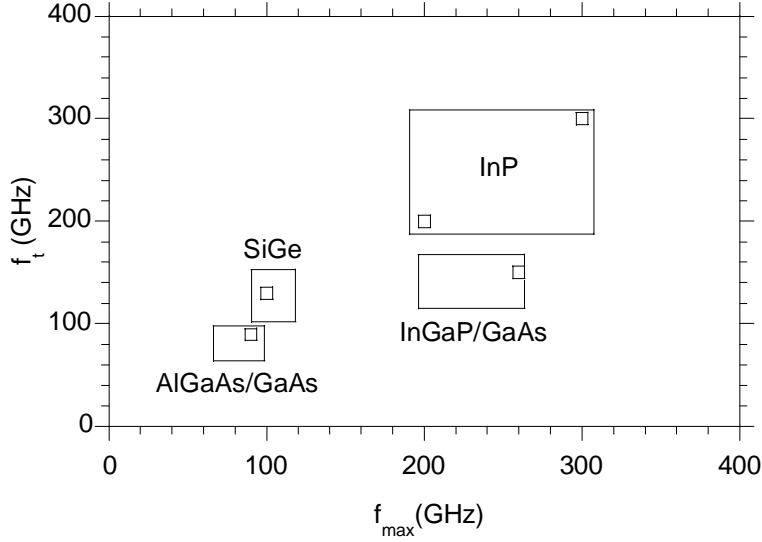
Fig. 1.1: *Shown above is the f_t and f_{max} regime of different HBT technologies reported in literature [1,2,3,4,5].*

Table 1.1: *Static frequency divider performance in different technologies.*

Ref.	Technology	Maximum	Power
[6]	Si MOSFET	16.8 GHz	3 mW
[7]	HEMTs	49.2 GHz	290 mW
[8]	Si BJT	30 GHz	630 mW
[9]	AlGaAs/ GaAs HBT	34.8 GHz	495 mW
[10]	SiGe HBT	67 GHz	175 mW
[11]	InAlAs/InGaAs	72.8 GHz	55 mW
[12]	InAlAs/InGaAs	75 GHz	800 mW

InP and SiGe HBT technology offer excellent RF as well as logic speed performance making them a good technology choice for building amplifiers as well as digital and mixed signal ICs for high-speed applications. InP HBTs offer superior RF performance when compared to SiGe HBTs, but in digital applications SiGe circuits have done nearly as well as InP circuits. This has been attributed to the advanced and mature silicon processing capabilities which enables increased current density (J_e) of operation, highly scaled device geometry (0.18 μm emitter width) and interconnect density, higher transistor count and reduced device as well as interconnect parasitics [2]. These technologies have been used to demonstrate transimpedance and power amplifiers [13,14], as well as flip-flops operating over 66 GHz.

The office of naval research (ONR) is currently engaged in the process of designing the next generation of electronic systems for naval radars. The enabling technology needs to provide logic-speeds up to 100 GHz and RF performance in the 300 - 400 GHz range. Such high frequency performance requires major advances in both InP and SiGe HBT technologies. The next section examines the approaches used to extend the frequency range of InP HBTs. The transferred-substrate approach is presented as a potential technology to realize logic-speeds above 100 GHz.

1.1   Motivation

One of the key electronic components needed for the next generation of naval radars is the direct digital frequency synthesis (DDFS) block that is used for signal

generation. This work was part of a bigger project aimed at demonstrating the basic building blocks of a DDFS system operating at high frequencies. The block diagram of a DDFS system is shown in Fig. 1.2. The digital signal processor outputs a digital word corresponding to the phase increment ($\Delta\phi$). This phase increment is added to the digital word corresponding to the stored value of the phase (ϕ) in the phase-accumulator. The output digital word ($\phi + \Delta\phi$) of the phase-accumulator (adder-accumulator) serves as the address of a Sine ROM. The Sine ROM is a look-up table and outputs the digital word corresponding to sin ($\phi + \Delta\phi$). This digital word is converted by the digital to analog converter (DAC) to analog sine wave.

The frequency tuning range of the DDFS system is from DC to ~ ($f_{ck}/3$) and the frequency resolution is given by $\Delta f = f_{ck}/2^N$, where N is the bit length of the phase-accumulator word [15]. The design of phase-accumulator, Sine ROM, and DAC clocking above 40 GHz are all significant design challenges. This work focuses on the design challenges in building high-speed adder-accumulators.
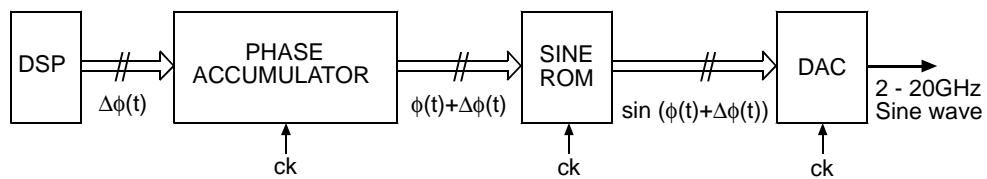
Fig. 1.2: *Block diagram showing the direct digital frequency synthesis approach.*

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1.2   HBT Technology to realize 100 GHz logic: the challenges

A typical HBT structure is shown in Fig. 1.3. W_e is the width of the emitter and is normally determined by the minimum definable feature size. High frequency HBT technologies use a self-aligned base to reduce extrinsic base resistance (r_{be}). The base mesa width (W_b) is determined by the transfer length (L_b) of the base contacts. The base width also determines the area of the base-collector junction, which contributes to the base-collector capacitance (C_{cb}). The base-collector capacitance C_{cb} has 2 components, the intrinsic component C_{cbi}, and the extrinsic component C_{cbx} as shown in Fig. 1.3. The transfer length of the collector contacts (L_c) and any alignment tolerance (L_{tol}) determine the collector mesa width (W_c). This HBT structure is referred to as the triple-mesa HBT structure. The emitter mesa isolates the emitter-base junction and the base mesa isolates the base-collector junction. The collector mesa provides device to device isolation.

The logic-speed of an HBT technology depends on a number of device parameter [16]. The most significant parameters include forward transit time τ_f, base-collector capacitance C_{cb}, base resistance r_{bb}, maximum current density of operation J_e, base-emitter capacitance (C_{be}) and extrinsic emitter resistance (r_{ex}) [16]. The extent to which the logic-speed depends on the device parameters is specific to the technology under consideration. In triple mesa HBT structures the base-collector capacitance has significant effect on the logic speed [17]. Scaling of the emitter finger width (W_e) has been used to reduce the intrinsic base-collector capacitance C_{cbi}. But, the reduction in the total base-collector capacitance ($C_{cb} = C_{cbi}$

+ C_{cbx}) with the scaling of emitter width W_e becomes negligible when the emitter width becomes smaller than the base contact width $\{W_e < (L_b + L_{tol})\}$. Thus, in sub-micron HBTs the extrinsic base-collector capacitance C_{cbx} is higher than the intrinsic base-collector capacitance C_{cbi} [17].
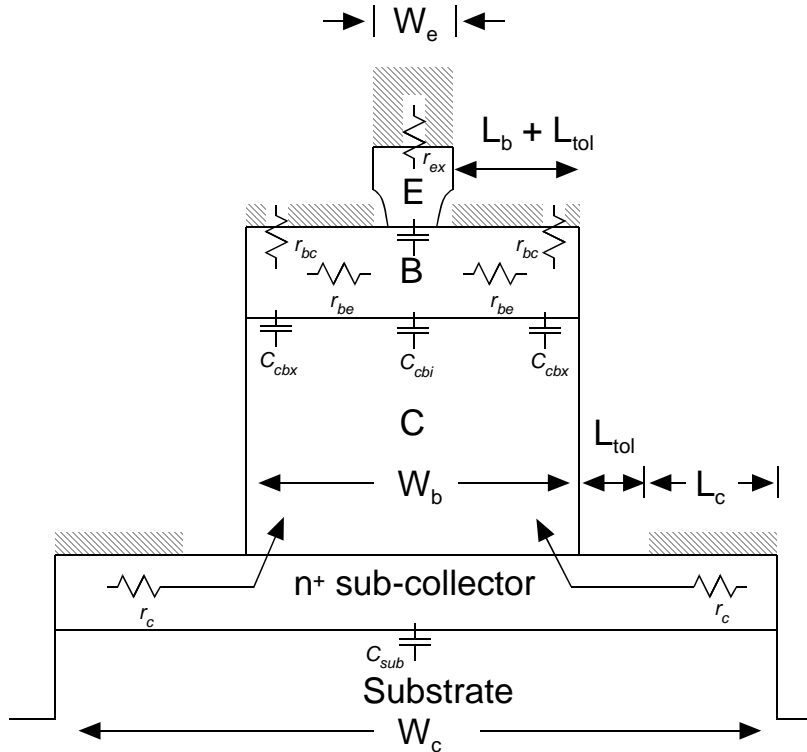
Fig. 1.3: *The structure of a triple-mesa HBT indicating the relevant intrinsic and extrinsic device parameters that contribute to device performance.*

A number of approaches have been put forward to reduce the extrinsic base-collector capacitance. These include the selective wet etch based under-cut of the base mesa [18] and the transferred-substrate HBT approach [19]. The basic

approach employed to reduce C_{cb} in both the transferred-substrate approach and selective wet etch undercut approach are shown in Fig. 1.4. Though excellent RF results [18] have been obtained by undercutting the base mesa, the issue of passivation of the base mesa under-cut remains to be addressed. The transferred-substrate HBT (TSHBT) approach involves flipping and bonding the processed InP wafer onto a GaAs wafer and etching away the InP substrate to expose the collector epitaxial layer. The collectors are then defined directly opposite to the emitter. Significant reduction in C_{cbx} is achieved by the use of Schottky collector contacts. The extrinsic collector region is partly removed by a collector recess etch [19]. Transferred-substrate HBTs have demonstrated excellent RF performances with f_t of 300 GHz [20] and extrapolated f_{max} of over 1 THz [21]. To date, a number of circuits have been fabricated in TSHBT process which include small signal amplifiers [22], static frequency dividers [12], analog to digital converters [23] and the carry and sum logic circuit for a 2-bit adder-accumulator [24].

There are also a number of other process and technological challenges that need to be addressed to realize 100 GHz logic technology. Increased base doping levels would lead to lower base contact resistance (r_{bc}) and base contact transfer length (L_b). Attempts to achieve base doping levels in excess of 10^{20} cm^{-3} using carbon dopants are already underway. Current transferred-substrate HBT digital circuits are fabricated in InAlAs/InGaAs single heterojunction bipolar transistors (SHBT). These transistors have low breakdown voltage (V_{br} <1.2V at J_e = 1 mA/μm^2) and poor thermal conductivity due to the use of InGaAs collectors and

InAlAs emitters. Improved heat sinking techniques are required to increase the current density (J_e) of operation. The emitter extrinsic resistance (r_{ex}) and forward transit time (τ_f) also need to be reduced. These requirements translate to careful design of epitaxial layer structure, the choice of doping levels, as well as appropriate ohmic contact metallurgy [16]. The effect of the various device parameters on circuit performance depends on the circuit under consideration. In most cases a trade-off among the various device parameters need to be made in the device design to obtain optimum circuit speed.

1.3   Nature and scope of this work

This work presents the design techniques used to improve the clock rate of a 2-bit adder-accumulator circuit. The 2-bit adder-accumulator circuit is to be used as the building block in an 8-bit pipelined adder-accumulator scheme. The first generation design used a wired-OR/AND approach in the carry logic (AND-OR) circuit to increase the clock rate. The second generation design used a new single 3-level series-gated logic gate that perform AND-OR operation needed to realize the carry logic of a full adder. This carry logic circuit is then merged with the latches to realize a merged AND-OR-Latch circuit. Simulations indicate that this 4-level series-gated structure is 1.8:1 faster compared to the wired-OR/AND implementation. A 75 GHz ECL static frequency divider was also fabricated as part of this work. This is the highest reported clock rate for divider operation.
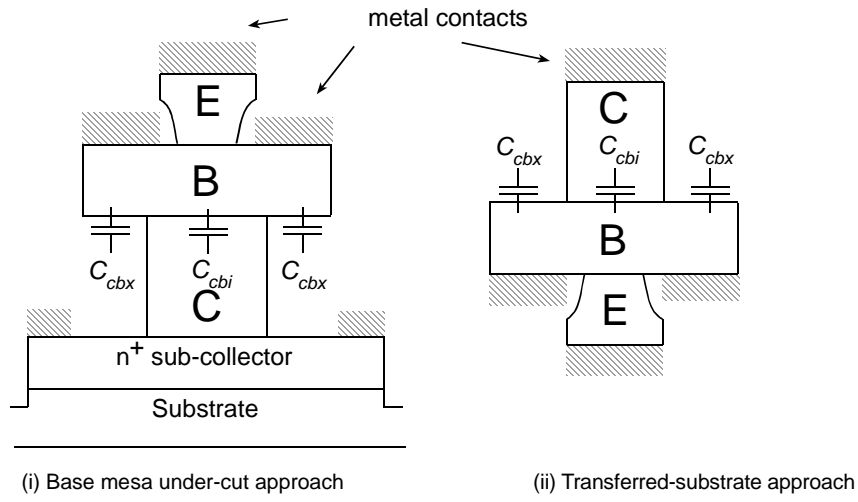
Fig. 1.4: *Approaches used to reduce the extrinsic base-collector capacitance (C_{cbx}) are shown above. Shown on the left is the selective removal of collector region by wet etching. On the right is the transferred-substrate approach.*

At the start of this work in fall 1997, transferred-substrate HBT technology had demonstrated small signal amplifiers as well as static frequency dividers. The static frequency divider was the largest digital circuit that was fabricated and had about 50 HBTs and operated up to 48 GHz [25]. Subsequent work by Q. Lee led to static frequency dividers clocking at 66 GHz in 1999 [26]. This circuit had about 76 transistors. S. Jagannathan realized a first order $\Sigma-\Delta$ analog to digital converter [23] clocking at 18 GHz with 150 HBT complexity in 2000. In this work we have demonstrated working circuits up to 250 HBT complexity.

Attempts to extend a technology, which demonstrated circuits having tens of transistors, to realize circuits having hundreds of transistors, brings forth a new set of failure mechanisms. To address these, one needs to define a set of test structures to identify and isolate the failure mechanisms. In addition to this, we also need to gather statistical information about these failure mechanisms which tells us the extent of integration that is possible. This work also presents the test structures designed to identify the various failure mechanisms and the statistical data collected from these structures.

1.4 Thesis organization

A number of adder-accumulator architectures have been reported in the literature. A brief review of the different adder-accumulators is undertaken in chapter 2. These include ripple carry adders (RCA), carry lookahead adders (CLA) and pipelined adders. This chapter also explains the choice of pipelined adder-accumulators for high clock rate applications.

The various approaches for increasing the clock rate of 2-bit adders is then discussed. Two generations of adder designs were carried out. These are described in chapter 3. The measurement results of the fabricated adder circuits are also presented in this chapter. The design and results of a 75 GHz static frequency divider circuit is presented in chapter 4.

Chapter 5 describes the various processing issues in the transferred-substrate HBT process (TSHBT). The TSHBT process is presented in a step-by-step manner.

The relevant processing issues at each step are presented with the help of wafer cross section figures and SEM pictures. The possible failure mechanisms are highlighted and test structures that identify these failure mechanisms are presented. The results of the various process and yield characterization test structures are also presented in chapter 5. The conclusions are presented in chapter 6.

Chapter 2

Synchronous adder architectures

Adders are key building blocks in a number of applications including Direct digital frequency synthesis (DDFS) and Arithmetic and logic unit (ALU) of a computer. There exist two classes of adders, namely the asynchronous adders and the synchronous adders. In general, asynchronous adders [27] perform the addition and then generate a control signal indicating the completion of an add operation. In such adders, the time to complete the addition depends on the input bits and the addition algorithm used. In synchronous adders, the input bits are available at the start of each clock cycle, and the sum output bits are generated at the end of each clock period. As the adder-accumulators used in DDFS systems are synchronous adders, a review of the different synchronous adder-architectures is presented in the following section.

Binary adders perform the function of adding two numbers, where each number is represented as a binary word. The addition operation in digital domain is represented by a set of logic operations that generate the output sum word. The next section details the logic operations involved in the addition of two binary words.

2.1   A full adder (FA).

The addition of two binary words is shown in Fig. 2.1. Also shown alongside, is the addition of the corresponding decimal numbers. In the decimal number system when you add 2 digits, if the sum is '10' or higher, then you 'carry over 1' to the next higher digit. Thus, the addition of each digit also includes the 'carryover' from the summing operation of the adjacent lower digit, and can also result in a 'carry over' to the next higher digit. These 'carrys' to the next higher digit are shown encircled in Fig. 2.1. Also shown in Fig. 2.1 is the addition of these two numbers, as represented by their binary equivalents. The addition of two binary bits also includes a 'carry-in' from the adjacent lower significant bit and a 'carry-out' to the adjacent higher significant bit. Thus, a 1-bit full adder has 3 inputs (A_i, B_i, and carry-in C_i) and two outputs (sum S_i, and carry-out C_{i+1}). This 1-bit adder is referred to in literature as a full adder.

The truth table of a full adder is shown in Table 2.1. The logic equation for the sum (S_i) and the carry-out (C_{i+1}) can be written as the sum of products (Eq. 2.1). The carry logic equation can be further reduced using Boolean logic identities as shown below.

$$\begin{aligned}
S_i &= \overline{A_i} \cdot \overline{B_i} \cdot C_i + \overline{A_i} \cdot B_i \cdot \overline{C_i} + A_i \cdot \overline{B_i} \cdot \overline{C_i} + A_i \cdot B_i \cdot C_i \\
C_{i+1} &= \overline{A_i} \cdot B_i \cdot C_i + A_i \cdot B_i \cdot \overline{C_i} + A_i \cdot \overline{B_i} \cdot C_i + A_i \cdot B_i \cdot C_i \\
&= B_i \cdot C_i + A_i \cdot B_i + A_i \cdot C_i
\end{aligned} \qquad (2.1)$$

The sum logic (S_i), is generated using a 3-input XOR gate whose inputs are A_i, B_i, and C_i. The generation of carry logic (C_{i+1}) involves realizing the minterms

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using AND gates, followed by the OR operation. This is shown in Fig. 2.2. Note that the propagation delay (T_{pd}) of a full adder is equal to the two gate delays needed to realize the carry logic.

Addition of two decimal numbers

Addition of corresponding binary numbers
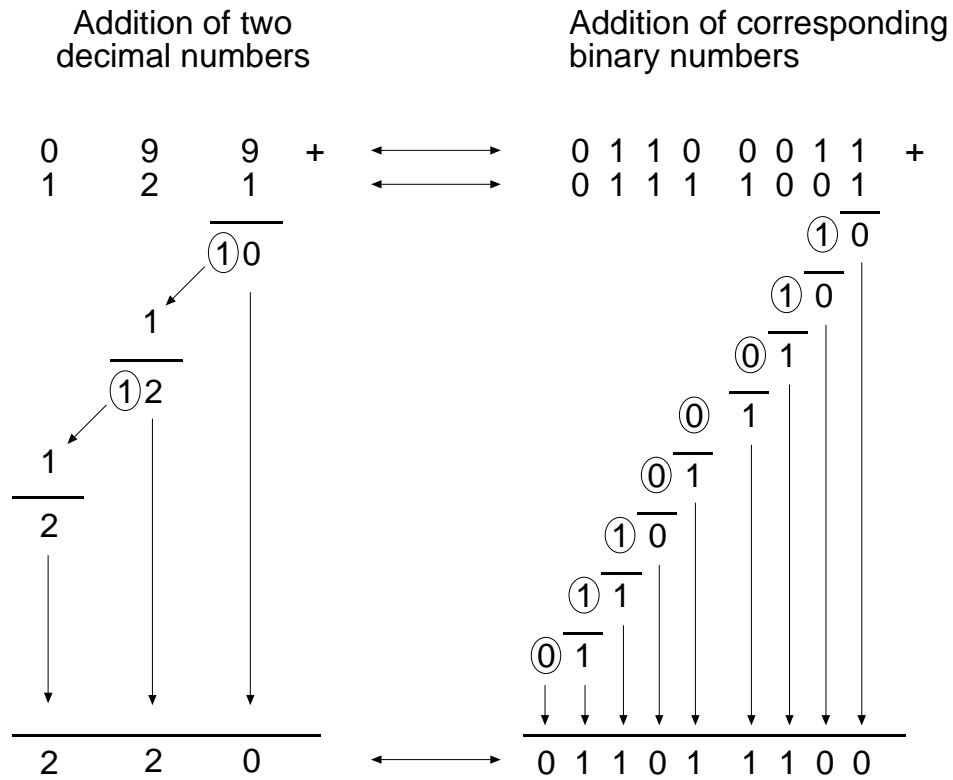
Fig. 2.1: *Shown in figure above is the addition of two decimal numbers and the corresponding addition of their binary equivalent. The 'carry over' digit/bit is shown encircled.*

Table 2.1 : *Truth table of a full adder.*

A_i	B_i	C_i	S_i	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
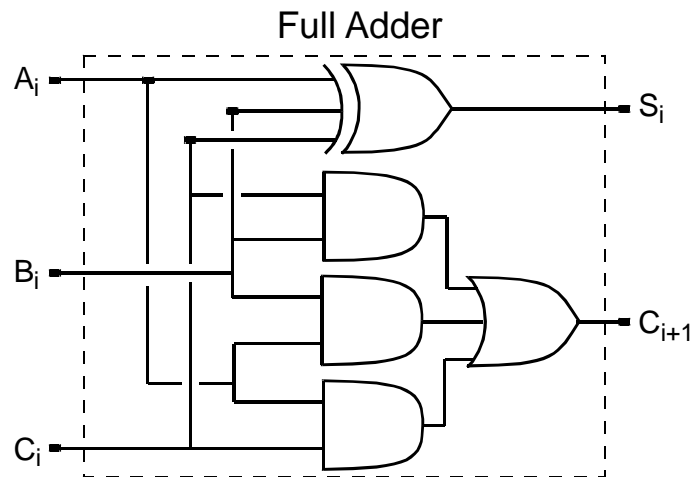
Fig. 2.2: *Logic gate realization of a full adder.*

2.2 *Ripple carry adder architecture (RCA)*

The ripple carry adder [27] is the simplest adder architecture and is shown in Fig. 2.3. The 4-bit adder shown in Fig 2.3 is made up of full adders that perform the addition for individual bits. In this architecture, the carry-out (C_{i+1}) of each full adder goes as the carry-in to the next significant bit full adder. Thus, to complete the addition you need to wait for the carry bits to propagate from the least significant bit (LSB) to the most significant bit (MSB). The worst case propagation delay to complete the addition {T_{pd} (4-bit adder)} for this 4-bit adder is shown below.

$$T_{pd}(4\text{ - bit adder}) = 4 * T_{pd}\left(\text{full adder}\right) + T_{MSFF}$$
$$= 4 * \left(2 * T_{gate}\right) + T_{MSFF}$$
$$T_{ck\,min} = T_{pd}\left(4\text{ - bit adder}\right) \quad\quad\quad (2.2)$$
$$f_{ck\,max} = \frac{1}{T_{ck\,min}} = \left(\frac{1}{4 * \left(2 * T_{gate}\right) + T_{MSFF}}\right)$$

The factor of '4' appears because the carry has to ripple through from the LSB to MSB, through 4 full adder blocks. The "(2 T_{gate})" term accounts for the gate delay involved in generating the carry-out of a full adder, and the T_{MSFF} accounts for the delay in the output master-slave flip-flop. The minimum possible clock period ($T_{ck\,min}$) must allow for this worst case delay for correct adder operation. Thus, the maximum clock frequency ($f_{ck\,max}$) is limited by the worst-case propagation delay as shown for a ripple carry adder. This can be extended for N-bit adder case also as shown below.

$$f_{ck\,max} = \frac{1}{T_{ck\,min}} = \left(\frac{1}{N*(2*T_{gate}) + T_{MSFF}} \right) \tag{2.3}$$
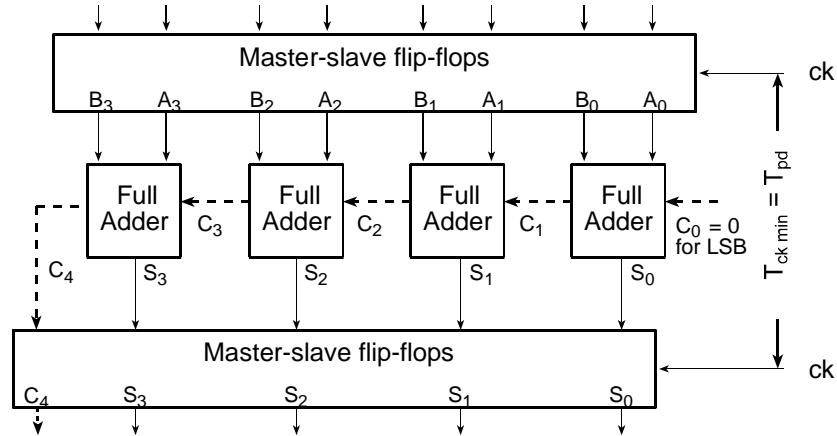
Fig. 2.3: *4-bit ripple carry adder (RCA) implemented using full adders. The worst-case propagation delay path is along the dashed lines.*

2.3 Carry lookahead adder architecture (CLA)

The carry lookahead adder [27] increases the clock rate by generating the carry-in of the various full adder blocks in 'parallel' using additional logic circuitry. This approach does away with the delay involved in the propagation of the carry-out from the LSB to the MSB as is the case with ripple carry adder. The carry lookahead approach is explained below.

Let $A = A_{n-1}.....A_1 A_0$, and $B = B_{n-1}......B_1 B_0$, be the augend and the addend inputs to a N-bit adder. C_i refers to the carry-in for the ith bit and C_{i+1} refers to the

carry-out from the ith bit. The subscript 'i' refers to any arbitrary bit. We define two additional variables called carry-generate (G_i) and carry-propagate (P_i) given by

$$G_i = A_i \cdot B_i$$
$$P_i = A_i \oplus B_i$$

(2.4)

It is possible to express both the carry and sum output bits in terms of the carry-generate and carry-propagate bit as shown below.

$$
\begin{aligned}
S_i &= (A_i \oplus B_i) \oplus C_i \\
&= P_i \oplus C_i \\
C_{i+1} &= (A_i \cdot B_i \cdot \overline{C_i} + A_i \cdot B_i \cdot C_i) + \overline{A_i} \cdot B_i \cdot C_i + A_i \cdot \overline{B_i} \cdot C_i \\
&= A_i \cdot B_i + (\overline{A_i} \cdot B_i + A_i \cdot \overline{B_i}) \cdot C_i \\
&= G_i + (A_i \oplus B_i) \cdot C_i \\
&= G_i + P_i \cdot C_i
\end{aligned}
$$

(2.5)

Starting from the least significant bit (LSB) ($i = 0$) we can recursively apply the above equation to generate the various carry-out bits as shown below.

$$
\begin{aligned}
C_1 &= G_0 + C_0 \cdot P_0 \\
C_2 &= G_1 + C_1 \cdot P_1 \\
&= G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1 \\
C_3 &= G_2 + C_2 \cdot P_2 \\
&= G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \\
C_4 &= G_3 + C_3 \cdot P_3 \\
&= G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3 \\
\vdots \\
C_n &= G_n + G_{n-1} \cdot P_n + G_{n-2} \cdot P_{n-1} \cdot P_n + \cdots + G_0 \cdot P_1 \cdot P_2 \cdot P_3 \cdots P_{n-1} \\
&\quad + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdots P_{n-1}
\end{aligned}
$$

(2.6)
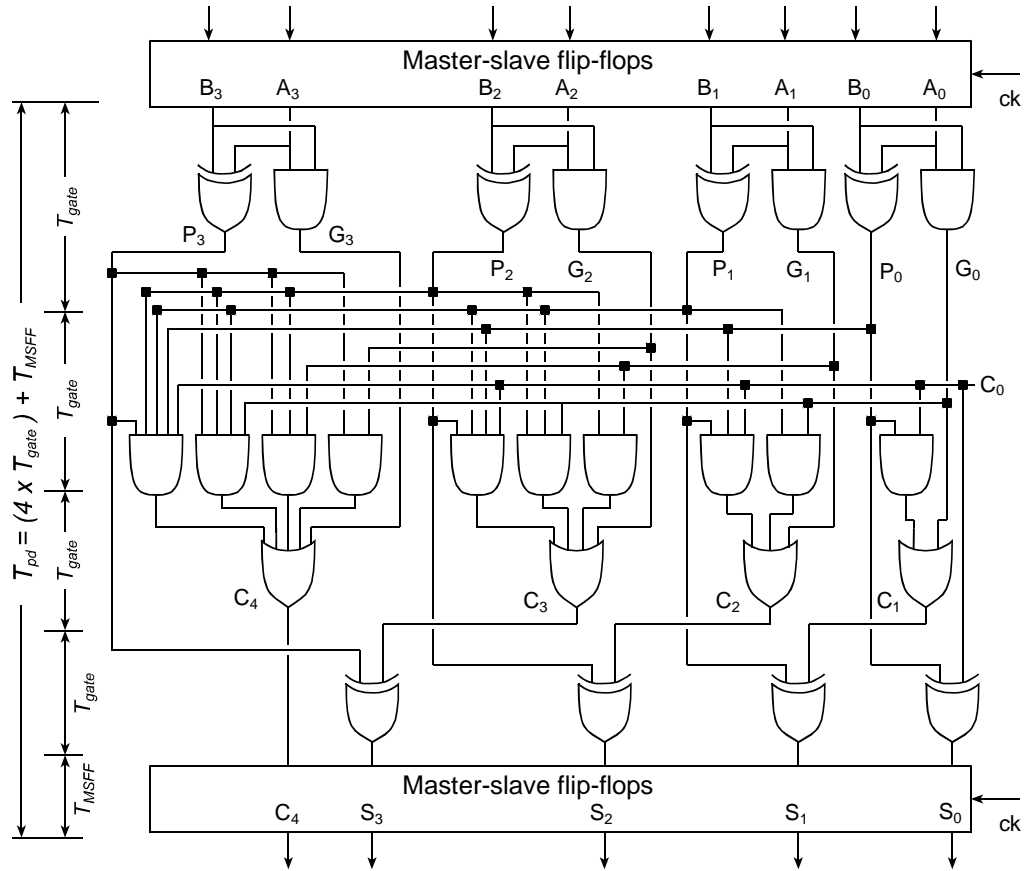
Fig. 2.4: *A 4-bit carry lookahead adder (CLA) architecture is shown above. The gate delays that determine the maximum clock rate is indicated on the left hand side. The carry-in bit $C_0 = 0$ because in the first 4-bit adder block there is no carry-in from the previous adder block.*

This set of equations is realized using the combinatorial logic circuit called the carry lookahead logic unit. In Fig. 2.4 is shown a 4-bit carry lookahead adder. The key features of this approach are shown in Fig. 2.4 and are listed below.

(i)   From Eq. 2.4 we see that all the carry-generate bits (G_i) and carry-propagate bits (P_i) can be generated simultaneously within a single gate (2-input AND or XOR gate) delay after the input words A and B are available.

(ii)   Once the carry-generate bits (G_i) and carry-propagate bits (P_i) are available, the carry-out bits (C_i) are generated within 2 gate delays corresponding to Eq. 2.6. The first gate delay corresponds to the multiple AND gates needed to generate the minterms in Eq. 2.6. (Fig. 2.4) The second gate delay corresponds to the OR gate that realizes the OR operation of the AND gate outputs to generate the carry bits (C_i).

(iii)   The addition operation is completed within 4 gate delays irrespective of the bit length N of the adder. The maximum clocking frequency of such an architecture (Fig. 2.4) is given by,

$$f_{ck\,max} = \frac{1}{T_{ck\,min}} = \left(\frac{1}{(4*T_{gate}) + T_{MSFF}} \right)$$
(2.7)

and is independent of the bit length N of the adder. This calculation neglects the effect of fan-in and fan-out on the gate delay (T_{gate}).

(iv)   As the number of bits 'N' increases, the gate count as well as the fan-in and fan-out of the gates increase drastically. The gate count of the carry

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lookahead logic unit increases as $N + (N - 1) + (N - 2)\ldots..+ 0$. Similarly, the fan-in and fan-out increases as N, making the gate delays larger as N increases.

Though faster than the ripple carry adder, the significant fan-in and fan-out requirement of CLA architecture leads to lower clock rate as the bit length N increases. The pipelined adder-accumulator offers significant speed improvement compared to the CLA architecture and is discussed in the next section.

2.4   *Pipelined adder architecture*

The pipelined adder approach [27,28] is illustrated with the example of a 4-bit adder. Let $A = A_3\ldots A_0$, and $B = B_3\ldots B_0$, be the inputs to the adder. The output sum and carry-out bits are given by $S = S_3\ldots S_0$, and $C = C_4\ldots C_1$ respectively. The carry-out (C_1) and the sum output (S_0) of the least significant bit (LSB) are generated by a full adder as shown in the upper right corner of Fig. 2.5. These outputs are latched to synchronize the output bits with the next instance of clock. The next higher input bits A_1 and B_1 are delayed by one clock period using latches and arrive at the input of the next full adder at the same instant as the carry-out (C_1) generated from the previous stage. The corresponding sum (S_1) and carry (C_2) output bits are generated and latched. The above process is then repeated for the higher bits. Thus, as you go higher towards the most significant bit (MSB), the inputs A_i and B_i get progressively delayed by one period through the use of MS flip-flops. Similarly, the sum output

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B_3 A_3 B_2 A_2 B_1 A_1 B_0 A_0

MS flip-flops ck   MS flip-flops ck   MS flip-flops ck   MS flip-flops ck

MS flip-flops ck   MS flip-flops ck   MS flip-flops ck   Full Adder C_0

C_1 S_0

MS flip-flops ck   MS flip-flops ck   Full Adder C_1 MS flip-flops ck

C_2 S_1

MS flip-flops ck   Full Adder C_2 MS flip-flops ck   MS flip-flop ck

C_3 S_2

Full Adder C_3 MS flip-flops ck   MS flip-flop ck   MS flip-flop ck

C_4 S_3

C_4 MS flip-flops ck   MS flip-flop ck   MS flip-flop ck   MS flip-flop ck

C_4 S_3 S_2 S_1 S_0

Latency = (4 T_{ck})

T_{pd} = (2 T_{gate}+ T_{MSFF})

Fig: 2.5: *A 4-bit pipelined adder realized using full adder logic blocks.*

bits $S_0 \ldots S_3$ are skewed in time by one clock period each as you go from the LSB to the MSB.

The key features of the general pipelined approach can be summarized as follows.

(i)   The total propagation delay (T_{tot}) involved in evaluating the outputs of a series of cascaded logic gates, is divided into N number of nearly equal logic propagation delay (T_{pd}) elements or blocks (ie $T_{tot} \sim N\ T_{pd}$). In the case of the 4-bit adder discussed above, $N = 4$, and the basic logic element or block is the full adder.

(ii)   The output bits of each of these logic blocks are latched to synchronize them with the clock edge. Some of the output bits of the logic blocks are inputs to the next logic block. In the case of the 4-bit adder, the carry-out bit (C_i) is an input to the next logic block.

(iii)   If some of the inputs are available at earlier clock instances, MS flip-flops are used to provide delays for these inputs, thus ensuring that all the inputs to a logic block are synchronized to the clock edge and arrive during the correct clock instance. This is very pronounced in the case of 4-bit pipelined adder where the input bits A_3 and B_3 get delayed by 3 clock cycles and arrive at the same time as the carry-bit C_3.

(iv)   Similarly, the sum-output bits from the full adders are generated at different clock instances, and they need to be realigned back so as to appear as a parallel output. This again is achieved by MS flip-flops.

(v)   The maximum clocking frequency of the pipelined logic is determined by the propagation delay through the individual logic blocks (T_{pd}) and the MS flip-flop set-up and propagation delay times. In the pipelined architecture shown in Fig. 2.5, the propagation delay T_{pd}(full adder) corresponds to the two gate delays associated with the full adder (Eq. 2.1). The maximum clock frequency is given by,

$$f_{ck\,max} = \left(\frac{1}{T_{pd}(\text{full adder}) + T_{MSFF}} \right)$$
(2.8)

This maximum clock rate is much higher than the maximum clock rate of the non-pipelined ripple carry adder (Eq. 2.2).

(vi)   Latency of a circuit is defined as the time required to generate the output once the inputs are available. In the case of non-pipelined 4-bit ripple carry adder the minimum latency is given by the total propagation delay T_{pd}(4-bit adder) (Eq. 2.2). This is because the output corresponding to a input arrives after one clock period. In the case of the 4-bit pipelined adder architecture shown in Fig. 2.5, the output corresponding to a set of inputs arrives after 4 clock cycles. Thus the minimum latency of the 4-bit pipelined adder is given by,

$$\text{Latency} = 4 * \text{T}_{\text{ck max}} = 4 * \left(\text{T}_{\text{pd}}\left(\text{full adder}\right) + \text{T}_{\text{MSFF}}\right) \tag{2.9}$$

The minimum latency of the 4-bit pipelined adder (Eq. 2.9) is higher than the minimum latency of the 4-bit ripple carry adder (Eq. 2.2) due to the presence of additional flip-flops used for data synchronization.

(vii)   The draw back of this approach is the increased circuit complexity as N increases. The number of input and output synchronizing MS latches increase as (N^2+N). Thus depending on the application, a trade-off between the clock speed and circuit complexity is necessary for a given value of N.

2.5   *Initial 8-bit pipelined adder-accumulator design*

An 8-bit pipelined adder-accumulator was designed during the initial phase of this work. For the adder to function as an accumulator, the sum output is fed back as one of the inputs (ie. $B_i = S_i$). This is shown in Fig. 2.6. As discussed in the earlier sections, the choice of pipelined adder-architecture was primarily dictated by the need for high clock rate adder-accumulators in DDFS systems. The 8-bit adder is realized using 2-bit adder blocks as shown in Fig. 2.6. The choice of 2-bit adder blocks allows for high clock rates while keeping the circuit complexity (resulting from synchronizing MS flip-flops) low enough that it can be realized in an HBT technology.

As discussed in Sec. 2.4, the maximum clock rate of a pipelined adder is limited by the propagation delay of the basic adder block used in the design. In the

case of the 8-bit adder shown in Fig. 2.6, this corresponds to the propagation delay associated with the 2-bit adder block. The main goal of this work was to evaluate circuit design techniques that would allow increased clock rate of operation of the 2-bit adder. The results from the design iterations carried out for the carry and sum logic circuits of a 2-bit adder are presented in Chapter 3.

An attempt was made to fabricate the 8-bit adder-accumulator in the transferred-substrate HBT process during the initial part of this work. The logic gates were realized using series-gated ECL logic. For testing purposes, the adder was configured as a binary counter by setting all the input bits A_i = '0' (B_i = S_i for accumulator operation) except for the least significant bit carry input C_0 = '1'. The completed chip photograph is shown in Fig. 2.7. The adder circuit had approximately 2000 HBTs. The fabrication of this IC brought forth a number of processing issues that significantly affects the yield of integrated circuits in TSHBT process. These are discussed later in chapter 5.
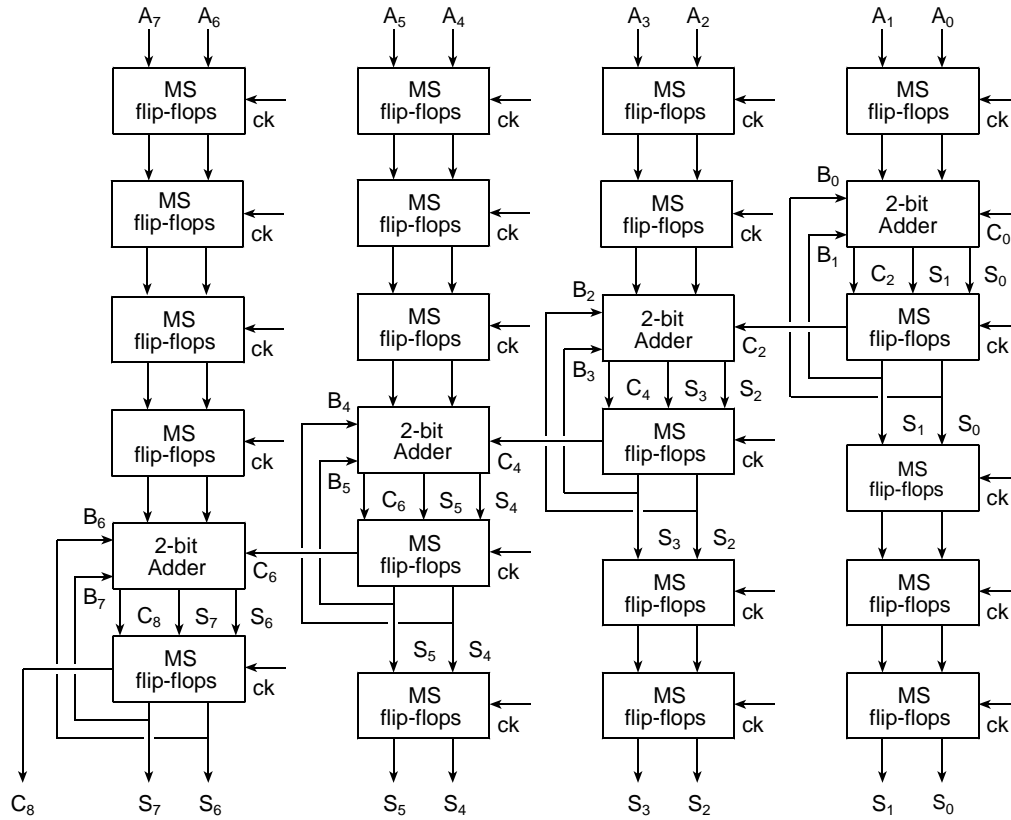
Fig. 2.6: *An 8-bit pipelined adder-accumulator realized using 2-bit adder blocks. To configure the adder as an accumulator, the sum output S is fed back as one of the inputs i.e. $B_i = S_i$.*
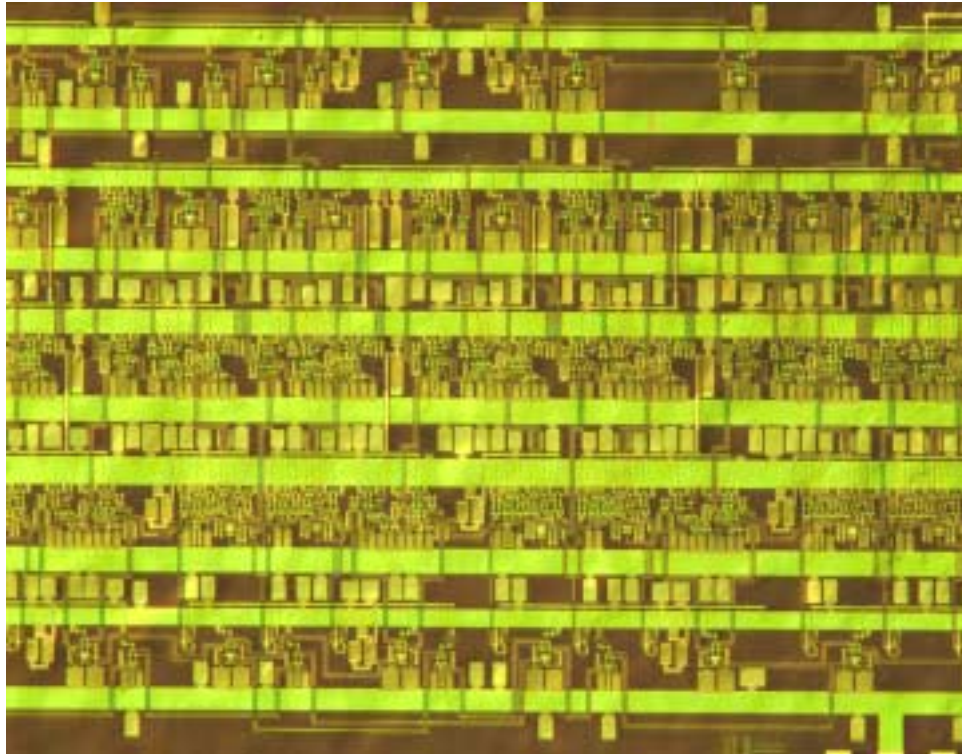
Fig. 2.7: *Chip photograph of the fabricated 8-bit adder-accumulator (2000 HBTs, non-functional circuit) is shown above.*

Chapter 3

Design of 2-bit adder block.

The design of the 2-bit adder is critical since its propagation delay (T_{pd}) determines the maximum clock speed of the 8-bit pipelined adder-accumulator. This was discussed in section 2.4 (Eq. 2.8). In this work, a number of design techniques are presented to improve the clock rate of the 2-bit adder block. These techniques are further discussed in this chapter. The maximum clock rate of operation of the different design techniques was evaluated by carrying out circuit simulations. Two different design versions were fabricated and tested. The measurement results from these wafers are also presented in this chapter.

The circuit simulation results presented here for the different circuit design approaches were carried out using the same HBT large signal model (shown in Appendix. D). This helps in identifying the improvements in the circuit performance stemming from better circuit design approaches as compared to better device design. A good device design is necessary to realize the full potential of the IC technology. The effect of the various device parameters on the propagation delay of an ECL latch is shown in Appendix C. These will be further discussed in chapter 4. The design approaches used to improve the clock rate of a 2-bit adder are presented below.

3.1 Design choice for 2-bit adder

Based on the discussions in chapter 2, there are two possible designs that can be used to realize a 2-bit adder. The 2-bit adder can be realized as a cascade of two full adders like in a ripple carry adder (Fig. 3.1) or as a 2-bit carry lookahead adder (CLA, Fig. 3.1). The critical delay path (i.e. worst-case propagation delay) for both the schemes involve four gate delays (T_{gate}). In the case of 2-bit CLA, this corresponds to the delay involved in generating S_{i+1} from the inputs A_{i+1}, B_{i+1}, and C_{i+1}. In the case of two cascaded full adders the critical delay path is the generation of C_{i+2}, from A_{i+1}, B_{i+1}, and C_{i+1}. Thus the maximum clock rate of operation of the 2-bit adder block (with output master-slave flip-flips (MSFF) as in Fig. 2.6) is given by,

$$f_{ck\,max} = \left(\frac{1}{T_{pd}(2\text{ - bit adder}) + T_{MSFF}} \right) = \left(\frac{1}{(4 * T_{gate}) + T_{MSFF}} \right) \tag{3.1}$$

The set-up time and propagation delay associated with the master-slave flip-flop is given by T_{MSFF} and is given by Eq. 3.4.

The critical path in the 2-bit CLA involves only 2-input logic gates as compared to the presence of 3-input OR gates in the case of 2 cascaded full adders. This makes the 2-bit CLA implementation marginally faster than the full adder implementation. There is no significant difference in both approaches in terms of the gate count.
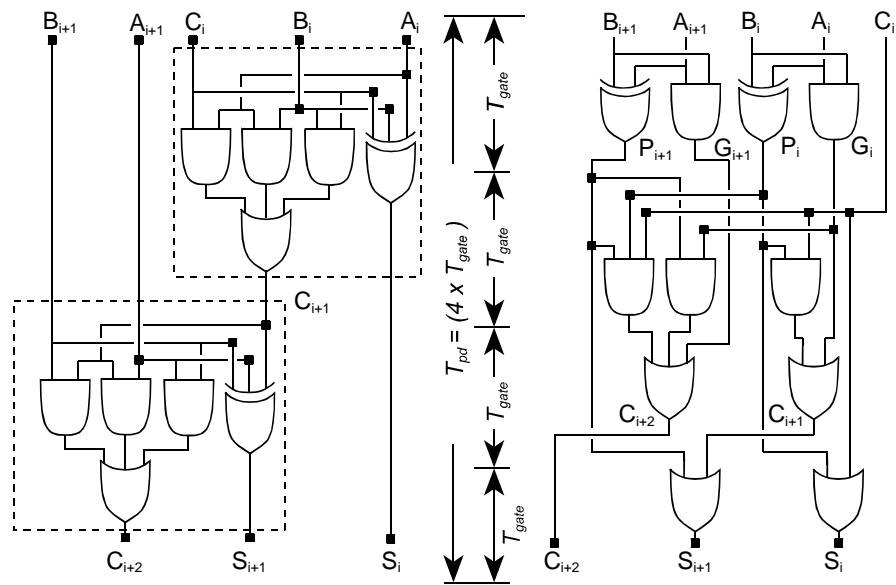
Fig. 3.1: *Shown on the left is the 2-bit adder implemented as 2 cascaded full adders and on the right is the 2-bit adder implemented as a carry lookahead adder (CLA). Also shown is the propagation delay involved for both schemes.*

3.2 Wired-OR approach

It is possible to increase the clock rate of the 2-bit adder block by realizing the OR gate using wired-OR implementation. The circuit implementation of the wired-OR approach is discussed later in this section. The wired-OR does away with the gate delay required for realizing the OR gates in the 2-bit adder implementations shown in Fig. 3.1. Full adder based realization of the 2-bit adder block has two OR gates in the critical delay path as compared to one OR gate in the critical path of the 2-bit CLA block. Thus the full adder based implementation (Fig. 3.2) of the 2-bit

adder is faster than the 2-bit CLA based approach, with maximum clock rate given by Eq. 3.2. Also, the use of wired-OR gate makes it possible to realize the 2-bit adder block using 2-input logic gates, rather than a set of 2 and 3-input logic gates.

$$f_{ck\,max} = \left(\frac{1}{(2 * T_{gate}) + T_{MSFF}} \right) \tag{3.2}$$
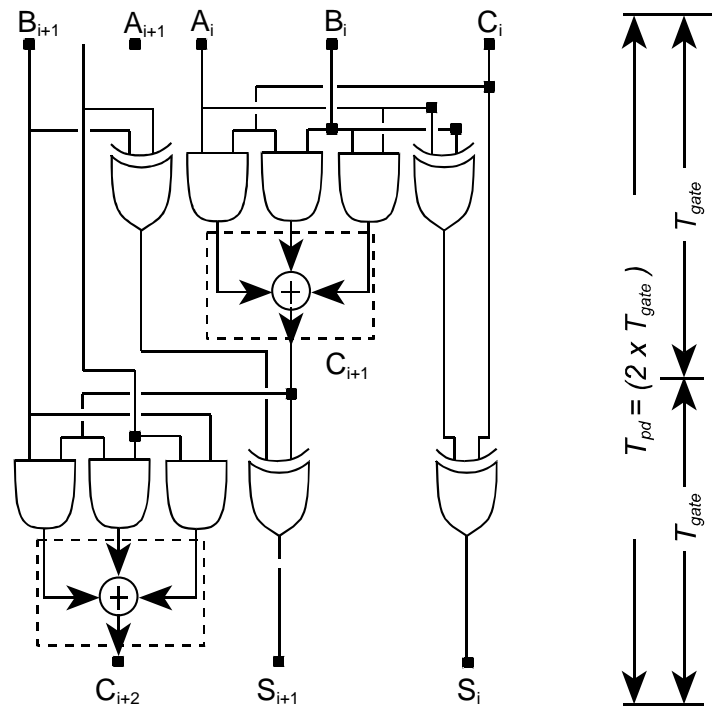
Fig. 3.2: *2-bit adder implementation using wired-OR gate is shown above. The wired-OR operation is shown within the dashed boxes. The details of wired-OR implementation are shown in Fig. 3.3.*

3.3   *Circuit implementation of Wired-OR and Wired-AND*

The details of the wired-OR implementation are discussed here. ECL logic employs differential inputs and outputs. This requires that the wired-OR operation must generate not only the correct output but also simultaneously generate the inverted output. Applying this to the full adder case means that the wired OR output must not only generate C_{i+1} but also generate $\overline{C_{i+1}}$. The logic equation for C_{i+1} is given by Eq. 2.1. Shown below are the logic equation for both C_{i+1} and $\overline{C_{i+1}}$. De-Morgan's law has been applied to simplify the $\overline{C_{i+1}}$ term in Eq. 3.3.

$$
\begin{aligned}
C_{i+1} &= B_i \cdot C_i + A_i \cdot B_i + A_i \cdot C_i \\
\overline{C_{i+1}} &= \overline{B_i \cdot C_i + A_i \cdot B_i + A_i \cdot C_i} \\
&= \overline{B_i \cdot C_i} \cdot \overline{A_i \cdot B_i} \cdot \overline{A_i \cdot C_i}
\end{aligned}
\tag{3.3}
$$

As can be seen from Eq. 3.3, C_{i+1} can be generated by doing a wired-OR operation. But, to generate $\overline{C_{i+1}}$, one needs to AND (wired-AND) the inverted outputs of the AND gates. Thus in order to replace the OR gate you need to accomplish wired-OR/AND of the 3 AND gate outputs as shown in Fig. 3.3. In ECL logic circuit it is relatively easy to do wired-OR by connecting together the outputs of the emitter followers of the logic gates (shown in Fig. 3.3).

To realize wired-AND logic is more difficult. Shown in Fig. 3.3 is the wired-AND gate realization to generate $\overline{C_{i+1}}$. This involves tying the collector node of the inverted output of the AND gates to a common resistor. A diode is placed across the

pull-up resistor to clamp the voltage to ~0.7V. The value of this pull-up resistor is chosen such that the collector node swings ~ 0.7V (i. e. I $R_{pull\ up}$ = 700 mV as against 300 mV). It is also important to maintain output swings (300 mV) compatible with the rest of the logic gates. For this purpose the common pull up resistor is utilized as a resistive voltage divider network so as to maintain compatible output voltage levels. This is shown in Fig. 3.3. Also note that diodes are used in the logic gate structure to ensure that the V_{ce} of all the transistors are below the breakdown limit (~ 1.2 V). These diodes are realized using transistors that have their bases shorted to the collector.

Throughout the above discussion it was assumed that there is negligible gate delay due to the wired-OR/AND approach outlined above. But that is not strictly true. In typical ECL logic, the emitter followers are always 'on' and see only small signal voltage swings across the base emitter terminals. Because of this, they provide a low impedance path for charging the base emitter capacitance C_{be} of the differential pair. But when you do wired-OR implementation, the emitter followers turn on and off depending on the output of the AND gates. An example of this is shown in Fig. 3.3. The switching on and off of the emitter followers not only introduces additional propagation delay in the emitter followers, but also affects the switching speed of the next logic gate that they drive.

Similarly in the case of wired-AND implementation, the large voltage swing (~ 0.7V) at the inverted output of the AND gates requires a larger than usual resistor value, which increases the gate delay of the AND gates. Also the presence of the

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diode across the pull-up resistor adds parasitic capacitance to the collector node of the AND gate. Before presenting the simulation results, the approach used for evaluating the propagation delay and the maximum clock rate of the 2-bit carry and sum logic circuits are presented. Also discussed in the next section is a simple testing approach to evaluate the clock speed of a complete 2-bit adder. All subsequent simulation results presented are based on this testing approach.
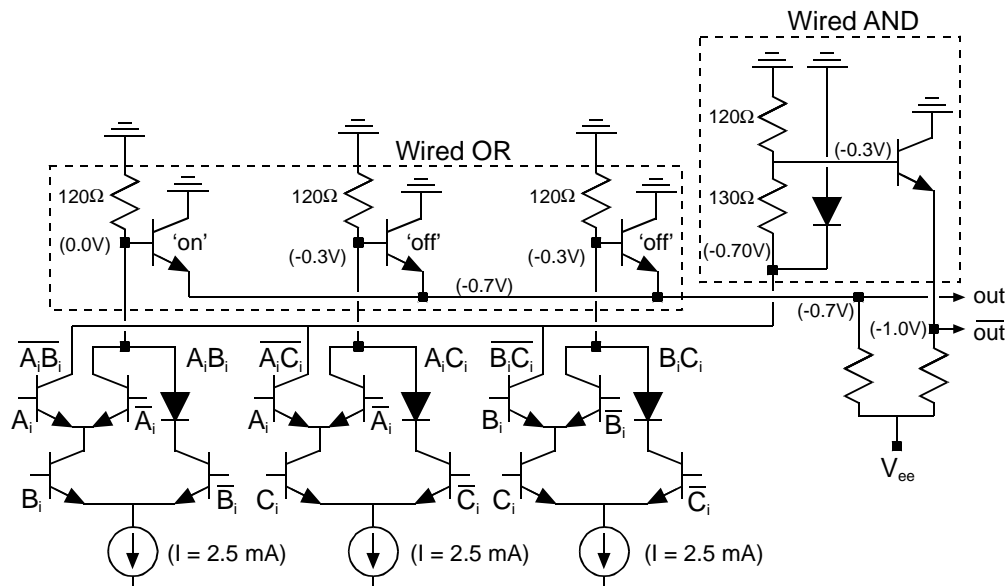
Fig. 3.3: *The wired OR and wired AND implementation are shown above. Also shown are the voltage levels for the specific case, $A_i = B_i = High$, $C_i = Low$.*

3.4   *Evaluating maximum clock rate: Test approach*

This section outlines the approach used to measure the propagation delay of both the sum and carry logic of the 2-bit adder. This approach is shown in Fig. 3.4. This is a general approach and can be used to measure the propagation delay of any combinatorial logic block. First a master-slave flip-flop (MS flip-flop) is configured as a divide by 2 and the maximum clock rate of operation is measured. The maximum clock rate of the divider is related to the propagation delay of the MS flip-flop (T_{MSFF}) and is given below.

$$f_{ck\,max}(\text{divider}) = \frac{1}{(T_{MSFF})} \qquad\qquad (3.4)$$
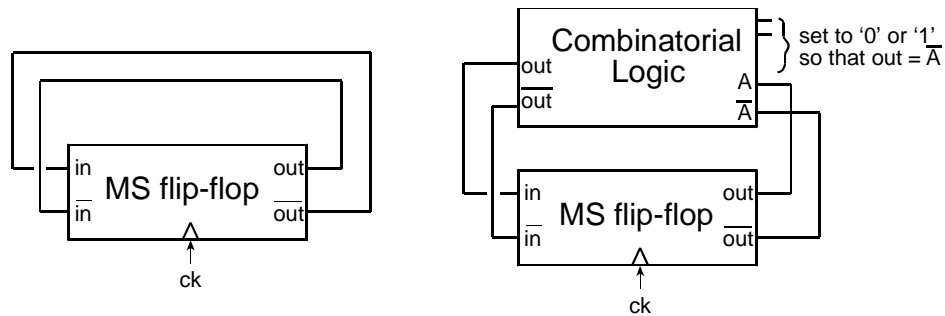
Fig. 3.4: *Evaluating the propagation delay of a combinatorial logic block by configuring it as a frequency divider. Shown on the left is an MS flip-flop configured as a frequency divider.*

To evaluate the propagation delay of a combinatorial logic circuit, the logic block is introduced in the feedback loop of the static frequency divider. The output of the MS flip-flop is connected as one of the input to the logic block. The other

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inputs of the logic block are set either high or low to enable frequency divider operation. Thus, when a new input value arrives at the input of the logic block it should propagate through the series of logic gates in the most critical delay path causing the output of the logic block to toggle. The feedback from the output of the flip-flop through the logic block to the input of the flip-flop must be out of phase to sustain frequency divider operation. The maximum clock frequency in this case is given by,

$$f_{ck\,max}\,(\text{logic block}) = \frac{1}{T_{MSFF} + T_{pd}\,(\text{logic})} \tag{3.5}$$

Thus, a measurement of the maximum clock frequency with and without the logic block in the feedback loop can be used to evaluate the propagation delay in the logic block. Therefore, from Eq. 3.4, and Eq. 3.5, the propagation delay in the logic block is given by,

$$T_{pd\,logic} = \frac{1}{f_{ck\,max}\,(\text{logic block})} - \frac{1}{f_{ck\,max}\,(\text{divider})} \tag{3.6}$$

The above approach is used to evaluate the propagation delay in the carry and sum logic circuit of the 2-bit adder. The logic block is replaced by the carry and sum logic circuits as shown in Fig. 3.5. The carry and sum logic circuit of the 2-bit adder used in the pipelined architecture uses MS flip-flops to synchronize the outputs (Fig. 2.6). Thus the clock rate as measured above (Eq. 3.5) is the maximum possible clock rate for the 2-bit adder circuit when used in pipelined adder architectures. Since the carry logic circuit is the most critical delay path, it has a

lower clocking frequency than the sum logic circuit and limits the clocking frequency of the 2-bit adder.

There also exists a simple testing approach to test the maximum clock rate of a complete 2-bit adder. To test the maximum clock rate of the 2-bit adder block with output latches, the 2-bit adder block is configured as an adder-accumulator by
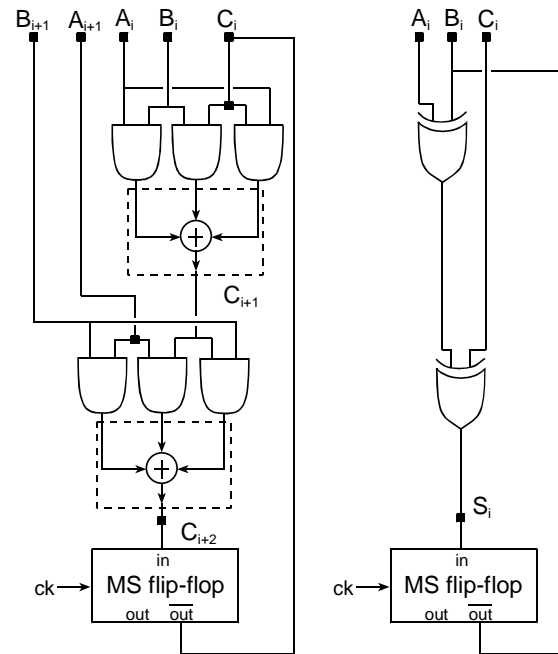
Fig. 3.5: *Evaluating the maximum clock rates of the carry and sum logic circuit by configuring them as frequency dividers. Frequency divider operation is achieved in carry logic circuit by setting the inputs $A_i = A_{i+1} = $ '1' and $B_i = B_{i+1} = $ '0' and in sum logic circuit by setting $A_i = C_i = $ '1'.*

feeding back the sum output as one of the inputs ($B_i = S_i$, $B_{i+1} = S_{i+1}$). The carry-in corresponding to the least significant bit is set to '1', and the inputs $A_i = A_{i+1} =$ '0'. This is shown in Fig. 3.6. This causes the 2-bit adder-accumulator to function as a binary counter, counting from '00' to '11' and back, in increments of one. The typical output for a 2-bit adder-accumulator realized using full adders is shown Fig. 3.7. The first sum output (S_i) is at half the clock frequency and the second sum output (S_{i+1}) is at one quarter the clock frequency. The carry out bit (not shown) C_{i+2} goes high for one clock period once in 4 clock cycles. The 2-bit adder clock rate is always slightly lower than the maximum clock rate of the sum and carry logic circuits, when tested as frequency dividers. This is due to the increased fan-out needed in the 2-bit adder circuit.
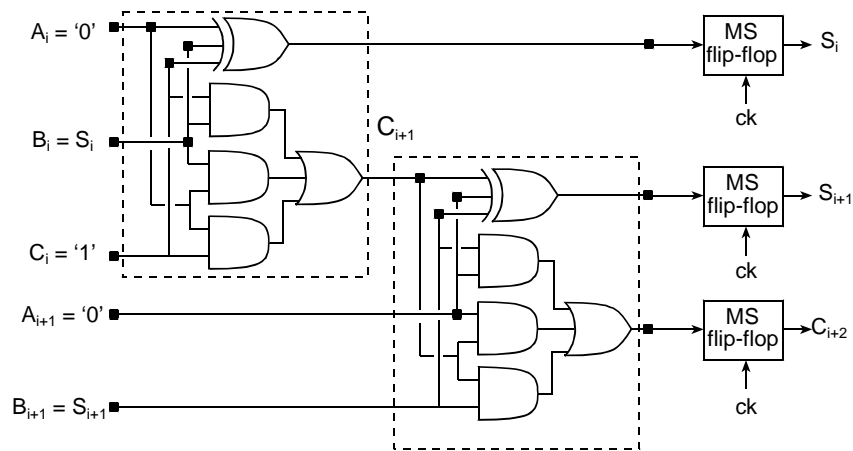
Fig. 3.6: *2-bit adder-accumulator configured as a binary counter by setting $A_i = A_{i+1} =$ '0' and $C_i =$ '1'. The corresponding simulated output is shown in Fig. 3.7.*

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3.5   *Comparison of Full adder and wired OR approach*

To compare the circuit performance of the different design approaches, circuit simulations were carried out using the HBT device model shown in Appendix D. The ADS computer aided design tool was used for circuit simulation and mask layout. The effects of interconnect lines and cross over capacitances on the circuit performance have not been included in any of the circuit simulations.
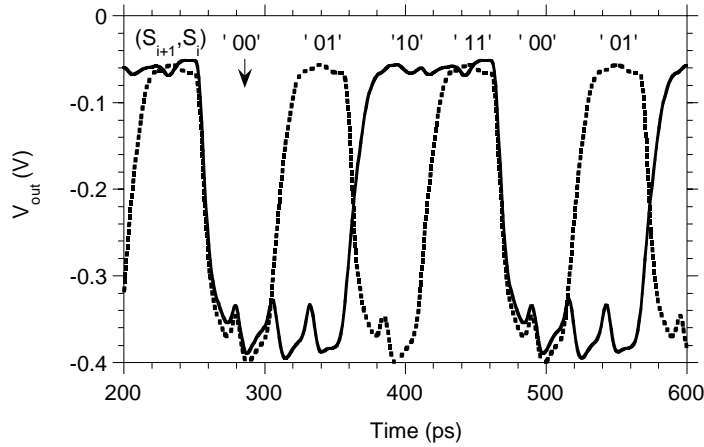
Fig. 3.7: *Simulated sum output waveforms (S_{i+1}, S_i) of a 2-bit adder for 19 GHz clock (f_{ck}) input. S_i (dotted line) is at f_{ck} /2, and S_{i+2} (solid line) is at f_{ck}/4. Also shown is the binary output sequence corresponding to the output waveforms.*

The simulations of the 2-bit carry logic circuit realized using the wired-OR approach shows significant reduction in the propagation delay as compared to the full adder implementation. The maximum clock rate of the MS latch when configured as a static frequency divider is 50 GHz and corresponds to 20 ps propagation delay. The maximum clock rate of the 2-bit carry logic circuit when

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configured as a static frequency divider (Fig. 3.5) is about 25 GHz for the wired-OR approach as opposed to 19 GHz for the full adder approach. The corresponding propagation delays are 20 ps for the wired-OR implementation as compared to 33 ps for the full adder implementation. The simulated output waveform for the carry logic circuit realized in wired-OR implementation is shown in Fig. 3.8. The sum logic circuit is identical in both the approaches. The 2-bit adder-accumulator realized using the wired-OR approach clocks up to a maximum clock rate of 24 GHz when configured as a binary counter. The simulated sum output waveforms are shown in Fig. 3.9.
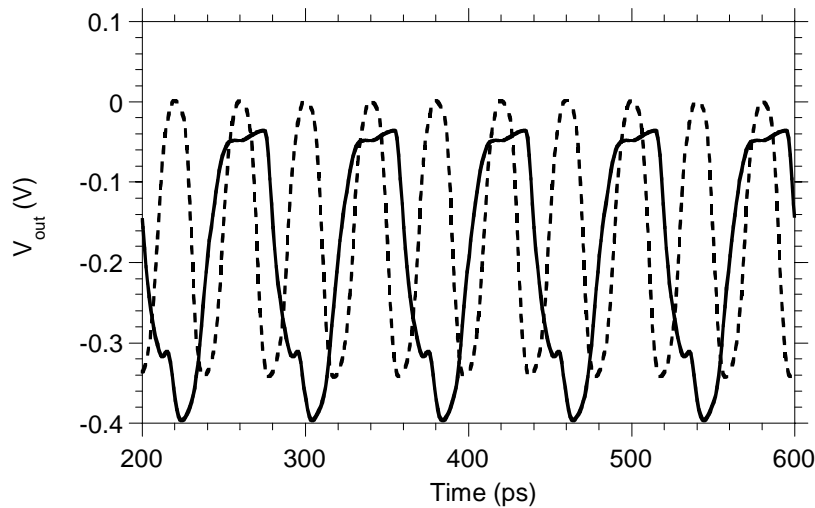
Fig. 3.8: *Simulated output waveform at 12.5 GHz of the carry logic circuit configured as a static frequency divider. The clock input (broken line) is at 25 GHz*

3.6   *Gate design considerations*

The designs were to be fabricated in transferred substrate HBT technology. Some of the considerations required for using this technology are summarized below to better understand the design flexibility/constraints imposed by the technology.

1) The maximum emitter current density of device operation, J_e is around 2.0 mA/μm^2. At this current density, the maximum allowable $V_{ce} = 1.0$ V. Operation above these limits leads to breakdown of the device. A conservative current density of 1.0 mA/μm^2 is used in circuit design.

2) The minimum feature size in this technology is about 0.6 μm on a flat surface and is dictated by the lithography tool (Stepper). Any surface topology will increase the minimum feature size.

3) TSHBT technology allows for microstrip interconnect lines. This is important when working in GHz frequency range, since terminated microstrip lines can be employed as interconnect lines to prevent multiple reflections from the load/source end. The maximum possible microstrip line impedance realizable is about 120 Ohm (2.0 micron line width) in this technology.

4) Passive elements realizable in this technology include resistors and capacitors. Resistors are realized using thin film NiCr metal with sheet resistivity of 50 Ω/Y (400 Å. thickness). Also possible are metal-insulator-metal (MIM) capacitors with silicon nitride (SiN) as the dielectric.

5) During the substrate transfer process, the wafer shrinks by approximately 0.3μm/mm. So, depending on the cell size, the collector mask level must provide for this shrinkage in terms of collector-to-emitter alignment tolerance (Fig. 3.11). Another possibility is to correct for wafer shrinkage by accounting for the shrinkage in the collector mask level. The latter method achieves superior circuit performance because the collector to base overlap area (that contributes to C_{cb}) is significantly smaller.
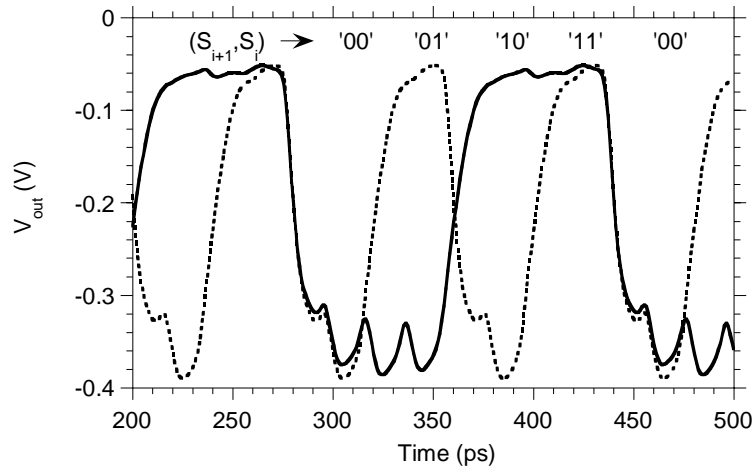
Fig. 3.9: *Simulated output waveform of the 2-bit adder-accumulator circuit when configured as a binary counter (setting $A_i = A_{i+1} = $ '0' and $C_i = $ '1'). The input clock frequency is at 24 GHz. S_i (dotted line) is at f_{ck} /2, and S_{i+2} (solid line) is at f_{ck}/4.*

Once the circuit topology has been finalized, the transistor level design starts with the choice of voltage swings for the logic levels. A logic swing of 300mV

provides sufficient noise margin and has also been successfully used in earlier work in this technology [25,26].

Gate-to-gate interconnect is run as microstrip lines terminated at the load end. This is shown in Fig. 3.10. The pull-up resistors of the gate are used as termination elements at the load end. Since the maximum realizable microstrip impedance value is 120 Ω in this technology, the maximum value of the pull-up resistor is limited to 120 Ω when used as microstrip termination elements. Power dissipation can be decreased by reducing the switching current I that is drawn by the logic gate (Fig. 3.10). Since the voltage swing is fixed (ΔV = I $R_{pull\ up}$ = 300mV), the switching current is given by,

$$I = \frac{\Delta V}{R_{pull\ up}} = \frac{300mV}{120\Omega} \approx 2.5\,mA \tag{3.6}$$

The value of the switching current (I = $J_e\ A_e$), along with the maximum allowable current density of operation (J_e = 1 mA/μm^2), decides the emitter area A_e of the transistors used in the current steering logic. In this case, the value of the emitter area A_e is 2.4 μm^2.

The extrinsic device resistances and capacitances are functions of emitter length and width as well as the alignment tolerances chosen for the process. The geometry dependence of the device parameters is shown in Appendix A and Appendix B. For a constant emitter area, the base contact resistance is inversely proportional to emitter length L_e. The extrinsic base-collector capacitance C_{bcx} depends on the area

of the extrinsic base-collector junction as shown shaded in Fig. 3. 11. As can be seen C_{cbx} also depends on the emitter length L_e for a given emitter area A_e. The emitter extrinsic resistance $r_{ex.}$ scales with the emitter area A_e.
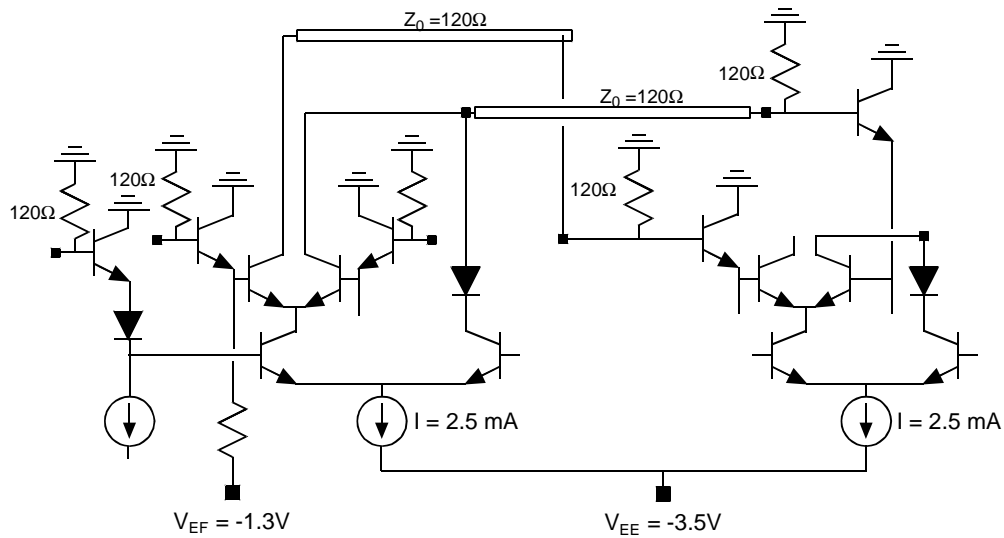
Fig. 3.10: *Design features of a 2-level logic gate including gate to gate interconnects, run as terminated microstrip line is shown above.*

A review of the basic scaling properties of transferred-substrate HBT and its effects on logic switching speed has been reported by Rodwell et al.[16]. Also shown in Appendix C is the method of time constant analysis of an ECL latch that describes the effect of various device parameters on its propagation delay. Excellent RF and digital circuit performance have been observed for emitter length-to-width ratios of 8 to 12 [20,21]. Hence, an emitter size of 4.0 μm x 0.6 μm was chosen.

Note that 0.6 μm is the minimum possible feature size. The rest of the device geometry then follows from the alignment tolerances defined by the technology and is shown in Fig. 3.11. A collector width of 3.0 μm was used to account for the wafer shrinkage of 0.3 μm/mm. As mentioned earlier, it is possible to account for wafer shrinkage by accounting for it in the collector mask level. This would have resulted in a collector width of 1.6 μm (i.e. $L_{corr} = 0$) which reduces the base-collector capacitance of the transistors by nearly 50% when compared to a 3 μm collector width. But at that point in time, the ability to correct for wafer shrinkage on the collector mask was not known to us. Hence, 3.0 μm wide collectors were used in this design.

Circuit simulations indicate that the optimum emitter follower (transistor) area is around two times the transistor area used in the differential pair. The emitter followers are biased at 1.0 mA/μm^2. Top level emitter followers use a lower negative power supply of 1.3 V and are biased with pull down resistors as shown in Fig. 3.10. The use of a lower power supply voltage (-1.3 V) for the emitter followers significantly reduces the power consumption as opposed to using the power supply voltage (-3.3 V) of the current switching transistors. The down side of doing this is the increased wiring complexity required to run the separate emitter follower power supply bus. The current switching transistors and the lower emitter followers are biased using current sources.

W_c = 3.0 μm

W_e emitter width,
L_e emitter Length,
W_b base width,
W_c collector width,
L_corr correction for
      wafer shrinkage,
L_tol Alignment tolerance,
L_b base contact transfer
      length,

C

L_{tol} = 0.5 μm

L_e = 4.0 μm

E

B

W_b = 4.0 μm

= (L_{corr} + L_{tol})

= (0.7 +0.5) μm

=   1.2 μm

= (L_b + L_{tol})

= (1.2 +0.5) μm

=   1.7 μm

W_e = 0.6 μm
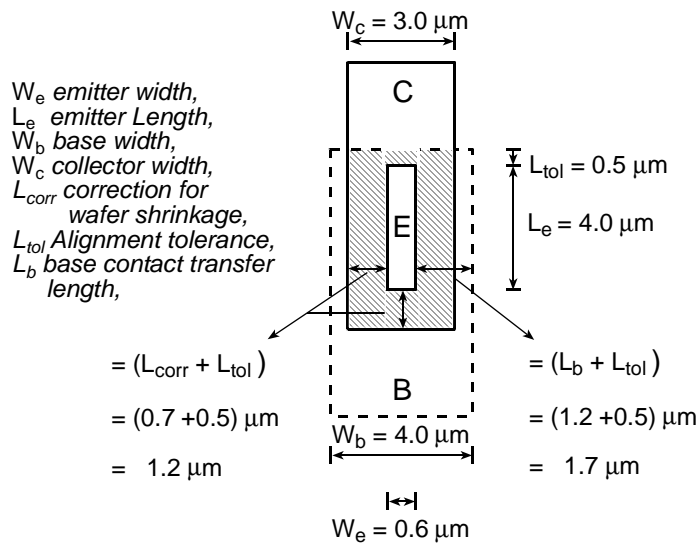
Fig. 3.11: *Device geometry of the transistors used in the differential pair. Shown shaded is the base-collector area that contributes to the extrinsic base-collector capacitance.*

3.7   Measurements and results: first-generation 2-bit adder

DC and RF measurements were carried out on the device. The epitaxial layer structure used is shown in Fig. 3.12. The results from the common emitter I_c-V_{ce} measurements are shown in Fig. 3.13. The transistors exhibit DC current gain in the range of 40 to 60 and operate up to a maximum current density (J_e) of 2.0 mA/μm^2. Gummel plot indicates an ideality factor close to 1 for the collector current and an ideality factor of 1.2 for base current. Measurement of base TLM (Transmission Line Measurement) patterns indicate a base contact resistivity of 1.6 x 10^{-6} Ω-cm^2, a transfer length (L_b) of 0.5 μm, and base sheet resistance of 850 Ω/Y.

Results of RF measurements on the above device gave a f_t and f_{max} of 140 GHz and 140 GHz respectively at $V_{ce} = 1.0$ V and $I_c = 5.0$ mA. This is shown in Fig. 3.14. Typical value of f_t and f_{max} for this device geometry is about 180 GHz and 200 GHz. The device parameters extracted from the S parameter measurements [29,30] are shown in Fig. 3.15. Measured base-collector capacitance C_{cb} was found to be two times larger than the typical value (~ 6 fF) for the device geometry used. This resulted in the lower than expected value of measured current gain (f_t) and power gain (f_{max}). The exact cause for the high C_{cb} could not be identified. Also the extracted base-collector intrinsic capacitance C_{cbi} is a significant fraction of C_{cb}. The effect of large C_{cb} is quite significant and degrades the digital circuit performance described later in this section.

The sheet resistivity of thin film deposited NiCr resistors was found to be 25 Ω/Y as opposed to the designed value of 50 Ω/Y. This was due to the malfunction of the deposition monitor during the NiCr deposition. This resulted in resistor values on chip that were lower than the design value by 2:1. This affected the current source biasing of the gates as the current sources are realized on chip as current mirrors. This is shown in Fig. 3.16. The design values are shown in parenthesis. As is shown below, the low value of resistors led to current sources operating at two times the designed value. Thus, the transistors are operating at $2mA/\mu m^2$ as opposed to the designed value of $1mA/\mu m^2$. This was confirmed by measurements carried out

1000 Å n+ InGaAs : 10^{19} cm-3 Si
199.2 Å n+ InGaAs/InAlAs Grade : 10^{19} cm-3 Si
700 Å n+ InAlAs : 10^{19} cm-3 Si
500 Å n+ InAlAs: 8.0×10^{17} cm-3 Si
299.7 Å InAlAs/ InGaAs Grade
400 Å p+InGaAs: 52 meV Band gap Grade : 4.0×10^{19} cm-3 Be
400 Å n InGaAs : 1.0×10^{16} cm-3 Si
50 Å n InGaAs : 1.0×10^{17} cm-3 Si
2550 Å n InGaAs : 1.0×10^{16} cm-3 Si
2500 Å InAlAs UID InAlAs Buffer layer

Fig. 3.12: *Epitaxial layer structure used in this process run is shown above.*
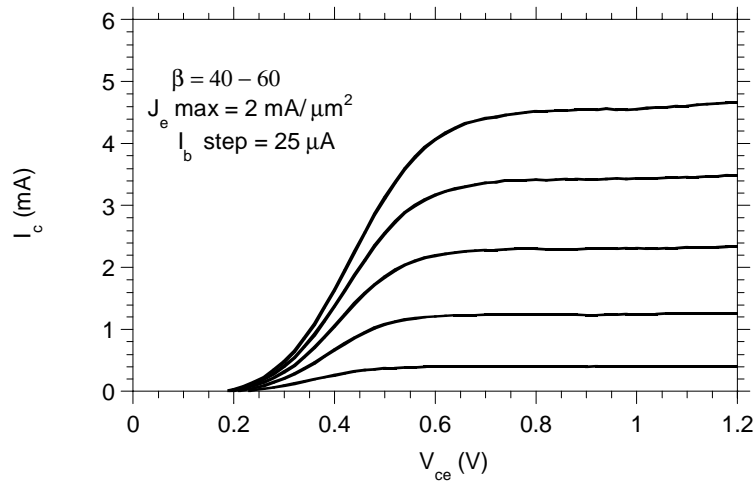
Fig. 3.13: *Common emitter $I_c – V_{ce}$ characteristics of a HBT with emitter dimension of 4.0 x 0.6 μm^2 and collector dimension of 5.0 x 3.0 μm^2.*
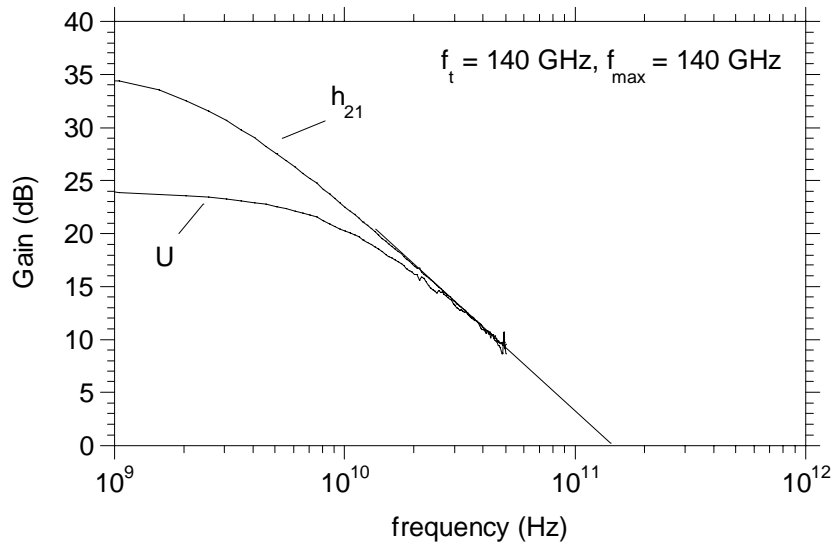
Fig. 3.14: *RF measurement results on a device with emitter dimension 4.0 x 0.6 μm^2, and collector dimension 5.0 x 3.0 μm^2 at V_{ce} = 1.0V and I_c = 5.0 mA.*

on the current source test circuits. The logic swing (I x R) is unaffected and is still 300 mV. This was verified during the DC functional testing of an XOR gate circuit.

The propagation delay of the master-slave flip-flop was measured by configuring it as a static frequency divider. The maximum clock rate was found to be 36 GHz and is much lower than the simulated value of 50 GHz. The carry and sum logic circuit shown in Fig. 3.5 was also tested and the maximum clock rate was found to be 8 GHz and 14.6 GHz respectively.
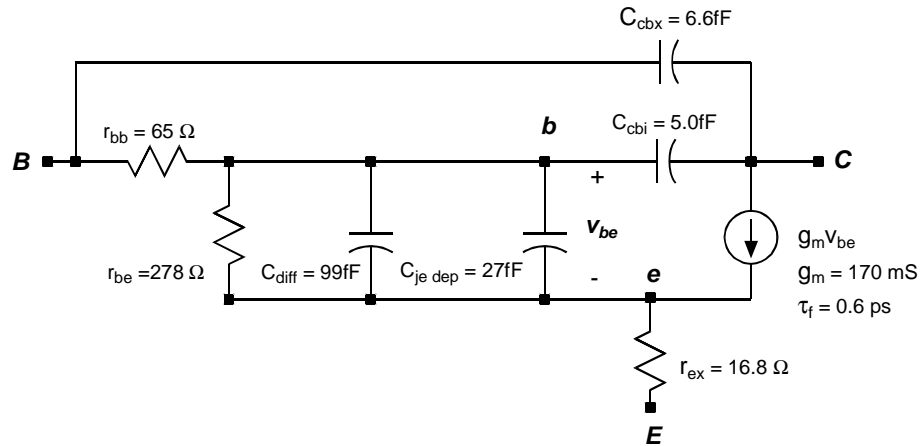
Fig. 3.15: *Hybrid-pi equivalent circuit model of the device The device had emitter dimension 4.0 x 0.6 μm^2 and collector dimension of 5.0 x 3.0 μm^2 and was biased at a V_{ce} of 1.0V and I_c of 5.0 mA.*

The fabricated chip photograph of the carry and sum logic circuits of the 2-bit adder is shown in Fig. 3.17 and Fig 3.18 respectively. The measured output waveforms of the carry and sum logic circuit are shown in Fig. 3.19 and Fig. 3.20 respectively. The carry logic circuit had approximately 250 transistors and the sum logic circuit had approximately 150 transistors. These are the largest circuits yielded so far in transferred-substrate HBT technology. The performance of these circuits was significantly lower when compared to simulated performance (25 GHz, Fig. 3.8). Simulations had indicated a maximum clocking frequency of 25 GHz. The reduction in the measured clock rate when compared to the simulated performance

is mainly due to the 2:1 larger base-collector capacitance (C_{cb}) of the devices measured during this process run. This was verified by simulating the circuit performance using the extracted parameters of the device. An attempt was also made to demonstrate a complete 2-bit adder-accumulator. The 2-bit adder-accumulator circuit has about 600 HBTs, and the yield on this and the subsequent process run was not high enough to realize a functional 2-bit adder-accumulator.
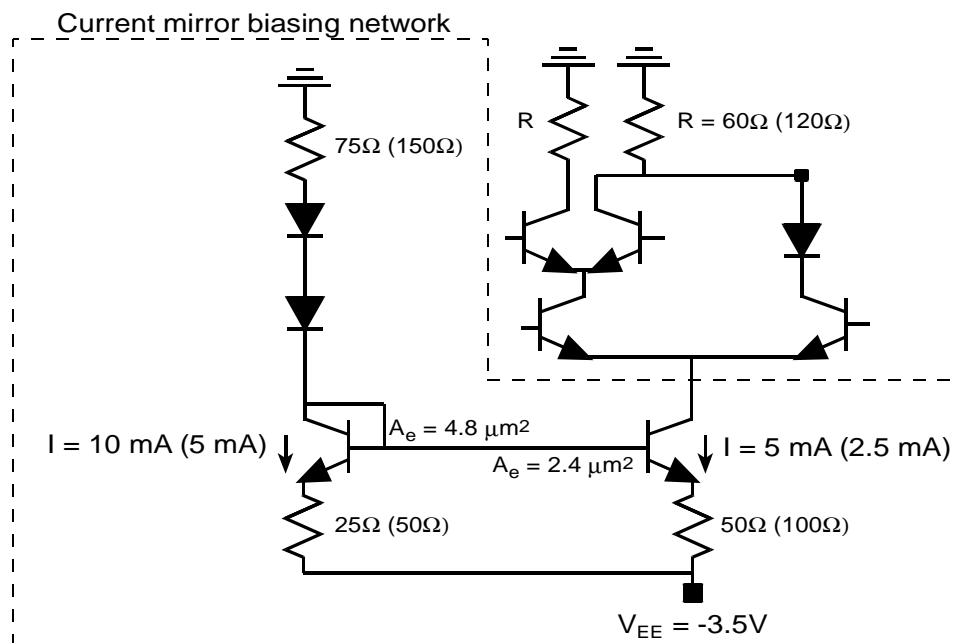
Fig. 3.16: *Current mirror biasing network of the logic gate is shown inside the dashed box. The measured values of resistors are also shown, with the design values indicated in parenthesis.*
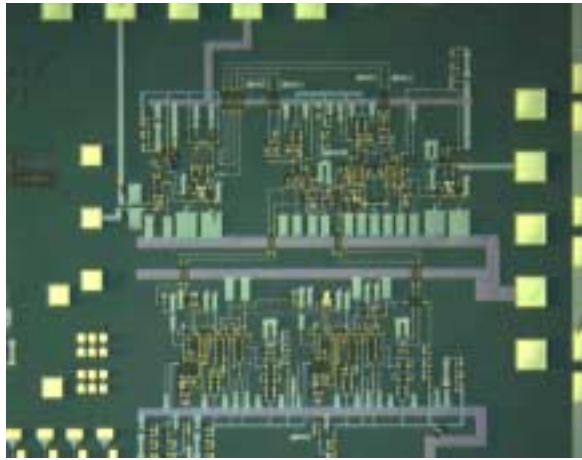
Fig. 3.17: *Chip photograph of the fabricated 2-bit carry logic circuit. The IC had approximately 250 transistors.*
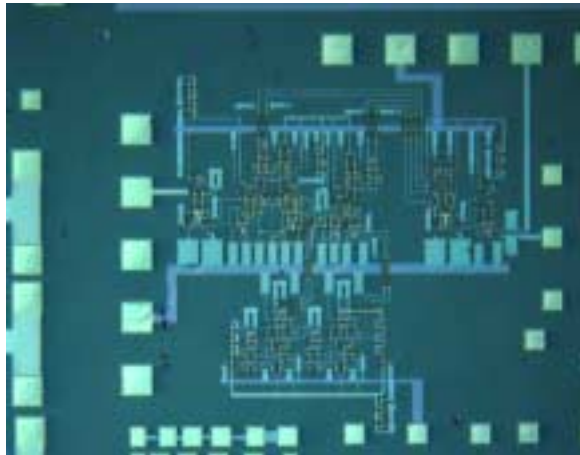
Fig. 3.18: *Chip photograph of the sum logic circuit (approximately 150 HBTs).*
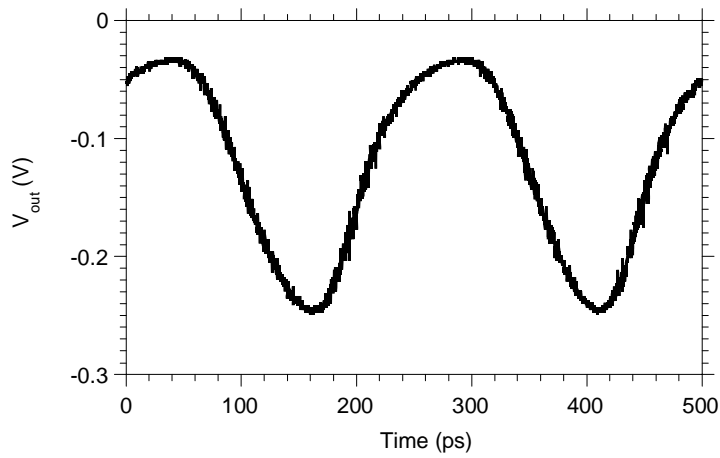
Fig. 3.19: *Measured output waveform of the carry logic circuit of a 2-bit adder configured as a frequency divider. The input clock frequency is 8 GHz, and the output waveform shown above is at 4 GHz.*
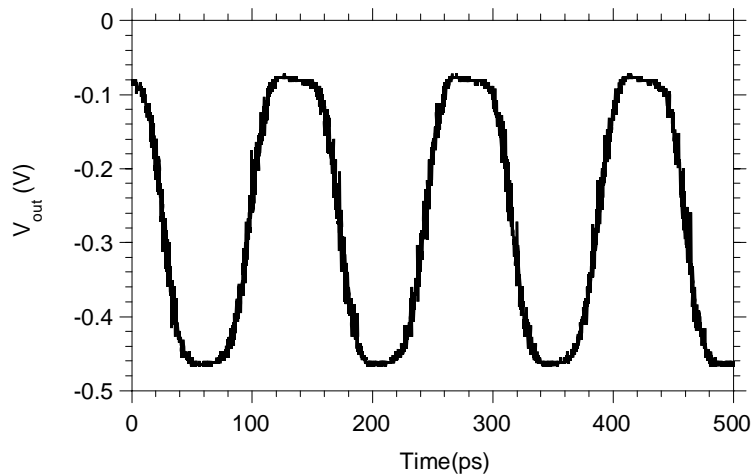
Fig. 3.20: *Measured output waveform of the sum logic circuit. The input clock frequency is 14.6 GHz and the output waveform shown above is at 7.3 GHz.*

3.8   Design modifications: New 3-level logic gate for carry logic

As has been discussed in section 3.2, the carry logic of the 2-bit adder is realized using AND-OR logic (Eq.3.3). Improvement in clock rate was achieved by realizing the OR gate through a wired-OR approach discussed earlier. It is possible to realize the AND-OR logic needed to generate the carry output by using a single 3-level series-gated logic gate. This is shown in Fig. 3.21.

Simulations of the single 3-level logic gate show that this structure should have lower propagation delay than the wired-OR/AND logic used earlier. Detailed analysis (MOTC, method of time constants) of the propagation delay associated with ECL gates have been reported earlier [29,31]. Also presented in Appendix C is the MOTC analysis of an ECL latch. MOTC analysis shows that the propagation delay in a series-gated logic gate consists of two components. The first component is the propagation delay involved as the current steers it's way from the current source through the differential transistor pairs all the way to the output node. The second component is the time delay involved in charging the capacitance associated with the output node. This is the most significant propagation delay term and depends on the capacitance associated with the output node (C_{cb}) as well as the resistance associated with the charging path. The presence of the larger pull up resistance (250Ω) and additional capacitance from the limiting diode at the output node of the wired-OR/AND implementation causes it to be slower than the 3-level series-gated logic gate implementation shown in Fig. 3.21.
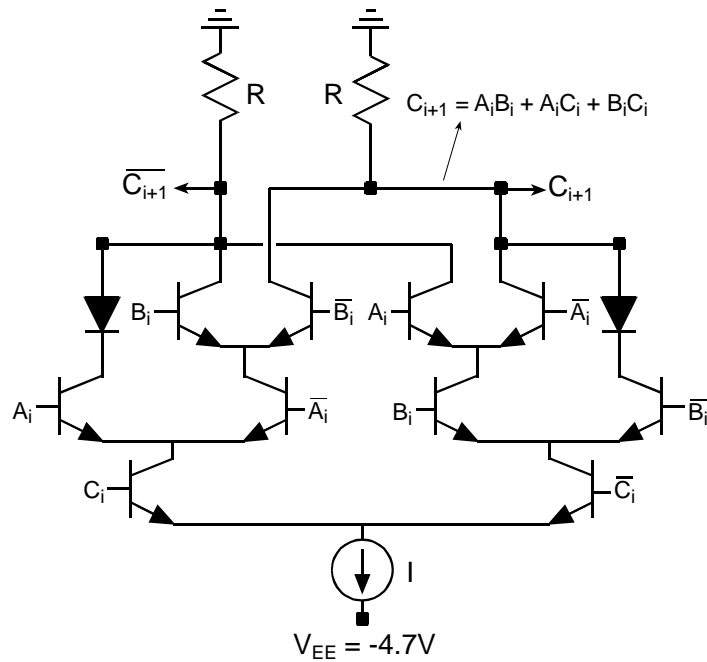
Fig. 3.21: *A new 3-level series-gated logic gate implementation of the AND-OR logic to generate the carry-out of a full adder.*

Simulations carried out using this new 3-level series-gated logic gate to implement the 2-bit adder carry logic (Fig. 3.22), exhibited a 1.1:1 improvement in speed as compared to the wired-OR/AND design. The maximum simulated clock rate was 27 GHz. The simulated output waveform is shown in Fig. 3.23. The propagation delay T_{pd} (carry logic) of the carry logic circuit (Fig. 3.22) is given by,

$$T_{pd}(\text{carry logic}) = 2 * \left\{ T_{pd}(\text{logic}) + T_{pd}(\text{ECL latch}) \right\} \qquad (3.7)$$

Where $T_{pd}(\text{logic})$ is the propagation delay associated with the 3-level series-gated logic gate and $T_{pd}(\text{ECL latch})$ is the propagation delay associated with the ECL latch. The maximum clock rate is related to the propagation delay of the carry logic circuit of the 2-bit adder as shown below.

$$f_{ck\,max}(\text{carry logic}) = \frac{1}{T_{pd}} = \frac{1}{2 * \left\{ T_{pd}(\text{logic}) + T_{pd}(\text{ECL latch}) \right\}} \qquad (3.8)$$
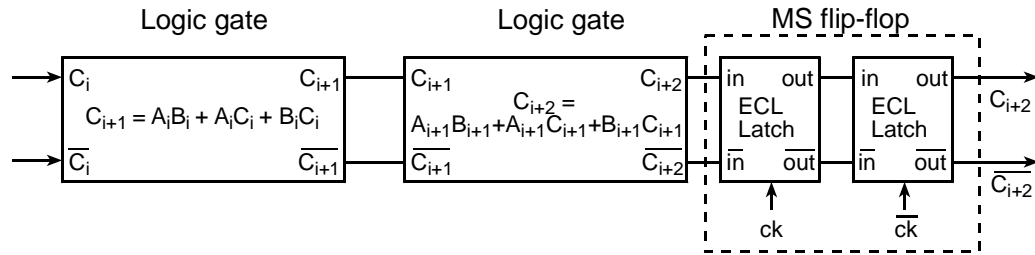
Fig. 3.22: *Carry logic circuit of the 2-bit adder is shown above. To evaluate the propagation delay of the carry logic circuit its configured as a frequency divider by setting* $A_i = A_{i+1} = '1',\ B_i = B_{i+1} = '0',\ \text{and}\ C_i = \overline{C_{i+2}}.$

It is possible to further increase the maximum clock rate of the carry logic circuit of the 2-bit adder as is discussed in the next section.
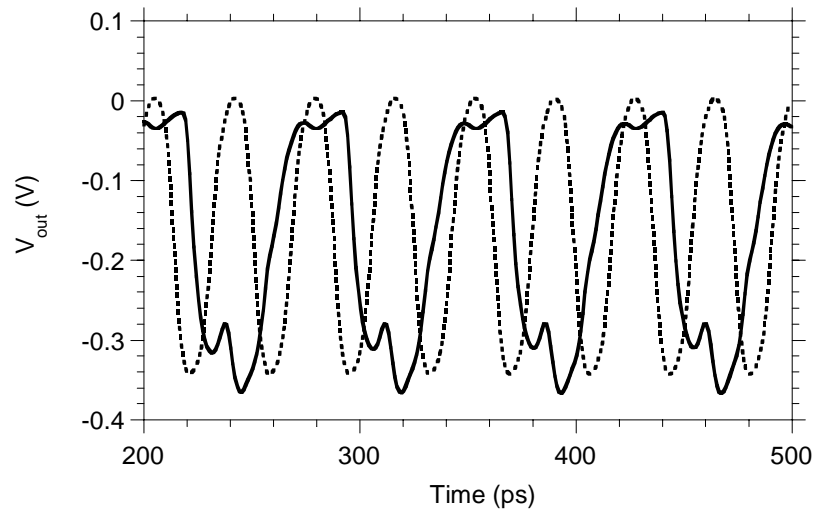
Fig. 3.23: *Simulated output waveform of the 2-bit carry logic circuit when configured as a frequency divider. The input clock frequency is 27 GHz, and the output frequency is 13.5 GHz.*

3.9 Merging the logic evaluation and latching operation

Further improvement in speed of the carry logic circuit discussed above can be achieved by merging the latching operation carried out by the MS flip-flop with the logic evaluation (AND-OR). Each of the ECL latch stages of the MS flip-flop (Fig. 3.24) can be merged with the logic gate. Shown in Fig. 3.24 is the circuit diagram of a ECL latch. To merge the logic evaluation with the latching operation, the input stage of the latch is replaced with the logic gate. This is illustrated in Fig. 3.25. The merged AND-OR-Latch results in a 4-level series-gated logic structure, with the

clock input forming the fourth level in the series-gated structure (Fig. 3. 25). The resulting circuit diagram of the carry logic circuit is shown in Fig. 3. 26.

The merged AND-OR-Latch approach shown in Fig. 3.26 has lower propagation delay as compared to realizing the carry logic using cascaded AND-OR gate with the MS flip-flop at the output (Fig. 3.22). This is analyzed below. The propagation delay associated with the ECL latch can be split into two components:

$$T_{pd}(\text{ECL latch}) = T_{pd}(\text{input stage}) + T_{pd}(\text{latch stage}) \qquad (3.9)$$

Where T_{pd}(input stage) and T_{pd}(latch stage) are the contributions to propagation delay corresponding to the input stage and the latching stage respectively of the ECL latch shown in Fig. 3.24. Based on the circuit diagram shown in Fig. 3.24, the propagation delay of the carry logic circuit using the merged AND-OR-Latch approach can be written as the sum of the propagation delays in the signal path. This is shown below.

$$\begin{aligned} T_{pd}(\text{carrylogic}) &= T_{pd}(\text{logic}) + T_{pd}(\text{latch stage}) \\ &+ T_{pd}(\text{logic}) + T_{pd}(\text{latch stage}) \\ &= 2 * (T_{pd}(\text{logic}) + T_{pd}(\text{latch stage})) \end{aligned} \qquad (3.10)$$

Note that T_{pd}(latch stage) corresponds to the propagation delay resulting from the latching stage of an ECL latch and should not be confused with the propagation delay of an ECL latch (Fig. 3.24, Eq. 3.9). The propagation delay of the merged AND-OR-Latch approach (Eq. 3.10) is lower when compared to the propagation delay of the non-merged implementation (Eq. 3.7) for the carry logic circuit

implementation shown in Fig. 3.22. The difference is the absence of the propagation delay associated with the input stage of the ECL latch in Eq. 3.10. The lower propagation delay of the merged AND-OR-Latch approach was confirmed by circuit simulations, which indicated a maximum clock rate of 42 GHz. This represents a 1.8:1 improvement in clock rate when compared to the wired AND/OR based implementation of the carry logic circuit of the 2-bit adder. The simulated output waveform is shown in Fig. 3.27.
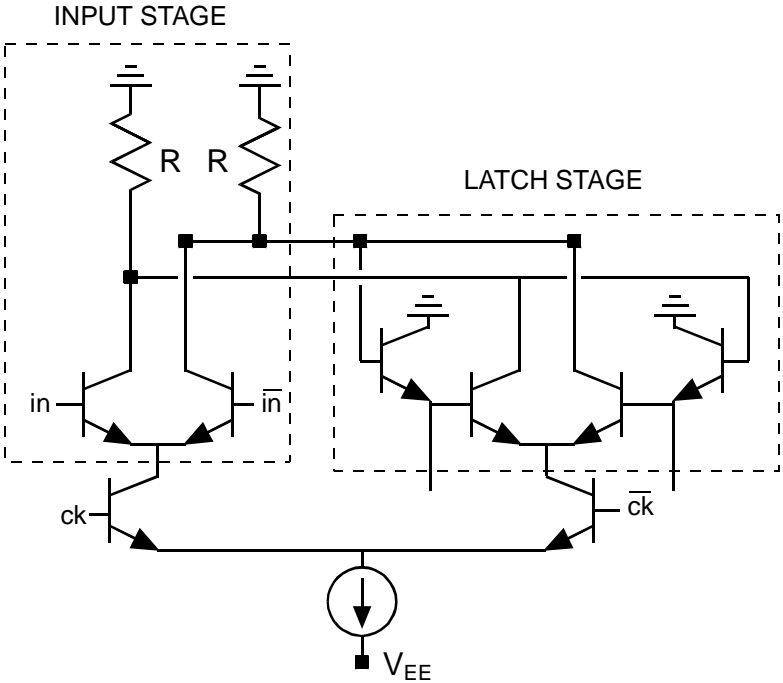
Fig. 3.24: *Circuit diagram of the ECL latch showing the input stage and the latching stage.*
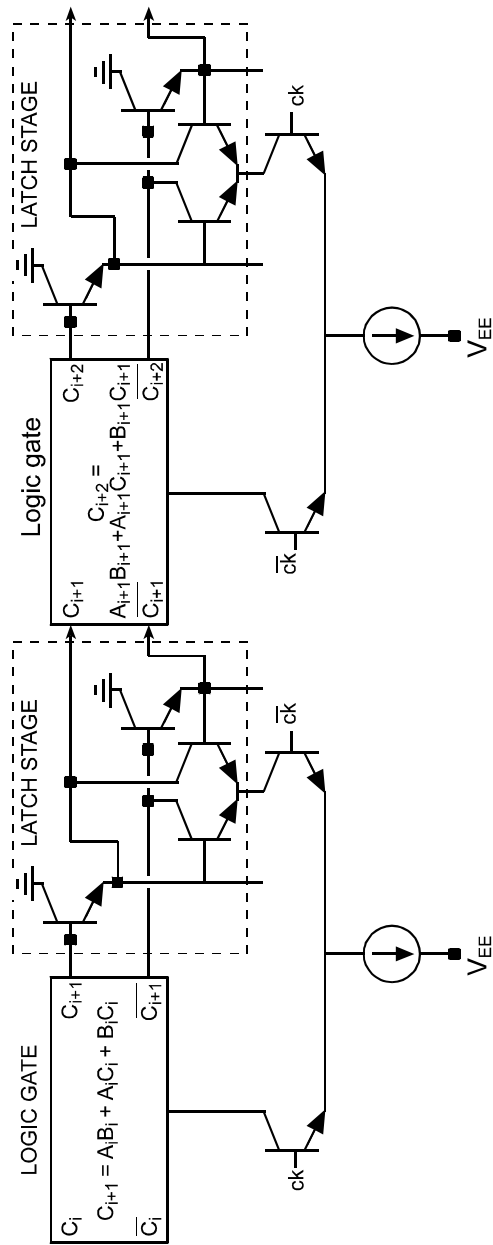
Fig. 3.25: *Merging the AND-OR logic gate (Fig.3.21) with the ECL latch in the carry logic circuit of the 2-bit adder.*
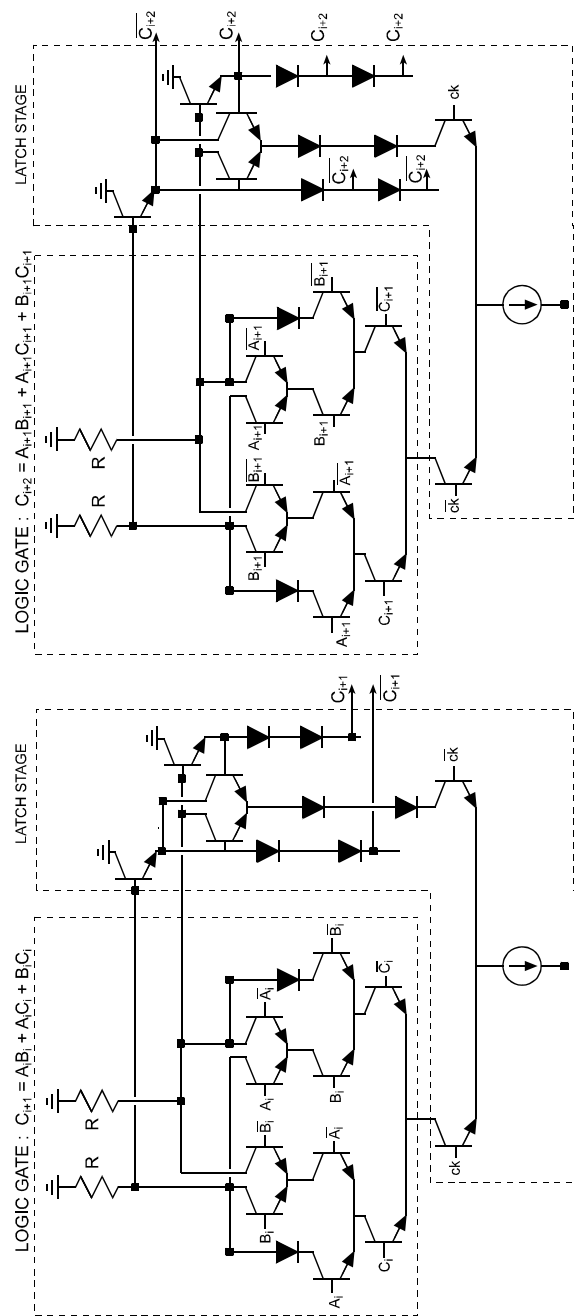
Fig. 3.26: *Circuit diagram of the carry logic circuit of a 2-bit adder using the merged AND-OR-Latch approach.*

Similar performance improvement can be achieved in the case of the sum logic circuit also by merging the XOR gate with the latching operation as shown in Fig. 3.28. An ECL latch is needed to provide a half clock cycle delay for the sum output. This ensures that when the sum is fed back as one of the inputs (for accumulator operation), it arrives at the correct clock phase.
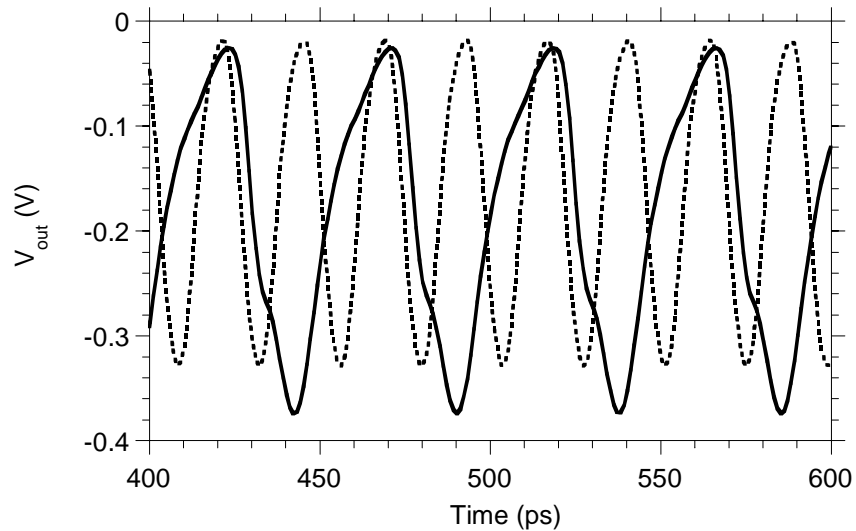
Fig. 3.27: *Simulated output waveform at 42 GHz for the 2-bit carry logic circuit when configured as a frequency divider.*

3.10   *Final 2-bit adder accumulator design*

The final 2-bit adder block diagram is shown in Fig. 3.29. The sum outputs S_i and S_{i+1} are fed back as one of the inputs (B_i and B_{i+1}). Note that the intermediate carry C_{i+1}, stays latched during $\overline{ck}$ and hence the second sum bit S_{i+1} is evaluated

during $\overline{ck}$. As mentioned earlier, an ECL latch is needed at the output of the merged XOR-Latch circuit to provide for an additional half clock cycle delay to the sum output. This ensures that the fed back sum outputs arrive at the same clock instant as the rest of the adder inputs.

A timing diagram of the 2-bit adder is shown in Fig. 3.30. Note that the output of the 2-bit adder, namely the sum bit S_i and carry out bit C_{i+2} are available after the falling edge of the clock. But the second sum output S_{i+1} of the 2-bit adder is available at the ECL latch output during the rising edge of the clock. To make sure that all the outputs of the 2-bit adder are available at the same instant in time, the S_{i+1} output to the next stage is taken at the output of the merged XOR-Latch gate. The ECL latch is needed at the output of the merged XOR-Latch gate to provide the half clock cycle delay needed for S_{i+1} to arrive at the adder input at the correct clock phase for accumulator operation (Fig. 3. 29).

3.11   *Choice of transistor geometry and circuit parameters*

The transistor geometry used in this circuit layout was slightly different from the earlier design. In the earlier design an emitter to collector alignment tolerance of 1.2 µm was used primarily to account for the wafer shrinkage (0.3 µm/mm) which occurs during substrate transfer. This significantly affects the circuit speed as a larger width results in larger base-collector capacitance (C_{cb}). The amount of wafer shrinkage did not vary much from process to process. In this design, wafer shrinkage was accounted for on the collector mask by shrinking the cell size at the
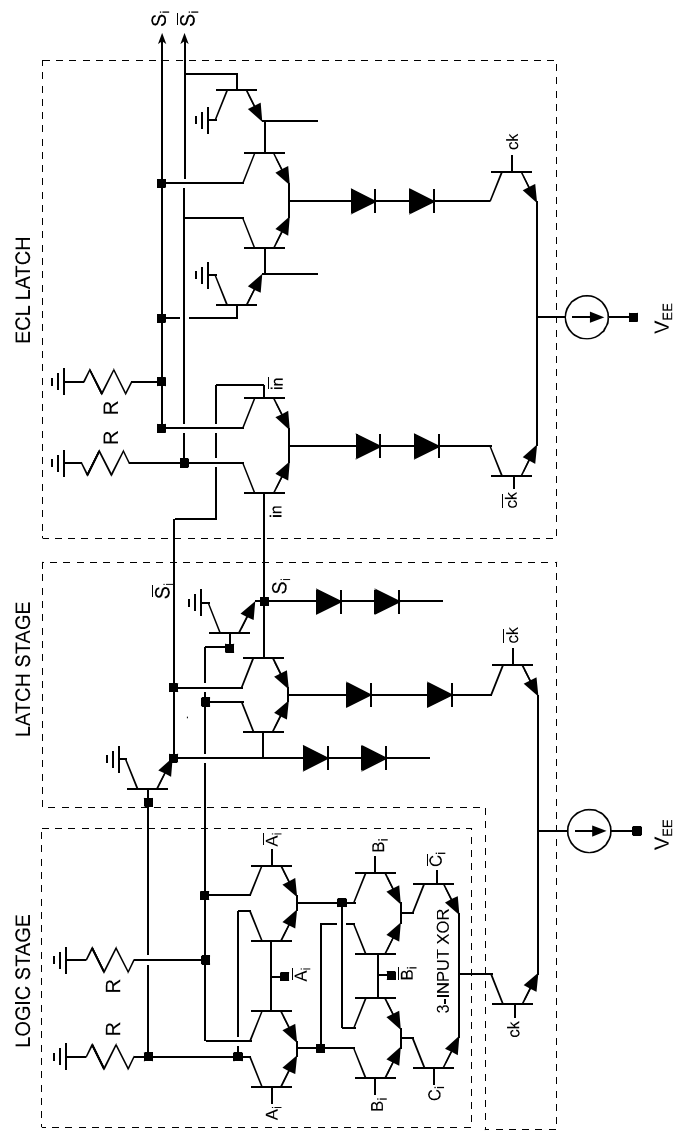
Fig. 3.28: *Circuit diagram of the sum logic circuit by merging the XOR logic gate with the MS flip-flop.*
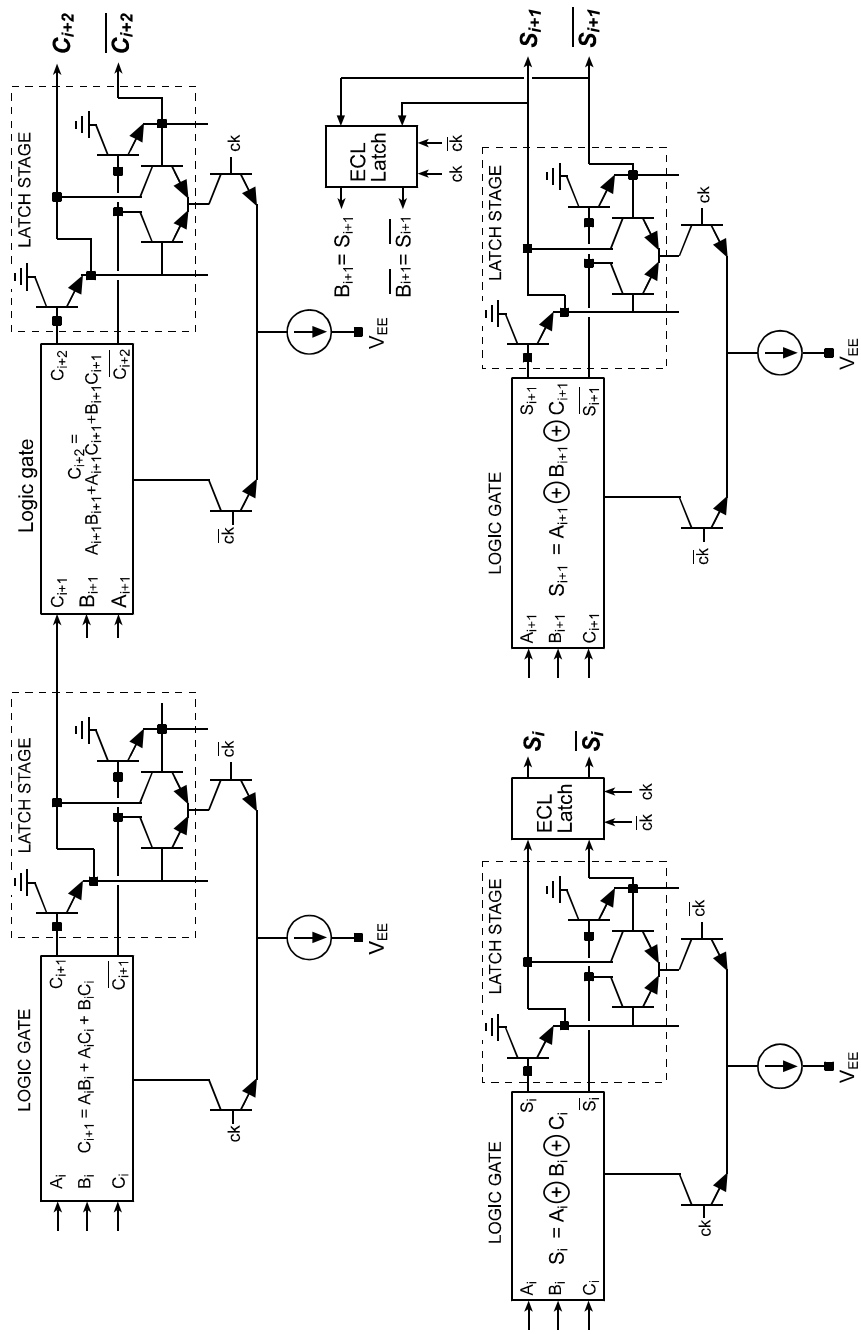
Fig. 3.29: *Block diagram of the final 2-bit adder design.*
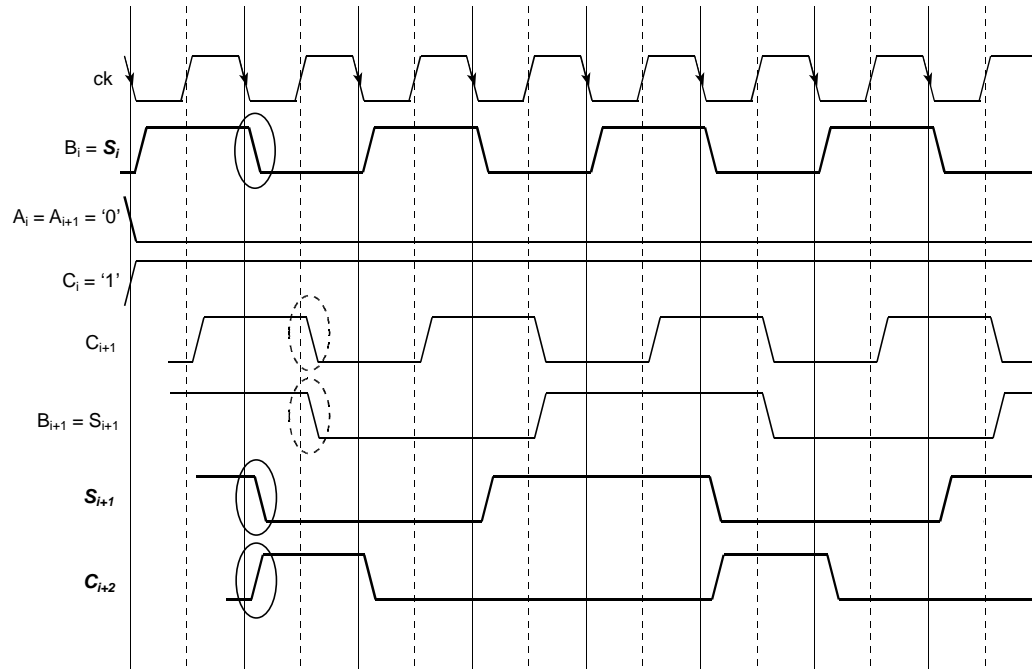
Fig. 3.30: *Timing diagram of the 2-bit adder circuit.*

collector level by the same rate. This allowed the use of significantly lower emitter to collector alignment tolerance of 0.5 μm in this design. This resulted in a lower base-collector capacitance when compared to the device layout used earlier (Fig. 3.11) The epitaxial layer structure used to fabricate the circuits is shown in Fig. 3.31. The significant difference from the earlier layer structure is the use of a 2000 Å n^- collector as opposed to a 3000 Å n^- collector.

Also a less aggressive emitter width of 1.0 μm was used for the transistors for better uniformity across the wafer and reproducibility from one process run to another. Gate to gate interconnect was run as terminated 100 Ω transmission line, instead of 120 Ohms used previously. The pull-up resistor (R) of the logic gate is used for terminating the gate-to-gate interconnects. The voltage swing (ΔV) used was 300 mV as before and the transistors were designed to operate at the maximum emitter current density (J_e) of 1mA/μm^2. This results in a emitter geometry of 3.0 x 1.0 μm^2 (corresponds to ΔV = 300 mV = A_e J_e R) for the switching transistors. The base width was still maintained at 4.0 μm. No other significant changes were made in the device design. The transistors used in the emitter follower and level shifting diodes used twice the switching transistor area (6.0 x 1.0 μm^2), except for the emitter follower used for level shifting and driving the lower-most clock input. These emitter followers are realized using transistors with four times the switching transistor area (12.0 x 1.0 μm^2) so as to reduce the charging path impedance caused by the three series connected diodes used for level shifting.

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3.12   Measurements and results: second-generation 2-bit adder

These new designs were fabricated on epitaxial layers shown in Fig. 3.31. The device results are presented initially to get an estimate of the device performance before presenting the circuit results. The common emitter DC I_c - V_{ce} curves and the Gummel plot of the transistor is shown in Fig. 3.32 and Fig. 3.33 respectively. The DC current gain (β) was low on these wafers ranging from 5 to 10 across the wafer.

The Gummel plots show collector and base current ideality factors of 1.0 and 1.2 respectively. The low current gains were due to growth problems associated with the epitaxial growth of the base. The exact nature of the problem is not clear, but it resulted from an incorrect attempt at band gap grading of the base. The effect of this is also found on the RF measurements carried out on the devices. The RF measurements indicate a current gain cut off frequency f_t of 120 GHz and power gain cut off frequency f_{max} of 160 GHz (Fig. 3.34). This is much lower than the peak measured value of f_t and f_{max} of 180 GHz and 300 GHz respectively on devices fabricated in similar epitaxial layer structures with the correct base band gap grading.

The device parameters extracted from S-parameters and other measurements are shown in the hybrid-pi equivalent circuit shown in Fig. 3.35. The forward transit time of the device is 0.82 ps and is much higher than typical measured values on other similar wafers (0.5 ps). Base contact TLM measurements on this process run

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were inconclusive since the measured resistance values did not follow the expected trend. Measurements carried out on the same wafer at IQE yielded a base sheet resistivity of 720 Ω/Y.

The low current gain β does affect the biasing of the pull down current sources. This is shown in Fig. 3. 36. The low value of current gain β results in a large base current I_b in each of the current source transistors. The reference voltage V_{ref} generated by the current mirror drives six of these current sources. Hence the base current of all these current sources add up and lead to significant reduction in the current flowing through the current mirror transistor. This causes the bias current value of the current sources to be significantly lower than the designed value. The bias current can be slightly increased by increasing the value of the negative voltage source (V_{EE}). Also the low current gain β increases the loading effect of the emitter followers on the output collector nodes of the logic gates leading to lower clock rates.

The circuit measurement results are discussed now. The 2-bit carry logic circuit was fabricated (Fig. 3.37) and tested. It clocked up to a maximum clock rate of 19 GHz. The measured output waveform at 19 GHz is shown in Fig. 3.38. This circuit had approximately 200 HBTs and dissipated approximately 1.5 W. The fabricated sum logic circuit is shown in Fig. 3.39 and clocks up to a maximum clock rate of 24 GHz. The measured output waveform is shown in Fig. 3. 40. The sum logic circuit had approximately 150 HBTs and dissipated 1.2 W.

1000 Å n+ InGaAs : 10^{19} cm^{-3} Si
199.2 Å n+ InGaAs/InAlAs Grade : 10^{19} cm^{-3} Si
700 Å n+ InAlAs : 10^{19} cm^{-3} Si
500 Å n+ InAlAs: 8.0×10^{17} cm^{-3} Si
299.7 Å InAlAs/ InGaAs Grade
400 Å p+InGaAs: 52 meV Band gap Grade : 4.0×10^{19} cm^{-3} Be
2000 Å n InGaAs : 1.0×10^{16} cm^{-3} Si
750 Å n+ InGaAs : 1.0×10^{19} cm^{-3} Si
2500 Å InAlAs $^{-3}$ undoped InAlAs Buffer layer

Emitter

Base
—

Collector
—

Fig. 3.31: *Epitaxial layer structure used in this work.*
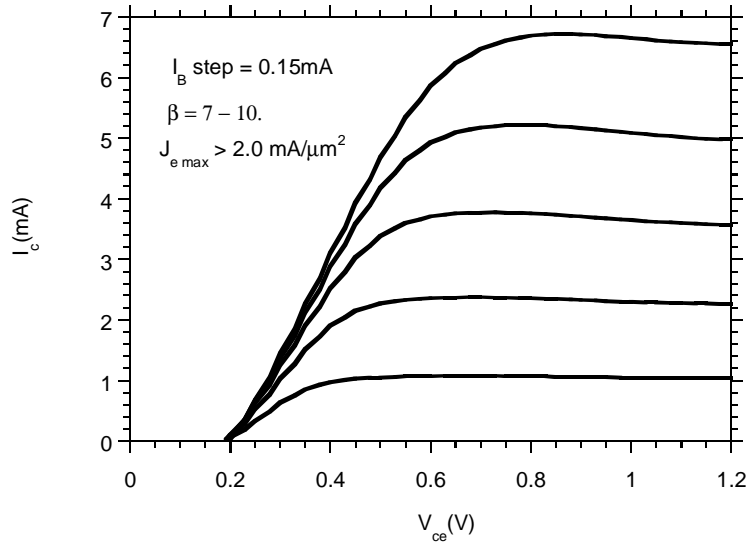
Fig. 3.32: *Common emitter DC I-V curves for a 3.0 x 1.0 μm^2 emitter and 5.0 x 2.0 μm^2 collector device. The current gain β is between 5 to 10 across the wafer.*
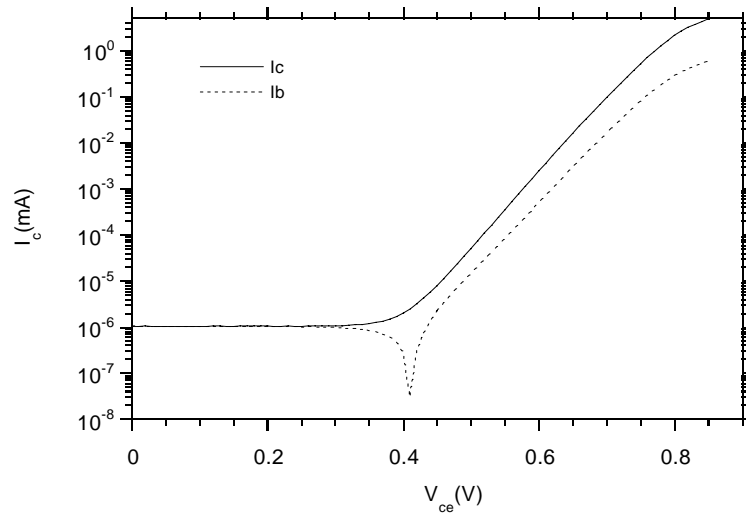
Fig. 3.33: *Gummel plot of a 3.0 x 1.0 μm^2 emitter and 5.0 x 2.0 μm^2 collector device.*
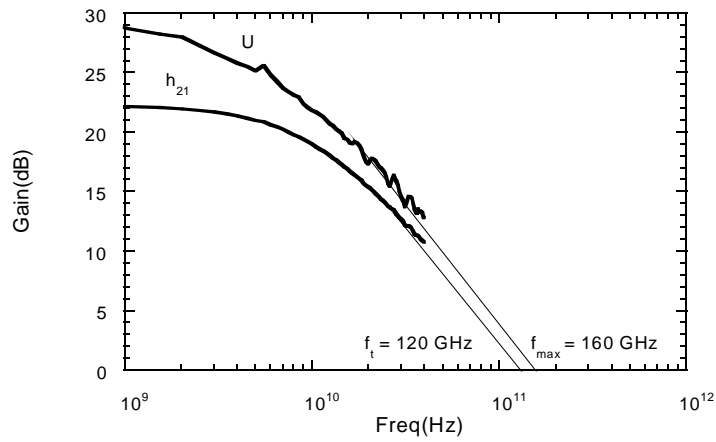
Fig. 3.34: *RF measurements of a 3.0 x 1.0 μm^2 emitter and 5.0 x 2.0 μm^2 collector device biased at $V_{ce} = 1.0$ V and $I_c = 3$ mA.*
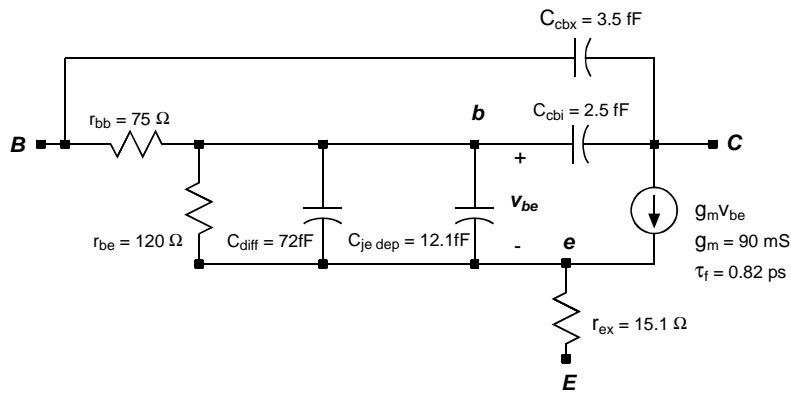
Fig. 3.35: *Hybrid-pi equivalent circuit of the device. The device had emitter dimension 3.0 x 1.0 μm^2 and collector dimension of 5.0 x 2.0 μm^2 and was biased at a V_{ce} of 1.0V and I_c of 3.0mA.*

For measuring the maximum clock rate, the carry (Fig. 3.26) and sum logic (Fig. 3.28) circuits were configured as frequency dividers as discussed earlier (sec. 3.4). The measured clock rates are significantly lower than the simulated maximum clock rates. This is partly due to the large forward transit time τ_f of the device resulting from the incorrect base epitaxial growth. Also the effects of interconnect lines and cross over capacitance have not been considered in the simulation results presented earlier. Interconnect lines and metal cross over capacitance will lead to lower clock rate of operation.

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Current mirror biasing network

LOGIC GATE

$I = I_{cs} + I_{b1} + I_{b2} + \text{-----}$
where $I_{b1} = I_{c1}/\beta$

$I_{b1} + I_{b2} + \text{-----}$

I_{cs}

$A_e = 6 \ \mu m^2$ $A_e = 3.0 \ \mu m^2$

$I_{c1} \sim I_{cs} /2$ $I_{c2} \sim I_{cs}$

150Ω

50Ω 100Ω 50Ω 50Ω

$V_{EE} = -5.0V$
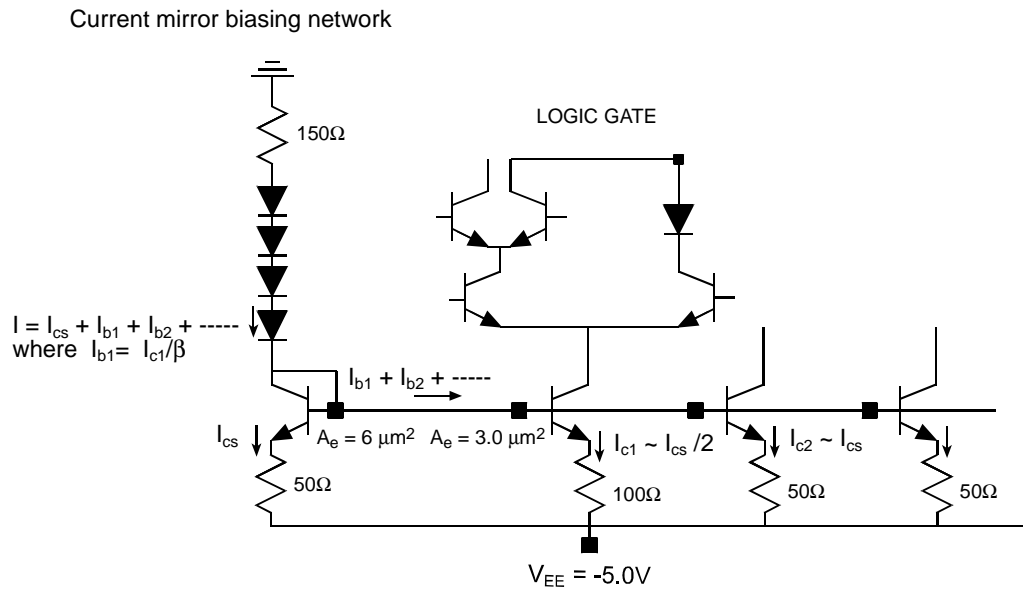
Fig. 3:36: *Effect of low current gain β on the current source biasing circuitry. The low β results in a significant base current component that reduces the value of I_{cs} from its designed value.*

The attempt to fabricate the complete 2-bit adder circuit (600 HBTs) shown in Fig. 3.29 did not succeed due to lower than required transistor yield on these and subsequent process runs. A chip photograph of the fabricated (non-functional) 2-bit adder is shown in Fig. 3.41. There are a number of possible failure mechanisms that limit the yield in transferred-substrate HBT process. These are discussed in the later chapters. Significant modifications are required in the process to achieve 600 HBT integration levels.
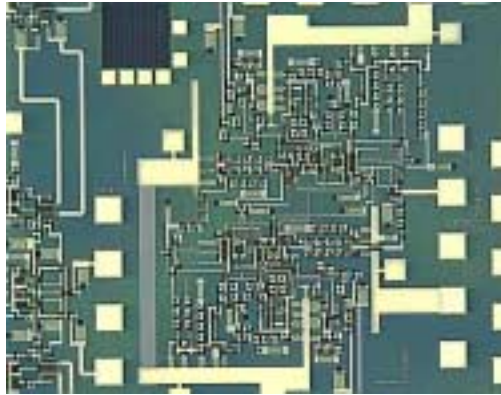
Fig. 3.37: *Chip photograph of the fabricated 2-bit carry logic circuit (200 HBTs).*
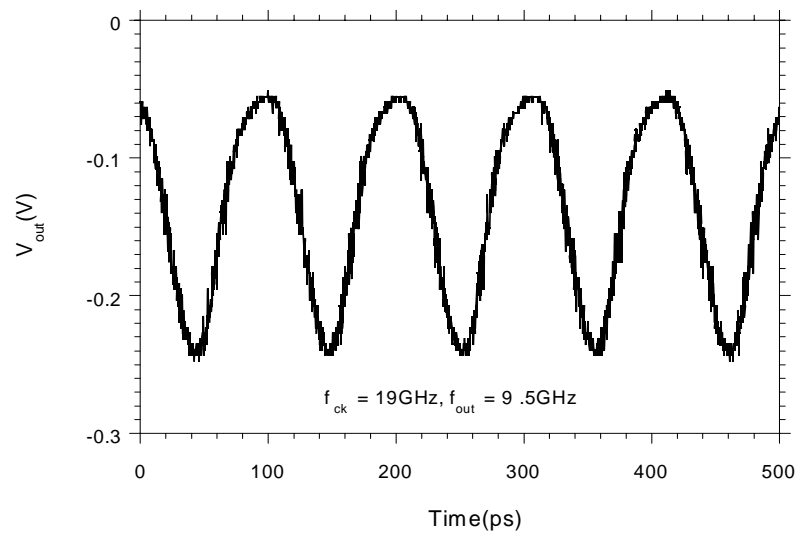
Fig. 3.38: *Measured output waveform of the 2-bit carry logic circuit for 19 GHz clock input. The output waveform is at 9.5 GHz.*
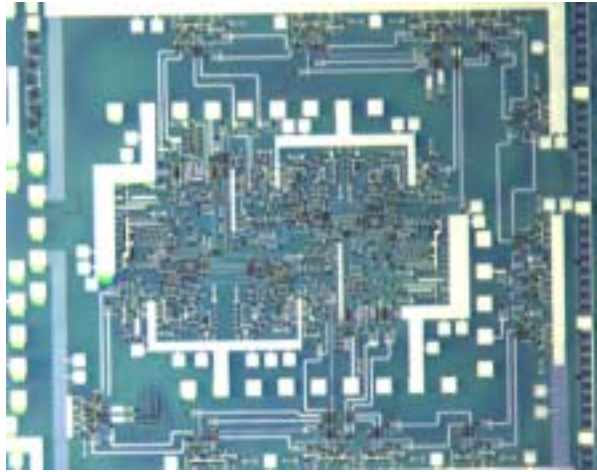
Fig. 3.39: *Chip photograph of the fabricated sum logic circuit (150 HBTs).*
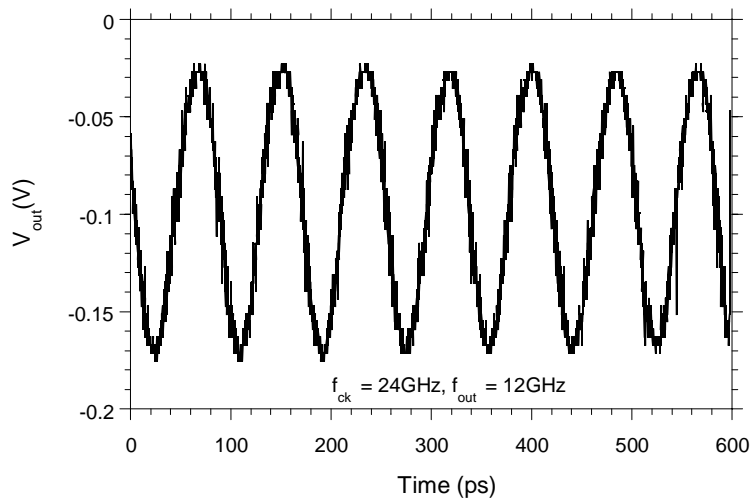
Fig. 3.40: *Measured output waveform of the sum logic circuit for 24 GHz clock input. The output waveform is at 12 GHz.*
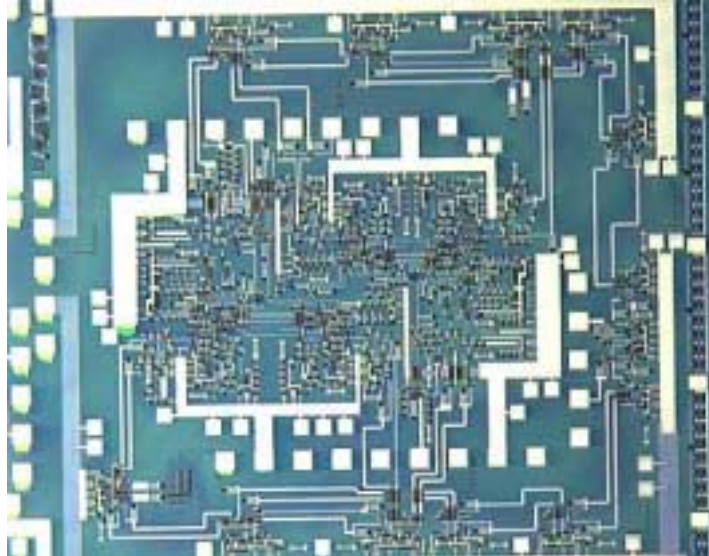
Fig. 3.41: *Chip photograph of a fabricated (non-functional) 2-bit adder circuit.*

Chapter 4

Static frequency divider

Master slave (MS) flip-flops are widely used in digital circuits for data synchronization. The emitter coupled logic (ECL) implementation of MS flip-flops consists of two series connected ECL latches clocked out of phase. An easy approach to test the maximum operating frequency of an MS flip-flop is to configure them as static frequency dividers. Frequency divider operation can be achieved by feeding back the inverted output as the input. Moreover, as discussed in the introductory chapter, the maximum operating frequency of the static frequency divider is used to compare the logic speeds of different semiconductor technologies. This effort was a continuation of the earlier efforts [25,26] to achieve logic speed of 100 GHz. A brief background of the earlier work on static frequency dividers in this technology is presented below.

In 1997 R. Pullela demonstrated the first static frequency divider [25] operating up to 48 GHz clock rate in transferred-substrate HBT technology. This was realized using CML (current-mode logic) latches. Further work by Q. Lee led to an ECL implementation of static frequency divider circuit clocking up to 66 GHz [26]. The maximum simulated clock rate in this case was 95 GHz. The difference

between the simulated and measured performance was attributed to losses at high frequencies in the cables and bias tees leading to insufficient clock power at the clock input to the divider. The static frequency divider circuit described here uses the same device footprint and circuit layout approach used by Q. Lee [26]. Significant changes in the layout were done by S. Jagannathan, which resulted in reduced layout parasitics. These are discussed further in this chapter. The large signal HBT model used for simulations in this chapter is shown in Appendix E.

4.1 Static frequency divider: (Method of time constant analysis)

The maximum operating speed of an MS flip-flop depends on a number of parameters including device capacitance (C_{be} and C_{cb}), base resistance (r_{bb}), extrinsic emitter resistance (r_{ex}) and the current density (J_e) of operation. Maximizing the clock rate of operation of a logic circuit requires optimization of the propagation delays associated with the logic gates. This requires knowledge of the relative contribution of the different device/circuit parameters to the propagation delay of the logic circuit. Method of time constant analysis (MOTC) can be used as an analytic tool to investigate the relative contributions of the various device parameters to the total propagation delay of logic gates [31, 32, 33].

Shown in Fig. 4.1 is the circuit diagram of an ECL latch used in the static frequency divider circuit. MOTC analysis requires that the transistors be replaced by their linearized equivalent circuit models. The hybrid-pi equivalent circuit used for HBTs in this work is shown in Fig. 4.2. Depending on the voltage swings seen

across the transistor, either the large-signal or small-signal device parameters are used. The transistors Q_1, Q_2, Q_3, Q_4 and Q_7 are switching transistors and see large-signal voltage swings. Hence their device parameters are evaluated as large-signal parameters. The transistors Q_5, Q_6, Q_8, Q_9, Q_{10} and Q_{11} are emitter followers and see small-signal base-emitter voltage swings. Hence their transconductances and base-emitter capacitances are evaluated as small-signal parameters.

In the latch shown in Fig. 4.1 the propagation delay is calculated as the difference in time for the emitter node of Q_6 to change after the clock changes at the base of Q_1. The relevant capacitors in the signal propagation path that need to be charged are shown external to the transistors. The method of time constant technique requires that the open circuit resistance seen across the terminals of each capacitance be evaluated by removing all the capacitors from the circuit [32]. The total propagation delay is related to the sum of the RC time constants associated with all the capacitors in the signal propagation path. Detailed MOTC calculations are shown in Appendix C.

The resulting RC time constants can be simplified considerably by assuming that all the switching transistors have the same geometry and equal base-emitter and base-collector capacitance. Also, all the emitter follower transistors are assumed to have the same device geometry. In that case, the propagation delay expression can be simplified as shown below. The emitter follower parameters are represented

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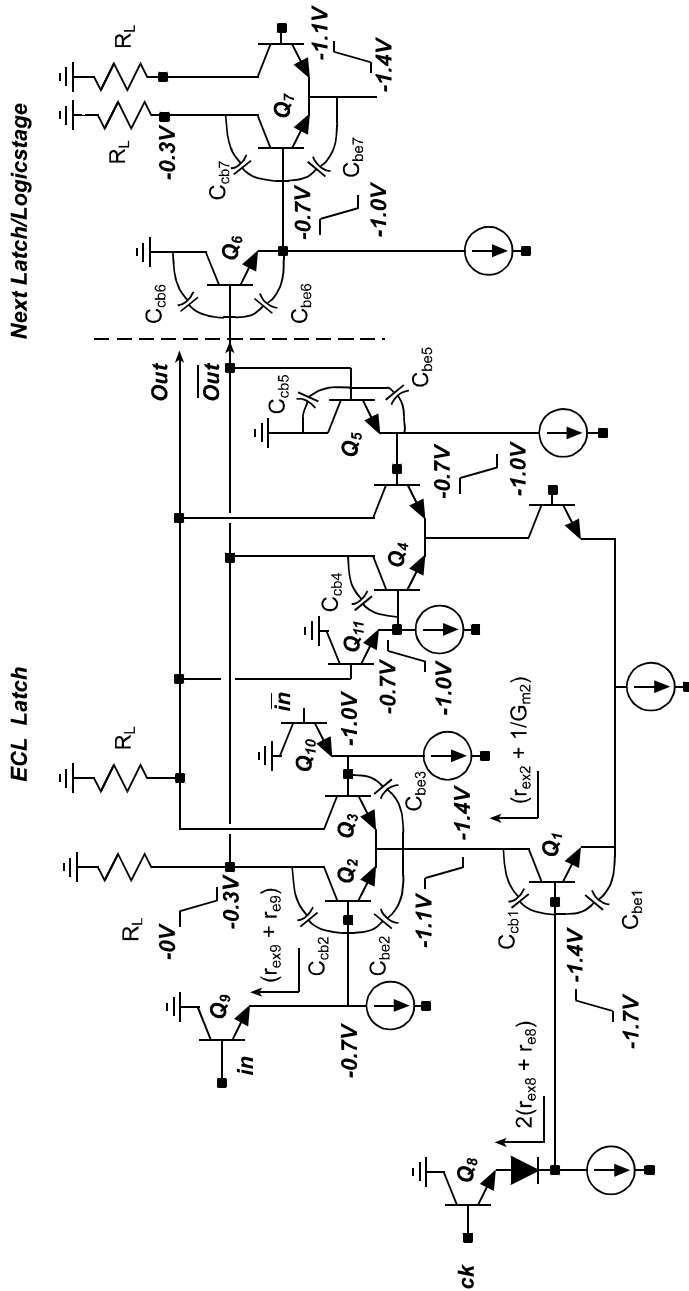
Fig. 4.1: *Circuit diagram of an ECL latch showing the relevant capacitances in the signal propagation path. The base emitter and base-collector capacitances contributing to the signal propagation delay are shown external to the transistor.*

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by subscripts 'EF'. If the subscripts 'EF'' are not present then the parameters correspond to the switching transistors. The maximum clock frequency of the static frequency divider is given by,

$$f_{ck\,max} = \frac{1}{2T_{pd}(ECL\ latch)}$$

(4.1)

Where $T_{pd}\ (ECL\ latch)$ is given by,

$$T_{pd}(latch) = 0.7 * \begin{Bmatrix} (r_{bb} + 2r_{exEF} + 2r_{eEF} + r_{ex} + 2R_L) * C_{diff} \\ + (2r_{bb} + 3r_{exEF} + 3r_{eEF} + 3r_{ex} + 3R_L) * C_{je\,depl} \\ + (7r_{exEF} + 7r_{eEF} + 4R_L + r_{ex}) * C_{cbx} \\ + (7r_{exEF} + 7r_{eEF} + 5r_{bb} + 4R_L + r_{ex}) * C_{cbi} \\ + 2r_{eEF} * C_{beEF} + 2R_L * C_{cbxEF} + 2(r_{bbEF} + R_L) * C_{cbiEF} \end{Bmatrix}$$

(4.2)

The resulting propagation delay of the ECL latch is about 7.21 ps. The details of the calculations and device parameters values used are shown in Appendix C. This results in a maximum clock rate of 69 GHz. Circuit simulations indicate a maximum clocking rate of 90 GHz.

The factor of 2 in Eq. 4.1 accounts for the delay through the two ECL latches in the MS flip-flop. The propagation delay expression (Eq. 4.2) can be rewritten in terms of the transistor area (A_e) or in terms of the current density (J_e). Extensive analysis and simulations have been done to evaluate both the optimum current density of operation and the optimum area ratio of the emitter follower transistor to the switching transistor (A_{eEF}/A_e) [29,31]. The optimum current density (J_e) of operation was found to be 3.0 mA/μm^2 [29]. Kirk effect limits the maximum current

density of operation to less than 2 mA/μm^2. The optimum transistor area ratio (A_{eEF}/A_e) was found to be close to 2. But in the frequency divider design presented in this chapter (and earlier divider designs [26]) the area ratio used was 1.0 for generating a compact and symmetrical layout.
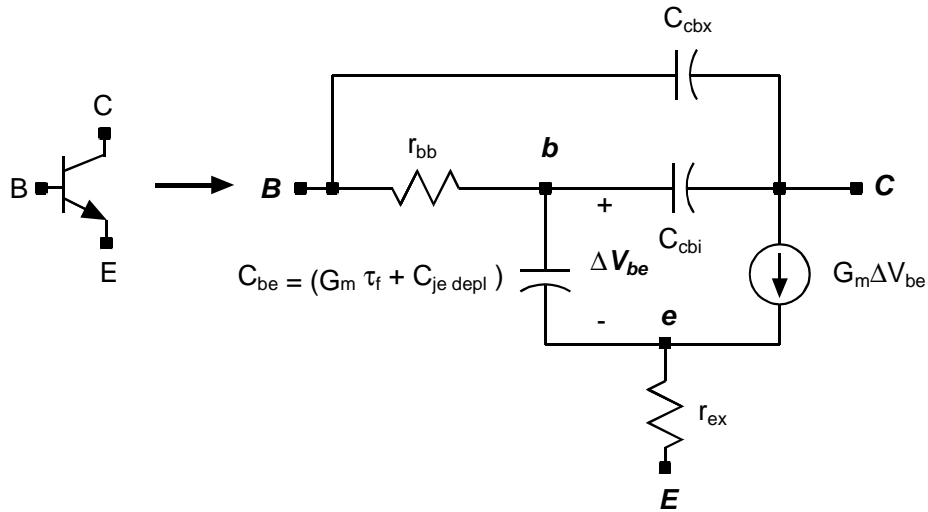
Fig. 4.2: *Hybrid-pi equivalent circuit used to represent the HBTs.*

4.2   *Static frequency divider: circuit design*

The static frequency divider circuit used in this work retains most of the design features in the previous divider design [26] done by Q. Lee in transferred-substrate HBTs. This includes using the same device geometry (mask dimensions are emitter: 12 x 0.7 μm^2, collector: 14 x 1.5 μm^2) and a similar circuit layout. The

circuit diagram of the frequency divider circuit is shown in Fig. 4.3. An output buffer (not shown in Fig. 4.3) with a voltage swing of 100 mV is used to bring the output off chip. The design features are listed below.

(i)   A small amount of series inductive peaking (90 pH) is employed along with the pull up resistors to increase the maximum clocking frequency. All inductors are realized using transmission lines.

(ii)   The output interconnect is run as doubly terminated transmission line with a line impedance of 90 Ω.

(iii)   Ringing in the emitter followers are damped out by the use of a series connected inductor and resistor combination. This inductor-resistor-inductor combination is connected between the emitter nodes of the emitter follower.

(iv)   The internal voltage swing at the output nodes is designed to be 300 mV (45 Ω x 7.5 mA). The voltage swing at the output of the output buffer is limited to 100 mV to reduce loading on the output nodes of the divider circuit. The effective maximum current density (accounting for 0.1 μm emitter under-cut during wet etch) of operation is close to 1 mA/μm^2.

Significant changes made to the earlier design [26] and are listed below.

(i)   Interconnect cross over capacitance was reduced by employing collector metal as another interconnect metal level. This results in a thicker (8000 Å)

and lower dielectric constant ($\varepsilon_r = 3.3$) insulator between the cross over metals when compared to the use of 4000 Å of SiN as the insulator.

(ii)   The earlier design [26] used keep-alive bias currents to weakly bias the input differential transistor pair of the latch from completely turning off. This is absent in this design.

(iii)   Also layout modifications were done to access the clock input pad with a single signal GSG probe. This allows the use of GSG probes having a waveguide input connector rather than a co-axial input connector. This is necessary to reduce cable/probe losses at high frequencies.

(iv)   In the previous design the clock input coming off-chip directly drives the base of one of the lower differential transistor pairs. The base of the other lower differential transistor pair is biased at the DC level of the clock input (~-1.55 V). In this design the clock input coming off chip drives an emitter follower. The level shifted output of the emitter follower drives the base of the lower differential transistor pairs.

(v)   During simulations, a 600 mV peak to peak (0 dBm) sine wave input is used to drive the clock input. The DC level of the clock input is –300 mV. The inverted clock input is biased at –300 mV.

The maximum simulated clock rate of operation of the static frequency divider is 90 GHz. The simulated output waveform at 90 GHz is shown in Fig. 4.4.
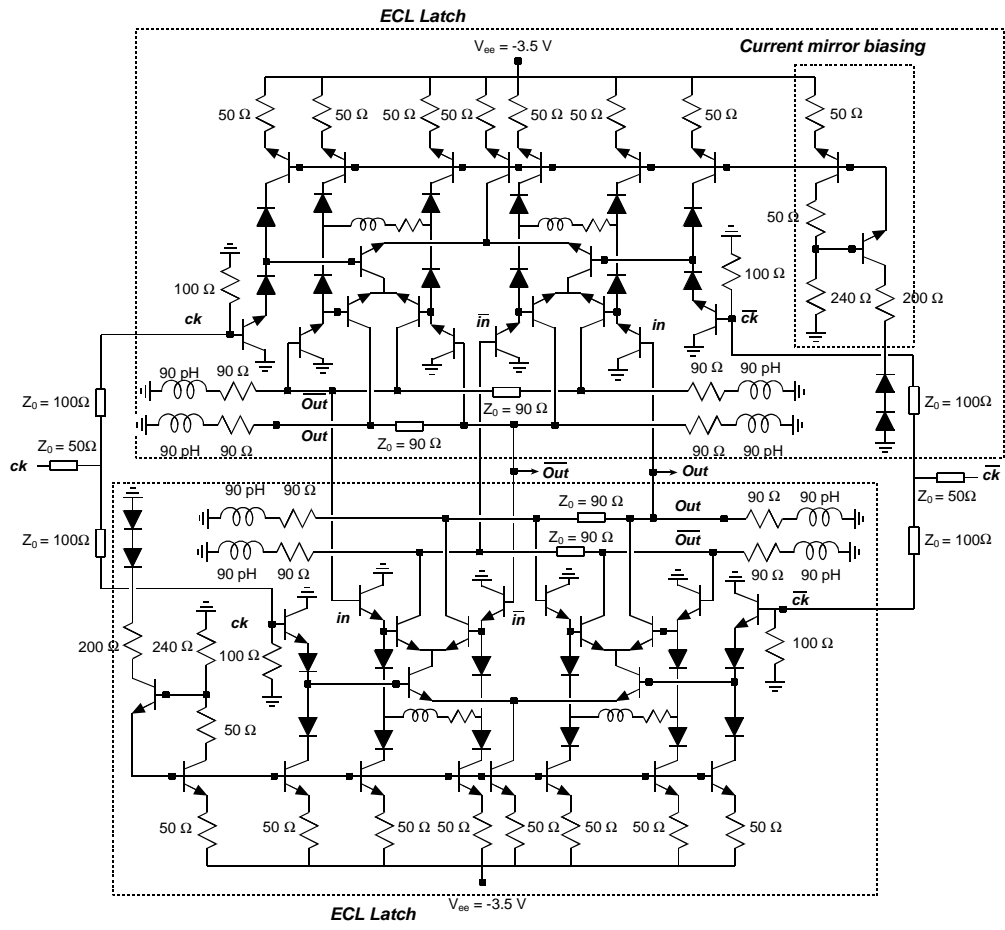
Fig. 4.3: *Circuit diagram of the static frequency divider circuit.*
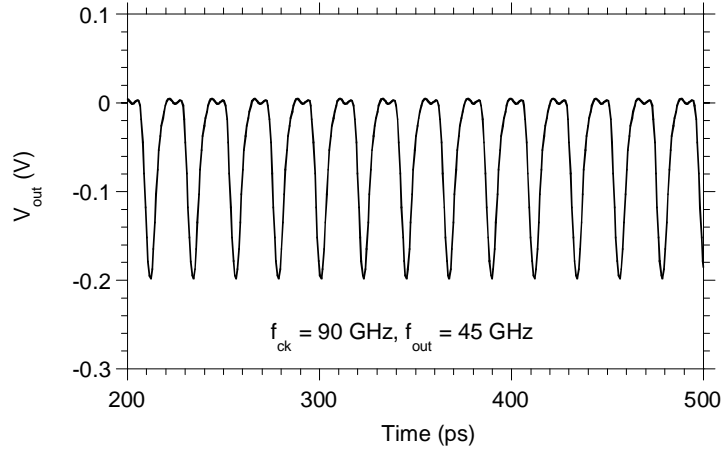
Fig. 4.4: *Simulated output waveform of the static frequency divider for 90 GHz clock input.*

4.3   Results and discussion

The epitaxial layer structure used in the fabrication of the static frequency divider circuit is shown in Fig. 4.5. The use of 2000 Å n⁻ collector (instead of the 3000 Å) allows for increased current density of operation before the onset of base-push out effect [16]. The device test structures in this mask set did not have a transistor geometry corresponding to that used in the divider. Hence the device results presented here correspond to a device with emitter dimension of 6.0 x 1.0 μm^2 and a collector dimension of 7.0 x 2.0 μm^2.

The common emitter I-V characteristic of this device is shown in Fig. 4.6 and the RF measurements is shown in Fig. 4.7. This device exhibits a f_t of 165 GHz and f_{max} of 220 GHz when biased at a V_{ce} of 1.0 V and an I_c of 6 mA. Based on this

RF data, the RF performance of the devices used in the divider (emitter: 12 x 0.7 μm^2, collector: 14 x 1.5 μm^2) can be estimated. A conservative estimate of the RF performance for these devices yields a f_t around 150 GHz and f_{max} around 250 GHz. The higher f_{max} for this device geometry is due to the reduced spreading resistance in the base and lower C_{cbi} due to the use of a narrower emitter (0.7μm as against 1.0 μm) and collector.

The chip photograph of the fabricated divider circuit is shown in Fig. 4.8. The measurement set-up used to measure the divider circuit is shown in Fig. 4.9. Bias tees with RF ports terminated in 50 Ω were used to provide the DC bias to the chip. Also a bias tee is used at the input of the clock probe to enable RF as well as a DC input to the clock pad. The inverted clock input is provided a fixed DC bias level. These are shown in Fig. 4.9.

1000 Å n^+ InGaAs : 10^{19} cm^{-3} Si	
199.2 Å n^+ InGaAs/InAlAs Grade : 10^{19} cm^{-3} Si	
700 Å n^+ InAlAs : 10^{19} cm^{-3} Si	Emitter
500 Å n^+ InAlAs: 8.0×10^{17} cm^{-3} Si	
299.7 Å InAlAs/ InGaAs Grade	
400 Å p^+InGaAs: 52 meV Band gap Grade : 4.0×10^{19} cm^{-3} Be	Base
400 Å n InGaAs : 1.0×10^{16} cm^{-3} Si	
50 Å n InGaAs : 1.0×10^{17} cm^{-3} Si	Collector
1550 Å n InGaAs : 1.0×10^{16} cm^{-3} Si	
2500 Å InAlAs $^{-3}$ UID InAlAs Buffer layer	

Fig. 4.5: *Epitaxial layer structure used to fabricate the static frequency divider.*
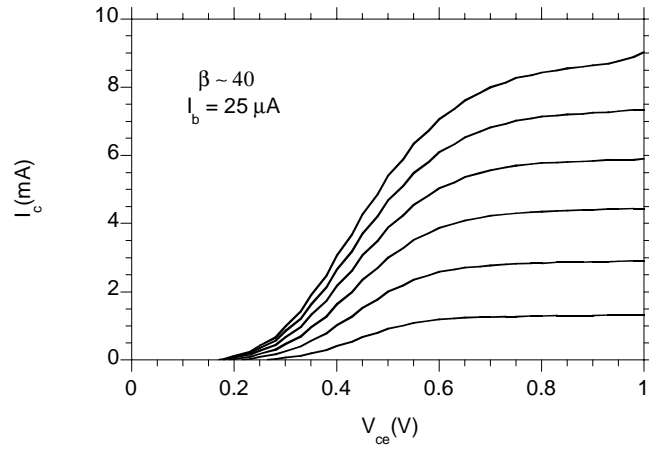
Fig. 4.6: *Common emitter I – V curves for a transistor with emitter dimension of 6.0 x 1.0 μm^2, and collector geometry of 7.0 x 2.0 μm^2.*
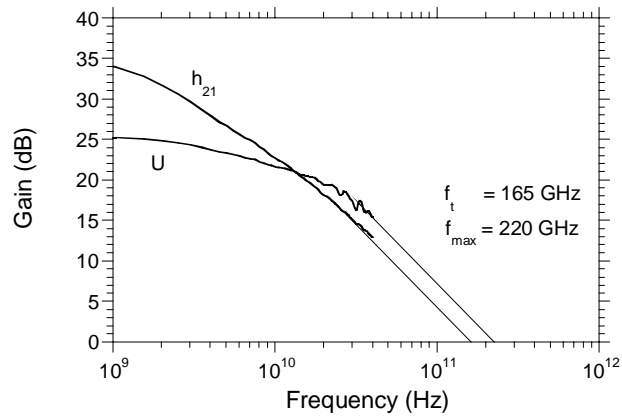
Fig. 4.7: *RF measurements of a transistor biased at a V_{ce} of 1.0 V and I_c of 6 mA (emitter dimension of 6.0 x 1.0 μm^2, and collector dimension of 7.0 x 2.0 μm^2).*
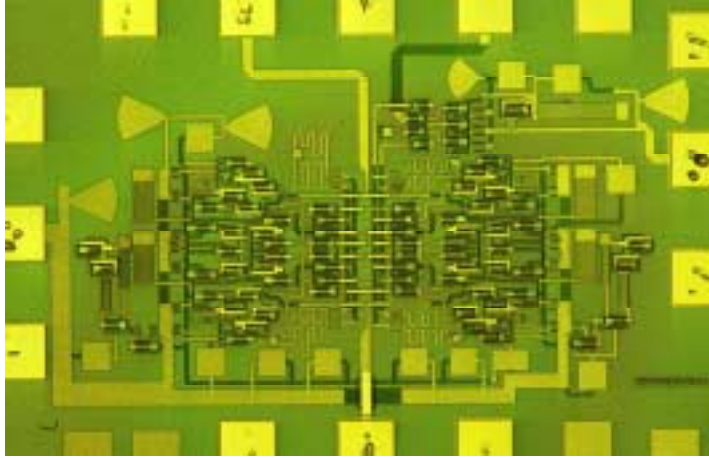
Fig. 4.8: *Chip photograph of the fabricated static frequency divider circuit.*

The measurements were carried out in three frequency ranges covering 5 GHz to 75 GHz. In the 2-26 GHz frequency range, the RF generator directly drives the clock input of the divider. In the 26-40 GHz frequency range, the 2-26 GHz synthesizer output drives a frequency doubler. A frequency tripler, driven by the 2-26 GHz synthesizer is used to generate the 50-75 GHz clock input. The measured output waveform has a voltage swing of 100 mV. This is the designed voltage swing of the output buffer. The maximum available power at the input to the clock pad for the different frequency bands are also shown in Fig. 4.9. This is the rated output power indicated in the data sheet of the synthesizers/frequency multipliers. Approximately 3 dB loss is likely to be present in the cable-bias tee-probe combination in the 50-75 GHz range.

The measured output waveform for 5 GHz and 69 GHz clock rates are shown in Fig. 4.10 and Fig. 4.11 respectively. The measured output waveform at 75

GHz clock rate shows a 6.0 GHz modulation of the output waveform (Fig. 4.12). The origin of the 6 GHz modulation was found to be from the 2-26 GHz synthesizer. The 2-26 GHz synthesizer output (at 25 GHz) shows a 6 GHz modulation (Fig. 4.13). The divider circuit dissipates about 800 mW. Approximately 80% of the total power dissipation result from the biasing currents of the emitter followers.
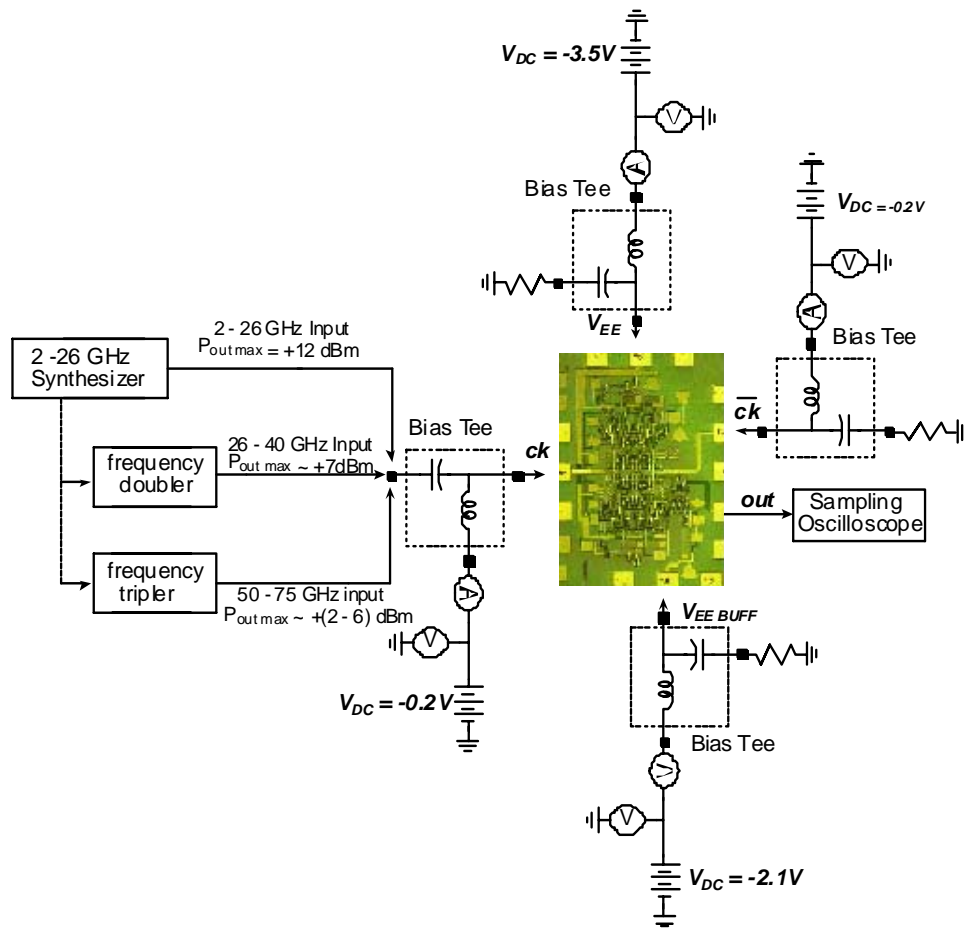
Fig. 4.9: *Measurement set-up of the static frequency divider circuit.*
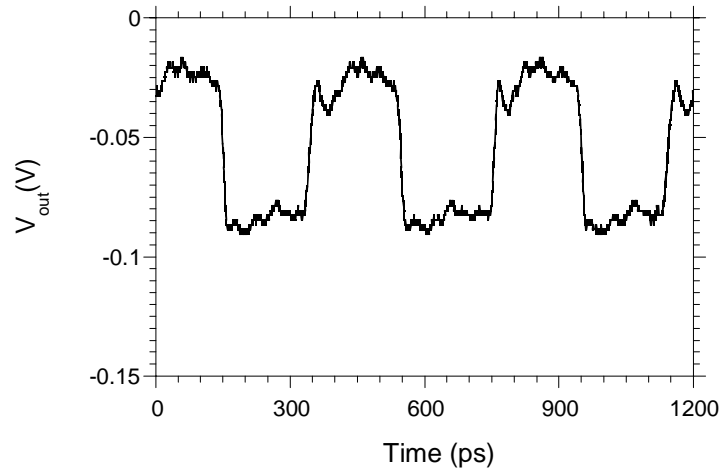
Fig. 4.10: *Measured output waveform for a 5 GHz clock input. The output waveform*

is at 2.5 GHz.
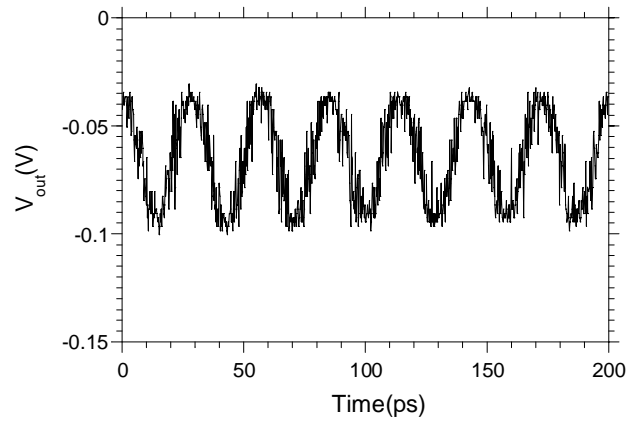
Fig. 4.11: *Measured output waveform for 69 GHz clock input. The output waveform*

is at 34.5 GHz.

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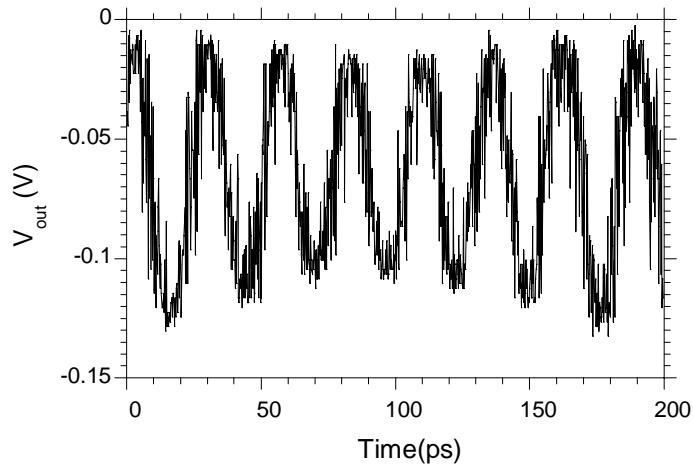
Fig. 4.12: *Measured output waveform at 37.5 GHz for a 75 GHz clock input.*
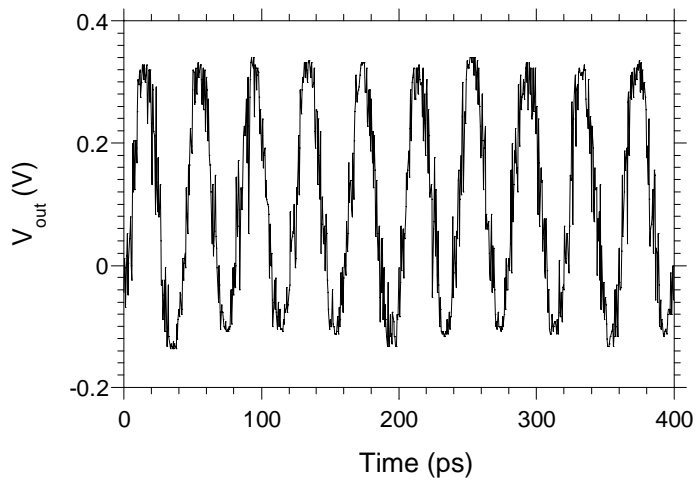
Fig. 4.13: *Measured RF output waveform of the 2-26 GHz synthesizer at 25 GHz.*

Note the presence of the 6.0 GHz modulation of the waveform.

Chapter 5

Processing issues and yield limiting mechanisms

This chapter focuses on the processing issues that limit the level of integration in transferred-substrate HBT (TSHBT) technology. Detailed process steps of TSHBT process can be found in Appendix F. The transferred-substrate HBT process steps are described in this chapter with the help of relevant device/wafer cross section at each step. The possible yield limiting mechanisms are then identified. Test structures used to identify the yield limiting mechanisms are presented. The mask layout of the test structures are shown in Appendix G. The results from the test structures are then presented to give an idea of the extent to which they affect the circuit yield.

5.1   Emitter lithography and metal deposition

The TSHBT process starts with the emitter lithography, which opens up the areas for emitter metal deposition. The deposited emitter metal combination is Ti/Pt/Au/Si. Silicon serves as the etch mask and protects the emitter metal in the subsequent emitter dry etch. The emitter photoresist profile and the resulting emitter metal profile after the lift-off are shown in Fig. 5.1 and Fig. 5.2. If the photoresist is underexposed (Fig. 5.1), the photoresist profile slopes outwards. During the emitter metal deposition, the emitter metal deposits at the same rate, both on top of the

semiconductor as well as on the edge of the photoresist. The emitter spikes result from the emitter metal, which deposits on the edge of the photoresist.

Underexposing the photoresist is preferred when compared to the lift-off profile of the photoresist (Fig. 5.2). The lift-off profile leaves a thin layer of metal on either sides of the emitter metal, which can cause base-emitter shorts in the subsequent base-emitter etch and self-aligned metal deposition. For this reason, the emitter photoresist is underexposed on purpose. The resulting emitter spikes persist through out the entire process and are of concern at the interconnect metallization step.

5.2 Base emitter etch and base metal deposition

Emitter metal deposition is followed by a series of etches to define the base-emitter junction of the device. First, a $CH_4/H_2/Ar$ based reactive ion etching is carried out to etch through the InGaAs emitter cap layer into the InAlAs emitter (Fig. 5.3). This is followed by a selective wet etch (HCl/HBr/H_2O/acetic acid) that etches the InAlAs but has a very low etch rate of InGaAs. This selective etch stops when it encounters the InGaAs in the InAlAs/InGaAs grade. Also the selective wet etch undercuts the InAlAs emitter layer making it possible to carry out a self-aligned base metal deposition. This is followed by the non-selective citric acid etch that etches through the grade into the p^+ base region. Base metal lithography is done to pattern the wafer and a self-aligned base metal deposition and lift-off is then carried

Ti/Pt/Au/Si = 200/400/8000/500 Å

Photoresist (PR)

~ 9000 Å

HBT epitaxial layer

InP Substrate

(i) After emitter lithography and metal deposition (under exposure)

Spikes in emitter metal after lift-off

Emitter metal

~ 8000 Å

HBT epitaxial layer

InP Substrate

(ii) After emitter lift-off
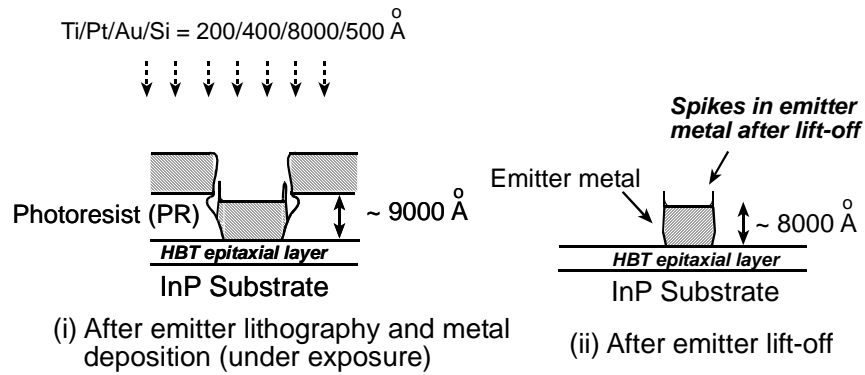
Fig. 5.1: *Cross section of the wafer during and after emitter metal deposition. Note the presence of emitter spikes. This is the result of an underexposed photoresist profile.*

Ti/Pt/Au/Si = 200/400/8000/500 Å

Photoresist (PR)

~ 9000 Å

HBT epitaxial layer

InP Substrate

(i) After emitter lithography and metal deposition (lift-off profile)

metal strands at the base of emitter metal

Emitter metal

~ 8000 Å

HBT epitaxial layer

InP Substrate

(ii) After emitter lift-off
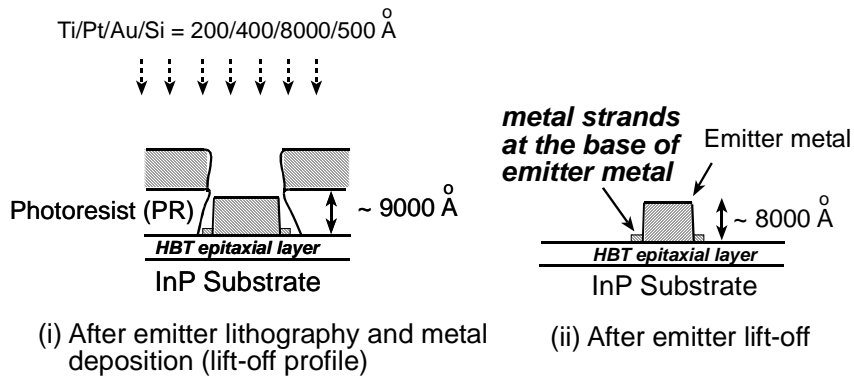
Fig. 5.2: *Cross section of the wafer during and after emitter metal deposition. Note the presence of metal strands at the base of the emitter metal due to the lift-off profile.*

out. Etch stop points of the different etches are shown in Fig. 5.3 in the epitaxial layer structure. The wet etches (both selective as well as non-selective wet etch) are both timed etches and have been reproducible from run to run. Resulting device cross sections are shown in Fig. 5.4.

The self-aligned base metal deposition relies on the combined shadowing effect of the emitter metal and the undercut in the InAlAs layer for successful base metal deposition. The extent of the InAlAs undercut is in the range of 500 Å from each side of the emitter. The possibility of a short circuited base-emitter junction exists if the InAlAs undercut is not uniform across the wafer due to some surface non uniformity from the earlier dry etch. Also the metal strands at the base of the emitter metal (Fig. 5.2) can fold down after the base-emitter etch and result in a base-emitter short during the base metal deposition. Electrical measurements do indicate the presence of occasional base-emitter shorts.

5.3 Base mesa isolation and polyimide passivation

A Cl_2 based reactive ion etching is used to etch the base mesa that isolates the active layers of each device. This etches approximately 4500 Å and stops halfway into the InAlAs buffer layer (Fig. 5.3 and Fig. 5.5). Polyimide (insulating polymer) is then spun on the wafer (~1.8 μm thickness). This is followed by a polyimide cure (Oven bake). A blanket layer of photoresist is spun on top of the polyimide, and the polyimide-photoresist combination is then subjected to an O_2 reactive ion etch to expose the emitter metal as shown in Fig. 5.6. This step also

results in the planarization of the device mesa structure. The wafer is then patterned using photoresist and a subsequent O_2 dry etch defines the polyimide mesa.

The roughness of polyimide surface is significant after the polyimide etch-back process. A SEM picture showing the extent of polyimide roughness is shown in Fig. 5.7. The roughness of the polyimide is important since any deposited metal or SiN on top of the polyimide takes on the roughness of the underlying polyimide layer. SEM pictures of metal and SiN on top of the polyimide are shown in later figures.

1000 Å n$^+$ InGaAs : 10^{19} cm^{-3} Si
199.2 Å n$^+$ InGaAs/InAlAs Grade : 10^{19} cm^{-3} Si
700 Å n$^+$ InAlAs : 10^{19} cm^{-3} Si
500 Å n$^+$ InAlAs: 8.0×10^{17} cm^{-3} Si
299.7 Å InAlAs/ InGaAs Grade
400 Å p$^+$InGaAs: 52 meV Band gap Grade : 4.0×10^{19} cm^{-3} Be
400 Å n InGaAs : 1.0×10^{16} cm^{-3} Si
50 Å n InGaAs : 1.0×10^{17} cm^{-3} Si
2550 Å n InGaAs : 1.0×10^{16} cm^{-3} Si
2500 Å InAlAs UID InAlAs Buffer layer

$CH_4/H_2/Ar$
dry etch (~ 2000Å)

$HCl/HBr/H_2O/Acetic$
acid wet etch (~ 600 Å)
Citric acid based
wet etch (~ 200 Å)

Cl_2 based dry etch
(~ 4500 Å)

Fig. 5.3: *The HBT epitaxial layer structure showing the various etch stop points*

5.4   Nickel-chromium (NiCr) thin film deposition

Resistors are realized using a thin NiCr metal film evaporated onto the wafer. Approximately 400 Å of NiCr yields about 40 Ω/Y. A thin layer (~ 30 Å) of Ti ensures good adhesion to the semiconductor. Approximately 300 Å of SiO_2 is

Ti/Pt/Au = 200/400/800 $\overset{\circ}{A}$

Base metal

PR ( ) PR

HBT epitaxial layer

InP Substrate

(i) After base metal deposition

Base emitter short

~ 1400 $\overset{\circ}{A}$

HBT epitaxial layer

InP Substrate

(ii) After base metal lift-off

emitter metal   base metal   PR: Photoresist
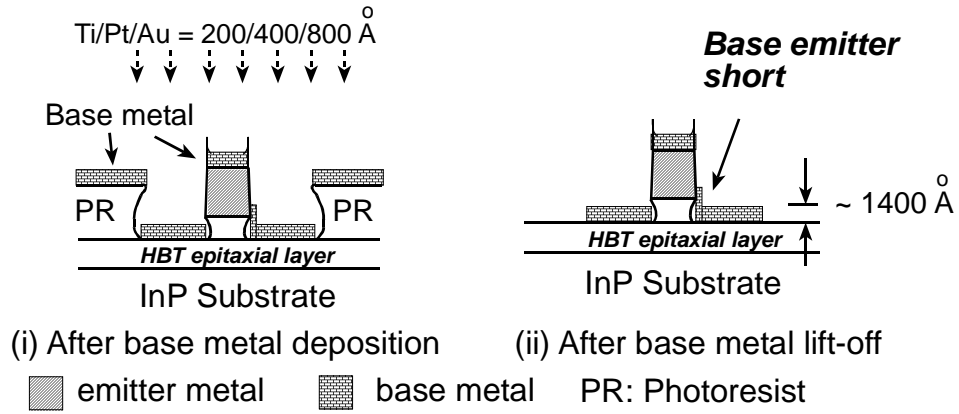
Fig. 5.4: *Self-aligned base metallization and the possibility of base-emitter shorts*

Cl$_2$ based dry etch

PR

e

HBT epitaxial layer

InP Substrate

(i) After base mesa lithography

e
b
c   ~ 4500 $\overset{\circ}{A}$

InP Substrate

(ii) After base mesa isolation etch

emitter metal   base metal   PR: Photoresist
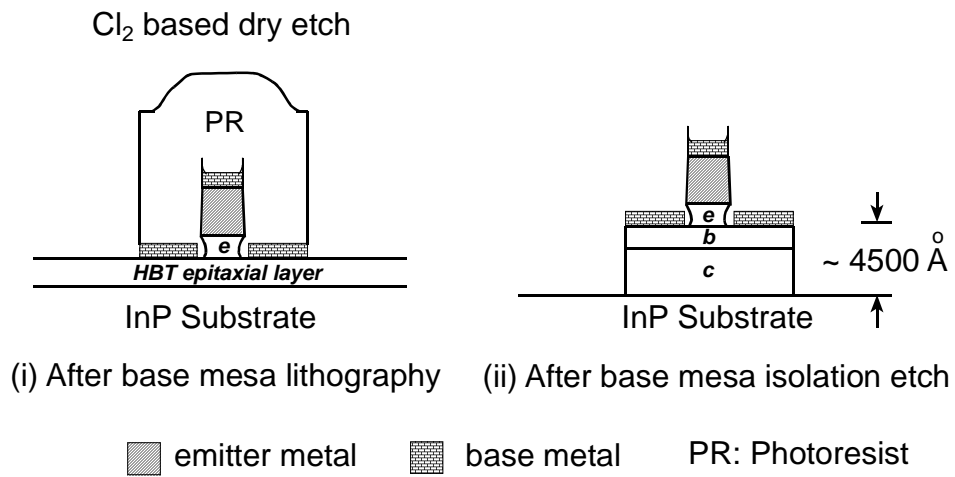
Fig. 5.5: *Cross section of the wafer after the base mesa isolation etch.*

O$_2$ dry etch to expose emitters

Photoresist

rough polyimide surface

Polyimide mesa

Polyimide

e

b

c

6000 Å

~ 1.0 µm

InP Substrate

InP Substrate

(i) Polyimide etch-back
to expose emitters

(ii) patterned polyimide mesa

emitter metal   base metal
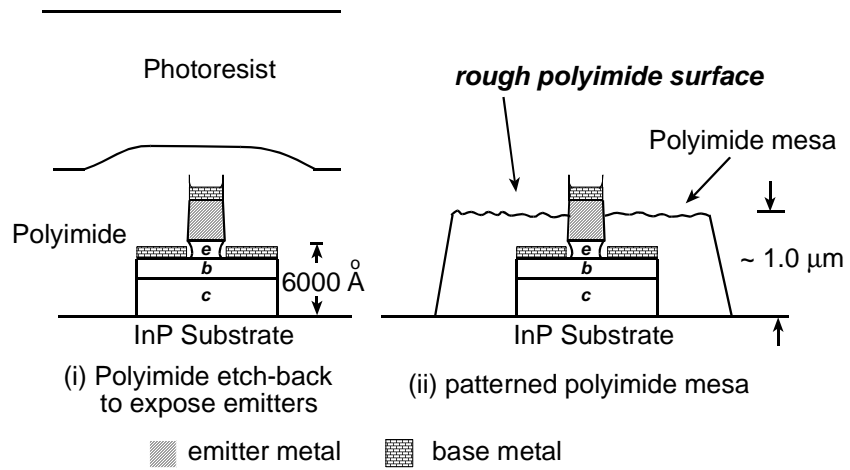
Fig. 5.6: *Device cross section after the base mesa isolation and polyimide device passivation step.*

Emitter

Roughness of
Polyimide
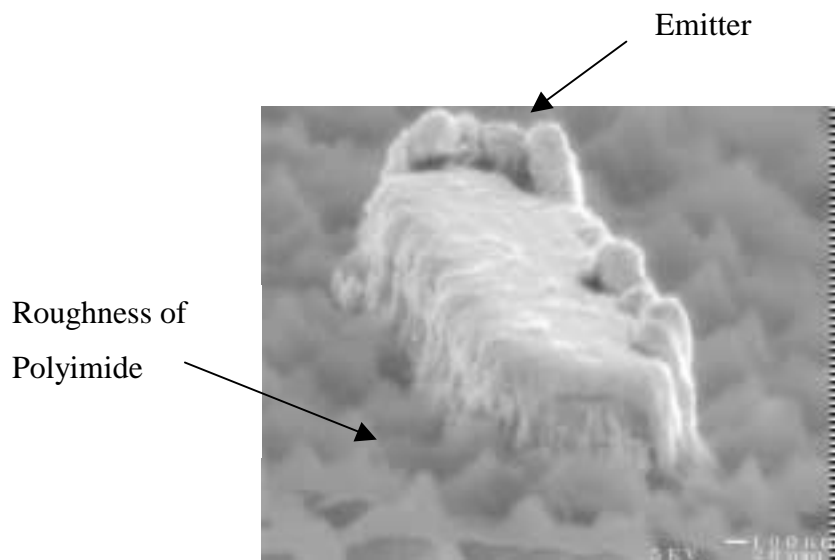
Fig. 5.7: *SEM picture showing the roughness of the polyimide layer.*

deposited before the NiCr deposition. The SiO_2 protects the NiCr resistor during the substrate removal etch (HCl based wet etch) carried out after the substrate transfer step. SiO_2 also provides isolation between the thin conducting Ti layer and the NiCr layer. It was observed (by co-workers) that the substrate removal etch does at times attack the NiCr resistors in spite of the SiO_2 protective film (Fig. 5.8). Even so, the results discussed later in this chapter all use this method for resistor protection.

An attempt to deposit and lift-off 1000 Å of evaporated SiO_2 prior to the resistor deposition process was carried out to protect the resistors from substrate removal etch. The deposited SiO_2 was meant to be a continuous layer with small vias to access the emitter, base and collector contact metals (Fig. 5.8). But lift-off from the small vias (3.0 x 3.0 μm^2) is difficult, and this approach was not reproducible from run to run. Another approach (developed by Yoram Betser) involved depositing 2000 Å of SiN and then etching vias in SiN using dry (O_2/CF_4) etch. This etch is a timed etch and results in over-etching the SiN to ensure open SiN vias. Approximately 500 Å of polyimide near the emitter metal also gets etched. This approach may be more reproducible than attempting to lift-off SiO_2 from small areas, but requires further development to be useful.

5.5   First Interconnect level (metal-1) metallization

The exposed emitter and base metal is contacted by the first interconnect metal level (metal-1). Approximately 1 micron of interconnect metal is deposited. During this evaporation, the wafer is mounted at an angle (~ 30 degrees) to the metal

source and also subjected to rotation to achieve step coverage of the polyimide mesa. The resulting metal pattern has slanting sidewalls, which is good for the step coverage during the metal-1 to metal-2 cross over.
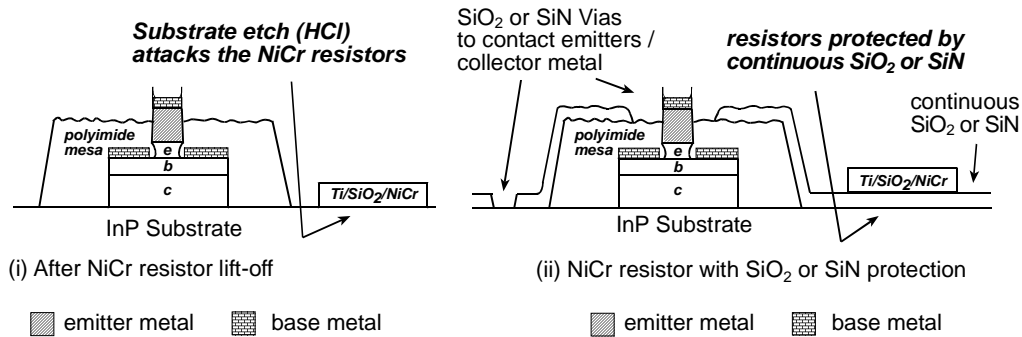
Fig. 5.8: *Wafer cross section after NiCr resistor deposition and lift-off. Shown on the right side is how the cross section looks if a resistor protection layer is added prior to resistor deposition.*

The angled metal evaporation and lift-off procedure creates a problem. A thin metal layer gets deposited on the photoresist edges (Fig. 5.9) and the semiconductor region shadowed by the lift-off profile of the photoresist. After the lift-off process, this thin metal layer sometimes shows up as folded metal at the base of interconnect metal layers. This is shown in Fig. 5.10.

Another possible failure mechanism can be created if there are discontinuities in metal-1 as it runs down the polyimide mesa. This is shown in Fig. 5.11. Also shown alongside is the SEM picture of excellent step coverage of the polyimide mesa by

metal-1. The roughness of metal-1 over polyimide can also be observed and contrasted against the smooth profile of metal-1 on top of the semiconductor.
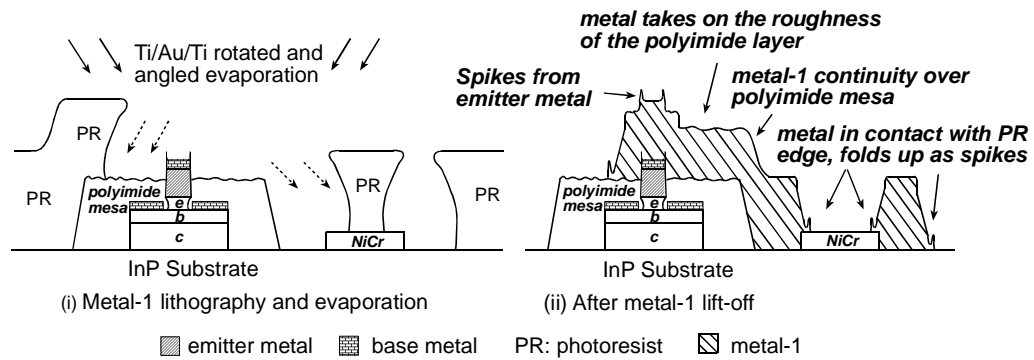
Fig. 5.9: *Device cross section during and after metal-1 deposition and lift-off.*
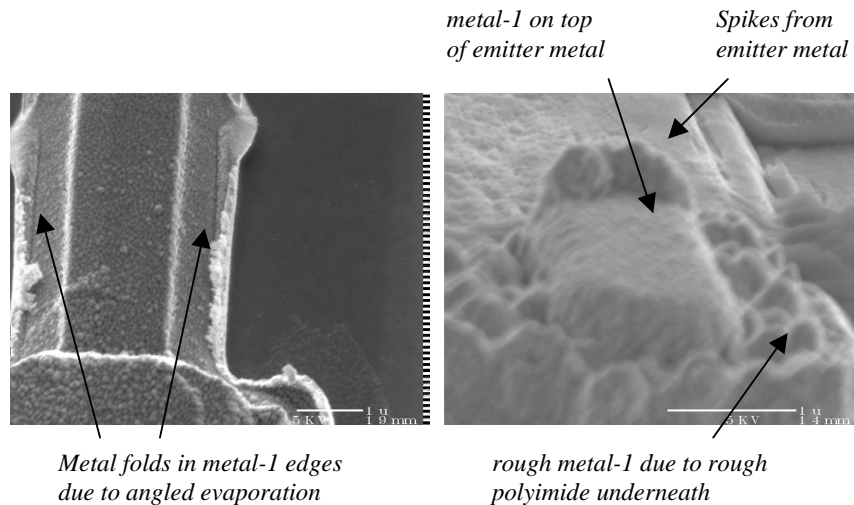
Fig. 5.10: *SEM pictures showing the features on metal-1 after lift-off.*

Excellent step coverage of metal-1
down the polyimide mesa

Possible break in metal-1 line
as it runs down the polyimide mesa

metal -1 on polyimide mesa

metal -1 on InP substrate
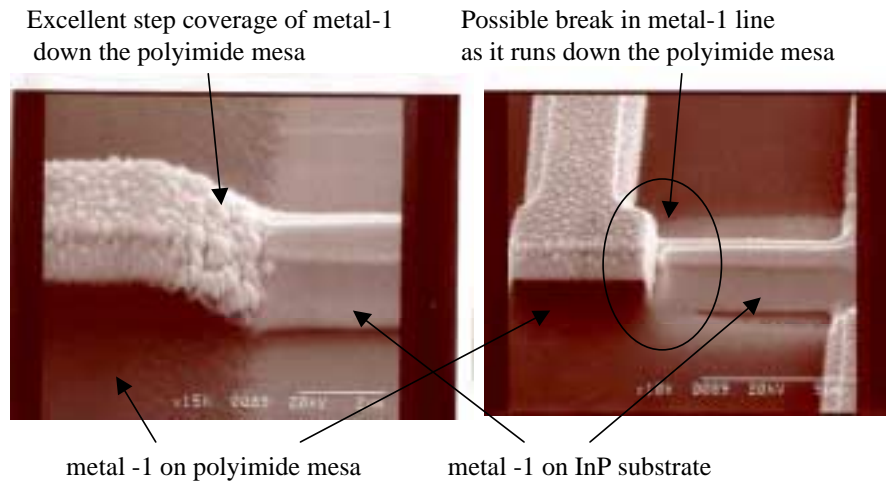
Fig. 5.11: *SEM picture showing both continuous as well as possible discontinuous metal-1 step coverage over polyimide mesa.*

5.6 Silicon nitride (SiN) dielectric deposition

After metal-1 deposition and lift-off, a blanket layer of SiN (~ 4000 Å) is deposited. Silicon nitride serves as the dielectric layer that provides electrical isolation between the two interconnect metal levels. Photoresist is spun on the wafer, and lithography is carried out to define areas corresponding to vias in SiN. The vias are etched in SiN using $SF_6/Ar/O_2$ based reactive ion etching. The smallest SiN vias that are reproducible from run to run is 2.0 x 2.0 μm^2. The cross section of the wafer after the SiN step is shown in Fig. 5.12. It is important that SiN provide excellent sidewall coverage of metal-1. This is especially important over the transistor area defined by the polyimide mesa. This is because the heat sink (second

interconnect metal, metal-2) for the devices is defined right on top of the SiN over the device region. Inadequate sidewall coverage or pin-holes in SiN can result in electrical contact between metal-1 and metal-2 (heat sink) which is not desirable.

SEM pictures after SiN deposition and patterning are shown in Fig. 5.13. Dielectric layers tend to charge up when bombarded with electron beams. Hence, it is difficult to obtain sharp SEM pictures (Fig. 5.13) with SiN layer on the surface. A thin layer of gold (~ 100 Å) is sputtered on top of SiN prior to doing the SEM. The SEM pictures show a rough SiN surface on top of the polyimide mesa. This is from the roughness of the underlying polyimide surface. The SEM pictures appear to indicate sidewall coverage of metal-1. But electrical measurements described later in the chapter seem to indicate that SiN does not provide adequate electrical isolation between metal-1 and metal-2 (next process step) over the devices.

5.7   Second interconnect level metallization (metal-2)

After the SiN etch, a second interconnect metal (metal-2) is deposited. This metallization is similar to the first interconnect metal level. The deposition procedure includes keeping the wafer at an angle (~ 30 degrees) to the metal sources and rotating the wafer holder. Hence metal-2 exhibits similar features as metal-1, and a cross section is shown in Fig. 5.14. The significant failure mechanism limiting IC yield is metal-1 to metal-2 electrical contact on top of the device. Since metal-2 (heat sink) is connected to the ground plane, a short between metal-1 to metal-2 will

SF$_6$/Ar/O$_2$ based dry etch **SiN Via**

SiN

SiN   SiN

polyimide
mesa e

b

SiN   SiN

SiN   c   NiCr   SiN

InP Substrate
(ii) Patterning and opening SiN via

▨ emitter metal ▨ base metal ◨ metal 1
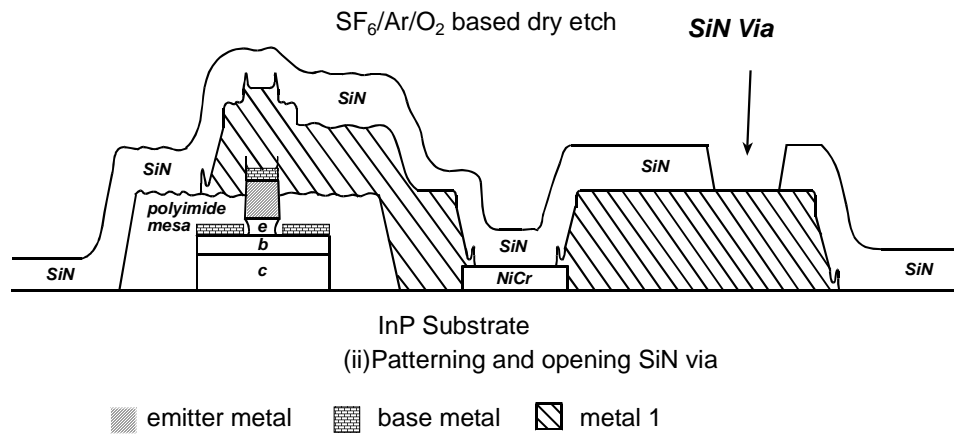
Fig. 5.12: *Wafer cross section after SiN deposition and patterning.*

SiN on polyimide mesa   SiN on metal-1 over polyimide mesa

SiN on metal-1 in contact with emitter metal
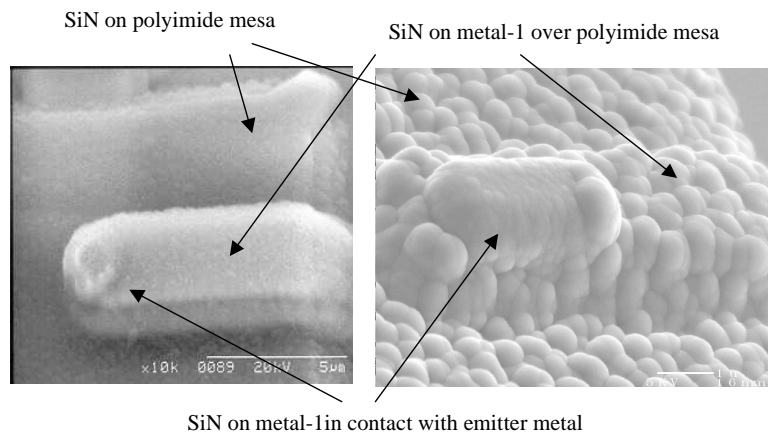
Fig. 5.13: *SEM picture taken after SiN deposition. The SEM picture shown on the right has a thin layer of gold (~ 100 Å) deposited on top of the SiN to improve the contrast and resolution (compared to the picture on the left side).*

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metal 2 heat sink

SiN via for metal 1 to metal 2 contact

SiN

SiN

SiN

polyimide mesa

e

b

c

SiN

NiCr

SiN

SiN

InP Substrate

(i) After metal 2 depsosition and lift-off

emitter metal   base metal   metal 1   metal 2
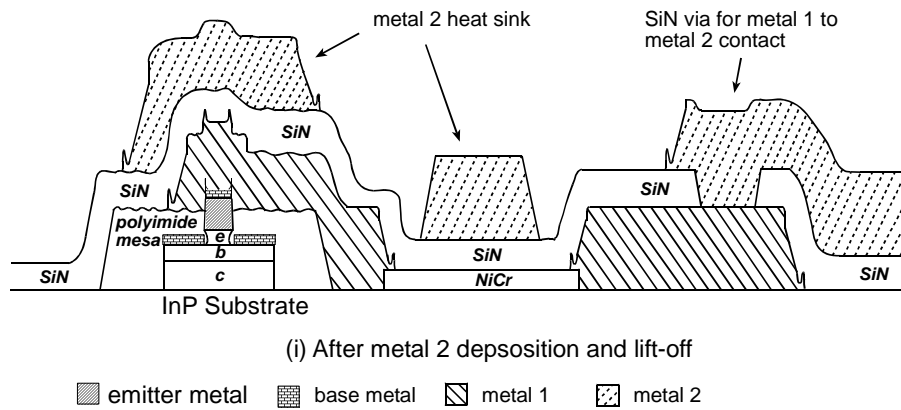
Fig. 5.14: *Cross section of the wafer after metal-2 lift-off.*

result in the emitter of the transistor being grounded. This failure mechanism is henceforth referred to as emitter shorts. Emitter shorting is the dominant failure mechanism and has resulted in the failure of a number of process runs. More detailed investigations into emitter shorts are discussed later in this chapter. SEM pictures of the metal-2 heat sink on top of the devices are shown in Fig. 5.15.

5.8   Benzocyclobutene etch and substrate transfer

Benzocyclobutene (BCB) is a low dielectric constant polymer and is used as the dielectric medium between metal-1/metal-2 and a continuous ground plane. The continuous ground plane is plated on top of the BCB. BCB is first spun on the wafer and cured. This is followed by a blanket deposition of SiN (1 μm thickness). Low temperature SiN deposition is used to prevent thermal stress in the stacked dielectric

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and metal layers. SiN is used as the etch mask for the BCB via etch. SiN is patterned, and vias in SiN are etched using $O_2/SF_6/Ar$ etch as described in Sec. 5.6. An O_2/CF_4 based reactive ion etching is used to etch BCB vias. The etch has a BCB:SiN selectivity of greater than 6:1. At the end of the BCB etch almost all of the SiN is etched away from the top of the BCB. The cross section of the wafer after BCB etch is shown in Fig. 5.16.

Metal-2 - SiN- metal-1 - emitter metal layer   *metal-2 heat sink*

metal-2 on top of the device   *metal-1 - SiN - metal-2 layers on polyimide*
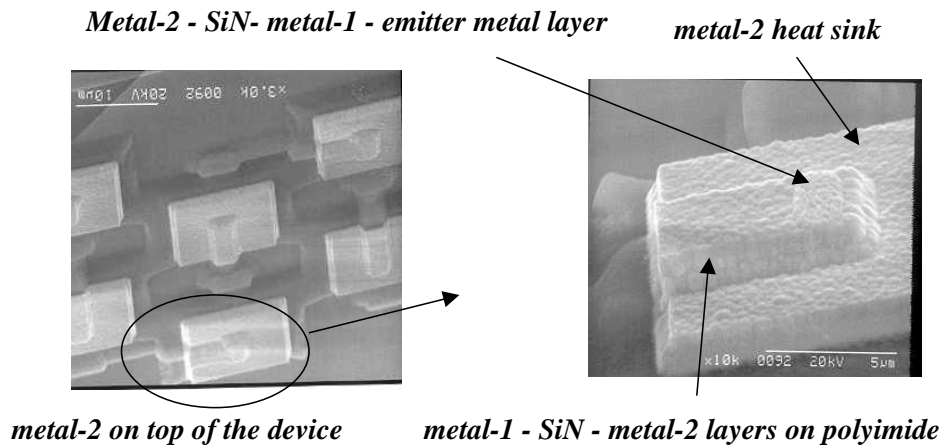
Fig. 5.15: *SEM picture after metal-2 deposition on top of the device. Shown on the left side is the SEM picture of the metal-2 heat sink of a number of transistors, and on the right side is an enlarged SEM picture of a transistor.*

The height of BCB on top of the resistor is about 1.5 μm more than the height of BCB on top of the device. Hence to open the BCB via on the resistor the BCB via on top of the device needs to be over-etched. This can result in an increase in the width of the BCB via. Metal-2 acts as a vertical etch stop layer for the BCB

via etch. If the BCB via goes out of the metal-2 window then the BCB etch etches

through the SiN layer. This is also possible if the metal-2 is misaligned with respect

to the BCB via beyond the alignment tolerance provided. If the BCB via etches the

SiN outside the metal-2 window, then the subsequent gold plating results in the
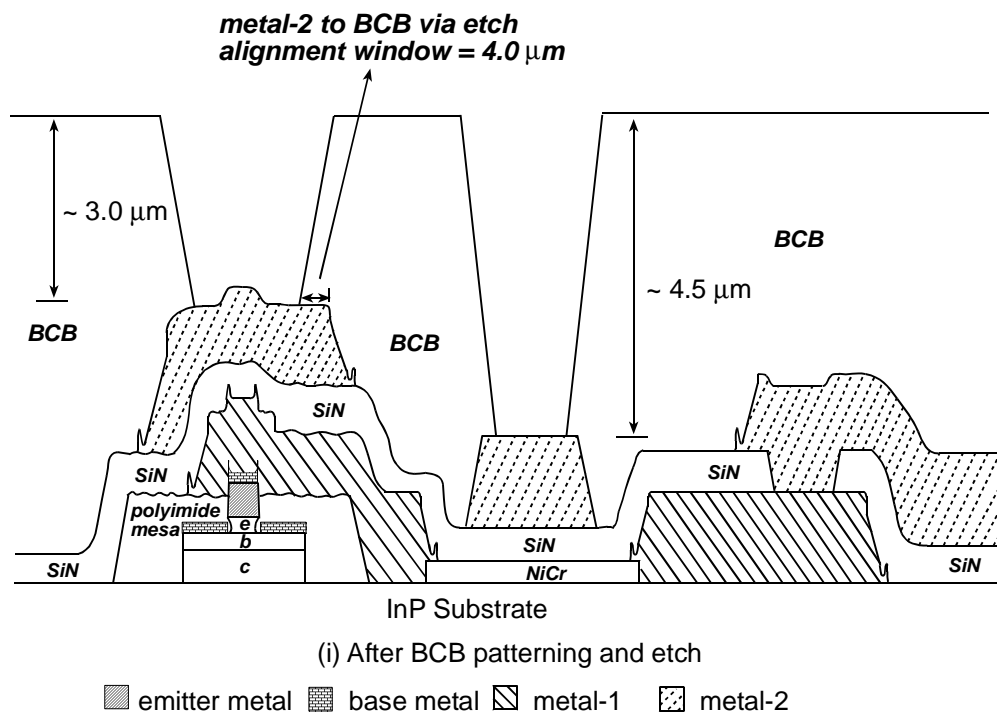
Fig. 5.16: *Cross section of the wafer after the BCB etch is shown above. Note that*

the thickness of BCB on top of the metal-2 heat sink is 1.5 μm less than the thickness

of BCB on top of the resistor. Hence to open the BCB via on top of the resistor the

BCB via on top of the device needs to be over-etched.

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ground plane making electrical contact to metal-1. This results in the emitters of the devices getting grounded and is a possible cause for emitter shorts. This was investigated by varying the alignment tolerance (from 4.0 μm to 5.5 μm) between the BCB via edge and the metal-2 edge. The measurements indicated no significant emitter shorts for both the alignment tolerances used. The end of the resistors that use metal-2 heat sink can also get connected to the plated ground plane if the BCB etch goes out of the metal-2 window.

A flash layer of Ti/Au is then sputtered onto the processed wafer as well as a GaAs wafer. The GaAs wafer is used as the carrier wafer to which the processed wafer is later bonded. Gold plating is carried out to form a continuous ground plane. As mentioned earlier, the presence of BCB between the continuous ground plane and the interconnect metals provide a low loss microstrip wiring environment. After gold plating, the wafer is placed on the bonder chuck (at 180^0 C) and indium solder is spread on the wafer. The processed wafer is then bonded to the GaAs carrier wafer. The sputtered Ti/Au on the surface of GaAs wafer and the plated gold on the surface of the processed wafer ensure adhesion between the two wafers when indium solder is used for bonding.

5.9   Substrate removal and collector deposition

Substrate removal etch (HCl etch) is then carried out to remove the InP substrate. Subsequent collector lithography and metal deposition defines the collectors of the transistors. A collector recess etch (citric acid etch) removes

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approximately 750 Å of the collector semiconductor outside the collector metal. The cross section of the completed wafer is shown in Fig. 5.17. A number of process runs tend to fail at the substrate transfer process. This is mainly caused by poor adhesion between the GaAs wafer and the processed wafer. Also if the adhesion between BCB and the sputtered Ti/Au layer is poor, then the epitaxial layer tends to peel away during substrate transfer.
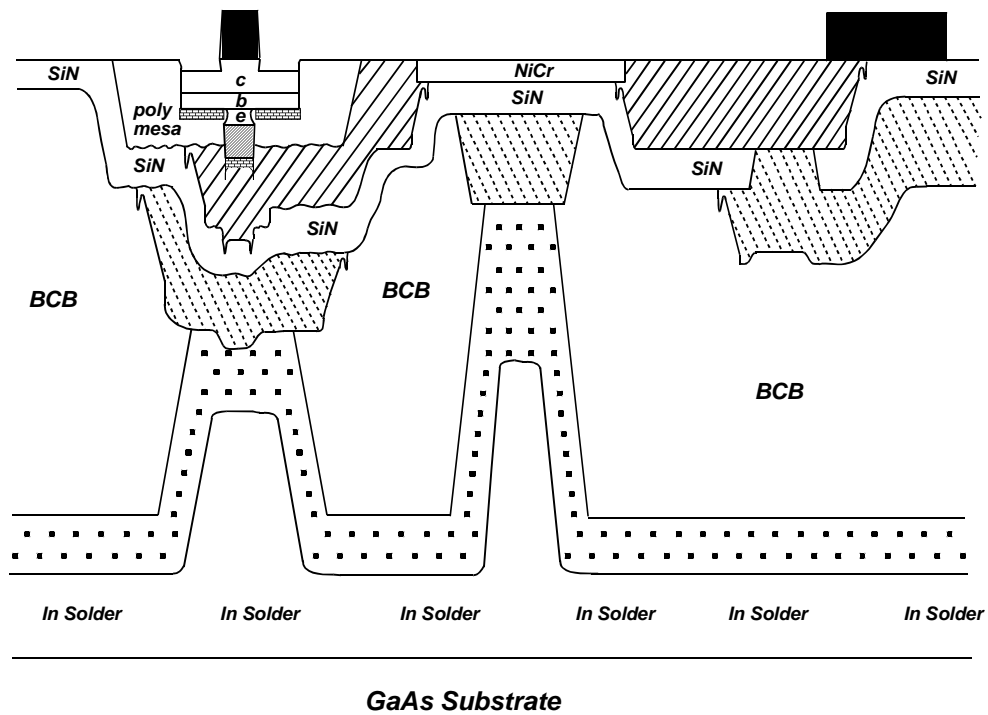
Cross section of the completed TSHBT wafer

■ collector metal   ▨ emitter metal   ▦ base metal   ▨ metal-1   ▨ metal-2   ▣ Plated gold

Fig. 5.17: *Cross section of the wafer after the completion of the process.*

5.10 Possible failure mechanisms

As was mentioned in section 5.7, the primary failure mechanism in this process is the emitter shorts. This is caused by the inadequate electrical isolation provided by the SiN layer present between the interconnect metals. This results in emitter of the transistor getting shorted to the metal-2 heat sink of the device. The possible causes for this and the other possible failure mechanisms identified in Sec. 5.1 to 5.9 are discussed below. The test structures used to identify the nature and extent of failure caused by each possible failure mechanism are presented. These failure mechanisms have been identified in the process steps discussed in Section 5.1 to 5.9.

5.10.1 Base emitter diode shorts

The self-aligned base metal deposition can cause base-emitter shorts as described in Section 5.2 (Fig. 5.2). To identify the presence of base-emitter shorts a test structure consisting of a parallel combination of 32 base-emitter diodes is used. This is shown in Fig. 5.18. If there is a base-emitter short, this shows up as a short circuit in the parallel diode chain. If there are no base-emitter shorts, then the parallel diode chain will show the I-V characteristics corresponding to a diode with a turn-on voltage around 0.7 V. The measurement results from three wafers are also shown in Fig. 5.18. In each of these wafers 24 diode chains were measured and the failure rate is shown in Fig. 5.18. The yield is about 96% (Wafer-III) in the best-processed wafer and approximately 71% (Wafer-I) for the worst-case. These

calculations assume that only one diode out of the 32 diodes is shorted in a defective test structure.

Parallel diode chain test structure (32 diodes in parallel)	Yield in % Yield / 24 diode chains
Wafer-I	71% 17 /24
Wafer-II	91% 22 /24
Wafer-III	96% 23/24
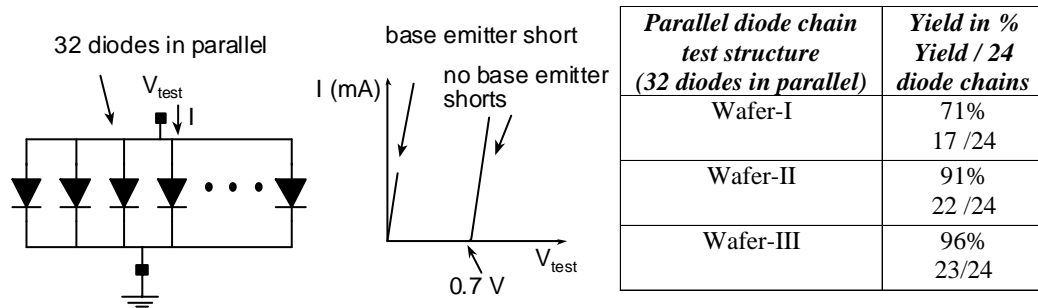
Fig. 5.18: *Parallel base-emitter diode chain used to identify and obtain the failure rate due to base-emitter shorts. Also shown are the expected I-V curves of the diode chain in the presence and absence of the base-emitter shorts.*

5.10.2 Polyimide roughness: (metal-1 to metal-2 short)

After the polyimide etch-back and patterning, the surface of the polyimide mesa is extremely rough. This is shown in Fig. 5.6 and Fig. 5.7 and is discussed in Section 5.3. The roughness of the polyimide layer transfers itself to the metal and the SiN layers that are deposited on it. The integrity of the electrical isolation provided by the SiN layer between metal-1 and metal-2 is therefore in question. To analyze this, MIM (metal-insulator-metal) capacitor-like test structure was used. Polygonal shaped areas of metal-1 is defined on top of the polyimide mesa. SiN is deposited on top of metal-1, followed by metal-2. The metal-2 layer is completely enclosed with in metal-1 area. The cross section of this test structure is shown in

Fig. 5.19. The area of the test structure was varied from 4000 μm^2 to 80,000 μm^2. The equivalent transistor count corresponding to 80,000 μm^2 is approximately 2600 transistors. A transistor presents approximately 30 μm^2 metal-1 to metal-2 overlap area. The test structure was tested for metal-1 to metal-2 shorts. The results from the measurements of this test structure are shown in Table 5.1 for three wafers. A wafer has between 15 to 20 test structures. The yield is close to 100% for the 4000 μm^2 test structure but reduces to close to 80% for the 80,000 μm^2. There is also a slight difference in the measured data from wafer to wafer. This shows that yield reduction due to polyimide roughness is significant for transistor counts of several thousand.
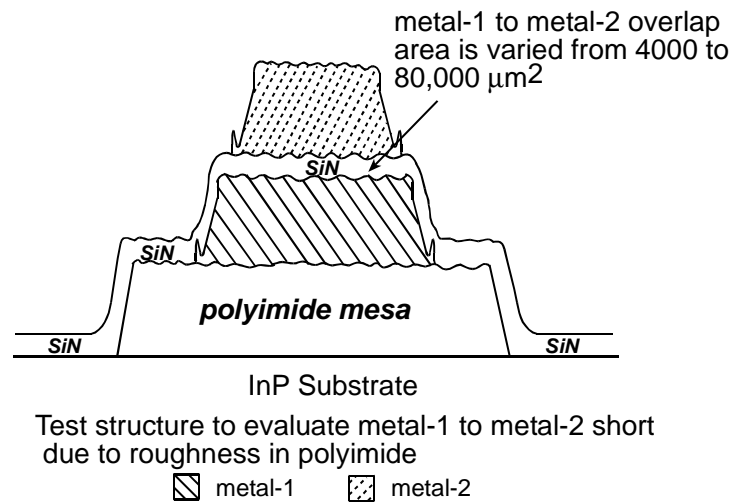
Fig. 5.19: *Test structure used to evaluate the effect of polyimide roughness on metal-1 to metal-2 electrical isolation.*

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Table 5.1: *Measured failure statistics from the test structure (Fig. 5.19) used to evaluate the effect of polyimide roughness.*

Metal-1 to metal-2 overlap	*Wafer-I Yield in %*	*Wafer-II Yield in %*	*Wafer-III Yield in %*
4000 μm^2	94% (17/18)	100 % (19/19)	100 % (19/19)
20,000 μm^2	89 % (16/18)	100 % (19/19)	95 % (18/19)
80,000 μm^2	78% (14/18)	95 % (18/19)	79 % (15/19)

5.10.3 SiN pin-holes

Pin-holes in SiN can also cause metal-1 to metal-2 shorts. To investigate the presence of pin-holes, a test structure similar to Fig. 5.19 is used. This is shown in Fig. 5.20. The metal-1–SiN–metal-2 MIM structure sits on the smooth semiconductor surface instead of the rough polyimide. Hence the roughness of polyimide does not come into picture during this measurement. The test structure was tested for metal-1 to metal-2 shorts. The result from this test structure is shown in Table 5.2. The metal-1 to metal-2 overlap area was varied from 4000 μm^2 to 80,000 μm^2. A wafer has between 15 to 20 pin-hole test structures. The pin-hole density is relatively low in all the measured wafers, and the failure rate is approximately 0% for the 4000 μm^2 test structure and nearly 10% for the 80,000

μm^2 (equivalent to 2600 transistors) test structure. This is about half the value for

the same test structure used to investigate the effect of polyimide roughness.
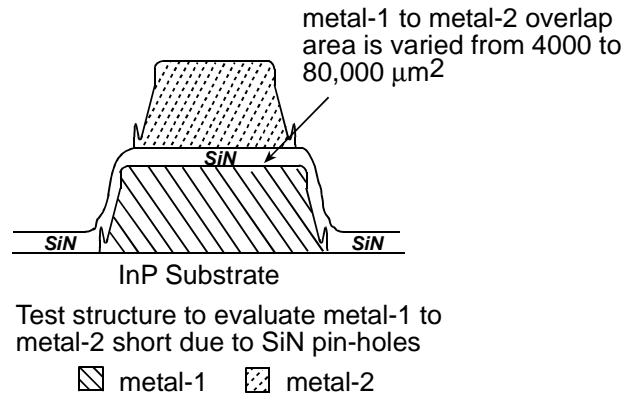
Fig. 5.20: *Shown in the figure above is the test structure used to evaluate the*

presence of pin-holes in SiN.

Table 5.2: *Measured failure statistics from the test structure (Fig. 5.20) used to*

evaluate the effect of SiN pin-holes.

Metal-1 to metal-2 overlap area	Wafer-I Yield in %	Wafer-II Yield in %	Wafer-III Yield in %
4000 μm^2	94% (16 / 17)	100 % (18/19)	100 % (19/19)
20,000 μm^2	100 % (17/17)	95 % (18/19)	95 % (18/19)
80,000 μm^2	87 % (15/17)	95 % (18/19)	100 % (19/19)

5.10.4 Silicon nitride sidewall coverage of metal-1

The presence of spikes in the base of metal-1 lines (Fig. 5.10) can cause metal-1 to metal-2 shorts due to inadequate sidewall coverage of metal-1. The metal-1 to metal-2 shorts resulting from this failure mechanism is a function of metal-1 perimeter seen between the metal-1-SiN-metal-2 layer. Hence, long narrow metal-1 lines (3 μm wide) are run on polyimide as shown in Fig. 5.21. Metal-1 lines are fully enclosed in metal-2 (Shown in Appendix G). The length of the metal lines was varied from 2 mm to 8 mm. Approximately 15-20 test structures were tested for metal-1 to metal-2 shorts in a wafer. The results are shown in Table 5.3 for three wafers. On an average the yield on 2mm lines is close to 100%, whereas for the 8 mm lines the yield is nearly 90%. The worst case data that was measured corresponds to 20% failure rate for 8 mm lines. The equivalent transistor count for the 8 mm line (16 mm perimeter) is about 650 transistors. Each transistor presents approximately 25 μm of metal-1 perimeter to metal-2.

5.10.5 Series connected base-emitter diode chain

The series diode test structure consists of 32 base-emitter diodes in series. This test structure mimics the topography seen by the transistors. The diode chain is realized using the basic transistor layout footprint wired together as series connected base-emitter junctions. The cross section of the device is shown in Fig. 5.22. The metal-2 heat sink above the device is grounded and is required to efficiently remove

metal-1 to metal-2 sidewall
length is varied from 2mm to
8 mm,

SiN

SiN

polyimide mesa

SiN   SiN

InP Substrate

Test structure to evaluate metal-1 to metal-2 short
due to inadequate metal-1 sidewall coverage by SiN

◪ metal-1   ◪ metal-2
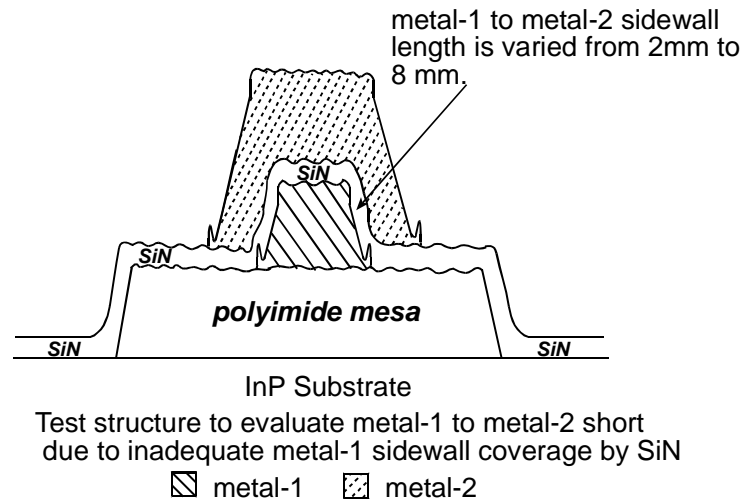
Fig. 5.21: *Shown above is the test structure used to evaluate the quality of sidewall coverage of metal-1 by SiN.*

Table 5.3: *Measured failure statistics from the test structure (Fig. 5.21) used to evaluate the quality of sidewall coverage of metal-1 by SiN.*

Length of metal-1 lines	Wafer-I Yield in %	Wafer-II Yield in %	Wafer-III Yield in %
2 mm	94 % (16 / 17)	95 % (18/19)	100 % (19/19)
4 mm	87 % (15/17)	100 % (19/19)	100 % (19/19)
8 mm	81 % (14/17)	95 % (18/19)	100 % (19/19)

heat as BCB has poor thermal conductivity. The heat sink can be modeled as a metal-1-SiN-metal-2 capacitor connected to the emitter of the base-emitter diodes (Fig. 5.22). To make sure that the emitter shorts are due to a metal-1 to metal-2 short, the heat sinks of all the devices are connected together to a separate pad as shown in Fig. 5.22. The diode test structure was tested immediately after the metal-1 deposition and showed a turn on voltage around ~ 22.5V. This corresponds to the turn-on voltage of 32 series connected diodes (32 x 0.7 V). After SiN and metal-2 step in the process, the following measurements were done to check the presence of metal-1 to metal-2 shorts over the device.

(i)   A test voltage was applied between the input of the diode chain and the metal-2 pad. The voltage was increased from 0 to 25 V and the presence of any current is monitored. In the absence of metal-1 to metal-2 shorts there should not be any current. In many cases measurements indicated I-V curves corresponding to one or more diode drops. This indicates the presence of metal-1 to metal-2 shorts along the emitters of the base emitter diode chain.

(ii)   A test voltage was applied between the input and output terminals of the diode chain. The measurements indicate an I-V curve corresponding to less than 32 diode drops. In many cases I-V curves corresponding to 3 or 4 diode drops were observed. This is indicative of multiple metal-1 to metal-2 shorts along the diode chain.

Typical I-V curves are shown in Fig. 5.23 for the above measurements. The expected I-V curves in the presence and absence of emitter shorts are shown in Fig. 5.23. The corresponding electrical equivalent circuit showing emitter shorts are shown in Fig. 5.22. Measured data on the series connected base-emitter diode chain is shown in Table 5.4. The measurement done on the wafer that yielded circuits up to 60 HBT complexity (wafer-II), had a yield of 40 % out of the 24 diode chains measured. The other 3 wafers show 0% yield and had no working circuits. Thus, emitter shorting is the primary failure mechanism, and a large number of process runs have failed due to the presence of emitter shorts.

Table 5.4: *Measured yield statistics from the series diode test structure (Fig. 5.21).*

Base-emitter diode chain (32 diodes)	*Wafer-I*	Wafer-II	*Wafer-III*	*Wafer-IV*
Yield in % (Yield / 24 structures)	0 % (0 / 24)	40 % (10/24)	0 % (0/24)	0 % (0/24)

5.10.6 *Metal-1 step coverage of polyimide mesa*

SEM pictures after metal-1 (Fig. 5.11) show the possibility of breaks in metal-1 lines as it runs down the polyimide mesa. To test the existence of this, the test structure shown in Fig. 5.24 is used. In this test structure, the metal-1 lines run across a number of polyimide mesas. The metal-1 connectivity at the ends of the
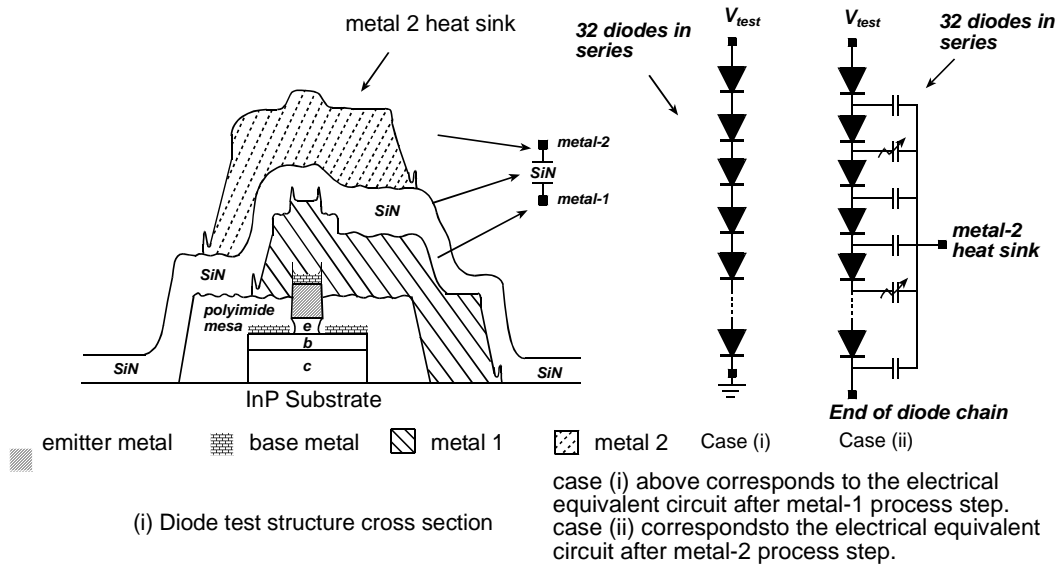
Fig. 5.22: *Cross section of a diode in the diode test structure and the electrical equivalent circuit of the diode test structure at metal-1 step and after metal-2 process step.*
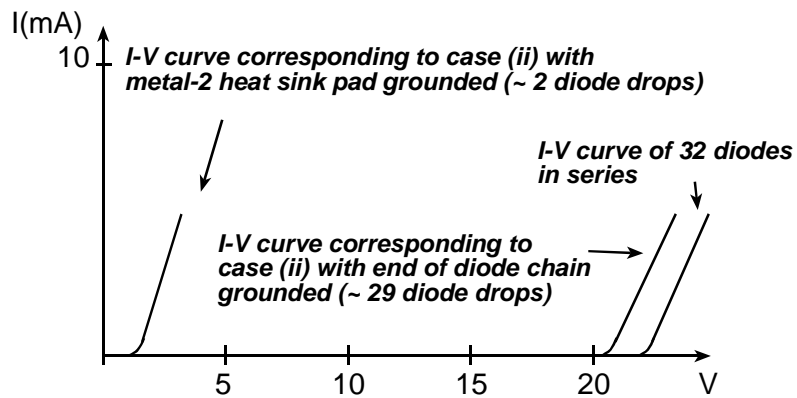
Fig. 5.23: *I-V curve corresponding to multiple metal-1 to metal-2 shorts for the case shown in Fig. 5.22.*
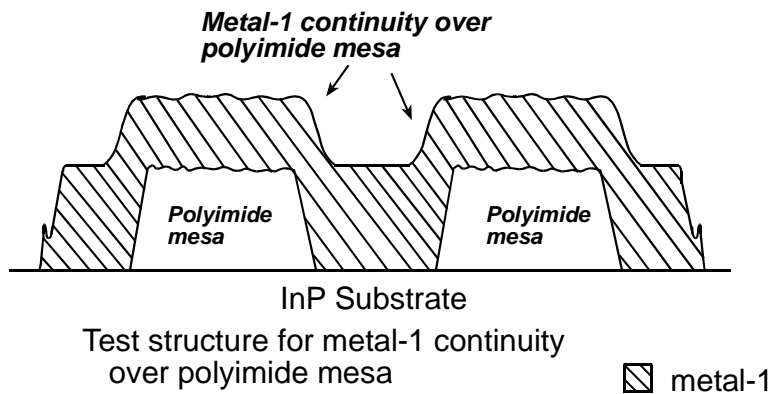
Fig. 5.24: *metal-1 step coverage of polyimide test structure and results*.

metal lines is measured to ensure no breaks in the metal-1 line as they run across the

polyimide mesas. The measurement results are shown in Fig. 5.24 for metal-1 lines

running down about 80 polyimide mesas. There are no indications of breaks in

metal-1 lines on any of the tested wafers.

5.10.7 Uniformity of SiN via etch

A 2.0 x 2.0 μm^2 SiN via is used in the circuits for achieving metal-1 to

metal-2 connectivity. To test the uniformity of the SiN via etching process, the test

structure shown in Fig. 5.25 is used. The electrical connectivity of the metal-1-SiN

via-metal-2 structure is tested. The results of the measurements for a chain

containing 100 SiN vias indicated no failures on all the 3 wafers that were tested.
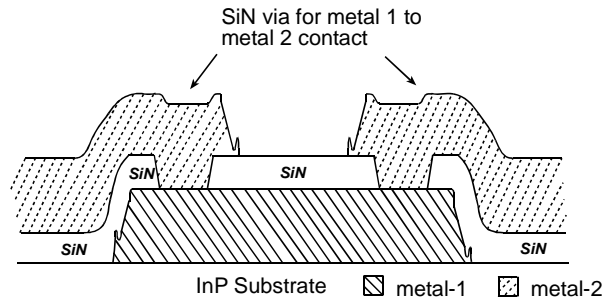
Fig. 5.25 *Test structure used to measure the uniformity of SiN via etching process.*

5.11 Conclusions from the yield test structures

Metal-1 to metal-2 shorts (emitter shorts) on top of the device mesa were identified as the primary failure mechanism in circuits built in the transferred-substrate HBT technology. This causes the emitters of the transistors in contact with metal-1 to be shorted to the metal-2 heat sink which is grounded (Fig. 5.14 and 5.16). In circuits, this causes the emitters of the transistors to be grounded. The heat sink is needed for the device in this technology because the insulating dielectric (BCB) used to realize microstrip lines is a poor thermal conductor. Hence, a metal-2 layer needs to be deposited on top of the device and BCB vias etched to ground metal-2.

Various test structures used to identify the cause of emitter shorts were discussed in the earlier sections. These include, polyimide roughness, pin-holes in SiN, and insufficient SiN coverage of metal-1 sidewalls. These test structures do not show sufficient metal-1 to metal-2 shorts to explain the high number of emitter

shorts. Neither do they mimic the exact topographical features seen by metal-1 and metal-2 on top of the device. The only test structure that does so is the series connected base-emitter diode chain, and it shows significant emitter to heat sink shorts across a number of wafers. Though series connected diode test structures indicate that emitter to heat sink shorts are due to insufficient electrical isolation provided by SiN, they do not clearly identify the exact cause leading to this. Different steps were attempted to provide better metal-1 to metal-2 isolation. These include increasing the SiN thickness from 4000 Å to 8000 Å and evaporating approximately 500 Å of SiO_2 before SiN deposition. Increasing the SiN thickness did not prevent emitter shorts. Deposition of SiO_2 by E-beam evaporation (done by S. Krishnan) seems to reduce the number of emitter shorts.

The other important failure mechanism is the base-emitter diode shorts. The cause of base-emitter diode shorts was discussed in Sec. 5.1 and Sec. 5.10.1. The emitter photoresist is intentionally underexposed to prevent base-emitter shorts. If the photoresist is not underexposed, then the resulting lift-off profile can lead to metal strands being deposited at the base of the emitter metal. These metal strands cause the base-emitter shorts during the subsequent base-emitter etch and base metal deposition. Underexposing the photoresist to prevent a good lift-off profile is very sensitive to photoresist aging as well as any variation in the optical power output of the lithography tool. Base-emitter diode shorts tends to become significant in circuits having 300 HBT complexity and higher.

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Chapter 6

Conclusion

6.1   Summary of achievements

In this work high-speed digital circuits were demonstrated in transferred-substrate HBT technology. The fabricated circuits include the carry and sum logic circuits of a 2-bit adder and a static frequency divider circuit clocking up to 75 GHz.

Two generations of adder circuits were fabricated and tested. The design of the first generation carry logic circuit of a 2-bit adder used a wired-OR/AND (Sec. 3.5) technique. Simulations indicate that this approach is 1.3:1 faster when compared to realizing the carry logic using AND gates and OR gates. The sum logic gate is realized using XOR logic gates (Sec. 3.5).

The carry and sum logic circuit corresponding to the wired-OR/AND adder design were fabricated and tested. The maximum measured clock rate of operation was 8.0 GHz for the carry logic circuit. This was much lower than the maximum simulated clock rate of 25 GHz for the carry logic circuit. The discrepancy between the simulated and measured data was mainly due to the 2:1 larger C_{cb} measured on this process run. Circuit simulation carried out using device parameters extracted from this process run indicates a maximum clock rate of 12 GHz for the carry logic circuit. The simulated data does not include the effect of interconnect lines and

metal cross over capacitances which will further degrade the circuit performance from the simulated data rates. Measurements of the sum logic circuit indicated a maximum clock rate of 14 GHz.

The second generation of adder circuits used a new single 3-level series-gated logic gate (Sec. 3.8) to realize the AND-OR logic necessary to generate the carry output of an adder. This new logic gate was merged with the synchronizing latches to form a 4-level series-gated AND-OR-Latch gate (Sec. 3.9). Circuit simulations carried out using the 4-level AND-OR-Latch gate to realize the carry logic of a 2-bit adder, shows a 1.8:1 improvement in clock speed when compared to the wired-OR/AND approach. Similarly, the sum logic circuit can also be realized by merging the XOR logic gate with the synchronizing latches as discussed in Sec. 3.9.

The carry and sum logic circuits corresponding to the merged AND-OR-Latch adder design were fabricated and tested. The measured clock rates for the carry logic circuit was 19 GHz and 24 GHz for the sum logic circuit. Device measurements indicated that the HBTs had very low current gains $(\beta = 5 - 10)$. Further, RF measurements indicated that the forward transit time of the device is about 0.85 ps when compared to 0.5 ps used in the HBT device models. The large forward transit time (1.7:1 larger) and low current gain of the devices were due to incorrect band gap grading during the base growth of the epitaxial layer. This led to lower measured clock rates when compared to the simulated clock rates for the carry and sum logic circuits.

The simulated and measured clock rates for the various design approaches are summarized in Table. 6.1. The best reported adder results known to us at this time correspond to a 12-bit adder-accumulator clocking at 7.5 GHz [36]. The circuit simulations for the various design approaches were done using the same device model (Appendix D) so as to identify the improvement in clock rates provided by each of these design approaches.

A static frequency divider circuit was fabricated and tested. Frequency divider operation was observed up to a maximum clock rate of 75.0 GHz. This is lower than the simulated clock rate of 90 GHz. Effect of interconnect lines and metal cross over capacitances are not included in the circuit simulation. The demonstration of frequency divider operation at 75 GHz brings the transferred-substrate HBT technology one step closer to realizing 100 GHz logic speeds. This is also the highest reported frequency divider operation in any semiconductor technology.

As a part of this work, the yield limiting mechanisms in transferred-substrate was investigated. The metal-1 to metal-2 short on top of the transistors was identified as the primary failure mechanism in transferred-substrate HBT technology. This causes the emitters of the transistors to get grounded resulting in the failure of 10 to 20 transistor circuits in many wafers. The emitter shorts result from insufficient metal-1 to metal-2 electrical isolation provided by the SiN dielectric layer. A number of approaches, including thicker SiN and deposition of a SiO_2 layer (by E-beam evaporation) prior to SiN deposition were attempted. Initial results indicate that deposition of thin SiO_2 layer seems to reduce the presence of

emitter shorts. Unfortunately, increasing the thickness of the deposited SiO_2 or SiN layer will result in reduced heat removal from the device because of the increased thermal resistance offered by the thicker layers.

Table 6.1: *Table shows the simulated clock rates for the various adder design approaches discussed in chapter 3. The measured performance for the designs fabricated are also listed.*

Design approaches to realize carry logic	*Simulated Performance ($f_{ck\ max}$)*	*Measured Performance($f_{ck\ max}$)*
Using discrete AND gates and OR gates (Sec.3.5)	19 GHz	(not fabricated)
Wired OR/AND approach (Sec. 3.5)	25 GHz	8 GHz
Single 3-level series-gated AND-OR logic gate (Sec. 3.8)	27 GHz	(not fabricated)
Merged 4-level series-gated AND-OR-Latch logic gate (sec. 3.9)	42 GHz	19 GHz

The other significant failure mechanism observed was the presence of base emitter diode shorts resulting from the self-aligned base-emitter metal deposition. The results from the test structures indicate that this can affect the yield in circuits having 300 and higher HBT complexity. This work demonstrated circuits up to

approximately 250 HBT complexity, the highest so far in transferred-substrate HBT technology.

6.2   *Suggestions for future work*

The performance of adder circuits designed and fabricated in this work does not correlate with the simulated circuit performance. For most part, the discrepancy was due to the difference between the measured values of the device parameters and the device parameter values used in the large signal HBT model. In the first generation of adder designs, the 2:1 larger C_{cb} observed on the wafer resulted in slower devices and lower clock rates. In the second generation of adder designs, the incorrect epitaxial growth of the HBTs resulted in large forward transit times and slower devices. The fabrication of the adder designs with faster devices corresponding to the HBT device models should result in carry and sum logic circuits clocking close to 40 GHz. Further improvements in adder clock rates are possible by improving the logic speed of the transferred-substrate HBT technology. This involves designing fast HBTs which will make it possible to achieve 100 GHz logic speeds in transferred substrate HBT technology.

The propagation delay analysis shown in Appendix C indicate that the transistor switching speed is primarily limited by the RC charging time constant associated with the base-emitter capacitance. The base-emitter depletion capacitance dominates the base-emitter capacitance of the switching transistor. Reducing the

base-emitter depletion capacitance involves careful epitaxial layer design and appropriate choice of emitter doping levels.

Significant increase in the switching speed of the device can be achieved by reducing the resistance in the charging path of the device capacitances. The significant resistances include the base resistance r_{bb}, the load resistance R_L, and the emitter extrinsic resistance r_{ex}. Base resistance can be improved by deep submicron scaling [16] (using E-beam lithography) of the device and also through the use of carbon doping in the base. Carbon doping in excess of $1x\ 10^{20}\ cm^{-3}$ (as compared to $4.0\ x\ 10^{19}\ cm^{-3}$ Be doping) is currently being pursued and should significantly reduce the base resistance.

Reduction in the value of the load resistance ($R_L = \Delta V/(J_e\ A_e)$) is possible if the maximum current density of operation (J_e) can be increased beyond $1\ mA/\mu m^2$ (currently being used). The maximum current density of operation is limited by the ability to remove heat from the device. The InGaAs and InAlAs layers used in the epitaxial layers of the HBTs have poor thermal conductivity. The use of InP emitters and collectors (InP/InGaAs/InP HBTs) can improve the heat removal from the device and result in lower values for the load resistance R_L. Careful epitaxial layer design should also be done to ensure that the increased current density of operation does not result in base push out [16]. The exact cause for the emitter resistance (r_{ex}) observed in transferred-substrate HBT technology is not known at this time. Attempts are already underway to identify the cause of r_{ex} and reduce its value.

Another limitation of the devices used in the transferred-substrate HBT technology is the low breakdown voltages (<1.2 V). Multiple diodes are needed, especially in the emitter followers, to ensure that the voltage levels across the devices are below the breakdown values. This results in increased transistor count even for a simple circuit like a static frequency divider. The use of InP collector instead of InGaAs collectors would ensure breakdown voltages in excess of 2.0 V. The saturated electron velocity in InGaAs and InP are comparable and hence there is no significant reduction in device performance. These modifications should result in a transferred-substrate HBT technology capable of logic speeds in excess of 100 GHz.

Appendix A

Specification of HBT parameters and device geometry
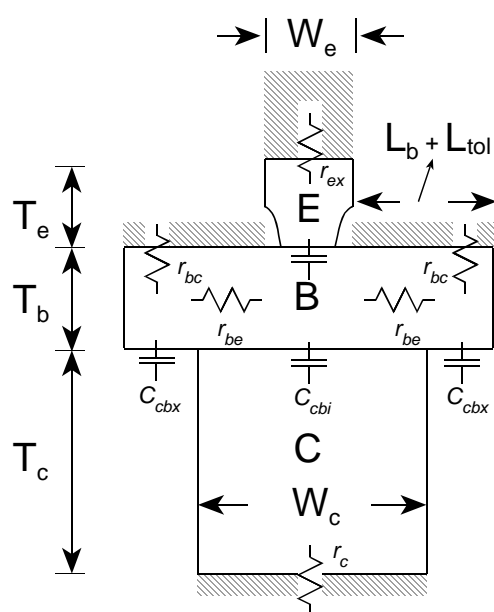
Fig. A.1: *Shown above is the transferred-substrate HBT device structure along with the abbreviation of the device parameters used throughout the thesis.*

W_e emitter width,
L_e emitter Length,
W_b base width,
W_c collector width,
L_c effective collector length,
L_{corr} correction for
       wafer shrinkage,
L_{tol} Alignment tolerance,
L_b base contact transfer
       length,
A_e emitter area (W_e x L_e),
A_c base collector junction
       area (W_c x L_c),

$W_c = W_e + 2(L_{corr} + L_{tol})$

C

L_{tol}

E

L_e

$L_c = L_e + L_{corr} + 2L_{tol}$

$(L_{corr} + L_{tol})$

$= (L_b + L_{tol})$

B

$W_b = W_e + 2(L_b + L_{tol})$

W_e
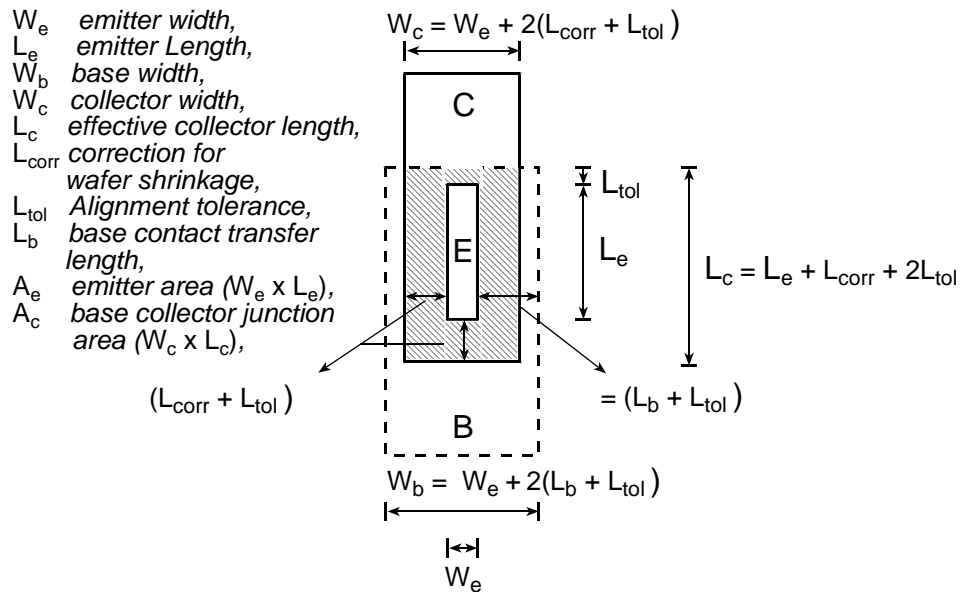
Fig. A.2: *Top view of the device layout showing the device dimensions. Shaded region corresponds to the extrinsic base-collector area that contributes to the base-collector capacitance.*

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Appendix B

Scaling properties of device parameters

Table B.1: *Scaling properties of device parameters*

Device parameter	*Geometry dependence*	*Dependence on Epitaxial layer parameters*
r_{ex}:	$\alpha\, A_e$	$\alpha\, [N_{De}^{-1} \exp(-k\, N_{De}^{-1/2})]^{1/2}$
r_{be}	$\alpha\, W_e$	$\alpha\, N_{Ab},\, T_b^{-1}$
r_{bc}	$\alpha\, L_e$	$\alpha\, [N_{Ab}^{-1} \exp(-k\, N_{Ab}^{-1/2})]^{1/2}$
r_c	$\alpha\, A_c$	$\alpha\, [N_{Dc}^{-1} \exp(-k\, N_{Dc}^{-1/2})]^{1/2}$
C_{je}	$\alpha\, A_e$	$\alpha\, N_{De}^{1/2}$
C_{diff}	$\alpha\, A_e$	$\alpha\ T_b,\, T_c, v_{sat}, \tau_f$
C_{cbx}^{*}	$\sim \alpha\, (A_c - A_e)$	-nil-
C_{cbi}^{*}	$\sim \alpha\, A_e$	$\alpha\, N_{Dc}^{1/2}$
$J_{e\,max}$	-nil-	$\alpha\, T_c^{-3/2}$, collector doping near the base (kirk effect)

*The exact partitioning of the base-collector capacitance C_{cb} into intrinsic and extrinsic base-collector capacitance is achieved by fitting the C_{cbi} value to correspond to the measured f_{max} as is described in [16]. In that case there is no dependence on emitter and collector geometries.

Assumptions involved are listed below [16,34,35].

(i)   The extrinsic emitter/collector resistance arises from the emitter contact and there is no significant contribution from the emitter/collector semiconductor. The dependence of contact resistivity ρ_c on doping is given by $\rho_c \propto \exp(-k\, N_D^{-1/2})$ [34]. The sheet resistivity (R_{sh}) is inversely proportional to doping density $(R_{sh} \propto N_D^{-1})$. The contact resistance is given by $R_c = (\rho_c\, R_{sh})^{1/2}$. The dependence of contact resistance on the doping density is given by,

$$R_c \propto [N_{De}^{-1} \exp(-k\, N_{De}^{-1/2})]^{1/2}$$

(ii)   The depletion width in the base is assumed to be negligible for both base-emitter and base-collector junctions. This is valid as long as the base is much more heavily doped than the emitter and collector region near the base.

(iii)   Base band-gap grading reduces the base transit time. This is accounted for as reduced forward transit time of the device.

(iv)   A n^+ sub-collector is assumed to be present in the collector layer. It is also possible to do away with n^+ sub-collector and use a schottky collector contact instead. This results in a fully depleted collector at zero bias. In that case, there is no doping dependence for the collector resistance or the base-collector junction capacitance.

N_{De} is the emitter cap doping, N_{Ab} is the base doping, and N_{Dc} is the n^+ sub-collector doping, τ_f is the forward transit time and v_{sat} is the saturated velocity in the collector.

Appendix C

Method of time constant analysis (MOTC) of ECL latch

C.1   MOTC analysis to calculate 3-dB bandwidth

A general n-port network having no inductors can be represented as a multi-port network with all capacitors shown external to the network. This is shown in Fig. C.1. The transfer function [32] for such a network is given by,

$$\frac{V_3}{V_1} = A_v \frac{1 + b_1 s + b_2 s^2 + \cdots}{1 + a_1 s + a_2 s^2 + \cdots} \qquad (C.1)$$
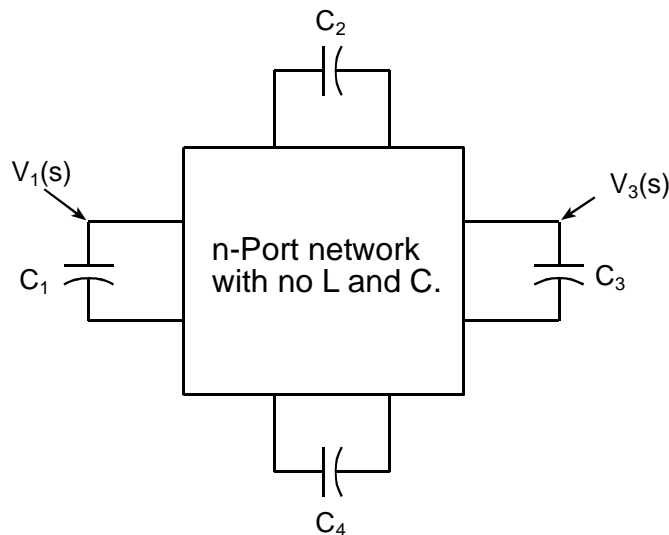
Fig. C.1: *N-port network with all capacitors shown external to the circuit.*

The MOTC analysis applies most directly to the small-signal frequency response of a linear system. Many circuits also include nonlinear elements, such as the voltage-dependent capacitances or current-dependent transconductances of

transistors. The nonlinear elements can be represented by their small/large-signal equivalent circuit values as described below. Assuming that the dominant pole approximation (i.e. $a_2 < a_1$), is valid, the 3-dB bandwidth of the above transfer function is given by

$$f_{3dB} = \frac{1}{2\pi a_1} \qquad\qquad (C.2)$$

The f_{3dB} approximation assumes that there are no zeroes in the transfer function and that the poles are on the negative real axis. This is a good assumption for the types of circuit under consideration as there are no intentional inductors in the circuits, and the circuits do not show any oscillatory or unstable behavior. Circuits exhibiting such behavior are not useful for high-speed digital applications. According to MOTC analysis, the dominant pole a_1, for the example containing four capacitors (Fig. C.1) is given by,

$$a_1 = R_{11}^o C_1 + R_{22}^o C_2 + R_{33}^o C_3 + R_{44}^o C_4 \qquad\qquad (C.3)$$

The resistances $R_{11}^o, R_{22}^o, R_{33}^o, R_{44}^o$ are the resistances seen across the respective capacitor nodes while all capacitors are open circuited. An example showing the evaluation of R_{11}^o is shown in Fig.C.2.

The resistance R_{11}^o can be evaluated by applying a test voltage V at the nodes corresponding to C_1 and evaluating the resulting current I when all capacitors are open circuited.
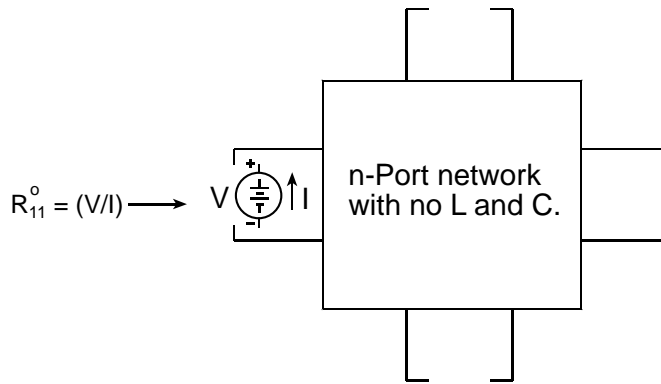
Fig. C.2: *Evaluation of* R_{11}^{o} *for the circuit shown in Fig. C.1 is shown above.*

C.2 MOTC Analysis to evaluate propagation delay (T_{pd})

The basic MOTC approach discussed in Section C.1 can be extended to evaluate the propagation delay in digital circuits. The propagation delay in an ECL latch is evaluated in the next section. This section discusses the steps and approximations involved in using MOTC analysis for propagation delay analysis.

(i)   The two nodes (input and output node) between which the propagation delay needs to be evaluated are identified.

(ii)   The non-linear device elements are converted to their linear equivalent circuits. Small-signal or large-signal equivalent circuit models are used depending on the voltage swings seen across the device terminals.

(iii) The various capacitances involved in the signal propagation path between the two nodes are identified, and the circuit is transformed to an equivalent circuit similar to that shown in Fig. C.1.

(iv)   The effective RC time constant τ (same as a_1) is given by Eq. C.3 and is evaluated as before (shown in Fig. C.2).

(v)   To evaluate the propagation delay, a single time constant exponential charging behavior $\{1\text{-}\exp(\text{-}t/\tau)\}$ of the output node is assumed. Propagation delay is defined as the time delay between a change at the output node, corresponding to a change at the input node. If the time delay is measured between the 50% point of input and output voltage swings, the propagation delay (T_{pd}) is then given by the time taken to charge the output node to 50% of the final value.

$$T_{pd} = (t, \text{ when } 0.5 = 1 \text{-} \exp(\text{-}t/\tau) \ ) = \tau \ln (2) \sim 0.7\,\tau. \tag{C.4}$$

(vi)   Also, MOTC analysis always predicts equal rise and fall times.

C.3   MOTC analysis of ECL latch

The MOTC analysis of the ECL latch is presented here. Shown in Fig. C.3 is the circuit diagram of an ECL latch. The input node corresponds to the clock input at the differential pair at the lower level. The output node corresponds to the emitter node of emitter follower output (Q_6) of the next stage. The MOTC calculation presented here corresponds to the propagation delay between these two nodes. The device capacitances present in the signal propagation path are shown external to the transistors. The transistors need to be replaced by their hybrid-pi equivalent circuits (Fig. C.4). The base to emitter resistance (r_{be} or r_π) which appears in parallel with

C_{be} is neglected as at high frequencies the parallel RC (r_{be} C_{be}) combination behaves as a capacitor. The definitions of the large-signal and small-signal parameters used in the equivalent circuits are shown below. The base-emitter depletion capacitance C_{je} is evaluated as follows.

$$C_{je}\left(\text{large - signal}\right) = \frac{1}{\left(V_1 - V_2\right)} \int_{V_1}^{V_2} C_{je}\left(V\right) dV$$

$$C_{je}\left(\text{small - signal}\right) = C_{je}\left(V\right) = \frac{C_{je}\left(0\right)}{\left(1 + \dfrac{V}{\phi_{be}}\right)^{m_{be}}} \tag{C.5}$$

Where V corresponds to the base-emitter reverse bias voltage, ϕ_{be} is the base-emitter built-in voltage and m_{be} is the base emitter junction grading factor. The voltages V_1 and V_2 correspond to the voltage seen across the junctions before and after the transistor switching.

The same equations hold good for the base-collector junction capacitance C_{cb} also. In the transferred-substrate HBT process, Schottky collector contacts are commonly used. In the case of Schottky collector contacts, the n⁻ collector is fully depleted, and hence the base-collector capacitance does not show any voltage dependence.

The evaluation of the large-signal and small-signal transconductances is shown below. η is the ideality factor and V_T is the thermal voltage. The value of ΔI or dI correspond to the difference in the current flowing through the transistors when the voltage across the base emitter junction changes by ΔV or dV. In the case of the

ECL latch, ΔV is 300 mV and I_c or ΔI is 7 mA ($R_L \sim 45\ \Omega$). The current switching transistors in the ECL latch sees large-signal voltage swings. Hence their device parameters are evaluated as large-signal parameters. The emitter followers in the ECL latch see small-signal base-emitter voltage swings and hence the base-emitter device parameters and g_m are evaluated as small-signal parameters. τ_f is the forward transit time of the device.

$$
\begin{aligned}
G_m \left(\text{large - signal} \right) &= \frac{\Delta I}{\Delta V} = \frac{1}{R_L} \\
g_m \left(\text{small - signal} \right) &= \frac{dI}{dV} = \frac{I_c}{\eta V_T}
\end{aligned}
$$

(C.6)

The base-emitter diffusion capacitance is evaluated as shown below.

$$
\begin{aligned}
C_{be\,diff} \left(\text{large - signal} \right) &= G_m \tau_f \\
C_{be\,diff} \left(\text{small - signal} \right) &= g_m \tau_f
\end{aligned}
$$

(C.7)

To evaluate the time constant, the resistances seen across the capacitors need to be evaluated as shown in Fig.C.2. The coupled emitter nodes of the lower clock transistor pair do not see any voltage swing and hence they behave as virtual ground nodes. This is because there is always a current flow in at least one of the lower differential clock transistors. This is not true of the top differential pair. In the case of the top differential pair, both devices are in cut-off and when the clock makes a low to high transition one of them begins to conduct. This leads to the simplified equivalent circuits (Fig. C.5 – C.8) which are used to evaluate the resistances across the capacitor nodes.
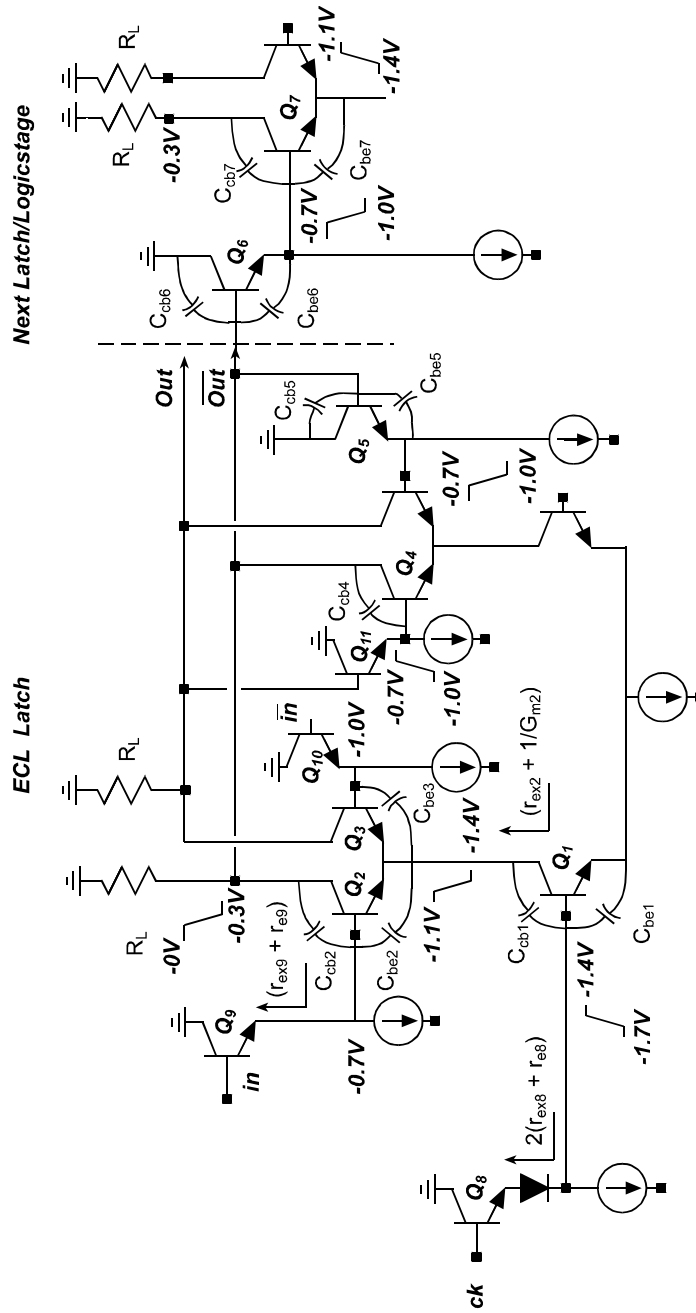
Fig. C.3: *Circuit diagram of ECL latch showing the relevant capacitances in the signal propagation path.*

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The equivalent circuit seen by the device capacitance of transistor Q_1 is shown in Fig. C.5. The collector node is connected to the equivalent resistance seen looking into the emitter of the upper differential pair. Applying Kirchhoffs current and voltage laws, the resistances across the nodes can be evaluated and are shown below. The numbers in the subscripts of the device parameters refers to the corresponding transistors shown in Fig. C.3.

The resistances seen across the device capacitances of transistor Q_2 are shown in Eq. C.9. The emitter of transistor Q_2 corresponding to the coupled emitter node of the upper differential transistor pair sees infinite impedance looking into the collector of Q_1 (Note that Q_3 is in cut-off). The resulting circuit is shown in Fig. C.6.
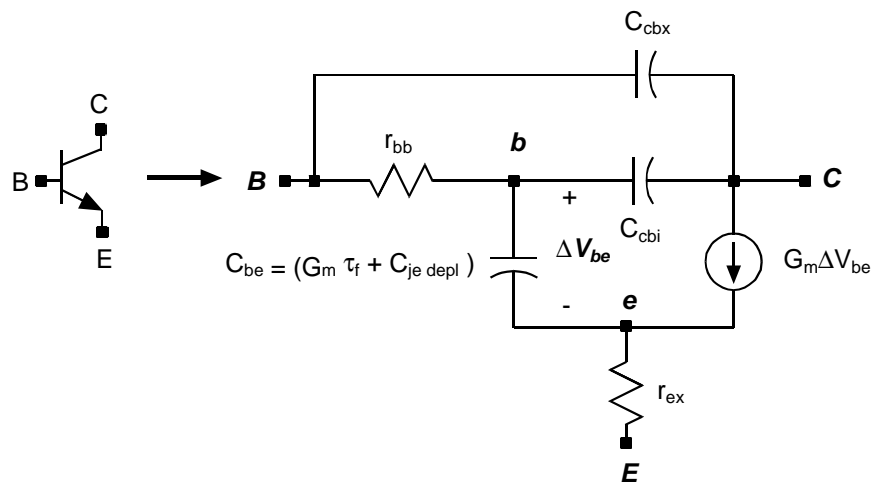
Fig. C.4: *Hybrid-pi equivalent circuit model used in the analysis.*

$$R_{be1} = \frac{\left(r_{bb1} + 2(r_{ex8} + r_{e8}) + r_{ex1}\right)}{1 + G_{m1}r_{ex1}} \approx \left(r_{bb1} + 2(r_{ex8} + r_{e8}) + r_{ex1}\right)$$

$$R_{cbi1} = r_{bb1} + 2(r_{ex8} + r_{e8}) + R_L + r_{ex2} + \frac{\left(r_{bb1} + 2(r_{ex8} + r_{e8})\right)(R_L + r_{ex2})G_{m1}}{(1 + G_{m1}r_{ex1})}$$

$$\text{(C.8)}$$

$$\approx 2r_{bb1} + 4(r_{ex8} + r_{e8}) + R_L + r_{ex2} \quad (\text{assumes } R_L \gg r_{ex1})$$

$$R_{cbx1} = 4(r_{ex8} + r_{e8}) + R_L + r_{ex2}$$

$$R_{be2} = (1/G_{m2}) = R_L$$
$$R_{cbi2} = r_{bb2} + r_{ex9} + r_{e9} + R_L \qquad\qquad \text{(C.9)}$$
$$R_{cbx2} = r_{ex9} + r_{e9} + R_L$$
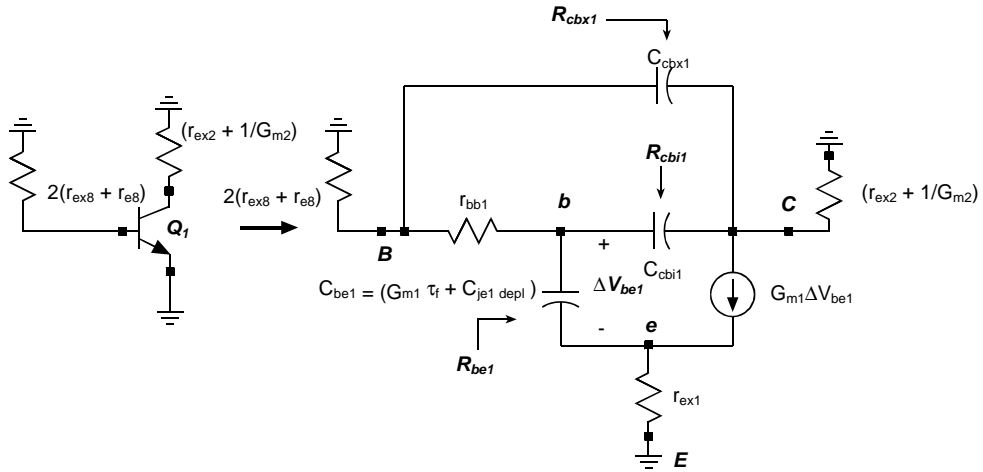
Fig. C.5: *The equivalent circuit used to calculate the resistances across the device capacitances of transistor Q_1.*

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Since transistor Q_3 is in cut-off, only the base-emitter depletion capacitance of Q_3 needs to be charged. The equivalent circuit used to calculate the resistance (R_{be3}) seen across the C_{be} of Q_3 is shown in Fig.C.7. The value of R_{be3} is given by,

$$
\begin{aligned}
R_{be3} &= (1/G_{m2}) + r_{ex2} + r_{ex3} + r_{e10} + r_{ex10} + r_{bb3} \\
&= R_L + r_{ex2} + r_{ex3} + r_{e10} + r_{ex10} + r_{bb3}
\end{aligned}
\tag{C.10}
$$

The resistances seen across the base-collector capacitances of Q_4 is identical to that of Q_2 since they both see identical resistor networks. They are given by,

$$
\begin{aligned}
R_{cbi4} &= r_{bb4} + r_{ex11} + r_{e11} + R_L \\
R_{cbx4} &= r_{ex11} + r_{e11} + R_L
\end{aligned}
\tag{C.11}
$$
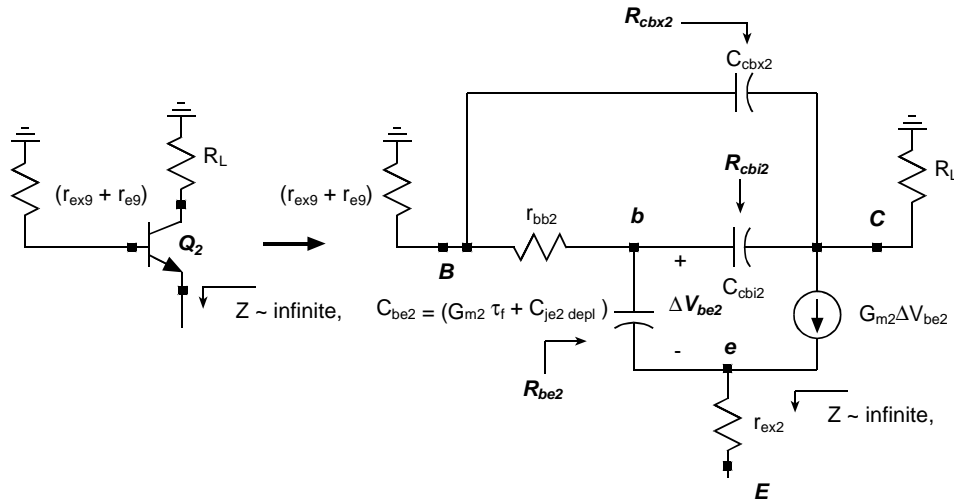
Fig. C.6: *The equivalent circuit used to calculate the resistances across the device capacitances of transistor Q_2.*
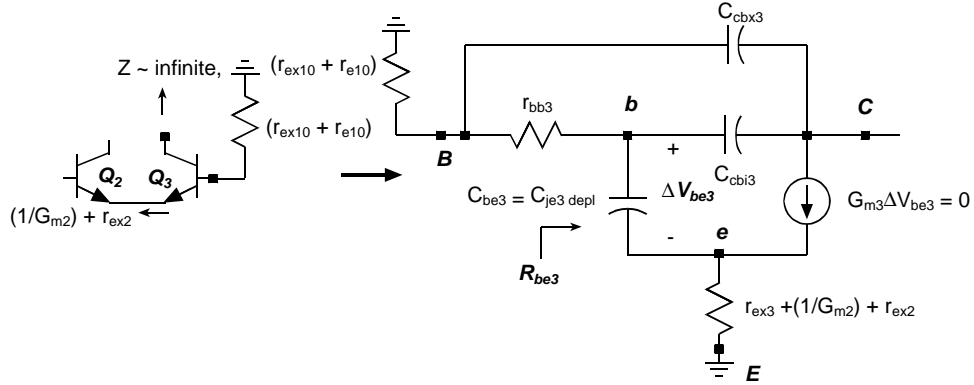
Fig. C.7: *The equivalent circuit used to calculate the resistances across the device capacitances of transistor Q_3. Note that Q_3 is in cut-off.*

Device capacitances of the emitter followers Q_5 and Q_6 see identical equivalent RC networks and are shown in Fig.C.8. The resistances seen across the capacitance of Q_5 and Q_6 are given below.

$$
\begin{aligned}
R_{be5} &= r_{e5} \\
R_{cbi5} &= r_{bb5} + R_L \\
R_{cbx5} &= R_L \\
R_{be6} &= r_{e6} \\
R_{cbi6} &= r_{bb6} + R_L \\
R_{cbx6} &= R_L
\end{aligned}
\tag{C.12}
$$

The device capacitances of transistor Q_7 (Fig.C.3) sees the same equivalent resistive network as seen by Q_2 (Fig.C.6). Hence the resistances seen across the device capacitances of Q_7 are similar to that of Q_2 and are given below. Note that even though the RC network seen by Q_2 and Q_7 are the same, the voltage swing seen

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across the junctions is different. Hence the capacitance values associated with the

devices are also different.

$$R_{be7} = (1/G_{m7}) = R_L$$
$$R_{cbi7} = r_{bb7} + r_{ex6} + r_{e6} + R_L \qquad\qquad (C.13)$$
$$R_{cbx7} = r_{ex6} + r_{e6} + R_L$$

The resulting time constant τ is given by,

$$
\begin{aligned}
\tau = {} & (r_{bb1} + 2(r_{ex8} + r_{e8}) + r_{ex1}) * C_{be1} + (R_L + r_{ex2} + 4(r_{ex8} + r_{e8})) * C_{cbx1} \\
& + (4(r_{ex8} + r_{e8}) + 2r_{bb1} + r_{ex2} + R_L) * C_{cbi1} + R_L * C_{be2} \\
& + (r_{ex9} + r_{e9} + R_L) * C_{cbx2} + (r_{ex9} + r_{e9} + r_{bb2} + R_L) * C_{cbi2} \\
& + (R_L + r_{ex2} + r_{ex3} + r_{e10} + r_{ex10} + r_{bb3}) * C_{be3} \\
& + (r_{ex11} + r_{e11} + R_L) * C_{cbx4} + (r_{ex11} + r_{e11} + r_{bb4} + R_L) * C_{cbi4} \\
& + r_{e5} * C_{be5} + R_L * C_{cbx5} + (r_{bb5} + R_L) * C_{cbi5} \\
& + r_{e6} * C_{be6} + R_L * C_{cbx6} + (r_{bb6} + R_L) * C_{cbi6} \\
& + R_L * C_{be7} + (r_{ex6} + r_{e6} + R_L) * C_{cbx7} + (r_{ex6} + r_{e6} + r_{bb7} + R_L) * C_{cbi7}
\end{aligned}
\qquad (C.14)
$$
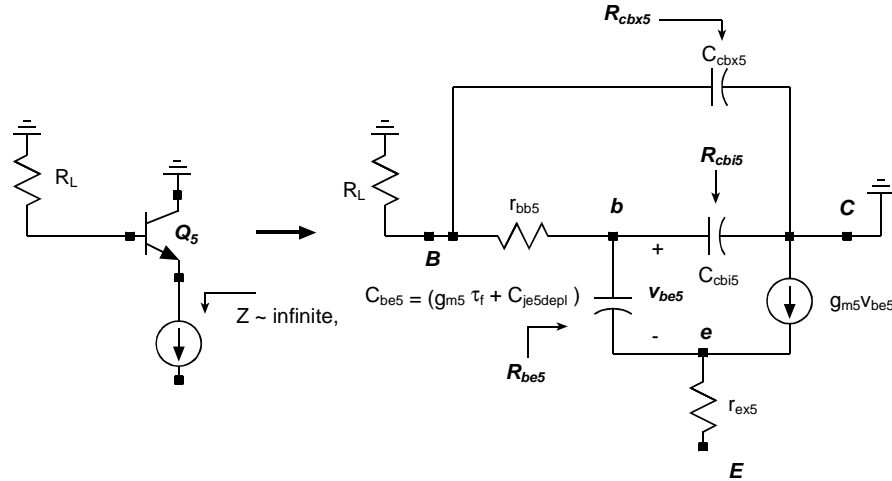
Fig. C.8: *The equivalent circuit used to calculate the resistances across the device capacitance of transistor Q_5 and Q_6.*

This can be further simplified by assuming that all the switching transistors have the same geometry and equal base-emitter and base-collector capacitances. This assumption can be extended for the emitter follower transistors also. In that case, the propagation delay expression can be simplified as shown below (Eq. C.15). The emitter follower parameters are represented by subscripts 'EF'. If the subscript 'EF" is not present then the parameters correspond to the switching transistors. The contribution of the base-emitter capacitances of the switching transistors are expressed in terms of the diffusion (C_{diff}) and the depletion capacitances ($C_{je\ depl}$) of the base-emitter junctions.

$$T_{pd}(latch) = 0.7 * \begin{cases} (r_{bb} + 2r_{exEF} + 2r_{eEF} + r_{ex} + 2R_L) * C_{diff} \\ + (2r_{bb} + 3r_{exEF} + 3r_{eEF} + 3r_{ex} + 3R_L) * C_{je\ depl} \\ + (7r_{exEF} + 7r_{eEF} + 4R_L + r_{ex}) * C_{cbx} \\ + (7r_{exEF} + 7r_{eEF} + 5r_{bb} + 4R_L + r_{ex}) * C_{cbi} \\ + 2r_{eEF} * C_{beEF} + 2R_L * C_{cbxEF} + 2(r_{bbEF} + R_L) * C_{cbiEF} \end{cases} \quad (C.15)$$

The device parameter values are shown in Table C.1 and correspond to 8 x 1 μm^2 emitter and 12 x 2 μm^2 collector devices. The voltage swings seen across the device terminals are shown in Fig. C.3. In this calculation, the emitter follower and switching transistors use the same transistor geometry to correspond to the static frequency divider implementation described in chapter 4.

The relative contribution of the different device capacitances and resistances to the propagation delay is shown in Table C.2. The time constant τ is given by

Eq.C.14 and is the sum of the RC time constants shown in Table C.2. This evaluates to 13.1 ps. The corresponding propagation delay (0.7 x τ) is given by equation C.4 and evaluates to approximately 9.2 ps.

Table C.1: *Device parameter values used to calculate the propagation delay.*

Device parameter	*Switching transistor*	*Emitter follower*
r_{bb}	30 Ω	30 Ω
r_{ex}	6.63 Ω	6.63 Ω
g_m or G_m	(1/45Ω)	(8 mA/32mV)
τ_f	0.5 ps	0.5 ps
C_{diff}	11.1 fF	125 fF
$C_{je}(0)$, ϕ_{be}, m_{be}	17.8 fF, 0.76 V, 0.5	17.8 fF, 0.76 V, 0.5
$C_{bc}(0)$, ϕ_{bc}, m_{bc}	8.2 fF, 0.7 V, 0.33	8.2fF, 0.7V, 0.33
Calculated C_{cb} values	(Q_1: 7.3 fF), (Q_2: 6.9 fF), (Q_4: 6.6 fF), (Q_7: 6.85 fF)	7.7fF
Calculated C_{je} values	(Q_1, Q_2: 36 fF) (Q_3: 21.8 fF), (Q_7: 29.36 fF)	63.3 fF
C_{cbx}/C_{cbi}	3	3

Table C.2: *The relative contribution of the different capacitances to the propagation delay is shown below. The capacitances correspond to the large or small-signal equivalent values.*

Device capacitance	Open circuit resistance	RC time constant
Q_1: $C_{be1} = C_{je\ depl} + C_{diff}$ $= (36 + 11.1)fF$ $= 47.1\ fF$	$R_{be1} = r_{bb} + 2(r_{exEF} + r_{eEF}) + r_{ex}$ $= 58\ \Omega$	2.7 ps
Q_1 : $C_{cbi1} = 1.8\ fF$	$R_{cbi1} = 2r_{bb} + 4(r_{exEF} + r_{eEF}) + R_L$ $+ r_{ex} = 154.26\ \Omega$	0.28 ps
Q_1 : $C_{cbx1} = 5.5\ fF$	$R_{cbx1} = R_L + 4(r_{exEF} + r_{eEF}) + r_{ex}$ $= 94.15\ \Omega$	0.52 ps
Q_2: $C_{be2} = C_{je\ depl} + C_{diff}$ $= (36 + 11.1)fF$ $= 47.1\ fF$	$R_{be2} = R_L = 45\ \Omega$	2.1 ps
Q_2 : $C_{cbi2} = 1.7\ fF$	$R_{cbi2} = r_{bb} + r_{exEF} + r_{eEF} + R_L$ $= 85\ \Omega$	0.14 ps
Q_2 : $C_{cbx2} = 5.2\ fF$	$R_{cbx2} = r_{exEF} + r_{eEF} + R_L$ $= 55.6\ \Omega$	0.29 ps

Q_3: $C_{be3} = C_{je\ depl} = 21.8$ fF	$R_{be3} = r_{bb} + r_{exEF} + r_{eEF} + 2\ r_{ex}$ $+ R_L = 99\ \Omega$	2.1 ps
Q_4 : $C_{cbi4} = 1.65$ fF	$R_{cbi4} = r_{bb} + r_{exEF} + r_{eEF} + R_L$ $= 85\ \Omega$	0.14 ps
Q_4 : $C_{cbx4} = 4.95$ fF	$R_{cbx4} = r_{exEF} + r_{eEF} + R_L$ $= 55.6\ \Omega$	0.28 ps
Q_5 : $C_{be5} = 188.3$ fF	$R_{be5} = r_{eEF} = 4\ \Omega$	0.75 ps
Q_5 : $C_{cbi5} = 1.9$ fF	$R_{cbi5} = r_{bbEF} + R_L = 75\ \Omega$	0.14 ps
Q_5 : $C_{cbx5} = 5.8$ fF	$R_{cbx5} = R_L = 45\ \Omega$	0.26 ps
Q_6 : $C_{be6} = 188.3$ fF	$R_{be6} = r_{eEF} = 4\ \Omega$	0.75 ps
Q_6 : $C_{cbi6} = 1.9$ fF	$R_{cbi6} = r_{bbEF} + R_L = 75\ \Omega$	0.14 ps
Q_6 : $C_{cbx6} = 5.8$ fF	$R_{cbx6} = R_L = 45\ \Omega$	0.26 ps
Q_7: $C_{be7} = C_{je\ depl} + C_{diff}$ $= (29.3 + 11.1)$fF $= 40.4$ fF	$R_{be7} = R_L = 45\ \Omega$	1.8 ps
Q_7 : $C_{cbi7} = 1.7$ fF	$R_{cbi7} = r_{bb} + r_{exEF} + r_{eEF} + R_L$ $= 85\ \Omega$	0.14 ps
Q_7 : $C_{cbx7} = 5.15$ fF	$R_{cbx7} = r_{exEF} + r_{eEF} + R_L$ $= 55.6\ \Omega$	0.29 ps

Following conclusions can be drawn from the analysis shown above.

(i)   The major delay component associated with the device capacitance is associated with the charging of the base-emitter capacitance C_{be}. In the case of the switching transistors, C_{be} is dominated by the base-emitter depletion capacitance, whereas for the emitter followers it is dominated by the diffusion capacitance.

(ii)   It is important to note that the delay associated with the charging of the output node (corresponding to $\overline{out}$ and the emitter node of Q_6 in Fig. C.3) is about 40 % of the total propagation delay of the latch. The capacitance associated with the output node ($\overline{out}$) includes the device capacitances of the two emitter followers (Q_5, Q_6) connected to the node, and the base-collector capacitance of transistors Q_2 and Q_4. They account for about 25% of the total propagation delay. Charging the emitter node of the emitter follower to the next stage (Q_6) contributes to 15 % of the total propagation delay.

(iii)   The lower level switching transistor Q_1 contributes about 27 % of the total propagation delay of the latch (~ 2.45 ps out of the total 9.2 ps). The introduction of an additional third level (3-level series-gated logic gate) adds approximately another 2.45 ps to the logic gate delay.

(iv)   The propagation delay analysis carried out here for an ECL latch can be extended to a 2-level series-gated ECL logic gate (eg. 2-input XOR/AND/OR gates) as they have very similar circuit architectures.

(v)   The propagation delay of two 2-level logic gates in series is much higher than the propagation delay of a 3-level equivalent logic gate. This can be shown based on the above calculations. A 3-input XOR logic operation can be realized using a single 3-input XOR gate or by two 2-input XOR logic gates in series. A 3-input XOR gate has approximately 11.65 ps (9.2 ps + 2.45 ps) propagation delay. The 9.2 ps delay correspond to the delay of a 2-input XOR gate. The additional 2.45 ps is to account for the delay corresponding to the third level as stated above (iii). The total propagation delay of the equivalent two 2-input XOR gates in series is about 18.4 ps (9.2 ps + 9.2 ps) and is about 1.55:1 higher than the propagation delay in a 3-input XOR gate.

The above MOTC calculation is a good starting point to understand the relative contribution of the different transistor parameters to the propagation delay or the logic speed of a circuit. More accurate evaluation of the circuit performance needs to be carried out by doing circuit simulations using the large signal device models.

In a static frequency divider (SFD) circuit, two ECL latches are connected in series to form a master-slave flip-flop. The inverted output of the slave latch is fed back as the input to the master latch to enable frequency divider operation. In analyzing the maximum operating frequency of the SFD, the delay associated with the charging of the base-emitter capacitance of Q_1 (Fig.C.3) does not affect the frequency of the SFD operation. This is because the delay associated with the

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charging of the base-emitter capacitance of the clock transistor shows up as a delay in both the master as well as the slave clock transistors. Hence, the propagation delay of the ECL latch when configured as a static frequency divider is 7.21 ps. This corresponds to a maximum clock rate of 69 GHz ($f_{ck\ max} = 1/\{2 \times T_{pd}$ (ECL latch)$\}$).

Appendix D

HBT model used for circuit simulation of Adders

The large-signal HBT model used in the simulation of the 2-bit adder design is shown below. This model corresponds to a device with an emitter dimension of 8 x 1 μm^2 and a collector dimension of 10 x 3 μm^2. The collector epitaxial layer is 3000 Å thick and is fully depleted at zero bias due to the use of a Schottky collector contact.
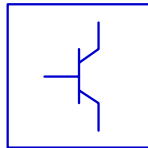
BJT_Model
HBT_adder

NPN=yes	Br=3	Cjc=1.8e-14	Re=6.63
PNP=no	Ikr=0	Vjc=0.7 V	Rc=0
Bf=50	Isc=5.0e-9 A	Mjc=0.33	Kf=0
Ikf=0	Nc=1	Xcjc=0.25	Af=1
Ise=5.0e-11 A	Var=38 V	Fc=0.8	Kb=0
Ne=1.67	Nr=1	Cje=1.78e-14	Ab=1
Vaf=12 V	Tr=0	Vje=0.76 V	Fb=1
Nf=1	Eg=1.11	Mje=0.5	Ffe=1
Tf=5.0e-13 sec	Is=5.0e-12 A	Cjs=0	Lateral=no
Xtf=0	Imax=	Vjs=0.75 V	AllParams=
Vtf=0	Xti=35	Mjs=0	
Itf=0	Tnom=77.96	Rb=30	
Ptf=0	Nk=0.5	Irb=3.0e-3	
Xtb=0	Iss=0	Rbm=30	
Approxqb=yes	Ns=1	RbModel=Libra	

Fig.D.1: *Large-signal HBT model used for adder circuit simulations.*

The model is nearly the same for an 8 x 1 μm^2 emitter and a 9 x 2 μm^2 collector device with 2000 Å thick collector and a 750 Å thick n$^+$ sub-collector. This corresponds to the device geometry and layer structure used in the second set of adder designs. The major difference in the two device models is in the ratio of the intrinsic base-collector capacitance to the total base-collector capacitance (X_{cjc}). X_{cjc} is 0.25 for the first device and close to 0.4 for the latter.

Appendix E

Large signal HBT SPICE model used for divider circuit simulations

The large-signal HBT model used for divider circuit simulations correspond

to a device dimension of 8 x 1 μm^2 emitter and 9 x 2 μm^2 collector. The device had

a 3000 Å fully depleted collector resulting from a Schottky collector contact. The

device parameters are shown below.
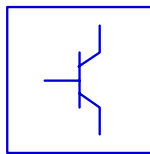
BJT_Model
HBT_divider

NPN=yes	Br=3	Cjc=0.82e-14	Re=6.63
PNP=no	Ikr=0	Vjc=0.7 V	Rc=0
Bf=50	Isc=5.0e-9 A	Mjc=0.33	Kf=0
Ikf=0	Nc=1	Xcjc=0.25	Af=1
Ise=5.0e-11 A	Var=38 V	Fc=0.8	Kb=0
Ne=1.67	Nr=1	Cje=1.78e-14	Ab=1
Vaf=12 V	Tr=0	Vje=0.76 V	Fb=1
Nf=1	Eg=1.11	Mje=0.5	Ffe=1
Tf=5.0e-13 sec	Is=5.0e-12 A	Cjs=0	Lateral=no
Xtf=0	Imax=	Vjs=0.75 V	AllParams=
Vtf=0	Xti=35	Mjs=0	
Itf=0	Tnom=77.96	Rb=30	
Ptf=0	Nk=0.5	Irb=3.0e-3	
Xtb=0	Iss=0	Rbm=30	
Approxqb=yes	Ns=1	RbModel=Libra	

Fig.E.1: Large-signal HBT model used for static frequency divider circuits.

Appendix F

Transferred-Substrate HBT Process flow

F.1   Emitter Contacts (Mask Layer: Emitter)

A. Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

2. Cold Acetone   3 min.

3. Hot Methanol   3 min.

4. Hot Isopropanol   3 min.

5. Running D.I.   3 min.

6. Blow dry with N_2.

7. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Photoresist application and exposure

Safety Note: The vapors from the photoresist are extremely harmful. Never

breathe if you put your head under the hood.

1. Cool down after dehydration, 5min.

2. Wafer on spinner with vacuum, blow with N_2.

3. Apply SPR 950-0.8 with syringe and filter to cover wafer.

4. Spin at 2.5 Krpm for 30 sec.

5. Soft bake 90^0 C, 1 min on hot plate.

6. Apply CEM with syringe and filter to cover wafer.

7. Spin at 4.0 Krpm for 30 sec.

8. Expose for 2.2 sec, set job offset to 34.

C. Development

1. Post bake 100^0 C 2 min, 10 sec.

2. Rinse in D.I., for 30 sec.

3. Develop in MF-701 for 2 min,20 sec.

4. Rinse in running D.I water, 3 min.

5. Blow dry with N_2.

D. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

E. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases/acid. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O = 1 : 10.

2. Dip in dilute HCl for 15 sec.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

5. Put wafer on E-beam mount. Level it.

6. Put in a new crystal.

7. Pump down to below 1 x 10^{-6} Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec)	Approx. Vernier
a. Ti	200	1-2	1.65
b. Pt	400	1	1.85
c. Au	8000	15	1.5
d. Si	500	2-3	1.6

F. Lift-off: ***Do Not let Acetone dry on Wafer***

1. Soak wafer in beaker of Acetone until metal comes loose.

2. If the lift-off is stubborn, leave the wafer soaking overnight. Seal the top of the beaker with Aluminum foil.

3. Squirt Acetone using Acetone squirt bottles.

4. Rinse with Methanol, and then Isopropanol from the squirt bottles.

5. Rinse in running D.I. water for 3 min.

6. Blow dry with N$_2$.

7. Check under microscope and dektak for thickness of metal.

F.2   *Base Contact etch :(no mask required)*

A. Oxygen Plasma descum of Photoresist

1. 300 mT of O$_2$.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

B. Surface preparation

1. Mix a dilute solution of $NH_4OH : H_2O = 1 : 10$.

2. Dip in dilute NH_4OH for 10 seconds.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

C. Dry etch

1. Clean both chucks and shield with Isopropanol.

2. O_2 plasma clean (20 sccm @ 12 mT, 500 V bias for 30 min).

3. Precoat chamber ($CH_4/H_2/Ar$ 4/20/10 sccm @ 125 mT, 300 V bias for 20 min).

4. Load wafer and align laser monitor, then pump down to low 10^{-6} Torr.

5. Etch ($CH_4/H_2/Ar$ 4/20/10 sccm @ 75 mT, 500 V bias) until slope changes.

6. Increase pressure to 110 mT. Etch until desired stop point is reached.

7. Remove polymer (O_2 50 sccm @ 125 mT, 200 V bias for a quarter of the etch time).

8. Vent chamber and remove sample.

D. Si Removal

1. 300 mT of CF_4.

2. Power = 100 W at low frequency.

3. Run for 1 min per 500 Å Si.

4. Check that Si has been removed with optical microscope.

5. Remove samples, clean chamber for 10 minutes with O_2 (300W, 300mT).

6. Replace samples and do standard descum (O_2 @ 100 w, 300 mT, 15 sec).

E. Selective etch

1. Mix a dilute solution of $NH_4OH : H_2O = 1 : 10$.

2. Dip in dilute NH_4OH for 10 seconds.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

5. Mix solution B- $HCl : H_2O = 4 : 1$ in HCl beaker.

6. Mix solution A- HBr : glacial acetic $= 1 : 1$ in solution A beaker with stirrer bar. Mix well.

7. Mix solution A and B $1 : 1$ by adding solution B then solution A to A + B beaker. Mix well.

8. No Stirring, etch for 10 sec.

9. Rinse in D. I for 3 min.

10. Blow dry with N_2.

F. Nonselective etch

1. Mix etchant as follows: 55 ml of 1M citric acid in 220 ml D. I. Mix well. Add 5 ml H_2O_2. Mix well. Add 1 ml H_3PO_4. Mix well.

2. Stirring at 200 rpm etch for 25 sec by suspending the wafer in a basket.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

F.3   Base Contacts (Mask Layer: Base contact)

A. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Photoresist application and exposure

Safety Note: The vapors from the photoresist are extremely harmful. Never

breathe if you put your head under the hood.

1. Cool down after dehydration, 5min.

2. Wafer on spinner with vacuum, blow with N_2.

3. Apply EIR AZ-5214 with syringe and filter to cover wafer.

4. Spin at 6.0 Krpm for 30 sec.

5. Soft bake, 95^0 C 1 min on hot plate.

6. Expose for 0.32 sec, set job offset to 24.

7. Hot plate bake, 105^0 C 1 min.

8. Flood Expose at 7.5 mW/cm^2 for 30 sec.

C. Development

1. AZ 400K : D. I. = 1 : 5.5.

2. Develop for 40 sec.

3. Rinse in running D.I water, 3 min.

4. Blow dry with N_2.

5. Observe under the microscope. If there is a suspicion that some photoresist is

remaining, then go back and develop for another 5 – 10 seconds.

D. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

E. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases/acid. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O = 1 : 10.

2. Dip in dilute HCl for 15 sec.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

5. Put wafer on E-beam mount. Level it.

6. Put in a new crystal.

7. Pump down to below 1×10^{-6} Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec)	Approx. Vernier
a. Ti	200	1-2	1.65
b. Pt	400	1	1.85
c. Au	800	15	1.5

F. Lift-off: *Do Not let Acetone dry on Wafer*

1. Soak wafer in beaker of Acetone until metal comes loose.

2. If the lift-off is stubborn, leave the wafer soaking overnight. Seal the top of the beaker with Aluminum foil.

3. Squirt Acetone using Acetone squirt bottles.

4. Rinse with Methanol, and then Isopropanol from the squirt bottles.

5. Rinse in running D.I. water for 3 min.

6. Blow dry with N_2.

7. Check under microscope and dektak for thickness of metal.

G. RTA for 60 seconds at 300^0 C. Run a test program first.

F.4 Base Isolation etch (Mask Layer: Base Mesa)

A. Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

2. Cold Acetone   3 min.

3. Hot Methanol   3 min.

4. Hot Isopropanol   3 min.

5. Running D.I.   3 min.

6. Blow dry with N_2.

7. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Photoresist application and exposure

Safety Note: The vapors from the photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Cool down after dehydration, 5min.

2. Wafer on spinner with vacuum, blow with N_2.

3. Apply SPR-518 with syringe and filter to cover wafer.

4. Spin at 4.0 Krpm for 30 sec.

5. Soft bake, 90^0 C, 1 min on hot plate.

6. Expose for 0.8 sec, set job offset to 20.

7. Hot plate bake, 110^0 C, 1 min.

C. Development

1. Develop in full beaker of MF-701 for 1 min, 30 seconds.

2. Rinse in running D.I water, 3 min.

3. Blow dry with N_2.

4. Observe under the microscope. If there is a suspicion that some photoresist is remaining, then go back and develop for another 5 – 10 seconds.

D. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

4. Hardbake photoresist at 120^0C for 20 min.

E. Isolation Etch

1. Load Si wafer to be used in RIE #5, Do not load sample.

2. Run a clean program (200 W cl$_2$ clean for 5 min).

3. Set-up laser monitor. Try to center the laser spot on Si wafer.

4. Etch conditons:

   a. Cl$_2$ flow rate = 20.0 sccm.

   b. chamber pressure= 5 mT.

   c. Power = 150 W.

   d. Voltage is around 350 – 400V.

5. Etch until 30 seconds after the slope changes. Approximately 6 min and 30

   sec for 3000 Å collectors and 5min 30 sec for 2000 Å collectors.

F. Resist strip

1. Remove photoresist with acetone in lift-off beaker for 3 min Squirt the wafer

   with acetone.

2. Rinse by spraying with Methanol and Isopropanol.

3. Run for 15 seconds.

4. Hardbake photoresist at 120^{0}C for 20 min.

G. Oxygen plasma photoresist removal (Optional).

1. 300 mT of O$_2$.

2. Power = 100 W at low frequency.

3. Run for 30 seconds.

4. Examine under microscope to ensure photoresist removal.

H. Characterization of process so far

1. Dektak etch depth, test base emitter diodes structures if any, measure TLMs.

F.5 Polyimide planarization (Mask Layer: Poly Etch)

    A. Solvent Cleaning

    1. Get Polyimide out of the refrigerator.

    2. Check the resistivity of the D.I. water. It should be > 17 MΩ.

    3. Cold Acetone   3 min.

    4. Hot Methanol   3 min.

    5. Hot Isopropanol   3 min.

    6. Running D.I.   3 min.

    7. Blow dry with N_2.

    8. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Polyimide spin and cure.

Safety Note: The vapors from polyimide are extremely harmful. Never breathe if you put your head under the hood.

    1. Mix adhesion promoter in designated beaker (Mix 0.3 ml of VM-651 from the bottle using plastic dropper, in 300 ml of D. I. water). Stir and then get a new dropper.

    2. Wafer on spinner with vacuum, blow with N_2.

    3. Apply adhesion promoter to cover wafer.

    4. Let it sit on the wafer for 20 sec.

    5. Spin at 3.0 Krpm for 30 sec.

    6. Hot plate bake, 125^0 C, 3 min.

7. Apply Pyralin PI-2556 polyimide to cover wafer with syringe and 1.0 μm filter.

8. Let it sit on the wafer for 20 sec.

9. Spin at 2.5 Krpm for 30 sec (to give 1.8 μm film).

10. Hard bake in programmable oven. (Program P-3).

   a. Hold at 90^0 C for 60 min.

   b. Ramp at 4^0 C / min to 150^0 C.

   c. Hold at 150^0 C for 60 min.

   d. Ramp at 4^0 C / min to 230^0 C.

   e. Hold at 230^0 C for 60 min.

   f. Ramp at 4^0 C / min to 170^0 C.

C. Photoresist application and exposure

   Safety Note: The vapors from the photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Remove from oven when below 50^0 C.

2. Wafer on spinner chuck with vacuum, blow with N_2.

3. Apply AZ 4330 with syringe and filter to cover wafer.

4. Spin at 5.0 Krpm for 30 sec.

5. Soft bake, 90^0 C, 30 min in petri dish without cover.

6. Hard bake, 120^0 C, 30 min in petri dish without cover.

D. Polyimide Etchback

1. Load RIE #1 according to instructions.

2. Pump down to low E-6.

3. Set-up laser monitor.

   a. Look for diffraction pattern to identify the beam. Laser signal should be about 500 mV. Use the outermost spot of the laser beam.

   b. Set up chart recorder for one hour and a range of –700 mV.

4. Etch conditons:

   a. O_2 flow rate = 7.0 sccm.

   b. Chamber pressure = 10 mT.

   c. Power = 60 W.

   d. Voltage is around 350 V.

5. Etch for 17.5 cycles.

E. Check and clean up

   1. Put in SEM and look at 1.0 μm emitter fingers to see if they are clear.

   2. If not, etch two minutes in PE-II-A at 100W, 300 mT then SEM again.

   3. Remove mung from the backside with ISO soaked Q-tip.

F. Photoresist application and exposure

   Safety Note: The vapors from the photoresist are extremely harmful. Never breathe if you put your head under the hood.

   1. Wafer on spinner with vacuum, blow with N_2.

   2. Apply SPR-518 with syringe and filter to cover wafer.

   3. Spin at 3.0 Krpm for 30 sec.

   4. Hot Plate bake, 90^0 C, 1 min on hot plate.

5. Expose for 1.1 sec, set job offset to 12.

6. Hot plate bake, 110^0 C, 1 min.

G. Development

1. Develop in full beaker of MF-701 for 1 min, 30 seconds.

2. Rinse in running D.I water, 3 min.

3. Blow dry with N_2.

4. Observe under the microscope. If there is a suspicion that some photoresist is remaining, then go back and develop for another 5 – 10 seconds.

5. Flood expose at 7.5 mW / cm^2 for 2 minutes.

6. Hard bake 120^0C, 30 min. in petri dish without cover.

H. Poly Etch

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 30 min.

I. Resist strip

1. Remove photoresist in MF-701, 2 minutes.

2. Rinse in running D.I. for 3 minutes.

3. Blow dry with N_2.

4. Inspect under microscope.

J. Reflow bake

1. Hot plate bake, 250^0C, 10 min. to reflow polyimide and complete the cure.

F.6 NiCr Resistors (Mask Layer: Resistors)

A. Solvent Cleaning

    1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

    2. Cold Acetone   3 min.

    3. Hot Methanol   3 min.

    4. Hot Isopropanol   3 min.

    5. Running D.I.   3 min.

    6. Blow dry with N_2.

    7. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Photoresist application and exposure

Safety Note: The vapors from the photoresist are extremely harmful. Never breathe if you put your head under the hood.

    1. Cool down after dehydration, 5min.

    2. Wafer on spinner with vacuum, blow with N_2.

    3. Apply EIR AZ-5214 with syringe and filter to cover wafer.

    4. Spin at 6.0 Krpm for 30 sec.

    5. Soft bake, 95^0 C 1 min on hot plate.

    6. Expose for 0.32 sec, set job offset to 18.

    7. Hot plate bake, 105^0 C 1 min.

    8. Flood Expose at 7.5 mW/cm^2 for 30 sec.

C. Development

    1. AZ 400K : D. I. = 1 : 5.5.

2. Develop for 40 sec.

3. Rinse in running D.I water, 3 min.

4. Blow dry with N_2.

5. Observe under the microscope. If there is a suspicion that some photoresist is remaining, then go back and develop for another 5 – 10 seconds.

D. Oxygen Plasma descum of Photoresist

4. 300 mT of O_2.

5. Power = 100 W at low frequency.

6. Run for 45 seconds.

E. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases/acid. Wear face shield at all times while at acid hood.

9. Mix a dilute solution of HCl : H_2O = 1 : 10.

10. Dip in dilute HCl for 15 sec.

11. Rinse in D.I. for 3 min.

12. Blow dry with N_2.

13. Put wafer on E-beam mount. Level it.

14. Put in a new crystal.

15. Pump down to below 1×10^{-6} Torr.

16. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec)	Approx. Vernier
a. Ti	25	1-2	1.65

b. SiO$_2$	300	1	1.85
c. NiCr	400	1.0	1.5

F. Lift-off: ***Do Not let Acetone dry on Wafer***

1. Soak wafer in beaker of Acetone until metal comes loose.

2. If the lift-off is stubborn, leave the wafer soaking overnight. Seal the top of the beaker with Aluminum foil.

3. Squirt Acetone using Acetone squirt bottles.

4. Rinse with Methanol, and then Isopropanol from the squirt bottles.

5. Rinse in running D.I. water for 3 min.

6. Blow dry with N$_2$.

7. Check under microscope and dektak for thickness of metal.

F.7   Metal-1 (Mask Layer: Metal-1)

A. Solvent Cleaning.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

2. Cold Acetone   3 min.

3. Hot Methanol   3 min.

4. Hot Isopropanol   3 min.

5. Running D.I.   3 min.

6. Blow dry with N$_2$.

7. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Photoresist application and exposure

Safety Note: The vapors from the photoresist are extremely harmful. Never

breathe if you put your head under the hood.

1. Cool down after dehydration, 5min.

2. Wafer on spinner with vacuum, blow with N_2.

3. Apply EIR AZ-5214 with syringe and filter to cover wafer.

4. Spin at 4.0 Krpm for 30 sec.

5. Soft bake, 95^0 C 1 min on hot plate.

6. Expose for 0.42 sec, set job offset to 18.

7. Hot plate bake, 105^0 C 1 min.

8. Flood Expose at 7.5 mW/cm^2 for 30 sec.

C. Development

1. AZ 400K : D. I. = 1 : 5.5.

2. Develop for 55 sec.

3. Rinse in running D.I water, 3 min.

4. Blow dry with N_2.

5. Observe under the microscope. If there is a suspicion that some photoresist is

   remaining, then go back and develop for another 5 – 10 seconds.

D. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

E. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of

concentrated bases/acid. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O = 1 : 10.

2. Dip in dilute HCl for 15 sec.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

5. Put the wafer on the rotating E-beam mount at an angle of 35^0 with respect

    to the metal sources. Rotate the wafer at about 15rpm.

6. Put in a new crystal.

7. Pump down to below 1 x 10^{-6} Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec)	Approx. Vernier
a. Ti	200	1-2	1.65
b. Au	9500	15	1.85
c. Ti	100	1.0	1.5

F. Lift-off: *Do Not let Acetone dry on Wafer*

9. Soak wafer in beaker of Acetone until metal comes loose.

10. If the lift-off is stubborn, leave the wafer soaking overnight. Seal the top of

    the beaker with Aluminum foil.

11. Squirt Acetone using Acetone squirt bottles.

12. Rinse with Methanol, and then Isopropanol from the squirt bottles.

13. Rinse in running D.I. water for 3 min.

14. Blow dry with N_2.

15. Check under microscope and dektak for thickness of metal.

F.8   SiN Etch (Mask Layer: SiN Via)

A. Solvent Cleaning.

    1. Wipe lower platen of the PECVD deposition chamber with ISO wipes. Careful its hot (~250^0 C).

    2. Run 60CLNSiN program to clean the chamber.

    3. Check the resistivity of the D.I. water. It should be > 17 MΩ.

    4. Cold Acetone   3 min.

    5. Hot Methanol   3 min.

    6. Hot Isopropanol   3 min.

    7. Running D.I.   3 min.

    8. Blow dry with N_2.

    9. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. SiN deposition and Photoresist application and exposure.

Safety Note: The vapors from the photoresist are extremely harmful. Never breathe if you put your head under the hood.

    1. Load wafer in the PECVD chamber. Run SiN25 (~2500 Å). Remember orientation.

    2. Unload the wafer. Rinse with ISO for 1 min.

3. Load wafer in the PECVD chamber. Rotate 90^0 from previous orientation. Run SiN15 (~1500 Å).

4. Unload the wafer and let it cool down for 5min.

5. Wafer on spinner with vacuum, blow with N_2.

6. Apply SPR 518-A with syringe and filter to cover wafer.

7. Spin at 4.0 Krpm for 30 sec.

8. Soft bake, 90^0 C 1 min on hot plate.

9. Expose for 0.9 sec, set job offset to 20.

10. Hot plate bake, 110^0 C 1 min.

C. Development

1. Develop in full beaker of MF-701 for 1 min. and 30 sec.

2. Rinse in running D.I water, 3 min.

3. Blow dry with N_2.

4. Observe under the microscope. If there is a suspicion that some photoresist is remaining, then go back and develop for another 5 – 10 seconds.

D. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 20 seconds.

4. Hardbake photoresist at 120^0C.

E. SiN Via RIE #3 Etch

1. Clean RIE#3 platen with ISO and clean wipes.

2. Pump down to lowE-5.

3. O_2 clean of the system as follows.

    a. O_2 flow rate = 20.0 sccm.

    b. chamber pressure = 10 mT.

    c. Voltage = 500 V.

    d. Minimize reflected power by tuning.

4. Load sample, pump down to at least 1 x 10^{-5} Torr.

5. Etch conditions.

    a. O_2 / SF_6 / Ar flow rate = 3.0 / 5.0 / 10.0 sccm.

    b. Chamber pressure = 20 mT.

    c. Voltage = 250 V.

    d. Minimize reflected power by tuning.

    e. Etch for 5 min (timed etch for 4000Å SiN).

6. Inspect under the microscope to ensure that the SiN vias are open. Else etch

    in RIE#3 in increments of 30 sec till all vias are clear.

F. Lift-off: ***Do Not let Acetone dry on Wafer***

1. Soak wafer in beaker of Acetone for 2 minutes.

2. Squirt Acetone using Acetone squirt bottles.

3. Rinse with Methanol, and then Isopropanol from the squirt bottles.

4. Rinse in running D.I. water for 3 min.

5. Blow dry with N_2.

6. Check under microscope and dektak for thickness of SiN.

F.9   Metal-2 (Mask Layer: Metal-2)

A. Solvent Cleaning

   1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

   2. Cold Acetone   3 min.

   3. Hot Methanol   3 min.

   4. Hot Isopropanol   3 min.

   5. Running D.I.   3 min.

   6. Blow dry with N_2.

   7.   Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Photoresist application and exposure

   Safety Note: The vapors from the photoresist are extremely harmful. Never

   breathe if you put your head under the hood.

   1. Cool down after dehydration, 5min.

   2. Wafer on spinner with vacuum, blow with N_2.

   3. Apply EIR AZ-5214 with syringe and filter to cover wafer.

   4. Spin at 4.0 Krpm for 30 sec.

   5. Soft bake, 95^0 C 1 min on hot plate.

   6. Expose for 0.42 sec, set job offset to 18.

   7. Hot plate bake, 105^0 C 1 min.

   8. Flood Expose at 7.5 mW/cm^2 for 30 sec.

C. Development

   1. AZ 400K : D. I. = 1 : 5.5.

2. Develop for 55 sec.

3. Rinse in running D.I water, 3 min.

4. Blow dry with N_2.

5. Observe under the microscope. If there is a suspicion that some photoresist is remaining, then go back and develop for another 5 – 10 seconds.

D. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

E. Evaporation

Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of concentrated bases/acid. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HCl : H_2O = 1 : 10.

2. Dip in dilute HCl for 15 sec.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

5. Put the wafer on the rotating E-beam mount at an angle of 35^0 with respect to the metal sources. Rotate the wafer at about 15rpm.

6. Put in a new crystal.

7. Pump down to below 1×10^{-6} Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec)	Approx. Vernier

a. Ti	200	1-2	1.65
b. Au	9500	15	1.85
c. Ti	100	1.0	1.5

F. Lift-off: ***Do Not let Acetone dry on Wafer***

1. Soak wafer in beaker of Acetone until metal comes loose.

2. If the lift-off is stubborn, leave the wafer soaking overnight. Seal the top of the beaker with Aluminum foil.

3. Squirt Acetone using Acetone squirt bottles.

4. Rinse with Methanol, and then Isopropanol from the squirt bottles.

5. Rinse in running D.I. water for 3 min.

6. Blow dry with N_2.

7. Check under microscope and dektak for thickness of metal.

F.10 BCB (Mask Layer: Metal-1)

A. Solvent Cleaning.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

2. Cold Acetone   3 min.

3. Hot Methanol   3 min.

4. Hot Isopropanol   3 min.

5. Running D.I.   3 min.

6. Blow dry with N_2.

7. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. BCB spin and cure

Safety Note: The vapors from BCB are extremely harmful. Never breathe if you put your head under the hood.

1. Turn N_2 flow up to maximum (100 sccm) in BlueM oven.

2. Wafer on spinner with vacuum, blow with N_2.

3. Apply AP-8000 with dropper to cover wafer.

4. Spin at 4.0 Krpm for 30 sec.

5. Blow dry with N_2.

6. Set spinner for 3.0 Krpm.

7. Apply BCB 57, spin at 4.5 Krpm for 30 sec.

8. Cure BCB in BlueM oven (Prog. 2) without petri dish cover. The base of the petri dish must be covered with Aluminum foil. The wafer is placed on top of the Aluminum foil.

C. SiN deposition and Photoresist application

1. Load the low temp SiN program in PECVD depositon system. Wait for the temperature to drop to 120^0 C.

2. Load wafer and RUN the low temp SIN deposition program to deposit approximately 1μm SiN.

3. Unload the wafer and let it cool down for 5 min.

4. Wafer on spinner with vacuum, blow with N_2.

5. Apply SPR-518A with syringe and filter to cover wafer.

6. Spin at 4.0 Krpm for 30 sec.

7. Soft bake, 90^0 C 1 min on hot plate.

8. Expose for 0.9 sec, set job offset to 40.

9. Hot plate bake, 110^0 C 1 min.

10. Flood Expose at 7.5 mW/cm^2 for 2 min.

D. Development

1. Develop in MF-701 for 1 min 30 sec.

2. Rinse in running D.I water, 3 min.

3. Blow dry with N_2.

4. Observe under the microscope. If there is a suspicion that some photoresist is remaining, then go back and develop for another 5 – 10 seconds.

E. Oxygen Plasma descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

G. SiN Via RIE #3 Etch

1. Clean RIE#3 platen with ISO and clean wipes.

2. Pump down to lowE-5.

3. O_2 clean of the system as follows.

   a. O_2 flow rate = 20.0 sccm.

   b. Chamber pressure = 10 mT.

   c. Voltage = 500 V.

    d. Minimize reflected power by tuning.

4. Load sample, pump down to at least 1×10^{-5} Torr.

5. Etch conditions.

    a. O_2 / SF_6 / Ar flow rate = 3.0 / 5.0 / 10.0 sccm.

    b. Chamber pressure = 20 mT.

    c. Voltage = 250 V.

    d. Minimize reflected power by tuning.

    e. Etch for 12 min (timed etch for 10000Å SiN).

6. Inspect under the microscope to ensure that the SiN vias are open. Else etch

    in RIE#3 in increments of 30 sec till all vias are clear.

H. Photoresist removal

1. Soak wafer in MF-701 for 2 min.

2. Rinse in running D.I. water for 3 min.

3. Blow dry with N_2.

4. Check under microscope and dektak for thickness of SiN.

I. BCBVia RIE #3 Etch

1. Clean RIE#3 platen with ISO and clean wipes.

2. Pump down to lowE-5.

3. O_2 clean of the system as follows.

    a. O_2 flow rate = 20.0 sccm.

    b. Chamber pressure = 10 mT.

    c. Voltage = 500 V.

d. Minimize reflected power by tuning.

4. Load sample, pump down to at least 1×10^{-5} Torr.

5. Etch conditions.

   a. O_2 / CF_4 flow rate = 3.0 / 12.0 sccm.

   b. Chamber pressure = 20 mT.

   c. Voltage = 250 V.

   d. Minimize reflected power by tuning.

   e. Etch for 30 min.

6. Unload wafer and inspect the Via under microscope to ensure the vias are open. Dektak the thickness of the Via.

7. Etch for additional 5 to 6 min with the following conditions to get 5.0μm.

   a. O_2 / CF_4 flow rate = 4/ 6 sccm.

   b. Chamber pressure = 20 mT.

   c. Voltage = 250 V.

   d. Minimize reflected power by tuning.

   e. Etch till the desired BCB thickness is achieved.

F.10   Bonding and Substrate removal

A. Solvent Cleaning of the carrier wafer.

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

2. Cold Acetone   3 min.

3. Hot Methanol   3 min.

4. Hot Isopropanol   3 min.

5. Running D.I.   3 min.

6. Blow dry with N_2.

7. Dehydration bake, 120^0 C, 30 min in petri dish without cover.

B. Sputtering of flash Ti/Au layer

1. Load the carrier wafer as well as the real wafer in the sputtering machine.

2. Pump down to 1E-6 Torr.

3. Set the Ar flow rate to 25 sccm.

4. Set chamber pressure to 10mT,power to 100 W. Sputter Ti for 5 min.

5. Cool down for 5 min.

6. Set chamber pressure to 10mT, power to 200 W. Sputter Au for 10 min.

7. Cool down for 10 min.

8. Unload both wafers.

C. Backside SiN deposition

1. Load the real wafer backside up, in the PECVD chamber.

2. Deposit 1000Å SiN on the backside of the real wafer (SiN10).

3. Unload the wafer.

D. Au plating: Plating conditions are 5mA, 2.5 Hours. Make sure no wires get

shorted in the process of carrying out the plating.

E. Bonding

1. Load the top chuck on the bonder. Clean both the chucks with ISO soaked

clean wipes.

2. Activate the pedestal VAC knob to hold the top chuck in place.

3. Place InP wafer on the upper chuck. GaAs wafer on the lower chuck.

4. Hit UP VAC, LO VAC to activate the vacuum for the upper and lower chucks.

5. Set upper and lower chuck temperatures to 180^0C.

6. Spread solder on the InP wafer.

7. Release LO VAC, get GaAs wafer and place it face down on the InP wafer.

8. Wet surfaces with In by dragging GaAs wafer around on InP wafer. After some time, check that GaAs and gold plated surfaces are completely covered with In.

9. Remove excess In with Q-tip, then move the wafers to the lower chuck.

10. Turn micrometer on side of bonder to ~ 5.

11. Turn top piece over, hit clamp (watch from side) then riser.

12. Wafer should be separated from the top chuck by a small gap now. Apply 400 grams or so of pressure by slowly turning the micrometer.

13. Set upper and lower chuck temperatures to 50^0C.

14. When chuck reaches 50^0C hit riser then clamp, then turn top piece over.

15. Get wafers clean up flip-chip bonder. Set chuck temperatures to 0^0C.

F. SiN removal

1. Remove SiN by immersing in buffered HF until SiN disappears.

2. 3 minute D.I. rinse.

G. InP substrate removal

1. Mix HCl:D.I., 3:1 in junk beaker.

2. Dip for 25 minutes or so. If there was polyimide on back of wafer, dip for 2 - 3 minutes, then try to scrape off polyimide. Repeat until polyimide is gone.

3. Mix another solution in InP etch beaker. Finish of the etch in that beaker.

4. Rinse in D.I. for 3 minutes.

F. Clean up

1. Test some base-emitter diodes.

2. Clean up edges of wafer with blade.

3. Dip for 30 seconds in 3:1 HCl : D.I, then 3 minute D.I. rinse.

F.11   Collector Contacts (Mask Layer: Collector)

A. No Solvent Clean

B. Photoresist application and exposure

Safety Note: The vapors from the Photoresist are extremely harmful. Never breathe if you put your head under the hood.

1. Configure collector job for mirror image. Enter the new alignment mark coordinates.

2. Measure the cell size along the x directions over 2 rows.

3. Find the average cell size along the x-axis and enter this new value in the stepper file.

4. Apply SPR 950-0.8 with syringe and filter to cover wafer.

5. Spin at 6 Krpm for 30 sec.

6. Soft bake 90^0 C, 1 min on hot plate.

7. Apply CEM with syringe and filter to cover wafer.

8. Spin at 6.0 Krpm for 30 sec.

9. Set system focus to 20.

10. Expose for 1.66 sec, set job offset to 34.

11. Change the system focus back to the original value.

G. Development

1. Post bake 100^0 C 2 min, 10 sec.

2. Rinse in D.I., for 30 sec.

3. Develop in MF-701 for 1 min,30 sec.

4. Rinse in running D.I water, 3 min.

5. Blow dry with N_2.

H. Oxygen Plasma Descum of Photoresist

1. 300 mT of O_2.

2. Power = 100 W at low frequency.

3. Run for 15 seconds.

I. Evaporation

   Safety Note: Wear Silver Shield gloves or equivalent when handling bottles of

   concentrated bases/acid. Wear face shield at all times while at acid hood.

1. Mix a dilute solution of HF : $H_2O = 1 : 10$.

2. Dip in dilute HF for 30 sec.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

5. Put wafer on E-beam mount. Level it.

6. Put in a new crystal.

7. Pump down to below 1×10^{-6} Torr.

8. Deposit material:

Material	Thickness (Å)	Dep. Rate (Å/sec)	Approx. Vernier
a. Ti	200	1-2	1.65
b. Pt	400	1	1.85
c. Au	4000	15	1.5

J. Lift-off: ***Do Not let Acetone dry on Wafer***

1. Soak wafer in beaker of Acetone until metal comes loose.

2. If the lift-off is stubborn, leave the wafer soaking overnight. Seal the top of the beaker with Aluminum foil.

3. Squirt Acetone using Acetone squirt bottles.

4. Rinse with Methanol, and then Isopropanol from the squirt bottles.

5. Rinse in running D.I. water for 3 min.

6. Blow dry with N_2.

7. Check under microscope and dektak for thickness of metal.

F.12   Collector recess etch

A. Solvent Cleaning

1. Check the resistivity of the D.I. water. It should be > 17 MΩ.

2. Cold Acetone   3 min.

3. Hot Methanol   3 min.

4. Hot Isopropanol   3 min.

5. Running D.I.   3 min.

6. Blow dry with N_2.

B. Collector recess etch

1. Mix etchant as follows: 55 ml of 1M citric acid in 220 ml D. I. Mix well.

    Add 5 ml H_2O_2. Mix well. Add 1 ml H_3PO_4. Mix well.

2. Stirring at 200 rpm etch for 1 min 30 sec. by suspending the wafer in a

    basket.

3. Rinse in D.I. for 3 min.

4. Blow dry with N_2.

END OF PROCESS.

Appendix G

Mask layout of the test structures

The base-emitter diode is shown

enlarged in Fig. G.2

SiN via

BCB via

Metal-1 (M1)

Metal-2 (M2)

Polyimide mesa

Base metal/mesa

Fig. G.1. Mask layout of the parallel base-emitter diode chain.

19 μm

15 μm

4.0 μm

M2 = 15 μm

Poly = 19 μm

L_e = 3.0 μm   M1 = 5.0 μm

3.5 μm   4.0 μm

Emitter (W_e = 1.0 μm)   Base metal/mesa   Metal-2 (M2)

Polyimide mesa   Metal-1 (M1)   BCB via (4 x 4 μm²)

Fig. G.2. Mask Layout of the transistor used in the series and parallel base-emitter diode chain.
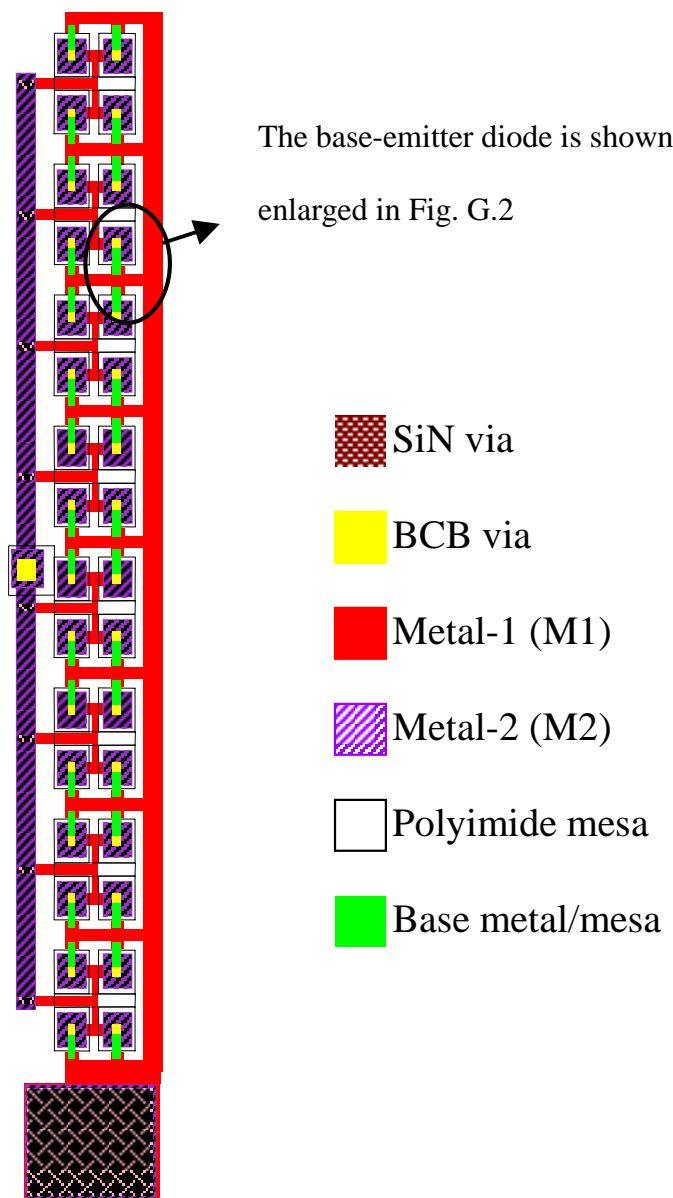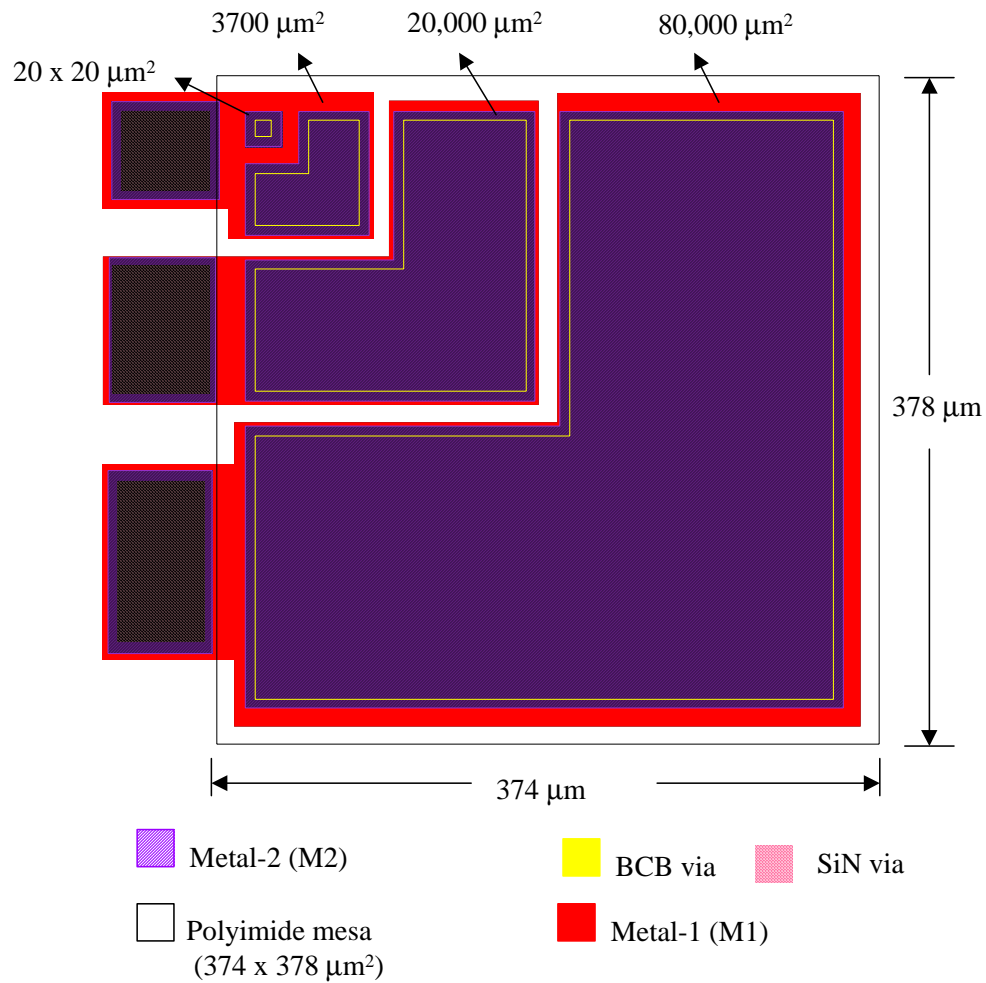
Fig. G.3. Mask Layout of the test structure used to evaluate the effect of polyimide roughness. The area of overlap between metal-2 and metal-1 was varied from 4000 μm^2 to 80,000 μm^2. The 3700 μm^2 and the 400 μm^2 structures share a common metal-1 pad. The metal-1-SiN-metal-2 structure sits on top of the polyimide mesa.
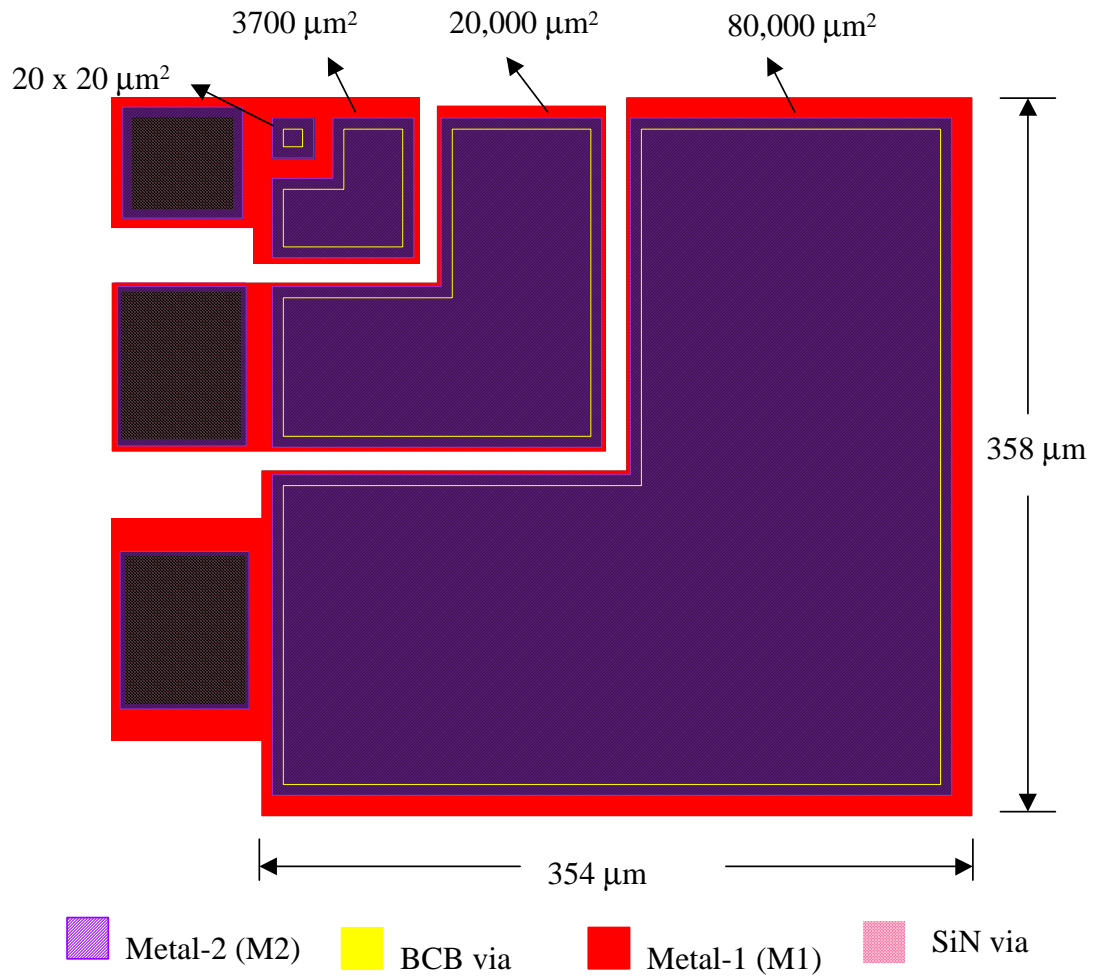
Fig. G.4. Mask layout used to evaluate the presence of SiN pin-holes. The area of overlap between metal-2 and metal-1 was varied from 4000 μm^2 to 80,000 μm^2.
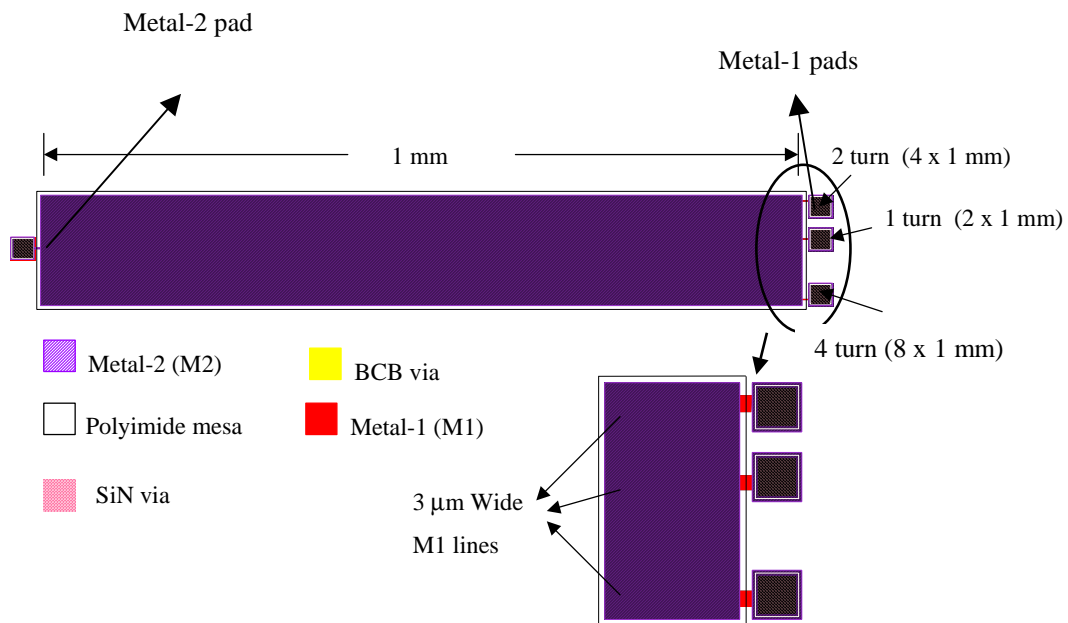
Fig. G.5. Mask layout used to evaluate the sidewall coverage of metal-1 lines by SiN. The circled area is shown enlarged. The narrow (3.0 μm wide) metal-1 lines are fully enclosed in metal-2. The length of the metal-1 line is varied from 2 mm to 8 mm. Each "turn" corresponds to a metal-1 line running along the length of the test structure and back.

The base-emitter diode is shown

enlarged in Fig. G.2

SiN via

BCB via

Metal-1 (M1)

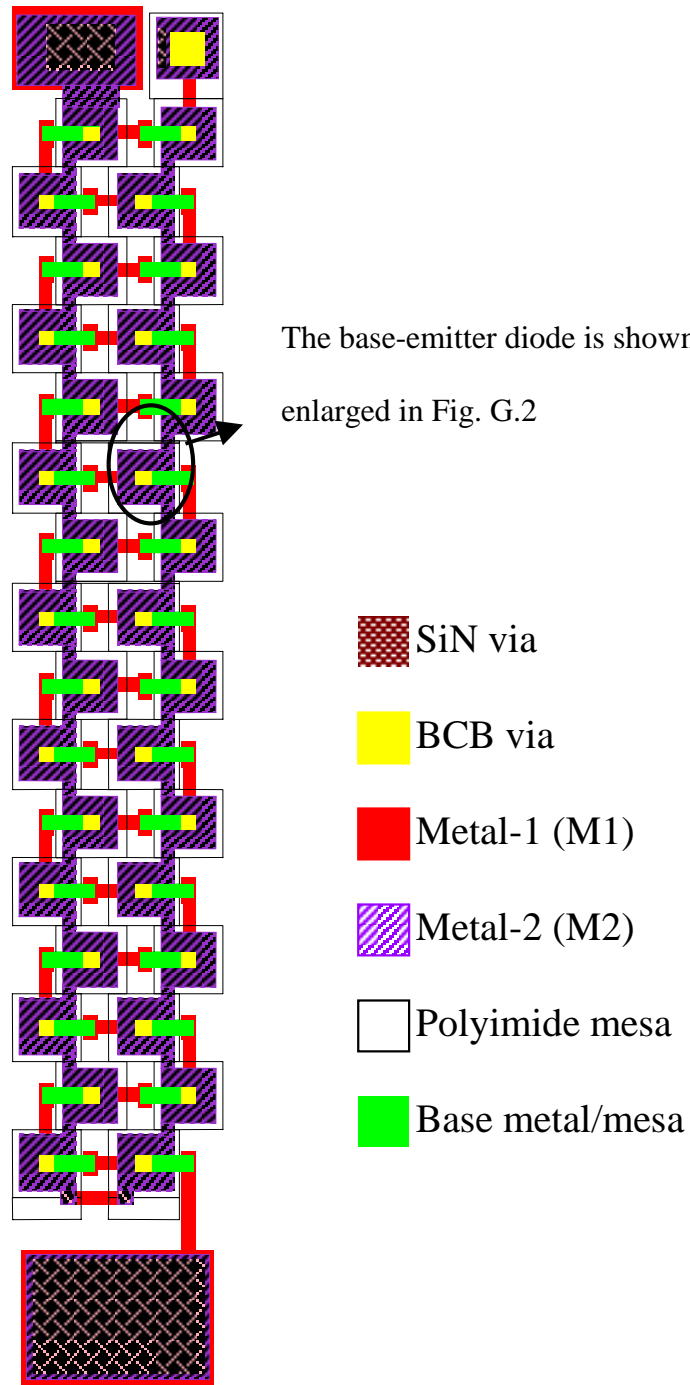Metal-2 (M2)

Polyimide mesa

Base metal/mesa

Fig. G.6. Mask layout of the series connected diode test structure.
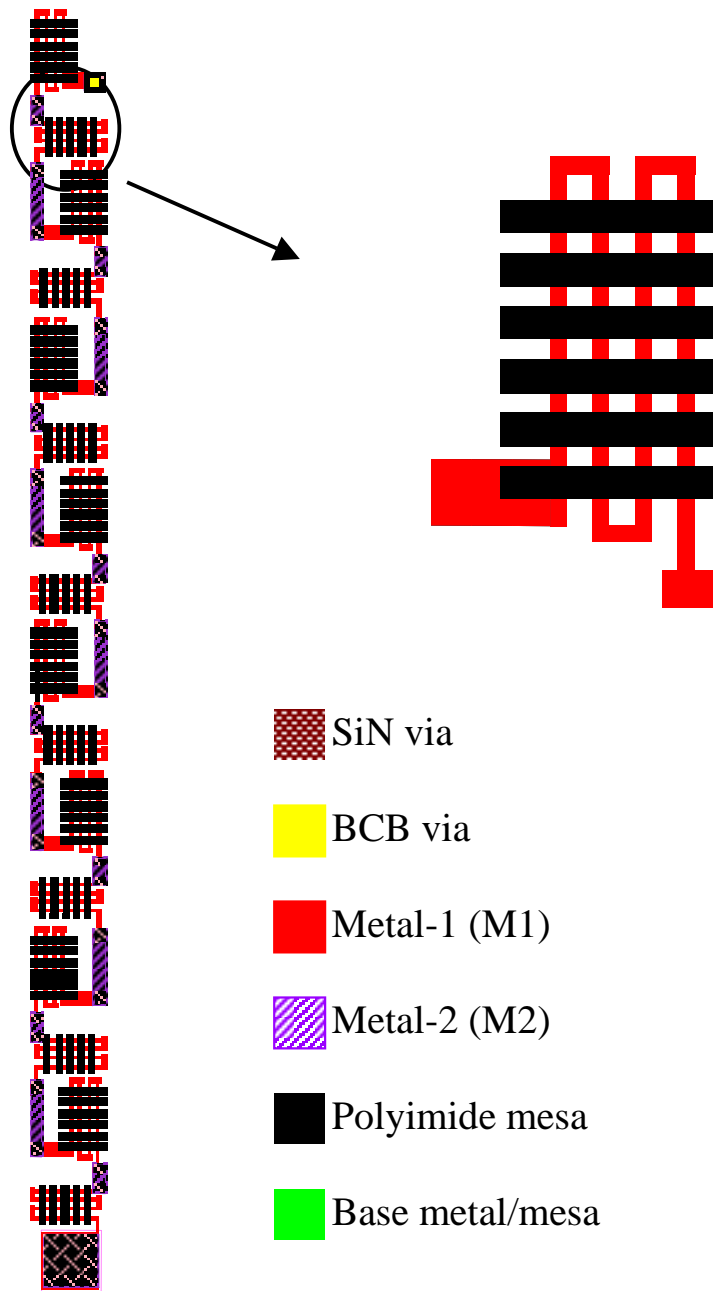
Fig. G.7. Mask layout of the test structure used to evaluate the step coverage of metal-1 lines over the polyimide mesa. The circled area is enlarged and shown in the figure. The metal-1 lines are 3.0 μm wide and run across approximately 80 polyimide mesas.

Legend:
- SiN via
- BCB via
- Metal-1 (M1)
- Metal-2 (M2)

Metal-1: 3 x 3 μm^2

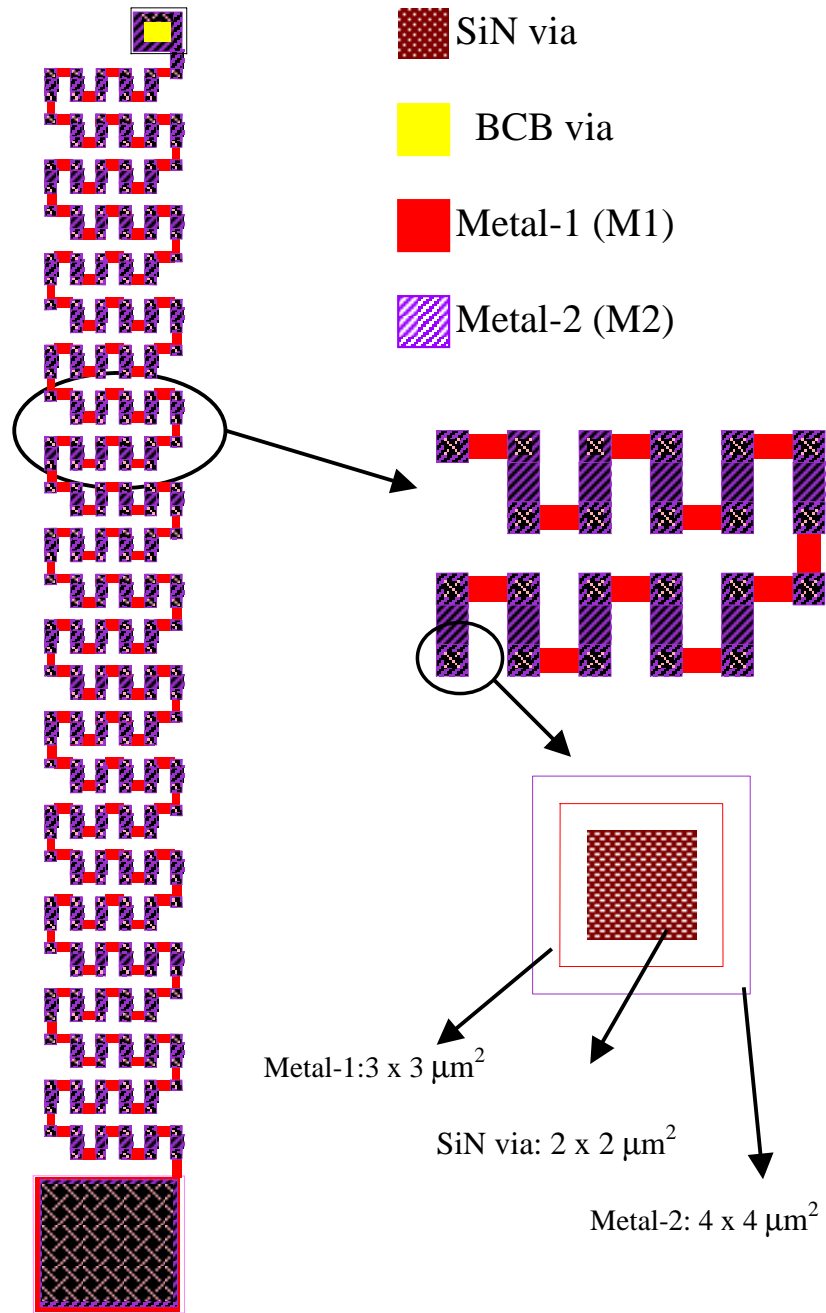SiN via: 2 x 2 μm^2

Metal-2: 4 x 4 μm^2

Fig. G.8. Mask layout of the test structure used to evaluate the uniformity of SiN via etch process. The circled areas are enlarged and shown in the figure along with the dimensions of the SiN via used.

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