UNIVERSITY of CALIFORNIA
Santa Barbara

High speed, manufacturable InP DHBTs and ICs with implanted collectors

A dissertation submitted in partial satisfaction of the
requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

Navin Parthasarathy

Committee in charge:

Professor Mark Rodwell, Chair
Professor Umesh Mishra
Professor Evelyn Hu
Dr. Bobby Brar

June 2006

The dissertation of Navin Parthasarathy is approved:

_____

_____

_____

_____
 Chair

August 2006

High speed, manufacturable InP DHBTs and ICs with implanted collectors

Copyright 2006

by

Navin Parthasarathy

Curriculum Vitæ
Navin Parthasarathy

EDUCATION

Master of Science (Hons.) in Physics
Birla Institute of Technology and Science, August 2000
Bachelor of Engineering (Hons.) in Electrical and Electronic Engineering
Birla Institute of Technology and Science, August 2000
Master of Science in Electrical Engineering
University of California, Santa Barbara, December 2002
Doctor of Philosophy in Electrical Engineering
University of California, Santa Barbara, April 2006

PROFESSIONAL EMPLOYMENT

2000 - 2005 Research assistant, Dept. of Electrical and Computer Engineering,
University of California, Santa Barbara
2006 Teaching assistant, Dept. of Electrical and Computer Engineering,
University of California, Santa Barbara

FIELDS OF STUDY

Major Fields: Physics of semiconductor devices, Design of high speed InP HBTs and technologies, Fabrication, Characterization and Modeling of InP based double heterojunction bipolar transistors (DHBTs) with implanted collectors
Design, fabrication and characterization of high static static frequency dividers

PUBLICATIONS

N. Parthasarathy, Z. Griffith, C. Kadow, U. Singisetti and M.J.W. Rodwell, "Collector-Pedestal InGaAs/InP DHBTs Fabricated in a Single-Growth, Triple-Implant Process", *IEEE Electron Device Letters*, vol. 52, no. 4, 2006.

N. Parthasarathy, C. Kadow, Z. Griffith, M.J.W. Rodwell, M. Urteaga, K. Shinohara, R. Pierson, B. Brar "Interface charge compensation in InP based Heterojunction Bipolar Transistors with implanted subcollectors", submitted to *Applied Physics Letters*, Feb. 2006.

N. Parthasarathy, Z. Griffith, C. Kadow, U. Singisetti, M.J.W. Rodwell, M. Urteaga, K. Shinohara, R. Pierson, B. Brar, "Selectively implanted subcollector DHBTs ", *IEEE conference on Indium Phosphide and Related Materials*, Princeton, New Jersey, May. 2006.

N. Parthasarathy, Z. Griffith, C. Kadow, M.J.W. Rodwell, M. Urteaga, K. Shinohara, R. Pierson, B. Brar, "Breakdown voltage enhancement in implanted pedestal-subcollector DHBTs", *Device Research conference*, College Station, Pennsylvania, Jun. 2006.

Z. Griffith, **N. Parthasarathy**, M.J.W. Rodwell, M. Urteaga, K. Shinohara, P. Rowell, R. Pierson, B. Brar, "An Ultra Low-Power ($\leq$ 13.6 mW/latch) Static Frequency Divider in an InP/InGaAs DHBT Technology", submitted to *IEEE MTT-S International Microwave Symposium*, San Francisco, California, Jun. 2006.

N. Parthasarathy, Y. DOng, D. Scott, M. urteaga, M. Rodwell, "Planar Device Isolation for InP based DHBTs", *2004 IEEE Device Research Conference*, Southbend, Indiana, Jun. 2004.

M. Rodwell, Z. Griffith, D. Scott, Y. Wei, Y. Dong, V. Paidi, M. Dahlström, **N. Parthasarathy**, C. Kadow, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, and C. Nguyen, "Transistor and Circuit Design for 100-200 GHz ICs", *IEEE Compound Semiconductor IC Symposium*, Monterey, CA, 24-27 October, 2004.

V. Paidi, Z. Griffith, Y. Wei, M. Dahlström, M. Urteaga, **N. Parthasarathy**, M. Seo,

L. Samoska, A. Fung, and M.J.W Rodwell, "G-Band (140-220 GHz) and W-Band (75-110 GHz) InP DHBT Medium Power Amplifiers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 598-605, 2005.

M. Rodwell, Z. Griffith, D. Scott, Y. Wei, Y. Dong, V. Paidi, M. Dahlström, **N. Parthasarathy**, C. Kadow, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, and C. Nguyen, "Transistor and Circuit Design for 100-200 GHz ICs", *IEEE Compound Semiconductor IC Symposium*, Monterey, CA, 24-27 October, 2004.

M. Urteaga, D. Scott, S. Krishnan, Y. Wei, M. Dahlström, Z. Griffith, **N. Parthasarathy**, and M. J. W. Rodwell, "G-band (140-220 GHz) InP-based HBT Amplifiers", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 9, pp. 1451-1456, 2003.

S. Krishnan, D. Scott, Z. Griffith, M. Urteaga, Y. Wei, **N. Parthasarathy**, and M. J. W. Rodwell, "An 8-GHz Continuous Time δ - σ Analog-Digital Converter in an InP-based HBT Technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 12, pp. 2555-2561, 2003.

Y. Wei, M. Urteaga, Z. Griffith, D. Scott, S. Xie, V. Paidi,**N. Parthasarathy**, and M. J. W. Rodwell, "75 GHz 80 mW InP DHBT Power Amplifier", *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, 8-13 June, pp. 919-921, 2003.

Abstract

High speed, manufacturable InP DHBTs and ICs with implanted collectors

by

Navin Parthasarathy

Novel HBT technologies have been designed and developed to enable continued scaling of InP based double heterojunction bipolar transistors(DHBTs), for their use in high speed, low power digital logic and mixed-signal systems. Significant reduction in parasitics have been achieved by the use of implanted subcollector and pedestal for independent collector scaling .

The base collector capacitance C_{cb}, contributes significantly to analog bandwidth and digital delay and must be reduced as DHBTs are scaled. Two different types of InP double heterojunction bipolar transistors have been designed, fabricated and charcterized employing Fe and selective Si implants to decrease C_{cb}. The first type, the selectively implanted subcollector DHBT, has a shallow Fe implant to compensate regrowth interface charge and a Si implant to form the subcollector. This selective implant eliminates the parasitic base collector capacitance associated with the base access pad area. These devices exhibit 361 GHz f_τ and 404 GHz f_{max}. A second device, the implanted pedestal-subcollector DHBTs allows for further reduction of C_{cb}. It has a thicker Fe implanted semi-insulating layer for reduced C_{cb} in the ex-

trinsic collector-base junction, a patterned buried subcollector formed by a deep Si implant and an collector pedestal created by a second Si implant. These InP pedestal HBTs have 352 GHz f_τ and 403 GHz f_{max}. The implanted pedestal-subcollector DHBTs have a DC current gain $\beta \approx 35$ and $BV_{CBO} \approx 7.8$ V. In addition to the compensation by the Fe implant of charge at the epitaxial growth interface, these two processes provide the following enhancements: elimination of C_{cb} in the base interconnect pad area, a single MBE growth and increased wafer planarity. In this first demonstration of these two processes, the f_τ and f_{max} are the highest reported for DHBTs with implanted collectors. Using these implanted collector processes, record low power delay products have been obtained for CML dividers operating at over 61 GHz with an operating power of less than 27mW. High speed CML stativ frequency dividers clocking to 135 GHz have been measured. ECL dividers utilizing implanted collectors have a self oscillation frequency of 96 GHz. There is a 20 % improvement in logic speed using this technology.

For high speed logic circuits, emitter resistance is an important parameter to be reduced. Highly scaled emitter junctions with simultaneously large emitter contacts, and thick extrinsic bases have been demonstrated with an emitter regrowth technology. These have attained 280 GHz f_τ.In conjunction with the implanted collector process, these InP DHBTs can attain a bandwidth of over 1 THz.

To

my Mother, Father and Ammu

Contents

List of Figures

List of Tables

1

Introduction

HIGH performance, manufacturable transistors are required for significant improvements in the bandwidth, dynamic range, power consumption and integration level of mixed-signal ICs used in military radar and communications transmitters. Large integration scales, $\approx$ 20,000 transistors, will be needed to realize complex signal processing functions, and power per gate must be accordingly reduced to achieve acceptable thermal densities for reliable device operation. Future microwave DACs and DDFS ICs will operate at 100-200 GHz clock speeds and will contain 10^4 - 10^5 transistors. This requires a breakthrough in combined IC speed and integration scales.

Despite tremendous advancements in CMOS technology, bipolar transistors remain competitive owing to larger breakdown voltages obtainable and more tolerant lithographic dimensions at a given bandwidth. SiGe and InP heterojunction transistors (HBTs) are the main competing high speed IC technologies. InP heterojunction transistors benefit from high carrier mobilities and saturated velocities and are compatible for integration with 1.3 - 1.5 μm optoelectronic components such as lasers and photodetectors [1]. SiGe HBTs have smaller junction dimensions and smaller extrinsic parasitics due to the maturity of the advanced silicon processes. Consequently, digital circuit speed in SiGe and InP has been comparable [2], with SiGe offering higher integration scales. Further scaling of InP HBTs is therefore important, and with the adoption of advanced SiGe-like fabrication processes, large potential improvements in speed and yield of InP HBTs are possible. InP HBT processes utilizing $\approx$ 500 nm width emitter junctions (W_e) and 500 nm width base contacts (W_b) have demonstrated 350 GHz f_τ, 400 GHz f_{max} and 150 GHz static frequency dividers [3, 4].

For $\approx$ 2:1 improvement in bandwidth, the collector layer must be thinned 2:1 and the base thinned $\sqrt{2}$:1. The operating current density must be increased 4:1 and the emitter resistance per unit emitter junction area reduced 4:1. Emitter and collector junction widths must both decrease 4:1. If the base contacts lie above

the active collector-base junction, the contact width and the contact resistivity must both decrease 4:1 [5]. In addition to difficulties in reducing contact resistivity, very narrow base contacts present challenges in process design for high yield fabrication and present significant bulk metal resistance along the length of the contact. Further, the parasitic base interconnect pad capacitance becomes a significant fraction of the total in small-area HBTs used in low-power logic.

This work describes InP DHBTs that address the above scaling issues and suggests a restructuring of the III-V fabrication scaling process to closely follow the Si/SiGe techniques. Fabrication steps have been developed aimed at improving the performance and manufacturability of a submicron InP DHBT device. The device epitaxy has been tailored to support a submicron process, with device parameters that are optimized for high digital logic speeds and not necessarily traditional transistor figures-of-merit (f_τ, f_{max}). Work has been presented on two unique device topolgies.

The first topology is a selectively implanted subcollector and pedestal HBT technology. Scaling of the collector base junction is achieved by the by the use of Fe and selective Si implants. DHBTs with implanted subcollector DHBTS are fabricated where the the parasitic capacitance associated with the area of the base access pad $C_{cb,pad}$, is eliminated. A reliable method for compensating the charge associated with the InP growth interface is also demonstrated. Further reduction in extrinsic collector base capacitance C_{cb}, is achieved by the addition of a selectively implanted pedestal in the second device topology. InP DHBTs employing a buried N^{++} sub-collector and N^+ collector pedestal formed fully by ion implantation are demonstrated. This novel DHBT structure provides the following enhancements over the existing pedestal InP DHBTs [6, 7]: reduced extrinsic C_{cb} associated with the pedestal, compensation of charge at the epitaxial growth interface, elimination of C_{cb} in the base interconnect pad area, a single MBE growth and increased wafer planarity and hence potentially improved yield in the fabrication of large circuits. In this first demonstration of the fully implanted pedestal-subcollector DHBTs, the f_τ and f_{max} are a record for transistors with implanted collectors.

This thesis is logically structured to explain the steps taken towards a SiGe-like highly scaled, manufacturable InP HBT. Chapter 2 discusses the basic theory and design of an InP based DHBT. Scaling laws for increasing HBT and digital IC bandwidth, and physical limits to scaling are presented. Chapter 3 presents the theory of ion implantation in InP and discusses the design of Silicon (Si) and Iron (Fe) implants in InP. The results pertaining to Si and Fe implants and high temperature annealing of InP are presented. Chapter 4 may be considered as two parts. In the first half, device results are presented for a DHBT with implanted subcollectors formed by a single Si implant. The effect of growth interface charge is shownand and an approach to eliminate this is proposed and developed. The second half, disc-

cuses the fabrication and device results of implanted subcollector DHBTs with two ion implants are discussed. Chapter 5 describes in depth the design and performance of the implanted pedestal-subcollector DHBT. Chapter 6 summarises the research effort and outlines directions for future work.

References

[1] "Properties of INDIUM PHOSPHIDE", *INSPEC Electron EMIS Datareviews Series No 6*, 1991.

[2] M. Khater, J.-S. Rieh, T. Adam, A. Chinthakindi, J. Johnson, R. Krishnasamy, M. Meghelli, F. Pagette, D. Sanderson, C. Schnabel, K.T. Schonenberg, P. Smith, K. Stein, A. Stricker, S.-J. Jeng, D. Ahlgren, and G. Freeman, "SiGe HBT Technology with f_{max} / f_τ = 350/300 GHz and gate delay below 3.3 ps", *Proc. IEEE Int. Electron Device Mtg*, San Francisco, CA, Dec. 13-15, 2004, pp. 247-250.

[3] M. Le, R. Hess, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee. J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J.W. Lai, M. Feng, "Self-aligned InP DHBTs for 150 GHz digital and mixed signal circuits" *International Conference on Indium Phosphide and Related Materials*, Glasgow, Scotland, May 8-12, 2005, pp. 325-330.

[4] M. Urteaga, P. Rowell, R. Pierson, B. Brar, M. Dahlström, Z. Griffith, M. J. W. Rodwell, S. Lee, N. Nguyen, and C. Nguyen, "Deep Submicron InP DHBT Technology with Electroplated Emitter and Base Contacts", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 239-240.

[5] M.J.W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S.C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. I. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlström. "Submicron Scaling of HBTs" *IEEE Trans. on Electron Devices*, Vol. 48, pp. 2606-2624, November 2001.

[6] Y. Dong, Z. Griffith, M. Dahlström, and M.J.W. Rodwell, "C_{cb} reduction in InP heterojunction bipolar transistors with selectively implanted collector pedestal", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 67-68.

[7] J.C. Li, M. Chen, D.A. Hitko, C.H. Fields, B. Shi, R. Rajavel, P.M. Asbeck, M. Sokolich, "A submicrometer 252 GHz f_τ and 283 GHz f_{max} InP DHBT with reduced C_{BC} using selectively implanted buried subcollector (SIBS)", *IEEE Electron Device Letters* , Vol. 26, no. 3, pp. 136-138, March 2005

2

InP DHBT Theory and Design

ADVANCES in the design and fabrication of InP heterojunction bipolar transistors have been made at UCSB since 1994. In this chapter, the InP HBT layer structure and HBT scaling laws are presented. The transit times, resistances and capacitances are examined. The various transistor figures-of-merit are described. The delays associated with a digital latch, regularly employed as retiming elements and decision circuits is derived. Lastly, device modeling and scaling limits are discussed.

2.1 Emitter
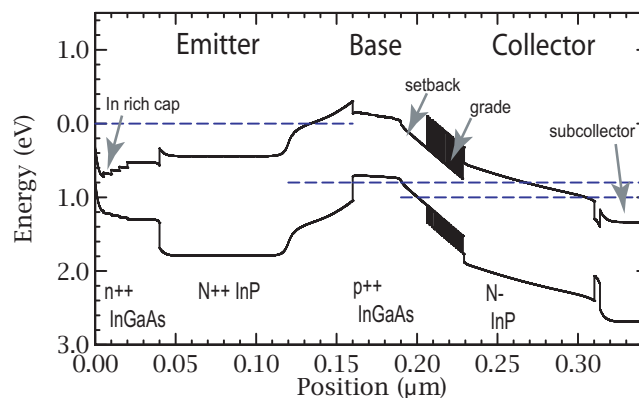
Figure 2.1: Energy band diagram of a typical HBT with V_{be} =0.9V and V_{cb} =0.2V

The band diagram of a typical NpN InP based DHBT is shown in Fig. 2.1. Under normal operation, the emitter base junction is forward biased. This lowers the emitter base potential and injects electrons into the base. As seen in Fig. 2.2, the emitter layer stack consists of very highly doped $In_xGa_{1-x}As$ used as the contact

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
5	$In_{0.85}Ga_{0.15}As$	$> 5 \cdot 10^{19}$:Si	Emitter cap
15	$In_{x}Ga_{1-x}As$	$4 \cdot 10^{19}$:Si	Emitter cap
20	$In_{0.53}Ga_{0.47}As$	$3 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$8 \cdot 10^{17}$:Si	Emitter
40	InP	$5 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$4 - 7 \cdot 10^{19}$:C	Base
15	$In_{0.53}Ga_{0.47}As$	$3.25 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$3.25 \cdot 10^{16}$:Si	B-C grade
3	InP	$2.75 \cdot 10^{18}$:Si	Delta doping
78	InP	$3.25 \cdot 10^{16}$:Si	Collector
5	InP	$1.5 \cdot 10^{19}$:Si	Sub-collector
6.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$:Si	Sub-collector
300	InP	$2 \cdot 10^{19}$:Si	Sub-collector
Substrate	Semi-Insulating InP		

Figure 2.2: Layer structure of a typical UCSB mesa-DHBT

layer and a N^- InP emitter. The InP-InGaAs base emitter heterojunction can be abrupt or graded. The DC current gain of a graded junction is higher than that of an abrupt junction since the hole barrier is larger. The ratio of emitter current between an abrupt and a graded emitter junction is

$$\frac{I_{E,abrupt}}{I_{E,graded}} \simeq exp\left(-\frac{\Delta E_c}{kT}\right) \qquad (2.1.1)$$

where ΔE_c is the conduction band discontinuity between InP and $In_{0.53}Ga_{0.47}As$ of the base. However grading presents many challenges and the base-emitter grade design is not straightforward for the forward biased junction [1]. It can be argued that for an abrupt emitter-base junction, the electrons that surmount the barrier are injected with a substantial kinetic energy roughly equal to ΔE_c. This kinetic energy corresponds to a high velocity which influences the base and collector transit times [2]. Besides the choice between a graded and abrupt base-emitter heterojunction, the 3 parameters about the emitter design are the InP emitter layer thickness (X_E), doping level (N_E) and the choice of emitter cap. X_E and N_E influence the base-

5

emitter junction capacitance. C_{je} per unit area is given by

$$C_{je} = \frac{\epsilon_{InP}}{X_{dep,E}} \simeq \frac{\epsilon_{InP}}{\sqrt{\frac{2\epsilon_{InP}}{qN_E}(\phi_{BE} - V_{BE})}} \qquad (2.1.2)$$

C_{je} is not purely a depletion capacitance and making $X_{dep,E}$ (or X_E) large fails in the limit of large depletion thicknesses. The emitter base junction capacitance C_{je} can also be given by,

$$C_{je} = C_{je1} + C_{je2} = \frac{\epsilon_{InP}L_eW_e}{X_{dep,E}} + \kappa X_{dep,E}T_bI_c \qquad (2.1.3)$$

where T_b is the base thickness and κ is a constant. If the current density is increased, while maintaining constant $X_{dep,E}$, the stored mobile electron charge is increased. It can be shown that the ideality factor η is,

$$\eta = 1 + \frac{1}{q}\frac{\partial(\Delta E_{fn,eb})}{\partial V_{be}} \qquad (2.1.4)$$

where $\Delta E_{fn,eb}$ is the change in quasi-Fermi energy due to recombination at the base-edge of the emitter. To maintain a high current density without significant voltage drop in the base-emitter depletion region, a high electron density is to be maintained. However, to obtain obtain a low ideality factor, the electron concentration in the depletion region must be kept high while keeping the thickness of the depletion region small. The emitter charging time $\tau_e = (kT/\eta qI_c) \cdot C_{je}$ is one of the major delay components determining f_τ and maximum digital logic speed [3].

The delay term $R_{ex} C_{cb}$ is a major limit to HBT scaling and R_{ex} degrades the digital noise margin. The emitter layer structure consists of a heavily doped and narrow bandgap contact layer (cap), a highly doped N^{++} wide bandgap emitter and a low doped N^- emitter of thickness X_E and doping N_E. If the heterointerfaces are designed properly to avoid conduction band barriers between layers, and if the thicknesses of the N^{++} layers are not significantly larger than X_E, the parasitic emitter resistance is determined mostly by the contact resistance between the metal and the semiconductor and the resistance in the undepleted portion of the N^- emitter. The emitter resistance for a standard mesa DHBT is then given by

$$R_{ex} \simeq \frac{\rho_{c,e}}{L_eW_{ec}} \qquad (2.1.5)$$

where $\rho_{c,e}$ is the emitter specific contact resistivity and ρ_{e1},is the bulk resistivity of the N^- emitter layer and the other dimensions are as shown in Fig. **??**. For submicron junctions, the junction width W_{ej} is smaller than the contact width due

to the lateral undercutting during the wet etching of the emitter. Surface depletion of the N^- layer further reduces the width of the electrically active junction. An undoped emitter is reported [4] to provide a higher f_τ at a given current density J_c. However, low doping leads to higher emitter charging times at high current densities.

2.1.1 Emitter Resistance

The emitter resistance is primarily determined by the ohmic contact resistance ρ_c. The ohmic resistivity ρ_c is,

$$\rho_c \propto \exp\left[\frac{\Phi_B}{N^{\frac{1}{2}}}\right] \tag{2.1.5}$$

The resistivity is proportional to the barrier height Φ_B and the doping of the emitter cap [5]. The resistivity can be reduced by using a highly doped, low bandgap semiconductor as the emitter cap. For the DHBTs described here, the emitter cap is $In_{0.85}Ga_{0.15}As$ which has a lower band gap than $In_{0.53}Ga_{0.47}As$. These are doped at over 3×10^{19} cm^{-3}. The maximum doping is limited by the solid solubility of Si dopants in $In_{0.85}Ga_{0.15}As$. The thickness of the emitter cap is 40 nm. This is limited by the Matthews-Blakeslee critical limit for strained $In_{0.85}Ga_{0.15}As$ growth. Furthermore, the cap is kept thin to prevent excessive undercut of the $In_{1-x}Ga_xAs$ layers during the emitter wet etch.

2.2 Base

The base-emitter turn on voltage is approximately the built in potential and for the abrupt emitter-base junction used in the designs in this thesis is given by,

$$\phi_{bi} = \frac{E_{gb} + \Delta E_c - \phi_p - \phi_n}{q} \tag{2.2.0}$$

E_{gb} is the bandgap of of the base layer. Ignoring high doping effects, E_g is ≈ 0.76 eV for $In_{0.53}Ga_{0.47}As$, ΔE_c is the conduction band offset to InP ≈ 0.26 eV. ϕ_p is the hole quasi Fermi level in the base with respect to the valence band and ϕ_n is the electron quasi Fermi level in the emitter with respect to the conduction band. For non-degenerately doped semiconductors, these electron and hole quasi Fermi levels are described by,

$$\phi_n = E_c - E_{fn} \tag{2.2.1}$$
$$\phi_p = E_{fp} - E_v \tag{2.2.2}$$

The p^{++} $In_{0.53}Ga_{0.47}As$ base is usually between 20-100nm and doped well over $10^{19}cm^{-3}$. The electron and hole currents in the base are,

$$J_n = \mu_n \frac{d}{dx} \phi_n \tag{2.2.3}$$

$$J_p = \mu_p \frac{d}{dx} \phi_p \tag{2.2.4}$$

The hole current should be very small ≈ 0 in a well designed bipolar transistor. The following generalized Moll-Ross current relation for a bipolar transistor with a non-uniform base is derived by Kroemer [6] as

$$J_n \approx -\frac{q \cdot exp(\frac{qV_{be}}{kT})}{\int_{base}[p/D_n \cdot n_{ib}^2]\, dx} \tag{2.2.4}$$

Here, D_n is the electron diffusivity in the base and n_{ib} is the intrinsic carrier concentration in the base.

The time it takes for an electron entering from the emitter to traverse across the base is the base transit time and can be expressed as,

$$\tau_b = \frac{Q_B}{I_n} = \frac{\int_0^{T_b} q \cdot n(x)\, dx}{J_n} \tag{2.2.4}$$

where T_b is the base thickness. When the electron transport is purely diffusive, the transit time is classically given by,

$$\tau_b = \frac{T_b^2}{2D_n} \tag{2.2.4}$$

This transit time calculation assumes uniform composition and doping in the base. To reduce τ_b, an electric field can be established in the base to so that electron transport is aided by the drift field [7]. If the grading of the base conduction band is linear, Equ. 2.2 is rewritten as,

$$\tau_b = \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right)\left[1 - \frac{kT}{\Delta E}\left(1 - \exp^{-\Delta E/kT}\right)\right] \tag{2.2.4}$$

where ΔE is the potential due to grading across the base. The grading may be done compositionally to vary the base bandgap or by varying the base doping. The HBTs presented in this work employ a doping grade producing a $\Delta E \sim 50$ meV. This in turn reduces τ_b by $\sim 50\%$ compared to an ungraded base. For transistors with very

thin bases operating at high current densities, Shockley's boundary conditions cases to be valid

$$\tau_b = \frac{T_b^2}{D_n}\left(\frac{kT}{\Delta E}\right)\left[1 - \frac{kT}{\Delta E}\left(1 - \exp^{-\Delta E/kT}\right)\right] + \frac{T_b}{v_{exit}}\left(\frac{kT}{\Delta E}\right)\left(1 - \exp^{-\Delta E/kT}\right)$$

(2.2.4)

The T_b/v_{exit} contribution is usually ignored by assuming that the electron concentration at the collector side of the base is zero. For a thin base this assumption is not valid and the correction term accounts for the finite electron concentration that exits the base. For bases thicker than 20nm, the base transit time $\tau_b \sim T_b^2$, while for bases thinner than 20nm, the base transit time $\tau_b \sim T_b$.

The base current components in a well designed HBT consists of bulk recombination current, surface recombination current, emitter-base space charge recombination current. These components need to be minimised to increase the current gain of the transistor. The surface recombination current is directly proportional to the emitter periphery. Unlike the GaAs surface, the free $In_{0.53}Ga_{0.47}As$ has a much lower surface recombination velocity of $\sim 1 \times 10^3 cm/s$. Further, BCB is used for device passivation and reduces the surface leakage current, compared to polyimide or Si_xN_y [8]. The base current is dominated by Auger recombination in the bulk. The Auger recombination rate is given as

$$U_A = C(n + p)(np - n_i^2) \approx (CN_A^2) \cdot \Delta n = \frac{\Delta n}{\tau_r}$$

(2.2.4)

where C is the Auger recombination co-efficient and Δn is the excess electron concentration in the base and τ_r is called the recombination lifetime and is a material parameter. The current gain can now be expressed as

$$\beta = \frac{\tau_n}{\tau_r}$$

(2.2.4)

The current gain is thus inversely proportional to the base thickness and the base doping. Reducing the base thickness and base doping however increases the base resistance and impacts the f_{max} of the bipolar transistor. The base resistance for a two sided base contact is given by,

$$R_{bb} = R_{bb,contact} + R_{bb,gap} + R_{bb,spread}$$

(2.2.5)

$$R_{bb,contact} = \frac{\sqrt{\rho_c \cdot R_{sh,b}}}{2L_E}\coth\frac{W_B}{L_T} \text{ where, } L_T = \sqrt{\rho_c/R_{sh,b}}$$

$$R_{b,gap} = R_{sh,b}\frac{W_{gap}}{2L_E} \text{ and } R_{b,spread} = R_{sh,b}\frac{W_E}{12L_E}$$

$$R_{bb} = \frac{1}{2}\frac{R_{sh,b}}{L_e}\left[L_t\coth\frac{W_b}{L_t} + W_{gap} + \frac{W_e}{6}\right]$$

(2.2.4)

where ρ_c ($\Omega \cdot \mu\text{m}^2$) and $R_{sh,b}$ ($\Omega/\square$) are the specific contact resistivity and sheet resistance of the base, and L_T is called the ohmic transfer length. The base contact resistance is $\propto L_T$. Therefore, scaling down the base-collector junction laterally increases the base resistance exponentially as seen in Eqn. 2.2.4. The base resistance is usually higher than the emitter and collector resistances due to the heavier effective mass and lower mobility of the hole.

When current is flowing through the device, an important reduction of extracted value of R_{bb} is observed as seen on Fig. 2.10 in §**??**. This decrease of R_{bb} is due to decrease in $R_{bb,spread}$, attributed to electron injection in intrinsic base [**?**]. If average electron velocity in the is about 3×10^7 cm/s, an emitter current density of 2 $mA/\mu\text{m}^2$ induces an electron concentration of 4×10^{16} ρ_c. This modifies the resistivity in the intrinsic base, due to the high electron mobility in p^{++} $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ of $\sim 3000 \, cm^2/V \cdot s$, compared to the hole mobility of $\approx 40 \, cm^2/V \cdot s$.

2.3 Collector

The collector design is critical to the performance of high speed transistors. There are breakdown advantages when the collector layer is made of a widegap material. In InP/InGaAs DHBTs, there is a discontinuity in the conduction band between the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ base and the InP collector layers. In order to prevent blocking of current, this discontinuity is removed by grading the energy gap from the base to the collector. The collector layer is thus a composite structure consisting of a $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ setback, a $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$- InP grade and wide bandgap InP collector as seen in the energy band diagram in Fig. **??**. The base-collector grading can be accomplished in one of two ways

- $\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$quaternary lattice matched to InP. By varying the ratio of the Group V element (As, P), from y=1 $\rightarrow$ y=0, the energy band is progressively graded from $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ to InP [9]. This is particularly convenient for MOCVD growth.

- InGaAs/InAlAs super-lattice grade with intermediate effective bandgap [10]. A chirped superlattice of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ is form results in delocalised electron states resulting in an effective bandgap. The periodicity has to be kept small, compared to the electron wavelength, to prevent electron reflection. In all the designs described in this thesis, the super lattice period is 1.5nm.

The electric field due to the grade, given by $\Delta E_c/T_{grade}$, opposes the built-in field. Two δ doping layers at the end of the grading length T_{grade}, acceptor at the base end

and donor at the collector end forms a dipole that cancels out the electrostatic field due to the grade [11]. The sheet charge density of this doping layer is given by

$$N_\delta T_\delta = \frac{\varepsilon_o \varepsilon_r \Delta E_c}{q^2 \cdot T_{grade}}$$

(2.3.0)

where N_δ and T_δ are the doping concentration and thickness of the δ layer. A setback layer of N-type $In_{0.53}Ga_{0.47}As$ is usually inserted between the base and the grade. This layer serves to ensure that have electrons have sufficient kinetic energy before entering the grade [10]. The potential drop in the setback layer, $\Delta\phi_{setback}$, can be a significant fraction of ϕ_{bi} which could result in lower breakdown. A rule of thumb is to design the setback such that $\Delta\phi_{setback} = \Delta E_c$. The rest of the collector consists of wide bandgap InP. The doping in the collector is chosen so that the collector is fully depleted at zero bias. To ensure full depletion in the collector at zero bias,

$$\phi_{bi} \geq \frac{qN_c(T_{setback} + T_{grade})^2}{2\varepsilon_o\varepsilon_r} + \frac{qN_\delta T_\delta(T_{setback} + T_{grade})}{\varepsilon_o\varepsilon_r} + \frac{qN_c T_{InP}^2}{2\varepsilon_o\varepsilon_r} - \frac{T_{grade}\Delta E_c}{q}$$

(2.3.0)

where $T_{setback}, T_{grade}$ and T_{InP} are the thicknesses of the setback, grade and InP layers respectively. N_c is the doping of the collector. From this expression the maximum allowable collector doping to ensure full collector depletion is,

$$N_{c,max} \approx \frac{1}{T_{InP}^2}\left[\frac{2\varepsilon_o\varepsilon_r}{q}(\phi_{bi} - \Delta\phi_{setback} - \Delta\phi_{grade})\right]$$

where $\Delta\phi_{setback}$ and $\Delta\phi_{grade}$ are the potential drops in the setback and grade layers. The potential dipole reduces the maximum collector doping significantly.

The transit time for an electron to through the collector is given by

$$\tau_c = \int_0^{T_c} \frac{1 - x/T_c}{\upsilon(x)}\, dx \equiv \frac{T_c}{2\upsilon_{eff}}$$

where τ_c is the collector transit time, $\upsilon(x)$ and υ_{eff} are the position-dependent and effective electron velocities in the collector drift region.

The subcollector layer is 300 nm of Si doped N^{++} InP. The subcollector is designed to reduce the collector resistance. The expression for collector resistance of a standard mesa DHBT, for a two sided collector contact is,

$$R_c = R_{c,contact} + R_{c,gap} + R_{c,spread}$$

(2.3.0)

$$R_c = \frac{1}{2}\frac{R_{sh,s}}{L_e}\left[L_t + W_{c,gap} + \frac{W_{cb}}{6}\right]$$

11

where ρ_c ($\Omega \cdot \mu\text{m}^2$) and $R_{sh,s}$ ($\Omega/\square$) are the specific contact resistivity and sheet resistance of the sub-collector, W_{cb} is the width of the collector mesa, $W_{c,gap}$ is the spacing between the collector mesa and contact, L_e is the emitter junction length, and L_t is the ohmic transfer length equal to $\sqrt{\rho_c/\rho_s}$. R_{gap} and $R_{c,spread}$ are reduced by decreasing the sheet resistance of the subcollector which can be expressed as

$$R_{sh,s} = \frac{1}{q\mu_n \cdot N_{sc} \cdot T_{sc}} \tag{2.3.0}$$

where T_{sc} is the thickness of the subcollector layer, μ_n is the mobility of the majority electrons, in N^{++} InP, $\mu_n \propto N^{-0.2}$[12]. Si is an amphoteric dopant in InP and above certain doping levels($\sim$ 4E19 cm^{-3}) starts to self compensate. The doping is chosen to obtain the lowest possible resistivity in the N^{++} layer. From the above expression, increasing the the subcollector thickness reduces the sheet resistance but this T_{sc}^{-1} decrease is insignificant beyond ≈ 0.5 μm. There is a practical concern for thick subcollectors in a standard triple mesa DHBT where device isolation is done by etching through the subcollector to the substrate. A thick subcollector thus results in a highly non-planar device which can compromise yield. A major portion of this thesis addresses these issues through the use of implanted subcollectors described in Chapter **??** . To reduce the contact resistance, a thin layer of highly doped In$_{0.53}$Ga$_{0.47}$As is used as the contact layer in standard triple mesa DHBTs [13]. Ternary materials have poor thermal conductivity (0.05 W/cm-K for In$_{0.53}$Ga$_{0.47}$As vs. 0.88 W/cm-K for InP) due to phonon Rayleigh scattering from the alloy disorder. This layer is kept thin to minimise the thermal resistance [14]. As will be described in detail in Chapter **??** , in the implanted DHBTs this InGaAs layer is undoped and designed to be 3.5 nm and is used as an etch-stop layer. The collector contact in these DHBTs is made to N^{++} InP.

2.3.1 Base-collector depletion capacitance, C_{cb}

The depleted space charge in the collector can be modeled as a parallel plate capacitance [15]. The collector is designed to be fully depleted at zero bias. This ensures a minmal variance in collector base capacitance as increased reverse bias is applied. For the mesa HBT structure shown in Fig. 2.3, the four components of the collector-base capacitance are,

$$C_{cb} = C_{cb,ex} + C_{cb,gap} + C_{cb,i} + C_{cb,pad} \tag{2.3.0}$$

$$C_{cb,ex} = 2\frac{\varepsilon_o\varepsilon_r L_e W_b}{T_c}, \quad C_{cb,gap} = 2\frac{\varepsilon_o\varepsilon_r L_e W_{gap}}{T_c}, \quad C_{cb,i} = \frac{\varepsilon_o\varepsilon_r L_e W_e}{T_c}, \quad C_{cb,pad} = 2\frac{\varepsilon_o\varepsilon_r A_{pad}}{T_c}$$
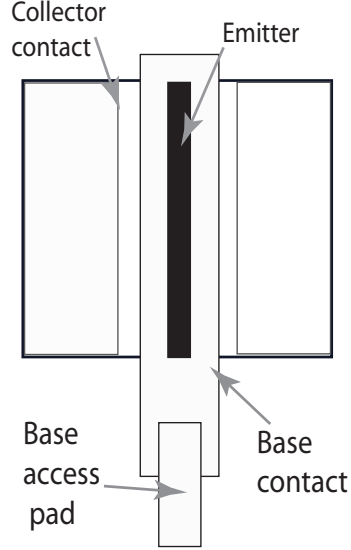
Figure 2.3: Top view of the mesa HBT showing the metal contacts

---

, where W_b is the width of the base metal-semiconductor junction, $W_{b,gap}$ is the spacing between the base contact and emitter mesa, and W_e and L_e are the width and length of the emitter junction. A_{pad} is the base access pad as seen in Fig. 2.3. A major portion of this thesis concerns the reduction of the collector-base capacitance. The collector base capacitance can be modeled as

$$C_{cb} = -\frac{\partial Q_{base}}{\partial V_{cb}} \tag{2.3.0}$$

But the transit time τ_f,

$$\tau_f = \tau_c + \tau_b \equiv \frac{\partial Q_{base}}{\partial I_c} \tag{2.3.0}$$

Therefore from Eqns. 2.3.1 and 2.3.1,

$$\frac{\partial C_{cb}}{\partial I_c} = -\frac{\partial \tau_f}{\partial V_{cb}} \tag{2.3.0}$$

If $\frac{\partial \tau_f}{\partial V_{cb}} > 0$, then $\frac{\partial C_{cb}}{\partial I_c} < 0$. This is called collector velocity modulation.

2.4   Figures of merit

Various figures of merit are used to describe the transistor.

2.4.1 Current-gain cutoff frequency f_τ

The current gain cut-off frequency for a bipolar transistor is given by [16],

$$\frac{1}{2\pi f_\tau} = \tau_c + \tau_b + C_{cb} \cdot (R_{ex} + R_c) + \frac{\eta kT}{qI_e}(C_{cb} + C_{je}) \qquad (2.4.0)$$

where τ_c and τ_b are the collector and base transit times, C_{cb} and C_{je} are the depletion capacitances for the collector and emitter, R_c and R_{ex} are the series resistances of the collector and emitter, and $(\eta kT/qI_c)^{-1}$ is the transconductance of the HBT. For a typical mesa DHBT with 120nm collector, 30nm base, emitter junction = 0.65×4.3 μm^2, $\rho_{c,C} = \rho_{c,E} = 10$ $\Omega \cdot \mu m^2$, base mesa width $=1.3$ μ m, $\tau_c = 0.188ps$, $\tau_b = 0.104ps$, $C_{cb} \cdot (R_{ex} + R_c) = 0.044ps$, $\frac{\eta kT}{qI_e}(C_{cb} + C_{je}) = 0.030ps$. The collector and base transit delay are seen to be dominant for the HBT described. As the devices are scaled vertically, these delays decrease. However the time constants associated with charging the base-collector capacitance starts to dominate. Thus reduction of base-collector capacitance gains significance as devices are scaled.

2.4.2 Power-gain cutoff frequency f_{max}

The HBT maximum oscillation (unity power-gain) frequency is,

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi (R_{bb}C_{cb})_{eff}}} \qquad (2.4.0)$$

dependent upon the HBT f_τ and a time constant $R_{bb}C_{cb})_{eff}$ that includes the effects of the distributed base-collector network [17]. Each component of C_{cb} is charged through a certain portion of the base resistance R_{bb}. Utilizing the definitions for C_{cb} and R_{bb} from Equ. 2.3.1 and 2.2.4 and assuming little undercut of the base-collector mesa,

$$(R_{bb}C_{cb})_{eff} \approx C_{cb,i}R_{bb} + C_{cb,gap}(R_{b,cont} + R_{b,gap}/2) + C_{cb,ex}R_{b,cont,0} + C_{pad}R_{b,cont,pad} \qquad (2.4.0)$$

where the collector-base capacitance underneath the emitter stripe $C_{cb,i}$ is charged through the entire base resistance, and the gap capacitance $C_{cb,gap}$ between the emitter mesa and base contact is charged through $(R_{b,cont} + R_{b,gap}/2)$. The extrinsic collector-base capacitance $C_{cb,ex}$ underneath the base contact is charged by currents traversing vertically through the contact above it, having a resistance $R_{b,cont,0} = \rho_c/L_eW_b$. The pad capacitance is charged by the vertical contact resistance associated with the base access pad, $R_{b,cont,pad} = \rho_c/A_{pad})$. For the sake of simplicity, Eqn. 2.4.2 for f_{max} ignores the effect of the collector and emitter series resistances since R_{bb} is usually much larger than R_c and R_{ex}. Power is dissipated in these resistances and their effect must be included especially if these resistances are $\sim R_{bb}$.

2.4.3   Maximum current density J_{kirk}

As the collector current density is varied, the injected electrons screen the background doping and modify the electric field profile in the collector. To account for this injected charge, Poisson equation can be written,

$$-\frac{d^2\phi}{dx^2} = \frac{dE}{dx} = \frac{1}{\varepsilon_o\varepsilon_r}\left[qN_c - \frac{J(x)}{\upsilon(x)}\right] \qquad (2.4.0)$$

where $\varepsilon_o\varepsilon_r$ is the dielectric constant, N_c the collector doping, $J(x)$ the collector current density, and $\upsilon(x)$ the electron velocity in the collector. Integrating Equ. 2.4.3 to solve for the electric field E(x),

$$E(x) = \frac{1}{\varepsilon_o\varepsilon_r}\int_0^x qN_c - \frac{J(x)}{\upsilon(x)} \ dx \qquad (2.4.0)$$

Assuming $J(x)$ and $\upsilon(x)$ to be constant and integrating the electric field over the collector to obtain the potential,

$$\phi_{bi} + V_{cb} \geq \frac{T_c^2}{2\varepsilon_o\varepsilon_r}\left[qN_c - \frac{J_e}{\upsilon_{eff}}\right] \qquad (2.4.0)$$

At a certain current density (injected electrons) at the base-side of the collector, $E(0) = 0$ at the edge of the base-collector junction. This is often referred to as the Kirk threshold current density

$$J_{Kirk} = J_{max} = \frac{2\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}(\phi_{bi} + V_{cb,i}) + qN_c\upsilon_{eff} \qquad (2.4.0)$$

where $V_{cb,i}$ is the intrinsic voltage across the base collector junction. $V_{cb,i} = V_{cb,applied} - I_c \cdot (R_c + R_{ex})$. At higher $J_e > J_{max}$ the position of the zero electric field pushes further into the collector. This causes the conduction and valence bands progressively flatten within the collector to a distance T_1, $0 \leq x < T_1$, $E(x) = 0$, so that the potential barrier for holes is zero. This causes the base to be be *pushed out* and hence the base transit time τ_b and collector-base capacitance C_{cb} increase. This is the classical definition of the Kirk effect [18]. As seen from Eqns. **??** ,higher HBT bandwidths are achieved at high current densities - J_{max} should be increased at a given collector thickness. From Eqn. 2.4.0, this can be done by increasing the $V_{cb,i}$ and/or increasing the collector doping N_c. When designing an HBT for use in a digital circuit, two bias conditions need to be considered: $V_{cb} = 0, J_e = J_{max}$ and $J_e = 0$. To maximize J_e, the collector doping should be designed as large as possible while fully depleting the collector at zero bias. From Eqn. 2.4.3 this is satisfied when,

$$N_{c,max} = \frac{2\varepsilon_o\varepsilon_r\phi_{bi}}{qT_c^2} \qquad (2.4.0)$$

and Eqn. 2.4.0 can be rewritten as

$$J_{max} = \frac{4\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}(\phi_{bi} + V_{cb}) \tag{2.4.0}$$

If the transistor is operating at J_{kirk}, the parasitic voltage drops across the collector and emitter resistances can greatly reduce the intrinsic collector-base voltage. J_{kirk} can be written as,

$$J_{Kirk} = \frac{4\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}(\phi_{bi} + V_{cb,applied} - I_c(R_c + R_{ex}))$$

$$J_{Kirk} = \frac{4\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}\left(\frac{\phi_{bi} + V_{cb,applied}}{1 + A_E \cdot (R_c + R_{ex})\frac{4\varepsilon_o\varepsilon_r\upsilon_{eff}}{T_c^2}}\right) \tag{2.4.0}$$

At the doping given by Eqn. 2.4.3, J_{max} is $2\times$ higher compared to a collector that
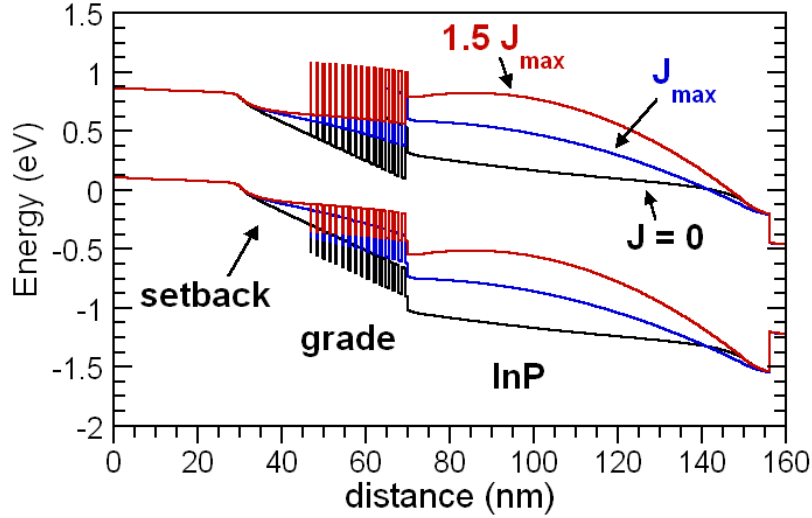
Figure 2.4: Band diagram at J=0, J_{kirk} and $1.5J_{kirk}$ for $V_{cb} = 0$

is undoped, greatly influencing logic speed through the use of smaller devices at a given operating current I_c. A band-diagram for the base-collector junction is shown in Fig. 2.4 for $J_e = 0$, J_{max}, and $1.5\ J_{max}$ at $V_{cb} = 0$. This clearly shows the base pushout regime. Beyond the maximum operating current density, the current gain falls and f_τ and f_{max} decrease.

2.5 Device modeling
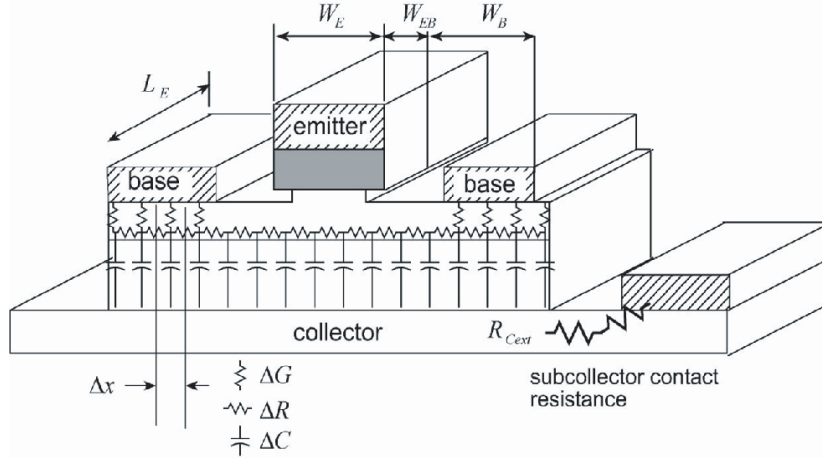
Figure 2.5: Mesa HBT showing distributed device resistances and capacitances

---

This section describes the small signal modeling schemes used to characterize InP HBTs from UCSB. It makes use of the measured S-parameters of the HBT in order to extract their electron transit time, resistances, and capacitances to create a hybrid-π equivalent circuit. It is an accurate, simplified, non-scaleable representation of an HBT compared to the true distributed nature of RC elements within the device. A SPICE model which is scaleable and physically based and includes bias and frequency dependence is used for circuit design and simulations. Fig. 2.6 shows the T-model equivalent circuit for an HBT. The T-model is physically derived and is intuitive.

$$\alpha(\omega) \approx \alpha_0 \frac{1}{1+j\omega\tau_b} e^{-j\omega\tau_c} \frac{sin(2\omega\tau_c)}{2\omega\tau_c} \tag{2.5.0}$$

where α_0 is the DC common base current gain. The T-model while physically based is difficult to work with except for analyzing common base stages. Through a series of transformations detailed in [19], the T-model can be simplified into a hybrid-pi model which is shown in Fig. 2.7. The hybrid-pi model shows that the base emitter capacitance consists of the junction capacitance and a diffusion capacitance. This diffusion capacitance, C_{diff} is an equivalent capacitance derived from the T-model as $C_{diff} = g_m\tau_f$ where $\tau_f = \tau_b + \tau_c$ is the total transit time through the base and the collector. The resistance R_{be} across the base emitter junction is also derived from the T-model and is given as $R_{be} = \beta/g_m$.

17
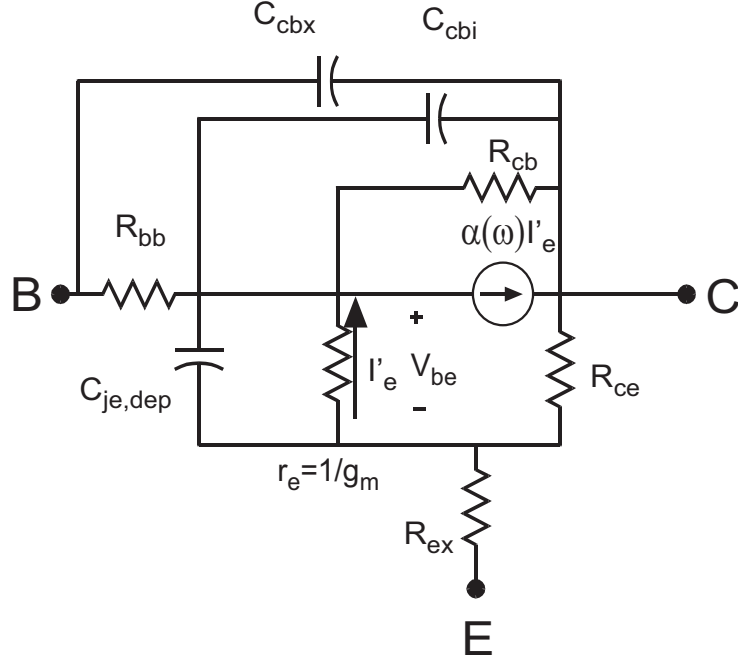
Figure 2.6: T-model equivalent circuit of an HBT

The various capacitances and resistances are extracted from RF (and DC) measurements.

The device transconductance g_m is given by,

$$g_m(\omega) = \frac{qI_e}{\eta kT} \cdot exp^{-j\omega\tau_f} \tag{2.5.0}$$

where η is the ideality factor of the collector current, extracted from the gummels as explained below. A non-unity ideality factor can arise when the current-voltage relations deviate from the elementary diode current formulation. This happens due to recombination currents, and thermionic emission over the heterobarrier at the base emitter interface.

The transistor Y parameters are obtained from the 2-port S parameter measurement of the device. At low frequencies,

$$Re(Y_{21})^{-1} = R_{ex} + \frac{R_{bb}}{\beta} + \frac{\eta kT}{qI_e} \tag{2.5.0}$$

$Re(Y_{21})^{-1}$ is plotted for various bias currents. $\beta = \partial I_c / \partial I_b$ is determined from the low frequency value of h_{21}. The intercept at $1/I_e = 0$ gives $R_{ex} + R_{bb}/\beta$ while η
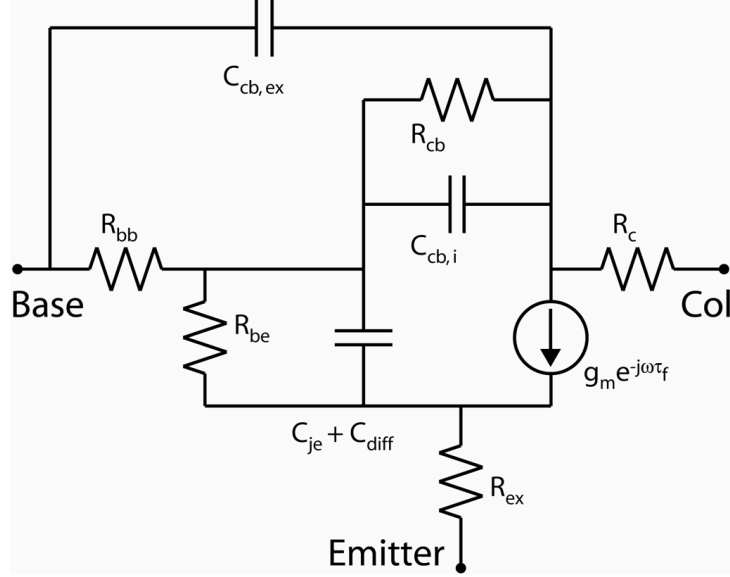
Figure 2.7: Hybrid-pi equivalent circuit HBT model

can be determined from the slope. The collector-base conductance $1/R_{cb}$ and total collector-base capacitance C_{cb} aree determined from the real and imaginary parts of Y_{12} at low frequencies,

$$Y_{12} = \left(\frac{1}{R_{cb}} + \omega^2 (C_{be} + C_{cb,i}) C_{cb,i} R_{bb} \right) + j\omega (C_{cb,i} + C_{cb,ex}) \tag{2.5.0}$$

This method involves RF measurements of transistors and is accurate but time consuming. An extraction from DC measurements is developed in this thesis. This involves extraction from Gummel plots, which are logarithmic plots of I_C and I_B vs. V_{BE}. The collector current can be expressed as,

$$I_C = I_{CO} e^{\frac{q}{kT_A}[V_{BE,i} - (T - T_A)\frac{\partial V_{BE,i}}{\partial T}]} \tag{2.5.0}$$

where T_A is the ambient temperature,$\sim$ 300K and $V_{BE,i}$ is the intrinsic base emitter voltage given by

$$V_{BE,i} = V_{BE} - I_C \cdot (R_{ex} + R_{bb}/\beta) \tag{2.5.0}$$

where V_{BE} is always the measured base emitter voltage. The effect of the emitter and base resistances are seen as deviations from the exponential dependence in the gummel plot (see Fig. **??**). In a linear plot, the resistances cause a leanover in the

current in the diode I-V characteristics. The change in V_{BE} as a result of temperature change in the device is given by,

$$\delta V_{BE} = -\Theta_{th} \cdot \frac{\partial V_{BE}}{\partial T} \cdot I_C \cdot \delta V_{CE} \tag{2.5.0}$$

where, Θ_{th} is the thermal resistance usually expressed in $^\circ$K/mW. The effect of
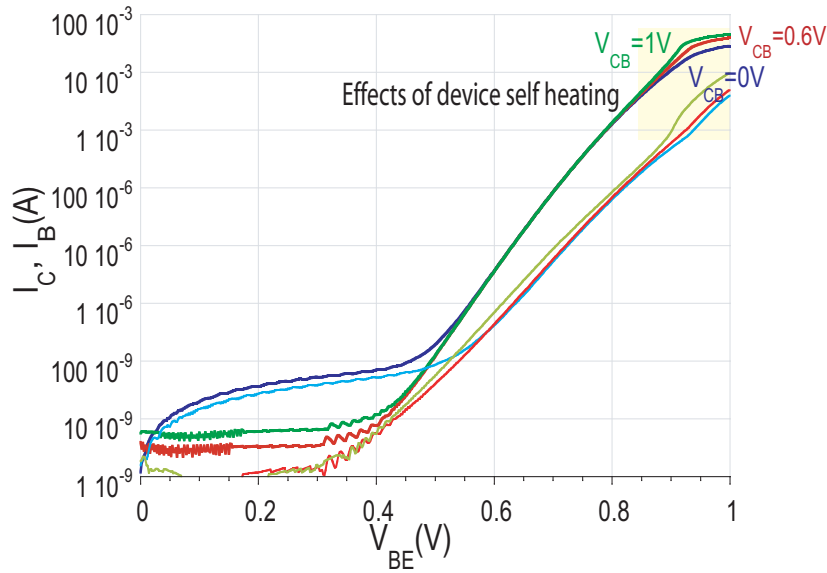
Figure 2.8: Effect of device heating, with V_{CB}, in the gummel plot

temperature on V_{be} is particularly large at high current densities and can be seen in the as measured gummel curves in Fig. 2.8. The device heating is due to increasing reverse collector base biases and therefore I_C in the gummels is dependent on the value of V_{CB}. In a well designed DHBT ,where the early voltages are very high ($\geq$ 1500V), I_C should not have any V_{CB} dependence in the active region of operation (the effect of collector resistance is ignored and will be revisited in Chapter **??**). In order to accurately extract R_{ex} from the Gummels, this thermal dependence of V_{BE} has to be removed, and it is then named as $V_{BE}^{isothermal}$. I_C vs $V_{BE}^{isothermal}$ should therefore have no dependence on V_{CB}. A method(unpublished) to extract isothermal gummels is suggested.

From Eqn. 2.5, the isothermal base emitter voltage is written as,

$$V_{BE}^{isothermal} = V_{BE} - \Theta_{th} \cdot \frac{\partial V_{BE}}{\partial T} \cdot I_C \cdot \delta V_{CE} \tag{2.5.0}$$

The detailed derivation is skipped but $V_{BE}^{isothermal}$ can be expressed in terms of V_{CB} and V_{BE} as,

$$V_{BE}^{isothermal} = \frac{V_{BE}}{1 + \Delta V_{BE}/\Delta V_{CB}} - \frac{V_{CB}}{1 + \Delta V_{CB}/\Delta V_{BE}} \quad (2.5.0)$$

This suggests that $\Delta V_{BE}/\Delta V_{CB}$ should be calculated at each I_C. However, in the Gummels measurement procedure, I_C is measured at various applied base emitter voltages V_{BE}. An approximate value of $\Delta V_{BE}/\Delta V_{CB}$ could be used for different ranges of I_C but due to this quantization error, kinks are seen in the resulting isothermal gummel curves. A simple mathematical analysis is shown below.

$$I_C \sim I_C(V_{BE}, V_{CB})$$
$$\partial I_C = 0 \text{ since}$$

$\dfrac{dV_{BE}}{dV_{CB}}$ is needed at constant I_C. This leads to

$$\frac{dV_{BE}}{dV_{CB}} = -\frac{\frac{\partial I_C}{dV_{CB}}\big|_{V_{BE}}}{\frac{\partial I_C}{dV_{BE}}\big|_{V_{CB}}}$$

$$(2.5.-3)$$

This approximates to a linear interpolation for small, discrete values of ΔV_{BE} and ΔV_{CB}. $V_{BE}^{isothermal}$ is thus calculated by using small values of ΔV_{BE} and ΔV_{CB}. Fig. 2.9 shows the isothermal gummels and as expected, I_C does not depend on V_{CB}. From the isothermal plot, $R_{ex} + R_{bb}/\beta$ is extracted as shown in Fig. 2.9. β is the current gain of the device known from the gummel curves. Usually β is large enough that the contribution of R_{bb}/β is neglected. The resistance seen in the emitter is thus plotted in Fig. 2.10.

Furthermore this method is also an extraction procedure for the thermal resistance of the device, Θ_{th}. which is seen from Eqn. 2.5 to be

$$\Theta_{th} = -\frac{\delta V_{BE}}{\frac{\partial V_{BE}}{\partial T} \cdot I_C \cdot \delta V_{CE}} \quad (2.5.-3)$$

where $\phi = \frac{\partial V_{BE}}{\partial T}$ is called the thermal-electrical feedback coefficient, expressed in $mV/^{\circ}K$. It is a property of the transistor and is approximately a constant ($\approx 2mV/^{\circ}K for InPDHBTs$.

The total delay τ_{ec}, that electrons experience through the HBT is,

$$\frac{1}{2\pi f_{\tau}} = \tau_c + \tau_b + C_{cb} \cdot (R_{ex} + R_c) + \frac{\eta kT}{qI_e}(C_{cb} + C_{je}) \quad (2.5.-3)$$
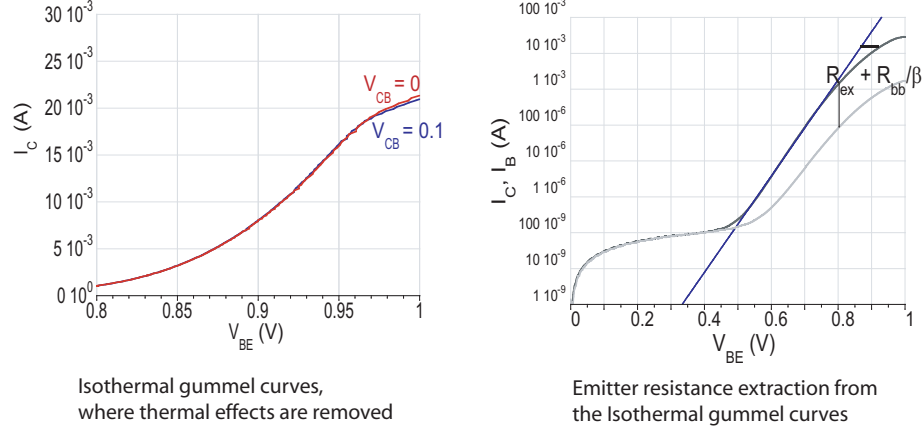
Figure 2.9: Isothermal gummel plot and effect of emitter and base resistances

f_τ is extracted from h_{21} at different bias currents and C_{cb}, R_{ex}, and g_m have already been determined. $\frac{1}{2\pi f_\tau}$ is plotted for the various bias currents at which f_τ is measured. The slope gives C_{je} since C_{cb} is already obtained from 2.5. R_{ex} is known from 2.5. with knowledge of R_c, $\tau_f = \tau_c + \tau_b$ and hence C_{diff} can be determined from the $1/I_e = 0$ intercept. R_c is usually calculated for the HBT geometry knowing the values, from TLM measurements, of contact resistivity ρ_c and sheet resistance R_{sh}. This not accurate especially when R_c is dominated by other than the contact resistance. An alternate method is explored in this thesis using the DC I_C-V_{CE} characteristics. From the Ebers-Moll model for a bipolar transistor, V_{CE} is given by

$$V_{CE} = \frac{kT}{q} ln \frac{1 + \frac{I_C}{I_B} \cdot (1 - \alpha_r)}{\alpha_r (1 - \frac{I_C}{I_B \cdot \beta_F})} + I_C(R_{ex} + R_c) + I_B \cdot R_{ex} \qquad (2.5.\text{-}3)$$

where β_F is the forward current gain and $\alpha_r = \frac{\beta_r}{\beta_r + 1}$ as defined in the Ebers-Moll equations [20]. If $\beta = I_C/I_B$ is kept constant for various values of I_C, term 1 in Eqn. 2.5 is constant. From the I_c-V_{CE} characteristics, V_{CE} is plotted vs. I_C, keeping β a constant. The slope of this curve gives $R_c + R_{ex} + R_{ex}/\beta$. R_{ex} has already been determined from Re(Y_{11}) and from the gummel extraction procedure described. R_c can now be extracted. The variation of V_{CE} with current is plotted for several values of β. This method extracts R_c from the saturation regime of transistor operation where I_C increases with V_{CE}. This is far from the usual operation of the transistor. The base resistance is determined by comparing the real part of Y_{11} of the measured
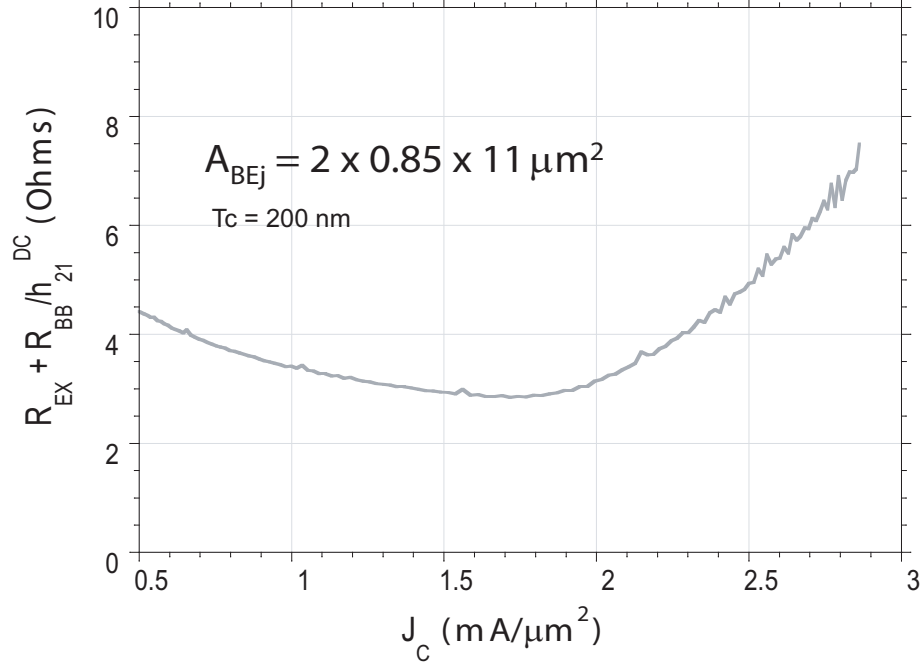
Figure 2.10: Extracted emitter and base resistance

HBT data to the equivalent circuit from the following relation,

$$Re(Y_{11}) \approx \frac{1}{R_{be}} + \omega^2 (C_{je} + C_{diff})^2 \cdot R_{bb} \qquad (2.5.-3)$$

Through the hybrid-π model, R_{bb} is adjusted to make the quadratic frequency dependence of $Re(Y_{11})$ match the measured trend.Once determined, R_{bb}/β is known. $C_{cb,i}$ is similarly determined from ReY_{12} in Eqn. 2.5. Mason's unilateral gain U is only influenced by $C_{cb,i}$. By simultaneously monitoring $Re(Y_{12})$ and U, $C_{cb,i}$ is adjusted while keeping the total C_{cb} constant to match the measured data.

Analysis of the hybrid-π network gives $Im(Y_{12}) = \omega C_{cb}$. From the S-parameters measured, Y_{12} can be extracted. This is used to extract the total C_{cb}. From the C-V

data at $I_c = 0$ mA, the doping density can be derived as follows.

$$C_{cb} = -\frac{Q_c}{V_{bc}} \qquad (2.5.-2)$$

$$dQ_c = qN(x_d)dx$$

In general, the doping density can be expressed as,

$$N(x_d) = -\frac{C dx}{q dV} = -\frac{C}{q}\frac{dC}{dV}\frac{dx}{dC} \qquad (2.5.-3)$$

$$N(x_d) = \frac{dC_{cb}/dV_{cb}}{q\epsilon A_c^2 C_{cb}^3} = -\frac{2}{q\epsilon A_c^2} \cdot \frac{dV}{d(1/C_{cb}^2)}$$

The depletion region edge is given by

$$x_d = \frac{\epsilon A_c}{C_{cb}} \qquad (2.5.-4)$$

. Therefore, the doping density can be plotted as a function of depletion distance in the collector. This neglects the effect of Deby length on the doping profile extracted [21]. Fig. 2.11 shows on a Smith chart measured HBT S-parameters and those of its equivalent circuit. The f_τ and f_{max} of the hybrid-π equivalent circuit is consistent with the value extrapolated for the HBT.

2.6   HBT delays within digital ICs

The HBT figures-of-merit f_τ and f_{max} describe the maximum bandwidth for a single device. They are of limited value in predicting digital logic speed. An standard benchmark for digital logic figure-of-merit, for a device technology, is the bandwidth of a static frequency divider shown in Fig. 2.12. It is a master-slave (M-S) flip-flop consisting of two series connected latches that are clocked out of phase 180° so that the input is transparent at the output only at the falling edge of the clock. As shown in the timing diagram in Fig. 2.12, when $\bar{Q}$ is connected to D, the output = $f_{CLK}/2$. MS latches are utilized as retiming elements for data synchronization and their maximum toggle rate often limits circuit bandwidth. For this reason, static dividers are a more realistic benchmark circuit in comparison to the narrow-band operation of dynamic frequency dividers and ring oscillators.

The propagation delay through the latch is dependent upon the combined charging times of the capacitances in the signal path. By modeling the latch as an n-port linear network having no inductors, the method of open circuit time constants (MOTC) can be used to evaluate the time constants associated with the poles a_n of
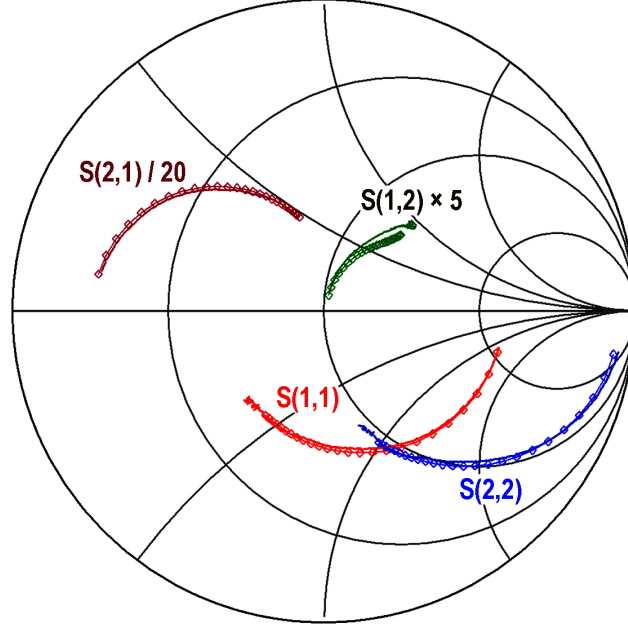
Figure 2.11: Measured (solid line) and simulated S-parameters (data points) of the HBT and the extracted hybrid-π equivalent circuit

---

the system. The transfer function for such a network is given by,

$$\frac{V_{out}}{V_{in}} = A_{v,midband} \left(\frac{1 + b_1 s + b_2 s^2 + \cdots b_n s^n}{1 + a_1 s + a_2 s^2 + \cdots a_n s^n} \right) \tag{2.6.0}$$

In order to utilize MOTC, the passive and active components of the network must behave linearly. Each arm of the differential pair (say Q_1 and Q_2) in Fig. 2.13, conduct current in alternate clock cycles. Thus the small signal values of g_m and C_{je} are no longer valid. To satisfy this requirement, the HBT transconductance g_m and diffusion capacitance C_{diff} of those devices operating as part of a differential pair (where the voltage swing across the base emitter junction is $\approx \ \Delta V_{logic} >> kT/q$) are modified,

$$G_{m, \, large-signal} = \frac{\Delta I_o}{\Delta V_{be}} \approx \frac{1}{R_{Load}} \tag{2.6.1}$$

$$C_{diff, \, large-signal} = G_m \tau_f \tag{2.6.2}$$

$$C_{je, \, large-signal} = \frac{1}{V_1 - V_2} \int_{V_1}^{V_2} C_{je}(V) \, dV \tag{2.6.3}$$

25
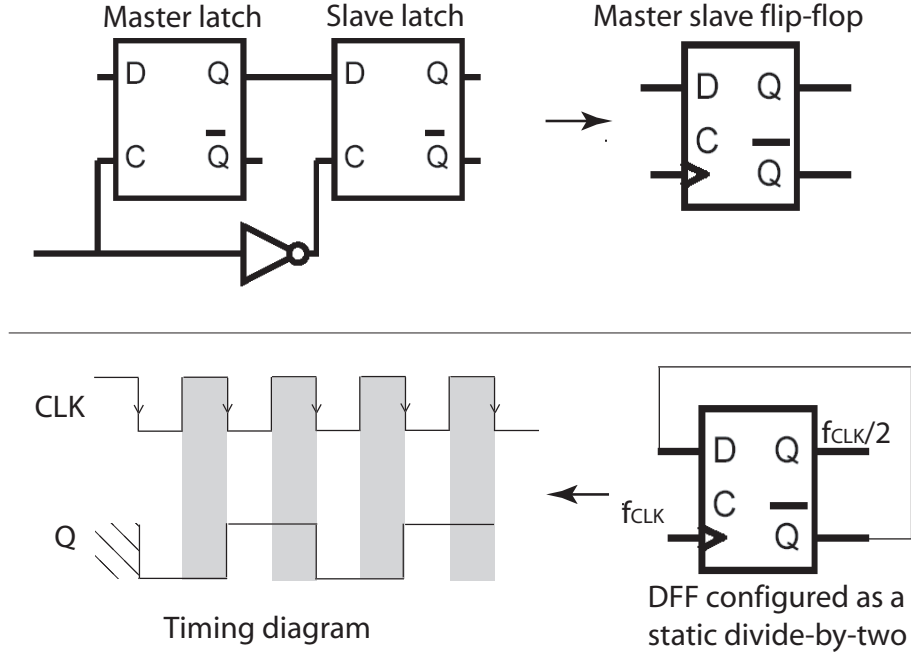
Figure 2.12: Static frequency divider and its timing diagram

Large signal operation greatly reduce G_m and C_{diff} by $\sim 1:10$. The depletion capacitance C_{cb}, is not altered and the charging (and discharging) of this capacitance constitutes a major delay in a digital circuit. From the method of time constants [**?**], a_1 is,

$$a_1 = R^0_{11}C_1 + R^0_{22}C_2 + R^0_{33}C_3 + \cdots R^0_{nn}C_n \qquad (2.6.3)$$

where R^0_{nn} is the effective resistance across the terminals of C_{nn} with other capacitances treated as open (for example, see [22]). The propagation delay is typically defined as the time required to effect a change in the output node when the input is toggled. Assuming $(1 - \exp(-t/\tau))$ charging behavior, $T_{prop} = a_1 \ln(2)$. However, to the level of accuracy of the assumptions used in the analysis, $T_{prop} = a_1/2$. Fig. 2.13 shows the significant resistive and capacitive delay elements in the signal
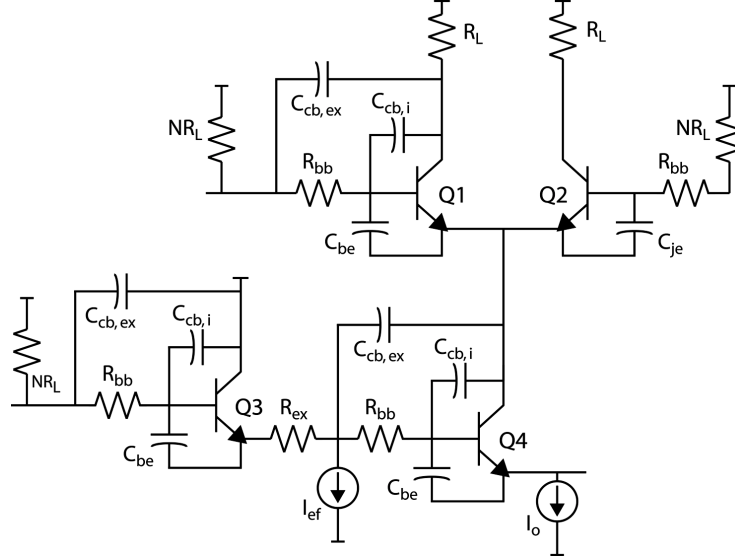
Figure 2.13: Delay path of a CML static frequncy divider during clock transition

path of a two level CML flip-flop. The propagation delay is simplified to

$$
\begin{aligned}
2T_{prop} \cong \ & N(\Delta V_{logic}/I_o)C_{cb3} \ + \ R_{bb}C_{cbi3} \\
& + \ [2(R_{ex3} \ + \ 1/g_{m3}) \ + \ (\Delta V_{logic}/I_o)]C_{cb4} \ + \ 2C_{cbi4}R_{bb4} \\
& + \ (C_{je4} \ + \ I_o\tau_f/\Delta V_{logic})(R_{bb4} \ + \ R_{ex3} \ + \ 1/g_{m3}) \\
& + \ [C_{je2} \ + \ C_{je1} \ + \ (I_o\tau_f/\Delta V_{logic})](\Delta V_{logic}/I_o) \\
& + \ (N \ + \ 1)(\Delta V_{logic}/I_o)C_{cb1} \ + \ R_{bb1}C_{cbi1}
\end{aligned}
\tag{2.6.0}
$$

where the devices are operating in the following modes: Q_3 emitter-follower, Q_4 common-emitter, Q_1 common-base, and Q_2 cut-off. N denotes the fan-out of identically connected gates in a larger circuit. As seen from Eqn. 2.6.0, the base and collector transit times play a relatively minor role in logic speed, in comparison to their strong contributions to f_τ. The most significant delays in the latch are from charging the depletion capacitances over the logic swing, $(C_{je} + C_{cb})\Delta V_{logic}/I_o$, where $\Delta V_{logic}/I_o = R_L$. This can be expressed in terms of the current density and transistor sizes as

$$
(C_{je} + C_{cb})\frac{\Delta V_{logic}}{J_e \cdot A_e} = \hat{C}_{je} \cdot \frac{\Delta V_{logic}}{J_e} + \hat{C}_{je} \cdot \frac{A_C}{A_E} \cdot \frac{\Delta V_{logic}}{J_e}
\tag{2.6.0}
$$

To minimize these capacitive delays, small devices should be used operating a current density J_e close to J_{Kirk} and the collector to the emitter area ration(A_C/A_E)

27

must be made small which is the objective of this dissertation. From the above expression 3.3, C_{cb}/I_c expressed in ps/V is an important metric to be considered while comparing digital circuits in various technologies.

ΔV_{logic} is dependent on the input noise margin which is influenced by R_{ex}. It is not evident from the gate delay expression, but R_{ex} has a large indirect effect on the maximum toggle rate. For the differential pair in Fig. 2.14, the differential switching current is described by,

$$I_{c1} - I_{c2} = I_o \tanh\left[\frac{q(V_1 - V_2)}{2kT} - \frac{I_{e1} - I_{e2}}{2} \cdot R_{ex}\right] \qquad (2.6.0)$$

With $R_{ex} \sim 0$, the current is completely switched when $V_1 - V_2 = 6kT/q$. As R_{ex} increases, at a fixed current I_o, increasing input voltage is needed to completely switch the differential pair. When the voltage drop across R_{ex} is $6kT/q$, more than $10kT/q$ potential difference is needed to switch the currents. If we assume an HBT junction temperature rise of $\sim 60°C$ when these devices operate in a larger circuit, the potential difference required to switch only the base-emitter junction is ~ 200 mV. Typically, $V_1 - V_2 = \Delta V_{logic} = 300$ mV for ECL and CML based latches. Thus the digital noise margin is ~ 100 mV $\approx 4kT/q$.
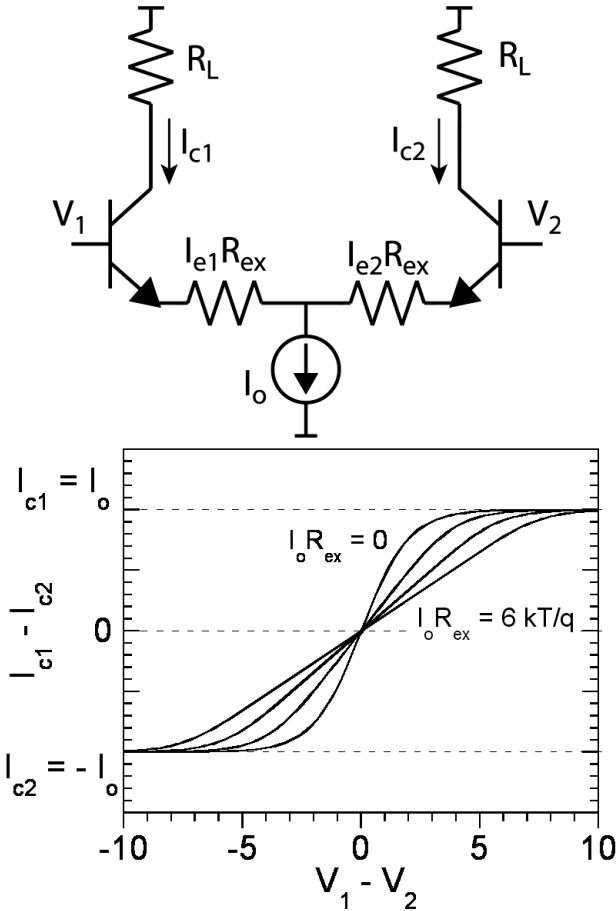
Figure 2.14: Current flow of a differential pair in the presence of emitter resistance – $I_o R_{ex} = 0, 2kT/q, 4kT/q$, and $6kT/q$. $V_1 - V_2$ is normalized to kT/q.

2.7 HBT scaling principles

The previous sections reviewed the relevant HBT transit and RC delays associated with discrete device performance and those of a digital latch. In order to improve HBT as well as analog and digital IC speed, all significant capacitances and transit times must be simultaneously reduced. This is summarised as the scaling laws for a HBT [3].

As seen in the earlier sections, f_τ is dominated by τ_f while increasing current density decreases digital delay. If T_c and T_b are decreased by γ and maintaining all device dimensions constant,

$$\tau_c \downarrow \gamma^2$$
$$\tau_b \downarrow \gamma^2$$
$$J_{kirk} \uparrow \gamma^2$$
$$C_{cb} \uparrow \gamma$$
$$R_{bb} \uparrow \ \approx \gamma \tag{2.7.-3}$$

If the collector junction areas are also reduced by $1{:}\gamma^2$, C_{cb} will also decrease by γ. To reduce R_{bb}, the base contact resistivity would have to be decreased by $\sim \gamma^2$. If the base ohmic contacts lie above the collector-base junction, their width must be reduced $1{:}\gamma$ to obtain the requisite reduction in C_{cb}; this necessitates a further reduction in the base contact resistivity $\rho_{c,b}$. However, this is very difficult and limited by the doping in the base, the work function of the contact metal used and by surface preparation prior to metal deposition. Therefore, one of the biggest challenges to vertical device scaling is the scaling of the collector base capacitance. Independent scaling of the emitter and collector junction is necessary and is the main subject of this dissertion.

It is also seen from Eqn. 2.7.-3 that current density increases with vertical scaling. If the emitter junction dimensions are kept constant I_e increases. This increases the power consumption in the device and thermal effects assume significance. Therefore it is equally important to scale the emitter junction area. The power consumption in the divider is very approximately,

$$P_L \propto \Delta V_{logic} \times J_e \cdot A_{je} \approx (6\frac{kT}{q} + 2J_e A_{je} R_{ex}) \times J_e L_e W_{je} \tag{2.7.-3}$$

The width of the junction area is limited by the lithographic and process tolerances. To decrease power consumption by $1{:}\gamma$ while maintaining high high current density, means decreasing the emitter (and device) length, so that the emitter junction area $A_{je} \downarrow \gamma^2$. This is especially important for low power logic. As seen in the previous

section, a significant component of the delay in logic circuit is

$$\hat{C}_{cb} \cdot \frac{W_{bm}}{W_{je}} \cdot \frac{\Delta V_{logic}}{J_e} + C_{cb,pad} \cdot \frac{\Delta V_{logic}}{J_e L_{je} W_{je}} \qquad (2.7.\text{-}3)$$

where $\hat{C}_{cb}$ is the device capacitance per unit area (not including $C_{cb,pad}$, the access pad capacitance). A certain access pad area($\approx 2 \ \mu m^2$) is needed for the device to reliably contact the metal interconnect and to maintain a low metal access resistance. This base pad cannot be scaled. As seen from Eqn. 3.3, as the length is decreased, $C_{cb,pad}$ becomes a significant fraction of the total C_{cb}. Chapter **??** addresses this through the use of implanted subcollectors.

In a standard triple-mesa DHBT process, decrease in the junction area is accompanied by an increase in the emitter resistance, the emitter contact area has decreased as well. Besides affecting logic speed and f_τ, as seen in the precious section an increase in R_{ex} severely impacts the noise margin of the logic circuit. If $\rho_{ex}/Aem \cdot J_e A_{ej}$ is to remain a constant where A_{em} is the area of the emitter contact, ρ_{ex} must decrease in proportion to increase in J_e. This is a process challenge and addressed by the use of highly doped InAs layers[**?**]. An alternate method to maintain R_{ex} constant, is to decrease A$_{je}$ and maintain A$_{em}$ constant. This can be done by severe undercutting of the emitter base junction which presents process difficulties or by emitter regrowth discussed in Chapter **??** .

Vertically scaling the collector thickness decreases the breakdown voltages, BV_{CEO} and BV_{CBO}. The breakdown voltage is limited by several factors in a DHBT. Firstly the term 'breakdown voltage' needs clarification. Traditionally, open base or open emitter voltage at a certain current level (50 μA) are often reported. At these current levels, leakage current due to passivation or surface states limit the maximum voltage attained. If the setback and grade layers are thick, impact ionisation could occur in these regions and thus the advantage of having wideband gap InP collector is lost. (It is unclear at this time whether breakdown is due to impact ionisation or tunneling.) Since operating J_e increases with vertical scaling, the maximum reliable power density associated with a *safe operating area* $P/A_e \sim J_e V_{ce} \propto \gamma^2 V_{ce}$ is a more significant applied voltage limit than the low-current breakdown voltages BV_{CEO} or BV_{CBO}.

The total emitter-base capacitance C_{je} is given by,

$$C_{je} \approx \frac{\kappa_1 L_e W_e}{T_{eb}} \qquad (2.7.\text{-}3)$$

If the emitter junction is scaled laterally, to first order C_{je} is reduced $\gamma^2 : 1$ (where κ_1 is a constant). Scaling requirements for the emitter depletion thickness T_{eb} are not easily summarized here and detailed analysis for scaling T_{eb} is reported in [3].

Table 2.1: Summary of simultaneous parameter scaling for a γ:1 increase in HBT and circuit bandwidth

key device parameter	required change
collector depletion layer thickness	decrease γ:1
base thickness	decrease $\sqrt{\gamma}$:1
emitter-base junction width	decrease γ^2:1
collector-base junction width	decrease γ^2:1
emitter depletion thickness	decrease $\gamma^{1/2}$:1
emitter contact resistivity, ρ_{ex}	decrease γ^2:1
emitter current density	increase γ^2:1
base contact resistivity – if contacts lie above B-C junction	decrease $\sim \gamma^2$:1
base contact resistivity – if contacts do not lie above B-C junction	unchanged
bias currents and voltages	unchanged

Lastly, reductions to device thermal resistance need to be considered. For discrete HBTs, a significant fraction of the heat generated in the collector is removed through the base and into the emitter metal. In large integrated circuits, the heat-sinking through the emitter is much less effective.. The thermal resistance normalized to the emitter junction area $\theta_{JA}A_{je}$ must be reduced in proportion to the square of the circuit bandwidth $\gamma^2 : 1$. Thinning the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ subcollector layer is imperative [14] to decreasing the device thermal resistance.

What is the impact of this scaling on ECL (and CML) logic speed? With a γ:1 scaling, the collector thickness T_c is reduced γ:1, the current density increased γ^2:1, and the dominant delay $C_{cb}\Delta V_{logic}/I_c$ reduced 1:γ, **only if** the access pad capacitance $C_{cb,pad}$ is eliminated. The parasitic voltage drop $R_{ex}I_c = \rho_{ex}J_e$ remains constant if ρ_{ex} is reduced rapidly by 1:γ^2. The scaling laws for a γ-fold increase in bandwidth are summarised in Table 2.1

2.8 HBT scaling limits, and solutions explored in this work

In order to increase circuit bandwidth, the transit times and capacitances of the device must be reduced while maintaining constant (total) resistances, currents, and g_m. This is realized by thinning the base and collector layers, narrower emitter and collector junctions, increased operating current density, and reduced contact ρ_c and

sheet ρ_s resistivities.

Emitter contacts as narrow as 0.4 μm can be achieved through standard optical lithography and evaporated metal-liftoff techniques. If the emitter contact is to be further scaled, advanced photoresist processes are needed to resolve smaller features using i-line stepper lithography. The height of the contact will be limited by the aspect ratio attainable from the e-beam metal evaporator. An electroplated emitter contact, or one formed through metal-sputtering and dry-etch, are alternative ways of producing tall, straight, narrower features. For these narrower contacts, the undercut of the emitter mesa becomes increasingly difficult to control. Dielectric sidewall spacer processes allow for very thin emitter semiconductor layers, minimizing the undercut during mesa formation. Furthermore, the spacer eliminates the need for evaporated self-aligned base contacts, where instead electroplating or metal-sputter dry-etch processes are used. These advanced processes are under development and are discussed in [23, 24]. As discussed, narrow emitters contacts lead to higher emitter resistance. Emitter contact resistivity, to N^+ In$_{0.85}$Ga$_{0.15}$As, as low as $10\,\Omega\cdot$ μm^2 is now standard at UCSB [13]. It is not clear how ρ_c can be further reduced by conventional deposition techniques. Advanced materials engineering such as the use of in-situ MBE grown ErAs ohmics may be beneficial. Regrown emitter junction HBTs have also been developed at UCSB as an alternative, where the ohmic contact is much larger than the emitter junction for reduced access resistance.

Thinner base and collector epitaxial layers can be achieved through growth. The base sheet resistance is $\propto T_b^{-1}$, and to keep it unchanged the bulk resistivity (ρ_{bulk}, $\Omega\cdot$cm) must be decreased through increased through base doping. As the doping approaches $7 \cdot 10^{19}$ cm^{-3}, the hole mobility decreases and the doping-mobility product remains relatively constant. This is a challenge that can be addressed through the use of extrinsic bases described in brief in Chapter **??** The InP DHBTs reported here utilize a 30 nm base and doping grade from $7 - 4 \cdot 10^{19}$ cm^{-3}. Through the appropriate choice of metal workfunction and highly doped semiconductor the contact resistivities are decreased. The Fermi level at the semiconductor surface is pinned due to a combination of surface states, native oxides, and metal-semiconductor diffusion at the interface. Surface preparation techniques to minimize their presence have been developed, and low values of contact resistance $\rho_c \approx 10\,\Omega\cdot\mu$m^2 values have been achieved. The resulting transfer length of the base contact is ~ 130 nm. Narrower collector junctions require narrower base contacts. A minimum width $\sim L_t$, the ohmic transfer length, should be maintained to prevent exponential increases to the contact resistance $R_{b,cont}$. These thin, narrow contacts have high access resistance and inductance that influence HBT performance. Furthermore circuits employing these narrow contacts are very difficult to yield in a manufacturing environment.

Therefore in order to satisfy the scaling requisites for the collector junction, im-

planted collector processes have been developed and is the main topic of this dissertation. The non scaleable collector base access pad capacitance is identified as a major parasitic. This parastic capacitance is eliminated through the use of implanted subcollectors. Independent scaling of the collector is highly desirable, within a simple, manufacturable process. A fully implanted pedestal and subcollector transistor is demonstrated where the extrinsic collector base capacitance is greatly reduced.

2.9 The scaled HBT
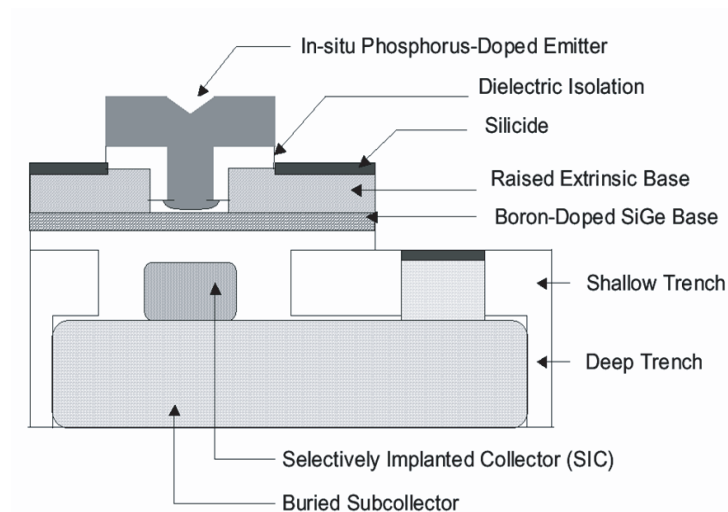
Figure 2.15: Modern SiGe HBT

Compared to modern SiGe HBT, InP HBT manufacturing is primitive. The SiGe HBT shown in Fig. 2.15, has buried subcollectors for zero pad capacitance, N^+ pedestal for lateral collector scaling, deep dielectric trenches for device isolation, thick extrinsic base and buried base ohmics for reduced R_{bb}, and submicron regrown emitters for emitter-base junction scaling while simultaneously maintaining wide emitter contacts. It has a planar geometry and large scale ICs are possible [**?**]. Due to this extreme scaling and reduction in relevant parasitics, SiGe HBTs are as fast as their InP counterparts for digital logic applications. Static frequency dividers of ~ 100 GHz have been demostrated with devices having cut-off frequencies of ~ 300 GHz. This serves as the motivation for scaling InP HBTs and in this thesis, technologies are developed for InP HBTs, to parallel the SiGe HBT manufacturing process.
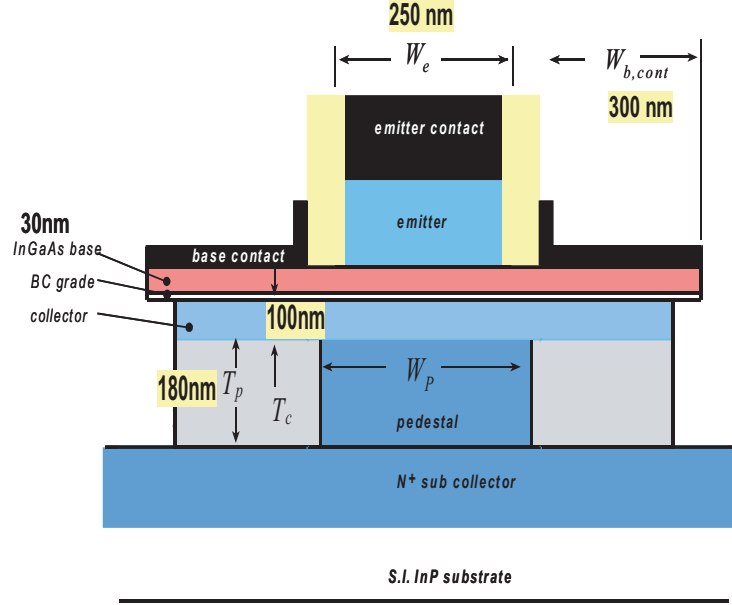
Figure 2.16: Scaled mesa HBT with collector pedestal

The bulk of this thesis examines technologies to reduce the base collector capacitance. In this sub-section, the expected performance enhancement with reduction in C_{cb} is calculated for highly scaled HBTs. A scaled mesa HBT is shown in Fig. 2.16 employing an emitter sidewall [23] and implanted pedestal-subcollector technology developed in this dissertation. Table 2.2 compares standard figures of merit for a device with 250nm emitter and 300nm base, with and without the implanted collectors.

This calculation assumes all contact resistivities $\rho_c \sim 10\,\Omega \cdot \mu\text{m}^2$, current density J_{kirk} is 13 $mA/\mu\text{m}^2$, wiring delay of 0.3 ps , and the width of the emitter junction

Table 2.2: Expected performance of a scaled InP DHBT with and without implanted collectors

Standard Figures of merit	standard mesa DHBT	mesa DHBT with implanted collectors
f_τ	490 GHz	550 GHz
f_{max}	600 GHz	800 GHz
f_{clock}	180 GHz	270 GHz
C_{cb}/I_c	0.4 ps	0.2 ps

$W_{je}= 0.25~\mu$m. The other vertical and lateral dimensions are as in Fig. 2.16. All other parameters are drawn from the state of the art UCSB mesa process [13]. Assuming that the breakdown mechanism is impact ionisation or tunneling, the breakdown voltages ($\approx 4V$) are not expected to be different for the two technologies. The power consumption of digital circuits at a given bandwith, is expected to be much lower for the mesa DHBT with implanted collectors.

It is seen from Table 2.2 that reduction in C_{cb} tremendously improves f_{max} and the maximum digital circuit speed f_{clock}, while the difference to f_τ is marginal. As discussed in the prior sections, f_τ is dominated by the transit delay in the device while f_{max} is approximately $\propto C_{cb}{}^{-1}$, and digital logic speed is severely impacted by the delay term, $C_{cb}~\Delta V_{logic}/I_c$. The numbers in Table 2.2 serve to illustrate that reduction in C_{cb} considerably enhances the high frequency performance of power amplifiers (which depends on f_{max}), and digital circuits.

References

[1] S. Tiwari and D.J. Frank, "Barrier and Recombination effects in the base-emitter junction of heterostructure bipolar transistors" *Applied Physics Letters*, Vol. 52(5), pp. 993-995, March 1988.

[2] T. Ishibashi, "Nonequilibrium Electron Transport in HBTs", *IEEE Transactions of Electron Devices*, vol. 48, pp. 2595-2605, Nov. 2001

[3] M.J.W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S.C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. I. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlström. "Submicron Scaling of HBTs" *IEEE Trans. on Electron Devices*, Vol. 48, pp. 2606-2624, November 2001.

[4] M. Ida, K. Kurishima, H. Nakajima, N. Watanabe and S. Yamahata, "Undoped-Emitter InP-InGaAs HBTs for High-speed and Low-Power Applications", Technical digest of the *International Electron Devices Meeting* , , pp. 854-856 Dec. 2000

[5] S.M. Sze, *Physics of Semiconductor Devices*, 2nd edition, New York: Wiley, 1981

[6] H. Kroemer, "Two Integral Relations Pertaining to the Electron Transport Through a Bipolar Transistor with a Nonuniform Energy Gap in the Base Region", *Solid State Electronics*, vol. 28, pp. 1101-1103, 1985.

[7] H. Kroemer, "Heterostructure bipolar transistors: What should we build ", *Journal of Vaccuum Science and Technology*, vol. B1, pp. 126-130, 1983.

[8] D. Burdeaux, P. Townsend, and J. Carr, "Benzocycobuthene (BCB)dielectrics for the fabrication of high density, thin film multichip Modules", *Journal of Electronic Materials*, vol. 19(2), pp. 1357-66, 1990.

[9] K. Kurishima, S. Yamahata, H. Nakajima, T. Kobayashi, and Y. Matsuoka, "Ultra-High fmax and fT InPlInGaAs Double-Heterojunction Bipolar Transistors with Step-Graded InGaAsP Collector", *IEEE Transactions of Electron Devices*, vol. 48, pp. 2595-2605, Nov. 2001

[10] M. Dahlström "Ultra high speed InP heterojunction bipolar transistors", *Ph.D dissertation, Royal Institute of Technology, Stockholm, 2003*, vol. 24, pp. 433-435, July 2003.

[11] C. Nguyen, T. Liu, M. Chen, R. Virk, and M. Chen, "Bandgap Engineered InP-Based Power Double Heterojunction Bipolar Transistors", *Proc. IEEE Int. Conf. on Indium Phosphide and Related Materials*, Cape Cod, MA, pp. 15-19, May, 1997.

[12] "Properties of INDIUM PHOSPHIDE", *INSPEC Electron EMIS Datareviews Series No 6*, 1991.

[13] Z. Griffith, M.J.W. Rodwell, X.-M. Fang, D. Loubychev, Y. Wu, J.M. Fastenau, and W.K. Lui, "InGaAs/InP DHBTs with 120 nm collector having simultaneously high f_τ, $f_{max} \geq 450$ GHz", *IEEE Electron Device Lett.*, vol. 26, August 2005.

[14] I. Harrison, M. Dahlström, S. Krishnan, Z. Griffith, Y-M. Kim, and M. J. W. Rodwell, "Thermal Limitations of InP HBTs in 80- and 160-Gb ICs", *IEEE Transactions on Electron Devices*, vol. 51, no. 4, pp. 529-534, 2004.

[15] B.G. Streetman, *Solid State Electronic Devices*, $4^t h$ edition, Prentice Hall, 1995.

[16] H.F. Cooke, "Microwave Transistors: Theory and Design" , *Proceedings of the IEEE*, vol. 59, pp. 1163-1181, 1971.

[17] M. Vaidyanathan and D.L. Pulfrey, "Extrapolated f_{max} of Heterojunction Bipolar Transistors" , *IEEE Transactions on Electron Devices*, vol. 46, pp. 301-309, Feb. 1999.

[18] C.T. Kirk, "A Theory of Transistor Cutoff Frequency (f_τ) Fall-Off at High Current Density", *IEEE Transaction of Electron Devices*, vol. ED-9, pp. 164, 1962.

[19] M. J. W. Rodwell, "ECE 202A notes", *ECE graduate course on Microwave circuit design, University of California, Santa Barbara.*

[20] J. J. Ebers, J. L. Moll, "Large-signal behavior of junction transistors, Proc. IRE, vol. 42, pp. 1761-1772, Dec. 1954.

[21] W. C. Johnson and P. T. Panousis, "Influence of Deby Length on the *C-V* Measurement of Doping Profiles", *IEEE Transactions on Electron Devices*, ED-18, pp. 965-973, 1978

[22] "ECE 218C notes", *ECE graduate course on Mixed signal IC design, University of California, Santa Barbara*.

[23] M. Urteaga, P. Rowell, R. Pierson, B. Brar, M. Dahlström, Z. Griffith, M.J.W. Rodwell, S. Lee, N. Nguyen, and C. Nguyen, "Deep submicron InP DHBT technology with electroplated emitter and base contacts", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 239-240.

[24] M. Le, G. He, R. Hess, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee, J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J-W. Lai, and M. Feng, "Self-Aligned InP DHBTs for 150 GHz Digital and Mixed Signal Circuits", *IEEE Int. Conf. on Indium Phosphide and Related Materials*, Glasgow, Scotland, May 8-13, 2005.

[25] J. Böck, H. Schäfer, H. Knapp, K. Aufinger, M. Wurzer, S. Boguth, T. Böttner, R. Stengl, W. Perndl, T.F. Meister, "3.3 ps SiGe bipolar technology", *Proc. IEEE Int. Electron Device Mtg*, San Francisco, CA, Dec. 13-15, 2004, pp. 255-258.

3

Ion Implantation in InP

ION implantation is a statistical process, where high energy ions penetrate a target surface and are slowed down in traversing matter. The ions of a material are implanted into another solid changing the physical properties of the solid. The ions impinge on the substrate with kinetic energies 45 orders of magnitude greater than the binding energy of the solid substrate.

Ion implantation is the method of choice in state of the art Si manufacturing to bring the dopants into the substrate material, mainly due to its ability to accurately control the number of implanted dopants and and to place them at the desired depth. Ion implantation works by ionizing the required atoms, accelerating them in an electric field, and directing this beam towards the substrate. When entering the substrate material the energy of the dopants decreases, while they interact with the target material. After some time the atoms come to rest at some depth depending on their initial energy. This depth has some distribution as the collisions with the target atoms are random. An important point for the device design is to know which initial energy is necessary to place the dopants at the required depth and what will be their spread. The LSS (Lindhard, Scharff, Schitt) theory [1] describes the distribution of the ions in matter based on statistical models of atom-atom collisions .

The two key parameters defining the final implant profile are fluence, also called as dose, given in ions/cm^2 and energy E (in keV). The dose or the areal flux of the ions, is related to the beam current I by the following formula:

$$\phi = \frac{I \cdot t_I}{q_i \cdot A_i} \tag{3.0.0}$$

were t_I denotes implantation time, A_i the beam area and q_i is the charge per ion. Typical beam currents and implantation doses range from $1\,\mu$A- 30mA and $\times 10^{11}$ - $\times 10^{16}$ ions/cm^2. The lowest energies used start at sub keV for ultra shallow junctions to the MeV range for deep wells. When the ions enter the substrate they continuously lose energy and momentum. There are two main effects that causes an energy loss,

- elastic collisions with the nuclei of the target material

- inelastic collisions with the electrons
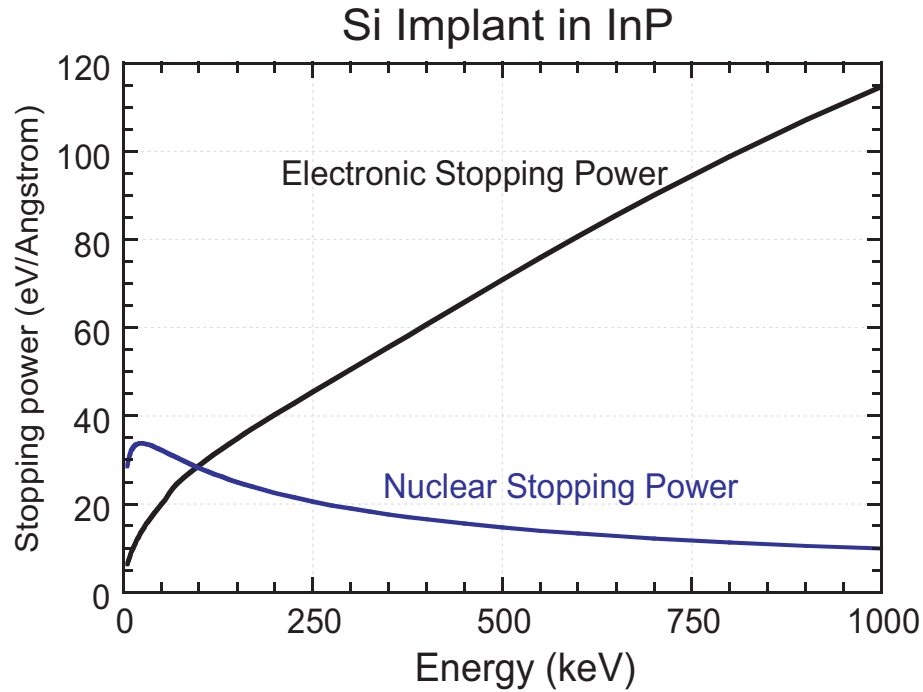
Figure 3.1: Nuclear and Electronic Stopping Power of Si implant in InP

The total stopping power S defined as the energy loss per unit path length of the ion can be defined as:

$$S = \frac{dE_{ii}}{dx}^{nuclear} + \frac{dE_{ii}}{dx}^{electronic} \tag{3.0.0}$$

where E_{ii} is the initial ion energy on impact.

$$\frac{dE_{ii}}{dx}^{electronic} \propto \sqrt{E_{ii}} \tag{3.0.0}$$

Both these components are functions of the mass of the target and incident ion and nuclear charge of the target. Fig. 3.1 is a plot of electronic and nuclear stopping powers calculated from *TRIM*, for Si implants in InP. The nuclear stopping is dominant at low energies while at high energies, the stopping is almost entirely due to the electrons of the target material, InP.

Due to the random nature of the collisions the total distance traveled (range) and its projection on the direction parallel to the ion beam (projected range) are random variables. R_p denotes the *projected range*, the depth were most ions stop. The *longitudinal projected straggle* ΔR_p, describes the statistical fluctuation of R_p. Based on the LSS theory, the implant profile (projected ranges R_p of a huge number of ions) is described by a Gaussian function since the sum of infinite random variables can be approximated by a Gaussian distribution as,

$$N(x) = \frac{n_{ii}}{\Delta R_p \sqrt{2\pi}} \cdot exp - \left(\frac{(x - R_p)^2}{2\Delta R_p^2} \right) \tag{3.0.0}$$

where $n_i i$ is the implant fluence in ions/cm^2, R_p is the implant range and ΔR_p is the longitudinal implant straggle. The profile is defined by the implanted fluence $n_i i$ in ions/cm^2, the projected range R_p in μm and the projected straggle ΔR_p in μm.

Thus, the range and straggle are functions of the implanted species, initial energy, and target material. Since each ion's final distribution is a random variable, statistical Monte Carlo simulations can predict the projected range and straggle of a huge number of ions. The software SRIM [2] is a group of programs which calculate the stopping and range of ions into matter using a full quantum mechanical treatment of ion-atom collisions. One component *TRIM* (the Transport of Ions in Matter) is a Monte Carlo Transport Calculation of ion interactions with multi-layer complex targets. It can calculate both the final 3-D distribution of the ions and also all kinetic phenomena associated with the ion's energy loss: target damage, sputtering, ionization, and phonon production while all target atom cascades in the target are followed in detail.

TRIM assumes that there is cylindrical symmetry in the final ion distributions. Thus the mean lateral range of the ions is zero while the ion straggling has its normal definition as the second moment of the lateral distribution. The lateral projected straggle thus directly describes the final distribution under an implant mask edge.

3.1 Implantation in InP

Seminal work on implantation in InP was carried out in the late 70s and early 80s by Donnelly and Hurwitz [3]. They demonstrated that Ion implantation is a feasible method to achieve either doping or isolation in InP. The magnitude of resistivity of implanted InP depends on the doping species. It is seen that activating acceptor implants are harder than donor implants. Another problem with acceptor species is their high rate of diffusion in InP. The implanted species Si, Ge, Se, S and Sn are all effective donors in InP and can produce heavily doped N-type layers. Many electronic applications require Semi Insulating(SI) InP with high resistivity of $\sim$ $\times 10^{10}$ $\Omega \cdot \mu$m. Resistivities in the SI range are usually obtained by doping with the deep acceptor Iron(Fe) or as is done in this thesis, by implanting Fe. All these implants require high temperature annealing at over 700°C.

As the implanted ions interact with the target nuclei, they can initiate a cascade of displacements. In general, the heavier ions create more damage. At high substrate temperature, defects are more mobile and more annealing can take place during the implant. It is seen in InP that there is significantly less damage if the implants are carried out at an elevated temperature over 170 °C [4]. Furthermore, the activation of the dopants and the mobility significantly improve when the implants are carried out at elevated temperatures [5]. This is attributed to a dynamic annealing process during implant. Since the implants are carried out at an elevated temperature, an implant mask should be used, that can withstand these temperatures.

During implantation, channeling can occur when the ion velocity is parallel to a major crystal orientation. The ions can travel considerable distances with little energy loss. Ion channeling can therefore produce a significant tail to the implant distributions. Most IC implantation is therefore done off-axis. A typical tilt angle is 7 °. Channeling is more a problem in single crystal materials than in III-V compounds. The power of an incident ion is

$$P_{ii} \propto V_{ii} \times J_{ii} \tag{3.1.0}$$

where J_{ii} is the ion current flux in mA/μm^2 and V_{ii} is the voltage $= E_{ii}/ioncharge$ If the incident power is transferred to the target crystal, it is dissipated as heat. In typical VLSI processes, where the implants in Si are carried out at room temperature or for damage implants in III-V's , this temperature rise can destroy the photoresist typically used as an implant mask. Therefore current is usually maintained small in such cases, usually ≤ 50 μA which means that for a given implant fluence, the implantation times can be very long and hence there is a higher probability of impurities. All implants done here are at a substrate temperature of 200 °C. Therefore, the implant current is less important for such implants. However, to not cause additional lattice heating, all implants are carried out at ≤ 50 μA.

3.1.1 High temperature annealing of implants in InP

One component of energy transfer when a high energy ion enters a wafer is collision with the lattice nuclei. Many of these atoms are ejected from the lattice during the process. Some displaced substrate atoms have sufficient energy to collide with other substrate atoms to produce additional displaced atoms. As a result, implantation process can produce considerable substrate damage that must be repaired during subsequent processing. Furthermore, if the implanted species is intended to act as a dopant, it must occupy lattice sites, here group III In sites. Both damage repair and implant activation are normally done by heating(annealing) the wafer after implant.

There exists a threshold dose above which the damage is complete. This critical dose depends on the implant energy, implant and target species and substrate temperature. As an ion passes through the crystal, point defects consisting of interstitials and vacancies are created by direct interactions with the target atoms. These are primary defects. A vacancy defect is also known as Schottky defect and an interstitial defect is called a Frenkel defect. Secondary defects occur when an implanted wafer is annealed. Secondary defects increases greatly at very high fluences near the critical dose [6].

Annealing processes are needed that minimize the secondary defects while activating the dopants. The temperature required for optimum activation of dopants in InP is well above the temperature (550°C) at which incongruent evaporation of group V species, Phosphorus P, occurs. Therefore some method of minimizing this loss is required. A common method of annealing is the proximity method where another InP wafer is placed face to face with the implanted InP substrate. As the wafers are heated up, each wafer begins to lose a small amount of P, but an overpressure is created that prevents further dissociation. This is not a satisfying solution since it relies on loss of P. Moreover it presents a safety issue when a conventional RTA chamber is used since P is highly flammable and poisonous. The best method is to anneal the InP wafer in a phosphorus atmosphere in the MBE chamber, but this choice is not available at this time at $UCSB$. Annealing in a enclosed graphite cavity with a P partial pressure is shown to be very effective even upto 900 °C [7]. A commonly used solution is the use of dielectric encapsulant such as SiO_2, Si_xN_y or Phosphosilicate glass (PSG) [3] where the wafer can be annealed in a conventional RTA.

SiO_2 is a poor encapsulant as it is hard to remove after anneal and also has vastly different thermal expansion coefficient from InP. Si_xN_y is used as an encapsulant here. In order to minimize scratching on the Si_xN_y on the top surface during backside deposition, the PECVD platen is first coated with 100-200 nm of Si_xN_y. All anneals are carried out in the Rapid Thermal Annealer(RTA) as this was the only tool available at this time. Furthermore, if the anneal is carried out at high tempera-

ture and for a short time, thermal equilibrium is not reached. Thus dopants greater than its solid solubility in InP can be activated. Stress and strain can cause cracking or a loss of adhesion, so it is important to use pinhole free Si_xN_y. Both sides of the wafer are coated with 40 nm of Si_xN_y deposited by PECVD. The quality and thickness of Si_xN_y are very critical to providing surface integrity during anneal. For annealing, the deposited Si_xN_y has to be very uniform and very smooth without
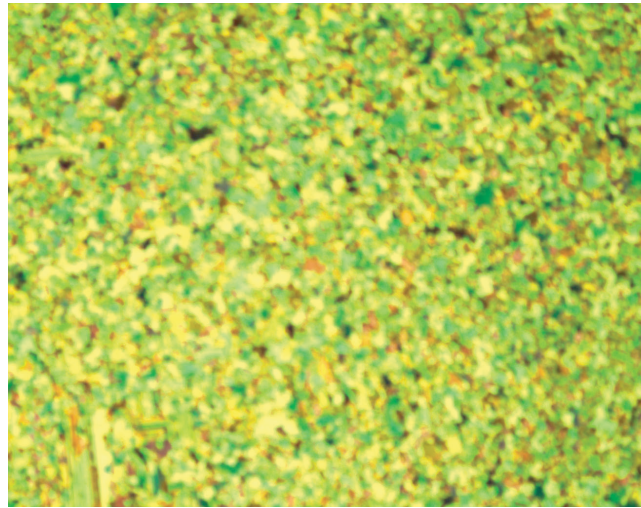
Figure 3.2: Poor quality Si_xN_y on InP

pinholes or defects. An example of poor quality Si_xN_y on InP is seen in Fig. 3.2. Si_xN_y has poor adhesion on InP and often results in a rough layer. Deposition of good quality Si_xN_y on InP is not trivial. PECVD deposited Si_xN_y adheres poorly to exposed InP surfaces. Prior to deposition, InP surfaces are treated with Ozone for 5-10 minutes. Studies by Driad *et al.* [8] showed that an ultra-violet ozone treatment (UV-ozone) is an effective way of cleaning a surface of organic and non-organic materials. The uv-Ozone also produces a uniform stoichiometric oxide film which passivates the defective surface layers associated with the native oxides of InP and those that occur due to processing. After a ten minute uv-Ozone treatment, the stoichiometric composition at the surface is restored. The oxide thus formed on InP has to be removed prior to Si_xN_y deposition. This is done by wet etching in Buffered Hydro-Fluoric(BHF) acid for 5-10 minutes, so that a clean surface of InP ensues. However, Fluorine radicals from BHF are attracted to InP surface [9]. Therefore the wafer is cleaned in running De-Ionized water (DI) for 5-10 minutes. It is seen that each of these steps is critical in ensuring a clean InP surface and hence good quality Si_xN_y as cap.

The thickness of the Si_xN_y cap is important. A thin layer of Si_xN_y ¡ 30 nm may not provide adequate surface coverage and is not reliable. A thicker Si_xN_y cap $\geq$ 60 nm results is numerous defects after anneal. The reasons are not well understood at this time. One postulate is that the Si_xN_y layer is strained and a thick cap may be relieving this strain at high temperatures leading to pinholes. The pinholes results in P desorbing from the surface and leaves behind deep pits $\sim$ 15 - 20 μm as seen in Fig. 3.4. Fig. 3.3 is such a micrograph of such a defect on the InP surface after a high temperature anneal(800 °C). Analysis of this anneal defect using Energy Dispersive X-Rays (EDX) indicates a very large concentration of Oxygen atoms. The atomic ratio of P to In is slightly lower.

Pitting on the surface of
InP after anneal ~ 1 µm

Element (Outer Shell)	Wt %	At %
C (K)	3.63	11.44
N (K)	0.00	0.00
O (K)	20.71	48.92
Si (K)	1.89	2.54
P (K)	14.37	17.54
In (L)	59.40	19.56
Total	100	100
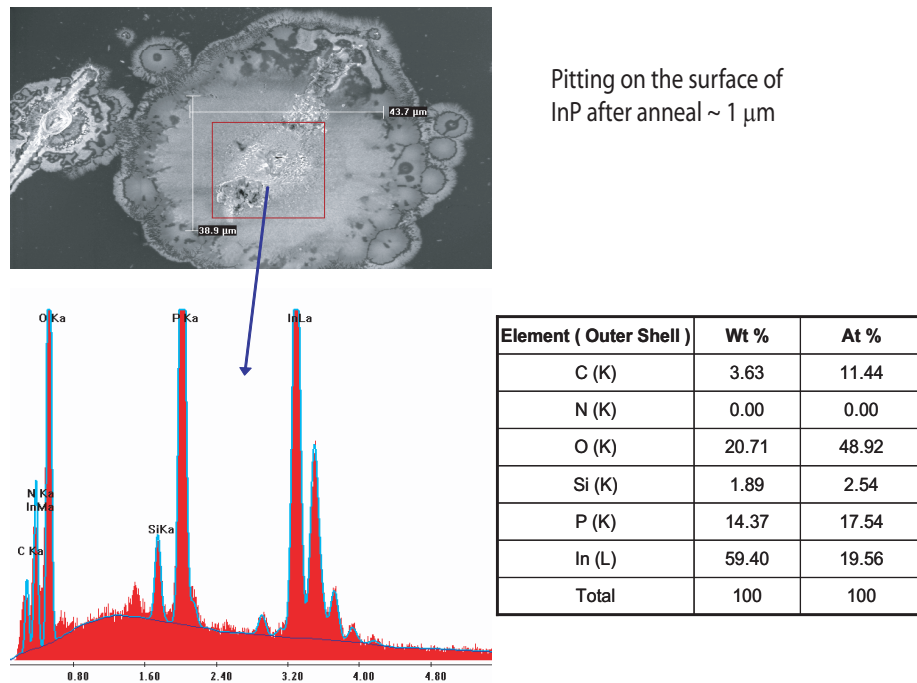
Figure 3.3: Rectangular pit formation on InP after high temperature anneal and EDX compositional analysis

The complete removal of Si_xN_y after anneal is critical. High temperature anneals cause the dielectric encapsulant to become stoichiometric and dense. These are typically harder to remove after such high temperature treatments. This was the main reason for rejecting SiO_2 as an encapsulant. It is seen that a long treatment in BHF ($\sim$ 10 minutes) is sufficient to remove this Si_xN_y cap. Fig. 3.5 is an EDX spectra of the InP surface after the Si_xN_y is removed in BHF and there is no

18 μm pitting on the surface after anneal due to failure of the cap
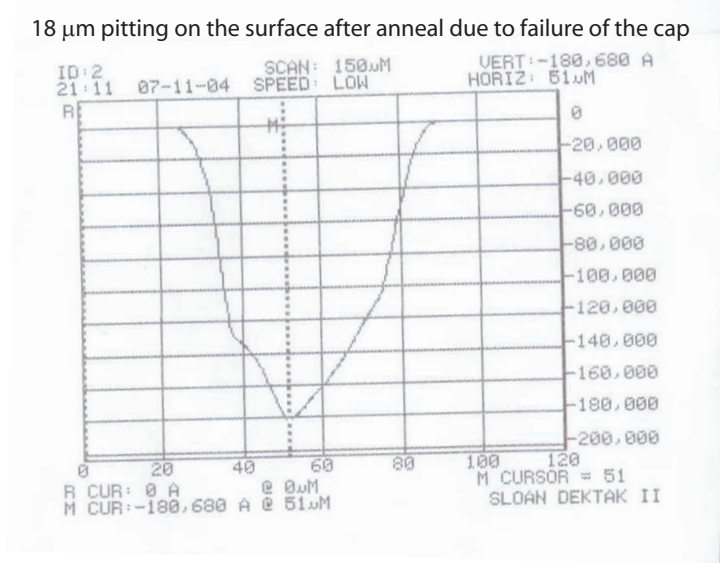
Figure 3.4: Pit formation on InP after high temperature anneal

evidence of Si_xN_y present.

One important consideration is the residual stress of the encapsulant [10]. Compressive stress may cause undesired buckling and cracking may occur if the tensile stress is too high. The bulk stress consists of an intrinsic and thermal part. The total bulk stress ($\sigma_{bulk,total}$) in dielectric PECVD layers is given by

$$\sigma_{total} = \sigma_{int} + \sigma_{th} \tag{3.1.0}$$

where σ_{int} and σ_{th} are the bulk intrinsic and thermal stress respectively. The thermal stress only results from the temperature change between deposition and anneal and the difference in thermal expansion coefficients of the film and the substrate. The thermal stress is given by

$$\sigma_{th} \propto (\alpha_f - \alpha_s)\Delta T \tag{3.1.0}$$

where α_f α_s are the thermal expansion coefficients of the film and substrate respectively. An encapsulant should therefore ideally have a thermal expansion coefficient similar to InP to prevent thermal stresses. Between 300 and 673K, the thermal expansion coefficient of InP is $4.6 \times 10^{-6}/^{\circ}$ K while that of Si_xN_y is $\sim 3.2 \times 10^{-6}/^{\circ}$ K. SiO_2 has a thermal expansion coefficient of $0.5 \times 10^{-6}/^{\circ}$ K which makes it less suitable as an encapsulant for InP.

In the long term however, annealing of InP in a phosphorus overpressure in a fully sealed chamber seems to be the best solution.

46

Element (Shell)	Wt %	At %
C (K)	3.66	18.39
F (K)	0.76	2.40
P (K)	20.78	40.23
In (L)	74.80	39.07
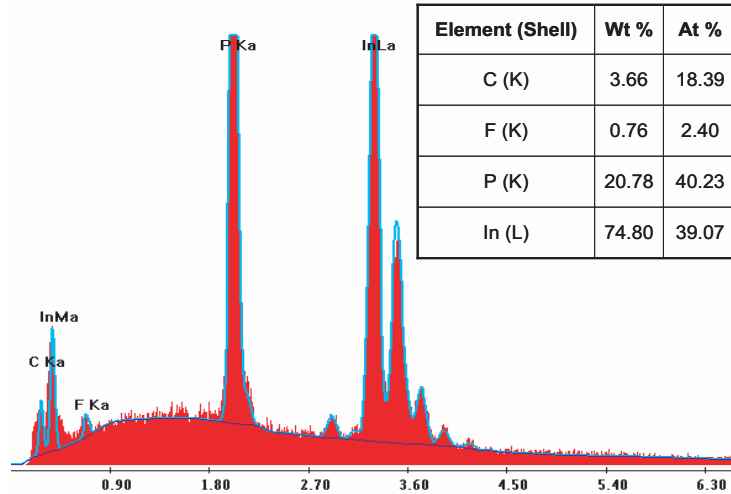
Figure 3.5: Analysis of the InP surface after anneal and cap removal

3.1.2 Si implantation in InP

N-type dopants implanted in InP have been shown to have an activation ≥ 80 % even when the doping levels is $\sim 1 \times 10^{19}$ cm^{-3} [11]. Si, Se and S are commonly used dopants. Among these Si is the lightest element and causes minimum damage. It has little diffusion which is not the case with S [12] and therefore the lateral spread can be better controlled with Si implants. Here, Si implantation is done wherever N-doping is required. The commercially available ion implant systems available at this time could do a maximum of 350 keV at a substrate temperature of 200 °C. Fig. 3.6 shows the distribution of Si in InP, as estimated by TRIM, when implanted at 350 keV. TRIM does not account for differences due to implant temperatures. Also this plot is a plot of ion range in atoms-cm^{-3}/ atoms-cm^{-2}. When multiplied by the dose in ions/cm^2 or (atoms-cm^{-2}) it gives the distribution of Si in cm^{-3}.

The Ion recoil distributions are seen in Fig. 3.7a. These are all the In and P atoms knocked out of their lattice sites, creating vacancies. The distribution of In and P recoils is shallower than the range of the Si (Fig. 3.6). Near the end of the Si tracks, the ions do not have enough energy to create massive cascades. At the peak of the damage plot in Fig. 3.7a, the vacancy rate of *In* is ~ 0.4 vacancy/ion-Å.For a dose of 5×10^{14} ions/cm^2, there are 2×10^{22} vacancies-cm^{-3}. The atomic concentration of In is 5.6×10^{22} atoms-cm^{-3}. The damage is therefore $\sim 35\%$. This is a pessimistic estimate. Due to elevated substrate temperature, $\sim 90\%$ of the damage is repaired
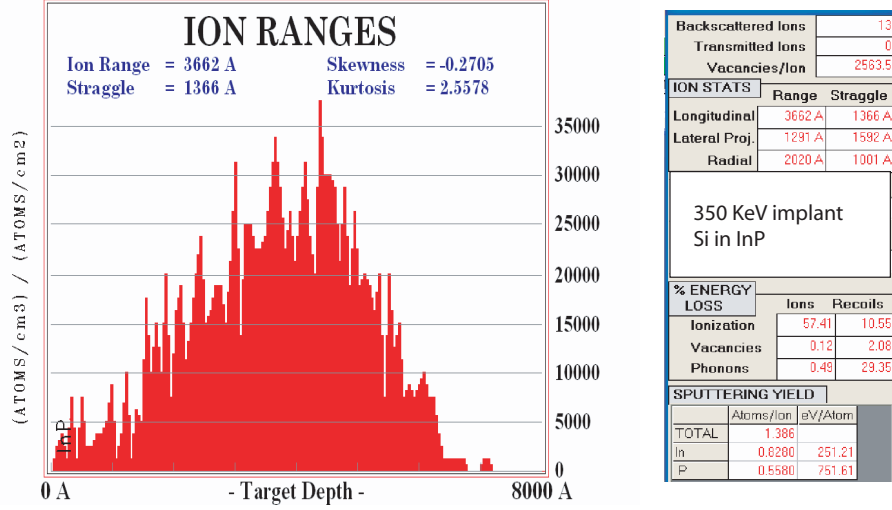
Figure 3.6: Ion Ranges for Si in InP at 350 keV

during implant. Therefore the InP crystal damage is ∼3.5 % and the implant layers are not quite amorphous.

Fig. 3.7b indicates the energy lost to recoiling target atoms that give rise to vacancies. From the plot, ∼ 200 keV of the ions energy is transferred to the recoiling In atoms. This can be estimated by assuming a constant energy transfer of ∼25 eV/ion-Å over a depth of 8000Å. So the total energy transfer to In recoils is ∼200 keV. Also, it is seen that the energy transfer to phonons is almost exclusively from the recoiling target atoms. An atom is knocked off its lattice site, giving rise to a vacancy when the energy is greater than the lattice binding energy. The total displaced atoms from their lattice sites is usually quantified as damage due to implant. These atoms leave behind vacancies and may form interstitials.

The Nuclear stopping power and electronic stopping power is also calculated from *TRIM*. At 350 keV the stopping power in eV/Å is,

$$S_n = \frac{dE_{ii}}{dx}^{nuclear} = 17.69 eV/\mathring{A} \tag{3.1.1}$$

$$S_e = \frac{dE_{ii}}{dx}^{electronic} = 55.65 eV/\mathring{A} \tag{3.1.2}$$

From the projected range and longitudinal straggle obtained from TRIM, and assuming a Gaussian distribution, the implanted profile of Si is plotted in Fig. 3.8. Also shown are the doping levels with 60 % and 100 % activation of the Si dopants.

Ion Recoil Distributions

Energy to Recoil Atoms

Figure 3.7: Ion Ranges for Si in InP at 350 keV

With 60 % activation, the average doping is $\sim 5 \times 10^{18}$ cm^{-3} over 6000 Å, and using a mobility of $\sim 1000 \; cm^2/V \cdot s$, the expected sheet resistance is $\sim 21 \; \Omega/\square$.

The lateral straggle is given as 1592Å. As discussed, cylindrical symmetry is used. Since the offset angle is small, the lateral range is assumed to be zero. The lateral distribution can be expressed as,

$$N(z) = N(x) \cdot exp - \left(\frac{z^2}{2\Delta R_z^2} \right) \quad (3.1.2)$$

where R_z is the lateral straggle distance. Lateral straggle is the distance in z when the concentration reduces to $e^{-1/2}$ of its peak value. The peak activated value (at the implant mask edge) is a function of x as seen in Fig. 3.8 and is $\sim 1 \times 10^{19}$ cm^{-3}. The lateral distribution is plotted in Fig. 3.9. The point at which the Si doping falls below the Fe doping present in SI InP, the region become Semi-Insulating again. In this dissertation, this is important and is defined as the lateral straggle due to Si implant. This straggle is $\sim 0.5 \; \mu$m. Table 3.1 lists the projected range and longitudinal and lateral straggle for Si at various energies in InP from Monte Carlo simulations.

Figure 3.8: Si doping profile in SI InP at 350 keV

Table 3.1: Silicon Implant in InP as calculated by *TRIM*

Implant energy	Projected Range	Longitudinal Straggle	Lateral Straggle
5	92	52	54
10	159	91	85
40	496	256	286
90	1020	490	540
140	1556	696	800
200	2204	902	1060
350	3662	1366	1592
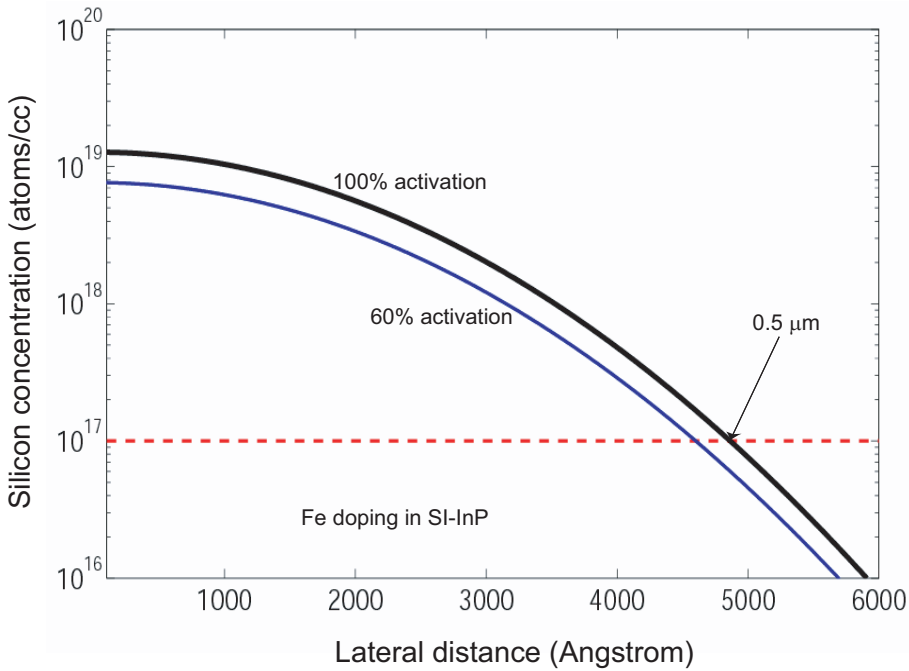
Figure 3.9: Lateral straggle of the 350 keV Si implant

Table 3.2: Implant conditions for basic, implanted subcollector HBT process

Implant species	Implant energy	Implant fluence	Offset angle	Implant temperature
Si	140 keV	3×10^{14} ions/cm^2	7 $^\circ$	200 $^\circ$ C
	40 keV	8×10^{13} ions/cm^2		
	10 keV	3×10^{13} ions/cm^2		
$I_{ions} \leq 10\mu$A				

Si implants are performed at the implant conditions stated in Table 3.2. After implant, the wafers were capped with Si_xN_y and annealed at various temperatures and times. Table 4.7 gives the mobilities and sheet charge density. It has been

Table 3.3: Hall measurements of resistivity and mobility for Si implants

Anneal temperature ($^\circ$C)	Anneal time (s)	Hall mobility ($cm^2/V \cdot s$)	Carrier density (cm^{-2})	Sheet resistance ($\Omega/\square$)
750	30	999	1.22×10^{14}	51.3
800	15	868	1.70×10^{14}	42.3
800	30	909	1.66×10^{14}	41.5
825	15	874	1.87×10^{14}	38.3
850	15	879	2.11×10^{14}	33.7

reported [11] that short anneals at temperatures over 775 $^\circ$C is required for complete activation of donor implants. However, above 800 $^\circ$C the Si_xN_y cap is not stable and there are numerous anneal defects throughout the wafer. The activation of Si for 800°C anneal is ~60%. Phosphorus(P) co-implantation is known to greatly increase the activation of Si. Si acts as donor only if it substitutes In atoms in the lattice. Co-implanting P increases this possibility. The profile of Si implant is obtained from SIMS and is shown in Fig. 3.10. It deviates little from the *TRIM* simulations.

The sheet resistance obtained above is high for the applications discussed in later chapters. Therefore the implant energy is increased, to enhance the implant depth. The details are in Chapter 4 . AFM scans in Fig. 3.11 of the implanted and annealed wafers indicate that the surface quality is restored to its original state after annealing at 800 $^\circ$C.
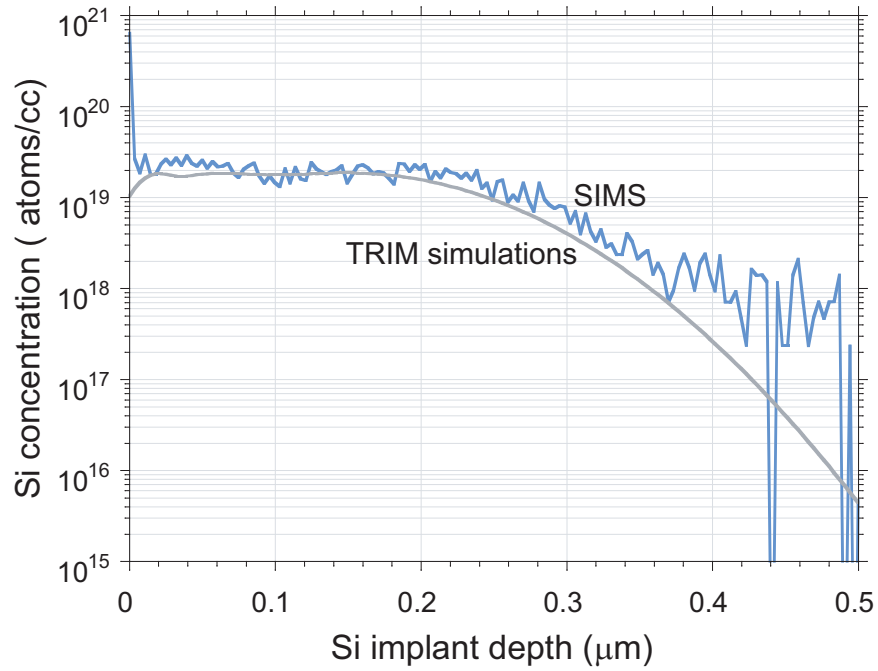
Figure 3.10: Si doping profile in InP at 140 keV from SIMS and simulated by *TRIM*

Virgin SI InP wafer
RMS roughness: 0.4 nm

As implanted
RMS roughness: 1.274 nm

After 800°C anneal
RMS roughness: 0.367 nm
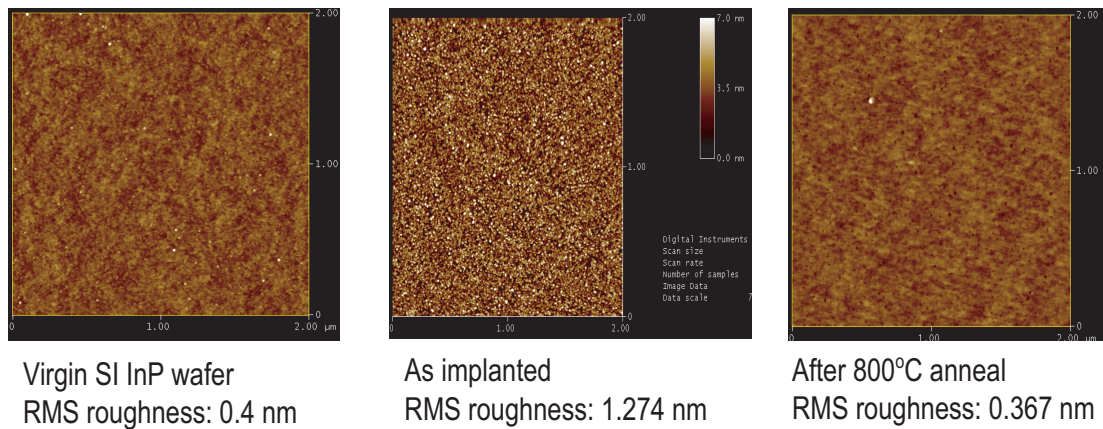
Figure 3.11: AFM scans of the implanted surface

3.1.3 Fe implantation in InP

Iron (Fe) is a mid gap acceptor in InP. Fe is a transition metal with tightly bound orbitals and hence a small Bohr Radius. Fe atoms occupy the In sites substitutionally and act as deep acceptor centers for free electrons. Indeed, SI InP substrates are formed by doping the crystal, during the Liquid Encapsulated Czochralski (LEC) growth phase, with Fe. Fe typically exists in InP with an oxidation state of +3 and it can accept one electron to reduce its oxidation state of +2.

Isolation can also be done by implantation. However in InP, implant isolation has not been as effective in creating high resistivity regions as in GaAs. The ion species H, He, B, O2 are utilized to create damage implants in n-type InP and, the reported value of 1 MΩ/$\square$ is insufficient for device isolation. Fe Implantation can be used to create deep levels; this chemical compensation ensures the crystallinity of the semiconductor after high temperature anneal. Isolation by chemical compensation is more apt if there is a requirement of subsequent regrowth of crystalline layers. Full compensation is achieved when the concentration of the deep acceptor levels N_A, exceeds the background doping N_D, the Fermi level E_F, is approximately pinned at E_A, the deep acceptor level due to Iron which is ~0.6eV below the conduction band [13]. This result is derived as follows. Consider a semiconductor with a shallow donor of active density N_D and a deep acceptor at E_f and active density N_A. n is the number of conduction band electrons and p is the number of valence band holes. Assuming Boltzmann statistics,

$$n = N_C e^{-(E_C - E_F)/kT} \tag{3.1.3}$$

$$p = n_i^2/n \tag{3.1.4}$$

where n_i is the intrinsic concentration in the semiconductor. The Fe acceptor has a negative charge if occupied and neutral if empty. The occupation of acceptors is given by,

$$n(E_A) = \frac{N_A g_A}{g_A + e^{-(E_F - E_A)/kT}} \tag{3.1.5}$$

$$p(E_A) = N_A - n(E_A) \tag{3.1.6}$$

where g_A is the degeneracy of the acceptor states. g_A is usually 4. Charge neutrality dictates that,

$$n + n(E_A) = p + N_D^+ \text{ where, } p = n_i^2/n \tag{3.1.6}$$

Complete ionization of the donor states is assumed. $n(E_A)$ can be simplified as,

$$n(E_A) = \frac{N_A}{1 + \theta/n} \text{ where,} \tag{3.1.7}$$

$$\theta = \frac{N_c}{g_A} exp \frac{E_A - E_C}{kT} \tag{3.1.8}$$

The charge neutrality equation can therefore be written in simplified form as,

$$n + \frac{N_A}{1 + \theta/n} = N_D^+ + \frac{n_i^2}{n} \text{ or,} \tag{3.1.9}$$

$$\frac{n^2}{N_D^2} + \left(\frac{N_A/N_D}{1 + \theta/n} - 1\right)\frac{n}{N_D} - \frac{n_i^2}{N_D^2} = 0 \tag{3.1.10}$$

If $N_A/N_D \geq 1$ and the semiconductor become semi-insulating, or intrinsic, then the number of conduction electrons is determined by the thermal generation, or $n = n_i$. In that case,

$$\frac{N_A/N_D}{1 + \theta/n} = 1 \text{ or,} \tag{3.1.11}$$

$$n = \frac{\theta}{x - 1} \text{ where, } x = \frac{N_A}{N_D} \tag{3.1.12}$$

or expanding θ and n from Eqn.3.1.4 and Eqn.**??** one obtains,

$$E_F = E_A - kTln[g_A(x - 1)] \tag{3.1.12}$$

As mentioned, this expression is only valid when $x = \frac{N_A}{N_D} \geq 1$. A plot of the Fermi level with x is given in Fig. 3.12. As evident from the figure, the Fermi level is pinned at the acceptor level even when $x = 20$. This is the reason why mid gap acceptors are used to compensate residual donors, when a SI semiconductor are needed. When the Fermi level is above the acceptor level, the acceptor states are filled. Since all the acceptor states are below the donor energy levels, the electrons preferentially occupy the acceptor sites. This means that the donor states are ionized and, if the donor density is less than the acceptor density, the conduction band is $\approx$ empty. In this case the Fermi level is at $\approx E_A$. Suppose more donors are added. First, all the acceptor states are completely filled. The remaining donors then ionize so that their electrons move into the conduction band. In this case, the Fermi level approaches the donor level as seen from Fig. 3.12.

The solid solubility of Fe in InP is 1×10^{17} cm^{-3}. However, this can be overcome during implantation, since it is essentially a non equilibrium process. Donnelly and Hurwitz first reported the effect of iron bombardment in InP. Since then, numerous studies have been conducted using iron implantation in InP [13, 14, 15]. Earlier work indicates [11] that prolonged anneal at temperatures over 650 °C is required for damage removal and complete activation of acceptor implants. Indeed, resistivities as high as 2×10^7 Ω-cm have been obtained, for Fe implanted in N^{++} doped InP(1×10^{14} cm^{-3}), after 650 °C anneal. However, room temperature implantation of Fe produces an amorphous implant region which results in significant defects even after anneal [16].
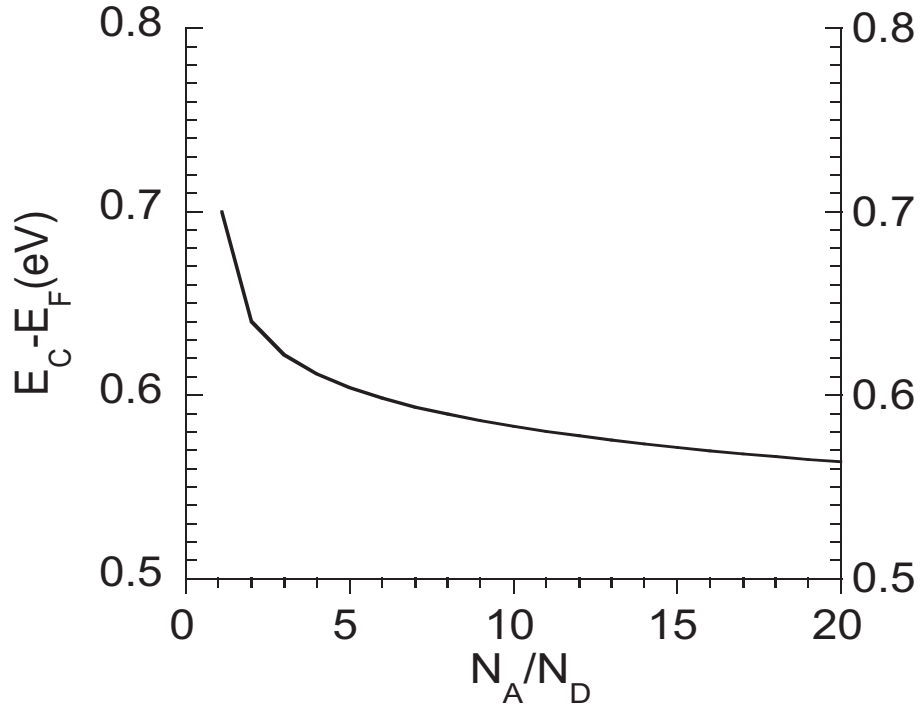
Figure 3.12: Fermi levels for various degrees of deep level compensation

---

To study the effect of Fe in N^{++} InP, Fe is implanted at 190 keV with a fluence of 4×10^{15} ions/cm^2 into epitaxially grown 130 nm N^- InP and 80 nm N^{++} InP. This was carried out at 200 °C to minimize crystal damage and increase Fe activation, which occurs due to enhanced dynamic annealing at this temperature [17]. As before, the post implant is carried out in a conventional a conventional RTA. Fig. 3.13 shows the SIMS profiles of Fe in the as-implanted and annealed wafers and also the theoretical LSS profile from *TRIM*. There is significant deviation from the theoretical profile, in that

- the Fe penetration is deeper than predicted by the TRIM software

- a reduction in the peak concentration

- a pileup of Fe at the surface

. These results concur with that reported earlier [18, 19, 15]. Several arguments exists to explain this phenomena. Fe tends to accumulate near the maximum damage
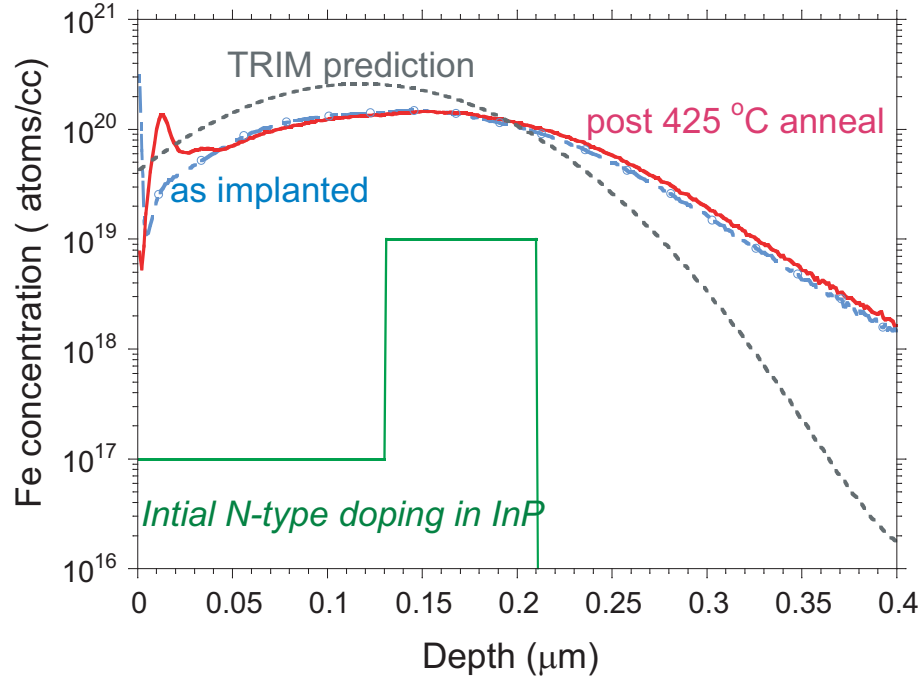
Figure 3.13: Fe profile in 130nm N^-/80nm N^{++} InP at 190 keV/4×10^{15} ions/cm^2 from SIMS and as simulated by *TRIM*

region with peaks at around $R_p + \Delta R_p$ of the Fe implant. This discrepancy is explained by the enhanced diffusivity of Fe in the amorphous phase [20]. The diffusion coefficient is $\sim 1 \times 10^{13}$ cm^{2}s^{-1}. Furthermore such accumulation at certain points, occur when the Fe implant fluence exceeds a certain amorphization threshold. This threshold is 1×10^{13} ions/cm^2 when implanted at room temperature [20] and between 2 and 5 $\times 10^{14}$ ions/cm^2 when implanted at 200 °C. A depletion of Fe atoms is also observed and this larger when the damage is higher. The Fe atoms are gettered and/or trapped at the secondary defects formed during annealing. Reconstruction of an amorphous layer is complicated and strongly influences the redistribution properties of Fe. . The RBS plots in Fig. 3.14 indicate the presence of an amorphous region upto a depth of 104 nm for the implant performed at 190 keV with a fluence of 4×10^{15} ions/cm^2. The anneal at 425°C is not sufficient to repair the crystal damage. As evident from SIMS, the implanted Fe concentration is well over the Si N-type doping in the structure. Fig. 3.15 shows a plot of measured resistivity of the sample with anneal temperature; the as-implanted sheet resistance is 3 M$\Omega/\square$. At temperatures of 500°C and above, the resistance of the Fe implanted layers drops.
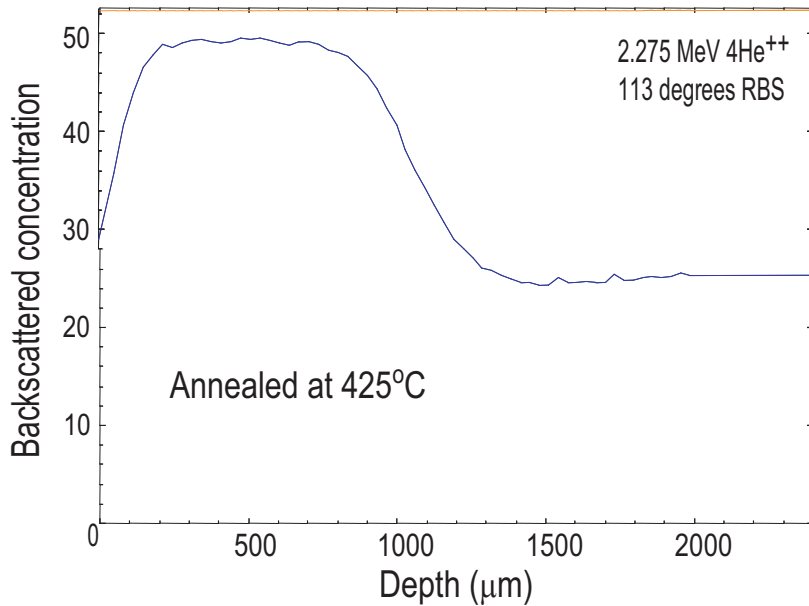
Figure 3.14: RBS plots indicating an amorphous region after anneal

Evidently, Fe does not fully compensate the Si electrically and RBS plots also indicate a thick amorphous layer. The data therefore suggests that conduction seen in the wafer is through hopping between the Fe sites, due to its high density. An anneal is also performed at 725 °C for 15 minutes, as suggested in the literature [13]; the sheet resistance is seen to be 70 $\Omega/\square$. At the chosen implant conditions, it is difficult to fully chemically compensate the high N^{++} doping. This could be due to formation of FeP precipitates, or due to the solubility limit of Fe in InP. It been reported that FeP precipitates were formed in CBE grown Fe doped InP above an Fe concentration of 2×10^{19} cm^{-3}, and the resistivity is seen to drop [21]. Some authors [22] have indeed resorted to using damage Iron implants for isolation. They obtain 5 M$\Omega/\square$ for a room temperature implant. However the amorphous nature of the implant renders it unsuitable for subsequent crystalline regrowth.

56Fe is a heavy element (compared to 28Si) and therefore creates a lot of damage to the crystal lattice during the implant process. Shown in Fig. 3.16 is the number of vacancies produced for Fe implanted at 150 keV, due to collisions with ions and recoiling atoms. The damage density is calculated for a dose of 5×10^{14} ions/cm^2 is
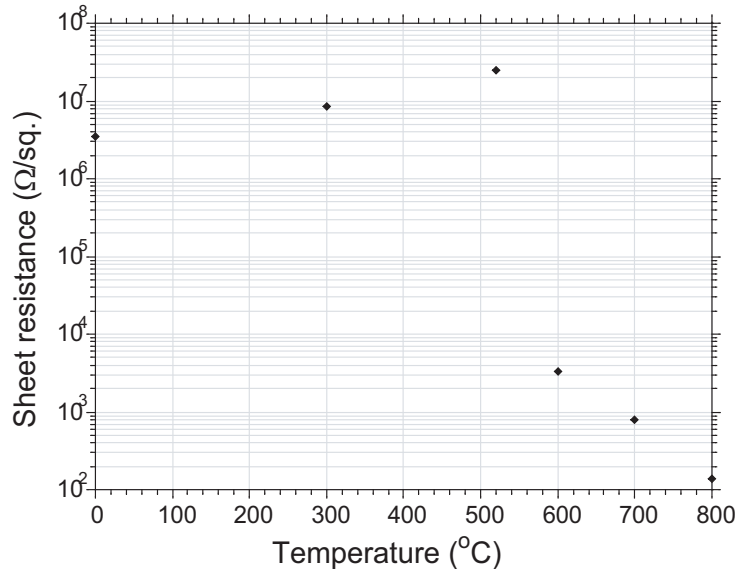
Figure 3.15: Resistivity with anneal for Fe implanted in 130nm N^-/80nm N^{++} InP at 190 keV/4$\times$10^{15} ions/cm^2

to be $\sim 5\times10^{22}$ atoms-cm^{-2}, almost 100 % damage. This calculation ignores the dynamical annealing present during implants at elevated temperatures, but as seen from RBS and in Chapter 5 , the implanted material is almost completely amorphous even when the implants are carried out at elevated temperature. This amorphous layer also influences certain chemical properties and this layer is seen to etch rapidly in BHF. It will be shown in Chapter 5 that annealing above 700 °C for long periods ($\geq$ 5 minutes) can anneal the damage completely for moderate doses (upto 2×10^{14} ions/cm^2) and energies upto 150 keV. It was seen from the RBS plots and the resistivity data that it is difficult to anneal the damage when the implant dose is above a certain threshold. Previous work suggests that this dose increases with implant temperature [17].

One important parameter ignored in this discussion is the lateral straggle of Fe. At 190 KeV, $\Delta R_z = 650$Å. The straggle becomes important when selectively masked implants are performed but throughout this work, Fe is implanted non selectively. Therefore, the lateral straggle is ignored here.
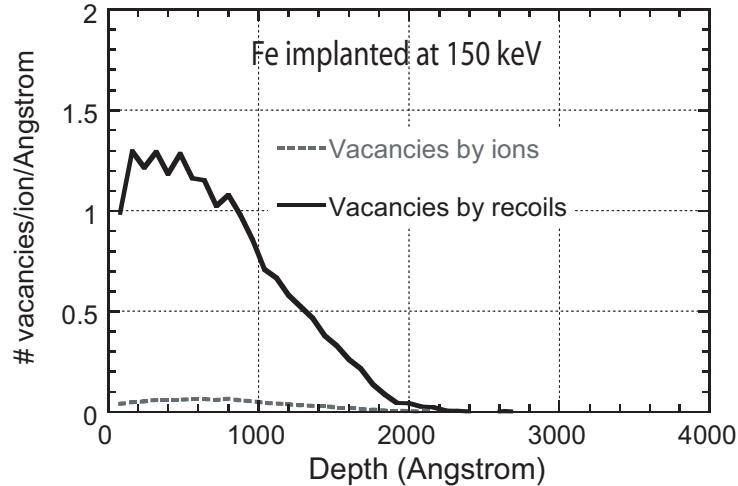
Figure 3.16: Damage in InP due to Fe implanted at 150 keV

3.1.4 Co-Implantation of Si and Fe

Si and Fe can be co-implanted as is done is Chapter 5 . Since Si and Fe re
activated only when they preferentially occupy group III sites, they both compete
for In sites, when co-implanted. If Fe is implanted first, annealed and then Si is
implanted, it has lesser group III sites to occupy. Hence the activation is reduced,
albeit marginally. Co-implantation has yielded schottky-N^{++} diodes. The Si is
implanted deep at 350 keV and Fe compensates the top 150 nm to form a SI region.

3.2 Mask for Implantation

. Traditionally in the Si VLSI industry, photoresist(PR) is used to mask the im-
plant. Since all the implants performed here, are heated implants, it rules out any PR
implant mask. Metal can be used as an efficient mask for implants. However, metals
can be difficult to remove. SiO_2 or Si_xN_y can also be used as mask. However, Si_O2
has a lower density than Si_xN_y and is therefore less efficient in stopping the ions.
Thermally deposited Si_xN_y has a density of $\sim$ 3.2 g/cc, while plasma deposited
Si_xN_y (at $<$ 300 °C) has a large concentration of hydrogen (10 -35 %) which lowers
its density to 2.4 - 2.8 g/cc [23]. Here, Si_xN_y is used as an implant mask whenever
selective implantation is carried out. Fig. 3.17 shows the profile of Si implants (300
keV/6$\times10^{14}$ ions/cm^2) with 1μm Si_xN_y on InP. As seen from the figure, the density
of Si at Si_xN_y-InP boundary is $\sim$ 1$\times10^{16}$ cm^{-3} which is not sufficient to cause N-
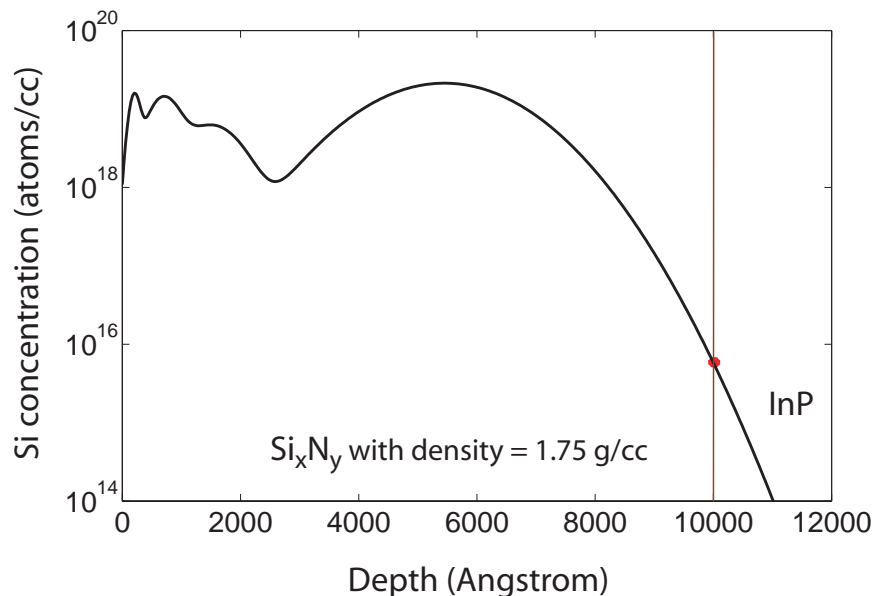
Figure 3.17: Si_xN_y implant mask for 300 keV Si implant in SI InP

type doping. Since the density of Si_xN_y from the PECVD is not exactly known, a much thicker mask than is predicted by *TRIM* is often used.

3.3 Growth on Implanted substrates

For fully crystalline growth, one of the requirements is a crystalline semiconductor and excellent surface morphology. As discussed in §3.1.1, the Si_xN_y has to be completely removed after anneal. Any Nitride remaining will cause poor growths and the Reflection-high energy electron diffraction (RHEED) signal patterns to be spotty. Fig. 3.5 is evidence that the process developed here results in complete removal of the Si_xN_y encapsulant after anneal. As will be seen in Chapter 4 and Chapter 5 , anneal conditions developed for Si and Fe implants result in a crystalline semiconductor and in excellent growth morphology. Several published results exists for MBE growths on implanted InP substrates and epitaxial layers. Dodabalpur et al. demonstrated InAlAs/InGaAs HBTs with good DC characteristics grown on Si implanted InP substrates [24]. High speed HBTs and IC technologies have been demonstrated for layers overgrown on Si implanted epitaxial material [25, 26].

MBE growth is initiated after a surface treatment consisting of a 10 min. ultra

violet(uv) ozone treatment followed by 5 min in BHF and 5 min. in DI water. As explained in §3.1.1, uv-ozone is an effective way of cleaning a surface of organic and non-organic materials and to form a stoichiometric oxide film. The BHF treatment removes this oxide. Prior to MBE growth standard oxide desorption is performed to rid the surface of remaining oxides. The RHEED patterns are seen to be streaky, indicative of excellent crystalline growth and the surface is observed under high resolution optical and electron microscopes to be comparable to fully epitaxial layers.

Having set a background into Si and Fe implantation in InP, Chapter **??** and Chapter 5 will explore practical applications of these implants for high speed devices.

References

[1] J. Lindhard, M. Scharff and H. E. Schiott, "Range Concepts and Heavy Ion Ranges", *Mat. Fys. Medd. Dan. Vid. Selsk.*,Vol. 33, No. 14, 1963

[2] J. Ziegler, "Stopping Range of Ions in Matter", *www.srim.org*

[3] J. P. Donnelly and C. E. Hurwitz, "Ion-implanted n- and p-type layers in InP", *Applied Physics Letters*, Vol. 31, pp. 418420, 1977

[4] J. P. Donnelly and C. E. Hurwitz, "The effect of implant temperature on the electrical", *Solid State Electronics*, Vol. 23, pp. 943-948, Sep. 1980

[5] G. Ciatto a, F. D'Acapito, B. Fraboni, F. Boscherini, N. El Habra, T. Cesca, A. Gasparotto, E.C. Moreira, F. Priolo "Local structure of Iron implanted in Indium Phosphide", *Nuclear Instruments and Methods in Physics Research* B 200, pp. 100104, 2003

[6] S. A. Campbell, "The Science and Engineering of Microelectronics Fabrication", Oxford University Press, $26nd$ edition, New York, 2001

[7] S. J. Pearton, "Ion beam processing and rapid thermal annealing of InP and related compounds", 2nd *International Conference on Indium Phosphide and Related Materials*, pp. 379-388, 1990

[8] R. Driad, W.R. McKinnon, Z.H. Lu, and S.P. McAlister, "Effect of UV-Ozone Oxidation on the Device Characteristics of InP-based Heterostructure Bipolar Transistors", *Journal of Electronic Materials*, Vol. 29, No. 12, 2000

[9] James W. Raring, Erik J. Skogen, Steven P. Denbaars and Larry A. Coldren, "A study of regrowth interface and material quality for a novel InP-based architecture",*Journal of Crystal Growth*, vol. 273, pp. 26-37

[10] A Tarraf, J Daleiden, S Irmer, D Prasai and H Hillmer, "Stress investigation of PECVD dielectric layers for advanced optical MEMS", *Journal of Micromechanics and Microengineering*, vol. 14, pp. 317323, 2004

[11] "Properties of INDIUM PHOSPHIDE", *INSPEC Electron EMIS Datareviews Series No 6*, 1991.

[12] M. V. Rao, "High-Energy (MeV) Ion Implantation and its Device Applications in GaAs and InP", *IEEE Transactions on Electron Devices*, Vol. 40, No. 6, Jun. 1993

[13] J. Cheng et al., "Semi- Insulating properties of Fe-implanted InP. I. Current limiting properties of n+ - semi insulting n+ structures", *Journal of Applied Physics*, Vol. 58(5), pp. 1780-1786, Sep. 1985

[14] S. J. Pearton et al., "Implant-induced high-resistivity regions in InP and InGaAs", *Journal of Applied Physics*, Vol. 66(2), pp. 656-662, Jul. 1989

[15] A. Gasparratto et al., "High-resistance buried layers by MeV Fe implantation in n-type InP", *Applied Physics Letters*, Vol. 75(5), pp. 668-670, Aug. 1999

[16] J. Vellanki, "MeV Fe and Co implants to obtain buried high resistance layers and to compensate donor implant tails in InP", *Journal of Applied Physics*, Vol. 73(3), pp. 1127-1132, Feb. 1993

[17] E.F. Kennedy, "Damage and re-ordering of ion-implanted layers of InP", *Applied Physics Letters*, Vol. 38(5), pp. 375-377, Mar. 1981,

[18] S.A. Schwarz et al., "Annealing behavior of ion-implanted Fe in InP", *Journal of Applied Physics*, Vol. 58(4), pp. 1698-1700, Aug. 1985

[19] H. Ullrich et al., "Redistribution of Fe and Ti implanted into InP", *Journal of Applied Physics*, Vol. 70(5), pp. 2604-2609, Sep. 1991

[20] A. Carnera, , "Production of Semi-Insulating Buried layers in epitaxially grown InP by Fe ion implantation", *Journal of Applied Physics*, Vol. 76(9), pp. 5085-5094, Nov. 1994

[21] Tsang et al., "Iron doped semi-insulating InP grown by Chemical beam epitaxy", *Applied Physics Letters*, Vol. 54(23), pp. 2336-2338, Jun. 1989

[22] Too et al., "Electrical isolation of n-type InP layers by Helium implantation at variable substrate temperatures", *Nuclear Instruments and methods in Physics research B*, Vol. 188, pp. 205-209, 2002

[23] P.K. Chu, "*http://personal.cityu.edu.hk/ appkchu/AP4120/7v.pdf*, Class Notes, City University of Hong Kong.

[24] A. Dodabalapur and T.Y. Chang, "Molecular Beam epitaxial growth of In-GaAlAs/InGaAs heterojunction bipolar transistors on highly resistive low temperature InAlAs epilayers", *Applied Physics Letters*, Vol. 61, Dec. 1992

[25] Mary Y. Chen, Marko Sokolich, David H. Chow, Steven Bui, Yakov Royter, Donald Hitko, Stephen Thomas III, Charles H. Fields, Rajesh D. Rajavel, and Biqiang Shi, "Patterned n Implant Into InP Substrate for HBT Subcollector", *IEEE Transactions on Electron Devices*, Vol. 51, No. 10, Oct. 2004

[26] M. R. Frei, J. R. Hayes, H. F. Shirokmann and C. Caneau, "Regrowth of $In_{0.53}Ga_{0.47}As$/InP p^+n heterojunctions by organometallic chemical vapor deposition", *Journal of Applied Physics*, Vol. 70, pp. 3967-3969, 1991

4

Implanted Subcollector DHBTs

HETROJUNCTION bipolar transistors are mostly fabricated in a triple mesa process. While these have achieved tremendous performance [1, 2] at the current scaling generation, there exists several issues that must be solved before scaling them further. Fig. 4.1 is an micrograph of a standard triple mesa HBT at UCSB [3]. In this device there is a significant portion of the base metal that lies outside the device active region. On the base access pad, is the base post which is ≈ 1 μm in height. This connects the base metal to the top level metal interconnect. The base post, and hence the access pad have to be ≥ 2 μm^2 in order to achieve a reliable and low resistance contact with the metal interconnect. As shown in the cross sectional view of the device in Fig. 4.2, the base pad contributes to the base collector capacitance.

As discussed in Chapter 2 , this base pad capacitance becomes an important parasitic as transistors are scaled. Low power logic can be achieved by using low current levels. However, to not impact the bandwidth, high current densities should be maintained. This necessitates the use of shorter length devices. Eqn.3.3 is repeated here.
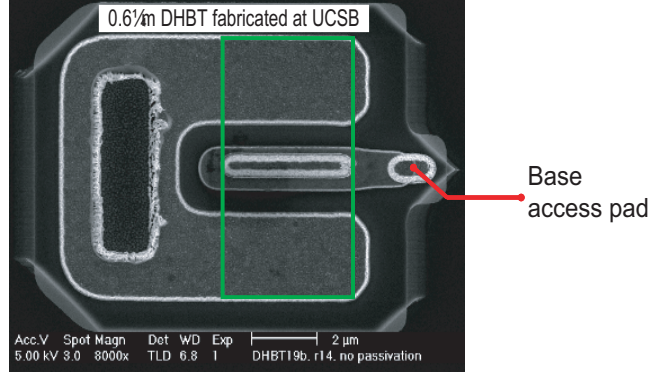
Figure 4.1: Planar view of a standard mesa HBT fabricated at UCSB

A major delay component determining digital logic speed is,

$$\hat{C}_{cb} \cdot \frac{W_{bm}}{W_{je}} \cdot \frac{\Delta V_{logic}}{J_e} + C_{cb,pad} \cdot \frac{\Delta V_{logic}}{J_e L_{je} W_{je}} \qquad (4.0.0)$$

where $\hat{C}_{cb}$ is the device capacitance per unit area (not including $C_{cb,pad}$, the access pad capacitance). For reasons explained, this base pad cannot be scaled. As seen from Eqn.3.3, as the length is decreased, $C_{cb,pad}$ becomes a significant fraction of the total C_{cb}.

As detailed in Chapter 2 , eliminating the pad capacitance reduces power consumption while maintaining the same bandwidth. Current state of the art mesa DHBTs have resulted in static frequency dividers operating at 150 GHz but consuming 600 mW [4]. In order to design a divider to operate at 150 GHz but at half the power, current mode logic (CML) can be employed for the data level and emitter coupled logic (ECL) for the clock level. With current mode logic, the transistors in the data level has a collector base swing of $-\Delta V_{logic}$ to $+\Delta V_{logic}$ as opposed to $-\Delta V_{logic} + V_{BE}$ to $+\Delta V_{logic} + V_{BE}$ for levels using emitter coupled logic. CML operation has greatly reduced maximum current density. From Eqn.3.3, C_{cb}/I_c increases and hence the delay. In order to maintain C_{cb}/I_c, a simple calculation and simulations indicate that C_{cb} has to be decreased by ~ 30 %.

There are several methods reported for eliminating this base access pad capacitance through the use of micro air-bridges [5, 6]. Fig. 4.2 shows a secondary electron micrograph of such as base pad. Typically in such processes, the subcollector under the feed lines from the base pad is removed by anisotropic wet etching. There are several disadvantages:
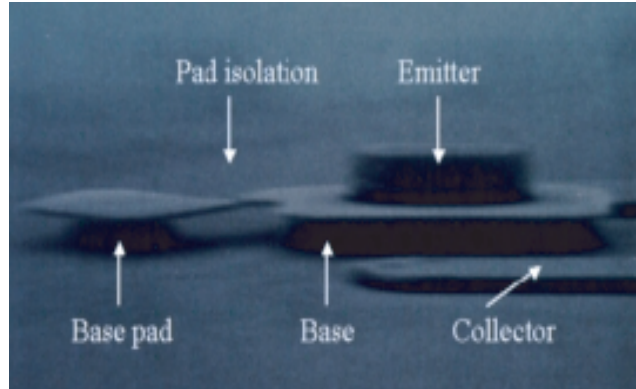
Figure 4.2: Air bridge to isolate the base access pad: Courtesy NTT, Japan

---

- The base feed lines are designed to be $\approx$ 0.6-0.8 μm to ensure complete removal of the semiconductor below. These present a very large access resistance.

- The use of thin feed lines and the presence of air gaps, presents a reliability issue.

This technique is thus unsuitable for high yield, manufacturable processes.

An alternate idea is to isolate the base pad by selective implantation. Ion implantation is a viable method to achieve isolation in the active regions and has been successfully employed in GaAs-AlGaAs HBTs [7]. As discussed in Chapter 3 , Fe implantation can be used to compensate the N-type collector and subcollector layers, where isolation is required Fig. 4.1. As detailed in the previous section a very high dose and energy of Iron is required to isolate N^{++} layers. Such Fe implants induces large defect density and is unsuitable where crystalline growth is required.

One of the main ideas explored in this thesis is the use of selective Si implants to eliminate the base pad capacitance.

4.1 Implanted subcollector HBT process

The process flow of the basic, implanted subcollector HBT is shown in Fig. 4.3. Starting with a template of Semi-Insulating InP, alignment targets for stepper based lithography are defined. Si_xN_y is deposited and patterns are defined by dry etch so that SI InP substrate is selectively implanted with Silicon(Si), an N-type dopant (Reasons for choosing Si are detailed in Chapter 3). Following the implant, the

Si_xN_y implant mask is removed in BHF. The Si dopant is activated and the implant damage is removed, by a high temperature anneal in the RTA. In order that the Phosphorus not dissociate during anneal, the top and bottom of the wafer is covered with 40 nm Si_xN_y. This ensures that a highly doped, isolated subcollector region is formed only where devices are to be formed. In Fig. 4.1, Si is implanted inside the drawn boundary. The base access pad lies outside the subcollector implant boundary. This means that the subcollector is not present under this pad and there is no terminating plate of charge for the electric field lines from the p^{++} base. The capacitance due to the base pad is therefore nearly eliminated. The HBT drift collector, base, and emitter layers are then grown by Molecular Beam Epitaxy (MBE). Devices are fabricated in a standard, all wet etch mesa process. However with the selectively implanted subcollector, HBT isolation does not require a mesa etch. As seen from Fig. 4.3, this reduces the HBT mesa height by ~ 500 nm significantly improving the planarity of the device and hence device yield in a complex IC process.
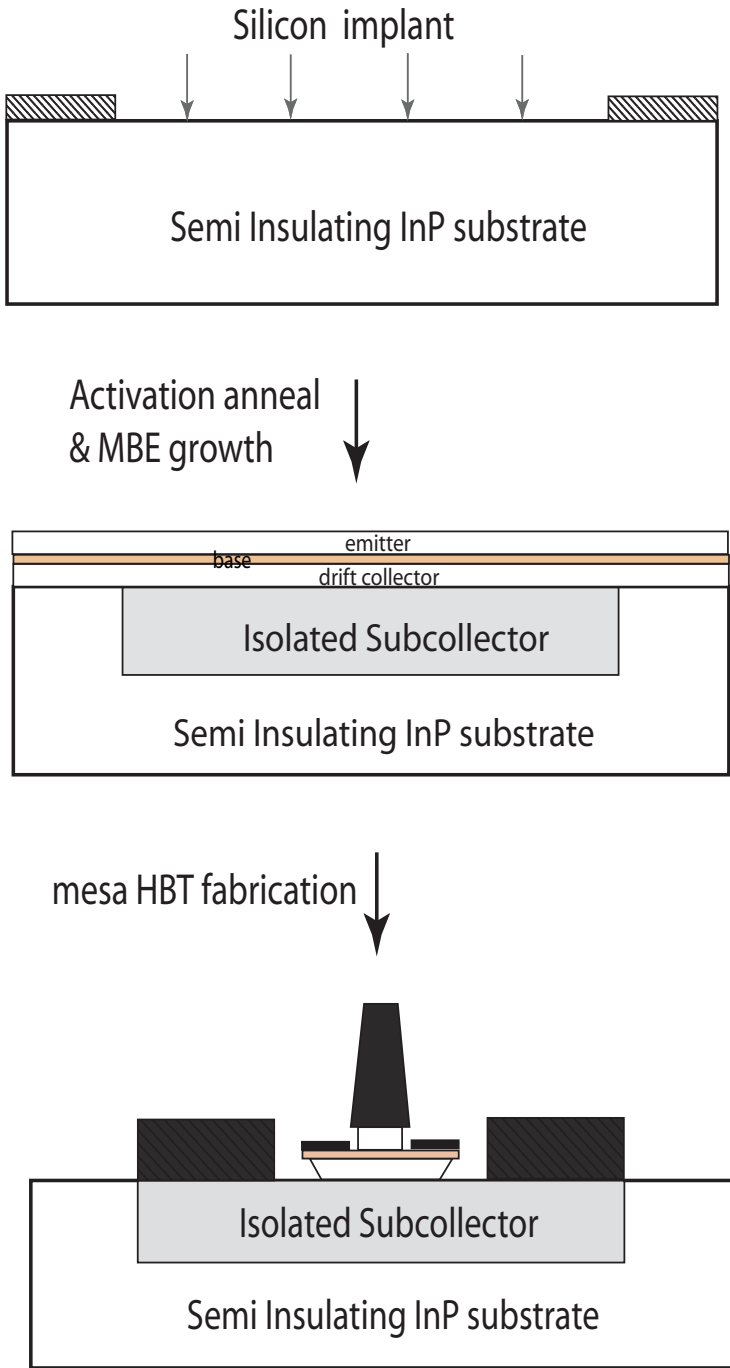
Figure 4.3: Basic implanted subcollector HBT process flow

Several criteria need to be satisfied for the implanted subcollector process.

- low sheet resistance subcollector

- high doping at the surface for low collector contact resistance

- crystalline, defect free semiconductor before growth

- excellent surface morphology comparable to InP substrate prior to growth

- planar surface with no recesses due to dry etches/implants/other processing

- high temperature stable alignment targets

- low contact resistivity ohmics to N^{++} InP

- good isolation between the N^{++} subcollectors

- defect free MBE growth $\Rightarrow$ low I_{CBO}, DC characteristics simlar to epitaxially grown HBTs

4.1.1   Si subcollector implant

From the expression for collector resistance in 2.3, the subcollector has to have high doping of $\sim$ 1-2$\times 10^{19}$, and a low sheet resistance comparable to a mesa DHBT $\sim$ 10 $\Omega/\square$. Furthermore the subcollector needs to be isolated with very low inter device leakage $\sim$ 1 pA/μm. The requirements for the implant are thus summarized below.

- Low $R_c \Rightarrow$ high doping $\Rightarrow$ high implant fluence

- Low $R_{sh} \Rightarrow$ thick subcollector $\Rightarrow$ high implant energy

- Good isolation $\Rightarrow$ excellent implant mask $\Rightarrow$ thick Si_xN_y

As discussed in Chapter 3 , the anneal should repair the crystal damage and also activate most of the dopants so that Si preferentially occupies the group III(In) site.

From the data in Table 3.2, the lowest sheet resistance when the Energy = 140 KeV (all other conditions are identical) is $\sim$ 45 $\Omega/\square$. This is high compared to 15 $\Omega/\square$ for epitaxially grown subcollector in a standard mesa DHBT. In an effort to decrease the sheet resistance, the maximum implant energy is increase to 200 KeV to increase the implant depth. Following *TRIM* simulations, the distribution of the implanted Si ions in InP is shown in Fig. 4.4 for the implant conditions given in Table 4.1.

This is a multiple energy-multiple fluence implant.
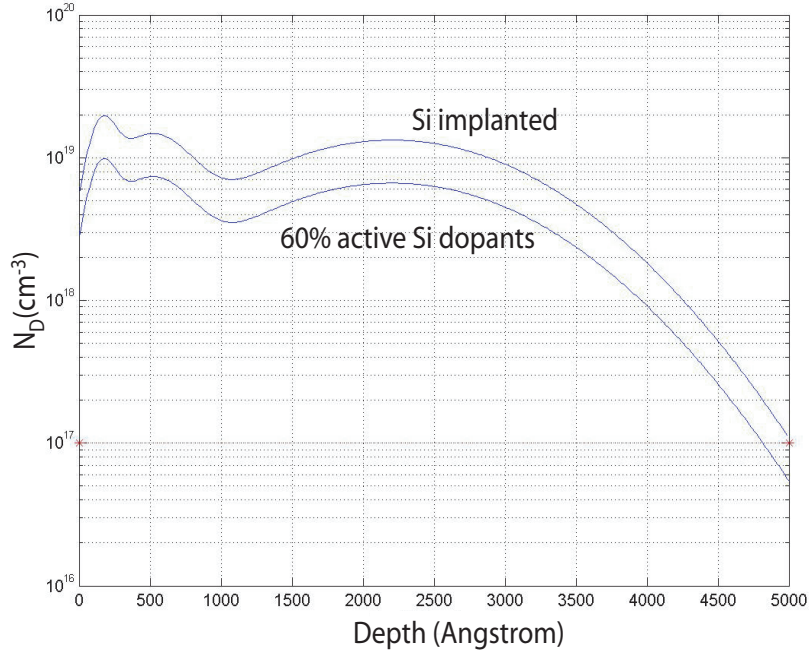
Figure 4.4: Concentration profile of Si in InP for implant conditions in Table 4.1

- The fluences and energies are chosen so as to obtain an overall concentration of $\geq 2 \times 10^{19}$ over ~ 250 nm. For epitaxially grown InP, the sheet resistance of such a layer would be $\sim 15 \ \Omega/\square$. The low energy component of the implant to ensure high doping at the surface for a good ohmic contact. This energy also ensures that the thickness of the $Si_x N_y$ implant mask is not excessive ($\approx 1 \ \mu$m). The implant fluences are kept within the known amorphization limits of Si implants in InP [8].

- All implants are done at an offset angle of $7°$ to prevent channeling through the substrate.

- During these implants the substrate temperature is maintained at 200 °C to minimize the crystal damage due to implant.

- During these implants the current is always kept below 10 μA, so that the substrate does not suffer from additional heating effects.

At this time, the highest known commercially available energy for Si implant at 200 °C is 350 KeV. In order to simplify the design of the implant mask and the process,

Table 4.1: Implant conditions for basic, implanted subcollector HBT process

Implant species	Implant energy	Implant fluence	Offset angle	Implant temperature
Si	200 KeV	3×10^{14} ions/cm^2	7 $^\circ$	200 $^\circ$ C
	40 KeV	8×10^{13} ions/cm^2		
	10 KeV	3×10^{13} ions/cm^2		
$I_{ions} \leq 10\mu$A				

the above conditions are chosen for first generation transistors in this process. This is shown to yield sufficiently low values of R_{sh}. Extensive discussion on implants in InP etc. has already been provided in Chapter 3

Sheet resistance

After this implant, a high temperature anneal is performed and the sheet concentration(n_{sh}), mobility(μ_n), activation(%) and sheet resistance of samples, for the above implant conditions, are determined from standard four point Hall measurements and shown in Table 4.7. 800 $^\circ$C for 30 seconds was chosen as the activation anneal for all Si im-

Table 4.2: Hall measurements of resistivity and mobility for Si implants

Anneal temperature ($^\circ$C)	Anneal time (s)	Hall mobility ($cm^2/V \cdot s$)	Carrier density (cm^{-2})	Sheet resistance ($\Omega/\square$)
800	30	722	3.3×10^{14}	26
850	15	900	3.1×10^{14}	22

plants. The activation is ≈ 60 %. The mobility is lower, and sheet resistance higher, when compared to epitaxially grown InP ($\sim 1000 \ cm^2/V \cdot s$). Calculations of collector resistance showed that it is still dominated by the contact resistivity. Hence these implant and anneal conditions were chosen as a starting point. The anneal at 850 $^\circ$ C for 15 seconds, yielded a lower sheet resistance but the quality of the Si_xN_y cap was compromised giving rise to several anneal defects as seen in Chapter 3 . The sheet resistance obtained from Hall measurements correlates with sheet resistances measured using the transmission line method (TLM).

An anneal at 800 $^\circ$C for 30s gives a resistance of $\approx 25 \ \Omega/\square$. It will be seen in Chapter 5 that the defects from the various dry etches and Si implant are sufficiently annealed out for these conditions. After implant and anneal, the active device layers are grown. There is no thick buffer as in a standard mesa DHBT process. From Atomic Force Microscopy(AFM) surface scans, the mean surface roughness for various anneal conditions. After annealing at 800 $^\circ$C for 30s, the mean roughness is 1.8

nm. Virgin SI InP has a mean roughness of $\sim$1.4 nm. AFM scans are also performed to evaluate the uniformity of the surface after implant. Si_xN_y is the implant masked and is dry etched to open up the regions where Si is to be implanted, as seen in Fig. 4.3. The implanted surface is subjected to ion bombardment during dry etching and implantation. It is critical that the surface is fairly planar before growth since MBE involves line of sight deposition and hence growth in trenches is not straight-forward. Fig. 4.5 shows a scan of such a selectively implanted section. The scan indicates rms planarity of $\sim$ 5nm.
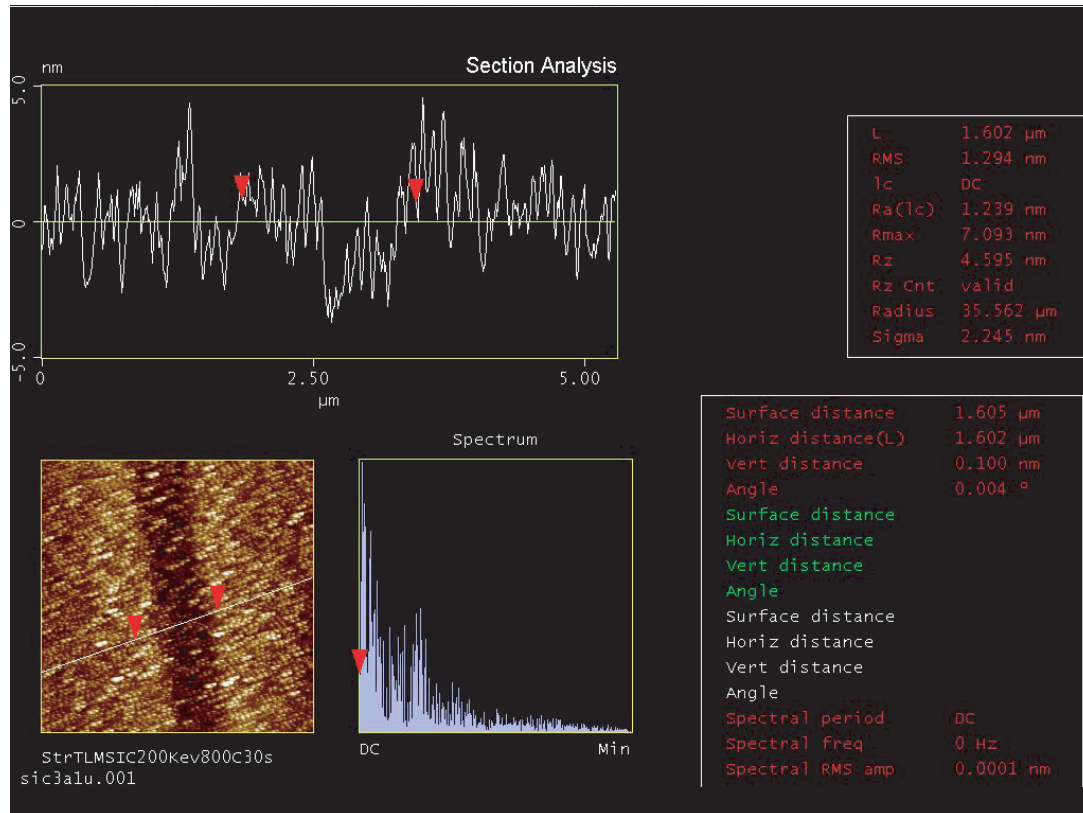
Figure 4.5: AFM scans of selectively implanted sections

Device Isolation

1μm thick Si_xN_y is the implant mask and from Fig. **??** in Chapter 3 , this is seen to be sufficient to stop Si at the chosen conditions. Higher energy $\Rightarrow$ thicker Si_xN_y
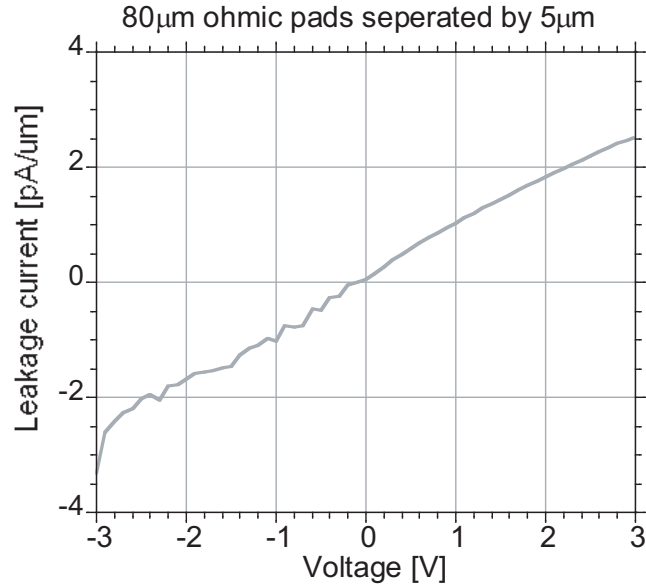
Figure 4.6: Device isolation between ohmic pads separated by 5 μm

implant mask $\Rightarrow$ unknown photoresist recipes to dry etch thick Si_xN_y in the reactive ion etcher (RIE) available at UCSB.

TLM patterns are formed to test the isolation of these subcollectors and hence the effectiveness of the Si_xN_y implant mask. Si is implanted under the N^{++} ohmic pads. Following activation by high temperature anneal, ohmic contacts are formed to InP. From Fig. 4.6, the leakage current in the regions masked during implant is $\sim$ pA/μm at 3V, where the ohmic pads were separated by 5μm.

4.1.2 Collector ohmic contacts

In a standard mesa DHBT process, collector ohmics are formed to N^{++} 6.5 nm $In_{0.53}Ga_{0.47}As$ to obtain low contact resistivities of $\sim 10\,\Omega\cdot\mu m^2$. As will be detailed in the next section, in the implanted subcollector DHBTs, the $In_{0.53}Ga_{0.47}As$ layer is undoped and merely used as an etch stop layer. Collector contacts are made to N^{++} InP formed by the Si implant. Collector resistance is of a mesa DHBT with a

two sided collector is given by Eqn.2.3 in Chapter 2 ,

$$R_c = R_{c,contact} + R_{c,gap} + R_{c,spread} \tag{4.1.0}$$

$$R_c = \frac{1}{2} \frac{\sqrt{\rho_c \cdot R_{sh}}}{L_e}$$

where ρ_c ($\Omega{\cdot}\mu$m^2) and $R_{sh,s}$ ($\Omega/\square$) are the specific contact resistivity and sheet resistance of the sub-collector. With $R_{sh,s} \sim 25 \ \Omega/\square$, base-collector spacing of 0.5 μm, base mesa width of 1.35 μm, contact resistivity $\geq 10 \ \Omega \cdot \mu$m^2, and assuming that the collector contact width is $\gg L_T$ the ohmic transfer length, the various components of R_c are given by

$$R_{c,contact} \geq 8\Omega \cdot \mu m, R_{c,gap} \approx 6\Omega \cdot \mu m, R_{c,spread} \approx 2.8\Omega \cdot \mu m \tag{4.1.0}$$

The contact resistance dominates even for contact resistivities as low as $10 \ \Omega \cdot \mu$m^2. Since collector contacts are made to wide bandgap InP, contact resistance assumes significance.

The effect of collector contact resistance on digital logic speed is given by,

$$f_{CLK}^{-1} \propto \cdots + C_{cb} \cdot \left(\frac{\Delta V_L}{I_c} + R_{c,contact} \right) \tag{4.1.0}$$

At the current scaling generation [4], for $\Delta V_{logic} = 300$ mV at an operating current of $I_c = 5$ mA/μm, the load resistance $R_L = \Delta V_L/I_c$ is $40 \ \Omega \cdot \mu$m. The collector contact resistance is in series with this load resistance. For the above values, $R_{c,contact}$ constitutes $\sim 16 \ \%$ of the delay term given by Eqn.4.1.2. Similarly, $C_{cb} \cdot R_{c,contact}$ delays reduce f_τ and f_{max}.

Collector ohmics are made to N^{++} InP. Since the barrier height are larger for wideband gap semiconductors, alloyed ohmics(AuGe) are typically employed to contact wide bandgap semiconductors. $Au_{0.88}Ge_{0.12}$ forms a eutectic at 365 °C. In GaAs, the Au reacts with GaAs leaving behind a large concentration of Ga vacancies and Ge diffuses, occupies the Ga sites and heavily dopes the underlying semiconductor N-type[9]. A thin interfacial Ni(1-5 nm) is used as the wetting layer and also serves to enhance the diffusion of the GeAu alloy[10]. However, the exact mechanism of ohmic formation with alloyed contacts is not well understood in N-InP.

Non alloyed ohmics such as TiPtAu to N-type InP typically yield high contact resistivities $\sim 800 \ \Omega \cdot \mu$m^2 [11]. Sputter cleaning, with an inert gas, the surface before contact metal deposition reduces the contact resistivity of such non alloyed ohmics to $\sim 40 \ \Omega \cdot \mu$m^2 [12]. This is attributed to the formation of In rich surface that is degenerately N^{++} doped. In contrast, alloyed GeAu ohmics yield low contact

Table 4.3: Contact resistivity of various metalization schemes to Si implanted InP

S.No	Metalization	Anneal (°C)	R_{sh} ($\Omega/\square$)	ρ_c ($\Omega \cdot \mu m^2$)
1	Ni(20nm)/Ge(50nm)/Au(50nm)/Ni(20nm)/Au	300	23	90-100
2	Ni(5nm)/Ge$_{0.12}$Au($\sim$80nm)/Ni(20nm)/Au	not annealed	16	200-230
		320	16	45-50
		360	16	25-30
		400	16	12-18
3	Pd(3nm)/Ti(17nm)/Pd($\sim$17nm)/Au	300	10	75-100
4	Ge(1nm)/Ni(5nm)/Ge(50nm)/Au(50nm)/Ni(20nm)/Au			
5				
6				
7				
1. Si implanted and annealed with the conditions given in subsection **??**				
2,4. Si implanted at a higher energy $\sim$ 325 KeV and annealed so that $R_{sh} \sim 15$ $\Omega/\square$				
3. Epitaxially grown N^{++} InP subcollector, with $R_{sh} \sim 10$ $\Omega/\square$				

resistivities to Si implanted InP of $\sim$ 7 - 10 $\Omega \cdot \mu m^2$. The low energy component(10 keV) of the Si implant employed here (see previous section) ensures a high surface doping for low contact resistance. Since collector contact formation to InP is not trivial, several experiments are carried out and the results are summarized in Table 4.3.

It is seen from the above data that the lowest contact resistivity is obtained with the AuGe eutectic annealed at 400 °C. However, it is seen that such anneals of the collector ohmics results in an increase in the base and emitter resistivities and is shown in Table 4.4. Further for alloyed ohmics, high anneals result in pits and poor surface morphology of the metal contacts.

Annealing at or above 360 °C causes the base contact resistivity to substantially increase. The base is doping graded from 8×10^{19} to 5×10^{19} from the emitter side to the collector. As the anneal temperature increases, the thin interfacial Pd diffuses, and forms contact with lesser doped material. The Pd and Ti can diffuse through the thin base at sufficiently high anneals. Shown in Fig. 4.7are plots of the base collector leakage current showing the effect of the various anneals. At 400 °C, the base metal nearly shorts the collector. GeAu contacts require anneals above the eutectic temperature to obtain low contact resistivity. As seen from the above table,

Table 4.4: Contact resistivity of base, emitter and collector ohmics at various anneals

Anneal °C	Emitter ρ_c ($\Omega \cdot \mu$m^2)	Base ρ_c ($\Omega \cdot \mu$m^2)	Collector ρ_c ($\Omega \cdot \mu$m^2)
	Ti(20nm)/Pd(40nm)/Au	Pd(3nm)/Ti(17nm)/Pd(17nm)/Au	Ni(5nm)/Ge$_{0.12}$Au($\sim$80nm)/Ni(20nm)/Au
unannealed	5	12	200-230
320	5	18	45-50
360	5	55	25-30
400	50	270	12-18

Ni/Ge/Au where ge and Au are deposited as separately yields the lowest resistivity at 300 °C. For the initial process runs, these were chosen as collector contacts. This is similar to regular non-alloyed contacts. In order to use the GeAu eutectic, the base and collector ohmic processes need to be revised. Either the base ohmic must be redesigned to withstand high temperature anneals or new collector ohmics must be developed to N^{++} InP that yield very low contact resistivities without the need for an anneal.

4.1.3 Alignment targets

All features are defined by lithography using the i-line (365nm) GCA wafer stepper in UCSB nanofabrication facility. As HBT feature sizes are scaled, alignment becomes critical. With the Dark field alignment system(DFAS) on the GCA stepper, alignment error better than 0.15 um is achieved. This system delivers the best alignment, when there is sufficient contrast between the targets and the field. This requires the targets to be at a significantly different height from the field. The first step of the implanted subcollector HBT process, consists of creating alignment targets subsequently used to align the wafer so as to correctly define features for the subcollector implant. The alignment targets must withstand the dry etch, high temperature (800 °C) processing steps and MBE regrowth and must have sufficient contrast. Etching into the substrate is the most straightforward method of forming alignment targets. However, the fear that subsequent growth might reduce its step height and affect its contrast precluded its usage. The ≥ 0.7 μm emitter metal also defines targets in a standard mesa process and provides excellent contrast for precise local alignment. However, most metal targets, such as Ti or Au are not compatible where a high temperature anneal is required [13]. The refractory metals, Tungsten, Molybdenum and Tantalum seem to be excellent choices. Molybdenum is etched in BHF which is used to remove the Si_xN_y implant mask while Tantalum deposition is not straightforward
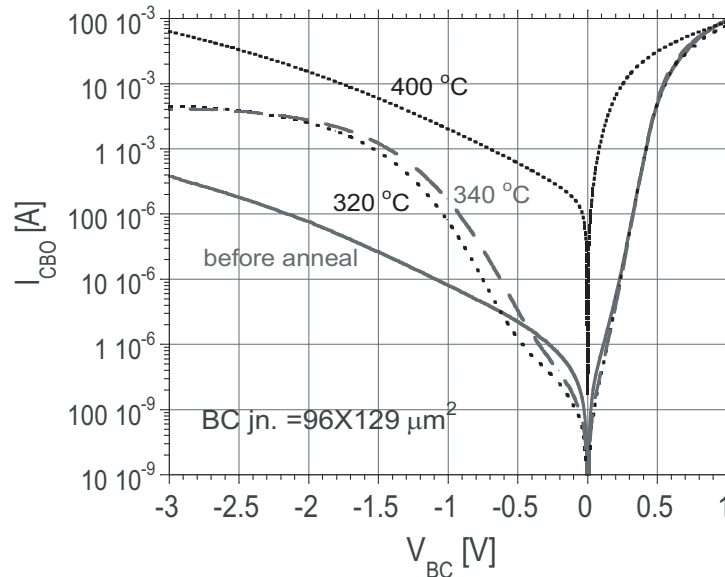
Figure 4.7: Base collector leakage upon annealing

and it is highly toxic. Hence the only viable option was Tungsten (W).

Pure W is a hard refractory metal with the highest melting point (3422 °C) of all metals. It has very low chemical activity at room temperatures and is attacked slightly by most mineral acids. Owing to its high melting point and it refractory nature, W is used extensively in high-temperature applications. In the implanted subcollector process, W was not attacked by any of the acids or bases used. The first process runs were carried out using W where 0.3 μm Tungsten is sputtered and dry etched to form the alignment targets. These targets however did not withstand the high temperature anneal step to activate Si, and formed defective outgrowths as shown in Fig. 4.8. Due to these outgrowths of metal, the DFAS local alignment system did not recognize the targets. This presented a huge problem since fine alignment of $\leq$ 0.15 μm was required which was obtainable reliably only by using the DFAS. One option was to reduce the anneal temperature for Si activation but this meant a compromise to device performance. Studies and analysis of these W targets are carried out using energy dispersive x-ray analysis (EDX). Detecting the characteristic fluorescence x-rays emitted from the sample as a result of excitation by the imaging electron beam, elemental analysis using EDX is performed. Fig. 4.9 shows the EDX spectra of the overhang metal features on the targets after anneal. A huge Oxygen concentration is detected. It is found that residual stress and structural prop-
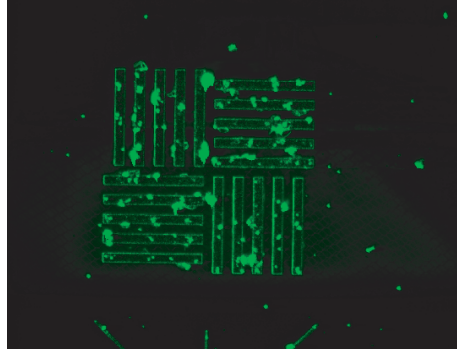
Figure 4.8: Tungsten alignment targets after high temperature anneal

erties of tungsten films, is a function of the sputtering gas pressure. There is also found to be a strong correlation between the stress and the microstructure of these films. The amorphous phase has been found to contain over 20% Oxygen and is reported to be metastable [**?**]. The thermal properties could thus be severely impacted by the presence of large oxygen impurities in the sputtered Tungsten.
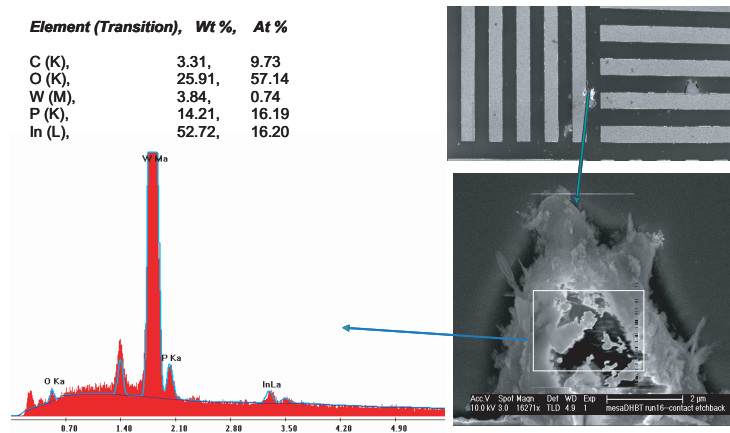
Figure 4.9: EDX spectra of the defects on the Tungsten targets after anneal

Ti(10%)W was reported to be stable after annealing at 800 °C [15]. TiW alloy has similar chemical properties to W. It could be easily dry etched and is not attacked by any of the chemicals used in this process. Furthermore, these targets had better contrast on the stepper's local alignment system than W, which is a dull grey metal.

TiW was sputtered at low pressures to a height of ~ 0.3 μm. These targets withstood an annealing temperature of 800°C. Tthey are stable(Fig. 4.10) after MBE growth, and are resolved by the stepper's alignment system.
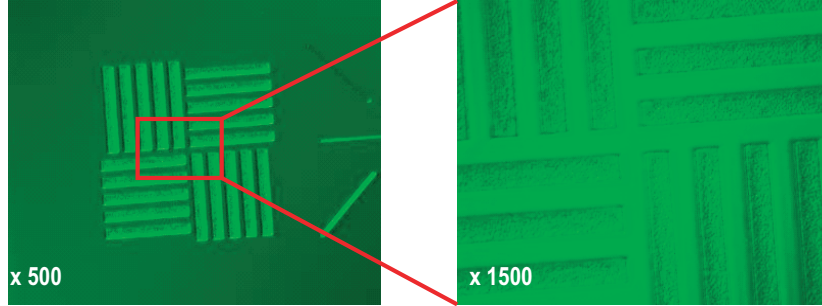
Figure 4.10: TiW alignment targets after high temperature anneal and MBE growth

4.1.4 Design of RF mask

The region where the base pad lies has to be masked during Si implant. Si has to be implanted under the collector contacts and in the active device region (Fig. **??**). The Si implant also has to be present under the emitter junction. In actuality, it has to extend beyond the length of the emitter junction due to current spreading. The length of the subcollector mask is determined as follows.

$$L_{sc} = L_E + T_c - \Delta x_E - \Delta x_{straggle} + 2\Delta x_{align} \qquad (4.1.0)$$

where L_E is the length of the emitter as on the photomask in Fig. 4.11, Δx_E is the longitudinal undercut of the emitter, $\Delta x_{straggle}$ is the straggle due to implant, Δx_{align} is the alignment tolerance. Since the subcollector and emitter are individually referenced to separate zero level targets, the alignment error doubles. The implant straggle from TRIM plots is seen to be ~ 0.2 μm. With $\Delta x_E = 0.4$ μm, $\Delta x_{align} = 0.2$ μm.

$$L_{sc} = L_E + T_c - 0.2 \qquad (4.1.0)$$

 To accommodate collector thicknesses below 200 nm, the length of the subcollector photomask is designed such that, $L_{sc} = L_E$. In order to compare the effectiveness of the subcollector implant process, the base pad is not isolated in some devices, so that the region under the base pad is not masked during implant.
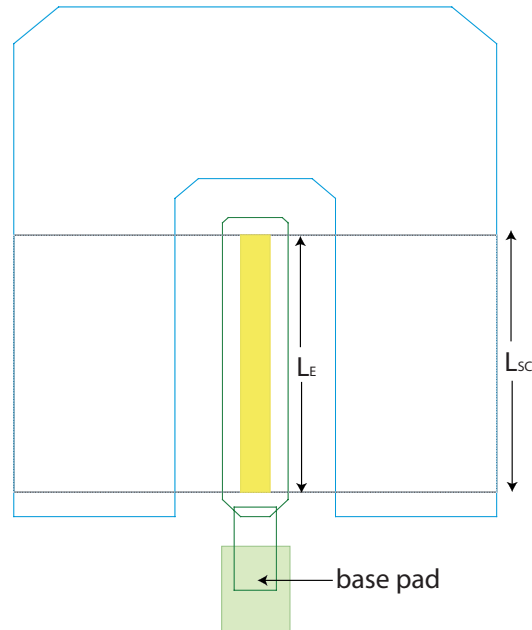
Figure 4.11: Layout of implant mask, seen with the emitter, base and base access pad

4.2 HBT design for implanted subcollector

The design of each layer in an HBT is detailed in Chapter 2 . With the lithographic capabilities available at the time 0.6 μm features can be reliably processed at UCSB, even for complex ICs. The implanted subcollector DHBTs have significant performance advantages when devices are scaled. However, the first generation transistors are intended to compare the advantages of this process against the mesa technology. In order to make intelligent assessments, performance comparisons has to be made against existing transistor results. Fast HBTS have been reported at UCSB, with collector thickness $T_C = 200$nm [16], 150 nm [17], 120 nm [3], 100 nm [18].

Static frequency dividers with $\Delta V_{logic} = 300$ mV, demonstrated a maximum clock speed of 140 GHz[4]. These have a C_{cb}/I_c of ≈ 0.5 ps/V. As stated earlier, C_{cb} reduction techniques results in superior bandwidth of digital logic circuits and the best performance metric for implanted subcollector DHBTs is maximum digital

logic speed. The minimum voltage swing is given by,

$$\Delta V_{logic} \geq 2 J_e \cdot \rho_e + 6 \frac{kT}{q} \tag{4.2.0}$$

A typical value of emitter contact resistivity repeatedly obtained is $\rho_c \sim 10\ \Omega \cdot \mu\text{m}^2$. If $J_e \sim 8\ mA/\mu\text{m}^2$, $J_e \cdot \% \sim 80$ mV. The device operating temperature is $\sim$ 400K, therefore 6kT/q $\sim$ 200 meV. The noise margin is only $\sim$ 20 mV. There for these values of contact resistivity, the maximum operating current density has to be maintained below 8 $mA/\mu\text{m}^2$. Furthermore the maximum operating power density of the ECL dividers is ~ 1.1V $\times$ 8 $mA/\mu\text{m}^2 \approx 9$ mW/μm^2 and such power densities should be supported in the layer designs.

As stated earlier, in order to compare against existing technology, the emitter and base layers for the first generation implanted subcollector DHBTs are identical to the mesa DHBTs reported [3]. The emitter base junction is abrupt, also due to ease of processing. (Selectively wet etching a In$_{0.52}$Al$_{0.48}$As- In$_{0.53}$Ga$_{0.47}$As grade is not straightforward). The base is designed to be 30 nm. For the contact metallurgy used and doping levels obtainable, this offers the best compromise between τ_b and R_{bb}. The collector design was an open choice. However, the maximum operating current density has to be kept below 8 $mA/\mu\text{m}^2$. 120nm collectors have a maximum operating current threshold of $\sim$ 8 $mA/\mu\text{m}^2$. From the scaling laws, in order to maintain the highest current density and lowest C_{cb}, 120 nm is the preferred choice. The minimum resolvable lithographic limit with good device yield for ICs at the UCSB nanofab facility, at this time is $\sim 0.6\ \mu$m. Minimum repeatable contact resistivities obtainable are, $\% \sim 10\ \Omega \cdot \mu\text{m}^2$. The lowest base resistivity for state of the art C doped, MBE grown In$_{0.53}$Ga$_{0.47}$As layer is 18 $\Omega \cdot \mu$m. For 30 nm bases, this yields an ohmic contact length of $\sim 0.13\ \mu$m. With an alignment tolerance of 0.15 μm, the base ohmic has to be at least 0.3 μm wide on either side of the emitter for low base resistance. For dividers, the emitter widths are designed to be $\geq$ than the present lithographic of 0.6 μm.

With new lithographic capabilities acquired recently at UCSB, and in conjunction with better specific contact resistivities that have been recently obtained, the implanted subcollector DHBTs will greatly benefit future laterally and vertically scaled transistors.

4.2.1 Design of InGaAs etch stop

In standard mesa DHBTs, the N^{++} subcollector is a composite structure and consists of highly doped N^{++} 6.5 nm InGaAs over 300 nm InP. The N^{++} InGaAs serves as the contact layer and also as an etch stop to selectively stop on the subcollector during the second mesa etch.

In the implanted subcollector DHBTs, the N^{++} InP is selectively implanted. N^{++} InGaAs cannot be present on these implanted subcollectors. This layer which if present and N^{++} doped, will form a terminating electrode under the base pad. This negates the entire idea of having selectively implanted N^{++} regions to eliminate the base pad capacitance. However an InGaAs layer is required as an etch stop. Therefore this InGaAs layer has to be necessarily undoped.

The InGaAs layer is to be sandwiched between InP layers and has a conduction band discontinuity of 0.25 eV with InP. A thin layer of InGaAs therefore forms a quantum well of electrons with a depth of 0.25 eV. It is critical that there be no electron/hole pile up in this quantum well. This means that the ground level for electrons in the quantum well must be much higher than the electron Fermi level. For a quantum well with infinite barriers, the ground state energy is given by

$$E_0 = \frac{\hbar^2 \pi^2}{2m_e^* L^2} \qquad (4.2.0)$$

where L is the thickness of the quantum well. By reducing the thickness of this well, the ground state energy can be increased. But, for a finite well, it can be shown that there always exists atleast one energy level. It can be shown that the number of levels [19] is given by,

$$N = 1 + Int \frac{2k_o a}{\pi} \qquad (4.2.0)$$

The ground state energy level for a quantum well of finite depth is given by,

$$E_0 = \frac{\hbar^2 k^2}{2m_e^*} \qquad (4.2.0)$$

where the wavevector k is defined by

$$\frac{kL}{coskL} = k_0 L \qquad (4.2.0)$$

and k_0 is given by

$$k_0 = \sqrt{\frac{2MV_0}{\hbar^2}} \qquad (4.2.0)$$

V_0 is the height of the well, here $V_0 = \Delta E_c = 0.25eV$. For example, in the extreme case of L = 0, $E_0 = V_0$. For L = ∞, $E_0 = 0$. Thus $0 \leq E_0 \leq V_0$; there is atleast one energy level in a quantum well with finite barriers. Simulations were carried out in 1-D Poisson to calculate the electron concentration in the InGaAs quantum well for quantum wells of width = 4nm and 5nm, and shown in Fig. 4.12. The InGaAs layer has to be thick enought to be an effective etchstop during the wet etching of the

InP collector. The ground state energy level is 0.13eV above the Fermi level for an InGaAs layer of thickness 4 nm while the electron concentration is $\sim 6 \times 10^{15}$ which is much lower than the collector doping of $\sim 3 \times 10^{16}$. The undoped InGaAs etch stop layer is designed to be 3.5 nm.
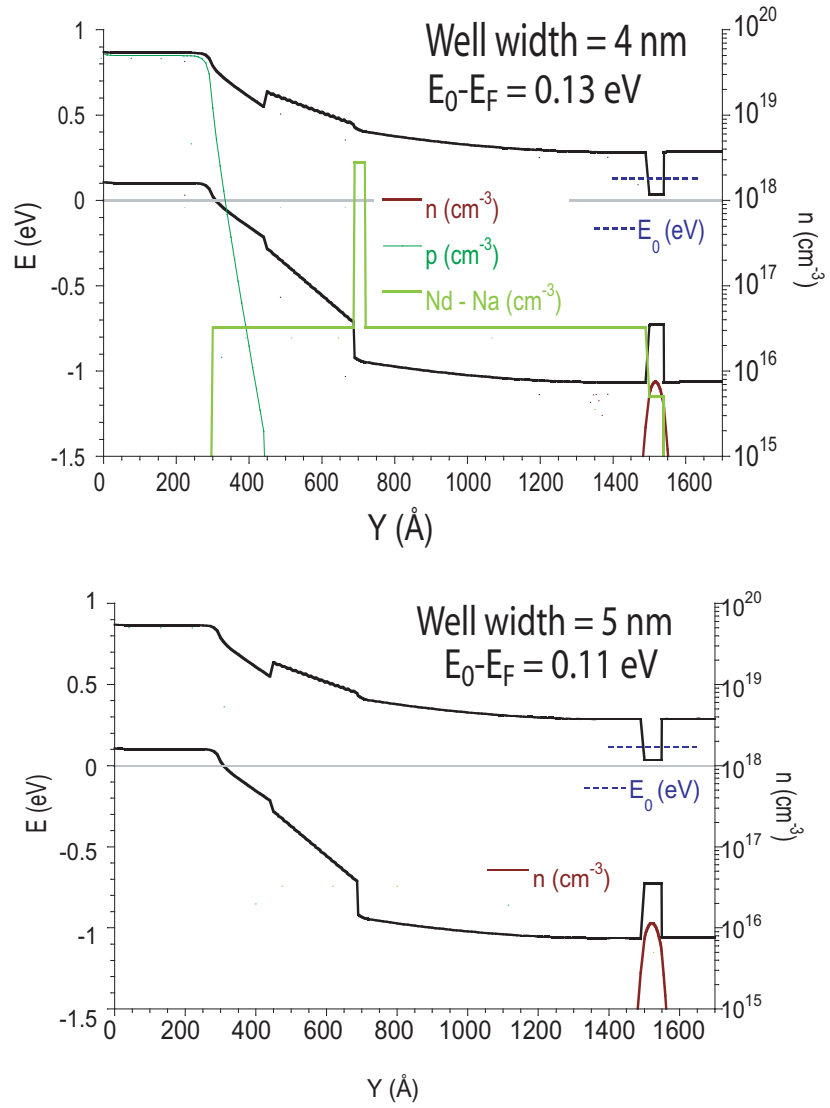
Figure 4.12: Electron concentration and Ground state energy level of quantum wells (4nm and 5nm) of UID InGaAs sandwiched between the collector and SI InP

4.3 Large area HBTs with implanted subcollector

In order to evaulate the layer structure, and growth on implanted substrates, SI InP is blanket implanted with Si at the conditions given Table 4.1. The wafer is annealed at 800 °C for 30 sec and subsequently growth was done by MBE at UCSB. The HBT layer structure consisted of a 150 nm collector and 30 nm base. Large area devices are fabricated where the emitter, base and collector are defined by 2 wet etches, followed by a single, common metalization (PdTiPdAu). From TLMs,
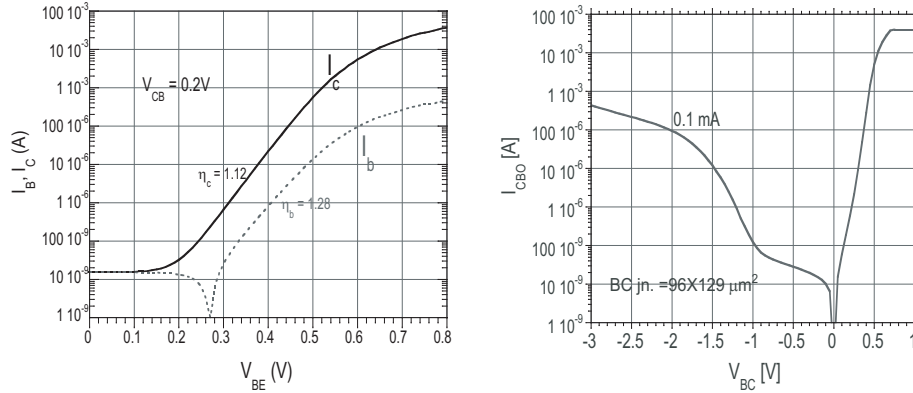
Figure 4.13: DC characteristics and base-collector leakage

the specific contact resistivities are 5-10 $\Omega \cdot \mu\text{m}^2$ while the base sheet resistance is very high ~ 3600 $\Omega/\square$. This is believed to be due to the surface depletion of $\sim$ 10 nm and chiefly due to miscalibration of the base Carbon doping and is corrected in subsequent growths. Fig. 4.13 shows the gummel characterisitics of these large area HBTs. These devices show a gain of ≈ 70. This high gain is further indicative of lower Auger recombination and hence low base doping. The plot on the right in Fig. 4.13 indicates that the leakage current at 2V is $\sim 8\times10^{-6}$ $mA/\mu\text{m}^2$. Extrapolating this for small area devices with a base collector area of $1.3\times5.25\mu\text{m}^2$, I_{CBO} is $\sim 5.6\times10^{-5}$ mA and I_{CEO} is $\sim 3\times10^{-3}$ mA which is a very low compared to operating currents of ≥ 10 mA and is hence indicative of a low base collector leakage and hence good growth on these implanted susbtrates. The very high base resistance is evident from the deviation from exponential charcterisitics even at moderate base emitter forward bias voltage of 0.8V.

Fig. 4.14 shows the Capacitance Voltage(CV) characteristics and the doping profile of the collector is extracted from the CV data. The data measured from the large area devices clearly illustrate that growth on implanted substrates is comparable to
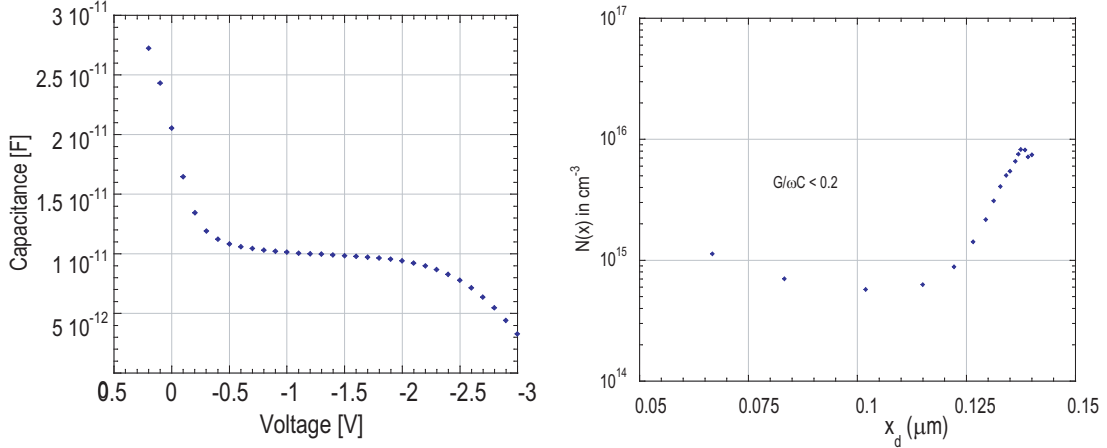
Figure 4.14: CV characteristics and doping profile

fully epitaxial structures.

4.4 RF process and device results

Large area devices have shown low leakage and good DC gain. Small area devices were processed with the layer structure shown in Table 4.5.

4.4.1 RF process

TiW alignment targets are defined, and following the process described in §4.1 and surface treaments elucidated in Chapter **??** , growths were carried out at $UCSB$'s MBE facility. A brief description of the process after growth is given below. The details are given in Appendix **??**. The emitters are accurately aligned to the TiW alignment targets. Alignment targets are also defined with the emitter metal and all further alignments are referenced to these. The emitter layer is then wet etched down to the base. $\sim 0.2\mu$m Base contacts and a base post of ~ 1 μm are deposited. Following this, the base mesa etch is performed down to the implanted InP subcollector. Collector contacts are defined using Ge/Ni/Ge/Au/Ni/Au. These were annealed only at a temperature of 300 °C to not impact the base contact resistivity. After the collector post is deposited, the wafer is planarized with Benzo Cyclo Butene(BCB) which is etched down to barely expose the metal posts. 100 nm of Si_xN_y is deposited to improve Metal-1(M1) adhesion and to form capacitors. The first level of intercon-

nect M1 then contacts the devices after forming vias in Si_xN_y. Devices are tested after this metalization step.

4.4.2 Device Results - Si Implanted subcollector DHBTs

The complete layer structure in the active device region are given in Table 4.5. The corresponding band diagram is depicted in Fig. 4.15. The projected $J_{Kirk} = 7$ mA/μm ^{2} at $V_{cb} = 0.0$ V and $J_{Kirk} = 11$ mA/μm ^{2} at $V_{cb} = 0.6$ V. The expected capacitance per unit area from Fig. **??** is ≈ 1 fF/μm^2.

Table 4.5: Layer structure: Si Implanted subcollector, 120 nm collector, 30 nm base

Thickness (nm)	Semiconductor Composition	Doping (cm^{-3})	Description
5	In$_{0.85}$Ga$_{0.15}$As	$> 4 \cdot 10^{19}$:Si	Emitter cap
15	In$_x$Ga$_{1-x}$As	$4 \cdot 10^{19}$:Si	Emitter cap
20	In$_{0.53}$Ga$_{0.47}$As	$4 \cdot 10^{19}$:Si	Emitter cap
80	InP	$3 \cdot 10^{19}$:Si	Emitter
10	InP	$8 \cdot 10^{17}$:Si	Emitter
40	InP	$5 \cdot 10^{17}$:Si	Emitter
30	InGaAs	$4 - 7 \cdot 10^{19}$:C	Base
15	In$_{0.53}$Ga$_{0.47}$As	$3.25 \cdot 10^{16}$:Si	Setback
24	InGaAs / InAlAs	$3.25 \cdot 10^{16}$:Si	B-C grade
3	InP	$3 \cdot 10^{18}$:Si	Delta doping
78	InP	$3.25 \cdot 10^{16}$:Si	Collector
3.5	In$_{0.53}$Ga$_{0.47}$As	undoped	Etch Stop
Substrate	Si implanted InP		Subcollector

The TLM measurements of the collector and, of the pinched and non-pinched base TLMs are given in Fig. **??**. Isolation between ohmic pads seperated by 10 μm is ~ 20 pA/μm.

Fig. 4.17 is a plot of the DC $I_C - V_{CE}$ characteristics. There is no evidence of gain compression till ≈ 9 mA/μm^2 at $V_{cb} = 0$V. The Gummel curves are plotted for $V_{cb} = 0$V and $V_{cb} = 0.3$V Fig. 4.18. The collector and base ideality factors are $\eta_c = 1.15$ and $\eta_b = 1.65$. These are in line with those obtained for fully epitaxial DHBTs. The leakage current I_{CEO} from the gummel curves is ≈ 90 pA at $V_{cb} = 0.3$V. The DC current gain of the transistor $= I_c/I_b$ from the gummel curves is shown in Fig. 4.19. The HBT's gain compression point is ≈ 6 mA/μm^2 at $V_{cb} = 0$V and 7 mA/μm^2 at $V_{cb} = 0.3$V.

Shown in Fig. 4.20 are I_{CEO} and I_{CBO}. I_{CEO} is collector-emitter leakage with the base open and defines the Common Emitter Breakdown Voltage, BV_{CEO}. I_{CBO}
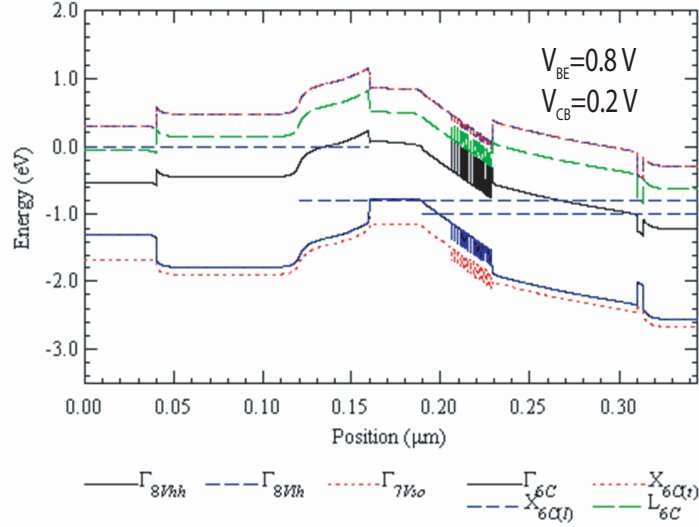
Figure 4.15: Band diagram of Implanted subcollector DHBT at $V_{be} = 0.8$V and V_{cb} $= 0.2$V

is the collector-base diode leakage with the emitter open and defines the Common Base Breakdown Voltage BV_{CBO}. It can be shown that $I_{CEO} = \beta\ I_{CBO}$ and hence BV_{CEO} is usually smaller than the common base breakdown BV_{CBO}.

Typically breakdown voltages are defined at a certain current, say $I_{CBO} = 50\ \mu$A. By this definition, BV_{CEO} (at $I_c = 50\ \mu$A) = 4.3V and $BV_{CBO} = 5.2$V. As detailed in Chapter 2 , with V_{be} spacings of 1mV and $V_{cb} = 0$V and 0.1V, the resistance as seen in the emitter $R_{ex} + R_{bb}/\beta$ is derived from gummels and plotted as function of current density Fig. 4.21. The decrease at low current densities(≈ 1 - $3\ mA/\mu$m^2) is an artifact due to the exponential curve fitting to I_c. However at medium current densities, $R_{ex} + R_{bb}/\beta$ is seen to decrease. This is due to two effects- the increase in current gain and more importantly decrease of base resistance at medium-high current densities. At these current densities, the base current is partly carried by electrons [20]. The thermal resistance can also be derived. Plotted in the right hand side of Fig. 4.21 is the thermal resistance,$\Theta_{th} \cdot \phi$ (also referred to as R_{th} are derived. The thermo electric feedback coefficient ϕ, for InP/InGaAs DHBT, at 1 mA/μm^2 is ≈ 0.001 mV/°C [21]. From this the thermal resistance at 1 mA/μm^2 is 2.1 deg K/mW. The collector resistance is extracted from the $I_C - V_{CE}$ characteristics of the transistor at saturation, using the Fixed β method described in Chapter 2 and is plotted in Fig. 4.22. This method returns the collector plus emitter series
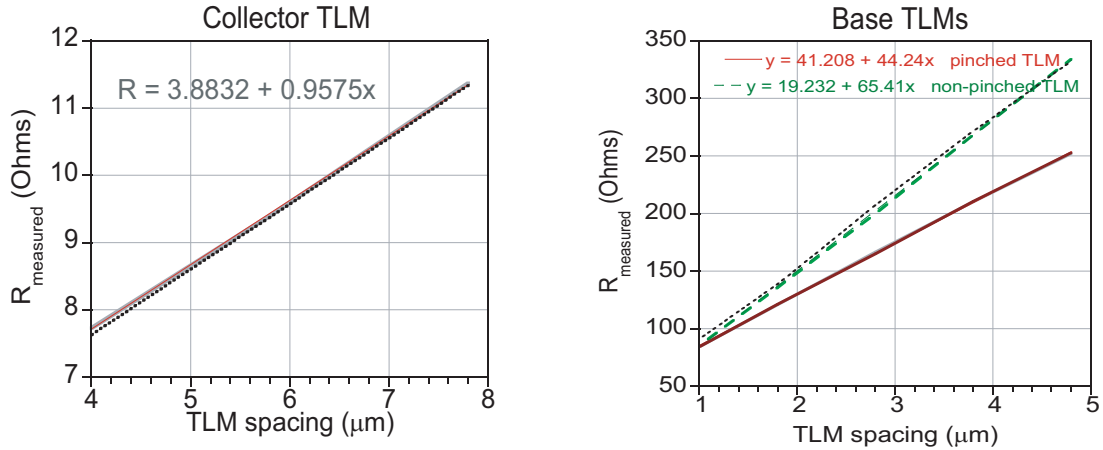
Layers	$R_{sh}\,(\Omega/sq)$	$\rho_c\,(\Omega{-}\mu m^2)$	$\rho_{horz}\,(\Omega{-}\mu m)$	$L_T\,(\mu m)$
Base	1100	50	115	0.21
Collector	24	100	100	2.04

Figure 4.16: Base and Collector TLM measurements

resistance. Since the emitter resistance is already known, $R_{ex} \approx 3\ \Omega$ the collector resitance is determined to be $\approx 12\ \Omega$. The device DC current gain, ideality factors, and collector leakage current are consistent with those measured from the triple-mesa HBT equivalent [3].
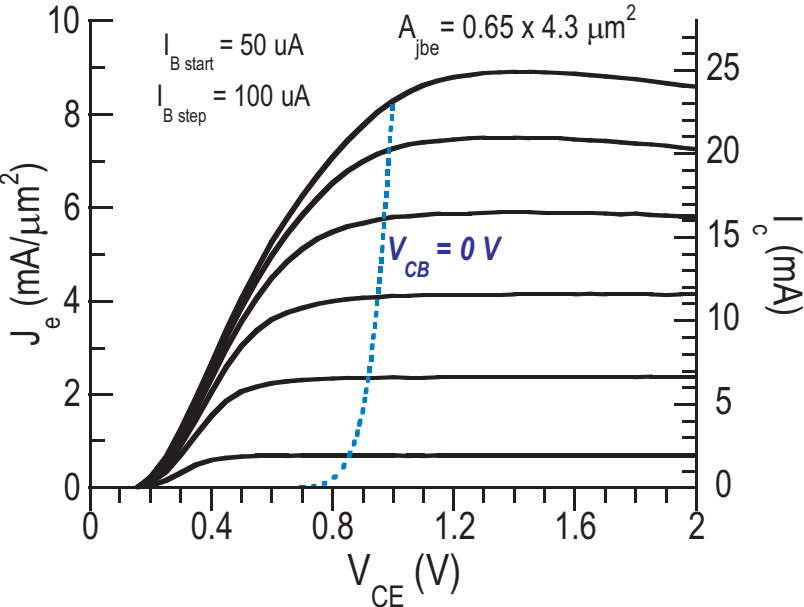
Figure 4.17: DC $I_C - V_{CE}$ characteristics
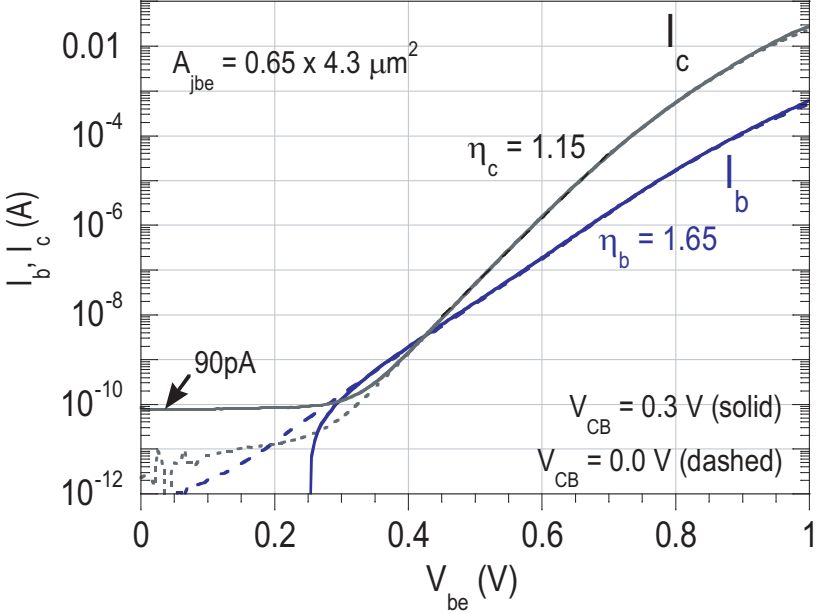
Figure 4.18: Gummel curves at $V_{cb} = 0V$ and 0.3V
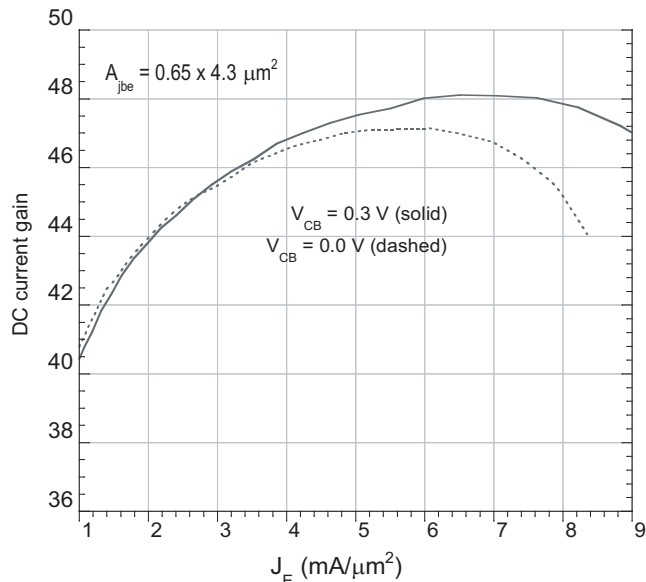
Figure 4.19: DC gain of the HBT at $V_{cb} = 0V$ and 0.3V
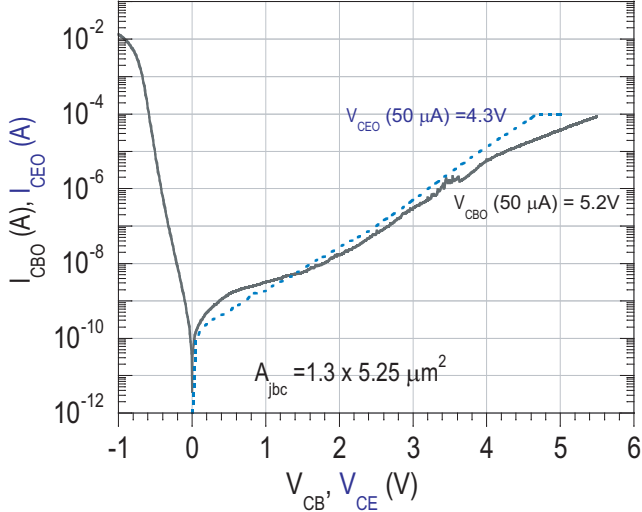
Figure 4.20: Leakage currents in the device
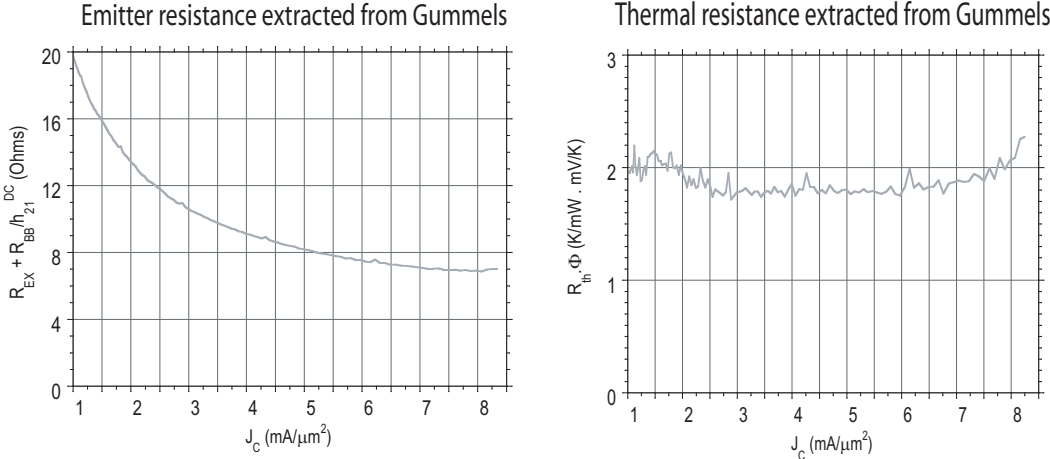
Figure 4.21: Extraction of Emitter resistance, and thermal resistance
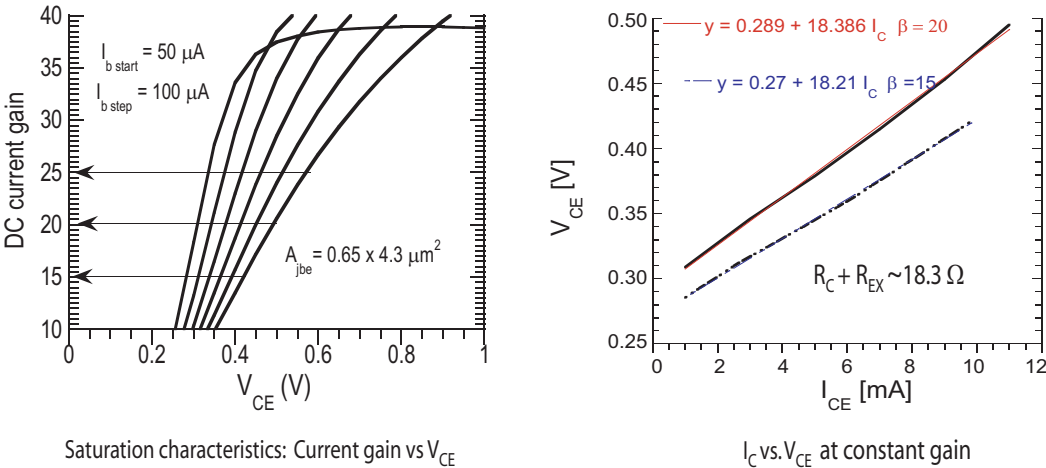
Figure 4.22: Extraction of Collector resistance

DC-45 GHz S-parameter measurements are carried out after performing an off wafer Line-Reflect-Reflect-Match calibration on an Agilent 8510C network analyzer. On-wafer open and short circuit pad structures identical to the ones used by the devices are measured after calibration in order to de-embed their associated parasitics from the device measurements. Shielded *Infinity* probes are used for microwave measurements. Their superior field confinement reduces unwanted couplings to nearby devices and transmission modes. The unilateral power gain, U and short circuit common emitter current gain, h_{21} are plotted in Fig. 4.23. Extrapolating these at 20 dB/decade, f_τ and f_{max} are obtained as the frequencies at which U and h_{21} are 0 dB respectively. The f_{max} and f_τ are lower than the standard, fully
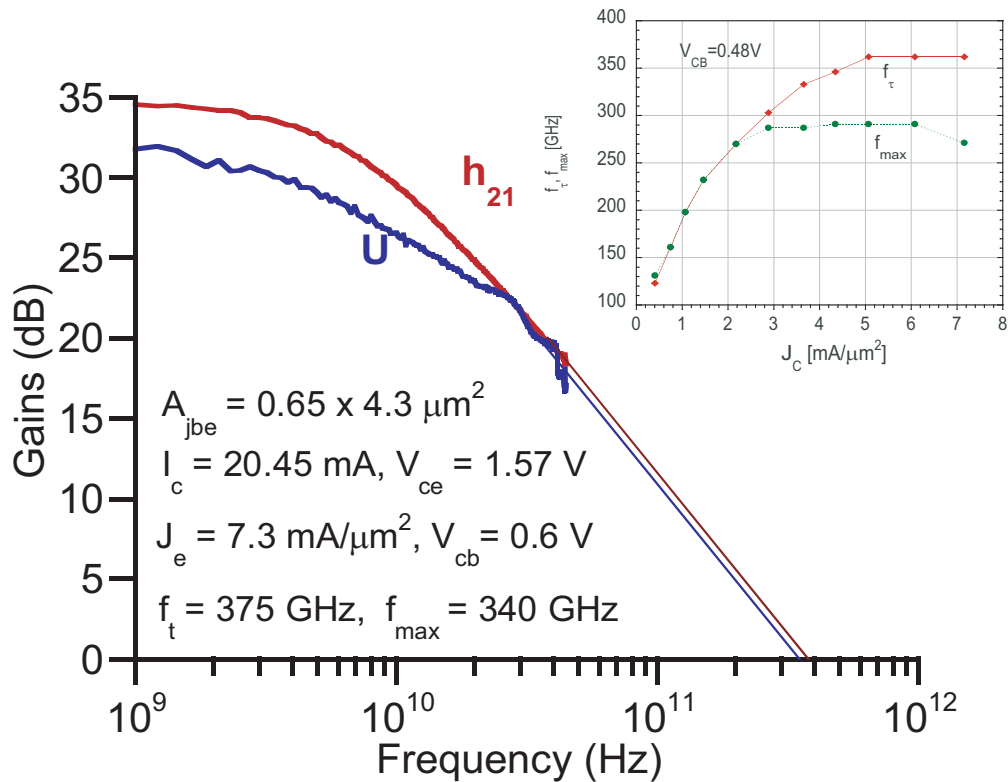
Figure 4.23: Microwave gains of Si implanted subcollector DHBTs

epitaxial, triple mesa DHBT. The base resistance is higher for these DHBTs(45 Ω vs. 35 Ω), since these were grown at UCSB where there are difficulties obtaining a high Carbon doping and hence lower base resistivity. Further, the collector resistance is higher (10 Ω vs. 2Ω) due to the poor ohmic contact. The capacitance voltage

characteristics of the implanted subcollector DHBTs at $I_c = 0$ mA, are plotted and compared with the standard mesa equivalent in Fig. 4.24. From the figure, contrary to the expected reduction, the C_{cb} is the same as that of the standard triple mesa device lower voltages. The C_{cb} is the same for the standard mesa device and the implanted subcollector DHBTs till ∼0.6V. $C_{cb,pad}$ is thus not eliminated. As seen from the CV plots, the capacitance of the implanted subcollector DHBTs where the pad is isolated progressively decreases with increasing bias. This is not seen in the triple mesa equivalent where the collector is fully depleted at ∼ 1V and the reduction in capacitance due to the Debye tail is negligible. In order to investigate this phenomenon, CV measurements ($I_c = 0$ mA) are made of devices where the base access pad is not isolated and plotted in Fig. **??**. The devices where the base access pad is isolated is similar to a standard mesa DHBT with a base access pad capacitance, since the Si implant is also performed in the regions under the base pad. It is seen from Fig. **??** that this capacitance decrease at high bias voltages is not observed for implanted subcollector DHBTs where the base pad is not isolated and closely follows the CV profile of the standard mesa DHBT. This data suggests the presence of some interface charge under the base access pad. This charge is progressively depleted at high collector base bias voltages and hence a reduction is seen in devices where the pad is isolated as in Fig. 4.1. The DC results compare with the standard mesa DHBT and hence indicate the feasibility of manufacturing microwave HBTs on implanted substrates. The RF results indicate that the expected C_{cb} reduction due to isolation of base access pad by implant is not present at low bias voltages. The capacitance due to the base access pad, $C_{cb,pad}$ is thus not eliminated at these voltages. This is attributed to an N-type charge at the growth interface which is depleted at progressively higher biases. The elimination of this interface charge is therefore crucial to the theoretically predicted operation of these implanted subcollector DHBTs.

4.5 Interface charge

It was seen from the previous section that there exists a positive interface charge that acts as terminating electrode for the base-collector electric field. This charge, if left uncompensated, results in incomplete depletion and hence no reduction in extrinsic C_{cb}. $C_{cb,pad}$ is thus still present in this bias range (till ∼3V). The interface charge is depleted at high bias voltages (∼ 4V) and hence there is a reduction in capacitance at those voltages. However, this is not very useful for bandwidth enhancement in transistor operation in InP based circuits.

The origin of this unintentionally introduced N-type conduction in exposed InP surfaces(epitaxial or substrate) is identified to be Si impurity states [22, 23]. These
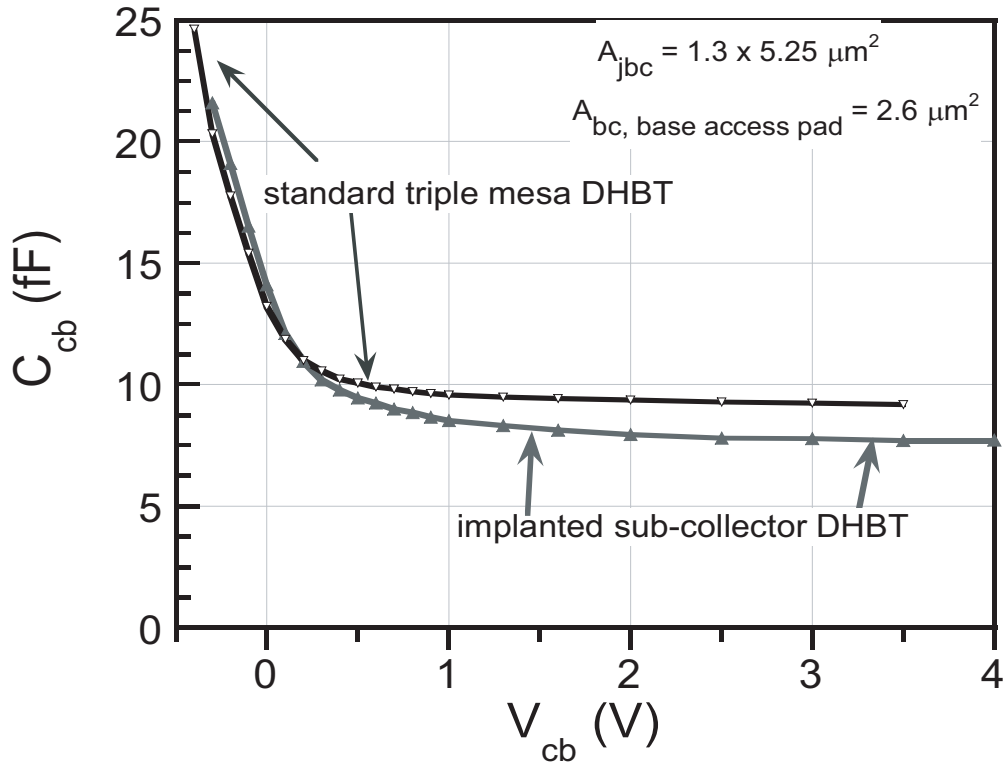
Figure 4.24: Capacitance voltage characteristics, at $I_c = 0$ mA, of implanted subcollector DHBTs with the base pad isolated

are verified by sheet charge measurements and SIMS. The Si donor states are formed as result of processing and also due to the ambient Si. Rhe Si atom sheet concentration was found to be proportional to the time of exposure to ambient air. The concentration of these Si donor states is thus heavily process dependent and is in the range of 1×10^{12} - 1×10^{13} cm^{-2}. This interface charge is also responsible for parallel conduction at the substrate interface in InP based HFETs. It is the cause of the low turn on, increased resistance and high capacitance in p-i-n InP based photodetectors, where the p layer is regrown and the interface charge is present on the surface of the i-layer. Regrown HBTs with implanted pedestals reported at UCSB [24] also suffer from this charge at the regrowth interface which resulted in no capacitance reduction at low bias voltages.

Several methods have been utilized for reduction of this interface charge, including advanced surface clean procedures [23], annealing in a phosphine ambient [22]

and overgrowth of a charge compensation layer [25]. This interface charge is process dependent and full compensation might not be possible with process techniques or an empirical p^{++} compensation layer.

4.5.1 Insufficient charge compensation with a p^{++} overgrowth

The interface charge is also present on epitaxially grown UID InP layers, as part of the pedestal process developed at UCSB [25]. Starting with a grown template of 200 nm UID InP over 300 nm N^{++} InP, Si is selectively implanted to form an N^{++} pedestal. The active collector, base and emitter layers are then regrown. Interface charge is present on the 200 nm UID epitaxial InP prior to regrowth and has the same effect as here. An empirically determined p^{++} In$_{0.53}$Ga$_{0.47}$As compensation layer was overgrown. In order to check the level of p^{++} doping required for compensation, various levels of p^{++} In$_{0.53}$Ga$_{0.47}$As from 2.5-7.5 $\times 10^{18}$ cm^{-3}, and a test sample with undoped In$_{0.53}$Ga$_{0.47}$As, are first overgrown on the template. This is followed by growth of the active device layer stack - the 120 nm N^- drift collector, base and emitter. This device has a 120 nm collector on UID InP and with sufficient compensation has a depletion depth of 320 nm. This is identical to the extrinsic region of the device in the regrown pedestal process [25]. Large area HBTs are fabricated and Capacitance - Voltage measurements indicate the extent of interface charge compensation. Fig. 4.25 shows the CV plots of the extrinsic device region with various levels of p^{++} compensation layers. As a result of interface charge, the layer without a p^{++} In$_{0.53}$Ga$_{0.47}$As layer has the largest capacitance at low bias voltages. The p^{++} In$_{0.53}$Ga$_{0.47}$As layer doped, in different samples, from 2.5-7.5 $\times 10^{18}$ cm^{-3} incompletely compensate the interface charge as seen in the partial reduction in capacitance. The capacitance at 1V, for the layers without any In$_{0.53}$Ga$_{0.47}$As overgrowth is $\sim$ 33 fF while the The capacitance at 1V, for the layers with 4 nm, 7.5 $\times 10^{18}$ cm^{-3} In$_{0.53}$Ga$_{0.47}$As overgrowth is $\sim$ 23 fF. Since the collector thickness is 120 nm and the thickness of the UID InP layer is 200 nm, if the interface charge is fully compensated, the expected capacitance when the collector is fully depleted is $\sim$13 fF. The tail in the CV at high biases indicates that the interface charge is insufficiently compensated and gets progressively depleted with increasing base collector voltage. As seen from the charge profile extracted from the CV data, there is a charge buildup at the growth interface, despite the 4 nm, 5e18 p^{++} In$_{0.53}$Ga$_{0.47}$As compensation layer. These results indicate that the empirical p^{++} layer is not a good solution to compensate the interface charge.

120 nm collector, 4 nm p+InGaAs overgrowth and 200 nm UID InP
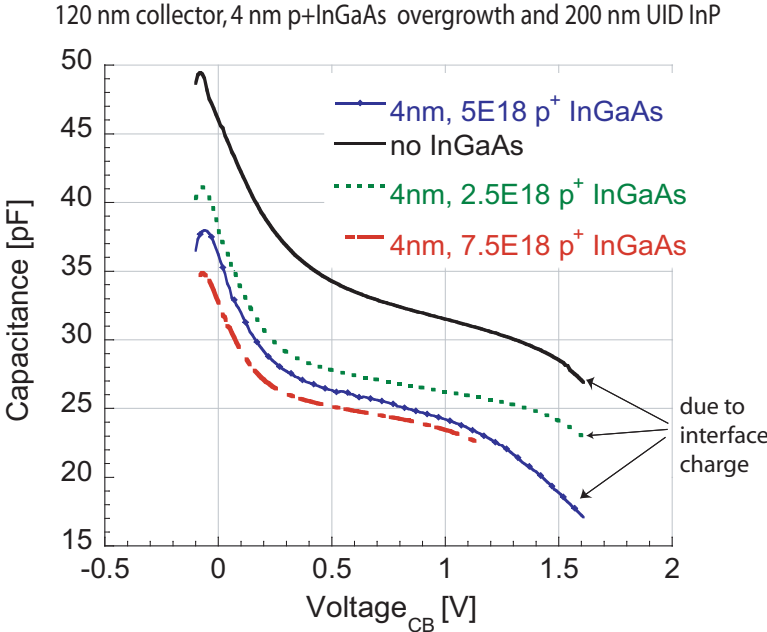
Figure 4.25: C-V measurements of HBTs where active device layers are grown over a 200 nm UID InP/300 nm N^{++} InP template. Various levels of p^{++} In$_{0.53}$Ga$_{0.47}$As layers are overgrown as the first layer on the template to determine the p^{++} doping required to compensate interface charge
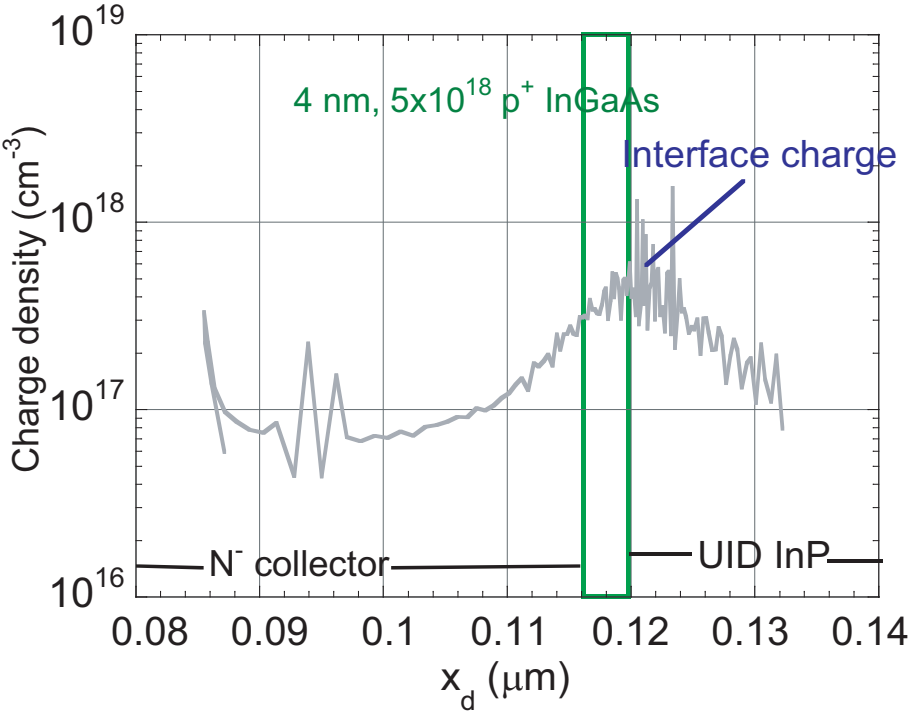
Figure 4.26: Interface charge density on 200 nm UID InP/300 nm N^{++} InP template with 4 nm of 5×10^{18} cm^{-3} p^{++} In$_{0.53}$Ga$_{0.47}$As overgrowth

4.5.2 Interface charge compensation using Fe implant

A new, robust technique is introduced in this dissertation wherein Fe implantation is used to eliminate this interface charge. As discussed in Chapter **??** , Fe is a mid-gap acceptor in InP and serves to compensate the donor states. Thus by sufficiently compensating the Si donor states with Fe, the N-type conduction at the interface is eliminated. The process thus involves, implanting a blanket sheet of Fe to compensate the interface charge. The subsequent selective Si subcollector implant then defines the isolated subcollector as in §**??**

The band diagram of the p^{++} $In_{0.53}Ga_{0.47}As$ and N^- collector region under the base pad is shown in Fig. **??** when there is an N-type interface present and the corresponding simulated CV profiles are shown in Fig. **??**. To first order, the electric field in the collector corresponds to,

$$\frac{\epsilon(V_{cb} + \phi_{bi})}{qT_c} = n_s + \frac{N_cT_c}{2} \tag{4.5.0}$$

where n_s is the regrowth interface charge density, N_c is the doping in the drift collector, and T_c is the thickness of the drift collector, ϕ_{bi} is the built-in potential of the base-collector junction and V_{cb} is the base-collector reverse bias voltage. In order to ensure complete charge depletion at the regrowth interface in the region under the base pad area

$$\frac{\epsilon(V_{cb} + \phi_{bi})}{qT_c} + n_{Fe} \geq n_s + \frac{N_cT_c}{2} \tag{4.5.0}$$

where n_{Fe} is the density of active Fe in cm^{-2}. If the collector is so designed as to be fully depleted at zero bias, then

$$\frac{\epsilon\phi_{bi}}{qT_c} = \frac{N_cT_c}{2} \tag{4.5.0}$$

Therefore $n_{Fe} \geq n_s$ for full charge compensation, even at zero bias. The Fe implant conditions are chosen to satisfy the above requirement. The conditions for the Fe implant are as follows

- The Fe implant conditions should be selected to fully compensate the N-type charge at the growth interface between the substrate and collector epitaxial layers, over the observed 1 5 $\times 10^{12}$ cm^{-2} range of regrowth interface charge densities.

- Some of the surface is unintentionally attacked during various process steps. The Fe implant should be therefore be sufficiently deep.

- Fe is a heavy ion and causes significant damage to the crystal. This should be completely annealed out before growth.

- The Fe implant should not be very high since the subsequent Si implant should overcome the Fe doping to form a highly N^{++} subcollector for the active device regions.

A experiment, similar to the one in §4.5.1, to check C-V curves of large area devices is performed to verify the compensation of interface charge by Fe. In order to determine the Fe doping required for complete compensation, Fe is implanted, at 50 KeV at three different fluences in a similar grown template, 200 nm UID InP over 300 nm N^{++} InP. These were then annealed at 700 °C for 5 minutes, which is shown in Chapter 5 to be sufficient to repair the lattice damage due to Fe implant for fluences below 2.4×10^{14} ions/cm^2. The active layers(with a 150 nm collector) are immediately grown after the Fe implant. Since the Fe implant is intended to compensate the interface charge, these do not have a compensating p^{++} overgrowth. Large area devices are fabricated to determine C-V characteristics . A fully epitaxial, standard DHBT with similar active layer structure is also co-processed for comparison. From Fig. 4.27 it is seen that the capacitance is reduced over the entire measured range of bias voltages, for all fluences of Fe. Thus the interface charge is fully compensated even for a fluence as low as 1×10^{13} cm^{-2}. Capacitance when collector is fully depleted for fully epitaxial DHBT is 1 fF/μm^2. Capacitance when collector is fully depleted for Fe implanted, regrown DHBT is 0.42 fF/μm^2. This corresponds to a depletion depth of $\approx$ 350 nm. $T_c(150nm) + T_{undopedInP}(200nm)$ = 350 nm. The depletion depth is increased and capacitance is therefore reduced, exactly as expected in the extrinsic device regions.

Fig. 4.28 and Fig. 4.29 shows further evidence of compensation of interface charge by Fe implant at two different fluences. In LACVD 3 and LACVD 6, Fe is selectively implanted. Since Fe is present only in the extrinsic region, current blocking effects (if any) due to Fe traps are removed. In both figures, LACVD1 and LACVD2 have similar profiles which is again proof that Si doping is sufficiently high to counter compensate Fe that no shift in built in voltages are observed. In LACVD5 and LACVD6, the effect of interface charge is observed, where the capacitance starts to decrease at $\sim$ 2V of reverse bias.
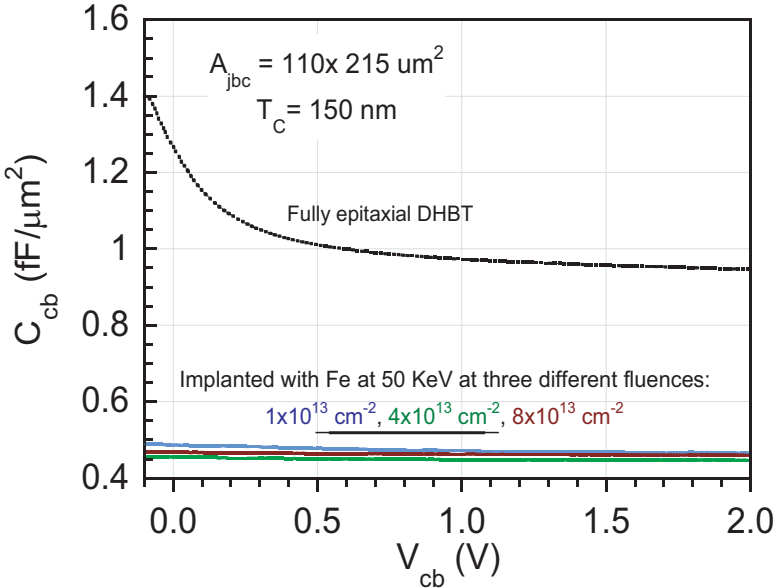
Figure 4.27: CV measurements of pedestal templates implanted with varying degrees of Fe compared with a standard, fully epitaxial DHBT
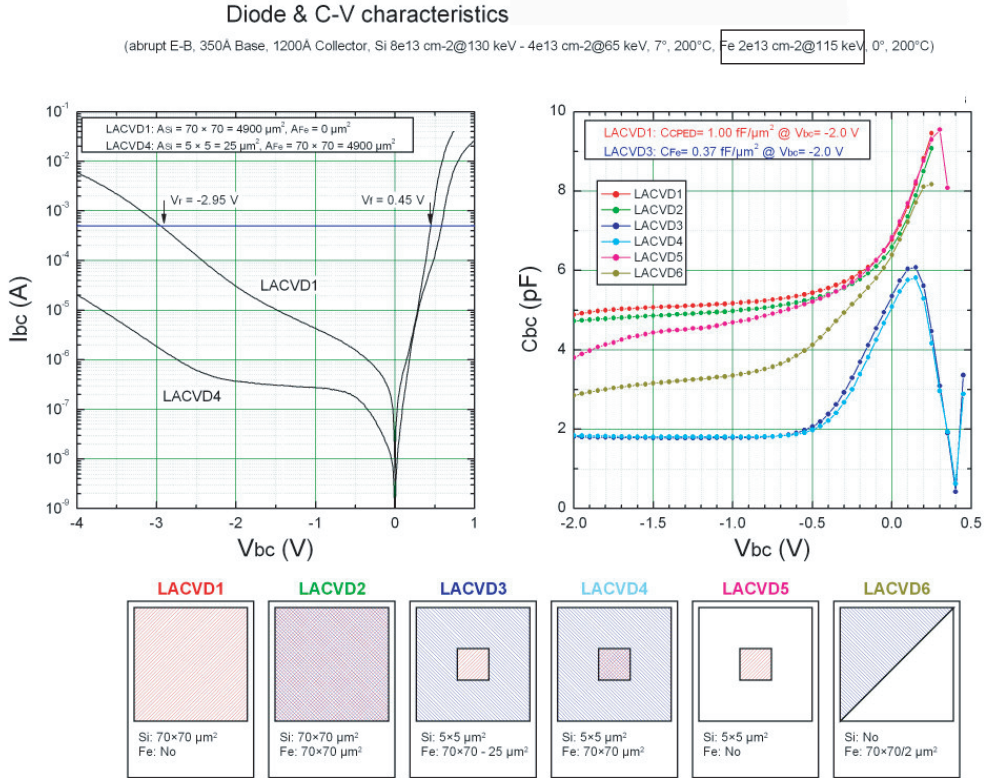
Figure 4.28: C-V's of various test structures: Fe is implanted at 2×10^{13} ions/cm^2: This data was obtained at RSC
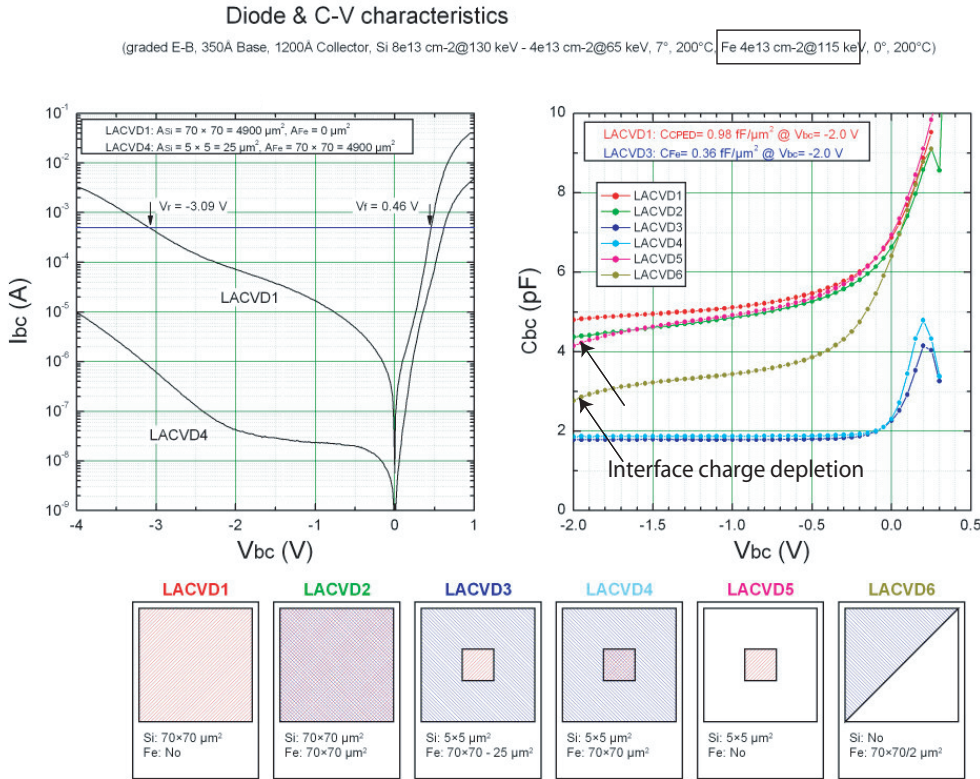
Figure 4.29: C-V's of various test structures: Fe is implanted at 4×10^{13} ions/cm^2: This data was obtained at RSC

4.5.3 Large area devices with Si and Fe implants

The selective Si subcollector implant that follows the blanket Fe implant must dope the region N^{++}. Large area HBTs are fabricated on templates with and without Si implant. On one set of templates, the active layers(with a 150 nm collector) are immediately grown after a 50 KeV, 2×10^{13} ions/cm^2 Fe implant. It was seen from the previous experiment that any fluence $\geq$ is sufficient for interface charge compensation. One another set of templates, following the Fe implant, a blanket Si implant similar to the one used for the implanted subcollector DHBT, is carried out and the active device stack is then grown. A fully epitaxial, standard DHBT with similar active layer structures is also co-processed as a comparison. Fig. 4.30 shows the C-V profile of the three different test structures. The std. mesa DHBT with 150 nm collector has a capacitance of ≈ 0.8 fF/μm^2 when fully depleted. The HBT overgrown on Fe implanted template has a capacitance of ≈ 0.34 fF/μm^2. In the intrinsic region under the emitter, the N^+ pedestal is present. This is exactly represented by the large area HBT where both Si and Fe are implanted prior to growth. The CV characteristics where Si and Fe are implanted, in Fig. 4.30, is similar to the standard mesa DHBT. This is to be expected, since a blanket N^+ pedestal layer is akin to a N^{++} subcollector layer. The built-in voltage of the base collector junction of the pedestal HBT is similar to the fully epitaxial HBT. This is the expected performance in the intrinsic portion of the device.
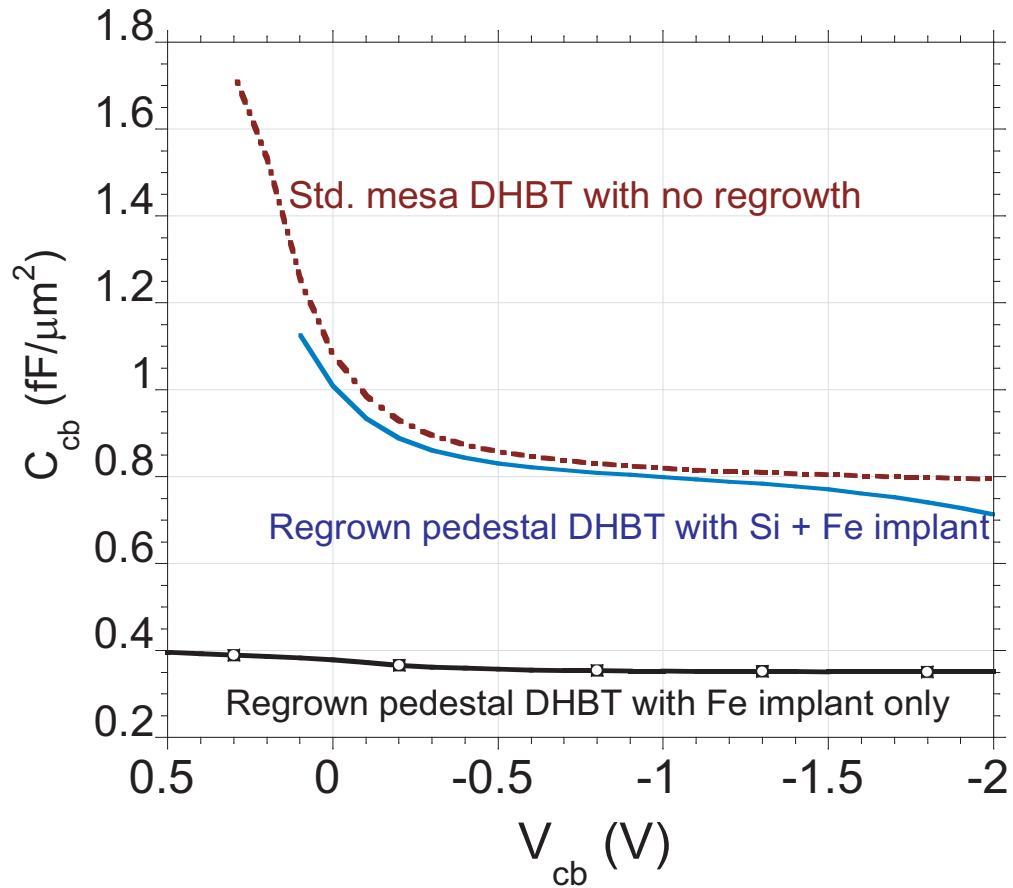
Figure 4.30: C-V characteristics of standard fully epitaxial HBT, regrown HBT with only Fe implant on 200 nm UID InP/ 300 nm N^{++} InP template, and regrown HBT with Fe and Si pedestal implants on 200 nm UID InP/ 300 nm N^{++} InP template
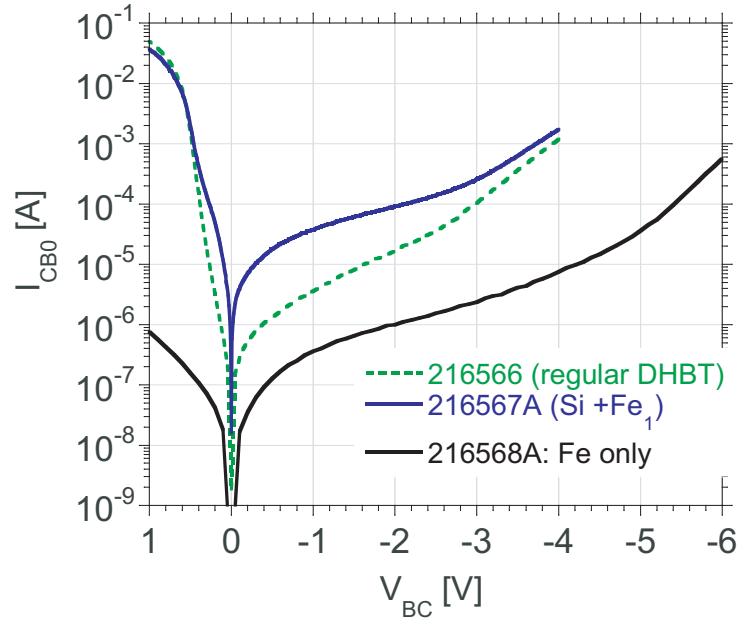
Figure 4.31: Comparison of reverse base collector leakage characteristics of std. mesa HBT, regrown HBT with Fe implanted on 200 nm UID InP/ 300 nm N^{++} InP template, and regrown HBT with Fe and Si pedestal implants on 200 nm UID InP/ 300 nm N^{++} InP template

The base collector leakage for the regrown device with Si and Fe implants is similar to a fully epitaxial HBT. The base collector leakage plot shows that I_{CBO} at 3V ~ 0.1 mA (10×10^{-6} $mA/\mu m^2$). For a microwave device with a base collector junction of ~ 7 μm^2, I_{CBO} and gain of ~ 50, I_{CEO} is $\approx 3.5 \times 10^{-3}$ $mA/\mu m^2$. This is a very small leakage current at 3V. The DC $I_C - V_{CE}$ characteristics do not shown any current blocking due to the Fe implant. The offset voltages and breakdown voltages are consistent with those measured for similar large area, fully epitaxial HBTs. There is a high series collector resistance which is possibly due to low doping in the pedestal(Si is implanted at 150 KeV / 2×10^{13} ions/cm^2 to minimize implant straggle which will be addressed in Chapter **??**).

Low collector contact resistivity and sheet resistance are obtained in §**??** even with an Fe implant. Therefore the Si implant sufficiently overcomes the Fe implant to form an N^{++} subcollector (or pedestal) and does not hamper the collector ohmic contact.
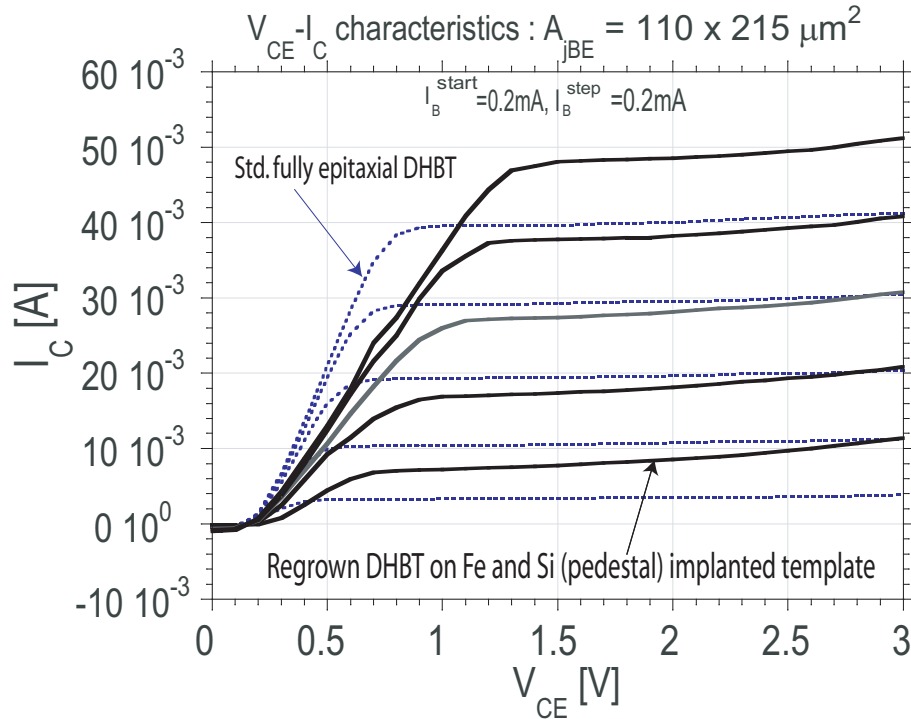
Figure 4.32: DC characteristics of regrown HBT with Fe charge compensation implant and Si pedestal implants on 200 nm UID InP/ 300 nm N^{++} InP template. The device characteristics of the standard fully epitaxial DHBT is shown for comparison

4.6 Implanted subcollector DHBTs with Fe

The process is modified to have include a blanket shallow Fe implant. It was seen from the previous section, that Fe implant with fluences $\geq 1 \times 10^{13}$ions/cm^2 is sufficient to compensate the residual interface charge. Fig. **??** shows the profile of the Fe at the implant conditions chosen, and also the Si subcollector implant. A low energy Fe is chosen to minimize current blocking effects and to ease the requirements on Si implants. Assuming ~ 10 nm of the surface is removed, the active Fe concentration is $\sim 1 \times 10^{13}$ cm^{-2}. This is much larger than the observed range of interface charge densities. The Si doping at the surface is designed to be high enough to enable a low collector contact resistance.

The process flow of the implanted subcollector HBT with Fe is shown in Fig. 4.33. A semi-insulating InP substrate is blanket implanted with Fe at 10 keV, at a fluence of 2×10^{13} ions/cm^2 as in Fig. **??**a. The wafer is then annealed in the RTA at 700

°C for 5 minutes to activate the Fe and to repair crystal damage. The process flow that follows is identical to that of the implanted subcollector HBT without Fe, described in §**??**. TiW alignment targets are defined. The sample is then selectively implanted, using Si_xN_y as the implant mask, with Si. The Si and Fe implant conditions are given in Table 4.6. The Si implants are activated by annealing at 800°C/10s. The Si implant dose is much larger then the Fe acceptor density in the selectively implanted region. This ensures that a highly doped, isolated subcollector region is formed. The base access pad lies outside the subcollector implant boundary and, in the absence of interface charge, does not contribute to C_{cb}. The active InP HBT layers are then grown by MBE. The device drift collector, base, and emitter layers for both wafers are identical to that of the DHBTs reported in §4.4. As before, Growth is initiated with a 3.5nm undoped InGaAs etch-stop layer between the InP collector and the InP substrate. The drift collector, base, and emitter layers are grown. Devices are formed by wet-etching the emitter and base mesas. The collector contact used is Ni/Ge/Au/Ni/Au as in §4.1.2 and are annealed at 320 °C.

Table 4.6: Implant conditions for implanted subcollector HBT process with Fe

Implant species	Implant energy	Implant fluence	Offset angle	Implant temperature
Fe	10 KeV	2×10^{13} ions/cm^2	7 °	200 ° C
Si	200 KeV	3×10^{14} ions/cm^2	7 °	200 ° C
	40 KeV	8×10^{13} ions/cm^2		
	10 KeV	3×10^{13} ions/cm^2		
$I_{ions} \leq 10\mu$A				

The sheet resistance of the subcollector with Si and Fe implant is determined from Hall measurements and shown in Table **??**. The different anneal conditions

Table 4.7: Hall measurements of resistivity and mobility for Si implants

Anneal temperature (°C)	Anneal time (s)	Hall mobility $(cm^2/V \cdot s)$	Carrier density (cm^{-2})	Sheet resistance $(\Omega/\square)$
700	60	925	2.6×10^{14}	26
750	60	956	2.5×10^{14}	26
700	300	905	2.5×10^{14}	27
750	300	872	2.7×10^{14}	26
800	10	710	3.3×10^{14}	27
800	30	886	2.8×10^{14}	25

shown here, all yield a subcollector sheet resistance $\sim$ 25-27 $\Omega/\square$. 800 °C for

30 seconds was chosen as the activation anneal for all Si implants. Ignoring the effect of Fe, the activation is $\approx 56\,\%$. These are similar to the values obtained for the implanted subcollector DHBTs without Fe. The surface Fe does not affect the resistivity of the subcollector.

Non selective Fe implant

Semi Insulating InP substrate

Activation anneal

Silicon implant

Fe

Semi Insulating InP substrate

Activation anneal
& MBE growth

emitter
base
drift collector

Fe   Fe

Isolated Subcollector

Semi Insulating InP substrate

mesa HBT fabrication

Fe   Fe

Isolated Subcollector

Semi Insulating InP substrate
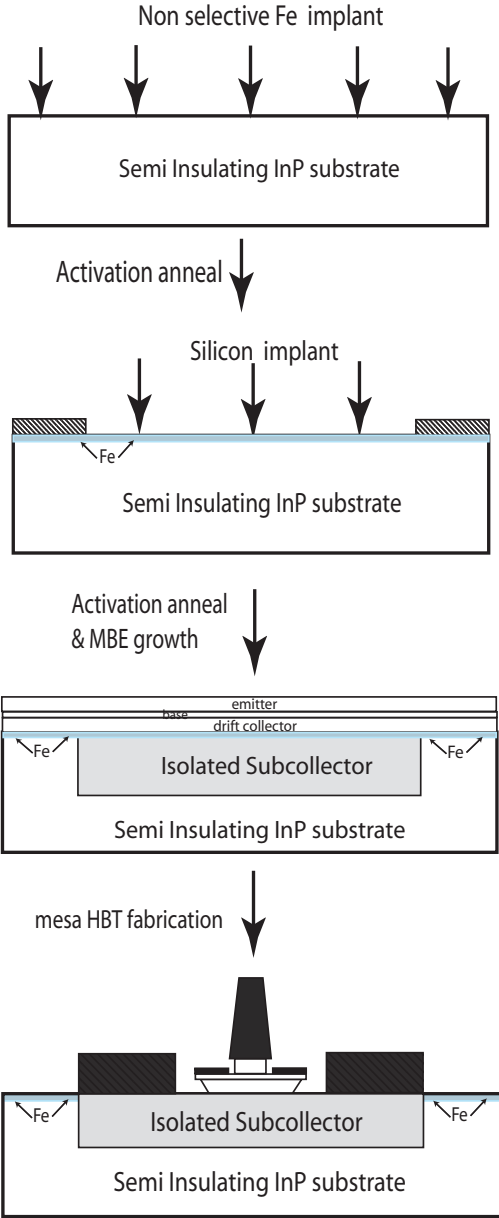
Figure 4.33: Process flow of the Implanted subcollector DHBT with Fe

4.7 Device Results - Si Implanted subcollector DHBTs with Fe

Large area devices have shown low leakage and excellent DC characteristics. Small area devices were processed with the identical layer structure shown in Table 4.5. The process has already been described in §4.4.1.

The TLM measurements of the collector and, of the pinched and non-pinched base TLMs are given in Fig. 4.34. The collector contact resistance is very high $\approx 500 \ \Omega \cdot \mu m^2$, while the sheet resistance is similar to that obtained in §4.4. Due to the 320°C anneal for the collector ohmics, the base ohmics also have high contact resistivity of $\approx 165 \ \Omega \cdot \mu m^2$. The Isolation between ohmic pads separated by 10 μm is 20 pA/μm. Fig. 4.35 is a plot of the DC $I_C - V_{CE}$ characteristics. There is no

Layers	R_{sh} (Ω/sq)	ρ_c ($\Omega-\mu m^2$)	ρ_{horz} ($\Omega-\mu m$)	L_T (μm)
Base	1050	164	415	0.40
Collector	25	500	112	4.48
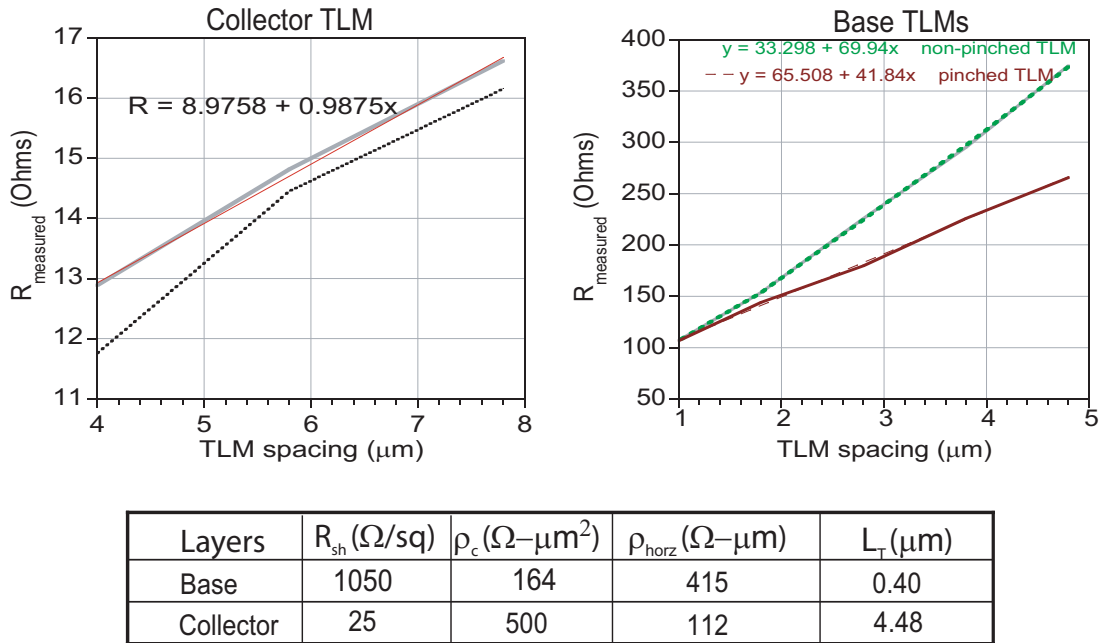
Figure 4.34: Base and Collector TLM measurements

evidence of gain compression till $\approx 7 \ mA/\mu m^2$ at $V_{cb} = 0$V. The Gummel curves are plotted for V_{cb} =0V and V_{cb} =0.3V Fig. 4.36. The collector and base ideality factors are $\eta_c = 1.11$ and $\eta_b = 1.58$., consistent with those obtained for fully epitaxial DHBTs. The leakage current I_{CEO} from the gummel curves is ≈ 1 nA at $V_{cb} = 0.3$V. The DC current gain of the transistor = I_c/I_b from the gummel curves is shown in

Fig. 4.37. The HBT's gain compression point is $\approx 4\ mA/\mu m^2$ at $V_{cb} = 0$V and 6 $mA/\mu m^2$ at $V_{cb} = 0.3$V. At high current densities, $V_{CB,i} = VCB, applied - I_C R_c$. From the TLMs and the geometry of the transistor, R_c for this transistor is $\approx 22\ \Omega$. At $I_c \approx 15$mA, $V_{CB,i} = VCB, applied$ - 0.3V. The base collector junction is forward biased till $V_{CB,applied}$ is ≈ 0.3V. Shown in Fig. 4.38 are I_{CEO} and I_{CBO}. The
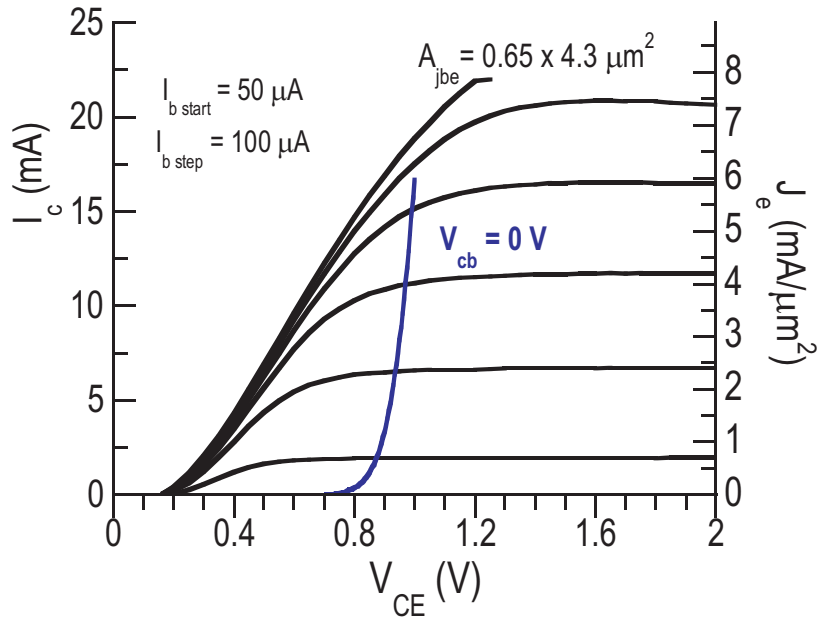
Figure 4.35: DC $I_C - V_{CE}$ characteristics

breakdown voltages are defined at $I_c = 1$ mA. $BV_{CEO} = 5.6$V and $BV_{CBO} = 6.9$V. For a fully epitaxial, standard mesa DHBT, the corresponding voltages are $BV_{CEO} = 5.5$V and $BV_{CBO} = 6.8$V at $I_c = 1$mA. The resistance as seen in the emitter, $R_{ex} + R_{bb}/\beta$ is derived from gummels and plotted as function of current density Fig. 4.39. $R_{bb}/\beta \approx 1\ \Omega$ and therefore $R_{ex} \approx 8\ \Omega$. Also plotted in Fig. 4.39is the thermal resistance,$\Theta_{th} \cdot \phi$ (also referred to as R_{th}). The thermal resistance at 5 $mA/\mu m^2$ is 2.6 deg K/mW. The collector resistance is extracted from the $I_C - V_{CE}$ characteristics of the transistor at saturation, using the Fixed β method and is plotted in Fig. 4.40. The emitter resistance , $R_{ex} \approx 8\ \Omega$, the collector resistance is determined to be $\approx 22\ \Omega$, consistent with the value calculated from TLM measurements. This is very high compared to the value of 1Ω that is typically obtained and is due to the poor ohmic contact to N^{++} InP. Contact resistivities as low as $7\ \Omega \cdot \mu m^2$ have been obtained with ohmics to N^{++} InP. Therefore the ohmic contact process can be improved.
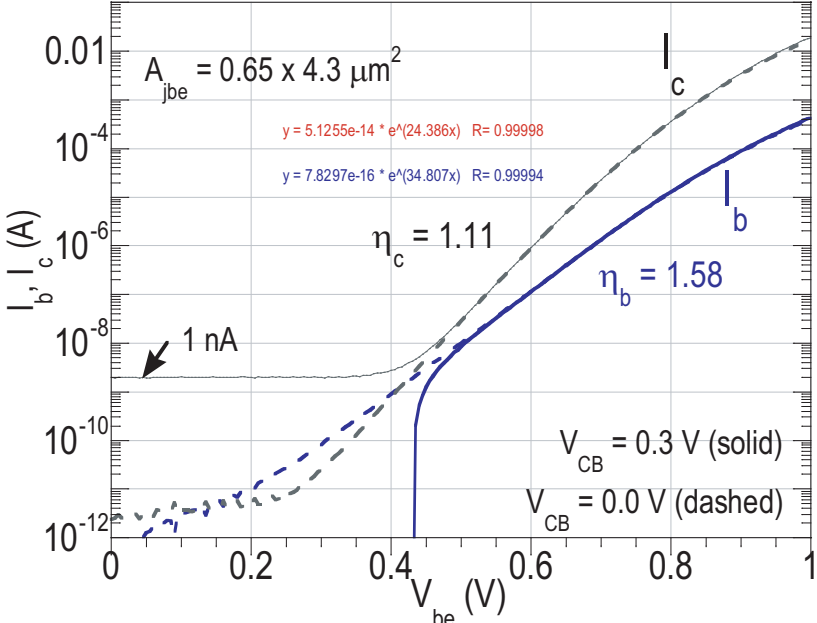
Figure 4.36: Gummel curves at $V_{cb} = 0V$ and 0.3V

The device DC current gain, ideality factors, and breakdown voltages are consistent with those measured from the triple-mesa HBT equivalent [3].
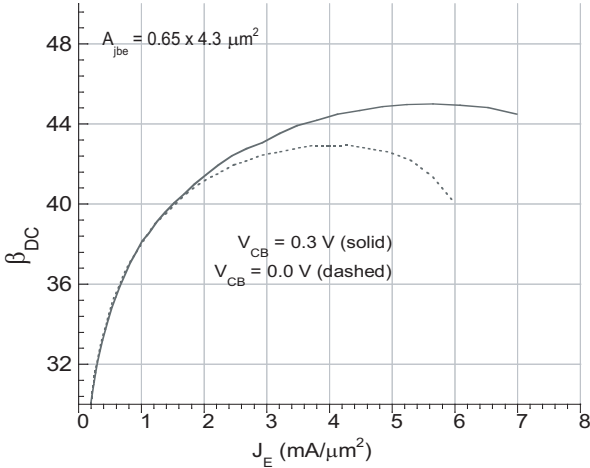
Figure 4.37: DC gain of the HBT at $V_{cb} = 0V$ and 0.3V
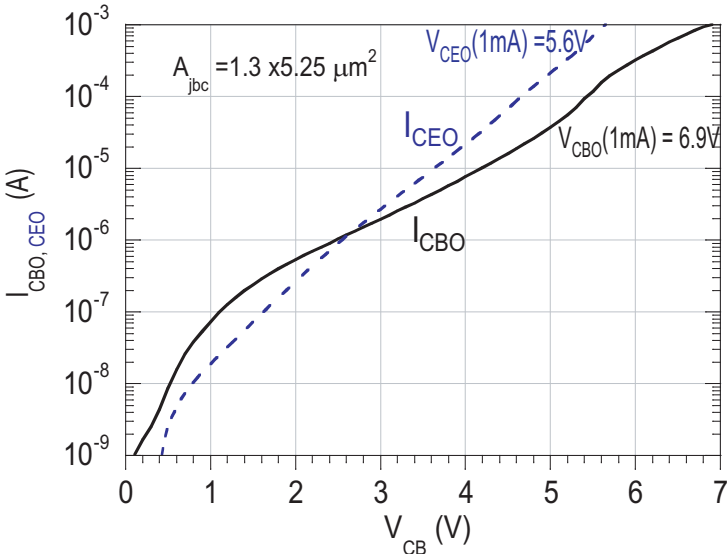
Figure 4.38: Leakage currents in the device
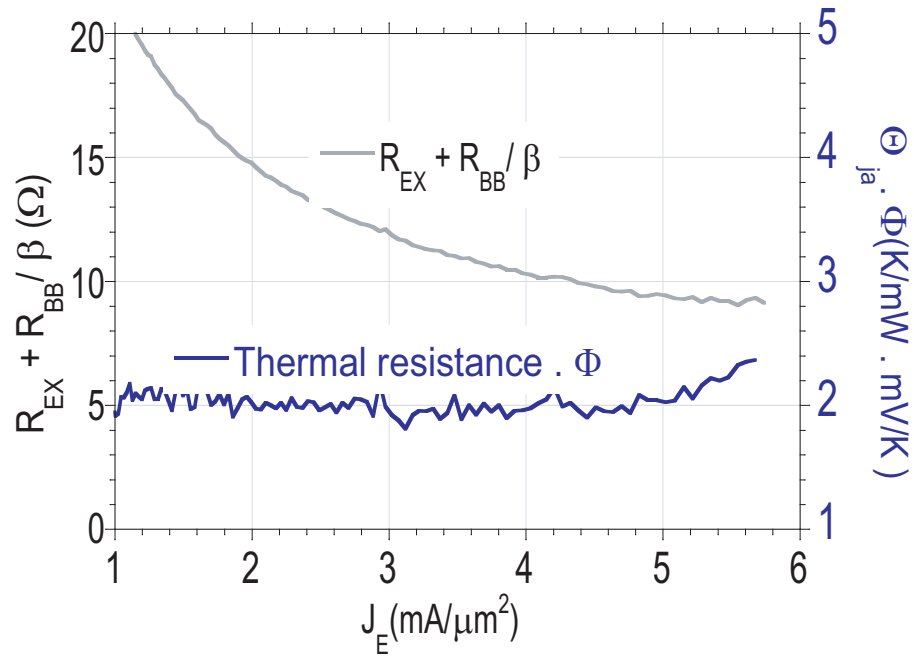
Figure 4.39: Extraction of Emitter resistance, and thermal resistance
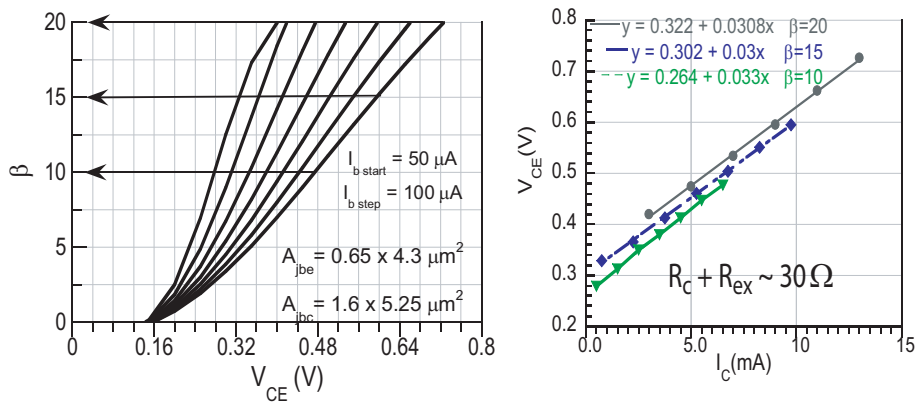
Figure 4.40: Extraction of Collector resistance

DC-45 GHz S-parameter measurements are carried out after performing an off wafer Line-Reflect-Reflect-Match calibration on an Agilent 8510C network analyzer. On-wafer open and short circuit pad structures identical to the ones used by the devices are measured after calibration in order to de-embed their associated parasitics from the device measurements. f_{max} is determined from extrapolation through a least-square-fit between the transfer function,

$$U(f) = \frac{U_{DC}}{1 + U_{DC} \cdot (f/f_{max})^2} \tag{4.7.0}$$

to the measured microwave gain U at measured frequencies. $1/f_\tau$ is the slope of $\text{Im}(1/h_{21})$ [26] and is shown in Fig. 4.41. This method is more exact than a least square fit to,

$$|h_{21}(f)|^2 = \frac{1}{1/\beta^2 + (f/f_\tau)^2} \tag{4.7.0}$$

From these, $f_{max} \approx 410$ GHz and $f_\tau \approx 362$ GHz. These are lower than the standard, fully epitaxial, triple mesa DHBT. The base resistance is higher for these DHBTs(45 Ω vs. 35 Ω), since these were grown at UCSB. Further, the collector resistance is much higher (22 Ω vs. 2Ω) due to the poor ohmic contact.

The capacitance voltage characteristics of the implanted subcollector DHBTs with Fe at $I_c = 0$ mA, are plotted and compared with the standard mesa equivalent in Fig. 4.24 and those of the implanted subcollector DHBT without Fe from §4.4. From the figure, The implanted subcollector DHBTs with Fe exhibit a C_{cb} reduction of ≈ 3 fF over the entire measured range of bias voltages due to elimination of the charge dipole at the growth interface. At full depletion, this corresponds to a 25% decrease in C_{cb}, which corresponds to the area of the base access pad. In contrast, the implanted subcollector DHBT without Fe detailed in §4.4, exhibit the same reduction only at very high bias voltages. The standard, fully epitaxial mesa DHBTs have a larger collector base capacitance due to $C_{cb,pad}$ being present. $C_{cb,pad}$ is thus eliminated using the implanted subcollector DHBT process with Fe. $A_{jBC} = 1.3 \times 5.25 \mu m^2$ $A_{pad} = 2.5 \mu m^2$. $C_{cb,pad}$ is thus ~ 28 % for this device.

The hybrid-pi model is extracted from the S-parameter and DC measurements. The S-parameters used to obtain the model correspond to those obtained at peak f_τ and f_{max} which is at $J_e = 6.8$ $mA/\mu m^2$ and $V_{cb} = 1.97$ V. The hybrid-pi model at I_c = 19.1 mA and $V_{cb} = 1.97$ V is shown in Fig. 4.44. The S -parameters of the actual device and the model are shown to closely agree in Fig. 4.45.

Device DC_7 does not have the base pad isolated and its CV profile is shown in Fig. 4.46. The capacitance is the same for all three processes indicating that they are equivalent, as far as $C_{cb,pad}$ is concerned. This is also further proof, that the decrease in capacitance is indeed due to the base access pad being isolated and not a fictitious
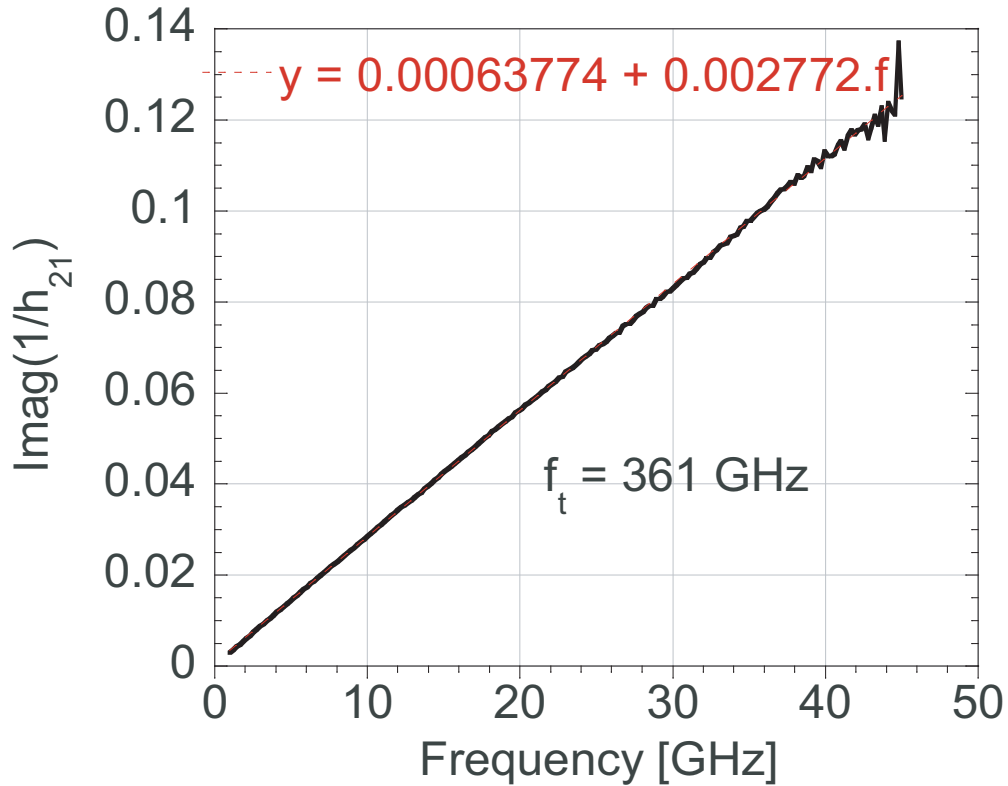
Figure 4.41: Extraction of f_τ- The slope of Imag(1/h$_{21}$) is f_τ

decrease due to variations in collector doping during growth, processing etc. For this device, $A_{j,BC} = 2.1 \times 5.25$ μm^2, $A_{pad} = 2$ μm^2. This corresponds to $\hat{C}_{cb} \approx 1.1$ fF/μm^2. Additional CV measurements of devices of different geometries shown in Fig. **??** determine the effective base collector area contributing to capacitance. Using $\hat{C}_{cb} \approx 1$ fF/μm^2 from Fig. 4.46, Table 4.8 shows the measured C_{cb} at full depletion for devices of various geometries and the effective pad area actually isolated, with subcollector implant boundary as drawn in Fig. 4.1.
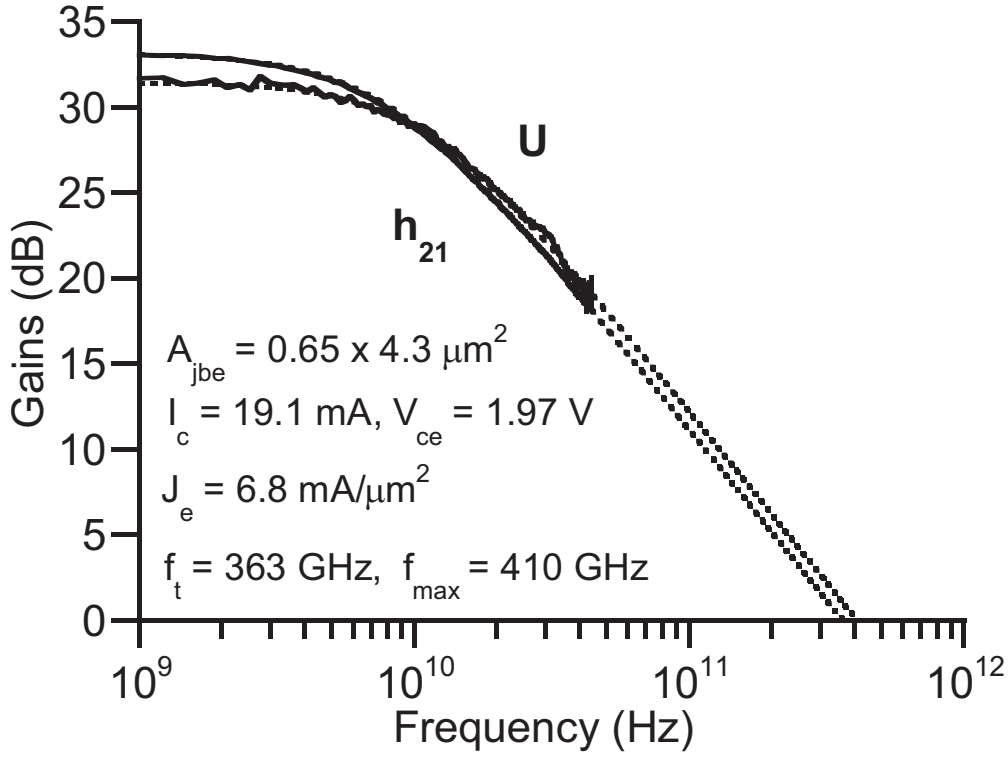
Figure 4.42: Microwave gains of Si implanted subcollector DHBTs

Figure 4.43: Capacitance voltage characteristics, at $I_c = 0$ mA, of implanted subcollector DHBTs with the base pad isolated

Figure 4.44: Hybrid-π device model at peak f_τ, f_{max}
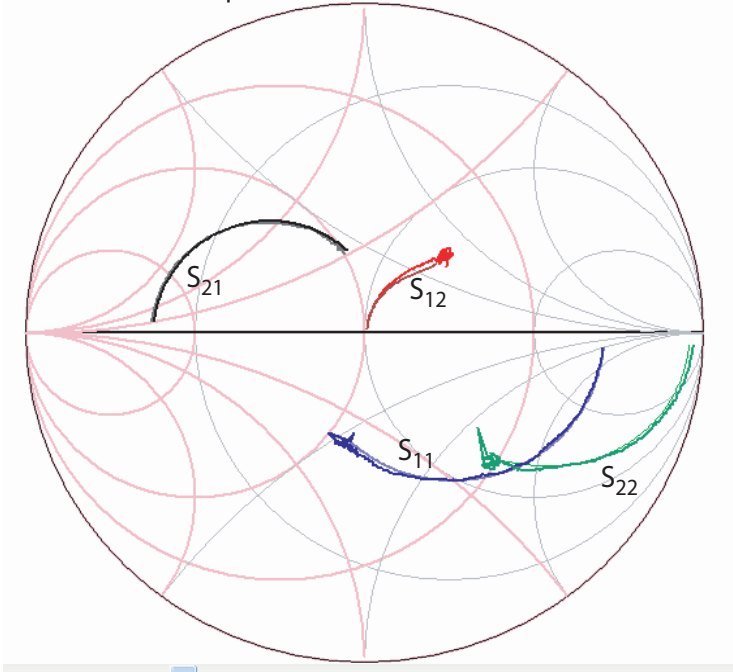
Figure 4.45: Measured S-parameters of the HBT and simulated S-parameters of the extracted hybrid-π equivalent circuit
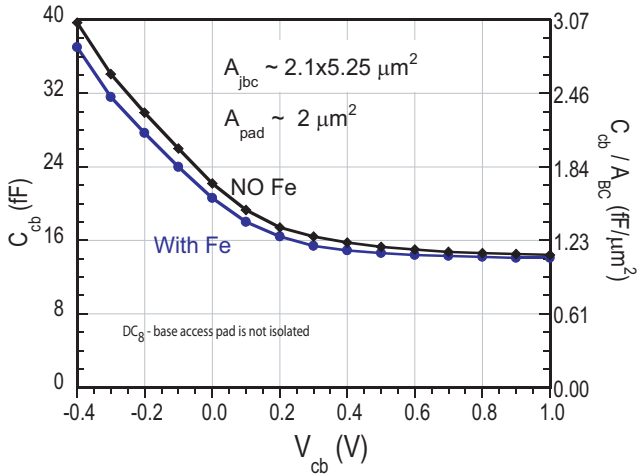
Figure 4.46: Capacitance voltage characteristics, at $I_c = 0$ mA, of implanted subcollector DHBTs with the base pad *not isolated*
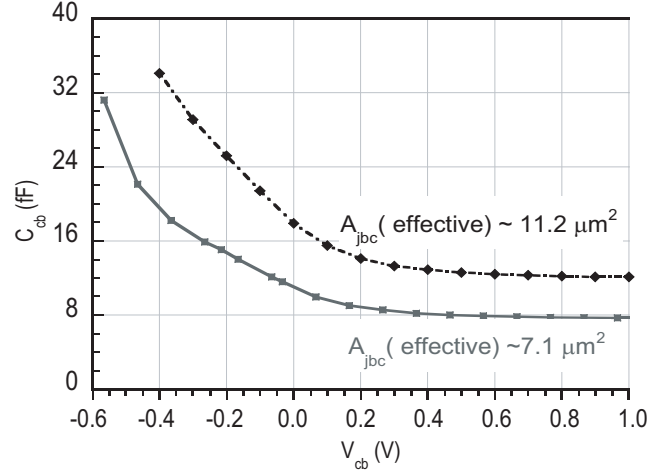
Figure 4.47: Capacitance voltage characteristics, at $I_c = 0$ mA, of implanted subcollector DHBTs with Fe, of different geometries with the base pad *isolated*

The slightly lower C_{cb} reduction than expected, is due to longitudinal implant straggle. Thus C_{cb} in the extrinsic region can be reduced even further by optimizing the design of the subcollector implant boundary in the photo mask. The DC results compare with the standard mesa DHBT and hence indicate the feasibility of manufacturing microwave HBTs on the doubly implanted substrates. The RF results indicate that C_{cb} is reduced corresponding to isolation of base access pad by implant, over the entire range of bias voltages. The interface charge dipole has been suppressed by the compensating Fe implant. The C_{cb} reduction would be more sig-

Table 4.8: Effective base access pad area isolated. The % C_{cb} reduction expected is in parenthesis

Device name	$A_{j,BC}$ on mask (μm^2)	A_{pad} on mask (μm^2)	C_{cb} at 1V (fF)	A_{pad} isolated (μm^2)	Actual(expected) % reduction in total C_{cb} (%)
DC1	1.1×5.25	2.55	6.77	2.07	25(30)
DC3	1.5×5.25	2.15	9.06	1.66	17(21)
DC4	1.5×7.25	2.75	11.77	2.73	20(20)
DC5	1.2×5.25	2.6	7.29	2.15	24(29)
DC6	1.2×7.25	2.6	9.58	2.43	21(23)
DC7	1.6×7.25	2.8	12.18	3.13	22(19)
DC15	2.1×5.25	2.85	12.0	2.13	16(17)

nificant for shorter length devices. The high collector contact resistance has resulted in lower f_τ and f_{max} compared to [3]. The ohmic contact process can be fixed by reversing the order of the base and collector ohmics. This permits a high temperature anneal for the collector ohmics reducing contact resistivity to $\approx 25\ \Omega \cdot \mu m^2$.

References

[1] M. Urteaga, P. Rowell, R. Pierson, B. Brar, M. Dahlström, Z. Griffith, M.J.W. Rodwell, S. Lee, N. Nguyen, and C. Nguyen, "Deep submicron InP DHBT technology with electroplated emitter and base contacts", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 239-240.

[2] M. Le, G. He, R. Hess, P. Partyka, B. Li, R. Bryie, S. Rustomji, G. Kim, R. Lee, J. Pepper, M. Helix, R. Milano, R. Elder, D. Jansen, F. Stroili, J-W. Lai, and M. Feng, "Self-Aligned InP DHBTs for 150 GHz Digital and Mixed Signal Circuits", *IEEE Int. Conf. on Indium Phosphide and Related Materials*, Glasgow, Scotland, May 8-13, 2005.

[3] Z. Griffith, M. J. W. Rodwell, X.-M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and W. K. Lui, "InGaAs/InP DHBTs with 120 nm collector having simultaneously high f_τ, $f_{max} \geq 450$ GHz", *IEEE Electron Device Letters*, vol. 26, no. 8, pp. 530-532, 2005.

[4] Z. Griffith, M. Dahlström, M. J. W. Rodwell, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, and C. Nguyen, "Ultra High Frequency Static Dividers > 150 GHz in a Narrow Mesa InGaAs/InP DHBT Technology", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Montreal, Canada, pp. 176-179, 13-14 September, 2004.

[5] W. Hafez, J. W. Lai, and M. Feng, "Submicron InP-InGaAs single heterojunction bipolar transistors with f_τ of 377 GHz", *IEEE Electron Device Letters*, Vol. 24(5), pp. 292-294, May 2003

[6] M. Ida, S. Yamahata, H. Nakajima, and N. Watanabe, "High-performance small InP/InGaAs HBTs with reduced parasitic basecollector capacitance fabricated using a novel base-metal design", *Proc. Int. Symp. on Compound Semiconductors (ISCS)*, 1999 No. 166, pp. 293296.

[7] F. Ren et al., "Implant isolation of GaAs-AlGaAs heterojunction bipolar transistor structures",*Applied Physics Letters*, vol. 56(9), pp. 860-862, Feb. 1990

[8] "Properties of INDIUM PHOSPHIDE", *INSPEC Electron EMIS Datareviews Series No 6*, 1991

[9] R. E. Williams, "Modern GaAs Processing Methods", *Artech House Publishers*Jul. 1990

[10] T. C. Shen, G.B. Rao, H. Morkoc, "Recent developments in ohmic contacts for III-V compound semiconductors", *Journal of Vacuum Science and Technology*, B10(5), Sep.- Oct. 1992

[11] A. Katz, B. E. Weir, S. N. G. Chu, P. M. Thomas, M. Soler, T. Boone, and W. C. Dautremont-Smith "Pt/Ti/n-InP nonalloyed ohmic contacts formed by rapid thermal processing", *Journal of Applied Physics*, – Vol. 67(8), pp. 3872-3875, Apr. 1990

[12] W. C. Dautremont-Smith, P. A. Barnes and J. Y. Stayt. Jr, "A nonalloyed, low specific resistance Ohmic contact to n-InP", *Journal of Vacuum Science and Technology*, B2(4), pp. 620-625, Oct.-Dec. 1984

[13] Y. Dong, "Fabrication Processes and Epitaxial Growth Technologies for Base-Collector Parasitics Reduction in Indium Phosphide HBT", *Ph. D thesis, University of California, Santa Barbara* Jun. 2004

[14] Y. G. Shen, Y. W. Mai, Q. C. Chang, D. R. McKenzie, W. D. McFall and W. E. McBride, "Residual stress, microstructure, and structure of tungsten thin films deposited by magnetron sputtering", *Journal of Applied Physics*, Vol. 87(1), pp. 177-187, Jan. 2000

[15] S. Abe, T. Mimura, N. Yokoyama, H. Ishikawa, "New Technology Towards GaAs LSI/VLSI for Computer Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 30, No. 7, Jul. 1982

[16] M. Dahlström, X.-M. Fang, D. Lubyshev, M. Urteaga, S. Krishnan, N. Parthasarathy, Y. M. Kim, Y. Wu, J. M. Fastenau, W. K. Liu and M. J. W. Rodwell, "Wideband DHBTs Using a Graded Carbon-Doped InGaAs Base", *IEEE Electron Device Letters*, Vol. 24, pp. 433-435, Jul. 2003

[17] Z. Griffith, M. Dahlström, M. J. W. Rodwell, X.-M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and W. K. Lui, "InGaAs/InP DHBTs for Increased Digital IC Bandwidth having a 391 GHz f_τ and 505 GHz f_{max}", *IEEE Electron Device Letters*, vol. 26, no. 1, pp. 11-13, 2005.

[18] Z. Griffith, M. Dahlström, M. J. W. Rodwell, X.-M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and W. K. Lui, "In$_{0.53}$Ga$_{0.47}$As/InP Type-I DHBTs w/ 100 nm Collector and 491 GHz f_τ, 415 GHz f_{max}", *IEEE International Conference on Indium Phosphide and Related Materials*, Glasgow, Scotland, 8-13 May, 2005.

[19] H. Kroemer, "Quantum Mechanics", *Prentice Hall*, New Jersey, 1994

[20] M. Kahn, S . Blayac, M. Riet, Ph. Berdaguer, V. Dhalluin, F. Alexandre, F. Aniel and J. Godin, " Effect of Base Thickness Reduction on High Speed Characteristics and Base Resistance of InGaAs/InP Heterojunction Bipolar Transistor" *IEEE International Conference on Indium Phosphide and Related Materials*, Santa Barbara, CA, May 2003

[21] W. Liu, H-F. Chau and E. Beam, "Thermal Properties and Thermal Instabilities of InP based Heterojunction Bipolar Transistors", *IEEE Transactions on Electron Devices*, vol. 43, No. 3, pp. 388-395, Mar. 1996.

[22] H. Ishikawa, S. Miwa, T. Maruyama and M. Kamada, "Origin of n-type conduction at the the interface between epitaxial-grown layer and InP substrate and its suppression by heating in phosphine atmosphere", *Journal of Applied Physics*, Vol. 71(8) , pp. 3898-3903, Apr. 1992

[23] M. Hollfelder, H. Hardtdegen, U. Breuer, H. Holzbrecher, R. Carius and H. Lth, "Unintentional impurity incorporation at the interface between InP substrate and buffer layer grown by LP-MOVPE", *Proc. of the 7th International Conference on Indium Phosphide and Related Materials*, Sapporo, Japan, 1995

[24] Y. Dong, Y. Wei, Z. Griffith, M. Urteaga, M. Dolstrom, A. Gossard, and M. Rodwell, "InP Heterojunction Bipolar Transistor with Selectively Implanted Collector", *2003 International Semiconductor Device Research Symposium*, Washington DC, 2003.

[25] Y. Dong, Z. Griffith, M. Dahlström, and M.J.W. Rodwell, "C_{cb} reduction in InP heterojunction bipolar transistors with selectively implanted collector pedestal", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 67-68.

[26] H. K. Gummel, "On the definition of cut off frequency f_τ", Proceedings . of the IEEE, Vol. 57, pp. 2159, 1969

5

Implanted pedestal-subcollector DHBT

IN Chapter 4 , a technology is developed to eliminate the capacitance associated with the base access pad. However, lateral scaling of the collector base junction has not been achieved. In narrow mesa DHBTs shown in Fig. **??** in Chapter 2 ,

$$C_{cb} \propto \frac{W_{cb}}{W_{eb}} \qquad (5.0.1)$$

$$R_{bb} \propto coth\frac{W_{eb}}{L_T} \qquad (5.0.2)$$

where L_T is the ohmic transfer length limited by the ohmic contact to p^{++} $In_{0.53}Ga_{0.47}As$. Therefore any lateral scaling of the collector base area will result in a large increase in base resistance and this is the single biggest challenge facing InP mesa DHBTs today [1]. Furthermore, narrow base ohmic present a large access resistance and are difficult to form. As described in Chapter 2 , independent definition of the collector base junction becomes more important as HBTs are scaled. In this chapter, a novel idea is proposed and developed wherein implantation alone is used to independently scale the collector-base capacitance.

5.1   Various approaches to collector scaling

As described in Chapter 2 C_{cb} scaling becomes important for future 250 nm HBTs. From Fig. **??** and Table 2.2, there is a large increase in f_{max}, f_τ and digital logic speed when the collectors are scaled.

The transferred substrate HBT in Fig. 5.1a dramatically scales the collector base capacitance. After base metal deposition, the wafer is planarized with BCB and then bonded to a carrier substrate. The wafer is then flipped over and the InP substrate is removed. A Schottky collector contact is then formed. Thus, the collector metal defines the base collector junction. This process has yielded devices with f_{max} of over a THz [2]. However, device yield was low due to the extreme complexity of the process which makes it unsuitable for even medium scale ICs.

A popular approach is to greatly undercut the collector as shown in Fig. 5.1b. This cantilever like structure [4], is also susceptible to failures and is not used for high yield ICs.

A variant to the transferred substrate process is the buried electrode process[3] in Fig. 5.1c, where a W electrode defines the collector contact. The active devices are grown over this, so that the W contact defines the base collector junction. This, requires growth over the W metal which is complicated.
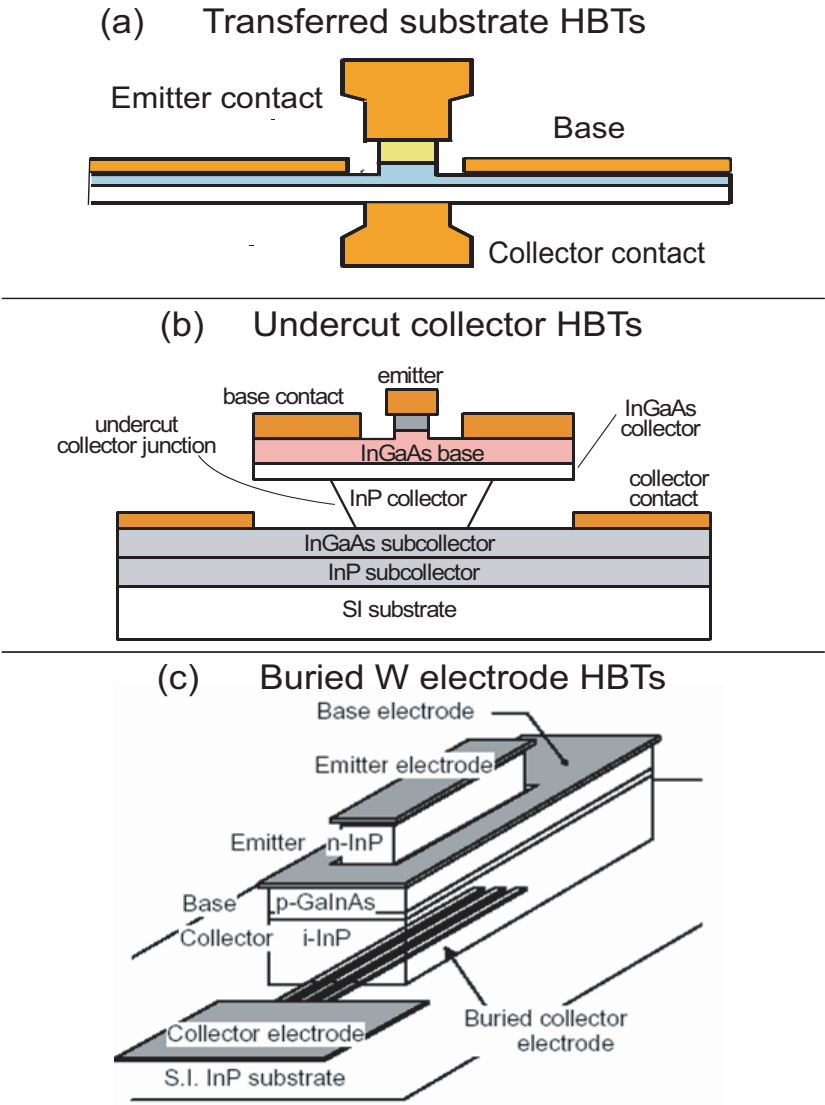
(a)   Transferred substrate HBTs

Emitter contact

Base

Collector contact

(b)   Undercut collector HBTs

emitter

base contact

InGaAs collector

undercut collector junction

InGaAs base

collector contact

InP collector

InGaAs subcollector

InP subcollector

SI substrate

(c)   Buried W electrode HBTs

Base electrode

Emitter electrode

Emitter   n-InP

Base   p-GaInAs

Collector   i-InP

Buried collector electrode

Collector electrode

S.I. InP substrate

Figure 5.1: Various approaches to collector scaling

The narrow mesa HBTs manufactured today suffer from scaling challenges as described in Chapter 2 . Ion implantation offers the possibility of selectively defining junctions while maintaining a planar process and is exploited in modern SiGe HBTs [5]. One such process for collector scaling in InP HBTs, is the regrown collector pedestal process [6] whose device structure is shown in Fig. 5.2. The process starts with a template consisting of 200nm Undoped InP over 300 nm N^{++} InP sub-collector. Si is selectively implanted to form an N^+ pedestal as shown in the figure. The drift collector, base, emitter layers are regrown and the device is formed. Thus, the intrinsic portion of the device over the collector has a collector depletion thickness defined by the thickness of the collector. In the extrinsic region, the depletion thickness is larger due to the undoped InP layer. Thus, the extrinsic capacitance is reduced, compared to mesa DHBT. The capacitances can be written as,

$$C_{cb,int} \propto \frac{W_p}{T_c} \tag{5.1.0}$$

$$C_{cb,ext} \propto \frac{W_{bc} - W_p}{T_c + T_p} \tag{5.1.0}$$

The regrown pedestal HBTs offer an alternative to the above complicated structures for collector scaling. However they [6] have the following drawbacks,

- DHBTs reported in [6] suffer from a process-dependent charge at the regrowth interface. A p^{++} InGaAs compensation layer is proposed as a solution but as seen in Chapter **??** , this is not repeatable

- Two MBE growths are required, the first forming the sub-collector and pedestal, and the second forming the active HBT layers

- The pedestal doping must be kept in the low 1×10^{18} cm^{-3} range to minimize broadening of the pedestal through lateral straggle of the Si implant. This increases the access resistance in the pedestal and adds to the collector resistance

- These pedestal HBTs reduce, but do not eliminate the extrinsic base pad capacitance

- The collector contacts are offset from the collector by another 200 nm due to the undoped InP layer. This worsens the planarity compared to a regular mesa DHBT

An alternative idea is developed that addresses each of the above issues. This process provides an Fe implanted extrinsic semi-insulating layer for increased depletion depth in the extrinsic collector-base junction, a patterned buried subcollector

formed by a deep Si implant and a collector pedestal created by a second Si implant. In addition to the reduced extrinsic C_{cb}, and compensation of charge at the epitaxial growth interface, this provides the following enhancements: elimination of $C_{cb,pad}$, a single MBE growth, possibility of higher doping in the N^+ pedestal, increased wafer planarity and hence potentially improved yield in the fabrication of large circuits.
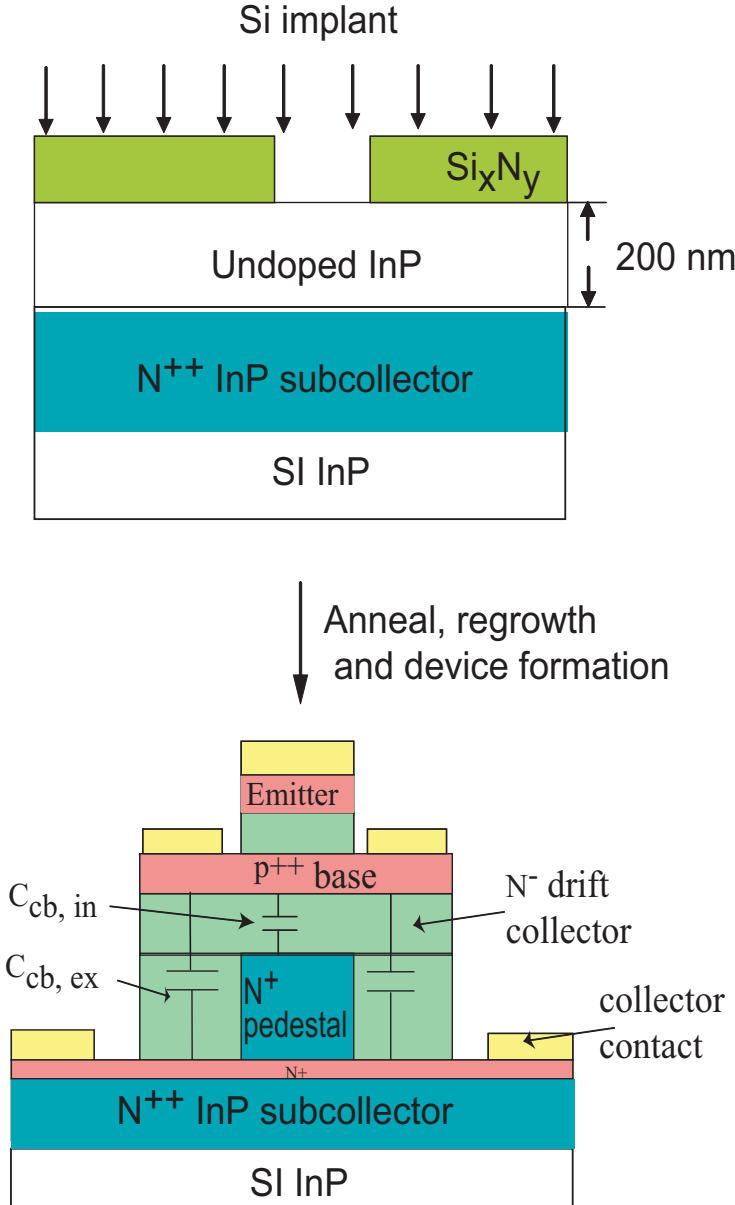
Figure 5.2: Pedestal HBT

5.2 Design of fully implanted pedestal-subcollector process

The process flow of the basic, implanted subcollector HBT is shown in Fig. 5.3. As before, alignment targets for stepper based lithography are defined on SI InP. The substrate is then implanted with Fe to a depth of $\sim$0.2 μm at a doping of $\sim 1 \times 10^{19}$ (cm^{-3} Fig. 5.3a). The damage due to the implant is annealed out and the sample is then selectively implanted, as in Fig. 5.3b, with Si at a very high energy (350 keV) so that the peak(at $\sim$ 0.5 μm) lies well below the Fe implant peak. This forms a buried N^{++} subcollector. An N^{++} pedestal linking to the buried subcollector is then formed by a second patterned selective Si implant. Raised N^{++} pedestals for the collector contacts are simultaneously realized (Fig. 5.3c). The sample is then annealed at 800 °C to activate the Si dopants. As before, the active InP DHBT layers, the N^- drift collector, base, and emitter layers are grown by MBE. Devices are formed by wet-etching the emitter and base mesas. HBT isolation does not require a subcollector mesa etch decreasing the total HBT mesa height by 500 nm. There are several advantages,

- The Fe implant forms a SI layer, equivalent to the undoped InP layer in the regrown pedestal HBT, over the N^{++} subcollector. The N^{++} subcollector is also formed by ion implantation. Thus this fully implanted pedestal-subcollector process requires no additional regrowth.

- The Fe implant automatically compensates the interface charge over a very wide range of charge densities

- The buried subcollector does not extend beyond the length of the emitter, similar to the implanted subcollector DHBTs with Fe. Thus the capacitance due to the base access pad is eliminated.

- The high Fe doping in the SI layer $\sim$ 5-8 $\times 10^{18}$ means that a high concentration of Si in the pedestal is permissible, since the straggle is now defined by the lateral distance at which the pedestal doping falls below the background Fe in the SI region.

- Raised N^{++} pedestals are simultaneously realized for collector contacts. Device isolation etch is not required due to the buried, isolated N^{++} subcollector. Thus the device planarity is better than a triple mesa DHBT by $\sim$ 500 nm

- It is very modular and can be inserted into any modern InP mesa HBT process.
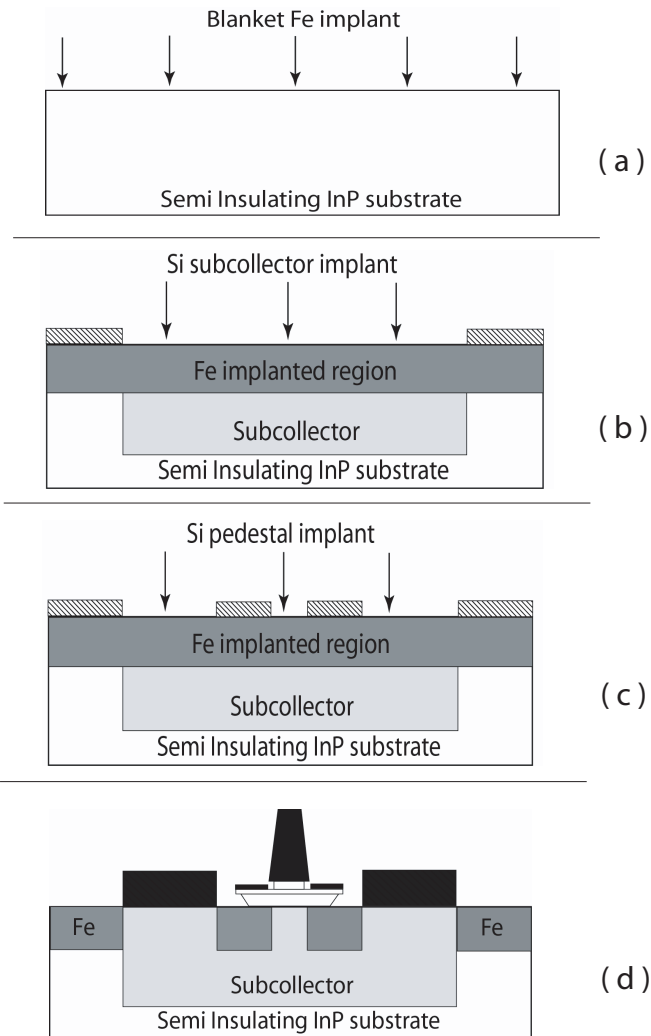
Figure 5.3: Implanted pedestal-subcollector DHBT process

Thus the fully implanted process, is an alternative to the regrown pedestal HBT and provides several enhancements. The various challenges of the implanted pedestal-subcollector process are,

- Low sheet resistance subcollector

- Formation of thick SI Fe implanted region

- Formation of N^{++} pedestals with low resistivity and low lateral straggle

- crystalline, defect free semiconductor before growth

- excellent surface morphology, comparable to InP substrate, prior to growth

- defect free MBE growth $\Rightarrow$ DC characteristics similar to epitaxially grown HBTs

Each issue is addressed in the subsequent sections.

5.2.1   Formation of buried N^{++} subcollector

The Si implant forms the subcollector as in the implant subcollector process. However, unlike the implanted subcollector DHBT, the main idea behind the implanted pedestal-subcollector DHBT is a deep Fe implant since it is used to compensate $\approx$ the top 0.2 μm of the subcollector. As seen in Chapter 3 , it is not easy to compensate very high N^{++} doping levels. Therefore, the Si implants should be of very high energy so that the peak lies well below 0.2 μm. This ensures that the Gaussian distribution (of the implanted Si) tails to $\sim 5 \times 10^{18}$ cm^{-3}, doping level at which Fe is reported to successfully compensate the N^+ doping. The highest commercially available Si doping at 200 °C is 350 keV. Further, it is seen that increasing the thickness of the SI region, is not beneficial as might be expected. The lateral broadening due to implant straggle is, to first order, $\sim T_p$, the height of the N^+ pedestal. If T_p is increased, $C_{cb,ext}$ decreases due to larger extrinsic depletion depth, but $C_{cb,int}$ increases due to a wider effective N^+ pedestal. Thus the two effects offset each other and for the minimum, optically resolvable implant mask dimension at UCSB of ~ 0.5 μm, it is seen that C_{cb} decrease is not significant beyond T_p of 0.2 μm.

Fig. 5.4 shows the SIMS profile and the simulated TRIM distribution for the implant conditions in Table 5.1 where Si and Fe are co-implanted. There is no diffusion of the Fe and Si as implanted. However, the fluences were slightly off, due to the poor calibration of the implant system. (This is not an artifact due to charge-mass interference in SIMS since 29Si and 54Fe also yielded similar results).

Table 5.1: Implant conditions for implanted pedestal-subcollector HBT process

Implant species	Implant energy	Implant fluence	Offset angle	Implant temperature
Si	350 KeV	$5{\times}10^{14}$ ions/cm^2	7 $^\circ$	200 $^\circ$ C
Fe	150 KeV	$2.4{\times}10^{14}$ ions/cm^2	7 $^\circ$	200 $^\circ$ C
$I_{ions} \leq 50\mu$A				
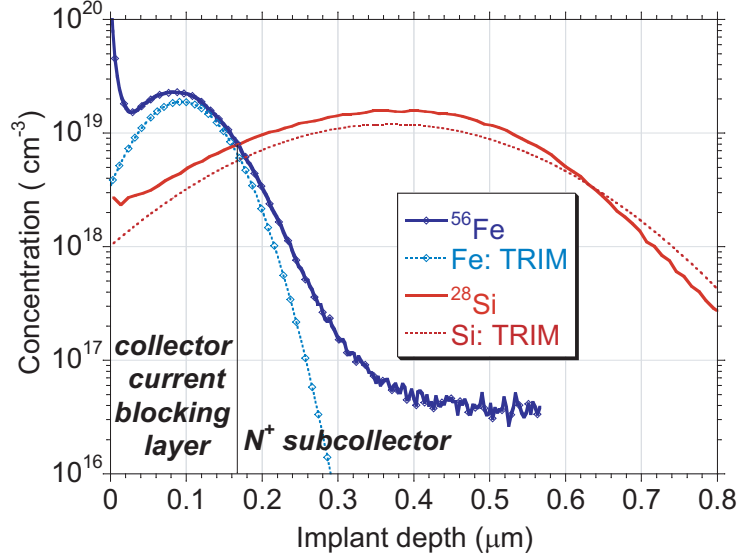
Figure 5.4: Distribution of Fe and Si from SIMS and simulated by TRIM

The shallow Fe implant in Chapter 4 is annealed at 700 °C for 5 min. The same anneal conditions for Fe are employed here. This shown in §5.2.2 to anneal the implant damage and activate the dopants. Fig. 5.5 shows the profile after such an anneal. There is significant depletion of Fe atoms and a peak of Fe is formed at $\sim$ 0.14 μm which is $R_p + \Delta R_p$. This is well observed in literature and is described in Chapter 3 . As seen from the plots, the Fe concentration falls below the Si concentration at a depth of $\sim$ 0.16 μm. Assuming 100% activation of Si and Fe, $T_p \sim 0.16$ μm. While $T_p = 0.2$ μm is desirable, these were nevertheless chosen for the first generation implanted pedestal-subcollector HBTs.

For these implant conditions, the sheet resistance is determined from Hall measurements and is shown in Table 5.2. The negative Hall voltage indicates that the

Table 5.2: Hall measurements of resistivity and mobility for deep Si and Fe implant

Anneal temperature (°C)	Anneal time (s)	Hall mobility ($cm^2/V \cdot s$)	Carrier density (cm^{-2})	Sheet resistance ($\Omega/\square$)
700	300	-1194	-2.0×10^{14}	25.8
700	600	-1224	-1.9×10^{14}	26.2
725	600	-1189	-2.0×10^{14}	25.7
750	300	-1236	-2.1×10^{14}	24.5

carriers are electrons. The sheet resistance is nearly the same for all the various an-
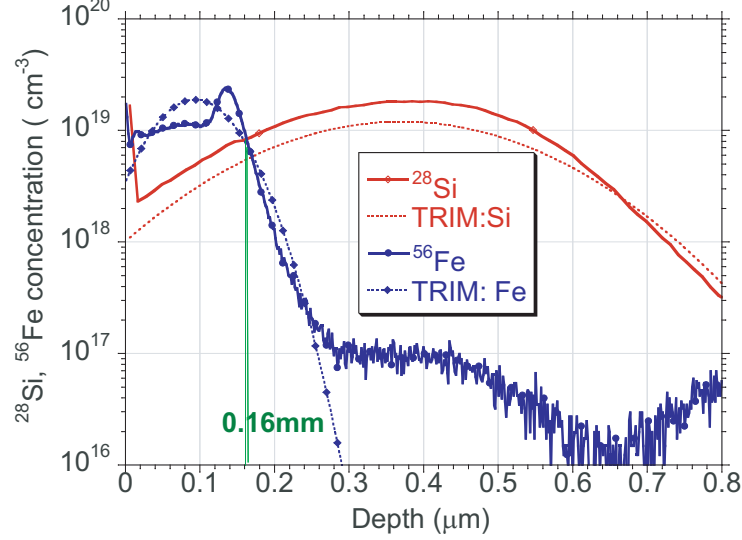
Figure 5.5: Distribution of Fe and Si after anneal

---

neals. However, 700 °C for 5 min gave rise to minimum defects due to the anneal. From the above data and measured concentration profiles, the activation of Fe and Si can be calculated. Assuming that the active Fe compensates Si upto 1632 Å, and integrating the Si concentration from this point, n_{Si}= 6.5 $\times 10^{14}$ cm^{-2}. From Hall measurements, $n_{Si,eff}$= 2.5 $\times 10^{14}$ cm^{-2}. Therefore activation of Si is $\sim$ 39 %. The active Si concentration at 1632 Å is therefore 3.8$\times 10^{14}$ cm^{-3}. Since one Fe atom compensates one Si atom, minimum activation of Fe is $N_{Fe}/N_{activeSi}$ at 1632 Å = 41 %.

5.2.2 Crystallinity

It is seen from Chapter 3 that 56Fe causes significant lattice damage. The crystallinity is evaluated from Ion channeling(RBS) measurements. The defects are quantified in terms of displaced In atoms. If displaced In fraction is 1, it is completely amorphous and if it is $\leq$ 0.02, it is crystalline. Sample is completely amorphous in the top 1500-2000 Å suggesting that Fe is creating most of the damage and that defects due to Si is much smaller. The In concentration in InP is 5.3$\times 10^{22}$ atoms-cm^{-3} and from the displaced In fraction in Fig. 5.7, the total number of In atoms displaced can be determined. From the discussion on Fe implants in Chapter 3 , it is seen that prolonged anneals at temperatures of $\sim$ 700 - 750 °C are required for damage removal and activation. Anneals at over 725 °C for prolonged periods
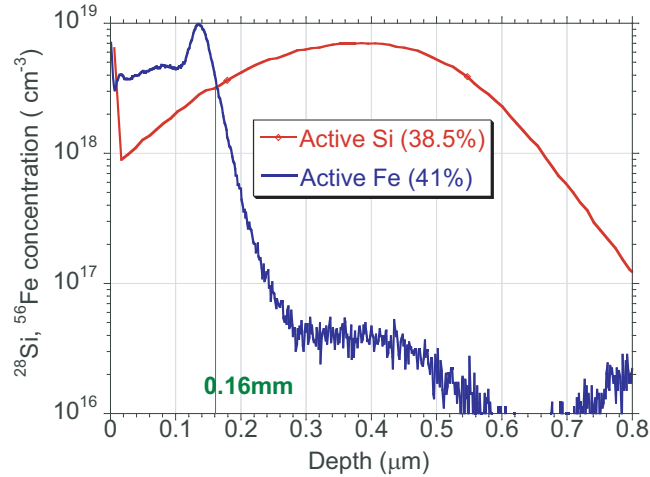
Figure 5.6: Distribution of Active Fe and Si calculated from Hall and SIMS

gave rise to several In rich zones due to failure of the Si_xN_y cap. The samples are annealed at 700 °C for 5 min. and the crystallinity is checked using RBS. As seen in Fig. 5.8 and Fig. 5.9, samples implanted with lower doses ($\leq 2.4 \times 10^{14}$ ions/cm^2) of Iron are completely recovered. There is surface damage where the implant fluence of Iron is higher (1×10^{15} ions/cm^2). The uncertainty for *In* defect measurement is 1 to 2 %.
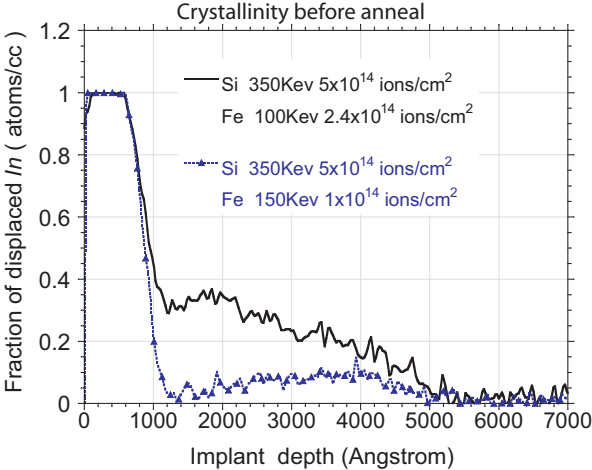
Figure 5.7: Crystallinity with co-implants of Si and Fe before any anneal
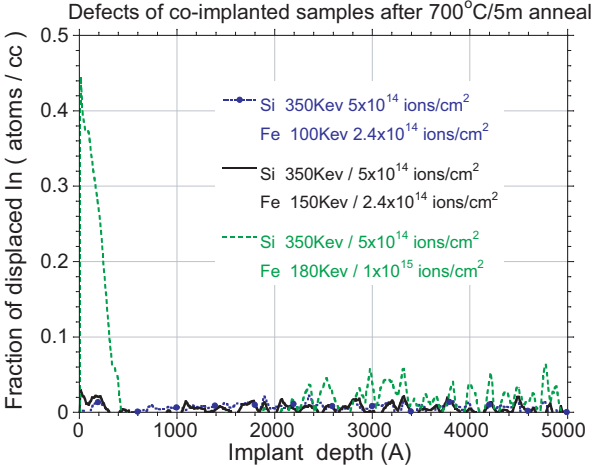
Figure 5.8: Crystallinity of Si and Fe co-implanted InP annealed at 700 °C/5 min
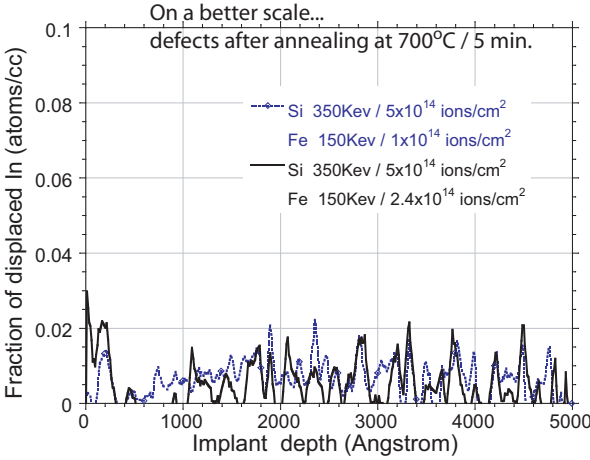
Figure 5.9: ...A more convincing scale

5.2.3 Surface morphology

Fig. 5.10 show the surface scans for various conditions. As implanted with Si and Fe, the surface is quite rough, ~ 18 nm. When annealed at 800 °C for 10 sec. the surface roughness reduces to ~ 12 nm. As seen from the previous section and from §3.1.3 in Chapter 3 , heavy acceptor elements in InP generally require prolonged anneals at temperatures over 650 °C. AFM scans of this co-implanted substrate, annealed at 700 °C for 5 min. indicates that the surface quality is comparable to virgin SI InP in Fig. **??** in Chapter 3 . This further validates the use of these annealing conditions for Fe implant.

5.2.4 The Fe implanted extrinsic layer

The Fe layer serves to increase the depletion depth in the extrinsic portion of the device under the base contact. Co-implantation of Si and Fe causes a difference in activation as opposed to the case when

- Fe is implanted first and annealed

- Si is then implanted and annealed

When Fe is implanted first and activated they have occupy *In* sites. The Si therefore has less sites to occupy.
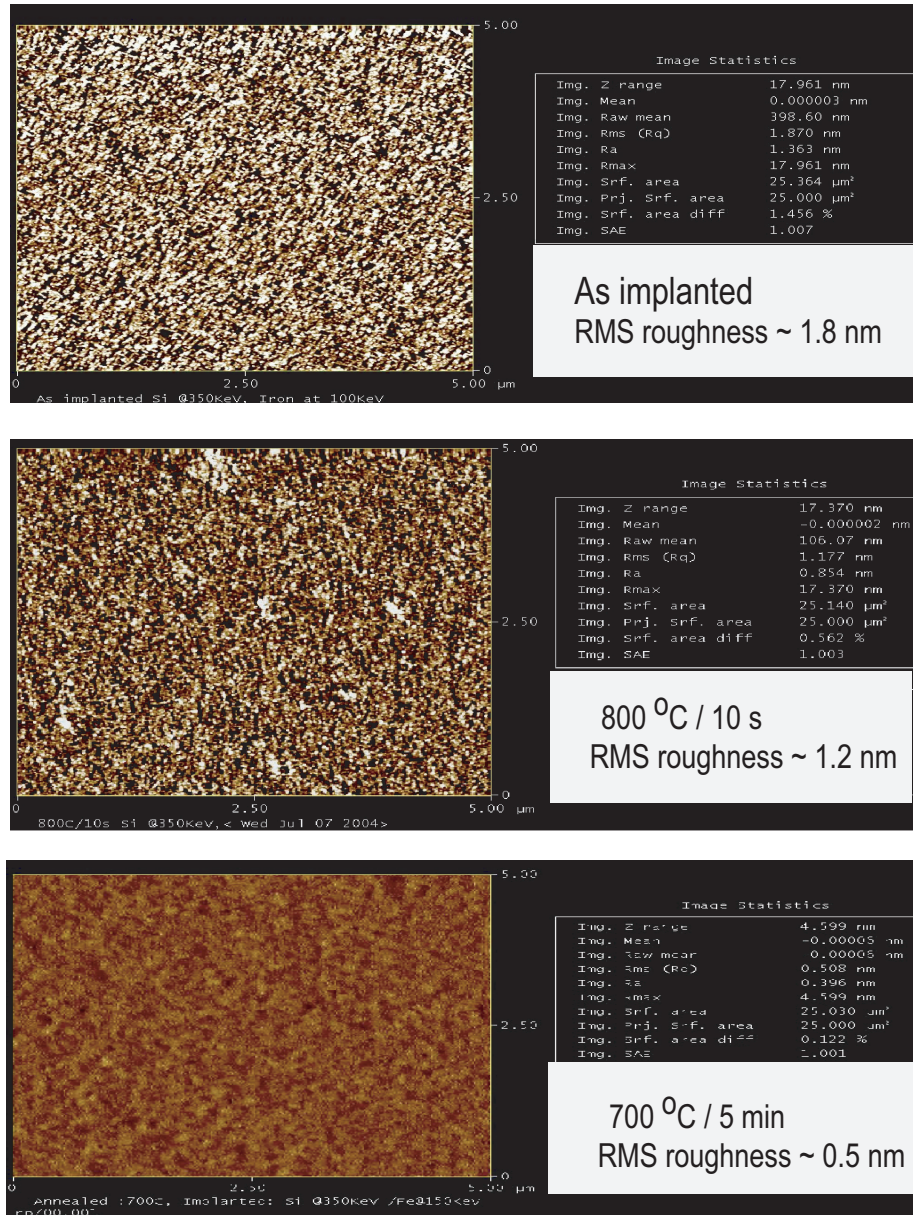
Figure 5.10: Surface scans of the Si and Fe co-implanted substrate

The current flow mechanism of an N^{++}-SI-N^{++} and p^{++}- SI - N^{++} layer stacks respectively is developed in [7]. The main purpose of the SI region is to decrease the capacitance in the extrinsic region by increasing the distance between the two charge dipoles in the base and subcollector. C-V measurements are used to check the presence of an active SI layer and if present, the thickness of this region. For this purpose, Schottky diodes are formed. The samples are non-selectively implanted first with Fe at the implant conditions , annealed at 700 °C for 5 min. They are then non-selectively implanted with Si and annealed at 800 °C for 30 sec. The implant conditions are the same as in in §5.2.1. Schottky contacts are placed on the top SI layer, while ohmic contacts are placed on the N^{++} subcollector. Fig. 5.12 shows the schematic of such a structure.
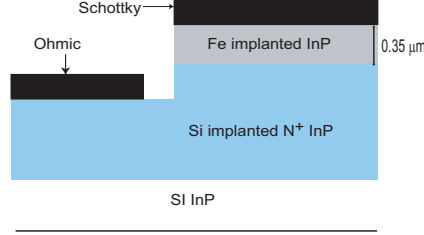
Figure 5.11: Sckottky diodes on Fe and Si implanted substrate

The contacts placed on the N^{++} regions are verified to be ohmic by checking the I-V characteristics (Fig. 5.13). Similarly the contacts on the top surface, implanted with Fe are verified to be Schottky by measuring the I-V characteristics of this SI-N^{++} diode. Fig. 5.14 also shows the Schottky diode characteristics of such a structure on a fully epitaxial structure (0.2 μm UID /0.3 μm N^{++} InP), which is the starting template in a regrown pedestal HBT process. The forward characteristics of the Schottky diode on the fully implanted structure indicates a very high *turn on* voltage. From the theory of transport in a SI region, the current increases sharply once the Trap Filled Voltage Limit is reached. FromFig. 5.14, V$_{TFL}$ is $\sim$ 2 V. In the case of a Schottky diode on the epitaxial template, the theory of transport is similar to a forward biased Schottky junction and the current sharply increases at $\sim$ 0.3 V. In the reverse bias case, te situation is quite different. The depletion region thickness at zero bias for the Schottky diodes on 0.2 μm UID /0.3 μm N^{++} InP is $\approx$ thickness of the UID region = 0.2 μm. The reverse diode current characteristics are dominated by the thermal generation in the intrinsic region. The breakdown is expected to be large in this case, due to the wideband gap of InP and the large depletion thickness. The thickness of the space charge region for the SI-N^{++} junction is calculated from the active Fe and Si doping profiles obtained in the previous case.

$$x_A = \sqrt{\frac{2\phi_{bi}}{qN_A}}$$

(5.2.0)

where, N_A is the active Fe concentration in the SI region, ϕ_{bi} is the built-in potential of the SI-N^{++} junction. Since E_{Fp} of the SI region $\sim E_A$ and E_{Fn} of N^{++} InP $\sim$ E$_c$, $\phi_{bi} \sim$ 0.7 eV. Assuming uniform $N_A \sim 1\times10^{18}$ cm^{-3} and $N_D \sim 1\times10^{19}$ cm^{-3}, x_A = 88 Å. Due to the small depletion region, the breakdown mechanism is possibly dominated by tunneling currents which could explain the dramatic increase in current at $\sim$ 1.5 V. The C-V characteristics in Fig. 5.15 of such the Schottky diodes indicate that there is a thick SI region. From the capacitance at zero bias,

the thickness of the SI region is deduced to be $\sim$ 177 nm. $x_{dep} \sim$ 200 nm for the Schottky diode on the epitaxial UID InP/ N^{++} InP, as expected since the thickness of the UID InP region as grown is 200 nm. The capacitance is fairly flat with voltage indicating that beyond the depletion thickness, the region is fairly N^{++}, such that the depletion region does not shift much with bias. Fig. 5.16 compares the C-V characteristics of two cases

- Fe is implanted and activated first followed by Si implant and activation

- Fe and Si are co-implanted and activated together

The depletion thickness is lower in the case when Si and Fe are co-implanted and activated together. This is possibly due to Si and Fe competing for the same In sites between 160 - 180 nm when Si and Fe concentrations are comparable, resulting in lower active Fe concentration, decreasing the thickness of the SI region.
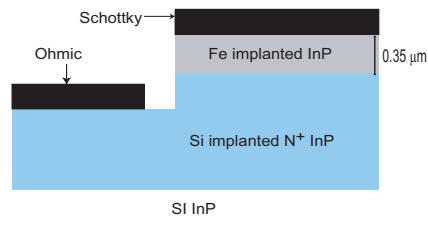
Figure 5.12: Sckottky diodes on Fe and Si implanted substrate
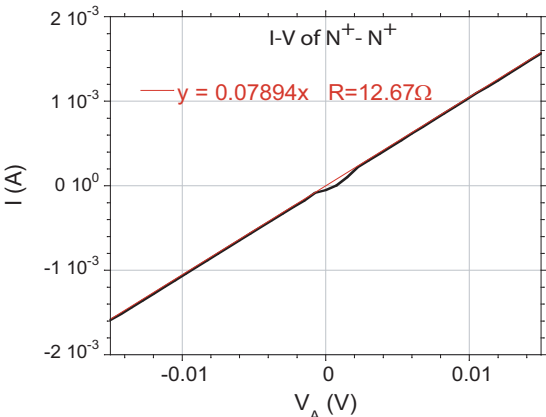
Figure 5.13: Ohmic transport between N^{++} pads
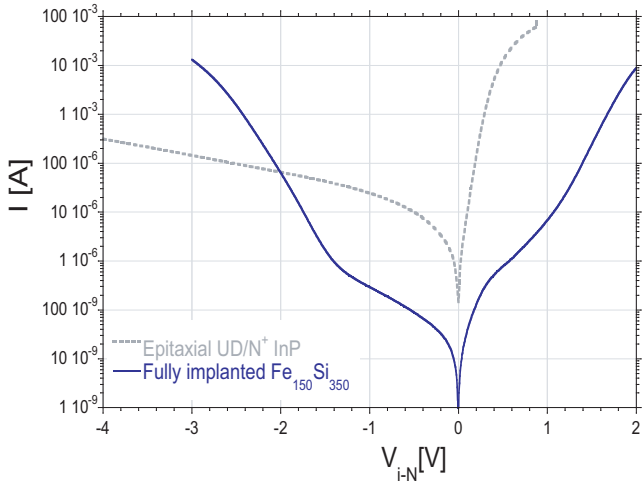
Figure 5.14: Sckottky diode characteristics of Fe and Si implanted substrate
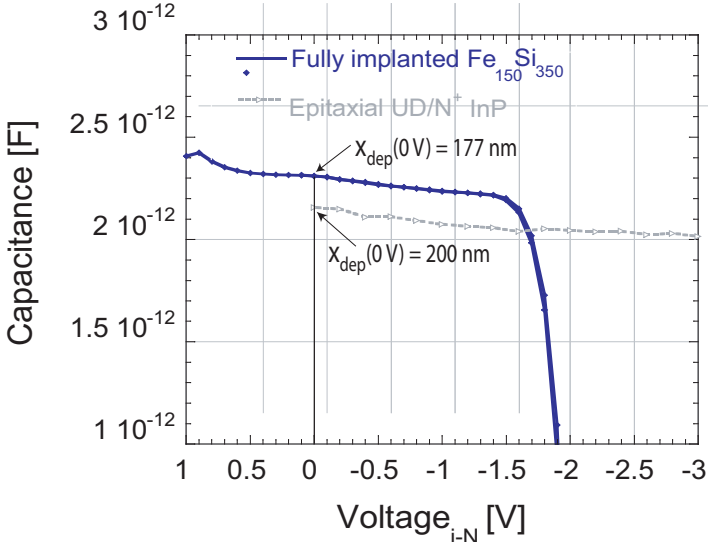
Figure 5.15: C-V of the Schottky diodes on Fe and Si implanted substrate, indicating the thickness of the SI depletion region
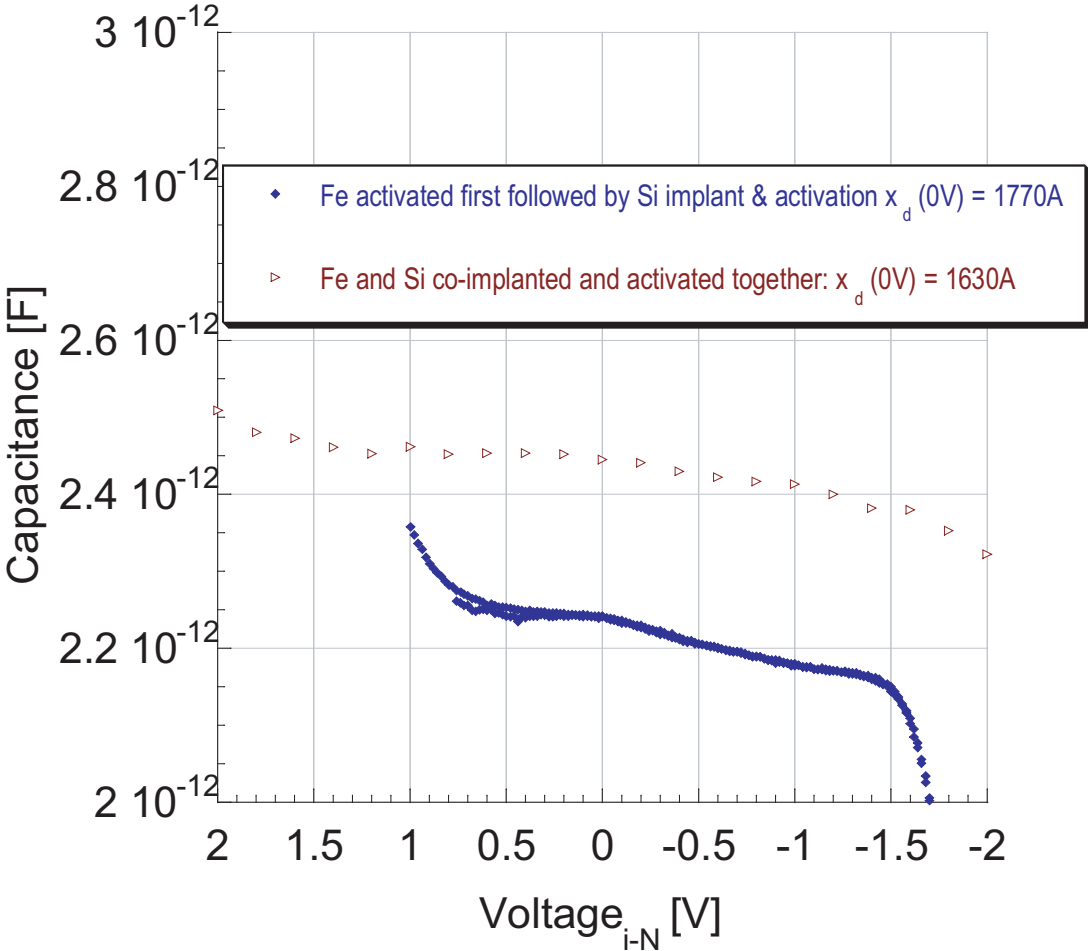
Figure 5.16: C-V of the Schottky diodes when Fe and Si are co-implanted and activated together, and when Fe is activated first followed by Si

Table 5.3: Implant conditions for formation of N^{++} pedestal

Implant species	Implant energy	Implant fluence	Offset angle	Implant temperature
Si	100 KeV	5×10^{14} ions/cm^2	$7\,^\circ$	$200\,^\circ$ C
	30 KeV	8×10^{13} ions/cm^2		
	10 KeV	4×10^{13} ions/cm^2		
$I_{ions} \leq 10\mu$A					

5.2.5 Formation of N^{++} pedestal

In §5.2.1, the active Fe and Si concentrations are computed. The pedestal doping needs to overwhelm the Fe concentration. Si is implanted at the conditions given in Table 5.3 in a substrate where Fe has been implanted and activated.

After annealing at 800 °C for 30 sec., Hall measurements indicate that the sheet resistance is ~38 $\Omega/\square$ and for $T_p \sim$ 180 nm, resistivity of the pedestal is $\sim$ 6.5 $\Omega \cdot \mu$m. When both the pedestal and subcollector are present, the sheet resistance of the combined stack is $\sim$ 17 $\Omega/\square$ and $n_{Si} = 4.7\times10^{14}$ cm^{-2} and the mobility is 800 $cm^2/V \cdot s$. Fig. 5.17 shows the concentration of Si and Fe after all three implants and anneals. With the chosen implant conditions, Si overwhelms the Fe peak.
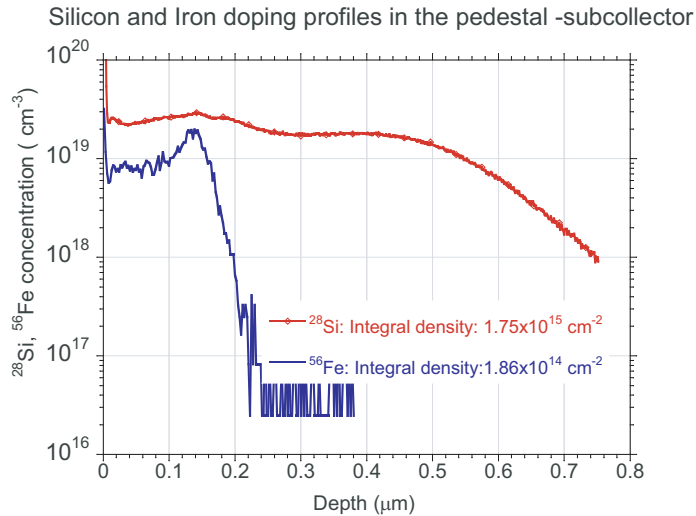
Figure 5.17: Concentration of Si and Fe after all three implants

It is seen that an anneal of 700 °C for 5 min. is required for Fe activation and damage removal. Good activation of Si is obtained only after annealing at 800 °C.
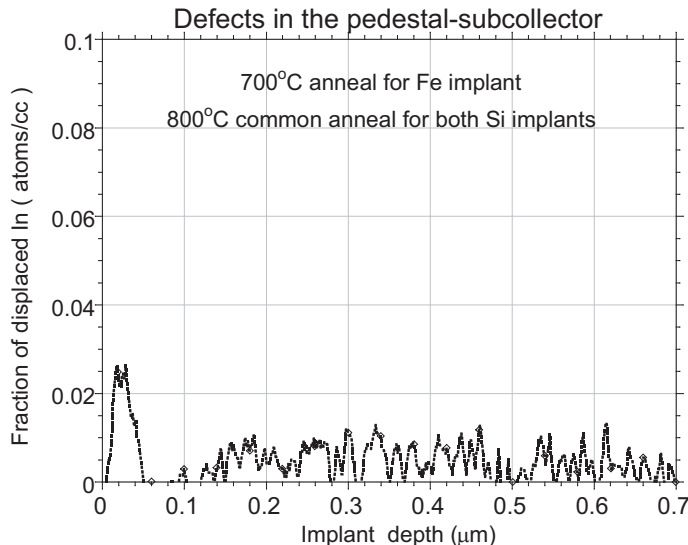
Figure 5.18: Crystallinity after all implants and dry etch

Since there are two Si implants, one for the subcollector and one for the pedestal, the question arises if two separate anneals are required to activate the Si dopants. It is seen that the TiW alignment marks does not hold up to two anneals at 800 °C. Fig. 5.18 shows the defect density after all three implants. The implant conditions for the Fe and Si subcollector implant are the same as in §5.2.1 and the above conditions are used for the Si pedestal implant. After the Fe implant, the sample is annealed at 700 °C for 5 min. Si is implanted for the subcollector and then the Si pedestal implant is carried out. Both the implants are annealed together at 800 °C for 30 sec. Fig. 5.18 shows that the defect density is within the noise of the measurements, indicating crystallinity of the InP substrate after 3 implants and 1 anneal for Fe and 1 common anneal for Si. Since these are identical implants, at different depths, a single anneal does not yield significantly different results for resistivities for the various layers. Fig. 5.18 shows the defect density after implants and also 3 dry etches; for the alignment targets, subcollector implant window, and pedestal implant window.

Lateral straggle due to the pedestal implant

As defined in Chapter 3 , the straggle is defined as the point when the active, lateral Si concentration falls below the background Fe doping. In the case of SI InP substrate, the active Fe doping is between 5×10^{16} cm^{-3} and 9×10^{16} cm^{-3}.

Therefore the lateral straggle is appreciable. The thick SI region over the N^{++} subcollector is formed by Fe implant, and has an active Fe concentration of 5×10^{18} cm^{-3}. Fig. **??** is a plot of the lateral straggle calculated from *TRIM*. The pedestal doping is seen from Fig. 5.17 to be $\sim 2 \times 10^{19}$ cm^{-3} and uniform Fe doping of 5×10^{18} cm^{-3} is assumed. The lateral spread is ~ 0.12 μm when the Si concentration falls below the active Fe doping assumed to be $\sim 5 \times 10^{18}$ cm^{-3}. This is not an exact solution since the Fe doping itself varies with distance. The exact calculation can be performed; however, *TRIM* profile of Fe implant has to be relied upon. From §5.2.1, the *TRIM* calculation is not representative of the Fe profile due to the diffusion of Fe during anneal. For this calculation the *TRIM* profile of Fe is assumed, with 40% activation of these Fe acceptors. In this case, the lateral straggle can be calculated as the lateral distance(z) at which

$$n_{Si}(x, z) exp(-z^2/2\pi\Delta R_z^2) = n_{Fe}(x, z) \qquad (5.2.0)$$

where ΔR_z is the lateral spread of the 100 KeV Si implant calculated from *TRIM* to be 577 Å. The lower energy implants are assumed to contribute insignificantly to this straggle. Fig. 5.20 shows the lateral straggle distance z which is ~ 0.25 μm.
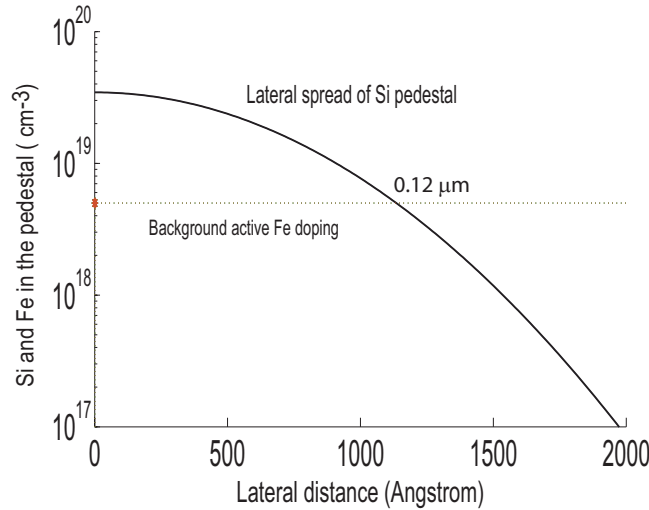
Figure 5.19: Lateral spread in the pedestal due to implant, assuming 2×10^{19}cm^{-3} doping at the mask edge. The lateral straggle is defined as the point when the Si concentration falls below the active Fe doping $\sim 5 \times 10^{18}$

The resistive straggle can be measured using special *dog-bone* TLM structures shown in Fig. 5.21. The spacing between the ohmic regions and the width of the
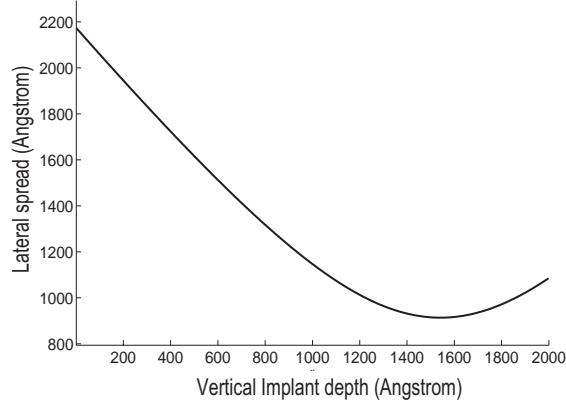
Figure 5.20: Lateral spread in the pedestal due to 100 KeV Si implant. The lateral straggle is defined as the point when the Si concentration falls the active Fe doping calculated from *TRIM* with Fe activation assumed to be 40 %

TLMs are varied. The width of the TLM should be comparable to the straggle, which renders standard TLMs for measuring contact and sheet resistivities useless for this purpose. The wafer is first implanted with Fe and annealed and then the pedestal Si implant is carried out selectively in the shaded regions shown in Fig. 5.21. Standard TLMs can measure, the sheet resistance and contact resistivity. The measured resistance for each TLM (of widths w_1, w_2 ...) is plotted vs. the TLM spacing x and the slope $m_s tr$ is calculated. The lateral resistive straggle is then calculated as follows

$$R_{sh} = m_{str} \cdot (w + \Delta w) \tag{5.2.0}$$

where w is the width of the TLM. Plotting $\frac{R_{sh}}{m_{str}}$ vs. the variation in TLM width as drawn on the mask w, Δw can be obtained. This is the lateral resistive straggle shown in Fig. 5.22. Note, the resistive lateral straggle also includes the effects of widening of the Si_xN_y implant mask during processing. Fig. 5.22 shows the resistive straggle of the Si pedestal implanted in an already Fe implanted substrate. The resistive straggle, $\Delta w \sim 0.1$ μm, which means that the implant widens by 50 nm on either side of the implant mask. However, it should be pointed out that resistive straggle is a pessimistic calculation and the capacitive straggle is more relevant. When the doping falls from 1×10^{19} at the implant mask edge to say, 5×10^{18} cm^{-3} at some distance Δw_R, the resistance increases ten-fold. The overall resistance is thus determined by the region of high doping. A 1×10^{19} cm^{-3} is much larger than the doping in the drift collector. The capacitive straggle should be defined as the

point when the doping falls to 10% of the collector doping or the point at which lateral Si concentration falls below the active Fe doping, whichever is lower.
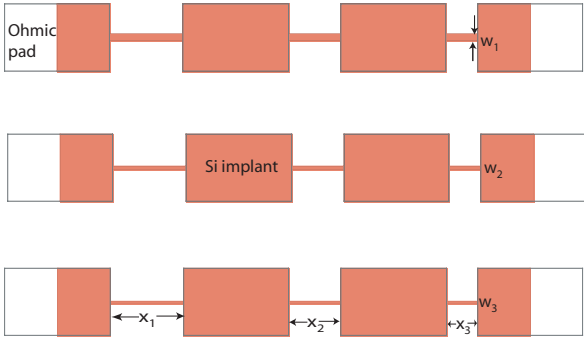
Figure 5.21: Straggle TLMs with varying spacing x, and width w– the shaded regions are implanted with Si, and ohmic contacts are formed over these
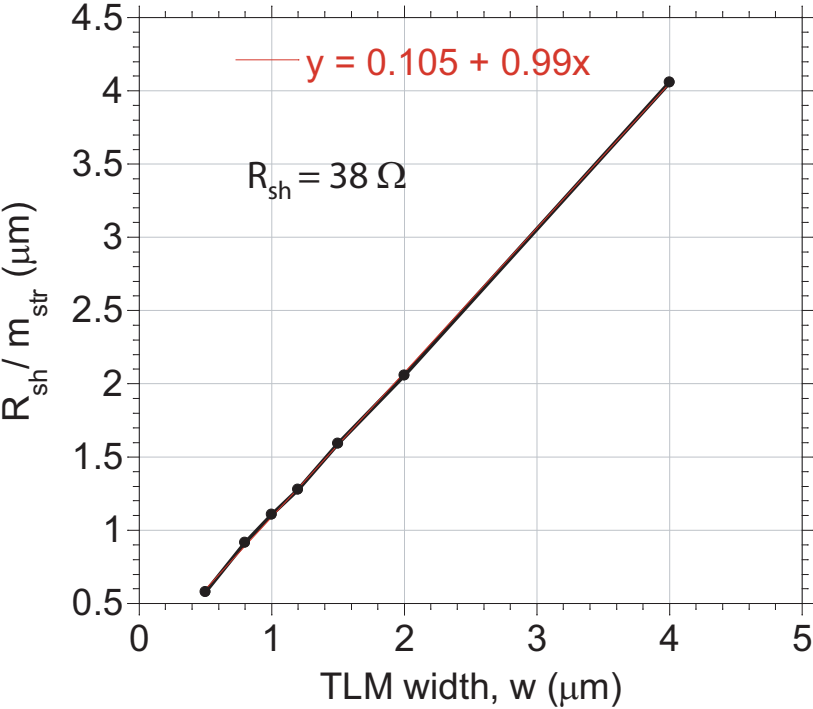
Figure 5.22: Resistive straggle of Si pedestal implant in Fe activated layer

Table 5.4: Contact and sheet resistivities

	Sheet resistance $\Omega/\square$	Contact resistivity $\Omega \cdot \mu m^2$	Horizontal resistance $\Omega \cdot \mu m$
Emitter	28	< 1	3
Base	1300	< 3	< 50
Collector	24-26	3000	350
Pd/Ti/Pd/Au contacts for all layers			

5.3 Large area device results

The RBS data in Fig. 5.18 is encouraging proof that good quality crystalline growth is feasible on this triple implanted substrate. Similar to the growth for implanted subcollector DHBTs, the drift collector, base and emitter are grown with the same layer structure as in Table 4.5. There is no pedestal layer, therefore this large area device is representative of the transistor in the extrinsic region under the base ohmic. The collector contact is formed by etching down $\sim 0.3\ \mu$m to place the contact pads on N^{++} Si implanted subcollector. The sheet resistance of the collector, base and emitter of these devices in Table 5.4 are very similar to fully epitaxial layers grown at UCSB. Also excellent growth morphology is observed (not shown). The large area DC results are shown in Fig. 5.23. These indicate that there is no gain in this transistor due to current blocking by the SI region below the drift collector. Only at very high collector base biases, does current start to flow as also evident from the diode leakage in Fig. 5.24. The Gummels in Fig. 5.23a show that there is no current gain when V_{cb} =0V and is $\sim$ 1 when V_{cb} =1V. The CV measurements in Fig. 5.25 indicate that the capacitance at zero bias is 0.5 $fF/\mu m^2$. The capacitance of a fully epitaxial HBT with identical layer structure but epitaxially grown 300 nm N^{++} subcollector is also shown and is $\sim$ 1.1 $fF/\mu m^2$. Thus there is a 55% decrease in capacitance due to the SI region at zero bias. This corresponds to a depletion thickness of 220 nm, or a thickness of the SI region of $\sim$ 120 nm. The capacitance measurements beyond 0.5 V for the DHBT grown on the Fe and Si implanted substrate were clouded by high parallel conductance and is not shown. The offset voltage is higher since higher V_{cb} is required to remove the current blocking due to Fe. The high knee voltage is due to the large resistance in the SI Fe implanted region. From Fig. 5.26, the V_{cb} is over 1V only when V_{cb} is over 2V. A large V_{cb} is needed for the base collector junction of this device to be not forward biased. This explains the large offset and knee voltages
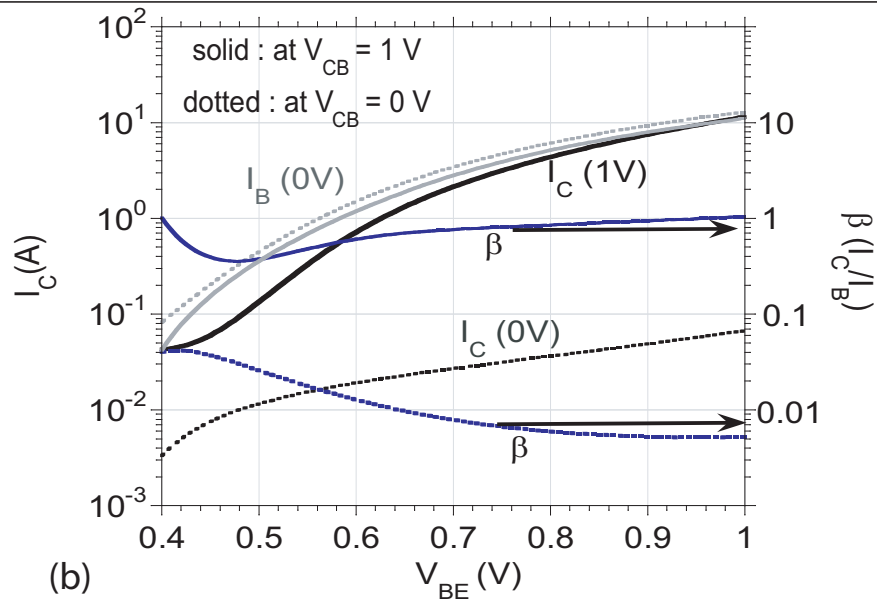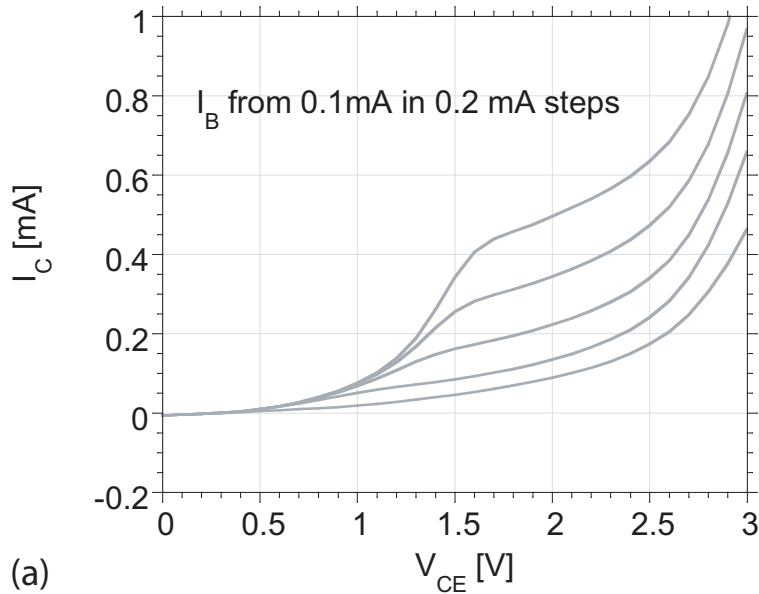
Figure 5.23: DC measurements of large area devices on Si and Fe implanted substrate – representative of extrinsic DHBT
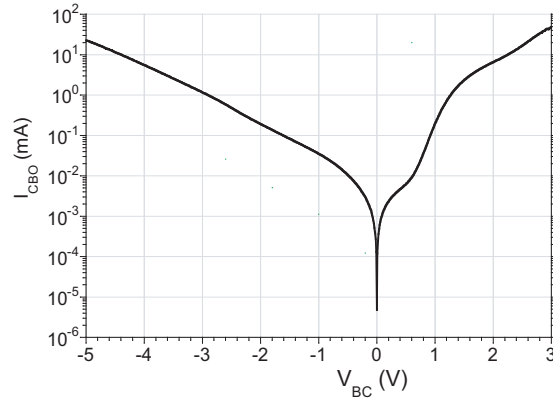
Figure 5.24: I_{CBO} of large area devices on Si and Fe implanted substrate – representative of extrinsic DHBT
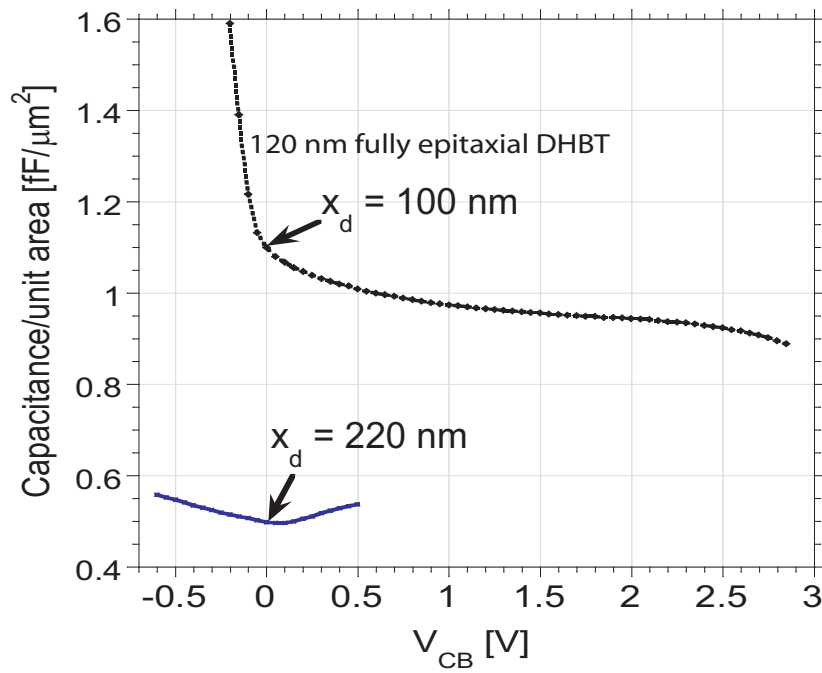
Figure 5.25: C-V measurements of large area devices on Si and Fe implanted substrate, showing a 55 % decrease in extrinsic capacitance compared to a standard epitaxial DHBT

160
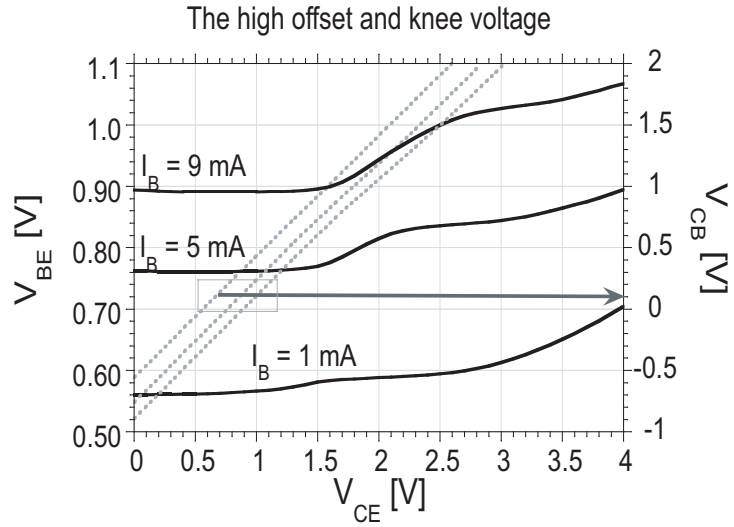
Figure 5.26: V_{be} and V_{cb} in the output characteristics
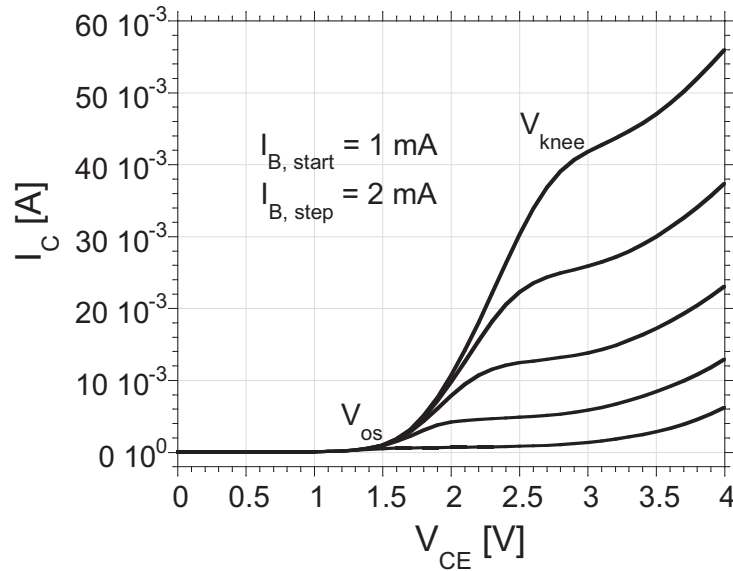
Figure 5.27: High V_os and high V_knee in the output characteristics

5.4 Device results - Implanted pedestal-subcollector DHBT

Large area devices have shown low leakage and excellent DC characteristics. Small area devices were processed with the identical layer structure shown in Table 4.5. The process has already been described in §4.4.1 and §5.2.

The TLM measurements of the collector and, of the pinched and non-pinched base TLMs are given in Fig. 5.29. The collector TLM structures is shown in Fig. 5.28. Thus the contact resistance measured is due to the ohmic contact and the resistance in the pedestal. This resistance from the TLMs is measured to be very high $\approx$ 160-210 $\Omega \cdot \mu m^2$. This is partially due to the poor collector ohmic contact. The sheet resistance of the implanted N^{++} subcollector is $\sim$ 21-22 $\Omega/\square$. The base sheet resistance is $\sim$ 600 $\Omega/\square$, and the base contact resistivity is $\sim$ 25 $\Omega \cdot \mu m^2$. The Isolation between ohmic pads separated by 10 μm is xx pA/μm as seen in Fig. **??**.   For the
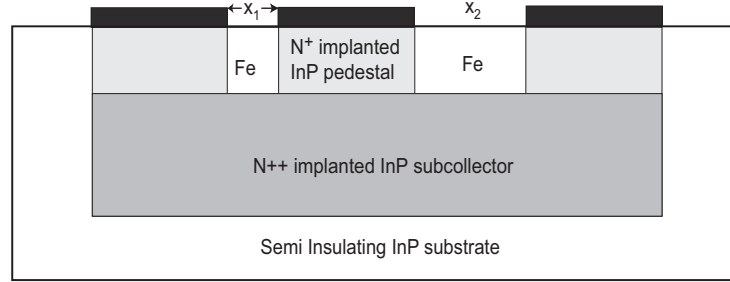
Figure 5.28: Collector TLM structure for the implanted pedestal subcollector DHBT

device with $A_{jBE} = 0.65 \times 4.3~\mu m^2$, $A_E = 0.7 \times 5.25~\mu m^2$ and active base collector area $1.3 \times 5.25~\mu m^2$, Fig. 5.30 is a plot of the DC $I_C - V_{CE}$ characteristics. The maximum current gain at V_{cb} =0 is ~35. The Gummel curves are plotted for V_{cb} =0V and V_{cb} =0.3V Fig. 5.31. The collector and base ideality factors are $\eta_c = 1.26$ and $\eta_b = 1.77$. The leakage current I_{CEO} from the gummel curves is $\approx$ 1 nA at $V_{cb} =$ 0.3V. The DC current gain of the transistor = I_c/I_b from the gummel curves is shown in Fig. **??**. The HBT's gain compression point is $\approx$ 4 $mA/\mu m^2$ at $V_{cb} = 0$V and 5 $mA/\mu m^2$ at $V_{cb} = 0.3$V. At high current densities, $V_{CB,i} = VCB, applied - I_C R_c$. From the TLMs and the geometry of the transistor, R_c for this transistor should be $\approx$ 11 Ω. At $I_c \approx$ 15mA, $V_{CB,i} = VCB, applied$ - 0.3V. The base collector junction is forward biased till $V_{CB,applied}$ is ≈ 0.3V. The collector resistance is extracted from the $I_C - V_{CE}$ characteristics of the transistor at saturation, using the Fixed β method
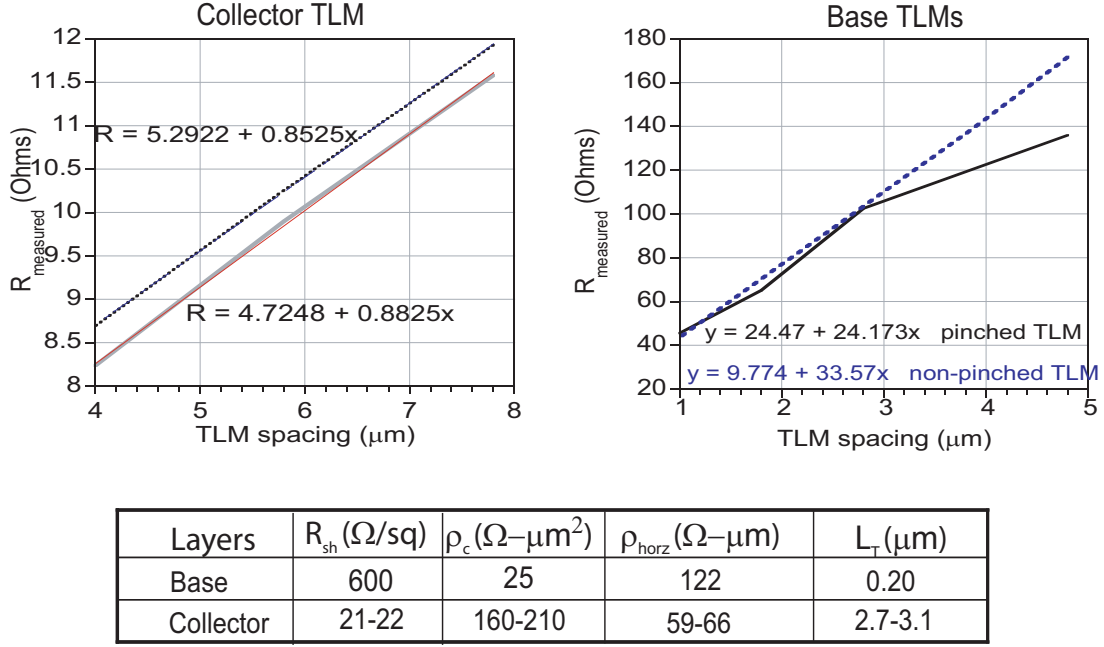
Figure 5.29: Base and Collector TLM measurements

and is plotted in Fig. **??**. The emitter resistance, $R_{ex} \approx 4$ Ω (from Fig. 5.35, the collector resistance is determined to be $\approx$ 32-34 Ω, consistent with the value calculated from TLM measurements. This is very high compared to the value of 1-3Ω that is typically obtained and is partly due to the poor ohmic contact to N^{++} InP.

The resistance as seen in the emitter, $R_{ex} + R_{bb}/\beta$ is derived from gummels and plotted as function of current density Fig. 5.35. From TLM's measured, $R_{bb}/\beta \approx 1$ Ω and therefore $R_{ex} \approx 4$ Ω. Also plotted in Fig. **??**is the thermal resistance, $\Theta_{th} \cdot \phi$ (also referred to as R_{th}). The thermal-electric feedback coefficient ϕ from [8], is 0.85 mV/° K at 5 $mA/\mu m^2$. The thermal resistance at 5 $mA/\mu m^2$ is therefore 2.7 ° K/mW, . Shown in Fig. 5.36 are I_{CEO} and I_{CBO} of a triple mesa DHBT and an implanted pedestal-subcollector DHBT. The breakdown voltages are defined at I_c = 1 mA. BV_{CEO} = 6.8V and BV_{CBO} = 7.6V. For a fully epitaxial, standard mesa DHBT, the corresponding voltages are BV_{CEO} = 5.5V and BV_{CBO} = 6.8V at I_c = 1mA. The breakdown enhancement in these implanted pedestal-subcollector devices is due to lower surface breakdown due to suppression of surface states. The safe operating area is a more relevant than breakdown voltage for digital logic circuits and is seen in Fig. 5.37. The maximum operating power density is seen to be $\sim$ 15 mW/μm^2.
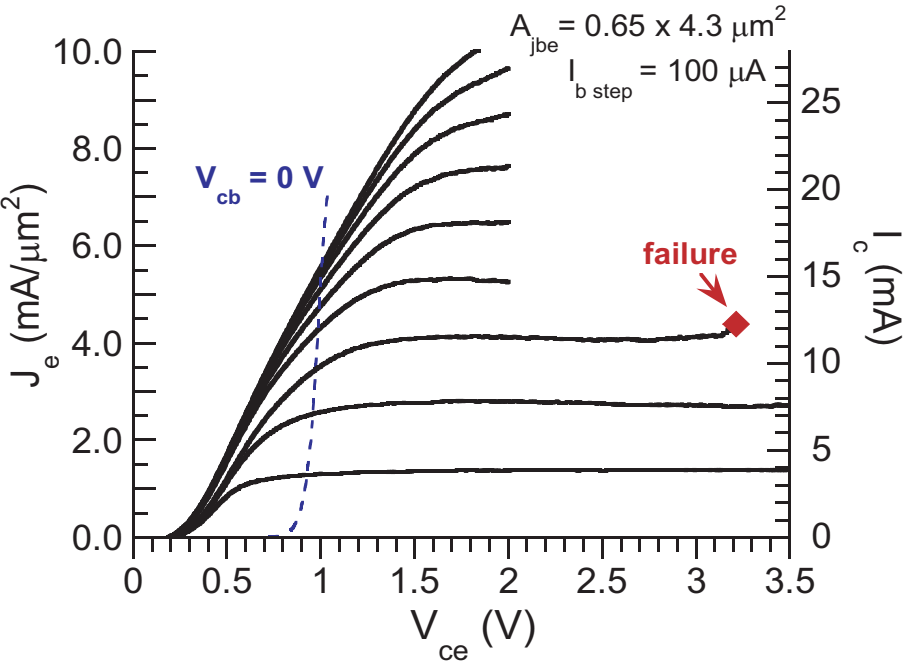
Figure 5.30: DC $I_C - V_{CE}$ characteristics
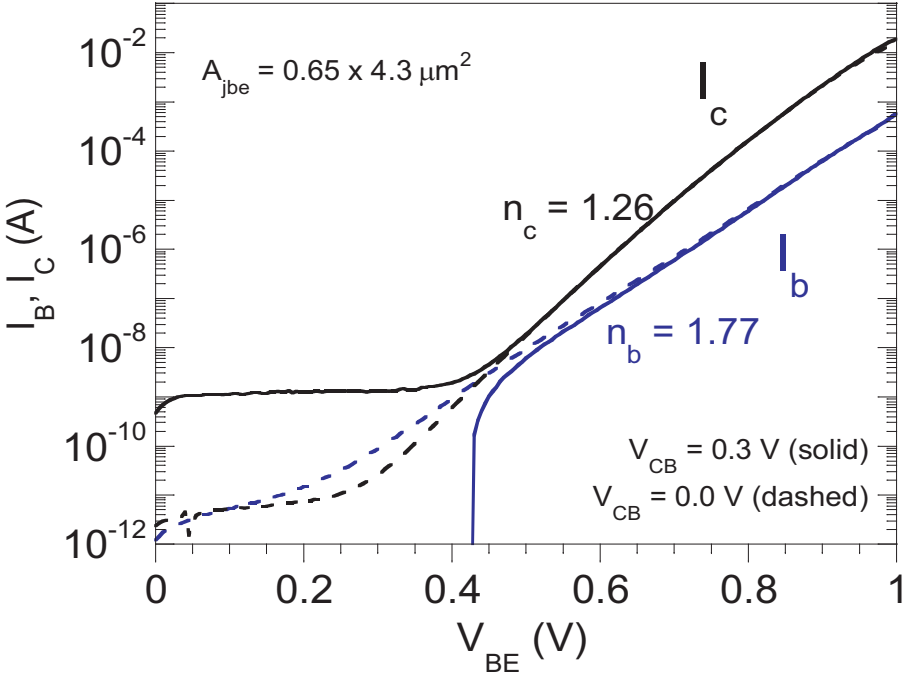
Figure 5.31: Gummel curves at $V_{cb} = 0$V and 0.3V
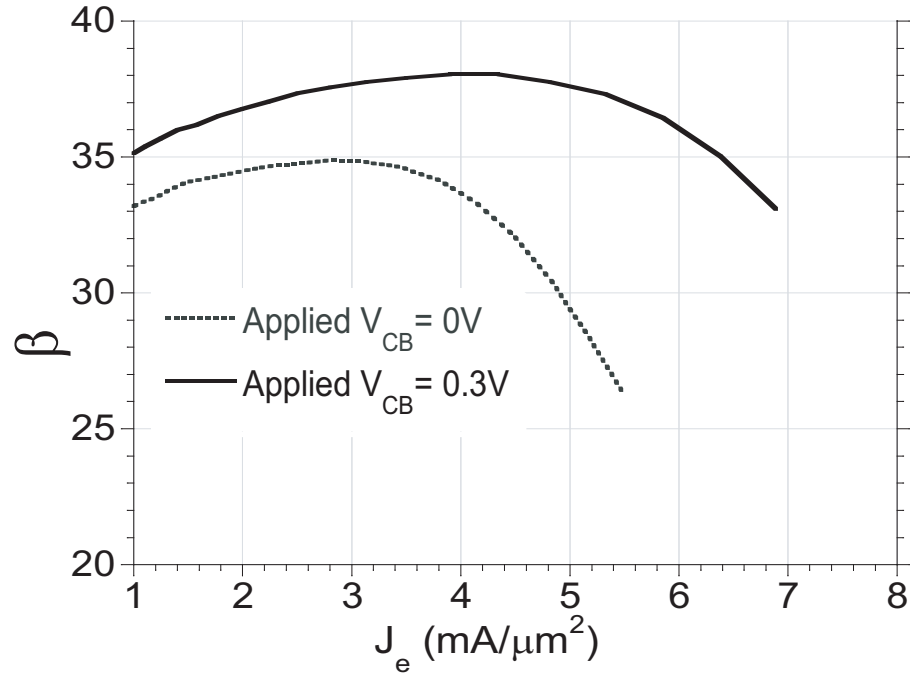
Figure 5.32: DC gain of the HBT at $V_{cb} = 0$V and 0.3V
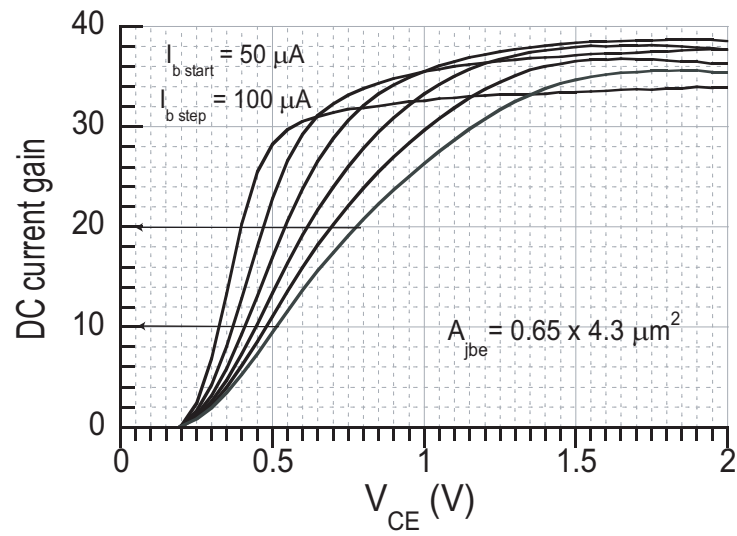
Figure 5.33: Extraction of Collector resistance from saturation characteristics
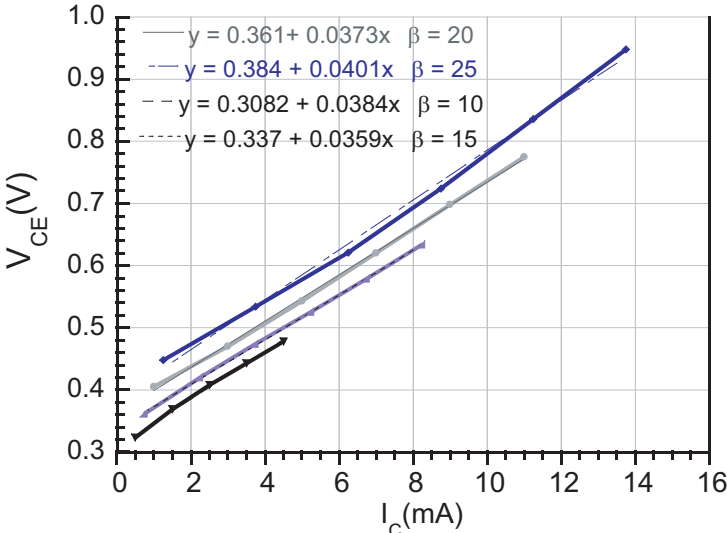
Figure 5.34: Collector resistance at various β's
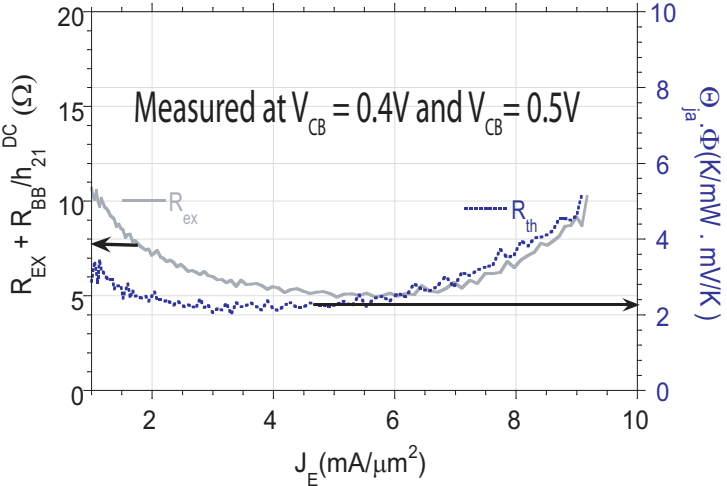
Figure 5.35: Extraction of Emitter resistance, and thermal resistance
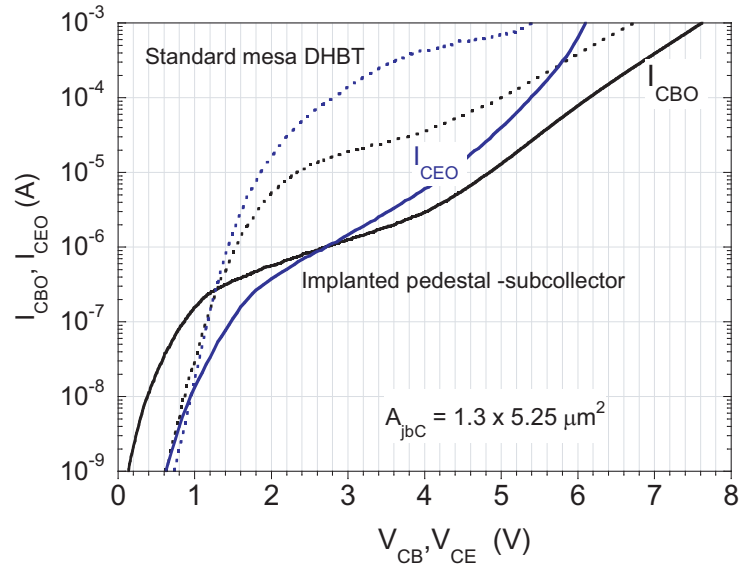
Figure 5.36: Leakage currents in the device
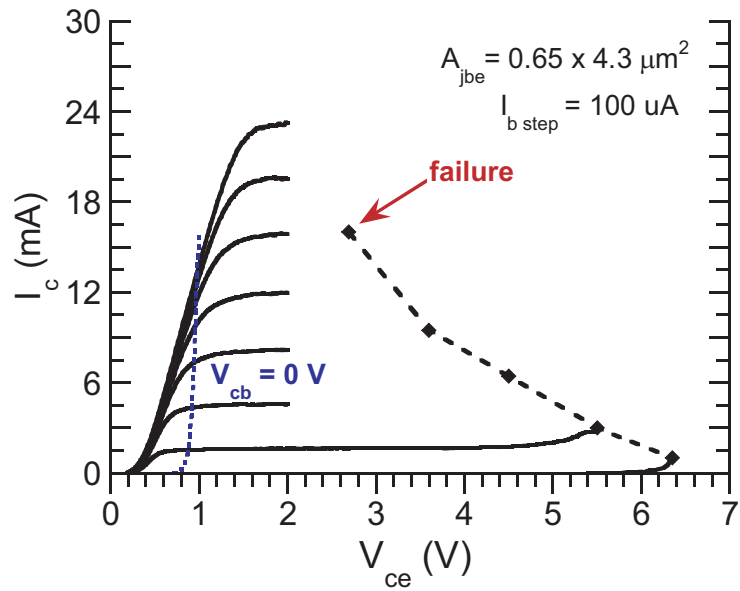
Figure 5.37: Safe Operating area of the device

DC-45 GHz S-parameter measurements are carried out after performing an off wafer Line-Reflect-Reflect-Match calibration on an Agilent 8510C network analyzer. On-wafer open and short circuit pad structures identical to the ones used by the devices are measured after calibration in order to de-embed their associated parasitics from the device measurements. f_{max} is determined from extrapolation through a least-square-fit between the transfer function,

$$U(f) = \frac{U_{DC}}{1 + U_{DC} \cdot (f/f_{max})^2} \tag{5.4.0}$$

to the measured microwave gain U at measured frequencies. $1/f_\tau$ is the slope of $\text{Im}(1/h_{21})$ as explained in Chapter 4 . A maximum 352 GHz f_τ and 403 GHz f_{max}
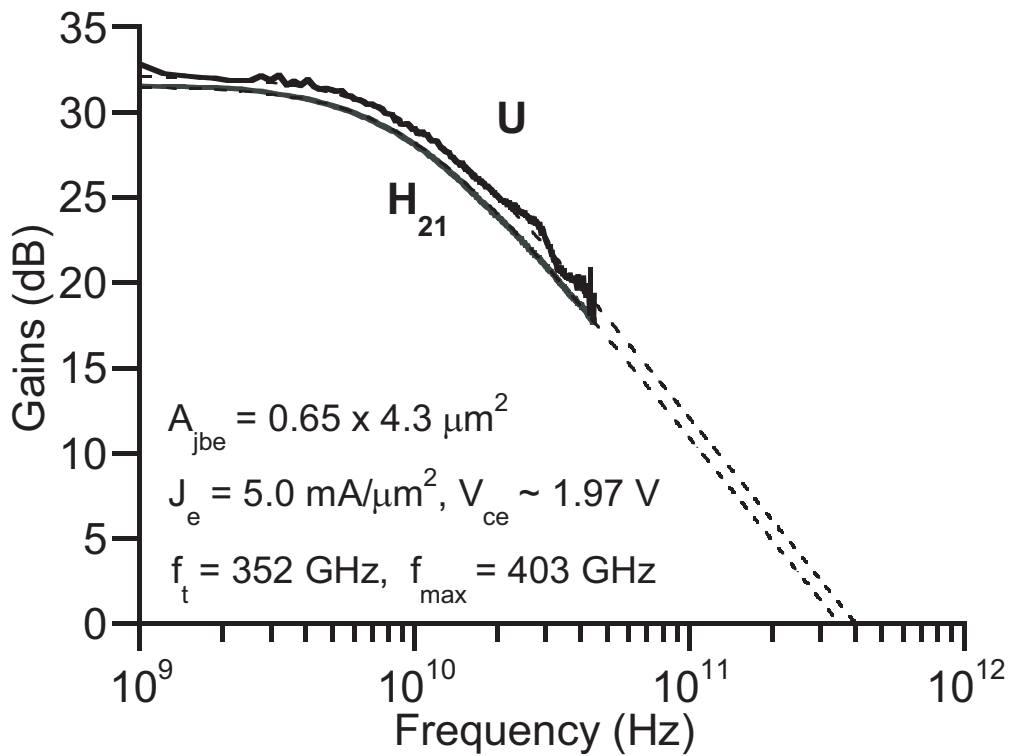
Figure 5.38: Microwave gains of Si implanted subcollector DHBTs

is demonstrated at $I_c = 14$ mA and $V_{cb} = 1.96$ V ($J_e = 5$ $mA/\mu m^2$, $C_{cb}/I_c = 0.43$ ps/V). These are lower than the standard, fully epitaxial, triple mesa DHBT. The collector resistance is much higher (32 Ω vs. 2Ω).

The capacitance voltage characteristics of the implanted subcollector DHBTs with Fe at $I_c = 0$ mA, are plotted and compared with the standard mesa equivalent in Fig. 5.39. From the figure, The implanted subcollector DHBTs with Fe exhibit a C_{cb} reduction of ≈ 3.2 fF over the entire measured range of bias voltages due to elimination of the charge dipole at the growth interface. At full depletion, this corresponds to a 25-27% decrease in C_{cb}. This is lower than expected reduction in C_{cb} and is attributed to lateral implant straggle. Here, $A_{jBC} = 1.3 \times 5.25 \mu m^2$ $A_{pad} = 2.5 \mu m^2$. The pedestal stripe as defined on the photo mask is 0.9×5.25 μm^2. The length of the subcollector as defined on the photo mask is 5.25 μm. The voltage drop $I_c \times R_c$ is significant and the collector potential must be progressively increased as I_c, to fully deplete the drift collector. The lower f_τ and f_{max} demonstrated by the implanted HBTs compared to their triple-mesa counterpart is due mostly to the increased delay associated with the terms kT/qI_c $(C_{cb} + C_{je})$ and R_c C_{cb}. Fig. 5.41 shows C_{cb}/I_c as a function of bias. C_{cb}/I_c is an important metric for digital logic circuits.
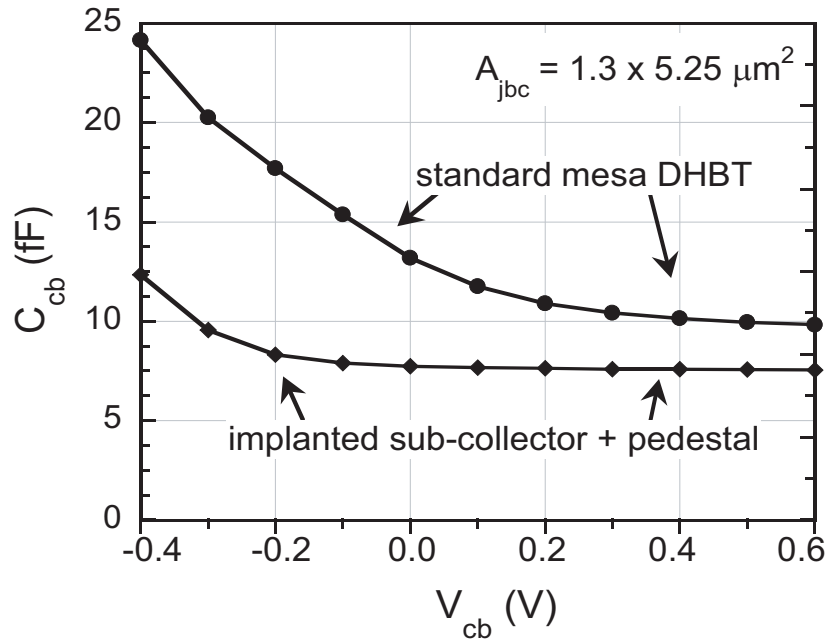
Figure 5.39: Variation of C_{cb} with C_{cb} at $I_c = 0$ mA for a mesa HBT and the pedestal HBT

The slightly lower C_{cb} reduction than expected, is due to lateral and longitudinal implant straggle. The DC results compare with the standard mesa DHBT and hence
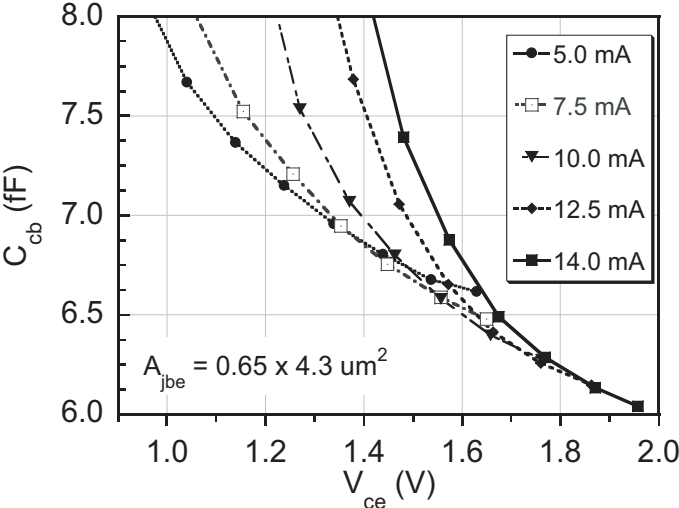
Figure 5.40: Variation of C_{cb} with V_{cb} at different I_c to show the effect of high series collector resistance

indicate the feasibility of manufacturing microwave HBTs on the triple implanted substrates. The high collector contact resistance has resulted in lower f_τ and f_{max} compared to [9].
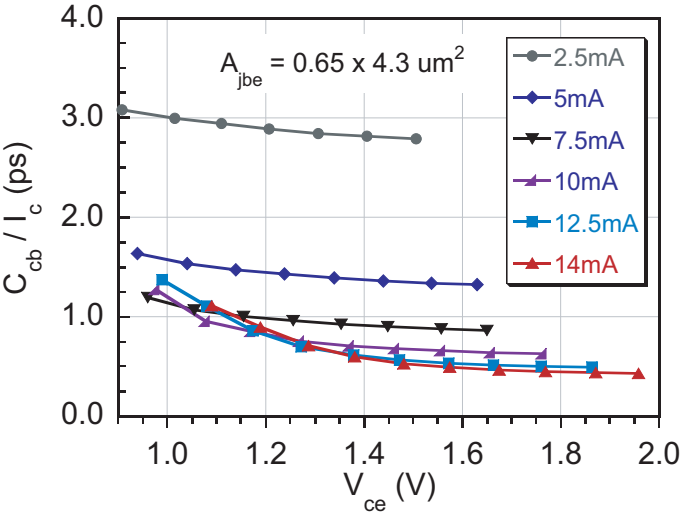
Figure 5.41: C_{cb}/I_c as a function of bias

5.5 Discussion

These first generation fully implanted pedestal-subcollector DHBTs have record bandwidths for implanted collector DHBTs. However, they suffer from some problems

- Large collector resistance

- less than expected C_{cb} reduction

These issues will be discussed in the following sections and solutions suggested

5.5.1 Pedestal vertical height and lateral straggle

In order to evaluate the height of the pedestal, C-V measurements are carried out on devices with no N^{++} pedestal implant. These have the N^- collector directly atop the SI Fe implanted region and therefore resembles the extrinsic portion of the device, $\hat{C}_{cb} = 0.54 \ fF/\mu m^2$. This is compared with a device, where the N^{++} pedestal and subcollector extends throughout the device so that it resembles a mesa structure. $\hat{C}_{cb}$ for this mesa-like device is 1.1 $fF/\mu m^2$ and the $\tau_c = 120$ nm. Therefore the height of the pedestal is deduced to be ~ 120 nm.

At full depletion, C_{cb} is measured as for various devices with different pedestal geometries and plotted as function of pedestal width to determine the lateral pedestal straggle.

$$\frac{C_{cb}}{\epsilon/T_c} \cdot \frac{1}{L_e} = 0.5 \cdot (W_{BC} + W_p) + \Delta W_p \qquad (5.5.0)$$

where ΔW_p is the capacitive lateral straggle on each side of the pedestal. This normalized capacitance is plotted vs. W_p and is shown in Fig. 5.43. From this, the straggle on either side is $\sim 0.2 \ \mu m$ and is responsible for the less than anticipated reduction in C_{cb}. This calculation ignores the longitudinal straggle due to the subcollector implant.

The simplest way to address the straggling problem is to reduce the dimension of the mask. However, less than 0.5 μm features are hard to define using the optical stepper system at *UCSB*. Therefore one method of reducing the Si_xN_y implant mask dimensions is shown in Fig. 5.44. However, the resistive straggle is seen to be $\sim$ 0.05 μm. Therefore reducing the mask dimension laterally, reduces the capacitance but adds to the vertical pedestal resistance. SIMS data on a test wafer, shows no diffusion of the Fe after growth.
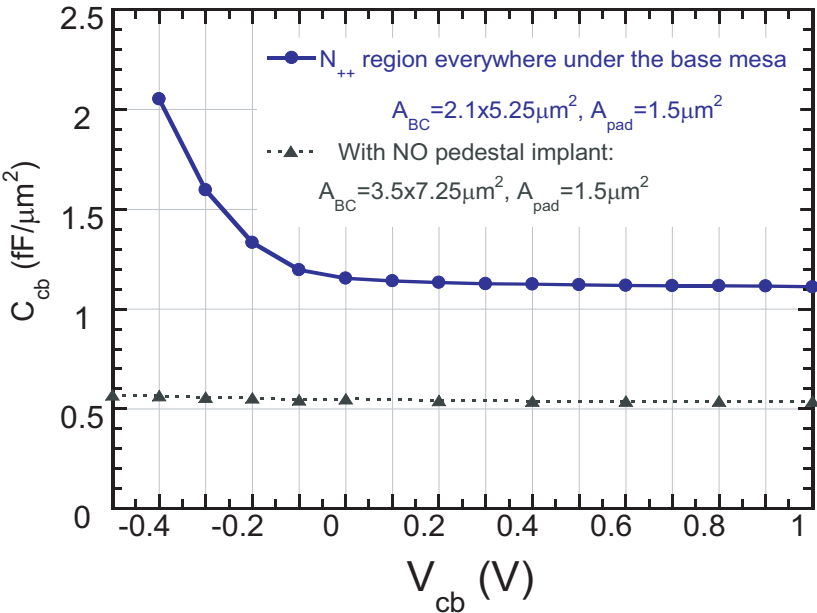
Figure 5.42: C-V measurements of a device without an N^{++} pedestal and one with N^{++} subcollector and pedestal everywhere in the device footprint so that it resembles a mesa geometry.
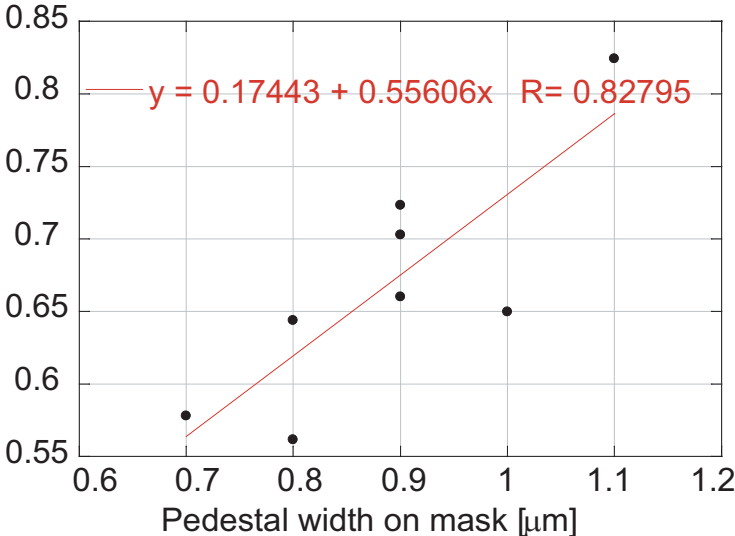
Figure 5.43: Normalized C vs. pedestal width to determine capacitive straggle due to implant
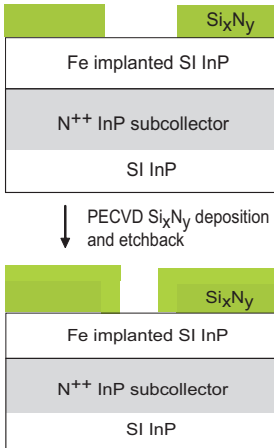
Figure 5.44: To obtain submicron features for implant mask...
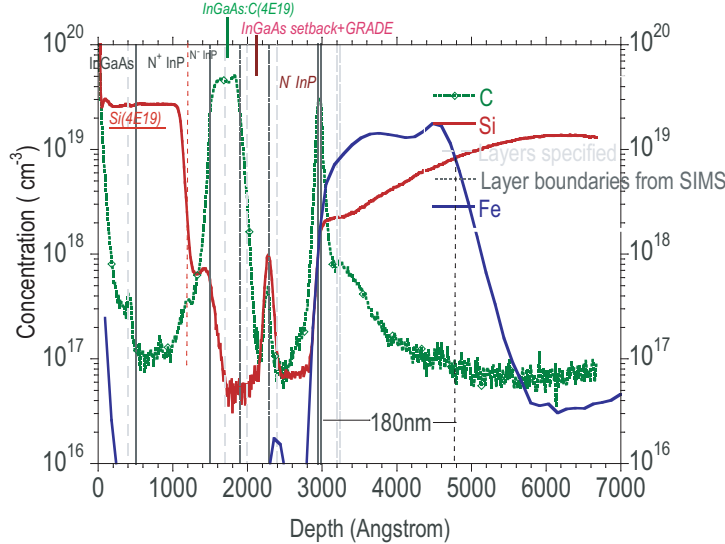
Figure 5.45: SIMS of the HBT layer stack after growth on implanted layers. There is no pedestal implant here

5.5.2 Excess Collector Resistance
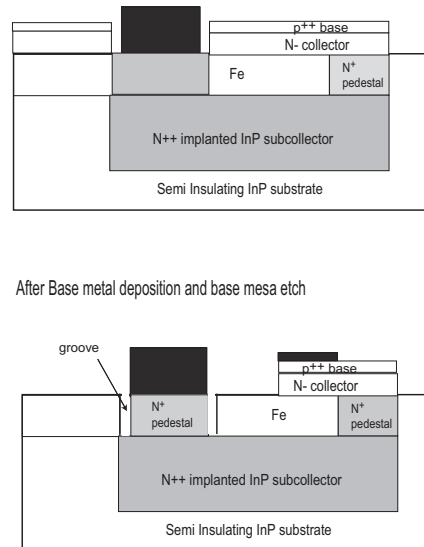
Figure 5.46: Reverse collector ohmic process

As with the implanted subcollector DHBTs, these DHBTs too suffer from poor collector contact resistance due to insufficient anneal. A new process is proposed, where the collector metal is deposited by recess etching through the base and collector layers. The collector metal does not perfectly fill this recess but instead resembles Fig. 5.46a. When the base mesa is etched, the semiconductor next to the collector contact is etched as well, as seen in Fig. 5.46b. However, this does not in any way impact the implanted pedestal-subcollector DHBT as the semiconductor etched away is Fe implanted InP layer. Therefore the reverse collector ohmic process is feasible for implanted pedestal subcollector DHBTs even with the current photo masks by merely reversing the deposition of the base and collector ohmics. This now permits a much higher anneal for the collector ohmic, reducing the contact resistivity to 20-25 $\Omega \cdot \mu m^2$.

From §5.4, it is seen that the calculated R_c from TLMs is 11 Ω. This does not explain the very high resistance seen in the devices of $\sim 32 \, \Omega$. Several devices were measured and the excess R_c values tabulated in Fig. 5.47.

These suggest that the excess resistance is due to the pedestal itself. Special test structures were placed on another wafer implanted similarly. The pedestal TLM is a special test structure (Fig. 5.48), where only the Si pedestal implant is carried out in a background of Fe already implanted and activated. From these, the sheet

177

$W_p(\mu m)$	$L_p(\mu m)$	$R_c(\Omega)$	R_c from TLM(Ω)	Excess R_c $(\Omega–\mu m)$
0.8	5.25	34.4	12	117.6
1	7.25	23.2	8.6	105.9
Mesa	Mesa	29.1	11.6	91.9
0.9	4.25	35.3	14.7	87.5
1.3	5.25	35.2	11.6	128.6

Figure 5.47: Excess Collector resistance of devices of various geometry

resistance of the pedestal is deduced to be ~ 38 $\Omega/\square$, exactly as measured earlier. The vertical contact resistance is now entirely due to the ohmic contact and is seen to be ~ 25 $\Omega \cdot \mu m^2$. The pedestal-subcollector TLM in Fig. 5.48 measures a contact resistivity of 60 $\Omega \cdot \mu m^2$. Since the pedestal resistivity is low, this means that there is a resistance of 35 $\Omega \cdot \mu m^2$ at the interface between the pedestal and the subcollector.

After 360°C anneal		
TLM	R_{sh} (Ω/sq)	ρ_c $(\Omega–\mu m^2)$
pedestal-subcollector	21	60
pedestal	38	25
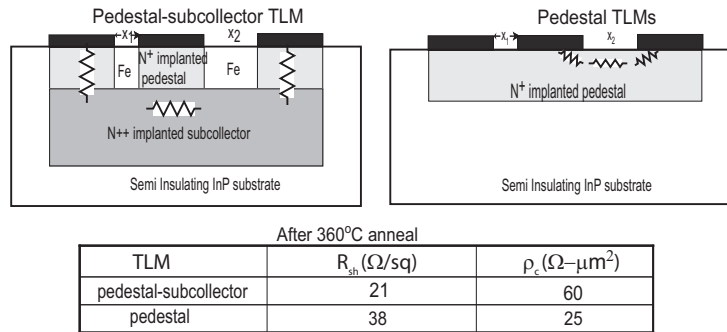
Figure 5.48: Special test structures to find the source of excess R_c

This is attributed to the large Fe pile up seen in §5.2.1. The R_c is not due to the narrow pedestal dimensions but instead due to insufficient Si at the region of Fe pileup. This is evident from the common emitter IVs of two devices in Fig. 5.49, one with a narrow pedestal and one where the pedestal and subcollector are present over the entire device footprint.

As discussed in Chapter 3 , the Fe preferentially piles up in the region of most damage. RBS does not detect defects below $\sim 1 \times 10^{20}$ cm^{-3}. This is still a large number of defects. e implant is performed at a lower dose (1×10^{14} ions/cm^2) and
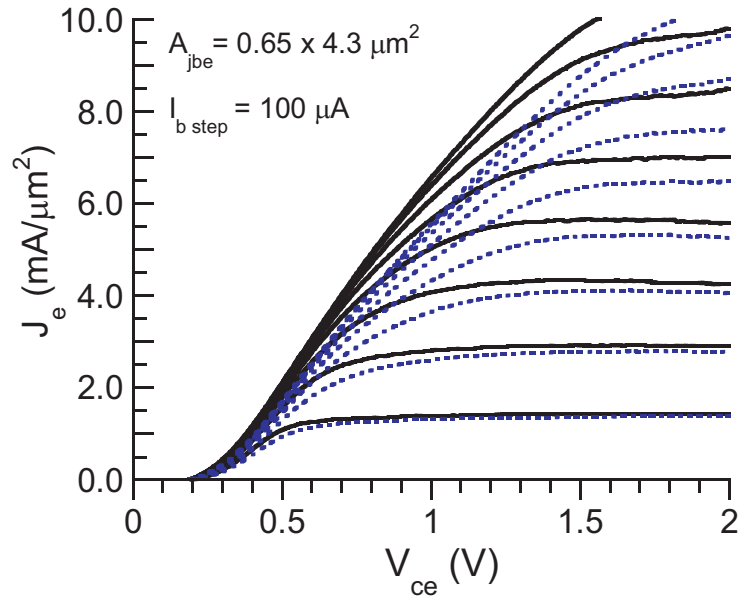
Figure 5.49: SIMS of the HBT layer stack after growth on implanted layers. There is no pedestal implant here

lower energy (100 keV) to check if there is a dose dependence of such damage. There is no evidence of Fe pile up at these implant conditions. CV measurements on Schottky diodes are performed to check the thickness of the Fe compensated layer for these conditions. This is shown in Fig. 5.51

While these first generation HBTs suffered from certain problems, it is shown that these can be resolved.
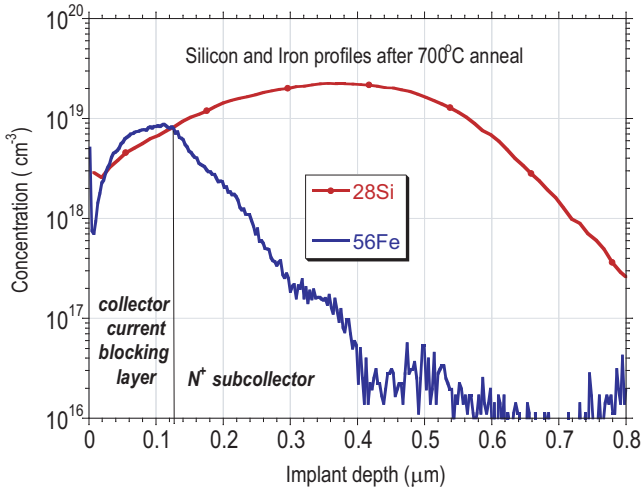
Figure 5.50: Distribution of Fe and Si after anneal
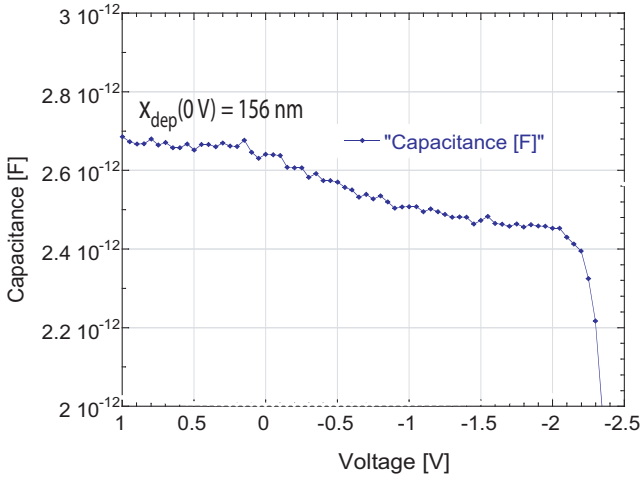
Figure 5.51: CV measurements of Schottky diodes to determine the depletion thickness for these implant conditions

References

[1] M.J.W. Rodwell, M. Urteaga, Y. Betser, D. Scott, M. Dalhström, S. Lee, S. Krishnan, T. Mathew, S. Jaganathan, Y. Wei, D. Mensa, J. Guthrie, R. Pullela, Q. Lee, B. Agarwal, U. Bhattacharya, S. Long, "Scaling of InGaAs/InAlAs HBTs for high speed mixed-signal and mm-wave ICs", *Int. J. High-Speed Electron. Syst.*, Vol. 11, no. 1, pp. 159-215, 2001.

[2] S. Lee, M. Urteaga, Y. Wei, Y. Kim, M. Dahlstrom, S. Krishnan, M. Rodwell, "Ultra high fmax InP/InGaAs/InP transferred substrate DHBTs", *Device Research Conference*, Santa Barbara, CA, 24-26 June 2002, pp. 107-108

[3] T. Arai, Y. Harada, S. Yamagami, Y. Miyamoto and K. Furuya, "C$_{BC}$ reduction in GaInAs/InP buried metal heterojunction bipolar transistor", *Proc. of the International Conference on Indium Phosphide and Related Materials*, Williamsburg, VA, May 14-18, 2000, pp. 254-257

[4] Y. Miyamoto, J. M. M. Rios, A. G. Dentai,S. Chandrasekhar,"Reduction of base-collector capacitance by undercutting thecollector and subcollector in GaInAs/InP DHBTs", *IEEE Electron Device Letters*, Vol. 17, No. 3, Mar. 1996

[5] J.-S. Rieh, M. Khater, K.T. Schonenberg, F. Pagette, P. Smith, T.N. Adam, K. Stein, D. Ahlgren, and G. Freeman, "Collector vertical scaling and performance tradeoffs in 300 GHz SiGe HBT", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 235-236

[6] Y. Dong, Z. Griffith, M. Dahlström, and M.J.W. Rodwell, "C_{cb} reduction in InP heterojunction bipolar transistors with selectively implanted collector pedestal", *Device Research Conference*, Notre Dame, IN, June 21-23, 2004, pp. 67-68

[7] J. Cheng et al., "Semi- Insulating properties of Fe-implanted InP. I. Current limiting properties of n+ - semi insulting n+ structures", *Journal of Applied Physics*, Vol. 58(5), pp. 1780-1786, Sep. 1985

[8] W. Liu, H-F. Chau and E. Beam, "Therma1 Properties and Thermal Instabilities of InP based Heterojunction Bipolar Transistors", *IEEE Transactions on Electron Devices*, Vol. 43, No. 3, pp. 388-395, Mar. 1996

[9] Z. Griffith, M. J. W. Rodwell, X.-M. Fang, D. Loubychev, Y. Wu, J. M. Fastenau, and W. K. Lui, "InGaAs/InP DHBTs with 120 nm collector having simultaneously high f_τ, $f_{max} \geq 450$ GHz", *IEEE Electron Device Letters*, Vol. 26, no. 8, pp. 530-532, 2005

6

Conclusions

IMPLANTED subcollector and pedestal DHBTs were demonstrated for the first time in an all implanted, manufacturable process. Record bandwidths for DHBTs with implanted collectors have been demonstrated. These were incorporated in high speed CML and ECL logic circuits that have demonstrated over 20% improvement in digital logic speed over conventional mesa DHBTs.

6.1 Accomplishments

As the current mesa InP DHBT is reaching its scaling limit, new process modules were characterized and added to further the limits of such devices [1]. The parasitic collector base capacitance is especially an important hurdle for high bandwidth analog circuits and high speed digital circuits. A manufacturable technology that enable submicron collector scaling of InP HBTs utilizing ion implantation is proposed and developed. For this purpose, Si and Fe implants in InP are extensively studied and characterized. With the lithographic dimensions feasible today, the device design has been tailored for high speed digital circuit performance.

Modern mesa DHBTs have an extrinsic access pad that contributes significantly to the collector base capacitance. This capacitance is non-scalable and becomes important as device length is reduced. A selectively implanted Si subcollector is suggested in Chapter 4 to eliminate this base access pad capacitance. However, devices fabricated did not show any reduction in collector base capacitance at low bias voltages due tp the presence of an N-type interface charge at the growth surface. A new method of eliminating this interface charge using Fe implants is proposed and demonstrated to work effectively over a wide range of charge densities [2]. Implanted subcollector DHBTs utilizing selective Si implants for isolation of the subcollector and Fe implants for eliminating the interface charge are developed. These devices is shown to almost completely eliminate this base access pad capacitance and have cut-off frequencies in excess of 350 GHz [3]. This technology enables for low power, high speed digital circuits. The bandwidth of the devices are limited by

the excessive base and collector resistance due to poor ohmic contacts. Improving the ohmic technology should yield superior, high speed devices in a simple process.

Further collector scaling is made possible through a novel fully implanted pedestal-subcollector technology described in Chapter 5 . An implanted, buried subcollector is formed in SI InP substrate by high energy Si implants. Fe is used to compensate the top 0.2 μm of Si to make this region Semi-Insulating. An additional set of Si implants then form an N^{++} pedestal link to the subcollector. Such a topology requires no extra growths and is very planar. By tailoring the width of the pedestal, the collector can be scaled independent of the base mesa dimensions. Several experiments and measurements are carried out to completely characterize this device structure. The sheet resistance of the subcollector and pedestal are designed to be low, so as to not hurt the collector resistance. The implant and anneal conditions are developed to result in a crystalline semiconductor before growth. Standard mesa devices can then be fabricated after growth. Thus this process is very modular. Microwave devices fabricated, demonstrated f_τ's of over 350 GHz and f_{max} of over 400 GHz [4]. The breakdown voltages are higher than triple mesa DHBTs due to lower active surface states. The C_{cb} reduction was $\sim$ 30 %. The large collector resistance and lateral straggle due to the pedestal implant has limited the performance of this device. The collector resistance is higher than a standard mesa DHBT, partly due to a poor ohmic contact and partly due to Fe piling up at the interface between the pedestal and the subcollector, causing a vertical resistance at this interface. This is due to the large implant dose of Fe. This has been solved by using a lower fluence of Fe where no such pile-up in observed (§5.5 in Chapter 5). The lateral straggle can be solved by reducing the dimensions of the implant mask, as discussed in §5.5 in Chapter 5 . With these two modifications, cut off frequencies in excess of 500 GHz are expected, at the current scaling node. As devices are laterally and vertically scaled, C_{cb} contributes increasingly to delay of analog and digital circuits. Such a technology should enable C_{cb} reduction in an elegant, high yield process.

Digital latches were fabricated using a similar collector pedestal process at Rockwell Scientific. These devices had cut-off frequencies of $\sim$ 350 GHz. Low power CML dividers having ΔV_{logic} is 250 mV and effective loading resistance of 100 Ω – I_{data} = 2.5 mA, are demonstrated [5]. The divider operation is fully static, operating from f_{clock} = 4 GHz to 61.2 GHz while dissipating 27.1 mW of power in the flip-flop from a single -2.30 V supply. The power-delay product of this circuit is 113.0 fJ/latch. This is a record low power-delay product for an InP DHBT-based static frequency divider. Without the implanted collector technology, dividers in a regular mesa DHBT process clocked at a maximum of 51 GHz while consuming 29.2 mW of power. Thus a 20% improvement in logic speed is achieved. Ultra high speed CML logic circuits have also been demonstrated. With the collector pedestal technology, the maximum f_{clock} is $\sim$ 135 GHz, while dividers in the triple mesa process

clocked at a maximum of 110 GHz. Initial testing of ECL static frequency dividers show promising results, with self oscillation frequencies in excess of 95 GHz, a 10 % improvement over the fastest logic circuits demonstrated [6]. These results have been obtained with first generation DHBTs with collector pedestals with the process still at its infancy. Very high bandwidth power amplifiers at over 300 GHz and digital circuits clocking at 200 GHz are feasible even in the near future.

6.2 Future work

The first demonstration of these implanted collector yielded devices with record bandwidths. However, the full potential of this process is limited by

- Large straggle due to pedestal implant

- Large vertical resistance in the pedestal collector due to Fe pileup

- Poor ohmic contacts to N^{++} InP

As discussed in §5.5, the contact resistivity to the N^{++} InP collector can be reduced by forming the alloyed collector ohmics before the base metal deposition, allowing a very high temperature anneal. The Fe pile-up is shown to be decreased at lower implant doses of Fe, while the pedestal implant mask can be redesigned to overcome the lateral implant straggle. By carefully choosing the implant doses of Fe and Si pedestal implant, these problems is shown to be overcome. Simulations predict device bandwidth in excess of 500 GHz with these enhancements.

The triple implanted pedestal subcollector process is very modular and can be inserted into many HBT technologies. Regrown HBTs have been demonstrated with 0.3μm emitter features [7]. As seen in Chapter 2 , the emitter resistance also needs to be reduced with scaling generations. Utilizing very thin collectors and base layers, the implanted collector processes can be combined with emitter regrowth, to decrease the transit times and RC charging time constants. Initial simulations predict devices with f_{max} close to 800 GHz (Chapter 2). The emitter resistance is limited by the contact resistivity of the ohmic contact. *Insitu* MBE deposited ErAs is known to form a perfect ohmic to InGaAs [8]. The implanted collector process can again inserted into a process utilizing ErAs ohmics for the emitter. All three processes can also be combined to yield HBTs with cut-off frequencies in excess of a THz and digital logic circuits clocking at over 300 GHz.

As seen in Chapter 5 , the Fe compensation of Si implant results in effective blocking of current till $\sim$ 2V. This suggests a restructuring of the HBT, to form a collector-up HBT such that Fe implant is used for emitter scaling, as seen in Fig. **??**.

A N^-/N^{++} template is grown and Fe is selectively implanted through the N^- emitter. Taking advantage of the lateral straggle of this implant, narrow emitter base junctions can be defined. The base and collector are then grown, and the device is formed in a similar triple mesa process as in [6]. The collector base junction is now very narrow and there is zero extrinsic capacitance. The emitter resistance is now a lateral resistance. The N^{++} emitter can be made thick to reduce the lateral access resistance in the semiconductor. This hurts device planarity, however, trench isolation techniques can be developed as in Fig. 6.2. The emitter resistance is, to first order, independent of the emitter base junction area.

$$C_{cb} \propto \frac{L_e W_c}{T_c} \tag{6.2.1}$$

$$R_{ex} \propto \frac{\rho_c}{L_e} \tag{6.2.2}$$

Hence, devices can be laterally scaled without significantly affecting the emitter resistance. This is particularly useful for high speed digital logic circuits.

With such enhancements described above, InP HBTs are poised to break the 1 THz barrier. These ultra high speed devices may find applications in high bandwidth communication links and sensing operations. The majority of the applications will remain unforeseen. Indeed, *the principal applications of any sufficiently new and innovative technology have always been applications that were created by that technology* [9].

Fe implant

N$^-$ InP

N^{++} InGaAs

N^{++} InP

MBE growth and
device formation

Collector
contact

N$^-$ collector

Emitter contact

Base

Fe implanted
current block

N$^-$ InP

N^{++} InGaAs

N^{++} InP

SI InP
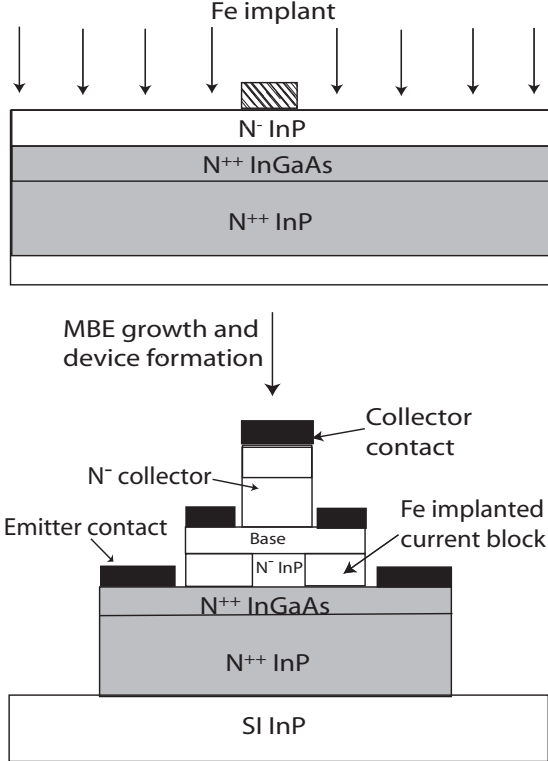
Figure 6.1: Proposal of a collector-up process with implants

spin on
glass

Si$_x$N$_y$

x

Trench width = 2μm
Trench depth = 0.5 μm

InP
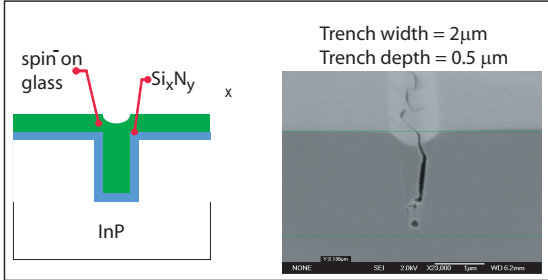
Figure 6.2: Trench isolation for InP HBTs

References

[1] M.J.W. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S.C. Martin, R. P. Smith, S. Jaganathan, S. Krishnan, S. I. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, and M. Dahlström. "Submicron Scaling of HBTs" *IEEE Trans. on Electron Devices*, Vol. 48, pp. 2606-2624, November 2001.

[2] N. Parthasarathy, C. Kadow, Z. Griffith, M.J.W. Rodwell, M. Urteaga, K. Shinohara, R. Pierson, B. Brar "Interface charge compensation in InP based Heterojunction Bipolar Transistors with implanted subcollectors", submitted to *Applied Physics Letters*, Feb. 2006.

[3] N. Parthasarathy, Z. Griffith, C. Kadow, U. Singisetti, M.J.W. Rodwell, M. Urteaga, K. Shinohara, R. Pierson, B. Brar, "Selectively implanted subcollector DHBTs ", *IEEE conference on Indium Phosphide and Related Materials*, Princeton, New Jersey, May. 2006.

[4] N. Parthasarathy, Z. Griffith, C. Kadow, U. Singisetti and M.J.W. Rodwell, "Collector-Pedestal InGaAs/InP DHBTs Fabricated in a Single-Growth, Triple-Implant Process", *IEEE Electron Device Letters*, vol. 52, no. 4, 2006.

[5] Z. Griffith, N. Parthasarathy, M.J.W. Rodwell, M. Urteaga, K. Shinohara, P. Rowell, R. Pierson, B. Brar, "An Ultra Low-Power ($\leq$ 13.6 mW/latch) Static Frequency Divider in an InP/InGaAs DHBT Technology", submitted to *IEEE MTT-S International Microwave Symposium*, San Francisco, California, Jun. 2006.

[6] Z. Griffith, M. Dahlström, M. J. W. Rodwell, M. Urteaga, R. Pierson, P. Rowell, B. Brar, S. Lee, N. Nguyen, and C. Nguyen, "Ultra High Frequency Static Dividers > 150 GHz in a Narrow Mesa InGaAs/InP DHBT Technology", *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Montreal, Canada, pp. 176-179, 13-14 Sep., 2004.

[7] Y. Wei, D. W. Scott, Y. Dong, A. C. Gossard and M. J. W. Rodwell, "280 GHz f_τ InP DHBT with 1.2 μm^2 base-emitter junction area in MBE Regrown-Emitter Technology", *2004 Device Research Conference*, Notre Dame, IN, pp. 237-238, Jun. 2004

[8] *Private communication with Prof. Art Gossard*

[9] H. Kroemer, "Nano-whatever: Do we really know where we are heading?", Physica Status Solidi(a), Vol. 202, No. 6, pp. 957964, 2005

A

Implantation Analysis

SEVERAL techniques exist to evaluate the implants. Various parameters relating to the implant need to be determined.

- Spatial distribution of the implanted ions to determine exact ion range and ion diffusion

- Crystallinity or defect density in the material due to the implant

- Surface quality of the implanted substrate

- Electrical properties, such as carrier mobility, sheet charge concentration, resistivity

- Substitutionality of the implanted dopants

Secondary Ion Mass spectrometry(SIMS)[1] is the preferred technique to evaluate depth profiles of the implanted ions and is used here to evaluate Si and Fe distributions in InP. During SIMS analysis, the sample surface is slowly sputtered away by bombarding with primary ions. The sputtering process produces secondary ions of the constituent elements of the substrate with a range of (translational) kinetic energies. Monitoring the secondary ion count rate of selected elements as a function of time leads to depth profiles. The analysis usually uses Cs^+ or O^- primary ions. The mass spectra of the secondary ions, obtained by continuously monitoring the ion signal while scanning a range of mass-to-charge (m/z) ratios, detects and distinguishes both atomic and molecular ions. The depth resolution of SIMS is between 2 - 30 nm. Mass interferences occur whenever another ion has the same nominal mass as the analyzed ion. Such interferences are called isobaric. During the analysis of iron in silicon for example, $28Si^{2+}$ interferes because it has the same mass-charge as as $56Fe^+$. In this case isotopes such as 29Si or 54Fe are detected and scaled using the corresponding sensitivity factors. SIMS is a destructive technique due to the sputtering away of the constituent elements.

Instrumental Conditions

Condition Number	1	2
Instrument	Cameca	Cameca
Elements Monitored	Si	Fe
Primary Ion Beam	Cs	Cs
Primary Ion Energy	14.5keV	5.5keV
Secondary Ion Polarity	Negative	Positive
Oxygen Leak	No	No
Charge Neutralization†	No	No
Surface Conductive Coating†	None	None
Liquid Nitrogen Cold Trap*	Yes	No

† Used for accurate analysis of insulating samples or substrates.
* Used to minimize instrumental background for atmospheric impurities.

Figure A.1: The conditions used for SIMS in this dissertation

To evaluate the damage or crystallinity, various methods are used such as Rutherford Backscattering spectrometry (RBS), Transmission Electron Microscopy (TEM), X-Ray Diffraction (XRD) and Photoluminescence spectra (PLs). Only RBS is discussed here since this is primarily used for evaluating crystal quality. Rutherford backscattering [2] detects the energies and amount of the backscattered ions from a solid target. Ion channeling is a specific application of RBS in which the absence of backscattering signal is quantified. In an ion backscattering application, alignment of the incident beam with a major crystallographic axis will allow the incident ions to be channeled down the open regions of the crystal lattice. For a channeled orientation, the incident ions can be transported to very great depths ($\geq$ 3-5 μm) from which backscattering events cannot be detected. If the crystal lattice contains either matrix or impurity atoms which are not in the crystal structure, that is, interstitial in the crystal structure, backscattering events can quantify the concentration of interstitial atoms (in units of atoms/cm^2). Thus, range and extent of damage from ion implantation, degree of crystal regrowth upon annealing, and the degree of impurity substitutionality/interstitiality can all be quantified in an ion channeling experiment. Here channeled and rotating random RBS spectra are acquired at detector angles of 160° and 100° from the forward trajectory of the incident He ion beam. The different depth resolution and backscattering kinematics afforded by the use of two different angles improve the accuracy of the measurements. The grazing detector spectra are sensitive to the surface layers of the crystal and provide more precise damage

depths. When the sample is moved in a rotating random orientation, the sample normal is precessed about the incident ion-beam. The backscattering spectrum from this orientation is representative of a spectrum from a polycrystalline sample and is normalizable as the signal for 100% amorphization at all depths. The channeled spectra can then be compared to the rotating random spectra to yield quantifiable channeling parameters.
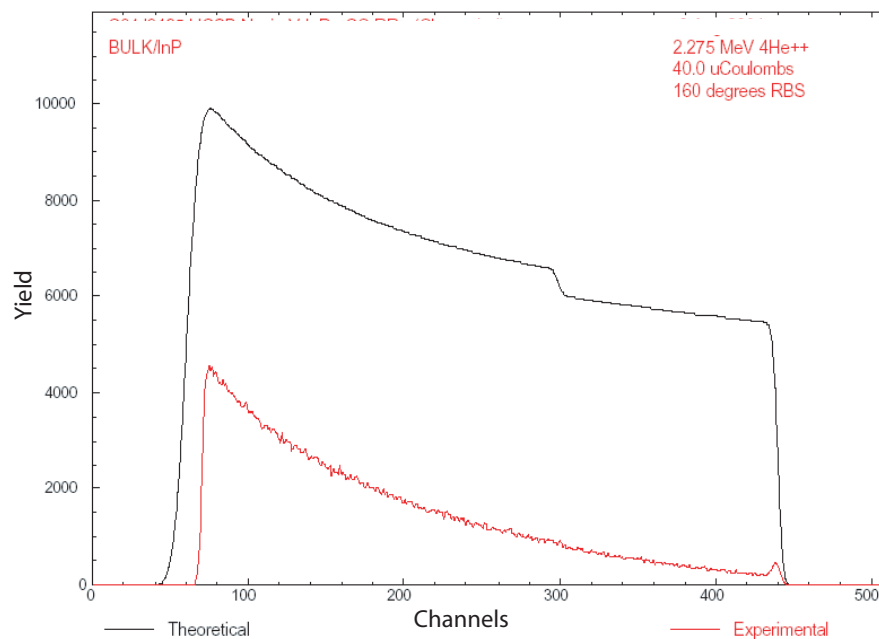
Figure A.2: A sample RBS spectra for SI InP:Fe substrate

To evaluate surface morphology, Atomic Force Microscopy(AFM) [3] is used. These are variations on a method of imaging surfaces with atomic or near-atomic resolution, collectively called scanning probe microscopy (SPM). A small tip is scanned across the surface of a sample in order to construct a 3-D image of the surface. Fine control of the scan is accomplished using piezoelectrically-induced motions. Any type of surface can be probed by the molecular forces exerted by the surface against the tip. The tip can be constantly in contact with the surface, it can gently tap the surface while oscillating at high frequency, or it can be scanned just minutely above the surface. Image processing software allows easy extraction of useful surface parameters.
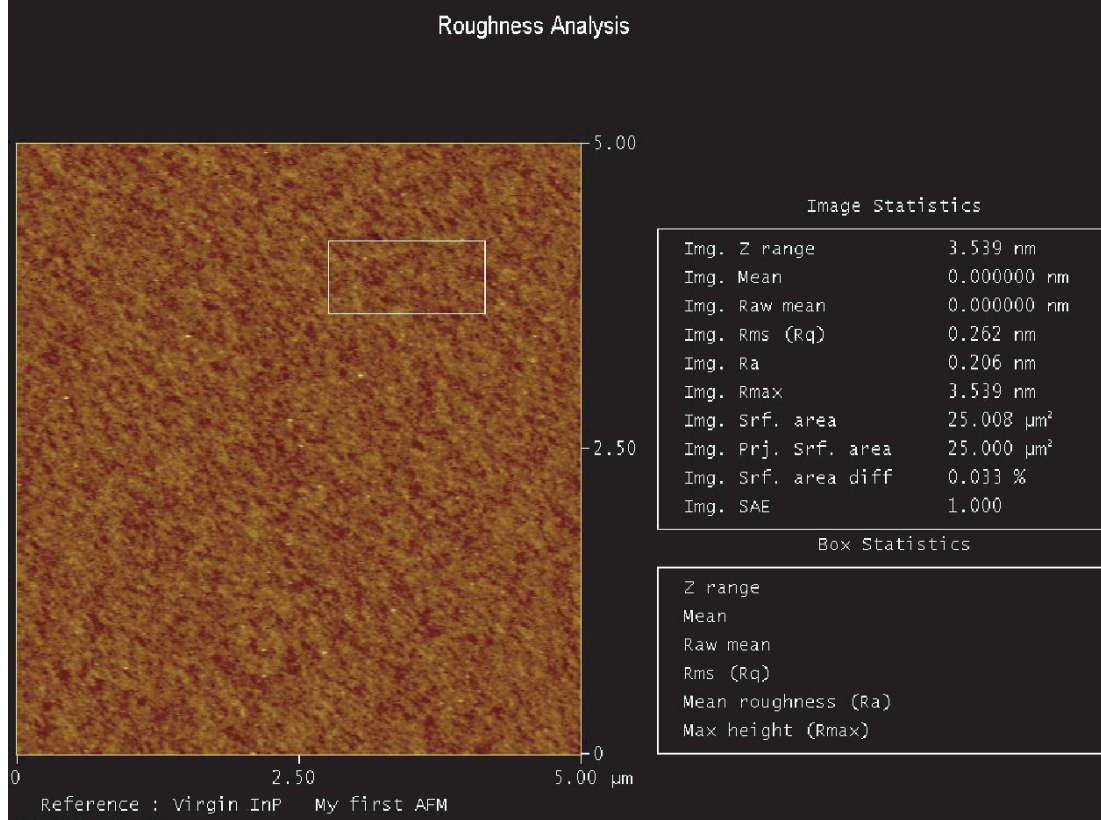
Figure A.3: AFM scan of SI InP substrate

Electrical properties such as mobility and sheet charge density are obtained from Hall measurements. The basic physical principle underlying the Hall effect [4] is the Lorentz force. When an electron current is(due to an applied Electric Field) in a direction perpendicular to an applied magnetic field, it experiences a force acting normal to both directions and moves in response to this force, resulting in an excess surface electrical charge on the side of the sample. This charge results in the transverse Hall voltage that can be measured. The sheet charge density can be extracted as

$$n_s = \frac{I \times B}{q \times |V_H|} \tag{A.0.2}$$

Thus, by measuring the Hall voltage V_H and from the known values of I, B, and q, one can determine the sheet density n_s of charge carriers in semiconductors. The Hall voltage is negative for n-type semiconductors and positive for p-type semi-

conductors. The sheet resistance RS of the semiconductor can be conveniently determined by use of the van der Pauw resistivity measurement technique [5]. Since sheet resistance involves both sheet density and mobility, one can determine the Hall mobility from the equation

$$\mu = \frac{1}{q n_s R_s} \qquad (A.0.2)$$

References

[1] W. Katz and J.G. Newman, "Fundamentals of Secondary Ion Mass Spectrometry", *Materials Research Society(MRS) Bulletin*, Vol 12., No. 6, Aug-Sep. 1987

[2] L. C. Feldman, J. W. Mayer, and S. T. Picraux, " Materials Analysis by Ion Channeling" Academic, New York, 1982

[3] G. Binnig, C.F. Quate, and C.H. Gerber, "Atomic force microscopy", *Physics Review Letters*, Vol. 56, pp. 930-933, 1986

[4] E. H. Hall, "On a New Action of the Magnet on Electrical Current", *American Journal of Math.* vol. 2, pp. 287-292, 1879

[5] L. J. Van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shapes", Philips Research Reports. 13, pp. 1-9, 1958

B

Implanted collector InP HBT / Circuit Process Flow

THIS appendix details the process flow for fabricating implanted collector InP DHBTs and circuits.

- The high temperature annealing steps are critical

    - Clean the quartz chamber in the RTA thoroughly with solvents. Clean the RTA chamber by flowing N_2 gas for atleast 1 hour just prior to actual anneal. Do atleast 2-3 dummy runs before actual anneal.

    - A very smooth Si_xN_y is very important for a defect free anneal. Clean the PECVD chamber for atleast 1 hour prior to deposition. When doing backside deposition, do not slide the wafer off the platen, and ensure that the platen is coated first with atleast 100 nm of Si_xN_y.

    - Pristine surface quality is to be maintained for all steps prior to growth. The wafer should always be handled at the edges with a clean tweezer. There should be absolutely no scratches on the wafer.

    - Any organics present on the wafer will give rise to pitting at the surface during anneal. The wafer should be very clean of PR and other organics before encapsulation with Si_xN_y.

- Extra precaution should be exercised when handling a 2 inch InP wafer.

    - Before spinning PR, always check the chuck vaccuum during spin with a dummy 2 inch GaAs wafer.

    - When placing clips on the wafer during sputtering or evaporation, make sure that they are not in the same direction from the major and minor flats (or the wafer will crack).

- Sometimes, the PR + a thick Si_xN_y implant mask will fail to resolve the alignment targets for local alignment in the GCA stepper. In this case, open windows over one set of alignment targets.

- The process tolerances are sensitive to the quality of the photoresist

    – If uncertain of the age and/or quality of the PR, pour a new bottle
    – This is especially important for SPR-518, SPR-510, SPR-955, CEM, and nLOF 2020

- When spinning PR, use a slow acceration

    – i.e. It should take $2 \rightarrow 2.5$ seconds to reach maximum spin speed

- For the following steps, a focus array is required for accurate features:

    1. Ni alignment targets lithography
    2. Pedestal implant lithography
    3. Emitter contact lithography
    4. Base contact lithography
    5. Base post lithography

    – Otherwise, the focus offset on subsequent steps is $= 0$
    – Always inspect the focus checkers thoroughly after development

- **Wafer orientation**

    – There are two type of wafers

        1. European / Japan flat option wafer where the minor flat is to the left of the major flat
        2. US flat option wafer where the minor flat is to the right of the major flat

    – To ensure proper semiconductor mesa etch undercut, the long-axis of the emitter should be oriented...

        * Perpendicular to the major flat for European / Japan flat option wafers
        * Parallel to the major flat for US flat option wafers

    – MBE growth can be performed only on full 2 inch InP wafers. The wafer is cleaved after growth

1. **Blanket Fe implant and anneal**

   - Ship the 2 inch SI epi-quality InP wafers for Fe implant. For implanted subcollector DHBTs, choose low energy-low dose implant as described in Chapter 4 . For the implanted pedestal-subcollector DHBTs, choose a higher energy (typically $\sim$ 150 keV) and higher fluence (1-3 $\times 10^{14}$ ions/cm^2). The implants are always carried out at 7° offset and at 200 $^\circ$C. This implant temperature is critical as described in Chapter 3 . Implant current should be maintained $\leq$ 50 μA.

   - Record N_s, K_s from ellipsometer

   - Deposition of Si_xN_y in the PECVD

     – Clean insides of PECVD with DI first, then ISO.
     – Perform 30 minutes clean of the PECVD and condition with Si_xN_y- use standard program
     – Surface preparation – 20 sec BHF + 2 min DI water rinse
     – Deposit 40 nm of Si_xN_y at 265 $^\circ$C on the wafer
     – Deposit 40 nm of Si_xN_y at 265 $^\circ$C on the platen
     – Prepare ozone reactor – run empty, 20 min
     – Surface Preparation for Si_xN_y deposition 1 – Oxidise wafer in uv Ozone for 120 sec
     – Surface Preparation for Si_xN_y deposition 2 – 30 sec clean in BHF, rinse in DI for 5 min
     – Deposit 40 nm of Si_xN_y on the top side
     – Solvent clean – 3 min 2-propanol, 3 min DI water rinse
     – Check quality of SiNx
     – If Si_xN_y looks rough or non uniform: remove in BHF for 10 min and rinse in running DI water for 5-10 min and repeat above steps from the uv Ozone. If Si_xN_y still looks rough, increase uv Ozone time to 200 sec
     – Deposit 100 nm of Si_xN_y on PECVD platen
     – Place wafer very, very gently with top side on platen. **Do not let it slide**
     – Deposit 40 nm of Si_xN_y on the back side

   - After 1h clean of RTA, run empty 700 $^\circ$C for 300s

   - Run actual wafer anneal at 700 $^\circ$C for 300s

   - Remove Si_xN_y cap by agitating in BHF for $\sim$ 10 min

- Rinse in running DI for 5 min

- Inspect under microscope to ensure that is no extensive pitting on the surface

- Record N_s, K_s using P270000 on Ellipsometer. When annealed fully, these should be same as for virgin SI InP substrate

2. **Alignment targets definition**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- HF clean – 5 min conc. HF:DI (10 ml: 200 ml), 5 min in running DI water

- Dehydration bake – 120°C, 10 min

- Cool wafer, 5 min

- Sputter TiW

  - Prepare sputter tool – load TiW source, TiW anode, TiW shims and W shield

  - Load wafer and after a quick pumpdown, ensure correct operation by turning on DC power and checking if plasma is light violet-blue

  - Ensure that the system pumps down to $\leq 3 \times 10^{-7}$T. At $\leq 1 \times 10^{-6}$ Torr, add LN_2 if necessary

  - RF back sputter for 2 min at 100 V

  - Sputter for 1-2 min at 200W with shutter closed

  - Open shutter and sputter on wafer for 30 min at 200W, for $\sim$ 350 nm of TiW

- Inspect under microscope

- Deposition of Si_xN_y in the PECVD

  - Clean insides of PECVD with DI first, then ISO.

  - Perform 30 minutes clean of the PECVD and condition with Si_xN_y- use standard program

  - Surface preparation – 20 sec BHF + 2 min DI water rinse

  - Deposit 40 nm of Si_xN_y at 265 °C on the wafer

- Lithography and for Ni metal liftoff

  - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

  - Photoresist spin – LOL-2000, 1 kRPM, 45 sec

- – Pre-exposure PR soft bake – 210 °C, 5 min
- – Photoresist spin – SPR-955-0.9CM, 3 kRPM, 30 sec
- – Pre-exposure PR bake – 95 °C, 1 min
- – Shoot 'Alignment Mark ' pattern in stepper, 0.9 sec
- – Post-exposure PR bake – 110°C, 60 sec
- – Develop in MF-701 developer, 60 sec
- – Rinse wafer – DI water for 2 min, N_2 dry
- – Inspect wafer using optical microscope

- Vent E-beam 4, load private source – Ni

- Allow system to pump-down for 90 min to $< 10^{-6}$ torr

- Deposit 300 Å of Ni at 1 Å/s

- Metal liftoff – 1165 stripper, 80°C, 2 hour

- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min

- Gently agitate sample surface with small pipet

- Rinse sample in 2-propanol before transferring to H_2O or Solvent clean

- If scum present, squirt with pipette and leave in PRX-127 (at ≥ 90 °C) for 15 min

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dry etch alignment targets

  - – Clean RIE_3 chamber with O_2/50 mT/500 V for 60 min
  - – Dry etch TiW with SF_6/Ar for 2.5/10 sccm, 20 mT, 100 V – Use laser monitor to determine stop time
  - – Over etch for 1 min 30 s
  - – Inspect under microscope
  - – Check height using profilometer

3. **Deposition of Si_xN_y as implant mask using the PECVD**
   The thickness of the Si_xN_y implant mask is determined by the implant conditions. Use TRIM and the discussion in this thesis to determine the thickness of Si_xN_y. For 350 keV Si implant, 140 nm of Si_xN_y is sufficient. Also load a GaAs dummy wafer along with actual wafer during all depositions

   - Clean insides of PECVD with DI first, then ISO.

   - Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Prepare ozone reactor – run empty, 20 min

- Surface Preparation for Si_xN_y deposition :1 – Oxidise wafer in uv Ozone for 200 sec

- Surface Preparation for Si_xN_y deposition :2 – 30 sec clean in BHF, rinse in DI for 5 min

- Deposit 40 nm of Si_xN_y on the wafer

- Check quality of SiNx. If Si_xN_y looks rough or non uniform: remove in BHF for 10 min and rinse in DI 5-10 min and repeat above steps from the uv Ozone. If Si_xN_y still looks rough, increase uv Ozone time to 300 sec

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and smooth, deposit 200 nm more of Si_xN_y on the wafer and the dummy GaAs

- Inspect under microscope

- Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and free of pinholes, deposit 400 nm more of Si_xN_y on the wafer and the dummy GaAs

- Inspect under microscope

- Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and free of pinholes, deposit 400 nm more of Si_xN_y on the wafer and the dummy GaAs

- Inspect under microscope

- Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and free of pinholes, deposit 400 nm more of Si_xN_y on the wafer and the dummy GaAs

- Record N_s, K_s using P270000 on Ellipsometer and calculate thickness from Filmetrics

4. **Subcollector Implant Mask lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-518, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90 °C, 60 sec
- Shoot 'Align Window' pattern in stepper, 0.7 sec – deliberately underexposed to not clear all photoresist over alignment targets
- Mini post-exposure PR bake – 90 °C, 10 sec
- Develop in MF-701 for 40 sec
- Rinse wafer – DI water for 20 sec, N_2 dry
- Inspect wafer using optical microscope and measure PR removed using profilometer
- Second pre-exposure PR bake – 90 °C, 20 sec
- Shoot 'Subcollector Implant' pattern in stepper, 1.0 sec
- Post-exposure PR bake – 105 °C, 10 sec
- Develop in MF-701 for 2 min
- Rinse wafer – DI water for 3 min sec, N_2 dry
- Inspect wafer using optical microscope and measure PR height profilometer

5. **Dry etch of Si_xN_y implant mask**

- uv flood expose wafer for 1 - 2 min
- Clean RIE_3 chamber with O_2 at 50 mT, 500 V for 60 min
- Place dummy real wafer and GaAs wafer with the same thickness of Si_xN_y in the chamber. Ensure that the laser strikes the center of the GaAs dummy wafer.
- Pump down to $\leq 9 \times 10^{-6}$ T. Dry etch using $CF_4 : O_2$, 20 : 2 sccm, 20 mT, 200 V. The etch rate is ≈ 400 Å / min
- Monitor reflected laser signal carefully. Not the time at which the etch has stopped, as indicated by a constant intensity of the reflected laser signal. Over etch for 2 min at 200 V, and then for 2 more min at 100 V.

- Inspect using optical microscope if Si_xN_y is removed fully wherever Si is to be implanted

- Measure height of PR + implant mask

- If Si_xN_y is uniform repeat dry etch with 1 min increments.

- uv flood expose wafer for 1 - 2 min

- Strip PR in conc. AZ-400K for 3 min

- Gently agitate sample surface with small pipet

- Rinse wafer – DI water for 2 min, N_2 dry

- If scum present, squirt with pipette and leave in PRX-127 (at $\geq$ 90 °C) for 15 min

- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

- Inspect wafer using optical microscope and measure thickness of Si_xN_y implant mask with the profilometer

- Carefully record misalignment of the subcollector implant pattern with the zero level targets over the entire wafer

- SEM subcollector implant patterns to measure actual dimensions of the subcollector implant windows

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dehydration bake – 120°C, 10 min

6. **Ship for Si subcollector implant**
   For implanted subcollector-pedestal implant, a multiple energy-fluence implant is performed to obtain $\sim 1 \times 10^{19}$ cm^{-3} over $\sim$ 400 - 500 nm for a low sheet resistance of the subcollector and a high surface doping. For implanted pedestal - subcollector process, Si implant is performed at 350 keV with a fluence of $\leq 6 \times 10^{14}$ ions/cm^2. Chapter 3 details the implant process.

7. **Post implant processing** – Si_xN_y (and Ni) removal

- Inspect wafers in the optical microscope and record misalignment again

- If scum present, squirt with pipette and leave in PRX-127 (at $\geq$ 90 °C) for 15 min

- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

- Prepare HF beakers – rinse thoroughly in DI and then breifly in BHF

- Agitate in 250 ml of HF continuously till Si_xN_y is seen to disappear and the wafer becomes colorless. Over etch for 10 min and ensure that no Si_xN_y remains

- Try to measure N_L, T_L of Si_xN_y on Ellipsometer – if Si_xN_y is fully gone, the reading will be in error

- Inspect wafers in the optical microscope and ensure that Si_xN_y is completely removed Also, ensure that Ni and Si_xN_y on top of TiW alignment targets are completely removed

- if Ni is not fully removed, repeat BHF wet etch with constant agitation in 5 min increments

- Measure height of alignment targets profilometer. Check profile across the implanted regions – there should be less than ~ 50 Å variation

8. **High temperature anneal**

- Record N_s, K_s of the InP wafer using P270000 on Ellipsometer

- Deposition of Si_xN_y in the PECVD

  – Clean insides of PECVD with DI first, then ISO.
  – Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program
  – Surface preparation – 20 sec BHF + 2 min DI water rinse
  – Deposit 40 nm of Si_xN_y at 265 °C on the wafer
  – Deposit 40 nm of Si_xN_y at 265 °C on the platen
  – Prepare ozone reactor – run empty, 20 min
  – Surface Preparation for Si_xN_y deposition 1 – Oxidise wafer in uv Ozone for 100 sec
  – Surface Preparation for Si_xN_y deposition 2 – 30 sec clean in BHF, rinse in DI for 5 min
  – Deposit 40 nm of Si_xN_y on the top side
  – Solvent clean – 3 min 2-propanol, 3 min DI water rinse
  – Check quality of SiNx
  – If Si_xN_y looks rough or non uniform: remove in BHF for 10 min and rinse in running DI water for 5-10 min and repeat above steps from the uv Ozone. If Si_xN_y still looks rough, increase uv Ozone time to 150 sec
  – Deposit 100 nm of Si_xN_y on PECVD platen

- – Place wafer very, very gently with top side on platen. **Do not let it slide**
- – Deposit 40 nm of Si_xN_y on the back side

- After 1h clean of RTA, run empty 800 °C for 30 sec, twice

- For implanted subcollector process, run actual wafer anneal at 800 °C for 30 sec
  For implanted subcollector-pedestal process, run actual wafer anneal at 600 °C for 10 sec

- Remove Si_xN_y cap by agitating in BHF for $\sim$ 10 min

- Rinse in running DI for 5 min

- Inspect under microscope to ensure that is no extensive pitting on the surface

- Record N_s, K_s of the wafer using P270000 on Ellipsometer. When annealed fully, these should be same as for virgin SI InP substrate

For a implanted subcollector process, proceed straight to surface preparation in step 15.
For implanted subcollector-pedestal process, proceed to next step which is definition of Si_xN_y mask for pedestal implant

9. **Deposition of Si_xN_y as pedestal implant mask using the PECVD**
   The thickness of the Si_xN_y implant mask is determined by the implant conditions. Use TRIM and the discussion in this thesis to determine the thickness of Si_xN_y. For 100 keV Si implant, 80 nm of Si_xN_y is sufficient. Also load a GaAs dummy wafer along with actual wafer during all depositions

   - Clean insides of PECVD with DI first, then ISO.

   - Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

   - Prepare ozone reactor – run empty, 20 min

   - Surface Preparation for Si_xN_y deposition :1 – Oxidise wafer in uv Ozone for 200 sec

   - Surface Preparation for Si_xN_y deposition :2 – 30 sec clean in BHF, rinse in DI for 5 min

   - Deposit 40 nm of Si_xN_y on the wafer

- Check quality of SiNx. If Si_xN_y looks rough or non uniform: remove in BHF for 10 min and rinse in DI 5-10 min and repeat above steps from the uv Ozone. If Si_xN_y still looks rough, increase uv Ozone time to 300 sec

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and smooth, deposit 200 nm more of Si_xN_y on the wafer and the dummy GaAs

- Inspect under microscope

- Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and free of pinholes, deposit 300 nm more of Si_xN_y on the wafer and the dummy GaAs

- Inspect under microscope

- Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- If Si_xN_y is uniform and free of pinholes, deposit 400 nm more of Si_xN_y on the wafer and the dummy GaAs

- Inspect under microscope

- Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program

- Solvent clean – 3 min 2-propanol, 3 min DI water rinse

- Record N_s, K_s using P270000 on Ellipsometer and calculate thickness from Filmetrics

10. **Pedestal Implant lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dehydration bake – 120°C, 10 min

- Cool wafer, 5 min

- Photoresist spin – SPR-510, 3 kRPM, 30 sec

- Pre-exposure PR bake – 90 °C, 60 sec

- Shoot 'Pedestal Implant' pattern in stepper, 1.4 sec

- Post-exposure PR bake – 105 °C, 10 sec

- Develop in MF-701 for 2 min

- Rinse wafer – DI water for 3 min sec, N_2 dry

- Inspect wafer using optical microscope. If misalignment to ZLTs is more than 0.1 μm, repeat lithography

11. **Dry etch of Si_xN_y implant mask**

- uv flood expose wafer for 1 - 2 min

- Clean RIE_3 chamber with O_2 at 50 mT, 500 V for 60 min

- Place dummy real wafer and GaAs wafer with the same thickness of Si_xN_y in the chamber. Ensure that the laser strikes the center of the GaAs dummy wafer.

- Pump down to $\leq 9{\times}10^{-6}$ T. Dry etch using CF_4 : O_2, 20 : 2 sccm, **10 mT**, 200 V. The etch rate is ≈ 400 Å / min

- Monitor reflected laser signal carefully. Not the time at which the etch has stopped, as indicated by a constant intensity of the reflected laser signal. Over etch for 2 min at 200 V, and then for 2 more min at 100 V.

- Inspect using optical microscope if Si_xN_y is removed fully wherever Si is to be implanted

- Measure height of PR + implant mask

- If Si_xN_y is uniform repeat dry etch with 1 min increments.

- uv flood expose wafer for 1 - 2 min

- Strip PR in conc. AZ-400K for 3 min

- Gently agitate sample surface with small pipet

- Rinse wafer – DI water for 2 min, N_2 dry

- If scum present, squirt with pipette and leave in PRX-127 (at ≥ 90 °C) for 15 min

- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

- Inspect wafer using optical microscope and measure thickness of Si_xN_y implant mask with the profilometer

- Carefully record misalignment of the pedestal implant pattern with the zero level targets over the entire wafer

- SEM pedestal implant patterns to measure actual dimensions of the window

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dehydration bake – 120°C, 10 min

12. **Ship for Si pedestal implant**
For implanted subcollector-pedestal implant, a multiple energy-fluence implant is performed to obtain $\sim 1\times10^{19}$ cm^{-3} over the existing Fe doping. Chapter 5 details the implant conditions.

13. **Post implant processing** – Si_xN_y (and Ni) removal

- Inspect wafers in the optical microscope and record misalignment again

- If scum present, squirt with pipette and leave in PRX-127 (at ≥ 90 °C) for 15 min

- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

- Prepare HF beakers – rinse thoroughly in DI and then breifly in BHF

- Agitate in 250 ml of HF continuously till Si_xN_y is seen to disappear and the wafer becomes colorless. Over etch for 10 min and ensure that no Si_xN_y remains

- Try to measure N_L, T_L of Si_xN_y on Ellipsometer – if Si_xN_y is fully gone, the reading will be in error

- Inspect wafers in the optical microscope and ensure that Si_xN_y is completely removed.

- Measure height of alignment targets profilometer. Check profile across the implanted regions – there should be less than ~ 50 Å variation

14. **High temperature anneal**

- Record N_s, K_s of the InP wafer using P270000 on Ellipsometer

- Deposition of Si_xN_y in the PECVD
    - Clean insides of PECVD with DI first, then ISO.
    - Perform 30 minutes clean of the PECVD and condition with Si_xN_y– use standard program
    - Surface preparation – 20 sec BHF + 2 min DI water rinse
    - Deposit 40 nm of Si_xN_y at 265 °C on the wafer

- Deposit 40 nm of Si_xN_y at 265 °C on the platen
- Prepare ozone reactor – run empty, 20 min
- Surface Preparation for Si_xN_y deposition 1 – Oxidise wafer in uv Ozone for 100 sec
- Surface Preparation for Si_xN_y deposition 2 – 30 sec clean in BHF, rinse in DI for 5 min
- Deposit 40 nm of Si_xN_y on the top side
- Solvent clean – 3 min 2-propanol, 3 min DI water rinse
- Check quality of SiNx
- If Si_xN_y looks rough or non uniform: remove in BHF for 10 min and rinse in running DI water for 5-10 min and repeat above steps from the uv Ozone. If Si_xN_y still looks rough, increase uv Ozone time to 150 sec
- Deposit 100 nm of Si_xN_y on PECVD platen
- Place wafer very, very gently with top side on platen. **Do not let it slide**
- Deposit 40 nm of Si_xN_y on the back side

- After 1h clean of RTA, run empty 800 °C for 30 sec, twice

- Run actual wafer anneal at 800 °C for 30 sec

- Remove Si_xN_y cap by agitating in BHF for $\sim$ 10 min

- Rinse in running DI for 5 min

- Inspect under microscope to ensure that is no extensive pitting on the surface

- Record N_s, K_s of the wafer using P270000 on Ellipsometer. When annealed fully, these should be same as for virgin SI InP substrate

If the alignment targets are stable, the wafers are ready for growth.

15. **Surface preparation**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Prepare ozone reactor – run empty, 20 min
- Surface preparation 1 – oxidize wafer surface in ozone reactor, 10 min
- Surface preparation 2 – conc. HF:DI water 5 ml:200 ml for 5 min
- Surface preparation 3 – Rinse in running DI water for 5 min
- Load sample **immediately** in the MBE chamber

MBE growth of drift collector, base, emitter layers. RHEED is continuosly monitored to ensure that the growth is excellent

16. **Wafer preparation for emitter lithography** – wet etch of semiconductor over TiW alignment targets

   - Inspect wafer in the SEM

   - Inspect wafer under the optical microscope. For the GCS stepper, alignment marks after regrowth are not resolved by the DFAS local alignment system. The layers on top of the alignment targets have to be removed

   - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

   - Dehydration bake – 120°C, 10 min

   - Cool wafer, 5 min

   - Photoresist spin – SPR-510, 4 kRPM, 30 sec

   - Pre-exposure PR bake – 90 °C, 60 sec

   - Shoot 'Align window' pattern in stepper, 1.4 sec

   - Post-exposure PR bake – 105 °C, 10 sec

   - Develop in MF-701 for 2 min

   - Rinse wafer – DI water for 3 min sec, N_2 dry

   - Inspect wafer using optical microscope

   - Prepare two beakers with...

      (a) H_3PO_4:DI water$_2$:DI water, 1:1:25 – use stirrer at 200 RPM
      (b) H_3PO_4:HCl, 4:1 – use stirrer at 200 RPM

   - Etch InGaAs emitter cap in H_3PO_4:H_2O_2:DI water $\approx$ 25 sec

   - Inspect under microscope and check in profilometer to ensure all InGaAs is etched

   - Etch InP emitter in H_3PO_4:HCl $\approx$ 40 sec

   - Inspect under microscope and check in profilometer to ensure all InP is etched

   - Etch InGaAs base in H_3PO_4:DI water$_2$:DI water $\approx$ 40 sec

   - Inspect under microscope and check in profilometer to ensure all InGaAs is etched

   - PR removal

- – Place sample in 1165 PR stripper, 80°C, 1 hour
- – Gently agitate sample surface with small pipet
- – Rinse sample in 2-propanol before transferring to DI water or Solvent clean
- – If scum is present, squirt gently in AZ-300T PR stripper, 80°C, 15 min
- – Rinse sample in 2-propanol before transferring to DI water or Solvent clean
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

17. **Wafer cleaving**

- For the local-alignment DFAS (Dark-Field-Alignment-System) system to work on the i-line GCA stepper, the minimum size of the sample to be processed should be greater than 1 x 1 inch^2.
- Cleave into 4 quarters carefully along the boundary of a die.

18. **Emitter contact lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-955, 2.5 kRPM, 30 sec
- Pre-exposure PR bake – 92 °C, 60 sec
- CEM coat and spin
    - – Coat wafer w/ CEM and let sit for 60 sec
    - – Then spin 4 kRPM, 30 sec
- Shoot 'emitter' pattern in stepper, 2.055 sec
- Post-exposure PR bake – 110 °C, 60 sec
- Development
    - (a) Rinse CEM from wafer surface using DI water, 30 sec
    - (b) Immediately transfer wafer to MF-701 developer
        - – Develop for 2 min 20 sec
- Rinse wafer – DI water for 2 min, N$_2$ dry
- Inspect wafer using optical microscope. Misalignment to pedestal should be ≤ 0.05 μm

19. **Emitter contact deposition**

- Prepare ozone reactor – run empty, 20 min

- Surface preparation – oxidize wafer surface in ozone reactor, 10 min

- Vent E-beam 4, load private sources – Ti, Pd, and Au

- Surface preparation – HCl:DI water 1:10 dip 10 sec, DI water rinse 10 sec, N_2 dry

- Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4

- Allow system to pump-down for 90 min to $< 10^{-6}$ torr

- Deposit emitter contact

  - Ti 200 Å (1 Å/sec)
  - Pd 400 Å (1 Å/sec)
  - Au 7500 Å
    * 1 Å/sec for 1-300 Å
    * 2 Å/sec for 301-500 Å
    * 3 Å/sec for 501-1000 Å
    * 4-5 Å/sec 1001-7500 Å

- Metal liftoff – 1165 stripper, 80 °C, 2 hour

- Remove metal and place sample in fresh 1165 stripper, 80 °C, 20 min

  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Anneal emitter contact, 300 °C, N_2 purge, 60 sec

20. **Emitter mesa etch**

- Prepare three beakers with...

  (a) NH_4OH:DI water, 1:10
  (b) H_3PO_4:H_2O_2:DI water, 1:1:25 – use stirrer at 200 RPM
  (c) H_3PO_4:HCl, 4:1 – use stirrer at 200 RPM

- Dip sample – NH_4OH:DI water solution 10 sec, DI water rinse 10 sec, N_2 dry

- Etch InGaAs emitter cap in H_3PO_4:H_2O_2:DI water $\approx$ 21 sec
  - Overetch should only be 3 sec from the time the color change is complete
  - Inspect under microscope to ensure all InGaAs is etched
- Etch InP emitter in H_3PO_4:HCl $\approx$ 35 sec
  - Overetch should only be 5 sec from the time the color change is complete
  - Inspect under microscope to ensure all InP is etched

21. **Base contact lithography**

- No solvent cleaned needed after emitter mesa etch
- Dehydration bake – 120°C, 10 min
- Photoresist spin – nLOF 2020, 4 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot 'base contact' pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

22. **Base contact deposition**

- Prepare ozone reactor – let run empty for 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Vent E-beam 4, load private sources – Ti, Pd, and Au
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit base contact
  - Pd 25 Å, Ti 170 Å, Pd 170 Å, Au 650 Å
    - 1 Å/sec for all metal depositions

        ∗ Higher deposition rates onto nLOF 2020 will leave more PR scum

- Metal liftoff – 1165 stripper, 80°C, 1 hour
- Remove metal and place sample in fresh AZ 300T stripper, 80°C, 10 min
    - Gently agitate sample surface with small pipet
    - Rinse sample in 2-propanol before transferring to DI water or Solvent clean
    - The sample can proceed to 'base-post' lithography if there is no scum on post-end of the base contact
        - ∗ Otherwise, repeat the AZ 300T step until that is the case

23. **Base post lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120°C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-955, 2.5 kRPM, 30 sec
- Pre-exposure PR bake – 92°C, 60 sec
- CEM coat and spin
    - Coat wafer w/ CEM and let sit for 60 sec
    - Then spin 4 kRPM, 30 sec
- Shoot 'base post' pattern in stepper, 2.055 sec
- Post-exposure PR bake – 110°C, 60 sec
- Development
    (a) Rinse CEM from wafer surface using DI water, 30 sec
    (b) Immediately transfer wafer to MF-701 developer, develop 2 min 20 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

24. **Base post deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Vent E-beam 4, load private sources – Ti, Pd, and Au

- Surface preparation – HCl:DI water 1:10 dip 10 sec, DI water rinse 10 sec, N_2 dry

- Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4

- Allow system to pump-down for 90 min to $< 10^{-6}$ torr

- Deposit base post

  - Pd 25 Å (1 Å/sec)
  - Ti 170 Å (1 Å/sec)
  - Pd 170 Å (1 Å/sec)
  - Au 9300 Å
    - ∗ 1 Å/sec for 1-300 Å
    - ∗ 2 Å/sec for 301-500 Å
    - ∗ 3 Å/sec for 501-1000 Å
    - ∗ 4-5 Å/sec 1001-9300 Å

- Metal liftoff – 1165 stripper, 80°C, 2 hour

- Remove metal and place sample in fresh 1165 stripper, 80°C, 20 min

  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

25. **Base mesa lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dehydration bake – 120°C, 10 min

- Cool wafer, 5 min

- Gently pipette SPR-510 onto the wafer and let it sit for 20-30 sec

- Photoresist spin – SPR-510, 4 kRPM, 30 sec

- Pre-exposure PR bake – 90°C, 60 sec

- Shoot 'base mesa' pattern in stepper, 1.0 sec

- Post-exposure PR bake – 110°C, 60 sec

- Development – MF-701 developer, 90 sec

- Rinse wafer – DI water for 2 min, N_2 dry

- Inspect wafer using optical microscope

26. **Base mesa etch**

   - Prepare three beakers with...
     (a) NH$_4$OH:DI water, 1:10
     (b) H$_3$PO$_4$:H$_2$O$_2$:DI water, 1:1:25 – use stirrer at 200 RPM
     (c) H$_3$PO$_4$:HCl, 4:1 – use stirrer at 200 RPM
   - Dip sample – NH$_4$OH:DI water solution 10 sec, DI water rinse 10 sec, N$_2$ dry
   - Etch InGaAs base, InGaAs collector setback, and ternary grade in H$_3$PO$_4$:H$_2$O$_2$:DI water $\approx$ 35 sec
     – Overetch should only be 5 sec from the time the color change is complete
     – Inspect under microscope to ensure all InGaAs is etched
   - Etch InP collector in H$_3$PO$_4$:HCl $\approx$ 35 sec
     – Overetch should only be 10 sec from the time the color change is complete
     – This extended overetch is for increased collector semiconductor undercut
     – Inspect under microscope to ensure all InP is etched
   - Strip PR mask – 1165 stripper, 80 °C, 20 min
     – Gently agitate sample surface with small pipet
     – Rinse sample in 2-propanol before transferring to DI water or Solvent clean

27. **NiCr Resistor lithography**

   - Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
   - Dehydration bake – 120°C, 10 min
   - Cool wafer, 5 min
   - Photoresist spin – SPR-510, 4 kRPM, 30 sec
   - Pre-exposure PR bake – 90 °C, 60 sec
   - CEM coat and spin
     – Coat wafer w/ CEM and let sit for 60 sec
     – Then spin 4 kRPM, 30 sec
   - Shoot 'Resistor' pattern in stepper, 2.2 sec

- Post-exposure PR bake – 110 °C, 60 sec
- Development
  (a) Rinse CEM from wafer surface using DI water, 30 sec
  (b) Immediately thereafter transfer wafer to MF-701 developer, develop 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

28. **NiCr Resistor deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 90 sec
- Vent E-beam 1, load private sources – Ti, SiO_2, NiCr
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 1
- Allow system to pump-down for 60 min to $< 2 \cdot 10^{-6}$ torr
- Deposit NiCr resistors
  - Ti 50 Å (1 Å/sec)
  - SiO_2 200 Å (1 Å/sec)
  - NiCr xxx Å (1 Å/sec)
    * For NiCr, Cr out-diffuses more quickly than than Ni
    * Thus, the source resistivity goes down after each deposition
    * Refer to the NiCr worksheet for accurate determination of NiCr deposition thickness for 50 $\Omega/\square$
- Metal liftoff – 1165 stripper, 80 °C, 2 hour
- Remove metal and place sample in fresh 1165 stripper, 80 °C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

29. **Collector contact lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120 °C, 10 min

- Photoresist spin – nLOF 2020, 3.5 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot 'collector contact' pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

30. **Collector contact deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 90 sec
  - Do not run sample any longer in the ozone reactor
  - Longer ashing will remove PR from above the emitter contact *and* oxidize too much of the InGaAs sub-collector contact layer
- Vent E-beam 4, load private sources – Ti, Pd, and Au
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter in the same direction as the sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit collector contact
  - Ti 200 Å (1 Å/sec)
  - Pd 400 Å (1 Å/sec)
  - Au 4500 Å
    * 1 Å/sec for 1-300 Å
    * 2 Å/sec for 301-500 Å
    * 3 Å/sec for 501-1000 Å
    * 4 Å/sec 1001-4500 Å
- Metal liftoff – 1165 stripper, 80 °C, 2 hour
- Remove metal and gently agitate in fresh AZ 300T stripper, 80 °C, 10 min
- Rinse in 2-propanol before transferring to DI water or Solvent clean

31. **Collector post lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120 °C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-518, 3.0 kRPM, 30 sec
- Pre-exposure PR bake – 90 °C, 60 sec
- CEM coat and spin – coat wafer w/ CEM and let sit for 60 sec, then spin 4 kRPM, 30 sec
- Shoot 'collector post' pattern in stepper, 2.6 sec
- Post-exposure PR bake – 110 °C, 60 sec
- Development
  (a) Rinse CEM from wafer surface using DI water, 30 sec
  (b) Immediately transfer wafer to MF-701 developer, develop 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

32. **Collector post deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – HCl:DI water 1:10 dip 10 sec, DI water rinse 10 sec, N_2 dry
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit collector post
  - Ti 100 Å (1 Å/sec)
  - Au xxxx Å (see list below for deposition rate)
    * The collector post needs to be level with the top of the emitter contact
    * Dektak to determine Au deposition thickness

  * ∗ 1 Å/sec for 1-300 Å
  * ∗ 2 Å/sec for 301-500 Å
  * ∗ 3 Å/sec for 501-1000 Å
  * ∗ 4-5 Å/sec 1001-xxxx Å
  – Ti 100 Å (1 Å/sec)
- Metal liftoff – 1165 stripper, 80 °C, 2 hour
- Remove metal and place sample in fresh 1165 stripper, 80 °C, 20 min

  – Gently agitate sample surface with small pipet
  – Rinse sample in 2-propanol before transferring to DI water or Solvent clean

33. **Resistor post lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120 °C, 10 min
- Cool wafer, 5 min
- Photoresist spin – SPR-518, 3.0 kRPM, 30 sec
- Pre-exposure PR bake – 90 °C, 60 sec
- CEM coat and spin – coat wafer w/ CEM and let sit for 60 sec, then spin 4 kRPM, 30 sec
- Shoot 'resistor post' pattern in stepper, 2.6 sec
- Post-exposure PR bake – 110 °C, 60 sec
- Development
  (a) Rinse CEM from wafer surface using DI water, 30 sec
  (b) Immediately transfer wafer to MF-701 developer, develop 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

34. **Resistor post deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au

- Surface preparation – HCl:DI water 1:10 dip 10 sec, DI water rinse 10 sec, N_2 dry

- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4

- Allow system to pump-down for 90 min to $< 10^{-6}$ torr

- Deposit resistor post contact

  - Ti 100 Å (1 Å/sec)
  - Au xxxx Å (see list below for deposition rate)
    - $*$ The resistor post needs to level with the top of the emitter contact
    - $*$ Dektak to determine Au deposition thickness
    - $*$ 1 Å/sec for 1-300 Å
    - $*$ 2 Å/sec for 301-500 Å
    - $*$ 3 Å/sec for 501-1000 Å
    - $*$ 4-5 Å/sec 1001-xxxx Å
  - Ti 100 Å (1 Å/sec)

- Metal liftoff – 1165 stripper, 80 °C, 2 hour

- Remove metal and place sample in fresh 1165 stripper, 80 °C, 20 min

  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

35. **BCB passivation**

- The 'Blue Oven' must be at room temperature 25°C or less before beginning

  - Otherwise, BCB will bubble during the cure and the sample will be ruined

- NOTE: there must not be any stops in the steps from sample surface preparation to loading the spun sample w/ BCB into the Blue oven

  - Any delays will allow increased surface oxide to regenerate on the semiconductor, increasing leakage currents
  - Oxygen contaminates BCB and prolonged exposure will compromise the cure and ruin the sample

- Prepare the 'Blue Oven' – run N_2 through chamber at 100%

- Prepare ozone reactor – run empty, 20 min
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120 °C, 10 min
- Cool wafer, 5 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, **NO WATER RINSE**
- Coat wafer with BCB 3022-35 – let sit on surface for 30 sec
- Spin BCB 1.5 kRPM, 30 sec – BCB thickness $\approx 1.88\ \mu$m
- Place sample into Al cup holder
    - The holder should be deformed such that the sample is completely level, yet has minimal contact with the bottom holder surface
    - Otherwise, cured BCB that has crept onto the bottom surface may prevent the sample from being removed from the holder
- Place sample (in holder) into the 'Blue Oven'
- Reduce N_2 flow to 60% after 3 min
- Load and run Program 5 (confirm in case it has been altered)
- Program sequence:
    (a) 5 min ramp to 50 °C, 5 min soak
    (b) 15 min ramp to 100 °C, 15 min soak
    (c) 15 min ramp to 150 °C, 15 min soak
    (d) 60 min ramp to 250 °C, 60 min soak
    (e) Natural cool down
    (f) Oven off
- Remove sample and inspect under the microscope
- Turn off the 'Blue Oven'

36. **Wafer planarization and interconnect surface preparation**

- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
    (a) Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 2 min
    (b) Inspect sample in FEI SEM to see if the device contacts and interconnect posts are exposed
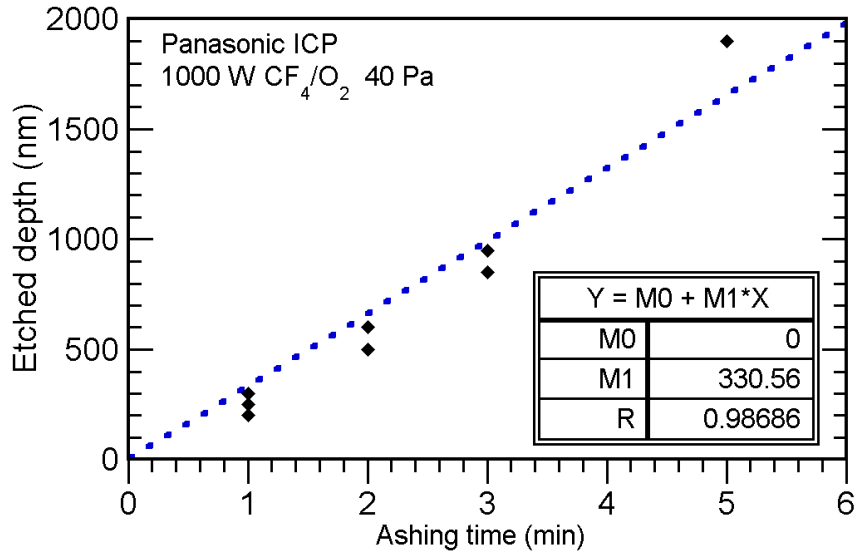
Figure B.1: BCB etch rate for the given CF_4/O_2 recipe

- Repeat the above etch (1 min increments) and inspection until all contact and posts are exposed
  - Be sure to run the wafer clean program in between each etch cycle
- Repeat the BCB passivation step for further sample planarization
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
  - (a) Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 3 min 30 sec
  - (b) Inspect sample in FEI SEM to see if the device contacts and interconnect post are exposed
- Repeat the above etch (1 min increments) and inspection until all contact and posts are exposed
  - Be sure to run the wafer clean program in between each etch cycle
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120 °C, 10 min
- Cool wafer, 5 min
- Prepare ozone reactor – run empty, 20 min
- Surface preparation – oxidize wafer surface in ozone reactor, 10 min

- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, **NO WATER RINSE**
- Deposit 100 nm SiN_x on the BCB surface by PECVD
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90 °C, 60 sec
- Shoot 'contact via' pattern in stepper, 2.0 sec
- Post-exposure PR bake – 110 °C, 60 sec
- Development – MF-701 developer, 90 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
- Load sample on carrier wafer for ICP etching
  - (a) SiN_x ICP etch CF_4 125 sccm, 90 sec
  - (b) Short BCB ashing CF_4/O_2 50:200 sccm, 10 sec
- Inspect sample in FEI SEM to see if the device contacts and interconnect posts are exposed
- Strip photoresist mask
  - (a) Flood expose sample, 15 sec
  - (b) Develop exposed PR – MF-701, 2 min
  - (c) Strip remaining PR in acetone – 3 min
  - (d) Inspect – if PR remaining, use 1165 stripper, 80 °C, 3 min
  - (e) Gently agitate sample surface with small pipet
- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

37. **Metal-1 interconnect lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120 °C, 10 min
- Photoresist spin – nLOF 2020, 4 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot 'Metal 1' pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec

- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

38. **Metal-1 interconnect deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit Metal-1 interconnect
  - Ti 100 Å (1 Å/sec)
  - Au 10 kÅ
    - ∗ 2 Å/sec for 1-300 Å
    - ∗ 3 Å/sec for 301-500 Å
    - ∗ 4 Å/sec for 501-1000 Å
    - ∗ 5-6 Å/sec 1001-10000 Å
  - Ti 100 Å (1 Å/sec)
- Metal liftoff – AZ 300T stripper, 80 °C, 20 min
- Remove metal and place sample in fresh AZ 300T stripper, 80 °C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

39. **Measure devices and TLMs**

- If device performance and TLMs are well behaved, continue

40. **SiN MIM capacitor formation**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dehydration bake 120 °C, 10 min

- Cool wafer, 5 min

- Prepare ozone reactor – run empty, 20 min

- Surface preparation – oxidize wafer surface in ozone reactor, 10 min

- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***

- Deposit 400 nm SiN_x onto the sample by PECVD

- Photoresist spin – SPR-510, 4 kRPM, 30 sec

- Pre-exposure PR bake – 90 °C, 60 sec

- Shoot 'SiN cap' pattern in stepper, 2.0 sec

- Post-exposure PR bake – 110 °C, 60 sec

- Development – MF-701 developer, 90 sec

- Rinse wafer – DI water for 2 min, N_2 dry

- Inspect wafer using optical microscope

- Clean carrier wafer in Panasonic ICP – CF_4/O_2 200:40 sccm, 7 min

- Load sample on carrier wafer for ICP etching

  (a) SiN_x ICP etch CF_4 125 sccm, 3 min
  (b) Short ashing CF_4/O_2 50:200 sccm, 15 sec

- Strip photoresist mask

  (a) Flood expose sample, 15 sec
  (b) Develop exposed PR – MF-701, 2 min
  (c) Strip remaining PR in acetone – 3 min
  (d) Inspect – if PR remaining, use 1165 stripper, 80 °C, 3 min
  (e) Gently agitate sample surface with small pipet

- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

41. **Metal-2 interconnect lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse

- Dehydration bake – 120 °C, 10 min

- Photoresist spin – nLOF 2020, 3 kRPM, 30 sec

- Pre-exposure PR bake – 111°C, 60 sec

- Shoot 'Metal 2' pattern in stepper – 0.46 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

42. **Metal-2 interconnect deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit Metal-2 interconnect
  - Ti 100 Å (1 Å/sec)
  - Au 10 kÅ
    * 2 Å/sec for 1-300 Å
    * 3 Å/sec for 301-500 Å
    * 4 Å/sec for 501-1000 Å
    * 5-6 Å/sec 1001-10000 Å
  - Ti 100 Å (1 Å/sec)
- Metal liftoff – 1165 stripper, 80 °C, 2 hour
- Remove metal and place sample in fresh 1165 stripper, 80 °C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

43. **Metal-2 to Metal-3 interconnect post lithography – 1**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120 °C, 10 min
- Photoresist spin – SPR 518, 3 kRPM, 30 sec

- Pre-exposure PR bake – 90 °C, 60 sec
- CEM coat and spin
    - Coat wafer w/ CEM and let sit for 60 sec
    - Then spin 4 kRPM, 30 sec
- Shoot 'M2 - M3 post' pattern in stepper – 2.8 sec
- Post-exposure PR bake – 110 °C, 60 sec
- Development – MF-701 developer, 2 min 30 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

44. **Metal-2 to Metal-3 interconnect post deposition – 1**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4
- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit M2-M3 post contact
    - Ti 100 Å (1 Å/sec)
    - Au 13 kÅ
        * 2 Å/sec for 1-300 Å
        * 3 Å/sec for 301-500 Å
        * 4 Å/sec for 501-1000 Å
        * 5-6 Å/sec 1001-13000 Å
    - Ti 100 Å (1 Å/sec)
- Metal liftoff – 1165 stripper, 80 °C, 30 min
- Remove metal and place sample in fresh 1165 stripper, 80 °C, 10 min
    - Gently agitate sample surface with small pipet
    - Rinse sample in 2-propanol before transferring to DI water or Solvent clean

45. **Thin-film BCB microstrip wiring envirnment – layer 1**

- The 'Blue Oven' must be at room temperature $25°C$ or less before be-ginning
    - Otherwise, BCB will bubble during the cure and the sample will be ruined
- NOTE: there must not be any stops in the steps from sample surface preparation to loading the spun sample w/ BCB into the Blue oven
    - Any delays will allow increased surface oxide to regenerate on the surface, increasing leakage currents
    - Oxygen contaminates BCB and prolonged exposure will compro-mise the cure and ruin the sample
- Prepare the 'Blue Oven' – run N_2 through chamber at 100%
- Prepare ozone reactor – run empty, 20 min
- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120 °C, 10 min
- Cool wafer, 5 min
- Surface preparation – clean wafer surface in ozone reactor, 10 min
- Surface preparation – $NH_4OH:DI$ water 1:10 dip 10 sec, N_2 dry, *NO WATER RINSE*
- Coat wafer with BCB 3022-35 – let sit on surface for 30 sec
- Spin BCB 1.5 kRPM, 30 sec – BCB thickness ≈ 1.88 μm
- Place sample into Al cup holder
    - The holder should be deformed such that the sample is completely level, yet has minimal contact with the bottom holder surface
    - Otherwise, cured BCB that has crept onto the bottom surface may prevent the sample from being removed from the holder
- Place sample (in holder) into the 'Blue Oven'
- Reduce N_2 flow to 60% after 3 min
- Load and run Program 5 (see passivation step)
- Remove sample and inspect under the microscope
- Turn off the 'Blue Oven'
- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min

    (a) Load sample on carrier wafer, BCB ICP etch CF_4/O_2 50:200 sccm, 90 sec

    (b) Inspect sample in FEI SEM to see if the interconnect posts are exposed

- Repeat the above etch (45 sec increments) and inspection until all contact and posts are exposed

    – Be sure to run the wafer clean program in between each etch cycle

46. **Metal-2 to Metal-3 interconnect post lithography – 2**

- Repeat this step

47. **Metal-2 to Metal-3 interconnect post deposition – 2**

- Repeat this step

48. **Thin-film BCB microstrip wiring envirnment – layer 2**

- Repeat this step

49. **Metal-3 adhession layer**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake 120 °C, 10 min
- Cool wafer, 5 min
- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 10 min
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Deposit 100 nm SiN_x on the BCB surface by PECVD
- Photoresist spin – SPR-510, 4 kRPM, 30 sec
- Pre-exposure PR bake – 90 °C, 60 sec
- Shoot 'Metal-3 via' pattern in stepper, 2.0 sec
- Post-exposure PR bake – 110 °C, 60 sec
- Development – MF-701 developer, 90 sec
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

- Clean carrier wafer in Panasonic ICP – CF_4/O_2 50:200 sccm, 7 min
- Load sample on carrier wafer for ICP etching
    (a) SiN_x ICP etch CF_4 125 sccm, 90 sec
    (b) Short BCB ashing CF_4/O_2 50:200 sccm, 10 sec
- Inspect sample in FEI SEM to see if the interconnect posts are exposed
- Strip photoresist mask
    (a) Flood expose sample, 15 sec
    (b) Develop exposed PR – MF-701, 2 min
    (c) Strip remaining PR in acetone – 3 min
    (d) Inspect – if PR remaining, use 1165 stripper, 80 °C, 3 min
    (e) Gently agitate sample surface with small pipet
- Rinse sample in 2-propanol before transferring to DI water or Solvent clean

50. **Metal-3 interconnect and ground plane lithography**

- Solvent clean – 3 min acetone, 3 min 2-propanol, 3 min DI water rinse
- Dehydration bake – 120 °C, 10 min
- Photoresist spin – nLOF 2020, 3 kRPM, 30 sec
- Pre-exposure PR bake – 111°C, 60 sec
- Shoot 'Metal 3' pattern in stepper – 0.47 sec
- Post-exposure PR bake – 114°C, 60 sec
- Development – MF-701 developer, 2 min
- Rinse wafer – DI water for 2 min, N_2 dry
- Inspect wafer using optical microscope

51. **Metal-3 interconnect and ground plane deposition**

- Prepare ozone reactor – run empty, 20 min
- Surface preparation – clean wafer surface in ozone reactor, 5 min
- Vent E-beam 4, load private sources – Ti and Au
- Surface preparation – NH_4OH:DI water 1:10 dip 10 sec, N_2 dry, ***NO WATER RINSE***
- Load sample in E-beam 4 – orient long-axis of emitter perpendicular to the direction of sample rotation inside E-beam 4

- Allow system to pump-down for 90 min to $< 10^{-6}$ torr
- Deposit Metal-3 (ground plane)
  - Ti 100 Å (1 Å/sec)
  - Au 15 kÅ
    * 2 Å/sec for 1-300 Å
    * 3 Å/sec for 301-500 Å
    * 4 Å/sec for 501-1000 Å
    * 5-6 Å/sec 1001-15000 Å
  - Ti 100 Å (1 Å/sec)
- Metal liftoff – 1165 stripper, 80 °C, 2 hour
- Remove metal and place sample in fresh 1165 stripper, 80 °C, 20 min
  - Gently agitate sample surface with small pipet
  - Rinse sample in 2-propanol before transferring to DI water or Solvent clean