UNIVERSITY OF CALIFORNIA
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Analog Integrated Circuits with AlInAs/GaInAs Transferred-Substrate HBTs

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering
by

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March 1998

The dissertation of Bipul Agarwal
is approved:

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March 1998

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1998

to my

parents

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Publications

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Abstract

Analog Integrated Circuits
with AlInAs/GaInAs Transferred-Substrate HBTs

by
Bipul Agarwal

A variety of analog integrated circuits for wideband systems including fiber-optic communication systems have been designed and fabricated in the transferred-substrate heterojunction bipolar transistors integrated circuit technology. Transferred-substrate HBTs have demonstrated very high f_{max} (>400 GHz), and are thus potential candidates for future, very-high speed integrated circuits. The high bandwidth of transferred-substrate HBTs is due to the process of substrate transfer, which allows lithographically defined, narrow and aligned collector and emitter stripes on opposite sides of the base epitaxial layer. Transistor bandwidth then becomes inversely proportional to the stripe width, increasing rapidly with scaling. An IC fabrication process has been developed, incorporating transferred-substrate HBTs, nichrome resistors, silicon nitride metal-insulator-metal capacitors, low-loss microstrip transmission lines, and three levels of interconnect metallization. The interconnects, microstrip on Benzocyclobutene (low dielectric constant), provide a low-capacitance wiring environment. A gold ground plane and short ground vias through the thin Benzocyclobutene substrate provide low ground-return inductance. Electroplated gold thermal vias provide transistor heat-sinking. These unique features of the transferred-substrate HBT IC process have enabled very high performance ICs. Four different integrated circuits with varying levels of integration were designed and fabricated. The first demonstration IC, a Darlington feedback amplifier, with two transistors, had 13 dB gain, 50 GHz bandwidth. An improvement on this basic design, a Darlington-cascode amplifier with three transistors had 11 dB gain and greater than 50 GHz bandwidth. A traveling-wave amplifier with six transistors had 6.7 dB gain, 85 GHz bandwidth. A differential amplifier with twenty-two transistors had 50 GHz bandwidth, 11 dB gain. These amplifiers, the first integrated circuits fabricated in the transferred-substrate technology, exhibit record per-

formance and good yield. Higher scales of integration and high-performance ICs for future high-speed systems should soon be possible.

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Chapter 1

Introduction

Fiber-optic communication systems are being used to transmit vast amounts of data at high speeds. They are employed in virtually all areas of telecommunication including trans-oceanic cables, long-haul terrestrial networks between cities, trunk-lines within metropolitan areas and subscriber loop systems. Recently, optical-fiber systems are being used for distribution of cable television and in local area networks for high-speed computer networking. The demand for higher bit-rate communication is rapidly growing as broadband integrated services involving multimedia become increasingly popular. 10 Gbit/s systems are being deployed and extensive research and development is being done for future 40 and 160 Gbit/s systems [1, 2, 3, 4, 5, 6]. Often, the transmission bit-rate of such systems is limited by the bandwidth of component electronic circuits in the transmitter and receiver. Circuit bandwidth is directly related to the device bandwidth, and is also influenced by circuit design and physical layout, power and cost budget, and communication strategies used. To meet the ever-increasing demand for higher bit-rates, circuit speed, and hence, device bandwidth must be continuously increased. Typically, device bandwidth is improved by scaling critical lithographic dimensions of the device, as well as by improvements in epitaxial growth and fabrication processes. The aim of this thesis was to develop a integrated circuit (IC) process incorporating a scalable device, and to demonstrate some first-generation ICs for future high-speed fiber-optic systems.

This chapter describes a typical fiber-optic communication system and the specific ICs of the system that have been examined in this thesis. Im-

plementation technologies (HEMT/HBT) are briefly discussed. The second chapter describes the important theoretical aspects of transferred-substrate HBTs. Chapter 3 deals with the device and IC technology in detail, including material growth and IC fabrication process. Electrical characteristics and device modeling are covered in chapter 4. Circuit design, simulations and circuit results are dealt with in chapter 5. Finally, chapter 6 draws conclusions from this work and projects future directions.

1.1 ICs for Fiber-Optic Systems

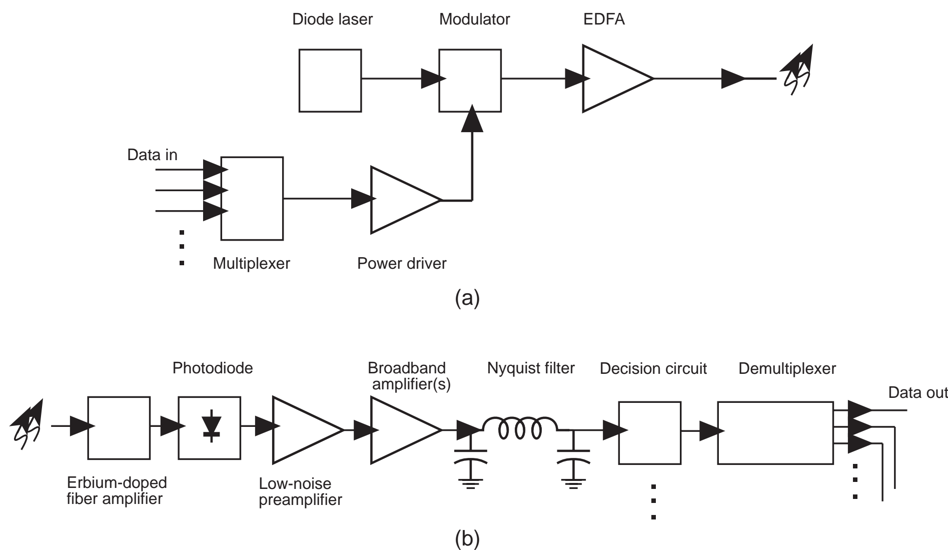


Figure 1.1: Block diagram of a typical fiber-optic system showing a) transmitter and b) receiver.

Figure 1.1 shows the block diagram of a typical fiber-optic communication system. The transmitter consists of a multiplexer (MUX) which combines several channels of digital data into one data stream at a higher bit-rate. This electrical data is then converted into a optical signal through a laser. The electrical signal could directly modulate the laser intensity, but is limited by laser bandwidth and chirp for data rates above 10 Gbit/s. At higher data rates, an external electro-optic modulator with a driver is used as shown. The modulated signal is transmitted via a optical fiber to

its destination. Post-amplification through erbium-doped fiber amplifiers (EDFAs) may be used to boost transmitter power. During transmission, the signal may be amplified or regenerated using optoelectronic repeaters, especially for long distances. At the receiver end, more EDFAs may be used to pre-amplify the signal. The optical signal is converted back to an electrical signal using a photodiode. A low-noise transimpedance preamplifier converts the small signal current generated by the photodiode into a signal voltage. The signal voltage is amplified by the main amplifier. Decision circuits then regenerate the actual transmitted digital data. This recovered data is then demultiplexed (DEMUXed) into the individual lower bit-rate data channels. A clock recovery circuit (not shown) extracts the clock (required by the DEMUX and decision circuits) from the amplified signal from the main amplifier. The positions of the DEMUX and the decision circuits in the link are interchanged in some cases. If the decision circuit is after the DEMUX, it needs to operate only at the single channel bitrate, but one circuit is needed for each data channel. As we can see, there are several important analog and digital circuits in the system which will determine the overall speed of the system. This thesis concentrates on the analog circuits within the fiber link. These include the laser driver, the transimpedance preamplifier, and the main amplifier. The performance requirements of each of these ICs will now be examined in more detail.

Modulator drivers are among the more difficult ICs to implement, as their output waveform must be large in amplitude and directly determines the shape of the transmitted optical signal. A wide bandwidth ($\sim 0.7\times$ bit-rate) is required at absolute minimum. High modulator driver output power is required because of the modulator's typical V_π of $\sim$ 10 V and its $\sim$ 50 Ω impedance. In-band gain flatness is important to preserve the shape of the incoming signal. The driver should have a low low-frequency cut-off for acceptable eye closure with long data sequences.

The transimpedance preamplifier determines the receiver signal-to-noise ratio and hence sensitivity. This stage must have a low input-referred noise current and flat gain over the signal bandwidth. Transimpedance (feedback) loading is often used to aid in simultaneously meeting noise and bandwidth constraints. The preamplifier frequently must also act as a single-end-to-differential converter if the subsequent gain stages are designed for differential operation.

Fiber-optic receivers require substantial amplification between the tran-

simpedance preamplifier stage output and the decision circuit input. The main amplifier, referred to as the linear channel provides this gain. Because there are many cascaded stages, the gain and group delay must be substantially flat over a bandwidth extending from a few KHz up to about 70% of the data rate. AGC or *symmetric* limiting characteristics are also required. To meet these requirements, broadband multistage differential amplifiers are generally employed. As mentioned earlier, differential or single-ended operation can be employed. The advantages of differential operation compared to single-ended are improved immunity to electromagnetic crosstalk, good common mode suppression, ease of dc biasing and symmetric non-saturating limiting characteristics. The amplifiers could be implemented in either lumped or distributed configuration. Distributed amplifiers generally obtain a higher bandwidth in a given transistor technology. However, good low-frequency response is difficult to achieve, in-band gain ripple is often present and die areas are large. Lumped amplifiers can be DC coupled, have smaller die areas and smooth gain-frequency characteristics.

1.2 Technology

High-speed fiber-optic systems require wideband circuits, which in turn require very high device bandwidths. Device bandwidth is indicated by two common figures of merit : f_τ, the current gain cut-off frequency, and f_{max}, the power gain cut-off frequency. For 100 Gbit/s fiber-optic communication ICs, circuit bandwidths must be $\sim$ 70 GHz, and devices having f_τ and f_{max} in excess of 200-250 GHz are required [7]. Future, higher bit-rate systems will require even higher device bandwidths. The two dominant high frequency transistors are high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs), both based on compound semiconductors. Early work in this thesis concentrated on ICs using AlGaAs/InGaAs PHEMTs. HEMT-based IC processes are generally simpler than HBT-based processes, and hence are easy to develop. Also, 0.1 μm AlGaAs/InGaAs HEMTs have sufficient bandwidth and breakdown voltage for 40 Gbit/s applications. A HEMT IC process was developed at UCSB, and devices with 1 μm gate lengths were successfully fabricated. However, HEMTs with sufficient f_τ for 40 Gbit/s require gate lengths with < 0.25 μm dimensions, necessitating the use of advanced lithographic tools like e-beam lithography or projection lithography systems. Unavailability of these tools

at the time, at UCSB, prevented fabrication of circuits designed in this process. Some designs were successfully fabricated in advanced HEMT processes in collaboration with industrial research laboratories.

An on-going demonstration HBT device technology [8] was then adapted and developed (jointly with R. Pullela and Q. Lee) into an IC process. The existent device technology was capable of yielding only discrete devices and the device performance was not adequate for the target integrated circuits. Several changes were made in the material layer structure and the physical device layout and structure. Key IC elements like resistors, capacitors and transmission lines were added. Multiple wiring levels, thermal vias and a low ϵ BCB substrate were incorporated, bringing the technology to a level where complex high-performance ICs could be fabricated. A variety of ICs were then fabricated in this technology. This is the primary focus of this thesis.

While some integrated circuits for 40 Gbit/s fiber-optic links have been demonstrated with both HEMTs and HBTs, the performance is limited by several factors including intrinsic device bandwidth, wiring capacitance for dense circuits and efficient heat-sinking for HBTs operating at high current densities. For very similar reasons, circuits for 160 Gbit/s systems will be more difficult to develop. This thesis concentrates on HBTs and addresses the aforementioned problems at once. A scalable HBT is developed which can be scaled to achieve high bandwidths for high-speed systems. Typically, HBTs are not scalable devices. A fundamental change is made in the device structure which renders these devices scalable and achieves record bandwidths. The problem of wiring parasitics is addressed by the use of BCB. Thermal vias provide heat-sinking. The transferred-substrate HBT IC process is developed and high-performance devices and the first integrated circuits in this technology with record performance are demonstrated. IC demonstration in this thesis paves the way for future very high-speed, very high-performance integrated circuits.

Chapter 2

Transferred-Substrate HBTs : Theory

Heterojunction bipolar transistors (HBTs) [9] have applications in medium-scale integrated circuits operating at GHz frequencies. HBTs have several advantages over Si-based devices and HEMTs including high bandwidth, high transconductance, high power density, low output conductance, low $1/f$ noise and very reproducible dc parameters. Target applications include digital phase-locked loops for microwave frequency synthesis, chip-sets for gigabit fiber-optic transmission, and wideband analog-digital converters. High circuit bandwidths are desirable; in Δ-Σ analog-digital converters, increased clock frequencies provide increased signal-noise ratios, while future optical transmission systems will require multiplexers, PLLs, and decision circuits with $\sim$ 100 GHz clock rates. In these applications, both the transistor current gain cut-off frequency f_τ, and the power gain cut-off frequency f_{max} must be considerably higher than the signal frequencies involved. 100 Gbps optical-fiber transmission ICs will require HBTs having f_τ and f_{max} greater than 200-250 GHz. A second-order Σ-Δ analog-digital converter having a 50 GHz sample rate would require HBTs with f_τ and $f_{max} \sim$ 200-300 GHz, but might provide 12 bits resolution at 1 GHz bandwidth. Broadband amplifiers for 40 & 100 Gbps communication would require HBTs with similar performance. HBTs with bandwidths of several hundred GHz will benefit many similar applications.

Progressive improvements in device bandwidths are needed to keep pace with the demand for integrated circuits operating at higher frequencies.

Device bandwidths are generally increased by scaling the device. Reducing the lithographic dimensions (lateral) and/or the semiconductor layer thicknesses (vertical) of a device is termed device scaling. With several important semiconductor devices, the device bandwidth increases as critical lithographic dimensions and layer thicknesses are reduced. Examples of highly scaled devices with large bandwidths are 0.1 μm gate length HEMTs, 0.25 μm gate length complementary metal-oxide-semiconductor (CMOS) transistors, 0.1 μm Schottky-collector resonant tunnel diodes (SRTDs)[10] and submicron Schottky diodes used as sub-millimeter wave mixers. HEMTs with short gate lengths ($\sim$ 0.1 μm) are presently the largest bandwidth three terminal devices. HEMTs with a power gain cutoff frequency (f_{max}) of 450 GHz have been reported [11]. The superior bandwidths of HEMTs is a result of the rapid improvement in HEMT bandwidth with deep submicron scaling. HBTs are usually fabricated with $\simeq$ 1 μm lithography and do not lend themselves to scaling as easily as other devices.

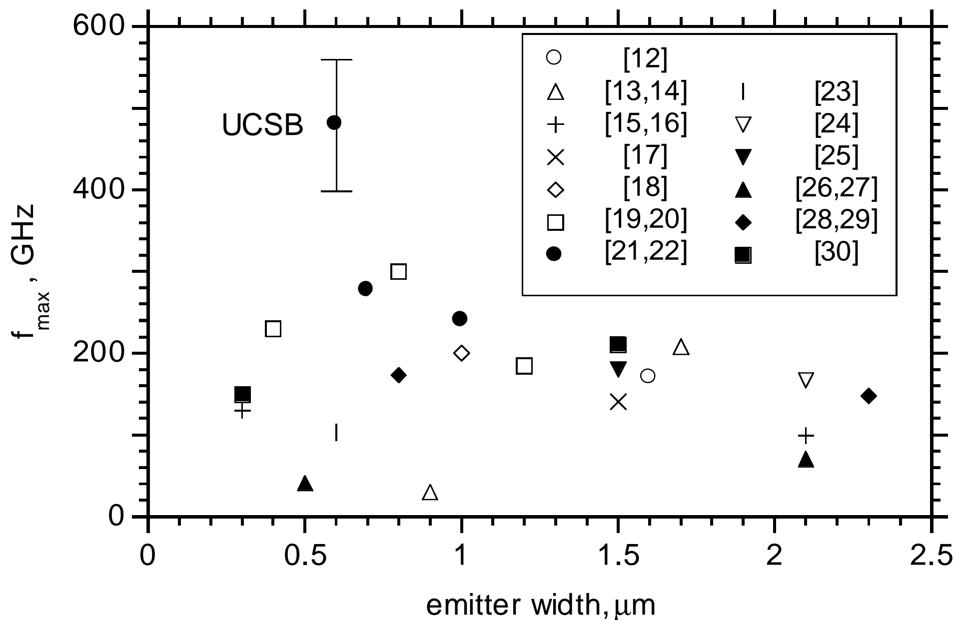
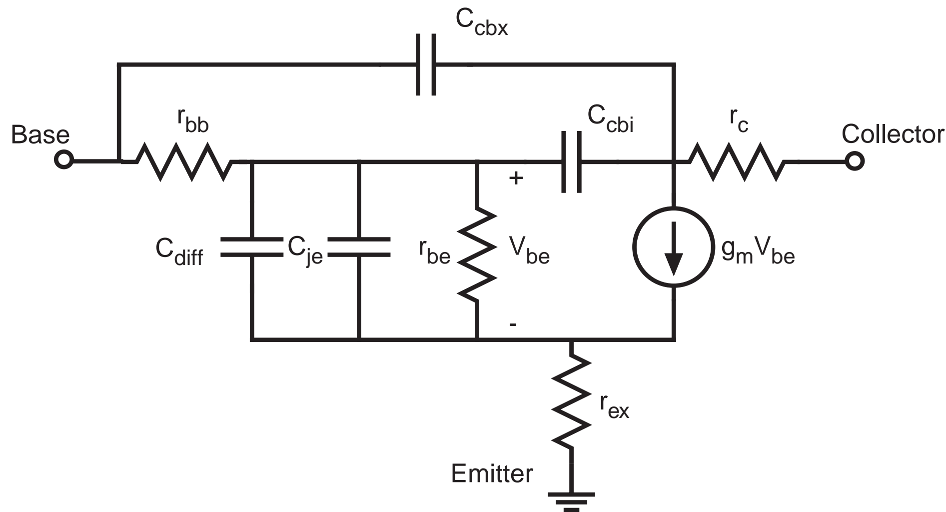


Figure 2.1: Comparison of f_{max} and emitter width for some HBTs in the literature.

Figure 2.1 shows f_{max} *vs.* emitter width for some HBTs reported in the literature. It can be seen that there is no strong correlation between f_{max}

and emitter width, at least for narrow emitters. Consequently, HBTs are not fabricated with deep submicron dimensions except where bias currents have to be limited for low power operation.



r_{bb} base resistance

r_c collector contact resistance

r_{ex} emitter contact resistance

$r_{be} = \beta / g_m$

$g_m = qI_c / kT$

C_{je} emitter-base junction capacitance

C_{diff} emitter-base diffusion capacitance $g_m \tau_f$

τ_f forward transit time $\tau_b + \tau_c$

C_{cbi} intrinsic collector-base capacitance

C_{cbx} extrinsic collector-base capacitance

Figure 2.2: Hybrid-π model of a HBT for calculation of the short-circuit current gain.

The relationship between f_{max} and emitter and collector widths will now be explored. Parts of this theoretical discussion were presented in [31], and are repeated here for the sake of completeness. A simple hybrid-π model of a HBT is shown in figure 2.2 with the model components related to the device parameters and biasing conditions. The expression for short circuit current gain corresponding to this device model is

$$A_I = \frac{-\beta}{1 + j\omega\beta\left[(1/g_m)\left(C_{be} + C_{cb}\right) + (r_{ex} + r_c)C_{cb}\right]} \tag{2.1}$$

under the following conditions : DC short circuit current gain $\beta \gg 1$, $\omega C_{cb} \ll g_m/(1 + g_m r_{ex})$, only first order terms in angular frequency ω considered and the extrinsic C_{cb} charging time is small.

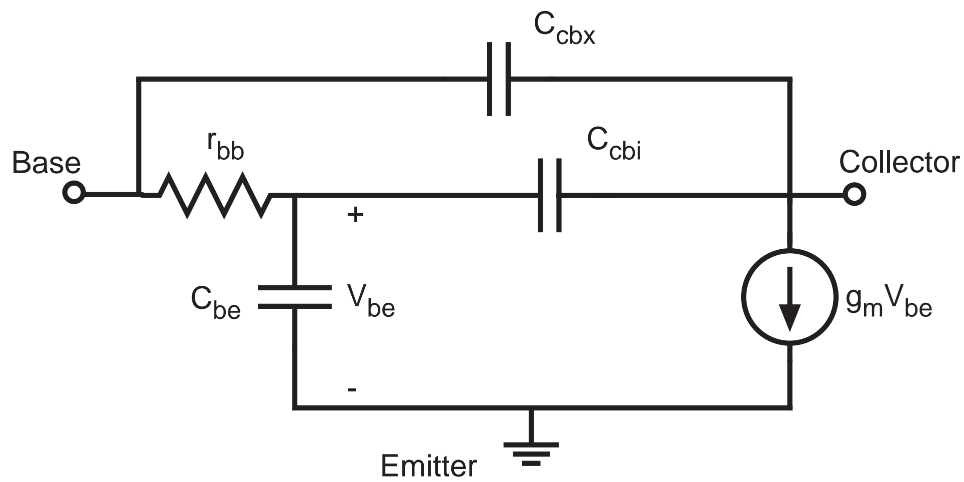
The short circuit current gain cutoff frequency f_τ corresponds to the frequency at which the magnitude of A_I is unity. Near this frequency, the imaginary part of the denominator in Eq. (2.1) is much larger than unity. The expression for f_τ as a function of device parameters and biasing conditions is therefore approximately

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{je} + C_{cb}) + (r_{ex} + r_c)C_{cb}. \tag{2.2}$$

Here τ_b is the base transit time, τ_c the collector transit time, kT/q the thermal voltage, I_c the collector current, C_{je} the emitter-base junction capacitance, C_{cb} the collector-base capacitance, r_{ex} the emitter contact resistance, and r_c the collector contact resistance. At a given current density, all terms except $r_c C_{cb}$ in the above equation are independent of lateral scaling. The base and collector transit times can be reduced by reducing the appropriate semiconductor layer thicknesses. Hence, f_τ can be improved by vertical scaling of the device, but is independent of lateral scaling.

The power gain cutoff frequency f_{max} is another important figure-of-merit of high-frequency HBT performance. F_{max} defines the maximum frequency at which a device can provide power gain. F_{max} not only depends on f_τ, but also on the base-resistance-collector-base-capacitance time constant as we shall now derive. F_{max} is the frequency at which the maximum available power gain G_{max} or Mason's unilateral power gain U [32] is unity. If the small signal equivalent circuit that was used for the derivation of f_τ is used, the derivation is extremely complicated and a simple usable expression does not result. A simplified model will be used which will yield a result that estimates f_{max} quite accurately. This has been verified in the literature [33].

Figure 2.3 shows a simplified small-signal hybrid-π model of a HBT. The input base-emitter resistance R_{be}, the output resistance r_{ce} and the collector resistance r_c are neglected. The extrinsic emitter resistance r_{ex} is assumed to be absorbed into the element values by applying emitter degeneration



r_{bb} base resistance

$g_m = qI_c / kT$

C_{be} total emitter-base capacitance

C_{cbi} intrinsic collector-base capacitance

C_{cbx} extrinsic collector-base capacitance

Figure 2.3: Simplified hybrid-π model of a HBT for calculation of power gain.

to the model elements. The base-emitter capacitance C_{be} is the sum of the junction and diffusion capacitances. Mason's unilateral power gain U is given in terms of two-port y-parameters as

$$U = |y_{21} - y_{12}|^2/4(Re(y_{11})Re(y_{22}) - Re(y_{12})Re(y_{21})). \tag{2.3}$$

For the HBT model shown above, the four y-parameters can be derived from simple network theory and are given below in terms of the element model values.

$$\begin{aligned}
y_{11} &= 1/r_{bb} + j\omega C_{cbx} + j\omega C_{cbi}/\omega^2 {C_{be}}^2 {r_{bb}}^2 \\
y_{12} &= -C_{cbi}/C_{be} r_{bb} - j\omega C_{cbx} - j\omega C_{cbi}/\omega^2 {C_{be}}^2 {r_{bb}}^2 \\
y_{21} &= g_m/j\omega C_{be} r_{bb} - j\omega C_{cbx} - j\omega C_{cbi}/\omega^2 {C_{be}}^2 {r_{bb}}^2 \\
y_{22} &= g_m C_{cbi}/C_{be} + j\omega C_{cbx} + j\omega C_{cbi}/\omega^2 {C_{be}}^2 {r_{bb}}^2
\end{aligned} \tag{2.4}$$

Using Eq. 2.4 in Eq. 2.3, U can be derived as a function of frequency and is given below.

$$U = ({g_m}^2 + \omega^2 {C_{cbi}}^2)/4\omega^2 C_{be} C_{cbi} r_{bb} g_m \tag{2.5}$$

By setting the unilateral gain equal to unity, the expression for f_{max} is derived and is given below.

$$f_{max} = \sqrt{f_\tau/8\pi r_{bb} C_{cbi}} \tag{2.6}$$

with the assumption that $\omega C_{be} r_{bb} \gg 1$, $C_{cbi} < C_{be}$ and $f_\tau = g_m/2\pi C_{be}$. As we can see from Eq. 2.6, no matter how large the value of f_τ is, power gain is available only at frequencies below f_{max}. Hence, to improve device bandwidth, is it important to improve f_τ as well as the $r_{bb}C_{cbi}$ time constant. Note that while the extrinsic collector-base capacitance has no impact on f_{max}, it does impact the performance of many circuits, and should be minimized.

We will now see what determines the $r_{bb}C_{cbi}$ charging time constant for HBTs. The cross section of a double-mesa HBT is shown in figure 2.4. The base resistance r_{bb} has three components. These are : the contact resistance from the base Ohmic contact, the sheet resistance from the gap between the emitter mesa and the base Ohmic contact, and the spreading resistance

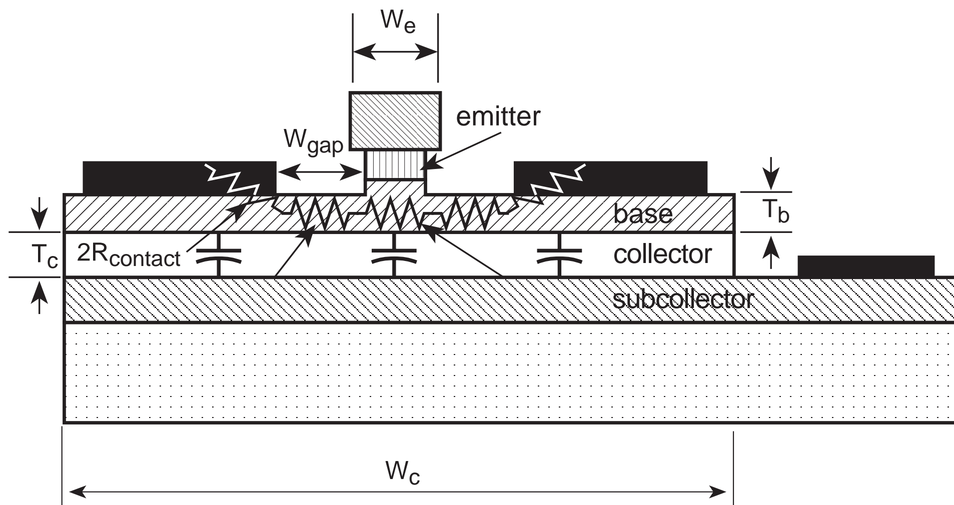


Figure 2.4: Schematic cross-section of a double-mesa HBT.

of the base layer underneath the emitter mesa. The contact resistance is given by

$$R_{contact} = \sqrt{\rho_{bc}\rho_{bs}}/2l \tag{2.7}$$

where ρ_{bc} is the specific contact resistance per unit area of the metal-semiconductor interface (units of Ω-cm^2), ρ_{bs} is the base sheet resistivity (units of $\Omega/\square$) and l is the transverse length of the emitter stripe (units of μm). The gap resistance is given by

$$R_{gap} = \rho_{bs}W_{gap}/2l \tag{2.8}$$

where W_{gap} is the separation between the emitter mesa and the base Ohmic contact. The spreading resistance is given by

$$R_{spread} = \rho_{bs}W_e/12l \tag{2.9}$$

where W_e is the emitter width. For HBTs fabricated with a self-aligned base-emitter process, $W_{\text{gap}} \simeq 0.1$ μm and R_{gap} is negligible. We note also that R_{spread} is proportional to the emitter width W_e, but that R_{contact} is independent of W_e. Hence, for narrow-emitter devices, the base resistance tends to be dominated by R_{contact} and is only weakly dependent upon W_e. The total collector-base capacitance is given by

$$C_{cb} = \epsilon l W_c / T_c \tag{2.10}$$

where, W_c is the width of the collector (= width of the base mesa), l is the length of the emitter stripe and T_c is the thickness of the collector depletion region. Hence, C_{cb} is proportional to the width of the base mesa which in turn is much wider than, and, independent of W_e. Note that only a fraction C_{cbi} of C_{cb} is charged through the base resistance r_{bb}. Determination of the C_{cbi}/C_{cb} ratio from the HBT physical dimensions has been mentioned [33] but has not been fully explored in the literature. We estimate that

$$C_{cbi} \simeq \epsilon l (W_e + 2W_{gap} + 2l_{contact}) / T_c \tag{2.11}$$

where

$$l_{contact} = \sqrt{\rho_{bc}/\rho_{bs}} \tag{2.12}$$

is the transfer length of the base Ohmic contact. This approximation is based upon taking the fraction of C_{cb} whose charging current shares a common path through the base with the currents associated with charging C_{be}. We note that the collector-base junction area of double-mesa HBTs is further increased by the presence of a base contact pad area necessary to bring interconnect metallization onto the base Ohmic metal. Lateral scaling below ~ 1 μm does not substantially improve the bandwidth of double-mesa HBTs.

A transferred-substrate HBT can be scaled laterally to improve bandwidth. The cross-section of a transferred-substrate HBT is shown in figure 2.5. Transferred-substrate HBTs have lithographically defined narrow emitter and collector stripes aligned to each other on opposite sides of the base epitaxial layer [34]. This is the special feature of the transferred-substrate HBT in contrast to the double-mesa HBT. The fabrication of transferred-substrate HBTs requires access to the emitter and the collector sides of the epitaxial film. The process of substrate transfer allows this access and is an essential step in the fabrication process. The base resistance is dominated by R_{contact} and is independent of W_e, as for the double-mesa HBTs. The collector-base capacitance C_{cb} is proportional to the width of the collector stripe W_c, if fringing capacitance is negligible (figure 2.5); $C_{cb} = \epsilon l W_c / T_c$, where l is the length of the collector or the emitter stripe and T_c is the thickness of the collector depletion region. If a constant ratio

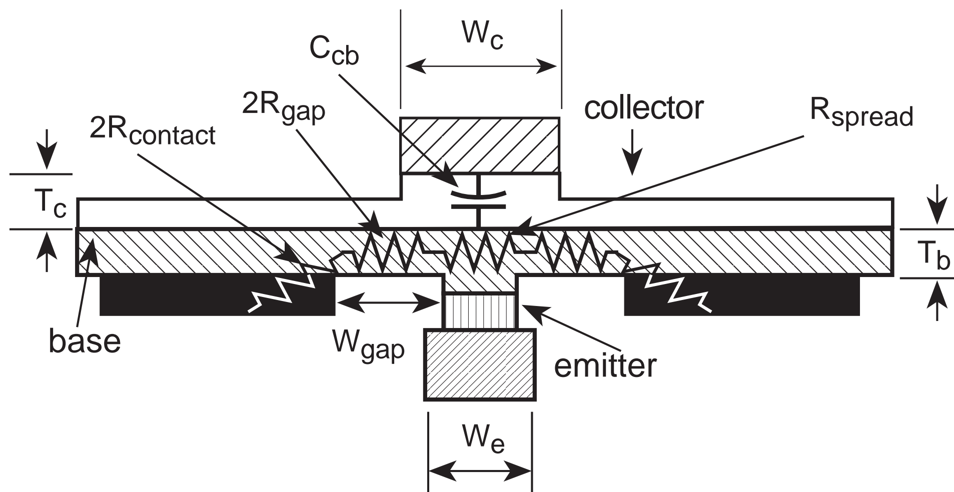


Figure 2.5: Schematic cross-section of a transferred-substrate HBT.

is maintained between the emitter and the collector widths, C_{cb} is proportional to the emitter width W_e. Noting that $r_{bb} \simeq R_{\text{contact}} = \sqrt{\rho_{bc}\rho_{bs}}/2l$, and $C_{cb} = \epsilon l W_c/T_c$ (where $W_c \propto W_e$), the $r_{bb}C_{cb}$ time constant is proportional to W_e. This, when used in Eq. (2.6) shows that the maximum frequency of oscillation f_{max} depends on W_e as

$$f_{max} \propto \frac{1}{\sqrt{W_e}}. \tag{2.13}$$

Hence, f_{max} rapidly improves with submicron lateral scaling of the device. The cross-section of the transferred-substrate HBT in figure 2.5 shows a direct Schottky contact to the collector depletion layer. An Ohmic collector with a heavily doped subcollector, with the subcollector semiconductor material etched away outside the Ohmic metal contact, could also be used. An Ohmic collector contact having the same width as the Schottky contact will also show the same variation of f_{max} with scaling. The two devices are almost identical except for an extra potential drop across the collector-base junction of the Schottky-collector device. This potential drop, due to the Schottky contact, is the difference between the work function of the metal Schottky contact and the electron affinity of the collector semiconductor. A Schottky collector contact provides a slight improvement in f_τ because of the absence of a collector contact resistance (Eq. (2.2)). It is also easier to

fabricate deep submicron Schottky collector contacts (e.g. 0.1 μm T-gate) than deep submicron Ohmic contacts. On the other hand, a Ohmic collector might improve transistor performance at low collector-emitter biases V_{CE}, as we will see later. This is due to the extra potential drop at the Schottky contact as compared to the Ohmic contact.

The scaling law of Eq. (2.13) suggests that the operating bandwidth of HBTs can be increased without bounds by lithographic scaling alone. In fact, to obtain usable devices, vertical scaling of the epitaxial layer thicknesses must accompany the lithographic scaling. Except in the case of reactively- matched amplifiers and distributed circuits where f_{max} is the sole determinant of circuit bandwidth, both f_{τ} and f_{max} are generally important for optimum circuit performance in a given technology. Devices with $f_{max} \ll f_{\tau}$, obtained by thinning the epitaxial layers *without* lateral lithographic scaling will show circuit bandwidth determined by r_{bb} and C_{cb}. Devices with $f_{max} \gg f_{\tau}$ (e.g. devices with relatively thick epitaxial layers and significant lateral lithographic scaling) will show circuit bandwidth dominated by $(\tau_b + \tau_c)$. Reduction of $(\tau_b + \tau_c)$ is obtained by thinning the epitaxial layers, which unfortunately increases $r_{bb}C_{cb}$. The transferred-substrate HBT allows for the subsequent reduction of $r_{bb}C_{cb}$. A device having high values for *both* f_{τ} and f_{max} is thus possible.

Several approaches have been reported for reducing the collector-base capacitance of HBTs, and thereby improving f_{max}. One approach is the reduction of the width of the base mesa [20]. This relies on improvements in base contact technology because a narrow base mesa results in a smaller base Ohmic contact area. The base contact width must be at least one transfer length if the contact resistance is to be kept small. In contrast, the transferred-substrate technique provides independent control of the base and collector contact widths. There have been other approaches to make the collector contact width independent of the size of the base mesa, such as selective etching to undercut the collector [35], collector isolation implant [36], contacting the base with a very narrow L-shaped contact [37], selective lateral oxidation of the emitter [38] for a collector-up growth, burying SiO_2 in the extrinsic collector [39], selectively regrowing the extrinsic collector [40], and, patterning and regrowing a narrow subcollector followed by regrowth of the other layers [41]. However, in almost all cases, minimal improvement in device f_{max} was obtained. Moreover, the scalability of these approaches has not been demonstrated. Transferred-substrate HBTs can

be scaled to deep submicron dimensions with the use of powerful fine-line lithography for fabricating narrow emitter and collector stripes leading to dramatic improvement in device f_{max}.

The first transferred-substrate HBT was demonstrated by U. Bhattacharya [31]. The device structure used there is shown in figure 2.6.

In this early work, a collector-up growth was used. The first step was formation of Ti/Pt/Au Schottky collector contacts. Epoxy was then used to bond the wafer to a carrier substrate using an in-house mechanical bonding fixture. After removal of the InP substrate, a infra-red based backside aligner was used to align to the collector alignment marks which were buried under the epitaxial layers. Emitter-base fabrication was then done. The process was completed with the formation of electroplated airbridge contacts to the base and emitter. This process required considerable development, especially in base-emitter processing and substrate transfer. The epitaxial material growth also evolved significantly as experiments were done to study every aspect of the layer structure. The concept of transferred-substrate HBTs was demonstrated. Peak f_τ and f_{max} obtained were 140 GHz and 170 GHz respectively.

The aim of the epoxy-bonded HBT reported above was to demonstrate transferred-substrate HBTs. In this, it was successful. Discrete devices with moderate yield were fabricated. Furthermore, these efforts built UCSB's general expertise in HBT technology. However, the ultimate goal of HBT development is to build integrated circuits. To this end, the epoxy-bonding technology is far from being suitable or adequate. First, the device performance was much poorer than is needed for high-performance integrated circuits. Device bandwidth in the range of 200-300 GHz or above is essential for circuit bandwidths in the range of 100 GHz. Improvements in the epitaxial layer structure and the physical device structure and transistor scaling are required to increase bandwidth. Second, essential elements of integrated circuits like resistors and capacitors need to be incorporated.

Third, transmission lines and interconnect wiring would be on a epoxy substrate. Epoxy is not known to be a good microwave substrate and hence would produce lossy transmission lines. Also, the high dielectric constant of epoxy would lead to significant interconnect capacitance. Microstrip transmission lines are not possible because of the absence of a ground plane and ground vias. Coplanar waveguide lines have to be used, which can be problematic with packaging. Fourth, HBTs operate at high current

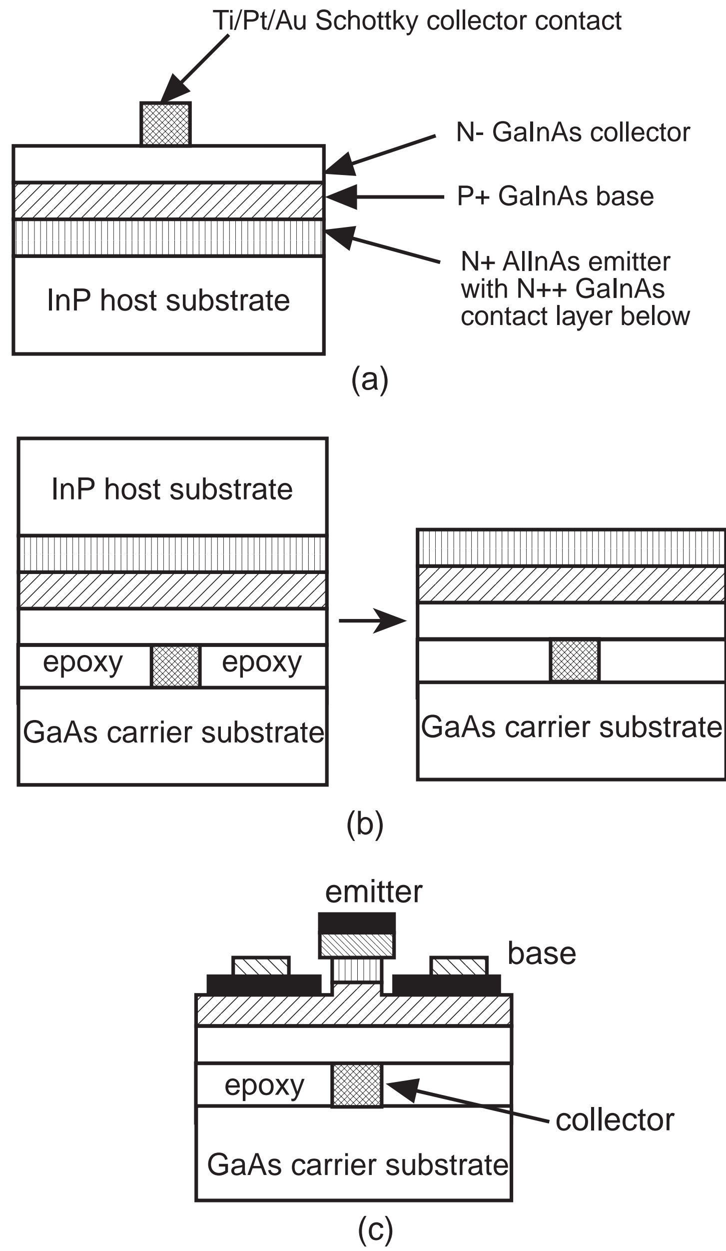


Figure 2.6: The first transferred-substrate HBT.

densities for high-speed operation. Effective heat-sinking is then vital. Heat dissipation in the epoxy process is through the epoxy substrate which has poor thermal conductivity. This prevents IC fabrication. Fifth, integrated circuits require high yield over large areas with good uniformity. The use of epoxy and the in-house bonding fixture is unsuitable for this purpose. The epoxy thickness was quite non-uniform, which led to poor device uniformity and less than adequate yield. The uncalibrated bonding pressure was also a problem, leading to wafer cracking. Sixth, only small substrates (about 1 cm $\times$ 1 cm) were used. While this was acceptable for discrete devices, ICs occupy larger areas, and larger substrates are needed. The epoxy process had not been demonstrated for large substrates. The bonding procedure would be a problem.

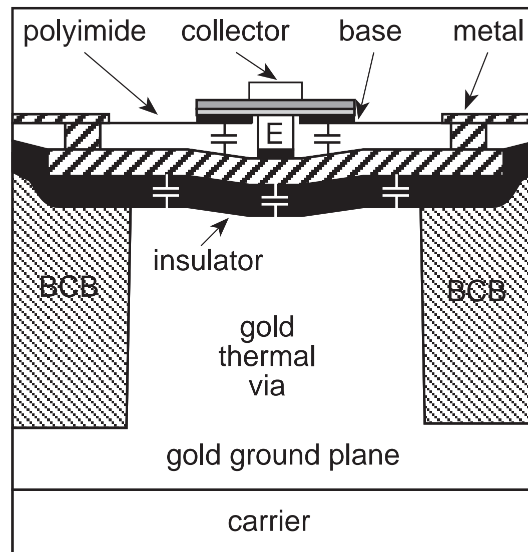
Seventh, the collector was buried in epoxy and this had two disadvantages. The collector recess etch, which is very important for reducing the fringing capacitance, had to be done before the process of substrate transfer. Hence the effect of recess etch could only be studied by processing two identical growth in the exact same way. Second, the effect of successive etches on a particular wafer could not be determined. There is strong evidence that the epoxy-bonded devices had excess parasitic collector-base capacitance, this because the collector-base junction is buried in epoxy.

These limitations of the epoxy-bonded transferred-substrate HBTs are removed by (first) eliminating the epoxy bonding step and (second) developing a collector-up structure fabricated from a emitter-up MBE growth. If a emitter-up growth is used, the collector contact is the last fabrication step and successive recess etches can be done to determine the best etch parameters with respect to device performance. The parasitic capacitance would be through air dielectric which has a lower dielectric constant compared to epoxy. In summary, the process is unsuitable for fabricating integrated circuits.

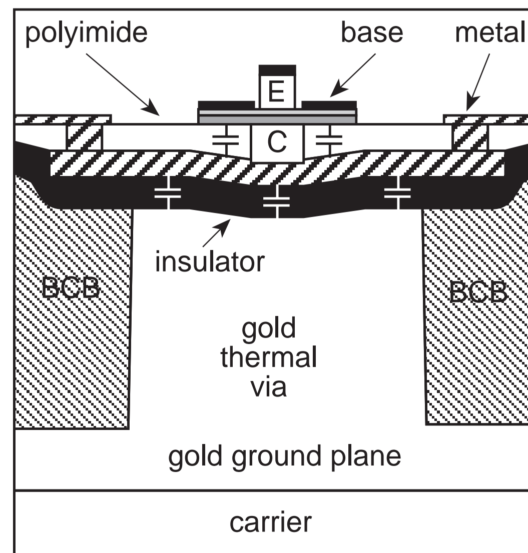
The proposed device structure and process addresses the problems discussed above. In addition to high device bandwidths, high frequency integrated circuit processes must incorporate a low capacitance wiring environment and low ground return inductance. For dense ICs, wire lengths, and hence transistor spacings must be small. Given that fast HBTs operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then vital. The transferred-substrate HBT IC process uses Benzocyclobutene (BCB), a low-loss, low dielectric-constant ($\epsilon_r = 2.7$), spin-on dielectric as the sub-

strate for microstrip interconnects, thus providing low capacitance. The thin ($\simeq$ 10 μm) BCB substrate with a gold ground plane underneath the entire IC also provides low inductance ground vias. Transistor heat-sinking is through electroplated gold thermal vias. Transmission lines for microwave circuits are microstrip lines on a BCB substrate. These lines have very low loss even at several tens of GHz and do not have the multimode propagation problems associated with coplanar waveguide lines (modes propagating between the frontside and backside ground planes). Three independent levels of wiring facilitate easy interconnection for dense circuits. Resistors are formed with thin-film nichrome (NiCr) and capacitors are metal-insulator-metal with PECVD SiN as the dielectric. The process of substrate-transfer is done using a automated flip-chip bonding machine with controlled temperature and pressure cycles. Epoxy is replaced with a In/Pb/Ag solder, with much better thermal performance and thickness uniformity. The use of standard IC materials like BCB and solder and a sophisticated bonding tool lead to high device uniformity and high yield. Larger substrates can be used facilitating the fabrication or large-area integrated circuits. Improvements in the epitaxial layer structure were made in the base and collector. The base layer was graded in bandgap and in doping to improve the base transit time. A pulse-doped layer was added to the collector to delay the onset of Kirk effect. All these improvements have transformed a demonstration device technology into a advanced IC process and made possible high-performance integrated circuits. The choice of emitter-up or collector-up is still open. A emitter-up growth was used and the rationality of this choice is explained below.

A schematic cross-section of the transferred-substrate device, with the emitter or the collector as the upper electrode is shown in figure 2.7. We now explain the motivation for designing such a structure and for choosing structure (a) instead of structure (b). Polymer layers conduct heat poorly and the thermal via is essential. As seen in the figure, there is a parasitic capacitance through the insulator between the contact metal and the grounded thermal via. This capacitance is between emitter and ground (figure 2.7(a)) or between collector and ground (figure 2.7(b)) depending on whether the collector or the emitter is the top electrode. From a circuit viewpoint, the emitter is a low-impedance node and the collector is a high-impedance node. The parasitic capacitance will affect circuit performance more strongly if it is at a high-impedance node. Hence using the collector



(a)



(b)

Figure 2.7: Schematic cross-section of device structure reported in this thesis. While (a) the emitter or (b) the collector could be the top electrode in this figure, the text explains the motivation for using the collector as the upper electrode.

as the top electrode is beneficial.

One of the main features of the transferred-substrate HBT is the reduction in collector-base capacitance C_{cb} obtained by using narrow collector stripes. If the collector is the lower electrode, a parasitic collector-base capacitance in series with a base resistance would exist as shown in the figure. The parasitic capacitance would be significant compared to the intrinsic device capacitance and would therefore degrade f_{max} significantly. On the other hand, if the emitter is the lower electrode, parasitic emitter-base capacitance resulting from the device structure is present. The emitter-base capacitance of the HBT itself is $\sim 100:1$ larger than the collector-base capacitance. Hence a small additional parasitic emitter-base capacitance introduced from the substrate-transfer process is only of minor concern. Again, using the collector as the top electrode is beneficial.

As an added advantage, a emitter-up growth also finally allows access to the extrinsic collector region, which can be recess etched to reduce the fringing collector-base capacitance. This is shown in figure 2.8. In figure 2.8(a), there is no recess etch, thus resulting in substantial fringing capacitance. In figure 2.8(b) only the collector sidewalls are removed leading to a ~ 30 % reduction in C_{cb}. This etch profile results if a dry etch is used or if a anisotropic wet etch is used. If a isotropic wet etch is used, lateral undercutting during the etch results in the profile of figure 2.8(c), which leads to a significant further reduction in C_{cb}. This has been verified experimentally. Hence the collector is designed to be the upper electrode.

There is one significant disadvantage to the collector being the top electrode. The thermal via should preferably be closest to the region where most heat is generated in the device. For a HBT, this happens to be the base-collector junction area as the electrons are swept towards the collector contact under high field. Given that the collector is on top to avoid excess C_{cb}, the thermal via has to be on the emitter side even though the heat generation is primarily in the collector. Hence, there is a trade-off between microwave and thermal design of the transistor.

It is expected that with submicron scaling of transferred-substrate HBTs, f_{max} in excess of 700 GHz should be possible. With this high bandwidth, integrated circuits operating at very high speeds should be feasible. Circuit speed depends on device bandwidth as well as on other key factors outlined above. The transferred-substrate HBT IC process has been designed to incorporate the key IC requirements. To realize high-speed circuits and

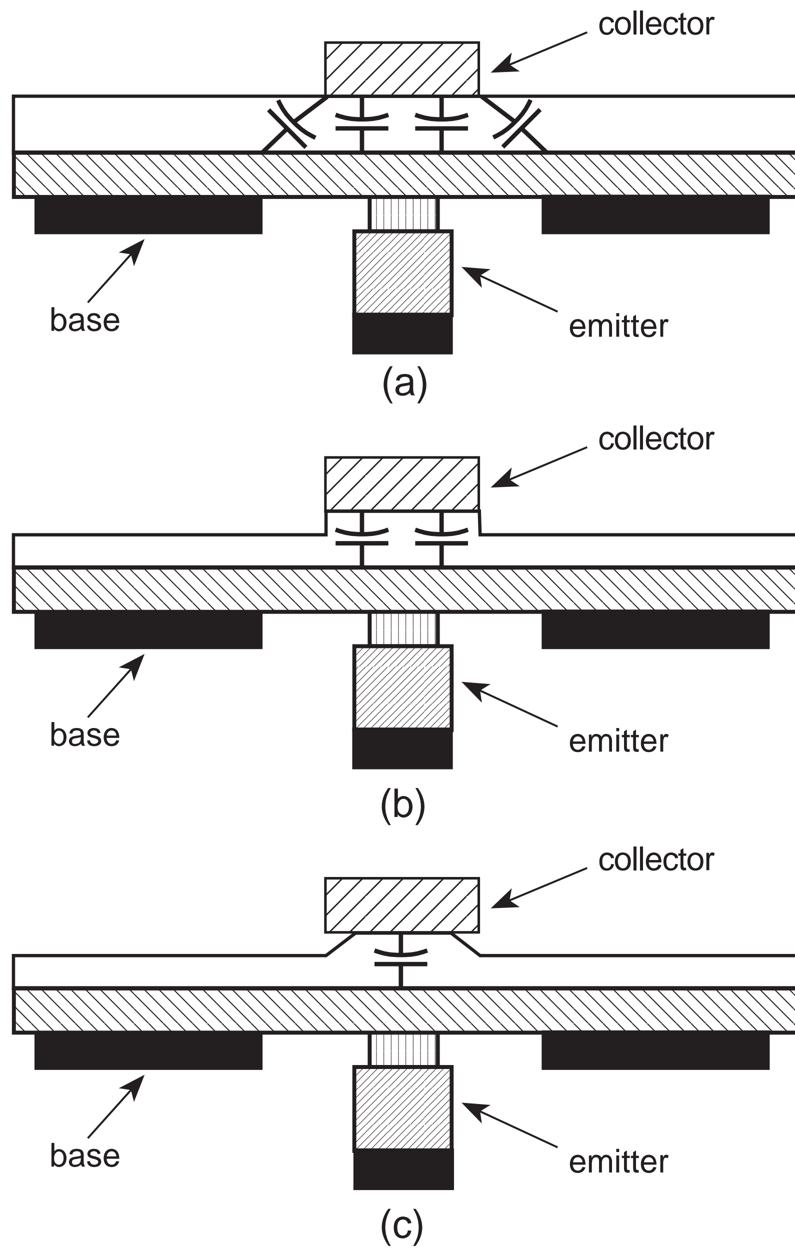


Figure 2.8: Recess etching the collector to reduce fringing collector-base capacitance.

devices, extensive process development was done. The fabrication process is presented in the next chapter.

Chapter 3

Fabrication

This chapter details the IC fabrication procedure. The process is complex with ten mask layers and tens of process steps. Starting with the work of Bhattacharya [31], process development involved extensive experimentation and multiple wafer runs, an effort which took two years of intense effort. The results from every process development experiment are not presented here in detail; only the final process is presented. The process is described in detail in the Appendix.

3.1 MBE layer structure

The AlInAs/GaInAs material system was chosen for the fabrication of transferred-substrate HBTs. This material system has several advantages over the AlGaAs/GaAs system including higher electron mobility, higher saturated electron velocity and lower surface recombination. Combined with the scalability of transferred-substrate HBT, the AlInAs/GaInAs system should yield very high-performance devices. The HBT epitaxial layer structure (figure 3.1(a)) is grown by molecular beam epitaxy (by D. Mensa) on a Fe-doped semi-insulating (100) InP substrate, starting with a 2500 Å AlInAs buffer layer. The GaInAs collector is 2700 Å thick, is Si-doped at $1 \times 10^{16}/\mathrm{cm}^3$ and contains a $5 \times 10^{11}/\mathrm{cm}^2$ Si pulse-doped layer 400 Å from the base. This pulse-doped layer delays the onset of base push-out [42] and depletes out-diffused Be in the collector. A thinner (2500 Å) collector was also used in some growths. Thin collectors increase the collector-base capacitance degrading f_{max}, but improve the collector transit time increasing

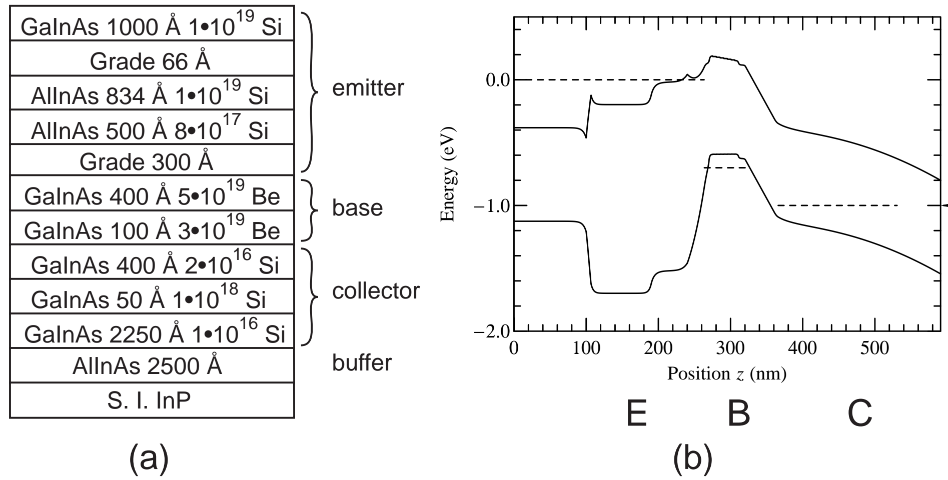


Figure 3.1: (a) MBE layer structure and (b) Band diagram under forward bias.

f_τ. Thinner collectors also improve the Kirk effect threshold thus enabling higher current density operation. Of course breakdown is worse in thin collectors because of the increased electric fields.

To reduce the base transit time, the 500 Å GaInAs base is graded in both doping and bandgap. The 100 Å of the $Ga_{0.47}In_{0.53}As$ base immediately adjacent to the collector is Be-doped at $3 \times 10^{19}/cm^3$. The remaining 400 Å of the base is Be-doped at $5 \times 10^{19}/cm^3$. By increasing the Ga cell temperature progressively during growth of the 400 Å layer, the Ga:In ratio is gradually increased, introducing a ~ 0.03 eV bandgap gradient across the 400 Å layer. In some of the results presented later, a thinner (400 Å) base was used. Thin bases improve the base transit time at the cost of increased base sheet resistance. Also, thin bases are difficult to grow in a controlled manner due to problems associated with outdiffusion of the Be dopant from the heavily doped base layer. The emitter-base etch involves a self-aligned etch down to the base epitaxial layer. Precise and uniform etching is desired to achieve low and uniform base resistance. With thin layers, more non-uniformity might result during this etch. An alternative to reducing the base thickness to improve transit time would be to increase the bandgap grading in the base. But, too much grading can cause excessive strain and growth defects in the semiconductor layers due to lattice mismatch. Also, GaInAs epitaxial layers with too much Ga behave more like GaAs which

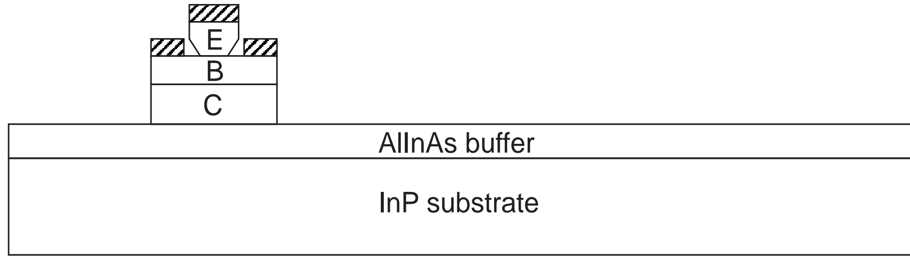
has a higher surface recombination velocity and might degrade the current gain of the device.

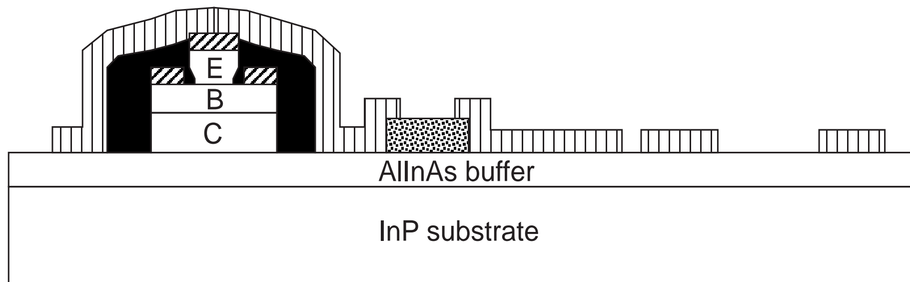
The base is then graded in 300 Å to the AlInAs emitter. The first 66 Å of the grade is Be-doped at $2 \times 10^{18}/\mathrm{cm}^3$ and the remainder is Si-doped at $8 \times 10^{17}/\mathrm{cm}^3$. The AlInAs emitter is about 1350 Å thick. The first 500 Å are Si-doped at $8 \times 10^{17}/\mathrm{cm}^3$ and the remainder is Si-doped at $1 \times 10^{19}/\mathrm{cm}^3$. This is graded in 66 Å to the InGaAs emitter cap. The emitter cap is n^+ doped with Si at $1 \times 10^{19}/\mathrm{cm}^3$. The emitter layer design is similar to [43]. A InAs emitter cap was used in some growths to reduce the emitter resistance.

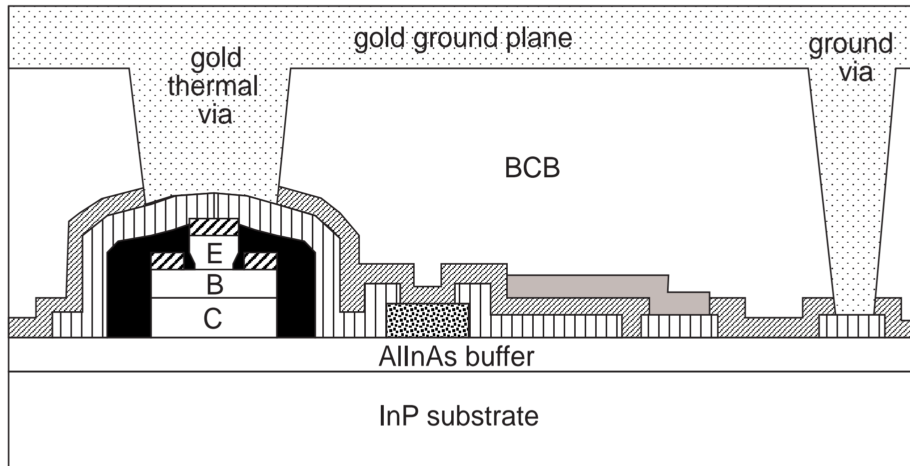
The band diagram corresponding to the layer structure of figure 3.1(a) under forward bias is shown in figure 3.1(b). The biasing conditions are as follows : base-emitter voltage $V_{BE} = 0.7$ V, collector-emitter voltage $V_{CE} = 1.0$ V, and a emitter current density of 1×10^5 A/cm^2. The collector current density is assumed to be the same as the emitter current density, as is the case of a narrow-collector HBT. The effect of the electrons in the collector space charge layer due to the collector current is included while calculating the electric field and the electrostatic potential in the collector space charge layer. An electron velocity of 3×10^5 m/s is assumed in these calculations. The pulse-doped layer causes significantly band-bending in the collector, close to the base as shown in the band diagram. As a result of this, the current density corresponding to Kirk effect threshold in increased as a higher electron charge is now needed to flatten the conduction band in the collector at the base edge.

3.2 Fabrication

Figures 3.2 and 3.3 show sequentially, the steps involved in fabrication of transferred- substrate HBTs. The fabrication process starts with the evaporation of Ti/Pt/Au/Si ($\sim$ 1 μm thick) emitter contacts. The Si layer is used as a mask for the following etches and is subsequently removed. A combination of a dry etch, a selective wet etch, and a non-selective wet etch is then used to etch down to the base epitaxial layer. The dry etch is done in a RIE system with $CH_4/H_2/Ar$ and it removes most of the unmasked emitter epitaxial layers. A laser monitor is used to determine the etch stop point and the etch conditions are designed to give a anisotropic vertical sidewall etch. A selective wet etch (which etches AlInAs selectively over GaInAs) is used to remove the remainder of the AlInAs emitter layer and expose the







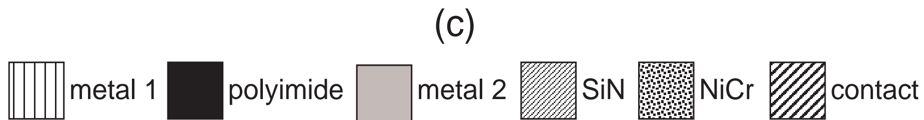


Figure 3.2: Fabrication process for transferred-substrate HBTs.

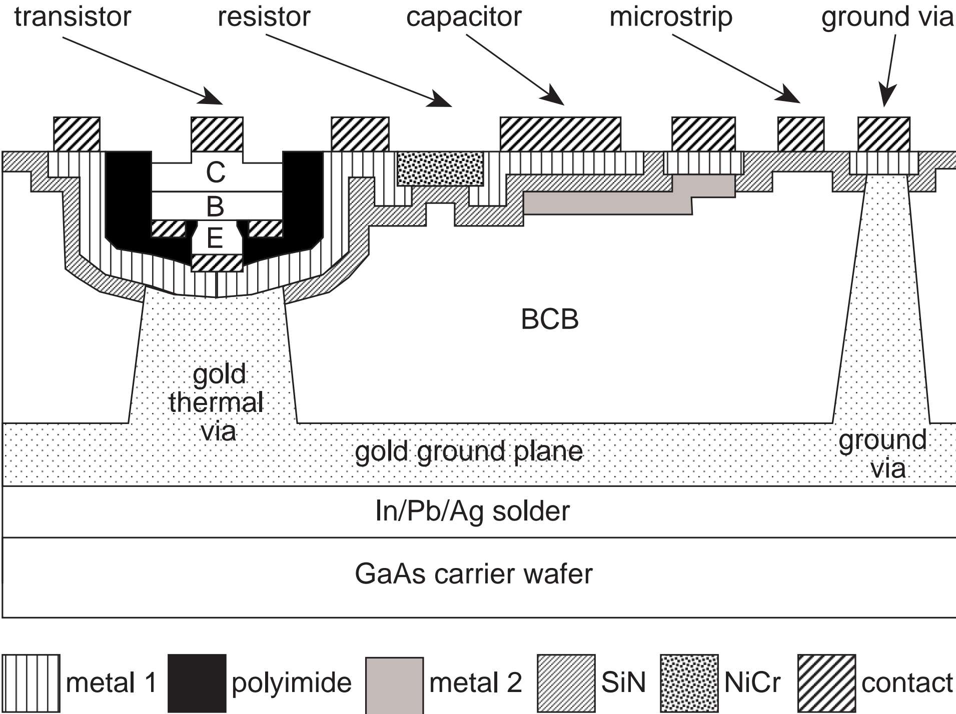


Figure 3.3: Fabrication process for transferred-substrate HBTs (contd.).

top GaInAs layer in the emitter-base grade. Lateral etching in this step reduces the emitter dimensions to below the lithographically defined area. The second wet etch is used to etch the 300 Å grade and expose the base GaInAs layer. This etch also reduces the lateral dimensions of the emitter. Figure 3.4 shows a SEM photomicrograph of the device cross-section after this step. The lateral undercuts can be seen in this cross-section.

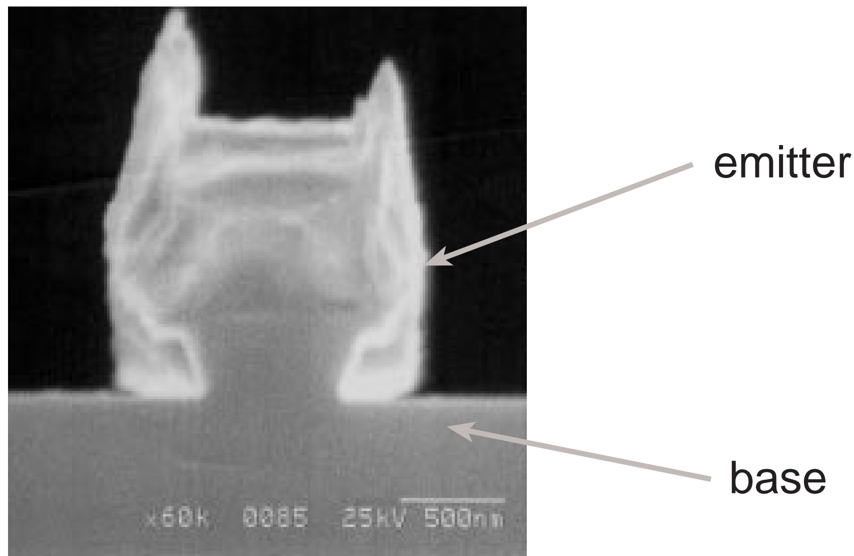


Figure 3.4: SEM cross-section of device after emitter-base etch.

Self-aligned Ti/Pt/Au base metal ($\sim$ 1000 Å thick) is evaporated and sintered at 300 °C for 1 minute. The base metal thickness is chosen to be less than the thickness of the undercut emitter layers to prevent electrical shorts between the emitter and base. Transistors are then isolated by forming mesas using a Cl_2/Ar RIE dry etch with photoresist as a mask, stopping on the AlInAs buffer layer. The process to this point is shown in figure 3.2(a). Thin film NiCr (500 Å) is evaporated on the wafer to form resistors with 50 $\Omega/\Box$ sheet resistivity. Several experiments were done to obtain the right thickness for a sheet resistivity of 50 $\Omega/\Box$. Resistors need to be passivated on either side (bottom and top). The bottom needs to be passivated because after substrate-transfer it will be exposed to air. Bottom passivation was achieved by evaporating 500 Å of SiO before evaporating NiCr. Top passivation is done either by polyimide or by SiN, both of which are used in subsequent steps and do not require any extra processing.

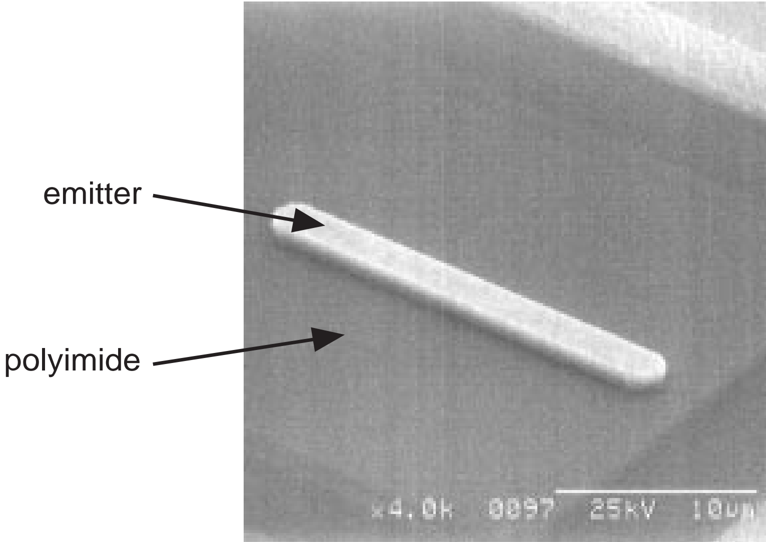


Figure 3.5: Polyimide planarization of the emitter finger.

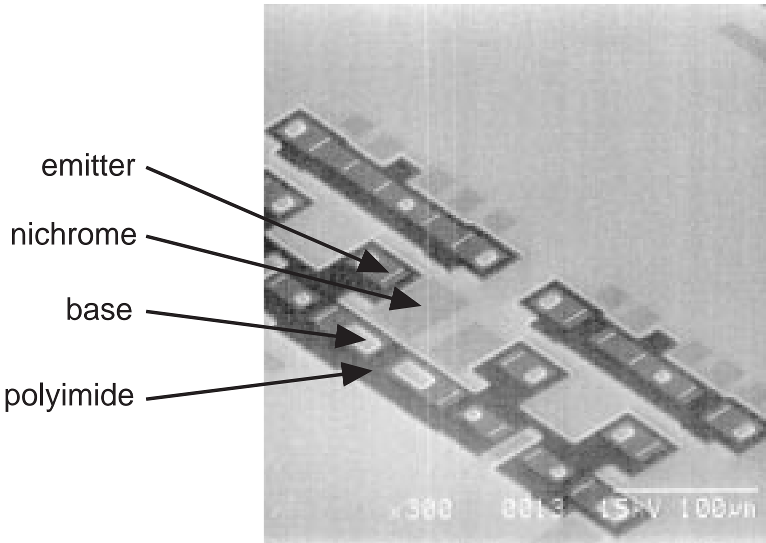


Figure 3.6: Wafer after polyimide etching.

The devices are passivated and planarized with polyimide in a dry O_2 RIE etch with photoresist as a mask. Figure 3.5 shows the emitter stripe after being planarized by polyimide. Polyimide also serves as interconnect crossovers for multiple wiring levels. After planarization, polyimide is left only around the devices (for passivation) and wherever metal-metal crossovers are required (figure 3.6). Reflowing the polyimide at 250 °C is done for ten minutes on a hot plate to round its edges for subsequent metal step coverage. The surface of the polyimide has to be smooth after the etch so that good subsequent lithogrpahy is possible on it. Smoothness is ensured by using a low etch rate by using low power in the RIE system.

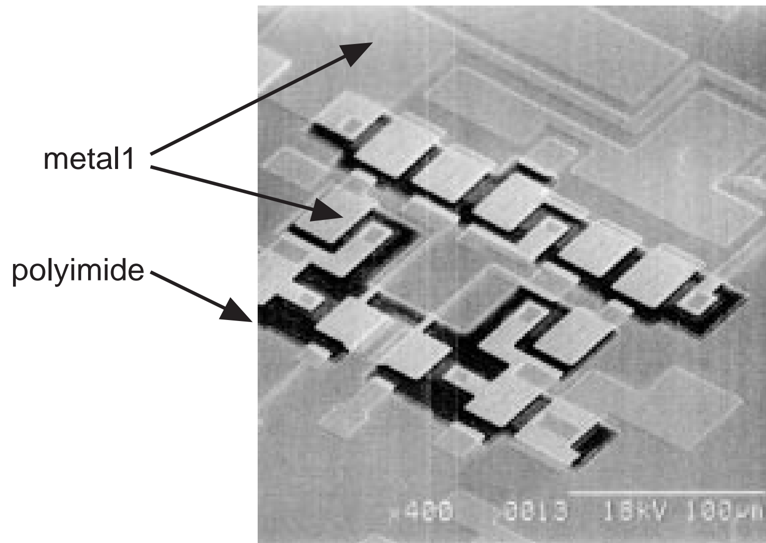


Figure 3.7: Wafer after the first level of metallization.

The first level of metallization (M1), Ti/Au/Ti (~ 1 μm thick) is evaporated at this point. Figure 3.7 shows a photomicrogrpah of the wafer at this point. This evaporation is done at an angle and with rotation of the wafer chuck to ensure adequate step coverage at the mesa and polyimide edges. Angle evaporation and rotation also give sloping edges in M1 which facilitate smooth subsequent crossovers. This metal forms most of the transmission lines, interconnect wiring, probe pads, capacitor bottom plate and resistor contacts. Emitters and bases are also contacted by this metal. The interface between NiCr and M1 needs thermal treatment for good contact. The exact temperature for this step was not determined in a separate ex-

periment, but a temperature of 250 °C that is used subsequently for other steps was found to be adequate (gives ∼ 0 contact resistance). Resistor measurements immediately after evaporation of M1 will show very high contact resistance.

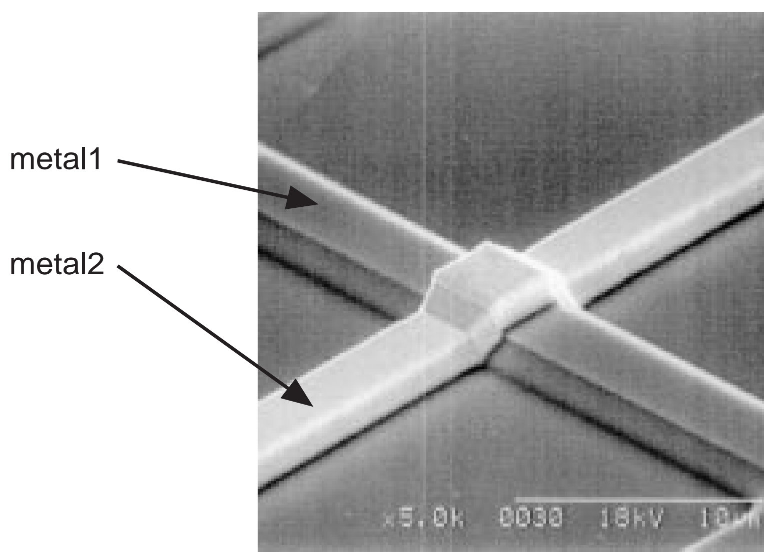


Figure 3.8: Wafer after second level of metallization.

SiN dielectric is then deposited over the entire wafer by PECVD at 250 °C. This dielectric serves three purposes : it forms the dielectric for metal-insulator-metal capacitors; it forms the insulator for crossovers between M1 and the second level of metallization; and, it forms a insulating layer over the whole wafer prior to the process of substrate transfer. These roles played by the SiN will become clear as we go through the process. The SiN is selectively etched away in some places with a $SF_6/O_2/Ar$ dry RIE etch, using photoresist as a mask. The purpose of this step is to expose the underlying M1 in some places, to be able to make contacts to it. The second level of metallization (M2) is done, similar to M1. M2 also forms the top plate for MIM capacitors. The process at this point is shown in figure 3.2(b). Figure 3.8 shows a crossover between M1 and M2. Note the sloping edges caused by angled evaporation of metal which enables smooth crossovers. Figure 3.9 shows photomicrograph of a wafer at this point. Figure 3.10(a) shows a photomicrograph of a device after this step.

The substrate transfer process starts by coating the wafer with a thick

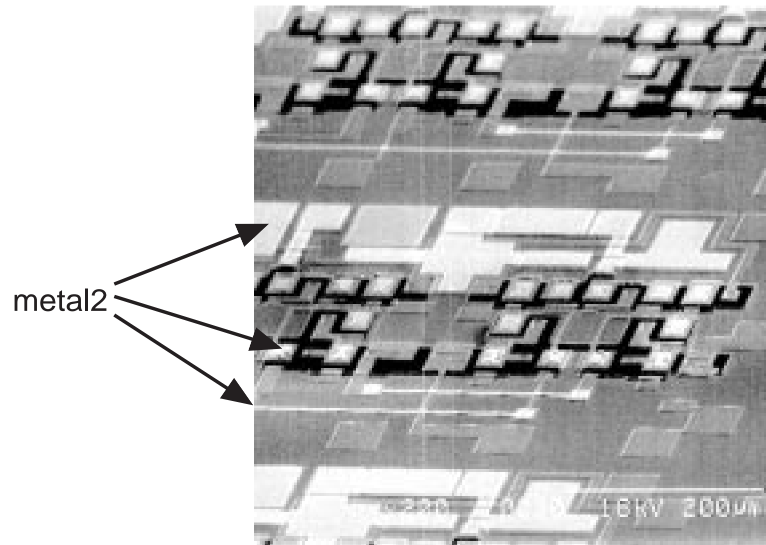


Figure 3.9: Wafer after M2 evaporation.

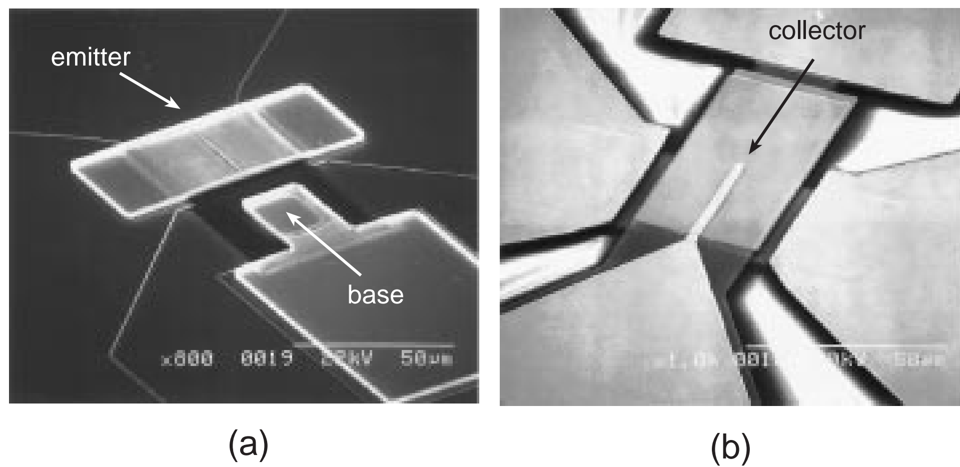


Figure 3.10: SEM photomicrograph of device after (a) partial fabrication and (b) complete fabrication.

($\sim$ 10 μm) layer of Benzocyclobutene (BCB, $\epsilon_r = 2.7$) and curing at a maximum temperature of 250 °C (with temperature ramp-up and ramp-down). Thermal vias on the emitters and ground vias are formed by dry etching openings in the BCB. A 200 Å thick Ni mask is used for this etch. Etching is done with SF_6/O_2 in a RIE system and results in a somewhat overcut profile. This etch also etches the SiN insulator layer in the vias. The Ni mask is removed with Ni etchant at 60 °C. A blanket BCB etch is done to cleanup the vias and to roughen the surface of BCB for good adhesion of the metals to follow. PECVD SiN is deposited on the backside of the wafer to prevent gold plating on the wafer backside in subsequent electroplating steps. The vias are then filled with thick Au ($\sim$ 10 μm) by electroplating. The electroplated Au also forms an electrically and thermally conducting ground plane, thus grounding all emitters.

Microstrip interconnect lines on BCB provide a low-capacitance wiring environment for dense circuits. Ground vias to the thick electroplated ground plane provide low ground return inductance. Thermal vias provide efficient heat-sinking for devices operating at very high current densities. Figure 3.2(c) shows the process at this point.

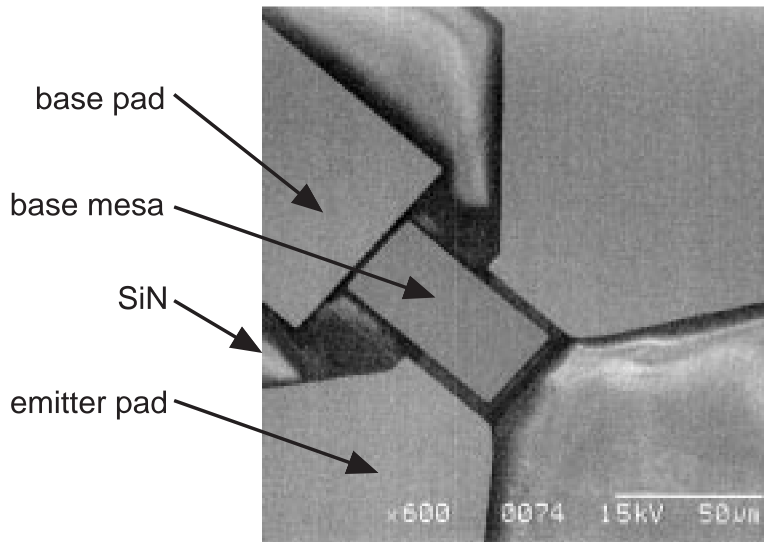


Figure 3.11: Wafer after InP substrate removal.

The wafer is then inverted and bonded to a GaAs transfer substrate (with sputtered Ti/Au on it) using a In/Pb/Ag solder at 180 °C. The solder

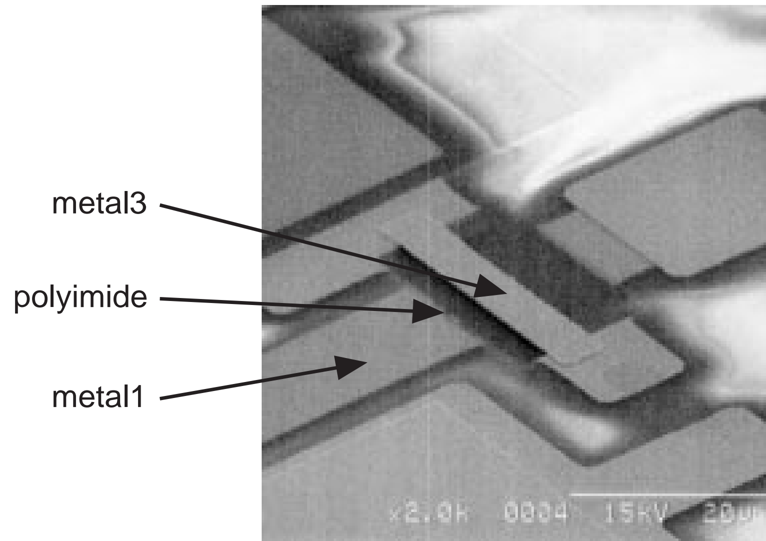


Figure 3.12: Wafer after collector (M3) evaporation.

should have a low melting point (lower than the curing temperature of preceeding polymers), should wet the electroplated Au surfaces when molten, have low stress, have good thermal conductivity and should be immune to the subsequent HCl etch. After experimenting with a variety of bonding materials, the In/Pb/Ag solder was chosen. This step is performed in a automated flip-chip bonder in order to ensure solder thickness uniformity and controlled bonding pressure and temperature. The backside SiN is etched away in buffered HF. The InP substrate is removed in an aqueous solution of HCl. The AlInAs buffer layer is also removed by the same etch thus exposing all the buried elements of the wafer. This etch stops selectively on the InGaAs collector layer. Figure 3.11 shows a photograph of a device after this step. Ti/Pt/Au Schottky collector contacts are then deposited. This metal layer could be used as a third level of metallization (M3), if needed, with polyimide as the insulator. Figure 3.12 shows such a crossover. Outside the active collector area, about 1500 Å of the collector drift region are then removed by a self-aligned wet etch to reduce collector-base fringing capacitance. This etch could also be done with reactive ion etching if more precise control (with a laser monitor) is needed for thinner collector layers. But, as explained before, a wet etch has the added advantage of lateral undercut thus further reducing the collector-base capacitance. The process

at this step is shown in figure 3.3. Figure 3.10(b) shows a photomicrograph of a completed device. Figure 3.13 (cross-section samples prepared by J. Guthrie) shows a SEM photomicrograph of the cross-section of an integrated circuit with active and passive components.

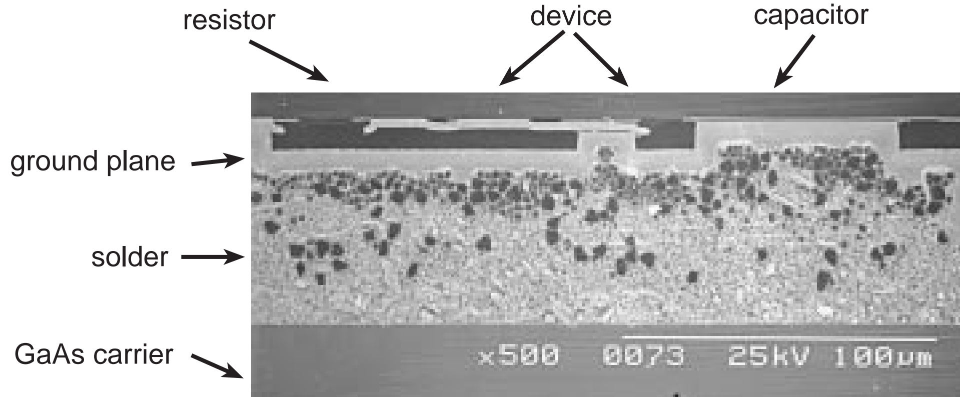


Figure 3.13: SEM photomicrograph of cross-section through an IC.

Transistors with non-grounded emitters (required in ICs) are fabricated by protecting the SiN insulator with M2 (figure 3.14) before applying BCB. As we can see, there is now a parasitic capacitance between the emitter of the device and the ground plane. This capacitance could be detrimental to circuit performance, depending on its value and the location of the device in a particular circuit. The magnitude of this capacitance will be estimated later. Power supply bypass capacitors could be formed similarly as shown in figure 3.14. On transistors not having the layer of M2, the SiN insulator is removed during the via formation etch, thus grounding the emitter. Figure 3.15 shows a SEM photomicrograph of the cross-section of a fully fabricated device with a non-grounded emitter.

The thickness of the SiN layer needs to be designed carefully. Thin layers give higher capacitance per unit area for MIM capacitors, thus making large on-wafer capacitors possible. In addition, thin layers also facilitate heat-sinking from the device because of lower thermal impedance. At the same time, thin layers increase the parasitic emitter-to-ground capacitance for devices with non-grounded emitters, which could become important in some circuit topologies. If large capacitors are needed and the emitter-to-ground capacitance cannot be tolerated, thin insulator for MIM capacitors can be

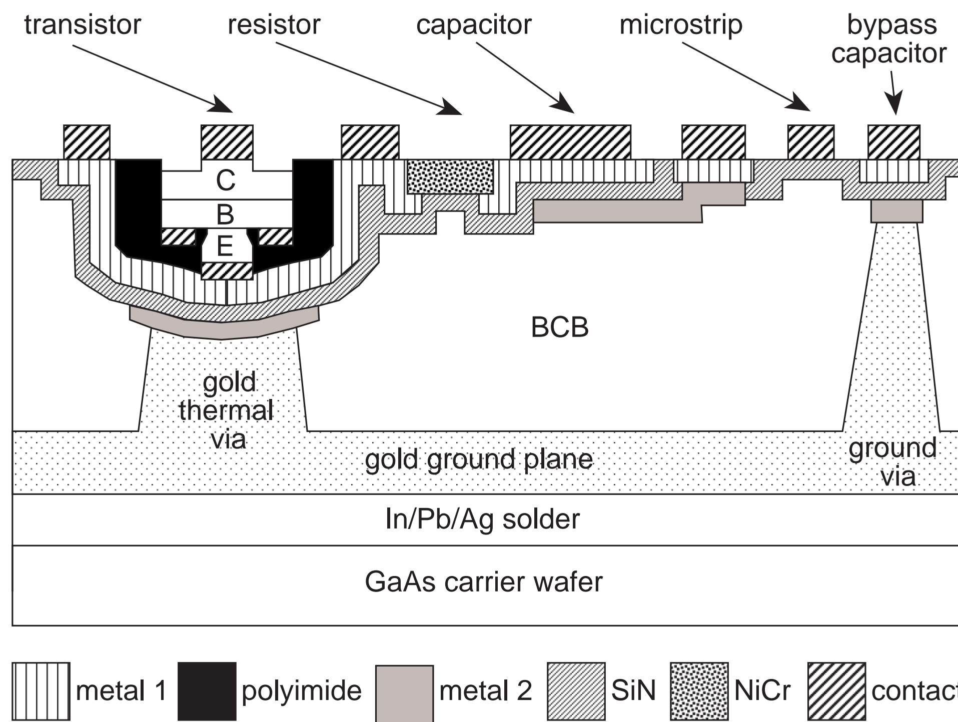


Figure 3.14: Fabrication process for devices with non-grounded emitters.

deposited in a separate step from the thick insulating layer used for the HBT.

Devices with non-grounded emitters should have similar performance and heat-sinking as the devices with grounded emitters. SiN has $\epsilon_r = 6$ and $\sim$ 10-30 W/m-K thermal conductivity depending upon PECVD deposition conditions. In the work reported here, for an HBT with a 0.8 $\times$ 25 μm^2 emitter, the thermal via is 10 $\times$ 24 μm^2. For non-grounded emitter devices, the calculated capacitance from the emitter airbridge to the grounded substrate is 25 fF (for 4000 Å SiN), which is much smaller than 730 fF base-emitter capacitance. The calculated 67-200 K/W thermal resistance of the SiN layer should result in less than 3.5 °C additional temperature rise for a device biased at 10^5 A/cm^2 and 1.0 V.

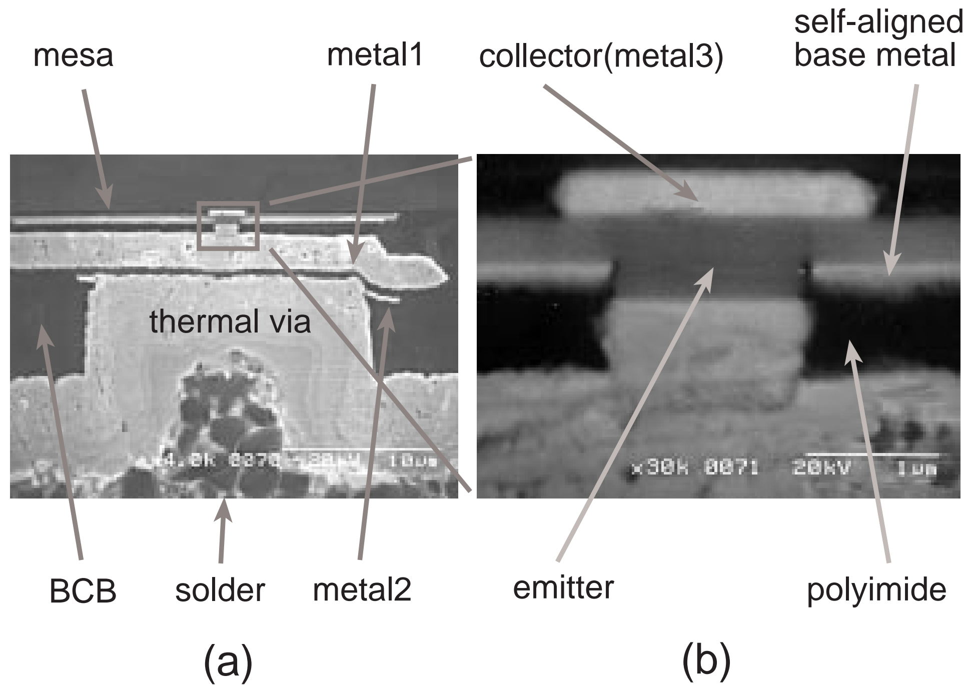


Figure 3.15: SEM photomicrograph of (a) cross-section through a device and (b) close-up of intrinsic device.

For integrated circuit applications, high device yield is required. The transferred-substrate HBT IC technology is constantly being improved towards this goal. The technology is currently capable of yielding circuits

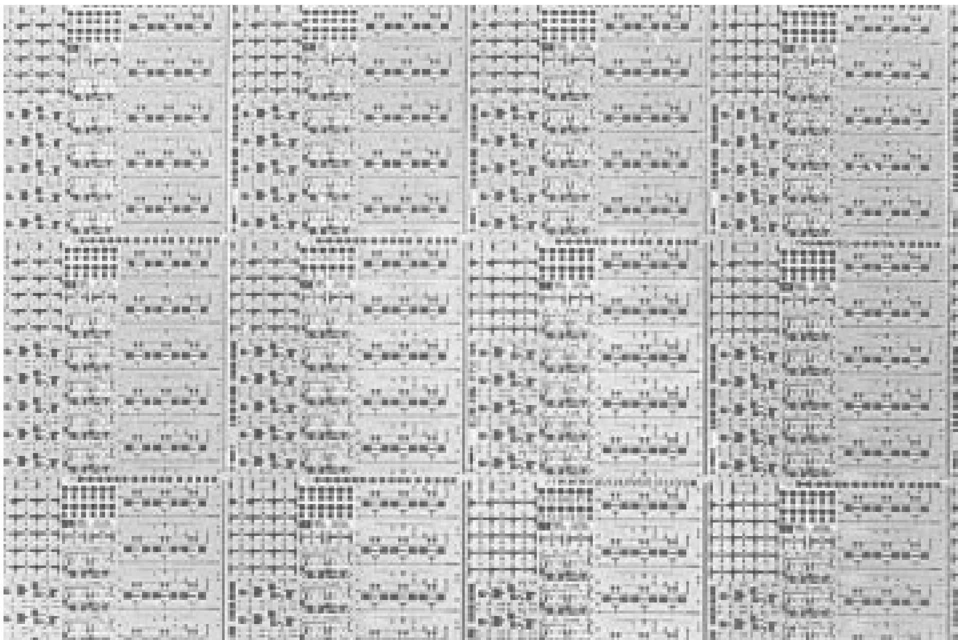


Figure 3.16: Photomicrograph of part of a wafer with ICs and discrete devices.

with few tens of transistors. Figure 3.16 shows a photograph of part of a recent wafer with discrete devices and integrated circuits. Quarters of 2-in round wafers were processed in this work with good unformity.

One important requirement of the transferred-substrate HBT IC process is that of alignment between the emitter and collector stripes. Currently, contact aligners with $\sim$ 1 μm linewidth and alignment capability are being used. Even so, over a large wafer (quarter of a 2-inch wafer) it is very difficult to achieve perfect alignment. In addition, the (quarter of 2-inch) wafer shrinks by few microns due to accumulated stress from the stacked up layers of BCB, electroplated Au and solder. To obtain working devices and circuits in spite of these problems, "staggering" is used in the mask layout. This involves having an array of similar devices or circuits next to each other, but with the emitter and collector deliberately and successively misaligned in steps of 0.5 μm and by a maximum of 1.5 microns. This ensures that at least one device or circuit in the array is well aligned and functions as expected. The other repetitions of the same device or circuit will be misaligned and will thus have poor characteristics. As a result, about 80 % of the wafer area is wasted. Discounting the deliberate misalignment, the *circuit* yield even on circuits with as many as twenty-two transistors was very high.

To obtain higher scales of integration, the alignment and wafer shrinkage problem should be addressed. The alignment problem is addressed by use of better lithographic tools (e.g. projection lithography systems). UCSB has recently acquired a wafer stepper with $\sim$ 0.5 μm resolution and $\sim$ 0.2 μm alignment tolerance. This system would avoid the need for staggering devices and circuits, thus saving wafer area. Smaller tolerances between layers will also enable more dense layout. The issue of wafer shrinkage can be addressed by either of two methods : J. Guthrie has developed an enhanced transfer substrate process in which the solder and carrier wafer are replaced by electroplating of Cu, thus forming a $\sim$ 200 μm thick copper substrate; alternatively, small levels of shrinkage can be compensated for by adjustment of the collector mask dimensions.

The transferred-substrate HBT IC fabrication process was developed. Several wafers with a variety of devices and integrated circuits were processed. Process development is closely tied with measurements, both during and at the end of the process to evaluate the MBE material, device structure and other elements of the IC process. Device measurements over a variety

of bias conditions are also required to model the device to be able to design integrated circuits with the devices. These measurements are presented in the next chapter.

Chapter 4

Device Results

A multitude of measurements both during the process and after completion of the process are needed for process development and process and material evaluation and characterization. A variety of devices were fabricated with different emitter and collector widths. Other device structures like common-base devices, devices with non-grounded emitters, devices with non-self-aligned emitter and base, and devices without thermal vias were also fabricated. Diagnostic structures like TLM patterns and large-area emitter-base and collector-base diodes are included. Passive structures to measure thin-film NiCr sheet resistivity, MIM capacitors, microstrip transmission lines and open and shorted microwave probe pads to measure pad parasitics were designed. For on-wafer calibration during network analysis for microwave measurements, open, short, thru and 50 Ω load standards were also designed. In addition to the process test structures mentioned above, various types of device measurements are done after completion of the process. These include dc measurements (Gummel, I-V characteristics and breakdown) and RF measurements (at varying bias). Parameter extraction can then be done based upon these measurements.

(a)	(b)	(c)
InAs 250 Å $3 \cdot 10^{19}$ Si		
GaInAs 250 Å $3 \cdot 10^{19}$ Si		
GaInAs 500 Å $1 \cdot 10^{19}$ Si		GaInAs 1000 Å $1 \cdot 10^{19}$ Si
Grade 66 Å	GaInAs 1000 Å $1 \cdot 10^{19}$ Si	Grade 66 Å
AlInAs 834 Å $1 \cdot 10^{19}$ Si	Grade 66 Å	AlInAs 834 Å $1 \cdot 10^{19}$ Si
AlInAs 500 Å $8 \cdot 10^{17}$ Si	AlInAs 834 Å $1 \cdot 10^{19}$ Si	AlInAs 500 Å $8 \cdot 10^{17}$ Si
Grade 300 Å	AlInAs 500 Å $8 \cdot 10^{17}$ Si	Grade 300 Å
GaInAs 500 Å $5 \cdot 10^{19}$ Be	Grade 300 Å	GaInAs 300 Å $5 \cdot 10^{19}$ Be
GaInAs 400 Å $1 \cdot 10^{16}$ Si	GaInAs 400 Å $5 \cdot 10^{19}$ Be	GaInAs 100 Å $3 \cdot 10^{19}$ Be
GaInAs 50 Å $1 \cdot 10^{18}$ Si	GaInAs 400 Å $2 \cdot 10^{16}$ Si	GaInAs 400 Å $2 \cdot 10^{16}$ Si
GaInAs 2550 Å $1 \cdot 10^{16}$ Si	GaInAs 50 Å $1 \cdot 10^{18}$ Si	GaInAs 50 Å $1 \cdot 10^{18}$ Si
AlInAs 1000 Å $1 \cdot 10^{16}$ Si	GaInAs 2050 Å $1 \cdot 10^{16}$ Si	GaInAs 2250 Å $1 \cdot 10^{16}$ Si
GaInAs 1000 Å $1 \cdot 10^{16}$ Si	AlInAs 2500 Å UID	AlInAs 2500 Å
AlInAs 1000 Å UID	S. I. InP	S. I. InP
S. I. InP		

Figure 4.1: MBE layer structures of wafers A, B & C.

Parameter	Wafer A	Wafer B	Wafer C
emitter width	0.7 μm	0.8 μm	0.75 μm
collector width	1.6 μm	1.8 μm	1.8 μm
bond medium	epoxy	solder	solder
graded base	no	yes	yes
transit time	0.95 ps	0.66 ps	0.67 ps
base resistance	7 Ω	12 Ω	8 Ω
collector etch-stop	yes	no	no

Results from three different wafers A, B and C will be presented here. The material and process used in these three runs are similar to that described in chapter 3, but not identical. Figure 4.1 shows the MBE layer structures of the three wafers. The important process differences between the three wafers are also shown in the table above. Devices were fabricated with nominal emitter dimensions of 1 μm $\times$ 25 μm and with nominal collector dimensions of 1 μm (narrow-collector) and 2 μm (wide-collector) $\times$ 29 μm. The actual areas of the emitters and collectors are somewhat lower than their nominal areas due to lateral undercuts caused by wet chemical etches. Devices with very wide collectors ($\sim$ 5 μm, very-wide-collector),

as is normally the case in double-mesa HBTs, were also fabricated. All devices have their emitters grounded by thermal vias, except where explicitly stated.

It is important in characterization to determine the emitter-base and collector-base junction areas fairly accurately. Wet chemical etches with lateral undercuts are used to reduce both the emitter-base and collector-base junction areas to below their lithographically defined dimensions. Junction dimensions can be determined in two ways : 1) by measuring (with a microwave network analyzer) the junction capacitance and comparing with known specific junction capacitance from large area junction measurements and 2) by measuring resistance of specially designed TLM structures. The second method will be explained in detail.

4.1 Test structures

TLM test structures are used to measure sheet and contact resistivities. Two kinds of TLM patterns were used. Figure 4.2 shows these patterns.

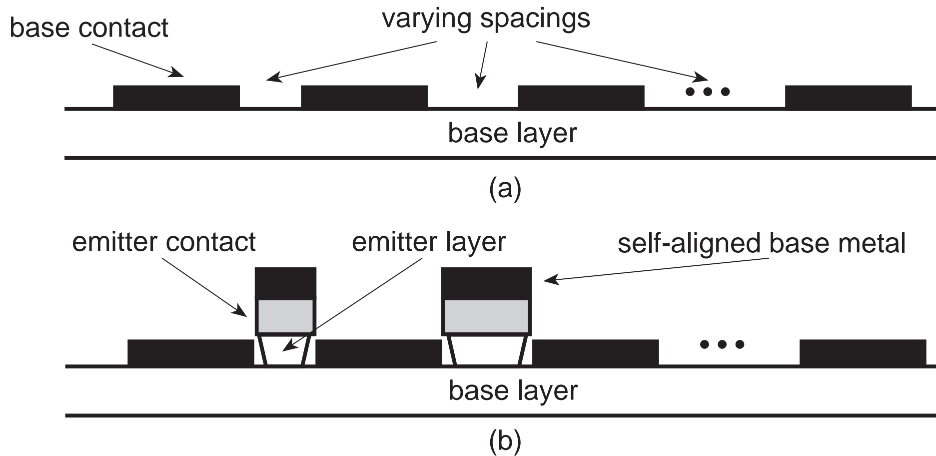


Figure 4.2: TLM patterns (a) normal and (b) with emitters.

The measured resistance of normal TLM patterns consist of contact resistance between the base layer and base metal and sheet resistance from the base layer. The different gaps will have the same contact resistance but different sheet resistances depending on the separation between base metal

pads. Sheet resistance depends mainly on the doping and layer thicknesses. Contact resistance depends on the doping, the sintering conditions and the interaction between the semiconductor and metal.

Figure 4.2(b) shows *pinched* or *emitter* TLM patterns, where emitters are present in the gaps between base metal pads. These TLM patterns are very similar to transistor emitter-base junctions, and should accurately determine the lateral undercut and base resistance. Measured resistance consists of contact resistance (same as normal TLMs), gap sheet resistance and base layer sheet resistance under the emitter. The following equations relate the terminal resistances to TLM dimensions and resistivities. For normal TLMs :

$$R_{normal} = 2\sqrt{\rho_{bc}\rho_{bs}}/L + \rho_{bs}W/L \tag{4.1}$$

where ρ_{bc} is the specific contact resistance per unit area of the metal-semiconductor interface (units of Ω-cm^2), ρ_{bs} is the base sheet resistivity (units of $\Omega/\Box$), W is the gap width and L is the length of the pad/gap. L is known, and from a plot of measured resistance *vs.* gap width, all the other quantities can be determined. For pinched TLMs :

$$R_{pinched} = 2\sqrt{\rho_{bc}\rho_{bs}}/L + \rho_{bse}W_e/L + 2\rho_{bs}W_{gap}/L \tag{4.2}$$

where W_e is the width of the emitter mesa, W_{gap} is the separation between the emitter mesa and the base Ohmic contact and ρ_{bse} is the sheet resistivity of the base layer under the emitter. Note that :

$$W = W_e + 2W_{gap} \tag{4.3}$$

From these equations all quantities can be determined. Figure 4.3 shows the variation of measured normal and pinched TLM data from a recent wafer with a 400 Å thick base layer. Using the above equations, the calculated quantities are shown below. It is important to note that for the emitter-TLMs, the measured resistance is plotted *vs.* the lithographic emitter width W which is not strictly true; we need to plot the measured resistance *vs.* the actual emitter width W_e. Hence, the equations have to be solved iteratively.

$\rho_{bs} = 795\ \Omega/\Box$
$\rho_{bc} = 6 \times 10^{-7}\ \Omega - \mathrm{cm}^2$
$\rho_{bse} = 647\ \Omega/\Box$

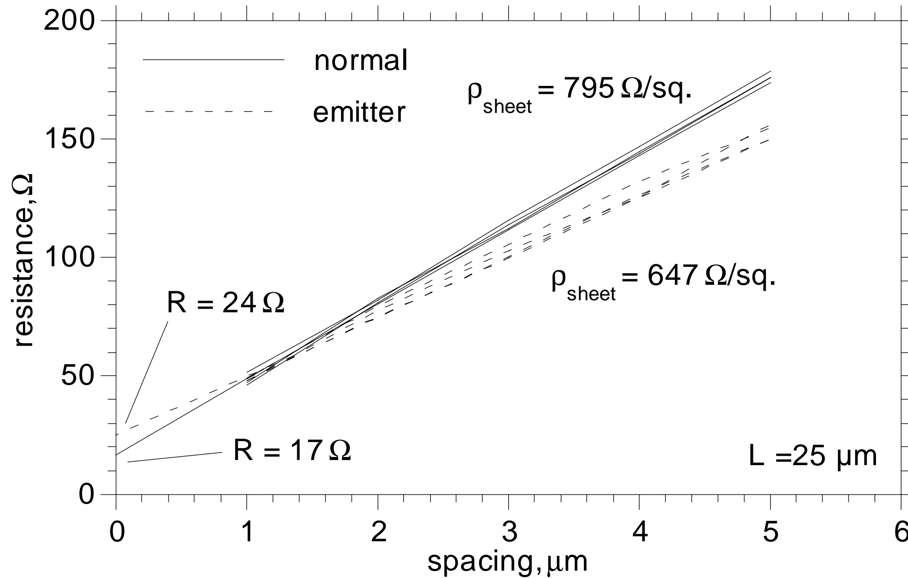


Figure 4.3: TLM measurements for normal and pinched TLMs across a quarter of a 2-inch wafer with a 400 Å thick base doped at $5 \times 10^{19}/cm^2$.

$W_{gap} = 0.1\ \mu$m

A vital point to note is that if the emitter-base etch stopped exactly on top of the base layer, ρ_{bs} and ρ_{bse} should be the same. The discrepancy between these two quantities is an indication of the etch depth. From the values calculated above, we can estimate that the final base thickness is $\simeq 400 \times 647/795 = 326$ Å.

An array of resistors was designed to measure NiCr sheet and contact resistivity. This array was also used to measure the current capacity. In the array, both the width and the length of the resistors was varied, thus yielding resistors or varying values. The sheet resistivity of thin-film NiCr is mainly determined by its thickness. Figure 4.4 shows the variation of resistor values in the array. For a NiCr thickness of 500 Å the sheet resistivity and contact resistivity are 50 $\Omega/\Box$ and zero respectively.

The current capacity of resistors was determined by burning the resistors with a current source. Figure 4.5 shows the current capacity of resistors in the array. The current capacity is mainly determined by the heat dissipation

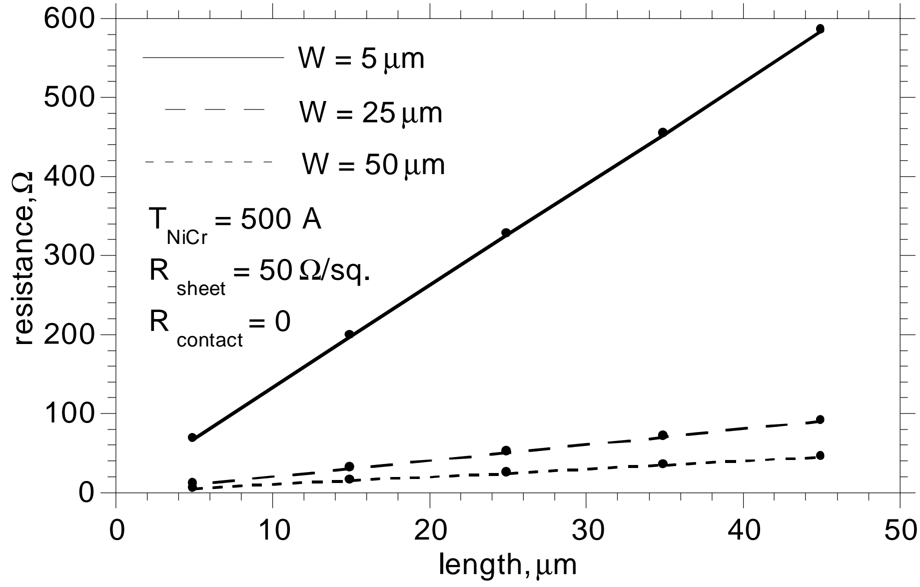


Figure 4.4: Variation of resistance with length and width for NiCr resistors.

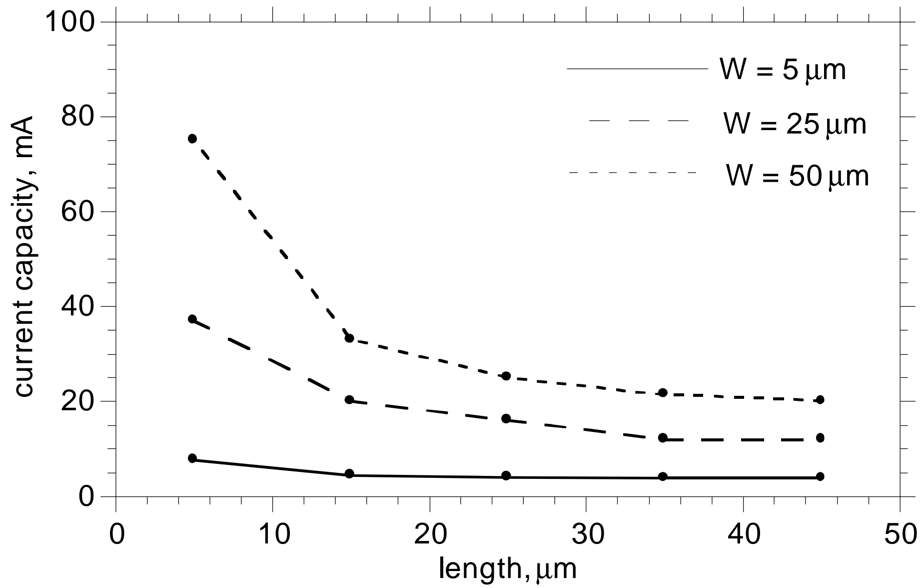


Figure 4.5: Current capacity of NiCr resistors for varying geometry.

around the resistor. The heat dissipation around the resistor is not very good as it is encapsulated with polymers. As it can be seen, the current capacity does not follow any empirical relationship with resistor width or length but is related in a rather complex way. In designing resistors in a circuit, individual current capacities need to be used from this graph. It was also found that passivation with SiO, SiN or polyimide or even with GaInAs did not make much difference in the current capacity. A thermal via (as in the devices) is needed to improve the current capacity of resistors and this has recently been demonstrated.

The capacitance of SiN MIM capacitors was determined by measuring capacitors of varying geometry (measured by O. Wohlgemuth). This value was found to be about 0.23 fF/μm^2 for a SiN thickness of 2000 Å, which gives $\epsilon = 5.2$ for SiN. The size of capacitors is limited by pinhole formation during the SiN deposition. The largest capacitor that was fabricated had an area of 150 μm $\times$ 100 μm. The yield on this capacitor was close to 100 % on a quarter of a 2-in wafer. Quantitative determination of capacitor area *vs.* yield has not been done at this point.

4.2 DC measurements

Figure 4.6 shows the Gummel plots of transferred-substrate HBTs. The collector current ideality factor n_c is close to unity. The base current ideality factor n_b is 1.2. All three wafers A, B & C have similar Gummel plots. The divergence of the curves at $\sim 10^{-9}$ A implies that I_{CBO} is about 1 nA. The collector width does not affect Gummel plots as expected, at least up to medium current densities. At high current densities, devices with different collector areas will exhibit the Kirk effect at different currents and current gain will drop earlier for narrow collector devices.

DC common-emitter characteristics of HBTs from wafer A are shown in figure 4.7. There were no narrow-collector or very-wide-collector devices on this wafer. The GaInAs base on this wafer is graded neither in doping nor in bandgap. Also this device was fabricated early in our HBT development efforts and substrate transfer was done using a die-attach epoxy instead of the In/Pb/Ag solder discussed earlier. The emitter and collector dimensions are 0.7 μm $\times$ 25 μm and 1.6 μm $\times$ 29 μm respectively. The small signal current gain at DC, β, is 27. The device shows high saturation voltages at high operating currents because of space charge screening effect in

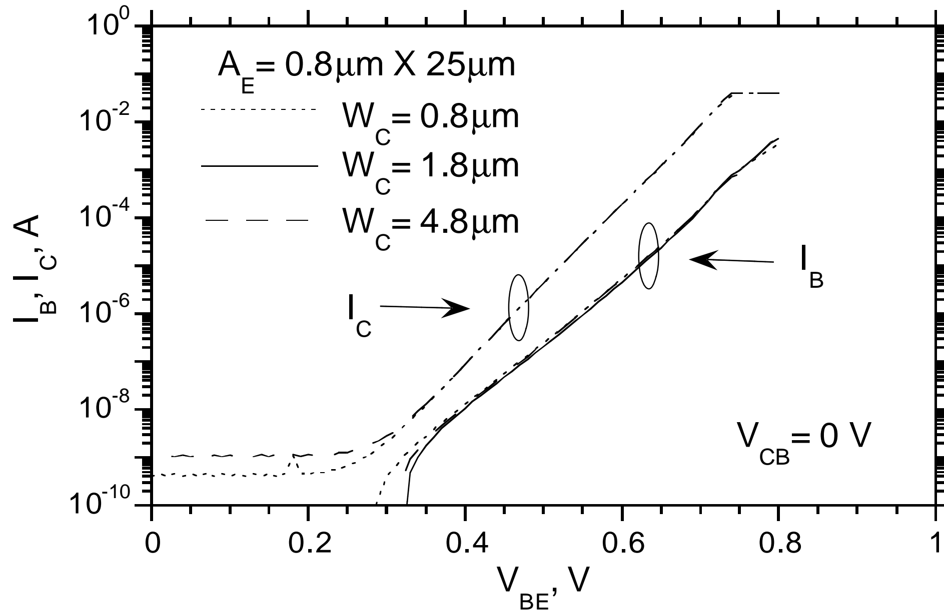


Figure 4.6: Gummel plots of transferred-substrate HBTs with 0.8 μm $\times$ 25 μm emitters and 29 μm long collectors of different widths.

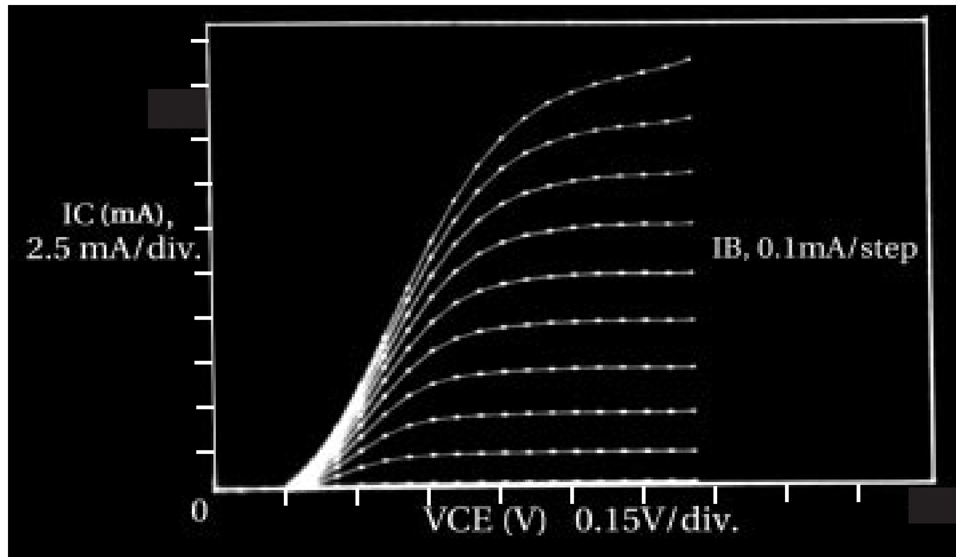


Figure 4.7: DC common-emitter characteristics of devices on wafer A with 0.7 μm $\times$ 25 μm emitters and 1.6 μm $\times$ 29 μm collectors.

the narrow collector-base junction. At higher current densities, the devices show significantly larger collector-emitter saturation voltages ($V_{CE,sat}$), arising from screening of the collector electrostatic field by the electron space charge. Screening occurs at a *collector* current density J_C satisfying the relationship [31] $(V_{CB} + \phi) = T_C^2(J_C/v_{sat} - qN_d)/2\epsilon$, where T_C is the collector depletion layer thickness, N_d the collector doping, ϕ the junction built-in potential, and v_{sat} the electron velocity. In wide-collector HBTs, there is significant lateral spreading of the electron flux at high current densities [44], reducing the collector space-charge density. Lateral current confinement in narrow-collector HBTs results in both increased $V_{CE,sat}$ and decreased emitter current density at the onset of f_τ collapse (Kirk effect), resulting in increased emitter charging times and reduced f_τ. This effect is explained in more detail in [31].

DC common-emitter characteristics of three different HBTs from wafer B (same as wafer C) are shown in figure 4.8. The three sets of curves correspond to narrow-collector (0.8 μm), wide-collector (1.8 μm) and very-wide-collector widths respectively. The small signal current gain at DC, β, is 65. The reason for higher β on these wafers compared to wafer A has not been fully explored. Two significant factors contribute to this observation. The degree of etch undercut during the emitter-base etch sets the separation between the edge of the emitter mesa and the base contact metal, controlling the magnitude of the base leakage currents. Further, the graded base decreases the base transit time, thereby decreasing the injected electron density required for a given collector current. Surface recombination currents are therefore reduced.

The effect of collector width on the collector-emitter saturation voltage can be seen by comparing the three sets of curves. If the collector is wide, the collector current density at a given current is lower, hence leading to less space charge screening in the collector and lower saturation voltage and a smaller space charge resistance (slope of I-V curve in the linear region). The effect of the collector width on the Kirk effect threshold is not very obvious here as neither device is in that regime even at the highest measured collector current. This delayed Kirk effect is due to the pulse-doped layer in the collector as explained earlier.

The slope of the I-V characteristics in the saturation region can be used to calculate the saturated electron velocity in the collector. Using the relationship $(V_{CB} + \phi) = T_C^2(J_C/v_{sat} - qN_d)/2\epsilon$ and taking its derivative

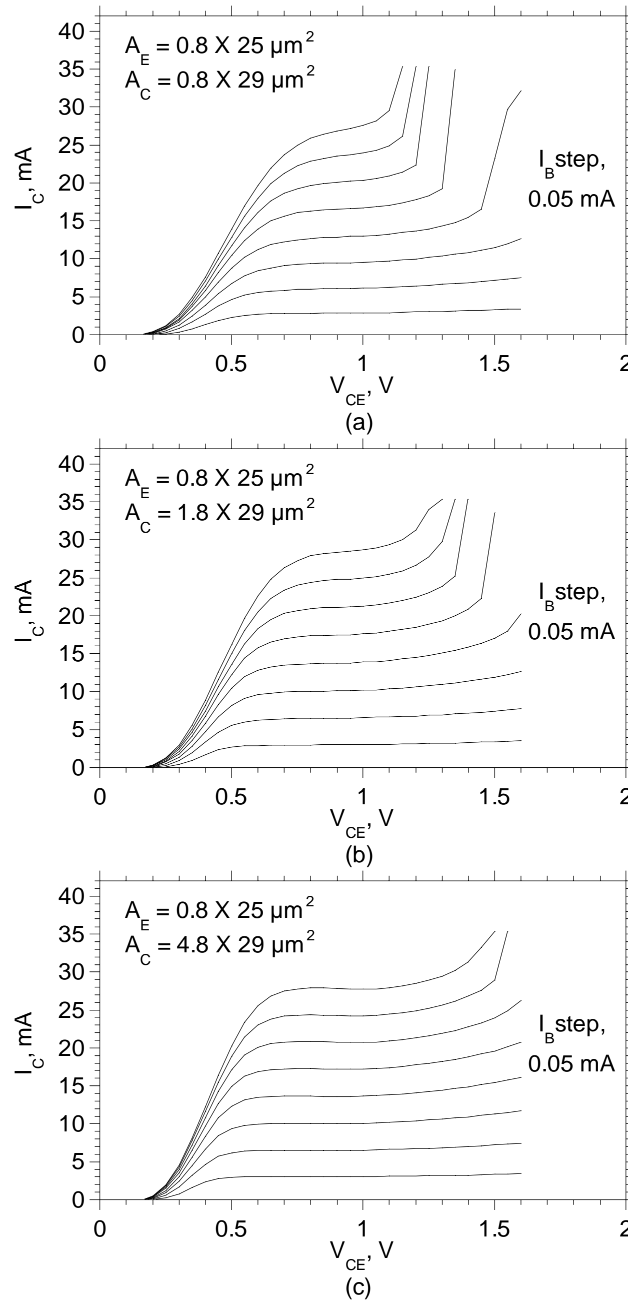


Figure 4.8: DC common-emitter characteristics of devices on wafer B with 0.8 μm $\times$ 25 μm emitters and (a) 0.8 μm $\times$ 29 μm collectors, (b) 1.8 μm $\times$ 29 μm collectors and (c) 4.8 μm $\times$ 29 μm collectors.

yields

$$R_{sc} = {T_c}^2 / 2\epsilon v_{sat} A_c \tag{4.4}$$

where R_{sc} is the space charge resistance (inverse of the slope of the I-V curve in saturation), T_c is the collector layer thickness, v_{sat} is the saturated electron velocity and A_c is the collector area. Using values for a wide-collector device from wafer B, the space charge resistance is found to be $\sim$ 15 Ω and the saturated electron velocity in the collector is calculated to be 3×10^5 m/s.

The common-emitter breakdown voltage BV_{CEO} is $\sim$ 3 V, decreasing to 1.5 V at 10^5 A/cm^2. The low breakdown voltage is due to the narrow-bandgap InGaAs collector material. InP collectors with a InGaAs/InAlAs linear grade would provide superior breakdown [45]. Our current facilities do not permit InP growth. Given that vertical scaling must accompany lateral scaling to obtain commensurate improvement in both f_τ and f_{max}, scaled 0.1 μm devices will demand very thin (1500-2000 Å) collectors, and InP must be employed.

The collector recess etch also affects DC characteristics of transferred-substrate HBTs. If the collector is not recess etched, the electrons spread laterally in the collector to regions where there is no collector contact underneath, due to the electron space charge. Once the electrons spread into regions of lower field (outside the collector contact), they need a higher vertical field to reach the collector contact. Hence, the saturation voltage increases. After recess etching, the electrons are physically confined to the area under the collector contact thus reducing $V_{CE,sat}$. Since the collector current is now confined to a smaller area, the collector current density for a given collector current increases. This should cause the onset of the Kirk effect at lower currents. This effect is presented in more detail in [31].

DC characteristics of the devices with 0.8 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors were measured in the common-base configuration also. Figure 4.9 shows these characteristics. The common base current gain α is 0.98. The common-base breakdown voltage BV_{CBO} is $\sim$ 6 V, decreasing to 1.5 V at 10^5 A/cm^2.

To investigate the effect of the thermal via on transistor performance, we now compare the DC characteristics of devices with non-grounded emitters (with thermal vias) and devices without thermal vias. Three devices are compared. All have 0.8 μm $\times$ 25 μm emitters and 4.8 μm $\times$ 29 μm

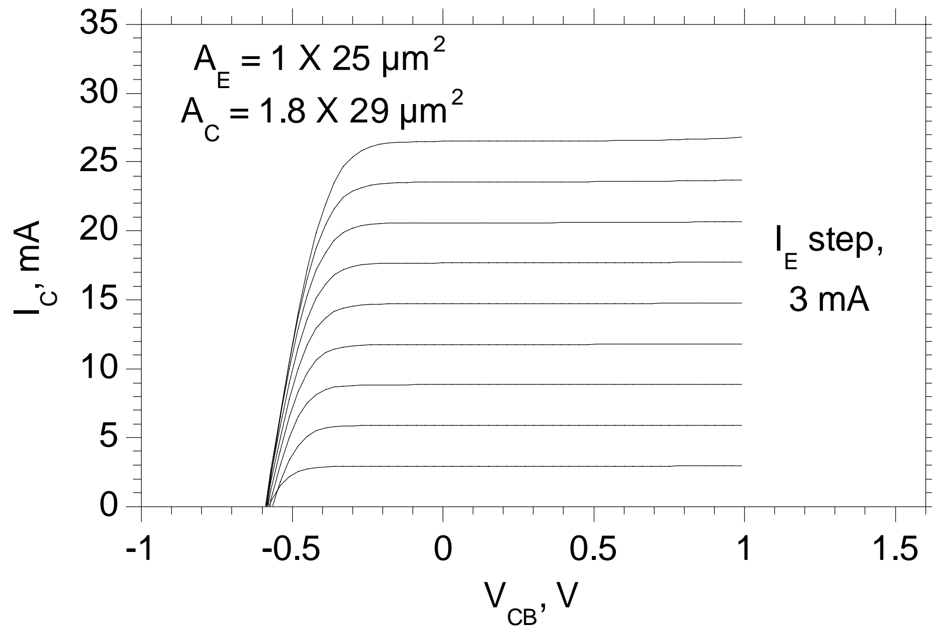


Figure 4.9: DC common-base characteristics of devices with 0.8 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors.

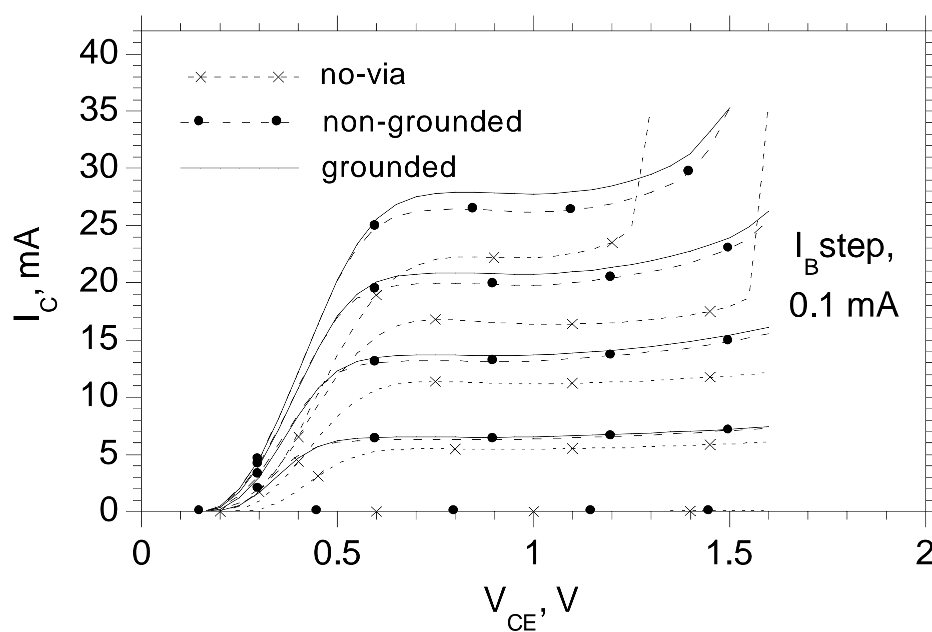


Figure 4.10: DC common-emitter characteristics of device with different heat-sink structures; emitter and collector dimensions are 0.8 μm $\times$ 25 μm and 4.8 μm $\times$ 29 μm respectively.

collectors. The first device has its emitter grounded with a thermal via (grounded), the second device has M2 to protect the insulator layer (non-grounded), and, the third device does not have a thermal via (no-via). Figure 4.10 shows their common-emitter characteristics. The observed variation in β is attributed to transistor self-heating. There is very little difference between the grounded and non-grounded devices, as was expected from the temperature calculations in the previous section. The no-via device has lower breakdown voltage, lower current gain and higher collector-emitter saturation voltage due to self-heating effects. Hence, a thermal via is essential at the current densities required for high transistor bandwidth operation.

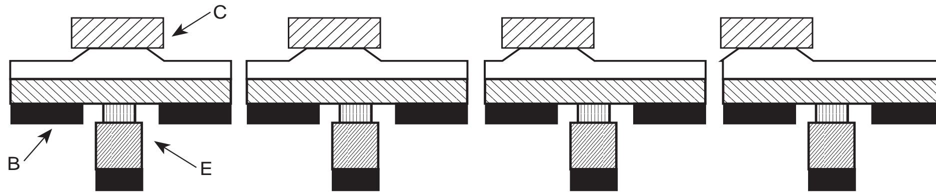


Figure 4.11: An array of devices with the collector offset from the emitter in steps of 0.5 μm.

For transferred-substrate HBTs, the emitter-base and collector-base junctions have to be aligned to each other. If they are misaligned, both the device DC and RF performance degrade. The lateral electron flow increases transit times and space charge screening in the collector. An array of four devices with identical dimensions was tested. In the first device, the emitter and collector stripes are aligned, but in the other devices the collector stripe is offset from the emitter successively in steps of 0.5 μm (figure 4.11). Common-emitter DC characteristics of the four devices are shown in figure 4.12. As we can see by comparing the four graphs, misaligned devices have lower current gain and higher collector-emitter saturation voltages at higher current densities.

4.3 RF measurements

The devices were characterized by on-wafer network analysis to 50 GHz. Figure 4.13 shows the short-circuit current gain h_{21}, and Mason's [32] in-

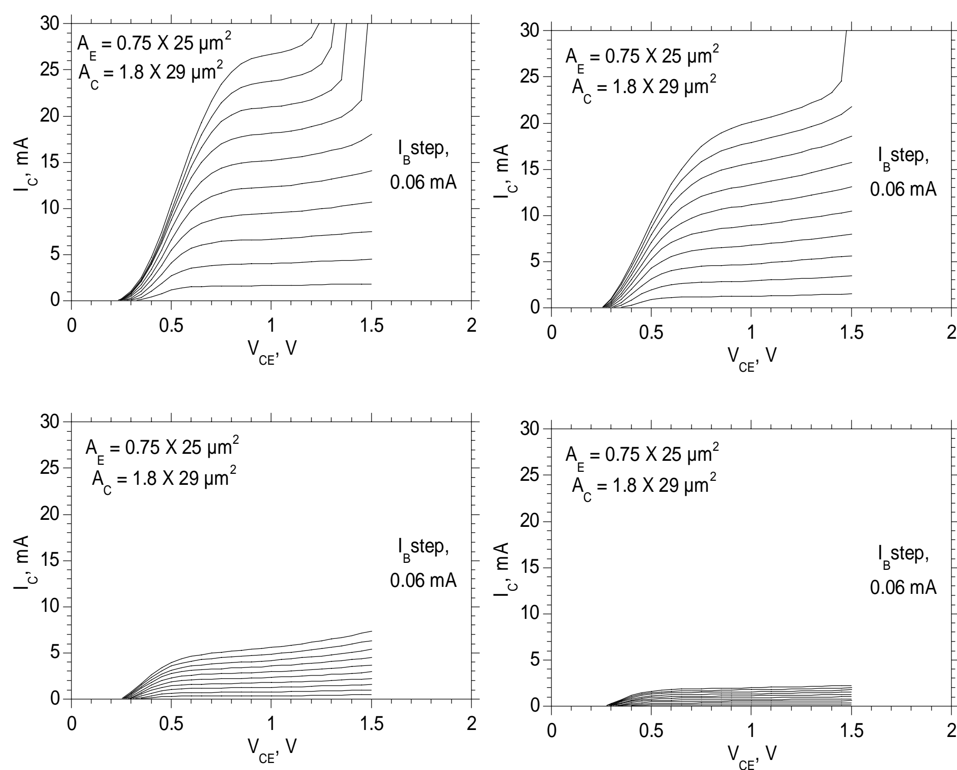


Figure 4.12: Effect of misalignment (0 μm to 1.5 μm) between emitter and collector on DC common-emitter characteristics of devices.

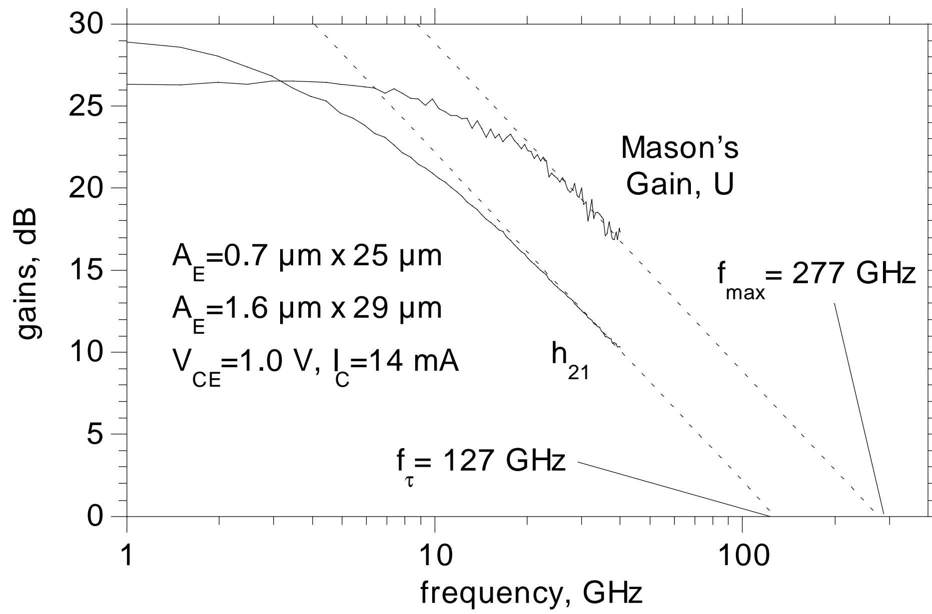


Figure 4.13: RF characteristics of devices from wafer A with 0.7 μm $\times$ 25 μm emitters and 1.6 μm $\times$ 29 μm collectors.

variant (unilateral) power gain U for devices from wafer A. Pad parasitics have not been stripped. Bias conditions are as shown. Extrapolating at -20 dB/decade, $f_{max} = 277$ GHz and $f_\tau = 127$ GHz. We have used Mason's gain for extrapolating f_{max} because of its characteristic -20 dB/decade slope, its independence of the transistor configuration (common-base *vs.* common-emitter), and its independence of pad inductive and capacitive parasitics.

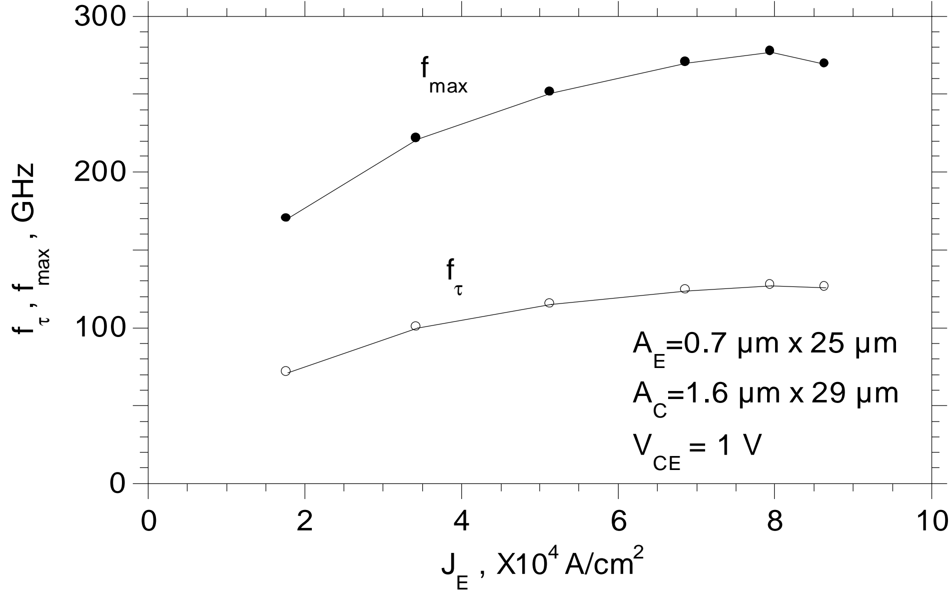


Figure 4.14: Variation of f_τ and f_{max} with emitter current density for devices on wafer A.

Figure 4.14 shows the variation of f_τ and f_{max} with bias. F_τ increases with current density and saturates at high current densities due to Kirk effect. The Kirk effect threshold is high due to the presence of the pulse-doped layer in the collector, close to the base. Kirk effect influences f_{max} more strongly than f_τ as is seen from the reduced f_{max} at high current densities. This is because when the base width increases, the base transit time increases and the collector transit time reduces thus keeping the sum of the two relatively constant. But, the reduced collector thickness increases C_{cb} and degrades f_{max}. The variation of RF parameters with V_{CE} was not explored on this wafer. By plotting $1/2\pi f_\tau$ vs. $1/J_E$ (Eq. 2.2), it is determined that the sum of the base and collector transit times $(\tau_b + \tau_c)$ is

0.95 ps. This is shown in figure 4.15.

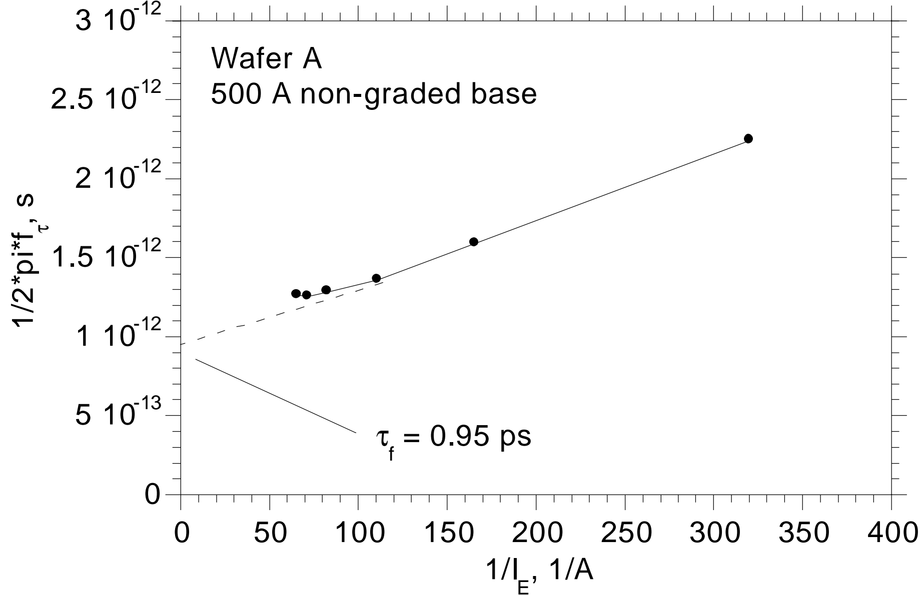


Figure 4.15: Extraction of forward transit time for devices on wafer A.

Figure 4.16 shows the short-circuit current gain h_{21}, maximum stable gain (MSG), and the unilateral power gain U for devices from wafer B. This wafer had a 400 Å graded base and a 2500 Å thick collector. The devices had 0.8 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors. Pad parasitics have not been stripped. Bias conditions are as shown. Extrapolating at -20 dB/decade, $f_{max} = 233$ GHz and $f_\tau = 170$ GHz. The f_{max} is lower than the devices on wafer A due to several reasons. First, we would expect the reduced base layer thickness to increase the base Ohmic contact resistance. In fact, the base Ohmic contact resistivity on this wafer was high thus leading to high base resistance and increased base contact transfer length. This increases the C_{cbi}/C_{cbx} ratio (Eq. 2.11). Second, the reduced collector layer thickness increases the collector-base capacitance. Third, and perhaps significantly, the emitter dimensions of devices on this wafer at 0.8 μm emitter width are slightly larger than those on wafer A. This too increases the C_{cbi}/C_{cbx} ratio, which causes f_{max} to reduce. The higher f_τ is a result of reduced base and collector transit times caused by thinner base and collector epitaxial layers. Operation at higher emitter current density was

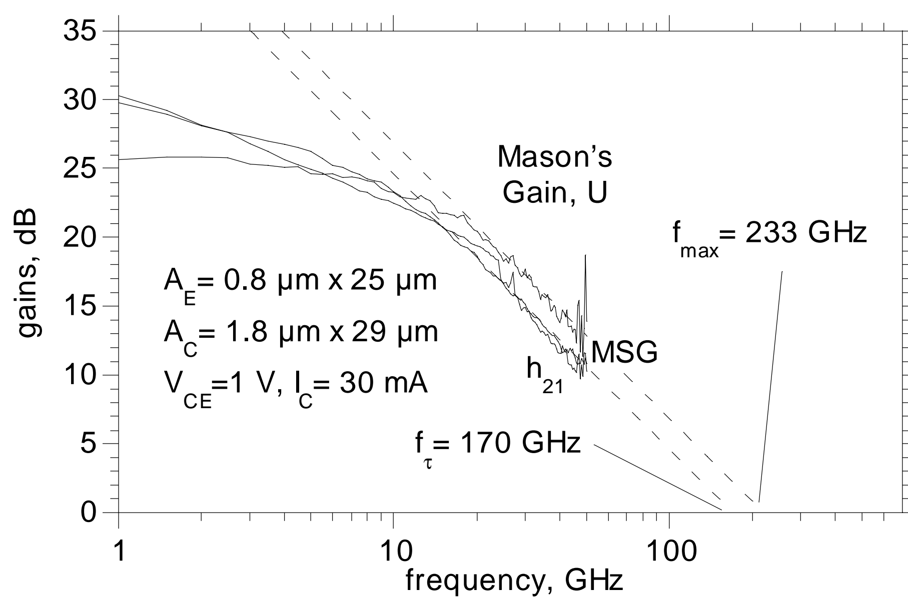


Figure 4.16: RF characteristics of devices from wafer B with 0.8 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors.

also possible on this wafer because of improved thermal performance of this device due to the In/Pb/Ag solder in place of the epoxy.

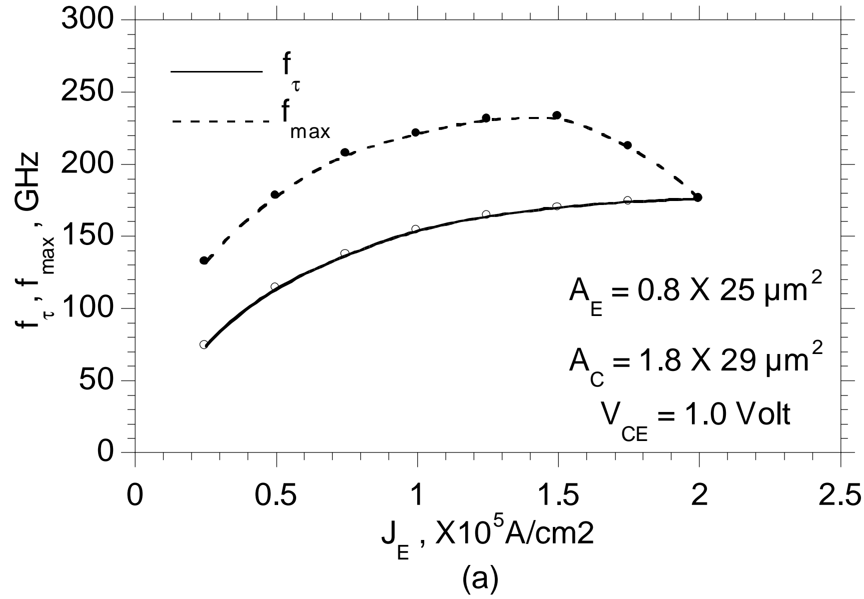
Figure 4.17(a) shows the variation of f_τ and f_{max} with emitter current density. The peak f_τ is 175 GHz. Again, the high Kirk effect threshold can be observed here. At low emitter current density, f_{max} reduces more dramatically than can be predicted by the reduction in f_τ alone. This is probably due to the pulse-doped layer in the collector which causes the collector to be partially depleted at low current densities. Figure 4.17(b) shows a plot of f_τ and f_{max} $vs.$ collector-emitter voltage, V_{CE}. At low V_{CE}, the collector is partially depleted leading to increased C_{cb} and reduced f_{max}. At high V_{CE}, f_τ and f_{max} decrease, suggesting a decrease in the collector electron velocity at high electric fields. For this device the sum of the base and collector transit times is 0.66 ps. The split between the base and collector transit times can be calculated roughly. Using $\tau_c = T_c/2v_{sat}$, $T_c = 2500$ Å, and $v_{sat} = 3 \times 10^5$ A/cm^2, the collector transit time is found to be 0.42 ps. Hence, the base transit time is 0.24 ps.

The variation of f_τ and f_{max} with bias was studied in great detail on this wafer. Figure 4.18 shows the variation of f_τ and f_{max} with collector current for different V_{CE}. Figure 4.19 shows the variation of f_τ and f_{max} with collector-emitter voltage for different collector currents.

Figure 4.20 shows the short-circuit current gain h_{21}, maximum stable gain (MSG), and Mason's unilateral power gain U for devices from wafer C. This wafer had a 400 Å base with kT bandgap grading and a 2700 Å thick collector. The devices had 0.75 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors. Pad parasitics on this wafer were measured and were found to be negligible. Bias conditions are as shown. Extrapolating at -20 dB/decade, $f_{max} = 370$ GHz and $f_\tau = 160$ GHz. The f_τ is higher than wafer A because of the graded base, and similar to wafer B. The f_{max} is higher than the devices on wafer A due to a higher f_τ and better base Ohmic contacts. The f_{max} is higher than wafer B also due to better base Ohmic contacts, and a narrower emitter geometry.

Figure 4.21 shows the variation of f_τ and f_{max} with bias. Figure 4.21(b) shows a plot of f_τ and f_{max} vs. collector-emitter voltage, V_{CE}. At low V_{CE}, the collector is partially depleted leading to increased C_{cb} and reduced f_{max} as with the other devices. At high V_{CE}, f_τ and f_{max} decrease as before. The forward transit time is 0.67 ps, similar to B.

Figure 4.22 shows experimental data correlating lateral scaling with f_{max}



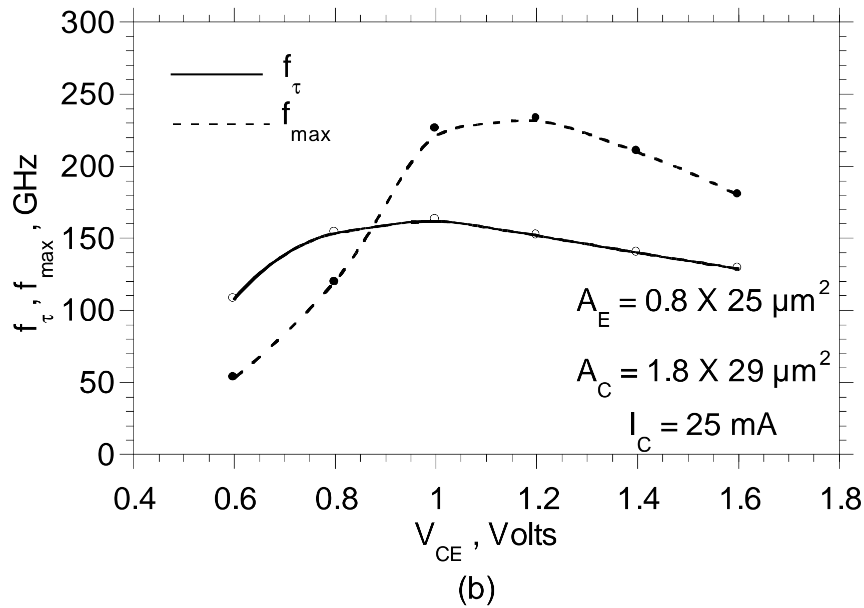


Figure 4.17: Variation of f_τ and f_{max} with (a) emitter current density and (b) collector-emitter voltage for devices from wafer B.

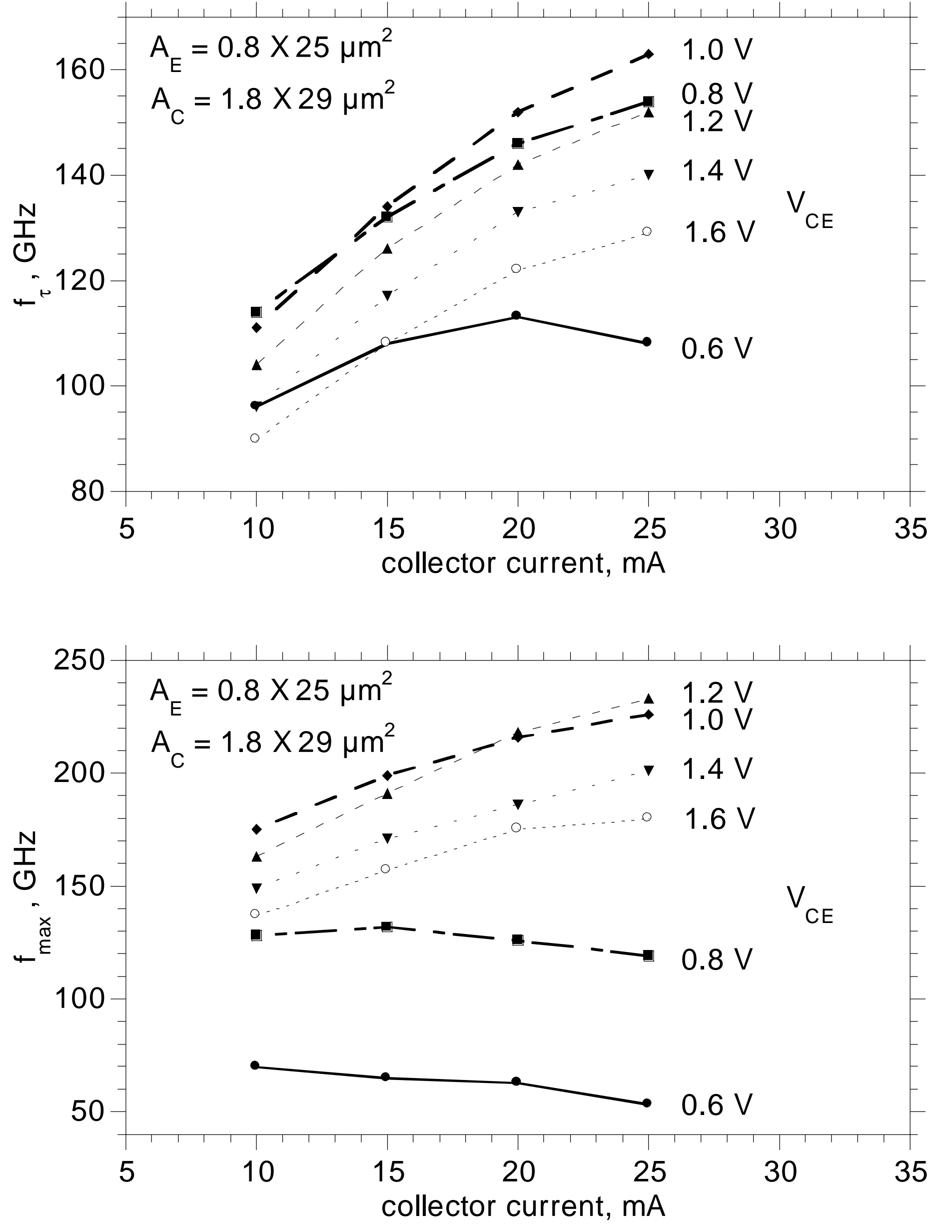


Figure 4.18: Variation of f_τ and f_{max} with collector current for various collector-emitter voltages for devices from wafer B.

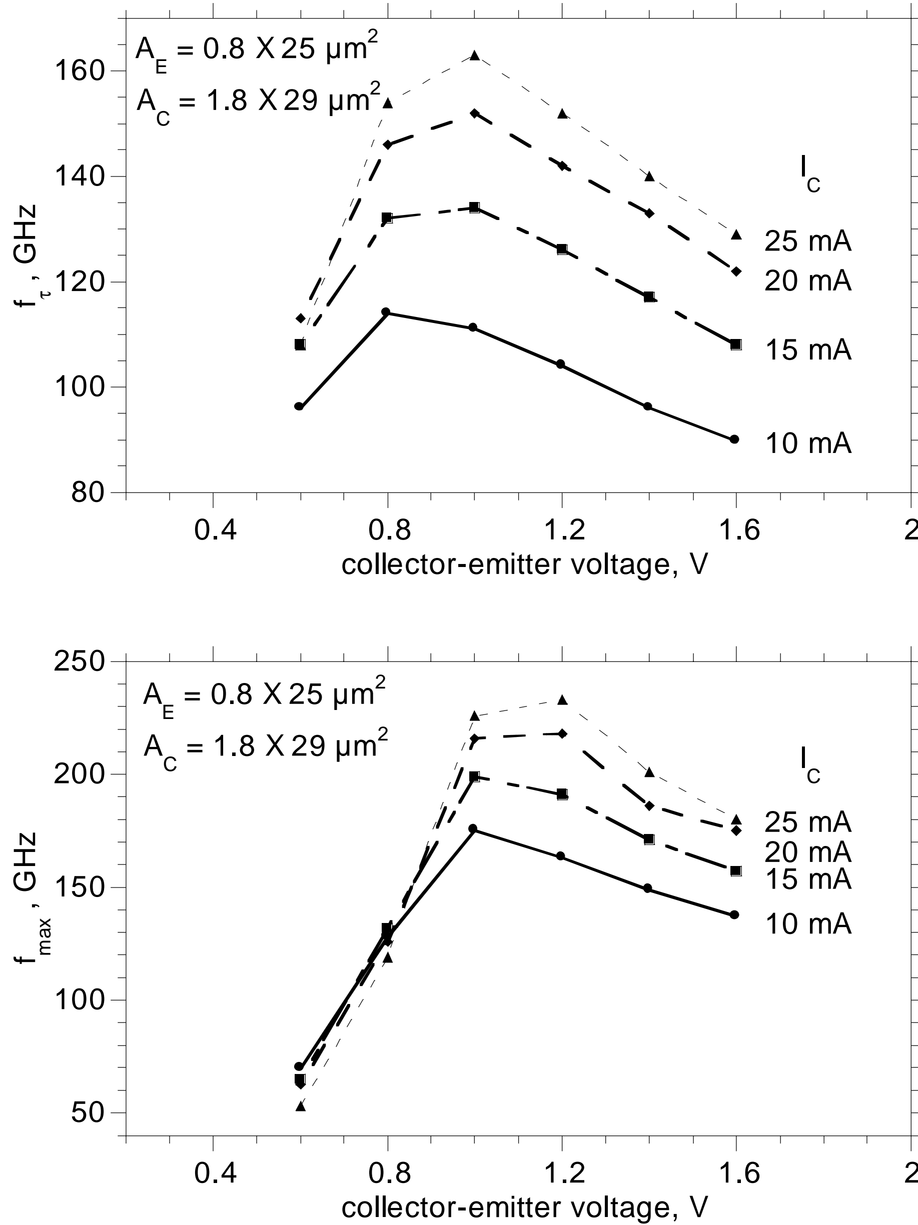


Figure 4.19: Variation of f_τ and f_{max} with collector-emitter voltage for various collector currents for devices from wafer B.

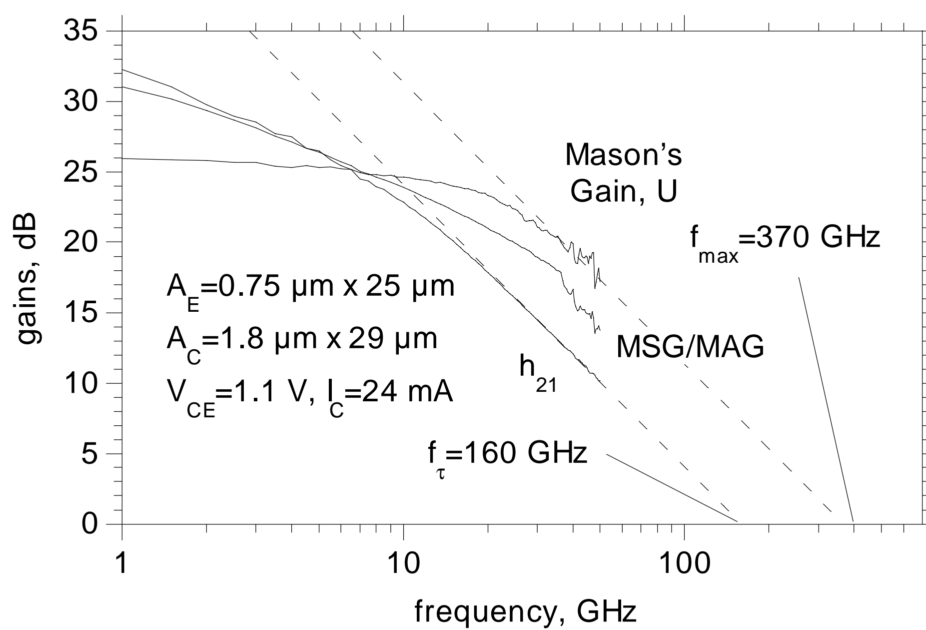
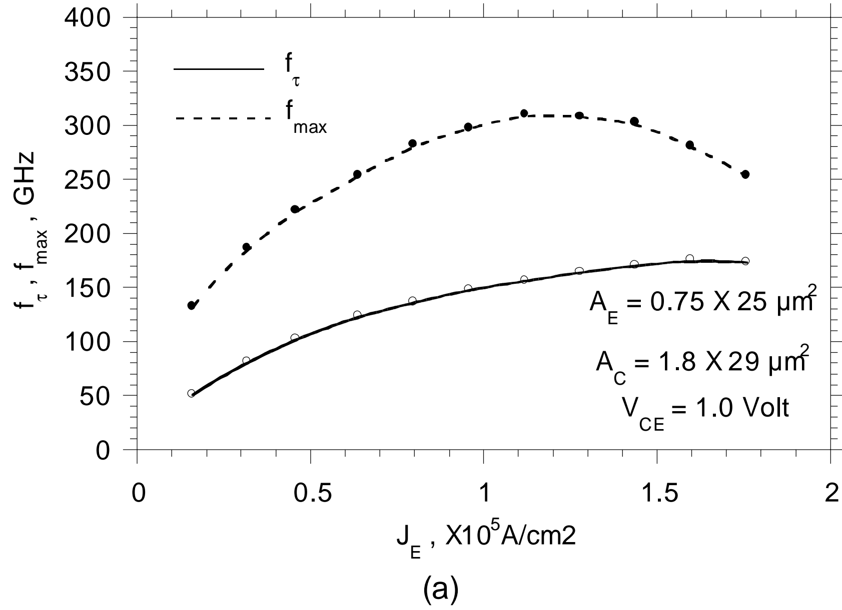


Figure 4.20: RF characteristics of devices from wafer C with 0.75 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors.



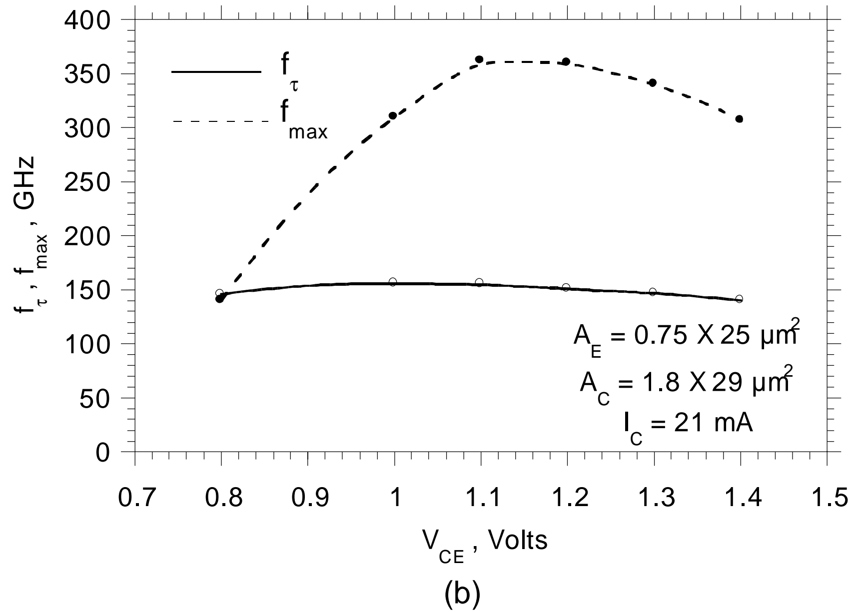


Figure 4.21: Variation of f_τ and f_{max} with (a) emitter current density and (b) collector-emitter voltage for devices from wafer C.

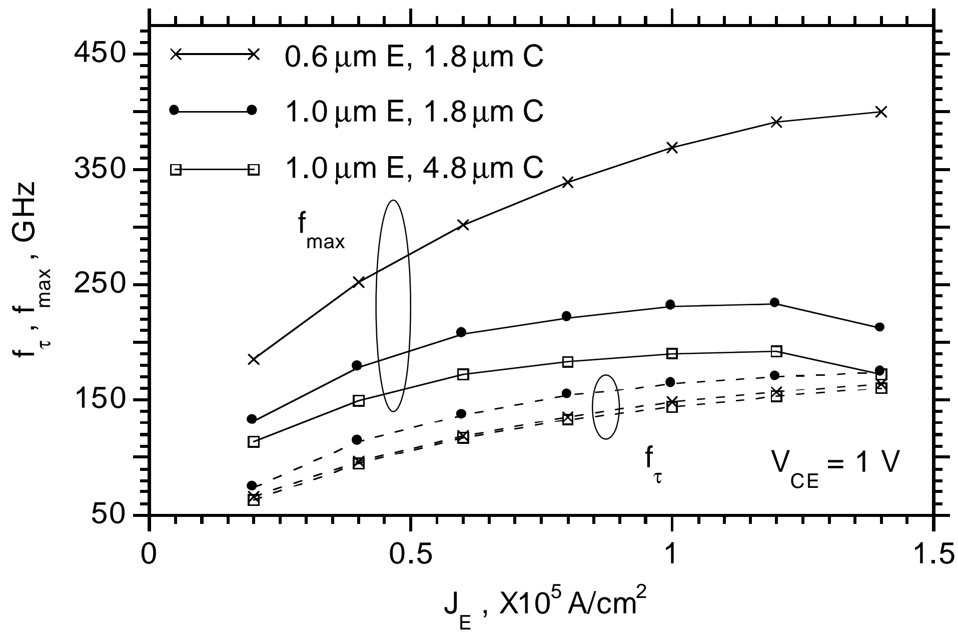


Figure 4.22: Variation of f_τ and f_{max} with J_E for devices with different geometry.

of transferred-substrate HBTs. Shown in the figure is the variation of f_τ and f_{max} with emitter current density for three different devices. The first one has a 0.8 μm $\times$ 25 μm emitter and 4.8 μm $\times$ 29 μm collector. The second one has the same emitter but a narrower 1.8 μm $\times$ 29 μm collector. Both these devices are from wafer B. The third one has the same collector as the second one but a narrower 0.6 μm $\times$ 25 μm emitter. This highly scaled device was fabricated by Q. Lee and is not reported in this thesis elsewhere. From figure 4.22 we can see that f_τ is similar for all three devices. Some difference is present due to the $r_{ex}C_{cb}$ term in the expression for f_τ (Eq. (2.2)). Reducing the collector width alone does not significantly improve f_{max}, as the intrinsic part of the collector-base capacitance remains the same. Scaling both the emitter and the collector improves f_{max} by a large amount. These devices are from different wafers and thus have slightly different parameters. The highly scaled device has a 500 Å base instead of the 400 Å base of wafer B. The base resistance on wafer B was somewhat higher. Hence, the comparison is not strictly correct but the general scaling trend can clearly be observed here. It is expected that with further submicron scaling of the emitter and collector dimensions, a much higher f_{max} can be obtained.

The effect of collector recess etch on RF performance of transferred-substrate HBTs is now explored. Figure 4.23 shows the variation of f_τ and f_{max} with collector current before and after recess etch. As expected, the f_{max} improves significantly after recess etch because of the reduced C_{cb}. F_τ also improves although to a smaller extent than f_{max}. This is due to the reduction in the $r_{ex}C_{cb}$ charging term in the expression for f_τ (Eq. 2.2). After recess etching, the collector current is confined to a narrower area thus increasing the collector current density. This lowers the Kirk effect threshold (f_{max} is now peaking at lower current) as can be seen from the graph. So it can be concluded that the recess etch improves f_{max} significantly and does not significantly affect f_τ. Hence, the collector recess etch improves overall device RF performance.

Figure 4.24 shows how misalignment between the emitter and the collector affect f_τ of transferred-substrate HBTs. As we can see, the effect of misalingment is to increase the average transit time of electrons from the emitter to the collector and thus reduce f_τ at a given current density. Also, in the regions where there is no collector contact and hence no electric field to attract the electrons, the electrons tend to spread laterally. Figure 4.25

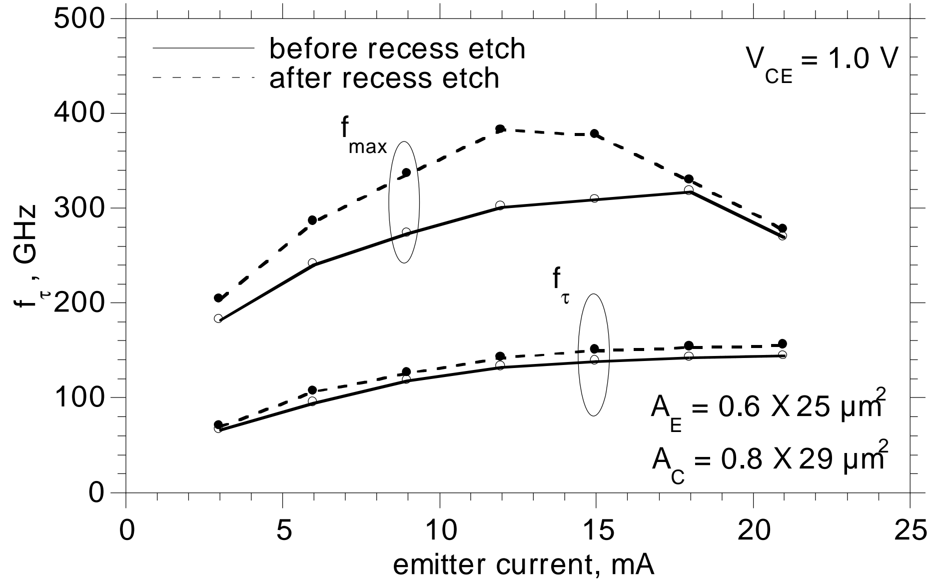


Figure 4.23: Effect of collector recess etch on RF performance.

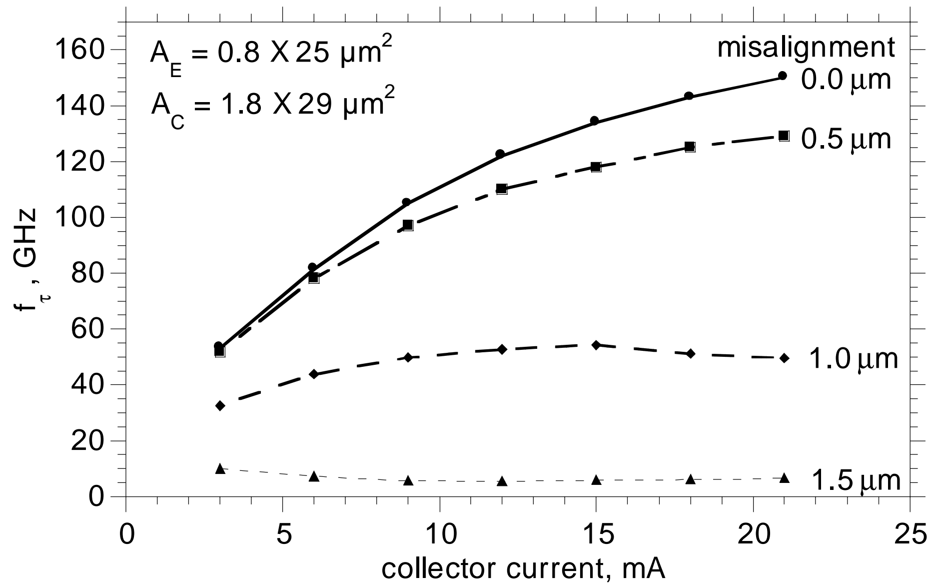


Figure 4.24: Effect of misalignment between emitter and collector on f_τ.

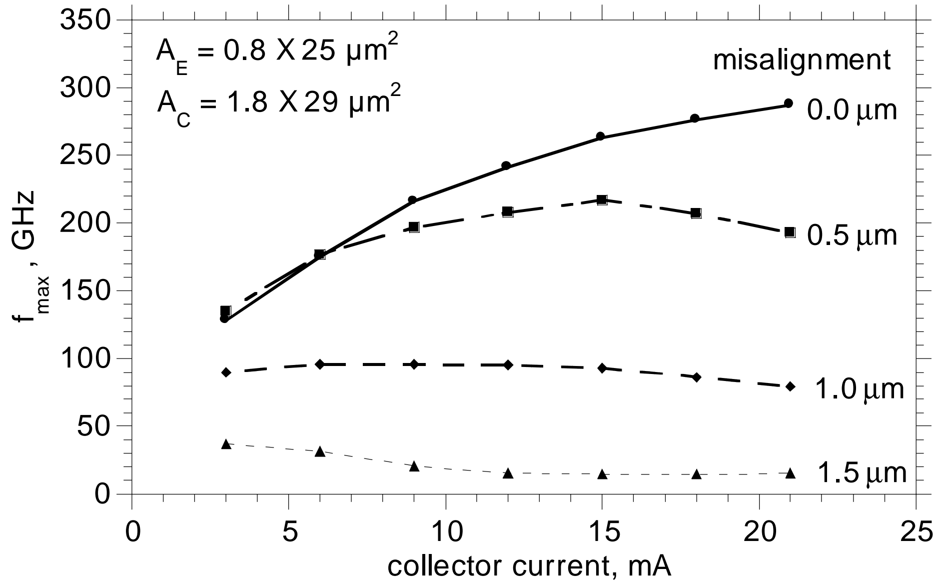


Figure 4.25: Effect of misalignment between emitter and collector on $f_{\max}$.

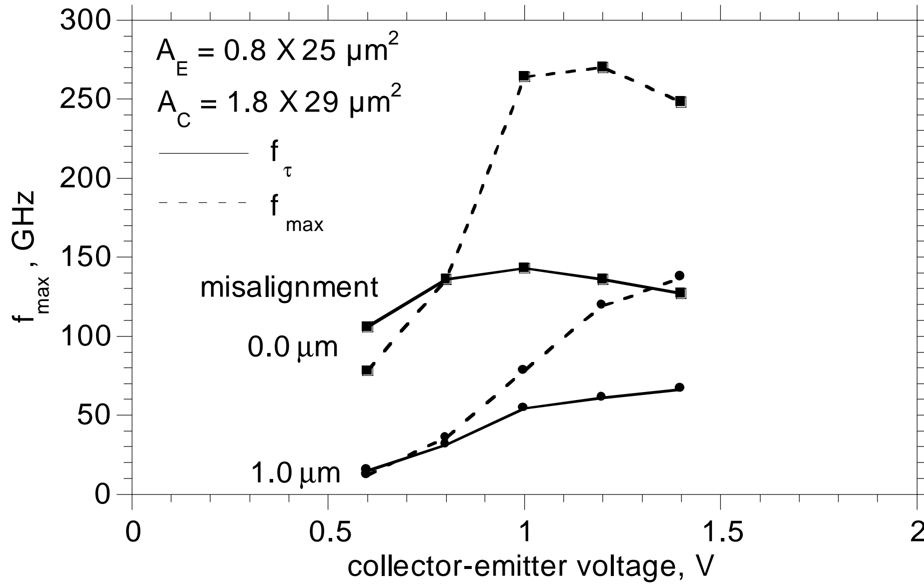


Figure 4.26: Effect of misalignment between emitter and collector on f_τ and $f_{\max}$.

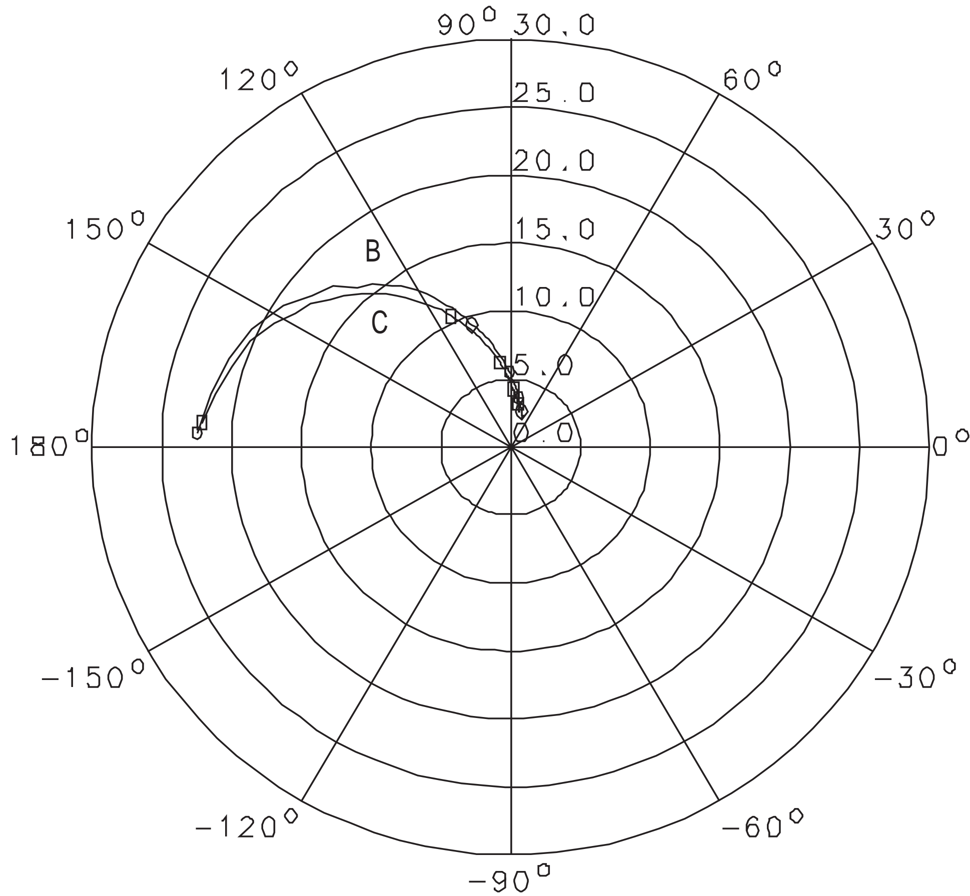


Figure 4.27: Measured s_{21} of devices from wafers B and C.

shows how f_{max} is affected by this misaligment. F_{max} reduces drastically for misaligned devices because of electron spreading and increase in effective area. Figure 4.26 shows how the collector-emitter voltage affects f_{τ} and f_{max} if the devices are misaligned. From these plots we can see how important it is to align the emitters to the collectors.

Measured s-parameters of devices from wafers B and C are shown in figures 4.27, 4.28 and 4.29. The bias conditions and device dimensions are as shown before. S_{21} and s_{12} are very similar for the two wafers. But, devices on wafer C had superior RF performance compared to the devices on wafer B. The lower base resistance and higher output resistance on wafer C can be observed from s_{11} at high frequencies and s_{22} at low frequencies

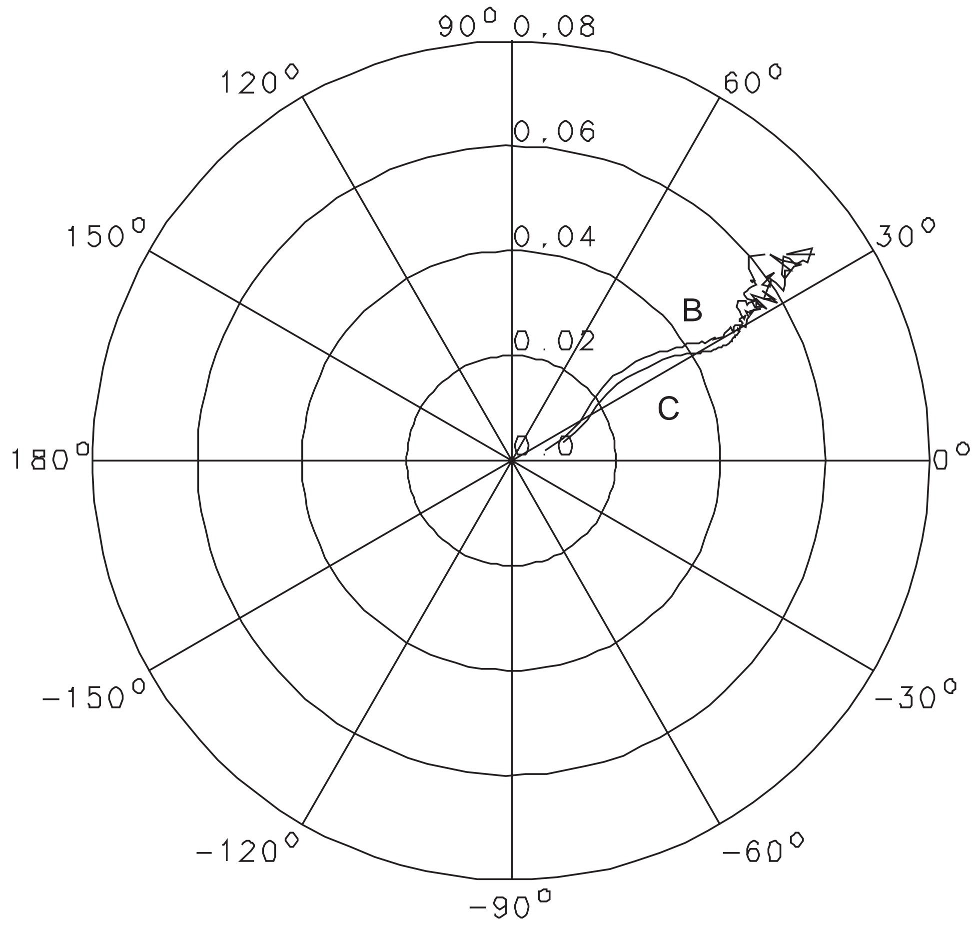


Figure 4.28: Measured s_{12} of devices from wafers B and C.

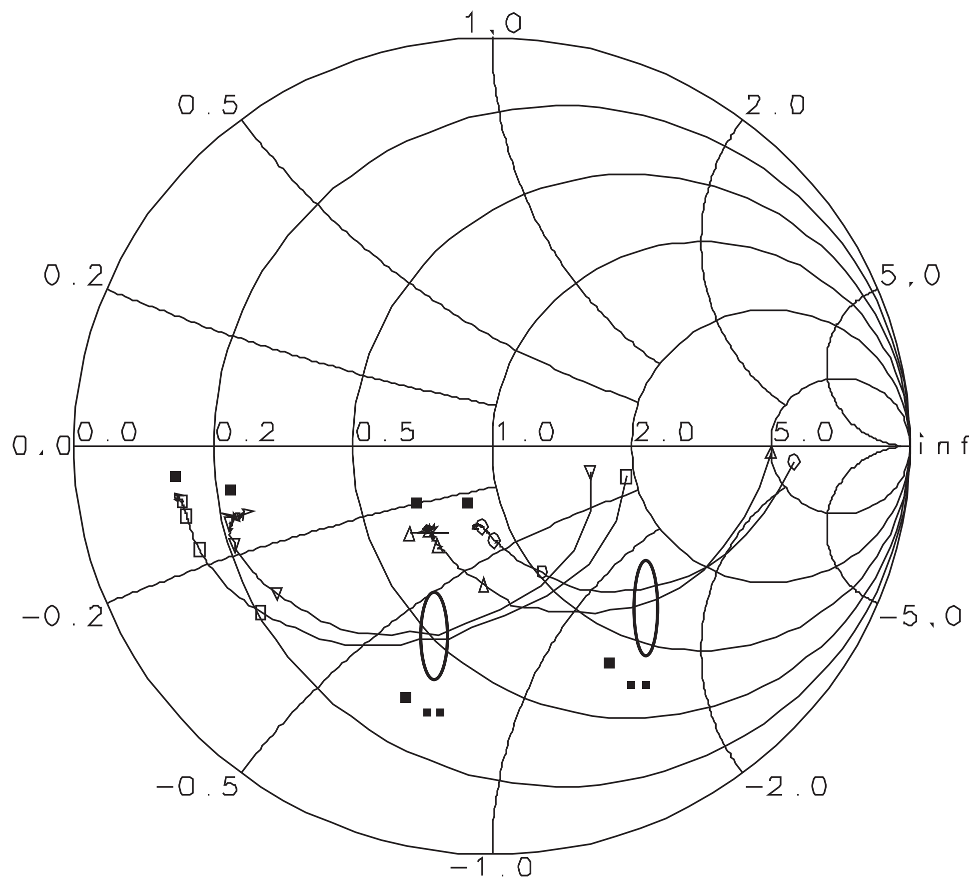


Figure 4.29: Measured s_{11} and s_{22} of devices from wafers B and C.

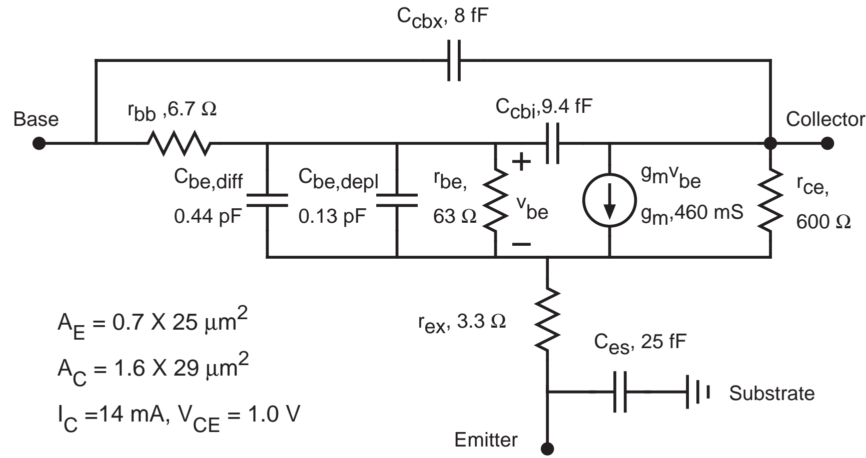


Figure 4.30: Small-signal hybrid-pi model of devices from wafer A.

respectively, both of which lead to lower f_{max}. The output resistance r_{ce} of the device is determined from the intersection of the s_{22} curve with the resistance axis at low frequencies. For wafer B, this turns out to be $\sim$ 250 Ω. This value correlates very closely with the slope of the common-emitter I-V characteristics about the appropriate bias point (figure 4.8, $V_{CE} = 1$ V, $I_C = 30$ mA). The intersection of s_{22} with the resistance axis at high frequencies is proportional to the C_{cbi}/C_{be} ratio (y_{22} from Eq. 2.4). As we can see, this ratio is higher for wafer B than for wafer C, and this also explains the lower f_{max} on wafer B.

Small-signal hybrid-π models of transferred-substrate HBTs from all the three wafers were developed. Figure 4.30 shows a model for devices from wafer A at the given bias conditions. All the parameters except the C_{cbi}/C_{cb} ratio were extracted from bias dependence of s-parameters rather than being fitted on a computer. The model extraction procedure follows the method described in detail in [31]. Pad parasitics are negligible. This model is simple enough to facilitate quick circuit design and analysis, and also provides a reasonable fit to the measured s-parameters. Figure 4.31 shows the comparison between measured and modeled RF characteristics of devices from wafer A. The primary discrepancy is in the low frequency output conductance, which we are unable to model. It is difficult to fit measured HBT s-parameter data to a hybrid-π model for any HBT operating close to the Kirk threshold. Charge-control analysis of an HBT operat-

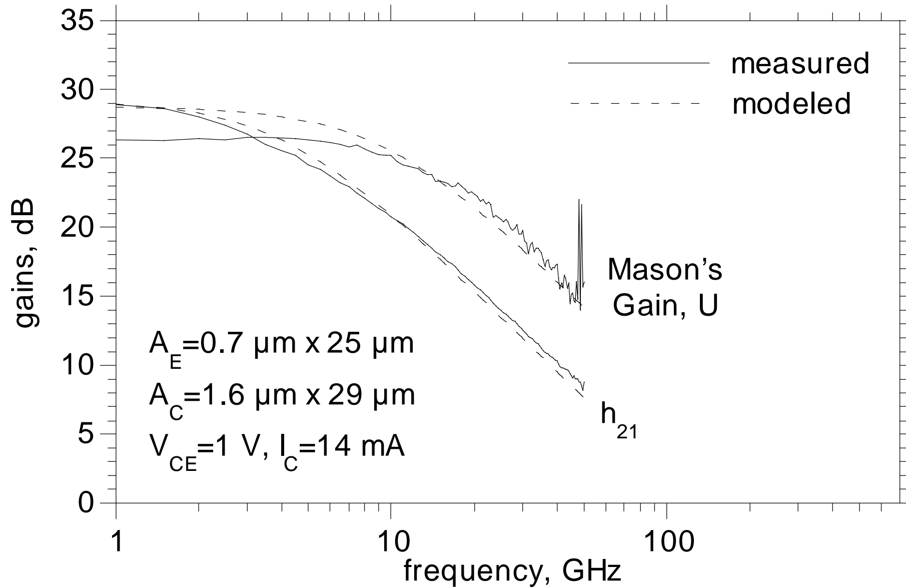


Figure 4.31: Comparison of measured and hybrid-π modeled RF characteristics of devices from wafer A.

ing in the region of collector field screening indicates that the base stored charge is modulated by the collector potential, an effect not modeled in the hybrid-π circuit. The low frequency unilateral gain is slightly different because the output conductance is not modeled well by just using r_{ce}. A SPICE model was also developed for transferred-substrate HBTs. Similar correlation between measured and modeled DC and RF characteristics was obtained.

Transferred-substrate HBTs with f_τ and f_{max} of 175 GHz and 370 GHz respectively have been demonstrated. High device yields and key IC elements have also been demonstrated. Integrated circuits operating to 100 GHz should be possible with this technology. To demonstrate the viability of this technology as a *IC* technology, integrated circuits need to be designed and fabricated in this process.

Chapter 5

Integrated Circuits

This chapter describes the various integrated circuits that were designed and fabricated in the transferred-substrate HBT IC process. Four circuits are presented. The first demonstration circuit is a two-transistor Darlington feedback amplifier. An improvement on this basic design, the Darlington-cascode amplifier, has three transistors. A traveling-wave amplifier with six transistors was designed. Finally, a variable-gain differential amplifier with twenty-two transistors was built. Two designs of the Darlington feedback amplifier from wafers B and C are presented. All the other circuits are from wafer C.

For designing integrated circuits, particularly in a manufacturing environment, fairly accurate device modeling is required and expected. Here, the circuits were designed as the process was evolving and the models are necessarily only approximate. Active devices (HBTs) have already been modeled (with a small-signal hybrid-π model) as shown in the previous chapter but it must be understood that the data set these models represent was not available at the time the ICs were developed. The model is made scalable with the emitter stripe length to facilitate the use of devices of varying areas in integrated circuit simulations. This is done in the usual fashion by making all model currents, capacitances and conductances proportional to the emitter stripe length. SPICE and similar programs use a bias-dependent model, thus enabling the use of a single model over a broad range of bias conditions. In the IC work reported here, bias-independent small-signal hybrid-π models were employed for circuit design, both due to limited characterization data available in a evolving and (then) immature

process, and due to time pressures. Such models must be independently created for each bias condition and cannot be used for large signal simulations. Passive devices like resistors and capacitors were also characterized. For circuits, only small-signal computer simulations with a hybrid-π model were done. The proper bias conditions were ensured by designing the bias network and applied voltages by hand, instead of allowing the computer to determine the voltages and currents for each transistor. The circuits could also be simulated with a full SPICE model or with measured s-parameter files. The SPICE model includes bias and large-signal effects also, but determination of all the SPICE model parameters requires extensive bias-dependent measurements. S-parameter files provide the most accurate simulations, but cannot be scaled with device area. For small circuits with few transistors, the use of hybrid-π models in simulations provide a reasonable prediction of performance, and designing the bias conditions is possible by hand.

The measured results were quite close to the simulated characteristics. Some differences were observed due to changes in device characteristics from one wafer to another. For example, the circuits on wafer B were designed and simulated with hybrid-π models of devices from wafer A. But, as shown in the previous chapter, devices from the two wafers had different RF performance. Specifically, the base resistance and collector-base capacitance were low on wafer B, and, f_τ and current gain were higher than wafer A. Similarly, wafer C had higher (370 GHz) f_{max} than wafer B but the circuits were designed with a very conservative (200 GHz) f_{max}. This affects the circuit performance significantly. Layout parasitics are also not easily modeled. Broadband amplifiers operating close to the technology limit are even more sensitive to variation in device characteristics and layout parasitics.

5.1 Darlington feedback amplifier

The first demonstration circuit in the transferred-substrate HBT IC process is a Darlington feedback amplifier [46]. Feedback amplifiers are suitable for demonstration of emerging IC technologies because of their simple design, low integration levels, few passive components and easy testability. Feedback amplifiers find use in fiber-optic receiver gain blocks and as low-noise transimpedance frontend amplifiers. A Darlington amplifier with series and shunt resistive feedback and 50Ω input/output impedance [46] was designed

and fabricated.

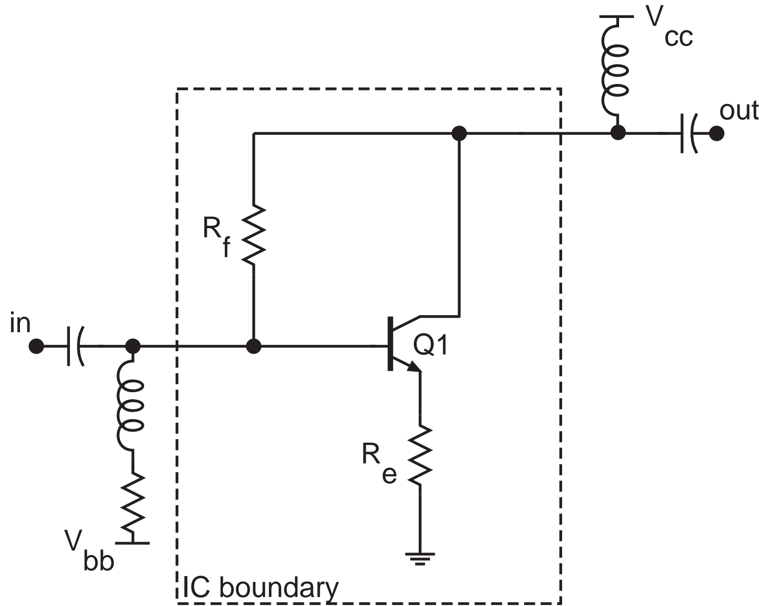


Figure 5.1: Schematic circuit diagram of common-emitter resistive feedback amplifier.

The design of resistive feedback amplifiers can be found in [46] and is reviewed here. Figure 5.1 shows a simple common-emitter feedback amplifier with resistive feedback. The desired (negative) voltage gain A is first specified, and a 50 Ω (=Z_o) input/output impedance is desired. The two design equations are :

$$g_{m,extrinsic} = 1/(r_e + r_{ex} + R_e) = (1 - A)/Z_o \tag{5.1}$$

$$R_f = Z_o(1 - A) \tag{5.2}$$

where $r_e = nkT/qI_C$ and r_{ex} is the extrinsic emitter resistance. The bandwidth of the amplifier can be estimated from the charging time constant. The first order input time constant is dominant, and consists of the emitter-base capacitance, the Miller-multiplied collector-base capacitance, the base resistance and the combined effect of the feedback and generator impedances as follows :

$$a_1 \simeq 1/2\pi BW \simeq (r_{bb} + Z_o/2)(g_{m,extrinsic}\tau_f + (1 - A)C_{cb}) \tag{5.3}$$

where r_{bb} and C_{cb} are the transistor base resistance and collector-base capacitance, $\tau_f = 1/2\pi f_\tau$ is the forward transit time and BW is the bandwidth of the amplifier. Hence we can see that as the gain is increased by increasing A (and hence $g_{m,extrinsic}$), the bandwidth reduces. The transistor area, the operating current and the emitter resistor need to be designed. If the transistor area is too large, r_{bb} is small but C_{cb} is large and vice versa. Hence, there is an optimum area and this can be found by taking the derivative of Eq. 5.3. Once the transistor area is determined, the emitter current is chosen for peak f_τ operation. R_e can then be calculated from Eq. 5.1. This elementary analysis yields reasonable values of gain and bandwidth. Further optimization can be done using a computer circuit simulator.

To further improve the gain-bandwidth of this amplifier, either a cascode or a Darlington stage can be used instead of the single transistor. The cascode cell has a common-emitter transistor followed by a common-base stage. The Darlington cell has a emitter-follower and a common-emitter transistor. If the transistor f_{max} is lower than f_τ, the Miller-multiplied collector-base capacitance is dominant. A cascode cell reduces this Miller multiplication and improves bandwidth. The cascode cell also reduces high frequency feedback from the output to the input and boosts the output impedance of the transistor. On the other hand, if the transistor f_τ is lower than f_{max}, a Darlington stage improves bandwidth. The emitter follower buffer presents a lower driving impedance ($\simeq r_e + r_{ex}$ as opposed to $Z_o/2$) to the input capacitance of the common-emitter transistor. Darlington stages also improve the overall current gain and increase the input resistance compared to a single transistor. If both f_τ and f_{max} are comparable, three transistors connected in a Darlington-cascode topology can be used to improve bandwidth. However, as the number of transistors is increased, biasing becomes more difficult and additional power supplies, resistive divider networks and bypass capacitors are needed.

In the transferred-substrate HBT technology, f_{max} is larger than f_τ. Hence a Darlington stage was used to boost bandwidth. Figure 5.2 shows a schematic circuit diagram of the amplifier. The dotted line shows the chip boundary. Q1-Q2 form the Darlington pair. The design equations are the same as for the common-emitter amplifier. Q2 is the main voltage gain

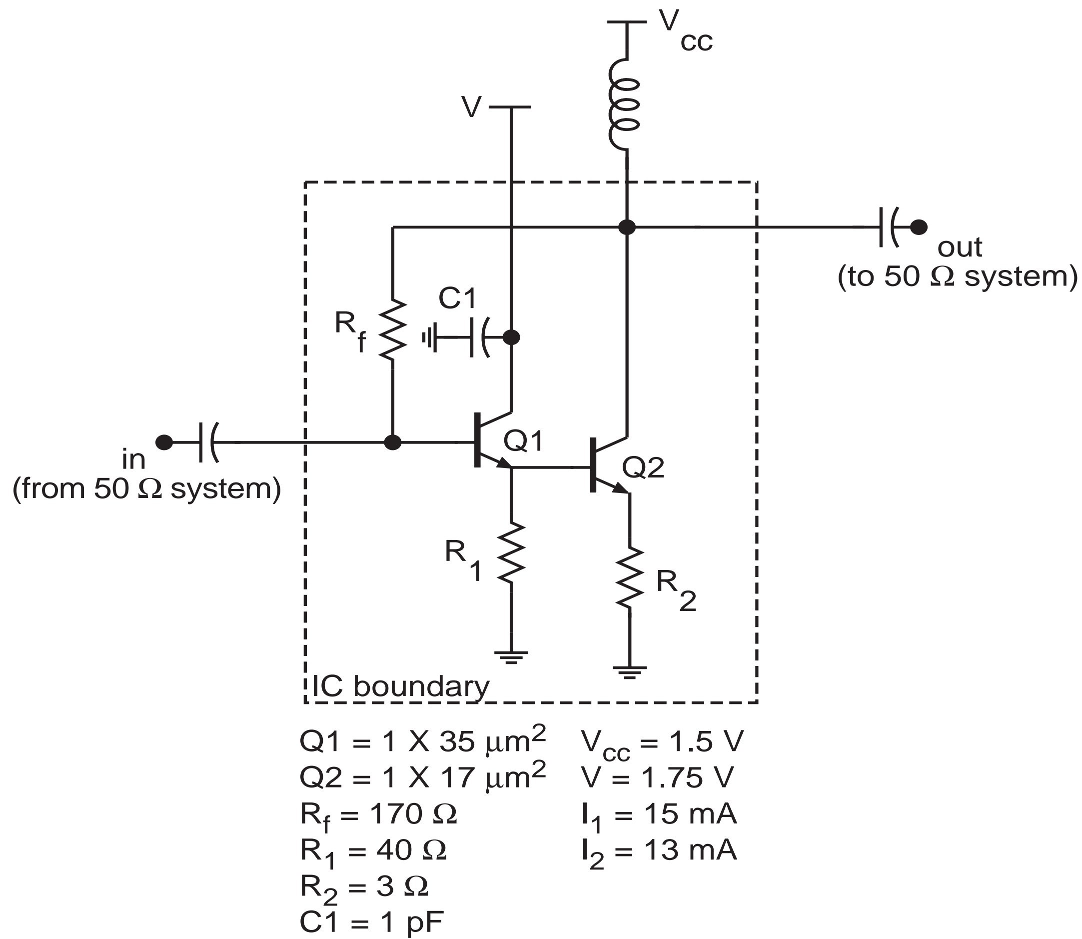


Figure 5.2: Schematic circuit diagram of Darlington feedback amplifier.

stage.

MOTC analysis was done to obtain the optimum areas. The transistor element values include the effect of the extrinsic emitter resistance r_{ex} through emitter degeneration. The sum of the first order time constants is :

$$a_1 \simeq (r_{bb1} + Z_o/2)((1/g_{m1} + R_1)^{-1}\tau_{f1} + C_{cb1}) \\ + (r_{bb2} + 1/g_{m1})((1/g_{m2} + R_2)^{-1}\tau_{f2} + (1 - A)C_{cb2}) \quad (5.4)$$

where the terms are identical to the common-emitter amplifier and the subscripts 1 and 2 correspond to the transistors Q1 and Q2 respectively. We must satisfy the gain relationship by setting $A_{v1}g_{m2,extrinsic} = (1 - A)/Z_o$, where A_{v1} is the voltage gain of the first transistor ($\simeq 1$) and $g_{m2,extrinsic}$ is the degenerate transconductance of the second transistor. The capacitance of the main gain transistor is now driven with a smaller impedance and the bandwidth is increased. But additional time constants are now added. Proper design can lead to improved bandwidth. This expression can be used to determine the emitter stripe lengths of Q1 and Q2 to maximize bandwidth. If the emitter stripe length of Q1 is large, its input capacitance is large, degrading bandwidth; if it is too small, its base and emitter resistances are large, increasing the driving impedance for Q2 and degrading bandwidth. Large Q2 emitter stripe length increases its Miller-multiplied base-collector capacitance whereas a small emitter stripe length increases the base resistance, through which the (degenerated) device input capacitance must be charged. Hence there optimum emitter stripe lengths for Q1 and Q2. Peak f_τ bias currents are chosen for both transistors. R_f, the shunt feedback resistor, is chosen to provide an input impedance of 50Ω. R_1 is the series feedback resistor in the emitter of Q1 and sets the Q1 emitter current density close to the peak f_τ bias. R_2 sets the degenerated transconductance of Q2 (and hence of the circuit) to provide the desired gain and 50 Ω output impedance. The circuit is biased with V_{CC} and an off-chip resistor connected through a bias-tee at the output. The collector of Q1 is not connected to the output, but is biased with and independent supply to eliminate Miller multiplication of its base-collector capacitance. The element values and bias conditions are as shown. The designed gain and bandwidth were 10 dB and 50 GHz respectively. The IC consumes 40

mW DC power. Figure 5.3 shows a photomicrograph of the amplifier. The chip dimensions are 0.35 mm $\times$ 0.4 mm.

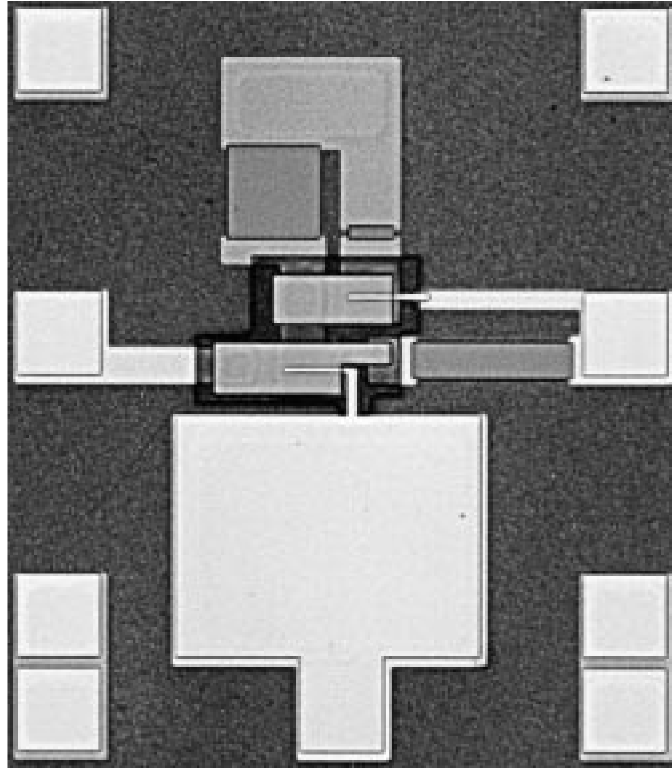


Figure 5.3: Photomicrograph of the Darlington feedback amplifier.

The amplifier characteristics were measured with a network analyzer to 50 GHz. Figure 5.4 shows the simulated and measured forward gain s_{21} of the amplifier. The measured low-frequency gain is about 13 dB and the 3-dB bandwidth (relative to the low-frequency gain) is 50 GHz. The gain peaking at high frequencies is due to the second (internal) pole (Eq. 5.4) in the feedback loop created by the emitter resistance of Q1 and the base resistance and input capacitance of Q2. This gain peaking can be reduced by adding some resistance in series with the base of Q2, or by increasing the degeneration of Q2, at the cost of reduced gain. The bandwidth is below the potential of the technology for several reasons. First, f_{max} is low on the current ICs (wafer B) due to high base Ohmic contact resistance. Second, the resistor current carrying capability was lower than expected, forcing the

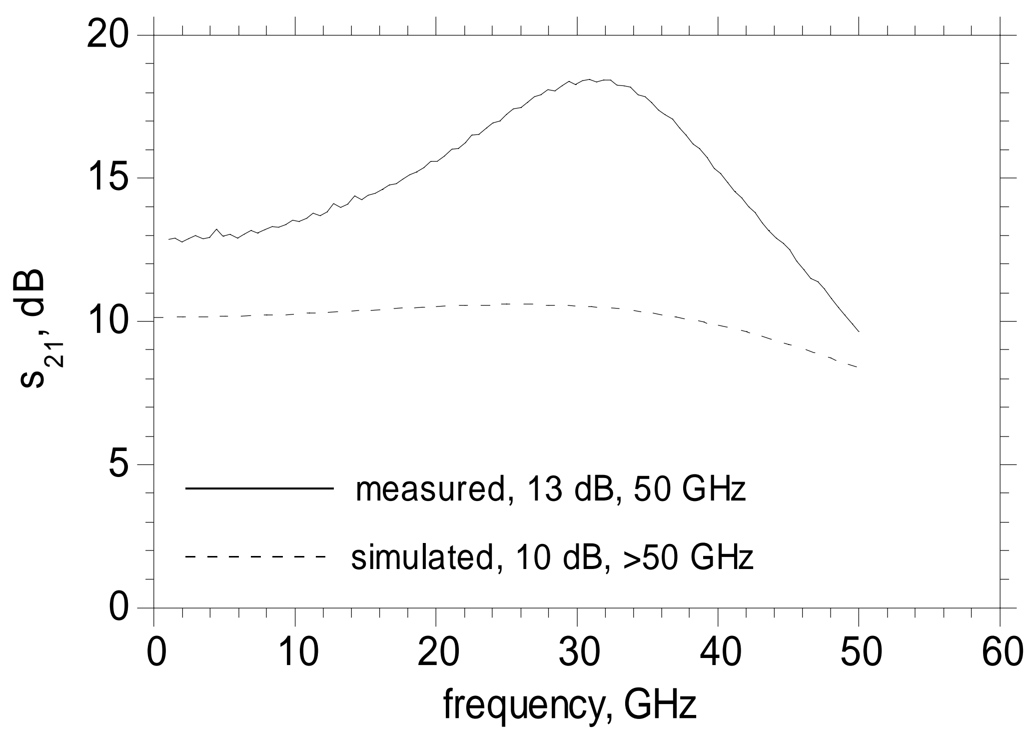


Figure 5.4: Measured and simulated forward gain s_{21} of the amplifier (wafer B). The simulation assumes the original model parameters

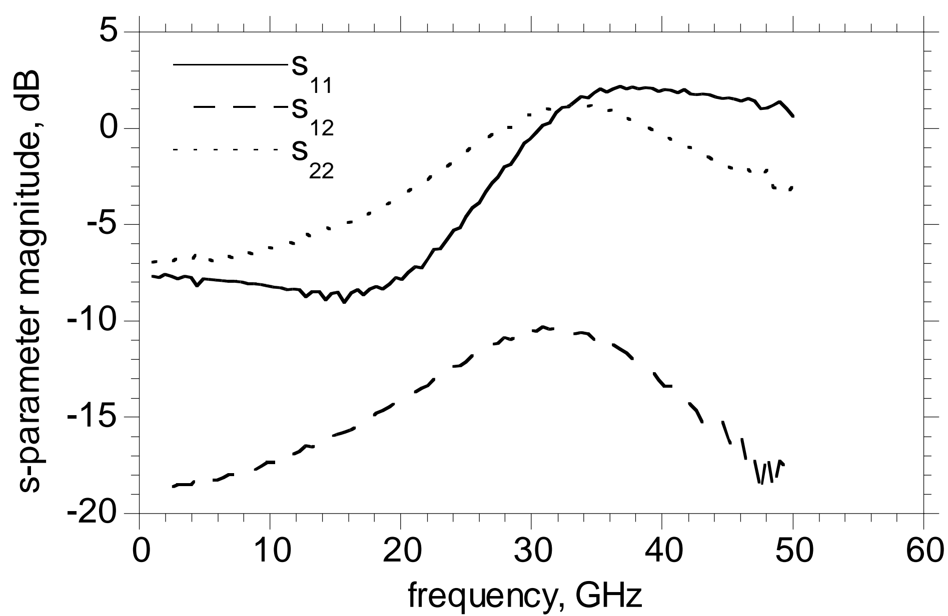


Figure 5.5: Measured input return loss s_{11}, output return loss s_{22}, and reverse isolation s_{12} of the amplifier.

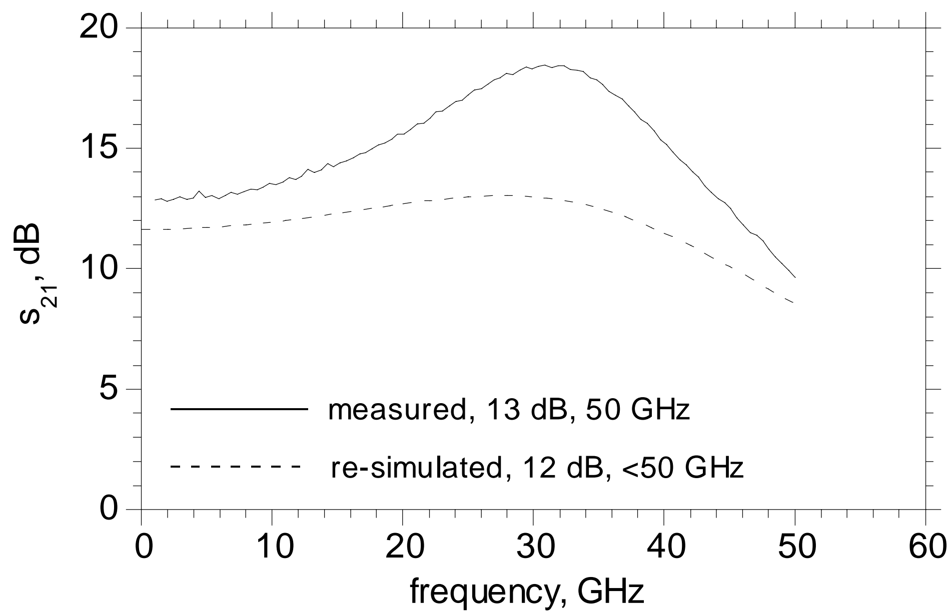


Figure 5.6: Comparison of measured gain and simulated gain with new transistor parameters.

transistor bias to be less than the intended design conditions. Also, since the base of Q1 and the collector of Q2 were biased with the same supply (1.5 V), V_{CE} for Q2 was high, which degrades transistor bandwidth. At the bias conditions at which the amplifier measurements were taken, the transistor f_τ and f_{max} are 120 and 175 GHz respectively. Figure 5.6 shows a re-simulation of the amplifier with transistor parameters from the current wafer. Although this simulation matches the measured data better than the previous simulation, the amplifier characteristics are not entirely predicted. Possible reasons for this are layout parasitics which are not easy to model and difficulty in modeling the output conductance of the devices. Figure 5.5 shows the input and output return losses and the reverse isolation of the amplifier. The return losses are poor at high frequencies indicating small (and even positive) reflection coefficients for the amplifier. The positive return losses are due to the negative input impedance of emitter-follower-common-emitter pair at high frequencies.

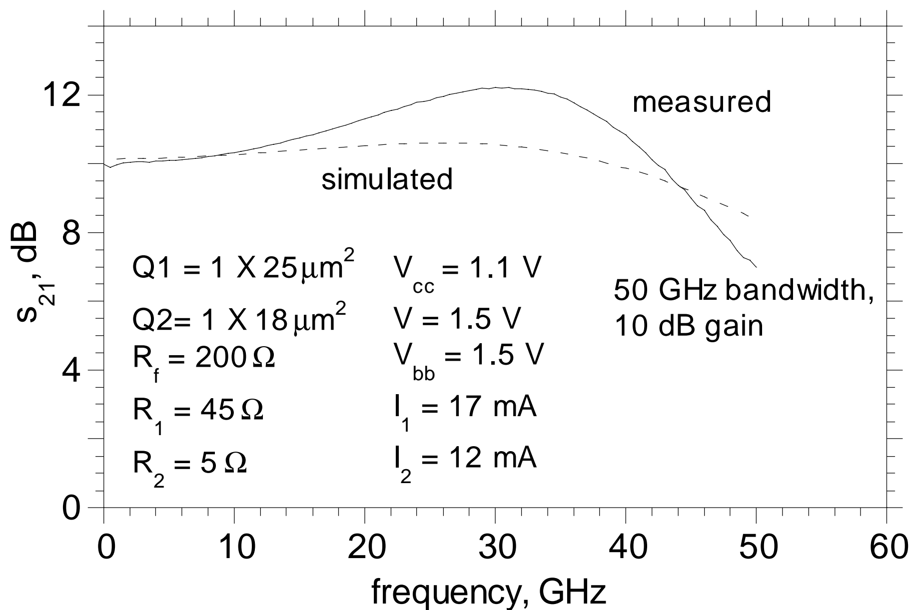


Figure 5.7: Measured forward gain s_{21} of the amplifier (wafer C).

A similar design was fabricated on wafer C and the results are shown in figures 5.7 and 5.8. The element values and bias conditions are also shown. An additional supply (V_{bb}) in series with a 2 kΩ resistor was connected

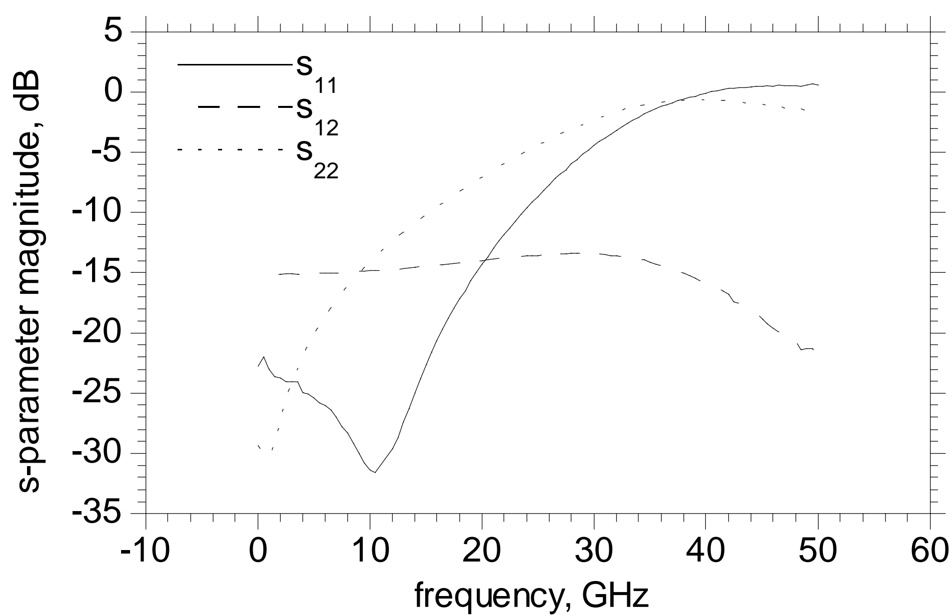


Figure 5.8: Measured input return loss s_{11}, output return loss s_{22}, and reverse isolation s_{12} of the amplifier.

through a bias-tee to the base of Q1 so that Q2 need not be biased at high V_{CE}. The difference in gain peaking and return losses is mainly due to the difference in the base resistance (r_{bb}) on the two wafers. This also causes the f_{max} to be quite different (233 GHz *vs.* 370 GHz). The resistors on this design were made wider to accommodate more current, resulting in higher current density operation. The gain was reduced by increasing the emitter resistor R_2. As with the amplifiers on wafer B, wafer C produced amplifiers with 50 GHz bandwidth, but the gain peaking was greatly reduced and input/output return losses improved.

As we have seen above, Darlington amplifiers in the transferred-substrate HBT process exhibit strong gain peaking and poor input return losses at high frequencies. This is a result of the parameters of the transferred-substrate HBT. Q1, an emitter follower driving the input capacitance of Q2, has an input impedance whose real part is negative at some frequencies. The resulting resonance - observed in both gain (s_{21}) and input impedance (s_{11}) - becomes progressively more severe as the base resistances (r_{bb}) of Q1 and Q2 are reduced. The low base resistance and collector-base capacitance of transferred-substrate HBTs strongly enhance this negative-resistance peaking.

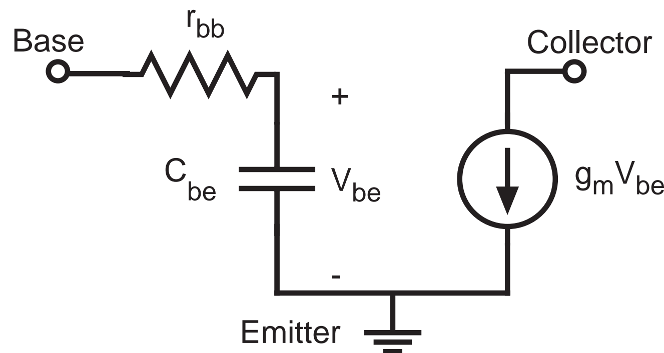


Figure 5.9: Simplified equivalent circuit of transistor for calculation of Darlington input impedance at high frequencies.

The input impedance and the transfer function for a Darlington pair will now be derived. The transistor model that will be used is shown in figure 5.9. R_{bb} is the base resistance, C_{be} is the input capacitance consisting of the diffusion and junction capacitances and g_m is the extrinsic

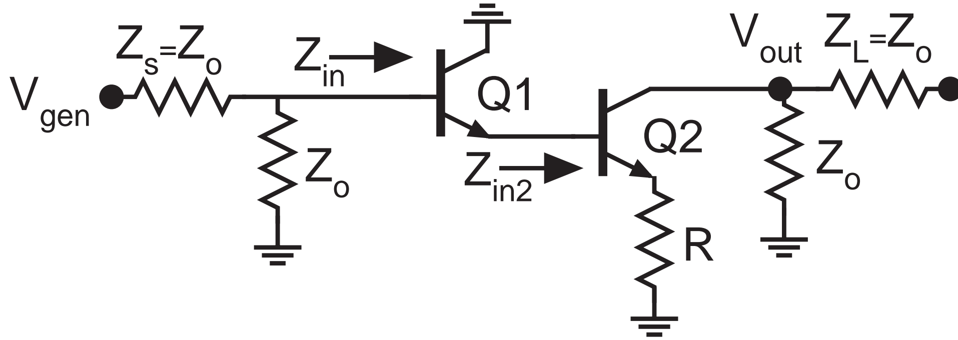


Figure 5.10: A HBT Darlington feedback amplifier.

transconductance. Degeneration due to the extrinsic emitter resistance can be absorbed into the element values and is not shown explicitly. C_{cb} is very small for transferred-substrate HBTs and is neglected to simplify the derivation. β is assumed to be infinite which allows the input resistance R_{be} to be open circuited. Figure 5.10 shows the Darlington amplifier with the transistor pair Q1-Q2 and the degeneration resistor R. Q1 can be assumed to be biased through a current source with infinite output impedance. The feedback resistor is converted to 50 Ω resistors at the input and output of the amplifier by the use of the Miller-multiplication approximation. The source and load impedances are assumed to be 50 Ω. First, let us look at the input impedance. The impedance looking into Q2 at the intermediate node between the two transistors Z_{in2} is

$$Z_{in2} = r_{bb2} + R + (1 + g_{m2}R)/j\omega C_2 \tag{5.5}$$

The input impedance of the overall stage Z_{in} is given by

$$Z_{in} = r_{bb1} + 1 + /j\omega C_1 + (1 + g_{m1}Z_{in2})/j\omega C_1 \tag{5.6}$$

Using Eq. 5.5 in Eq. 5.6 and simplifying gives

$$\begin{aligned} Z_{in} = {} & (r_{bb1} + r_{bb2} + R) - (g_{m1}[1 + g_{m2}R]/\omega^2 C_1 C_2) \\ & + (1 + g_{m1}[r_{bb2} + R])/j\omega C_1 + (1 + g_{m2}R)/j\omega C_2 \end{aligned} \tag{5.7}$$

As we can see from Eq. 5.7, the real part of the input impedance has both a positive and a frequency-dependent negative term. Hence, at some fre-

quencies, the input impedance will have a negative real part thus leading to positive input reflection coefficients and gain peaking. Using actual values for all terms from a fabricated amplifier, the frequency at which the real part becomes zero is 100 GHz. Below this frequency, the real part will be negative. The output impedance can be similarly derived.

Now, let us look at the transfer function of the amplifier. An approximate analysis by the method of time constants will be used. The mid-band voltage gain of the amplifier is given by (ignoring degeneration due to resistor R)

$$A_v = V_{out}/V_{gen} = (1/2).(g_{m2}).(Z_o/2) \tag{5.8}$$

The first order and second order time constants are given by

$$a_1 = C_1(1/g_{m1}) + C_2((1 + g_{m1}r_{bb2})/g_{m1}) \tag{5.9}$$

$$a_2 = C_1(1/g_{m1})C_2(r_{bb1} + r_{bb2} + Z_o/2) \tag{5.10}$$

The transfer function is given by

$$H(s) = V_{out}/V_{gen} = A_v/(1 + a_1 s + a_2 s^2) \tag{5.11}$$

This equation is of the form

$$H(s) = A_v/(1 + 2s\xi/\omega_n + 2s^2/{\omega_n}^2) \tag{5.12}$$

Such a transfer function leads to complex poles. The values of ω_n and ξ determine the frequency response of the amplifier. If $\xi < 1/\sqrt{2}$, the system is underdamped and gain peaking will be observed; for $\xi = 1/\sqrt{2}$, the system is critically damped or maximally flat and for $\xi > 1/\sqrt{2}$ the system is overdamped. The frequency ω_n denotes the resonant frequency where gain peaking is observed. Using actual values of degenerate capacitances and extrinsic transconductances from the Darlington amplifier, $\xi = 0.67$ and $f_n = 48$ GHz. This shows that the system is underdamped and will show some gain peaking. If the base resistance is lower, the damping factor reduces and the peaking increases. This calculation has been done with several assumptions and is only approximate, hence the values of the resonant frequency and damping factor are not entirely correct, but it does predict

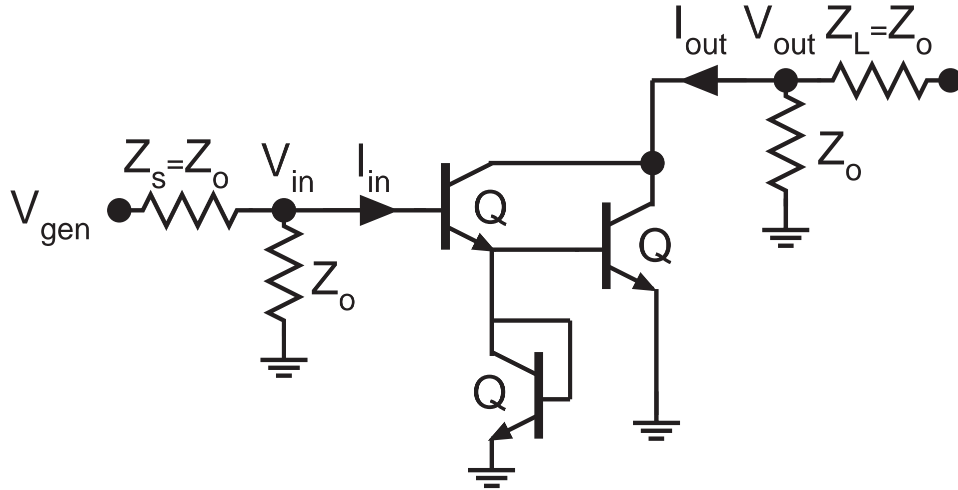


Figure 5.11: A HBT mirror-Darlington feedback amplifier.

the amplifier behavior correctly. If a mirror-Darlington [47] configuration is used, the complex poles are eliminated we shall now see.

Figure 5.11 shows the circuit diagram of a mirror-Darlington amplifier. Assuming that all devices are of the same size and neglecting r_{bb}, the transfer function of the amplifier is given by

$$H(s) = V_{out}/V_{gen} = (1/2).(g_m).(Z_o/2).(1/(1 + sCZ_o/4)) \tag{5.13}$$

As we can see, there is only a simple pole in this transfer function at $C.Z_o/4$. this is because the internal pole is cancelled by a zero caused by connecting the output of the first transistor to the output of the amplifier and biasing the first transistor with a diode. Hence, there is no gain peaking. The input reflection coefficient is given by

$$Z_{in} = V_{in}/I_{in} = 2/sC \tag{5.14}$$

Hence, the input reflection coefficient is simple imaginary and does not exhibit the behavior of the Darlington. The current gain of the mirror-Darlington is given by

$$A_I = I_{out}/I_{in} = 2f_\tau/f \tag{5.15}$$

which implies that the current gain is twice that of a single transistor and so is the f_τ. Hence it is a f_τ-doubler. Amplifiers using this configuration will thus have higher bandwidth. The treatment given above is over-simplified and expressions become very complicated if a full model of the transistor is used and if the transistors are not of the same size. Even so, the mirror-Darlington configuration will perform better than the simple Darlington. ICs based on mirror-Darlington or f_τ-doubler [48] configurations will be developed in the future.

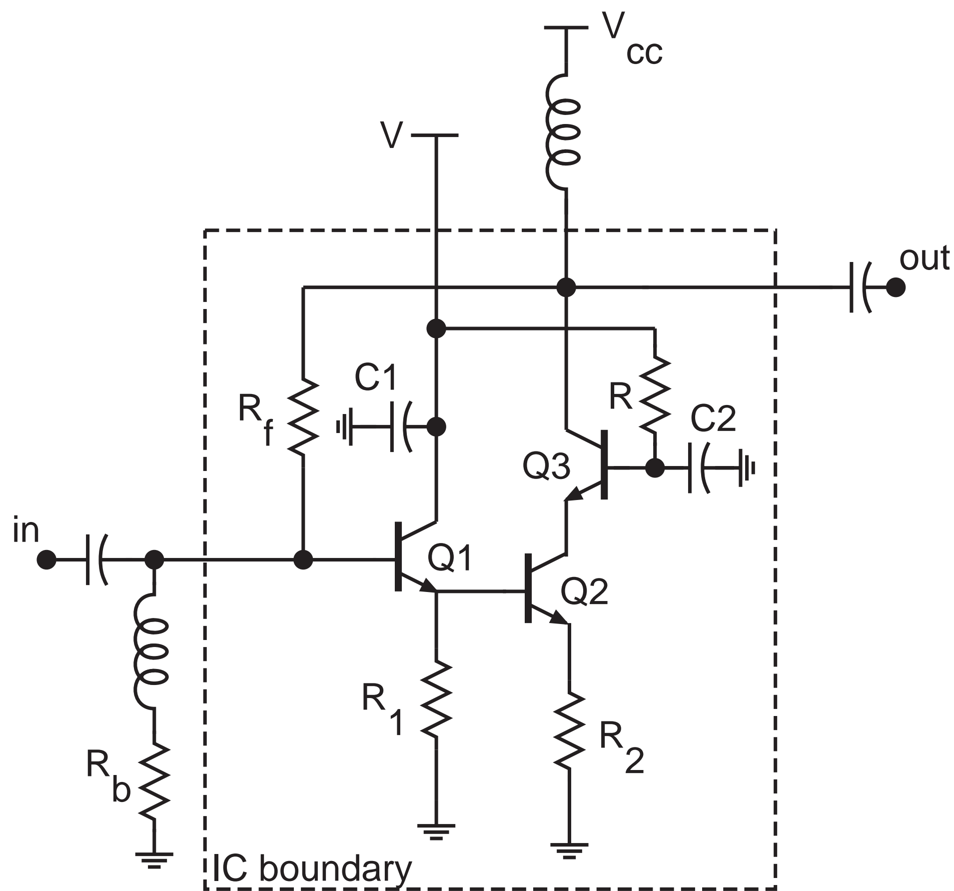
5.2 Darlington-cascode feedback amplifier

In an attempt to obtain improved amplifier bandwidth, a cascode cell was added to the basic Darlington cell. This created a Darlington-cascode composite amplifier. Figure 5.12 shows a schematic circuit diagram. An additional transistor Q3 is connected in a cascode configuration with Q2 at the output. A detailed MOTC analysis of the Darlington-cascode gives a dominant time constant :

$$\begin{aligned} a_1 \simeq & (r_{bb1} + Z_o/2)((1/g_{m1} + R_1)^{-1}\tau_{f1} + C_{cb1}) \\ & + (r_{bb2} + 1/g_{m1})((1/g_{m2} + R_2)^{-1}\tau_{f2} + [1 + (1/g_{m2} + R_2)^{-1}/g_{m3}]C_{cb2}) \\ & + \tau_{f3} \end{aligned} \tag{5.16}$$

where the terms are self-explanatory. By comparing Eqs. 5.4 and 5.16, it is evident that Miller multiplication of C_{cb} of Q2 is now reduced as represented by the terms $(1 + (1/g_{m2} + R_2)^{-1}/g_{m3})$ instead of $(1 - A)$. By scaling the emitter areas of Q1-Q3 to minimize the total time constant, there is predicted a $\sim$ 40 % improvement in the stage bandwidth relative to the Darlington amplifier.

The base of Q3 is biased through the same supply as the collector of Q1, because both the nodes are at the same potential. R_b forms a voltage divider network with R_f, to bias the base of Q1 at the desired voltage. It is externally connected through a bias-tee because of the limited current capacity of on-chip resistors. This amplifier was designed for the same gain as the first amplifier, and it had a simulated bandwidth of about 70 GHz. The power consumption of the IC is 64 mW. Figure 5.13 shows a



Q1 = 1 X 25 μm^2
Q2 = Q3 = 1 X 18 μm^2
R_f = 200 Ω
R_1 = 45 Ω
R_2 = 5 Ω
R_b = 500 Ω

V_{cc} = 2.1 V
V = 1.9 V
I_1 = 16 mA
I_2 = 13 mA

Figure 5.12: Schematic circuit diagram of the Darlington-cascode feedback amplifier.

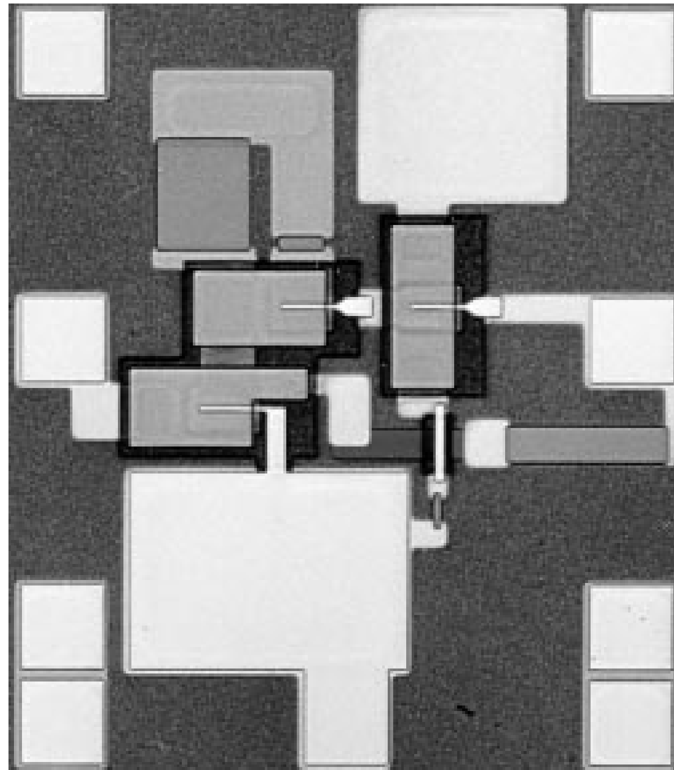


Figure 5.13: Photomicrograph of the Darlington-cascode amplifier.

photomicrograph of the amplifier. The chip dimensions are the 0.35 mm × 0.4 mm.

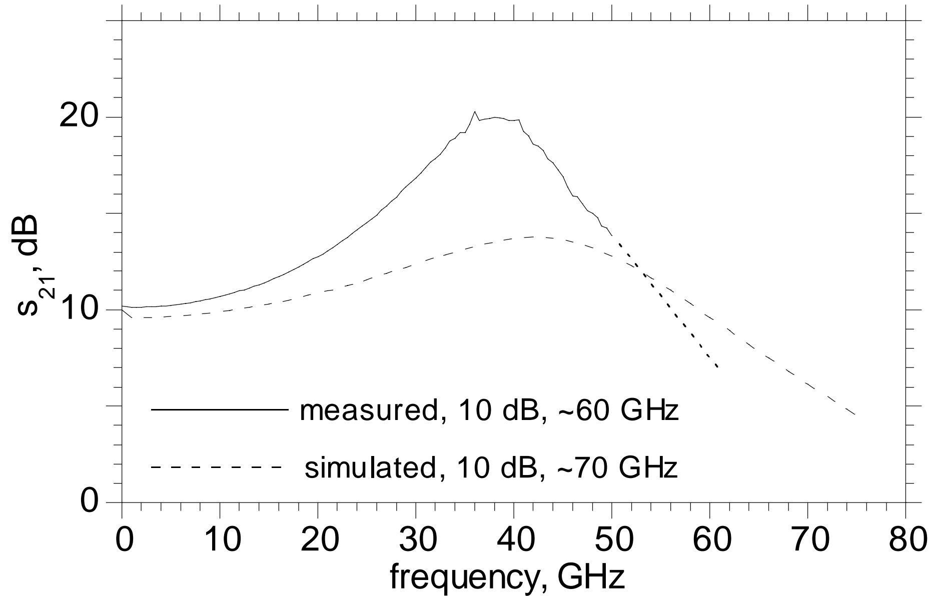


Figure 5.14: Measured forward gain s_{21} of the amplifier.

The amplifier characteristics were measured with a network analyzer to 50 GHz. Figure 5.14 shows the forward gain s_{21} of the amplifier. The low-frequency gain is 10 dB and the 3-dB bandwidth (relative to the low-frequency gain) is greater than 50 GHz. Network analyzer measurements were also done between 75 and 100 GHz in an attempt to determine the amplifier bandwidth. The bandwidth was found to be between 50 and 75 GHz. Interpolation to find the exact bandwidth could not be done because the gain characteristic does have a well behaved roll-off. Excessive gain peaking and reflection coefficients greater than 0 dB are observed. To improve the gain-bandwidth and the return losses, mirror-Darlingtons [47] and f_τ-doublers [48] have to be employed.

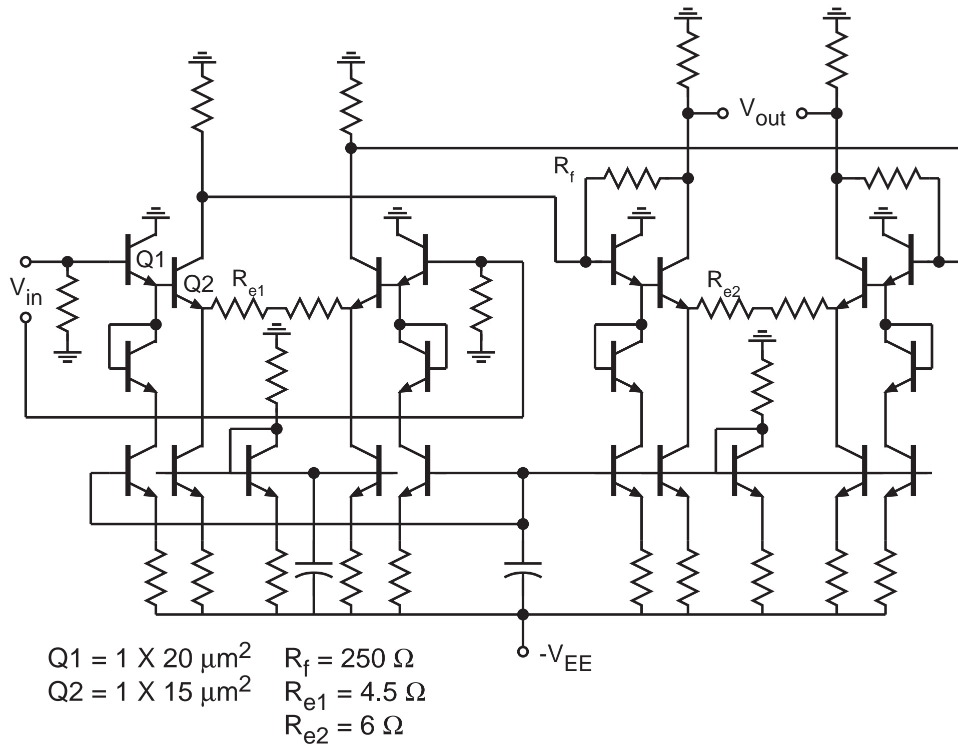


Figure 5.15: Schematic circuit diagram of the differential amplifier.

5.3 Differential amplifier

In addition to the single-ended resistive feedback amplifiers of the previous section, differential DC coupled amplifiers were also designed and fabricated. As with all differential circuits, the design is based on a half-circuit model, and is therefore strongly related to the design of the single-ended amplifiers. Differential amplifiers have symmetric and non-saturating limiting characteristics set by transistor cutoff, and AGC can be applied without introducing DC level shifts to the signal. For this reason differential stages are preferred for the AGC/limiting [49, 50] stages of optical receivers. Future high-speed fiber-optic systems will require amplifiers with very high bandwidths. A two stage DC-coupled broadband lumped differential amplifier is described in this section.

Figure 5.15 shows a schematic circuit diagram of the amplifier with the element values. A variation of the classic transadmittance-transimpedance

design by Cherry & Hooper [51], with 50 Ω interstage impedances is used here. The first stage has a emitter-coupled pair with input emitter follower buffers with emitter degeneration. 50 Ω shunt input resistors set the input impedance of the overall amplifier. 50 Ω output resistors are used in the collectors, setting a 50 Ω output impedance of the first stage. The second stage employs transimpedance loading to obtain a 50 Ω input impedance and 50 Ω output impedance. Level-shifting diodes are used to bias all transistors below breakdown. Active biasing with transistor current mirrors and a single negative supply is used. Input and output DC levels are designed to be the same at -0.45 V thus enabling DC coupling between successive stages of the amplifier. The transadmittance of the first stage is given by $g_{m1,extrinsic}$. The transimpedance of the second stage is given by the feedback resistor R_f. Hence the overall gain is $g_{m1,extrinsic}R_f$. By varying the bias currents in the first stage, the amplifier gain can be varied. The emitter currents of the emitter-coupled pair in the first stage was varied with a external variable resistor in the current reference transistor. In real systems, this is done by applying a control voltage. Whether applied via a variable resistance or a variable voltage, both vary the reference current and the bias current through the input transistor pair, and thus change the gain of the amplifier. The amplifier bandwidth is designed to be controlled by the second stage, thus giving a variable-gain (constant bandwidth) amplifier. Bandwidth analysis is similar to that of the Darlington amplifier. The first stage has a current dependent input time constant, and hence the stage bandwidth varies with bias. The second stage time constant is made dominant and hence the overall amplifier bandwidth is controlled by the second stage, independent of the first stage bias. The simulated gain-frequency characteristics are shown in figure 5.17. The bandwidth was about 50 GHz and the gain could be varied from 7-13 dB by changing the bias current in the gain control stage from 4-12 mA as shown. Figure 5.16 shows a photomicrograph of the amplifier. A total of 22 transistors are used. The chip dimensions are 0.75 mm × 0.44 mm.

The amplifier performance was measured with a network analyzer to 50 GHz. Only single-ended characteristics (two-port) were measured, with the other ports terminated in 50 Ω. At the designed bias conditions (shown on graph), variable gain operation was observed as desired. I_{ref} is the current through the reference transistor in the amplifier first stage. The input DC level of -0.45 V was applied with a independent supply. However, the gain

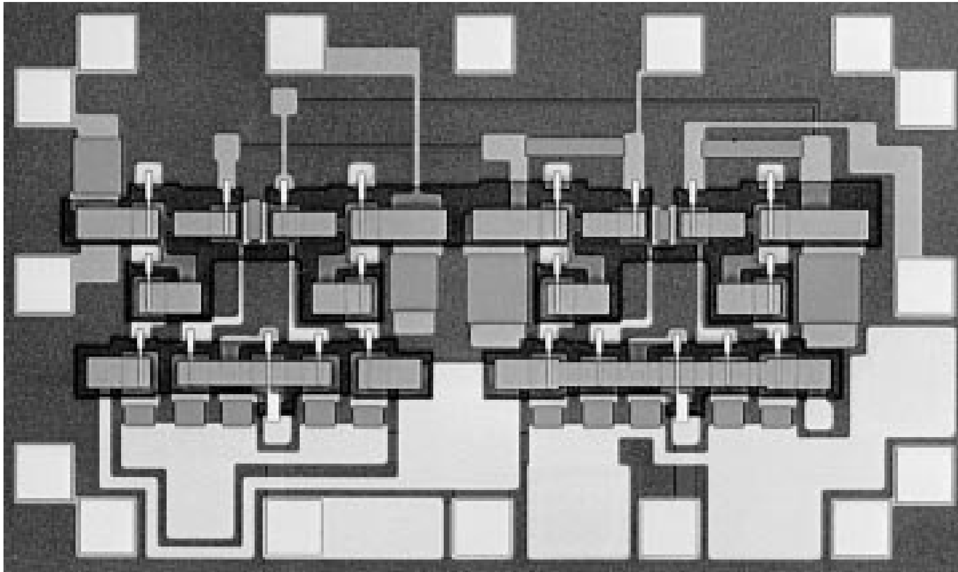


Figure 5.16: Photograph of the differential amplifier IC (0.75 mm × 0.44 mm).

characteristics exhibited oscillations at ~ 40 GHz as shown in figure 5.18. The origin of these oscillations is as yet unclear. Layout parasitics may be responsible as may the negative resistance effects seen in the Darlington stages, particularly in the second stage. By lowering the bias voltage (biasing the transistors at reduced V_{CE}), stable operation was achieved. Figure 5.19 shows the forward gain s_{21} of the amplifier. The low-frequency gain is 11 dB and the 3-dB bandwidth is >50 GHz. However, at this bias, the gain could not be varied independent of the bandwidth, as the first stage now affects the bandwidth as well as gain. The dashed curve shows the gain of a different amplifier at different bias conditions. A lower bandwidth and a more flat response is obtained. The bias voltages and overall current is the same, but the reference current in the first gain stage is reduced (from 14 to 11 mA) and that of the second gain stage is increased. The difference in gain-bandwidth could also be due to spread in transistor characteristics across the wafer. The low frequency gain is the same, but the in-band gain variation is less than 1 dB, and the bandwidth is 40 GHz for the dashed curve. Such flat gain response is important for acceptable bit-error-rates in high-speed systems. The gain ripple at high frequencies is a result of us-

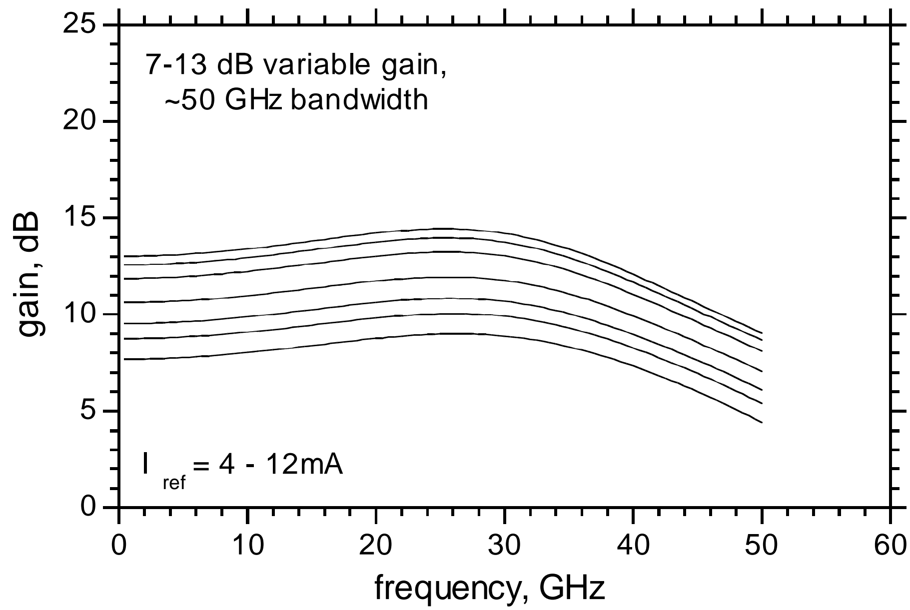


Figure 5.17: Simulated variable forward gain s_{21} of the amplifier. I_{ref} is the current through the reference transistor in the amplifier first stage.

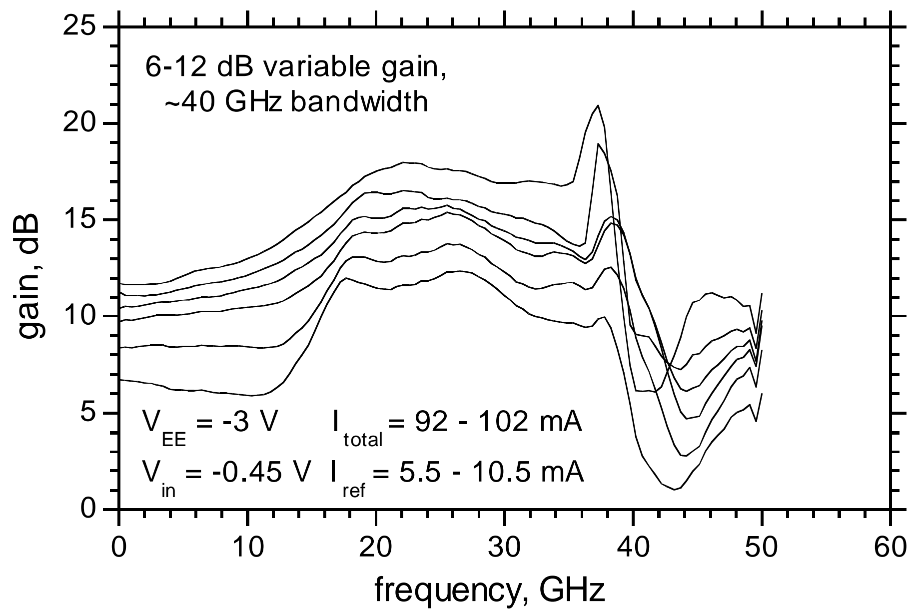


Figure 5.18: Measured variable forward gain s_{21} of the amplifier. I_{ref} is the current through the reference transistor in the amplifier first stage.

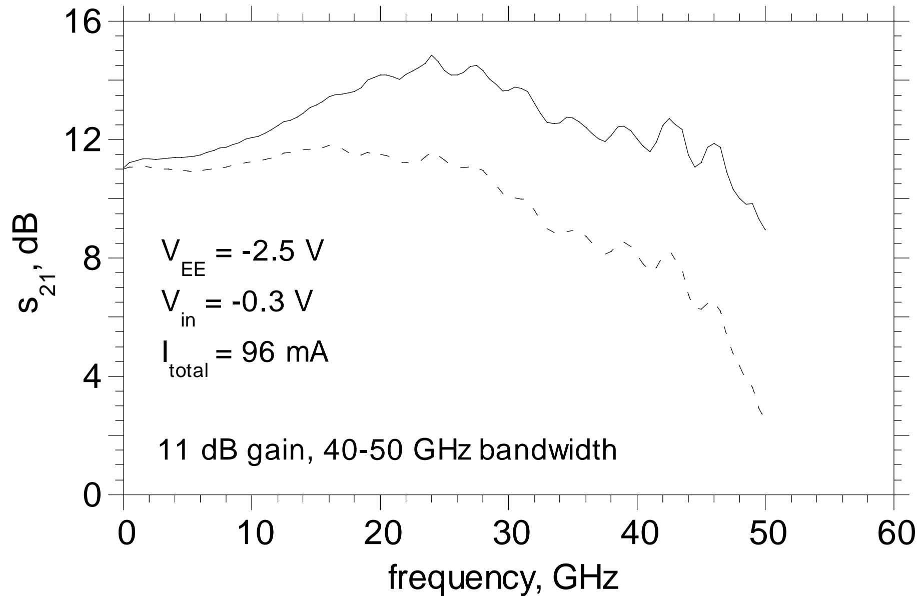


Figure 5.19: Measured forward gain s_{21} of the amplifier.

ing a 2-port calibration with off-chip terminations of the two unused ports. Figure 5.20 shows the input and output return losses and the reverse isolation of the amplifier. The reverse isolation is very good because there is no direct feedback path from the output to the input. The input return losses are poor at high frequencies as in the case of the Darlington amplifiers. The output return loss is poor even at low frequencies due to the low V_{CE} bias leading to poor output conductance of the device. The IC consumes 250 mW DC power.

5.4 Distributed amplifiers : Theory

This section reviews distributed amplification theory briefly. In general, amplifying circuits can be classified into two categories : lumped and distributed. Lumped circuits can either be resonant or non-resonant. Resonant circuits are impedance-matched at the input and the output to the generator and the load for some frequencies and hence, achieve the full power gain of the device for those frequencies. Non-resonant circuits have broad-

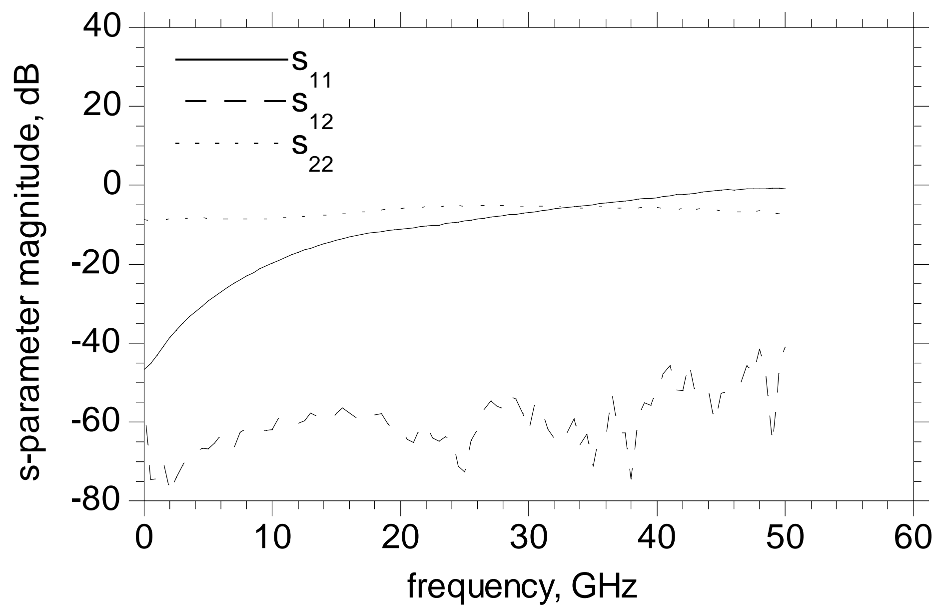


Figure 5.20: Measured input return loss s_{11}, output return loss s_{22}, and reverse isolation s_{12} of the amplifier.

band gain up to frequencies limited by device parasitics. Since they are not impedance-matched, they achieve power gains well below those available from the device. Distributed circuits incorporate a set of lumped semiconductor devices into a transmission line. The lines provide matching at the input and output. Device parasitics are absorbed into the transmission lines, and hence broadband gain limited by the device available power gain and Bragg cutoff frequency of the distributed structure is obtainable.

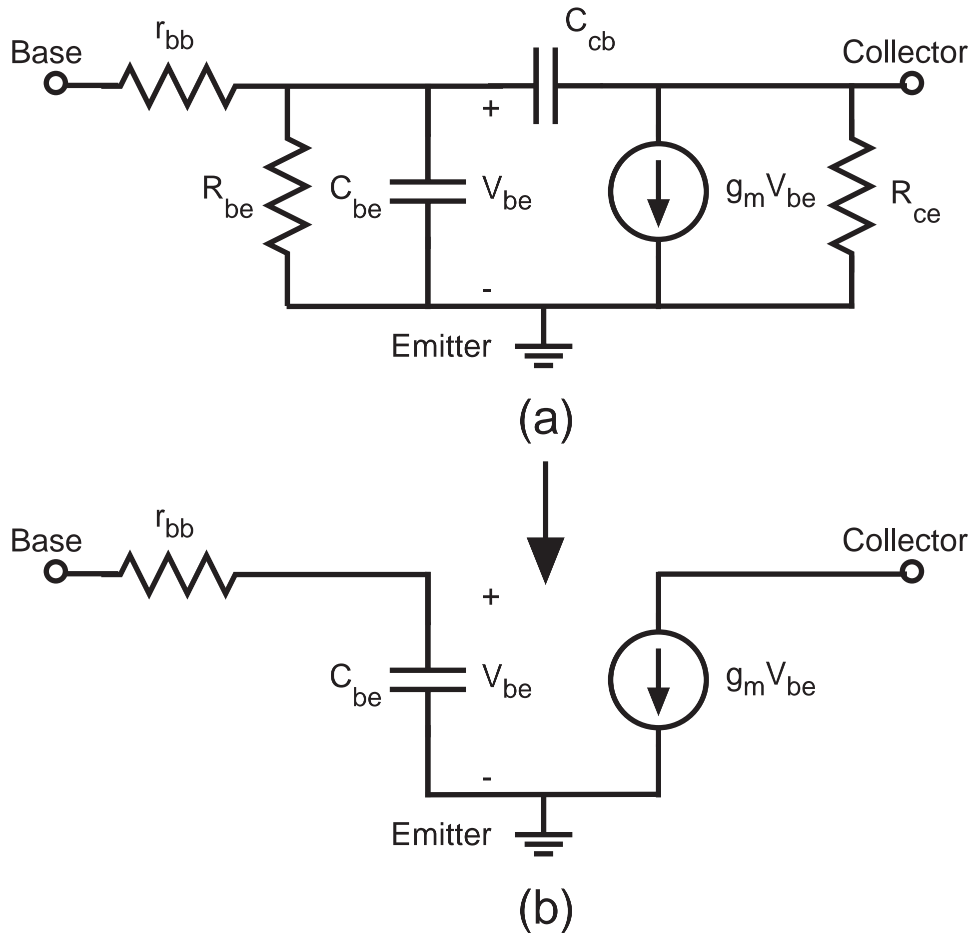


Figure 5.21: (a) Small-signal equivalent circuit of the HBT and (b) simplified model.

Figure 5.21(a) shows the small-signal hybrid-π equivalent circuit of a HBT. Developing the theory of distributed amplification with such a model

is extremely complex, especially because of the feedback capacitance C_{cb} and the input resistance R_{be}, and will not help gain insights into design and trade-offs. A few simplifications are first made. First, let us look at a cascode cell as the active device instead of a single HBT. A cascode cell has lower output conductance and lower Miller-multiplied feedback capacitance than a single HBT. Hence, these two elements can be ignored, at least for amplifiers not designed near extreme limits of HBT available gain. The input resistance R_{be} complicates the input analysis and is effective only at low frequencies, especially for high current gain β. At high frequencies, it is shorted out by the input capacitance and hence it can also be ignored. The extrinsic emitter resistance can be absorbed by emitter degeneration and the collector resistance is negligible. The final model that will be used is shown in figure 5.21(b). The element values scale with transistor area in the usual fashion.

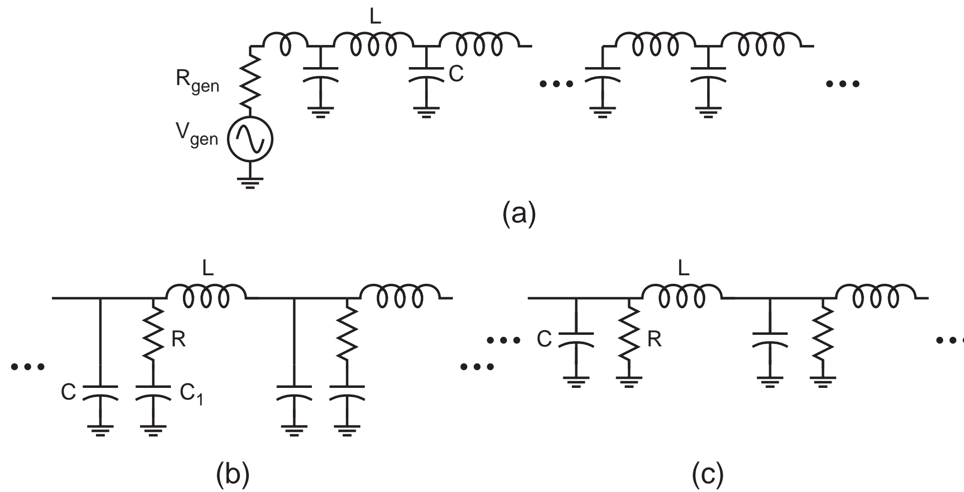


Figure 5.22: Periodic synthetic transmission lines (a) without loss, (b) with frequency-dependent loss and (c) with frequency-independent loss.

Figure 5.22(a) shows a LC synthetic line with no attenuation below the Bragg frequency and very high attenuation above it. The Bragg frequency ω_B for such a distributed structure is given by

$$\omega_B = 2/\sqrt{L/C} \tag{5.17}$$

For frequencies well below the Bragg frequency, the structure is lossless, has a characteristic impedance $Z = \sqrt{L/C}$ and a per section delay $\sqrt{LC}$. If a small series resistance R is added with a portion C_1 of the shunt capacitance as in figure 5.22(b), the frequency-dependent attenuation becomes

$$\alpha \simeq \omega^2 {C_1}^2 R Z_o/2 \tag{5.18}$$

Adding a large shunt loading resistance R as in figure 5.22(c) introduces a frequency-independent loss as

$$\alpha \simeq Z_o/2R \tag{5.19}$$

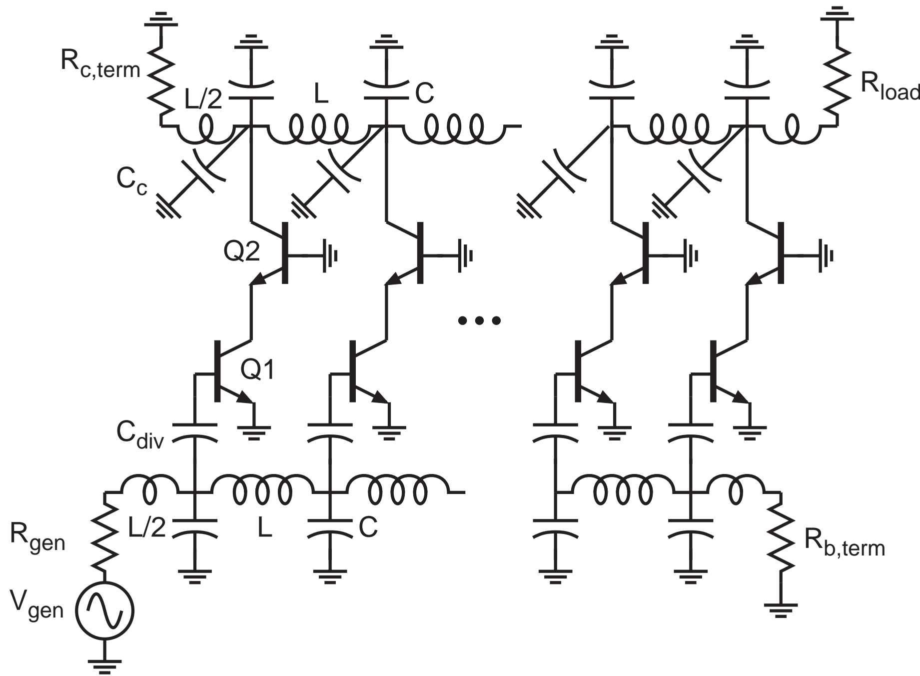


Figure 5.23: Circuit diagram of the traveling-wave amplifier.

Figure 5.23 shows the schematic circuit diagram of the amplifier with cascode gain cells loading a periodic synthetic transmission line and figure 5.24 shows it's small signal equivalent circuit. The base and collector lines are terminated with the characteristic impedance Z_o. Both the input and output transmission lines are assumed to have the same characteristic impedance for velocity matching as we shall later see. C_{div} is the

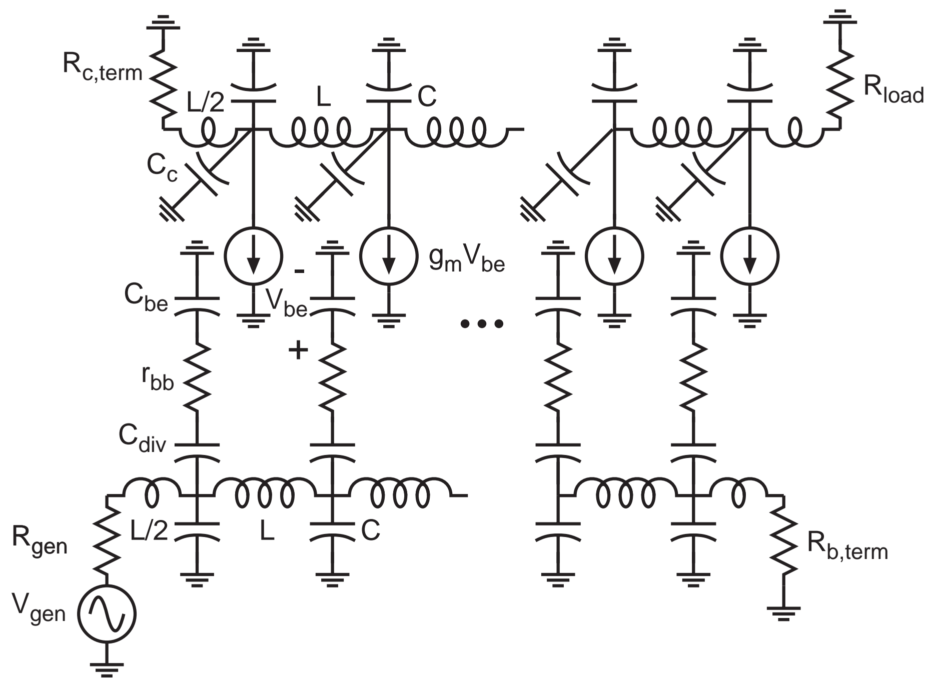


Figure 5.24: Small signal model of the traveling-wave amplifier.

input division capacitor which helps improve gain-bandwidth. If M is the capacitive-division ratio,

$$M = C_{div}/(C_{div} + C_{be}) \tag{5.20}$$

C_c is a shunt capacitor in the collector line for velocity matching between the input and output lines and is needed because only the input line is loaded with the device capacitance. The line inductance and capacitance along with the device capacitances are designed to synthesize input and output lines with characteristic impedance Z_o. The amplifier has N sections. The following equations are derived from the above equations. For the input line :

$$\omega_{B,b} = 2/\sqrt{L/(C + MC_{be})} \tag{5.21}$$

$$Z_o = \sqrt{L/(C + MC_{be})} \tag{5.22}$$

$$\alpha_b \simeq N\omega^2 M^2 {C_{be}}^2 r_{bb} Z_o/2 \tag{5.23}$$

For the output :

$$\omega_{B,c} = 2/\sqrt{L/(C + C_c)} \tag{5.24}$$

$$Z_o = \sqrt{L/(C + C_c)} \tag{5.25}$$

$$\alpha_c \simeq 0 \tag{5.26}$$

For each transistor, the input signal propagates through a fraction of the base line before driving that transistor's input and producing a collector current $Mg_m V_{be}$. The collector current generates a forward wave on the collector line of amplitude $Mg_m V_{be} Zo/2$. All the individual waves will add in phase if the input and output lines are perfectly delay-matched. The overall amplifier gain is

$$A_v = -NMg_m Zo/2 \tag{5.27}$$

The number of sections is limited by the input line losses (since output line losses are negligible). The input voltage to the Nth stage is attenuated by

$e^{-(N-1/2)\alpha_b}$. The maximum number of transistors N_{max} for a given desired bandwidth ω_{BW} is given by

$$N_{max}\omega_{BW}{}^2 M^2 C_{be}{}^2 r_{bb} Z_o \simeq 1 \tag{5.28}$$

Using Eqs. 5.27 and 5.28, the gain-bandwidth product is given by

$$A_v \omega_{BW}{}^2 = g_m / M C_{be}{}^2 r_{bb} \tag{5.29}$$

If aggressive capacitive-division (smaller M) is used, the number of sections used can be higher and gain bandwidth improves, but not without limits. In the above derivation, the transmission line skin-effect and radiation losses have been neglected. These losses impact the highest attainable gain-bandwidth in a given technology. If these losses are made negligible, the available power gain from the device can be achieved. A traveling-wave amplifier fabricated in the transferred-substrate HBT process will now be presented.

5.5 Traveling-wave amplifier

Traveling-wave amplifiers (TWAs) are very broadband circuits. Broad bandwidth is achieved by absorbing the transistor parasitics into synthetic input and output 50 Ω transmission lines. Flat gain is achieved up to the Bragg frequency of the distributed line, and limited by the available gain from the device. Hence, the amplifier gain-bandwidth product depends critically on the transistor f_{max}. To date, TWAs based on HEMTs have demonstrated considerably higher bandwidths than those based on HBTs [52, 53], primarily due to the higher f_{max} of HEMTs. Transferred- substrate HBTs have high f_{max}, comparable to that of high-performance InGaAs/InAlAs/InP HEMTs, and, should thus also yield TWAs with very high bandwidths.

TWA design with HEMTs has been covered in detail in [52]. HEMT traveling wave amplifiers (TWAs) with $\sim$ 100 GHz bandwidths have been demonstrated [52, 54, 55]. Pusl et al. [52] used capacitive voltage division on the gate synthetic line to obtain very wideband TWAs. Capacitive division decreases the frequency-dependent losses on the input synthetic transmission line as shown in the previous section. With these losses reduced, the number of TWA cells can be increased to increase TWA gain. In this manner, the feasible gain for a given design bandwidth is increased.

With very small capacitive division ratios, losses associated with the device input resistance are reduced to the point where other loss mechanisms are significant. If the dominant loss mechanisms are the device series input resistance and the shunt output conductance, the capacitive division TWAs can obtain gain-bandwidth products close to the transistor f_{max}.

For design bandwidths above 100 GHz, TWA design is also strongly impacted by both the losses and physical dimensions of the input synthetic transmission line. With small capacitive division ratios and design bandwidths above 100 GHz, transmission-line skin-effect losses become the dominant factor limiting the amplifier bandwidth, and the required transmission-line lengths become shorter than the physical dimensions of the devices which leads to a physical layout problem.

HBT TWA design differs considerably from that using HEMTs. The HBT transconductance - hence input capacitance ($C_{be} \simeq g_m/2\pi f_\tau$) - per unit HBT emitter area is large. To obtain the desired Bragg frequency, either very small HBTs must be used, or input capacitive division [52] must be employed. Very small HBT areas lead to high input (base) resistance, higher than HEMT input (gate) resistance (r_{bb} $vs.$ r_{gate}). This favors the use of very high capacitive division ratios for HBT TWAs. As explained before, bandwidth is also strongly influenced by the frequency-dependent transmission line losses, which become dominant at high frequencies. For transmission lines on a BCB substrate as in the transferred-substrate HBT IC process, the line skin-effect losses are reduced and the wave velocity is increased due to low dielectric constant of the BCB substrate. A increased wave velocity implies longer transmission lines for a given electrical delay. The amplifier can then be laid out. The low transmission line losses make high bandwidths feasible.

Figure 5.25 shows a schematic circuit diagram of the capacitive-division TWA. Cascode-connected HBTs are used for several reasons. Without the cascode cell, the frequency dependent output impedance of the common-emitter stages would introduce large output line losses. This is a second feature of HBT TWAs that differs substantially from HEMT TWAs. The output impedance of a HEMT is - to first order - R_{ds}. For a HBT driven by a resistive generator impedance, the frequency-dependent output impedance arises from feedback through C_{cb}. This is the origin of the HBT s_{22} data presented in chapter 4. Cascode connected transistors greatly increase the cell output impedance, decreasing collector line losses to the point where

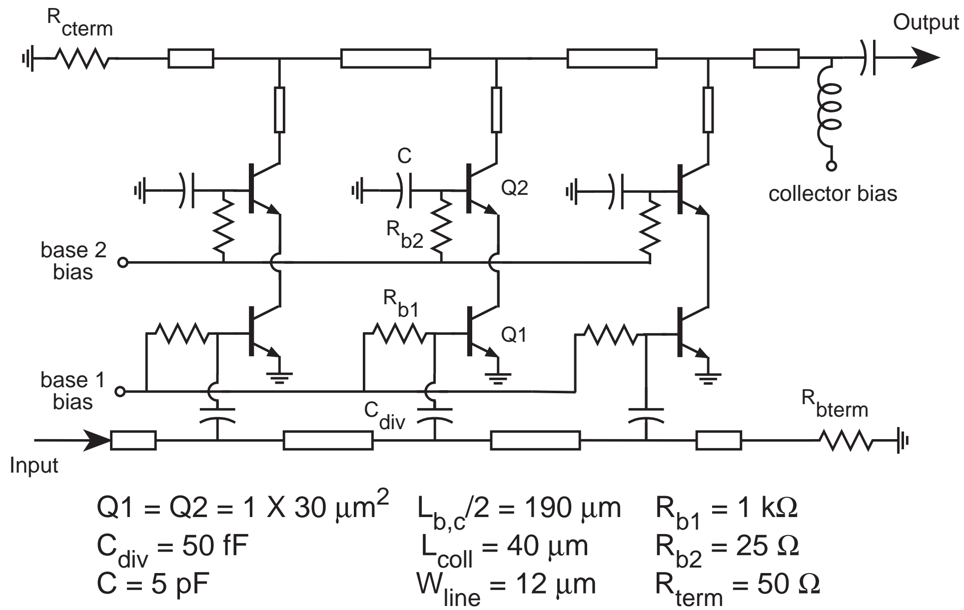


Figure 5.25: Schematic circuit diagram of the HBT TWA.

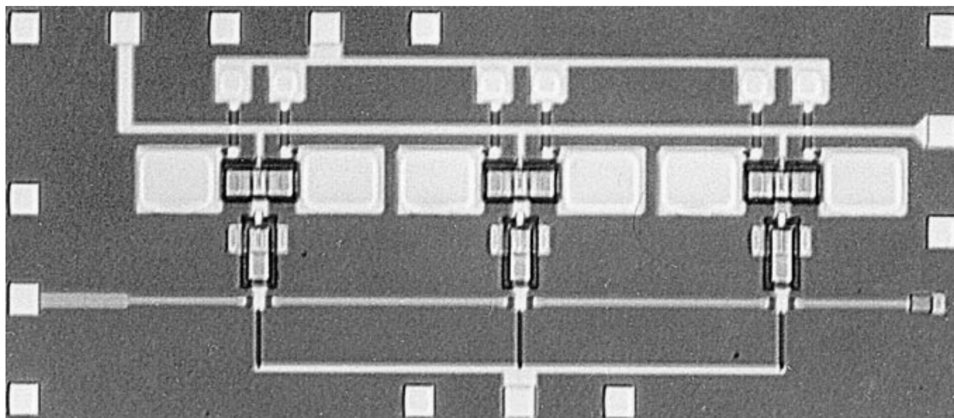


Figure 5.26: Photomicrograph of the HBT TWA.

input line losses dominate.

The base and collector lines are composed of 75 Ω microstrip line sections. C_{div} is the division capacitor at the input of the common-emitter transistor Q1. A short length of microstrip is used at the output of the cascode cell to improve velocity matching between the input and output lines. The microstrip lines, together with the division capacitor and the cascode stage synthesize 50 Ω input and output lines. R_{bterm} is the 50 Ω base-line termination resistor. R_{cterm}, the collector-line termination resistor is off-chip to sustain the high collector bias current, and is connected through a microwave probe. R_{b1} is a large resistor to bias the input of Q1. The base of the common-base transistor Q2 is biased through an independent supply. AC ground at this node is provided by large bypass capacitors. R_{b2} provides decoupling between the multiple cells and prevents oscillations from resonance between the bias probe inductance and the bypass capacitors. The collector bias is through a bias tee at the output of the chip. Amplifiers with 3 cascode cells were fabricated. The simulated gain is about 7 dB and the designed bandwidth is 90 GHz. Figure 5.26 shows a photomicrograph of the fabricated chip. The die size is about 1.4 mm × 0.6 mm.

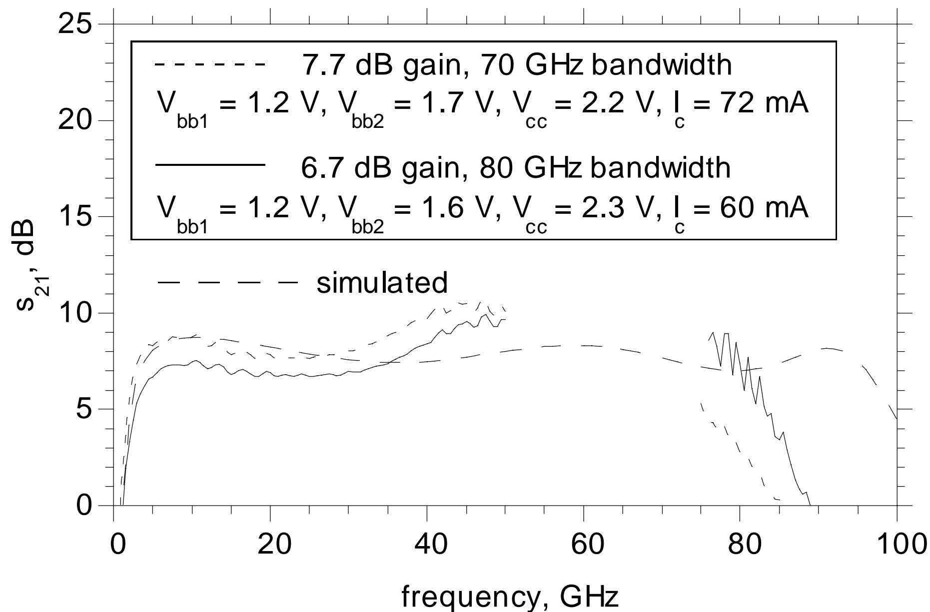


Figure 5.27: Measured forward gain s_{21} of the amplifier.

The amplifiers were tested with network analyzers from DC-50 GHz and 75-110 GHz. Figure 5.27 shows the forward gain of the amplifier under two different bias conditions. The solid curve shows a mid-band gain of about 6.7 dB. The 0-dB bandwidth (where the gain drops below the mid-band gain) is 80 GHz. The 3-dB bandwidth is 85 GHz. The dashed curve shows the gain at a different bias condition. The mid-band is 7.7 dB, the 0-dB bandwidth is $\sim$ 70 GHz and the 3-dB bandwidth is 76 GHz.

From this curve, we can also observe gain peaking at high frequencies. The gain-frequency response of TWAs is strongly impacted by device f_{max} and the designed Bragg frequency. During design, a conservative HBT model with a 200 GHz f_{max} (wafer B) was assumed. HBTs on wafer C have 370 GHz f_{max} which results in the observed gain peaking. Given the 370 GHz f_{max}, redesigning the amplifier would permit bandwidths greater than 70-80 GHz. The low frequency cut-off is about 2 GHz and is determined by the transistor f_τ/β. Figure 5.28 shows the input and output return losses and the reverse isolation. The amplifier output return loss s_{22} shows many resonances because of the off-chip collector-line termination. The chip consumes about 250 mW.

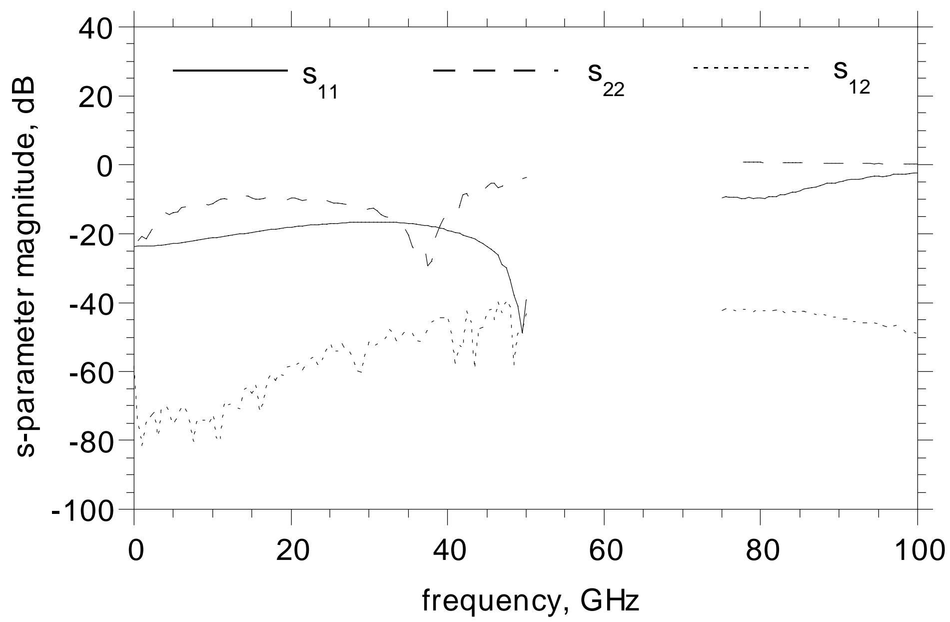


Figure 5.28: Measured input return loss s_{11}, output return loss s_{22}, and reverse isolation s_{12} of the amplifier.

Chapter 6

Conclusions

The transferred-substrate HBT IC process was developed from a demonstration device technology to a high performance IC technology. Several changes were made in the basic device structure, the material growth and the process. The devices and passive elements were modeled for integrated circuit simulations. Hybrid-π and SPICE models were developed for HBTs, but only the hybrid-π models were used in circuit simulations. Biasing of the circuits at the desired points was done by hand. The first demonstration integrated circuit fabricated in this process was a Darlington feedback amplifier. Two transistors were used. Series and shunt feedback was used. The amplifier was designed for 50 Ω input and output impedance. This amplifier had 13 dB gain, 50 GHz bandwidth. An improvement on this basic design, a Darlington-cascode amplifier was then fabricated. This amplifier had three transistors. The gain was 10 dB and the bandwidth was greater than 50 GHz. Since transferred-substrate HBTs have a higher f_{max} than f_τ, a distributed amplifier should achieve very high bandwidths. A capacitive-division traveling-wave amplifier with six transistors was fabricated. This amplifier had 85 GHz bandwidth, 6.7 dB gain. Finally, a two-stage broadband differential amplifier was designed and fabricated. This amplifier has 50 Ω input and output impedance and is DC coupled. The gain and bandwidth are 11 dB and 50 GHz respectively.

As explained earlier, due to our limited lithographic capabilities, the technique of "staggering" had to be employed, thus wasting wafer area. With the use of projection lithographic systems in future, this problem can be solved. This will also enable smaller alignment tolerances and hence

smaller die areas per circuit. Apart from the circuits that were intentionally mis-aligned, the *circuit* yield was very high, even for the differential amplifier with twenty-two devices. Hence, larger scales of integration are possible. The circuits presented in this thesis have some of the best performance ever reported in literature, especially in terms of bandwidth. This is a result of high intrinsic device bandwidths and the special IC process features highlighted earlier. Scaling of the emitter and collector to sub-micron dimensions should achieve even higher bandwidth devices and circuits. The use of the In/Pb/Ag solder for substrate transfer reduces yield by retaining voids in it during the process of wafer bonding. Also, the final carrier substrate (GaAs) is electrically non-conducting. This could be a problem if the ICs have to be diced and packaged. Both these problems can solved at once by the use of thick ($\sim$ 200 μm) electroplated copper for the ground plane, which also becomes the carrier. In most circuits, f_τ is very critical in determining the circuit performance. Hence the f_τ needs to be improved by reducing the base and collector layer thicknesses and by introducing more bandgap grading in the base. The breakdown voltage of the devices is very low (1.5 V @ 10^5 A/cm^2) due to the narrow bandgap InGaAs collector. For modulator drivers and power amplifiers, high breakdown voltage is needed. InP collectors or composite collectors with quarternary semiconductor layers can improve breakdown. The extrinsic base regions can be regrown with heavily-doped wide-bandgap material graded to a low-bandgap materialfor metal contact. The wide-bandgap material will improve the electron confinement in the device thus increasing the current gain and the heavy doping will reduce the base resistance thus increasing f_{max}. The resistors in the current process have limited current-carrying capability. Often, this proved to be a major limitation, forcing lower bias currents or off-chip resistors. Hence, the current capacity needs to be improved. One way to achieve this would be to have thermal vias on the resistors, similar to the devices. A parasitic capacitance is then formed in series with the resistor, which should be included in the model. In the MIM capacitors, pinhole formation might be a problem for very large area capacitors. A quantitative analysis is required to determine how capacitor yield varies with capacitor area.

Accurate device modeling is very important in integrated circuit design. As the technology emerges, the device performance changes. Hence, the simulated and measured circuit performance differ as shown earlier. It would be advantageous to be able to have minor or no variation in de-

vice performance from one run to another. In this thesis, only small signal hybrid-π models were used, and biasing was done manually. As the integration levels increase, this becomes difficult, and full SPICE models including dc bias, breakdown and Kirk effect have to be used in simulations. Layout of large circuits need a library-based modular approach and computer design rule checking (DRC). Finally, a layout-driven simulation approach is needed for dense circuits with long interconnect wires.

In conclusion, analog integrated circuits with record performance have been fabricated in the transferred-substrate HBT IC technology. With improvements in lithographic capabilites, device scaling and device improvements outlined above, very high bandwidth devices with $f_{max} \sim 700$ GHz and very high-performance medium-scale integrated circuits operating at 100-200 GHz are feasible.

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