University of California
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Digital Integrated Circuits in the Transferred-Substrate HBT Technology

A Dissertation submitted in partial satisfaction
of the requirements for the degree of
Doctor of Philosophy
in
Electrical and Computer Engineering
by
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June, 1998

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June, 1998

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Abstract

Digital Integrated Circuits
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Rajasekhar Pullela

The explosive growth in the fiber-optic and wireless telecommunications market over the last ten years has increased the demand for broadband analog and high clock-rate digital systems. Future fiber-optic communication systems will operate at data rates much higher than 40 Gb/s. ADCs in military radar receivers and multi-channel commercial wireless receivers require as high a resolution as 16 effective bits (96 dB SNR) at a bandwidth of 100 MHz. Transistors with f_t and f_{max} in the range of 500 GHz to 1 THz will be necessary to meet these requirements. The transferred-substrate HBT technology is suitable for these high speed and high peformance applications. In addition to high device bandwidth, the transferred-substrate process offers the significant advantages of a low parasitic microstrip wiring environment with integral ground plane and a low thermal impedance environment for high power operation and increased packing density. HBTs with peak f_t of 220 GHz and $f_{max} > 400$ GHz have been fabricated; the high f_{max} is due to the low C_{cb} from the transferred substrate process. First digital ICs - current mode logic (CML) and emitter coupled logic (ECL) flipflops connected as static 2:1 frequency dividers, operating at a peak clock frequency of 47 GHz and 48 GHz respectively, have been demonstrated. The technology has the potential to yield ICs at 100 Gb/s clock rates. Current process technology is capable yielding at least 100 component circuits with reasonable yield. Higher levels of integration and yield are possible if the stepper is used for photolithography.

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Chapter 1

Introduction

The internet and the globalization of business and trade has created an unprecedented demand for higher bandwidth and higher complexity communication networks. The explosive growth in the wireless and fiber-optic telecommunications market over the last ten years has increased the need for broadband analog and high clock-rate digital systems.

1.1 Wireless communication systems

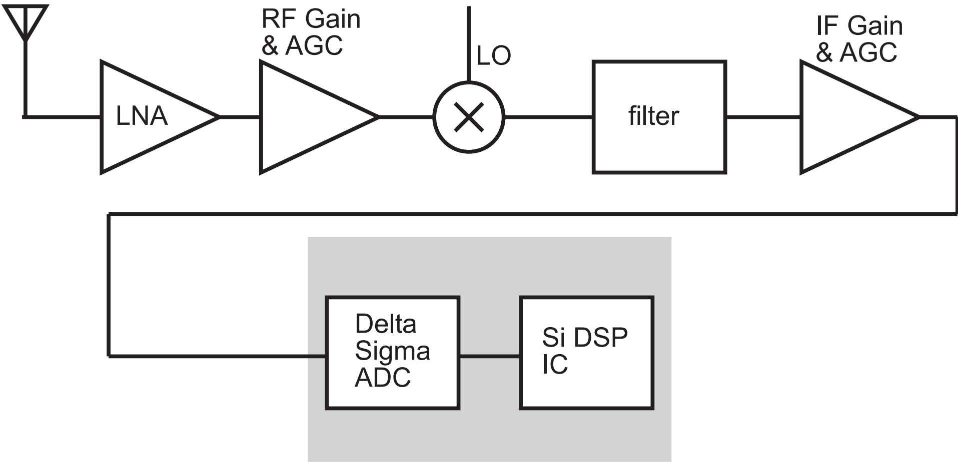


Figure 1.1: Block diagram of advanced digital wireless receiver

Wireless receivers incorporate several steps of mixing and filtering before the RF signal is down-converted to baseband. Mixers and filters are analog circuit components requiring very careful design to meet the speed (bandwidth), noise and linearity (dynamic range) specifications. Because of the cost, physical size and design effort associated with these components, efforts are now underway to replace analog components with digital signal processing (1.1). This requires a wide band and high dynamic range analog to digital converter (ADC) at the front end. After digitization, down conversion and filtering is done in the digital domain. The system design thereafter becomes a software exercise analogous to the design of a digital signal processing (DSP) system.

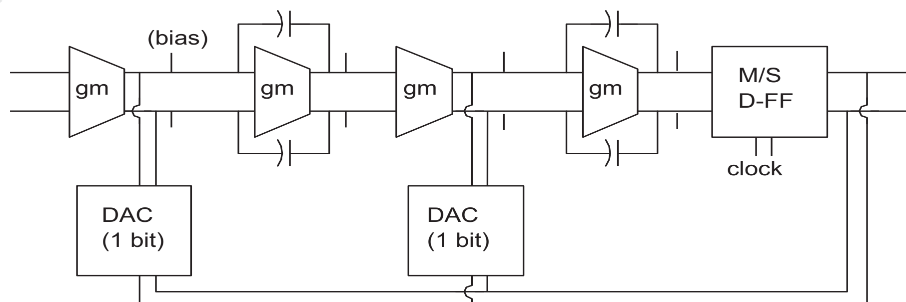


Figure 1.2: Block diagram of second order sigma delta modulator

The bandwidth and the signal to noise ratio (SNR) of the receiver are often limited by ADC performance. State of the art Nyquist rate ADCs have achieved 8-b 2 GS/s [1] or 6-b 4 GS/s performance with Rockwell AlGaAs/GaAs HBTs [2]and 4-b 8GS/s in the Hughes InP technology [3]. Oversampling sigma-delta ADCs operating at clock rates up to 3-4 GHz in the Hughes InP HBT technology have achieved 9-b dynamic range over a bandwidth of 50 MHz [4], [5]. ADCs in military radar receivers and multichannel commercial wireless receivers require as high a resolution as 16 effective bits (96 dB SNR) at a bandwidth of 100 MHz. Such high resolutions can only be implemented with sigma-delta converters. The block diagram of a 2nd order sigma-delta modulator is shown in fig. 1.2. Adopting

the circuit implementation of the modulator used in [3], greater than 40 GHz clock rate is required to meet the specifications. Transistors with f_t and f_{max} in the range of 500 GHz to 1 THz will be necessary. Higher order sigma-delta modulators reduce the clock rate to transistor bandwidth ratio. Even so, a large improvement in the transistor bandwidth is necessary before such circuits are feasible.

1.2 Optical fiber communication systems

Fiber-optic networks at 10 Gb/s (OC-192) are currently in deployment, while 40 Gb/s systems have been demonstrated in some laboratories [6], [7], [8], [9]. More recently, enhancements to the data rates have been achieved using wavelength division multiplexing (WDM), wherein several TDM (time division multiplexing) systems are connected in parallel. As the number of parallel TDM systems increases, so does the complexity, cost and size of the WDM system. Improving the bandwidth of the electronic components increases the data-rate of TDM systems, reducing the number of parallel channels required for a desired data-rate. A combination of fast TDM - 100 Gb/s or higher data-rate TDM systems, and WDM is necessary to efficiently realize the THz data rates required in future optical communication systems.

Fig. 1.3 shows a fiber-optic receiver which consists of analog amplifier stages, a phase lock loop (PLL) for clock recovery, a demultiplexer circuit and master-slave D flip-flops used as decision circuits and static frequency dividers. The performance of the D flip-flop limits the maximum clock rate in the system. To enable easy testing, the D flip-flop is often configured as a static frequency divider. High clock rate static frequency dividers have been achieved in various technologies - 40 GHz in the Toshiba AlGaAs/GaAs HBT technology [11], 44 GHz in the Hitachi InP/InGaAs HBT technology [12], 35 GHz in Seimens Si bipolar technology [13], 42 GHz in Seimens SiGe technology [14] and more recently 50 GHz in the SiGe HBT technologies [15]. The maximum clock speed in all these technologies is limited by the bandwidth of the devices. 100 GHz clock rates in future TDM systems can only be achieved by doubling the existing transistor bandwidth.

Bipolar transistors are suitable for high speed circuits because of their reproducible DC characteristics, excellent control of turn-on voltage, high transconductance and high bandwidth. Wide band-gap emitter in Hetero-

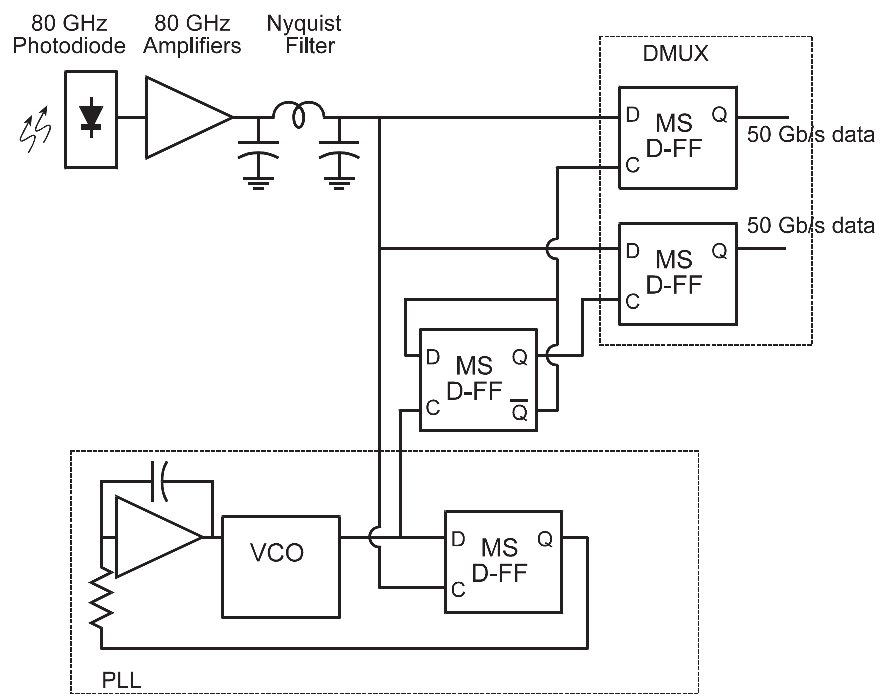


Figure 1.3: Block diagram of fiber-optic receiver

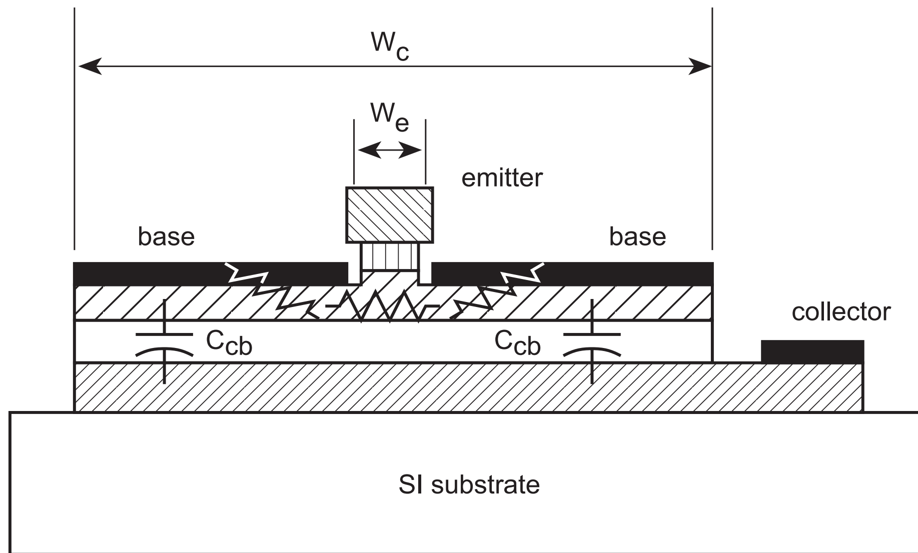
junction bipolar transistors (HBTs) enables the use of high base doping without degrading the emitter injection efficiency. This reduces the base resistance in HBTs compared to Si bipolar transistors, while maintaining high current gain (β). The material properties of InP-based semiconductors provide attractive features for high speed devices and ICs. High electron mobility and electron saturation velocity in the InGaAs base and InGaAs (or InP) collector layers respectively leads to low transit times and low access resistances. While AlGaAs/GaAs HBTs have a turn-on voltage of 1.4 V, the small bandgap of the InGaAs base sets the turn-on voltage in the InAlAs/InGaAs HBT at 0.7 V. The low turn-on voltage reduces the power consumption and allows smaller supply voltages.

Because of all the above advantages, HBTs in the InP material system are the devices of choice for high speed ICs [16], [17], [18]. There is however, one problem - while the bandwidth of HEMTs (0.1 μm HEMTS) and CMOS (0.18 μ m) transistors are improved by reducing their lithographic dimensions, the bandwidth of normal mesa HBTs does not improve significantly by scaling emitter dimensions below ~ 1 μ m. This scaling problem is solved by the transferred substrate process [19] - a process which modifies the HBT topology so that HBT bandwidth can be improved by reducing lithographic dimensions.

1.3 Transferred substrate HBT technology

Transistor performance is measured by two figures of merit, short circuit current gain (f_t) and maximum oscillation frequency (f_{max}). Fig. 2.1a shows the cross-section of a normal mesa HBT. For sufficiently narrow emitters R_b is independent of the emitter width; the base resistance is limited by the contact resistance between the base metal and the base epitaxial layer. C_{cb} is a function of the size of the mesa, which in turn is a function of the base metal width. Since the transfer length of the base ohmic contacts sets the minimum width of the base metal, C_{cb} is independent of emitter width. f_t is dependent mainly on the thickness and transport properties of the base and collector epitaxial layers. f_{max} is a function of f_t, R_b and C_{cb}. As all three parameters are independent of emitter width, f_{max} does not improve with reduced emitter dimensions.

To reduce extrinsic C_{cb} a number of techniques have been reported in the literature: buried SiO_2 under the base contact [20], selective lateral



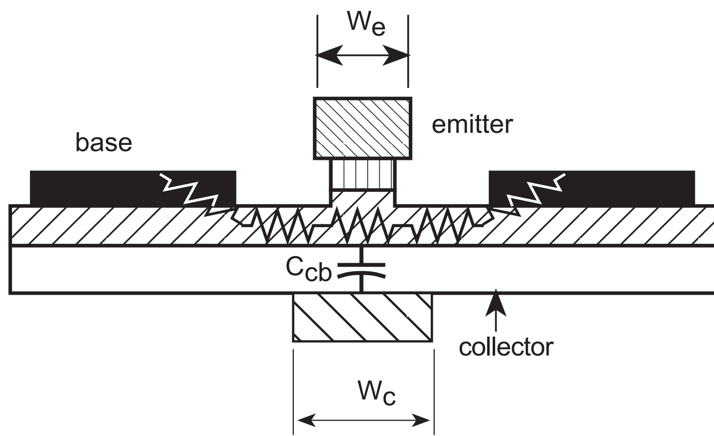


Figure 1.4: Cross-sections, a) Normal mesa HBT, b) transferred substrate HBT

oxidation of InAlAs emitter layers for collector-up HBT [21], isolation implant of the extrinsic base-collector [22] and regrowth of the HBT layers after definition of narrow subcollector region [23]. These techniques have achieved some reduction in the C_{cb} and small improvements in f_{max}. The scalability of these techniques however, has not been proved experimentally.

The transferred substrate process allows fabrication of narrow emitter and collector metal fingers on opposing sides of the epitaxial layers (fig. 2.1b). The N+ subcollector under the base contact is removed by etching using the collector metal as a mask. A simpler method is to avoid the N+ layer completely by defining a Schottky contact directly on the N-collector. C_{cb} in the transferred substrate HBT is defined by the dimensions of the collector contact metal. f_{max} improves if the reduction in emitter width is accompanied by a corresponding reduction in collector width. Deep submicron scaling of both the emitter and the collector contacts can be achieved by using projection lithography or E-beam lithography.

The transferred substrate technology renders the HBT scalable. Higher bandwidth devices required for ICs operating at high data rates can be fabricated by scaling the emitter and collector dimensions. Due to collector space charge effects (chapter-3) 1:2 ratio of emitter width to collector width seems to be the optimum for RF performance. Measured performance reveals that if the collector width is less than the emitter width, high collector current density effects reduce f_t and ultimately f_{max}. Initial work on transferred substrate HBTs with Schottky collector contacts has been reported and analyzed in [19]. Due to the device topology (chapter-2) and low thermal conductivity of the epoxy used for epitaxial transfer, the first generation transferred substrate technology, described in [24], is not suitable for ICs.

In this work the transferred substrate process has been improved. It is now an IC process in which HBTs with heat sinks, NiCr resistors and SiN MIM capacitors are fabricated. The heat sink permits high packing density of HBTs. The benzocyclobutene (BCB) dielectric enables a low loss, low parasitic capacitance and low ground return inductance microstrip wiring environment. This work achieves a big improvement in the existing transferred substrate HBT bandwidth - peak f_t of 150 GHz and f_{max} of 170 GHz was obtained in the old epoxy transferred substrate process [24]. InAlAs/InGaAs HBTs with f_{max} exceeding 400 GHz and f_t exceeding 220 GHz have been fabricated in this work [25]. This represents a big

improvement in state of the art for HBT bandwidths - the best RF performance in HBTs reported prior to this work is an f_t of 228 GHz and f_{max} of 227 GHz [16].

Some analog circuits have been demonstrated [26]. This thesis work is the first demonstration of digital ICs in the transferred substrate technology. Master slave D flip-flops connected as static 2:1 frequency dividers in the CML and ECL families have been designed and fabricated. Integration of about 50 components per IC has been achieved. When the stepper is available for photolithography, integration levels of about 1000 HBTs per IC will be possible with minor changes in the existing process.

Chapter 2

Process Development

The first generation of transferred substrate HBTs were fabricated by Dr. Uddalak Bhattacharya in a process which was suitable only for discrete devices [24]. The old process which uses epoxy to transfer the transistor epitaxial layers to the carrier substrate is unusable for integrated circuits due to the poor thermal conductivity of the epoxy fig. (2.1a). High current density operation in HBTs is required for maximum bandwidth. To operate several HBTs at high current density in a densely packed integrated circuit an efficient means of conducting heat away from the device is essential.

Heat generated in the HBT can be removed by providing a thermal via, filled with plated gold, either on the emitter metal contact or on the collector metal contact. The via provides a low thermal resistance path from the device to a back-side ground plane, which is considered to be at the ambient temperature. The transistor contacts are separated from the plated gold in the via by a thin layer of silicon nitride (SiN). A $4000-5000\AA$ SiN layer adds negligible thermal resistance to the heat flow path, but adds some parasitic capacitance. If the via is implemented on the collector side, C_{cb} increases as the collector-base junction (C_{cb}) will be surrounded by SiN instead of air. Given that the transferred substrate process aims at achieving high f_{max} by reducing C_{cb}, the extra capacitance from the thermal via cannot be tolerated. If the thermal via is implemented on the emitter side (fig. 2.1b), the effect of any parasitic capacitance will be swamped by the base-emitter capacitance (C_{be}), which is at least an order of magnitude larger than the via capacitance. No degradation in the RF performance is expected for the this structure.

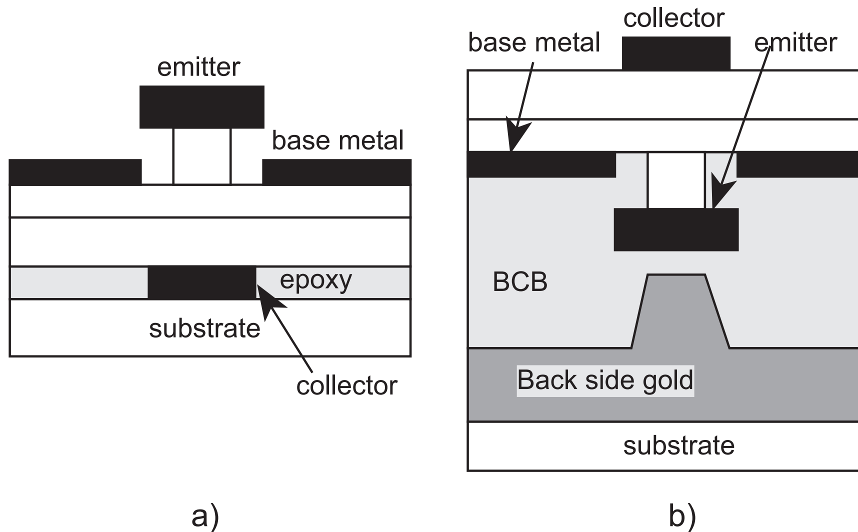


Figure 2.1: a) Old (epoxy process)) transferred substrate HBT suitable only for discrete HBTs, b) New transferred substrate HBT suitable for ICs

In the transferred substrate epoxy process, HBTs were fabricated with a final emitter up structure. To fabricate thermal vias on the emitter side, it is necessary to fabricate HBTs with their collector up, so that the emitter metal contact is accessible from the back side. In this thesis work, collector-up HBTs with thermal vias under their emitter metal contact are fabricated in an IC process which includes SiN MIM capacitors and NiCr resistors. The epoxy, used in the old process, to attach the transistor epitaxial layers to the carrier substrate is replaced by conductive In-Pb-Ag solder.

Each ECL static frequency divider consists of more than 50 components, including HBTs, NiCr resistors and SiN bypass capacitors. For such medium scale digital integrated circuits high component yield is necessary - achieving the required yield was the biggest challenge faced in this work.

The IC fabrication aspect of the work will be described in detail in this chapter. The discussion will include the various steps involved in the fabrication process, the problems encountered, and the solutions to these problems.

2.1 Transferred substrate IC process

The IC process is shown in table 2.1 and figs. 2.2, 2.3. Initial process steps which involve emitter metal evaporation, base mesa etch and metalization, mesa isolation, polyimide planarization, metal-1, SiN dielectric deposition and etch and metal-2 layers are similar to a normal mesa HBT process. This is followed by the transferred substrate process steps - BCB deposition and etch, plated back- side gold, In-Pb-Ag solder bonding to GaAs carrier, InP growth substrate removal, collector metal and collector recess etch. Major process steps are explained in detail in the later sections. In-Pb-Ag solder (instead of epoxy in the old process) is used due to its higher thermal conductivity, high bond strength and good surface wetting properties. Fig. 2.3b shows the cross-section of the IC after the process. The HBTs, NiCr resistors, SiN capacitors and 3 layers of metal are fabricated in a 10 mask layer process. The HBT connections to the base, emitter and collector contacts can be seen in fig. 2.12a. 2 layers of evaporated metal are used to wire the various circuit components while the thick back-side plated metal serves as a microstrip ground plane for the other two metal layers. Heat generated in the HBT is conducted away through the plated gold in the via to the back-side ground plane. The thick gold in the ground plane spreads the heat laterally, reducing the thermal resistance for heat flow through the substrate.

5 μm of BenzoCycloButene (BCB) serves as the dielectric between the metal wires and the microstrip ground plane. BCB has a low dielectric constant ($\epsilon_r = 2.7$) and low loss. Ground connections to the wiring on BCB are made by etching vias and filling them with plated gold. Given that the BCB is only 5 μm thick, the vias have very low inductance. The combination of the microstrip wiring on a low loss, low ϵ_r dielectric with low inductance ground vias gives rise to a predictable and low parasitic wiring environment on the IC.

2.2 Emitter mesa etch

The emitter mesa is defined by a combination of dry and wet etches. Ti/Pt/Au/Si is lifted off during the definition of the emitter contact. Si acts as the mask protecting the emitter metal during the dry etch. A combination of $CH_4/H_2/Ar$ gases is used for dry etching through the InGaAs

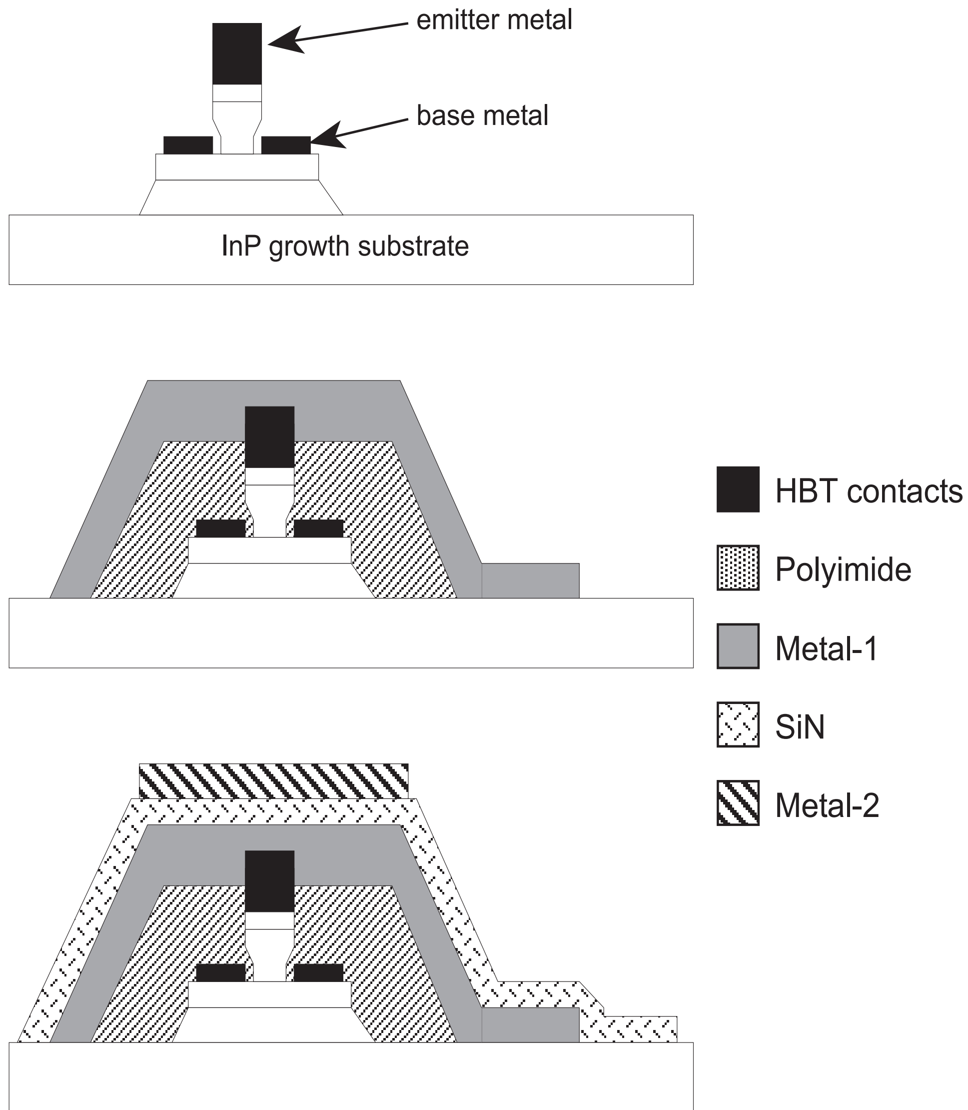


Figure 2.2: Transferred substrate process cross-section upto process step 10

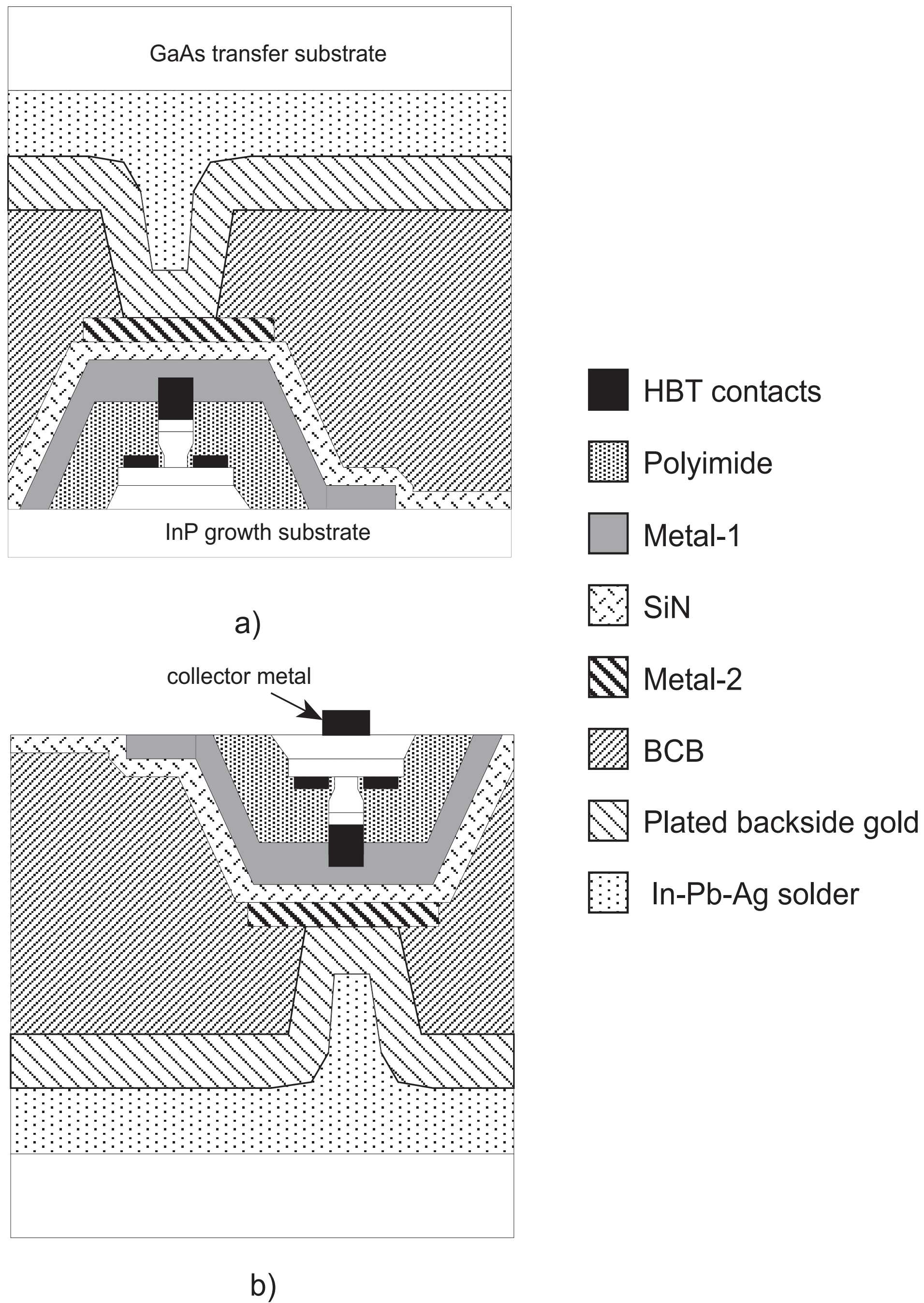
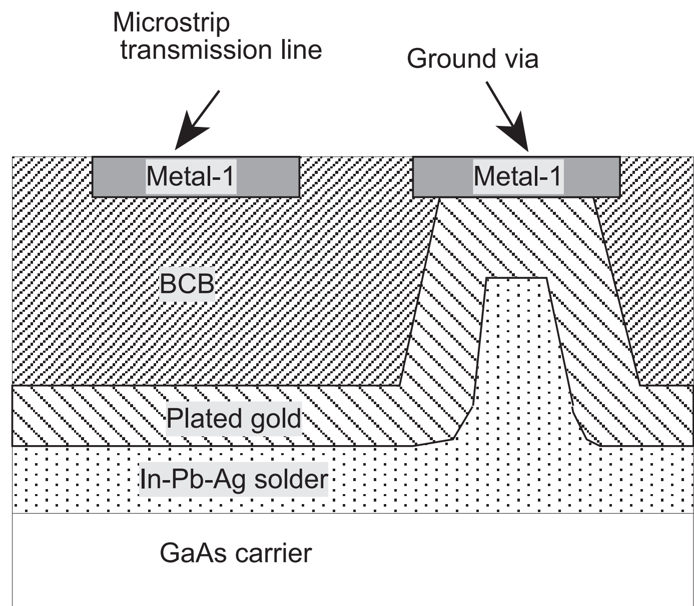
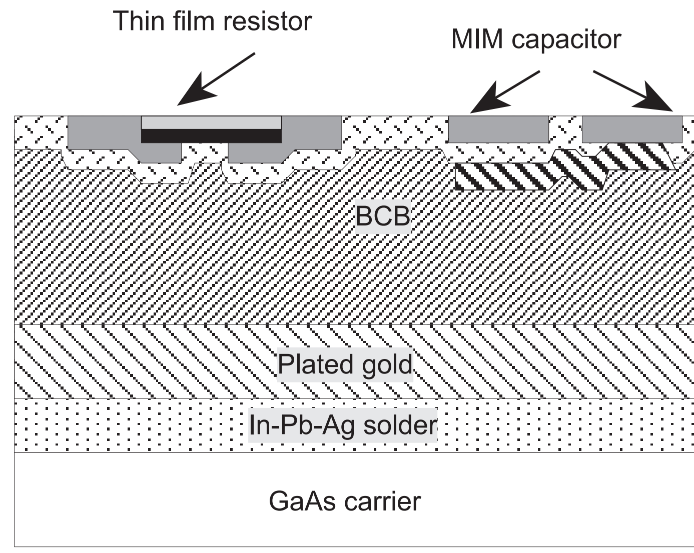


Figure 2.3: Wafer cross-section upto a) process step 14, b) process step 16 (final)



a)



b)

Figure 2.4: a) Microstrip wiring on the IC, b) NiCr resistors and SiN capacitors.

Step number	Process details	Step number	Process details
1	Emitter metal*	9	SiN* PECVD and etch
2	Base etch	10	Metal-2*
3	Base Metal* deposition and sinter	11	BCB spin cure
4	Isolation etch*	12	Via etch*
5	Polyimide deposition and RIE	13	Thick plated gold
6	Polyimide plasma etch*	14	Bonding and substrate etch
7	NiCr resistors*	15	Collector metal*
8	Metal-1*	16	Recess etch

Table 2.1: Major process steps, * indicates steps involving lithography.

cap layer and partially into the InAlAs emitter. The intensity of a laser beam reflected from the etched surface is used to monitor the etch depth. The trace is an unique signature dependent on the layer structure of the material. Hence, it is an accurate tool to decide the end-point of the dry etching process. The end-point is reproducible from run to run. After the completion of dry etching, the remaining Si on the emitter contact is removed by a short CF_4 plasma etch.

The base current in the HBT is dominated by leakage current from the emitter to the base Ohmic contacts, through surface states in the etched InGaAs surface. It might therefore be necessary to space the base contact away from the emitter mesa edge by a short distance. If this distance is large then base resistance increases through the introduction of a gap resistance.

A selective wet etch is next performed. The ‘A+B’ etch (chemistry given in appendix)removes InAlAs with a high selectivity compared to InGaAs. This is a timed etch used to define the amount of lateral undercut. As this etch is selective on the basis of Al versus Ga content of the material, it stops at a point in the graded emitter-base junction where the Ga content is large enough. The vertical distance etched is small compared to the desired undercut. Over-etching therefore occurs in the vertical direction. This has

the beneficial effect of making the surface uniform by removing any non-uniformity left behind by the dry etch. An uniform surface close to the base is thus exposed. A short, timed, and non-selective etch is used next to reach the base.

The combination of dry and wet etches used to define the emitter mesa has several benefits. The wet etch that follows the dry etch removes damage in the semiconductor due to the dry etch process. The selective wet etch stops accurately on the base layer with a controlled undercut in the lateral direction (fig. 2.5).

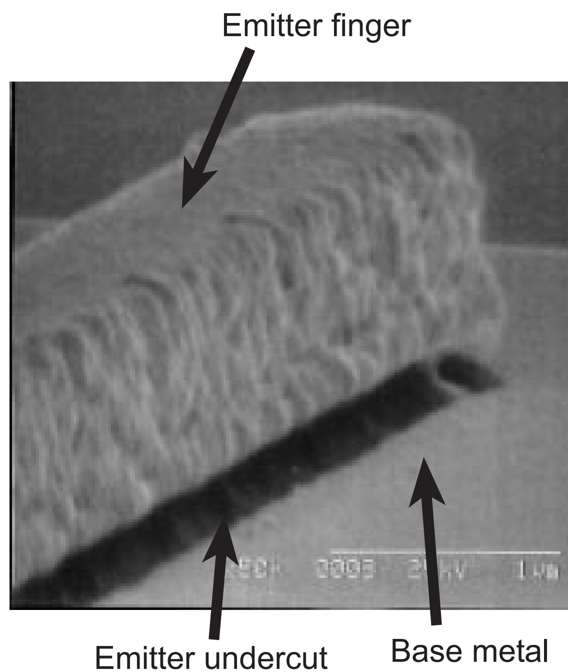


Figure 2.5: Photomicrograph of base-emitter after base etch.

Emitter mesa etch is followed by base contact Ti/Pt/Au/Ti metalization and sintering. The Ti layer on top serves as a sticking layer and improves adhesion between the base metal and the polyimide which is spun on in a subsequent process step.Transmission line measurement (TLM)structures on the base are used to evaluate the quality of the base ohmics. Excellent ohmic contacts with specific contact resistivity, $r_c = 5 \times 10^{-7} \Omega\text{cm}^2$, are obtained. The TLMs also indicate that $\simeq 100$ $\mathring{A}$ of base epitaxial layer is

etched before depositing the ohmic contact metal.

The devices are then isolated by in a Cl_2 dry etch process which removes the collector layers and approximately half the InAlAs buffer layer.

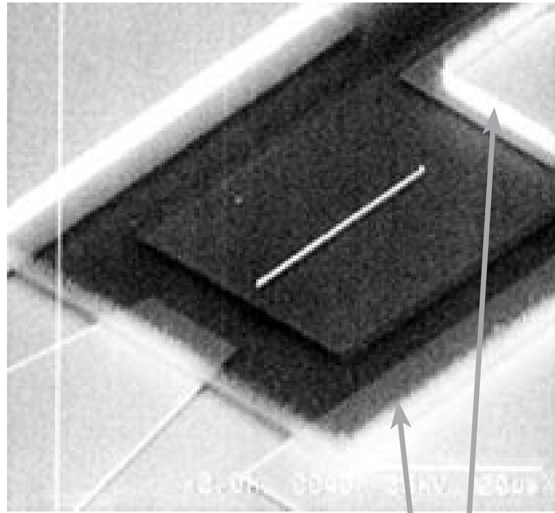
2.3 Polyimide process

Polyimide is used to passivate the base-emitter junction (prevents base-emitter leakage current). HBT emitters are surrounded by the base mesa on all sides. Polyimide is coated and then etched so that the emitter finger is exposed, while the base metal is covered with polyimide. Metal-1, which is used to connect the emitter to other circuit elements, flows over the polyimide preventing a base-emitter short. Two significant problems were observed with the old polyimide process used in the old process [24].

2.3.1 Step coverage of metal over polyimide step

After mesa isolation, the polyimide process starts with spinning a 1.8 μm polyimide layer. To planarize the surface a 3 μm layer of photoresist (AZ-4330) is spun on the wafer. This resist is patterned. The patterned photoresist and blanket polyimide combination is etched in oxygen RIE until the top of the emitter metal finger is exposed. RIE is necessary to get precise etch control, uniformity and smooth etch surface. The process however, leaves a very steep and ragged edge with thin hair-like structures around the edge of the mesa (fig. 2.6a).

The polyimide dry etch process is followed by metal-1 deposition. HBT emitters are connected to various circuit components in this metal layer. The metal, deposited by sputtering (followed by plating) or E-beam evaporation is expected to flow from the exposed emitter finger on top of the polyimide layer, down the polyimide step on to the substrate. As E-beam evaporation is a directional process, the evaporated metal breaks at the polyimide step. HBTs with open emitters are obtained. A continuous sputtered flash (metal) layer is required for electro-plating. Though metal deposited in the sputtering machine covers vertical edges, the hair-like structures and the ragged edge on the polyimide make step coverage difficult. For good step coverage, it is necessary to sputter the metal layers at pressures exceeding 50 mT. Given the limitations of the sputtering machine in our



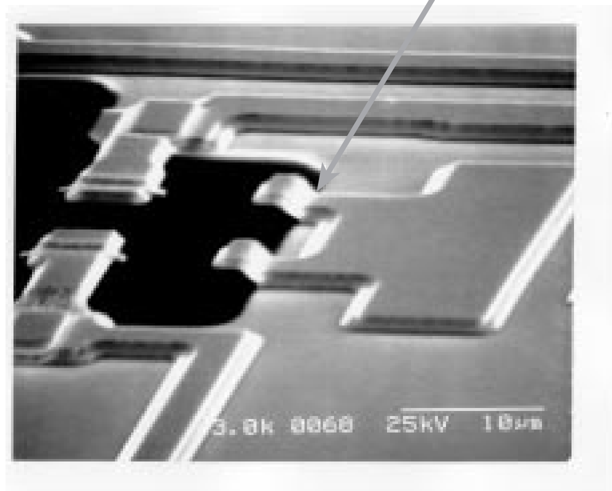


Figure 2.6: a) Old polyimide etch profile, b) New polyimide etch profile (after metal-1 evaporation)

clean room, it is not possible to obtain good quality metal layers (especially Titanium) at such high pressures.

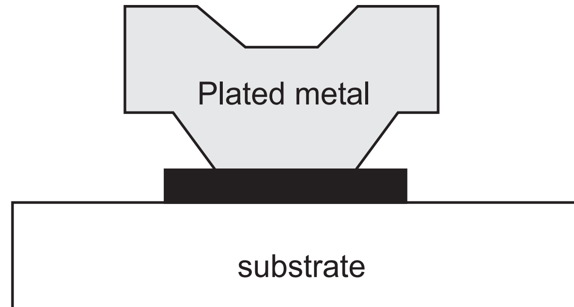


Figure 2.7: ‘T’ structure of plated metal.

A combination of O_2 RIE etch and O_2 plasma (non directional) etch is developed to solve the above problem. Unlike the old process, $AZ - 4330$ spun on the polyimide is not patterned before the RIE etch. The wafer with blanket photoresist and blanket polyimide is etched until the emitter metal is exposed. At this point the entire wafer is covered by a layer of polyimide with the emitter fingers sticking out. Another layer of AZ-4330 is spun on the wafer and patterned. This time the polyimide is removed by plasma etching at relatively high pressure with photoresist as mask. As O_2 plasma also etches the photoresist mask at the same rate as the polyimide, the photoresist mask should be sufficiently thick to protect the polyimide in the masked areas. The combined effect of the soft mask and the non-directional plasma etch gives rise to a gradual (sloping) step in the polyimide (fig.2.6b). Plated or evaporated metal can flow over the edge easily.

2.3.2 Cracks on mesas and open base-emitter junctions

Another problem is noticed towards the end of the fabrication process, after the wafer with its epitaxial, metal and dielectric layers is flipped onto a carrier substrate and the InP growth substrate etched away. Stress, caused by the difference in thermal expansion coefficients of the underlying layers, causes cracks in the semiconductor mesas on top of the emitter. The emitter, which is under the mesa can be seen through these cracks. In often

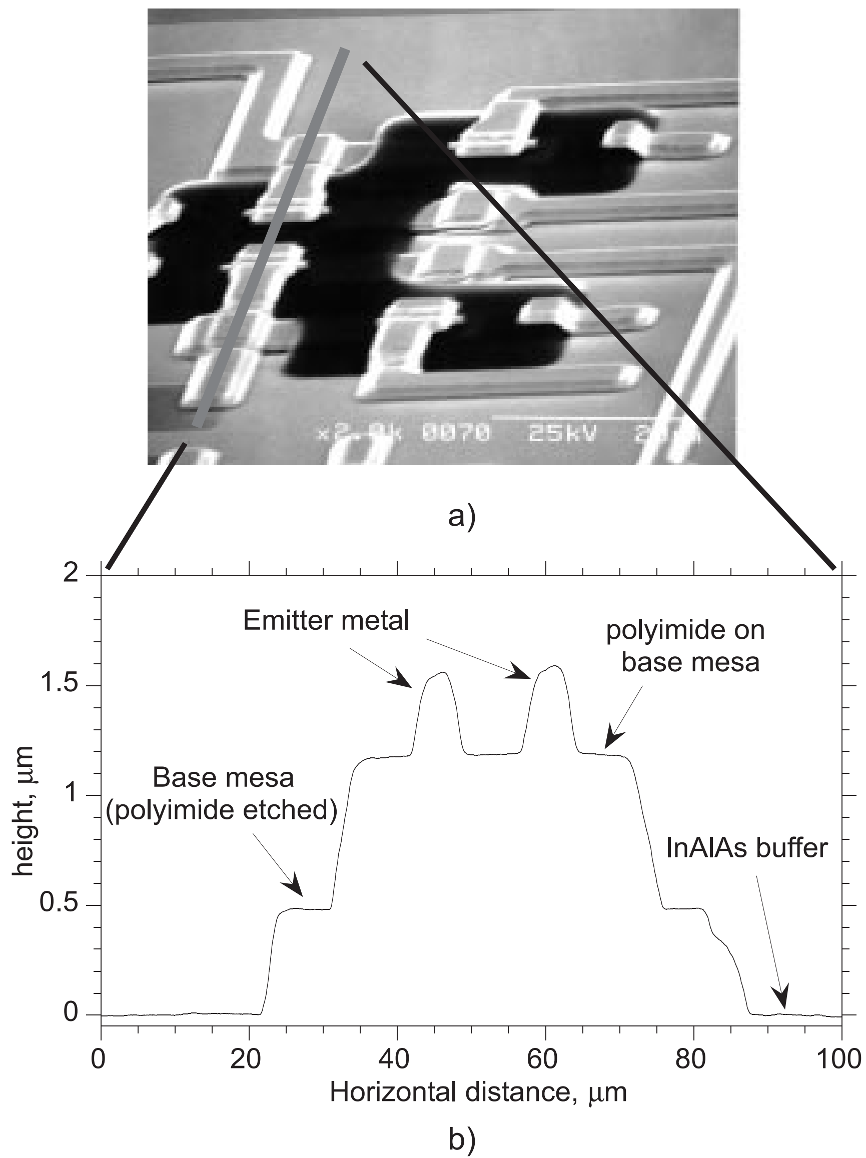


Figure 2.8: Surface profilometer (dektak) measurement after polyimide etch, a) Photograph showing profilometer path, b) Plot of polyimide thickness along the path shown in (a).

cases, no visible damage was seen, but an electrically open base-emitter junction was obtained. After collector lithography the problem worsened and in some runs almost all the base emitter junctions were open.

After numerous experiments and failed process runs with combinations of plated metal, evaporated metal, various thicknesses of BCB, different solders and finally substitutes for the polyimide, the open base-emitter junctions were attributed to problems in the polyimide process. It is suspected that the polyimide does not fill the narrow gap in the emitter undercut as it preferentially wets the base metal rather than the semiconductor. When the polyimide is cured, a void is created. Under stress the semiconductor buckles into the void, creating cracks in the mesas.

SF-11 is a dielectric which has lower viscosity and stress compared to polyimide. When SF-11 is used for planarization instead of polyimide, much higher device yield is obtained. DC current gain is only 15 as SF11 does not passivate the base-emitter junctions. The low β is not sufficient for designing circuits.

The problem was finally solved by using a less viscous polyimide from a different vendor. The new polyimide and the cure process was suggested by Roger Malik of Ovation semiconductors. The new polyimide improved the yield considerably. This was a vital step in improving yield so that we could transition from fabricating 2-3 HBT circuits to $50-100$ HBT circuits.

2.4 Resistors, metal layers and MIM capacitors

2.4.1 NiCr Resistors

Nickel Chromium (NiCr) resistors are evaporated prior to Metal-1 deposition, either before or after the polyimide process. Sheet resistance of $50\ \Omega/\Box$ is obtained for a 450 $\AA$ thick NiCr layer. Thinner NiCr can be used for higher sheet resistance. For NiCr layers smaller than 300 $\AA$, the variation of sheet resistance with thickness is too large to obtain reproducible resistor values. It is therefore recommended that the sheet resistance be chosen so that NiCr thickness exceeds $300\AA$.

A 200 $\AA$ silicon (Si) layer evaporated before the NiCr layer serves two purposes. Towards the end of the process, after the substrate removal etch,

the backside of the NiCr/Si layer is exposed to the collector recess etch. The silicon layer protects the resistors during the Methane-Hydrogen-Argon dry etch (if dry etch is used). The Si also acts as dielectric encapsulant preventing NiCr exposure to the atmosphere.

2.4.2 Angle evaporated metal process

Step coverage of metal flowing down the mesa edge and polyimide edge is an issue. The old device process uses electro-plated metal to connect the base contact and emitter contact metal of the HBT to the wires running on the semi- insulating substrate (fig. 2.6b). A sputtered flash layer combined with electro-plating provides adequate step coverage. However, the plated metal layer cannot be used in the current IC process due to step coverage problem of subsequent metal layers deposited on the plated metal layer.

Electro-plated metal is defined by a combination of two mask layers, the post and the airbridge. The electro-plating process and subsequent etching of the flash layer constrains the post mask to be at least 2 μm smaller than the airbridge mask layer. This gives rise to a 'T' shaped metal structure (fig. 2.7).

Metal-2, deposited after metal -1 deposition, is used as a wiring plane and also as an etch stop layer in the BCB via etch process for non-grounded emitters. In the IC layout there are several places where metal-2 crosses metal-1 with SiN as the inter layer dielectric. At these cross-overs the 'T' structure of metal-1 poses problems of step coverage, both for evaporated metal and electro-plated metal. While sputtering will cover near vertical edges, it is observed that the sputtered flash layer does not deposit in the undercut. This gives a break in the flash layer and consequently no metal will be deposited on top of the 'T'.

Due to these problems, an alternate process was developed for the two metal layers. Image reversal of EIR-5214 with a dark field mask gives a resist profile with large under-cut. Metal-1 is defined in a single EIR-5214 step with E-beam evaporation at an angle, so that the polyimide and mesa steps are covered. Rotation of the wafer during evaporation ensures that there is no directional dependence for step coverage. The good undercut profile in the photoresist ensures metal lift-off. The metal thus deposited has a sloping side-wall, convenient for cross-overs (fig. 2.9). Metal-2 is also deposited in an identical fashion.

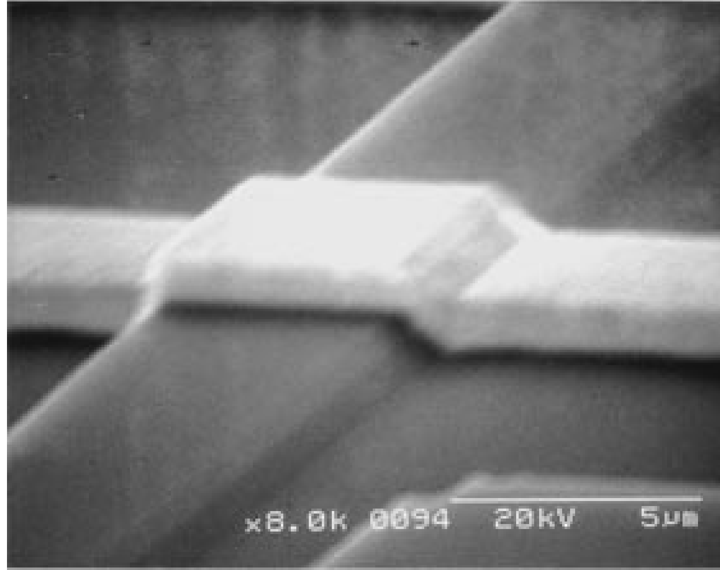


Figure 2.9: Metal-2 and metal-1 crossover.

The above angle evaporation process has another very significant advantage. Packing density is increased due to much tighter design rules compared to previous electro-plated metal design rules. For the combination of two mask layers - post and airbridge, and the alignment tolerance between the two, the minimum width of electro-plated metal-1 is 7 μm, with 5 μm spacing between two metal-1 lines. For the angle evaporated metal process, a minimum width and spacing of 3 μm and 4 μm respectively can be easily realized. Smaller linewidths can be realized using the stepper for lithography. This might be more necessary to increase the packing density than reducing the wiring capacitance.

2.4.3 SiN and metal-2 process steps

After Metal-1 deposition, 4000 $\mathring{A}$ of SiN is deposited. SiN serves as the dielectric for cross-overs between metal-1 and metal-2. For metal-1 to metal-2 via connections, the SiN is etched using a $SF_6/O_2/Ar$ dry etch. This is followed by the deposition of metal-2, using the angle evaporation process discussed above.

The combination of metal-1/SiN/metal-2 gives MIM capacitors. Both

grounded and non-grounded capacitors are obtained. Also, Metal-2 deposited on top of SiN on the HBT emitter acts as etch stop layer during the BCB etch, protecting the SiN. The electro-plated metal for the back side ground plane contacts metal-2, instead of metal-1. HBTs with non-grounded emitters are obtained.

2.5 Transfer substrate process steps

While the process steps discussed above are similar to that those in a normal double-mesa HBT process, the steps discussed in this section are unique to the transferred substrate process.

2.5.1 Benzocyclobutene (BCB) process

BCB is used as the dielectric layer between the backside ground plane and the microstrip wires because of its excellent microwave properties and low dielectric constant. Thick BCB layers can be deposited with low-stress and low cure temperature cycles. Depending on the impedance required for the transmission lines in the integrated circuit, the thickness of the BCB can be varied. In digital circuits, if the wire to wire spacing on the IC is less than the BCB thickness, the wiring capacitance is mainly due to coupling capacitance between the wires rather than between the wire and the back side ground plane. Given that wires on the digital IC are closer than 4 μm, BCB thickness of 5 μm is adequate.

In any semiconductor process it is difficult to fabricate metal or dielectric structures with large aspect ratios (vertical to lateral dimensions). BCB dielectric layer is the thickest layer in the transferred-substrate process. The size of a single HBT in a digital circuit is limited by the BCB via dimensions and the associated metal-2 etch stop layer dimensions. If thinner BCB is used, smaller size vias can be defined. Also, the tolerance between the via and the metal-2 etch stop layer can be reduced. Packing density of HBTs can be increased, reducing chip area and wiring capacitance. For these reasons the smallest BCB thickness which does not degrade circuit performance should be used. BCB thickness of 5 μm is used in the digital ICs. For analog circuits with transmission line matching circuits, thicker BCB should be used to obtain the desired impedance on the transmission lines.

The BCB vias are defined in a dry etch process. To deposit the flash layer (sputtered metal layer) required for electro-plating gold in the BCB vias, the via should have sloping side-walls. Sloping side-walls are obtained by selecting the RIE etch parameters for a non-isotropic etch and by using a soft mask to protect the BCB during the etch.

Adhesion of sputtered flash layer to the BCB surface is enhanced by etching the top surface of the BCB ($\simeq 1\ \mu$m) before flash metal deposition. A BCB etch process incorporating the requirements of dry processing and surface roughening after via etch has been developed. 5500 $\AA$ of photoresist (multiple layers) is patterned and hard baked on 6 μm of BCB cured in an O_2 free atmosphere. SF_6/O_2 etches photoresist and BCB with a 1:1 ratio. In a single dry etch, the via pattern is transferred from the photoresist to the BCB, the photoresist mask completely removed and $\simeq 1\ \mu$m of BCB under the resist mask etched.

After the via etch, Ti/Au flash layer is sputtered on the BCB. 1000 $\AA$ of SiN is then deposited on the back side of the wafer. The SiN layer prevents plated gold from encroaching onto the back side of the InP substrate and causing problems with the substrate removal etch. Thick gold (about 10 μm) is then plated. The plated gold serves as a heat sink and as a back side ground plane for the micro-strip wires on the IC.

2.5.2 Wafer bonding and substrate removal Etch

The wafer bonding and substrate removal process is unique to the transferred substrate process. It is required as it permits the definition of a collector contact on the back side of the epi layers. The wafer bonding step involves transferring the processed layers from the InP growth substrate to a GaAs carrier wafer. To enhance adhesion and wettability of solder, the GaAs transfer substrate is first coated with a thin layer of sputtered gold. After Au plating on the BCB, the InP epi wafer and the GaAs transfer substrate are bonded together at 180° C and 1000 gms of pressure using Indium-lead-silver solder. In-Pb-Ag solder has good thermal conductivity. It is soft and easily wets metal surfaces. After bonding, the wafers are cooled down slowly to room temperature. SiN on the back side of the InP growth substrate is etched in buffered HF solution. The InP substrate is removed in an aqueous solution of HCl. As HCL selectively etches InP and InAlAs (buffer layer) over InGaAs (collector) with a very high selectivity

ratio, the etch stops on the InGaAs collector layer.

The solder used here has a thermal conductivity similar to GaAs. Though this is far better than the epoxy used in the old process, the thermal resistance of thick solder and GaAs carrier substrate can limit performance of dense integrated circuits. The solder and the carrier substrate can be eliminated altogether if the backside metal layer (ground plane) is thick enough to mechanically support the wafer. A transferred substrate copper process which replaces the solder and the carrier substrate with $\sim 200\ \mu$m of plated copper is currently under development [27].

2.5.3 Collector metal and recess etch

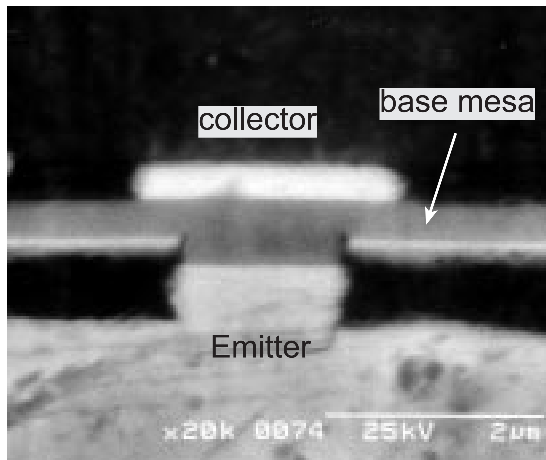


Figure 2.10: Cross-section of transferred substrate HBT (credit: James Guthrie).

After substrate removal, Ti/Pt/Au collector metal is deposited The collectors are then recess etched to reduce the collector-base capacitance (fig. 2.3b). Both dry and wet etching techniques have been used for this purpose. Collector width decreases due to undercut from the wet etch, improving f_{max} considerably. For epitaxial layers with N+ sub-collectors the recess etch should remove the N+ subcollector layer completely - otherwise the entire mesa area contibutes to C_{cb}.

Optical contact lithography limits alignment tolerance to 2 μm. Collector-emitter alignment is critical. HBTs with misaligned collectors have poor

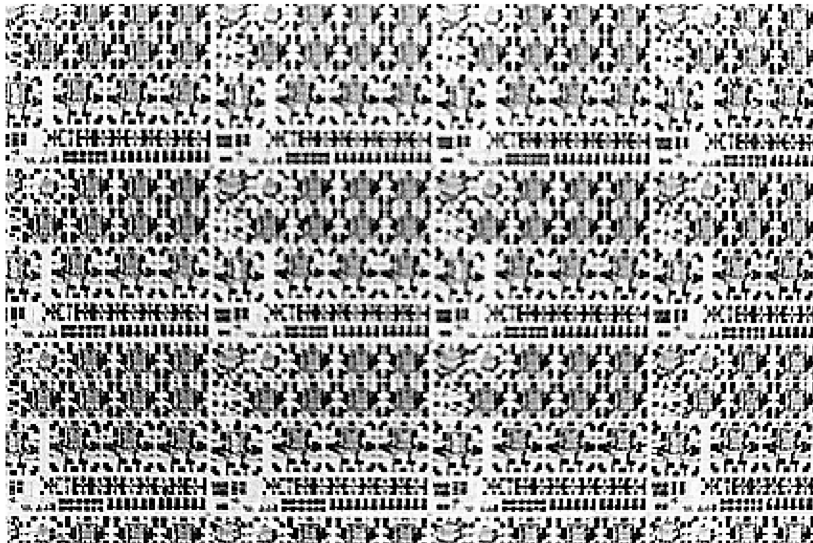
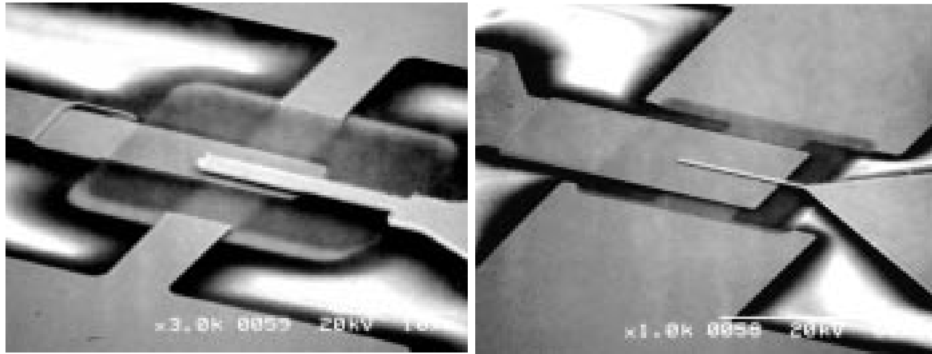


Figure 2.11: Photograph of transferred substrate IC wafer, area : $1.2cm \times 0.9cm$.

DC and RF characteristics. In every cell, a stagerred alignment of collector to emitter is used - collectors are misaligned (on the mask) from the emitter in steps of 0.5 μm on either side. After fabrication, atleast one HBT in each cell has emitter and collector aligned to each other. This staggering alignment limits yield to less than 15 %. Better alignment tolerance and much higher yields can be obtained if the stepper is used for photolithography.

A detailed process flow has been included in the appendix. Some photographs of devices and circuits fabricated in this process are shown in fig. 2.12.



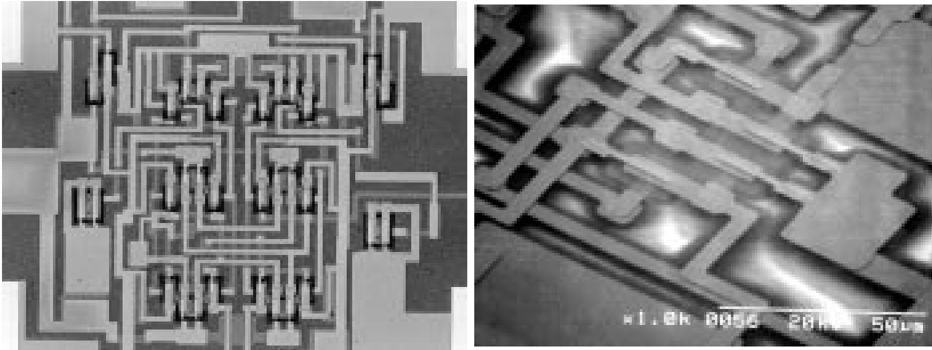


Figure 2.12: After the IC process, a) Small mesa HBT with evaporated metal design rules, b) Big mesa HBT with plated metal design rules for comparison c) Close-up of static frequency divider, d) A set of 4 HBTs in the ECL static frequency divider.

Chapter 3

Device Design and Characterization

This chapter deals with the design and characterization of HBTs. HBTs fabricated as part of this thesis work, for use in emitter coupled logic (ECL) and current mode logic (CML) digital circuits are discussed here. Device bandwidth is measured by the two figures of merit - f_t and f_{max}. In the transferred substrate process, high f_{max} HBTs are obtained by definition of narrow collector fingers. High f_t is obtained by scaling of the epitaxial layers and changes in the existing device layout to the reduce extrinsic base-emitter capacitance. In contrast with small signal analog circuits, which operate at a fixed bias point, performance over the entire voltage swing effects switching speed of the digital gate. The variation of device RF characteristics with bias and the design of the epitaxial layers for optimum RF performance over the voltage swing of the logic family is discussed here.

Small signal hybrid-*pi* models and spice models are developed for the HBTs, resistors and capacitors incorporating various parasitic elements. Limitations of these models and their accuracy is examined.

3.1 Characterization of HBTs

Both DC and RF measurements were carried out on the transferred substrate HBTs. The common emitter characteristics and the Gummel plots have been obtained using a semiconductor parameter analyzer. The scattering parameters (S-parameters) are measured on a 0-50 GHz network

analyzer. f_t, f_{max}, and other frequency dependent parameters are calculated from the S-parameters. The results of these measurements and their implications will be discussed in this chapter.

DC characterization includes contact and sheet resistivity measurements of the HBT base ohmics and the NiCr resistors. Transmission line measurements (TLMs) for this purpose are discussed below.

3.1.1 Transmission line measurements

Two kinds of TLM patterns are used, pinched TLMs and non-pinched TLMs (fig. 3.1). Base-sheet resistance and base contact resistance are calculated from the TLM data. The p-base layer between the base ohmics of the pinched TLMs is protected by the emitter metal during the base-etch. Therefore, the measured sheet resistance in these TLMs depends on the as-grown base thickness and doping. In the non-pinched TLMs, we measure the sheet resistance of the etched base layer. Comparison of pinched versus non-pinched TLM sheet resistance gives an estimate of the amount of base epitaxial material that has been etched in the base-etch process. In principle, comparison of pinched and non-pinched contact resistance can be used to determine the undercut in the emitter finger. In practice however, the precise width of the emitter is not known - the under-cut determined from the TLMs is not reliable.

The TLMs on the base ohmics for one of the IC runs, in which ECL circuits were fabricated, is plotted in fig. 3.2. Peak f_t and f_{max} of HBTs on this wafer are 220 GHz and 470 GHz respectively. The sheet resistance of the as-grown 400 $\mathring{A}$ base layer measured from the pinched TLMs is 595 $\Omega/\Box$, while the sheet resistance of the etched base layer measured from the non-pinched TLMs is 821 $\Omega/\Box$. The specific contact resistivity (r_c), which is a measure of the quality of the base ohmics, is $\sim 5.5 \times 10^{-7}$ Ωcm^2. The base layer thickness after the base etch, calculated from the ratio of the pinched to non- pinched TLM sheet resistance, is ~ 360 $\mathring{A}$. From this data we conclude that approximately 140 $\mathring{A}$ of the base epitaxial layer has been etched before putting down the base contact metal.

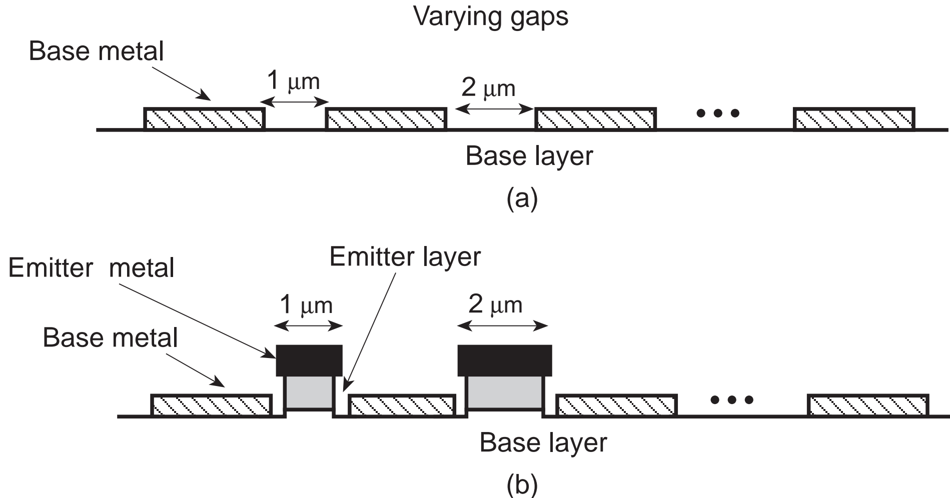


Figure 3.1: Cross section of base ohmic TLM structures, a) Non-pinched TLMs, b) Pinched TLMs.

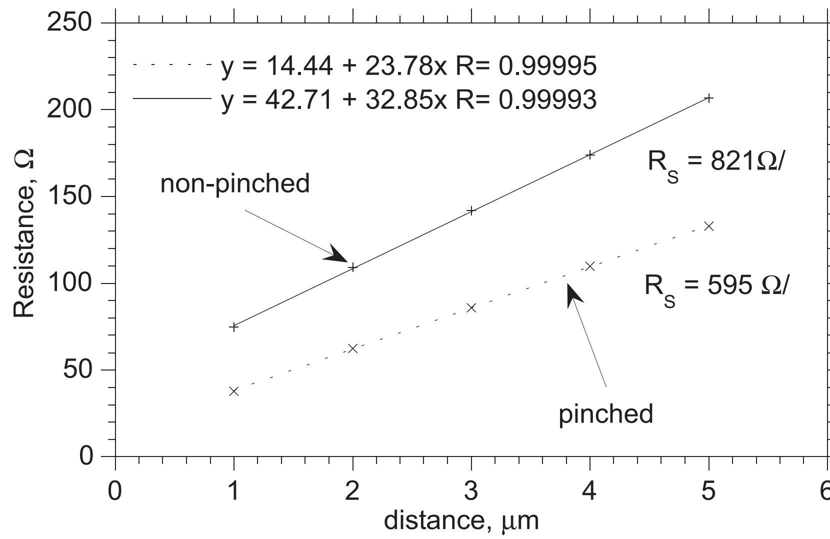
3.2 Baseline transferred substrate HBT

In this section we discuss the design and results of the 'baseline' transferred substrate HBT. This is the first transferred substrate HBT for which an f_{max} greater than 400 GHz was obtained. All subsequent device designs are modifications of the epitaxial layers and layout of this device. The HBTs which are used in CML and ECL circuits will be discussed in the next section.

3.2.1 Baseline HBT epitaxial layer design

Fig. 3.3 shows the epitaxial layer structure of the baseline device. Device physics and tradeoffs involved in the epitaxial design of previous transferred substrate AlInAs/InGaAs HBTs have been discussed in [24]. The epitaxial layer structure of the baseline HBT, designed by Dino Mensa, incorporates two significant improvements.

kT bandgap grading across the base epitaxial layer generates a base electric field which adds onto the existing diffusion gradient to speed up the electrons in the base [28]. f_t is increased due to reduced base transit time.



a)

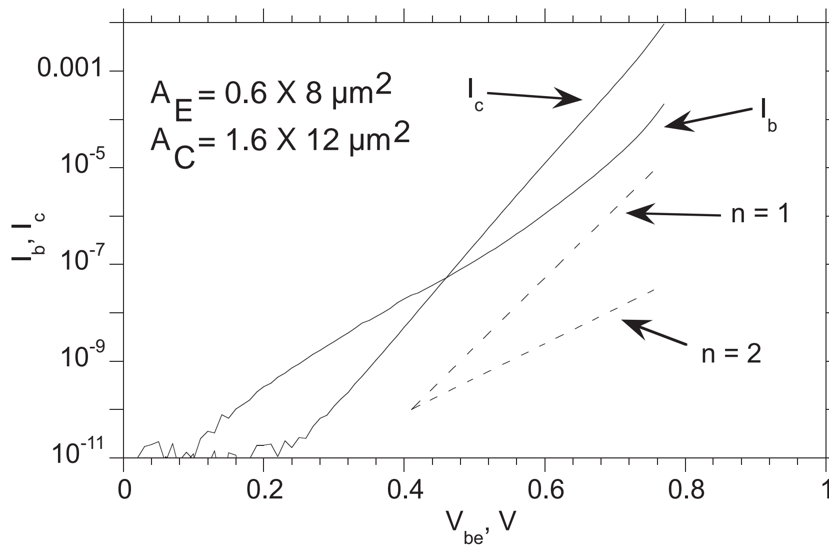


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Figure 3.2: a)TLM measurements of base ohmics on an IC run, b)Gummel plot of HBTs on the process run.

Layer	Region
GaInAs 1000 Å $1 \bullet 10^{19}$ Si	emitter
Grade 66 Å	
AlInAs 834 Å $1 \bullet 10^{19}$ Si	
AlInAs 500 Å $8 \bullet 10^{17}$ Si	
Grade 300 Å	
GaInAs 400 Å $5 \bullet 10^{19}$ Be	base
GaInAs 100 Å $3 \bullet 10^{19}$ Be	
GaInAs 400 Å $2 \bullet 10^{16}$ Si	collector
GaInAs 50 Å $1 \bullet 10^{18}$ Si	
GaInAs 2250 Å $1 \bullet 10^{16}$ Si	
AlInAs 2500 Å	buffer
S. I. InP	

Figure 3.3: Epitaxial layer structure of baseline HBT.

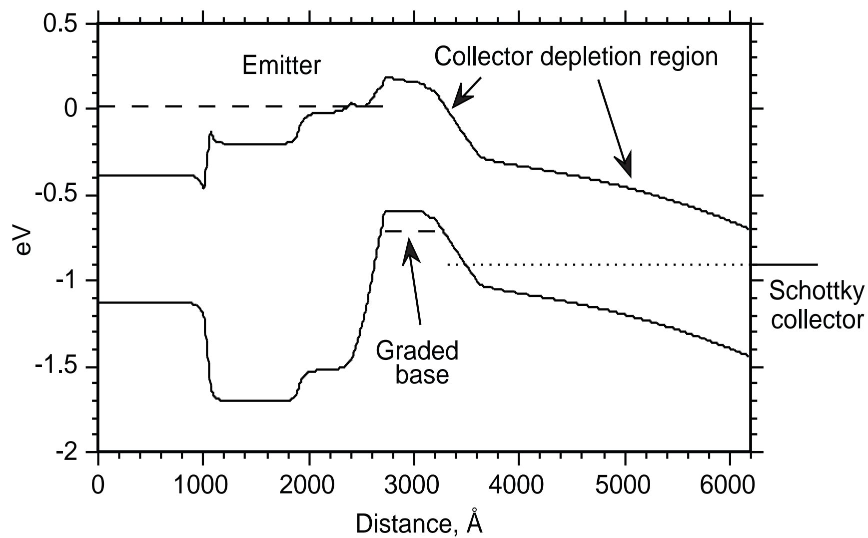


Figure 3.4: Band diagram of baseline HBT.

$$f_t = \frac{1}{2\pi\left(\frac{kT}{qI_c}(C_{je}+C_{bc})+r_{ex}C_{bc}+\tau_f\right)}$$

where τ_f is the forward transit time, I_c is the collector current, C_{je} is the base-emitter capacitance, C_{bc} the base collector capacitance, r_{ex} is the extrinsic emitter resistance.

The effect of C_{je} and C_{cb} on f_t is reduced by operating the transistor at high current density; peak f_t is limited only by τ_f and $R_{ex}C_{bc}$. As the collector current density increases, a different effect which reduces f_t with increasing current density takes over. At high collector current density, the field associated with the electron flux in the collector swamps the built-in and applied fields, causing an electrostatic shielding effect on the electrons leaving the base. The electric field in the collector, at the base edge, goes to zero. The result is an increase in base width of the transistor (Kirk effect). For large collector currents, the base transit time and collector-base capacitance increase, causing f_t and f_{max} to drop. A pulse doped layer placed 400 $\mathring{A}$ from the base edge in the collector depletion region delays the onset of kirk effect by increasing the electric field in the depletion region close to the base edge [29]. Higher f_t can then be obtained by operating the transistor at higher current density without base push-out.

The band diagram corresponding to the layer structure of fig. 3.3 is shown in fig. 3.4. Biasing conditions are as follows, $V_{be} = 0.7$ V, $V_{ce}= 0.9$ V. The slope of the conduction band in the base is equal to the quasi-electric field in the region. As electrons leave the base and enter the collector they are accelerated to the saturation velocity- the velocity with which they transit through the collector depletion region and exit through the Schottky collector contact. The Schottky barrier for Ti/Pt/Au metalization on InGaAs is 0.2 V.

3.2.2 DC common emitter characteristics

DC common emitter characteristics of HBTs with collector widths of 1 μ m and 2 μm are shown in fig. 3.5a and fig. 3.5b respectively. The 1 μm collector device shown here is picked from a set of 9 devices in one cell, where the collectors in each device are displaced from the emitters in steps of 0.5 μm, to a maximum of 2 μm on either side. Manual alignment during

contact lithography and wafer shrinkage due to the transferred substrate process limit the alignment precision to 2 μm. As a result, only one of the devices in each cell has its collector aligned to the emitter. Other HBTs in the cell have misaligned collectors, resulting in poor DC and RF characteristics. The effect of misalignment between the emitter and collector has been discussed in [26]. Collector-emitter alignment is less critical in the 2 μm collector devices due to the wider collectors. About two 2 μm collector devices in each cell exhibit good DC and RF performance.

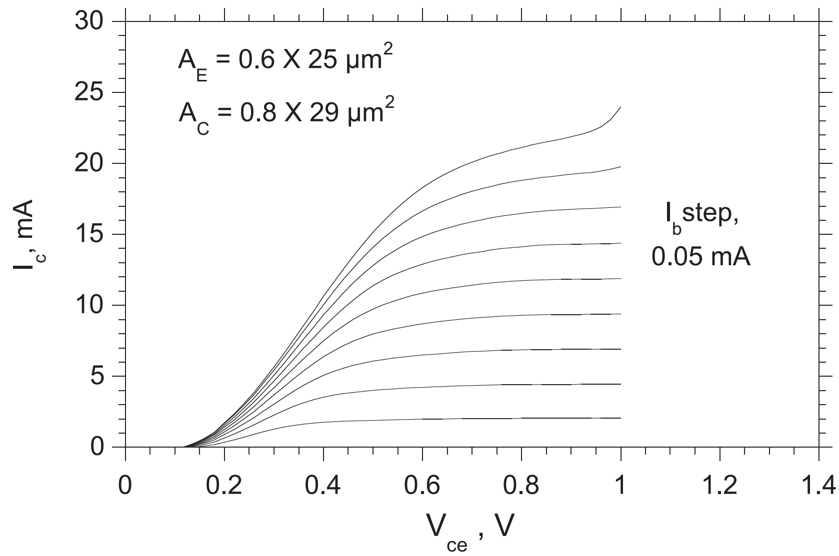
The staggered alignment of collector and emitter is also used in the ICs. The yield is greatly reduced as only one or two out of 9 circuits in each cell will be aligned. The next generation of devices and ICs will be fabricated using the stepper for photo-lithography. Given the tight alignment control (0.2 μm) available with the stepper, the staggered arrangement is not necessary. Much higher device and IC yield will be possible.

DC common-emitter characteristics of the HBTs are shown in fig 3.5. The small signal current gain at dc is 55. At high current density, narrow-collector (1 μm) devices show significantly larger collector-emitter saturation voltages ($V_{ce,sat}$), due to screening of the collector electrostatic field by the electron space charge. Screening occurs at a collector current density J_c satisfying the relationship $(V_{cb} + \phi) = T_c^2(J_c/v_{sat} - qN_d)/2\epsilon$, where T_c is the collector depletion layer thickness, N_d the collector doping, ϕ the junction built-in potential, and v_{sat} the electron velocity. In wide-collector HBTs, which have $\geq$ 2:1 collector to emitter width ratio, there is significant lateral spreading of the electron flux at high current, reducing the collector space-charge density. Lateral confinement of electrons in narrow-collector HBTs results in both increased $V_{ce,sat}$ and decreased emitter current density at the onset of f_t collapse (Kirk effect), resulting in increased emitter charging times and reduced f_t.

The common-emitter breakdown voltage BV_{CEO} is $\sim$ 2.5 V, decreasing to 1.5 V at 1 $\times 10^5$ A/cm^2. A discussion about the breakdown mechanism in these HBTs has been included in the latter part of this chapter.

3.2.3 RF Characteristics of baseline HBT

Fig. 3.6 shows the short-circuit current gain h_{21}, maximum stable gain (MSG), and Mason's unilateral power gain U. Mason's gain is used for extrapolating f_{max} because of its characteristic -20 dB/decade slope and its in-



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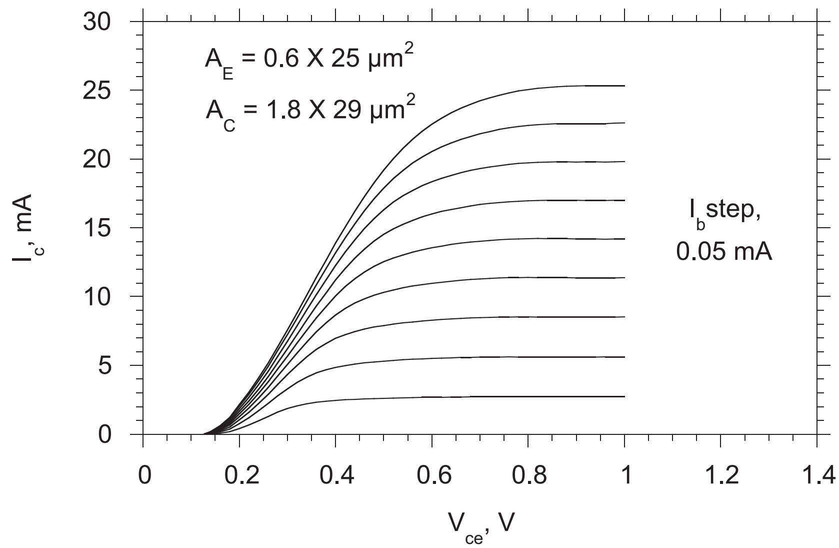


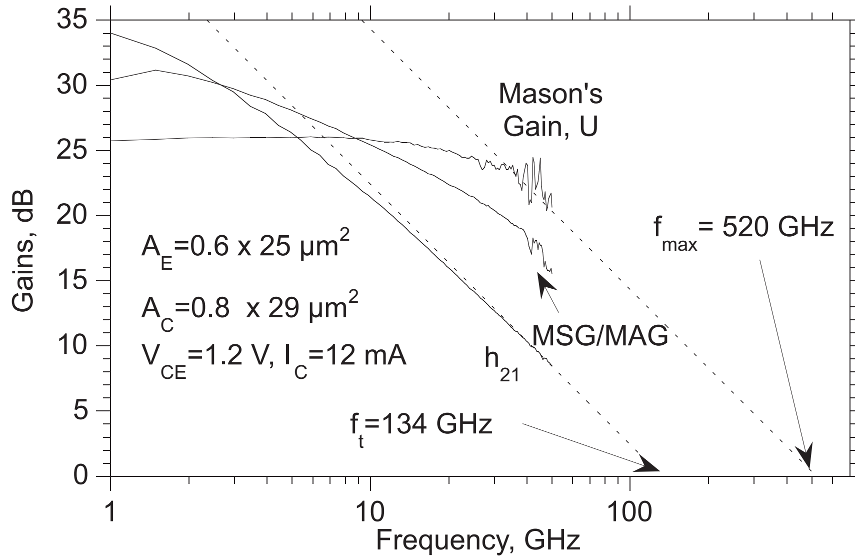
b)

Figure 3.5: DC characteristics of baseline HBTs, a) Nominal 1 μm collector width b) Nominal 2 μm collector width.

dependence of the transistor configuration (common-base vs. common emitter), and its independence of pad inductive and capacitive parasitics. Pad parasitics on these transistors, fabricated on thick BCB ($\simeq 10\mu$m) is small enough to be neglected. Bias conditions are as shown. Extrapolating at -20 dB/decade, f_{max} is 400 GHz and f_t is 164 GHz for the 2 μm width collector devices (fig. 3.6). 1 μm collector devices have 134 GHz f_t and 520 GHz extrapolated f_{max}. The high f_{max} is due to the reduced $r_{bb}C_{cb}$ time constant, both due to the low base ohmic contact resistance and reduced C_{cb} from the transferred substrate process. The MSG ($\simeq (\omega C_{cb})^{-1}(r_{ex} + (kT/qI_E))^{-1}$) is higher for the narrow-collector devices because of the reduced C_{cb}.

The estimates of f_{max}, obtained by extrapolating data from 50 GHz to 500 GHz are at the limit of reliability for a 50 GHz network analyzer. f_{max} is estimated by calculation from $f_{max} \simeq \sqrt{f_t/8\pi r_{bb}C_{cbi}}$. C_{cbi} is the intrinsic base-collector capacitance, the fraction of C_{cb} charged through the base resistance r_{bb}. r_{bb} consists of sheet resistance and contact resistance. The measured base sheet resistance on this wafer is 600 $\Omega/\square$. We calculate [24] a 2.4 Ω base spreading resistance. Due to poor TLM design on this wafer, the specific contact resistivity falls below levels which can be reliably measured. We therefore use a specific contact resistivity of 60 $\Omega - \mu\text{m}^2$ obtained from measurements on subsequent wafer runs, where the TLM structures were redesigned. 3.8 Ω base contact resistance is estimated. C_{cb} is extracted from S- parameter measurements by plotting the imaginary part of the reverse admittance parameter Y_{12} vs. frequency. The C_{cbi}/C_{cb} ratio is not readily predicted from device geometry, but is often fitted by comparing measured and modeled S-parameters. In order to match the measured S-parameters to the modeled S-parameters it is necessary to assume C_{cbi}/C_{cb} ratio of 0.25 for the 2 μm collector devices and 0.5 for the 1 μm collector devices. For wide-collector devices, measured $f_t = 164$ GHz, $C_{cb} = 22.7$ fF, $C_{cbi} = 5.7$ fF and f_{max} calculated from $\sqrt{f_\tau/8\pi r_{bb}C_{cbi}}$ is 430 GHz. For narrow-collector devices, $f_t = 134$ GHz, $C_{cb} = 8.2$ fF, $C_{cbi} = 4.1$ fF, and calculated $f_{max} =$ 460 GHz. Both the above calculations and the microwave measurements indicate that f_{max} is at least 400 GHz.

A low value of C_{cbi}/C_{cb} ratio has been used in the above calculations. This low value is difficult to justify, given the physical dimensions of the HBT emitter and collector. To explain the low C_{cbi}/C_{cb} ratio a second order effect, C_{cbi} cancelation, is being investigated [31]. This is a negative collector capacitance component which arises from the modulation of the



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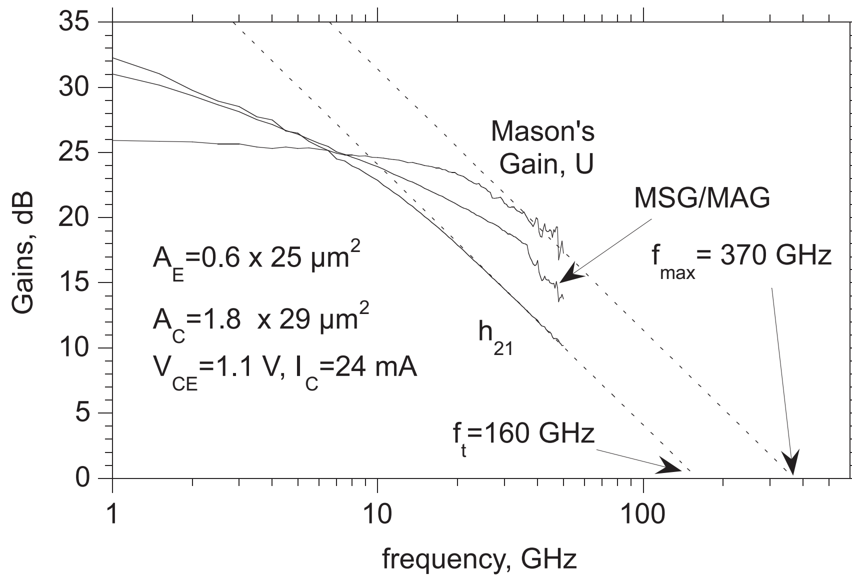


b)

Figure 3.6: RF characteristics of baseline HBTs, a) Nominal 1 μm collector width, b) Nominal 2 μ m collector width.

electron space-charge by the collector base voltage at high collector current.

Base pushout due to collector space charge screening occurs at a lower collector current in the narrow collector device, resulting in an increase in the emitter charging time and a drop in f_t. For collector widths greater than 2 μm, f_t degrades as the increase in the $R_{ex}C_{cb}$ time constant offsets the improvement due to reduced collector current density.

3.2.4 Bias dependence of RF parameters

Bias dependence of the S-parameters is used to extract the values of the HBT intrinsic and extrinsic device parameters. V_{ce} swings between 0.4 V to 0.7 V in CML circuits and 0.7 V to 1.4 V in ECL circuits. The bias dependent RF parameters are therefore necessary to predict digital circuit performance.

Variation of f_t with collector current for V_{ce} = 1 V is shown in fig. 3.7a. At low currents, f_t is dominated by the emitter charging time. As the collector current increases, f_t increases due to reduced emitter charging time. f_t levels off at high currents due to base push-out (Kirk effect). f_{max} follows f_t at low current density. At high current density, f_{max} falls due to a drop in f_t and an increase in C_{cb} due to base push-out.

The variation of RF characteristics with V_{ce} is shown in fig. 3.7b. At low currents, the electron concentration due to current flow in the collector is negligible compared to the back-ground doping. $(V_{cb,min}+\phi) = T_c^2(qN_d)/2\epsilon$, where T_c is the collector depletion layer thickness, N_d the collector doping and ϕ the junction built-in potential. For a given T_c and N_d, V_{cbmin} is required to deplete the background doping in the collector. Therefore, at low V_{cb} and low currents, the collector-base junction is undepleted. C_{cb} is high due to the undepleted collector - f_t and f_{max} are lower than that predicted from an increase in the emitter charging time due to small emitter current. As the collector current increases, N_d is compensated by J_c/qv_{sat}, which is the effective negative charge density due to current flow in the collector. Therefore, at moderate collector currents for a given V_{ce}, the collector is fully depleted. The RF characteristics improve until the collector current reaches the Kirk threshold for a given V_{ce}. With increasing V_{ce}, the Kirk threshold is pushed to higher current density. The HBT can be operated at higher currents without base pushout - both f_t and f_{max} are higher. For V_{ce} >1.2 V electrons in the collector acquire enough energy to

transfer in to the satellite valley, where the peak electron saturation velocity is lower. f_t therefore drops with increasing V_{ce} beyond 1.1 V.

The baseline transferred substrate HBT has achieved very high f_{max}. Traveling-wave structures or resonant matched circuits are limited by f_{max} in the circuit. Other circuits like feedback amplifiers and digital logic circuits are limited by f_t and f_{max}. For high circuit bandwidth, it is desirable to have a high f_t and f_{max}. In the next section, high f_t designs for CML and ECL circuits are discussed.

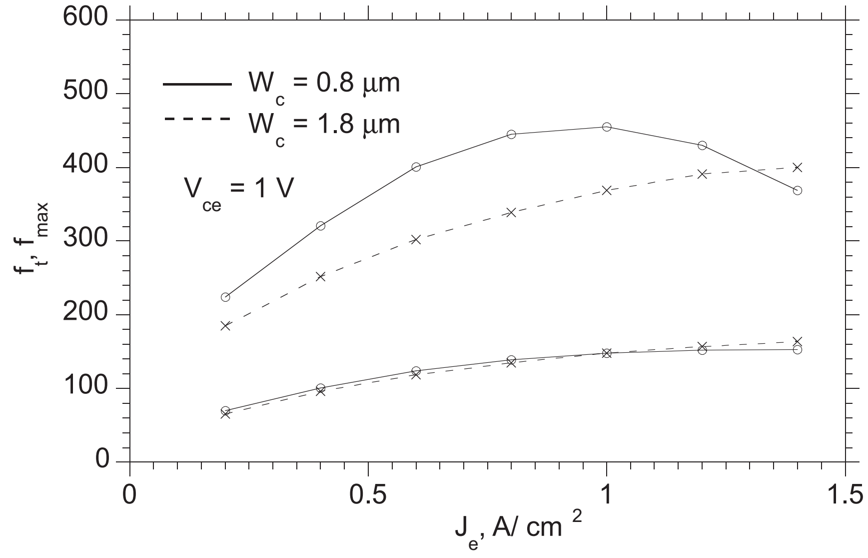
3.3 HBTs for digital integrated crcuits

Small signal analog circuits like amplifiers can be biased at a fixed bias point for peak f_t and f_{max}. In digital logic circuits, transistor performance over the voltage swing of the transistor is important. The epitaxial layer structure should therefore be optimized for the voltage range of operation of the logic family. Digital circuits require both high f_t and f_{max} for high clock rates. Epitaxial layer structure used for the baseline HBT, discussed in the previous section, is modified to obtain higher f_t and better RF performance in the voltage range of operation of the digital circuit. Epitaxial layer structures for high f_t devices were designed by Dino Mensa. HBTs with 2 μm collector width are used in ICs as they have higher f_t than 1 μm collector width HBTs. The 2 μm collector width devices also have a higher IC yield as they are less sensitive to misalignment between emitter and collector fingers. Two different devices, fabricated for current mode logic (CML) and emitter coupled logic (ECL) families, are discussed below.

3.3.1 Epitaxial Layer Structures of CML and ECL HBTs

The first layer structure (fig. 3.8a) is optimized for CML circuits where V_{ce} swings between 0.4 V and 0.7 V. In this voltage range, the baseline HBT has very poor DC and RF characteristics. These effects are mainly due to insufficient reverse bias on the collector-base junction. At this V_{cb}, there are two potential problems - undepleted N- collector at low collector currents and base push-out (Kirk effect) at high collector currents.

In the CML HBT design, collector thickness is reduced to 2000 $\AA$ and



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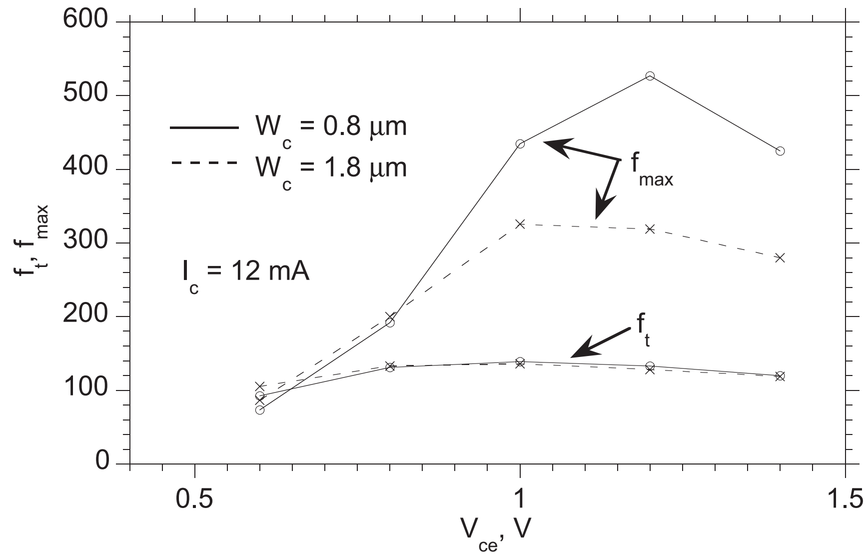


b)

Figure 3.7: Variation of baseline HBT RF characteristics with bias a) Variation with collector current, I_c. b) Variation with collector voltage, V_{ce}.

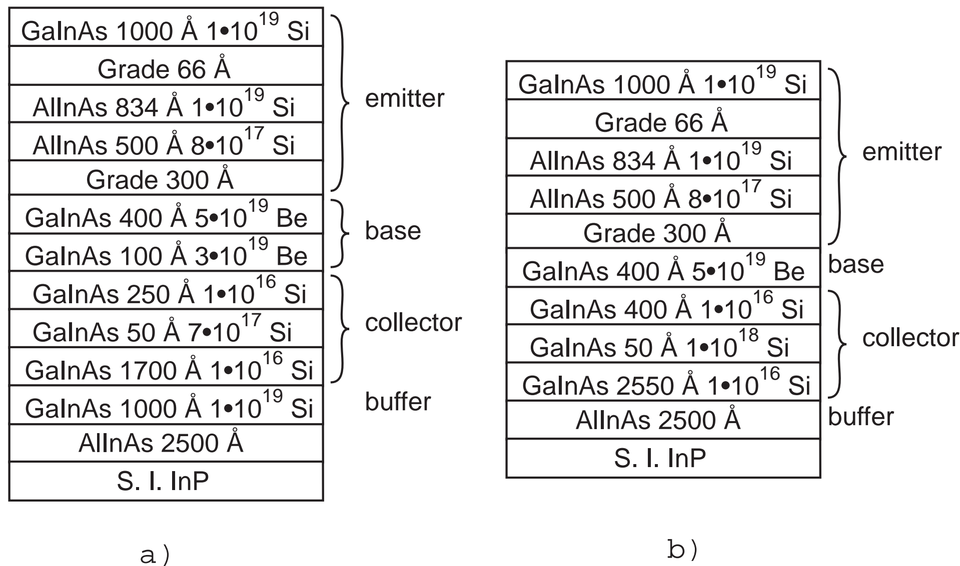


Figure 3.8: Epitaxial layer structures, a) CML HBT, b) ECL HBT.

a 1000 $\AA$ n+ sub-collector is added. The difference in the epitaxial designs, without the subcollector and with the subcollector, can be seen by comparing the band diagrams of fig. 3.4 and fig. 3.9 respectively. For the same external V_{cb}, the effective voltage dropped across the collector-base depletion layer is higher in the Ohmic sub-collector HBT compared to the Schottky collector HBT. $(V_{cbmin} + \phi) = T_c^2(qN_d)/2\epsilon$, where T_c is the collector depletion layer thickness, N_d the collector doping and ϕ the junction built-in potential. For the same collector width and doping, a smaller V_{cbmin} is required as ϕ is larger in the Ohmic collector device. Also, the fraction of the V_{cb} dropped across the pulse doped layer is reduced by decreasing the doping and pushing the pulse layer closer to the base. These changes are effective in depleting the collector at lower V_{cb}. Further, all the above changes are instrumental in increasing the electric field in the collector for a given V_{cb}. Base push-out for low V_{cb} occurs at higher current density, resulting in higher f_{max} and f_t.

In ECL circuits V_{ce} swings between 0.7 V to 1.3 V. The ECL epitaxial layer design is a only minor modification in the baseline HBT layer structure. Base thickness is reduced to 400 $\AA$ while the base band gap grading is increased to 2kT. The reduced base transit time should increase f_t of the

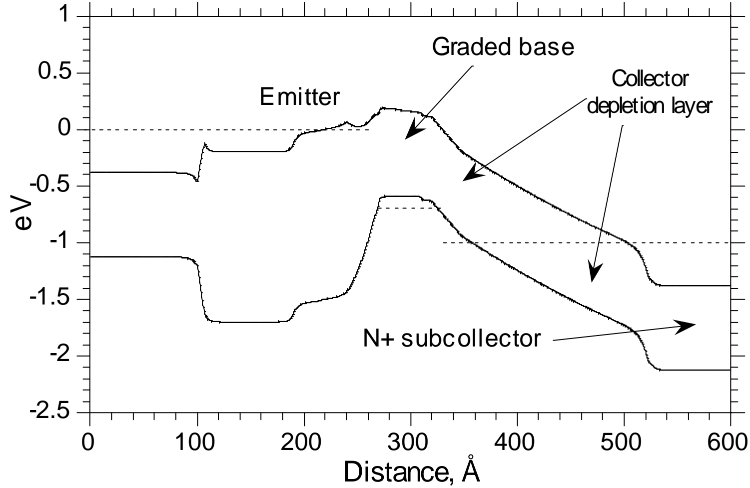


Figure 3.9: Band diagram of N+ subcollector CML device.

HBT. No significant changes are expected in the saturation or breakdown characteristics.

3.3.2 Extrinsic C_{be} reduction for high f_t

In digital logic circuits the device is switched between off and on states by the logic '0' and logic '1' levels. In the on-state, the diffusion capacitance $C_d = g_m \tau_f$, swamps the effect of the base-emitter depletion capacitance (C_{je}). In the off state, C_{je} is charged through any resistance connected to the base of the transistor, while C_d goes to zero. The propagation delay analysis (discussed in the next chapter) reveals that the switching speed of an ECL gate using the transferred substrate HBTs is limited more by C_{je} than C_d. At the device level, reducing C_{je} is one way to achieve higher f_t at all current densities.

C_{je} in the device is the sum of the intrinsic device junction capacitance and the extrinsic layout capacitance. Fig. 3.10 shows a comparison of the baseline device layout and the new layout used in the digital devices. The new device layout achieves a 80 % reduction in extrinsic base-emitter and base-substrate capacitance. The total base-emitter depletion capacitance

of the HBT is smaller. Emitter charging time is reduced resulting in higher f_t at all currents. This extrinsic device capacitance does not effect f_{max} of the transistor.

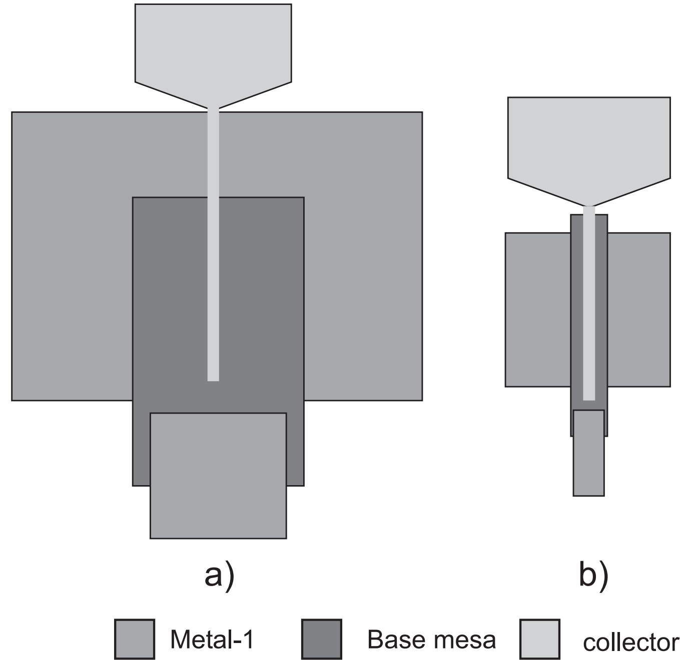
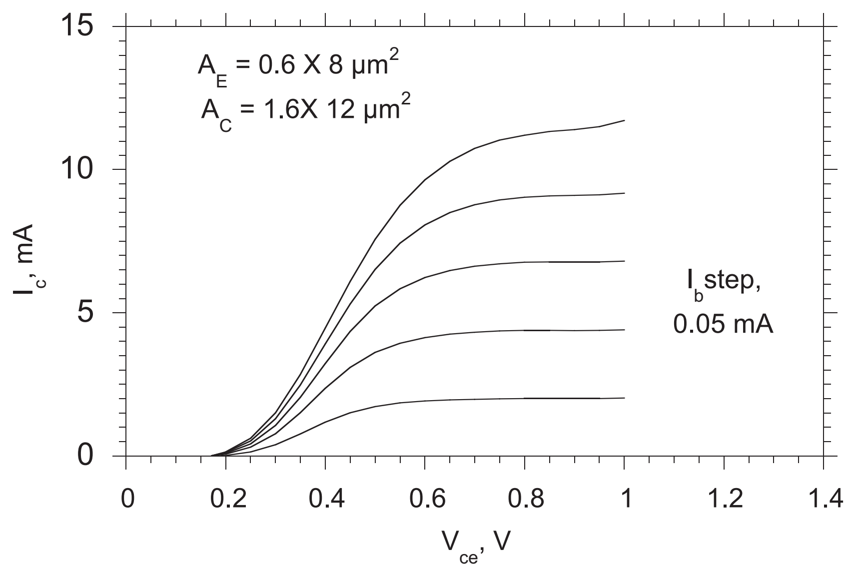


Figure 3.10: Comparison of HBT layouts a) Large mesa HBT b) Small mesa HBT.

3.3.3 DC characteristics and breakdown voltage

The common emitter DC characteristics of the CML and ECL device are shown in the fig. 3.11. The DC current gain for both devices is ~ 55. The improvement in the saturation characteristics of the CML device compared to the ECL device (and the baseline device) can be clearly seen. The space-charge resistance $R_{sc} = T_c^2/2\epsilon v_{sat} A_c$, is a measure of the slope of the DC characteristics in the saturation region. R_{sc} is smaller for the CML device due to reduced collector width (T_c). The Ohmic subcollector increases ϕ, the built in potential of the base-collector junction. This reduces the voltage at which the common-emitter DC characteristics intersect the x-axis (offset voltage).



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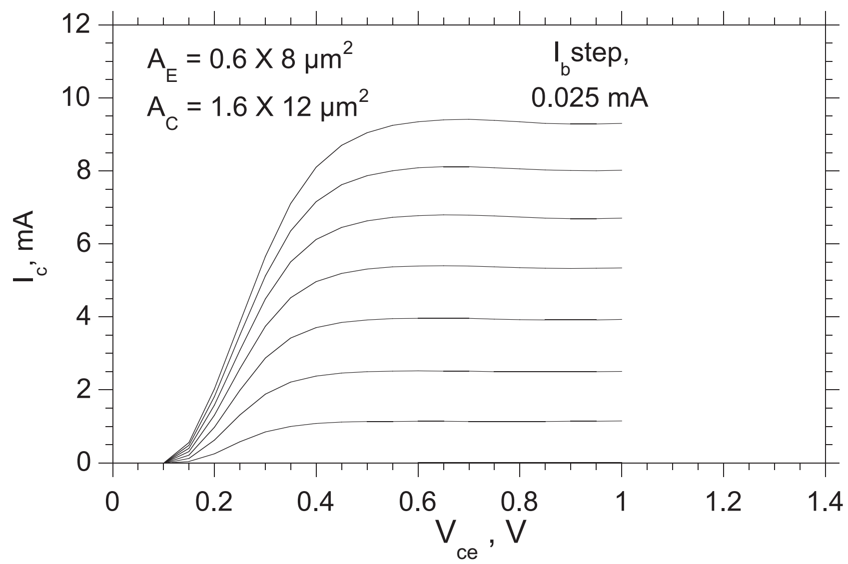


b)

Figure 3.11: DC common emitter characteristics, a) ECL HBT, b) CML HBT.

The common-emitter DC characteristic of the CML HBT for zero base current is shown in fig. 3.12, $BV_{CE0} \sim 2.4$ V . For the ECL device, a similar common- emitter characteristic is seen with $BV_{CE0} \sim 2.7$ V. Breakdown voltage in the common-base mode is higher as the collector leakage current is not multiplied by the current gain of the transistor. In the common-base mode, with zero emitter current, the CML device has a breakdown voltage $BV_{CB0} \sim 5$ V.

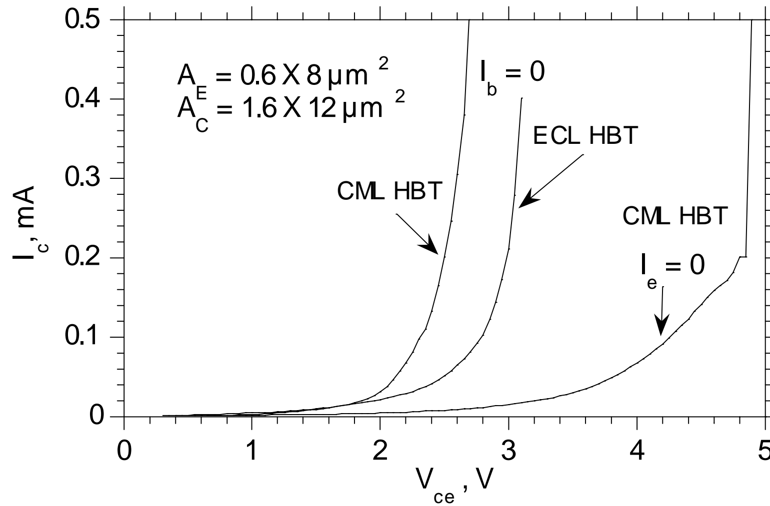


Figure 3.12: Breakdown characteristics of ECL and CML device in common emitter and common base mode.

At high current density, both the CML and the ECL device breakdown at $V_{ce} \sim 1.4$ V in the common-emitter mode and 1.8 V in the common base mode (fig.3.13). In digital logic circuits which employ differential pairs, the maximum current through the emitter of the HBT is limited by the current source. Also, a finite value resistance, between 0 Ω to 100 Ω, is connected to the base of the transistor in CML or ECL circuits. The breakdown voltage for this mode of operation, which is neither common-emitter nor common-base, is expected to be between 1.5 V and 2 V. Given that maximum V_{ce} is 1.3 V in the digital logic circuits, the breakdown voltage obtained here is sufficient.

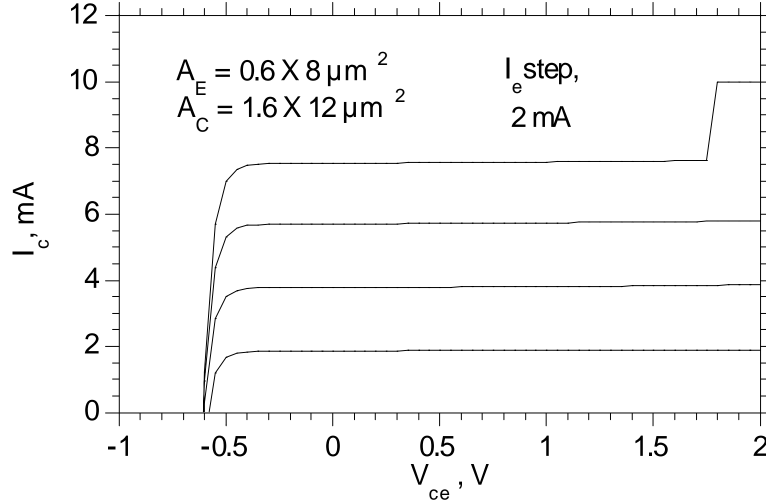


Figure 3.13: Common base DC characteristics of CML device.

For more complex digital circuits requiring multiple emitter followers for level shifting from the upper level gates to the lower level gates, a higher breakdown voltage is desirable. To improve the breakdown voltage, it is necessary to understand the breakdown mechanism in the current devices. Usually breakdown in the base-collector junction of InGaAs collector HBTs occurs due to one of three reasons - band to band tunneling (zener), impact ionization (avalanche) or thermal generation in the space charge region. For the transferred substrate schottky collector HBTs, an additional breakdown mechanism which involves hole tunneling from the collector metal to the semiconductor at high electric fields should also be considered.

In the CML device, the N+ sub-collector suppresses hole tunneling by providing a barrier for hole flow (fig. 3.9). If hole tunneling is the dominant effect causing breakdown in these devices, the CML device should have better breakdown voltage than the ECL device. A comparison of the measured breakdown voltages of the two devices reveals that hole tunneling is not the dominant breakdown mechanism. It is therefore clear from this data that the Schottky collector contact does not degrade the breakdown voltage of the HBT.

Low collector breakdown voltage and poor saturation characteristics in InGaAs collector HBTs has been explained by thermal generation in the collector space charge region [32].

$$I_c = \frac{\alpha M}{(1-\alpha M)} I_b + \frac{M}{(1-\alpha M)} I_{c0}$$

where α is the overall base transport factor, M is the collector multiplication factor, I_{c0} is the collector leakge current.

$$I_{c0} = q n_i W_c / \tau \propto \exp(\frac{-E_g}{2kT})$$

where W_c is the width of the collector space charge layer, n_i is the intrinsic carrier concentration and τ is the effective generation-recombination lifetime.

Due to the low bandgap of InGaAs compared to InP or GaAs , I_{c0} is several orders of magnitude larger. As I_{c0} is temperature dependent, device self heating from internal power dissipation gives rise to the soft breakdown characteristics at high currents.

At low currents and high V_{cb} (fig. 3.12), I_{c0} increases exponentially. Temperature dependent measurements by others [32] have shown that the breakdown voltage of InGaAs collector HBTs decreases with increasing temperature. Breakdown in these HBTs is therefore attributed to Zener tunneling. In contrast, Avalanche multiplication dominates in GaAs collector devices where breakdown voltage increases with temperature.

To reduce thermal generation and improve breakdown characteristics at high currents, the collector depletion width has to be reduced. Comparing the low current breakdown charctersitics with the high current breakdown characteristics, we conclude that the breakdown mechanism in the CML HBT which has a 2000 $\AA$ collector is dominated by thermal generation effects. To improve the breakdown characteristics at high currents, HBTs with collector depletion width smaller than 2000 $\AA$ should be fabricated. Reducing the collector thickness however, increases the band to band tunneling current at a given bias, causing Zener breakdown at lower V_{cb}. HBTs should be fabricated with the optimum collector epitaxial layer thickness for maximum breakdown voltage. From the experimental data for the 2000 $\AA$ collector device, we can conclude that the optimum collector width is less than 2000 $\AA$.

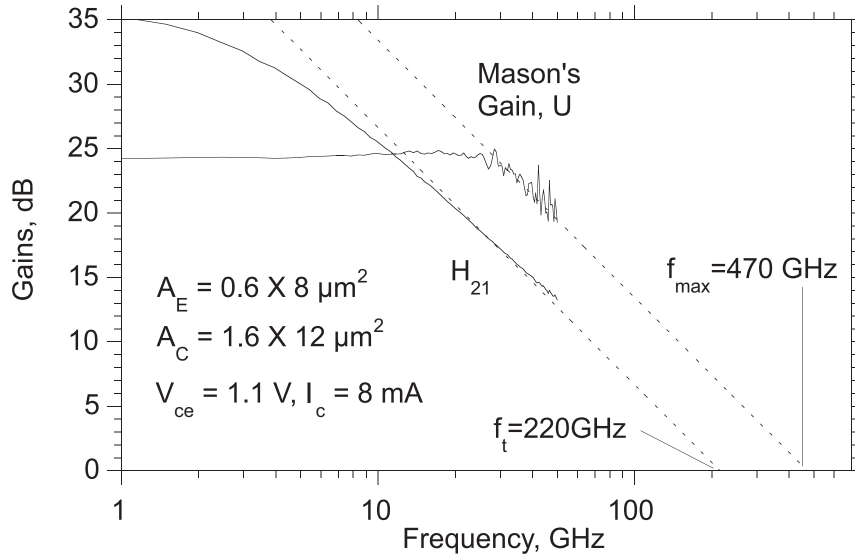
3.3.4 RF characteristics of ECL and CML HBTs

In digital ICs, the thickness of the BCB polymer layer has been reduced to 5 μm, so that smaller thermal vias can be fabricated, for increased packing density of HBTs. The pad capacitance is given by $\epsilon A/w$, where A is the pad area and w is the thickness of the BCB layer. The pad capacitance of 28 fF, which contributes about 40 % of the total base-emitter junction capacitance (70 fF), has to be stripped off the intrinsic device before extracting device parameters. f_t is obtained by extrapolating the short circuit current gain of the transistors after adding a negative input capacitance equal to the measured pad capacitance. f_{max}, which is independent of extrinsic lossless elements, is unaffected by the pad capacitance.

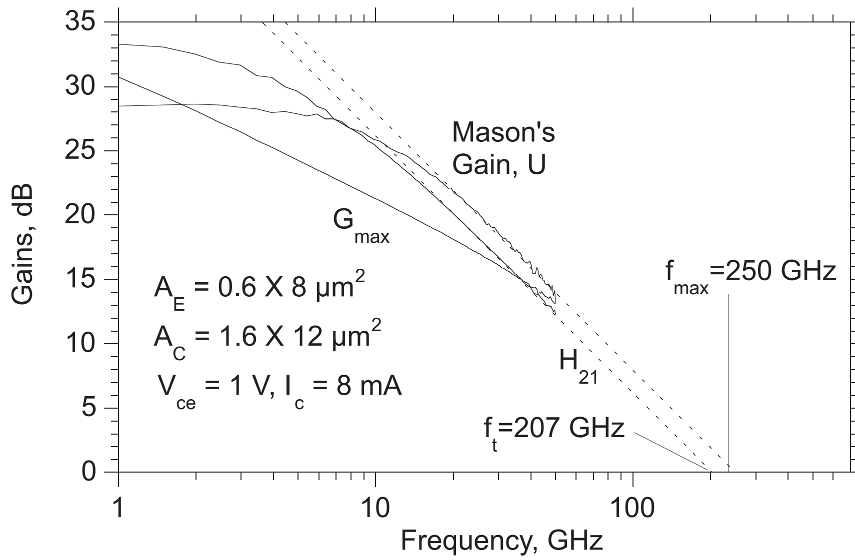
f_t and f_{max} of the ECL and CML devices are extrapolated from the gain plots shown in fig. 3.14. In the ECL device f_t = 220 GHz and f_{max} = 470 GHz. As expected, f_t is higher due to reduced base transit time and reduced extrinsic base-emitter capacitance. When compared with earlier devices, C_{je} for a similar sized ($1 \times 8 \mu\text{m}^2$) emitter has reduced from 65 fF to 40 fF. At low collector-base voltage and low collector currents, C_{cb} increases as V_{cb} is not sufficient to fully deplete the collector. f_t drops due to an increase in the $C_{cb}R_{ex}$ charging time. f_{max} falls, both due to increase in C_{cb} and decrease in f_t. At low collector-base voltage and high collector current, the electric field in the collector is not sufficient to prevent base push-out. The increase in base transit time and collector-base capacitance under these conditions reduces both f_t and f_{max}. f_{max} drops from 470 GHz at V_{ce} = 1.1 V to 140 GHz at V_{ce} = 0.6 V.

The CML device has peak f_t of 207 GHz and f_{max} of only 250 GHz (fig. 3.14). The base resistance of the CML device is only marginally higher than the ECL device. The low f_{max} is due to large C_{cbi}. The increase in C_{cbi} for this device is much higher than that expected due to the reduction of the collector thickness from 3000 $\AA$ to 2000 $\AA$. It is suspected that the low C_{cbi} in the baseline and ECL device is related to the design of the collector N+ pulse doped layer (launcher). To improve device performance at low V_{ce}, the launcher in the CML HBT has been weakened by moving it closer to the base edge in the depletion layer. The difference in the launcher design could be responsible for the increased C_{cb} in the CML device.

Although the CML HBT has poor peak f_{max}, the RF characteristics at low V_{ce} (in the range 0.4 V to 0.7 V) are much better than those for the ECL device (figs. 3.15 3.16). This is due the changes in the epitaxial design

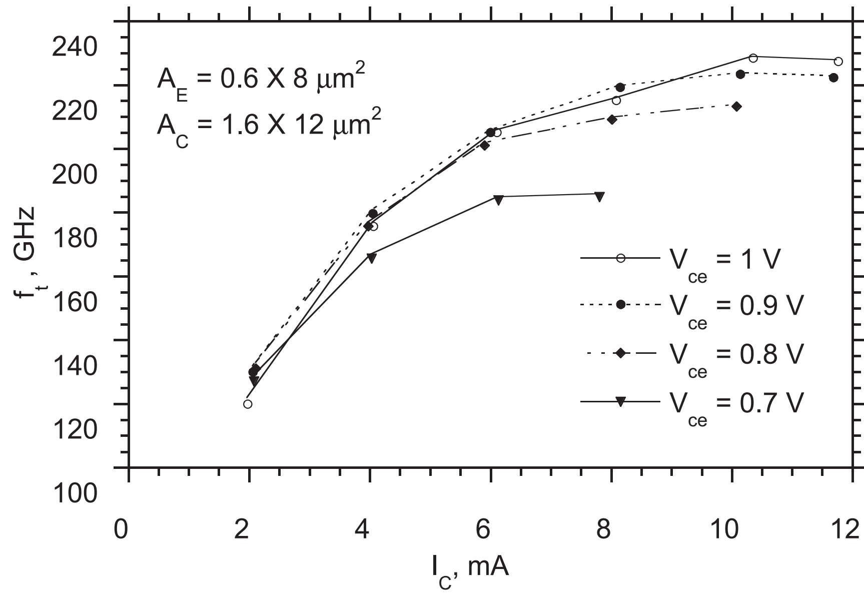


a)

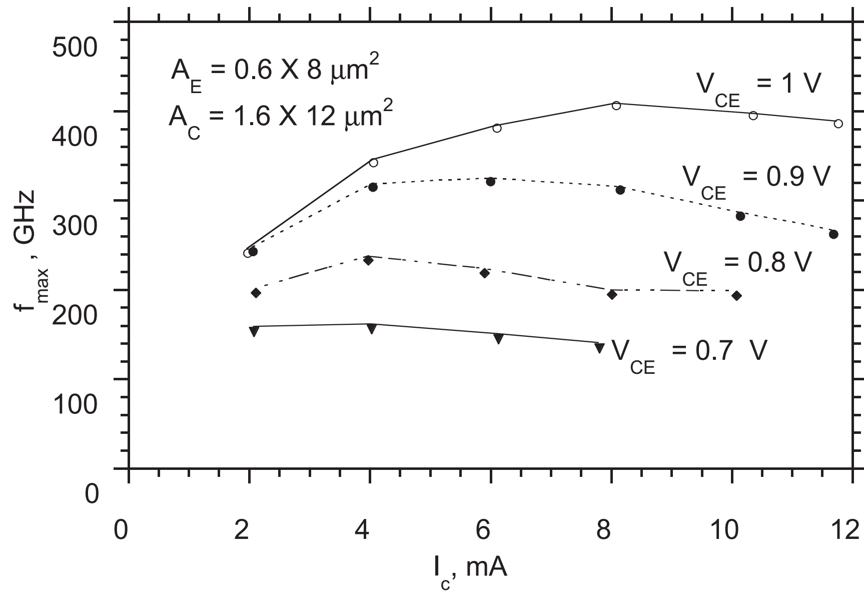


b)

Figure 3.14: a) RF characteristics of ECL device, b) RF characteristics of CML device.

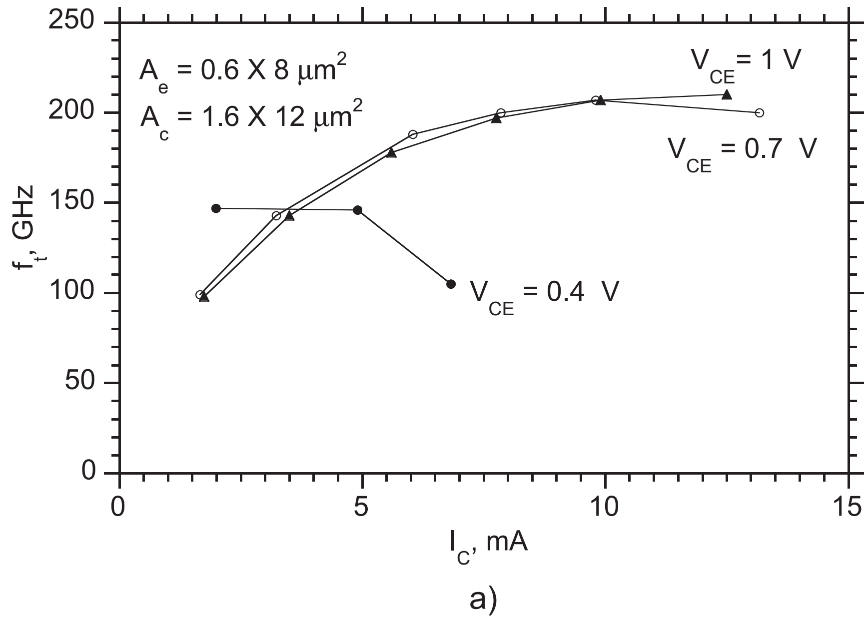


a)

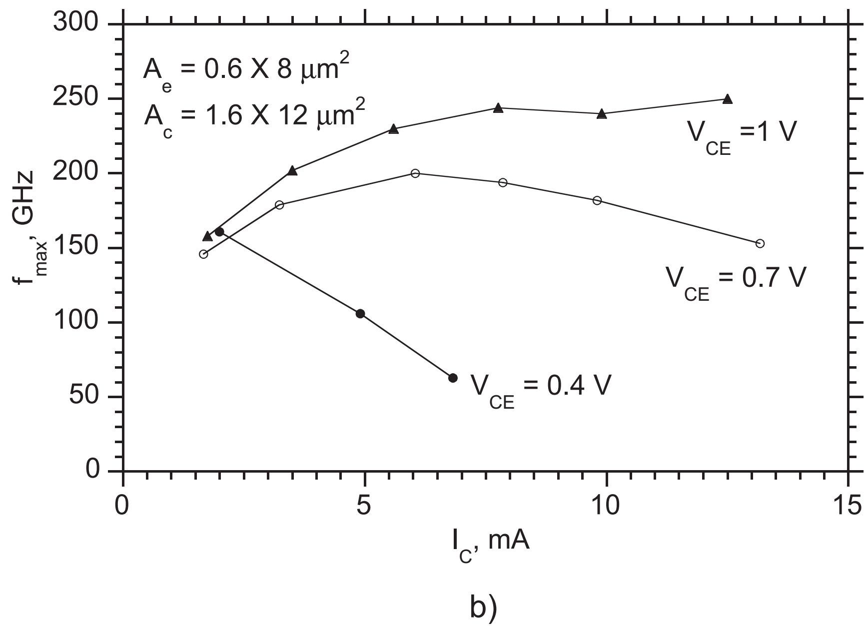


b)

Figure 3.15: Variation of ECL HBT RF parameters with I_c for different V_{ce}, a) Variation of f_t, b) Variation of f_{max}.



a)



b)

Figure 3.16: Variation of CML HBT RF parameters with I_c for different V_{ce}, a) Variation of f_t, b) Variation of f_{max}.

for lower saturation voltage.

In both the ECL and CML devices discussed above, the RF characteristics degrade as we bias the collector-base at the lower end of the voltage swing of the corresponding logic family. There are two variables in the design of the collector depletion region, the thickness of the depletion region and its doping. The doping in the collector region is chosen so that base pushout occurs at current density higher than 2 $\times 10^5 A/\text{cm}^2$. The base push out limit sets $N_d = J_c/(qv_sN_d)$, where N_d is the doping in the collector depletion region and v_s is the saturation velocity. The collector width is then chosen, so that the collector is completely depleted at the lowest V_{cb} of operation, $W = \sqrt{2qV_{bi}/qN_d}$. Using these expressions, the doping and minimum collector width of the device for a given voltage swing can be calculated. For devices used in CML logic circuits, the minimum collector width and collector doping should be 1400 $\mathring{A}$ and 2 $\times 10^{16}/\text{cm}^3$ respectively.

3.4 Device models

3.4.1 Hybrid π Models

Small-signal hybrid-π models of the two digital devices have been developed. Fig. 3.17 shows the hybrid-π model of a bipolar transistor. The model extraction procedure has been discussed in detail [24]. This simple model provides a reasonable fit to the measured S-parameters at a given bias and is useful for designing small signal analog circuits.

Fitting the S-parameters to the device model using computer optimization does not yield any insight into the physics of device operation. Further, the component values obtained by such an optimization have no physical significance. In the model shown here, the values of the various components have been determined from the bias dependence of the measured S-parameters. Emitter-base capacitance and forward transit time are extracted from plots of $1/(2\pi f_t)$ versus $1/I_c$. Slope of imaginary part of Y_{12} gives total collector-base capacitance. Extrinsic emitter resistance and transconductance are estimated by plotting real part of Y_{21} versus I_c. Output resistance R_{ce} is estimated from S_{22} at low frequency. Parasitic capacitance from emitter to ground is estimated from the overlap of the thermal via with the extrinsic emitter contact metal and the SiN capacitance per unit area.

If the base resistance is much higher than $1/(\omega C_{be})$, the output resistance is $1/(2\pi f_t C_{cbi})$. For this case, S_{22} at high frequency gives an estimate of C_{cbi}. For our devices however, the base resistance is comparable to $1/(\omega C_{be})$ = j30 Ω at 50 GHz. The output resistance is a function of both the intrinsic and the extrinsic base-collector capacitances. Hence C_{cbi} cannot be extracted from the measured high frequency S_{22} of the device. The split between the extrinsic and the intrinsic collector-base capacitance (C_{cbi}/C_{cb}) for the device model can be estimated from extrapolated f_{max}. Given that f_{max} is obtained by extrapolating Masons gain from 50 GHz to >400 GHz, the C_{cbi}/C_{cb} value thus obtained should be verified.

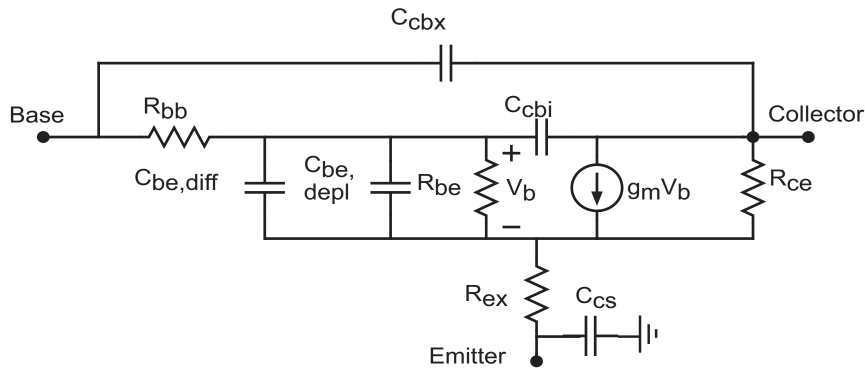
Base resistance is estimated by extrapolating S_{11} at high frequencies. S_{11} extrapolation to estimate the base resistance is valid only if the pad capacitance is subtracted out from the measured S-parameters. Large negative capacitance in the spice simulation could lead to unreliable extrapolations. An approximate device model should first be obtained by neglecting the effect of pad capacitances. It is necessary to re simulate the resulting device with the pad capacitances added and compare the S-parameters with the measured S-parameters. R_b and the split between intrinsic and extrinsic C_{cb} should be tweaked, until a good fit between the measured and the modeled S-parameters is obtained.

The hybrid Pi model is valid only under low and medium current density. It is difficult to fit measured HBT S-parameter data to a hybrid-π model for HBTs operating close to the Kirk threshold. The base stored charge of a HBT operating in this regime is modulated by the collector potential, an effect not modeled in the hybrid-π circuit. Another discrepancy is in the difference between the measured and simulated unilateral gain at low frequency. The roll off in the measured unilateral gain is probably an artifact of overdriving the HBT inputs at low frequency.

The hybrid-π model of the ECL and CML HBTs for V_{ce} = 1 V and I_c = 8 mA are listed below. Both devices have a 1 × 8 μm^2 emitter and 2 × 12 μm^2 collector.

Hybrid-π ECL HBT : R_b = 30 Ω, $C_{je,depl}$ = 40 fF, $C_{be,diff}$ = 170 fF, R_{be} = 200 Ω, C_{cbi} = 2 fF, C_{cbx} = 5.5 fF, g_m = 280 mS, R_{ex} = 7 Ω, C_{cs} = 7.5 fF.

Hybrid-π CML HBT : R_b = 32 Ω, $C_{je,depl}$ = 40 fF, $C_{be,diff}$ = 160 fF, R_{be} = 200 Ω, C_{cbi} = 5 fF, C_{cbx} = 9 fF, g_m = 280 mS, R_{ex} = 5 Ω, C_{cs} = 7.5 fF.



a)

```
.MODEL CMLHBT NPN IS = 5e-012 BF = 50 NF = 1 VAF = 12 IKF = 0
ISE = 5e-011 NE = 1.67 BR = 3 NR = 1 VAR = 38 IKR = 0 ISC = 5e-009
 NC = 1 RB = 43 IRB = 0.003 RBM = 33 RE = 3.5 RC = 0 CJE = 1.8e-014 VJE =
0.756 MJE = 0.5 TF = 5e-013 XTF  = 0 VTF = 0 ITF = 0 PTF = 0
CJC = 1.9e-014 VJC = 0.7 MJC = 0.33 XCJC = 0.25 TR  = 0 CJS = 0
VJS = 0.75 MJS = 0 XTB = 0 EG = 1.11 XTI = 35 KF = 0 AF = 1 FC =  0.8 NK = 0.5
ISS = 0 NS = 1

.MODEL ECLHBT NPN IS = 5e-012 BF = 50 NF = 1 VAF = 8 IKF = 0
 ISE = 5e-011 NE = 1.67 BR = 3 NR = 1 VAR = 38 IKR = 0 ISC = 5e-009
 NC = 1 RB = 30 IRB = 0.003  RBM = 30 RE = 6.5 RC = 0 CJE = 1.8e-014 VJE =
0.756 MJE = 0.5 TF = 5e-013  XTF = 0 VTF = 0 ITF = 0 PTF = 0
 CJC = 8.2e-015 VJC = 0.7 MJC = 0.33 XCJC =  0.25 TR = 0 CJS = 0
 VJS = 0.75 MJS = 0 XTB = 0 EG = 1.11 XTI = 35 KF = 0 AF = 1 FC = 0.8 NK = 0.5
ISS = 0 NS = 1
```

b)

Figure 3.17: a) Hybrid-pi model of a bipolar transistor, b) Spice models of CML and ECL HBT.

3.4.2 Spice Models

A SPICE model is developed for the ECL and CML HBTs (fig 3.17). The spice model is used in the simulations of the digital logic circuits. In addition to the device S parameters, a measurement to determine the off-state depletion capacitance of the device was performed by Shrinivasan Jaganathan and Dino Mensa. The spice models are verified by comparing the spice generated S-parameters with the measured S-parameters of the device. The pad capacitance must be added to the HBT during the verification of device models.

The SPICE model developed here does not model the Kirk effect and current gain roll off at high current densities. This model is valid only for V_{ce} in the range of 0.8 V to 1.2 V. At lower V_{ce}, the collector is either undepleted or in base push-out domain depending on the current. Both these effects and the drop in f_t, f_{max} at $V_{ce} > 1.1$ V are not included in the model. Good correlation between measured and modeled DC, RF characteristics is obtained at low and medium current density for V_{ce} between 0.9 V and 1.1 V.

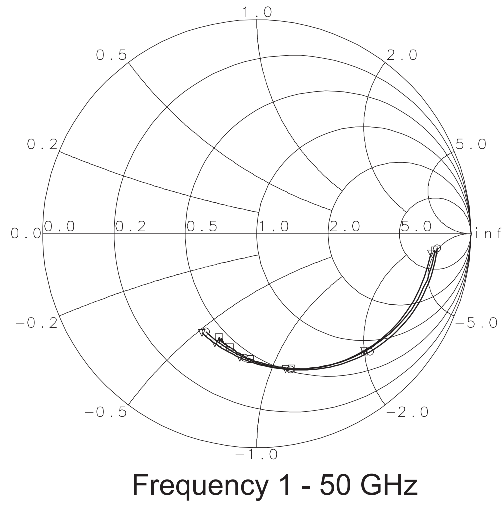
The models have been extracted at V_{ce} = 1 V. Excellent correlation is observed between the device and its models at V_{ce} = 1 V, for I_c up to 8 mA. The emitter area for both the CML and the ECL devices is 0.6×8 μm^2. The fig. 3.18 shows a comparison of the measured Vs. simulated S-parameters of the SPICE model and hybrid-π model at V_{ce} = 1 V and I_c = 8 mA.

3.5 Resistors

Resistors are characterized using TLM structures. 240 $\mathring{A}$ of NiCr gives a sheet resistance of 150 $\Omega/\Box$. Contact resistance between NiCr and metal-1 is negligible. In the ECL and CML static frequency dividers, current sources are implemented with resistors. A 0.75 $k\Omega$ current source resistor in the static divider circuits carries a current of 6 mA. Resistors are fabricated on BCB, which has almost zero thermal conductivity. Current capacity is therefore very poor . A 0.75 $k\Omega$ resistor which is 6 μm wide can only pass 3 mA of current.

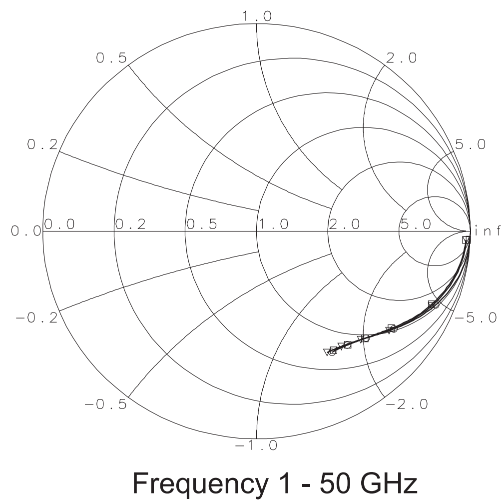
The current capacity of the resistors is improved by adding a thermal via on every resistor, so as to completely cover the NiCr layer and partially

□ Measured S11 ○ Hybrid-pi model S11 ▽ Spice model S11



a)

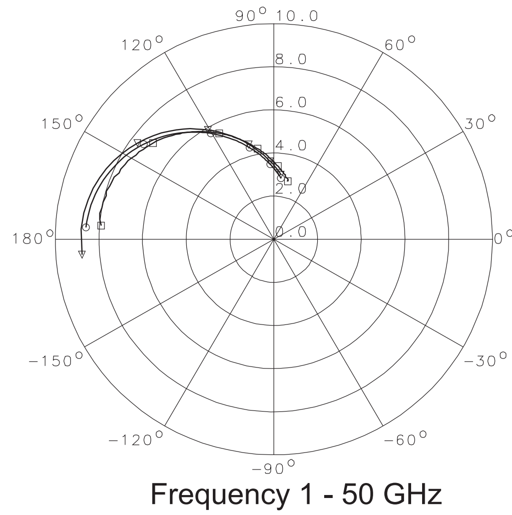
□ Measured S22 ○ Hybrid-pi model S22 ▽ Spice model S22



b)

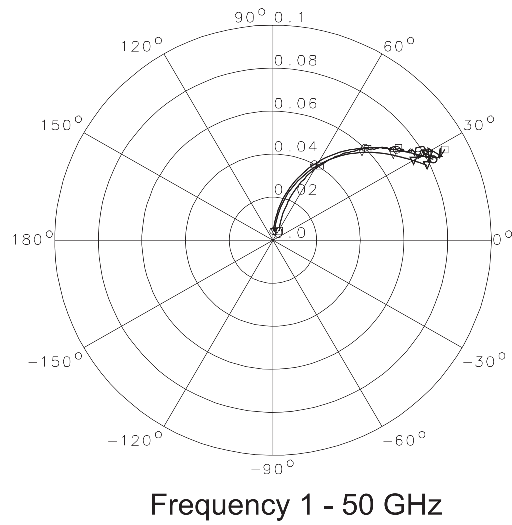
Figure 3.18: Comparison of simulated Vs. measured S-parameters of ECL HBT, a) S_{11}, b) S_{22}.

□ Measured S21 ○ Hybrid-pi model S21 ▽ Spice model S21



c)

□ Measured S12 ○ Hybrid-pi model S12 ▽ Spice model S12



d)

Figure 3.18: Comparison of simulated Vs. measured S-parameters of ECL HBT, c) S_{21}, d) S_{22}.

overlap its metal-1 contacts. In addition, the resistor width is increased from 6 μm to 15 μm. With these modifications, the 0.75 $k\Omega$ resistors are able to handle more than 10 mA of current. The via however, creates a distributed parasitic capacitance of 0.125 fF/μm^2 from the resistor to ground. When included in circuit simulations, the via capacitance has negligible effect on circuit performance.

The NiCr thickness of 240 $\AA$ is not recommended for use in future ICs. The sheet resistance is very sensitive to NiCr thickness for such thin layers. A sheet resistance of 50 $\Omega/\Box$ for a 450 $\AA$ NiCr layer is much more reproducible.

Chapter 4

Digital Integrated Circuits

Master-slave D-flipflops are important building blocks in fiber transceivers, sigma-delta ADCs and systems requiring high speed digital logic. The flipflop is a regenerative memory element similar to a latch, with a trigger pulse (clock) to control its change of state. In sequential logic circuits flipflops are necessary to avoid race conditions and resynchronization. The flipflop is therefore a fundamental building block for digital state machines. The maximum clock speed of the D-flipflop often limits highest speed of operation of the system. To evaluate the performance of a digital technology, D-flipflops configured as static 2:1 frequency dividers are used as bench mark circuits. Static frequency dividers are designed and fabricated in the current mode logic (CML) and emitter coupled logic (ECL) families. In this chapter, the design and results of the static divider circuits are discussed.

100 Gb/s logic can be realized with transistor bandwidth in the range of 300-400 GHz. The transferred substrate HBT technology yields the necessary HBT bandwidth in a low parasitic microstrip wiring environment. The technology has the potential to yield medium scale integrated circuits operating at 100 Gb/s clock rates.

4.1 Basic CML and ECL gates

100 GHz logic requires a combination of high HBT bandwidth and optimized circuit designs which utilize the full potential of the transferred substrate technology. The MS D-flipflop consists of series gated logic gates whose switching speed depends on a variety of circuit parameters including

the logic swing, load resistance, peak operating current density and area ratios of the different transistors. Design optimization can be performed using SPICE simulations. Such optimization however, does not offer any insight into the operation of the logic gate, nor the dominant time constants in the propagation delay. An analytical model is therefore developed. The analytical model predicts the dependence of switching speed on the various circuit and device parameters.

Switching speed in logic circuits is related to the logic voltage swing. In rough terms, there is an optimum voltage swing at which the switching speed is maximum; the lower this optimum voltage swing, the higher the switching speed. A low optimum voltage swing is commonly achieved by adopting a differential-mode operation (CML and ECL), where the need for exact references is eliminated. The optimum voltage swing in the CML and ECL circuits is in the range of 200 mV-400 mV. In addition, cross-talk is reduced and other unwanted common-mode signals like ground bounce are eliminated. Fig. 4.1a shows a basic current mode logic gate. The circuit consists of a current switching differential pair with resistive loads and a current source. The current source can be realized using a transistor or a resistor. Transistor count in the circuit is minimized by using a resistor current source. Given a 300 mV logic swing, V_{ce} for the on-transistor is 0.4 V, while that for the off-transistor is 0.7 V. The CML device is used in the CML circuits. The epitaxial layer structure of this device has been designed specifically for use in the CML circuits (3.8a).

The circuit diagram of a basic ECL gate is shown in fig. 4.2a. Emitter followers at the output improve the drive capability in the presence of capacitive loads. The emitter-followers also act as voltage level shifters, so that V_{ce} for the switching transistors is in the range 1.1 V to 1.4 V. The ECL HBT RF performance peaks for this bias. The epitaxial layer structure for this device is shown in fig. 3.8b.

The hybrid-*pi* parameters for the HBTs used in the digital logic circuits are shown in table 4.1.

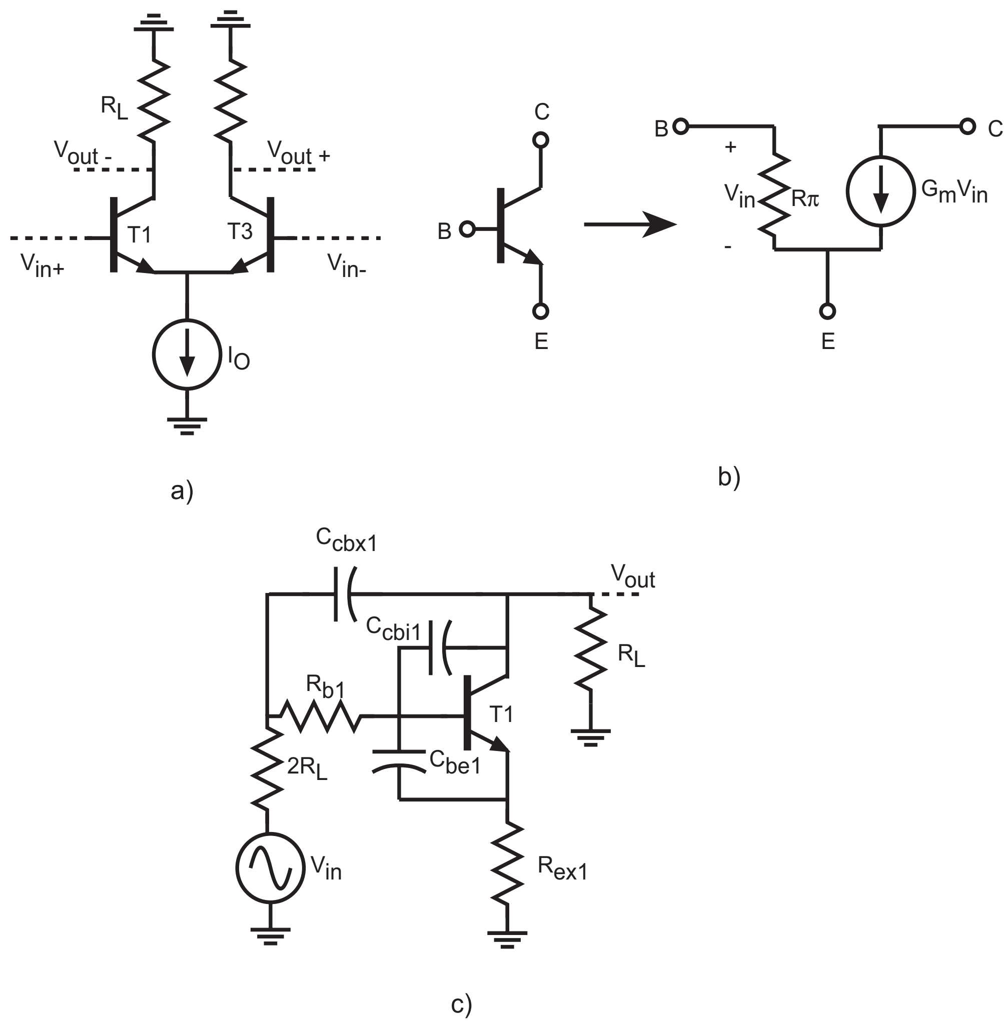


Figure 4.1: a) Basic CML gate. b) HBT without parasitics. c) CML equivalent circuit used for calculating propagation delay.

Device parameter	$1 \times 8\ \mu m^2$ emitter $2 \times 12\ \mu m^2$ collector CML HBT	$1 \times 8\ \mu m^2$ emitter $3 \times 12\ \mu m^2$ collector CML HBT	$1 \times 8\ \mu m^2$ emitter $2 \times 12\ \mu m^2$ collector ECL HBT	$1 \times 8\ \mu m^2$ emitter $3 \times 12\ \mu m^2$ collector ECL HBT
C_{jeoff}	20 fF	20 fF	20 fF	20fF
C_{jeon}	40 fF	40 fF	40 fF	40fF
C_{cbi}	3.5 fF	5 fF	2 fF	3 fF
C_{cbx}	10.5 fF	15 fF	6 fF	9 fF
R_b	30Ω	30Ω	30 Ω	30 Ω
R_{ex}	5 Ω	5 Ω	5 Ω	5 Ω
τ_f	0.5 ps	0.5 ps	0.5 ps	0.5 ps

Table 4.1: Device parasitics of transferred substrate HBTs used in digital ICs.

4.2 Propagation delay analysis for CML and ECL gates

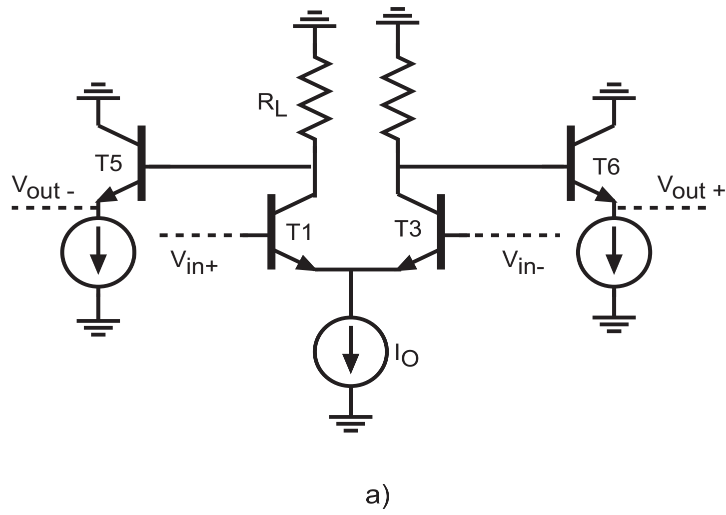
To ease calculating the switching speed of the logic gate, all the active and passive components have to be linearized [33], [34]. The emitter-base diode resistance (g_m), depletion capacitance (C_{je}) and diffusion capacitance (C_d) of the HBT are linearized by considering their average value during the switching period.

The following linearized models are assumed:

1. The resistance of the base-emitter junction is approximated by a linear resistor. The large signal output voltage swing of the logic gate is equal to the input voltage swing. The logic gate therefore has unity large signal gain.

$$G_m R_L = 1 \text{ or } G_m = 1/R_L$$

where G_m is the large signal transconductance of the device and R_L is the collector load resistance.



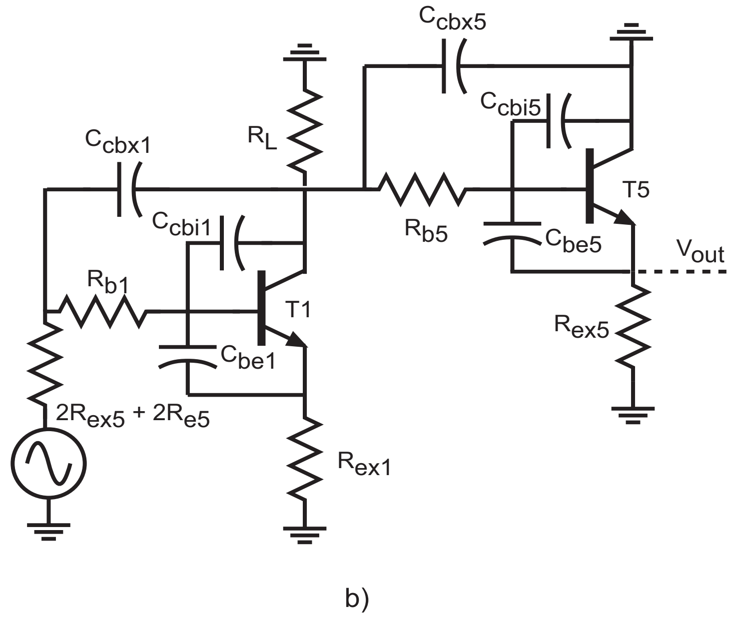


Figure 4.2: a) Basic ECL gate. b) ECL equivalent circuit used for calculating propagation delay.

2. Average C_{je} is obtained from the measured C-V characteristics of base-emitter diode.

$$C_{je} = 1.5C_{je}(0)$$

where $C_{je}(0)$ is the zero-bias value of the base-emitter depletion capacitance.

3. The total charge injected in to the base of the transistor from zero collector current to I_0 is given by $I_0\tau_f$. The average capacitance is the ratio of the charge transferred to the change in voltage across the capacitance.

$$C_d = I_O\tau_f/\Delta V = \tau_f/R_L$$

where C_d is the average diffusion capacitance and τ_f is the forward transit time of the device.

4. It is assumed that the base-collector capacitance does not change with transistor bias. This is a good approximation for a fully depleted schottky collector.

4.2.1 CML propagation delay analysis

The equivalent circuit of the CML gate used for calculating the propagation delay is shown in fig. 4.1c. The hybrid-π model is used to represent the HBT. The HBT with its parasitic capacitances and resistances stripped off is shown in fig. 4.1b. The method of time constant analysis (MOTC) is used to estimate the propagation delay, which is the time between the 50 % cross-over points of the input and the output voltages [36], [35]. For a single pole response the 50 % cross-over point is given by $ln(2)\tau_{total}$. Assuming a fan-out of 2, the source resistance is twice the load resistance of the previous logic gate. As discussed earlier, large signal g_m, C_{je} and C_d are used in the following analysis.

$$\begin{aligned}
\tau &= (2R_L + R_b + R_{ex})C_{be} + (4R_L + 2R_b + R_L)C_{cbi} + (4R_L + R_L)C_{cbx} \\
&= R_L(2C_{be} + 5C_{cb}) + R_b(C_{be} + 2C_{cbi}) + R_{ex}C_{be} \\
C_{be} &= C_{je} + \tau_f/R_L \\
T_{pd} &= ln(2)\tau = 6.8\ ps
\end{aligned}$$

To achieve the minimum propagation delay in a given technology, circuit parameters like voltage swing (ΔV), load resistance (R_L), peak operating current density (J_c) and transistor area (A) have to be appropriately selected. The above expression for the propagation delay can be used to perform an optimization, which will yield the optimum values of the various circuit elements. Given the number of variables in the expression, it is difficult to find the minimum value, without first fixing the values of some variables. A detailed discussion of the optimization process for the basic digital gate can be found in [33].

For the CML designs fabricated as part of this work $\Delta V = 300$ mV and $R_L = 50\ \Omega$. The 50 Ω load resistance is chosen so that no additional buffer stage is needed to drive the output load. While it is desirable to operate the device at very high current density for minimum propagation delay, base push-out and device heating limit the peak operating current density to $1 \times 10^5 A/\mathrm{cm}^2$.

The dominant delay in the CML gate is the term involving the load resistance and the device capacitance. This term contributes 72 % of the propagation delay of the logic gate. Replacing R_L by $\Delta V/(J_c A)$ where A is the area and J_c is the peak current density :

$$\begin{aligned} \tau_{dom} &= R_L(2C_{je} + 5C_{cb}) = \frac{\Delta V}{J_c A}(2c_{je}A + 5c_{cb}A) \\ &= \Delta V(2c_{je}/J_c + 5c_{cb}/J_c) \end{aligned}$$

where c_{cb} and c_{je} are the capacitances per unit device area.

The transferred substrate process achieves a big reduction in the intrinsic and extrinsic C_{cb} when compared to a normal mesa HBT process. CML circuits designed in the transferred substrate process will therefore achieve very high operating speeds.

The next generation of transferred substrate HBTs will be fabricated with emitters and collectors scaled to deep submicron dimensions. Deep submicron scaling does not improve c_{je}/J_c and c_{cb}/J_c. Given that these terms dominate the propagation delay, deep submicron scaling will not improve the switching speed significantly for CML gates. If higher current density of operation is acceptable, the optimum current density should be chosen so as to obtain minimum value of the sum of the two RC time

constants (τ_1 and τ_2) shown below.

$$\begin{aligned}\tau_1 &= R_L(2C_{je} + 5C_{cb}) \\ \tau_2 &= R_b C_d\end{aligned}$$

The current density for which the sum of τ_1 and τ_2 is minimum is given by J_{opt}, for which τ_1 is equal to τ_2.

$$\begin{aligned}J_{opt} &= \Delta V \sqrt{\frac{2c_{je} + 5c_{cb}}{r_b \tau_f}} \\ \tau_{opt} &= 2\sqrt{r_b \tau_f (2c_{je} + 5c_{cb})} \\ \tau_{total} &= \tau_{opt} + 2\tau_f + 2R_b C_{cbi} + R_{ex} C_{be} \\ T_{pd-opt} &= 3.7\ ps\end{aligned}$$

At the optimum current density of 5.5 $\times 10^5 A/\mathrm{cm}^2$ the propagation delay of the CML inverter has reduced to almost 50 % of the non-optimized value at 1 $\times 10^5 A/\mathrm{cm}^2$. At the optimum current density of operation, the dominant term in the CML propagation delay is proportional to the square root of the base resistance and τ_f. While deep submicron scaling reduces r_b, vertical epitaxial layer scaling reduces τ_f. Reducing r_b or τ_f will increase the optimum current density for minimum propagation delay. Therefore, the switching speed of CML gates can be improved if deep submicron scaling of emitter/collector dimensions and vertical scaling of the transistor epitaxial layers is accompanied by an increase in the peak operating current density.

The above analysis has neglected terms like R_{ex}, whose contribution to the propagation delay becomes significant as the current density increases. As a result, the optimum delay predicted from the analysis might not be accurate. Even then, the optimization is useful as it reveals the strategy for maximizing the speed of the logic family.

The above analysis also assumes a constant ΔV. To first order, in the above model, R_L does not effect the optimization. For different R_L, the transistor area ($A = \Delta V/(R_L J_{opt})$ can be chosen given the J_{opt} and ΔV.

4.2.2 ECL propagation delay analysis

For the ECL logic gate the equivalent circuit used for propagation delay estimation is shown in fig. 4.2b. Propagation delay is split into two terms - τ_1 is the delay in the switching transistor and τ_2 is the delay in the emitter follower.

$$\begin{aligned}\tau_1 &= (2R_{ex5} + 2r_{e5} + R_{b1} + R_{ex1})C_{be1} + (4R_{ex5} + 4r_{e5} + 2R_{b1} + R_L)C_{cbi1} + \\ &\quad (4R_{ex5} + 4r_{e5} + R_L)C_{cbx1} \\ \tau_2 &= r_{e5}C_{be5} + (R_L + R_{b5})C_{cbi5} + R_L C_{cbx5}\end{aligned}$$

where $C_{be5} = C_{jeon} + \tau_f g_m$

Optimum ratio of areas (A1/A5) for minimum gate delay can be calculated from the time constant expression if different areas are assumed for the two devices. This has been discussed in [33]. The following analysis assumes a 1:2 area ratio. The 1×8 μm^2 emitter, 2×12 μm^2 collector ECL device whose model is shown in table 4.1 is used.

$$\begin{aligned}\tau &= \tau_1 + \tau_2 = 2.5\ ps + 1.6\ ps = 4.1\ ps \\ T_{pd} &= ln(2)\tau = 2.8\ ps\end{aligned}$$

As in the CML case an optimum current density for the switching transistor in the ECL gate can be calculated.

$$J_{opt} = \Delta V \sqrt{\frac{3c_{cb}}{r_b \tau_f}}$$

The propagation delay for the ECL gate is however, less sensitive to the current density than the CML gate, as several terms contribute to the propagation delay. C_{je} contributes 38 %, C_d contributes 24 % and C_{cb} contributes the remaining 38 %. The contribution from C_{je} is greater than that from C_d. It is clear from this analysis that any further improvement in the transit time will be swamped by the effect of C_{je}. Significant improvements

in the ECL switching speed require submicron scaling of emitter/collector dimensions and lateral scaling of the epitaxial layers with a corresponding decrease in C_{je}.

The transfer function of the emitter follower has a zero which reduces its propagation delay. In order to keep the analysis simple, the effect of the zero on the gate delay has been ignored. A more accurate estimate of the propagation delay of the emitter follower can be found in [37].

4.2.3 Comparison with SPICE simulation

SPICE models developed for the CML and ECL HBTs, discussed in chapter-3, are used in the SPICE simulations. The device model used for SPICE simulations does not include the variation of RF parameters with collector-emitter bias. Given the circuit topology, the average value of various parasitic elements in the voltage range of operation is estimated and used in the models. Also, high current effects in the devices are not modeled. The simulation error due to the high current effects is however negligible, as the devices in the circuit are designed to operate at low or medium current density only.

Fig. 4.3 and fig. 4.4 show the switching characteristics of the CML inverter. These are the outputs of logic gates embedded a long string of inverters. Each inverter in the string has a fan-out of two. The propagation delay shown in the figure is the delay through a string of four inverters, from which the propagation delay through a single inverter is calculated.

The propagation delay of the CML gate for two different current densities has been evaluated. The current density of 1×10^5 A/cm^2 is used in the designs fabricated here, while the current density of $5 \times 10^5 A/\text{cm}^2$ is close to the optimum current density calculated from the time constant analysis. The propagation delay for the CML inverter improves from 8 ps at $1 \times 10^5 A/\text{cm}^2$ to 5 ps at $5 \times 10^5 A/\text{cm}^2$.

The propagation delay evaluated from SPICE simulation of a string of ECL inverters is shown in the fig. 4.5. While time constant analysis for the ECL gate predicts a propagation delay of 2.8 ps, the propagation delay obtained from simulation of the ECL gate is 3.75 ps. Ringing at the emitter follower outputs is a potential problem. SPICE simulations indicate that the problem of ringing in the emitter-followers is aggravated by the low C_{cb} in the transferred substrate HBT.

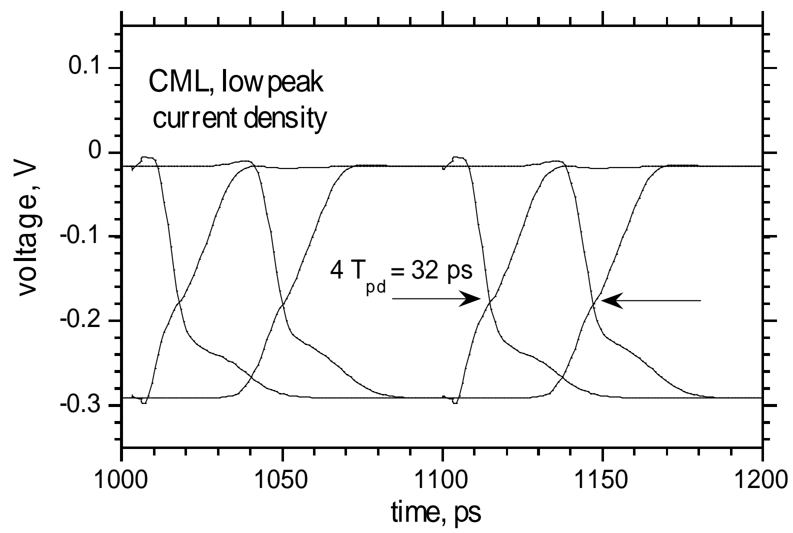


Figure 4.3: SPICE simulation of string of CML gates at current density 1 $\times 10^5 A/\mathrm{cm}^2$.

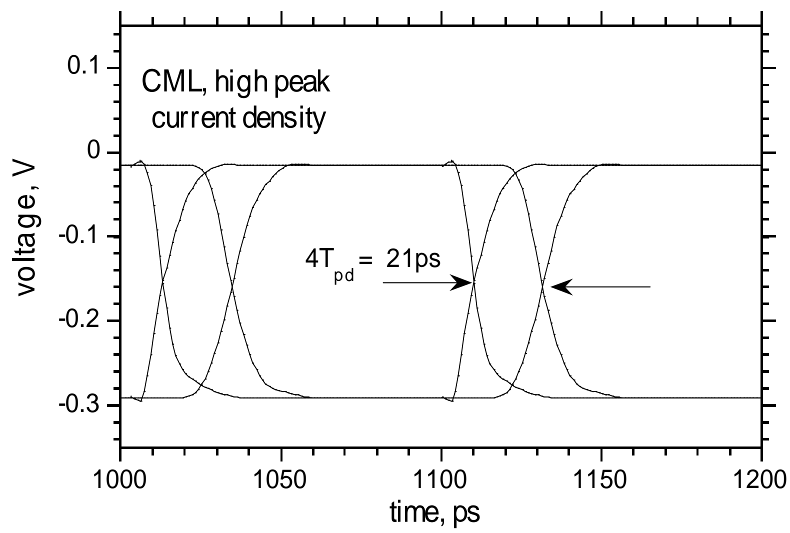


Figure 4.4: SPICE simulations of string of CML gates at current density 5 $\times 10^5 A/\mathrm{cm}^2$.

SPICE simulations indicate that ringing increases when the area of the emitter follower is small compared to the switching transistor. An 4:1 area ratio of the emitter follower to the switching transistor reduces ringing (without getting rid of it completely) without significant loss in switching speed. To completely eliminate ringing other circuit techniques, like a damping resistor at the output of the emitter follower should be used.

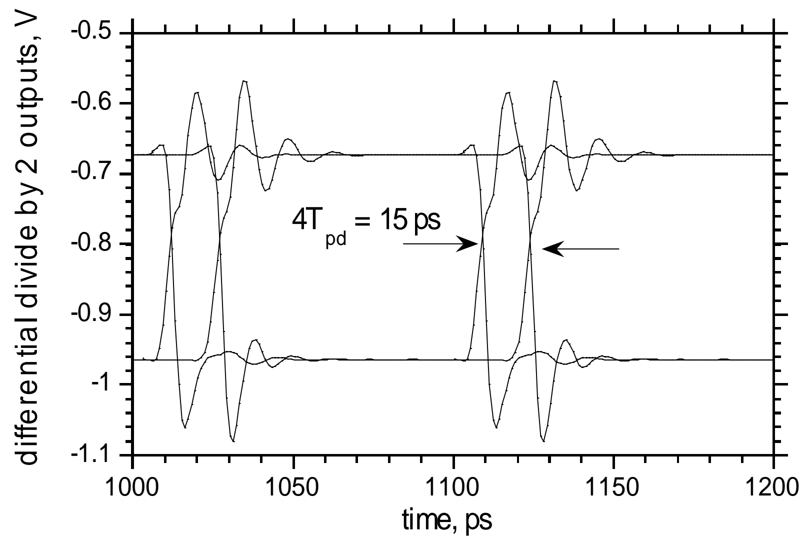


Figure 4.5: SPICE simulations of string of ECL gates.

4.3 Series gated CML and ECL gates

Digital logic circuits in the ECL and CML families employ series gated logic to realize the basic NAND function. A master-slave D-flipflop consists of the two series gated stages. The switching speed of the series gated circuits is related to a large number of device and circuit parameters. The propagation delay can be obtained from SPICE simulation. However, circuit optimization using SPICE simulations requires a large number of simulation runs as a number of circuit parameters can be varied. To narrow the

design space and identify the dominant delay terms, it is necessary to develop a simple, yet reasonably accurate analytical model for the propagation delay of these gates [37].

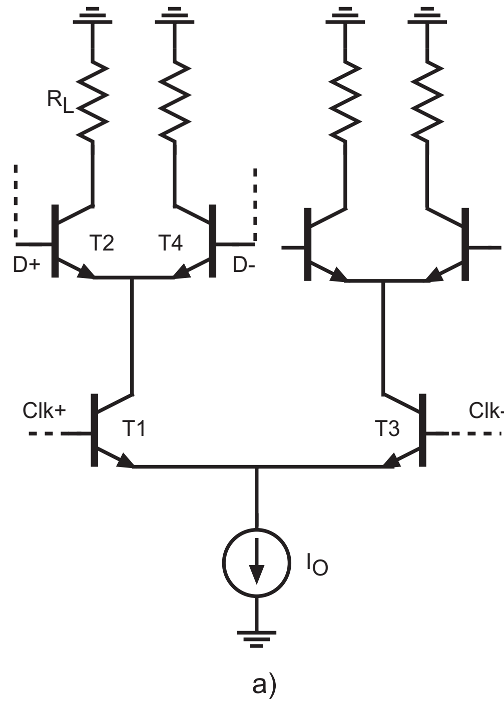
4.3.1 CML Series Gated Logic

To predict the operating clock speed of the D-flipflop and the static frequency divider, it is necessary to estimate the delay for signal propagation from the input on the gate lower level to the output on the gate upper level. The basic CML series gated configuration used in the D-flipflop is shown in the fig. 4.6a. To calculate the propagation delay for a lower level input, we assume that the upper level inputs remain constant during the switching event. While the base-emitter voltage for T2 is poised on the edge of conduction, T4 is switched off by the upper level inputs. T4 can therefore be omitted from the rest of the analysis.

As T2 is biased on the edge of conduction, the voltage change required for current flow in the base-emitter junction is smaller than the full logic swing ΔV. The average value g_m and C_d for this transistor are therefore higher than the earlier calculated average values. Also, on-state C_{je} should be used for this case. Approximating the diode I-V characteristics with a straight line in the conduction region, R_d and C_{du} have been calculated below. R_d, the average diode resistance of T2 $(1/G_m)$ while C_{du} is the average diffusion capacitance of T2 during the switching event.

The propagation delay is split into three parts τ_1, τ_2 and τ_3. τ_1 is the propagation delay from the lower level input voltage to output on the collector of T1 while τ_2 is propagation delay from the collector of T1 to the output voltage on the collector of T2. The equivalent circuits for calculating these delays are shown in the fig. 4.7b and fig. 4.7c. τ_1 is the delay in the lower level common-emitter stage while τ_2 is the delay in the upper level common-base stage. τ_3 is the RC time constant involving the load capacitance at the output node.

In a common-emitter amplifier, the effect of C_{cb} is increased by the Miller multiplication factor, which is the voltage gain of the circuit. For the CML series gated structure shown in fig. 4.7c, the common emitter stage has a voltage gain of $R_O/R_L \simeq 0.3$. To make the following analysis simple, we ignore the Miller multiplication factor in the following time constant analysis.



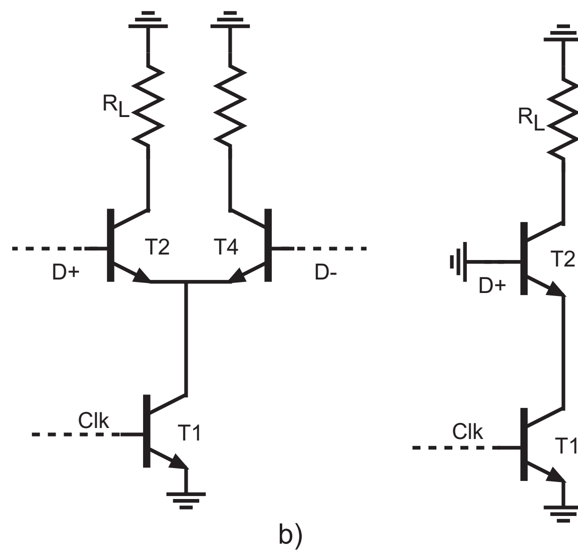


Figure 4.6: a) Series gated CML gate. b) Simplified series gated CML gate.

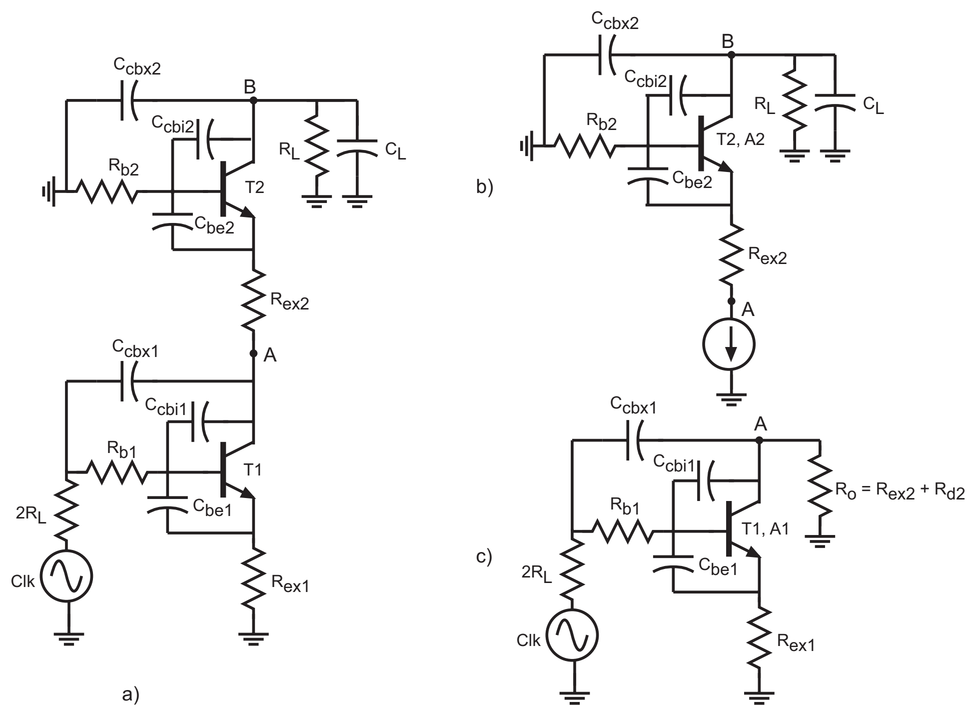


Figure 4.7: a) Simplified CML series gate with parasitics b) Upper level common base stage c) Lower level common emitter stage

$$
\begin{aligned}
R_d &= \frac{V_t}{I_O/2} \\
\tau_1 &= (2R_L + R_b + R_{ex})C_{be} + (2R_L + R_b + R_O)C_{cbi} + \\
&\quad (2R_L + R_O)C_{cbx} \\
\tau_2 &= R_d C_{beu} + (R_L + R_b)\, C_{cbi} + R_L C_{cbx} \\
\tau_3 &= R_L C_L
\end{aligned}
$$

where V_t is the thermal voltage

In the static divider, the output of the series gate is connected to two upper level differential pairs. Emitter current in these differential pairs is being switched off by the lower level inputs during the transition period. The load capacitance is therefore the average value of the on capacitance and the off state capacitance of the differential pairs. The average load capacitance seen by the series gate is given below:

$$
C_L = 2\left(0.5C_d + C_{je} + C_{cb}\left(1 + 0.5\left(\frac{R_L}{R_d + R_{ex}}\right)\right)\right)
$$

The propagation delay is estimated using the device model for CML device with 1 $\times 8\mu$m^2 emitter and 3 $\times 12\mu$m^2 collector.

$$
\begin{aligned}
R_d &= \frac{V_t}{I_O/2} = 30mV/3mA = 10\Omega \\
C_{be} &= C_{je} + \tau_f/R_L = 30fF + 10fF = 40fF \\
C_{beu} &= C_{jeon} + \tau_f/R_d = 40fF + 50fF = 90fF \\
\tau_{total} &= \tau_1 + \tau_2 + \tau_3 = 7.6\ ps + 2.05\ ps + 8\ ps = 18.25\ ps \\
T_{pd} &= ln(2)\tau_{total} = 12.8\ ps
\end{aligned}
$$

A large fraction of the propagation delay (44 %) is due to the poor drive capability of CML gate for capacitive loads. Both the basic CML gate and the series CML gate can be improved by operating the transistor at higher current density. Deep submicron device scaling should therefore be accompanied by a rise in the peak operating current density for faster CML circuits.

4.3.2 ECL series gated logic

Minor modifications in the CML delay expression are necessary to obtain the propagation delay expression for the ECL series gated logic gates. The equivalent circuits for calculating the delays are shown in the figure. τ_1 and τ_2 evaluated for the CML gate are modified to include the delay of the emitter followers.

$$
\begin{aligned}
\tau_1 &= (R_{ex5} + r_{e5} + R_{b1} + R_{ex1})C_{be1} + (2R_{ex5} + 2r_{e5} + \\
&\quad 2R_{b1} + R_{ex1} + R_{d2})C_{cbi1} + (2R_{ex5} + 2r_{e5} + R_{ex1} + R_{d2})C_{cbx5} + \\
&\quad r_{e5}C_{beon5} + (2R_s + R_{b5})C_{cbi5} + 2R_sC_{cbx5} \\
\tau_2 &= R_{d2}C_{be2} + (R_L + R_{b2})C_{cbi2} + \\
&\quad R_LC_{cbx2} + 2r_{e7}C_{be7} + 2(R_L + R_{b7}/2)C_{cbi7} + 2R_LC_{cbx7} \\
\tau_3 &= (R_{ex7} + r_{e7})C_L
\end{aligned}
$$

The ECL load capacitance is identical to that calculated for the CML series gated logic. The output time constant (τ_3) however, is much smaller for the ECL gate as the output capacitance is driven by the emitter-follower. For comparison the propagation delay of the ECL gate is estimated using the same device model as the CML gate.

$$
\begin{aligned}
C_L &= 160fF \\
\tau &= \tau_1 + \tau_2 + \tau_3 = 5.2\ ps + 4.9\ ps + 0.8\ ps = 10.9\ ps \\
T_{pd} &= ln(2)\tau = 7.6\ ps
\end{aligned}
$$

In going from CML to ECL, the switching speed of the series gated logic gate has improved from 14.5 ps to 8.5 ps. The improvement in switching speed of the ECL circuit is mostly due to the decrease in τ_3. As in the basic ECL gate, the emitter follower buffer improves the drive capability of the gate for capacitive loads. The improvement however, is at the expense of a big increase in the power dissipation.

Though extremely cumbersome, the analytical model developed here can be used to optimize the design of the series gated ECL logic gates. The

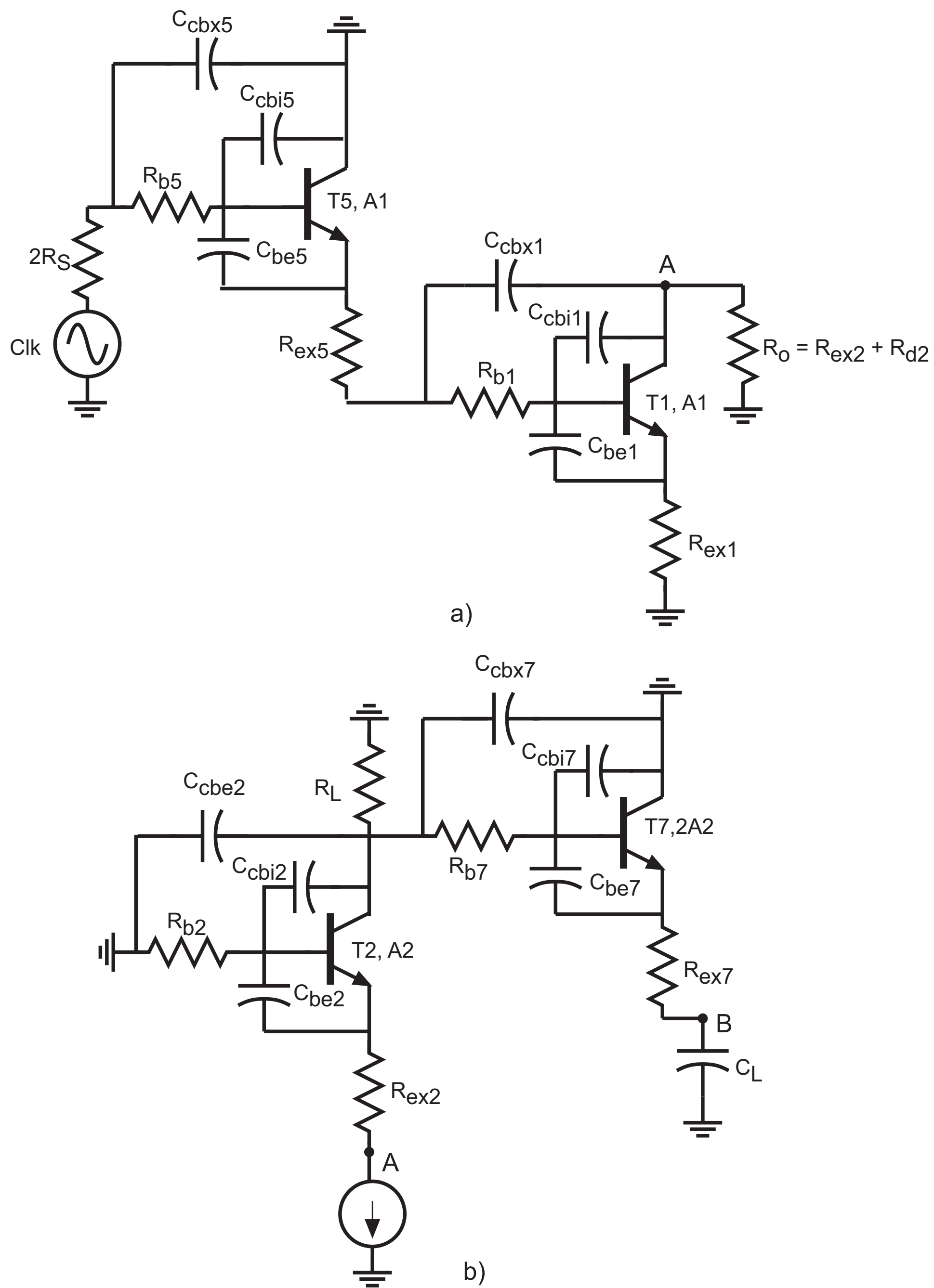


Figure 4.8: ECL series gate with parasitics. a) Lower level common emitter stage. b)Upper level common base stage.

number of variables in the circuit is larger than the ECL basic gate due to the presence of four transistors in the signal path, each of which could have a different area. If the ratio of the areas of the transistors is known, the optimization process can be made simpler. A simplified delay model with fixed transistor area ratios has been used in the next section of this chapter.

The ECL circuit fabricated in this work is implemented with nominal 2 μm collector ECL HBTs. For a full ECL circuit which involves a single level of emitter follower buffers on upper and lower levels, the propagation delay is estimated below.

$$\tau = \tau_1 + \tau_2 + \tau_3 = 4.8\ ps + 2.9\ ps + 0.55\ ps = 8.25\ ps$$
$$T_{pd} = ln(2)\tau = 5.8\ ps$$

Given the delay from the lower level input to the output on the upper level (T_{pd}), the maximum operating frequency of the divider is $1/(2T_{pd})$. The maximum clock frequency predicted from these calculations is 40 GHz and 85 GHz for the CML and ECL static frequency dividers respectively. The propagation delay expressions derived in the above analysis are useful to evaluate the effect of the various device and layout parasitics on the switching speed of CML and ECL static frequency dividers.

4.3.3 Optimized ECL series gate design

The propagation delay expression for the ECL dividers has several terms arising from the different parasitic components in the upper and lower level transistors. To help optimize the design of the ECL logic gate a simplified expression for the propagation delay is derived. Some terms in the delay expression have been neglected as their contribution to the total delay is small. Other terms which are invariant with transistor size and load resistance have also been omitted from the analysis below. They will be added after the optimum value is obtained.

$$T_{pd} = ln(2)\left(2C_dR_{ex} + C_{beu}R_d + C_{be}R_b + C_{cb}(3R_L + 2R_S)\right)$$

$2\tau_f$ in the propagation delay is from the emitter followers in the lower and upper level. The 2nd and 3rd terms are the contributions from the depletion and diffusion capacitance in the HBT.

$$\begin{aligned}
C_{beu} &= C_{jeon} + 5C_d = 2C_{je} + 5C_d \\
C_{be} &= C_{je} + C_d \\
\tau &= 2C_d r_{ex}/A + (2c_{je}A + 5C_d)r_d + (c_{je}A + C_d)r_b/A + c_{cb}A(3R_L + 2R_S) \\
\tau &= 2C_d r_{ex}/A + c_{je}r_b + 2c_{je}AR_L/5 + \tau_f + C_d r_b/A + +c_{cb}A(3R_L + 2R_S)
\end{aligned}$$

where c_{je} and r_b are calculated per unit area, A is the device area.

To simplify calculations further, we assume $R_L = R_S$ and again drop terms which are independent of transistor size. Given that $R_L = \Delta V/(J_c A)$, we calculate the minimum value of the expression.

$$\begin{aligned}
J_{opt} &= \Delta V \sqrt{\left(\frac{(5c_{cb} + 2c_{je}/5)}{\tau_f\,(r_b + 2r_{ex})}\right)} \\
\tau_{opt} &= ln(2)\left(2\sqrt{\tau_f(r_b + 2r_{ex})(5c_{cb} + 2c_{je}/5)}\right) \\
J_{opt} &= 3 \times 10^5\ A/\text{cm}^2 \\
\tau_{opt} &= 1.35\ ps \\
\tau &= 1.95\ ps\ \ \text{at J}_\text{c} = 1 \times 10^5\ \text{A/cm}^2
\end{aligned}$$

The τ_{opt} in the above expression is entirely a function of the intrinsic device parasitics. Given R_L and ΔV, the device area for minimum propagation delay is chosen so that the transistor operates at the optimum current density. For a given technology, we can then calculate the minimum delay using the full propagation delay expression and the optimum current density. For static frequency dividers designed using 2 μm collector ECL HBTs, optimum current density is 3 $\times 10^5$ A/cm^2. The peak clock frequency of the circuit at this current density (both simulated and calculated) is ~95 GHz. This is an improvement of ~ 10% from the the peak clock frequency at a current density of 1 $\times 10^5$ A/cm^2 - the peak current density used in this

work. It should be noted that the propagation delay in the ECL series gate is effected by a number of other terms; the optimized term(at its optimum value), with the ECL HBT device parameters, is no longer the dominant term. A change in current density from 3 $\times 10^5$ A/cm^2 to 1 $\times 10^5$ A/cm^2 therefore reduces the clock frequency only by $\sim$ 10%. Larger deviations from the optimum current density can result in a rapid increase in the propagation delay.

The optimization performed here does not take into account the effect of base push-out, which degrades HBT RF performance at current density exceeding 1 $\times 10^5$ A/cm^2. 3 $\times 10^5$ A/cm^2 current density without the on-set of base push-out can be achieved if the epitaxial layer is redesigned (thinner collectors). Digital ICs require a number of HBTs connected together by short metal wires in a small area. If all HBTs operate at very high current density, there is a chance that the IC will get too hot. Given that this work is the first demonstration of digital ICs in the transferred substrate technology, a conservative approach is adopted. Peak current density is limited to 1 $\times 10^5$ A/cm^2.

4.4 Layout of static frequency dividers

Careful layout of the circuit is required to reduce the parasitics on the critical paths by limiting wire lengths. Any parasitic capacitance on the collectors of the switching transistors in the ECL circuits deteriorates performance. While there is negligible parasitic capacitance from the wires on BCB, cross overs between metal-1 and metal-2 layers add 2.5 fF of capacitance per crossover. The microstrip back side ground plane eliminates ground return loop inductance by providing a continuous ground return path for high frequency signals on the IC. In this wiring environment, every wire is a transmission line sitting on BCB. Given the dimensions of the line and the properties of BCB, the wires can be modeled as a known lengths of transmission lines. For a BCB thickness of 5 μm and a line width of 4 μm, Z_0 is 88 Ω and velocity is 212 μm/ps. The wiring parasitics are extracted from the layout using the automatic extraction tool available in EESOF. For the circuits fabricated here, the circuit size is small enough (compared to the wavelength) that the wire parasitics can be modeled as lumped elements. It should be noted however, that in a dense layout the wire to wire coupling between closely spaced lines becomes significant. This coupling

capacitance between wires requires an electro-magnetic simulation. This effect had not been modeled here.

4.5 CML static frequency divider

4.5.1 Circuit Design

The schematic of a CML master-slave D-flipflop connected as a 2:1 static frequency divider is shown in the fig. 4.9. The D-flipflop consists of two identical cascaded stages a master stage and a slave stage. The differential pair of Q1, Q2 tracks the input voltage while Q3, Q4 regenerate the voltage at the collector nodes to the full digital logic levels.

A differential voltage swing of 600 mV and a load resistance R_L of 50 Ω is chosen. For this ΔV and R_L, the current I_0 is 6 mA. For minimum delay it is desirable to operate the transistor at the optimum current density calculated from the propagation delay analysis. Kirk effect and thermal breakdown however, limit the peak current density to 1 $\times 10^5$ A/cm^2. For this peak current density, the transistor area is 5 μm^2. The CML device with 8 $\times$ 0.6 μm^2 emitter and 12 $\times$ 3 μm^2 collector is used. 3 μm^2 collector width is used to increase yield by reducing the effect of collector-emitter misalignment. The hybrid-π model parameters for this transistor are listed in the table-1. The model for this HBT used in the SPICE simulations has been discussed in the previous chapter.

The circuit diagram of the CML static divider is shown in the fig. 4.9. One of the two differential clock inputs is capacitively grounded on-wafer. DC bias for this input is provided through an input pad. The second differential clock input is driven by a sinusoidal clock signal. The Tektronix 40 GHz sampling head provides one of the 50 Ω load resistance termination for the slave stage. The second 50 Ω load resistance for the slave stage is on-wafer. The 50 Ω loads are implemented with NiCr thin film resistors without thermal vias. The resistor current sources, which dissipate considerable energy due to their large resistance, require thermal vias to transfer the heat away from the resistors. The area of the CML static divider IC is limited by the size of the I/O pads to 400 $\times$ 400 μm^2 (fig 4.10).

SPICE simulation and estimation by the time constant analysis predicts a peak clock frequency of 35 GHz for the CML static divider with nominal 3 μm collector HBTs. The SPICE simulations include the para-

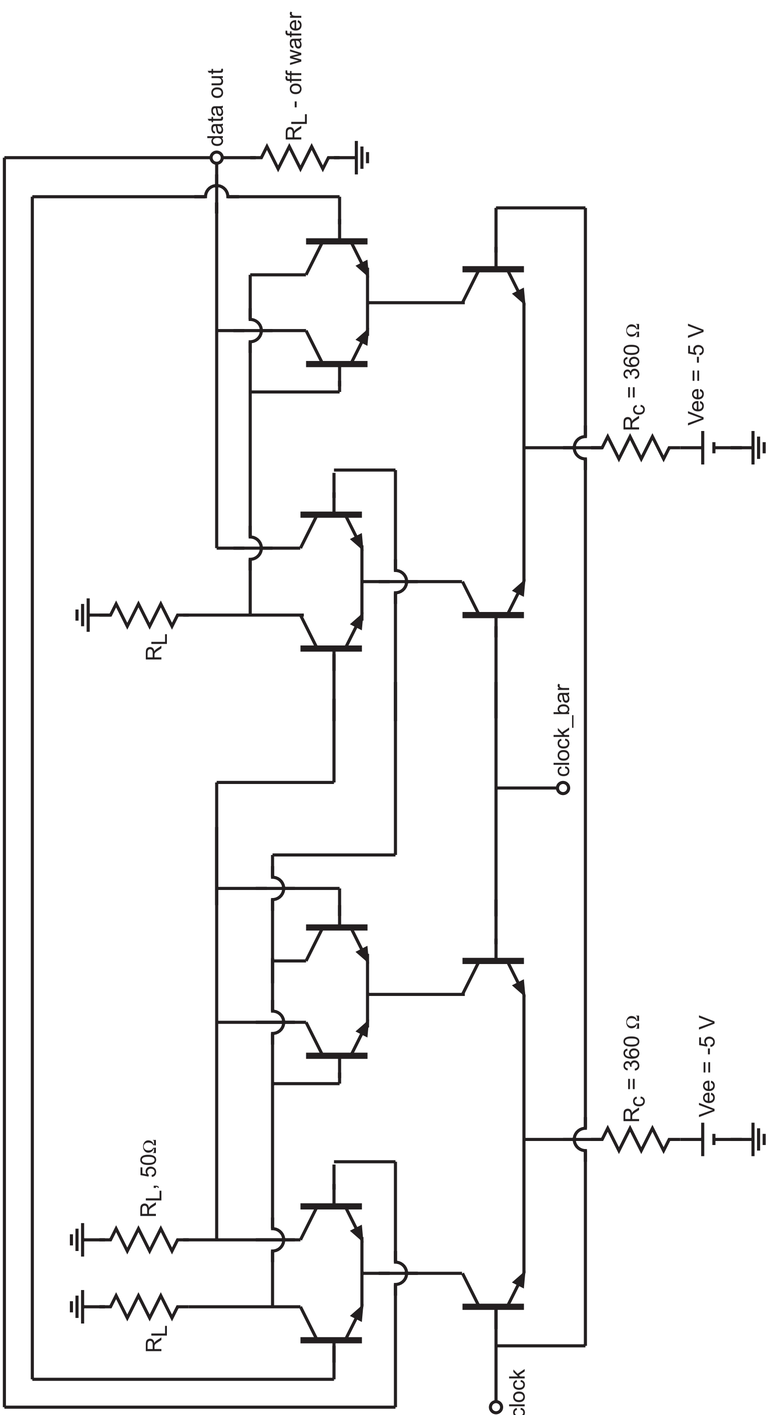


Figure 4.9: Circuit diagram of CML 2:1 static frequency divider.

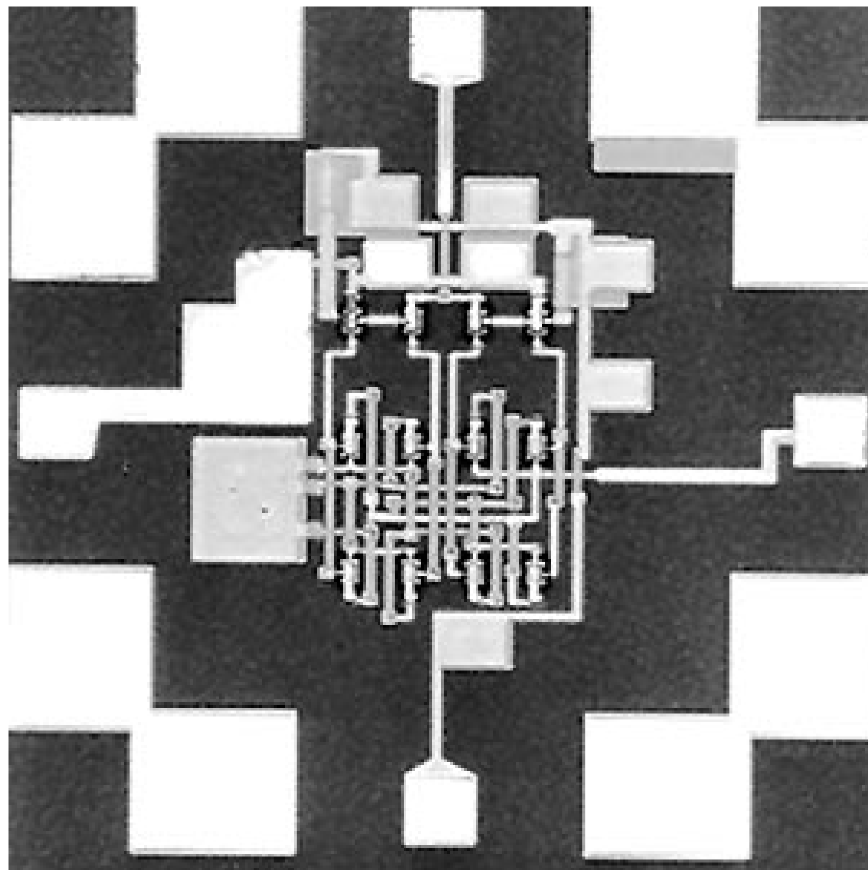


Figure 4.10: Photograph of CML static frequency divider.

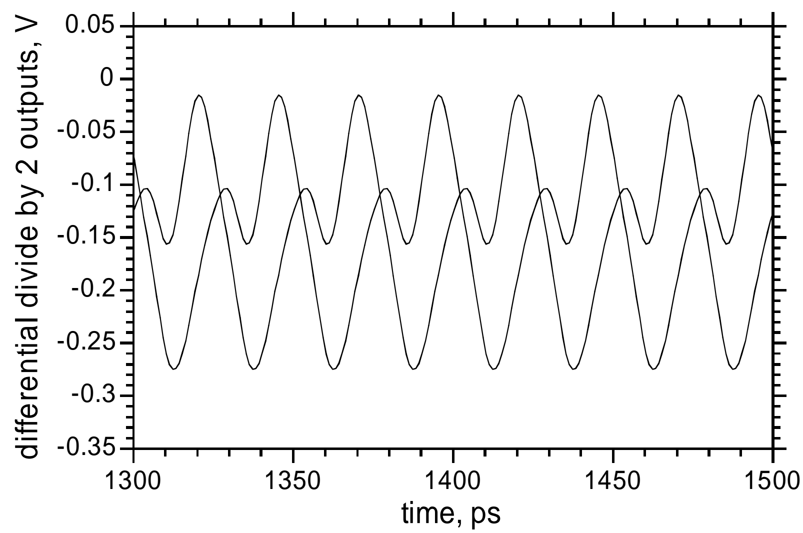


Figure 4.11: Simulated divide by 2 output of CML divider for a 35 GHz clock input.

sitic wiring capacitance and the thermal via capacitance of the HBTs and NiCr resistors. The clock signal in the CML static divider feeds through the collector-base capacitance of the off transistor in the lower stage and the emitter-base capacitance of the off transistor in the upper stage. The effect of this feed through is a component in the outputs, at the clock frequency. The simulated output waveform of the CML divider is shown in fig. 4.11. The divide by 2 frequency component and the clock feed through component can be seen in the simulated output of the CML divider.

4.5.2 CML static frequency divider results

Figs. 4.12 and 4.13 show the output waveforms of the CML static divider for clock frequency of 20 GHz and 47 GHz respectively. Stable divide by 2 operation is achieved in the entire band from 4 GHz to 47 GHz. The clock feed through component, which is at the clock frequency, is filtered out by the limited bandwidth of the measurement set-up. This low pass filtered clock component at the output of the circuit causes a negative shift in the output DC levels. The circuit dissipates about 75 mW of power from a 5 V supply. For clock frequency higher than 50 GHz the CML divider has a spurious divide by 4 output. This spurious divide by 4 operation is also seen in the SPICE simulations of the static divider at high clock frequency.

The measured peak clock frequency of the CML static divider is higher than the clock frequency of 35 GHz predicted from the SPICE simulation of this circuit. Devices in the CML circuits are operating in the linear region of the common emitter I-V characteristics, where the collector region is either undepleted or in base push-out domain depending on the collector current. The SPICE model used here does not predict the variation of device RF parameters with bias, in this bias range. Also, the hybrid-π model used for the time constant analysis is not an accurate description of the device in this regime. Therefore peak clock frequency of the CML static divider predicted from circuit simulations or the analytical model is not accurate.

4.6 ECL static frequency divider

The design of the ECL static frequency circuits is discussed in this section. The ECL dividers ar expected to operate at much higher clock speeds compared to the CML circuits. Hence layout parasitics and other high frequency

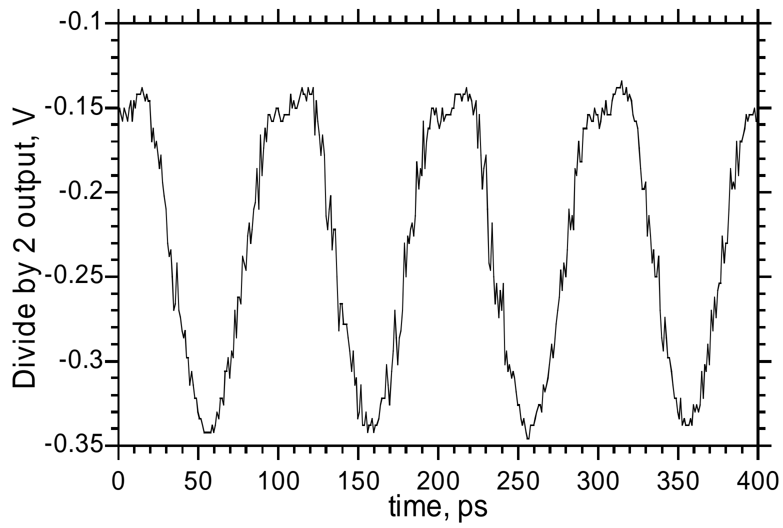


Figure 4.12: Output of CML static frequency divider for 20 GHz sinusoidal clock input.

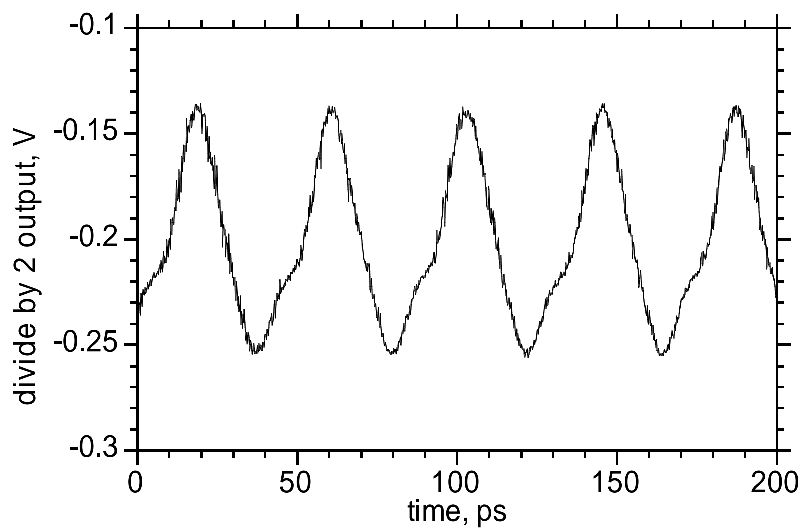


Figure 4.13: Output of CML static frequency divider for 47 GHz sinusoidal clock input.

effects have a be considered more carefully.

4.6.1 Circuit Design of ECL Static Dividers

Two versions of the ECL circuit were fabricated. The first version is implemented with single ended clock input, while capacitively grounding the other differential input on-wafer. Emitter-followers are added to the differential pairs on the upper level (fig. 4.14b). The lower differential pair is directly connected to the clock inputs without an emitter-follower buffer stage. SPICE simulation of this pseudo-ECL single ended I/O static frequency divider with 3 μm collector HBTs predicts a peak operating clock frequency of 65 GHz.

The current IC technology uses two metal layers, which are separated by a 4000 $\AA$ SiN dielectric layer. When wires in the layout cross each other, there is a parasitic crossover capacitance. Given the area of each crossover and the average number of overs on the collector lines of the upper level devices, we estimate an average crossover capacitance of 10 fF. The output pads add a parasitic capacitance of 15 fF each to the collector nodes on the output differential pair. The total parasitic capacitance C_p is therefore 25 fF. If the wiring parasitics and the thermal via capacitance is included, the peak clock frequency of ECL single-ended I/O static frequency divider (fig. 4.15a) with 3 μm collector HBTs drops from 65 GHz to 55 GHz. It is important to realize that the single-ended I/O static divider discussed here, is not a true ECL circuit as the lower switching pair is not driven through emitter followers. The peak clock speed of 55 GHz is less than that expected for a true ECL static divider.

In the second version, differential I/O ports are used. The differential I/O increases the number of I/O ports. A buffer stage is used to drive the clock inputs to the lower switching pairs (fig. 4.14a - this is a true ECL circuit with emitter follower buffers for every switching transistor. The circuit size, which is pad limited, is doubled (4.15b). In order to DC couple the clock inputs, HBTs connected as diodes are used for level shifting. Also an additional DC input port provides the positive supply voltage (+0.3 V) necessary to bias the emitter followers at V_{ce}= 1 V to 1.3 V instead of 0.7 V to 1 V. This circuit is fabricated with nominal 2 μm collector ECL HBTs. SPICE simulations indicate a peak clock frequency of 80 GHz without any layout parasitics. When layout parasitics are added, the peak

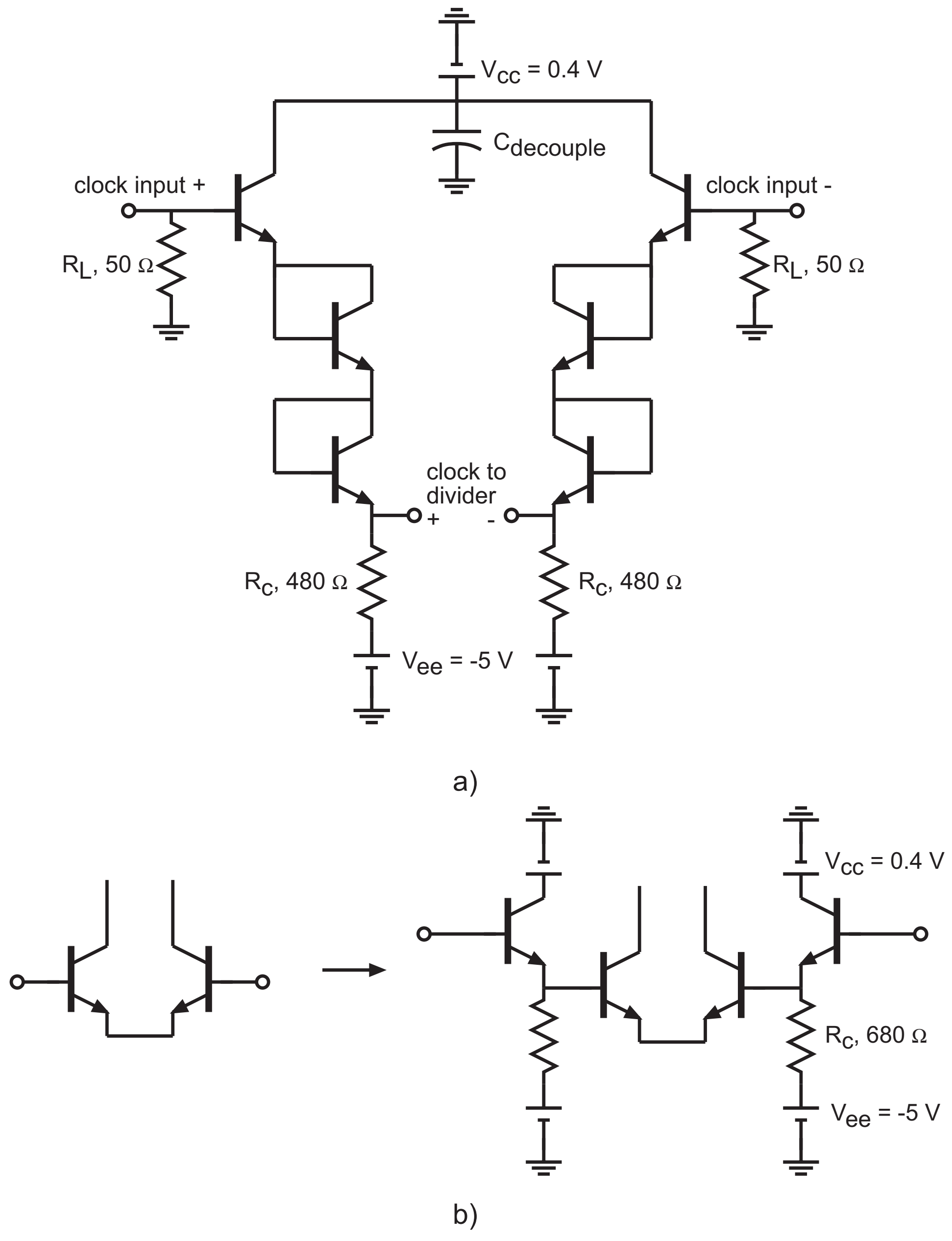
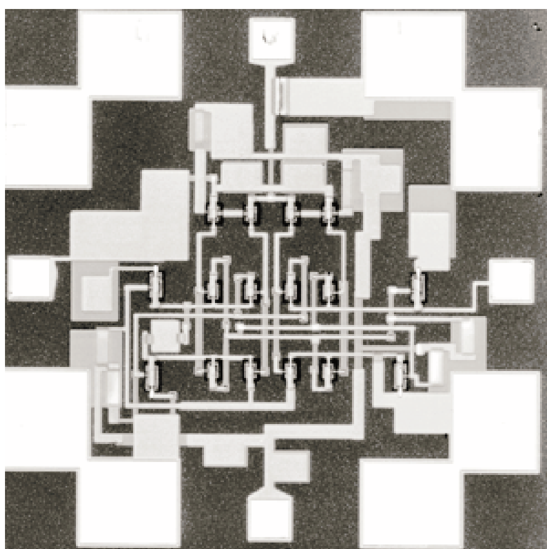
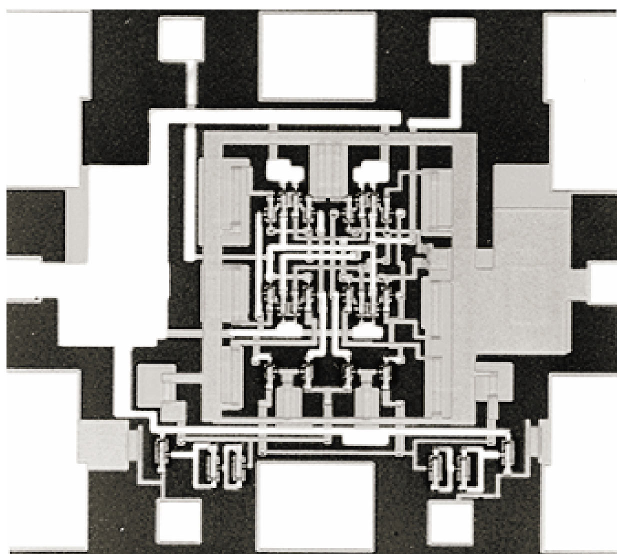


Figure 4.14: Circuit diagram for ECL 2:1 static divider. a) clock buffer stage b) emitter followers added to upper level switching differential pair



a)



b)

Figure 4.15: a) Single ended I/O ECL static frequency divider. b) Differential I/O ECL static frequency divider.

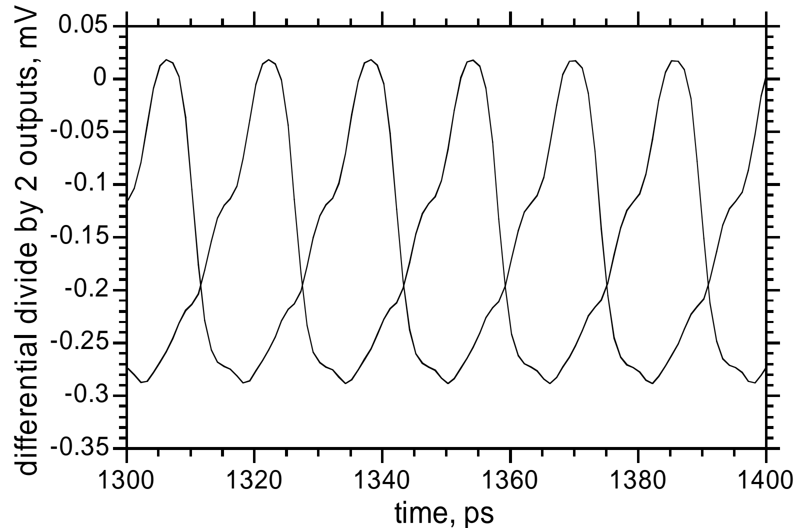


Figure 4.16: Simulated output of ECL divider for 65 GHz clock input.

clock frequency drops to 65 GHz. Time constant analysis predicts a peak clock frequency of 70 GHz for this circuit. Fig. 4.16 shows the simulated output waveforms of this circuit. The clock feed through, which adds a clock component to the outputs of the CML static divider, is eliminated by the emitter followers in the ECL divider.

4.6.2 ECL static frequency divider results

Figs. 4.17, 4.18 show the output waveforms of the fabricated ECL single-ended static frequency divider for clock frequency of 10 GHz, 43 GHz and 48 GHz respectively. Peak operating clock frequency is 48 GHz. The circuit dissipates about 350 mW of power from a 5 V supply. At high clock frequency the output voltage does not swing the full logic levels. This is due to the lack of a high gain buffer stage at output of the circuit. As in the CML divider, the ECL 2:1 divider also produces a spurious divide by 4 output for clock frequency in the range 50 GHz to 63 GHz.

SPICE simulations and the propagation delay analysis predicted a peak operating clock frequency of 55 GHz for this circuit. C_{cb} increases by more

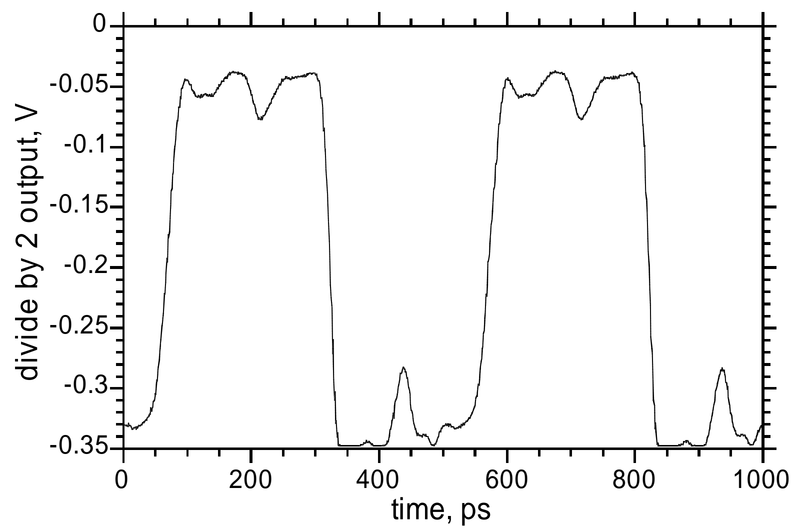


Figure 4.17: Divide by 2 output of single ended I/O ECL divider for 4 GHz clock input.

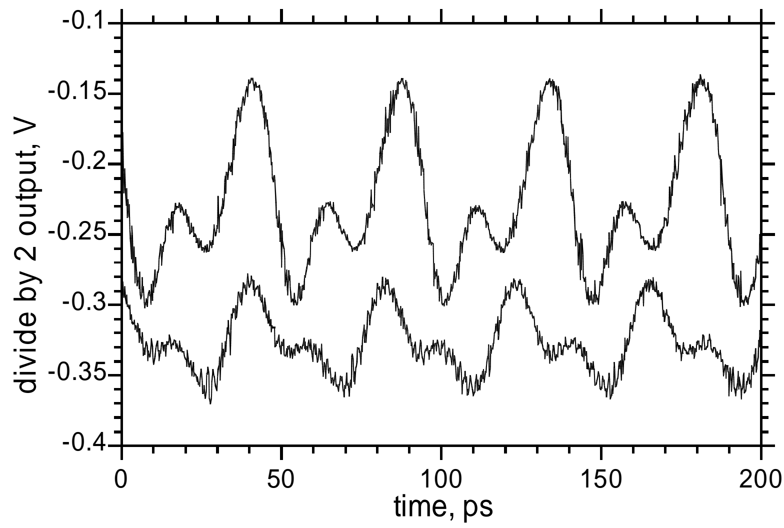


Figure 4.18: Divide by 2 output of single ended I/O ECL divider for 43 GHz and 48 GHz clock input.

than a factor of two from V_{cb} = 1.0 V to V_{cb} = 0.7 V, an effect which has not been included in the device models used for making these predictions. The measured peak operating clock frequency of 48 GHz for this circuit is as expected.

The minimum clock input power necessary for stable divide by 2 outputs is shown in fig. 4.19. The sensitivity is maximum at the resonant frequency of 32 GHz. At higher frequencies more input power is needed for faster switching. At low frequencies the sensitivity goes down for sinusoidal clock inputs. The rise time of the signal at the zero crossing is insufficient to switch the signal currents from the load to the latch state in a short time. This results in an ambiguous state in which the load and the latch stage are both partially on and fighting against each other. The problem is avoided by using square wave inputs with fast rising and falling edge.

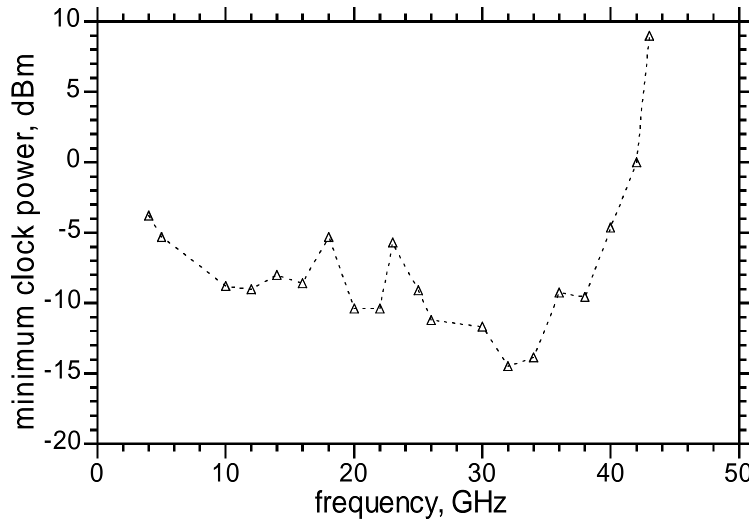


Figure 4.19: Minimum clock input power of ECL divider for divide by 2 operation.

The differential I/O static frequency divider is different from the single ended I/O static divider in two respects - the collector width is 2 μm instead of 3 μm and this circuit employs a clock buffer (fully ECL). The circuit

works up to a peak clock frequency of 48 GHz. Given the peak clock frequency of 70 GHz predicted from SPICE simulations of this circuit, the measured performance is disappointing. Also, the divide by 2 operation of this circuit over a range of clock inputs, from 5 GHz to 48 GHz, is very sensitive to DC bias conditions. The problem is probably due to ringing in the emitter followers of the clock buffer stage. Ringing was observed in the simulated outputs of the basic ECL gate. In a cascaded string of logic gates, if the gate switches before its inputs settle, an incorrect logic value is transmitted to the next gate.

The load seen by the emitter follower in the clock buffer is the sum of the input capacitance and the base resistance of the differential pair in the series gate. At the input of the emitter follower, this impedance will be transformed into a capacitance and a negative resistance. Given that the clock signal is provided through a 50 Ω source resistance, the negative resistance which occurs over a wide range of input frequency could potentially lead to oscillations or instability at a frequency determined by the parasitics. Some circuit techniques for reducing ringing at the output of the emitter followers have been suggested in section 5.2.

4.7 Comparison with SiGe static divider design

Static frequency dividers operating at 50 GHz have been reported using SiGe HBTs [15]. These circuits are fabricated in a technology with device f_t of only 100 GHz. The ratio of the maximum static divider frequency to device f_t achieved in the SiGe technology (0.5) is extremely high. In this section we try to understand the design and optimizations in the SiGe digital circuits.

Comparing the SiGe HBT with the transferred substrate HBT of the same area we find that the SiGe device has 3 : 1 higher C_{be} (from both τ_f and C_{je}), about 7 times higher C_{cb} and 3.5 : 1 lower R_b.

Device parameter	TSHBT $8 \times 0.6\ \mu m^2$	TSHBT $1\ \mu m^2$	SiGe HBT $0.14 \times 1.5\ \mu m^2$	SiGe HBT $1\ \mu m^2$
C_{je}	30 fF	6 fF	4 fF	19 fF
C_{cb}	12 fF	2.4 fF	3.6 fF	17 fF
R_b	30 Ω	150 Ω	210 Ω	44 Ω
R_{ex}	5 Ω	30 Ω	50 Ω	11 Ω
τ_f	0.5 ps	0.5 ps	1 ps	1 ps

In the SiGe design, the differential voltage swing is 800 mV, current is 2 mA and $R_L = 200\ \Omega$. We calculate the optimum current density using the ecl propagation delay expression from Section 4.3.3.

$$J_{opt} = 14.5\text{mA}/\mu\text{m}^2$$

In the SiGe design of [15] the current density of operation is 10 mA $/\mu$m^2, which is close to the optimum obtained from the propagation delay analysis. Multiple emitter followers are used in the SiGe design so that the switching transistors can be biased at V_{cb} exceeding 1.5 V. At this high V_{cb}, base push-out is suppressed by the large electric field in the collector. The SiGe devices can therefore operate at very high current density without degradation in RF performance. In these circuits, the design effort is focused at maximizing the speed by pushing the operating current density to a maximum. At lower current densities the $5R_LC_{cb}$ term in the ECL propagation delay expression (4.3.3) increases rapidly; this reduces clock speed.

Ignoring layout parasitics SPICE simulations and the propagation delay analysis predict that the static frequency dividers implemented with the transferred substrate InP HBTs can achieve a peak clock frequency of $\simeq$ 95 GHz. If ringing in the emitter followers of the ECL divider is eliminated, the peak clock frequency will be limited by the layout parasitics and the peak current density of operation. The ringing can be avoided with modifications in the circuit design and layout of the ECL gate (section 5.2). The parasitics can be eliminated by improving the process technology. The peak current density of operation can be increased either by epitaxial layer redesign or by using multiple emitter followers for higher V_{cb} as in the SiGe designs. Higher V_{cb} operation requires an improvement in the existing

breakdown voltage of the HBT. With these changes, the clock frequency to peak f_t ratio obtained in the transferred substrate HBTs will be $\simeq 0.5$.

From the optimum delay expression it can be seen that the propagation delay is a function of f_t, f_{max}, C_{be} and R_b of the transistor. C_{cb} in the current optimized transferred substrate design (4 fF) is low enough that the parasitic wiring capacitance will dominate. Most of the wiring capacitance for the current design is due the cross over between metal-1 and metal-2 layers. Technology development for future digital ICs should therefore focus on reducing the wiring parasitics in addition to device parasitics - C_{je}, τ_f and R_b. Deep submicron scaling accompanied with lateral device scaling will improve both f_t and R_b. C_{je} is more difficult to improve as it requires careful epitaxial design of the base-emitter junction. With improved R_b and f_t, the optimum current density for the deep sub-micron design will be higher. The HBTs will have to be designed to be able to operate at higher current density without base push-out. With these modifications, it should be possible to realize digital ICs operating at clock rates higher than 100 GHz.

Chapter 5

Conclusion

5.1 Summary of Achievements

HBTs with ultra-high bandwidth have been fabricated in the transferred-substrate process. Peak f_{max} exceeding 400 GHz has been achieved in the 'baseline HBT'. Other HBT designs have been optimized for performance in the voltage range of their operation in digital logic circuits. These devices employ an improved epitaxial layer structure and layout to increase f_t, while keeping f_{max} high. The ECL HBT has a peak $f_t = 220$ GHz and $f_{max} > 400$ GHz, while the CML HBT has peak $f_t = 207$ GHz and $f_{max} = 250$ GHz. The high f_{max} in the baseline and ECL HBTs is due to the low C_{cb} from the transferred substrate process.

Current mode logic (CML) and emitter coupled logic (ECL) flipflops connected as static 2:1 frequency dividers operate at a peak clock frequency of 47 GHz and 48 GHz respectively. While the performance of the CML circuit is expected, the ECL circuit performance is far below the peak clock frequency of 70 GHz predicted from spice simulations.

An integration level of 50 circuit components has been achieved. This includes HBTs, resistors and capacitors. Current process technology is capable yielding at least 100 component circuits with reasonable yield; the yield being limited only by the staggered alignment of emitters and collectors. Efficient HBT heat sinking in the integrated circuits has permitted high packing density and hence, reduced wire lengths. Microstrip wires fabricated on BCB provide a low capacitance and low loss wiring environment.The backside ground plane, which is only 5 μm away from the metal

wires on BCB, eliminates ground bounce on the IC and realizes ground connections with very small via inductance.

The old transfer substrate epoxy process was suitable only for building discrete devices. With that process as the starting point, a technology for medium scale integrated circuits has been developed. The technology has yielded HBTs with extremely high bandwidth, some analog circuits [26] and first digital ICs operating at clock rates approaching 50 GHz have been demonstrated. If sufficient time is devoted to developing better device models and circuit design strategies suitable for the transferred substrate technology, much better digital circuit performance than that achieved in this thesis work is possible. Given the high f_t and f_{max} of the HBTs and low parasitic microstrip wiring environment, analog and digital circuits for clock rates exceeding 100 GHz are feasible.

5.2 Suggestions for future IC designs

Performance of ECL static frequency dividers fabricated in this work does not correlate with the simulated circuit performance. The discrepancy can be attributed to errors in the device model or errors in the estimation of the layout parasitics. Improper design of the emitter followers results in ringing at their outputs. Spice simulations indicate that ringing can be a problem if base-collector capacitance is much smaller than the base-emitter capacitance. In the presence of ringing, circuit performance is unpredictable as incorrect digital logic levels are transmitted along a chain. The problem is more of faulty circuit performance rather than a reduction in switching speed. Such errors can be eliminated with more careful device modeling and circuit design techniques which render the circuit insensitive to small changes or errors in component values. One such technique to reduce ringing is a damping resistor between the outputs of the emitter followers in a ECL differential pair. The various methods to reduce ringing often result in a decrease in a pulse steepness and clock speed. Another method of reducing ringing without substantial loss of speed is to bias the emitter followers at a low DC current. The off-going emitter follower is switched off for a short time towards the end of the switching event, damping the response [38]. The emitter followers should not drive any transmission lines in the layout, as they provide a completely mismatched termination impedance. The wiring in the digital circuit should be driven by the load resistance of

the current switch pair. The load resistance (R_L) and the impedance of the transmission lines (Z_0) should be selected so that reflections are eliminated.

Input and output buffers reduce the effect of the pad and external parasitics on the performance of the critical core modules. Output buffers should be implemented with a differential current switching pair instead of emitter followers, as the output resistance of the current switch provides a better match for driving transmission lines. Emitter follower input buffers should be used only after careful consideration of the effect of driving source impedance, line inductance and pad parasitics.

Current levels of integration and yield are limited by optical contact lithography. With the stepper better alignment tolerances will increase the circuit yield, saving real estate on the wafer for more design variations of the same circuit. Circuit designs tweaks for increasing performance can then be tried. One such tweak to achieve 5 - 10 % speed improvement is inductive matching on the collector loads of the current switching pair. Another circuit technique for higher speed is to implement the current switch pair in the ECL circuit with a f_t doubler [39] stage. Such design techniques will be useful for small circuits like static frequency dividers. The increase in design complexity, transistor count and heat dissipation associated with these designs might render them unsuitable for more complex circuits like A/D converters.

5.3 Transferred substrate technology for future ICs

HBTs with lower saturation voltages should be designed so that good RF performance is maintained at low V_{ce}. This is critical for CML circuits as the devices operate at $V_{ce,min} = 0.4$ V. The saturation curves can be improved by reducing the collector thickness, so that the electric field at any given V_{ce} is higher. High electric field in the collector improves transistor performance at the base push-out limit (Kirk) and also aids in depleting the N- collector at low reverse bias voltage.

Reducing the collector N-thickness also improves the breakdown voltage at high currents by decreasing the number of thermally generated carriers in the space charge region. The breakdown voltage however, is limited by Zener tunneling to a maximum of $V_{ce} \sim 2$ V . More complex digital circuits

involving multiple circuit stages higher breakdown allows greater circuit design freedom. Breakdown voltage higher than 2 V will be obtained only if the InGaAs collector is substituted with an InP collector.

The propagation delay analysis suggests that the optimum current density for the CML logic gate is greater than 5 $\times 10^5$ A/cm^2. About 35 % improvement in the switching speed of CML logic is obtained by operating the transistor at 5 $\times 10^5 A/\text{cm}^2$ instead of 1 $\times 10^5$ A/cm^2. CML has several advantages compared to ECL - design simplicity, smaller transistor count and lower power dissipation. If CML is to be used for large digital circuits without significant speed degradation, the HBTs should be able to operate at very high current density. The issues regarding breakdown voltage and Kirk effect at very high current densities should be addressed.

R_b and τ_f can be improved by deep submicron scaling [40] and lateral scaling of the transistor epitaxial layers [41] respectively. As τ_f is reduced, C_{je} limits the switching speed of digital logic gates. C_{je} can be reduced by careful design of the base-emitter junction [42]. Carbon doping [43] in the base is currently being pursued to permit higher base doping and greater long term reliability of the HBTs. As the diffusion coefficient of carbon is orders of magnitude less than that of beryllium, greater control of the doping profile in the emitter-base grade can be obtained.

Plated copper substrates [27] will soon replace the solder and the GaAs carrier wafer. The backside ground plane should ease IC packaging requirements. Superior heat sinking of the HBTs due to the excellent thermal conductivity of copper will permit higher current density operation and higher levels of integration.