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InP HBT Power Amplifier MMICs toward 0.4W at 220GHz

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requirements for the degree Doctor of Philosophy

in Electrical and Computer Engineering

by

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March 2013

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March 2013

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ABSTRACT

InP HBT Power Amplifier MMICs toward 0.4W at 220GHz

by

Thomas Benjamin Reed

RF power amplification above 200GHz has become more critical as higher frequency bands are sought for radar and space applications. At 220GHz, a low-loss free-space propagation window is very alluring for potential systems, however, a single transistor cannot produce sufficient output power requisite for a wireless system. This work demonstrates solid-state power amplifier MMICs targeting up to 0.4W at 220GHz.

Power amplifier cells are designed using four 6μm-long common emitter and common base InP HBTs to form a cascode. Single InP HBTs with 250nm-wide emitters and have shown a peak f_{MAX} of 700GHz and peak f_T of 400GHz. The cascode cell shows above 15dB of small signal available gain at 220GHz. Non-inverted microstrip IC interconnects shield the InP substrate and provide a low-loss environment for impedance tuning and power combining. Multiple levels of power combining are performed on wafer to reach a high overall saturated output power at 220GHz. Experiments were designed to find the limits of transistor density, the optimal Class A load line, the optimal number of power combining levels and gain stages, the maximum physical size, and the maximum possible DC power consumption at the IC level.

In the first attempt, a 4-Cell SSPA was reported to have 48.8mW of saturated output power at 220GHz with a compressed gain of 4.5dB. On a second maskset, a

2-stage, 8-Cell SSPA had 90mW of saturated 220GHz output power at 8.2dB of compressed gain. A third set of designs demonstrates a 4x increase in output HBT periphery over the 8-Cell SSPAs in Tapeouts 1 and 2. In full-thickness RF power measurements, 180mW of saturated power was observed at 214GHz when air cooled. When heat removal by wafer thinning and mounting is complete, power levels may be close to the 400mW shown in simulation.

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1
Introduction to SSPA Design

1-A INTRODUCTION

Extremely high frequency (30GHz to 300GHz) and far-infrared (300GHz to 3THz) electronics have been an area of high interest for many because of new transistor process technologies that can operate at those frequencies in the fundamental harmonic. Previous access to these frequencies was only possible through harmonic generation: A lower-frequency power amplifier produces a large output power and then a fraction of that power is converted into a high frequency signal through a frequency multiplier circuit. By using the frequency multiplier, however, the designer pays a significant toll in linearity, signal-to-noise ratio, and power-added efficiency.

With the maturing of higher frequency device processes, including the scaled InP DHBT, power amplification at high frequency has been made possible [1]. Fundamental tone circuits, including power amplifiers can now be designed and fabricated at these higher frequencies. As a result, systems requiring high power, linearity, SNR, and PAE can be considered. Even higher frequencies can then be accessed using harmonic frequency multipliation. The frontier of frequency can again be pushed higher

than before.

This pursuit is not solely for the breaking of records. Real systems are currently being researched that can demonstrate the usefulness of circuits above currently ubiquitous microwave/RF frequencies. Many of these circuits target low-loss free-space propagation windows located around 96GHz, 220GHz, 340GHz, and 670GHz, among others. These are local minima for free-space propagation losses due to absorption by common molecules in our atmosphere including H20 and O2 [2].

Future synthetic aperture radars and high resolution imaging systems will benefit greatly from continued development of solid state power amplifiers at these target frequencies. Efforts to increase the saturated power at 220GHz have been increasingly active. High power signals at 220GHz can be used to drive multiplier chains for THz applications or drive higher power vacuum tube amplifiers at the fundamental frequency [3]. Multiple power amplifier (PA) monolithic millimeter-wave integrated circuits (MMICs) can be mounted as pixels to form a high-powered array for radar systems. Many of these wireless applications will require additional output power at 220GHz to overcome attenuation due to weather events including heavy rain, humidity, dust storms, or fog.

1-B DESIGN CHALLENGES AT 220 GHZ

Although 220GHz may be a local minimum for atmospheric absorption, this value is added onto already high signal attenuation caused by the spreading of electromagnetic energy in free space. The Friis formula shows that the magnitude of a received

signal after travelling through free space decreases as the square of range and also as the square of frequency [4].

This loss is a dominant factor in determining the minimum output power for a demonstration system. The amount of power necessary for a system at 220GHz can vary depending on system specifications—like range, antenna gain, bandwidth, and LNA noise factor. A simple communication system example can be illustrative of what the power requirements are at this frequency.

In a communications example, a 1Gbps wireless link is devised. With the right coding algorithm, a 3dB signal-to-noise ratio can be sufficient to extract data. A current status update on low-noise amplifiers (LNAs) showed that LNAs from 210-280GHz showed noise figures ranging from 7.5-11.5dB [5]. If a noise figure of 10dB is used in the example, the minimum received power at the receiver would be -70.8dBm.

$$\frac{P_{rec}}{P_t} = \alpha_{atm} G_t G_r \left(\frac{\lambda}{4\pi R} \right)^2 = -1dB + 20dBi + 20dBi - 139dB = -100dB$$

Eq. 1. Friis Transmission Formula

Solving for the free-space signal attenuation can lead to a minimum transmitted power. For the example, a range of 300m at 220GHz, Tx/Rx antennas with 20dB antenna gain, and an atmospheric absorption of 3.3dB/km are selected. As a result, the absorption loss is 1dB and the free-space power spreading results in 139dB of signal loss. The result is a minimum transmitted power of 29.2dB or 0.83W.

$$P_{rec,\min} = kTFBQ^2$$
$$P_{rec,\min} = -173.8dBm / Hz + 10dB(NF) + 90dB(1Gbps) + 3dB(Q^2) = -70.8dBm$$

Eq. 2. Wireless System Power Budget

This example illustrates that for systems at 220GHz, significant range can be used for this wireless system given that enough power can be generated. For a radar system, the usable range would at best be half that of the communication system example and lower for non-100% reflection of power. In either case, high minimum power requirements can only be met by increased development of power amplification at this frequency.

Apart from the high system power requirements at 220GHz, there are limitations to the potential gain and output power at the IC level. For a PA cell to have appreciable gain and output power at 220GHz, the transistor finger count and length will be limited by issues associated with device self-heating and interconnect parasitics of the multi-finger device [6]. At these frequencies, higher output power is achieved through on-wafer power combining. Careful design of the combiner is necessary to avoid excessive skin-effect loss; no significant increase in output power can come from combining if the insertion loss exceeds 1.5dB for a two-to-one power combiner.

Power amplifiers also struggle because the load tuning impedance for highest output power is almost never a “matched” impedance. Although high power generation may be occurring at the current source of the transistor, a percentage of that power may never be transferred to the load. This reduces the overall gain and output

power of the amplifier. Mismatched impedances increase the risk of standing waves, flow of power into other undesirable spurs, and waveform distortion.

1-C NOTEWORTHY RESULTS

A noteable high-output power, solid-state, G-band (140-220 GHz) power amplifier is a sub-50nm InP HEMT amplifier having 75mW of saturated output power at 210 GHz in a waveguide-block package. The amplifier MMIC is designed with two side-by-side amplifiers with four common source stages. Each amplifier stage splits to and combines power from four HEMTs. Each of the eight total output HEMTs have a gate length of 120um. This design was done using a coplanar waveguide interconnect environment [7].

However, the work described in this dissertation uses InP HBTs. An early G-band medium power amplifier using InP HBTs produced greater than 8mW saturated output power at 190 GHz [8]. 300 GHz medium power amplifiers have been reported using 256-nm InP HBTs [9].

While 250nm InP DHBTs have much higher off-state breakdown compared to state-of-the-art InP HEMTs [10, 11], the usable voltage swing and current swing on the IV-plane (where MAG/MSG is appreciable) is similar. A closer examination of the MAG/MSG of a cascode cell formed with these technologies at high-mm-wave frequencies shows that the InP HBT cell yields more dB of gain compared to its InP HEMT counterpart.

For demonstration of a power amplifier at these same frequencies, low-loss

interconnects are essential. The use of a multi-layer, thin-film, substrate-shielded non-inverted microstrip environment using low-loss BCB (εr = 2.7) available in the InP HBT processes allows very compact PA cells and combiner networks to be formed. These networks have much lower loss compared to similar networks formed in grounded coplanar waveguide (G-CPW) on thinned InP substrates, used in InP HEMT processes.

Power combining with multiple gate or emitter fingers is necessary for high saturated output power. On-wafer 4:1 and 2:1 power combiners have been demonstrated in a microstrip wiring environment at 95 GHz resulting in 427-mW of output power in a HEMT power amplifier [12]. 4-1 combiners at 220GHz were realized with similar Dolph-Chebyshev structures using coplanar waveguide in the 75mW amplifier reported above [6]. Additionally, a 206-294GHz mHEMT amplifier has been demonstrated using an identical non-inverted, shielded, thin-film microstrip environment with dense interconnect vias as the amplifiers reported here [13].

For a more complete coverage of all the power amplifier and low noise amplifier results, a recent Samoska paper may be consulted [5]. Amplifier power density (Watts per millimeter of transistor output periphery) are also reported in the Samoska paper.

1-D NOVEL METHODS IN 220GHZ PA DESIGN

Taking the previous work and design challenges into consideration, this work shows that with correctly sized HBTs, care can be taken to model interconnect parasitics

within each power amplfier cell. Multiple modular cells can then be placed in parallel and power combined for a large overall power.

Rather than using a single-transistor amplifier in each PA Cell, an ac-coupled cascode was designed using a 4x6μm-long common emitter HBT and a 4x6μm-long common base HBT to provide high maximum available/stable gain (MAG/MSG) and high power handling at 220GHz. Interconnects, tuning networks, and DC chokes are modeled individually and collectively using a 2.5-D EM simulator to take into account openings in the ground plane, parasitic capacitances, and any inductive coupling behavior. Power combiners in low-loss thin-film microstrip have been demonstrated using a Dolph-Chebyshev structure for 4:1 combining/splitting and a quarter-wave structure for 2:1 combining. Power supply simulation revealed potential instabilities in the RF circuit and those design weaknesses were mitigated by RF stabilization of the power supply feeds.

Using this approach, state-of-the-art ICs were demonstrated. A 4-Cell amplifier with 48.8mW of output power at 220GHz was measured with first pass design success. A 4.5dB compressed gain was measured at that power level. This MMIC had an S21 of 10.1dB at 220GHz and a 3dB bandwidth from 206 to 254GHz. Its DC power consumption was 1.1W [14]. An 8-Cell PA on the same maskset could not be driven fully into compression, but did show 58.4mW of output power. The S21 of this PA MMIC was 8.9dB at 220GHz and the DC consumption was 2.2W [15].

In a second tapeout, multi-cell PA MMICs were fabricated using similarly

sized output amplifier stages. Additional gain stages were added to decrease the power requirements of the RF source used in power testing. An 8-cell, 2-stage amplifier showed 90mW of output power at 220GHz at 8.2dB compressed gain [16]. It had an S21 of 14.8dB at 220GHz and a DC power consumption of 4.46 W. In addition a 4-Cell, 3-Stage amplifier showed an S21 of 26.8dB at a DC power consumption of 3.38W. This design had an output power of 55.5mW at 220GHz with 17dB gain [17].

The third tapeout sought to increase power density in the PA Cells and increase the number of power combining levels. A PA Cell with 8x6μm HBTs was designed using a novel 3-port output power tuning network. One PA uses 16 of these new PA Cells in the output stage for an overall 4x increase in HBT output periphery. The 3-stage amplifier was designed to target 400mW output power at a gain of 17dB. In initial full-thickness substrate tests, the PA MMIC (2.2mm x 2.5mm) biases properly with a total DC power consumption of 11W and an S21 of 9.9dB in the first lot was below simulated estimates. The lower gain is due to insufficient heat dissipation of the full-thickness DUT. Full-thickness power measurements with forced air cooling showed a drastically higher gain and output power. The largest amplifier showed 180mW of saturated output power at 214GHz with cooling.

1-E INP HBT TECHNOLOGY DESCRIPTION

Indium Phosphide (InP) is a III-V semiconductor material that has been of research interest because of its low effective mass and potential for very high velocity electron transport. Heterojunction Bipolar Transistor (HBT) technology has historically been a

transistor type used to maximize the transition frequency (f_T) and maximum frequency of oscillation (f_{MAX}) and is common for RF PAs in other material systems including GaAs. Device high frequency operation is limited by the transit time for an electron to travel through the base and collector of the transistor. Capacitor charging time constants associated with access resistances and parasitic capacitances—caused by depletion, diffusion, and electric field across bulk semiconductor—also have a strong effect on f_T and f_{MAX} as shown in the formulas below [18].

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_{bb} C_{cbi}}} \qquad f_T = \frac{g_m}{2\pi(C_{be} + C_{cbi})}$$

Eq. 3. f_{MAX} and f_T for an HBT small signal model

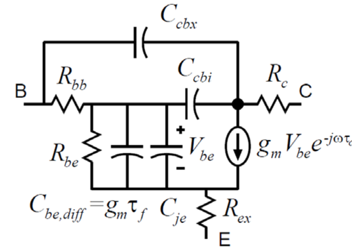


Fig. 1. HBT Small Signal Model. Mark Rodwell

Many of the developments in the InP HBT at UCSB in Mark Rodwell's group have followed a desire to reduce the transit time within the HBT by scaling base and collector thicknesses and seeking to reduce the parasitic resistances and capacitances through major materials efforts and lateral device scaling [1]. The time constants associated with transit and capacitor charging are the factors that determine a transistor's maximum oscillation frequency. Miguel Urteaga and Zach Griffith demonstrated the 250nm InP HBT technology at UCSB with f_{MAX} over 400GHz [19, 20]. Later, Ashish Baraskar demonstrated the reductions in base contact resistance that would be necessary to reach above 1 THz f_{MAX} [21]. Vibhor Jain demonstrated a 220nm InP HBT technology generation with an f_T of 480GHz and f_{MAX} of 1.0 THz [22].

According to Mark Rodwell's transistor scaling roadmap [1], in order to get even faster transistors, further reduction of access and contact resistances must occur.

UCSB Technology Description

Work done within the University of California, Santa Barbara cleanroom in InP HBT research (Mark Rodwell Group) is done mostly with the purpose of achieving very high frequency transistors. The focus of masksets in the UCSB process is to create scaled transistors and little else—to facilitate faster processing, measurement, and improvement to subsequent transistors. Limited space is granted to circuit designers in these very experimental processes for circuit design (see Appendix 1). Even with space for circuits, only an ideal physics transistor model exists for circuit simulation of this experimental device process. This model is based solely on the ideal physical structures found in the HBT—e.g. collector thickness and corresponding InP electrical permittivity for C_{CB}. This model's value is limited for an experimental process because, materials within the device, their physical size, shape, and relative position are highly variable in processing.

A full IC process for the UCSB designs include transistors, a thin Au film (0.2-0.3μm-thick) parallel to the InP substrate at the level of the collector (Coll MET) used as a ground plane, and a 0.8-1.0μm-thick layer of Au (MET 1) that can be placed to contact the emitter metal. A 0.8-1μm-thick layer of BCB (Er=2.7) is used as a dielectric layer between Coll MET and MET 1. In design work, it is convenient to use MET 1 as a signal interconnect for microstrip transmission lines. No resistors or capacitors are available in this process.

Given the challenges associated with using the UCSB process for circuit design, it has the potential to be an extremely high speed process. Most recent reported

data shows that f_{MAX} of these transistors has reached above 1 THz [22].

Teledyne Technology Description

Apart from UCSB's research laboratories, more mature InP HBT processes exist that make high-transistor-count InP circuits more feasible. The work described in this dissertation was brought about primarily using IC tapeouts at Teledyne Scientific Company, located in Thousand Oaks, CA. Many of the processes which Teledyne has perfected were born in the labs of UCSB, Rodwell, and his former Ph.D. students.

For the majority of design work done for this dissertation project, the Teledyne 250nm InP HBT process was used. The HBT has a breakdown voltage of 4.5V. The integrated circuit technology features single InP HBTs that have peak f_T of 400GHz and f_{MAX} of 700GHz. However, transistor gain, f_T, and f_{MAX} vary strongly with Quiescent bias point. Typically, current densities near the kirk current and base-collector voltages just above the knee voltage result in the highest transistor f_T/f_{MAX} for these transistors.

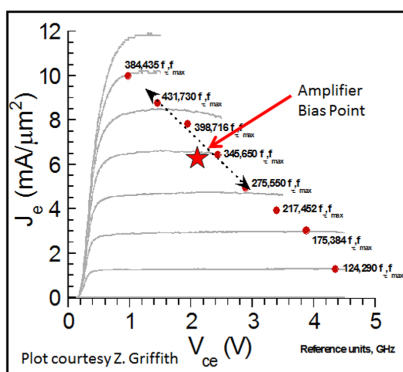


Fig. 2. Plot of f_T and f_{MAX} vs. bias point of the HBT

Data taken from a UCSB 250nm InP HBT [Z. Griffith, et al., "Z. Griffith, E. Lind, M. Rodwell, Xiao-Ming Fang, D. Loubychev, Ying Wu, J. Fastenau, A. Liu, "Sub-300 nm InGaAs/InP Type-I DHBTs with a 150 nm collector, 30 nm base demonstrating 755 GHz f_{MAX} and 416 GHz f_T," *Indium Phosphide & Related Materials, IEEE 19th Annual Conference on*, pp.403,406, 14-18 May 2007].

New transistor device layouts were also developed at Teledyne for use in PA design for this project. Using longer HBTs or multi-finger HBTs, a much higher total

current and higher maximum RF power can be realized versus a single short device optimized for high frequency performance. For HBTs longer than 6um, parasitic base feed inductance and resistance causes significant degradation in maximum available gain for a single transistor. As a result, multi-finger HBTs were developed for larger RF power handling. The trade-off in device layout centers in the compactness of the multi-finger layout versus transistor self-heating. A more compact cell has reduced parasitic inductance, resistance, and phase difference associated with the routing signal to all the bases, emitters, and collectors of the multi-finger device [6].

With a compact HBT layout, there is more dc power consumption per unit area. Self-heating effects can drastically reduce the transistor gain. In work done by Z. Griffith at Teledyne, various types of multi finger devices were laid out and tested. As a result of his work, a 4-finger HBT was created with 4 single-sided HBTs each with 6μm emitters. This device was selected for PA MMICs because it maintained a level of high frequency performance at 220 GHz that was comparable to the performance of a single finger HBT. A single common-emitter HBT (CE) shows a f_T=350GHz and f_{MAX}=590GHz at the amplifier's quiescent bias point of Je=5.5mA/μm^2 and a Vce=1.8V. In comparison, The 4-finger HBT as described had f_T=333GHz and f_{MAX}=530GHz under the same bias conditions. This shows that the parasitics associated with using the multi-finger HBT does little to decrease the available gain at 220GHz in PA designs. For PA design, both a common emitter and common base 4-finger HBT were developed. The physical size of the CE device was 18x7.5μm^2. The physical size of the CB device was 6x9μm^2 [6].

Development of this process technology has resulted in a designer's guide containing design rules to increase device and circuit yield. As the technology has evolved, the process has featured a 3- or 4-layer Au interconnect stack depending on the desires of the customer and the end use of the circuits being designed. Metal layers in the interconnect stack can flexibly be used for transmission lines, grounding, or power supply. For a 1μm thick metal interconnect, the maximum supported current density is 5mA/um. For the PA interconnects, the MMIC process had 4 metal layers not including the thin collector metal layer (CMET). During the first iteration of designs, all four metal layers were 1μm thick with 1μm of BCB (Er=2.7) between each layer. The result was a maximum microstrip transmission line dielectric height of 5um. In subsequent runs of the PA designs, Teledyne provided a thicker 3μm MET 4 layer to allow for greater current flow to the design under test for the same width of power supply line.

NiCr resistors are available on the collector metal layer at 50ohm/square. The thickness of the resulting NiCr layer is quite small (.02um). The resistors are limited to 1mA/μm of width, but have been shown to handle higher current densities. Capacitors are available in the process between the MET 1 and MET 2 layers in the process. A thin layer (0.2um) of Silicon Nitride is deposited with another layer of Au above it. A via connects the top CAPM layer to MET 2. The result is a capacitor that can be designed with 0.3 fF/μm^2. A very convenient capacitor to ground with few parasitic effects beyond 220GHz can be generated When MET1 is selected as a ground plane and MET2 is used to access the top capacitor metal layer.

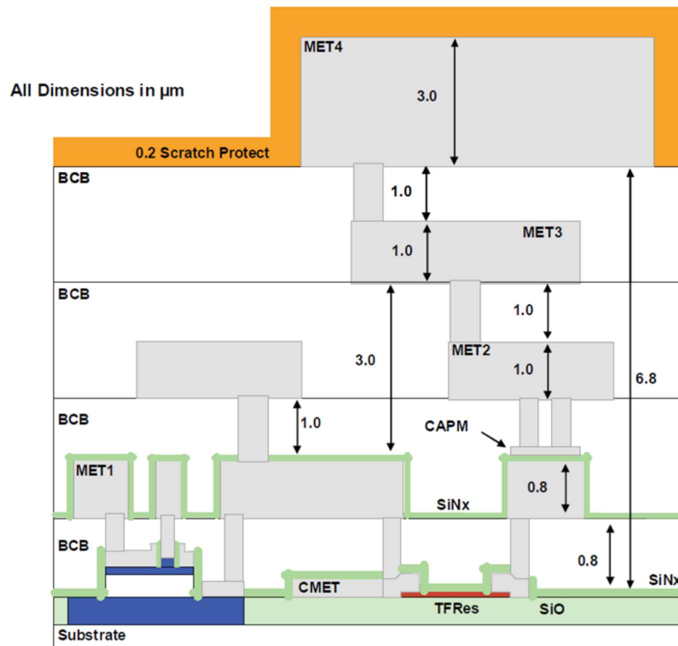


Fig. 3. HiFIVE Interconnect Stack for PA Design.

[Z. Griffith, M. Urteaga, R. Pierson, P. Rowell, M. Rodwell, B. Brar, “A 204.8GHz Static Divide-by-8 Frequency Divider in 250nm InP HBT,” *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2010 IEEE*, pp.1-4, 3-6 Oct. 2010.]

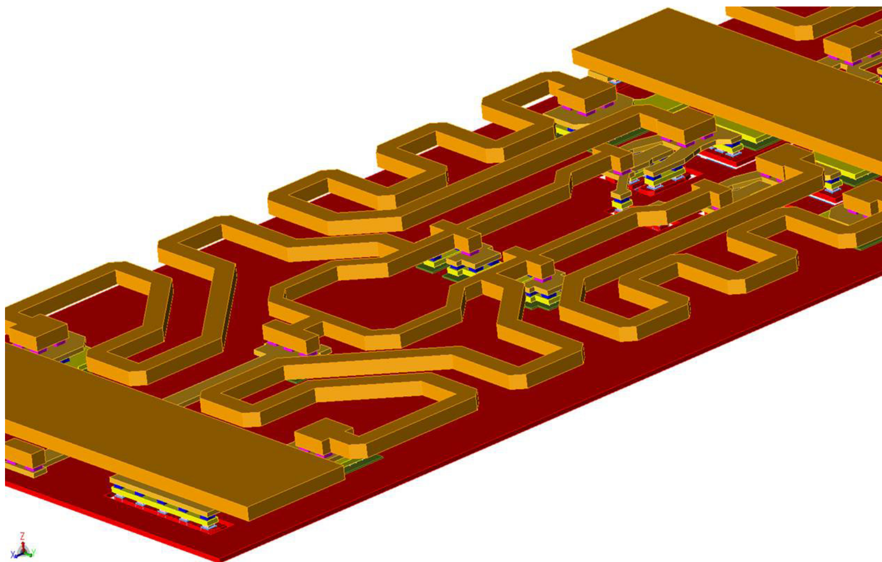


Fig. 4. ADS 3-D Rendering of Tapeout 3 PA Cell with two 4x6µm HBTs

2.1
Microwave Power Amplifier Design

2.1-A LINEAR AMPLFIERS

When speaking with colleagues in other disciplines about amplifiers, I simply describe an amplifier as a system where upon putting in a signal, you get the same signal out, just larger. Audio amplifiers connected to microphones and speakers are a much more palpable example (versus high frequency amplifiers) for non-engineers. Someone speaks at one level and a much louder sound comes out.

Like most things, amplifiers also have limitations. The most significant limit for an amplifier is the range of power levels within which it can operate as a linear amplifier [23]. Suppose you have two signals. When put through a system, each input results in a unique output. A linear system is one in which the system performs operation such that if any linear combination of those two signals is input into the system, then the output is the linear combination of the two individual outputs. This is shown below:

$$f(Ax + By) = Af(x) + Bf(y)$$

Eq. 4. Linear Combinations

Linear amplification allows designers to enlarge a signal without distorting it. An amplifier's linear range is bounded at low and high power. The linear limit of an amplifier at low input powers is the minimum detectable signal above the amplifier's input noise floor.

The upper limit on amplifier linearity has to do with the maximum amount of voltages and currents that can be generated by the amplifier. If driven with larger RF input power, no gain in RF ouptut power will be shown. This roll-off in output power is called gain compression because the gain is reduced to zero as more power is applied to the input. There are two ways to quantify this gain compression effect. The maximum power observed as a plateau in P_{OUT} vs. P_{IN} is called the saturated output power. When signals are fully compressed, other non-linear effects can cause significant distortion to communication signals. Many engineers value a different statistic called the 1dB-compression point. This is the output power level where the gain has dropped by 1dB from the small signal level.

Besides gain compression, there are other large-signal distortion effects that can be important in amplifier design for communication systems. When two or more nearby tones are sent through any system with nonlinearities (including amplifiers, mixers, etc.), the system generates harmonics of the individual fundamental tones and sum and differences of the two frequencies. The third order difference frequencies lay close enough to the signals of interest that they can't be filtered out in typical systems and can cause signal distortion.

The third-order term in the output signal is usually not significant relative to

the rest of the signal under small signal conditions because it has a small Taylor series coefficient. Being a cubic (x^3) term, the power level (in dB) increases three times faster than the linear or fundamental output term (x^1). This means that at a given power level, the third order term and the first order term will be equivalent in power level. The input power level at which these two terms have equal power levels is considered the Third Order Intermodulation Intercept Point (IIP3).

In practice, the amplifier is in heavy gain compression much before the third-order signal gets anywhere near the power level of the fundamental signal. To get a value of IIP3, the $P_{OUT}1$ and $P_{OUT}3$ versus P_{IN} can be observed in the amplifier's linear range. The trends for $P_{OUT}1$ and $P_{OUT}3$ can be extrapolated so that an intercept point can be found.

For the amplifiers reported in the academic literature, the way power amplifier statistics are reported varies. For circuits up to 67GHz, it is common to see noise figure, IIP3, P1dB, and saturated output power. For higher frequencies including 220GHz, noise figure and IIP3 are often omitted because of the complexity of creating a proper test bench for such measurements. Currently available measurement systems above 67GHz are expensive, rare, and often lack sufficient dynamic range to give reliable data. However, it seems likely that new generations of spectrum analyzers and signal generators reaching up to 220GHz may come soon.

2.1-B TRANSISTOR AMPLIFIER TOPOLOGIES

From what are high frequency amplifiers constructed?

Designing amplifiers with highly scaled transistors is an effective way to achieve RF amplification at high frequency. The technology used for the amplifiers reported here is described in depth in the InP HBT technology section of this dissertation. A standard transistor is a three port device. In a common transistor amplifier configuration, one of the ports is used as an AC ground reference, another is used as an RF output current source, while the third port is an RF input that controls that current source [24]. Device operation for amplifiers usually has the base-emitter junction forward biased to control current flow while the base-collector junction reverse biased to act as a current source. Three common single transistor amplifiers are shown below:

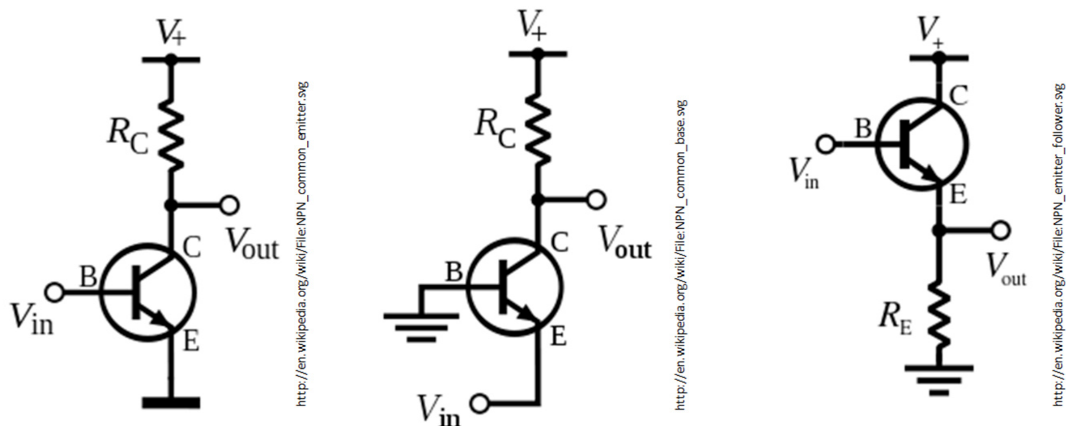


Fig. 5. Single Transistor Amplifier Topologies: Common Emitter, Common Base, and Emitter Follower

When biased and supplied with an RF input signal, the common emitter amplifier acts as a trans-conductance amplifier meaning an RF Input voltage results in an

RF current swing. The common base is a voltage gain amplifier, meaning the RF current flowing from input to output is constant while voltage swing increases from input and output. The common collector (also known as an emitter follower) is a current gain amplifier.

	Voltage Gain	**Input Resistance**	**Output Resistance**
Common Emitter	$-g_m*R_c$	$R_\pi=\beta/g_m$	R_c
Common Base	g_m*R_c	$1/g_m$	$R_c\|\|r_{out}$
Emitter Follower	1	$\beta*R_E$	$1/g_m$

Fig. 6. Table of Voltage Gain, Input Resistance, and Output Resistance for Amplifier Topologies

In linear amplifiers, transistors act as an energy conversion device. DC power is converted into RF power proportional to the RF input signal. The drain efficiency is a ratio of RF output power to DC power consumption in the circuit. Similarly, the power added efficiency (PAE), is the RF output power minus RF input power all divided by the DC power consumption.

Apart from single transistor amplifier configurations, other multi-transistor amplifiers are possible. One very common topology for high gain and bandwidth is a cascode amplifier.

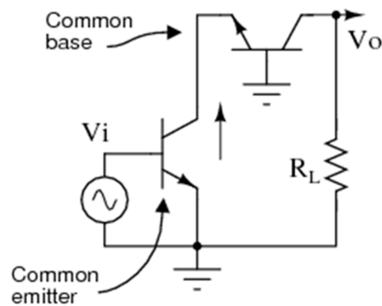


Fig. 7. Diagram of a Cascode Amplifier

A cascode amplifier as a two or more transistor amplifier topology has the benefit of two gain stages in row including a transconductance stage and a voltage gain stage that can result in a higher overall output impedance than a common emitter alone. Cascodes also have great input-output isolation which makes RF matching network design a more straight-forward effort at high frequency. However, the large available gain at high frequency could also result in potential instabilities over large RF bandwidths. The gain of a cascode amplifier is shown below:

Other amplifier topologies exist (e.g. a Cherry-Hooper amplifier) but such amplifiers require a large number of transistors that are to be connected in close proximity. This makes routing signals to each transistor with low parasistics tricky. Also, introducing many transistors in a small area can incur a penalty with grounding the circuit at high frequency. Selection of a low-metal layer ground plane will result in many holes in that plane and impede the flow of ground return currents. A high-metal layer ground plane selection will incur added resistance and inductance for grounding through vias.

2.1-C BANDWIDTH CONSIDERATIONS AND PARASITICS

Amplifier design can take different forms depending on what frequency of operation is desired relative to the maximum frequency of oscillation of the transistor. Near the flat band of gain for a transistor, closed loop transfer function theory, compensation, and feedback can be used to extend the bandwidth of the amplifier and achieve gains near the beta or gm of the transistor.

At frequencies near f_{MAX}, device capacitances become increasingly more significant. At these frequencies, gain slopes that drop 20dB per decade have had more than a decade drop from its 3dB bandwidth for InP HBTs. An unmatched transistor will likely have an S21 gain less than 0dB as frequency approaches f_{MAX}, meaning that if no tuning techniques are applied to the transistor's ports, it will not act as an amplifier at all.

At high frequency, "microwave" techniques can be used to achieve the maximum available or stable gain of the transistor amplifier. For frequencies below f_{MAX}, the MAG/MSG is greater than zero for common emitter and common base transistors. MAG is the term for the maximum gain possible at a given frequency given that the amplifier is unconditionally stable. MSG is the term for the maximum gain possible for a potentially unstable amplifier after it has been stabilized or made unconditionally stable.

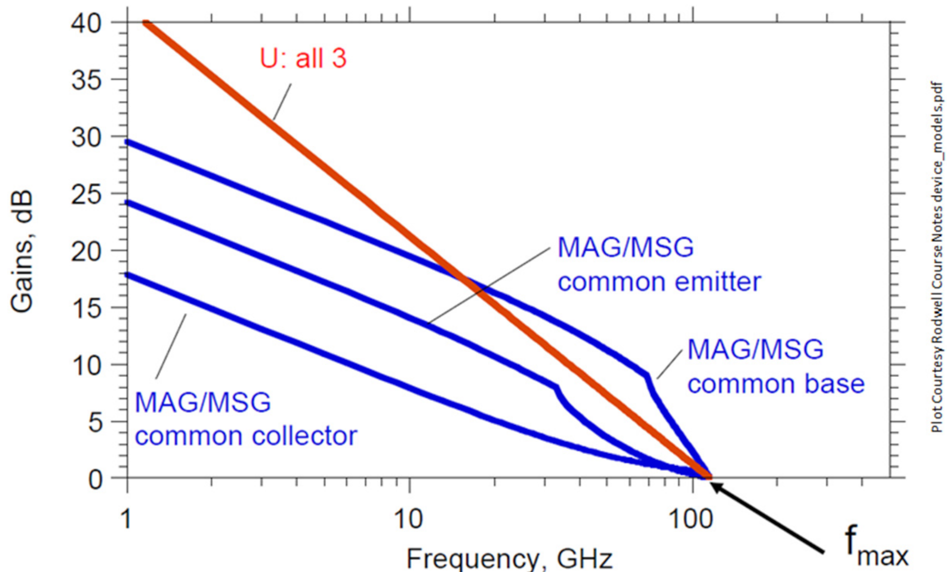


Fig. 8. Plot of MAG/MSG for CE, CB, EF Amplifiers

One noteable characteristic of all these amplifiers is that since the transistor current gain, capacitances, and transit time are what dominate the maximum frequency of oscillation, the f_{MAX} of the transistor remains the same no matter which configuration (e.g. CE, CB, EF topologies). However, the relative position of parasitic capacitances and resistances at each port have a significant impact on the available gain and input/output impedance of the transistor amplifier. In order to get amplifiers to provide gain at high frequency, careful consideration of transistor impedances must be taken. It will be shown that "Microwave"-style (millimeter-wave) matching and tuning networks will provide a way to access gain at frequencies like 220GHz.

2.1-D RF POWER AMPLIFIERS

Power amplifiers are designed to push transistors to their highest possible RF power densities. At lower frequencies, PAs with watts, kilowatts, or megawatts can be de-

signed depending on the size of transistor used. In all cases, high power is achieved by swinging RF voltages and currents to a transistor's physical limits.

A transistor's operation is limited by maximum and minimum voltages and currents. This portion of the IV-plane can be described as a transistor's high performance operating area. The linear or saturation region of operation is a desirable place for amplifier gain. This is limited at low voltage bias by the saturation (or knee) voltage. This is the bias above which the collector-base junction in the transistor is reverse-biased and acts as a current source. In other words, this is the minimum voltage to turn the amplifier on. A hard limit to maximum operating voltages is the breakdown voltage of the transistor. At this voltage, large electric fields lead to avalanche breakdown, a current multiplication effect, and irreversible damage. A softer limit on the maximum voltage in a transistor exists as well. As the transistor swings into the higher voltage area of operation, the f_T/f_{MAX} are reduced because of increased base-collector capacitance. The result is a reduction of maximum available gain at the design frequency.

Current limits also exist. At low currents (near zero) the transistor has little or no gain. At high currents the transistor reaches the kirk current limit—meaning the current density is so high that base transit time increase significantly due to base push out, thus reducing the available gain of the transistor at the design frequency. In addition, high power densities (product of instantaneous current and voltage) can lead to reduced performance over time and device destruction. Since power density is based on the time averaged power density of the transistor, a $y = 1/x$ curve can be drawn to

show the safe long-term power density limit of the transistor.

The resulting high performance operating area of the Teledyne 250nm InP HBT is shown below:

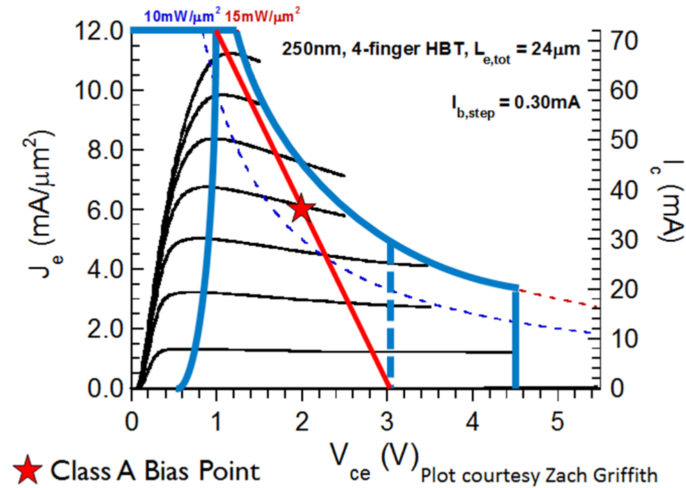


Fig. 9. Transistor Safe Operating Area and Class A load line
The Class A amplifier is biased at the midpoint of its load line. This is marked with a star. Blue lines denote operating area limits due to Kirk effect, destructive power density, breakdown, and gain reduction.

In this InP HBT process, voltages are limited by the breakdown voltage, V_{CE} =4.5V, and the knee voltage, V_{CE}~=0.8V. Maximum available gain at 220GHz drops significantly above 3V. The maximum current density in the transistor is ~12mA/µm² or for a single 6µm-long transistor 17.5mA. The destructive power density limit is at 20mW/µm² with a safe long-term operating power density of 15mA/µm². Within the region on the IV curve defined by these limits, an amplifier can operate with gain and avoid degraded performance or destruction.

As a designer, it is possible to control how voltages and currents swing in the IV plane. The way in which currents and voltages swing in an amplifier is called the Load Line. One thing to note is that if the amplifier has any energy storage parasitics (capacitance or inductance), the load line won't look like a line at all. Instead a curve

will show how instantaneous currents and voltages change throughout the sinusoidal cycle. There is an advantage to turning an oval or circular load line into a linear relationship. As higher power levels are introduced, circular load lines take up more of the IV plane and could potentially begin sweeping instantaneous power densities outside the transistor's power density limit

2.1-E CLASS A POWER AMPLIFIERS

A classic loadline is used in a Class A amplifier. In this power amplifier, a large output power is generated by sweeping the loadline from one corner of the safe operating area to the other. At one end, there is the maximum instantaneous current and the minimal knee voltage. At the other end of the load line, there is near-zero current and voltages near breakdown. For a Class A power amplifier, the transistor will be biased at the center of the load line—$V_{CE}=(V_{BR}+V_{KNEE})/2$ and $Ic=I_{MAX}/2$. The resulting output power will be $(V_{BR}-V_{KNEE})*(I_{MAX})/8$. With knowledge of the DC bias point and the maximum RF output power, a collector efficiency can be calculated. For a $V_{KNEE}=0V$, a class A power amplifier consumes an average of $(V_{BR}/2)*I_{MAX}/2=V_{BR}*I_{MAX}/4$, while the RF output power is $V_{BR}*I_{MAX}/8$. The resulting maximum theoretical collector efficiency is 50% [23].

The actual efficiency of the transistor will always be less than 50%. The knee voltage cannot be zero, not only does the collector base junction need to be reverse biased by a small voltage to stay on, but the emitter base junction must be significantly forward biased. In the InP HBTs used in this project that knee voltage was up to 1.0V

at the maximum current value. In addition, any IR drops in bias control resistance and power feeds adds to the total DC power consumed. The RF power will pass through transmission lines, power combiners, pads, waveguide transitions, and waveguides that all have a finite associated loss. These losses can reduce the RF output power significantly. Smaller RF output and larger DC consumption reduces efficiency directly.

Efficiency may seem relatively arbitrary in a laboratory setting. But for system design, power consumption can be heavily restrictive. In a real-world, millimeter-wave system, an array of power amplifiers may be flown or mobilized. On a flight, there is a finite amount of power that can be directed from flight sytems and digital processing to amplification.

With large arrays or power requirements, there will always be a portion of the DC power that is not converted into RF power. All other power is turned into heat that increases the temperature of the transistors, substrate, and surrounding environment. With large arrays, temperature gradients can reduce the relative performance across the array or potentially cause damage to some of the pixels. At the IC level, increased temperatures can also decrease performance of single transistors and potentially cause failure of an entire MMIC. If a DC power budget exists, then a higher efficiency PA will produce more RF output power at a set DC power level and leave less total power to heat the system.

2.1-F OTHER POWER AMPLIFIER CLASSES

Much effort has gone into exploring other amplifier classes with a goal of extracting

the highest possible efficiency. The trade-off for higher efficiency is lower linearity or maximum output power.

Class AB, Class B, and Class C power amplifiers are variations of the Class A amplifer [23]. In order to reduce the DC power consumption in each transistor, the current is biased below $I_{MAX}/2$. For Classes B and C, the bias current is set at 0. For class C, the voltage is also biased below the Class A quiescent voltage. The resulting waveform for a class B amplifier is a half-wave amplifier. Transient waveforms for Classes AB and C also look similar to Class B's half-wave shape with a different fraction of time where the transistor is completely off. Where Class A amplifiers are a pure sinusoid and having a single tone spectrum, these amplifier classes with sharp off-on waveforms begin to develop strong coupling of energy into the third-order harmonics and higher. DC power is only consumed when both voltage and current are non-zero. The theoretical efficiency of each of these PA classes are greater than the class A amplifier.

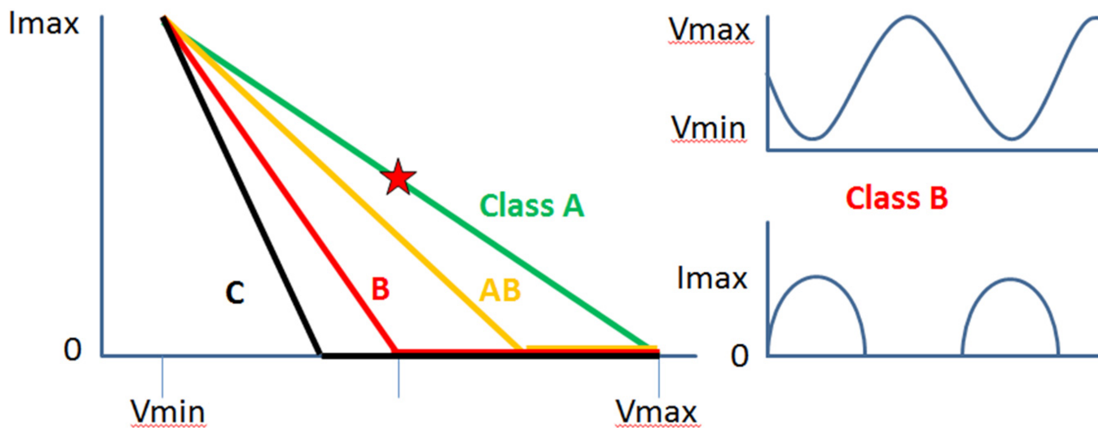


Fig. 10. Load Lines for PA Classes A, AB, B, and C
Fig. 11. DC power is consumed during time periods when both voltages and currents are non-zero.

Class D, E, and F are “switch-mode” power amplifier classes. These amplifiers also trade off linearity for theoretical drain efficiencies near 100%. In order to achieve such efficiency, transistors must be operated well below the maximum frequency of oscillation so that output waveforms can utilize higher order harmonic terms for waveform shaping. These amplifier classes further reduce the time when both voltage and current are non-zero. Some switch-mode transient waveforms are shown:

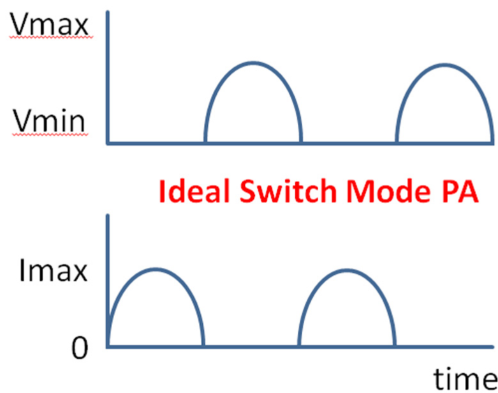


Fig. 12. Desired Waveforms for an ideal switch-mode PA

Theoretical maximum PAE is 100% for these amplifiers since there is no instantaneous power consumption.

2.1-G POWER AMPLIFIER TUNING

After deciding on a particular amplifier class and load line, the next step is to design a load impedance such that the voltages and currents actually swing to form that load line. The load line represents how the transistor’s electron current source swings voltage and current. Electron current does not include displacement currents that “flow” in capacitors.

For example, the frame of reference for a load line in a common emitter HBT would be inside the parasitic capacitance on the collector. In this case, the intrinsic

device capacitance is not seen as part of the device, but rather a local tuning element. With a linear load line, the desired impedance seen at the current source is purely real. Given a load line's change in voltage ($dV= V_{MAX}-V_{KNEE}$) and change in current ($dI=I_{MAX}-0$), the real load line resistance is just dV/dI.

For low frequency circuits, one can get the correct load line by applying a resistor with a value equal to the load line, since resistors are linear elements and have a fixed ratio of current to voltage. At high frequency, where interconnects within the circuit are not small electrically, microwave techniques and transmission line theory must be considered.

At high frequency the idea of a resistor, capacitor, inductor, and wire are fictional. Even small structures have picohenries and femptofarads of parasitic inductance and capacitance that can lead to dominant reactances at 220GHz. This makes modeling of every interconnect, transmission line, capacitor, and resistor a critical part of design.

The point of this discussion is that given all the imperfections in your tuning networks, two things must be accomplished by a tuning network connected to the transistor. First, at a minimum there must be reactive cancellation. To first order, this means cancellation the collector-base capacitance internal to the transistor for a common base HBT. In a tuning network, this could be done with a shunt inductance or with a pi section.

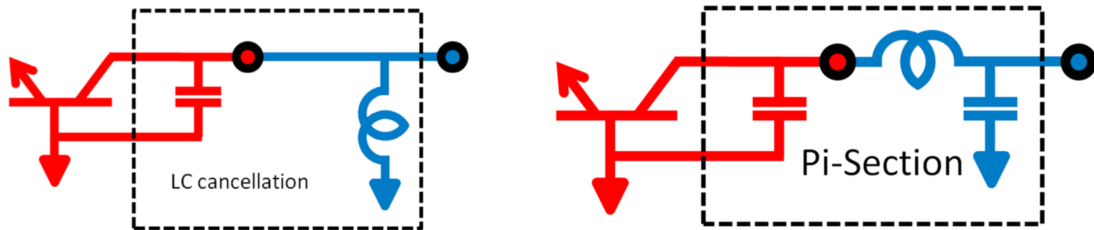


Fig. 13. LC and Pi network cancellation of common-base output capacitance

Second, the tuning network must provide the correct load line impedance to the electron current source of the transistor. This ensures that the trajectory (and linear relationship between voltage and current) travels in the correct area of the IV-plane. No matter the load line resistance required, the resulting amplifier will undoubtedly be connected to a larger system for test or system assembly. 50ohms is a typical system impedance, and a tuning network must transform that 50ohm system impedance to the real load line impedance desired at the electron current source.

The resistance of the load line that is required is affected by the number and size of transistors and other technology specifications. For example a transistor sized to handle a maximum current of 125mA and with V_{KNEE}=1V and V_{BR}=6V, will have a class A load line resistance of 40ohms. A transistor size twice as large should operate at the same current density and have a load line of 20ohms. This becomes important when considering the relative difficulty of doing impedance transformation from a 50ohm system impedance to 20 ohms compared to transforming to 40ohms.

2.1-H TRANSMISSION LINES

For Integrated Circuit (IC) design, several types of signal transmission lines are possi-

ble. The most common are non-inverted microstrip, inverted microstrip, and coplanar waveguide transmission lines. In addition to transmission line structures, integrated waveguides are often used in optics and metallic rectangular waveguides are used in packaging, long-distance transmission, and module-to-module interconnects.

Transmission line theory is an important factor when the distance that a signal must travel is a significant fraction of a wavelength (or larger) at that frequency. Conversely, over short electrical distances, transients and reflected waves caused by transmission lines may be negligible.

Transmission lines have a signal path and ground path with different potential energies [25]. The fundamental mode of propagation of a voltage-current wave (electro-magnetic wave) in a coaxial and parallel plate transmission line is a TEM (Transverse Electro Magnetic) mode with electric fields as shown below. The fundamental TEM mode is one of many possible solutions to the wave equation. With a TEM mode, a wave can propagate along the length of the transmission line with electric and magnetic fields being excited in the two orthogonal directions.

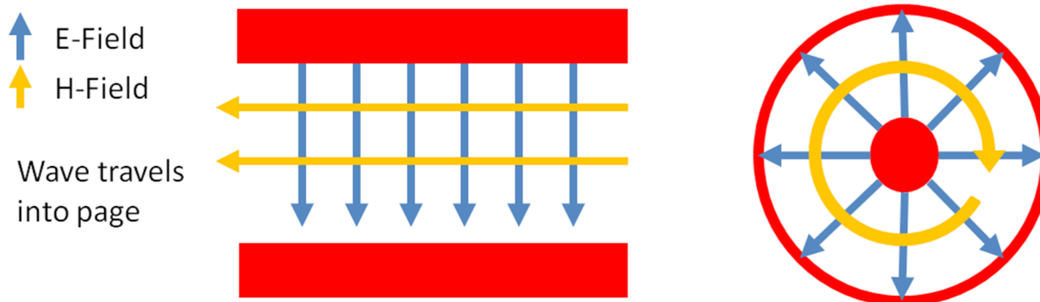


Fig. 14. TEM Transmission Lines: Infinite Parallel Plate and Coaxial Lines

In a microstrip transmission line, the ground may be considered an infinite

plate, but the signal line is of finite width. The fields of the fundamental microstrip mode are not uniform in one direction. But, in the central region of the line, field lines look similar to a TEM transmission line. Microstrip is considered a “quasi-TEM” transmission line.

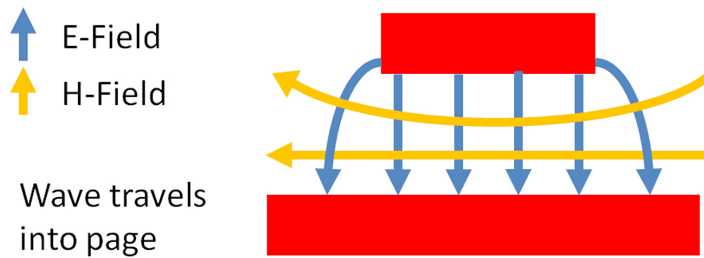


Fig. 15. Quasi-TEM Transmission Lines: Microstrip Lines

In any transmission line, the signal line provides a forward path for current flow and the ground provides a reference for voltages on the signal line and a return path for current flow. A standard model for a transmission line is a series inductance and a shunt capacitance for a lossless transmission line. A lossy transmission line model has the inductor and capacitor with an added series resistance and shunt conductance.

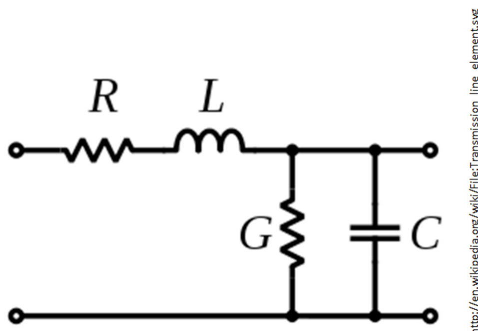


Fig. 16. Model of a transmission line

When a voltage wave is propagated in the transmission line, a corresponding

current wave is also excited. The ratio of voltage to current for each wave is constant and is called the characteristic impedance of the transmission line. In a lossless transmission line, the value of the characteristic impedance is only dependent on its energy storage components—inductance and capacitance per unit length. The equations for characteristic impedance are shown. A complex impedance means that there is loss per unit length in the transmission line.

$$Z_{o,Lossy} = \sqrt{\frac{R + j\omega L'}{G + j\omega C'}} \qquad Z_{o,Lossless} = \sqrt{\frac{L'}{C'}}$$

Eq. 5. Characteristic Impedance for lossy and lossless transmission lines

The linear capacitance density (C') of the transmission line is computed like a parallel plate capacitor. The electrical permittivity of the dielectric is multiplied by the effective width of the capacitor and divided by the dielectric thickness. The effective width of the transmission line corresponds to the width where the electric fields originate and terminate on signal and ground, respectively. A wider microstrip line with a shorter distance to ground will have greater capacitance.

The linear inductance density (L') is a little more complicated to compute. A loop of current is formed as forward currents travel down a transmission line and return along the ground plane. The current loop generates a magnetic field through the center of the loop. Inductance is increased with a narrower signal line. Inductance is increased logarithmically for greater distance from the ground plane. Relative magnetic permeability of a typical dielectric is 1. Comparing two transmission lines in the

same material system, a narrower signal line with greater distance from the ground has greater inductance.

With this understanding, it makes sense that as a transmission line is narrowed, the inductance increases and the capacitance decreases, leading to greater characteristic impedance and a transmission line that behaves similarly to a series inductor. Conversely, a wider microstrip transmission line will lead to a smaller characteristic impedance and behavior similar to a shunt capacitor.

When a transmission line is terminated with a load impedance, the input impedance varies with the value of the load impedance, the transmission line electrical length, and the characteristic impedance of the transmission line. An equation for input impedance for a transmission line is shown below.

$$Z_{in}(l) = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)}$$

Eq. 6. Input impedance of a loaded transmission line

2.1-I IMPEDANCE MATCHING

Now is an important time to consider impedance matching. Impedance matching is relevant for two reasons. Impedance matching leads to the best possible outcome for transferring power from a generator to a load. Impedance matching with transmission lines can also reduce reflections and transients that can distort signals.

To begin thinking about the power transfer taking place in a simple circuit, consider a 100V AC voltage generator with a finite impedance of 50ohms. Now, con-

sider a load with a variable impedance that can be swept from being a short circuit, thru a 50ohm, to an open circuit. When the generator is attached to the short circuit load, the current is simply the generator voltage divided by the generator resistance or 2A. However, there is no voltage drop at the load, so no power is consumed or transferred to the load. When connected to an open circuit, there is 100V across the load, however no current flows and therefore no power.

As the impedance of the load is adjusted to the generator impedance, the total power transferred to the load reaches a maximum. When a 50ohm load is selected, 100ohms is seen at the voltage source and 1A of current flows through the circuit. 50V is dropped across the load for a total of 50W transferred to the load. While considering only these impedances is far short of a proof, it is useful in understanding how power is transferred from a generator with a finite impedance.

A similar idea holds for complex impedances. When impedances are complex conjugates, it is said that the impedances are matched. The maximum power is transferred from the generator to the load. This occurs for the same reasons described above. The real impedances are matched and allow maximum power transfer, while the conjugate values for reactance cancel at the interface where power transfer is being considered.

At the interface between two impedances, conservation of energy is in effect. When a wave with RF power hits an interface, a reflected wave of power returns to the source. The incident wave is called a forward travelling wave and the reflected wave is a reverse wave. For a matched load, all the RF power is transferred to the

load and there is zero reflected energy. A transmitted wave with RF power equal to the forward wave continues through the interface. In the case where impedances are not matched, a reflected wave and a transmitted wave are generated. A greater difference in impedance at the interface corresponds to a larger amount of reflected power and less power transmission. Still the sum of reflected and transmitted power must be equal to the incident RF power at the interface. A reflection coefficient can be created to demonstrate the value of the reverse voltage waves relative to the forward voltage wave.

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad \mathrm{T} = 1 - \Gamma$$

Eq. 7. Reflection and Transmission Coefficient

When transmission lines and other more complex passive structures are introduced into a circuit design, the importance of impedance matching increases. Consider a generator, a transmission line, and a load. Mismatched impedances at the two interfaces can create a series of reflected voltage waves on the transmission line as shown below. Such reflections can add standing waves, delay, or otherwise distort the signal received at the load.

In cases where the source and generator impedances are the same, selection of the right transmission line characteristic impedance can be straight forward. Select RG=RL=Zo. When the impedances on generator and load are not the same, there are various techniques to transform the impedance so that one or both sides have a result-

ing impedance match and the power can be losslessly transferred from the generator to the load.

2.1-J IMPEDANCE TRANSFORMATION

There are several ways to transform impedances [25]. Generally, impedance transformation is a band-limited operation.

A quarter-wave transformer is one classic way to transform impedances. This uses the equation shown above (for transmission line input impedance) to match the generator impedance to an arbitrary real load impedance. When the transmission line is a quarter wavelength long at the desired frequency, the input impedance is reduced to sqrt(Zo*ZL). If Zo is chosen such that this expression equals the impedance of the generator, then impedances will be matched. Full power transfer will occur between two different impedances through the chosen transmission line.

$$Z_{in}\left(\frac{\lambda}{4}\right) = \frac{{Z_o}^2}{Z_L}$$

Eq. 8. Quarter-wave transformer input impedance

Other matching networks can be chosen to transform impedances. Many are more easily visualized on a Smith Chart.

2.1-K USING SMITH CHARTS

Smith Charts are a useful way to visualize the complex impedance plane on the unit circle [25]. The x-axis represents the real component of an impedance normalized

to a system impedance. Commonly a 50ohm system is selected, so the center point of the unit circle that sits at a normalized impedance of 1, also represents the system impedance. At the coordinate (-1,0) a short circuit or 0 impedance is represented. At (1,0), the impedance is infinite or an open circuit.

A complex impedance (R+jX) can be found on the Smith Chart by finding R on the x axis and travelling along a circle which has a diameter defined by the points r=R and r=infinity on the x-axis. As X becomes a larger positive number, the impedance is found on the upper portion of that circle and closer to (1,0). If X is negative, then the impedance is found by travelling away from r=R on the lower portion of the circle.

This principle also has direct application to loads constructed with a series of connected components. A resistor with value R may be chosen, then an added series capacitance or inductance can be added to move along its circle of constant resistance.

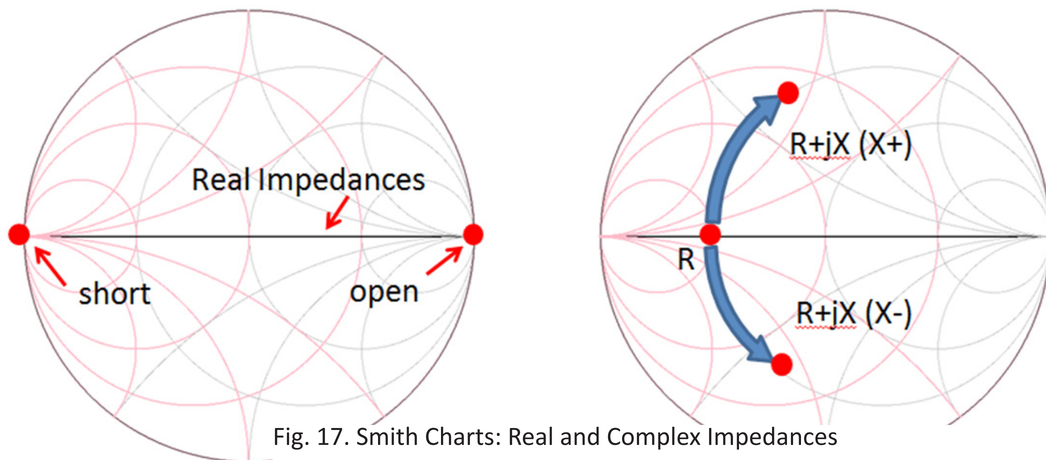


Fig. 17. Smith Charts: Real and Complex Impedances

Admittance is the inverse of impedance. The Smith Chart for admittance is reflected about the y-axis. When components are added in parallel, the admittances

add. Admittance is written as Y=G+jB, where G is the conductance and B is the susceptance. Small admittances correspond to large impedances, hence a zero admittance is at the coordinate (1,0) on the Smith Chart. The short circuit or infinite admittance is located at the coordinate (-1,0). Circles of constant conductance are defined by diameter endpoints at the constant conductance and at infinite inductance (-1,0). An admittance can be found by moving along the circle of constant conductance arcing up to the appropriate susceptance for an inductive susceptance or arcing down for a capacitave susceptance.

In loads, a parallel connection of components can correspond to a sum of admittances. For example, a resistor with conductance G and an inductor with susceptance -B can be connected in parallel and the result will be an admittance at G-jB above the x-axis along the circle of constant conductance equal to G.

Passive components can be added in various ways to transform impedances around the Smith Chart. Adding combinations of inductors and capacitors in series and parallel to the load can, in theory, provide any impedance on the Smith Chart with no additional loss. A summary of how to use these components to move around the Smith Chart is shown below.

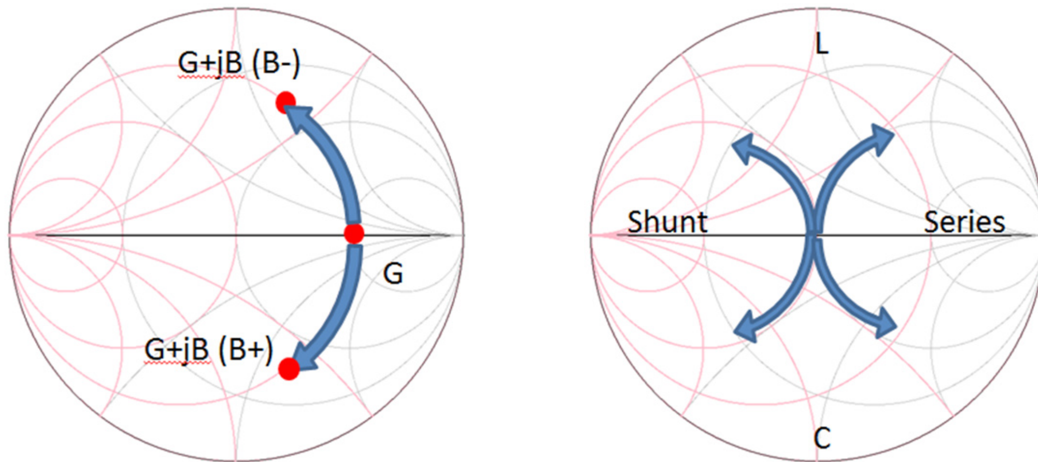
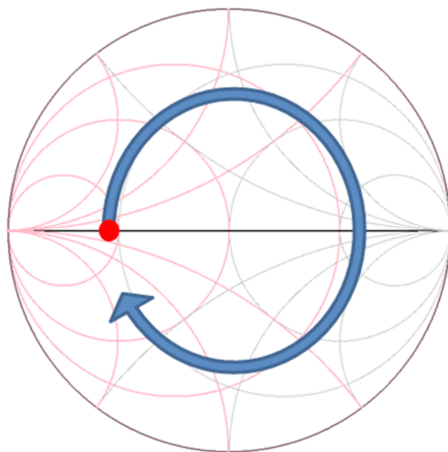


Fig. 18. Smith Charts: Admittances and Series/Shunt L/C

Smith Charts are a useful way to consider transmission lines as well. If the system impedance is the same as the transmission line's characteristic impedance, the center of the chart will be the Zo of the transmission line. When a load is attached to the end of a short transmission line, the input impedance shown on the Smith Chart will be at the value of the load. As the electrical length of the transmission line is increased, the resulting input impedance can be found by moving around a circle centered at the middle of the Smith Chart clockwise. The arc swept around the Smith Chart relates to the number of half-wavelengths of transmission line length. For example, a transmission line that is one-eighth of a wavelength (pi/4) is 0.25 half-wavelenths and would travel around one quarter of the Smith Chart as shown below.

Transmission lines with other characteristic impedances (not equal to the system Zo) can be shown on the Smith Chart as well. Non-system-Zo lines transform impedances in circles around the Smith Chart not centered (0,0). An inductive (or

high Zo) transmission line will circle around the Smith Chart similar to the average of a 50ohm transmission line's circle and the circle traced by a series inductor or capacitor. A capacitive (or low Zo) transmission line will transform impedances around a circle like a hybrid of the circle of constant conductance and the 50ohm circle as shown below.



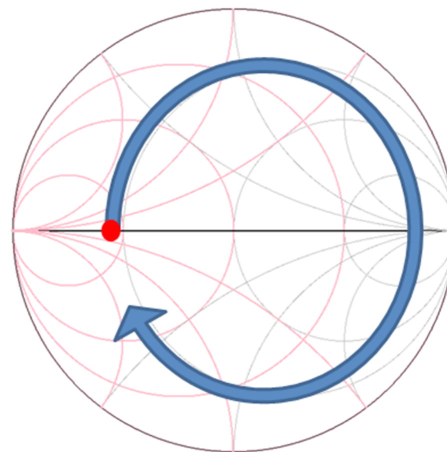


Fig. 19. Smith Charts: Tracing Input Impedance with 50ohm and >50ohm TLines in a 50ohm system

2.1-L SMITH CHART IMPEDANCE MATCHING NETWORKS

An impedance transformation is done with series- and shunt-connected inductors and capacitors [26]. Consider a mismatched, real impedance load and generator as shown. When a series inductor is added to the load impedance at point A on the Smith Chart, the impedance is transformed to point B. When the susceptance from a shunt capacitor is added to the admittance at point B, the result is a real impedance at point C.

The bandwidth of this lossless impedance matching network is related to the

Q factor of the network. The Q factor is the ratio of reactance to resistance and also the ratio of bandwidth to center frequency. Lines of constant Q factor can be drawn on the Smith Chart. An impedance closer to the edge of the smith chart (far from the real axis) is associated with high Q factor and a more limited bandwidth. The Q of a matching network can be reduced by using multiple small LC networks. This method transforms a smaller amount of the overall impedance with each LC network and can reduce the overall matching network Q.

There are instances where an impedance at generator or load is already in a high Q region of the Smith Chart. In these cases, the overall Q of the circuit cannot be reduced by reducing the matching network Q and the circuit bandwidth cannot be optimized further.

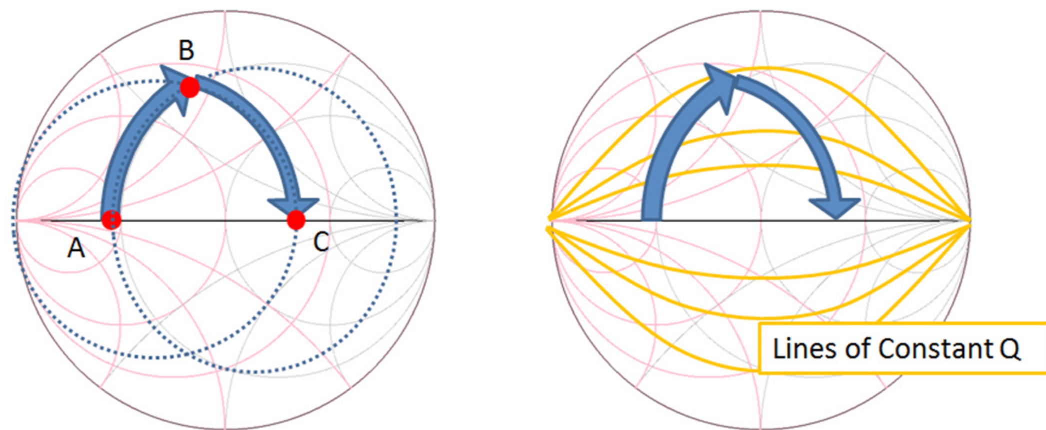


Fig. 20. Smith Charts: Series L/Shunt C impedance matching and Lines of Constant Q

2.1-M TRANSISTOR IMPEDANCE MATCHING

This discussion on transistor amplifiers, power transfer, and impedance matching leads naturally to a discussion about microwave or millimeter wave amplifiers [26]. In

transistors operating at high frequency, as described above, the S21 of a single un-matched transistor may be less than 0dB—and provide no amplification. However, the S21 is low because of gain reduction in the transistor at high frequency and parasitic capacitances that don't allow power transfer to and from the source and load. Even with these parasitics, the transistor will have positive available gain at frequencies up to the f_{MAX} of the device.

Impedance matching can help the designer achieve the transistor's maximum available or maximum stable gain. Impedance matching makes it possible to transfer the maximum amount of power from the generator to the transistor, utilize the transducer gain of the transistor, and then transfer the maximum amount of power from the transistor to the load.

For a unilateral device—meaning the product of S21*S12 is very small—the process of impedance matching the transistor is straight forward. When S21*S12 is zero, the reflection coefficient into a 50ohm system is equal to S11 on the input and S22 on the output. The reflection coefficient corresponds 1:1 to an impedance looking into the input and output of the transistor. When the transistor is biased, the S-parameters can be sampled and the complex impedances on input and output can be recorded at the desired frequency.

When the transistor input and output impedances are known, lossless matching networks can be chosen to provide an impedance match at the transistor ports, source, and load simultaneously. A lossless matching network can transform the system impedance (at source and load) to the complex conjugate of the transistor impedance.

The result will be full power transfer between the generator/load and the transistor.

For a non-unilateral device a similar approach can be used iteratively. In these cases a feedback mechanism (e.g. a feedback capacitance) makes S21*S12 a non-negligible value. In these cases, the S11 and S22 S-parameters do not directly correspond to the input and output impedances. The input impedance now has a significant dependence on what impedance is placed onto the transistor output and vice versa.

The iterative process to achieve maximum available gain is as follows: Lossless matching networks are used to provide impedance matching at the input port. The output port is then impedance matched. This match will have changed the input impedance of the transistor depending proportional to the magnitude of S12. Then the input is re-matched, and that action will detune the output. This process continues until an acceptable match is found on the input and output if the process converges. Unfortunately if S12 is large enough, there may not be a point of convergence in this iterative process.

2.1-N STABILITY FACTOR AND STABILITY MEASURE

Stability is a critical principle in amplifier design. Stability refers to the possibility of undesirable, self-sustaining oscillations in the circuit. Instabilities can be cause for concern for several reasons. In-band instability could mean that an output may contain spurs that will distort desired data in a system. Additionally, any instability consumes DC power meant for amplification. The result could be lower gain or output power of the signal meant to be amplified and significantly lower power added efficiency.

Oscillations can lead to destruction of devices and permanent circuit failure.

A circuit with unconditional stability will not oscillate at a particular frequency no matter what passive impedances are being seen by the amplifier's input or output. This becomes important when considering how the circuit will be used. In a circuit designed for unsupervised use, it is not always known under what conditions a consumer will use the circuit. Any number of impedances could be applied at the ports of these circuits. For this reason, it is essential to determine that an amplifier will be unconditionally stable over all frequencies.

On the other side, a potentially unstable circuit is also not guaranteed to oscillate. It will only oscillate when loaded on input and output with impedances that will cause the system to have positive feedback and a loop gain large enough to sustain oscillation.

The set of impedances that can cause oscillation for an amplifier can be marked on a Smith Chart using stability circles. The stability circle marks the border between impedances that can make the transistor oscillate and impedances that will not. There are occasions when the region within the circle is the stable region and others when outside the circle represents the stable set of impedances. Input and output have two different stability circles called the source and load stability circles.

When a system is unconditionally stable, the entire Smith Chart is within the stable region of the stability circle. If one of the stability circle (source or load) plots shows that the amplifier is unconditionally stable, then the other will also show unconditional stability. Besides looking at stability circles to determine unconditional

stability, there are more direct ways to ensure stability over all frequencies.

Rollett Stability Factor (K) and Stability Measure can show unconditional stability at a single frequency. These two scalars can be calculated using amplifier S-parameters, so it can computed for any two-port system. If K is greater than 1 and Stability Measure is greater than 0 at one frequency, then the necessary and sufficient criteria are met to ensure unconditional stability at that frequency. In most cases, S-parameters will be swept over many frequencies. In this type of simulation or measurement, stability measure and factor can be determined over a wide range of frequencies to determine stability in and out-of-band.

$$\text{K (Stability Factor)} = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{21}S_{12}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$\text{B1 (Stability Measure)} = 1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2$$

Eq. 9. Rollette stability factor and stability measure

Unconditional stability should be verified over any frequency at which the transistor has a potential for small signal gain. Although oscillations above f_T are unlikely, this could mean verifying stability up to f_{MAX} or 650GHz for the 250nm InP HBT process. On the low end, stability may be checked to 1GHz or lower. In many cases, narrow bandwidth matching networks and other passives in microwave/millimeter-wave amplifiers tend to filter out signals at these lower frequencies and low frequency RF power is shorted to ground thus stabilizing the amplifier at those frequen-

cies. Intermediate frequencies where filtering is minimal (50-60GHz for a 220GHz amplifier) and the amplifier has large maximum stable gain, could be a source of undesirable out-of-band oscillations.

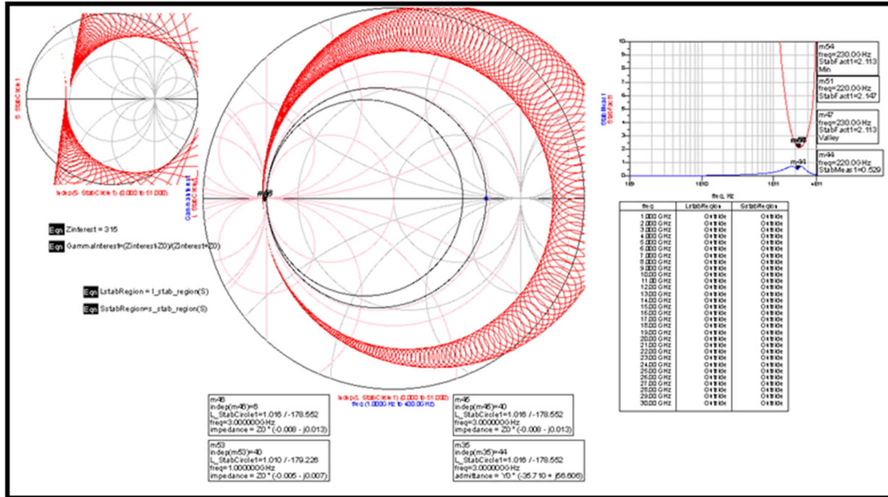


Fig. 21. A Simulation of Source & Load Stability Circles, Stability Factor, and Stability Measure
Simulation over a broad range of frequencies can give the designer perspective about what impedances could cause oscillation and what type of stabilization to use.

At frequencies where the transistor is potentially unstable, the maximum available gain is technically infinite with oscillations generating real RF output with zero RF input. However, the maximum stable gain of the amplifier is the maximum stable gain when the amplifier has been stabilized just to the point of unconditional stability at that frequency. This is the maximum gain possible when K=1.

In order to achieve the maximum stable gain, the circuit is first stabilized and then impedance matched. To stabilize, additional RF loss is added to the circuit to reduce the loop gain in the feedback path through which oscillations could be sustained. When loss is added, the Smith Chart effectively shrinks.

As an example, a stability circle overlaps the Smith Chart near its upper left

corner The region inside the circle represents potentially unstable load impedances. When 10ohms is added in series to that port, the Smith Chart shrinks. The short circuit location is now where the 10ohm location was on the original Smith Chart. The unstable region is now outside the entire Smith Chart and the circuit is now unconditionally stable.

Once stabilized, the same types of lossless impedance matching networks discussed earlier may be used to achieve the maximum available gain of the stabilized transistor.

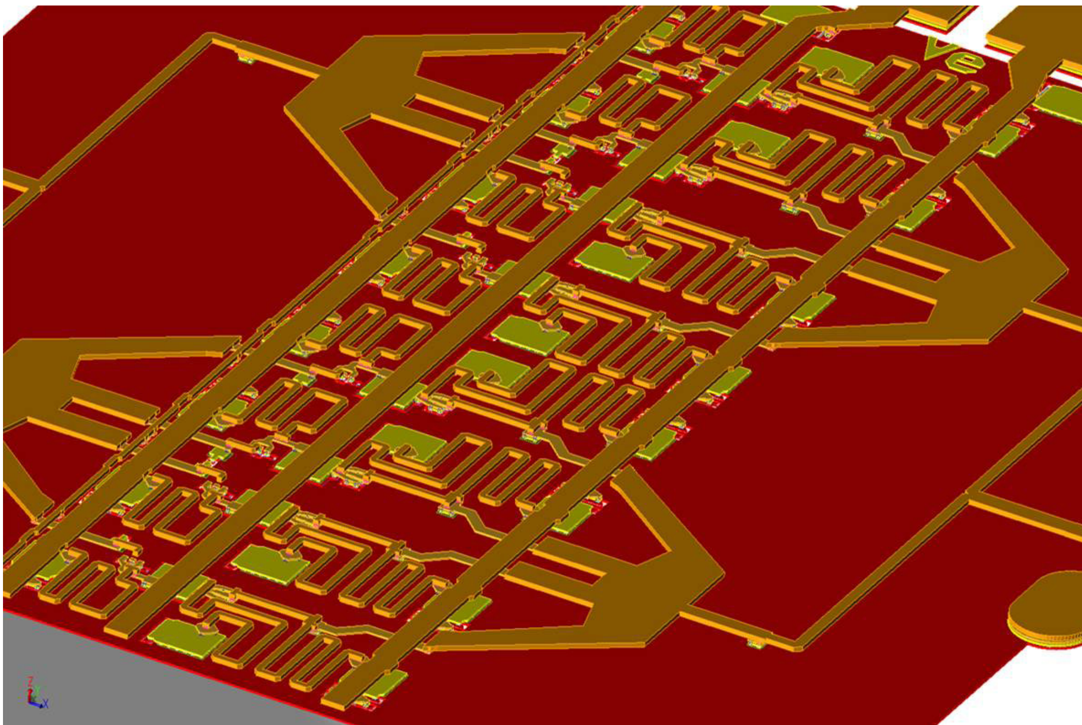


Fig. 22. 3-D Rendering of an 8-cell SSPA

2.2
220GHz SSPA Design

2.2-A ADJUSTING MICROWAVE METHODS FOR 220GHZ

Details of MMIC design work at high frequency are often hard to find, because many entities consider the design methodology to be proprietary. However a few items are clear.

Methods for output tuning often begin with using an ac-shorted shunt stub or ac shorted shunt inductor to cancel the transistor's collector capacitance. On the Smith Chart, the shunt inductor subtracts susceptance to bring the admittance to the circle of $R=R_{LL}$. A series inductance is added to make the final impedance the real load line impedance at the electron current source in the small signal model of the HBT. This is often seen as the lowest Q solution to output tuning.

Since the 4x6μm HBT used for design is operating very close to f_{MAX}, the collector-base reactance is highly significant at 220GHz: The S22 trajectory of the amplifier traces into a very high-Q region of the Smith Chart and is dominant in determining the output amplifier tuning bandwidth. As long as the quality factor of the tuning network is less than that of the multi-finger HBT, the tuning network will not

increase the amplifier Q and decrease the power bandwidth. So a potentially higher-Q, but more compact tuning network (e.g. a Pi-section or a multi-pole tuning network) could be used without reducing amplifer bandwidth.

Harmonic suppression is also used in high frequency PA design for harmonic suppression and waveform shaping. This is especially important for higher-class, less-linear PAs. At the cost of PA Cell space, quarter-wave shorted stubs can be useful for 2nd harmonic suppression in Class AB, B, C amplifiers, as the 1st, 3rd, … harmonic sees an open and the 2nd, 4th, … harmonic sees a half-wave short. However harmonics well above f_{MAX} may have no gain with which to create distortion to waveforms.

In addition to tuning networks, on-wafer power combining has been critical to achieving the most power at the IC level. Some approaches use classic microwave techniques to achieve power splitting. Two-to-one power splitters and combiners have been prevalent at the final levels of power combining. These have included marchand baluns, Wilkinson power combiners, and novel methods of waveguide probing and excitation. Some of these splitters have in-phase outputs, while others produce 180 degree phase shifts. But often these are large electrically and large insertion losses can be incurred.

A more desirable splitter would split signals with an electrical delay that is shorter than a quarter wavelength to reduce the insertion loss incurred. Combining of four or more signals in one combiner will reduce the levels of power combining. Lange and ring couplers are great examples of microwave combiners that can be used for combining more than two ports. These hybrids are large electrically, and they re-

quire a low loss transmission line environment to ensure balanced signal cancellation at each port. Four-way Dolph-Chebyshev power combiners can combine four signals in a short electrical distance. These combiners have proven to result in a lower total loss due to phase mismatch, impedance mismatch, and conductor loss than losses in the classic microwave hybrid combiners.

2.2-B 220GHZ PA MMIC SPECIFICATIONS & TECHNOLOGY

The PA MMIC project had specifications for a final power amplifier module. The PA operating frequency is 220GHz and the PA is to be mounted into a waveguide module for use in a larger system. The solid state PA would be used as a medium power amplifier to drive a travelling wave tube amplifier. The preamplifier is critical since no other commercial source exists to date that can drive the tube into compression.

The specifications given for the PA MMIC required 10dB gain, 50mW of output power and a bandwidth of 10GHz. Further gain, bandwidth and saturated output power would also be beneficial in driving the last non-IC stage.

Designing a 50mW amplifier is not straight forward. The approach taken for the amplifiers described here was to design a modular PA Cell that tuned a reasonable amount of transistor periphery for high power. Following the design of those PA cells, on wafer power combiners were designed to sum power from multiple PA Cells on the MMIC.

The PA Cell design starts with selecting a reasonable size of transistor periphery. A single 6x.25μm^2 transistor can reach a saturated output power of up to 6mW at

its collector. As the number of HBTs and their length increases in a single PA Cell, the greater the phase difference between HBTs incurred while distributing the RF signal power to each device. A compact cell must dissipate heat proportional to the total HBT periphery. As the temperature rises, the possibility of thermal instability and circuit performance degrades. Both of these factors have the potential to reduce the overall amplifier gain, stability, and output power. It is up to the designer to determine how many transistors should be placed in parallel in a single PA cell.

In work done at Teledyne Scientific by Zach Griffith, several compact multi-finger HBTs were fabricated to compare to the performance of a single-finger HBT. It was learned that above a 4-finger HBT, the f_T and f_{MAX} of the multi-finger HBTs dropped significantly. The 4-finger HBT appeared to be the best combination of high current handling capability and performance consistant with the single-HBT f_T and f_{MAX}. The single 6μm-long HBT had an f_T=350GHz and f_{MAX}=590GHz at a Vce=2V and Ic=5.5mA/μm^2--amplifier's quiescent bias point. The 4x6μm HBT had f_{MAX}=530GHz and f_T=333GHz at the same voltage and current density.

One of the reasons the 4x6μm HBT performed better than the others was that the device was laid out in an elegant way as to allow minimal feed and overlap parasitics and good grounding for the common node of the device.

The 4x6μm HBT was used heavily in developing PA MMIC Cells. On-wafer power combiners were designed relative to the size of the PA Cells to achieve a higher overall saturated output power.

2.2-C 220GHZ PA CELL DESIGN

For 220GHz PA design, several transistor amplifier topologies were taken into account. For a single transistor, a common base HBT had greater available gain at 220GHz than a common emitter HBT. Feedback through C_{CB} in the common base modulates the base voltage because of parasitic resistance and inductance in the base. This additional feedback makes the common base device potentially unstable over a large band of frequencies, but also allows large available gain given the right impedance is applied to input and output. Large feedback also means that the amplifier (given larger transistor S12) is less unilateral.

Grounding of the common device port is a greater challenge for these HBTs versus an ideal circuit. In an ideal circuit, a common emitter HBT has a grounded emitter node and a common base HBT has a grounded base. When a signal leaves the base semiconductor in an HBT, travels through the base mesa metal, and arrive at the first layer of metallization, ohms of resistance and pH of inductance are incurred. If a further set of vias are added to access a higher metal layer chosen as ground, additional resistance and inductance are added. The result is (1) a larger S12—higher design complexity, (2) less stability, and (3) lower available gain.

At 220GHz, the maximum available gain of the common emitter was around 6dB. The MSG of the CB amplifier was around 10dB. In order to fully stabilize these circuits over all frequencies, the MAG/MSG would be reduced by 1dB. The approach to design the PA is not to provide a small signal impedance match on the output, but

rather provide the correct load line impedance to the transistor current source. This would likely reduce the gain of the final amplifier again depending fully on what type of mismatch the load line would incur. Additional gain would have to be added to achieve the gain requirements for this amplifier.

An approach using a cascode was also considered. The benefit of the cascode is higher available gain from the active part of the circuit and a low S12 for a more unilateral tuning strategy. However, some downsides exist with this topology. Potential oscillations may occur within the two transistor system not captured in the stability factor/measure. Stabilization over the entire frequency spectrum must be considered. In a cascode, both the base of the common base transistor and the emitter of the common emitter transistor must still have an AC ground. In a classic cascode that is DC coupled only one of the transistors can be connected to ground potential. One node (likely the base of the common base transistor) may be chosen to optimize the output performance of the cascode, but the other node (emitter on a common emitter transistor) is left to have a poor AC ground through vias and a bypass capacitor.

For the designs described here, a cascode was selected to utilize the high available gain at 220GHz. The common emitter and common base of the cascode are AC coupled to allow grounding of CE emitter and the CB base directly to the ground plane on the metal 1 layer. This is done with only a small penalty in DC power consumption, since the voltage drop and current in each device would be consumed whether or not the circuit is AC or DC coupled. The penalty in power consumption is paid in resistive losses in the two additional DC power supply feeds that must bias the

CE collector and CB emitter.

In order to AC couple these circuits a DC blocking capacitor must be designed. Since metal 1 and CapM (capacitor metal) that connects to metal 2 is used, a hole in the metal 1 ground plane is generated. The hole could be dangerous for two reasons. First, complex structures are tricky to model using EM simulation software. On unique structures, it is difficult to know if the simulation has properly taken into account all the parasitics associated with it. Second, ground plane holes may force ground return currents to flow in a much longer or narrower path than a solid ground plane—increasing inductance. As the ground is part of the circuit, added resistance or inductance could be incurred. To reduce the risks associated with ground return currents, the ground plane was extended to collector metal beneath the DC blocking capacitor.

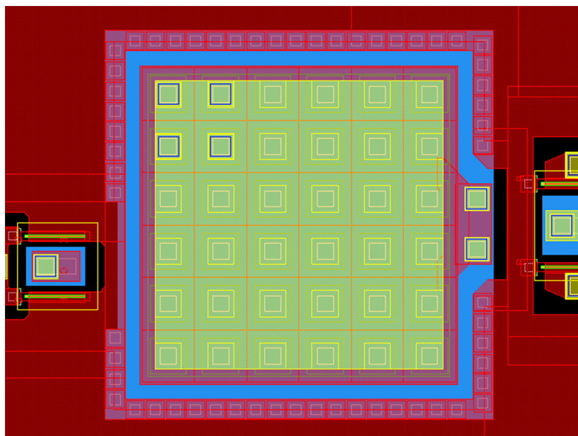


Fig. 23. A DC Blocking Capacitor

This DC blocking cap is modeled as a series capacitor with a shunt capacitor to ground on the metal 1 side. Although this structure is lower risk, the shunt capacitance to ground in non-negligible. This DC blocking capacitor was also used between

stages in multi-stage amplifiers. To reduce loss due to the capacitance to ground, tuning was done on both sides of the circuit to create a low-loss impedance match at 220GHz. For the 3rd PA MMIC tapeout an updated version was designed for even lower loss.

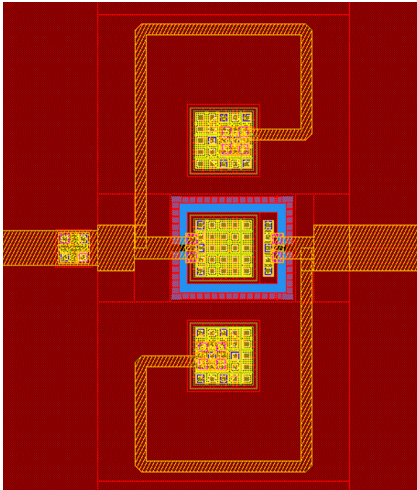


Fig. 24. A 220GHz tuned DC block
The Capacitor is located at the center creating a hole in the ground plane and is connected to the circuit at left and right. The cap is tuned for low S21 using high-Zo ac-shorted shunt stubs.

2.2-D PA CELL DC DESIGN

A class A load line was selected to generate a large saturated output power. The DC bias point for a class A load line was discussed previously in this document. For this amplifier, the minimum VCE for large signal operation is 1V at high currents. The maximum current per 6µm transistor is 17.5mA. The maximum voltage, was unclear from the transistor models. Technically, the transistor breakdown voltage is 4.5V Vce, but above 3V of bias, there is a significant reduction in small signal gain.

For the first experiment designed with this technology, three load lines and bias points were used to determine how large signal gain is affected when the RF signal swing enters the region of the IV-plane with lower available gain. The three

designs set V_{CB} on the common based device of the cascode at 1V, 1.25V, and 1.5V. The resulting RF voltage swing for each amplifier was respectively 2V, 2.5V, and 3V. The potential output power is proportional to the voltage swing. DC bias current set in each transistor for these designs were set to half of the maximum current or 8.75mA in each 6μm transistor. Since a 4x6μm HBT was used for this design, each common base multi-finger PA cell in the first and second tapeout ran at 35mA.

The common emitter device ran at a similar current bias point with lower voltage. This bias point was selected, because a plot of transistor f_T/f_{MAX} showed greater gain versus low-power bias points. The current in the 4x6μm common emitter device was set to 35mA with a Vce of 1.8V.

The DC conditions were set using pull up and pull down resistors and quarter wave DC chokes. The DC chokes were present on the CE collector, the CB emitter, and the CB collector. The CE emitter and CB base were directly tied to the ground plane and ground potential. The DC choke was designed as a quarter-wavelength, high-impedance transmission line at 220GHz in the BCB dielectric. The transmission line was then terminated with a large capacitance. In this design the large capacitance used was 270fF. The resulting DC chokes appear as a short at DC and as a very high impedance for a small band around 220GHz. Using a higher-impedance transmission line in the choke creates a lower-Q, wider passband for RF signals.

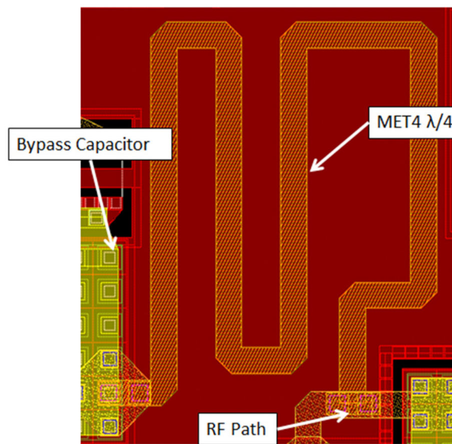


Fig. 25. A Quarterwave RF choke
The choke is used to provide bias to the transistor at DC while maintaining a high impedance at the design frequency.

The pull-up resistors on the CE base and CB emitter set the currents in the CE and CB devices, respectively. The on voltage of a base-emitter junction stays very close to 0.83V in this process over a wide range of currents. The CE pull up resistor is connected between base and the positive power supply and provides the base current to control the collector current. The current gain, or beta, in this process is ~28. Hence, for a 35mA current flow, 1.25mA must be driven into the base. Depending on the power supply voltage, a resistor is then chosen. Since this resistance is electrically large compared to the 50ohm system, a choke is not necessary on this supply.

On the CB emitter, a pull down resistor was used with the same diode drop to bias the CB collector to 35mA. The current in the pull down resistor is the base current plus the collector current. The resistor value depends on the selection of negative supply voltage.

On Tapeout 1, each bias was controlled with a separate voltage supply. V_{B1} (CE Base voltage supply) =1.8V, Vc1 (CE collector voltage supply)=2.1V, V_{E2} (CB

emitter voltage supply)=- 4V, and V_{C2} (CB collector voltage supply)=1.35, 1.6, 1.85V depending on the load line. A 0.35V drop was incurred on each collector from ballasting resistors used to ensure that the same current was being supplied to all the PA cells in the design. An 800 ohm pull up resistor was used for DC bias of the CE base, and a 90ohm pull down resistor was used to bias the CB device.

On subsequent tapeouts, the CE collector and CE base supply were tied together since relatively little current flows into the base of the transistor. The same magnitude of positive and negative voltages were used to reduce power supply complexity on future modules being made from these designs. On Tapeout 2, a collector supply of 2.1V was used to bias CE collector and base and the CB collector. A -2.1V supply was used for the CB emitter. The pull-up, pull-down, and ballasting resistors were resized accordingly. On Tapeout 3, each cell contained two of the 4x6μm HBTs. This amplifier still used the same biasing scheme, voltage, and current density. As a result, the base pull-up resistor was reduced in length by a factor of 2. Other resistances were reduced by a factor of two by placing two resistors in parallel to double the total PA Cell currents.

2.2-E MATCHING AND TUNING NETWORKS

The goal of RF tuning networks in this design was to provide impedance matching on the input of the device so that maximum power is transferred from a 50ohm system to the transistor. On the output, the transistor load line and the saturated output power of the PA cell was more critical than output impedance matching for the overall circuit

goals.

The Input was matched with an L/C tuning network. The input to the 4x6μm CE HBT has an S11 near the real axis on the left side of the Smith Chart. By adding a series L, shunt C, the impedance at 220GHz can be transformed to near 50ohms. For an inductive element, a high impedance transmission line sized to be the narrowest possible wire according to design rules on metal 4 was used. According to simulation, this inductive transmission line had a characteristic impedance greater than 90ohms. The MIM capacitor was contacted with vias from metal 4 to metal 2 and the capacitor top metal with the other plate being the ground plane. Impedance transforming the input impedance of the transistor to 50ohms can be optimized by adjusting transmission line lenth and MIM capacitor area to minimize S11 at 220GHz. The 220GHz Smith Chart tuning path is shown.

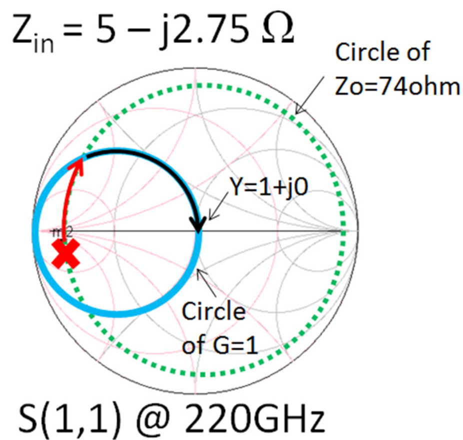


Fig. 26. Smith Chart: PA Cell Input Tuning

For the output, RF tuning was done to provide the proper load line impedance to the electron current source in the transistor. The transistor's collector-base capaci-

tance and other parasitics related to routing the signal from the device to the metal 4 layer through the hole in the ground plane can be considered as a part of the tuning network. To design this tuning network, a pi section is designed to transform a 50ohm impedance to the load line impedance. The pi section adds a series high impedance transmission line as an inductive element and a shunt MIM capacitor as the capacitive element. The resulting tuning network is compact.

The resulting transistor load line is viewed by tracing the instantaneous electron current and collector voltage on the transistor's IV plane. Depending on how a model is defined, the electron current can be found by measuring the current inside the collector-base capacitance of the HBT. If the model is a black box, a negative capacitance (same value as C_{CB}) can be placed in parallel with the collector base capacitance and readded after measuring current.

The instantaneous IV trajectory can be very telling with regards to the impedance seen by the transistor. A flat line implies a constant, real relationship between voltage and current and real impedance. If the load line appears to open up like an eye, it shows that there is energy storage and release through a wave cycle. This means that the impedance seen at the current source is a complex value. In order to operate over a linear load line, any non-zero reactance must be cancelled in the tuning network thus closing the eye. Final adjustments to the tuning network values are done by changing the values of transmission line length and MIM area while viewing the simulated load line versus the desired loadline and saturated output power.

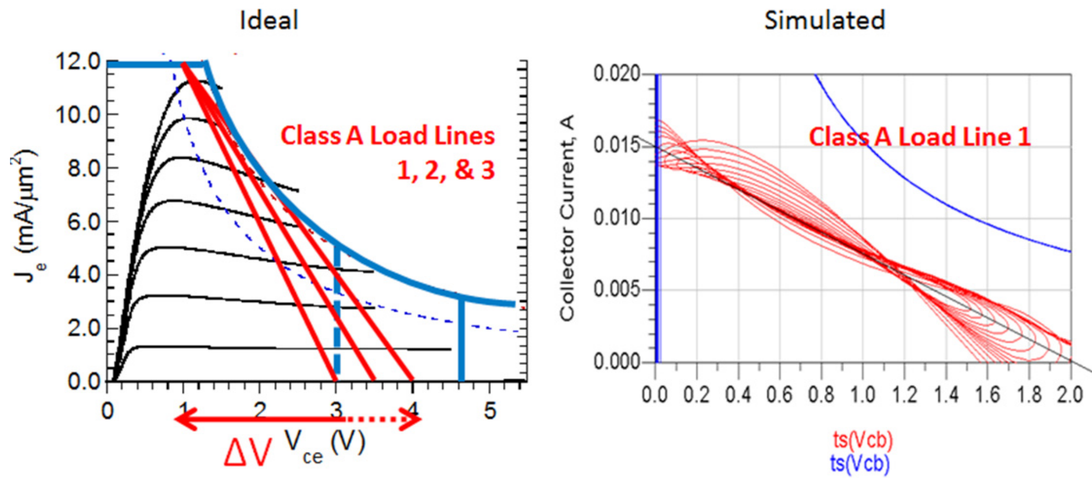


Fig. 27. Ideal vs. Simulated Load Lines

After creating a tuning network that shows best-case loadline, the input impedance of the tuning network is considered the optimal load line impedance. If other topologies for the tuning network are chosen, this impedance will still result in a best case load line for that class of amplifier.

Another method for finding the optimal load impedance sweeps a dummy impedance placed at the output of the transistor. Impedance is then swept over a large range on the Smith Chart, and power data is recorded to determine what power and efficiency results from all tuning network impedances. This experiment is considered a load pull. A tuning circuit can then be designed to provide the desired impedance at the output of the transistor.

The final output tuning network for the load line 3 (LL3) amplifier (3V and 17.5mA loadline) in Tapeouts 1 and 2 consisted of a 50μm-long transmission line in metal 4 and a 40fF capacitor to ground. Other load lines designed in Tapeout 1 were

within another 10µm of length of the LL3 size. The capacitance was within 10fF of the LL3 capacitance. The final input tuning network was a 10µm-long transmission line and a 23fF capacitor. Any remaining distance from the RF tuning networks to the edge of the PA cell was filled with a 50ohm transmission line sitting in the metal 3 layer. Metal 3 was chosen for the RF signal path to allow any necessary power supply feeds to pass over in metal 4. Power supply crossovers in metal 4 lay perpendicular to RF current flow in metal 3 to avoid any mutual inductance that could couple RF signal into the power supply or introduce power supply noise into the RF signal.

For Tapeout 3, a similar optimal load line impedance was used. In each PA Cell two 4x6µm-long common emitter and common base HBTs were used to make a cascode amplifier with twice the possible saturated output power. The goal of this was to double the HBT density to achieve double the RF output power within the same physical IC area. This presented some challenges with DC power consumption and heat dissipation.

In work done at Teledyne Scientific by Dr. Zach Griffith and Teledyne's thermal simulation team, thermal issues with high HBT density were considered [6]. As discussed earlier in the technology description section of this document, Dr. Griffith performed several experiments to determine the feasibility of multi-finger HBTs. He discovered that above 24µm of emitter length in the 4x6µm parallel HBT layout, high frequency performance and available gain dropped significantly due to transistor self heating. The successful demonstrations of 220GHz power amplifier MMICs in Tapeouts 1 and 2 showed that it was possible to place up to eight 4-HBT devices within

100μm center-to-center and still achieve strong gain performance with a full thickness InP substrate. Post-measurement thermal simulations showed that although the junction temperature was nearly 170 degrees C, the HBTs were able to dissipate heat through the substrate and through the direct metal connections to ground planes and large area capacitors in the design.

Further simulations were done for the higher density PA Cells in Tapeout 3 with the closest common-base, 4x6μm HBTs being placed 30μm center-to-center. Results showed that transistor self-heating would increase significantly for a design on full-thickness InP substrate. On a wafer thinned to 2 mils (~50um), simulations showed successful heat sinking through the InP substrate could successfully bring the junction temperature back near 170 degrees C in each 4-HBT device of these higher density circuits. Even with wafer thinning, these designs appear to be near a minimum HBT spacing for heat removal that is not small electrically at 220GHz [6].

For the Tapeout 3 PA Cell with two 4x6μm cascodes, having devices spaced distant electrically (30μm at 220GHz) means that the output and input tuning networks must be considered a three port tuning network being used for pre-power combining. Tuning network complexity increases dramatically: The network should provide the optimal impedance to each of the transistors that will result in the desired Class A load line. The network should also transform the transistor impedance sufficiently to reduce impedance mismatch at the output of the tuning network and transfer a high percentage power to the 50ohm load system.

There are three major challenges associated with designing this tuning net-

work (similar to the three challenges of match, losslessness, and isolation in all three port networks). First, the network must be symmetrical to generate the same amount of RF power from each HBT and provide the same impedance. Second, not only must the 50ohm impedance be transformed to the optimal impedance at the 1st HBT port, but the 2nd HBT port must be part of the optimal impedance transformation to the 1st port. Third, The two HBT ports should be isolated electrically to prevent RF power loss and avoid potential instability caused by feedback.

The Tapeout 3 8-finger HBT PA Cell featured a symmetrical tuning network that used an L-R-L path between the two 4x6µm HBTs to increase isolation between the transistors and stabilize the circuit. The L-R-L consisted of narrow interconnect feeding vias to a 100ohm resistor from each HBT port. The remaining two network paths connected the HBTs to the output with an LCLC tuning network. Each side of the tuning network also connected to a separate quarterwave choke for common-base collector DC bias to each 4x6µm HBT individually. To achieve the right impedance transformation, the two HBT ports were selected to have a port impedance equal to the small signal collector impedance at full bias.

The input matching network was designed to achieve a small signal match to the common emitter HBTs at 220GHz. Since the two 4x6µm CE HBTs were placed closer than their CB counterparts, the input feeds were smaller electrically and the tuning network required less complexity. The bases of the common emitter were fed with a high impedance line and those came together into a lower impedance line about twice as wide as the base feed interconnects. This lower-impedance transmis-

sion line's length was adjusted so it's delay would place the resulting input impedance on the circle of constant normalized G=1 on the admittance Smith Chart. A shunt tuning capacitor was added to bring the input impedance to the system impedance of 50ohms.

In addition to input/output tuning, inductive peaking was considered between the CE and CB HBTs to boost overall amplifier gain. Before adding any inductive element, the parasitics associated with the interconnects between the transistor ports and the transmission line metal layers are considered. In addition, the model for the DC blocking capacitor is considered in this inter-stage quasi-matching network. It was determined that adding any additional elements between the CE and CB actually reduced the overall MAG/MSG of the cascode. In addition a short path resulted in the best MAG/MSG for the amplifier.

2.2-F CIRCUIT, LAYOUT, AND EM SIMULATION

Layout and Electromagnetic Simulation starts very early in the MMIC design process at 220GHz. At these frequencies, even an extra 2µm of interconnect length can create a significant change in impedance. Some components, including quarterwave chokes, are large electrically and physically. Early floorplanning can give the designer an idea of what physical area and shape each choke, capacitor, and tuning network can take.

After an initial circuit simulation is run with ideal components, the designer can begin replacing each of the ideal components with EM models of layout components and EM models of other interconnects not considered in the ideal simulations.

In all the tapeouts of the PA MMICs designed here, single-component EM simulations were done using ADS Momentum, a 2.5-D electromagnetic simulation tool included with Agilent ADS. Compared to a full 3-D simulation, a 2.5-D simulation runs faster and sufficiently accurate models are generated for microstrip transmission lines and other planar circuits. In layout, polygons are designed for each layer in the lateral dimensions. The third dimension is defined by a substrate file that describes all the materials and their thicknesses. Within the substrate file, dielectrics are defined by their thickness, electrical permittivity, magnetic permeability, and loss tangent. Metals are defined by their thickness and their electrical conductivity. Bulk semiconductor is typically modeled as a dielectric. In the substrate files used for these tapeouts, the main dielectric used was BCB (Benzocyclobutene) with a relative dielectric constant of 2.7 and loss tangent of 10^{-5}. Gold conductors had a conductivity of 3.48×10^{-7} siemens/meter. The InP substrate had a dielectric constant of 12.7. The MIM capacitor dielectric silicon nitride had a 0.2μm thickness and a capacitance per unit area of 0.3fF/μm^2.

Given signal and ground ports placed in the design, S-parameters can be computed by running the simulator. The simulator breaks the entire design into a mesh that is sized much smaller than a wavelength of the highest frequency being simulated. Electric and magnetic field relationships are solved for in each area of the mesh using material definitions and boundary conditions, then the mesh is sewn back together and a full solution of electric and magnetic fields is found for the entire structure. Then S-parameters are exported relating power flow among each of the user-

defined ports. The process is repeated for a variety of frequencies and S-parameters are interpolated for frequencies spaced uniformly across the user-defined frequency range.

A majority of the tuning effort is done with single-component EM simulations, because EM simulation of small area components can be done quickly. Besides RF paths, the RF chokes and power supply are also carefully simulated to ensure that there is no possibility of an out-of-band resonance that could lead to instability anywhere in the MMIC.

As full sections of the PA cell layout are finalized, EM simulation of groups of local components and further adjustment can be done to model any remaining interaction between nearest neighbor passive structures in the design. If the amplifier is still performing as desired, the full PA Cell minus active parts can be simulated for EM interactions among interconnects, power supplies, chokes, and tuning networks. Since this simulation takes the most computational power and time (up to a day or more for the tapeouts described here), care should be taken to assure a working design before reaching this step.

2.2-G 2:1 COMBINER DESIGN

Design of the two-to-one (2:1) power splitter and combiner was very similar in design to the Wilkinson power combiner. In the Wilkinson power combiner, two totally different signals can be summed together. If each port is a 50ohm system, the design includes two quarter wave transmission lines at 70.7ohms—transforming 50 to

100ohms and isolating combined ports for the even mode signal. The two 100ohm impedances are placed in parallel to create a 50ohm impedance. In order to isolate the two ports being combined for the odd mode signal, a 100ohm resistor is typically added between the two ports.

In the 250nm InP HBT interconnect stack, an 8.2µm-wide, 70ohm transmission line on metal 4 with a metal 1 ground plane is used for quarter-wavelength transmission lines. No odd mode suppression resistor is added for this Wilkinson-like design, since the signals being split and combined are in-phase. This reduces overall electrical length each combined signal must travel and the combined ports can be placed a half guide wavelength apart. In Tapeouts 1 and 2, the ports are placed 400µm apart—below the half guide wavelength of 430µm in this design. The design was simulated in ADS Momentum to verify electrical performance.

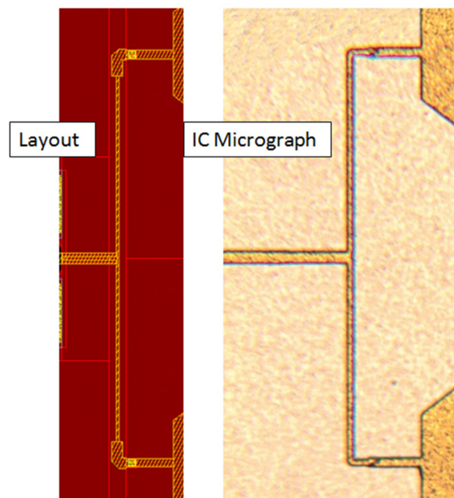


Fig. 28. Layout and IC Micrograph View of 2:1 Combiner

In simulation, this combiner had a 0.7dB insertion loss per splitter/combiner. However in measurement, the loss was slightly lower at 0.6dB loss per combiner due to an overly-conservative loss computation by Momentum [14].

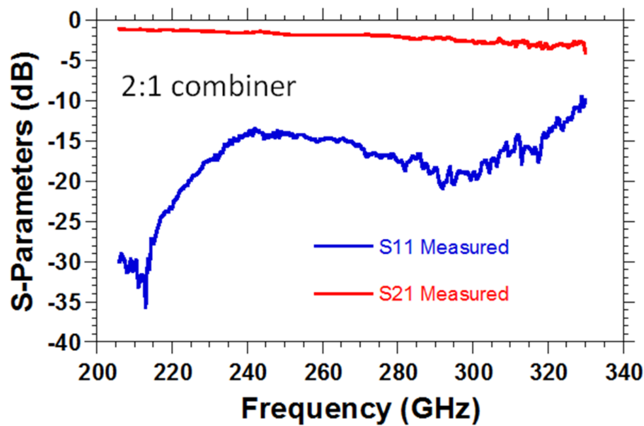


Fig. 29. S11 and S21 of Back-to-back 2:1 Combiner
The combiner showed 1.25dB loss back to back.

2.2-H 4:1 COMBINER DESIGN

The 4:1 combiner used in Tapeouts 1-3 was designed with inspiration from Dolph-Chebyshev power combiners demonstrated in coplanar waveguide [7]. The main idea is to use less-than-quarter-wavelength paths to feed the same amplitude of power to each of four 50ohm ports. The four ports are spaced at 100um, meaning that the shortest path from the inner and outer ports is different. However, by adjusting the shape and width of the transmission lines, the relative amplitude of power is equalized. The resulting sum port is then be tuned to 50ohms using a short L-C network. The resulting combined ports have a simulated return loss around 8dB while the main port return loss is near 20dB.

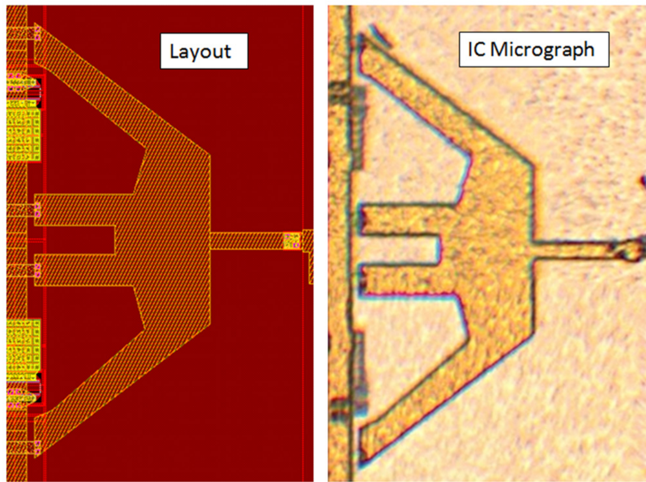


Fig. 30. Layout and IC Micrograph View of 4:1 Dolph-Chebyshev Combiner

When placed back-to-back, this power combiner had an insertion loss of 1.3dB at 220GHz [14]. Again this is less than the simulated value because of an overly conservative loss calculation. The back-to-back measurement is important for the overall amplifier because each PA Cell offers a similar gain and phase change to the signal assuming similar loading across the inner and outer PA Cells. This power combiner was successfully demonstrated in 4- and 8-cell power amplifier MMICs.

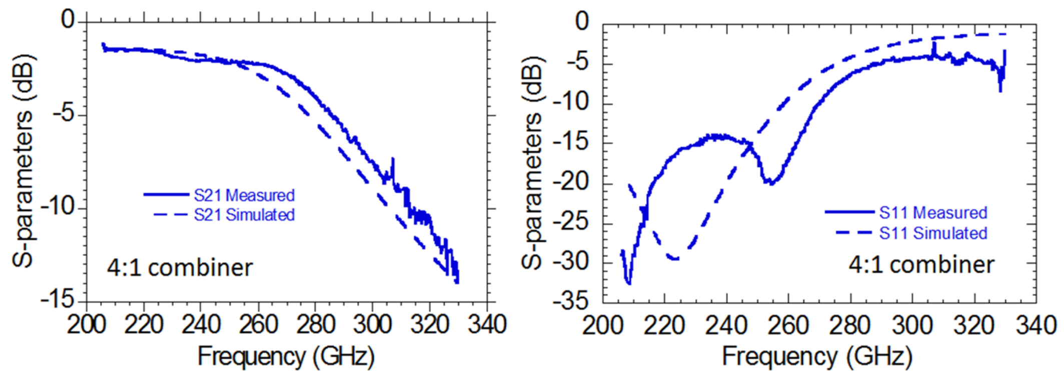


Fig. 31. S-parameters for Back-to-back 4:1 power combiners. Measured vs. Simulated

An updated 4:1 power combiner was designed for 220GHz PAs in Tapeout

3. One concern for the first 4:1 combiner was the phase and impedance difference between inner and outer PA Cells in multi-stage MMICs. The new 4:1 combiner was designed with four PA Cells spaced 120µm apart and sought to provide a better impedance match at 220GHz at all 5 ports. The design places two of the four 50ohm ports in parallel to create one 25ohm port. A quarter-wavelength, 50ohm transmission line is used to transform the impedance to 100ohms. And the two 100ohm ports are placed in parallel to create a 4-port 50ohm impedance and a 4:1 combiner.

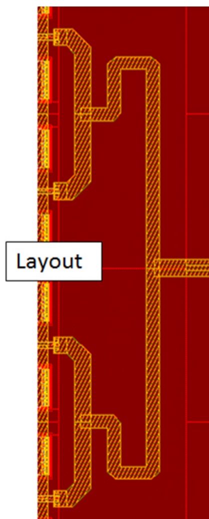


Fig. 32. Layout of New 4:1 Combiner used in Tapeout 3

In simulation, the 4:1 combiner has an insertion loss of 1.6dB. The return loss is over 10dB for each of the four combined ports. The return loss of the main port is more than 15dB. No RF data is yet available for this part.

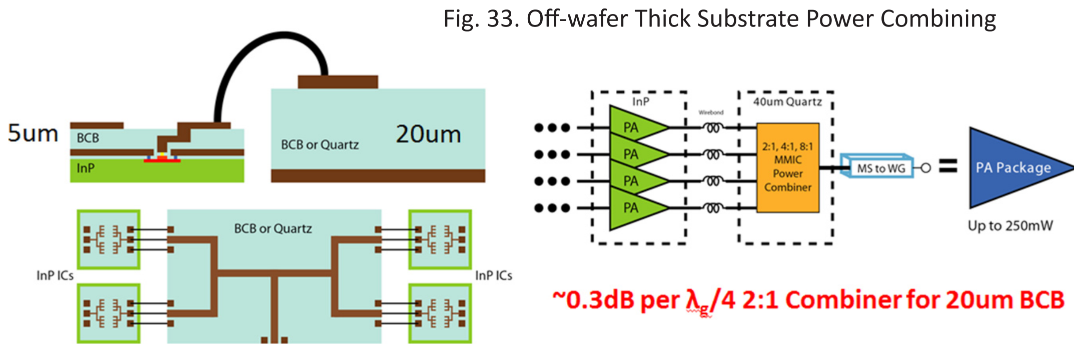
2.2-I OFF-WAFER COMBINERS FOR LARGER POWER

Additional power combining on wafer will require transmission line lengths much greater than a quarter wavelength. For Tapeout 3, an additional level of 2:1 combin-

ing is done. However any additional power combining will incur so much loss, that no additional saturated output power will be added by additional PA Cell combining on-wafer.

Even after reaching a maximum on-wafer power level, off-wafer combining can offer a higher overall power level. One way to combine would be to employ Wilkinson power combiners (or other 2:1 methods) in a much larger geometry and incur less resistance per unit length. This could be done in a thicker, lowloss dielectric substrate. PA MMICs can be diced and mounted directly to such a board and power combined 8 or more times.

Fig. 33. Off-wafer Thick Substrate Power Combining



Another approach leverages waveguide technology for power combining. For the MMIC to be packaged for general use, it will likely need to be placed within a waveguide module. Initially, the transition to waveguide could incur 1.5-4dB of insertion loss, but the waveguide can be as low loss as .013dB per waveguide length. Signals can be summed two- or more-to-one using magic tees or by placing waveguide transitions in phase along the waveguide input.

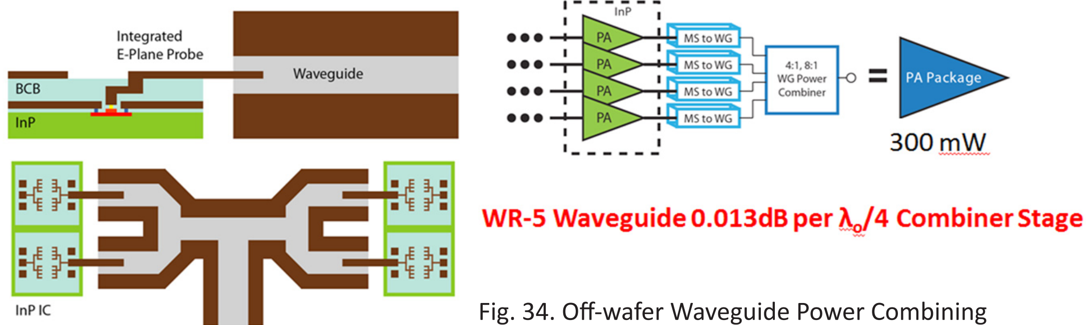


Fig. 34. Off-wafer Waveguide Power Combining

Depending on the desired application, free-space transmission of the high frequency signal may be required. On-wafer antennas have been demonstrated at lower frequencies and could be effective at 220GHz. Arrays of these amplifiers and antennas can be driven in parallel effectively power combining in free space.

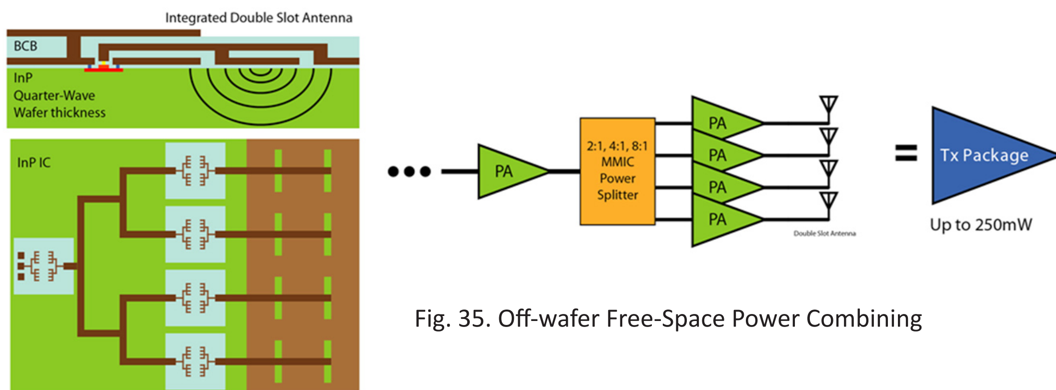


Fig. 35. Off-wafer Free-Space Power Combining

2.2-J PA MMIC SYNTHESIS

With a simulated PA Cell and a suite of power combiners, a multi-cell, multi-stage PA MMIC can be simulated and taped out. Between stages, tuned DC blocking can provide a 50ohm impedance on each side while ensuring the proper potential at output

of one stage and input of the next. Interconnects between the amplifier and RF pads are made with 50ohm transmission lines in metal 4 that are 12.5μm-wide. Full EM simulation of pads are included in final circuit simulations.

Power supply routing to DC pads is also modeled as transmission lines in simulation. This can help identify potential instabilities caused by the power supply. If detected, potential instabilities can be suppressed by adding resistive bypass to ground along the power supply line. In Tapeout 2 designs, power supply simulations showed potential instabilities around 60GHz caused by addition of the power supply network. After adding several shunt 5ohm + 270fF RC structures to ground, the potential instabilities were suppressed. The reason behind adding a 5ohm impedance instead of strictly an ac short is that oscillations may be occurring as a result of ground plane geometry, or long stretches of un-bypassed power supply. Added capacitance (energy storage) keeps any undesirable impedance near the edge of the Smith Chart—which is more likely to be an unstable region. The 5ohm resistor brings any undesirable power supply impedance further inside the Smith Chart and provides a loss mechanism for unwanted waves on the power supply line.

At the MMIC level, a variety of experiments were performed for each tapeout. During Tapout 1, experiments were designed to explore the three load lines described earlier in this section. In addition, multi-cell amplifiers were designed to verify the effectiveness of on wafer combining techniques. Versions with 1, 2, 4, and 8 cells were placed on the maskset for each load line. Passive structures including back-to-back versions of the power combiners were also included on the maskset.

On Tapeout 2, further gain was desired at the highest power levels to fully saturate the power amplifiers. 4- and 8-cell amplifiers of the LL3 (3V swing) load line were designed with 1, 2, and 3 stages. The amplifiers were all placed within a standardized RF/DC pad frame to enable waveguide packaging of these parts. Standardized voltage supply values were used for these designs at +/- 2.1V.

Designs from Tapeout 3 were created to demonstrate a higher HBT count PA Cell. New power combiners and other structures were designed to reduce combining losses and combine power from up to 16 PA cells and achieve up to 400mW of power on wafer. The new passive structures were also placed in breakouts to measure their individual performance. For multi-port passive structures, a 50ohm load termination was developed to enable measurement of the impedance seen from each port.

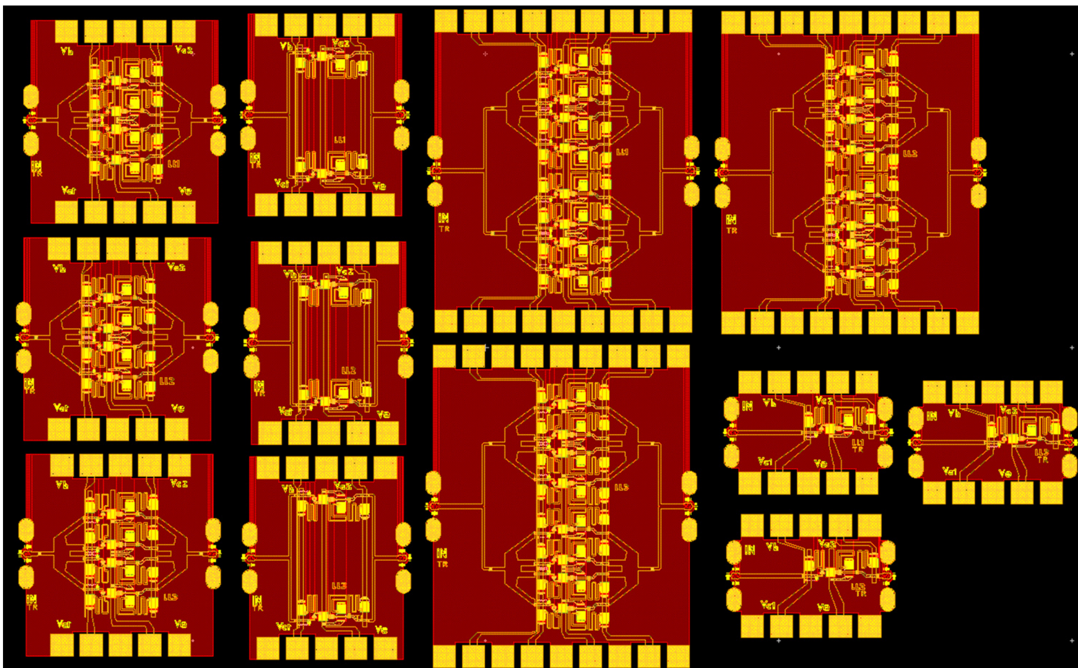


Fig. 36. Layout Library for Tapeout 1
2-, 4-, and 8-Cell PAs are designed with LL1, LL2, LL3 Load Lines.

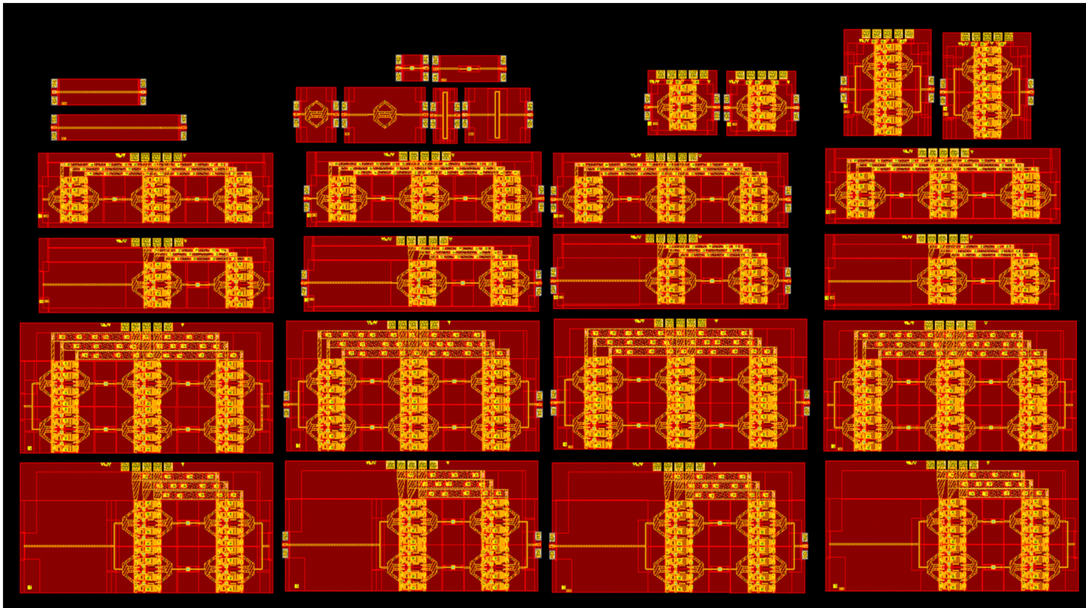


Fig. 37. Layout Library for Tapeout 2

4- and 8-Cell LL3 PAs. 2- and 3-Stage PAs are taped out with GSG pads & waveguide transitions.

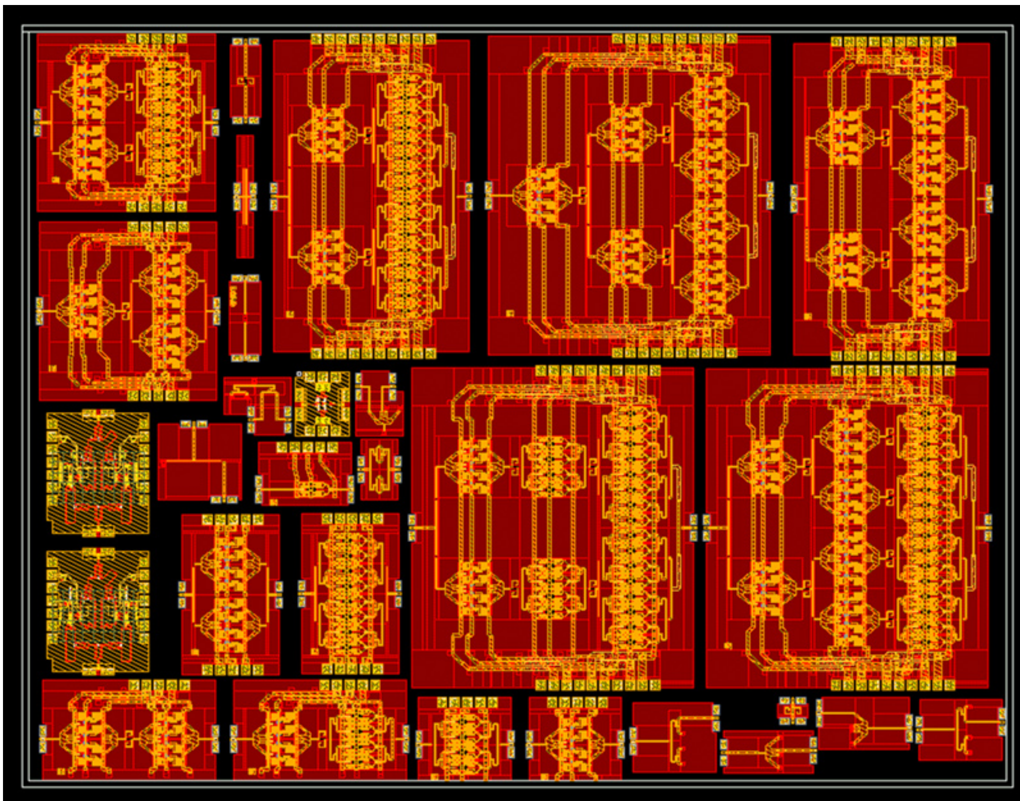


Fig. 38. Layout Library for Tapeout 3

4-, 8-, and 16-Cell PAs are designed using the previous PA Cell and a PA Cell with 2x HBT periphery.

2.2-K EFFICIENCY ACCOUNTING IN AN 8-CELL PA MMIC

The theoretical power added efficiency of a Class A power amplifier is 50%. Additional DC power consumption and RF loss decrease the overall efficiency of the amplifier MMIC.

In this work, DC power consumption is much larger than the transducer power dissipation in the PA output transistor. For the cascode, the DC power consumption is the DC power consumed within common emitter and common base HBTs and the power consumed in any resistors used for biasing the circuit. In the 4-HBT cell designed for Tapeout 1, The common emitter stage was biased with a VCE of 1.76V and a collector current of 33.6mA. The four bases were biased at 1.18mA through an 800ohm resistor. The base power supply was 1.8V and the collector supply was at 2.1V. 10ohm resistor with a corresponding 0.34V drop was used to ensure equal division of current from the power supply. The base-emitter diode voltage drop was 0.85V for a total DC power consumption in the common emitter of 72.7mW.

In the common base HBTs, the emitter was biased with 35mA and the diode drop was again 0.85V. A -4V voltage and a large resistor was used to bias the emitter. The base current was 1.3mA at a 0V potential. The collector was biased at 33.8mA and 1.5V for a total VCE of 2.35V. The collector power supply was at 1.85V with a 10ohm resistor to ensure equal current spreading. This collector bias resistor had a 0.35V voltage drop. The total DC power consumption on the common base side including ballast resistors was 202.5mW. This makes the entire PA cell DC consumption equal to 275mW for a single PA Cell.

The portion of the VCE used for class A quiescent bias was 1.5V. The remainder was used for base-emitter bias and knee voltage. The current used for bias was the entire 33.8mA. Using this information, the maximum RF voltage and current swing for class A operation is 3.0V and 67.6mA. This corresponds to a theoretical RF power of 25.4mW from a 4-HBT device or 6.34mW per HBT finger.

In simulation, an 8-cell power amplifier shows 6.25mW per HBT finger. RF losses also decrease the total output power and power added efficiency. Losses are incurred in the tuning network, cell transmission lines, and power combiners. In an 8-Cell PA simulation, the 4-HBT device showed an output of 25mW. The tuning network and additional 50ohm transmission line had 1.3dB loss bringing output power at the cell level to 18.6mW. The 4:1 combiner had 0.53dB loss bringing the total power of four cells to 66mW. The 2:1 combiner showed 0.49dB loss in simulation for a total power of 118mW. All totaled, 2.29dB loss was observed from the HBT to the MMIC level. For more detail, see figure 39 and 40 below.

Although the resulting efficiency is lower than optimal, DC power was traded off with design risk. The resulting 118mW RF output power and 2.2W power consumption for 8 cells results in a collector efficiency of 5.4% and is in line with measurement of fabricated ICs. It is clear that greater DC power optimization is possible by reducing resistor size and power consumption and by choosing a single transistor amplifier topology. Further optimization of efficiency can be done by reducing losses in the output tuning network of the PA Cell.

8-Cell Output Stage

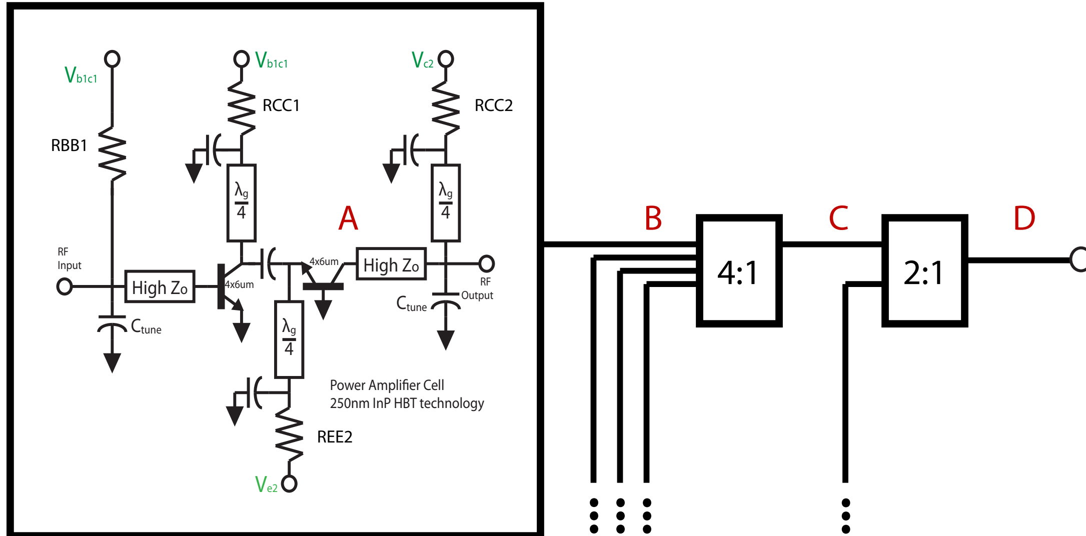


Fig. 39. Schematic diagram of an 8-Cell SSPA with detail shown of a single PA Cell

Cell Component DC Voltages & Currents	Assoc. Power (mW)	RF Transducer Power	Assoc. Power (mW)	RF Losses from Tuning Networks & Combiners	Assoc. Power (mW)
Resistor Power----------		CB HBT DC Power (VCE*Ic)	634	Point A HBT RF Power	200
RBB1 (.95V@9.44mA)	8.97				
RCC1 (.34V@269mA)	91.46				
REE2 (3.15V@281mA)	882	Common Base VBE*Ic	230	Point B RF Power at Cell Level (1.3dB RF Tuning Loss)	149
RCC2 (.35V@270mA)	94.5	Common Base VCB*Ic	404		
---Total Resistor Power	1077				
		Ideal Class A RF Power	202		
Transistor Power--------				Point C RF Power at 4-Cell Level (0.53dB 4:1 Combiner Loss)	132
Common Emitter HBT VCE=1.76V, Ic=269mA	473	Point A Actual HBT RF Power	200		
Common Base HBT VCE=2.35V, Ic=270mA	634			Point D RF Power at MMIC Level (0.49dB 2:1 Combiner Loss)	118
---Total Resistor Power	1107				
Total 8C PA DC Power	2184				
				Ratio of MMIC RF Power to DC Power	5.4%

Fig. 40. Efficiency Table of DC power consumption and RF power losses in an 8-Cell SSPA
The points of reference for power listed in this table refer to the points A, B, C, and D in Fig. 39. Currents and power levels shown in the table refer to currents and power levels observed in simulation for all eight PA Cells.

2.3
SSPA Measurement and Calibration

2.3-A DESCRIPTION OF S-PARAMETERS

S-parameters can be used to characterize transistors and circuits in the small signal/linear region of operation. Compared to Z- and Y-parameters, which would require perfect current or voltage sources and therefore perfect open and short circuits over a wide bandwidth, S-parameters can be measured using a finite, non-zero system impedance. S-parameters are heavily used in RF transistor modeling and circuit design precisely for this reason. Once S-parameters are obtained, matrix manipulation can be used to convert S-parameters into Z-parameters, Y-parameters, hybrid parameters, or an ABCD matrix. Transforming the data among these other forms is particularly useful in generating a high-frequency transistor model by de-embedding series and shunt parasitic components one-by-one in the model. Once device models are developed, amplifiers are designed and fabricated.

Two-port S-parameters describe the interactions of the amplifier's ports with the generator and the load. Power at a single frequency is sent to the design under test (DUT). This forward travelling wave is measured in terms of a normalized volt-

age wave. The magnitude and phase of the normalized voltage wave can be computed from the power level and the system Zo—typically 50ohms. Waves coming out of the amplifier back to the generator or to the load are called reverse waves. The reverse waves' magnitude show the circuit's response to the stimulus from port 1 or 2.

S11 is a ratio of the normalized voltage of the reverse wave coming from port 1 to the normalized voltage forward wave going into port 1 given that the source driving port 1 is the only port turned on. One major component of S11 (especially in unilateral circuits or circuits with low feedback) is the reflection of power directly back to the source. In an amplifier this reflected power is the amount of power that is never transferred to the DUT. Similarly, S22 in an amplifier shows the fraction of power being transferred from the DUT to the load.

S21 is a ratio of the normalized reverse voltage wave travelling toward port 2 from the DUT to the normalized forward voltage wave travelling to the DUT from port 1 with a power source only at port 1. In amplifiers, this is the gain of the amplifier. It's opposite, S12 represents the isolation of the input, port 1, from the output, port 2. A completely unilateral amplifier has S12 equal to zero meaning that a signal can only travel in one direction. A non-unilateral system where the product of S12 and S21 is large enough can create a feedback loop gain large enough to support oscillations in the system. Such oscillations can generate spurious outputs and consume DC power meant to be used for RF amplification.

2.3-B VNA SETUP & CALIBRATION

S-parameters are measured on a Vector Network Analyzer (VNA). As of today, there are no wideband VNA's currently available that can measure above 110GHz. This is likely due to the difficulty in (1) generating a signal with sufficient power and linearity above 110GHz, but also (2) transferring the signal to the DUT using coaxial transmission lines. With the advancement of transistor technology, the generation of power over wider bandwidths for such testing is bound to continue, but coaxial limits may dominate. In order to ensure a good 50 ohm Zo, slot modes must be suppressed in a coaxial transmission line. This requires smaller geometries of cables for high frequency operation. Coaxial cables with small diameter are not only hard to create, but are less rugged and have greater resistance per unit length. Conductor losses increase with the square of frequency and demand higher performance and equalization from the attached system. At some point, choosing other options for signal transmission is wise.

As an alternative to wideband VNA setups with metal connectors, frequency extender modules (FEM) have become a common accessory for high frequency VNA systems. FEMs typically take a 10 GHz signal—low frequency compared to the up to and over 1 THz they may drive—and multiply the signal with doubler and tripler modules until reaching the desired band. The resulting harmonics that sweep these higher frequency bands are significantly lower in power and aim to cover a waveguide band. Compared to copper coaxial transmission lines, waveguides are much lower in loss per meter. Care is taken to choose the right size rectangular metallic waveguide. The size must be chosen so that the operating frequency is not below the cutoff

frequency of the waveguide's fundamental mode and not above the cutoff frequency of its higher order modes. Waveguide standards exist however. Metal WR-03 waveguides have a physical dimension of a 0.034x0.017mils2 (or 0.86x0.43mm2) cross-sectional opening and are used commonly in systems that operate from 220-330GHz. WR-05 covers the 140-220GHz band. The waveguide standards are listed in the table below.

Frequency Band	Waveguide Standard	Frequency Limits (GHz)	Inside Dimensions (inches)	Inside Dimensions (mm)
V band	WR-15	50 to 75	0.148 x 0.074	3.7592 x 1.8796
W band	WR-10	75 to 110	0.100 x 0.050	2.54 x 1.27
F band	WR-8	90 to 140	0.080 x 0.040	2.032 x 1.016
G band	WR-5	140 to 220	0.0510 x 0.0255	1.2954 x 0.6477
	WR-4	170 to 260	0.0430 x 0.0215	1.0922 x 0.5461
H band	WR-3	220 to 325	0.0340 x 0.0170	0.8636 x 0.4318
Y band	WR-2	325 to 500	0.0200 x 0.0100	0.508 x 0.254
	WR-1.5	500 to 750	0.0150 x 0.0075	0.381 x 0.1905
	WR-1	750 to 1100	0.0100 x 0.0050	0.254 x0.127

Fig. 41. Table of Waveguide Standards V-band and above

Frequency extender modules measure forward and reverse waves using waveguide directional couplers. This allows the multiplier chain to drive the DUT and stay isolated from the reflected wave. The complex values of the forward and reverse voltages are then measured from the coupled waves. This data is used to generate high frequency gain and impedance information.

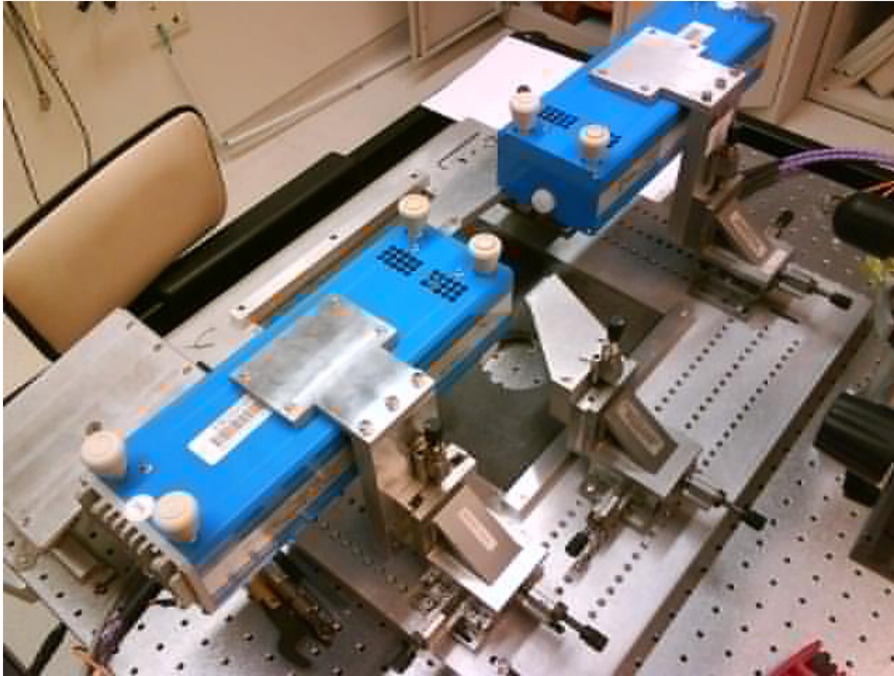


Fig. 42. Image of 220-325GHz OML Frequency Extender Modules

Given that the electronics and waveguides have limited operating bandwidth, a whole collection of FEMs must be purchased to get a full frequency response from the circuit. For example a 220GHz amplifier may be measured in the 210-325GHz band with WR-03 modules to capture in-band performance. Then WR-05, WR-10, and WR-15 FEMs must be used to measure 140-220GHz, 75-110GHz, and 50-75GHz respectively. The VNA can be used directly to measure DC-50GHz.

Calibration is the next step in producing reliable data. In some cases, data will be used to look at performance of a circuit or amplifier. In other cases, S-parameter data is used to produce device models. Device modeling measurements at high frequency will likely require continuity among waveguide bands and clear impedance trajectories on the Smith Chart. Single transistor performance is very sensitive to

small RF and DC changes compared to a circuit test. Device measurements require the highest requirements of calibration. For circuit measurements, sensitivity to the quality of calibration is lower.

The quality of calibration can be found by measuring the S-parameters of an impedance standard and comparing to the ideal case. When a 50ohm VNA system is calibrated and a Thru standard is measured, the ideal return losses (S11 and S22) are zero—or negative infinity dB. It would be expected that S12 and S21 on an ideal Thru standard would have no loss or be equal to 0dB.

2.3-C CALIBRATION TOLERANCES

In practice, even with system calibration, there is error due to the noise floor of the VNA leading to a limit on the precision of the measurement. Some of this error can be reduced with averaging multiple sweeps and selecting VNA power levels in the middle-upper part of its dynamic range. This will keep signals used for calibration high above the system noise floor. In order to take measurements precise enough for modeling transistors, the calibration of the VNA at high frequency must be sensitive enough to measure capacitors in the device model to within 0.1fF or less. For device measurements, models for InP HBTs have successfully been developed after achieving calibration with Thru standard S11 and S22 less than -30dB and Thru standard S12 and S21 greater than 0.05dB.

The requirement for VNA calibration for viewing circuit performance measurements is relaxed. For circuit measurements, the data will be used merely for pre-

sentation and comparison to simulation rather than for modeling of small device parasitic effects. Second, RF power levels for an amplifier may be more than 1000x larger than that used to drive a single, unmatched transistor. Data points in large-signal measurements will be less sensitive to noise or other disturbances. Thru-standard S11 and S22 may be tolerated at -20dB and S12 and S21 may be tolerated at +/- 0.1dB

2.3-D VNA CALIBRATION METHODS

There are a variety of Calibration methods. The purpose is to measure the effects of delivering a signal from the output of a network analyzer to a particular plane of reference through cables, transmission lines, waveguide structures, probes and transitions. For example an OML frequency extender head may be designed to have an internal 50ohm reference plane inside its directional coupler. The amplifier is to have a reference plane at the GSG pads where probes will contact the IC pads. When an amplifier is measured, signals from the coupler will go through a section of waveguide, a transition from waveguide to coplanar waveguide, see a shunt tuning stub, and transition from a PCB to floating GSG probe arms. The parasitic effects and delay of the path from DUT to measurement will change the amplitude and phase of S-parameters in the measurement. Calibration uses mathematical algorithms to effectively move the reference plane of the measurement to any user defined reference plane.

Common reference planes used in measurement include the end of a 50ohm coaxial cable at the point it connects to the DUT. Another reference plane could be the end of a waveguide flange that connects to another waveguide flange in the DUT. For

on wafer measurements, the reference plane could be the location where probes touch the DUT's pads or some offset distance away from the pads.

One calibration method that is common for circuit testing at high frequency is the Short-Open-Load-Thru (SOLT). This method uses data captured while providing an impedance standard at the reference plane of the system. For example, in on wafer measurement, an impedance standard substrate may be used to land 3-pronged Ground-Signal-Ground (GSG) probes onto impedance standards printed on the surface of the substrate. In this instance, the impedance standards would have short circuit to ground pads, an open circuit relative to the ground pads, a pair of resistors connecting the signal pad to ground pads (Load), and a standard connecting port 1 and its associated grounds to port 2 and its ground pads (Thru). Once these standards are measured correction factors are calculated and those terms are sent to the VNA. When the calibration is applied, the reference plane for the measurements displayed on the VNA will be located at the probe tips.

For higher frequency testing, Line-Reflect-Reflect-Match (LRRM) and Thru-Reflect-Line (TRL) [27] calibration can provide flexibility in having a reference plane far from the RF pads. These methods allow for an offset from the pads, where circuits and transistors can be isolated electrically.

This is important for transistor testing, because interaction between pads and transistors can impact measurements of transistor performance and device modeling. As an example of calibration offsets, a single common emitter transistor is measured on wafer using TRL calibration. When designed, its base is connected to the GSG pad

for port 1 with a 250µm-long, 50ohm transmission line. The emitter is grounded. And the collector is connected to the GSG pad for port 2 with a 250µm-long, 50ohm transmission line. The associated reference planes for port 1 and 2 are located at the transistor end of the two 250µm transmission lines. An associated Thru standard would appear to be 2 GSG pads separated by 500µm of 50ohm microstrip transmission line. The Reflect standard would look similar to the Thru, but have the 2 reference plane ports terminated with either an open or short to fully reflect the incident power. And the Line standard would be similar to the thru, but have the pads separated by 500µm plus some predetermined length of transmission line that is on the order of one quarter to one half of a wavelength for the band of interest.

Some technique and luck can be associated with getting a quality calibration. Calibration depends on the quality of the impedance standards purchased or fabricated. Technique comes from ensuring that the test bench is in good condition and the probes and the impedance standards are not in disrepair from repeated use. Technique also comes in to play when making contact with pads in general. When probes are landed exactly in the center of the pad every time, then uncertainty about the resistance, inductance, and capacitance seen at the probe tip can be reduced and that will be reflected in the resulting calibration.

The user can also increase the probability of achieving good calibration by ensuring that all probes (e.g. all ground and signal tips) are making good electrical contact with the impedance standards and with the DUT. Given that the probes themselves have all pins (e.g. ground signal ground) in the same plane, positioner/actua-

tor equipment can often be adjusted for probe arm angle relative to the plane that the wafer chuck and samples lay on. Probe planarity can be checked using a contact substrate. The probe is lowered onto the soft metal, lifted, and pulled back. By inspection, the user can see the marks left by the probe in the metal and determine if the probe is lowering parallel to the substrate.

2.3-E POWER SWEEP TESTING

A major part of measuring the performance of a power amplifier is to see how much power can be sensed at the output of the amplifier. In some instances a VNA could be used to measure power performance by running sweeps over the whole band and sequentially stepping up the power level of the VNA. However, most VNAs are set up to deliver only small power levels in the band of operation although the Agilent PNA appears to be able to deliver near 10dBm (10mW) in much of the 0.1-26.5GHz band. At high frequency, the maximum power levels being delivered to a DUT could be as low as -25dBm from a VNA in the WR-3 band (220-325GHz). Before the work reported in this dissertation, the only medium solid state power amplifiers that had been reported showed around 10dB gain and had output power measured from 5 to near 50mW (7 to 17dBm). In these instances, and for the work reported here, the VNA does not have enough power to drive these amplifiers into gain compression. This makes it clear that the VNA with frequency extender modules alone is not sufficient to show the large signal or power performance of these high frequency circuits.

220GHz large signal measurements can be performed using a frequency multi-

plier chain. A single-frequency signal can be taken from a standard signal generator at 12.2 GHz and multiplied in a series that includes a K-band diode tripler, a W-band diode tripler and an H-band doubler. The WR-4 H-band doubler is tuned for maximum power at 220GHz. This system available from Virginia Diodes, Inc. makes power generation possible at 220GHz. Using the 220GHz PAs as a driver, frequency multiplication could again extend current technologies to reach even higher frequencies.

One might question why a power amplifier at 220GHz would be important given that a power source already exists at that frequency. A distinction must be made between systems that operate with fully fundamental tone circuits and those that use multiplied signals. In system designs using the multiplier chains, the original signal carrying data is then multiplied up to the desired frequency but with great amounts of conversion loss. The result is that with each mixing, the noise floor creeps nearer to the signal. Any data has a higher probability of getting distorted and the bit error rate increases significantly. In fundamental tone circuits, much smaller reductions in signal-to-noise ratio are incurred. In addition, diode triplers and doubler are possible with nearly any new transistor/diode technology.

For measuring power levels, a calorimeter has been developed by Erickson. Their power meter is fed by waveguide and detects power levels over a huge frequency band—several GHz to several THz. RF power is detected by measuring the temperature increase of a material that heats when hit with high frequency waves. Although the sensor is wideband, the measurement can be relatively frequency selective, by choosing the proper waveguide sections for signal transmission. Spurious signals

below the waveguide cutoff do not propagate in the waveguide. Signals higher-order waveguide modes have a more lossy path in the waveguide (note: above single mode operation, the transistor has less than 0dB available gain).

In the following image, the power bench setup is shown. The multiplier chain has a WR-4 waveguide flange which connects through a waveguide probe to the DUT. The output of the DUT drives power into the output-side waveguide probe. A wave-guide transition mates with the power sensor's WR-10 waveguide and the RF power flows to the calorimeter.

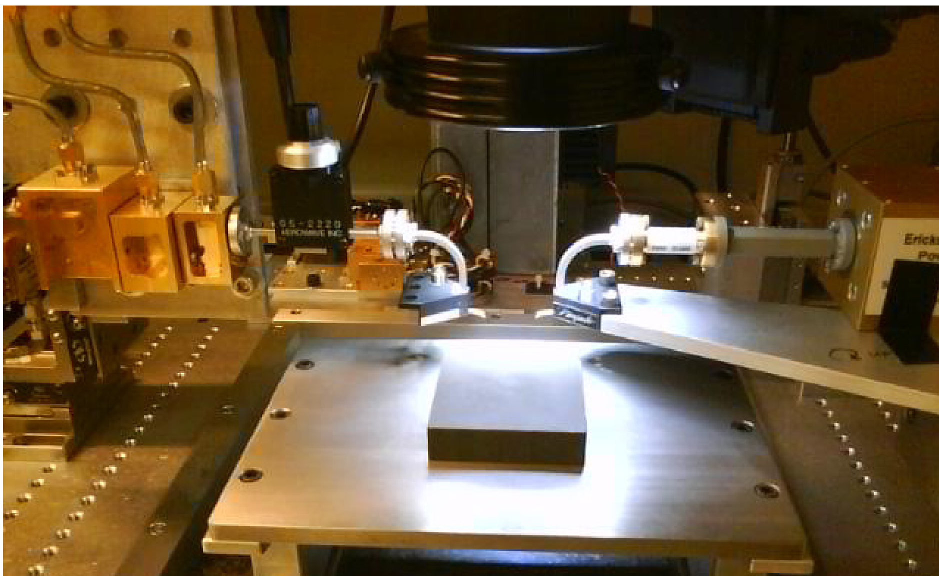


Fig. 43. Image of VDI Multiplier Chain and Power Test Bench

2.3-F POWER SWEEP

A power sweep can be performed by incrementing the 12.2 GHz RF power level on the signal generator to increment the 220GHz power at the DUT. The signal genera-tor frequency can be adjusted to provide power at each of the desired frequencies near the multiplier chain RF center frequency (e.g. 210-230 GHz all have significant power

levels from the VDI power source). Calibrated data can provide information about P1dB, saturated output power, and compressed gain under high RF drive.

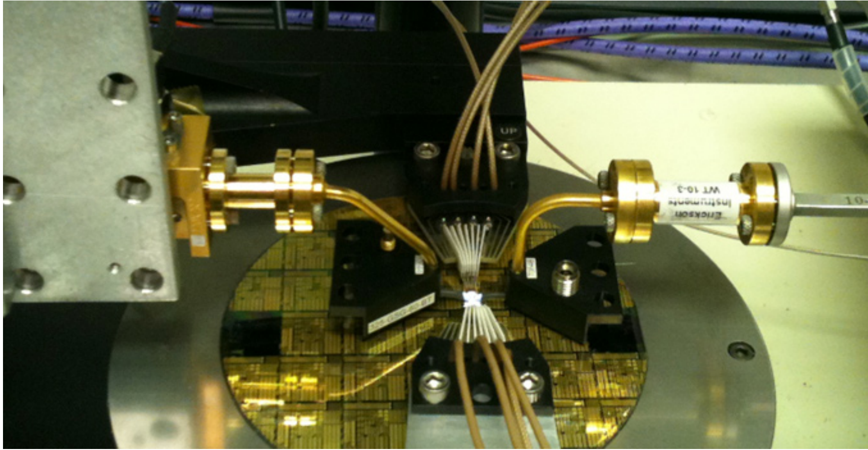


Fig. 44. Image of wafer probes contacting the processed InP wafer

2.3-G CALIBRATION OF THE POWER BENCH

The Power Bench is much less sophisticated than the VNA setup. In this case, calibration takes the form of computing loss in each of the passive components leading to and from the DUT. After measuring passive components and the whole system including the DUT, a spreadsheet program can be used to compute the resulting RF input power and RF output power with a reference plane at the pads of the DUT.

To compute the losses associated with the setup, a thru impedance standard can be used in conjunction with the rest of the setup discussed. The 220GHz signal is first measured with the multiplier chain waveguide flange directly connected to the power meter. This shows the maximum RF input drive power. Any other sections of waveguide/tapers used in the final setup are placed between the multiplier chain and the power meter and power data is recorded. Finally, the probes are attached and the full system is used to measure the power from the Thru standard.

Loss from additional waveguide sections is the first measured power minus the second. Loss from both probes is the second measurement minus the third. An assumption is made that both the waveguide probes have equivalent amounts of loss. So the DUT input power is the multiplier chain power minus the loss of one probe. The DUT output power is the measured power plus the loss in any added waveguide sections and the loss of one probe.

Care must be taken to do multiple point power sweeps during calibration because, the diodes in the power source do not operating linearly. It is important to note what signal generator power levels at 12.2 GHz corresponds to a particular power level at 220 GHz.

3
Results of HiFIVE PA MMICs

3.1-A RESULTS OF HIFIVE 1 PA MMICS

Twelve InP HBT Power Amplifier MMICs were submitted for mask assembly on December 15, 2010. A wafer lot finished processing in early May 2011 and PA MMICs were power tested on May 14, 2011. The amplifiers were tested as described in the section of this document devoted to high frequency measurement methods.

3.1-B LOAD LINE COMPARISON & 2 CELL PA

The 2-cell amplifier shown above was biased at I_{C1} = 66mA, I_{C2} = 66mA, V_{C2} = 1.85 V, Vc1 = 2.1V, V_{E2} = -4.1V, and V_{B1} = 1.82 V. The measured gain, as shown below, at 220 GHz is 10.9dB with a local maximum of 11.8dB at 206 GHz with S21 dropping 3dB below peak at 248 GHz [14].

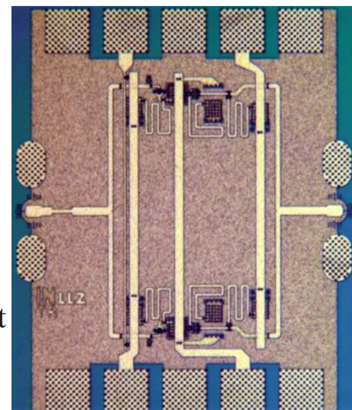


Fig. 45. 2-Call PA Image

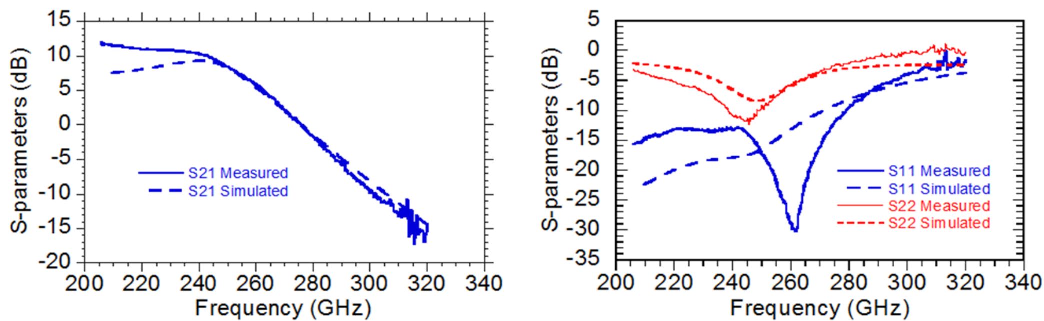


Fig. 46. 2-Call PA S-parameters, measured vs. simulated

Output Power measurements were taken using a WR-5 VDI multiplier chain centered at 200GHz and a WR-4 multiplier chain centered at 220GHz.

In power testing, the 2-cell amplifier was held at the same bias as for RF testing. The LL3 design showed 26.3mW of saturated output power at 208GHz. The power sweep for all three 2-Cell Amplifiers is shown below. The LL3 design consistently showed greater output power than LL1 and LL2 designs.

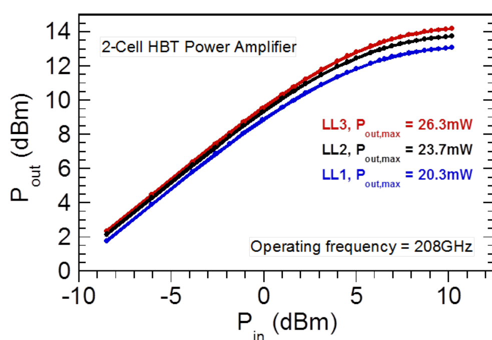


Fig. 47. 2-Call PA power sweep comparison among three load lines

3.1-C 4-CELL AMPLIFIERS

The small signal gain of the LL3 4-cell amplifier is shown below With I_{C1} = 132mA, I_{C2} = 132mA, V_{C2} = 1.80 V, Vc1 = 2.1V, V_{E2} = -4.2V, and V_{B1} = 2.10 V, the measured

gain at 220 GHz was 10.1dB. The 3dB bandwidth extends from 206GHz to 254GHz [14].

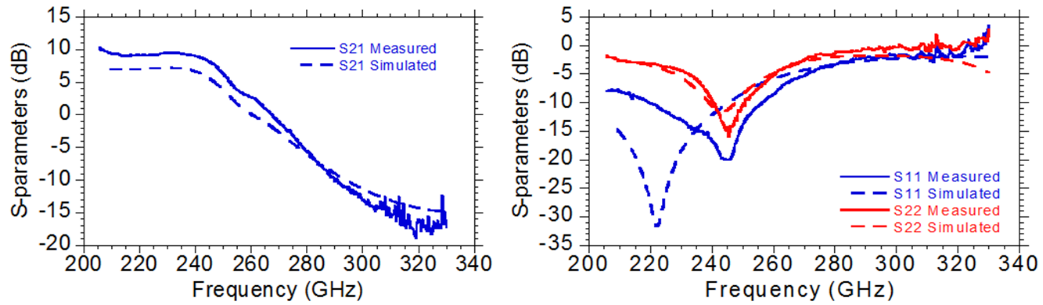


Fig. 49. 4-Cell PA S-parameters

For P_{IN} vs. P_{OUT} measurements, the 4-cell amplifier was biased under the same conditions as for RF testing. The 4-cell SSPA had an output power of 48.8mW and a gain of 4.5 dB at 220GHz. See the plot below for 220 GHz power sweep results. The output power and gain vs. RF input frequency is also shown below. Results show that the 4-cell amplifier can produce greater than 48mW of output power over 210-220GHz.

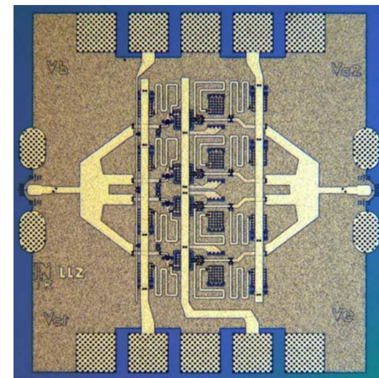


Fig. 48. 4-Call PA Image

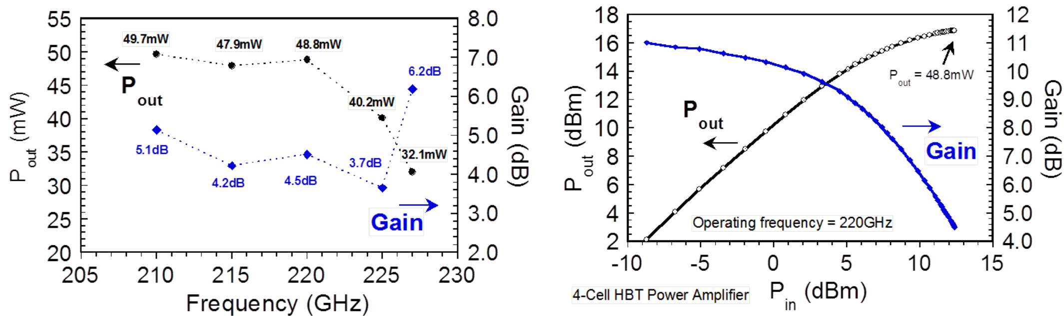


Fig. 50. 4-Cell PA power and gain vs. frequency (left) and 220GHz power sweep (right)

The preceeding results demonstrate the effectiveness of the design methodology to synthesize an operating PA cell. In addition, both the two- and four-to-one power combiner structures are demonstrated and match well with simulation. The larger amplifiers demonstrate using both of these levels of power combining in a single PA MMIC.

3.1-D 8-CELL AMPLIFIERS

For S-parameter measurements on the Agilent 8510 with frequency extender modules, the DC bias conditions of the 8-cascode-cell PA MMIC are: V_{B1} = 1.8V, Vc1 = 2.1V, I_{C1}= 260mA, V_{E2} = -4.2V, V_{C2} = 1.8V, I_{C2} = 262mA. The figure below shows the S-parameters of the 8-cell SSPA. At 220GHz, the gain is 8.9dB, and at 217GHz the peak gain is 9.1dB. The 3-dB bandwidth extends from 206GHz to 242GHz [15].

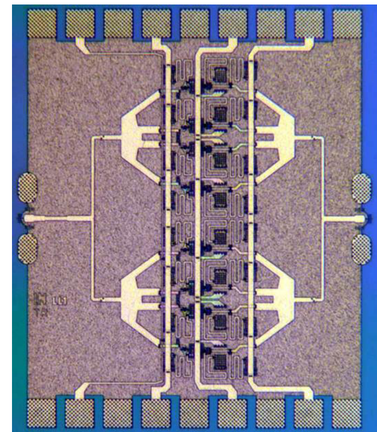


Fig. 51. 8-Call PA Image

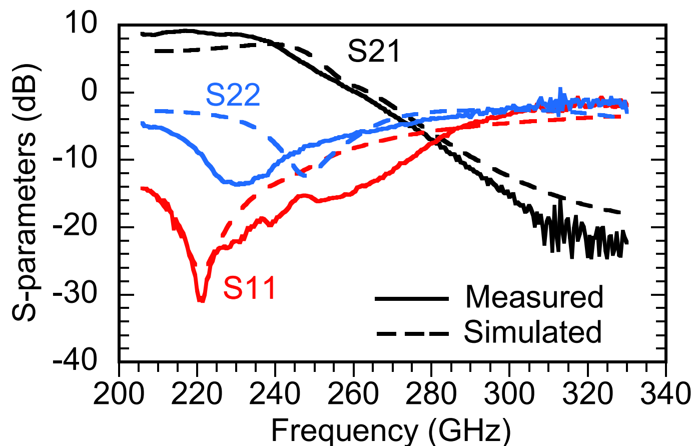


Fig. 52. 8-Call PA S-parameters 206-325GHz

A power sweep was performed at 220GHz with the 8-Cell SSPA. Unlike measurements shown for the 2- and 4-cell amplifiers, source power was insufficient to drive the amplifier into saturation. However, heavy gain compression was observed.

Under the aforementioned DC bias conditions, the 8-cell SSPA demonstrated 58.4mW output power with 5.4dB compressed gain at 220GHz. At 215GHz, 66.1mW was measured with 6.6dB gain. The figure below shows the SSPA P_{OUT} and gain from 210-227GHz, where at least 50mW of output power is measured from 215-225GHz.

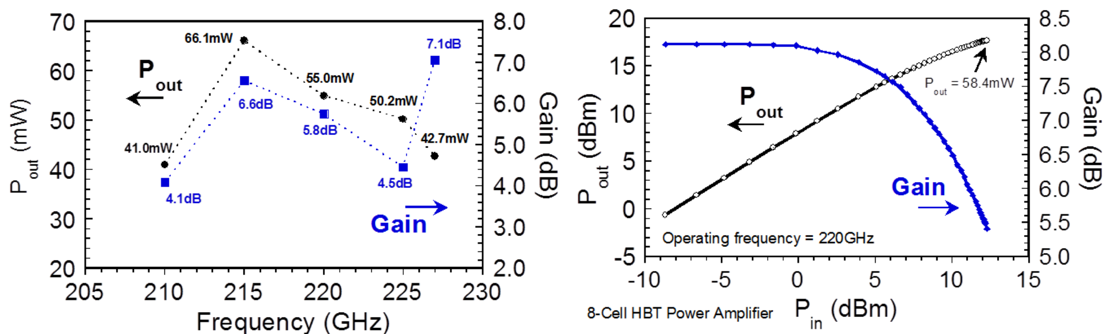


Fig. 53. 8-Cell PA power and gain vs. frequency (left) and 220GHz power sweep (right)

3.1-E TAPEOUT 1 CONCLUSIONS

This set of designs showed the potential for first-pass design success with this maturing 250nm InP HBT process. These designs demonstrated the ability to use multiple levels of power combining to combine power from large numbers of PA Cells on wafer. Source power limitations didn’t allow all SSPAs to be driven fully into compression. Future work considered additional gain blocks to overcome the available power limitations at 220GHz.

3.2-A RESULTS OF HIFIVE 2 PA MMICS

Tapeout 2 represented an effort to increase the overall gain of the PA MMICs while remaining at the same saturated output power levels. In order to accomplish this, PA blocks similar to those used in Tapeout 1 were cascaded for additional gain. From Tapeout 1, the 4- and 8-Cell PAs were updated with the LL3 load line (3V swing).

The amplifiers in Tapeout 2 were re-designed to operate at +/-2.1V power supply rails for reduced module power supply complexity. The metal interconnect stack was adjusted to a thicker 3µm metal 4 layer. PA designs were also placed in standardized pad frames to standardize the physical size and pad placement of the IC. The 4-cell multi-stage amplifiers were placed in one pad frame with a physical size of 2.24mm x 0.71mm. The 8-cell multi-stage amplifiers were placed in a pad frame with a physical size of 2.42mm x 1.22mm.

Designs for HiFIVE-2 were officially submitted on November 17, 2011. Wafers finished early February 2012. RF testing began February 8, 2012.

3.2-B 4-CELL MULTI-STAGE PAS

Four Cell, 2-stage amplifiers had a DC power consumption of 2.00W. The S21 of the 4-Cell 2-Stage was 16.4dB at 220GHz with a 3dB bandwidth extending from below 210 to 242GHz.

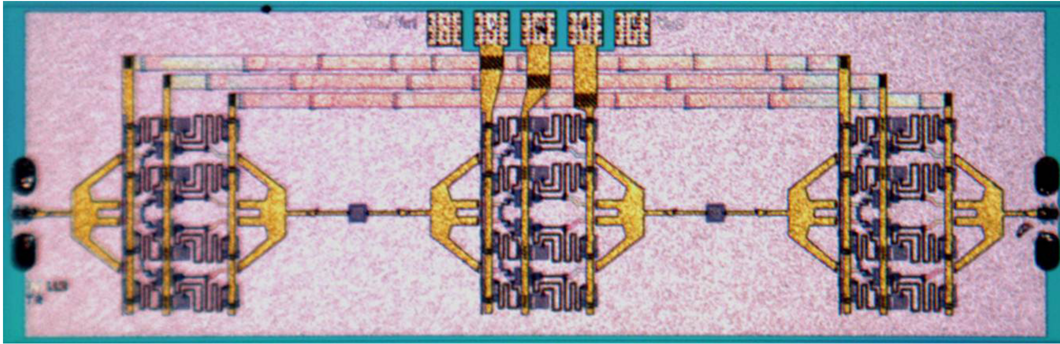


Fig. 54. 4-Call, 3-Stage PA Image

The DC power consumption of the 4-Cell, 3-Stage PA shown above is 3.38W. At a DC bias of VC1 = 2.75V, I_{C1} = 462mA, V_{C2} = 2.35V, I_{C2} = 443mA, V_{E2} = -2.2V, and IE2 = 462mA, the S21 gain of the 3-stage, 4-cell SSPA MMIC at 220GHz is 26.8dB. Figure 4 shows the measured S-parameters for the amplifier. The 3-dB bandwidth extends from at least 210GHz to 235GHz [17].

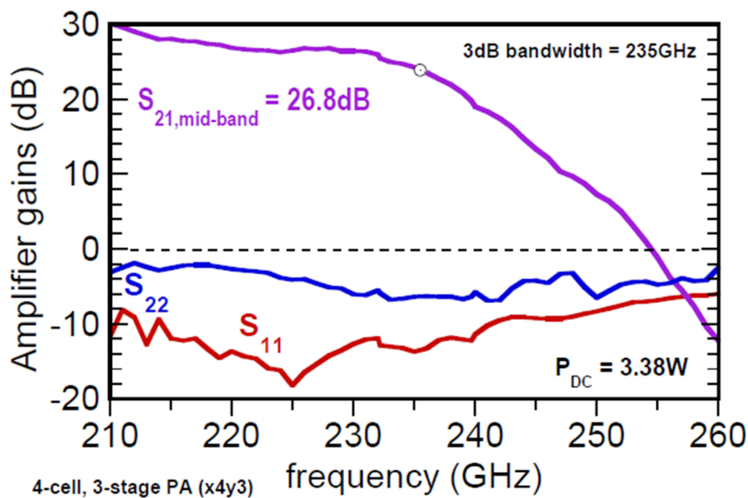


Fig. 55. 4-Call, 3-Stage PA S-parameters 210-260GHz

With the same DC bias conditions as used to capture S-parameters, the 3-stage, 4-cell SSPA MMIC was tested for power performance. Power measure-

ments from 205-235GHz are shown below. The data suggests a 5% downward shift in load line tuning from 220 to 210GHz. For 2.0mW P_{IN} at 220GHz, the amplifier P_{OUT} is 59mW (1.68% PAE) and the compressed gain is 14.7dB. From 205-225GHz, the SSPA MMIC P_{OUT} is greater than 50mW.

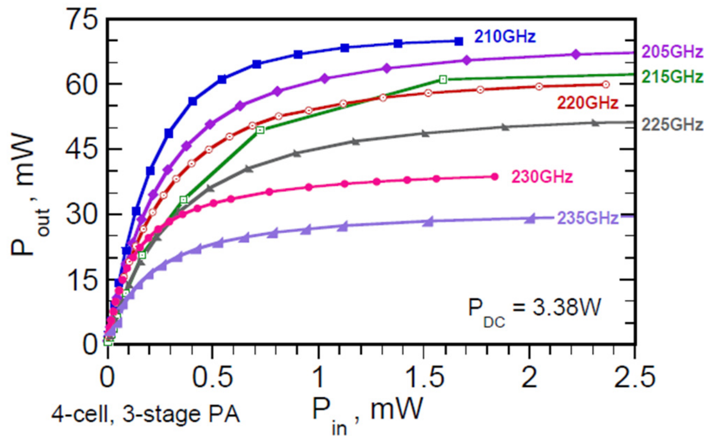


Fig. 56. 4-Call, 3-Stage PA Power Sweeps from 205-235GHz

3.2-C 8-CELL MULTI-STAGE PAS

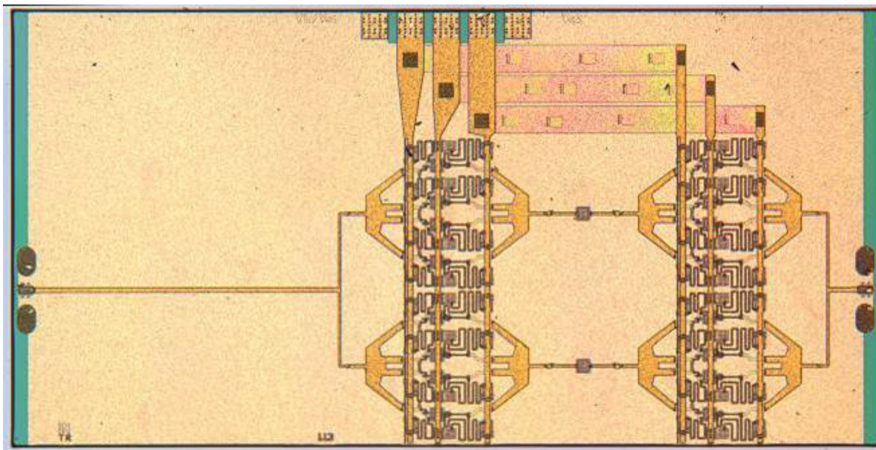


Fig. 57. 8-Call, 2-Stage PA Image

The 8-Cell, 2-Stage amplifier PDC is 4.46W. At a DC bias of Vc1 = 2.75V, I_{C1} = 599mA, V_{C2} = 2.3V, I_{C2} = 582mA, V_{E2} = -2.3V, and Ie2 = 609mA, the measured small

signal power gain of the 8-cell SSPA at 220GHz is 14.8dB. The plot below shows the measured S-parameters for the amplifier in two bands. The S21 gain is greater than 12dB from 142 to 240GHz and input return loss is greater than 10dB from 190 GHz to 260 GHz [16].

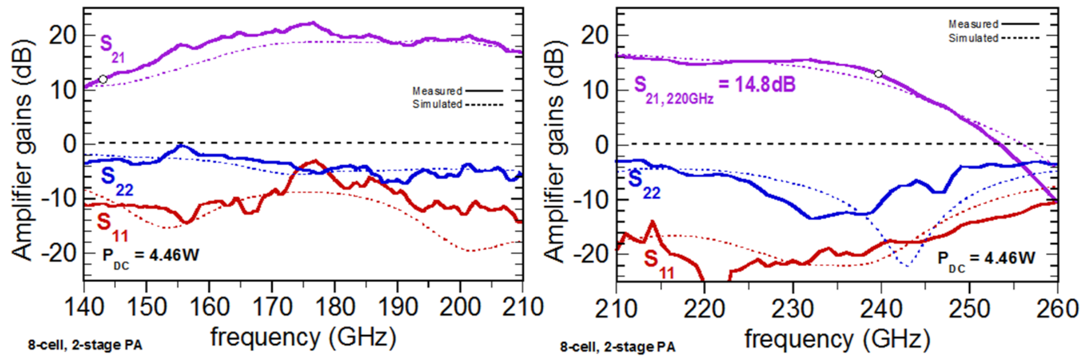


Fig. 58. 8-Call, 2-Stage PA S-parameters in two bands covering 140-260GHz

Using identical DC bias conditions from RF testing, the 2-stage 8-cell amplifier demonstrated 90mW output power P_{OUT} with 8.2dB compressed gain at 220 GHz (13.6mW P_{IN}). For an 8mW P_{IN} at 220GHz, the amplifier P_{OUT} is 80mW and the compressed gain is 10dB. From 210-225GHz, the SSPA has greater than 65mW saturated P_{OUT}, and from 210-220GHz the SSPA shows greater than 75mW saturated P_{OUT}.

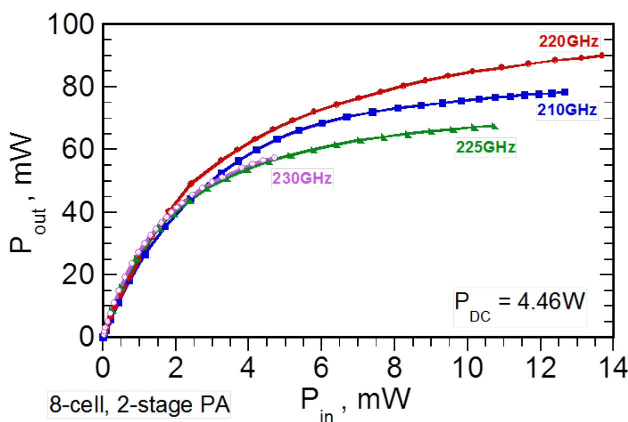


Fig. 59. 8-Call, 2-Stage PA power sweeps 210-230GHz

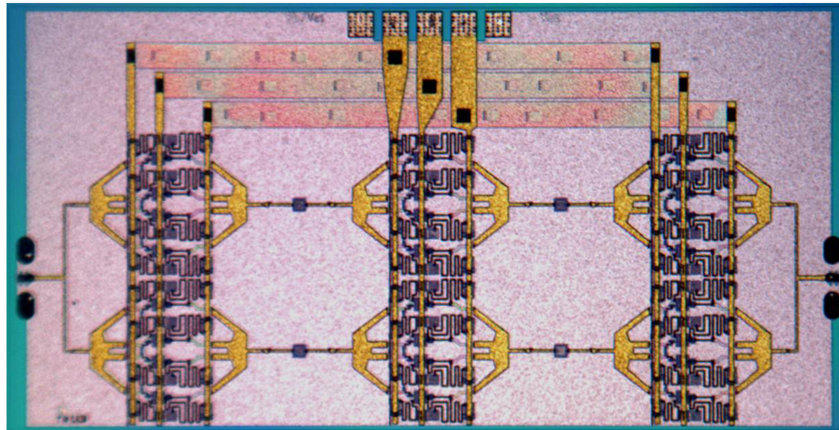


Fig. 60. 8-Call, 3-Stage PA Image

Eight Cell 3-stage amplifiers were also designed and included on this maskset. The DC power consumption at similar current densities and bias voltages was 6.46W. The S-parameters below show 22.3dB S21 gain at 220 GHz and higher gain at lower frequencies with 3-dB bandwidth up to 232GHz.

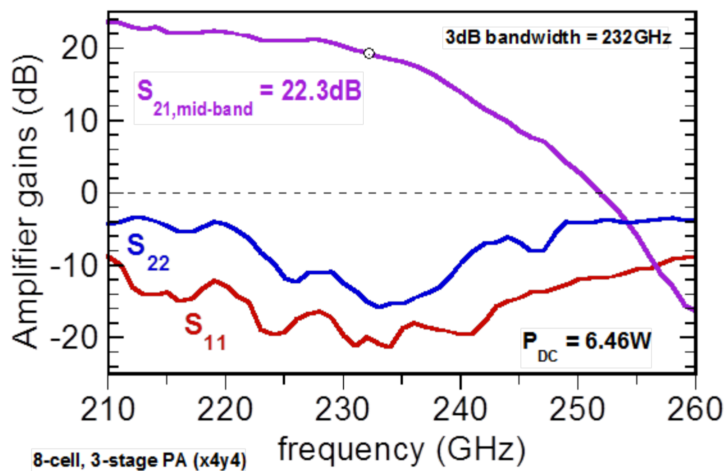


Fig. 61. 8-Call, 3-Stage S-parameters 210-260GHz

The power levels for this design were lower than the 8-cell, 2-stage amplifier. The power sweep showed a saturated output power of 73mW at 220GHz and a higher 83mW at 215GHz. Given a 1mW input, this amplifier output 55mW of power or over 17dB gain.

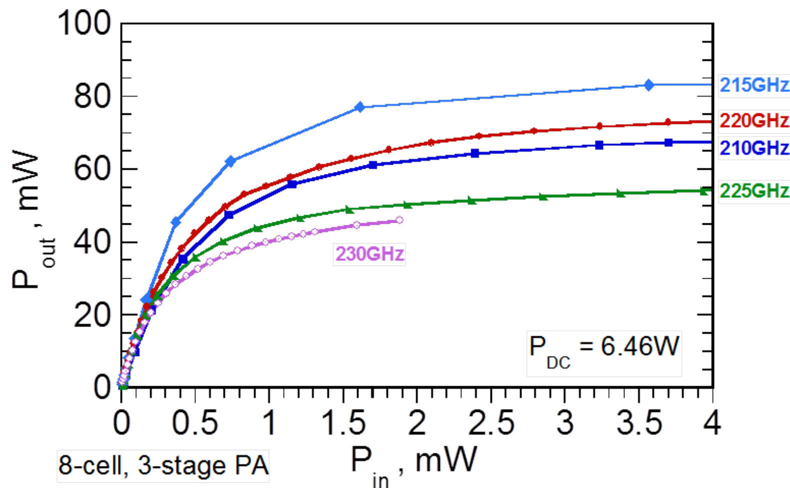


Fig. 62. 8-Call, 3-Stage Power Sweep Results 210-230GHz

3.2-D TAPEOUT 2 CONCLUSIONS

During testing, the 3-stage amplifiers reached power levels below those seen in simulation. This is likely due to the effects of phase mismatch between inner and outer PA cells in the 4:1 power combiner, with waveform distortion increasing with each additional stage. Low PAE was recorded for most of these multi-stage amplifiers, because of high DC power consumption in initial drive stages. But, with the added stages, the full saturated output power of the 8-Cell amplifiers was observed at 90mW.

3.3-A RESULTS OF HIFIVE 3 PA MMICS

The third set of HiFIVE SSPA designs was finalized at Teledyne Scientific on October 12, 2012. The first lot of wafers finished January 23, 2013 and a second lot finished in late February 2013. S-parameters of full-thickness circuits from lot 1 were taken on January 31, 2013. RF power measurements with forced-air cooling on lot 2 wafers

were taken March 8, 2013.

For Tapeout 3 a new PA cell was constructed to increase the HBT emitter periphery by a factor of 2. With some novel output tuning network design, the resulting PA Cell has is designed for double the output power of the previous PA cell designs. Updated power combiners will allow combining from up to 16 PA Cells. Smaller driver stages are employed to maintain the necessary overall amplifier gain, reduce DC power requirements, and increase PAE over previous results.

While S-parameter data is available to demonstrate that these circuits act as small signal amplifiers, RF power data that demonstrates the maximum power capabilities of this technology is still emerging. In small signal testing, it was clear that self-heating and reductions in device performance at full bias were occurring. For these amplifiers to work as designed, heat extraction with wafer thinning and mounting on a thermally conductive block must be executed before RF power testing. Preliminary RF power data was measured on a full-thickness wafer with top surface forced air cooled to between -40C and -15C.

3.3-B 16-CELL PA

The 16-Cell PA uses the previous PA cell used in Tapeout 2. A 4-Cell and 8-Cell PA operate as driver amplifiers for this design. The S-parameters are shown to have 25.09dB S21 gain at 220 GHz and a 3dB bandwidth from below 210 to 233GHz. S11

is below -10dB from 210 to 244GHz. The physical MMIC area was 2.22mm x 2.51mm and the DC power supplies were I_{C1}=960mA (V_{BC1}=2.55V), Ie2=-940mA (V_{E2}=-2.09V), and V_{C2}=2.65V for a total DC power consumption of 6.7W. Full-thickness, forced-air-cooled RF power data shows 123mW of saturated output power at 220GHz and 164mW at 214 and 208GHz.

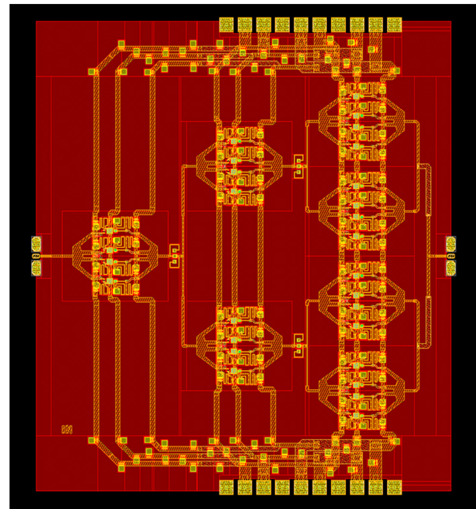


Fig. 63. 16-Cascode, 3-Stage PA Image

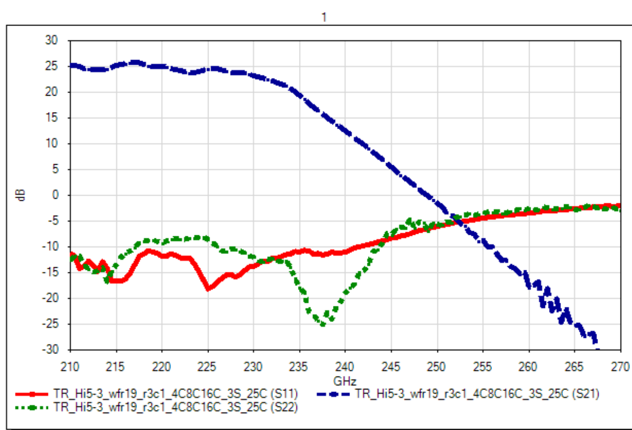


Fig. 64. 16-Cascode, 3-Stage PA S-parameters 210-270GHz

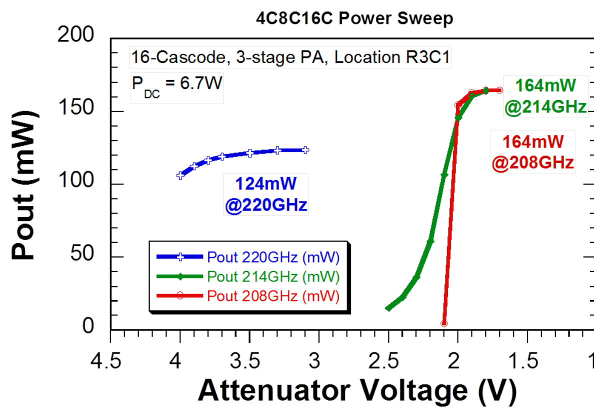


Fig. 65. 16-Cascode, 3-Stage PA Power Sweeps 208-220GHz

3.3-C 8-CELL PA USING NEW 8X6μm HBT

The 8-Cell PA using the 8x6μm HBT has the device periphery to provide up to 210mW of 220GHz power in simulations. This output stage is driven with an 8-Cell amplifier from Tapeout 2. The S-parameters are shown below. DC power supplies were I_{C1}=710mA (V_{BC1}=2.52V), Ie2=-840mA (V_{E2}=-2.2V), and I_{C2}=780mA (V_{C2}=2.44V) with a total DC consumption of 5.5W. The two stage amplifier on full-thickness substrate had 14.9dB S21 gain and a 3dB bandwidth up to 236GHz. The physical size of this two stage amplifier was 1.4mm x 1.4mm. RF power data was measured at the same bias at room temperature and with forced-air cooling. With no cooling, $P_{OUT,SAT}$,sat was 89mW at 220GHz, 98mW at 214GHz, and 109mW at 208GHz. With cooling, $P_{OUT,SAT}$ was 115mW at 220GHz, 144mW at 214GHz, and 118 at 208GHz—showing a 8-46% increase in saturated P_{OUT} with cooling.

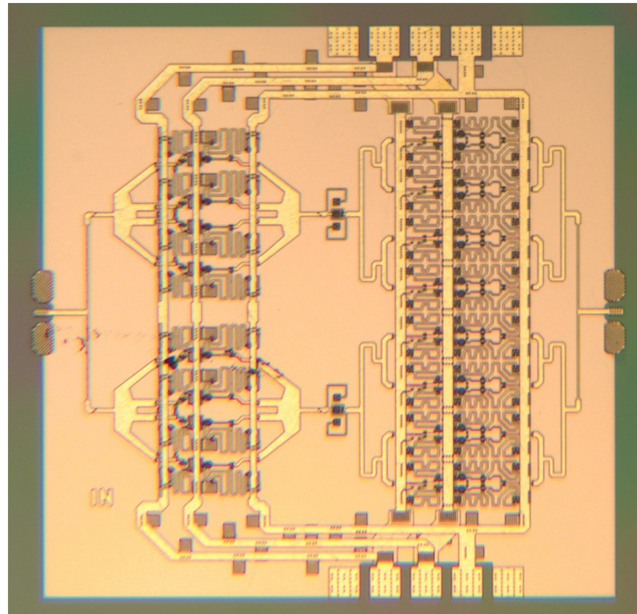


Fig. 66. 16-Cascode, 2-Stage with new PA Cell Image

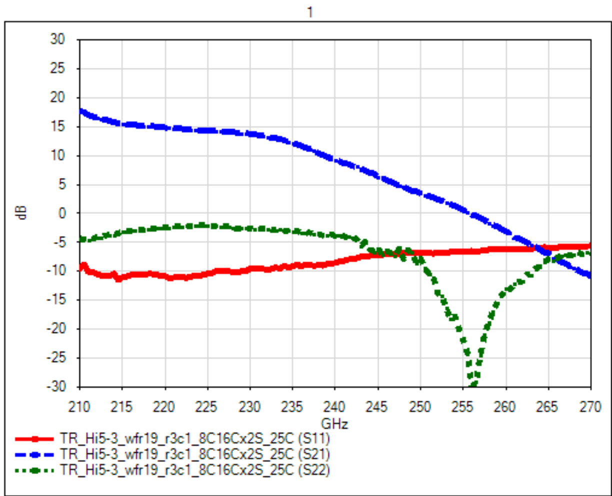


Fig. 67. 16-Cascode, 2-Stage with new PA Cell S-parameters 210-270GHz

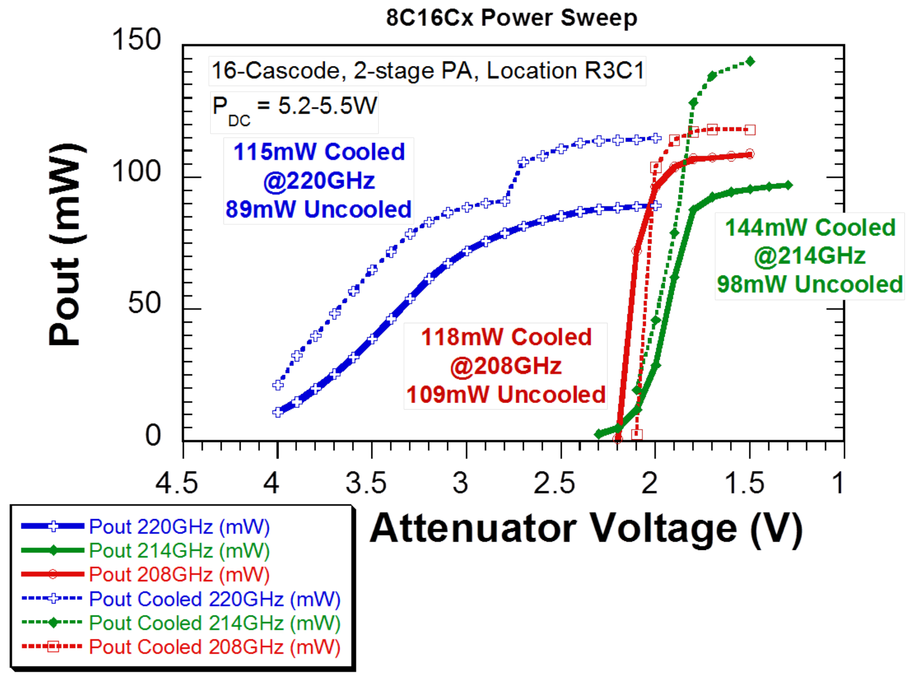


Fig. 68. 16-Cascode, 2-Stage with new PA Cell power comparison of cooled measurements

Forced cool air flowed to the top of the wafer during testing. Cooled power was 10-40% greater than uncooled.

3.3-D 16-CELL PA USING NEW 8X6μm HBT

This PA MMIC 16 of the new 8x6μm PA Cell designed for Tapeout 3 and uses the largest hierarchy of power combining. The physical size is 2.51mm x 2.22mm. If results from RF power testing mimic simulation, up to 400mW is possible from this

MMIC. S-parameters measured on a full-thickness substrate are shown below. 9.0dB gain is present at 220 GHz with a 3dB bandwidth from below 210GHz to 238GHz. The DC supplies were biased at I_{C1}=1.57A (2.64V), I_{C2}=-1.67A (V_{E2}=-2.35), and V_{C2}=2.85V for a total DC consumption of 12.9W.

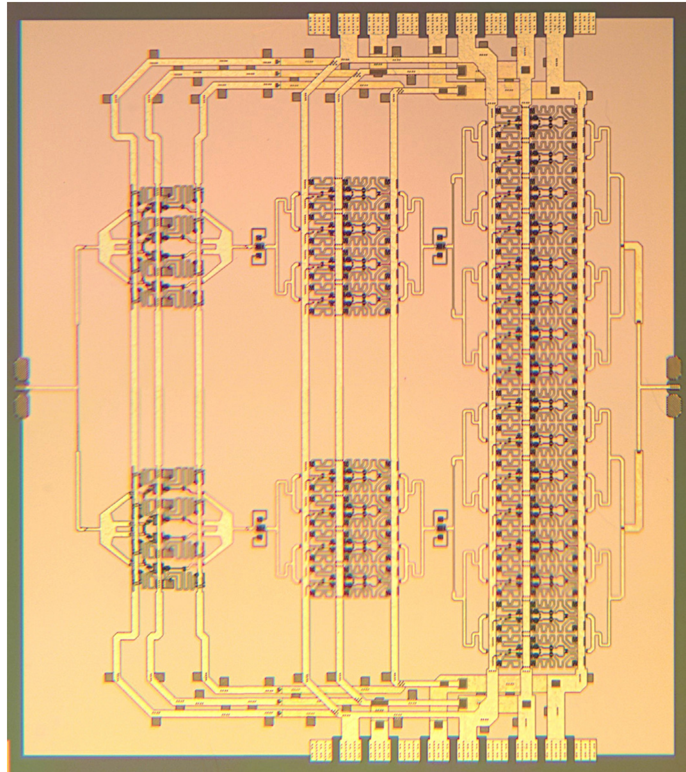


Fig. 69. 32-Cascode, 3-Stage PA using new PA Cell Image
This 8C16Cx32Cx uses the new PA cell on stages 2 and 3.

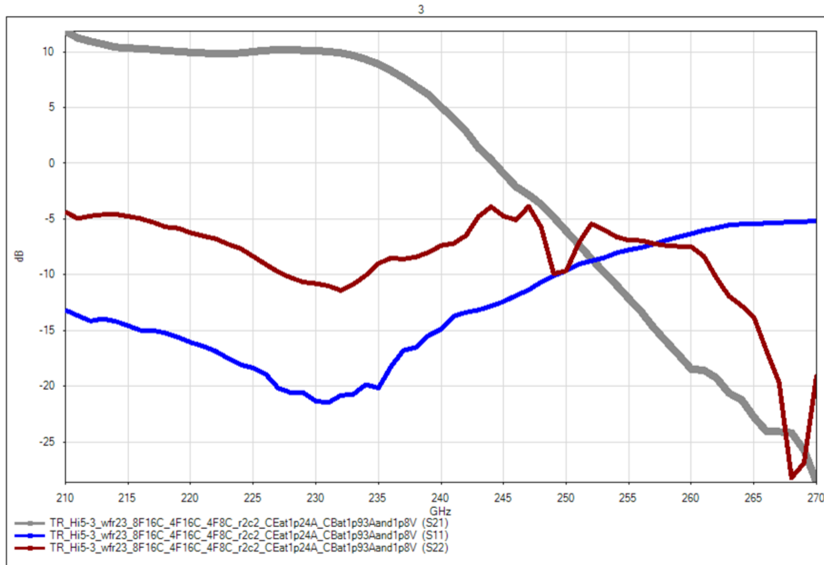


Fig. 70. 32-Cascode, 3-Stage PA S-parameters
These measurements were performed on a 8C16C32Cx that uses the new PA cell on stage 3 only.

RF power data was measured at the same bias and with forced-air cooling. $P_{OUT,SAT}$ was 157mW at 220GHz, 180mW at 214GHz, and 145mW at 208GHz.

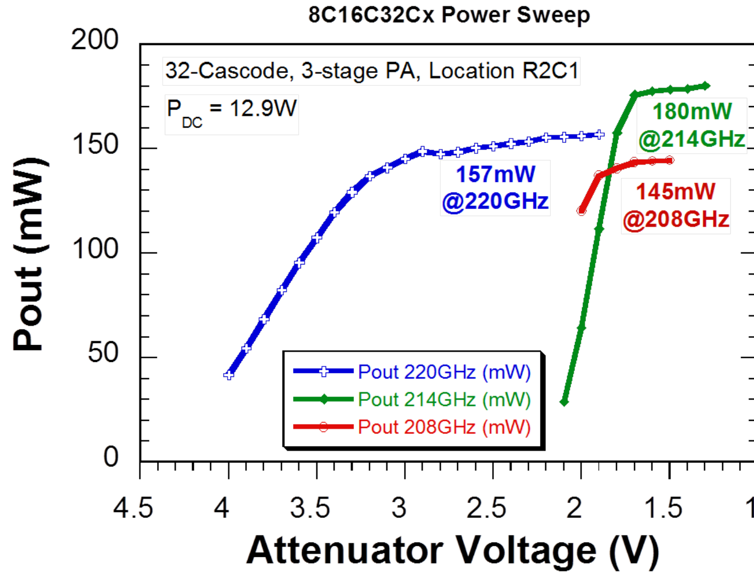


Fig. 71. 32-Cascode, 3-Stage PA cooled power sweep.
These measurements were performed on a 8C16C32Cx that uses the new PA cell on stage 3 only.

3.3-E TAPEOUT 3 CONCLUSIONS

The measurements in this section demonstrate that the amplifiers can bias and handle high DC power densities in a full-thickness substrate. Strong reduction in device performance as a result of transistor self-heating is observed in full-substrate circuits where nearest-neighbor HBT distance has decreased from 100µm to 30um. Wafer thinning, dicing, and mounting should be performed before reaching any final conclusions about the performance of these PA MMICs and the new design techniques used in Tapeout 3.

4
Future Work and Conclusion

4-A FUTURE MODULE CONSTRUCTION

The future of already fabricated 220GHz InP HBT PA MMICs is clear. In order to be useful in a system, the PA MMIC must be made available in a waveguide module. Care has been taken by others on this project to design a low-loss E-plane probe transition from microstrip to waveguide. Heat can be conducted into the metallic waveguide block. DC supply feeds can also be routed through the assembly.

4-B FUTURE MMIC WORK

Future PA MMIC work at 220GHz continues. Although large output power is very desirable, there are physical limits regarding the amount of DC power that can be produced and dissipated in PA module. Higher PAE amplifiers are critical to the success of such systems.

In order to achieve desired PAE levels, several ideas can be employed to increase RF output power density and decrease DC power consumption. To increase RF power, lower-insertion-loss tuning networks and power combiners can be imple-

mented. New schemes for power combining of four or more ports could be highly beneficial in this effort. Transistors with more available gain at 220GHz and the same breakdown voltage could eliminate the need for a cascode thus decreasing power consumption by 30-50%. Reduced headroom given to ballasting resistors could also provide DC power savings at the price of thermal stability.

Further updates could include higher-order PA class amplifiers. Although class D and E are attractive because of a high theoretical PAE, these switch-mode classes require operation far below f_{MAX}. However, added PAE from a class AB, B, or C could reasonably be accomplished with a transistor operating near f_{MAX}.

4-C CONCLUSION

Solid state power amplifiers for 220GHz applications are explored in this dissertation. As a frontier for high power generation, 220GHz circuits presents additional challenges when compared to W-band and below. The shortest interconnects must be modeled accurately (e.g. a 2µm piece of wire has a 1 degree electrical delay). Microwave structures that rely on quarter-wave geometries are highly useful as long as large conductor losses are mitigated. New, fast InP HBT devices are maturing with f_{MAX} well above 220GHz, yet the available gain still leaves little headroom for mismatches and losses in any of the amplifier's associated passive networks.

Given these challenges, it has been demonstrated that using a cascode to increase the available gain of the amplifier block can make PA design possible at 220GHz. The designer can then take advantage of classic microwave techniques—

scaled to micrometers—to transfer power to and from the transistors. Class A load line tuning can provide a way to get large output power from the output transistor. Multi-level power combining can then multiply the final MMIC output power. These methods may be scaled at the wafer and module level to reach above 1Watt at 220GHz.

The End.

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Appendix: Other Circuit Designs

A1-A UCSB INP HBT PA MMIC

In addition to work with Teledyne's 250nm HBT process, UCSB Rodwell Group provided limited space on a maskset for design of power amplifiers with its experimental 250nm HBT process. Without the maturity of a foundry process, there was no pre-tapeout model developed using device measurements. Instead, a physics-based model was developed by Mark Rodwell and previous graduate students at UCSB for circuit simulation. Model parameters were adjusted prior to simulation to better represent the highly scaled devices [28].

The final circuit used two single-sided common-base HBTs with the two emitters laying end-to-end. The emitter area of each HBT was $0.23x4.3\mu m^2$. Similar devices processed previously had demonstrated to have $\beta = 50$, an $f_T = 400$ GHz, and $f_{MAX} = 400$ GHz with $V_{CB} = 0.7$ V, Vce = 1.65 V, and Ic = 14 mA [1]. The metal interconnect stack consisted of two metal layers. The lower layer is deposited at the collector level and is 0.2µm thick. The upper layer sits directly on top of the emitter metal. These two gold metal layers are separated by 0.9µm of BCB.

Amplifier matching networks were designed using Agilent Advanced Design System (ADS) and ADS Momentum for electromagnetic simulation. The input was small-signal matched using a quarter-wave transformer. The output was tuned for maximum saturated output power using an shorted-stub matching network and a series high impedance transmission line. The short was provided on the stub using a radial stub that provided a large capacitance to ground. DC bias was designed to be supplied through the RF input and output off wafer.

The amplifier underwent small-signal testing using an Agilent N5242A PNA-X with OML frequency extenders for the 140-220 GHz and 220-330 GHz bands. The network analyzer was calibrated using an on-wafer Thru-Reflect-Line (TRL) Calibration. The TRL reference planes were placed 250µm from the RF GSG pads. GGB picoprobes with built-in bias tees and 75 µm pitch were used to deliver an isolated RF signal and bias to the power amplifier pads. DC bias was provided using an Agilent 4155C with a current source module on the emitter and a voltage source module biasing the collector. Amplifiers were biased over a range of values including V_{CB} = 0.5 and 1.0 V and Ie = 5 mA, 10 mA, 15 mA. For power testing, a VDI 200 GHz Frequency Extender Module was driven by an Anritsu 40 GHz frequency synthesizer. Power measurements were taken using an Erickson sub-millimeter wave power meter.

With V_{CB}=0.5 V and Ie=15 mA, the power amplifier reached an S21 of 3.18 dB at 221 GHz. S11 reached a minimum at 230 GHz, while S22 reached a minimum at greater than 200 GHz. During large signal testing, the PA had a gain of 1dB at an output power of 4.8 dBm at 200 GHz with V_{CB}=1 V and Ie=20 mA. At 210 GHz, the PA

had a gain of 1dB at an output power of 4.1 dBm with V_{CB}=1 V and Ie=20 mA. Again, the amplifiers reported here were designed for an HBT device technology undergoing development. Improvements in HBT performance will increase amplifier gain and operating frequency.

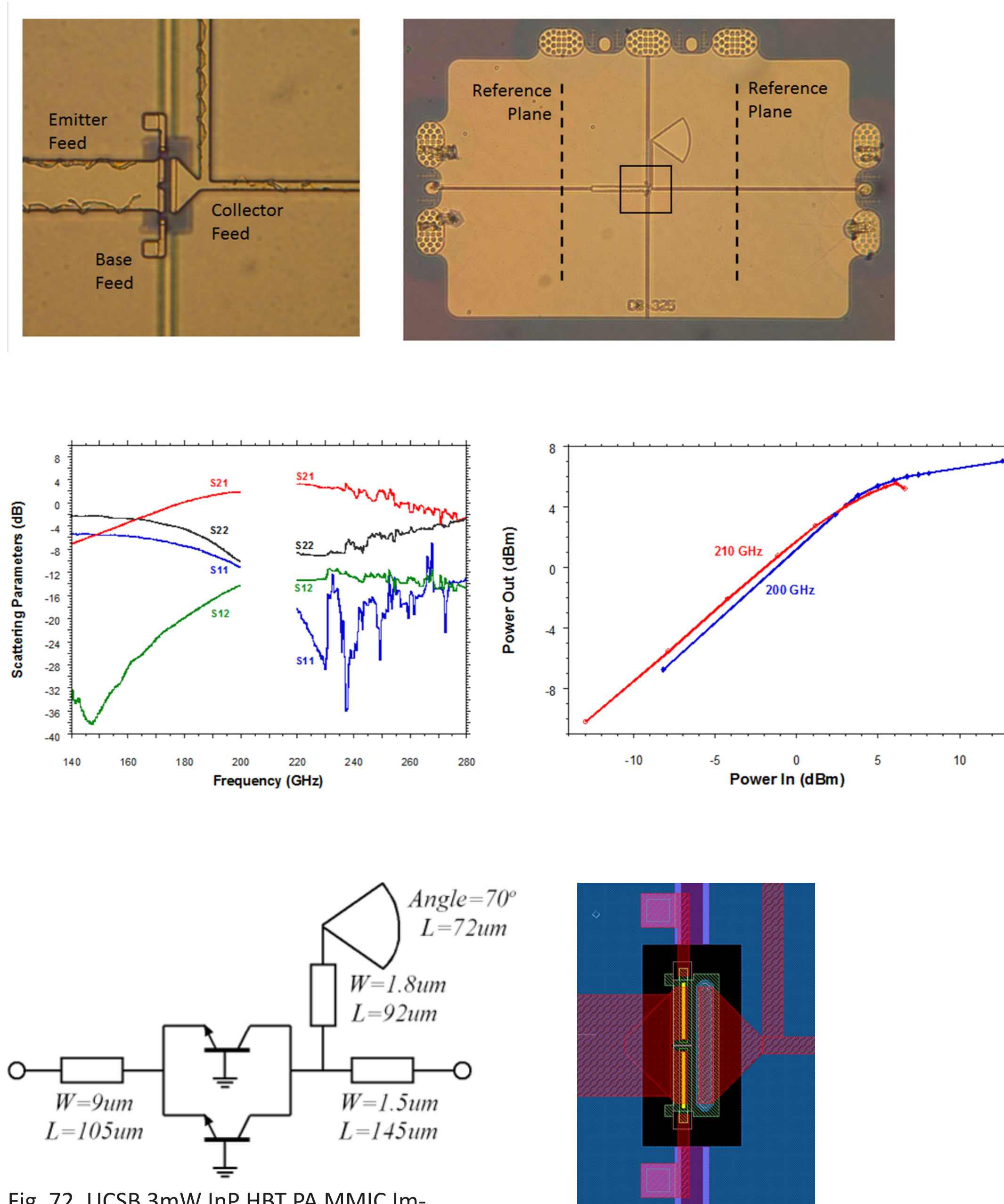

Fig. 72. UCSB 3mW InP HBT PA MMIC Images, Design, and Results

V-band DPDT Switch

As part of a larger transceiver system, a single-pull-double-throw switch was designed to switch an antenna between a 1W power amplifier and a low noise amplifier at 44GHz. The LNA required 30dB of isolation from the 30dBm PA signal. Also less than 1dB insertion loss could be incurred through each path to the antenna.

For the switch, two varieties were used. A diode bridge switch was designed for high off-state power handling and a shunt diode switch was placed between signal and ground. When the diode bridge is turned off it has the ability to handle high voltages. When on, the diode bridge can provide small diode on-resistance. The shunt diode acts as a very large resistance with no current flowing. When turned on, RF signal current is drawn through the low resistance to ground.

After tapeout, design mistakes were discovered that drastically increased the insertion loss of the switch and led to a redesign.

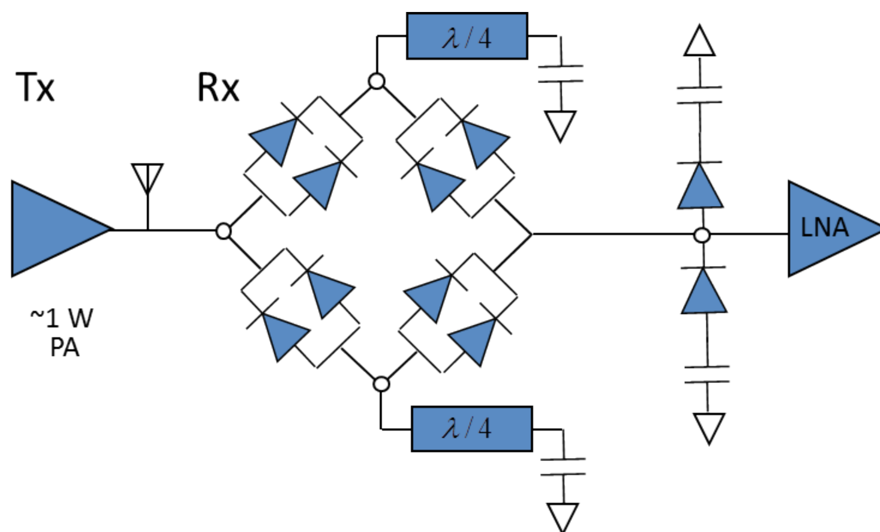

Fig. 73. Tx/Rx Switch Schematic

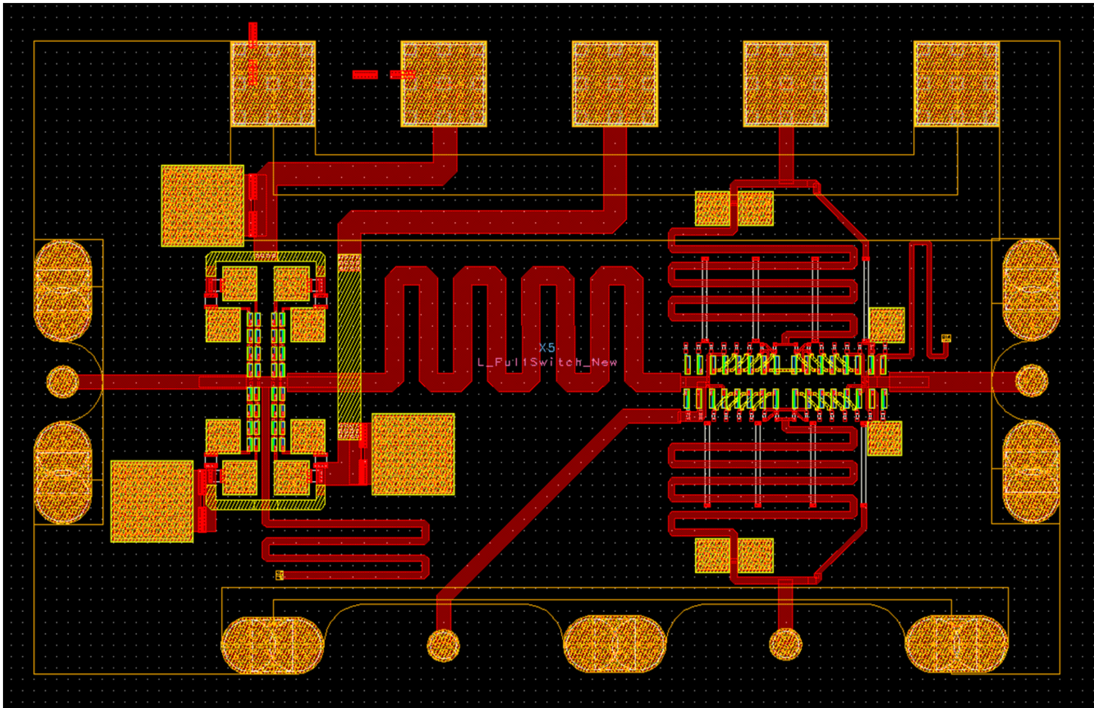

Fig. 74. Tx/Rx Switch Layout

A1-B V-BAND PHASE SHIFTER PIXEL

In addition to a switch, a IQ Channel phase shifter pixel was also a desirable circuit component in a receiver at 44GHz. The pixel splits a signal evenly into an I and Q channel. Next, each channel can be multiplied by a value between -1 and 1. Finally, after summing all the I and Q outputs of all the pixels the Q channel goes through a 90 degree phase shift.

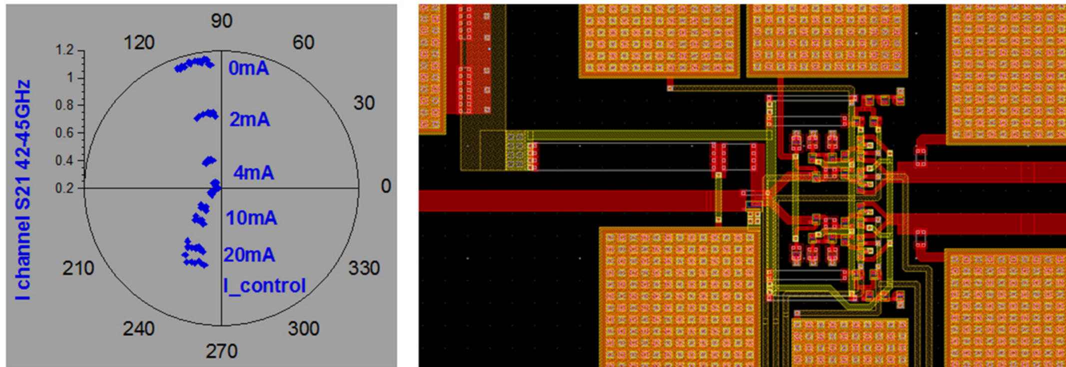

Fig. 75. Phase Shifter Pixel Layout and Tuning Range Measurements

The amplifiers are tuned to have a gain maximum at 44GHz. The gain of the pixel is near 2dB. The gain is shown for the I and Q channels versus gain control current at 44GHz.