A 40 Gb/s Asynchronous Optical Packet Buffer Based on an SOA Gate Matrix for Contention Resolution

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Abstract: We demonstrate a 40 Gb/s optical packet buffer with asynchronous and autonomous control for use in contention resolution. Layer-2 (packet recovery) measurements are presented with less than 1 dB power penalty up to 10 circulations.

1. Introduction

Optical packet switching provides a means of communication that is flexible, scalable, fast switching, and high capacity [1]. Optical buffers are a necessary component to resolve contention and congestion. Practical buffers to date have relied on fiber delay lines that provide low-loss and large delays, but are fixed in size. Most optical buffers can be characterized as either feed-forward or feed-back. Feed-forward buffers commonly utilize wavelength routing schemes which lessen the number of active components, but require many delay lines in order to achieve a variable delay. Feed-back buffers offer a large variable delay with the use of few delay lines [2]. Re-circulating loop buffers offer the advantage of being compact and thus amenable to integration. They are commonly composed of only a switch and delay line. Several types of switches have been developed and show promising results towards integration of optical buffers [3, 4]. Further integration of buffers to include on-chip delay lines has been proposed through the use of hybrid integrated switches with low loss waveguides [5]. A re-circulating loop buffer is studied because of its potential for integration on chip and practical application in future optical routers. In this work, a re-circulating buffer with asynchronous and autonomous control at a data rate of 40 Gb/s is investigated. A dynamic range in excess of 20 dB and a power penalty less than 1dB is achieved up to 10 circulations, corresponding to 1.92 µs of delay.

2. Background

A 2x2 semiconductor optical amplifier (SOA) gate matrix is used here as the switching mechanism for a re-circulating buffer. The major criteria that an optical buffer must meet is bit rate scalability up to and in the future beyond 40 Gb/s, low crosstalk (<-40 dB) and high extinction (> 40dB) for cascadability, and fast switching times (1-5 ns) [3]. The 2x2 SOA gate matrix achieves all the aforementioned requirements but has the disadvantage of introducing amplified spontaneous emission (ASE) which degrades the optical signal to noise ratio (OSNR). This necessitates the use of a band pass filter (BPF) in the loop to suppress noise. However, the filter cannot remove noise at the signal wavelength; therefore, the number of circulations in a re-circulating buffer based on SOAs is limited by accumulated ASE. In order to increase the number of circulations, 2R or 3R techniques must be incorporated in the loop.

This type of buffer can be incorporated into an optical packet switch based on optical label swapping [6]. A label is used to determine where to route packets while the payload information is not processed electronically. This allows the payload to be at a high bit rate while the label can be at a lower bit rate for the electronics. An important requirement of a packet switch is the ability to account for the asynchronous nature between the optical data and electronic control plane [7]. A major component to resolving this issue is the payload envelope detector (PED) [8]. The control plane uses the payload envelope to obtain a precise time reference to the start and end of packets for control signal generation in the packet switch. A PED and a field programmable gate array (FPGA) are used in this experiment to detect and forward packets, completely autonomous and self-controlled. Contention resolution is demonstrated by using the optical buffer to avoid temporal collisions.

3. Experimental Setup and Results

A re-circulating buffer based on a 2x2 SOA gate matrix is depicted in Fig 1. Four SOAs were used as the gates for the buffer and to provide gain to compensate for losses. Four 3dB splitters were placed on the ports of the buffer and attenuators were used to balance gain and loss. In order to suppress accumulated

ASE, a BPF with a bandwidth of 2.4 nm was placed in the loop. The delay through any port configuration of the switch, T_{path}, is 120ns and the delay through the loop, T_{loop}, is 60 ns. The total delay of the buffer per number of circulations can be given as

$$T(n) = (n+1)T_{path} + nT_{loop} \quad (1)$$

Packets entering the buffer can either be placed in the loop by way of $path_{13}$ or pass through the buffer via $path_{14}$. Once a packet is in the loop it can either re-circulate by way of $path_{23}$ or exit via $path_{24}$. Packets can simultaneously circulate and pass through the buffer.
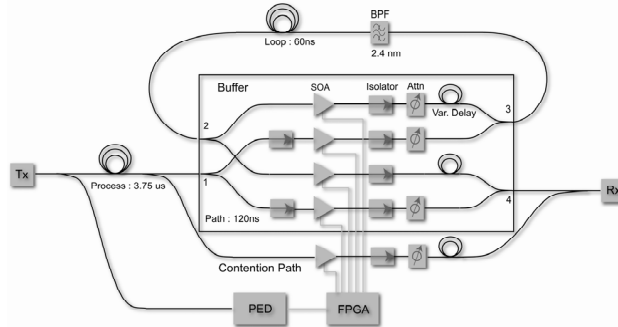

Fig. 1. Schematic of experimental setup

A schematic illustrating contention resolution is shown in Fig. 2. The setup consists of an optical buffer and a contention path. The contention path simulates an input port configured to send traffic to the same output port as the buffer. The relative delay of the buffer to the contention path is the same as stated in Eqn. 1. Fig. 2(a) shows two transmitted packets, labeled 1 and 0. The transmitted signal is split equally in power to the buffer and the contention path. Fig. 2(b) shows the packets located in the buffer and contention path. The first packet, labeled 1, going to the buffer must circulate because there is a second packet, labeled 0, it will collide with in the contention path. The second packet going to the buffer passes straight through with a delay of T (0) since it will not collide with any packets. The packet in the loop exits after one circulation, T (1), because there is no packet to contend with at the output. Fig. 2(c) shows successful rearrangement of packets at the receiver labeled 1, 0, 0, and 1.

Fig. 2 (a) Packets from transmitter   (b) Packets in buffer and contention path   (c) Packets at receiver
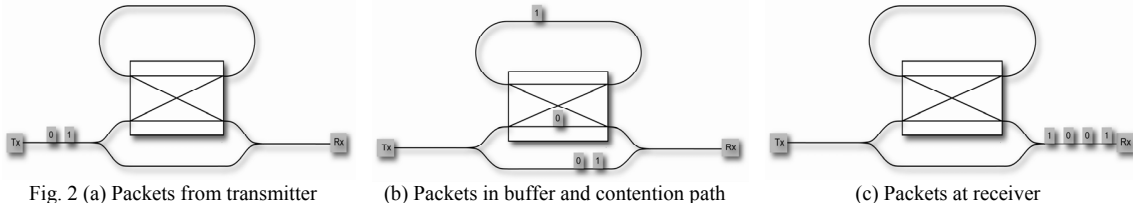
In this experiment, 40 byte RZ packets at 40 Gb/s are used as data with 60 ns timeslots for switching. The transmitted signal is tapped for electronic control processing. The PED is used to detect incoming packets and generate packet envelopes. The envelopes enter an FPGA based controller board where they are processed and the behavior of the buffer is determined. The FPGA board operates asynchronously to the transmitter and therefore takes into account any relative drift between clocks. Moreover, it must also cope with the fact that the data rate is not an integer multiple of the 100 MHz clock running the FPGA board. On entering the FPGA board, the envelopes are expanded to 60 ns and aligned to the local clock through an SR latch and a series of D flip-flops. Using delayed versions of the detected envelopes, the controller determines how to forward packets. The processing time in the electronic control plane is compensated for by adding 750m of fiber, corresponding to 3.75 μs delay. The transmitted signal is split equally after the processing delay to the buffer and the contention path. An SOA is used in the contention path to gate the incoming packets and thus avoid issues pertaining to intraband crosstalk. All packets that are transmitted pass through the contention path. The packet stream is engineered to exercise all states of the buffer. The first packet circulates once, the third twice, the sixth thrice, and so on until ten circulations. Fig. 3(a) shows the first five packets of the input data stream. The packets are labeled according to the number of circulations i.e. 0, 1 and 2 circulations. Fig. 3(b) shows the packets from the buffer and contention path. The first packet, labeled 1, must circulate because a second packet, labeled 0, is located 120 ns later. The second packet can pass through the buffer since there is no packet 120ns later. Since there is no packet 300ns after the first packet, the buffered packet can exit. The third packet, labeled 2,

must circulate twice because it is blocked by packets at 120ns and 300ns later. The fourth and fifth packets, both labeled 0, pass through the buffer because they will not collide with other packets. The packet labeled 2 exits the buffer 480 ns after it entered. Fig. 3(c) shows that the first five packets are rearranged properly thus avoiding collisions.
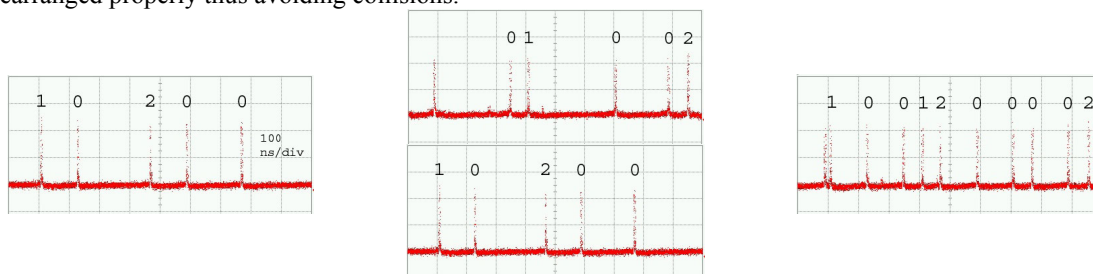

Fig. 3(a) Packets from transmitter   (b) Packets from buffer and contention path   (c) Packets at receiver

Layer-2 (packet recovery) measurements were conducted at various input powers for the contention path (CP) and 0, 2, 6, and 10 circulations. Fig. 4(a) shows results at low input power (-29 dBm). The signal degrades as the number of circulations increases due to accumulated noise. Fig. 4(b) shows measurements at an optimal input power (-24dBm). The power penalty is less than 1 dB at this input power because neither noise nor saturation is a major issue. Fig. 4(c) shows results at high input power (-3 dBm). Saturation distorts the signal as well as causes the gain to decrease in the SOAs which leads to poor signal quality. Nonetheless, the buffer offers a large dynamic range in excess of 20 dB, which makes it suitable for an optical packet switch.
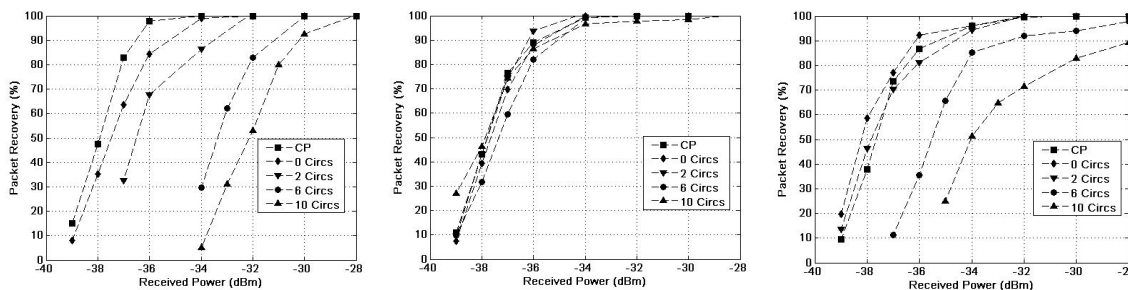

Fig. 4(a) Packet recovery at Pin= -29dBm   (b) Packet recovery at Pin= -24 dBm   (c) Packet recovery at Pin= -3 dBm

4. Summary

A fiber loop re-circulating buffer is investigated and less than 1 dB of power penalty is achieved at 40Gb/s for 10 circulations, equivalent to 1.92 µs of delay. A payload envelope detector and FPGA are used asynchronous to the optical data to control the buffer and forward packets. Successful rearrangement of 65 packets in a data stream with 195 timeslots is shown which demonstrates contention resolution.

5. Acknowledgement

6. References

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