Fast Optical Clock Recovery and Signal Regeneration Applications of a Monolithic Mode Locked Laser with DBR Mirrors and an Optical Amplifier

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Abstract *We demonstrate optical packet clock recovery with locking in less than 700 ps (25 bits) using a novel device which is compatible with other monolithic components. Regenerative capabilities are analyzed using bit error rate tests.*

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Introduction

Monolithic mode locked lasers (MLLs) have been suggested as compact devices that can perform clock recovery with regenerative properties [1-3]. For example, the recovered clock from an MLL may have reduced timing jitter and amplitude noise compared to the input data. For optical packet switching networks, it may be necessary to perform 3R regeneration of short data packets, using a clock recovery element combined with a nonlinear optical gate [4-5]. The clock should be recovered within several bits to minimize latency, and retiming and reshaping of degraded data is necessary. Here we investigate the locking and hold times of a monolithic MLL with an SOA which is injection locked to short 35 Gb/s data packets. We also present a quantitative analysis of the clock recovery capabilities of this device by performing bit error rate (BER) tests. The results indicate that a high quality clock can be recovered even from severely degraded input signals.

Device Design and Experimental Setup

The device was fabricated on an InP substrate with InGaAs/InGaAsP offset quantum wells, allowing for active and passive waveguide sections and for potential integration with many other types of components [6]. Figure 1 shows the device, which consists of a rear SOA (not used in these experiments), an MLL, a 550-μm long output SOA, and a curved and flared output waveguide which reduces back reflections [3, 7].

The MLL consists of a rear DBR mirror (90% power reflectivity), a 50-μm long saturable absorber section, a 550-μm long gain section, a 290-μm long gain section, a 100-μm long phase section, and a 40% reflecting front DBR mirror. The mirror gratings were defined using holography and placed lithographically. Due to the precise mirror placement, knowledge of the group index, and some tunability in the mode locking frequency (~300 MHz), the device was capable of mode-locking and clock recovery at the desired frequency (35.00 Gb/s), which is important for practical applications. The device was designed for 35 GHz operation due to measurement limitations, but could easily be fabricated for 40 GHz or much higher bit rates [2] by changing the length.

In the results presented here the device is hybrid mode locked, meaning the input data stream is sent to a photodetector (PD), an amplifier (not required but improves performance), and a coplanar stripline (CPS) probe placed on the device's absorber. The amplifier outputs 10 dBm of electrical power. Under this setup the device's output clock has Gaussian pulses which are tunable between 4 and 8 ps, a time bandwidth product of 0.51, an extinction ratio of 12 dB, and an average output power of 8.3 dBm [3].

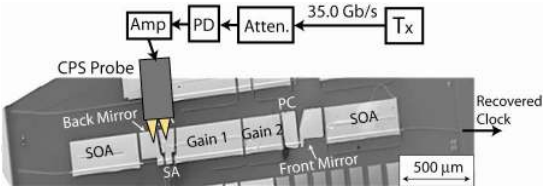

Figure 1: Basic experimental setup, with a scanning electron micrograph of the monolithic device.

Experimental Results

To examine the locking time and hold time of the device, we transmitted 9 ns packets of 35 Gb/s data with 100-200 ns inter-packet gaps. Since the laser is passively mode-locked, it sends out pulses even when there is no input signal. However, the phase of these pulses fluctuates randomly over time unless the laser is locked to an input signal. Thus by using the averaging function on the oscilloscope, we can determine when the laser has locked to the input signal. When there is no input signal, the laser pulses average out to zero. When the input is injected, the laser pulse phases gradually align and the average of the pulses becomes nonzero.

The locking capabilities as determined by this technique are shown in Figure 2. The top 2 oscilloscope traces show the input packets and output clock with 20 ns/division. The next two traces show a single packet and recovered packet clock with 2 ns/division. Clearly the clock is held for longer than the duration of the input signal. This is essential for

use in a 3R regenerator, since the clock must persist for at least the duration of the packet. The bottom two traces are on a scale of 500 ps/division, showing that the clock is recovered within 700 ps (25 bits). Therefore this type of device could be combined with a nonlinear gate to achieve 3R regeneration of optical packets with low latency [5].

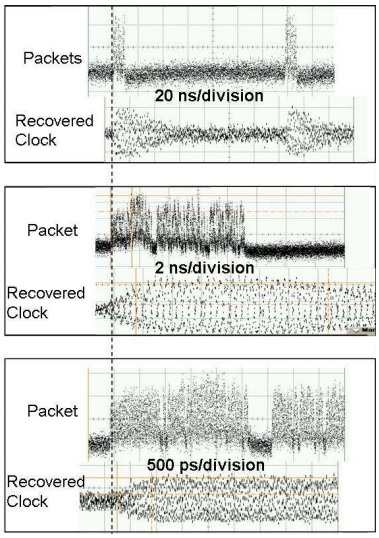

Figure 2: Oscilloscope traces of the input packets and recovered clock output by the device for 3 different time scales, demonstrating the fast locking time and long hold time of the device.

To test the regenerative capabilities of the device, we used the setup shown in Figure 2. A 35 Gb/s 2^31-1 PRBS signal is sent to the device. The output clock is sent to a lithium niobate modulator driven by the electrical data signal from the BERT, encoding the original data onto the output clock. This allows us to test the quality of the recovered clock by performing BER tests. This setup simulates what would be possible if an ideal nonlinear gate were used to gate the clock pulses in a 3R regenerator. First the BER of the clock was measured with a normal input signal, shown in the lower left inset in Figure 2. Next the input signal was passed through 25 km of Corning SMF-28 fiber, which significantly degraded the signal as shown in the lower middle inset in Figure 2.

The BERs of the recovered clock are shown for both cases in Figure 3, demonstrating almost no difference. It should be noted that the BERT was unable to synchronize to the degraded input signal, meaning it could not determine which bits were 1's and which were 0's. If the BERT could not distinguish what was a 1 or 0, then a nonlinear gate would not be able to either. However the clock was still recovered for this signal with negligible penalty. This indicates that this clock recovery device would not be the limiting factor in a 3R regenerator.

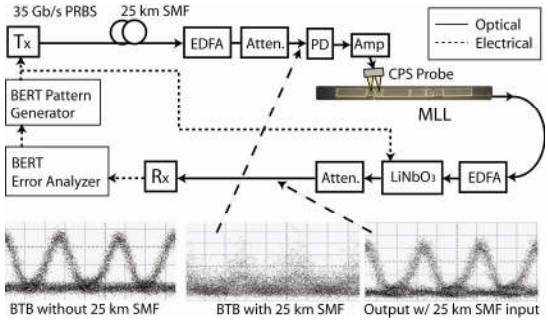

Figure 3: Experimental setup used to obtain BERs to test the recovered clock. The clock is recovered in the device and the output of the device is gated using a modulator driven by the original electrical signal from the BERT.

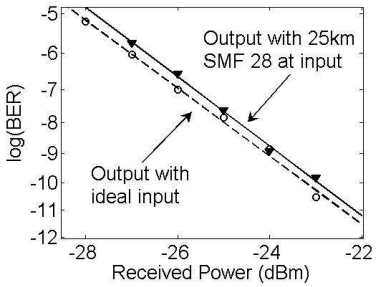

Figure 4: Bit error rates of the output sent to the receiver as shown in Figure 2 with a normal input and with input signal degradation.

Conclusions

We have demonstrated optical clock recovery with locking times of <700 ps using a monolithic MLL integrated with an SOA. The fast locking and regenerative capabilities of the device indicate that the device may be useful for packet 3R regeneration. Furthermore, the compatibility of the device with other components indicates that a monolithic packet 3R regenerator can be realized.

Acknowledgements

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