The Nature of the Charges, Currents, and Fields in and About Conductors Having Cross-Sectional Dimensions of the Order of a Skin Depth

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Abstract —**The nature of the charge, current, and field patterns is investigated in and about transmission line conductors operating in a frequency range where one or more of the cross-sectional dimensions of the conductors is of the order of a skin depth. Questions are addressed concerning whether quasi-TEM approximations can be used. Examples are considered which simulate the relatively lossy, longer on-chip interconnects in high-speed digital circuits. For comparison, approximations to MMIC line examples, which usually have larger cross-sectional dimension and hence are less lossy, are also examined.**

I. Introduction

CURRENTLY many on-chip, high-speed digital circuits and MMIC circuits utilize frequencies and conductors such that one or more dimensions of the transmission-line conductor cross sections may be of the order of a skin depth. For conciseness we will herein refer to transmission lines operating under these conditions as d lines. The use of transmission-line circuits operating in the d-line range greatly complicates the calculation of the operation of such circuits since the usual skin-effect approximations [1] do not apply. A number of authors have dealt with various approaches for characterizing lines operating in the d-line range [2]–[4]. However, to our knowledge the nature of the charges, currents, and fields associated with such operation has not been made clear in the literature. A sound understanding of the distribution of these quantities in lines operating in the d-line range is helpful, for example, in deciding whether a quasi-TEM mode approximation is valid in a given situation and for answering other related questions to be posed below. It may also be helpful for devising improved approximations for analyzing lines operating in this range.

Using physical reasoning and a simplified example for which exact analysis is easily accomplished, the nature of the field, charge, and current distributions for transmission lines operating in the d-line range will be pictured and observations will be made relating to the applicability of the quasi-TEM approximation. The authors are herein primarily concerned with on-chip high-speed digital circuits. Though the on-chip interconnect lines in such circuits are mostly very short and can be modeled by lumped elements, some of the signal bus lines are sufficiently long that wave analysis is required. Herein, for comparison, examples which approximate MMIC circuits operating under d-line conditions are also discussed.

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II. Some Questions and an Example

In order to focus our discussion let us pose some questions concerning d-line operation which we will endeavor to answer in Section III.

1) A key question is whether the quasi-TEM-mode approximation is valid so that L, C, R, and characteristic impedance, TEM-mode line parameters are applicable for analyzing a given circuit operating in the d-line range. The answer to this question will be determined by the answers to the other questions below.

2) A conductor operating in the d-line range has current and fields propagating throughout its cross section (instead of at or very near the surface, as in the conventional microwave case). For this situation is the net free charge density necessarily confined to the surface of the conductor so that the static line capacitance per unit length commonly used in TEM-mode analysis is truly applicable?

3) Lines operating on the d-line range may be very lossy because of their extremely small cross sections. For example, for the case of an on-chip high-speed digital circuit the conductors might have cross-sectional dimensions of 2 by 0.5 μm. The dc resistance of such a line made of gold is of the order of 250 Ω/cm. In such digital cases the signal and return lines are typically both on the top surface of the substrate, and they may have the same dimensions. Thus a pair of coplanar strips of this sort would have a total dc resistance of the order of 500 Ω/cm. Such large line resistance suggests there will be a sizable E field in the direction of current flow. Will this

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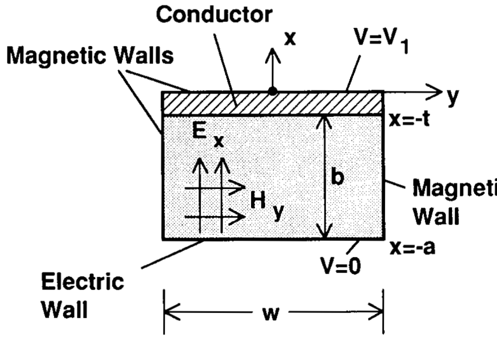

Fig. 1. The simplified transmission-line structure used in this paper for examining charge, current, and field patterns associated with conductors with one or more dimensions of the order of a skin depth.

axial $\boldsymbol{E}$-field component be large enough to invalidate the quasi-TEM-mode approximation?

4) Will the field distortion due to the multiple-dielectric nature of typical d lines invalidate the TEM-mode approximation?

5) Another somewhat peripheral but insightful question relates to the fact that for low-loss line operation in the TEM mode the phasor current I for the line can be computed from the phasor surface charge density ρ_s by

$$I = v_p \oint_{\text{c.s. perimeter}} \rho_s \, dl \tag{1}$$

where v_p is the phase velocity and ρ_s is integrated around the perimeter of the line cross section (c.s.). Equation (1) applies to a typical low-loss microwave situation where both the current and charge are at or very close to the surface of the conductor. However, in the case of d-line operation strong current flow extends throughout the conductor cross section. Can this deep axial current flow be computed from charge density observed at the surface in some manner similar to (1)?

In order to aid in gaining a qualitative understanding of d-line operation, we will use the example in Fig. 1, which is assumed to extend into and out of the paper and which has wave propagation in the z direction (into the paper). This example is chosen to be as simple as possible yet it involves all of the phenomena relevant to the above questions except for question 4. At the top is a conductor of height t and width w. Below it is a dielectric of relative dielectric constant ϵ_r with an electric wall (i.e., a perfect conductor) at the bottom. The sides and top are capped with magnetic walls which will terminate normal $\boldsymbol{H}$ field and forbid normal $\boldsymbol{E}$ field, thus eliminating all fringing fields. The $\boldsymbol{H}$ field $\boldsymbol{H}_y$ is uniform in the y direction while the $\boldsymbol{E}$ field lies in the $x-z$ plane and is also independent of y. The fields are TM to z, but if the conductor at the top had perfect conductivity the fields in the dielectric would become an exact TEM wave in the z direction.

The structure in Fig. 1 is not a practical structure but it can be crudely related to practical structures. The pair of coplanar strips in Fig. 2(a) have a symmetry plane in the middle with $V = 0$, which acts like the electric wall in Fig. 1. (Fig. 2(a) approximates many high-speed digital on-chip situations where any ground plane on the bottom is too far away compared to the conductor spacings to have any effect.) The distance b in Fig. 2(a) roughly relates to the spacing b in Fig. 1. Fig. 2(b) shows an analogous microstrip situation where the ground plane is taken to be an electric wall since it would typically be thicker with loss effects much less than for the conductor at the top which is operating in the d-line range. The point of parts (a) and (b) of Fig. 2 is not to generate quantitative values for the parameters of these lines but to provide some guidance in picking values for b in order to observe the *correct order of magnitude* for effects in the model in Fig. 1. In the on-chip high-speed digital circuit examples to be discussed later we will assume that in Fig. 2(a) the conductors are 2 μm wide spaced by 2 μm, and we will use $b = 2.5$ μm for b in the model in Fig. 1. However, for MMIC microstrip cases as in Fig. 2(b) we will assume the substrate is 4 mils (102 μm) thick and we will use that value for b in Fig. 1.

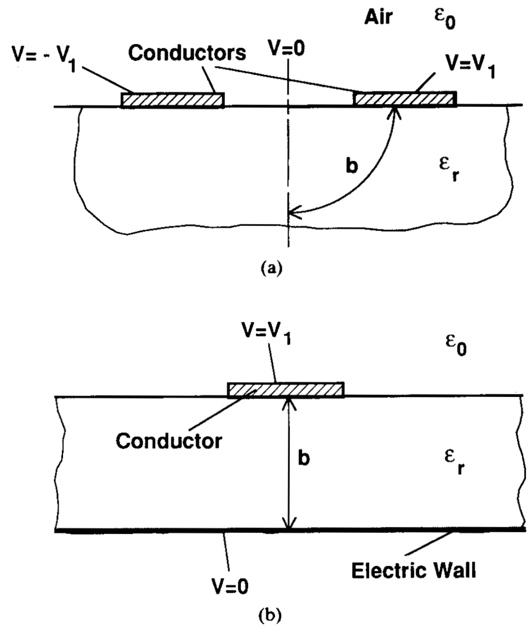

Fig. 2. (a) A pair of coplanar strips such as often occur in on-chip high-speed digital circuits. (b) A conventional microstrip line such as might be used in MMIC applications.

Using methods as in [5], the wave equation was solved in both the dielectric and conductor regions for the TM mode described above. As is commonly done, the conductivity inside the conductor was accounted for by introducing a complex dielectric constant:

$$\epsilon_c = \left(\epsilon_m - j\frac{\sigma}{\omega} \right) \tag{2}$$

where σ is the conductivity, and the real part ϵ_m of the dielectric constant in the conductor is assumed to be roughly the same as that for air, ϵ_0. For good conductors the second term in (2) is large compared to the first term for low frequencies to frequencies well beyond the millimeter-wave range so, as is usual [1], we use

$$\epsilon_c \approx -j\sigma/\omega. \tag{3}$$

After applying the boundary conditions the field solutions led to the characteristic equations

$$(k_{xd}/(\epsilon_0\epsilon_r))\tan(k_{xd}b) = (k_{xc}/\epsilon_c)\cot(k_{xc}t) \tag{4}$$

$$k_{xc}^2 + k_z^2 = k_c^2 = \omega^2\mu\epsilon_c \tag{5}$$

$$k_{xd}^2 + k_z^2 = k_d^2 = \omega^2\mu\epsilon_0\epsilon_r \tag{6}$$

where k_{xc} and k_{xd} are the complex magnitudes of the x components of the k vectors in the conductor and dielectric, respectively, and k_z is the z component of the k vector in both regions. In this situation all of the k-vector components in both the conductor and the dielectric are complex, and for accuracy, double precision was used in solving (4) to (6). The field solutions using these k-vector components were then used for exploring the features of propagation under d-line conditions.

III. Discussion of the Questions

As noted above, the answer to question 1 hinges on the later questions. The answer to question 2 is that the net free charge is definitely confined to the surface, just as it is for the static case. This is easily seen from the equation of continuity

$$\nabla\cdot \boldsymbol{J} = \nabla\cdot(\sigma \boldsymbol{E}_c) = -j\omega\rho \tag{7}$$

where ρ is the charge density per unit volume. This equation shows that for there to be net charge in a homogeneous conductor the $\boldsymbol{E}$ field $\boldsymbol{E}_c$ within the conductor must have divergence. However, the fields within the conductor, regardless of its shape, can always be represented as a superposition of plane waves (complex in this case) each of which has zero divergence for a homogeneous medium. This is because the direction in which the fields have spatial variation is always orthogonal to the $\boldsymbol{E}$ and $\boldsymbol{H}$ fields. Thus, the only place where charge can occur is at the conductor surface, where $\boldsymbol{E}$ and $\boldsymbol{J}$ are discontinuous. We conclude that, at least as far as charge being on the surface is concerned, the static line capacitance is still relevant for d-line operating conditions, just as it is for ordinary TEM-mode conditions (where the skin depth is assumed to be small compared to the conductor dimensions [1]).

An interesting sidelight to the above is that by use of (7) and Gauss's law applied to a small pillbox volume at the surface of the conductor one can readily show that the surface charge density is given by

$$\rho_s = jJ_n/\omega = j\sigma E_{nc}/\omega \tag{8}$$

where the subscripts n imply the current or $\boldsymbol{E}$-field components just inside the conductor surface which are *normal* to the surface and pointing toward the interior of the conductor. For the case of Fig. 1, the surface charge density should also be equal to the normal $\boldsymbol{D}$ field in the dielectric or $-\epsilon_0\epsilon_r E_{xd}$. The field expressions for the case

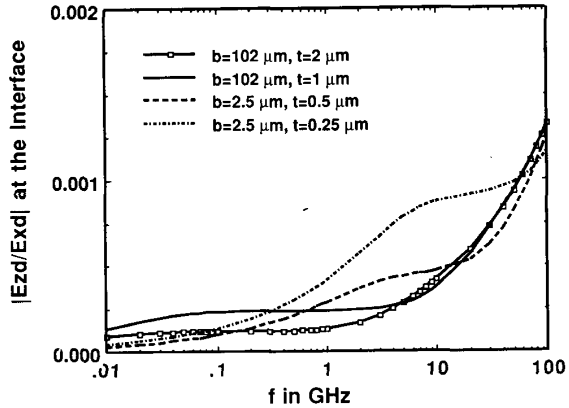

Fig. 3. The ratio of the axial (i.e., z-directed) component of $\boldsymbol{E}$ field to the transverse (x-directed) component in the dielectric at the surface of the conductor in Fig. 1 for various conductor and dielectric thicknesses.

in Fig. 1 were found to check this relationship, as expected. Equation (8) implies that lines of current flow are terminated by the time derivative of charge on the surface. Note that since $D_c = \epsilon_m E_c$ in the conductor, and because we have dropped ϵ_m in (3) because of its negligible effect, the $\boldsymbol{D}$ field within the conductor is not a consideration when computing the surface charge distribution.

Let us now consider question 3 relating to sizable $\boldsymbol{E}$ field in the direction of the current flow (E_z for Fig. 1) due to the large resistance of the conductors, and the fact that this could disrupt the quasi-TEM approximation. To explore this matter values of $|E_{zd}/E_{xd}|$ were computed versus frequency for the structure in Fig. 1 for various parameters. To roughly simulate an on-chip high-speed digital circuit of the form in Fig. 2(a), parameters $t = 0.25$ and 0.5 μm and $b = 2.5$ μm were tried, as discussed in Section II, and $t = 1$ and 2 μm was tried with $b = 102$ μm to roughly simulate an MMIC case of the form in Fig. 2(b). The conductors were assumed to be gold ($\sigma = 4.1 \times 10^7$ S/m) and the dielectric GaAs ($\epsilon_r = 13$). The results are plotted in Fig. 3. Note that even though in the high-speed digital cases the very thin lines are quite lossy, $|E_{zd}/E_{xd}|$ is not large enough to invalidate the quasi-TEM approximation. The reason for this can be better understood from the rough approximation[1]

$$|E_{zd}/E_{xd}| \approx 2b|\text{Im}\, k_z| \tag{9}$$

which was derived working from [1, p. 241, eq. (4)]. Here $|\text{Im}\, k_z|$ is the attenuation constant in Np/m. Equation (9) shows that $|E_{zd}/E_{xd}|$ is small because b is small in these examples. Clearly for a given line voltage, making b small will make E_{xd} large, which will tend to reduce $|E_{zd}/E_{xd}|$. But even when b was increased from 2.5 μm to 102 μm, $|E_{zd}/E_{xd}|$ was not greatly affected because $|\text{Im}\, k_z|$ in (9) had decreased as b was increased. Thus, in none of these

[1]For the examples tried, this approximation gave answers 15% to 45% smaller than those computed from the exact equations for Fig. 1.

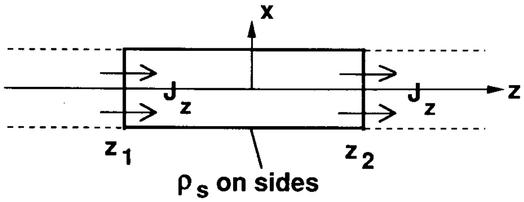

Fig. 4. A section of a conductor carrying current in the z direction.

examples is the axial $\boldsymbol{E}$ field caused by conductor loss sufficient to invalidate the quasi-TEM approximation. It is expected that the same conclusion will apply to related examples of more practical form, as in parts (a) and (b) of Fig. 2.

A rigorous analysis of question 4 is beyond the scope of this paper; however, some observations can be made. The presence of multiple dielectrics can distort the field from that of the static case by coupling to substrate modes. For the on-chip high-speed digital case the dimensions of the cross-sectional field patterns of the lines on the substrate surface are typically so small compared to the substrate dimensions that the overlap integrals between the d-line modes and substrate modes should be extremely small. Thus, field distortion (and dispersion) due to interaction between the d-line and substrate modes should be negligible in most on-chip digital situations of this type, and the validity of the quasi-TEM approximation should not be affected.

In MMIC cases such as that in Fig. 2(b), the extent of the cross-sectional field pattern is usually much larger than in on-chip high-speed digital cases, so the above-mentioned effects due to the presence of multiple dielectrics are much more significant. Nevertheless, the quasi-TEM approximation is still useful if the frequency sensitivity of the line impedances and propagation constants are accounted for. (These matters are discussed extensively in sources such as [6].)

The answer to question 5 in Section II is that there is indeed a general relation similar to (1) from which the line current can be computed from the surface charge density under d-line (or other) conditions. To see this, consider the section of a conductor shown in Fig. 4. Applying Gauss's law to (7) and recalling that the charge is only on the surface, we obtain

$$\oint_{\text{surface}} \boldsymbol{J}\cdot d\boldsymbol{s} = -j\omega\oint_{\text{surface}} \rho_s\, ds \tag{10}$$

where the surface integrals are taken over the solid-line region in Fig. 4. On the left and right end surfaces the only contribution to (10) comes from J_z while on the sides the only contribution is due to ρ_s. These phasor quantities can be expressed as

$$J_z = J_z(x,y)e^{-jk_z z} \qquad \rho_s = \rho_s(x,y)e^{-jk_z z} \tag{11}$$

assuming propagation in the $+z$ direction. Using (11) in

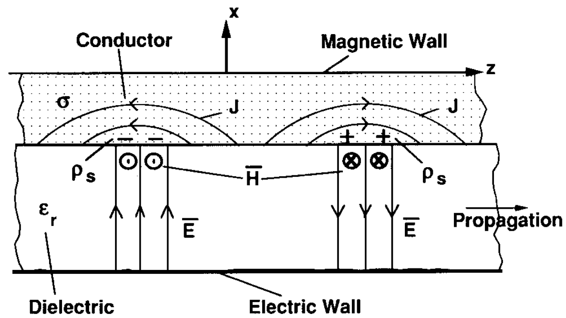

Fig. 5. A side view of a transmission line as in Fig. 1 showing the general pattern of surface charge density ρ_s and current density $\boldsymbol{J}$ at the conductor along with $\boldsymbol{E}$ and $\boldsymbol{H}$ fields in the dielectric for a propagating wave under d-line conditions.

(10) and integrating in the z direction gives

$$\int_{\text{c.s.}} J_z(x,y)\,ds\left(e^{-jk_z z_2} - e^{-jk_z z_1}\right) = -j\omega\int_{\text{c.s. perimeter}} \rho_s(x,y)\,dl\left(\frac{e^{-jk_z z_2}}{-jk_z} - \frac{e^{-jk_z z_1}}{-jk_z}\right). \tag{12}$$

Now a factor consisting of the difference between two exponentials can be canceled from both sides of (12), which leaves

$$I = \int_{\text{c.s.}} J_z(x,y)\,ds = \frac{\omega}{k_z}\int_{\text{c.s. perimeter}} \rho_s(x,y)\,dl. \tag{13}$$

For the lossless case, ω/k_z is the phase velocity in (1). For d-line situations ω/k_z can be thought of as a complex phase velocity, the imaginary part being associated with the fact that the wave is attenuating. We checked (13) as applied to the example in Fig. 1, with exact agreement.

Using (13), (8), and the field equations for the example in Fig. 1, the nature of the charge, current, and field patterns for this example was deduced. They reveal that the propagating fields, currents, and charges are as sketched in Fig. 5. Note that the current patterns terminate on the conductor bottom surface at points where the *time derivative* of ρ_s is large (in accord with (8)), whereas the large charge densities occur halfway between these points. This causes the large values of J_z to occur at values of z for which ρ_s and the $\boldsymbol{E}$ and $\boldsymbol{H}$ fields in the dielectric are also large, as would be expected for a propagating wave. Analogous patterns should hold for other shapes of conductors operating under d-line conditions.

IV. Conclusions

For the on-chip, high-speed digital situation, where the transmission lines may be very lossy because of their small cross sections, it was shown that the relatively small conductor spacings lead to strong transverse $\boldsymbol{E}$ fields as compared to the $\boldsymbol{E}$ field in the direction of propagation caused by resistance. As a result the quasi-TEM approximation is useful in spite of the large loss. Also, charge was shown to be confined to the surface of the conductors so that static capacitance calculations such as are commonly used for TEM-mode analysis are still relevant, even though here propagating fields and current penetrate deeply into the conductor. The lines of current were found to begin and end on the surface where the time derivative of surface charge density is large. Indeed, it was seen that the total internal current in a conductor can always be computed from the surface charge density as long as the conductor is homogeneous. It was also noted that because of the small conductor cross sections and spacings there should be little degradation of the quasi-TEM approximation due to the presence of multiple dielectrics in on-chip high-speed digital applications.

Typical MMIC-circuit transmission-line conductors operating in the d-line range work much the same. But, as discussed above, the transverse field patterns will tend to become much more distorted with increasing frequency due to their considerably larger conductor dimensions and spacings in the presence of multiple dielectrics.

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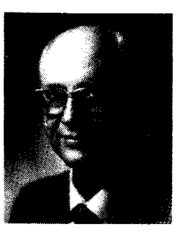

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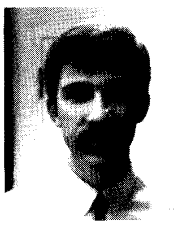

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