

A 13W Current Mode Class D High Efficiency 1 GHz Power Amplifier

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Abstract - 13 watt Current Mode Class-D (CMCD) with 60% efficiency is presented. This amplifier is the highest power switch mode microwave power amplifier reported to date. The CMCD architecture is an improvement over the Voltage Mode Class-D in that the parasitic reactance in the active device can be absorbed into the tank circuit resulting in a zero voltage switching condition.

I. Introduction

Modern cellular telephone base stations consume a large amount of electricity in the process of amplifying signals sent to hand sets. Typically, the final power amplifier consumes a large portion of this energy due to very poor efficiency. Classical designs such as Class-A are able to achieve the linearity required for complex modulation signals such as those used for CDMA. Class-A amplifiers can at best achieve 50% efficiency, but in practice achieve far less due to the high peak-to-average power ratio required for CDMA.

Switch Mode power amplifiers increase the efficiency by reducing the average drain/collector voltage-current product. Since active devices work as switches instead of current sources, DC power dissipation is ideally zero if there were no switch dissipation and no power wasted in harmonics. Class D and Class E are the most popular switch mode amplifiers. The Class D amplifier has been widely used in power converters, but has been seen very little use at RF and microwave frequencies. The parasitic reactance of the device will deteriorate the efficiency at high frequency because $1/2CV^2$ or $1/2LI^2$ energy is dissipated every cycle. In a Current Mode Class D (CMCD) amplifier, however, the parasitic capacitive susceptance at the device output can be absorbed into the output tank circuit. Efficiency is improved since ZVS (Zero Voltage Switching) is possible.

CMCD also provides higher power output capability than a Class E amplifier. The peak drain voltage and peak drain current of CMCD is πV_{dd} and $2 I_{dd}$, while for Class E the peak voltage and current are $3.6 V_{dd}$ and $2.8 I_{dd}$. Thus, for the same output power level, a CMCD amplifier has smaller stress upon the device than Class E.

Optimum Class E operation requires a specific load impedance and shunt susceptance at the drain of the device. The maximum shunt capacitance allowed is related to frequency by

$$C_S = \frac{P_{out}}{\pi f V_{dd}^2}$$

where P_{out} = output power, f = frequency (Hz) and V_{dd} is the supply voltage [1]. Thus, at a given frequency and power level, C_S is determined. If the device area necessary to accommodate the peak drain current requires a $C_{ds} > C_S$ then optimum Class E is not possible at that frequency or power. This makes it difficult to obtain several watts of power above 1 GHz with Class E unless devices with very high current per unit area are available. CMCD amplifiers have no firm restriction of this type, thus can efficiently utilize higher current, higher voltage devices such as LDMOS transistors. Much higher power can therefore be obtained.

The CMCD amplifier architecture as first presented by Kobayashi, Hindricks and Asbeck [2] achieved nearly 90% drain efficiency at 900 MHz with 870 mW output power. A similar design concept was also reported that achieved very high output power (1.1 kW) but at only 7 MHz [3]. In Class E, a 1 watt push-pull locked oscillator was reported at 1.9 GHz with 41% efficiency [4]. The amplifier described below provides high output power, (13 watts, at 1 GHz), and high efficiency (60%) while using devices with high drain-source capacitance.

II. Theory of Operation

Figures 1 and 2 show the schematics and drain voltage and current waveforms of ideal Voltage Mode and Current Mode Class D amplifiers. CMCD is a dual of the VMCD with the voltage and current waveforms interchanged. In both cases, the two devices are driven on and off in opposite phase.

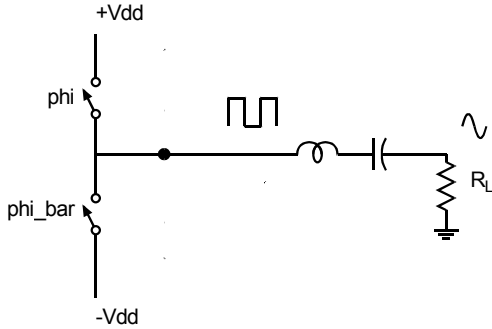


Figure 1: VMCD with Voltage Waveform

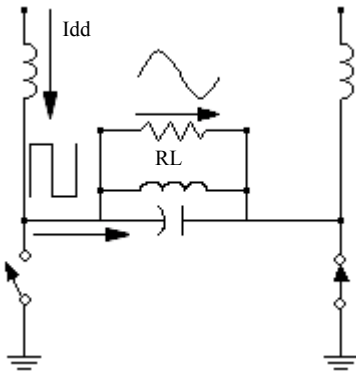


Figure 2: CMCD with Current Waveform

In VMCD a series-tuned tank circuit is employed to block harmonic currents, while in CMCD a parallel output tank circuit bypasses the harmonic components of the current, allowing only the fundamental-frequency components to reach the load.

Ideally since there is no DC power dissipation and harmonic power loss, 100% drain efficiency should be expected. However in practice, finite on-resistance and parasitic capacitance and inductance of the device will decrease efficiency. At each cycle, energy of $1/2CV^2$ or $1/2LI^2$ is lost when voltage or current changes. At higher frequencies, this loss is more dominant than the loss of the switch resistance and reduces efficiency significantly. ZVS (Zero Voltage Switching) or ZCS (Zero Current Switching) is required. For most transistors, capacitance loss is dominant, that's why in most cases we want ZVS. Our investigation into CMCD indicates that the parasitic capacitance can be absorbed into the resonator network to achieve ZVS.

Loss is also produced if the device switching time is significant at the frequency of operation, f . Better efficiencies are obtained with transistors whose f_t is much higher than f .

Figure 3 shows the schematic of a Current Mode Class D amplifier with simple switch model. The C_{ds} is

alternately grounded by the complementary switches. So at each cycle, there is always a capacitor with value of C_{ds} that appears in parallel with the resonant tank. Thus it will be possible to utilize the device parasitic capacitance when designing the resonant network. By subtracting the same amount of capacitance from the tank capacitor, the effect of C_{ds} can be absorbed. The value of C_{tune} was adjusted to get ZVS when designing the CMCD.

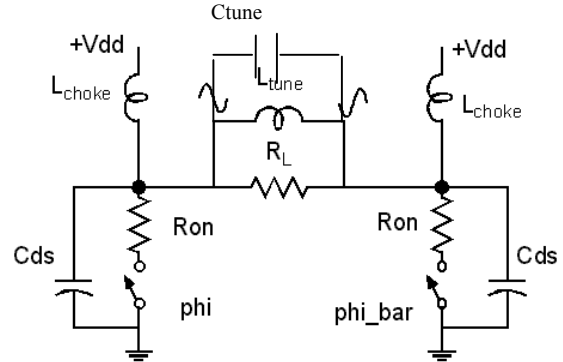


Figure 3: CMCD with Simple Switch Model

III. Design

A packaged LD MOSFET device (Ericsson PTF 10135) was used to implement the CMCD power amplifier. The LDMOS device model was extracted from measured data [5]. The device is intended for large signal applications (5 watts) from 1.0 to 2.0 GHz. However, at a higher frequency than 1 GHz, the large package inductance made the device more inductive than capacitive when it is in cutoff. This CMCD PA was designed for 1 GHz operation. The design simulation was carried out using the Agilent/EEsof ADS circuit simulator. Figure 4 shows the schematic diagram of the design.

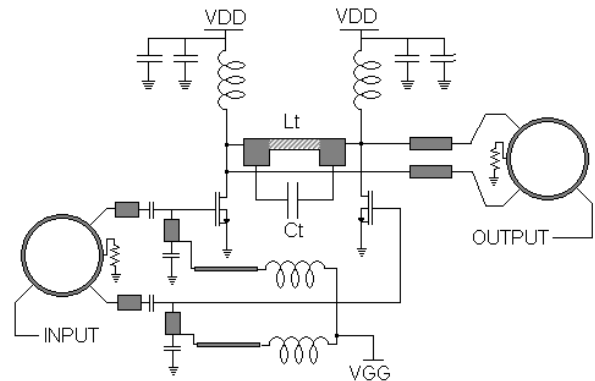


Figure 4: Schematic of actual amplifier

Since the CMCD is inherently a push-pull type of architecture, baluns are required on the input and output. Input and output coupling use 180 degree ‘rat-race’ hybrids. These are built on high dielectric substrate ($\epsilon_r=10.2$; Rogers 3010) to minimize the physical size. Tuning of the hybrids was necessary to achieve balanced amplitude and phase accuracy. The rat-race hybrid has the benefit of providing a high impedance at even harmonics and low impedance at odd harmonics. This condition is desirable for the CMCD/inverse F amplifier [6].

Input matching networks were added between the input of two transistors and the input hybrids to reduce the input mismatch. Large signal S-Parameters were used to design the matching network. However, a tuner was still required at the input hybrid to obtain the maximum transducer gain of 14 dB.

Our tank circuit comprised of L_t and C_t was designed by first converting from an ideal parallel inductor and capacitor, to a parallel capacitor and microstrip transmission line. A constraint on the tank circuit design was the physical dimensions of the drain tab on the FET package. ADS and Momentum were used to optimize the transmission line length, interconnections, capacitor value, and layout.

Figure 5 shows the simulated drain voltage waveform. The tank circuit was adjusted to achieve ZVS.

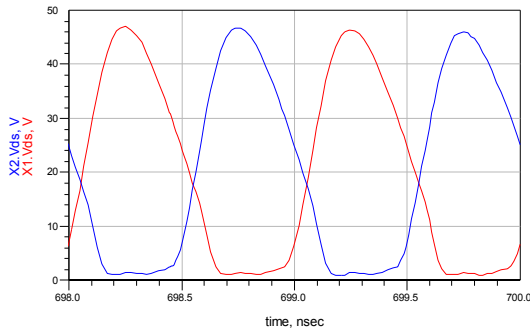


Figure 5: Simulated Drain Voltage Waveform

IV. Measurements

Measurements were performed on the completed amplifier in the test setup shown in figure 6. The input signal comes from an Agilent ESG series signal generator, which is then boosted by a Mini-Circuits ZHL-42 amplifier. The output signal first passes through a 10 dB directional coupler and then into a high power 50-ohm load. The coupled port of the directional coupler is first attenuated and then feeds a 2-way splitter, which goes into the power meter and a spectrum analyzer.

Drain and power added efficiency were measured against input drive level. Figure 7 shows that the drain efficiency and power added efficiency increase dramatically as the drive level increases. Output power increases directly with the drain supply voltage, or by increasing the drive level. A maximum output power of 13 W was observed with a drain efficiency of 60% and transducer gain of 14 dB. The corresponding power added efficiency was 58%. The 0.5 dB loss in the output rat-race hybrid was not subtracted from the measured data, so the intrinsic efficiency is about 67%.

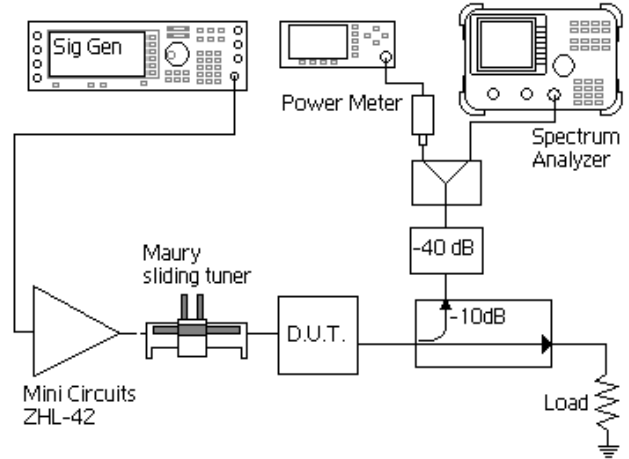


Figure 6: Test Setup

For low drive levels, the amplifier is linear, and efficiency is low since bias currents dominate input power. Beyond 25 dBm input power, the amplifier begins operating in switch-mode and eventually efficiency levels off as the maximum output power of the amplifier is achieved. Power added efficiency drops, as the extra input power does not yield any increased output power.

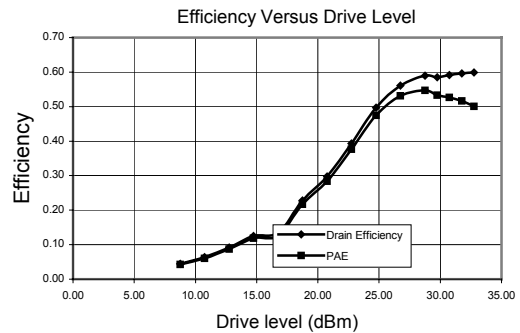


Figure 7: Efficiency versus input drive level

The drain voltage waveforms are measured by placing a resistor in series from the drain to the input of a high speed sampling oscilloscope. This gives a voltage divided sample of the output waveform. Figure 8 shows

the measured drain voltage with the amplifier operating at 10 watts.

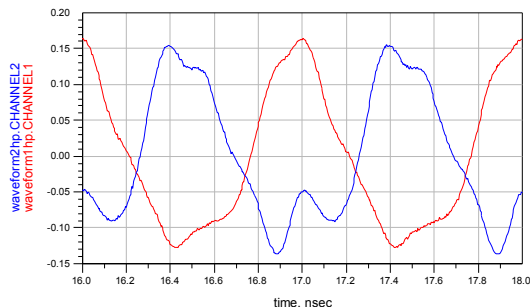


Figure 8: Drain Voltage Waveform

The drain waveform has the expected characteristic of a nearly half-sinusoidal voltage, thus the overlap between the current and voltage waveforms is minimal.

Figure 9 is a photograph of the completed amplifier with input and output hybrids. The amplifier itself is bonded to a copper heat sink and the hybrids to aluminum plates.

V. Conclusions

Our amplifier achieves 13 watts of output power with 60% drain efficiency and 58% power added efficiency, and a gain of 14 dB. This sets a new record for power output at microwave frequencies among reported switch-mode RF power amplifiers.

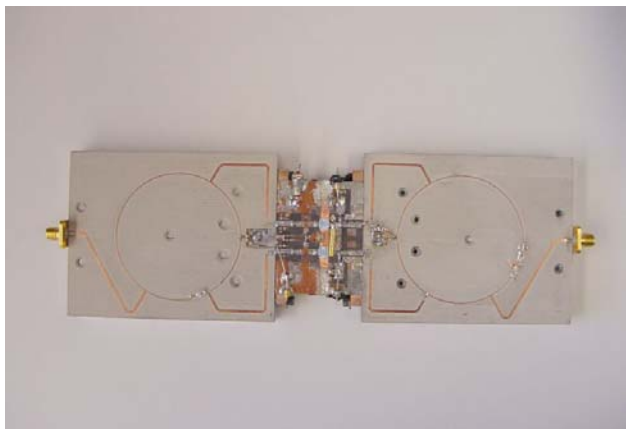


Figure 9: Photograph of completed amplifier

VI. References

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VII. Acknowledgements

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