

Design and Implementation of a Common Collector Class B RF Power Amplifier in InGaP HBT Technology

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Preface

Time flies! It feels if it happened yesterday when I arrived at the small Santa Barbara airport, left the plane and dove into the humid warm air of the Californian spring. A tropical sunset and a mild sea breeze welcomed me and the sureness of the absence of rain for the upcoming months made me smile. I will never forget the Tuesday volley ball evenings at east beach with sunset, palm trees, dolphins and the moonlight reflected on the surface of in the sea...

During my half year stay at UCSB I was able to gain a lot of experience in RF IC design. I was lucky to be given the opportunity to create designs and perform measurements at Skyworks Inc. in Newbury Park, one hour south of Santa Barbara. With this arrangement, I was both a student at UCSB and an intern at Skyworks Inc. The opportunity to work in a corporate environment in the same area of research was very precious to me.

I am deeply indebted to a long list of people who made this wonderful time possible. I would like to thank Professor Steve Long for his great and warm support during my whole stay, Ken Weller and Nick Cheng of Skyworks Inc. for their extraordinary generosity, Professor Werner Bechtold for helping me getting abroad, and finally Amy Vanmun, Peter Tran and Renato Negra who helped me with the design.

Furthermore, I would like to thank the lab staff at UCSB, in particular Tom Collins, Vikas Manan, Jingshi Yao, Yan Ghao, Joe Lai and David Schmelzer. I would also like to thank the people at Skyworks Inc. who helped me in several ways during the design phase, namely Pete Zampardi, Doel Roy, Bob Williams, Judi Ulmer, Bac Tran, Yuh "Steve" Zhao, Theresa Leyva, Karen Wiktorowicz, and many more.

Contents

1	Introduction	1
1.1	Outline	1
1.2	Task description	1
1.3	Motivation	2
1.4	Design goals	3
2	Power Amplifier in Theory	7
2.1	A generic power amplifier	7
2.2	Definitions of the figures of interest	9
2.2.1	Gain, Power, Efficiency	9
2.2.2	Quality factor Q	10
2.2.3	Linearity	11
2.3	Negative feedback of the common collector	11
2.4	Different modes of operation	14
2.4.1	Class A	14
2.4.2	Class B and AB	18
2.4.3	Class C	18
2.5	Load Impedance	19
2.5.1	Conjugate match versus load-line match	19
2.5.2	Load-line match from CE Class A to CC Class B	20
2.6	Stability analysis	22
2.6.1	Large signal S parameter simulations with two sources	23
2.6.2	Small signal simulation at Class A	24
2.6.3	Small signal simulation at Class B with large signal gain	25
2.6.4	Small signal simulation at Class B	26
2.6.5	Transient Analysis (with two sources)	26
2.6.6	Derivation of a small signal HBT model including large signal parameters	26
2.6.7	Conclusions	27

3	Target technology	29
3.1	Setup	30
3.2	On-Chip	30
3.2.1	Hetero Bipolar Transistor (HBT)	31
3.2.2	Maximum current and voltage	36
3.2.3	Metal layers	36
3.2.4	Spiral inductors	37
3.2.5	MIM capacitors	37
3.2.6	Thin film resistors	37
3.2.7	Through waver vias	38
3.2.8	Bond Pads, Transmission Lines	38
3.3	Off-chip	39
3.3.1	Laminate board	39
3.3.2	Bondwires	39
3.3.3	Transmission lines	45
3.3.4	Spiral inductors	46
3.3.5	0201 components	46
3.3.6	Vias	47
3.4	Evaluation	48
3.4.1	Comparison inductors	48
3.4.2	Comparison capacitors	48
3.4.3	Comparison resistors	49
3.4.4	Conclusions	49
4	Implementation	51
4.1	Design strategy	51
4.2	The active device	52
4.2.1	Ballast resistor	52
4.2.2	Bias point	54
4.2.3	Scaling of the design	60
4.3	The passive network	61
4.3.1	Output network	63
4.3.2	Stabilization resistance	68
4.3.3	Input network	68
4.3.4	Common collector	70
4.4	Simulation setup	71
4.4.1	Load and source pull simulation	71
4.4.2	Stability simulation	72
4.5	Test structures	72
4.6	Layout	74
4.6.1	Layout of the die	74

4.6.2	Layout of the laminate	81
5	Measurements	85
6	Conclusion	87
A	Theory of load and source plane stability circles	89
B	Simulations of on-chip spiral inductors	91
C	LC networks	97

Chapter 1

Introduction

The design and measurements of a common collector class B power amplifier is presented and confronted with the design and measurements of a common emitter power amplifier in order to investigate the advantages and drawbacks of the two architectures in comparison.

1.1 Outline

Starting with this first chapter, task and motivation are quoted [2, 3] and the design goals are specified in both words and numbers. In the following chapter, the theoretical aspects of the power amplifier are explained in order to have a good fundament to get started with the design. In the subsequent chapter, the technology in which the amplifiers are designed are set forth in detail since only a good understanding of the available instruments make the decisions traceable which are made during the design process. Chapter four demonstrates the implementation of the amplifiers based on the knowledge gathered in the preceding chapters. Judgment of the feasibility of the presented architecture is made, founded upon measurement, in chapter five. Furthermore, answers on the questions posed throughout the thesis are presented and concluded in a final, closing chapter.

1.2 Task description

[2, 3] The objective of this project is to design a single-ended common collector amplifier at 1.8 GHz. The main challenge is to provide unconditional stability while still maintaining adequate transducer gain to circumvent power added efficiency compromised by low gain. The technology to be employed

for implementation of the amplifier is the Skyworks InGaP/GaAs HBT process. The amplifier will consist of a chip with input matching and stabilizing networks mounted on a laminate substrate. The laminate will include the output matching network so that higher efficiency can be maintained. Devices and circuits will be fabricated and tested. Up to my knowledge, no one has reported on an RF common collector PA (there may be good reasons for this, but we will see!).

1.3 Motivation

[2, 3] The BJT version of push-pull common drain Class B amplifier is the most widely used topology in the audio regime. The common drain amplifier has the potential to become a linear amplifier with good efficiency, when biased at or above Class B. For common source Class B the transfer function is:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = g_{\text{m,non-linear}} \cdot R_{\text{load}} \quad (1.1)$$

Non-linearity in the trans-conductance $g_{\text{m,non-linear}}$ shows up strikingly in the non-linearity of the net transfer function. However, for the common drain configuration, the transfer function is:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = g_{\text{m,non-linear}} \cdot \frac{R_{\text{load}}}{R_{\text{load}} + \frac{1}{g_{\text{m,non-linear}}}} \quad (1.2)$$

As the trans-conductance is much larger than the conductance of the load, the effect of nonlinear transconductance is much less. In other words, the strong series-series negative feedback presented by the load linearizes the amplifier. The linearity is analyzed in the frame work of push-pull. The circuit diagram and the transfer function at various bias conditions are shown in Figs 1.1 and 1.2 respectively. This analysis does not include the parasitic capacitance, which really hurts the performance at the frequencies higher than one-tenth of the transit frequency f_T ¹. The transfer function is non-linear at Class C conditions as both devices are cut off for part of any given cycle. However, as we approach the Class B bias conditions, the linearity improves drastically. The circuit exhibits low distortion even at Class AB bias and improves further as the bias is increased into Class A

¹As shown in table 3.4 in subsection 3.2.1, the transit frequency of the implemented HBT is essentially higher than ten times the design frequency (46.3 GHz vs. 1.8 GHz). Thus, the parasitic capacitance has no severe impact on this analysis and the assumption is reasonable.

operation. Even if the transfer function is nonlinear about the pinch off, this configuration linearizes the amplifier when biased at Class AB. However, the distortion increases and does not follow this trend as the frequency is increased beyond 10 % of f_T due to capacitance distortion.

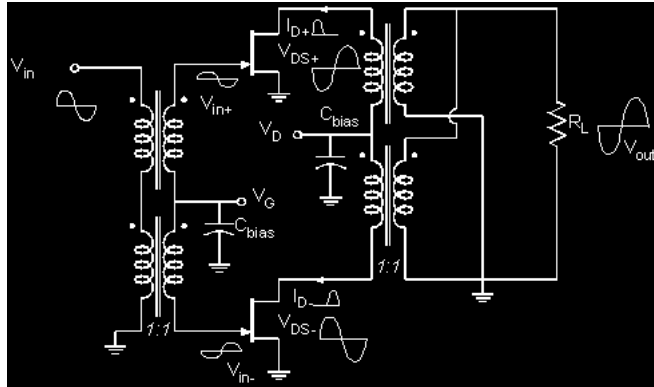


Figure 1.1: Schematic of a push-pull common-drain class B power amplifier [2, 12].

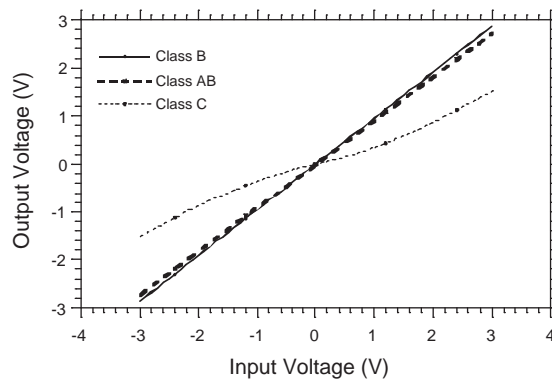


Figure 1.2: Voltage transfer function of the structure in Fig. 1.1 under different bias conditions [2, 12].

1.4 Design goals

As stated before, the design, implementation and measurement of two power amplifiers are to be accomplished:

- Class B common collector

- Class B common emitter

The amplifiers will be implemented single ended, consisting of a single stage and designed for narrow band width as presented in [12]. The core question to be answered is

Given a common collector and a common emitter Class B power amplifier designed in the same manner and technology. In comparison, does the stabilized common collector architecture attain comparable gain and efficiency by exhibiting better linearity, and therefore result in a better over-all performance?

The specifications for the power amplifiers are not given in the task description [2, 3] since the feasibility of a common collector amplifier in general has to be analyzed. The single given number is the design frequency², being 1.8 GHz, indicating the usage in a hand-held device as a GSM cell phone³ with an output power of 1 Watt respectively 30 dBm. The specifications in table 1.1 for the class B amplifiers, referring to -1 dB compression, are chosen to provide a frame for the design with the following comments as a justification:

- Attaining 10 dB gain would be a very good number, though the value must not be much below since it would negatively affect the PAE.
- The output power and the power supply voltage have values that possibly appear in a cell phone.
- The bandwidth is not an issue, say, the design is made for a narrow bandwidth.
- The amplifiers consist only of a single stage and is single ended.
- The amplifiers are optimized for linearity and efficiency.

²The term “design frequency” used throughout this thesis refers to the in table 1.1 specified center frequency of 1.8 GHz.

³European tri-band GSM operates at 900, 1800 and 1900 MHz. US tri-band occupies 800/850, 1800 and 1900 MHz.

Table 1.1: Class B power amplifier specifications, defined at -1 dB compression.

Parameter	Symbol	Value	Unit
Center frequency	f_0	1.8	GHz
Bandwidth	B	200	MHz
Gain	G	10	dB
Output power	P_{del}	1	W
		30	dBm
Power supply voltage	V_{dd}	4	V
Port impedance level	$R_{\text{in}}, R_{\text{out}}$	50	Ω
Number of stages		1	
(Power added) efficiency	PAE, η	maximum	
Linearity		maximum	

Chapter 2

Power Amplifier in Theory

This chapter is thought to be an introduction into the theory of RF power amplifier design. It discusses a conceptual structure of a generic power amplifier, definitions of the key figures, miscellaneous modes of power amplifier operation, and stability investigations. To be pointed out, one section's concern are the peculiarities of the common collector architecture.

2.1 A generic power amplifier

The power amplifiers presented in this thesis basically consist of an active device as the amplifying element and a passive network connected to each, the input and the output port, as illustrated in Fig. 2.1.

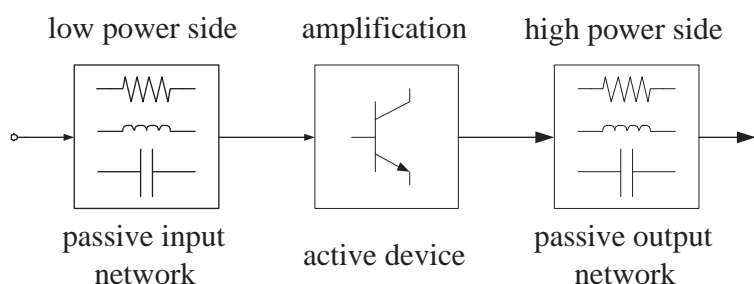


Figure 2.1: Very simplified diagram of a single stage power amplifier.

Dividing the circuit into two different types of blocks, it is reasonable to investigate the duties of each block in order to achieve the design goals including figures like output power, gain, linearity and efficiency. Surprisingly, the allocation of the tasks turns out to be uneven...

Active device The task of the active device is to amplify the signal input power via multiplying the current and/or voltage by a constant factor. The device is mostly an array of transistors, e.g. HEMTs, HBTs, MOSFETs or BJTs. Requirements on operating frequency, maximum collector / drain current, maximum output voltage and linearity determine the choice of the device type and number.

The particular active device as part of the design presented in this thesis consists of an array of several HBTs in parallel. Therefore, it is in the following chapters consecutively referred to as “the HBT” or “the HBTs”.

Yet it is the heart of the PA, it is not the main concern of the design, as in contrast to a CMOS analog integrated circuit, since the laid out transistor is given as part of a technology and only few degrees of freedom are on-hand. One could be very mischievous and say that it is the donkey which pulls the cart (or from the point of view of a device engineer, the engine in a racing car).

Passive network The engineering of the passive input and output network is the essential part of the PA design. The function of this circuits includes to ...

Stability ... ensure and maintain stability of the amplifier for defined load and source impedances.

Matching ... transform the impedance levels at the ports of the active device to a desired interface level, e.g. 50Ω .

Filtering ... filter the out of band frequency components in both directions. Ideally, the outer world and the active device should be isolated from each other below and above the design frequency. Mind that there are (dc) connections to the circuit through the bias and power supply which can be a source of disturbing signals if their ac parts are not cleared!

Wave shaping ... provide short circuits to ground for a particular list of harmonics and suppress the remaining components. The voltage and current waves flowing through the active device are hence shaped, e.g. to half-sine waves, allowing a particular mode of operation. The harmonic shorts and suppressions are part of the output network.

Biasing ... bias the active device. The biasing of the transistor determines together with the wave shaping the class of operation and therefore figures as linearity, efficiency and gain.

2.2 Definitions of the figures of interest

2.2.1 Gain, Power, Efficiency

To start have a look at the illustration in Fig. 2.2. The gain G of the amplifier is simply defined as the amplification of the available power P_{avs} at the input port to the power P_{del} delivered to the load resistance R_{load} . P_{del} is calculated by the fundamental components (frequency f_0) of the load current I_{load} and load voltage V_{load} as showed below.

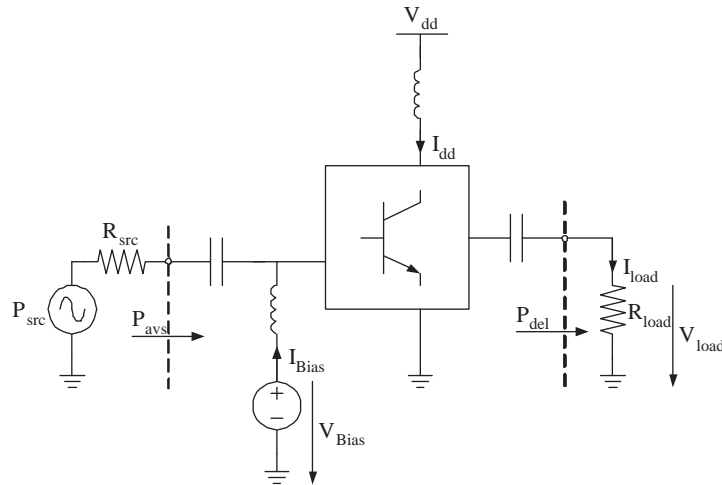


Figure 2.2: PA schematic.

$$G = \frac{P_{del}}{P_{avs}} \quad (2.1)$$

$$P_{del} = \frac{1}{2} \operatorname{real}(\underline{V}_{out} \cdot \underline{I}_{out}^*) \Big|_{f=f_0} \quad (2.2)$$

The dissipated dc power consists of two contributions, one being the power supply (V_{dd} times I_{dd}), and the other being the (less significant) bias voltage source (V_{Bias} times I_{Bias}).

$$P_{dc} = V_{Bias} \cdot I_{Bias} + V_{dd} \cdot I_{dd} \approx V_{dd} \cdot I_{dd} \quad (2.3)$$

The main concern of a power amplifier design is to achieve a good efficiency η , i.e. the ratio between the delivered power at the fundamental frequency and the dissipated dc power. Furthermore, taking into account the amplification capability of the amplifier, the power added efficiency (PAE) can be defined.

$$\eta = \frac{P_{del}}{P_{dc}} \quad (2.4)$$

$$\text{PAE} = 100 \cdot \frac{P_{del} - P_{avs}}{P_{dc}} [\%] = 100 \cdot \eta \left(1 - \frac{1}{G}\right) [\%] \quad (2.5)$$

2.2.2 Quality factor Q

In the following chapters, the quality factor (Q) of an RLC resonator is mentioned repeatedly. It is defined as the ratio of the stored energy and the average dissipated power, multiplied by the frequency. Regarding a parallel configuration with a resistor, a capacitor and an inductor in parallel, the equation for the Q is listed below. Notice that at resonance frequency $\omega_0 = \frac{1}{\sqrt{LC}}$, the amplitude of the current through the reactive devices is Q times the current delivered by the source.

$$Q_p = \frac{R}{\sqrt{L/C}} = \frac{R}{\omega_0 L} = \omega_0 RC \quad (2.6)$$

$$|I_{L,\omega_0}| = |I_{C,\omega_0}| = Q|I_{in,\omega_0}| \quad (2.7)$$

For the Q of the series RLC resonator with the three devices in series see the equation below. Here, the voltage across the reactive devices is multiplied by Q.

$$Q_s = \frac{\sqrt{L/C}}{R} \quad (2.8)$$

$$|V_L| = |V_C| = Q|V_{in}| \quad (2.9)$$

Finally, it is important to state that the bandwidth of the resonator is inverse proportional to the Q. It will be shown later that a higher Q is required to ensure good harmonic shorts for an amplifier with a lower output impedance level. Due to the lower bandwidth, the requirement on the precision of the devices increases in order to achieve the short at the correct frequency.

$$\frac{\text{BW}}{\omega_0} = \frac{1}{Q} \quad (2.10)$$

2.2.3 Linearity

A first way to describe linearity is defined straight forward as the derivative G' of the gain G where zero stands for perfect linearity. If G' at higher power levels starts to deviate from zero, compression ($G' < 0$) or expansion ($G' > 0$) occurs. However, this definition is a pure amplitude to amplitude analysis at the design frequency and does not take into account anything like bandwidth or phase shift. This finds application later on in this thesis to find the bias point with maximum constant gain.

$$G' = \frac{dG}{dP_{in}} \quad (2.11)$$

Another, widely prevalent definition is based on a two tone signal analysis. Two sine signals (f_1 and f_2) separated by a very small frequency offset ($f_2 - f_1 \ll f_1$) and amplified by a nonlinear amplifier produce frequency components lying very close by to the signal frequencies. This components are caused by the third and fifth order term of the (nonlinear) transfer function and are called *third* respectively *fifth order intermodulation products* (IM3 resp. IM5). The telecom industry is highly interested in keeping them as low as possible since for a modulation incorporating frequency multiplexing, the intermodulation products fall into the neighboring channels¹. The IM3 suppression (IM3S) is now the ratio between the two tone powers and the power of the intermodulation products. All powers in the equation below are referred to the output.

$$\text{IM3S} = \frac{P_{f_1} + P_{f_2}}{P_{2f_1-f_2} + P_{2f_2-f_1}} \quad (2.12)$$

2.3 Negative feedback of the common collector

In a CC structure the input and the load resistance are in series in contrast to the parallel configuration for the CE amplifier, see Fig. 2.3. This has

¹Another definition which is even more specific for the telecom industry is called *adjacent channel power ratio* (ACPR) where the two tones are replaced by two actual modulated signals. Since the amplifier is designed for a single frequency without any claim on bandwidth, this measurement would not lead to meaningful results.

two main effects, namely a better linearity and an increased tendency to instability.

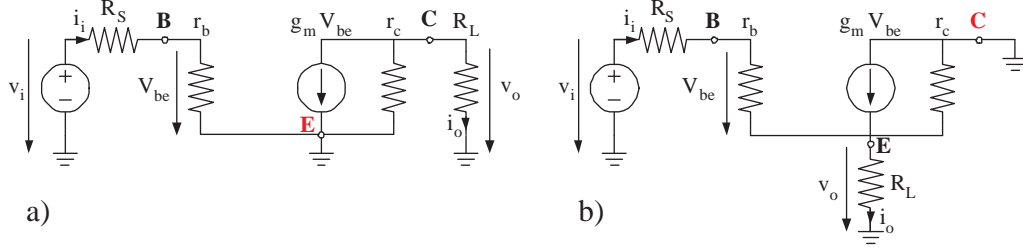


Figure 2.3: Simplified small signal equivalent circuit of the CE a) and the CC b) architecture.

The analysis of the small-signal equivalent circuit of the CE can be done in a straight forward manner, resulting in a voltage gain A_v of

$$A_v = \frac{v_o}{v_i} = \frac{r_b}{R_S + r_b} g_m \cdot r_c \parallel r_L = \frac{r_b}{R_S + r_b} \frac{g_m r_c r_L}{r_c + r_L} \approx g_m r_L \quad (2.13)$$

with the input and output resistance seen at the transistor terminals towards the transistor as listed subsequently. The CE structure has a high resistance level at both the input and the output.

$$R_i = r_b \quad (2.14)$$

$$R_o = r_c \quad (2.15)$$

Notice that the voltage gain is directly proportional to the non-linear transconductance g_m . The input and output resistances do not depend on each other, i.e. the amplifier is unilateral. The current gain β_0 is related to the g_m by the following equation:

$$g_m V_{be} = \beta_0 i_i \quad (2.16)$$

The CC case is a bit more complicated and due to the topic of this thesis, a closer look is taken. Again, see figure 2.3, this time for the CC small signal equivalent circuit. [5] From a large-signal standpoint, the output voltage v_o is equal to the input voltage v_i minus the base-emitter voltage V_{be} . Since the base-emitter voltage is a logarithmic function of the collector current, the base-emitter voltage is almost constant even when the collector current varies. If the base-emitter voltage were exactly constant, the output voltage

of the common-collector amplifier would be equal to the input voltage minus a constant offset, and the small-signal voltage gain of the circuit would be unity. For this reason, the circuit is also known as an emitter follower because the emitter voltage follows the base voltage.

When the input voltage v_i increases, the base-emitter voltage of the transistor increases, which increases the output current i_o . However, increasing i_o increases the output voltage v_o , which decreases the base emitter voltage by negative feedback. The key point here is that the common collector configuration is not unilateral. As a result the input resistance depends on the load resistor R_L and the output resistance depends on the source resistance R_S . As a benefit, the negative feedback lowers the sensitivity of the voltage gain on the nonlinear transconductance g_m . In the simple small signal model of 2.3, the nonlinear base capacitance is neglected which is an oversimplification at RF frequencies.

The equation for the voltage gain is listed below. For a large r_c and $g_m R_L$, the voltage gain approaches unity and the amplifier performs a voltage follower.

$$\begin{aligned} A_v = \frac{v_o}{v_i} &= \frac{R_L r_c (g_m r_b + 1)}{r_b r_c + r_c R_S + R_L (g_m r_b r_c + r_b + r_c + R_S)} \\ &\approx \frac{R_L (g_m + \frac{1}{r_b})}{1 + \frac{R_S}{r_b} + R_L (g_m + \frac{1}{r_b})} \approx 1 \end{aligned} \quad (2.17)$$

The input (R_i) and output (R_o) resistance is given in [5]. R_i can be calculated by removing the input voltage source and driving the input by a current source; for R_o , the load resistance R_L has to be removed and the Thevenin-equivalent resistance by looking into the output terminal has to be found.

$$R_i = r_b + (\beta_0 + 1)(R_L \parallel r_c) \quad (2.18)$$

$$R_o = \left(\frac{r_b + R_S}{\beta_0 + 1} \right) \parallel r_c \approx \frac{1}{g_m} + \frac{R_S}{\beta_0 + 1} \quad (2.19)$$

The emitter follower has high input resistance, low output resistance, and near-unity voltage gain. It is most widely used as an impedance transformer to reduce loading of a preceding signal source by the input impedance of a following stage. It also finds application as a unity-voltage-gain level shift because the dc output voltage is shifted from the dc input voltage by V_{be} , respectively by once the threshold voltage. Due to the tendency to instability and the unity voltage gain this structure is rarely used for signal amplification.

2.4 Different modes of operation

A short summary of the classic modes of amplifier operation are presented and the important trade offs are pointed out. Detailed treatment of the topic can be found in [5, 8, 10]. In general, a distinction is made between two major types of power amplifiers: transconductor type amplifiers (Classes A, AB, B and C) and switching type amplifiers (Classes D, E and F).

2.4.1 Class A

For the Class A amplifier, the bias is chosen so that the amplifier works linearly. By setting the bias voltage exactly in the middle between the cut-off voltage and the saturation voltage, a maximum efficiency of 50 % can be achieved. The signal level must not exceed these two limits in order to avoid clipping, see blue curve in the first graph of Fig. 2.4. A major drawback of this structure is that for zero input signal power, the amplifier still dissipates the same dc power. Power wasted in such a standby period causes two problems. First, in battery-operated equipment, it has a severe impact on the battery life time and should therefore be avoided. Second, any power wasted in the circuit is dissipated in the active devices, increasing their operating temperatures and thus the chance of failure. The classes presented later on will sacrifice linearity and gain for an increased efficiency and much lower dc dissipation for zero input signal power.

The conduction angle is defined as the part of a period during which the transistor is carrying current. For Class A, this angle is 2π since the transistor is switched on during the whole period of a sine wave. By lowering the bias point, the swing of the signal brings the input voltage temporarily below the cut off voltage, the transistor switches off and the conduction angle is reduced consequently. However, by only reducing the conduction angle no improvement in efficiency is achieved. It is also necessary to increase the input drive level and to provide suitable impedance terminations at harmonics of the signal frequency. Increasing the input level by maintaining the output level signifies lower gain. Defining V_q as the bias point and $V_t = 0$ as the idealized cut off voltage, the required signal voltage amplitude will be

$$V_s = 1 - V_q \quad (2.20)$$

In figure 2.4 the base emitter voltage waveform (V_{be}), the collector emitter voltage waveform (V_{ce}) and the collector emitter current waveform (I_{ce}) are plotted for all four classes. Notice the increase of the input signal power for higher classes of operation reducing the over all gain of the amplifier.

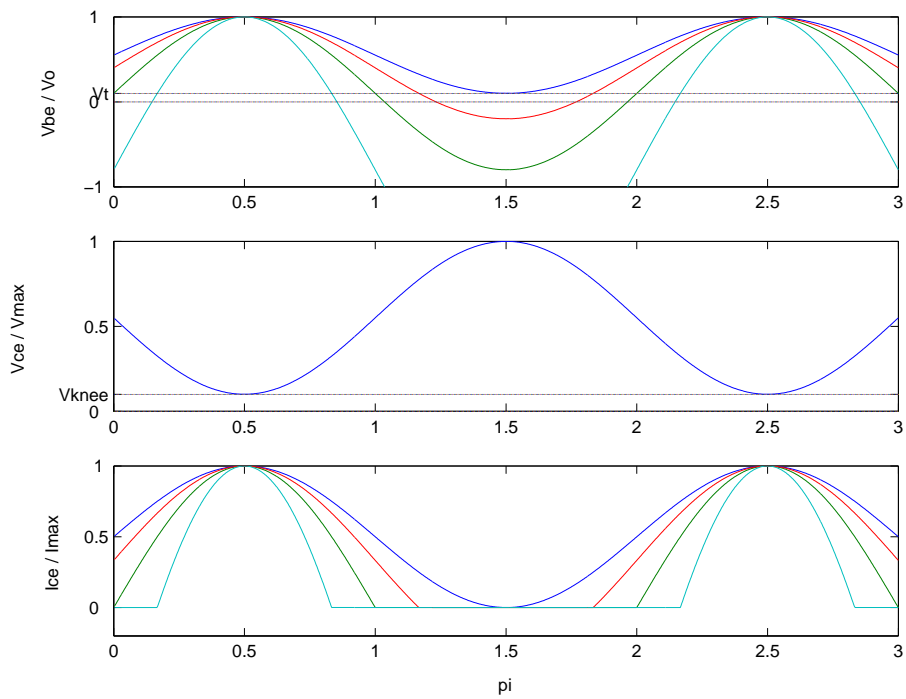


Figure 2.4: Normalized voltage (V_{be} , V_{ce}) and current (I_{ce}) waveforms for Classes A, AB, B and C.

Furthermore, the output voltage waveform stays the same for all classes, whereas the output current waveform tends to become a half sine wave. These waveforms are obviously of mathematical nature, neglecting nonidealities and nonlinearities of a real transistor.

It is intuitive that the dc current component will decrease as the conduction angle is reduced, resulting in higher efficiency. However, it is less obvious what happens to the fundamental component; furthermore, harmonics will be generated. A Fourier analysis of the current wave forms of figure 2.4 is done in [8] and the Fourier components can be calculated by solving the following integral, where α is the conduction angle.

$$I_n = \frac{1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} [\cos(\theta) - \cos(\alpha/2)] \cos(n\theta) d\theta \quad (2.21)$$

Evaluating the integral in equation (2.21) for $n = 0$ gives the dc term. The fundamental term is given for $n = 1$, analogous the term for the n^{th} harmonic. The Fourier components of the emitter current versus a sweep over the conduction angle is plotted in Fig. 2.5.

$$I_{dc} = \frac{I_{max}}{2\pi} \frac{2 \sin(\alpha/2) - \alpha \cos(\alpha/2)}{1 - \cos(\alpha/2)} \quad (2.22)$$

$$I_1 = \frac{I_{max}}{2\pi} \frac{\alpha - \sin(\alpha)}{1 - \cos(\alpha/2)} \quad (2.23)$$

$$I_{n \geq 2} = \frac{2I_{max}}{\pi} \frac{[\cos(\alpha/2) \sin(n\alpha/2)]/n - [\cos(n\alpha/2) \sin(\alpha/2)]}{(n-1)(n+1)(1 - \cos(\alpha/2))} \quad (2.24)$$

All harmonics of the load are shorted and generate no voltage, so the collector emitter voltage is a pure sine wave whose magnitude will be set by the load resistor value to generate the maximum permissible voltage swing, in a fashion similar to the previous consideration of a class A amplifier. The output signal power and the dissipated dc power are therefore calculated by the following equation, the efficiency η and the PAE are given in equations (2.4) and (2.5). The RF output power and the efficiency versus a sweep over the conduction angle are showed in Fig. 2.6.

$$P_1 = \frac{V_{dc}}{\sqrt{2}} \cdot \frac{I_1}{\sqrt{2}} \quad (2.25)$$

$$P_{dc} = V_{dc} \cdot I_{dc} \quad (2.26)$$

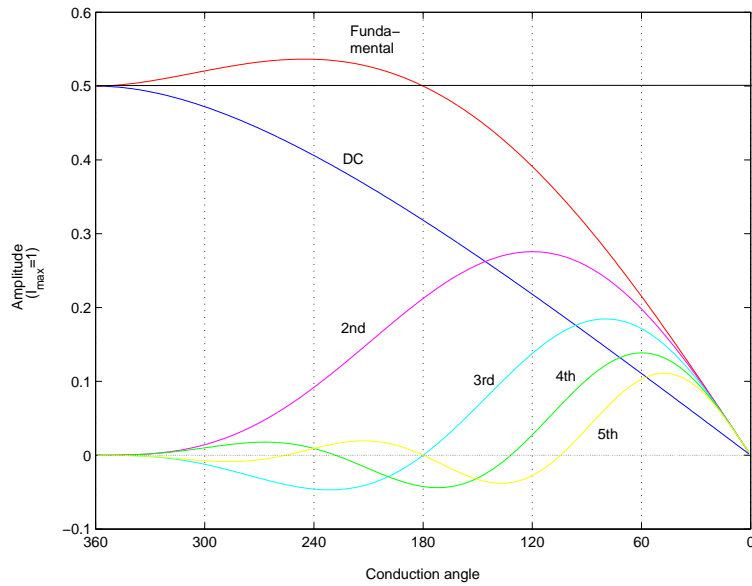


Figure 2.5: Normalized ($I_{max} = 1$) collector emitter current decomposed into Fourier components versus a sweep over the conduction angle.

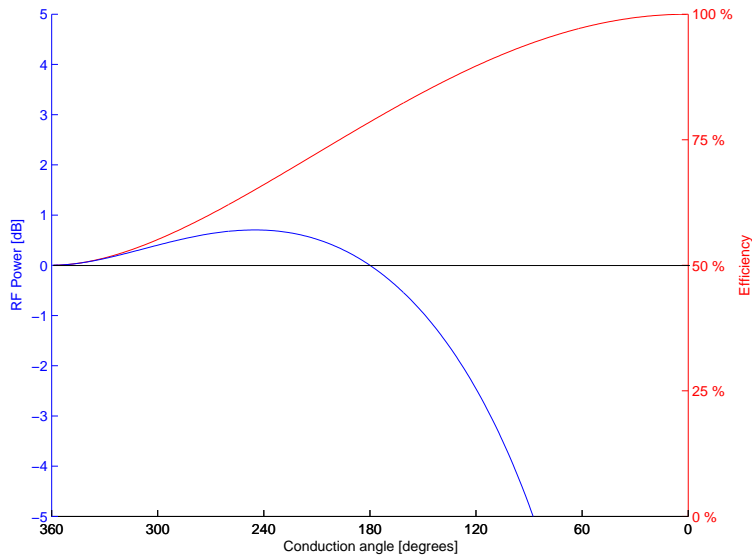


Figure 2.6: RF output power and efficiency versus a sweep over the conduction angle.

2.4.2 Class B and AB

For class B, the bias voltage equals the cut off voltage, resulting in a conduction angle of half the period and a half sine wave for the output current. An exact 50 % conduction duty cycle is a mathematical point, of course, so true class B amplifiers do not actually exist. Class B amplifiers are usually built in a push-pull configuration of two transistors as shown in Fig. 1.1 in the first chapter. In contrast to the class A mode, no (or much less) current flows at zero input signal. The maximum efficiency is $\frac{\pi}{4}$ or 78.5 %. In table 2.1, the current magnitudes of the Fourier components for class B are listed. For the ideal case, all odd current harmonics are zero, so shorts have to be provided for the even harmonics. A small bias adjustment around the Class B (conduction angle of π) point can be considered to be a viable method of controlling the precise level of the third harmonic component. This results in a good linearity as no odd order intermodulation products appear (IM3 and IM5). Notice that the fundamental current has the same magnitude as at Class A.

A conduction duty cycle somewhere between 50 % and 100 % is typical for Class AB being the mode for most practical power amplifier implementations with high linearity requirement.

Table 2.1: Normalized current magnitude of individual frequency components at a conduction angle of 180° (class B).

Frequency component	Normalized on I_{max}
dc	0.3183
Fundamental	0.5000
2 nd	0.2122
3 rd	0.0000
4 th	-0.0424
5 th	0.0000

2.4.3 Class C

If the bias is arranged to cause the transistor to conduct less than half the time, class C operation is obtained. For a conduction angle shrinking towards zero, the efficiency approaches 100 %. An easy and hence popular way is to connect the base to ground resulting in zero bias voltage. Large efficiency

can then be achieved at the cost of reduced power-handling capability, gain, and linearity.

2.5 Load Impedance

It is generally known that the most power is transferred to a load if there is a conjugate match of the generator output impedance to its load impedance.

$$Z_{out} = Z_{load}^* \quad (2.27)$$

However, in literature [8, 9] another principle is proposed named load-line match. Why is a conjugate matched load not optimal in order to extract maximum power out of the device?

2.5.1 Conjugate match versus load-line match

A conjugate match does not take into account the physical limits of the active device in terms of maximum current and voltage. Take for an example [8] the simple case in which the current generator can supply a maximum limiting current of 1 A and has an output resistance of $R_{out} = 100 \Omega$, please refer to Fig. 2.7 for an illustration. Applying the conjugate match theorem, a load of $R_{load} = 100 \Omega$ would be selected for maximum power transfer leading to a very large voltage across the generator terminals of $V_{out} = 50 \text{ V}$. If the current generator were the output of a transistor, it is likely that this would exceed the voltage rating, V_{max} , of the device; in addition, the transistor voltage would be limited by the available dc supply.

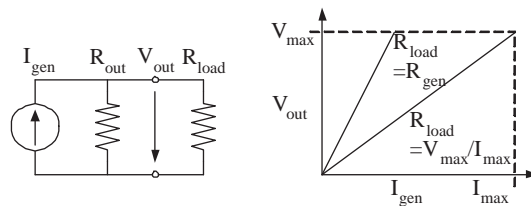


Figure 2.7: Conjugate match and load-line match.

In the presented example, the maximum voltage would be reached much before the maximum current would be attained; the transistor is not used to its full capacity. To utilize the full range of current and voltage, a lower value of load resistance would need to be selected, referred to as load-line match, R_{opt} , which in the simplest form simply would be the ratio

$$R_{opt} = V_{max}/I_{max} \quad (2.28)$$

where it has been assumed that $R_{out} \gg R_{opt}$. In fig 2.8 the load-line for Class A is showed. For the low-voltage configuration used in his thesis, the power supply voltage $V_{dd} = 4$ V is much lower than the collector-emitter breakdown voltage² ($V_{bCE} = 12.9$ V), therefore V_{max} is determined by V_{dd} .

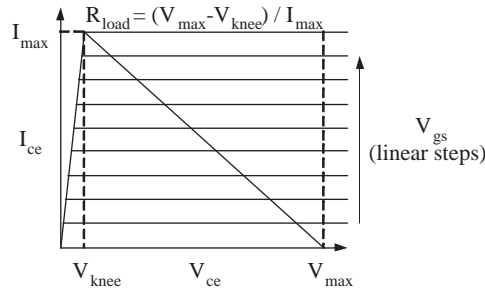


Figure 2.8: Load line in a I_{cc} versus V_{ce} plot.

2.5.2 Load-line match from CE Class A to CC Class B

In Class A operation, the dc part of the output voltage and current are ideally half of the maximum voltage, likewise are the voltage and current of the fundamental.

$$V_{dc} = V_1 = \frac{V_{max}}{2} = V_{dd} \quad (2.29)$$

$$I_{dc} = I_1 = \frac{I_{max}}{2} \quad (2.30)$$

The optimum load resistance that has to be presented in order to utilize the full voltage and current range of the transistor according to the load-line match concept, is

$$R_{opt} = \frac{V_{max}/2}{I_{max}/2} = \frac{V_{dc}}{I_{dc}} = \frac{4 \text{ V}}{26.325 \text{ mA}} = 304 \ \Omega \quad (2.31)$$

²The breakdown voltages of the implemented HBT are listed in table 3.3 in subsection 3.2.1.

resulting³ in 304Ω . Two factors complicate this simple reasoning. The first is that the knee in the I/V curve makes it impossible to have I_{max} at zero V_{ce} , lowering output power and efficiency. The second is due to the nonlinearities of the HBT, so the $I_{ce}(t)$ waveform is generally not sinusoidal.

This optimum load resistance *does* depend on the mode of operation. However, as can be seen in Fig. 2.5, the current at the fundamental frequency has the same value at Class B ($\alpha = \pi$) and at class A ($\alpha = 2\pi$). Furthermore, the collector emitter voltage is the same, so the load resistance for Class B and Class A are equal. The same argumentation holds comparing a CE and a CC amplifier. Since the voltage and current waves are the same, the load resistance is transferable.

In the load resistance calculations above, the knee voltage V_{knee} is neglected. For a real transistor, the minimum voltage $V_{ce,min} = V_{knee}$ is greater than zero at maximum $I_{ce,max}$ (see Fig. 2.9). As a consequence, the V_{dc} is not simply $V_{max}/2$ but rather

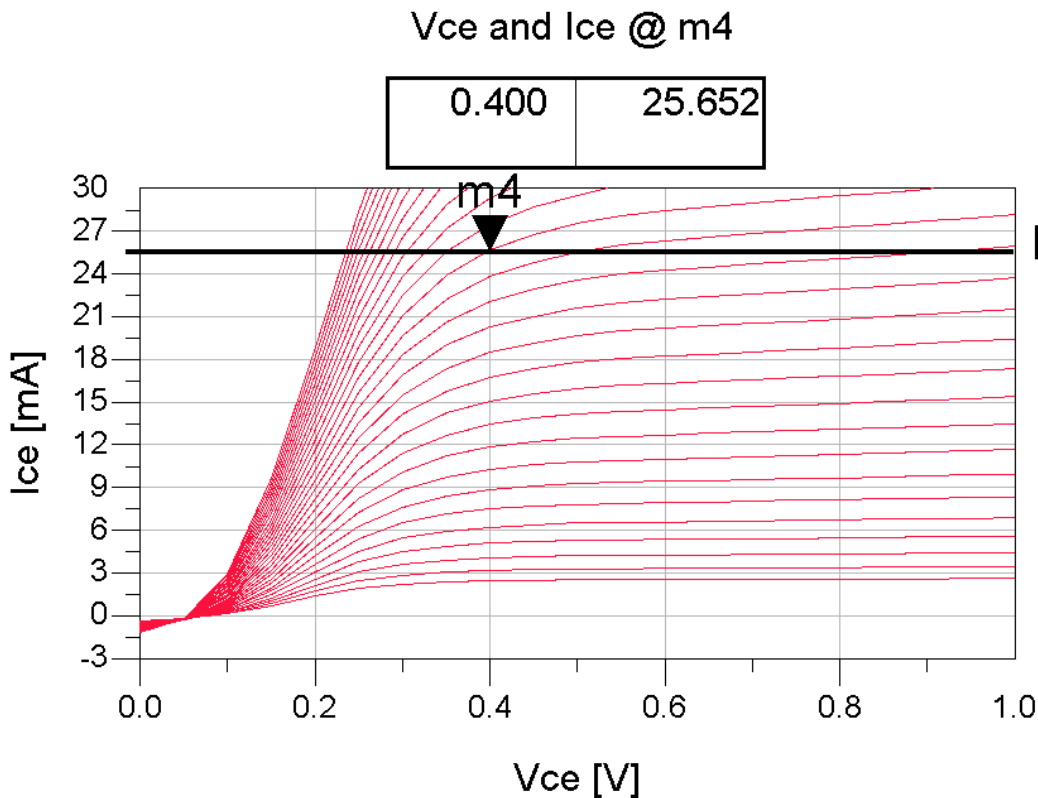


Figure 2.9: I_{ce} versus V_{ce} plot to determine the knee voltage.

³The value of I_{max} is taken from table 3.2.

$$V_{dc} = \frac{V_{max} - V_{min}}{2} + V_{min} = \frac{V_{max} + V_{min}}{2} \quad (2.32)$$

Since $V_{dc} = V_{dd} = 4 \text{ V}$ and $V_{min} = V_{knee} = 0.4 \text{ V}$, V_{max} results in

$$V_{max} = 2(V_{dd} - V_{knee}) + V_{knee} = 2V_{dd} - V_{knee} = 7.6 \text{ V} \quad (2.33)$$

With the maximum voltage, we can designate the optimum load resistance according to

$$R_{opt} = \frac{V_{max} - V_{min}}{I_{max} - I_{min}} = \frac{7.6 \text{ V} - 0.4 \text{ V}}{26.325 \text{ mA}} = 273.5 \text{ } \Omega \quad (2.34)$$

By taking into account the knee voltage, the optimum load resistance becomes slightly reduced.

2.6 Stability analysis

The topic of power amplifier stability is treated very faintly in publications. Presumably, a regular CE amplifier design is like to be stable. In contrast, the CC amplifier has a high tendency to instability, making the problem much more acute, so a way to predict the extent of instability has to be found.

The theory of the stability circles is treated in [6, 7] and will not be discussed here. For convenience, the stability equations and a guide line how to interpret the stability circles is summarized in the appendix A. Since the theory is based on amplifiers operating at small signal levels, it is likely not to be adequate for power amplifier designs.

The term unconditional stability, designating a stable amplifier for every combination of passive input and output termination, is often proposed as the design goal for a stable amplifier. The equations expressing this condition with K as the stability factor and Δ as defined in the appendix A are

$$K > 1 \text{ and } |\Delta| < 1 \quad (2.35)$$

To fulfill unconditional stability for the common collector amplifier, a substantial part of the gain would have to be sacrificed. In practice, the amplifier is most likely embedded into a radio circuit with a well defined interface impedance level, making it pointless to ensure stability for every possible impedance combination. Hence, for the presented circuit, stability has to be ensured for the case of $50 \text{ } \Omega$ plus minus a tolerance in terms of resistance and reactance. Nevertheless, the impedance levels causing instability

should be determined. As a conclusion, not unconditional stability has to be achieved but rather unconditional knowledge about stable and unstable regions in terms of frequency and impedance levels.

A stringent but not sufficient condition for stability at the given impedance levels is that for the whole frequency spectrum the absolute values of the reflection coefficients are below unity.

$$|S_{11}| < 1 \text{ and } |S_{22}| < 1 \quad (2.36)$$

Additionally to the fulfillment of these conditions, the stability circles have to be inspected to ensure a sufficient large range of stable impedances, especially if with some tolerance of the port impedances has to be reckoned.

The utilized software to simulate the behavior of the circuit is Agilent's Advanced Design System (ADS). As many other software packages, it offers the possibility to perform small signal S-parameter simulations. Since the power amplifier operates at power levels way beyond small signal, applying the above stated conditions on such a simulation might not allow correct predictions about stability. The upraising question is how to simulate the stability and how to apply the theory of the stability circles in order to have a good predication. Several propositions are presented in the subsequent sections and concluded finally.

2.6.1 Large signal S parameter simulations with two sources

Since the power dependence of the parasitics of the transistor is likely to have an impact on the stability behavior, this kind of simulation promises to be the most appropriate. The idea is to start with a harmonic balance simulation setup and insert twice, before the load resistance and after the input signal generator, an ideal, loss less, directive coupler. The coupler copies the signal from either direction to a 50Ω resistance so that the S-parameters can be determined based on the voltage. Furthermore, a second signal generator at the output is added operating at very low power and a small frequency offset $f_0 + f_{off}$. See Fig. 2.10 for a screen shot of the schematic in ADS. The equations for the S-parameters are listed below.

$$S_{11} = \frac{V_{b_1, f_0}}{V_{a_1, f_0}} \quad (2.37)$$

$$S_{21} = \frac{V_{b_2, f_0}}{V_{a_1, f_0}} \quad (2.38)$$

$$S_{12} = \frac{V_{b_1, f_0 + f_{off}}}{V_{a_2, f_0 + f_{off}}} \quad (2.39)$$

$$S_{22} = \frac{V_{b_2, f_0 + f_{off}}}{V_{a_2, f_0 + f_{off}}} \quad (2.40)$$

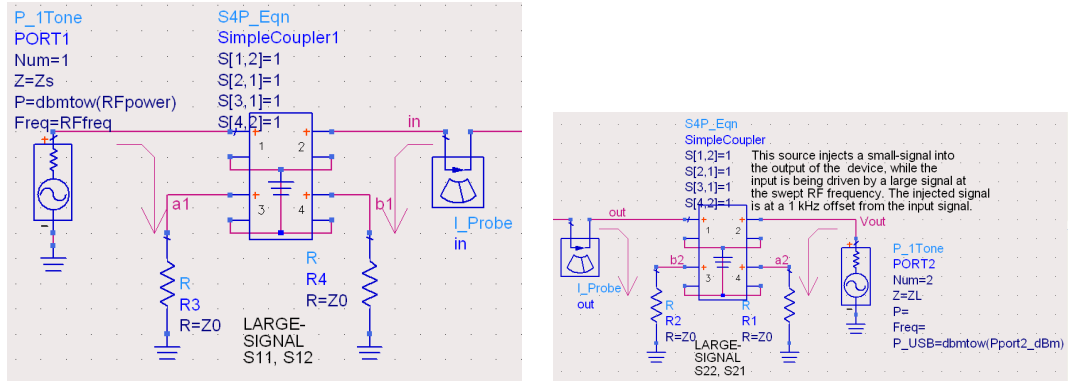


Figure 2.10: Ideal, lossless, input and output coupler allowing to determine the large signal S-parameters in ADS.

ADS offers this setup in one of its libraries. Unfortunately, the results turned out not to be very credible since the simulated gain differed from the one determined by the HB simulation. A reason might be that the ideal behavior of the directed coupler confuses the HB simulation. The results for low power should perfectly match the results of the small signal simulation which does not hold. Finally, a very high sensitivity to the stability resistors is observed. A question to be answered would be at what power level is the highest probability for instability and is it sufficient to ensure stability at this power level?

2.6.2 Small signal simulation at Class A

Another approach is to state that if the amplifier is stable at Class A operation, it will also be stable at Class B. The argumentation is that the gain at Class A operation is higher than for Class B and increased gain causes

higher instability. However, this approach is very conservative and therefore of poor utility since more gain is annihilated as necessary to ensure stability. Furthermore, the power dependence of the parasitics is neglected.

2.6.3 Small signal simulation at Class B with large signal gain

An intuitive approach is to determine the large signal g_m of the amplifier by connecting the two peak points in the I_{ce} versus V_{be} time domain chart and looking for a tangent with the equivalent g_m in the dc large signal behavior of the transistor, i.e. determining a new bias point which would give the same transconductance for the small signal simulation as there is for the large signal behavior. Stability indicators like the K factor, $|\det|$ and the source and load plane stability circles can now be determined. The detailed procedure is described below:

1. Plot in time domain I_{ce} versus V_{be} of an HB simulation at the desired power level and frequency.
2. Determine the large signal g_m by either
 - average the g_m over the whole period
 - or simply take the two extremal values and calculate $\frac{I_{ce,max}-I_{ce,min}}{V_{be,max}-V_{be,min}}$
3. Plot I_{ce} versus V_{be} of a dc simulation of the transistor and determine the bias voltage V_{be} at which the transistor has the equivalent g_m , i.e. look for the tangent with the slope g_m at the IV -curve.
4. Perform a small signal stability simulation of the whole amplifier at the new bias point.
5. Check stability circles and input and output reflection coefficients.

However, for the Class B bias point selected in this thesis, the transistor has its maximum gain at small signal levels and mainly maintains its gain over increased power levels until the compression point. Therefore, at a higher power level, the gain is reduced and therefore the stability increased, i.e. the bias point for the large signal g_m is below the original bias point.

Performing several simulations at various bias levels, an increased instability is observed at higher bias, making the presumption reasonable that a stable Class A operation is a sufficient but conservative condition, as stated earlier.

This approach might be interesting for amplifiers operating at modes above Class B because they exhibit a point with maximum gain due to initial expansion followed by compression for a sweep over power. The tangent g_m for this maximum gain could be easily determined and would probably be the point of maximum tendency to instability.

2.6.4 Small signal simulation at Class B

In theory, the output of a Class B amplifier driven with zero input signal is cut off, say, there is no current flowing and therefore zero gain. In reality, the highest gain is found at zero input power and the gain decreases with increasing input power due to compression of the transistor. Neglecting the power dependent reactive devices, zero input power should be the problematic point for instability and the small signal simulations would be sufficient.

2.6.5 Transient Analysis (with two sources)

Instead of a simulation performed in frequency domain, a transient analysis is made and the waveforms are inspected for ringing or the spectrum of the waveforms is examined for unwanted components. Additionally, two sources, as presented in the large signal S-parameter simulation, would include the effects of signals reflected at the output load.

Transient analysis is a poor way to determine stability because the simulation is expensive in terms of calculation and data outlay and because the interpretation of the simulation results is problematic. In case the simulated time span is not long enough or the frequency resolution is too coarse, ringing can easily be overlooked. As a conclusion, this procedure is inferior to a frequency domain analysis, however it may suit as a way to double check the simulations as it is the only procedure which is not based on S-parameters.

2.6.6 Derivation of a small signal HBT model including large signal parameters

The final idea is to derive a model of the transistor to represent the behavior at a particular power level which can be embedded in a small signal stability simulation. This model should take into account the relevant power dependent reactive devices. A good understanding of the transistor and the causes for ringing is necessary for the synthesis of an accurate model. This method is considered as complex and troublesome.

2.6.7 Conclusions

The core question is if the following statements hold:

- There is a power level that has maximum tendency to stability.
- This power level is always the point with maximum gain.
- The power dependent reactive parasitics have no big influence on the stability behavior at the frequencies of interest.

The first two statements seem to be true, the third will be reviewed during the measurements of the circuit. The two CE circuits seemed to be stable by default whereas the stability circles of the CC circuit showed high sensitivity to changes of the stabilization resistors.

The small signal analysis seems to be the best but not satisfying indicator for stability of the Class B CC circuit. Thus, the topology of the circuit will be chosen the way that stabilizing resistors can be inserted and changed flexibly so that a tuning for stability will be possible.

Chapter 3

Target technology

Despite the fact that this thesis is about the design of a common collector power amplifier, a whole chapter is dedicated to the technology in which this amplifier is designed, going into every detail of each available type of component. This is appropriate since only with a good understanding of the technology the outcome of a design will be successful. Additionally, the art of a power amplifier design does not lie in the drawing of a schematic but much more in the practical realization of it, for the technology imposes the rules for what is possible and what is not. Simulations with ideal components show a hypothetical, maximum attainable performance. Therefore, nothing but a fabricated and measured circuit is a valid prove if a particular concept is feasible (for a specific technology). Finally, a deep analysis of the technology is necessary to ascertain the cause of a nonfunctioning circuit.

The process provided by Skyworks Inc. for the design of common emitter power amplifiers for the cell phone industry is presented in this chapter. The process is mature and optimized for the same frequency range and almost the same type of circuits, making it optimal for this project.

It offers various ways to implement an inductance, a capacitance, a resistance and an HBT. The choice of the components has a great influence on the design and redesigns became necessary in order to optimize the performance of the circuit when a component turned out to be unsuitable.

In a first section, the setup of the circuit is explained. The performance of the various components off- and on-chip are presented subsequently. Finally, the components are compared and for each component, the optimal role in the design is allocated.

3.1 Setup

The circuit consists of an integrated circuit, a laminate board and a PCB test board.

IC The core of the design is the die with on-chip components such as HBTs, spiral inductors, MIM capacitors, thin film resistors and through-wafer vias connecting to a backside metallization. It would be possible to do a monolithic design, though off-chip components allow to achieve a better (power added) efficiency. The IC is fabricated in-house and measures $900 \times 1200 \mu\text{m}$.

Laminate The chip is mounted on a 4 layer laminate board carrying off-chip components like other ICs, spiral inductors, transmission lines and vias to ground. The connection between the die and the laminate is done by hand soldered bond wires and by the backside metallization connected to ground. Since the fabrication of the laminate is not done in-house, the production and shipping causes a long waiting time. The die and the laminate together build the power amplifier circuit. The dimensions of the laminate board are $5 \text{ mm} \times 8 \text{ mm}$.

Test board The laminate board is mounted on a PCB test board¹ which contains 50Ω SMA connectors, dc pins for the power supply, the bias voltage and ground; furthermore some bypass chip capacitors connected between each dc pin and ground. This board is not part of the actual circuit design, as it is a standard, ready to use, test setup to measure the power amplifier, hence no modifications of the PCB board can be undertaken. See figure 3.1 for an illustration.

3.2 On-Chip

The InGaP HBT4 process is modern and still mature since the chips are fabricated with the twentieth run. It consists of 15 masks, seven for the active devices (HBTs and diodes), six for the passive components and interconnects and two for the through wafer vias and the back side street. The substrate is GaAs with a relative dielectric constant of 12.9 and a thickness of $100 \mu\text{m} \pm 13 \mu\text{m}$. The layout is done in *Cadence*.

¹Part number is EN18D635001.

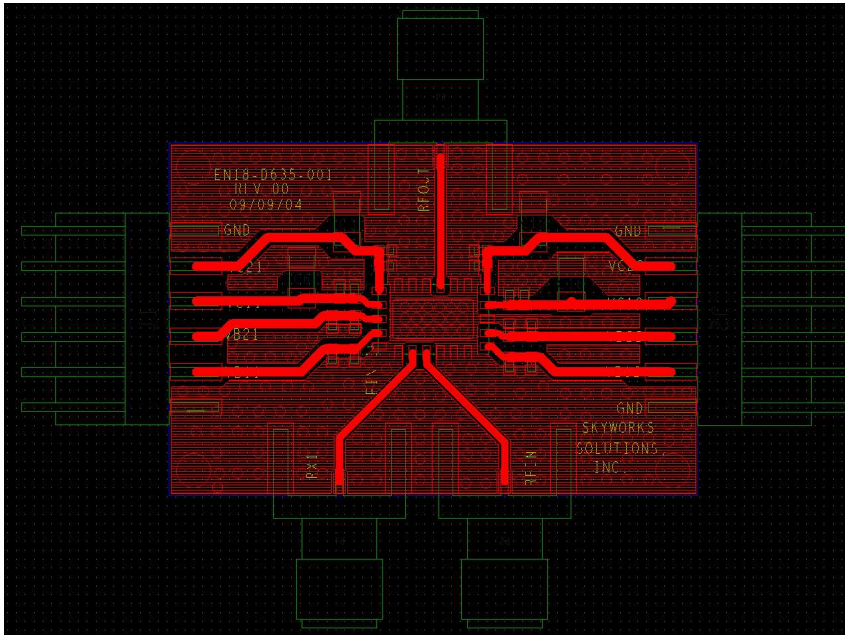


Figure 3.1: Layout view of the test board.

3.2.1 Hetero Bipolar Transistor (HBT)

InGaP HBTs are GaAs HBTs using an InGaP emitter rather than an AlGaAs emitter; they are NOT InP/InGaAs. The material properties of InGaP relative to GaAs improve several device characteristics such as better dc gain at low bias, lower $1/f$ -noise and a versus temperature more stable peak dc gain. Table 3.1 points out the difference of the materials between the implemented InGaP technology and the close related AlGaAs.

Table 3.1: Material configuration of AlGaAs and InGaP HBTs [37]

Layer	HBT technology	
	AlGaAs	InGaP
Contact	InGaAs	
Emitter	AlGaAs	InGaP
Base	C-doped P+ GaAs	
Collector	GaAs	
Substrate	GaAs	

Two epi materials are released for the HBT4 process: -401 is targeted to address the CDMA designs with improved thermal performance and higher

linearity requirements, and -423 is targeted to address the GSM designs with improved ruggedness². Ruggedness is determined by a combination of breakdown voltage and thermal stability for the transistors, see table 3.3 for a comparison. Per run, one of the two materials is used. Additionally, for both materials, the process provides two types of npn transistors, differing in the area. They are named q56re0 and q117re0 and their properties are listed in tables 3.2 (emitter area and maximum emitter current), 3.4 (transit frequency) and 3.5 (gain). The implemented³ transistors are the q56re0 with 423 material. Note the bold numbers referring to the in the design relevant figures.

Table 3.2: Emitter area and maximum current for the q56p0re and q117p0re HBT [34].

Parameter	q56p0re	q117p0re	Unit
Emitter	horse shoe ring emitter		
Area	58.5	120.1	μm
Max. emitter current (1)	14.625	30.025	mA
Max. emitter current (2)	26.325	54.045	mA

Table 3.3: Breakdown voltages for the q56p0re HBT at 25 °C [34].

Breakdown between	Condition		Voltage [V]
	Bias	Material	
Base – Collector	$I_C = 200 \text{ nA}$	423	26.9
		401	27.0
Base – Emitter	$J_E = 100 \text{ nA}/\mu\text{m}^2$	423	7.0
		401	9.3
Collector – Emitter	$J_C = 0 \text{ nA}/\mu\text{m}^2$ Open base	423	12.9
		401	14.8
	$J_C = 330 \text{ nA}/\mu\text{m}^2$	423	20.3
		401	16.9

To the current density in table 3.2 has to be said that the value in (1) is the recommended value which guarantees the required operation lifetime

²CDMA designs operate typically at class AB, consist of 96 HBTs for the last stage with 28 to 29 dBm output power. GSM designs have higher output power (34 to 36 dBm) and much lower linearity requirements, so the mode of operation is above class B.

³There was no actual choice since this was the only run at this time.

Table 3.4: HBT transit frequency f_T at $V_{CE} = 1.5$ V, $T = 27^\circ$ C [34]

Condition		Transit Frequency	
Material	I_{CE}	q56p0re	q117p0re
P423	$0.25 \text{ mA}/\mu\text{m}^2$	46.3 GHz	47.3 GHz
	$0.1 \text{ mA}/\mu\text{m}^2$	32.8 GHz	33.4 GHz
P401	$0.25 \text{ mA}/\mu\text{m}^2$	46.9 GHz	48.9 GHz
	$0.1 \text{ mA}/\mu\text{m}^2$	31.0 GHz	31.8 GHz

Table 3.5: HBT gain at $0.1 \text{ mA}/\mu\text{m}^2$, $V_{CE} = 1.5$ V, $T = 27^\circ$ C [34]

Condition		Gain	
Material	Frequency	q56p0re	q117p0re
P423	0.9 GHz	30.0 dB	31.4 dB
	1.9 GHz	26.8 dB	26.0 dB
	2.4 GHz	25.8 dB	23.3 dB
	5.8 GHz	17.1 dB	15.2 dB
P401	0.9 GHz	30.4 dB	31.7 dB
	1.9 GHz	27.2 dB	25.8 dB
	2.4 GHz	26.1 dB	23.2 dB
	5.8 GHz	18.2 dB	15.2 dB

whereas the value in (2) is rather for a “laboratory environment” and at peak currents. However, the maximum current during operation is not the limiting factor. Since compression occurs already at lower current levels for Class B, the transistors operate anyway below the boundaries depicted under (2).

A single q56p0re transistor is displayed in Fig. 3.2 whereas in Fig. 3.3 the same transistor in array configuration is showed. Notice that the base and collector connection is done by metal 1 (gray) while the emitter contact takes place on metal 2 (yellow). Beside collector, emitter and base contact there are two extra features of the device:

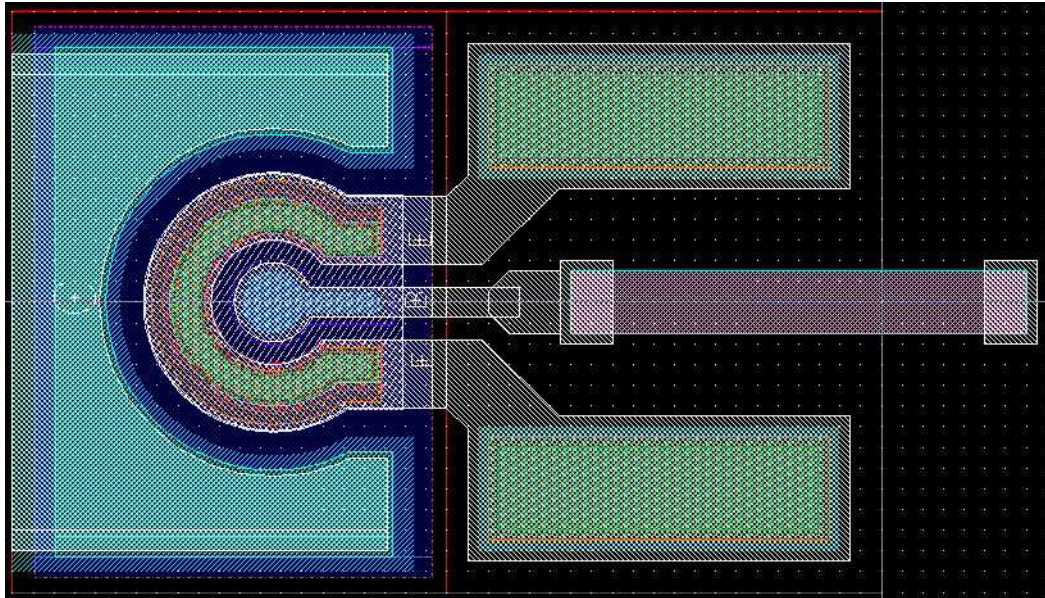


Figure 3.2: Layout view of a q56p0re horse shoe ring emitter HBT with collector, emitter and heat shunt, base and ballast resistor. Metal 2 is invisible.

Heat shunt

The two heat shunts to the emitter connected provide an extra thermal path to the substrate allowing a quick way to spread the heat from the device to other parts of the chip. They are not required, but highly recommended.

Ballast resistor

The ballastic (series) resistor at the base ensures thermal stability via a negative feedback. In case a transistor gets hot, it consumes more current,

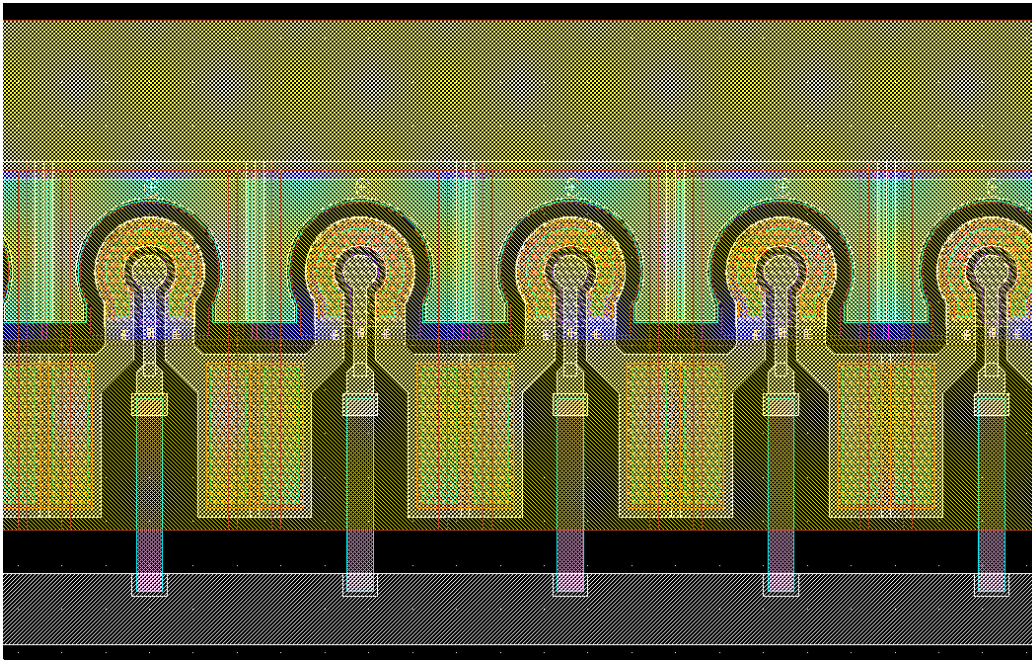


Figure 3.3: Detail layout view of an array of q56p0re HBTs. Metal 2 is yellow, metal 1 is gray.

the voltage over the resistor drops which lowers the bias point and therefore stabilizes the HBT array. By choosing the size of the resistance, gain is traded for stability. At each base $300\ \Omega$ are implemented which have to be specified in the HBT model and inserted in the layout of the HBT⁴.

Device reliability

[34] The nominal maximum rated junction temperature for active devices is $150\ ^\circ\text{C}$. The cell phone specification for reliability guidelines is T0.1% equals 10,000 hours⁵, i.e. the time to 0.1% cumulative failures. In conservative terms, T0.1% of the circuit is the same as the value for a single transistor, i.e. one transistor fails ... one circuit fails. To achieve this minimum operation lifetime, the transistor operation should not exceed the following conditions:

⁴Due to a “beginner” mistake (no LVS after the layout), no resistor was implemented. A second, metal change run, which is used for minor modifications after the first tests, allowed to fix the problem.

⁵This equals 1 year and 52 days of non-stop operation. Realistically, the device is in a stand-by mode or even switched off for a considerable amount of the operating life time. Moreover, a single broken transistor does not necessarily mean a malfunctioning circuit. Thus, this restriction is more conservative than it looks like at a first glance.

$T_j = 150$ C, $V_{ce} = 5.0$ V, and $J_e = 0.25$ mA/ μm^2 . This maximum emitter current density correlates with the maximum emitter currents specified in table 3.2.

Diodes

Alluded for completion, various diodes are available, mainly for ESD protection. No ESD protection is implemented in the design since it is already provided by the 0201 components.

3.2.2 Maximum current and voltage

[34] The maximum dc current limits for interconnect and resistor elements are summarized in table 3.6. Here the current flow direction is considered as in parallel to the element layer surfaces, and the current density is defined as the current flowing through the element divided by the width of the element. J_{fail} is the dc current density at which the element fails catastrophically, J_{lin} is defined as the maximum current density at which it starts to deviate from the linear IV relationship at about 10% and J_{estm} is the estimated, recommended safe current density.

Table 3.6: Maximum dc current densities

Device	J_{fail} (dc)	J_{lin} (dc)	J_{estm} (dc)	Units
Base	1.5	1.1	-	mA/ μm
Collector	7.5	6	1.5	mA/ μm
TaN Resistor	6	6	1.0	mA/ μm
Metal 1	90	70	3.0	mA/ μm
Metal 2	70	60	7.0	mA/ μm
TWV single	> 4	-	0.5	A
TWV double	> 4	-	0.8	A

Nothing is specified for the maximum ac current density, yet it sounds reasonable to take the root mean square value of the ac current and apply the limitation of the dc current density.

3.2.3 Metal layers

The process offers two gold metal layers with capacitance of 0.0195 fF/ μm^2 in between. See table 3.7 for the layer thickness, the sheet resistance and its

variation.

Table 3.7: Metal layer specifications

Parameter	M1	M2	Units
Thickness	1073	2000	nm
Sheet resistance	27.0	13.3	m Ω /sq
$\pm 4\sigma$ variation	7	4.6	%

3.2.4 Spiral inductors

There are two different spiral inductors available, namely solenoid and stacked M1/M2. Solenoid inductors have clear advantage over the stacked ones in terms of inductance area density. M1/M2 stacked inductors have a higher Q than the solenoid ones for the same inductance. Since quality is more critical than area, the stacked version is selected for implementation. The coil is defined by the *segment width*, the *space between segments*, the *number of turns* and the *xsize* and *ysize*. Low requirements to the inductance, the Q and the current density allow the design of very compact devices. Nevertheless, for high values, the device may cover a significant area of the die. See appendix B for simulated values of inductance, resistance and quality factor of the implemented stacked spiral inductors. Values of rather low quality factors are reported [31, 32, 33].

3.2.5 MIM capacitors

The capacitance of the metal-insulator-metal (MIM) capacitor [38] is calculated by the metal-nitride-metal capacitance, the fringing capacitance and the poly overlay capacitance (due to the connector on metal 2). There is no particular model that represents the MIM capacitor in a circuit simulation which would take into account frequency dependency or geometrical properties, since the behavior is, compared to the other devices, fairly ideal. The metal-nitride-metal capacitance is the main contributor to the total capacitance.

3.2.6 Thin film resistors

The resistors are made of a layer of Tantalum Nitride (TaN) with a sheet resistance of convenient 50 Ω /sq. The only on-chip resistors are the ballast

resistors at the base of the HBTs. Stabilization resistors are not done on-chip because of the lack of tuning capability. There is no particular model to represent nonidealities of the resistor during simulations of the circuit.

3.2.7 Through waver vias

The process contains a very low inductive, high conductive, through waver via connecting the circuit on the die to the back side metallization. The chip is mounted on a metal layer on the laminate which is connected to ground. For a common emitter design, this furnishes the designer with a high inductive path from the emitter to ground. Furthermore, shunt inductances and capacitances can be realized completely on-chip.

Table 3.8: Specifications for the Through Waver Via (TWV) [34]

Via type	Resistance	Inductance
Single	7.7 m Ω	16.8 pH
Double	4.6 m Ω	11.4 pH

The inductance of the double via is not half the value of the single value due to the mutual conductance. Two geographically separated single vias would result in half the inductance, though the parasitic inductance of the extra transmission lines would compensate for this countermeasure. The back side metal layer has a thickness of 5 μm and a sheet resistance of 9.4 m Ω /sq. The inductance of the M1 interconnect is at least comparable to or even larger than the TWV inductance.

3.2.8 Bond Pads, Transmission Lines

The bond pads have a low capacitance of 20 fF which is negligible. The wide transmission lines on the high power side are negligible in terms of inductance. The thin line going along the bases of the transistor array could be significant. Momentum analysis predict a difference of 80 nH between the last and the first transistor of the array which is a rather small value lying within the variation of the bondwires.

3.3 Off-chip

3.3.1 Laminate board

The laminate board with the dimensions of $5\text{ mm} \times 8\text{ mm}$ has four layers, the bottom layer being the ground layer and the top layer carrying the off-chip components. The layout on the laminate board is done on the software called *Cadence Advanced Package Designer (APD)*.

Since there is enough area on the laminate to layout the components of the circuit, some limitations are made that makes the design less susceptible to parasitics and simulation inaccuracies:

Components appear only on top metal layer Components are exclusively placed on the top metal layer. Components on lower layers would interfere with the electromagnetic field of the transmission lines on a higher level. A single model of the transmission line allows to describe the behavior and it can be verified by measurements of the implemented transmission lines in a test setup. Finally, only one type of vias is used, namely the big, through laminate via from the top to the bottom layer.

Attempt to avoid parasitics (think big) One could say the layout is not done very economically. Since there is enough space, area is “wasted” by adding very wide metal stripes where extra inductance should be avoided. Large amounts of vias are placed to lower the parasitic inductance and resistance. Placing a lot of metal and vias should eliminate the influence of the (0201) contact and via parasitics, reducing the possible source of mistakes due to component variations and nonidealities to as small as possible.

3.3.2 Bondwires

Wirebonding is a common interconnection for modern microwave devices because of the rather simple and reliable processes involved. At millimeter-wave frequencies, however, the bondwire parasitics are significant and consequently limit the external performance of packaged devices [17].

Bond wires are usually considered as incommensurate parasitic inductances which are best avoided by choosing minimum length, defined by the design rules, and by putting several wires in parallel. However, parallel bond wires cause two problems:

Whereas on the laminate, the extra area overhead is not significant, the extra bonding pads on chip consume a considerable amount of area. Moreover, the inductance is not lowered by the factor equal to the number of wires

in parallel. Due to the mutual inductance between the parallel devices, the total inductance results in somewhat less than the initial value. To determine the total inductance, not only the features of the individual bondwire have to be taken into account, but also angle and spacing between the bondwires, making it difficult to control and estimate the resulting total inductance.

Taking a closer look at the properties of a bondwire, one finds a high conductive inductor making it interesting to implement it as device, rather than consider it as a parasitic inductance. As extra benefits, it offers a very convenient way to tune the circuit and, since bondwires appear anyway in the design, no extra area is consumed. Several designs are reported that take advantage for the good properties of the bondwire inductance [15, 16, 17, 18, 19, 20, 21, 26, 27, 28, 29, 30]. Two imperative requirements follow thereafter, namely the inductance value of the bondwire has to be predictable and controllable:

- A model has to describe the bondwire with sufficient precision. This allows to determine the dimensions of the bondwire in order to accomplish the desired inductance.
- It should be possible to build the bondwire according to these dimensions by attaining pleasing accuracy and reproducibility.

Model at Skyworks

A simple mathematical analysis is proposed in [25] for the case, when the bondwire is electrically short compared to a wavelength, i.e. up to 40 GHz for bondwires of less than $0.7 \mu\text{m}$ in length, allowing to represent the bondwire as an inductance with a series resistance. An enhanced model developed at Skyworks Inc. reflects the comportment of the device to a pleasing degree⁶. In table 3.9 the accounted bondwire properties are listed and Fig. 3.4 illustrates the properties in the setup.

The model does not include the frequency which may surprise since a transmission line with a comparable length will doubtless show a frequency dependent inductance. As a dissent, a practically constant inductance up to 10 GHz for a gold wire with a length of 0.5 mm is shown in [15]. Since the model is used for the design of circuits working around 2 GHz and incorporating only the first couple of harmonics, the simplification seems to be reasonable.

⁶According to communications of designers at Skyworks Inc. who verified the model with measurements.

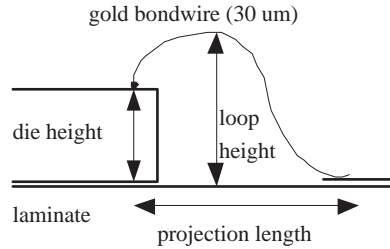


Figure 3.4: Setup of a bondwire connecting bond pads on the die and the laminate board.

Table 3.9: Accounted bondwire properties in the model and implemented values.

Property	Value
Material	Gold (Au)
Thickness	30 μm
Projection length (PLEN)	615 μm
Loop height	150 μm
Die height	100 μm

In Figs 3.5 and 3.6, the simulation results of a 30 μm diameter gold bondwire is disclosed. Choosing a projection length of 615 μm , an inductance of around 400 pH is achieved⁷. It can be seen in Fig. 3.6, that a change in the length of 10 % results in a change in the inductance of about 10 % to 20 %. A variation of the loop height of ± 25 μm around 150 μm (equals a variation of ± 30 %), results in a variation of the inductance of ± 7 %. This would lead to the conclusion that the inductance is less sensitive to variations of the loop height. Though, we are talking about handcrafted bondwires and the maximum precision is probably around ± 20 μm in length and height. Due to the parasitic inductance, it is favorable to be rather below than above a desired inductance level.

This leads to the in [26] proposed procedure:

- Bondwires can be used as part of the active circuit to reduce unwanted parasitics.
- Coarse tuning can be achieved by changing the (projection) length of the bondwire.

⁷The well known rule of thumb that 1 mm equals 1 nH seems to apply in this case.

- Fine tuning can be achieved by changing the shape (or loop height) of the bondwire.

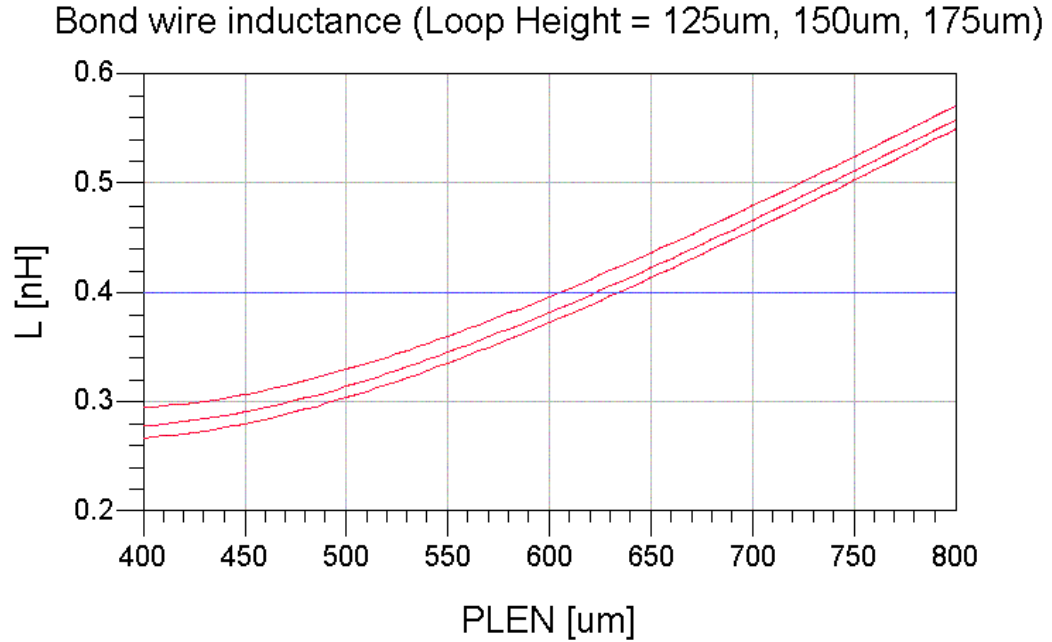


Figure 3.5: Simulated inductance of an Au bondwire, diameter $30 \mu\text{m}$, die height $100 \mu\text{m}$.

Inductances with bondwires in the order of half a nano henry are realizable, allowing frequencies at the harmonics with few pico farads which can be easily integrated. An LC series resonator, consisting of the on-chip capacitor, the bond-pad, the bondwire, the bondpad on the laminate and the via to ground, exhibits a very low series resistance and thus a very high Q (the parasitic capacitances of the bond pads are negligible as mentioned in subsection 3.2.8). Given an inductance of 0.4 nH , the capacitance values for the LC resonators at the fundamental and the harmonics are calculated with equation (3.1) and listed in table 3.10.

$$\frac{1}{\sqrt{LC}} = \omega \quad \longrightarrow \quad C = \frac{1}{L\omega^2} \quad (3.1)$$

Reproducibility

Means to improve the reproducibility of the desired inductance of the bond wire are:

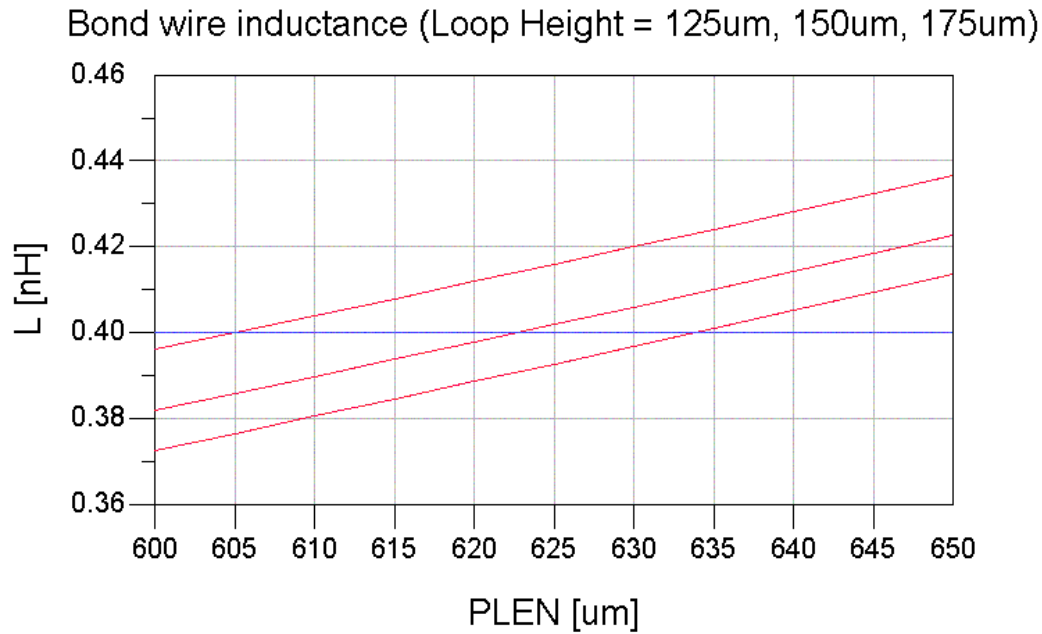


Figure 3.6: Simulated inductance of an Au bondwire, diameter 30 μm , die height 100 μm , detailed.

Table 3.10: Capacitance values for an LC resonator with $L = 0.4$ nH.

Frequency #	[GHZ]	Capacitance [pF]
f_0	1.8	19.545
f_2	3.6	4.886
f_3	5.4	2.172
f_4	7.2	1.222
f_5	9.0	0.782

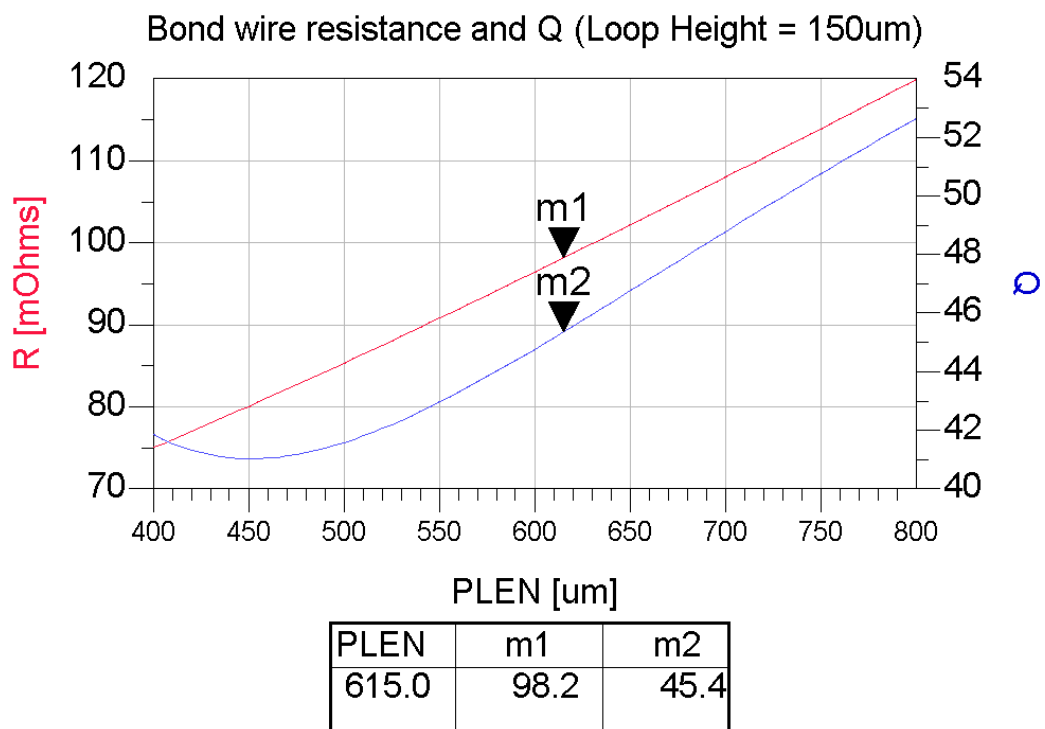


Figure 3.7: Simulated resistance (m1) and Q (m2) of a gold bondwire, diameter 30 μ m, die height 100 μ m.

- All bond wires have the same inductance, i.e.
 - same length
 - same loop height
- Bondwire is perpendicular to the die edge.
- “Cross-hair” metal stripes to ensure the precision of the length.
- Measurement setup for the prototype bondwire, so properties and reproducibility can be measured.
- One wire per line, i.e. no parallel wires, avoids problem of mutual inductance (which is difficult to simulate).
- Loop height is hard to control, though has limited impact on inductivity. The height ranges between 125 and 175 μm .
- Die alignment must (also) be precise and reproducible.
- Bond pad parasitic capacitance is 20 fF which is negligible.

3.3.3 Transmission lines

Transmission lines (TML) are the classical microwave components. Closed form equations and available computer models allow to predict the behavior at a high precision. The minimum width of the line is 60 μm . There are two ways to implement the TML in the design:

- TML as a filter when the dimensions are in the area of the wave length.
- TML as a high Q inductor where the length is much smaller than the wave length.

A quarter wave length at design frequency TML would perform a good short at even and a good open circuit at the odd frequencies which would make it the ideal harmonic termination circuit for power amplifiers. Nevertheless, the TML would not fit on the laminate so lumped components and therefore lumped components are used in the design to perform the filter structure.

For the minimum width of 60 μm , inductance values in the range of nano henries can be achieved with a high Q. A short TML with a width of at least 300 μm (width of the connector pads of the 0201 components) results in a fairly low inductance which can be considered as a negligible parasitic.

3.3.4 Spiral inductors

Compared to chip inductors or on-chip spiral inductors the conductance of a transmission line on the laminate is increased thanks to a larger width of the transmission line. Designing a spiral inductor cannot be done straight forward as it requires momentum analysis to determine the behavior of a particular device. Devices and transmission lines nearby the spiral impose an influence on the electromagnetic field and lower therefore the accuracy of the simulated values. The lower end of a reasonable achievable inductance is defined by the parasitic inductance of the transmission lines connecting to the spiral inductor. Realizable values are therefore rather in the area of tens of nano henries especially when the inductor covers multiple layers. The spiral behaves like an electrical short transmission line resulting in an increasing inductance over frequency. The good Q faces a high area consumption and a high complexity of the simulation.

3.3.5 0201 components

Various vendors provide chip capacitors, inductors and resistors in different package sizes. For the target technology, the smallest devices available have to be taken, i.e. the so called 0201 components with package dimensions $0.3 \text{ mm} \times 0.6 \text{ mm}$. Due to the parasitics of the package, these components exhibit strong nonidealities which have to be taken into account during the design process. In contrast to the other presented devices, 0201 components exhibit a resonance frequency, sometimes as low as the design frequency. The behavior of the device resembles only to the ideal one far below the resonance frequency. At or beyond, the behavior changes dramatically. There are two different ways to use the device:

- With the actual inductance or capacitance value, assuming the resonance frequency is very high.
- At the resonance frequency, neglecting the actual value of inductance or impedance.

Since there are only small inductance and capacitance values available, dc chokes and blocks are realized with elements operating at the resonance frequency. An inductance behaves like an open circuit and a capacitor performs a short circuit. The 0201-devices of Johanson for 33 nH and 33 pF have their resonance frequency at 1.8 GHz. Above or few below the resonance frequency, the blocking capacitor acts as a band pass, resulting in additional filtering in the signal path.

A design rule defines the minimum spacing of the two 0201 components as 150 μm . Having several components in parallel, the parasitic inductance of the transmission line becomes significant which has to be taken into account by incorporating a large amount of devices.

The device variation becomes an issue for small components, since the lower the value of the inductance or capacitance, the harder it becomes to fabricate the value precisely. Furthermore, parasitics and some of the variations are independent of the value of the component, making small components even more prone to imprecision.

Johanson [44] supplies the designer with good chip inductors and capacitors, a broad palette of available values, and a good software library to simulate the devices. Chip resistors are provided by Murata [45].

Chip capacitors Chip capacitors are available in the range between 0.3 pF and 33 pF. The series conductance is rather high. For larger capacitance values, the resonance frequency comes into the area of the design frequency. To lower the impact of the limited conductance and guarantee a higher quality factor as it is required for the output L network with the shunt capacitance, two devices with half the capacitance can be connected in parallel. This offers even better filtering characteristics at higher harmonics, since the resonance frequency is shifted to a higher frequency.

Chip inductors Chip inductors are available from 1 nH to 33 nH. The series conductance is rather low compared to the capacitor. To increase it, again, several devices can be put in parallel. In contrast to the parallel connected capacitors, higher inductance values have to be chosen, which lowers the resonance frequency.

Chip resistors Chip resistors are used to stabilize the amplifier. They are assumed to be fairly linear and ideal.

3.3.6 Vias

Various kinds of vias are available. Since there is simply the connection from the top layer to the bottom layer required, only one type of via is implemented. It is the one that has the lowest parasitics and consumes the most area. The parasitics of the via are subsequently neglected and on all layouts, including the test measurement setup, the via is considered as a perfect ground connection.

3.4 Evaluation

The problem group are truly the inductors. Either they appear as non-avoidable parasitics or they exhibit a very nonideal behavior. The available capacitors and resistors show fairly good characteristics. The 0201 components offer flexibility for tuning but contain high parasitics and only limited values are available.

3.4.1 Comparison inductors

On-chip spiral inductors have a rather low Q and the size depends on the current. This makes them suitable for the matching on the input side due to the very low area overhead. Although, on the output side, the low Q would greatly reduce the efficiency of the amplifier and the high current densities would require huge elements.

Bondwires have a good Q and can be used for tuning [26]. Available inductance values range in between 0.1 nH to 1nH and are limited by the minimum and maximum bondwire length.

On-laminate transmission lines are very good representable by models, have a good Q and are rather small. Values lie in the lower nano henries.

On-laminate spiral inductors exhibit a good Q but require large area and the modeling is rather complex.

0201 chip inductors are very lossy. They can be suitable for dc chokes when used at the resonance frequency. The collector dc current however can reach 1 A and more which exceeds the (dc) current rating of the component by factors.

3.4.2 Comparison capacitors

- 0201 capacitors are good for dc blocks in the signal path since they allow free additional filtering of the signal.
- On-chip capacitors are superior because every wanted value in the range from below 1pF and to above 100pF, delimited by the area on-chip, is available, whereas the behavior is practically ideal, compared to the

chip capacitors. Furthermore, the variation of the on-chip capacitance is very low.

3.4.3 Comparison resistors

- On-chip resistors are very small, precise, have low parasitics but do not allow any flexibility in terms of tuning.
- 0201 resistors in comparison, exhibit parasitics and comparatively large, but allow an easy way of tuning.

3.4.4 Conclusions

At the design frequency, it lends itself to use the parasitic inductances as the actual inductors of the intended circuit. Implemented values should be in the range above 0.5 nH, resp. pF, and below 10 nH, resp. pF. The maximum value may be exceeded by dc blocks, dc chokes or on-chip bypass capacitors.

Building the input matching and the biasing circuit at the input side, a combination of bondwires, 0201 dc blocks and chokes, and on-chip capacitors and inductors will result in an optimum in flexibility, area overhead, and performance.

For the harmonic shorts at the output, series-LC shunts can be built by on-chip capacitor – bondwire combinations. Transmission lines off-chip and 0201 capacitors form together an L network in order to transform the resistance to the desired 50 Ω . The highest realizable short is at the fifth harmonic which is at 9 GHz.

Chapter 4

Implementation

Based on the knowledge of the target technology and the theory of the power amplifier, it is now possible to introduce the implemented circuits. There are several levels of abstraction, starting with a schematic and ending with the final layout of the integrated circuit and the laminate board.

4.1 Design strategy

Usually, designs for commercial products are based on preceding versions built in the same technology, i.e. the process and the design flow become more mature with every iteration. As an outsider, it is a difficult task to acquire all the needed information concerning the technology and its specialties in order to end up “first time right”. Hence, to establish a design flow is like putting the pieces of a puzzle together. Some traps are specifically related to this particular process and can only be avoided by learning from experience of other designers, respectively their habits¹. Subsequently, the design strategy is listed point for point. Obviously, there was a lot of back and forth in this flow.

- Investigate the behavior of the transistor, determine the bias point.
- Start the design with a single transistor.
- Chose the output filter structure.
- Design a simple input bias network.

¹Engineers in the industry do sometimes things in a particular way because they know it works, without worrying about not being aware of the “why” or “how”, respectively why this way is superior to a possible alternative. Never touch a working system! This is the fundamental difference between research and industry.

- Calculate the ideal load and source impedance according to the literature.
- Optimize the impedances with load and source pull iterations.
- According to the simulation results, scale the design to achieve sufficient performance.
- Again, do iterations of load and source pull.
- Replace ideal by real components.
- Determine stability resistors.
- Do the layout of the chip and the board.

4.2 The active device

As mentioned earlier, the transistor leaves only few degrees of freedom in the design, namely the size of the ballast resistor and the number of devices in parallel. The bias point for maximum linearity is solely defined by the transistor (given a specific power supply voltage).

4.2.1 Ballast resistor

A ballast resistor is inserted at the base for each transistor to avoid the thermal runaway[14]. For the produced integrated circuits, a resistor of $300\ \Omega$ is chosen. During the attempt to measure the circuit, the transistor drew a huge amount of current when the bias voltage is increased to 1.28 V or above ($V_{dd} = 4\ \text{V}$). The reason was simply because the ballast resistor was chosen too low, respectively the power supply voltage too high. Fig. 4.1 shows a dc simulation I_{ce} versus V_{be} of the (88) transistor array with a ballast resistor of $300\ \Omega$. The simulation is done by forcing a base current, applying different power supply voltages and measuring the base voltage. For the case of $V_{dd} = 4\ \text{V}$ and $V_{be} = 1.28\ \text{V}$, the function shows two possible solutions for the current, explaining the sudden jump after a small change of the base voltage. For the target power supply voltage of 4 V, a ballast resistor of $900\ \Omega$ would have been required as can be seen in Fig. 4.2. An adequate power supply voltage for a ballast resistor of $300\ \Omega$ is 2 V, being the flattest curve in Fig. 4.1. Since the slope is lowered, stability and linearity is traded for gain.

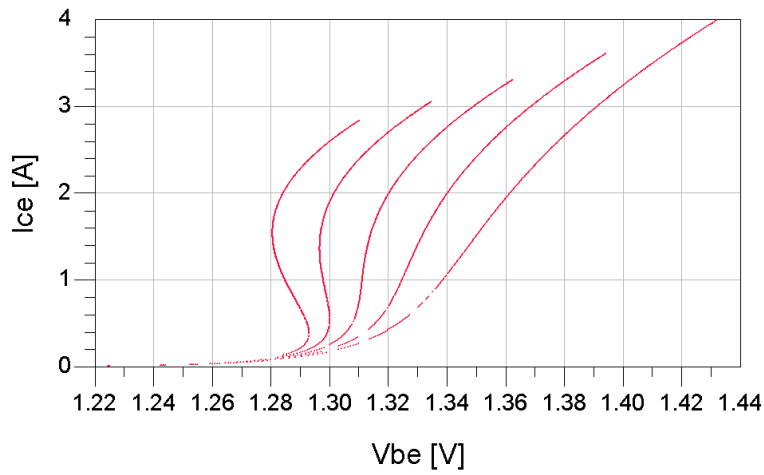


Figure 4.1: I_{ce} versus V_{be} of 88 HBTs in parallel with V_{dd} from 4 V to 2 V (step size 0.5 V) at $R_b = 300 \Omega$.

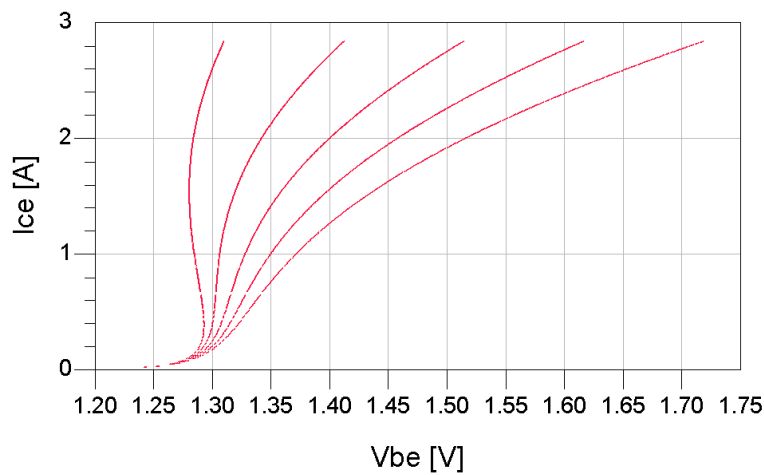


Figure 4.2: I_{ce} versus V_{be} of 88 HBTs in parallel with R_b from 300Ω to 900Ω (step size 150Ω) at $V_{dd} = 4$ V.

4.2.2 Bias point

As stated earlier in this thesis, the Class B operation is defined by biasing the active device at the cut off voltage, resulting in a conduction angle of exactly π . Due to the exponential voltage current relationship of the HBT, this definition does not really lead to a concrete voltage (see Fig. 4.3 for a plot of I_{ce} versus V_{be}).

Based on linearity of odd part of the transfer function

A more practical, real world approach for a Class B PA design with a pHEMT is proposed in [12, 13]. Class B operation is usually realized in a (differential) push-pull configuration which cancels out the even harmonic components. For a narrow bandwidth PA as proposed in this thesis, this can be achieved by shorting the even order components to ground with an output filter, making the two setups equivalent for this consideration.

No significant even order terms will appear at the output, making the odd terms the main contributor to nonlinearity. As showed earlier with the Fourier component decomposition of the collector current, the magnitude of the odd order terms is highly sensitive to the bias point, showing a minimum at ideal Class B operation and making it therefore reasonable to chose the bias point at the point of maximum linearity somewhere above cut off towards Class AB.

The procedure is illustrated in Fig. 4.4 with $f(x)$ being the transfer function of the transistor. $f(x)$ is decomposed into its even and odd part.

$$f(x) = f_e(x) + f_o(x) \quad (4.1)$$

$$f_e(x) = f_e(-x) \rightarrow f_e(x) = \frac{1}{2}(f(x) + f(-x)) \quad (4.2)$$

$$f_o(x) = -f_o(-x) \rightarrow f_o(x) = \frac{1}{2}(f(x) - f(-x)) \quad (4.3)$$

Choosing the bias voltage too low (Class C) or too high (Class AB) results in a non continuous gradient of the odd part of the transfer function around the bias point, whereas for Class B operation the same curve is ideally linear.

In the left part of Fig. 4.5 the base voltage to collector current transfer function of a single HBT is plotted for different bias voltages. On the second plot, the odd function is showed. The bias voltage is varied from 1.20 V to 1.50 V with a step of 0.05 V. The interpretation is exactly the same as for Fig. 4.4. The bias point of the blue curve is too low for Class B, the bias point for the black curve is too high, whereas the turquoise curve with a bias

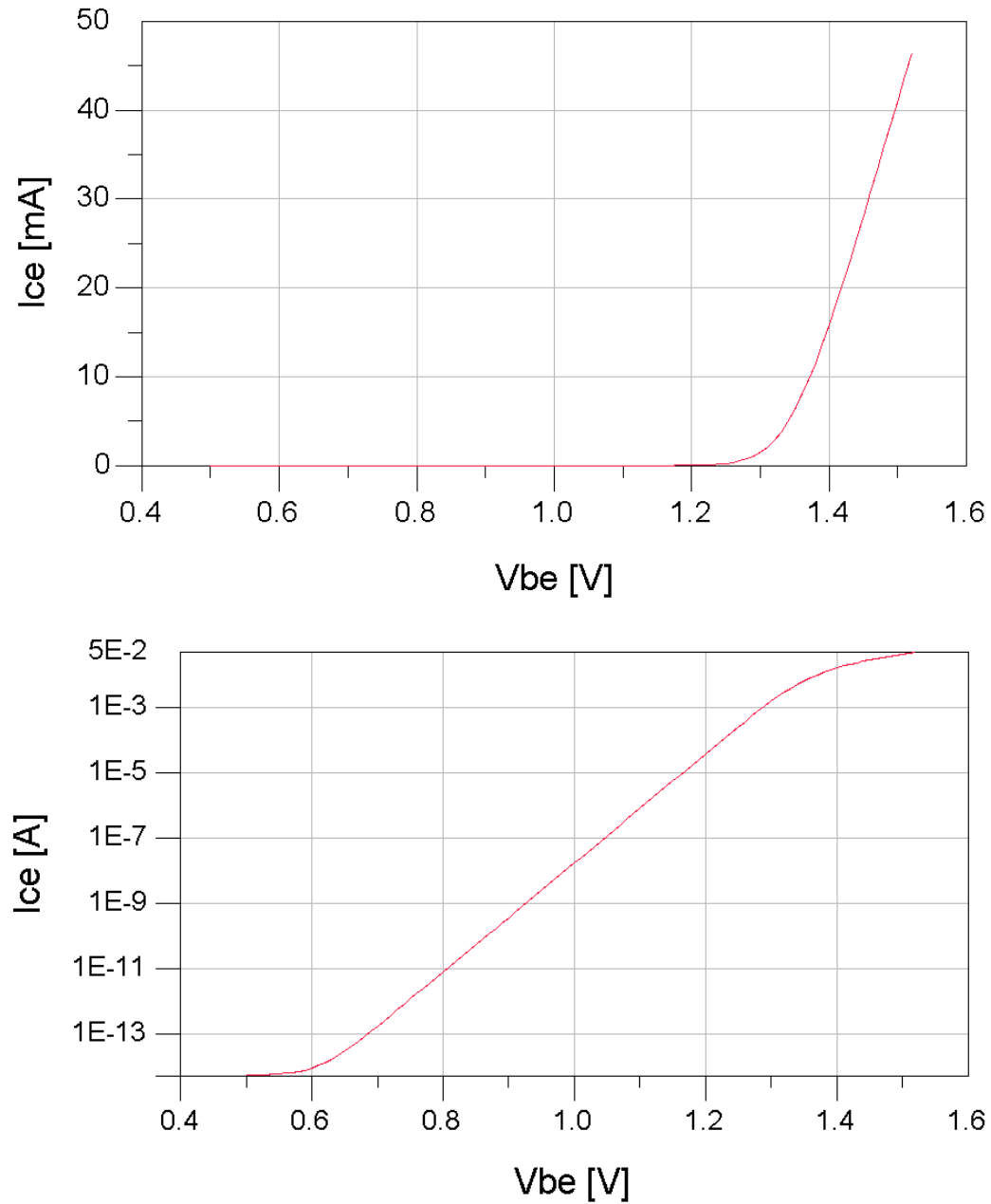


Figure 4.3: Linear and log plot of I_{ce} versus V_{be} of a single HBT ($V_{dd} = 2$ V).

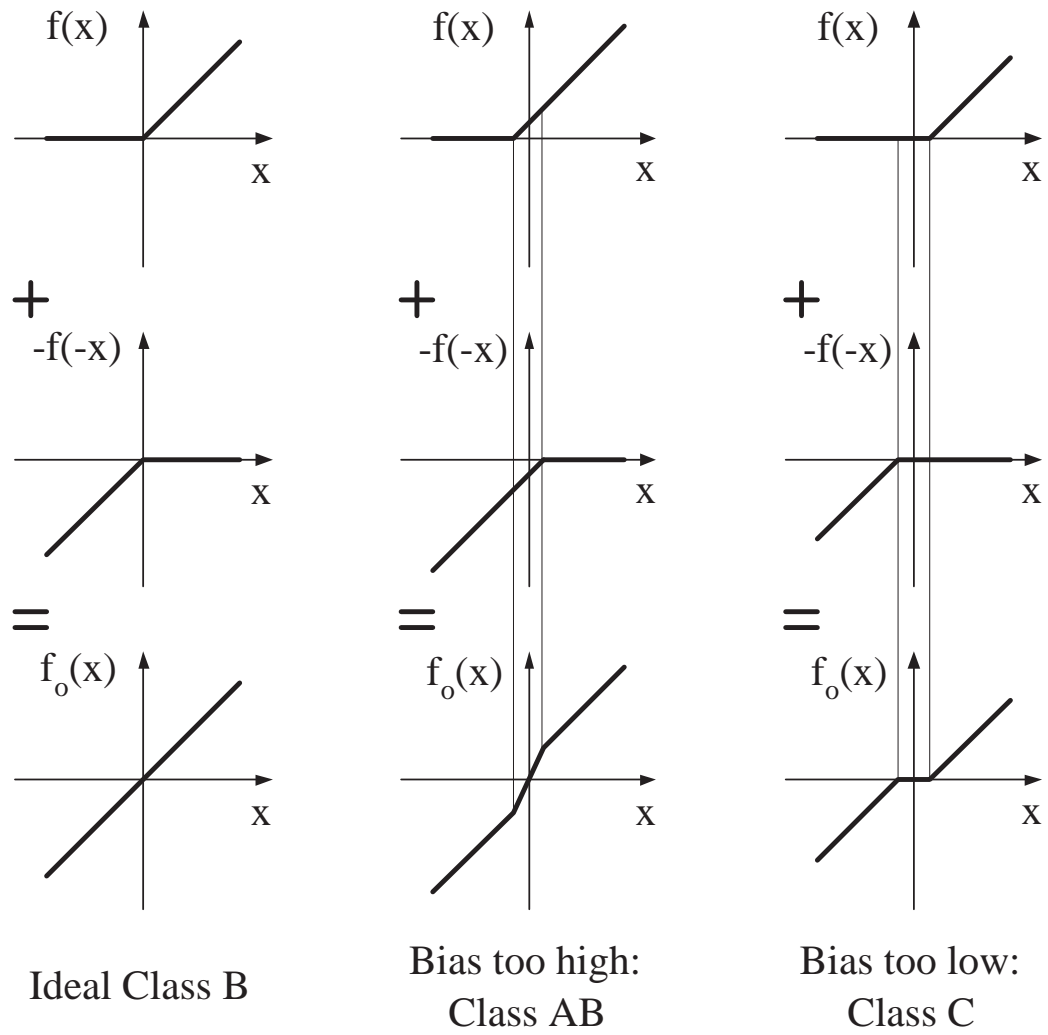


Figure 4.4: Determining the Class B bias point via the odd component of the transfer function.

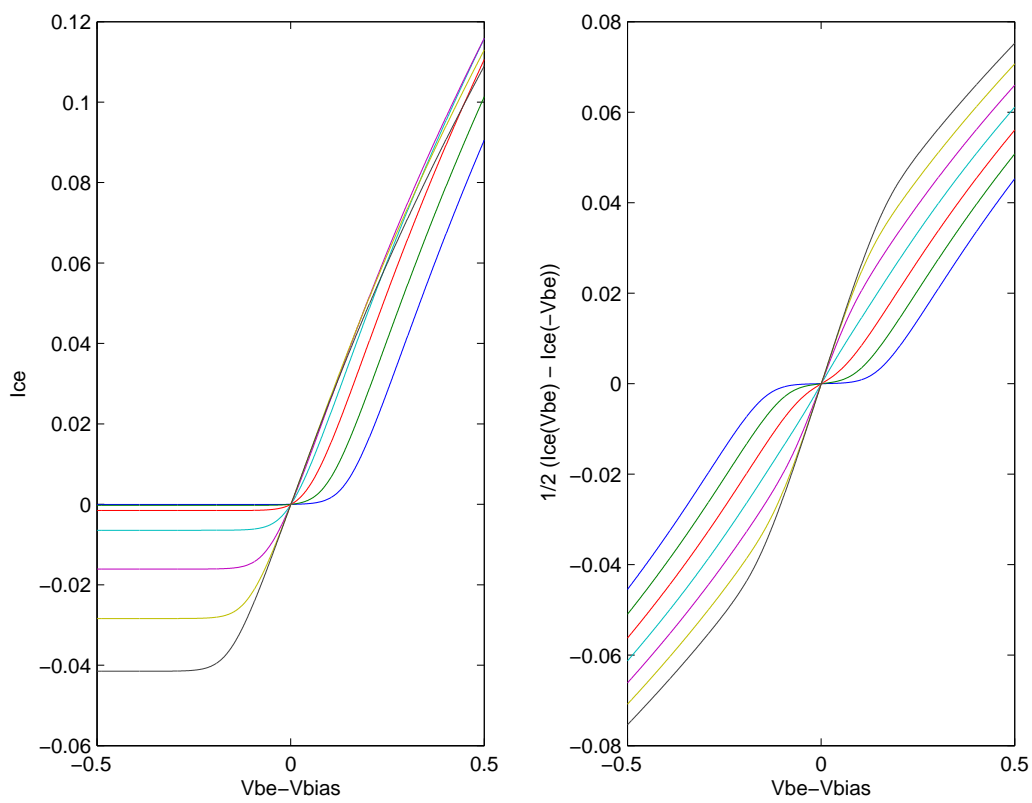


Figure 4.5: Voltage current transfer function and its odd part for 1.20 V to 1.50 V (step 0.05 V) bias voltage, $V_{dd} = 2$ V, $R_b = 300$ Ω .

voltage of 1.35 V shows best linearity. Taking a closer look at the function (sweep from 1.32 V to 1.36 V) as showed in Fig. 4.6 and plotting the second derivative of the odd part, the red curve with a bias voltage of 1.34 shows the best linearity (second derivative has smallest deviation from zero). The dc current for a such a high bias voltage at zero input power is not negligible for it is around a third of the dc current at maximum power level. However, this is definitely *not* the a Class A bias point! Comparing the behavior of the turquoise and the black curve of the *total* transfer function around the bias point (left graph in Fig. 4.4) makes it obvious that the black curve is more linear, being very close to Class A.

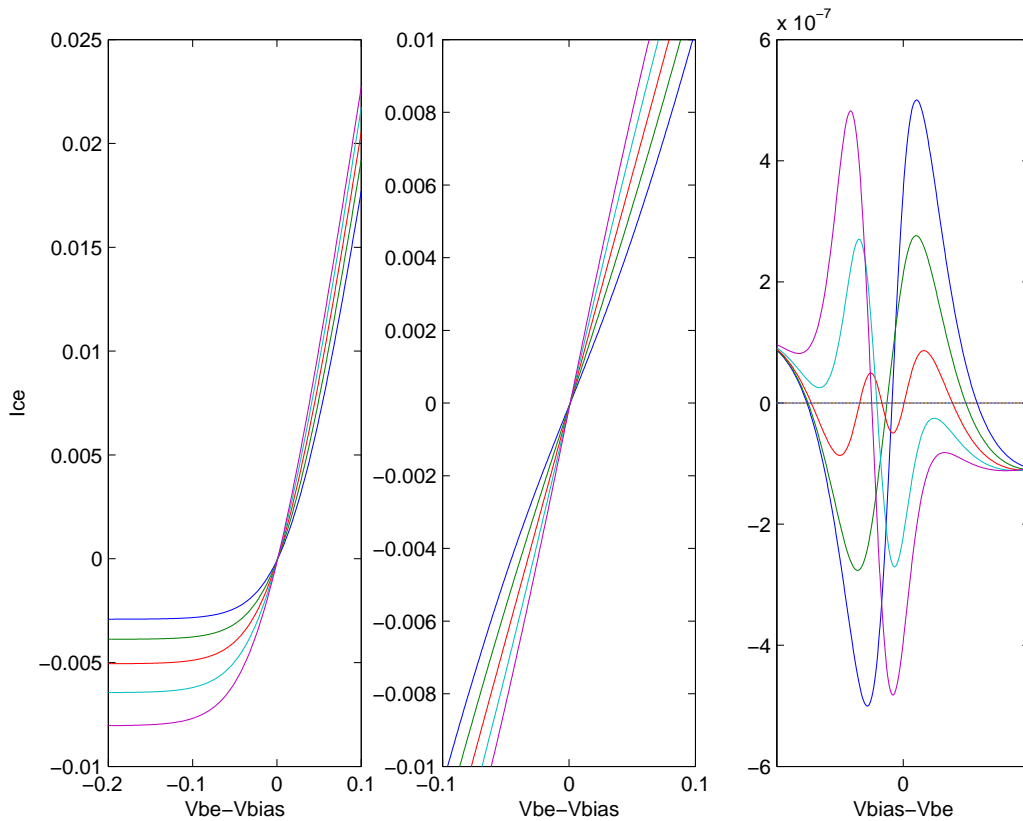


Figure 4.6: Detailed view of the voltage current transfer function, its odd part and the second derivative thereof for 1.32 V to 1.36 V (step 0.01 V) bias voltage, $V_{dd} = 2$ V, $R_b = 300 \Omega$.

The bias voltage is hence exclusively determined by the behavior of the transistor and is independent of the number of transistors in parallel or the architecture of the amplifier, so the same voltage can be used for the CC and CE structure. Notice that the ballastic resistor, considered as a part of the

transistor, has a large influence on the linearity! However, the analysis for the same HBT at $V_{dd} = 4$ V delivers about the same bias voltage for Class B (1.32 V).

Based on linearity of a sweep over power

The amplifier is simulated over a range of input power levels (-5 dBm to 20 dBm) and bias voltages (1.28 V to 1.36 V) as showed in Fig. 4.7. For a low bias voltage, the amplifier exhibits initially expansion, followed by a maximum of gain and finally compression, as it is typical for Class C. By increasing the bias voltage, a point can be found, where the gain over power stays constant up to a point where compression occurs (the middle curve in Fig. 4.7). Increasing the bias voltage further increases the gain but also decreases the compression point, i.e. compression occurs earlier. This bias point for maximum linearity is 1.32 V for $R_b = 300 \Omega$ and $V_{dd} = 4$ V as can be seen in the plot of the derivation of the gain. As stated before, is independent of the number of transistors in parallel or the amplifier architecture.

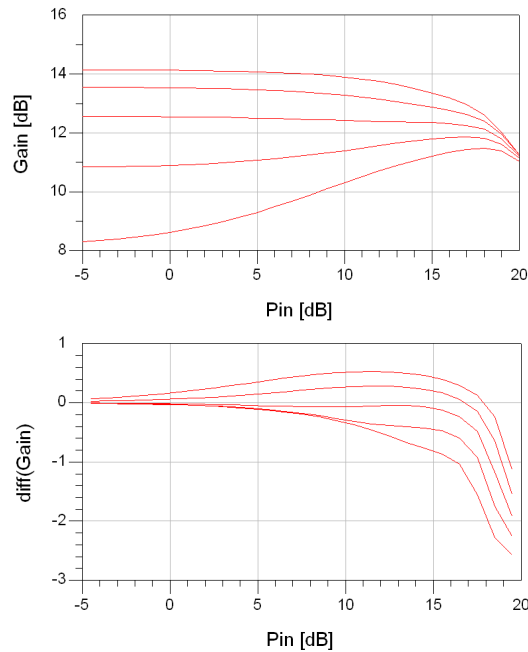


Figure 4.7: Sweep over input power and at various bias voltages (1.28 V to 1.36 V) at $R_b = 300 \Omega$ and $V_{dd} = 4$ V.

Unfortunately, due to the exponential behavior of the HBT, this bias point is rather high. For zero input signal, about half the dc current for

full power operation is flowing, making it necessary to lower the bias voltage during the stand-by mode. With a multi stage amplifier the signal can be predistorted in a previous stage to compensate for the expansion of the last stage. As a result, the bias voltage can be chosen at around 1.25 V.

4.2.3 Scaling of the design

A first design approach is done with a single transistor to get a feeling for the interrelation between load impedance, maximum current and linearity. How many transistors are now necessary to achieve 1 Watt output power? To answer this questions, the trade offs between the number of transistors in parallel and the performance have to be considered.

Current and power Increasing the number of transistors allows a higher maximum current and due to the constant power supply voltage in an increased overall output power. The maximum current is defined by the length of the operation life time.

Linearity Since the transistor starts to clip at high signal levels, an increased number of transistors pushes the point of compression to a higher power.

Impedance level However, as the number of transistor increases, the impedance level is lowered accordingly, which in turn makes it harder to fulfill the requirements of the quality factors of the matching network and the harmonic shorts. As soon as the series resistances of the shorts come into the same order of magnitude of the impedance level of the transistors, areas of alternating expansion and compression arise over a large range of input power which destroys the whole linearity.

In the industry, the number of transistors is given by the required operation life time for a given power level. For this thesis, initially a number of 88 transistors in parallel is chosen and CC and a CE design is realized. Since there were three dies available, another amplifier, designed for the same output power but containing only 44 transistors, is implemented, exceeding the mentioned current limits and could therefore not find application in a commercial product.

4.3 The passive network

The design of the passive network is the main concern of the design. Describing the signal flow at various frequencies gives a first idea of how the circuit is going to look like. In Fig. 4.8, each of the six schematics show an HBT embedded in a circuit including two signal ports, a bias voltage source and a power supply. The schematics represent the power amplifier for the dc case (a and d), the fundamental frequency (b and e) and the evenharmonics (c and f) in each, a common collector and a common emitter amplifier architecture. The signal flow for each of the cases is highlighted by a bold line. Fig. 4.9 shows the combination of the three circuits in a single one. Let us point out some interesting details how the combination can be done without interference:

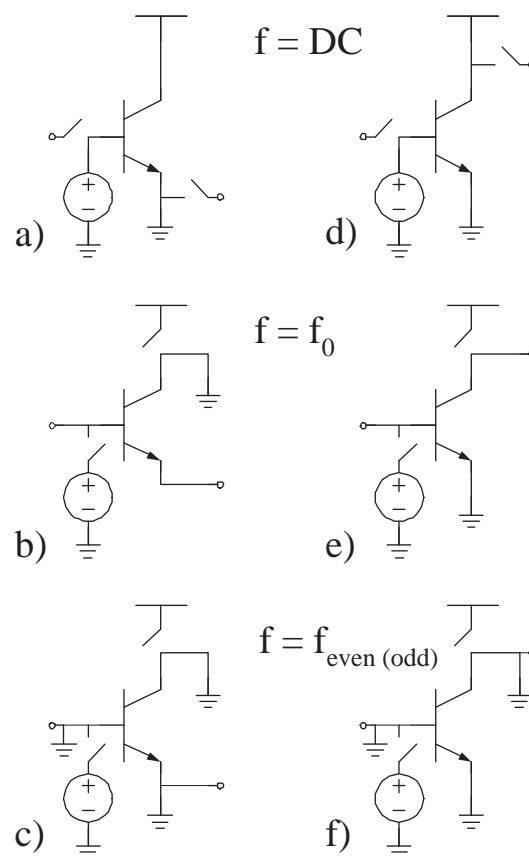


Figure 4.8: CC (a,b,c) and CE (d,e,f) PA schematic for dc, fundamental and even harmonics.

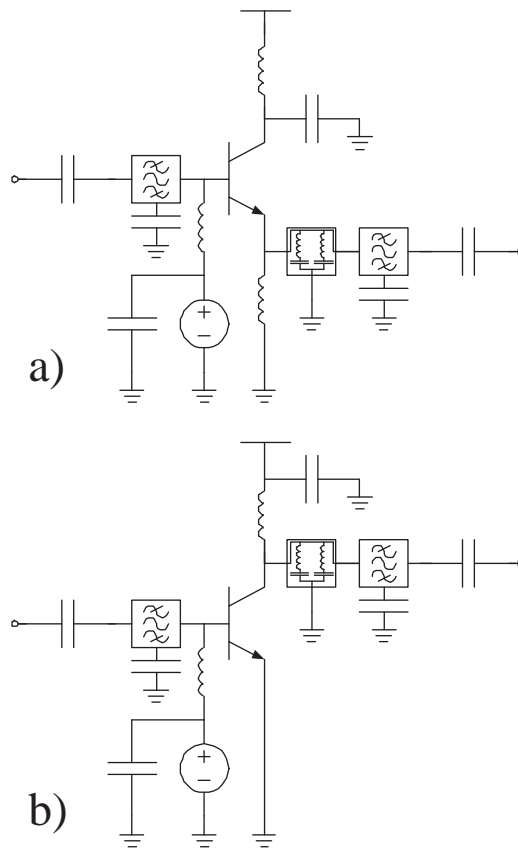


Figure 4.9: The twice three schematics from figure 4.8 realized in a CC (a) and CE (b) design.

dc paths There is a dc current flowing between the power supply and ground and the bias voltage source and ground, respectively. There is no ac connections of these ports allowed to the circuit. As a consequence, apparent ac components from these ports have to be grounded by bypass capacitance, respectively choked by a large inductance. Furthermore, there is no dc connection from the amplifier ports to the active device, imposing the requirement of a dc block.

Signal path The RF signal, carried at the fundamental frequency, flows from the input port to the base and from the grounded collector (emitter) through the transistor to the output port. No signal is allowed to pass the ports other than at the design frequency, making a band pass filter necessary. Mind the out of band components produced in the transistor and reflected at the output propagating to and fro and causing the amplifier to ring for the case of a bilateral transistor.

Harmonic path The harmonics add up together with the fundamental component to a distinct voltage and current wave form. Therefore, the even harmonic components of the current have to go through the collector-emitter channel from ground to ground. As a consequence, harmonic shorts are required at the output side at the emitter (CC), respectively at the collector (CE).

CC vs. CE Notice the difference between the two amplifier architectures regarding the common port of the transistor: Whereas for the CE, the emitter is in all three cases (d, e and f) of Fig. 4.8 connected to ground, the collector does not have the same potential for ac and dc, making the design more complicated.

4.3.1 Output network

In the preceding section, four blocks were identified being part of the output network:

- A (choke) inductance.
- A block performing harmonic termination.
- A block filtering the signal and transforming the resistance level.
- A blocking capacitor.

The harmonic termination block has to be before the impedance transformation – filtering block because otherwise, the harmonics would not find a low impedance path through the filter but rather would be reflected. An impedance transformation prior to filtering and harmonic termination would be beneficial since the requirement to the high Q of the various filters would be less stringent.

The tasks of the output network for a class B amplifier are to

1. ... provide a short for the dc current.
2. ... provide a short to ground for even harmonics.
3. ... hinder the odd harmonics to occur at the output load resistance.
4. ... hinder at the load reflected parts of the output signal to occur at the output of the transistor.
5. ... provide the transistor with a particular load impedance at the fundamental.
6. ... transform the load impedance to the output load resistance ($50\ \Omega$).

The classic way to fulfill these requirements in microwave technology is to use a quarter wave length shunt transmission line to perform the shorts at even harmonics and another transmission line to perform matching and filtering at the output. Unfortunately, this is not an option for the target technology and design frequency, hence, only a limited amount of harmonics can be incorporated into the design.

Output matching and filtering

The easiest way to perform an impedance transformation is by using an L network as shown in Fig. 4.10. By choosing a low pass structure with a series inductance and a shunt capacitance, the odd harmonics will not appear at the output resistance. This accomplishes points 3, 5 and 6. Furthermore, the blocking capacitor is connected at the high impedance side of the L network, reducing the impact of the resistive losses in the capacitor. The series L in this structure is the most critical in the design to efficiency, since its series resistance degrades directly the efficiency of the amplifier.

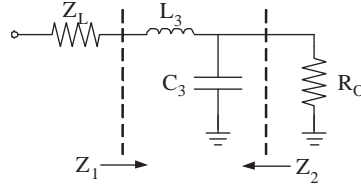


Figure 4.10: Matching L network in low pass configuration for impedance transformation.

Harmonic termination

Various LC combinations allow the desired function, depending of the required amount of shorts that have to be implemented. Let us take for an example a series LC network as showed in Fig. 4.11.

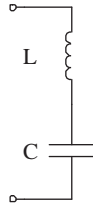


Figure 4.11: A series LC network

The transfer function of the LC network is represented in the complex impedance manifesting between the two clamps as listed in equation (4.4), respectively (4.5) for the admittance. Solving this impedance for zero results in the frequency at which this structure has its maximum conductivity, say a short circuit. Solving the admittance for zero, the frequency for a maximum resistivity, i.e. an open circuit, is discovered. The zero for an admittance is a pole for the impedance. The zero (short circuit) and pole (open circuit) for the examined structure is listed in equations (4.6) and (4.7). Notice that for a more complex structure several poles and zeros will appear.

$$Z = \frac{1 - \omega^2 LC}{j\omega C} \quad (4.4)$$

$$Y = \frac{j\omega C}{1 - \omega^2 LC} \quad (4.5)$$

$$Z = 0 \rightarrow z_1 = \frac{1}{\sqrt{LC}} \quad (4.6)$$

$$Y = 0 \rightarrow p_1 = 0 \quad (4.7)$$

The lumped components of the target technology become very unpredictable above 10 GHz, so the fifth harmonic is the highest possible to be implemented. Adhering this, the required poles and zeros for the targeted circuit are listed in the equations below. There should be an open circuit at the design frequency and three shorts, at dc and the first two even (odd) harmonics.

$$z_1 \quad @ \quad \text{dc} \quad (4.8)$$

$$p_1 \quad @ \quad f_0 = 1.8 \text{ GHz} \quad (4.9)$$

$$z_2 \quad @ \quad f_2 = 3.6 \text{ GHz} \quad (4.10)$$

$$z_3 \quad @ \quad f_4 = 7.2 \text{ GHz} \quad (4.11)$$

A profound examination of LC networks has been done and is presented in appendix C. Two valuable observations are made that are valid for LC with shunt and series inductances and capacitances which is stated here without proof²:

1. The frequency at which a zero (short) occurs depends only on the devices connected in series to the short.
2. The frequency at which a pole (open) occurs can be controlled by an extra parallel device without affecting the frequencies of the zeros.

This leads straight to the structure in Fig. 4.12. Two series LC structures perform each a short at a desired frequency and an extra shunt inductance adds a zero at dc. Besides the three zeros, this structures contains two poles. Fortunately³, one of the poles will be below the frequency of the two (ac) zeros, resulting in a zero-pole-zero-pole-zero pattern. According to observation 1, the frequencies of the shorts depend only on the individual series LC resonator. The extra parallel inductance has now a double function, performing the one of a dc choke but also, as stated above in observation 2, allows to tune the first pole towards the fundamental frequency, once the values for the two harmonic shorts are determined. The second pole, named a “parasitic” pole, will then land somewhere between the two RF shorts, preferably not right at the third harmonic.

²The two statements can easily be verified by examining the figures and equations in the appendix, chapter C.

³This is another reason why this structure was preferred to some other compositions of presumable interest.

The symbolical calculation of the two poles is done with Mathematica as it results in a mere complex term. See below the plot of the dependence of the two poles to L_0 , given the values of the two LC resonators.

$$z_1 = 0 \quad (4.12)$$

$$p_1 = f_1(L_0) \quad (4.13)$$

$$z_2 = \frac{1}{\sqrt{L_1 C_1}} \quad (4.14)$$

$$p_2 = f_2(L_1) \quad (4.15)$$

$$z_3 = \frac{1}{\sqrt{L_2 C_2}} \quad (4.16)$$

$$(4.17)$$

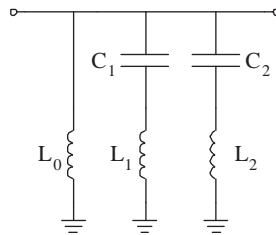


Figure 4.12: Network performing the harmonic termination.

This structure has another benefit: Since the output network has to make advantage of the off-chip inductances like short transmission lines exhibiting a better Q, there will be a series inductance due to the bondwire in every line attached to the output pin of the transistor. These bondwires can contribute to all of the inductances in the output network including the matching L.

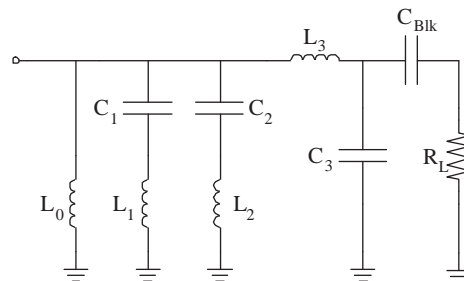


Figure 4.13: The complete output network.

4.3.2 Stabilization resistance

An unstable amplifier can be stabilized by inserting resistance into the input and/or output network. The loss caused by the resistance lowers the gain, so the fed back signal is not high enough anymore to let the amplifier ring. Components causing ringing out of band can be filtered out with lossy reactive devices performing an open at the design frequency and a resistive path to ground at the problematic frequency. Yet for ringing in band, there is no sophisticated approach known other than adding losses.

Adding the resistance at the output reduces the efficiency whereas adding it at the input, only the gain is affected. Therefore, stabilization in power amplifier design is done at the input. Since losses are inserted, the use of low Q components for matching and filtering at the input is possible.

4.3.3 Input network

The input network is kept rather simple, i.e. no sophisticated input filter is implemented. Even without this filter, the design of the input network turns out to be quite tricky. The inductors of the input match are realized by combinations of bondwires and on-chip spiral inductors. See in appendix B for the simulation results of the implemented spiral inductors. In table 4.2 and 4.4 the values for the capacitors and inductors of the input matching network are listed. Furthermore, in table 4.1 the input impedance to which the input network is transforming the 50Ω is listed.

For all designs, a shunt inductance at the bias is necessary for the biasing of the transistor. In the CC design (see Fig. 4.14), it was possible to include this inductance into the matching network consisting of a series and a shunt inductance, realized by each a bondwire and an on-chip spiral inductor. Stabilization resistors are added in the signal path (R_1) and in the shunt path to ac ground (R_2). The stabilization resistor must not be added into the dc bias path because it results in a power dependent bias point⁴ which destroys the whole linearity. The performance turns out not to be very sensitive on the matching, i.e. the variations of the bondwires will not have a great effect. Since there are resistors in series with both inductors, a low Q does not have an impact on the performance.

No stabilization resistors are intended for the CE design as showed in Fig. 4.15 since the simulations predicted stability. The matching is realized with a shunt inductor (on-chip spiral inductor connected to a through waver via)

⁴For the ideal case, the dc current and voltage at the base stay constant over increased power. However, simulations predict an increase of the current by at least a factor of three.

and a series (MIM) capacitor. Neither the bond wire in the signal path nor the bias itself could be implemented in the matching network.

Table 4.1: Matched input impedance at 1.8 GHz.

Design	Complex Impedance	Capacitance
CC 44	$10.88 + j 29.55$	2.99 pF
CC 88	$5.85 + j 18.81$	4.70 pF
CE 88	$2.50 + j 1.46$	60.56 pF

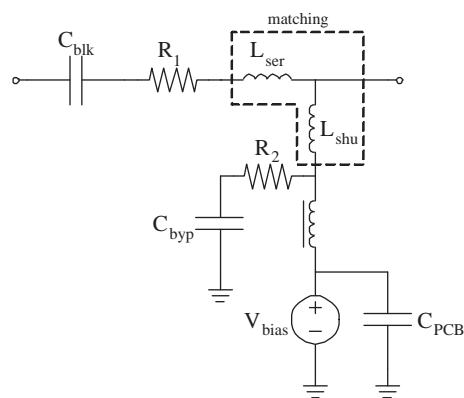


Figure 4.14: Schematic of the input network of the common collector amplifier.

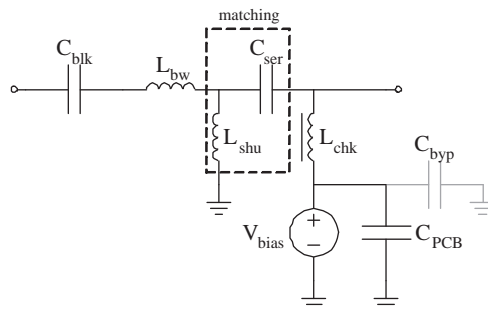


Figure 4.15: Schematic of the input network of the common emitter amplifier.

4.3.4 Common collector

The design of the *common* collector, i.e. the collector node at a constant voltage, brings the necessity of separating the ac path from the dc path. In theory, this is done simply by ensuring a good ac ground via a huge bypass capacitor and by establishing the dc connection to the power supply by means of a large choke inductor as showed earlier in Fig. 4.9. For a load impedance of around $5\ \Omega$, this capacitance has to exceed a hundred pico farads in order to guarantee a good short at the fundamental.

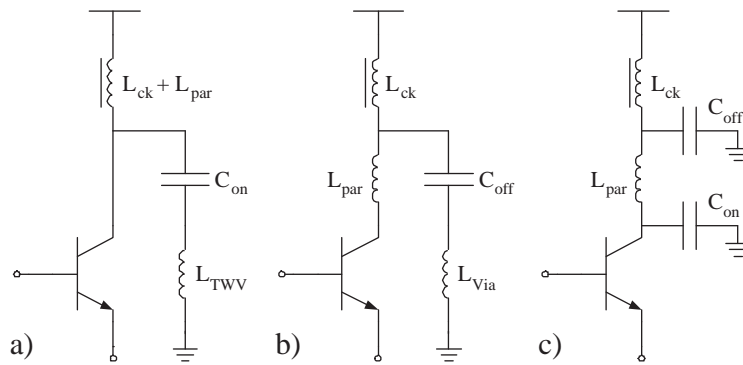


Figure 4.16: Three ways to achieve an ac ground at the collector.

Placing the entire bypass capacitance on-chip and connecting with a through waver via to ground, as shown in Fig. 4.16 a), results in a huge area overhead of easily half the chip area, all wasted for the ac ground. On the other hand, implementing the bypass capacitance off-chip, see drawing b) of Fig. 4.16, is neither a solution. Due to the parasitic (series) inductance of the chip capacitors and the contributions by the bondwire, the connecting transmission line and the via to ground, this structure resembles much more a series LC resonator, with a frequency likely below or at the design frequency, resulting in anything else but a broad band ac ground.

It seems now reasonable to distribute the bypass capacitance, i.e. having several stages of shunt capacitors and series inductors, e.g. an on-chip capacitor in the order of tens of pico farads and an off-chip capacitor of above a hundred pico farads, see Fig. 4.16 c). Unfortunately, this structure is likely to present high impedances at the collector (at various frequencies) due to the resulting parallel LC resonator built by the on-chip bypass capacitor and the bondwire inductance (the off-chip bypass capacitor is a short at high frequencies). A well known, widespread technique in oscillator design is to present a high impedance at the collector and a negative feed back to the input with a phase shift of π . Since the common collector does

have an inherent negative feedback, oscillation is not avoidable when the bypass capacitance is distributed as described above. To avoid the design of an oscillator, the very uneconomical version of an enormous on-chip capacitor is chosen for the presented design, being the only way to achieve reasonable high and stable gain.

One could have the idea to connect the backside of the chip to V_{dd} instead to ground, i.e. mirroring the CE design. However, there is no use of having a low reactive path to the power supply. The connection to ground through the bypass capacitor would have to be done off-chip via a bondwire, so this solution is even worse than the ones proposed above.

As a conclusion, finding a feasible way to realize an ac ground at the collector seems to be the major stumbling block of this structure. Even if it is possible to achieve high linearity and comparable (stable) gain and efficiency, the prize of a good ac ground at the collector is very high, making the common collector less attractive compared to the common emitter. However, at a frequency ten times higher than the design frequency, the required capacitance would be ten times less and hence would the occupied area, making the prize of an ac ground more affordable.

4.4 Simulation setup

4.4.1 Load and source pull simulation

For maximum power transfer, the input impedance at the interface has to be a conjugate match to the input port of the transistor. For the load impedance, the load line match is preferred to a conjugate match. A way to optimize the amplifier is to perform load and source pull simulations by varying the devices of the input and output matching network and determining the values which result in the highest efficiency and/or gain. As a benefit, the sensitivity of the performance on the device variations can be estimated. However, there are three facts that make the interpretation of the simulation results ambiguous:

Instability Instability results in higher simulated gain. Picking the load resistance which delivers maximum gain does not always mean maximum gain for the stabilized amplifier.

Bilateral behavior Since the CC amplifier is bilateral, several iterations of load and source pull simulations are required, since a modified load impedance changes the input impedance and vice versa.

Maximum efficiency vs. maximum gain Whereas at the input, a conjugated match has to be achieved and therefore maximum efficiency and gain fall together at the same presented input impedance, the two maxima are likely to be found at different load impedances. A plausible explanation is that for a given output load and a sweep over input power, the maximum efficiency occurs at a point where the amplifier is already in strong compression. For a load pull simulation at a given input power, maximum power means probably rather minimum compression and therefore increasing efficiency with further increased power.

Considering the previous statements, the following conclusion can be drawn, given a target maximum input power and several iterations of load and source pull simulations:

- An optimization towards maximum efficiency will lead to a maximum where probably heavy distortion occurs.
- Optimization for maximum gain will either lead to a point where the circuit is highly unstable or where the circuit is greatly linear but has a very low efficiency.

An engineering approach is finally advised by choosing a source/load impedance setup where sufficient gain and high efficiency is achieved. The linearity, resp. the degree of compression, should frequently be checked by comparing the small signal gain with the gain at the operating point.

4.4.2 Stability simulation

The load and source plane stability circles and the input and output reflection coefficients of the CC and CE circuit are illustrated in Fig. 4.17 and Fig. 4.18. The difference of the stability behavior of the two structures is palpable. For the CE (without any stabilization), all the stability circles go around the load and source plane circle, i.e. the amplifier is by nature unconditionally stable. In contrast, for the CC, even with very large stabilization resistors, the circles fall all over the source and load plane and the magnitude of the reflection coefficients are above one around the design frequency.

4.5 Test structures

Under the motto “design for testability”, several test structures are included into the design. On the CE chip, the harmonic filter capacitors are

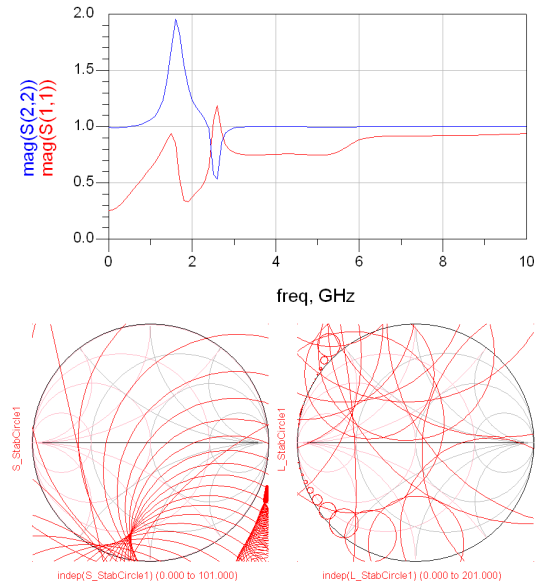


Figure 4.17: Reflection coefficients and load / source plane stability circles for CC44 with stabilization resistors of $30\ \Omega$ ($V_{dd} = 4\ \text{V}$, $R_b = 300\ \Omega$) from 100 MHz to 10 GHz.

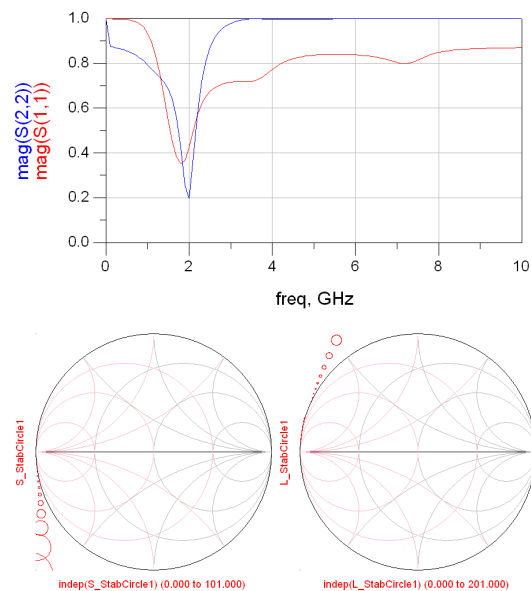


Figure 4.18: Reflection coefficients and load / source plane stability circles for CE88 ($V_{dd} = 4\ \text{V}$, $R_b = 300\ \Omega$) from 100 MHz to 10 GHz.

connected to a through waver via. On the CC 44 chip, one bondpad is connected to a through waver via which allows to measure the inductance of the bondwire. The third laminate board contains exclusively test structures and ground signal ground (GSG) pads with short and open circuits. By measuring the reflection coefficient of the ground connection, the inductance of the probe pad transmission line can be measured and subtracted from the measurements of the filter structure and the bondwire.

4.6 Layout

Three different designs are layouted, produced and tested, resulting in three different dies and two different laminates, one for the two CC chips and one for the CE chip. The third laminate is for test structures only. In Fig. 4.19 and 4.20 the schematic for the CC and CE design is showed.

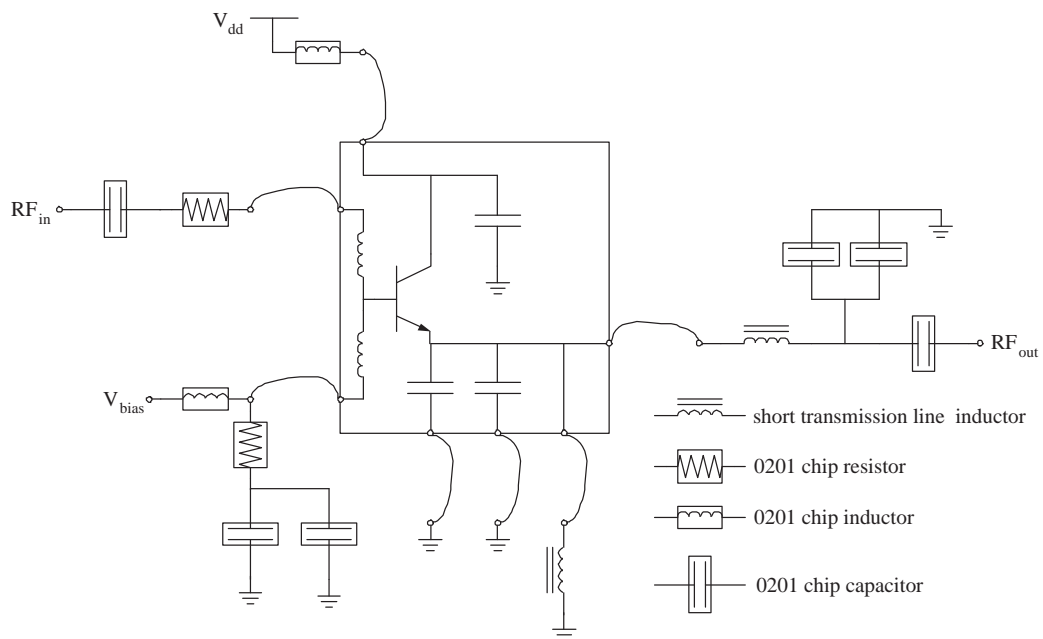


Figure 4.19: Schematic of the CC44/88 chip mounted on the laminate board.

4.6.1 Layout of the die

The three layouts are the following:

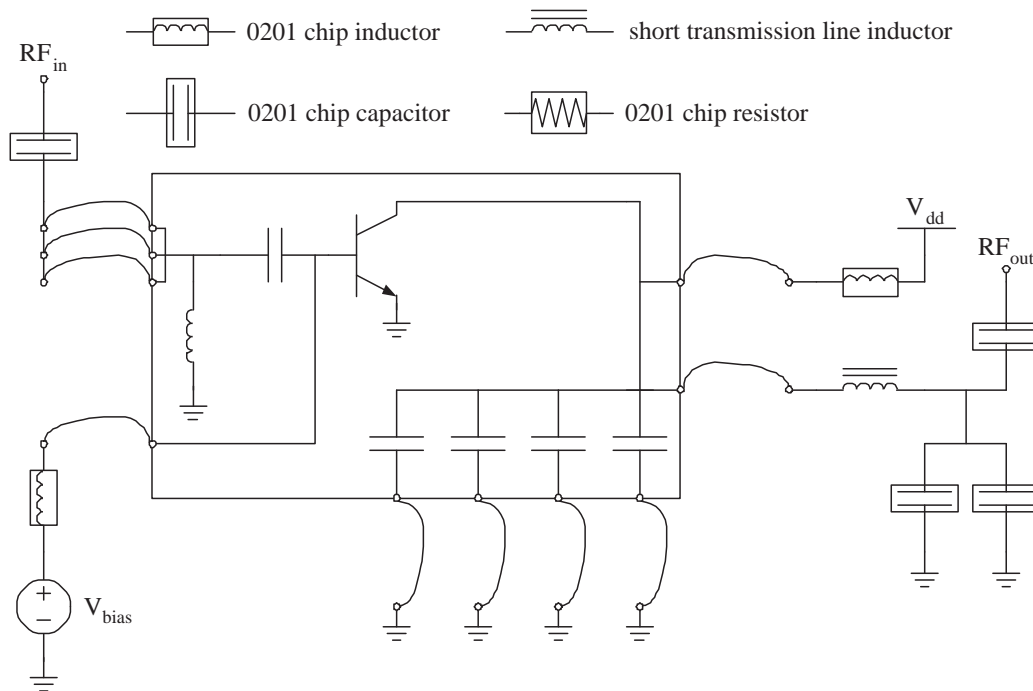


Figure 4.20: Schematic of the CE88 chip mounted on the laminate board.

CC 44 A common collector class B power amplifier with 44 HBTs in parallel. Additionally, a measurement setup for a single bondwire is implemented.

CC 88 A common collector class B power amplifier with 88 HBTs in parallel.

CE 88 A common emitter class B power amplifier with 88 HBTs in parallel. Not only shorts for the second and fourth but also for the third and fifth harmonic are implemented.

Fig. 4.21 shows the layout of the CC 44 chip providing a measurement setup for a single bondwire by a single bondpad (uppermost pad on the left side) with a connection to ground by a trough waver via. A mostly similar design is showed in Fig. 4.22 with the layout of the CC 88 chip. Notice the huge on-chip capacitor ensuring a good ac ground.

The common emitter layout is displayed in Fig. 4.23. The four bond pads along the upper side build a test structure for the harmonic shorts. The collector current on the output side (along right edge) is too high for the

width of the transmission line, so both metal layers are used to transport the current.

In tables 4.2 and 4.3 the implemented on-chip capacitors are listed. The implemented on-chip spiral inductors can be found in table 4.4.

Table 4.2: Implemented on-chip capacitances

Device	C [pF]	length [μm]	width [μm]	area [μm^2]
CC44 collector	351	685	550	376,750
CC88 collector 1	225.6	440	550	242,000
collector 2	41.3	260	170	44,200
collector 3	18.3	325	60	19,500
collector 4	7.6	95	85	8,075
Σ collector:	292.8			313,775
CE88 input series C	9.36 pF	83	120	9,960

Table 4.3: Implemented filter on-chip capacitances

Harmonic	C [pF]	length [μm]	width [μm]	area [μm^2]
2 nd	4.916	62	84	5,208
3 rd	2.165	27	84	2,268
4 th	1.221	15	84	1,260
5 th	0.779	10	79	790

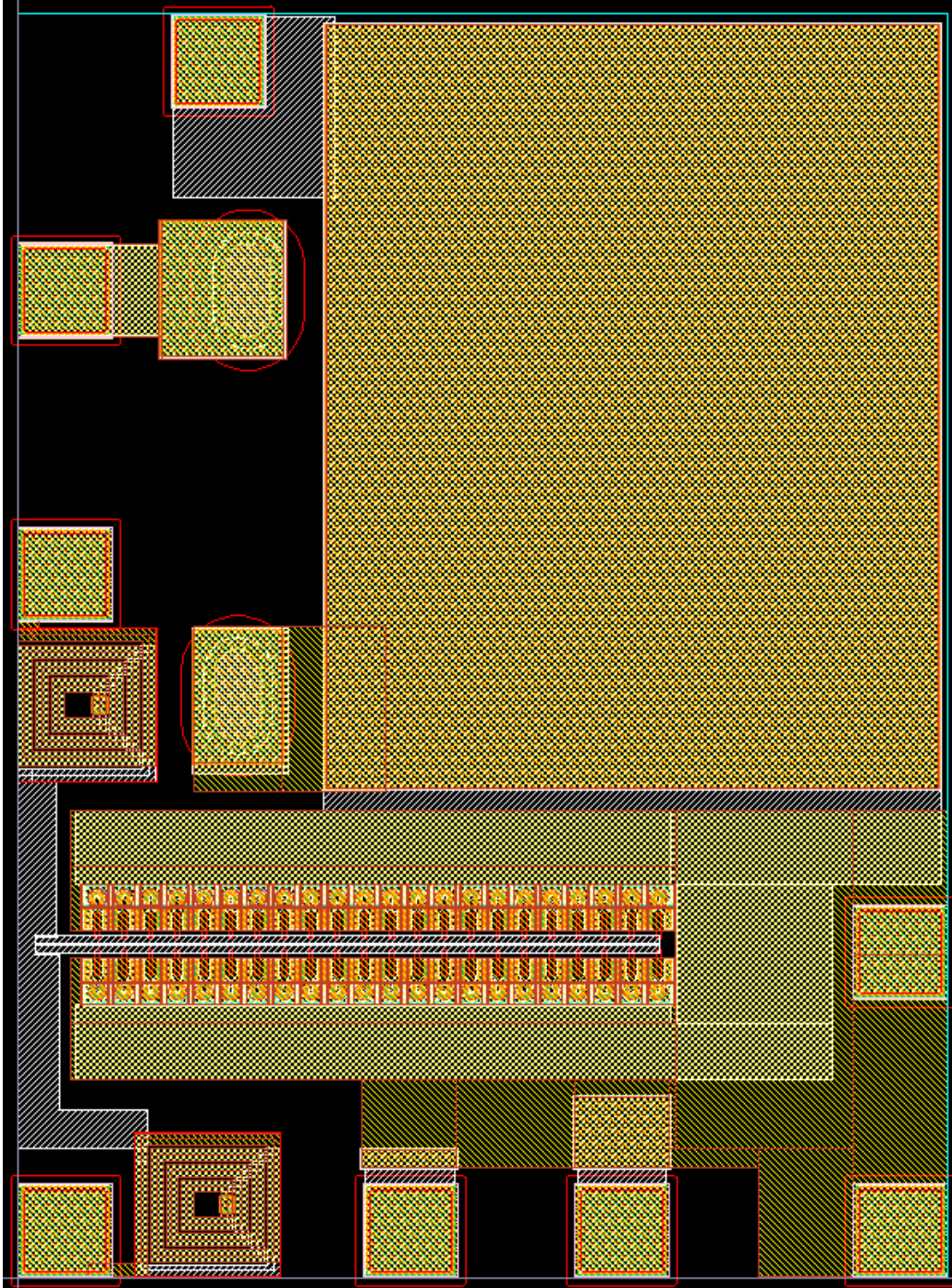


Figure 4.21: Layout of the common collector chip with 44 HBTs in parallel and the option for a single bondwire measurement

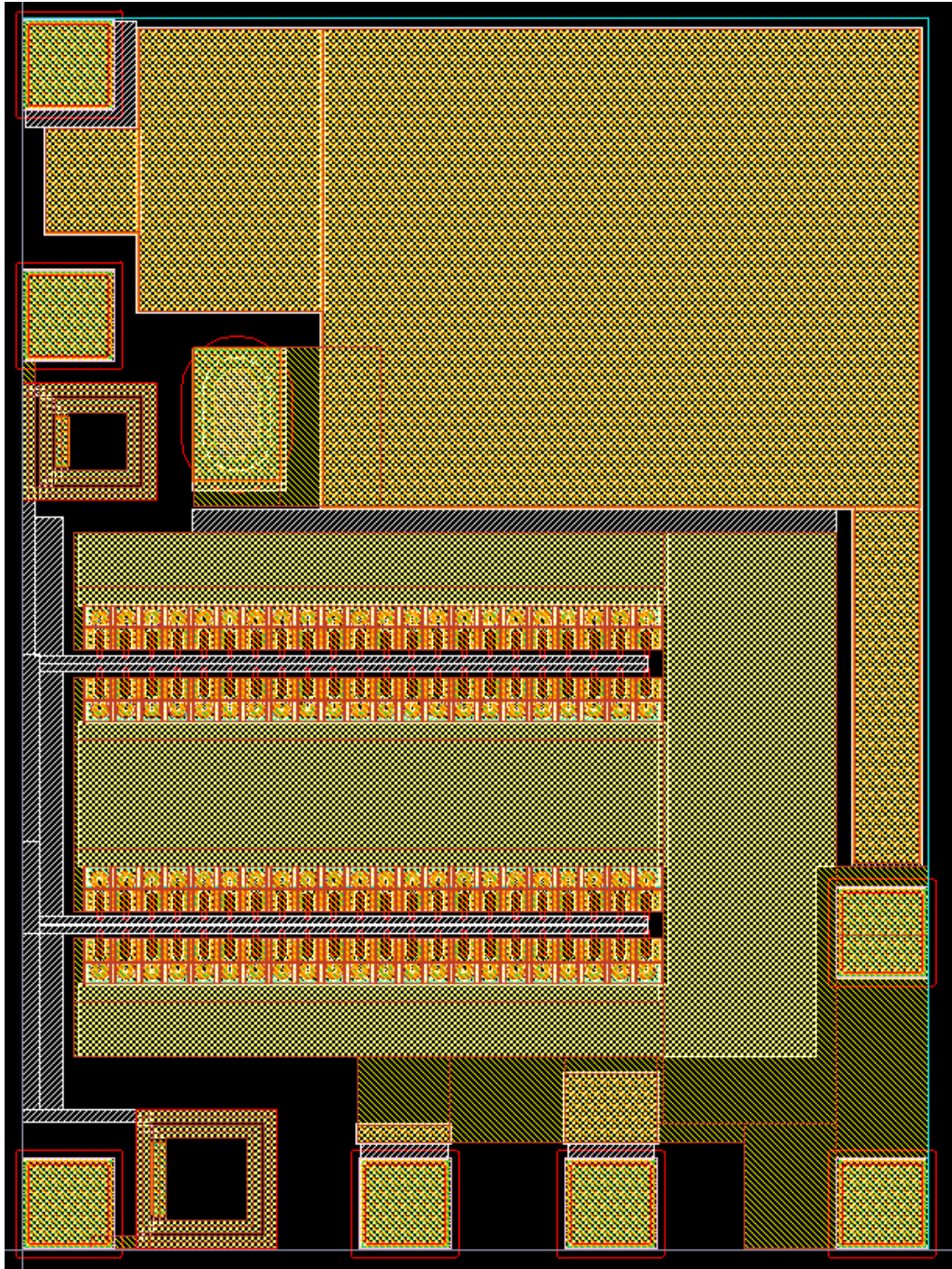


Figure 4.22: Layout of common collector chip with 88 HBTs in parallel



Figure 4.23: Layout of common emitter chip with 88 HBTs in parallel

Table 4.4: Implemented input matching on-chip spiral inductors

Device	segment width [μm]	segment spacing [μm]	turn number	xsize [μm]	ysize [μm]	L at 1.8 GHz [nH]	R [Ω]	Q
CC44								
series L	12.0	3.0	3 1/4	24.0	25.0	4.011	4.757	9.537
shunt L	11.0	3.0	3 1/2	23.0	24.0	4.444	5.776	8.723
CC88								
series L	12.0	3.0	2	54.0	54.0	2.522	3.394	8.404
shunt L	12.0	3.0	1 1/7	75.0	75.0	2.218	3.720	6.743
CE88								
shunt L	18.0	3.0	1 3/4	20.0	20.0	1.015	1.370	8.379

4.6.2 Layout of the laminate

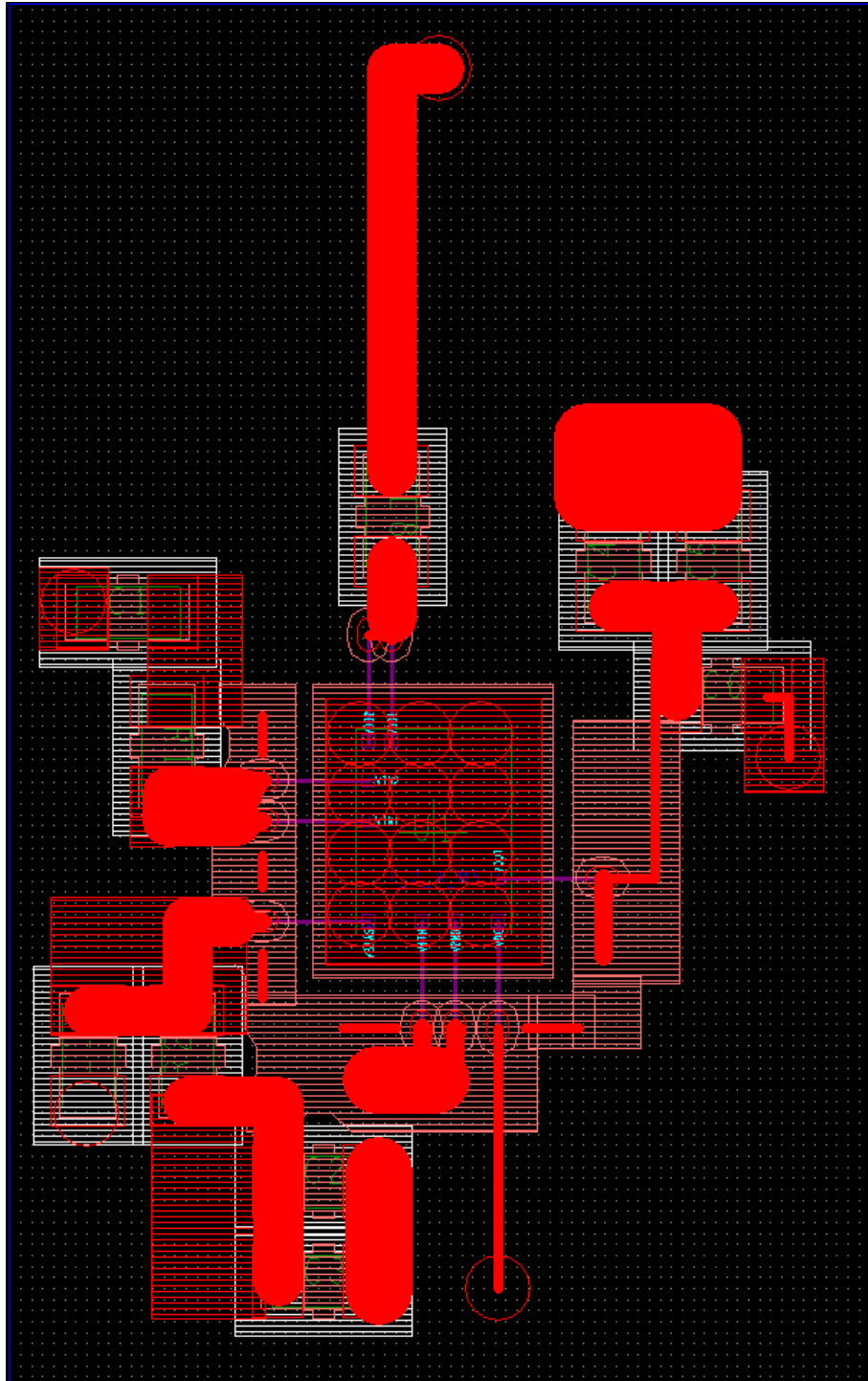


Figure 4.24: Layout of laminate board for CC44 and CC88 chip

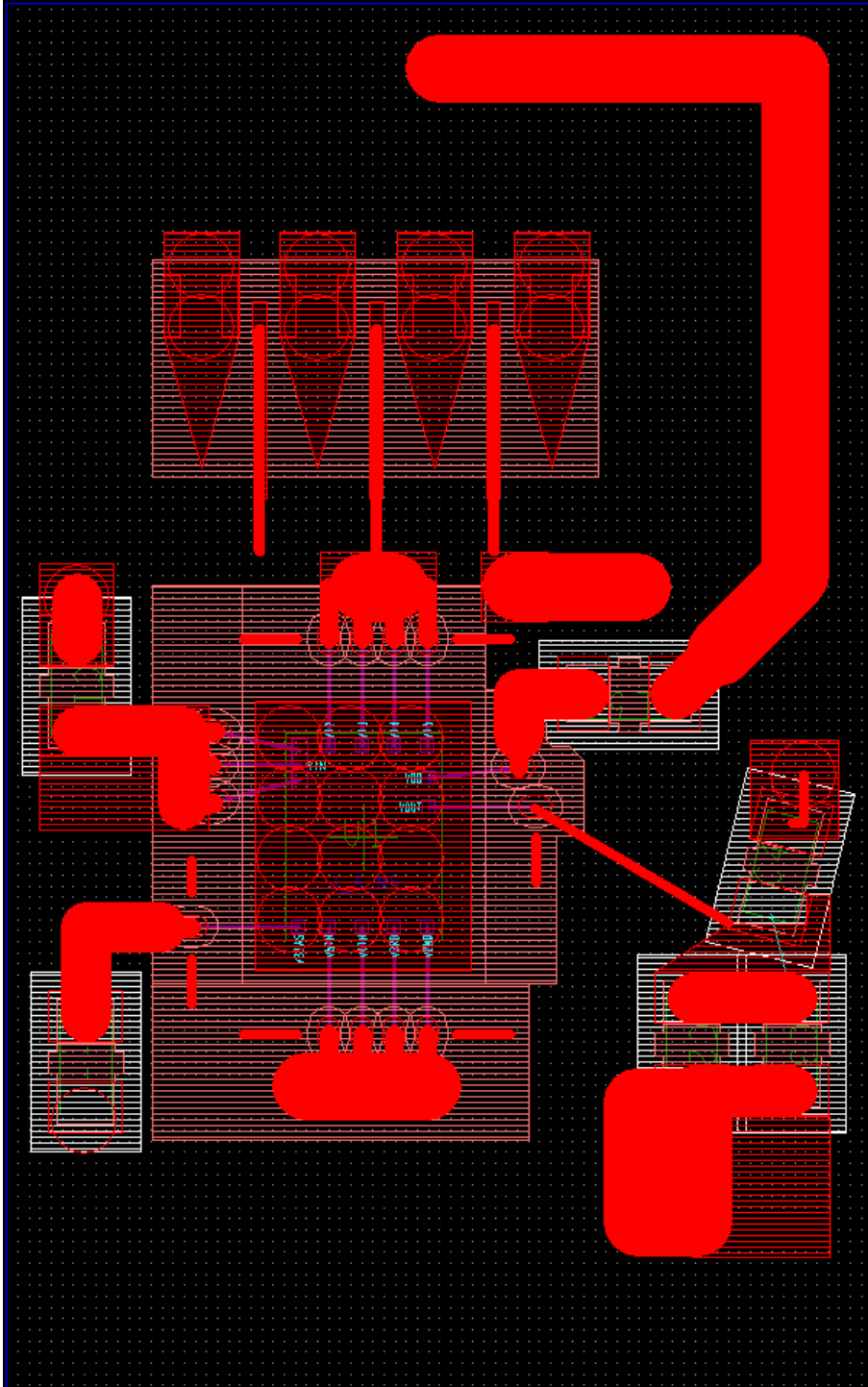


Figure 4.25: Layout of laminate board for CE88 chip

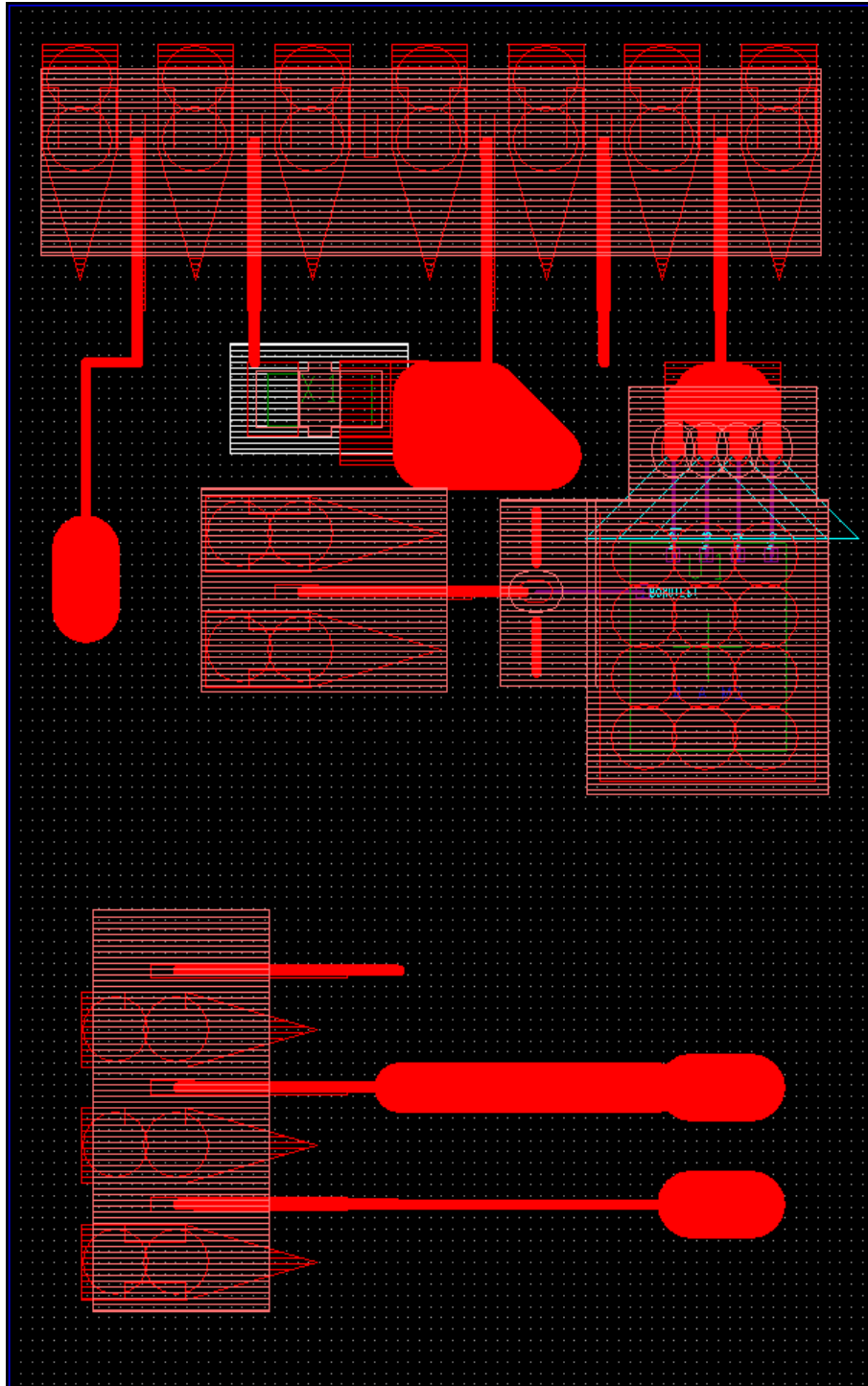


Figure 4.26: Layout of laminate board for test structures

Chapter 5

Measurements

The measurements of the implemented circuits are to be presented in this chapter. Numbers of measured figures like gain and efficiency of the power amplifiers are expected to be found here. Unfortunately, the amplifiers turned out to be unstable and none of the mentioned figures can be stated here.

Output filter There was not enough time to make detailed measurements of the test structures since other more pressing problems had to be solved first. However, the second harmonic short could be measured for two samples and the frequency behavior looked promising making the statement possible that the structure on-chip capacitor – bondwire – via to ground is a good series LC resonator. However, electronic data could not be acquired.

The measurements of the designs did uncover the following problems:

Choke inductor First, the 0201 inductor performing a choke turned out to have a rated current much below the requirements resulting in several burned elements. The device is replaced by a large 0603 wirewound chip inductor from Coilcraft[46] with a nominal inductance of 68 nH (170 nH at 1.8 GHz) and a rated current of 600 mA.

Thermal runaway and ballast resistor Second, as explained in subsection 4.2.1, the implemented ballast resistor at the base of each HBT of 300 Ω was chosen to low for a power supply voltage of 4 V. For the target voltage of 4 V, 900 Ω would have been required to prevent the thermal runaway. In order to avoid this problem, the power supply voltage was lowered to 2 V. The load presented at the output would not allow

anymore to go to the same high power but a comparison between CC and CE in terms of linearity would still be possible.

Bias oscillation for CE For the CE design, oscillations produced by the bias network were measured. Several values for the bypass capacitors on the PCB board and attempts to add resistors in series with the capacitors resulted all in an oscillation between 20 and 70 MHz, once the bias voltage was applied. With an input signal, these low frequency components were mixed up and appeared in side bands of the signal frequency. It was not possible to stabilize the bias network so now gain or efficiency measurements were possible. However, the amplifier itself seemed to be stable so a careful redesign of the bias network would lead to a working circuit.

Amplifier oscillation for CC In contrast to the CE design, no oscillation was observed by simply applying the bias and power supply to the amplifier. However, with increasing signal power, side bands around the design frequency arose. No low frequency components did appear, making the assumption reasonable that the oscillations are caused by the amplifier itself which is consistent with the simulation results. Stabilization resistor values of 10, 12 and 18 Ω did reduce (drastically) the gain but could not prevent the oscillation. Since the bias network is incorporated into the matching and filtering network, there are no low frequency stability problems.

Chapter 6

Conclusion

The design, implementation and measurement of a common collector and a common emitter Class B RF power amplifier in InGaP HBT technology at a frequency of 1.8 GHz is presented. Based on the analysis of the small signal model, the simulation results and the measurements, a high tendency to instability can be reported for the common collector structure. It was not possible to stabilize the design by inserting resistance. As a conclusion, this architecture is not recommended for amplifier design, even though it possibly offers better linearity compared to the common emitter. The latter structure proved to be more stable, however for a next design, the bias network would have to be done more carefully. The bias network of the common collector design is stable because it was possible to incorporate it into the matching and filtering network.

Beside the tendency to instability another fundamental problem of the common collector structures is reported, being the separation of the ac and dc path at the collector node. To avoid high impedances at RF frequencies, a very large capacitor has to be implemented on chip which makes this structure unattractive.

The harmonic terminations are realized in a very efficient way by using on-chip capacitors and bondwire inductors. Even though for the hand assembled prototypes the precision is not very high, for a machine assembled commercial product, this technique would offer a very inexpensive and space-saving way to implement the in power amplifiers utilized output filter structure.

Appendix A

Theory of load and source plane stability circles

Load (Γ_L) Plane and Output Stability Circle

- For what load resistance R_L is the input reflection coefficient $|\Gamma_{\text{IN}}| < 1$?
- Reflection on stability circle: $|\Gamma_{\text{IN}}| = 1$
- Condition for center of plane: $\Gamma_L = 0$ (matched output)
- Reflection at center of plane: $|\Gamma_{\text{IN}}|_{\text{Center}} = |S_{11}|$

Source (Γ_s) Plane and Input Stability Circle

- For what source resistance R_s is the output reflection coefficient $|\Gamma_{\text{OUT}}| < 1$?
- Reflection on stability circle: $|\Gamma_{\text{OUT}}| = 1$
- Condition for center of plane: $\Gamma_s = 0$ (matched input)
- Reflection at center of plane: $|\Gamma_{\text{OUT}}|_{\text{Center}} = |S_{22}|$

$$|\Gamma_s| < 1 \quad (\text{A.1})$$

$$|\Gamma_L| < 1 \quad (\text{A.2})$$

$$|\Gamma_{\text{IN}}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (\text{A.3})$$

$$|\Gamma_{\text{OUT}}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1 \quad (\text{A.4})$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 |S_{12}S_{21}|} \quad (\text{A.5})$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (\text{A.6})$$

$$K > 1 \quad (\text{A.7})$$

$$|\Delta| < 1 \quad (\text{A.8})$$

Γ_L values for $|\Gamma_{\text{IN}}| = 1$ (**Output Stability Circle in Load Plane**)

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \quad (\text{A.9})$$

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \quad (\text{A.10})$$

Γ_s values for $|\Gamma_{\text{OUT}}| = 1$ (**Input Stability Circle in Source Plane**)

$$r_s = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \quad (\text{A.11})$$

$$C_s = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \quad (\text{A.12})$$

Appendix B

Simulations of on-chip spiral inductors

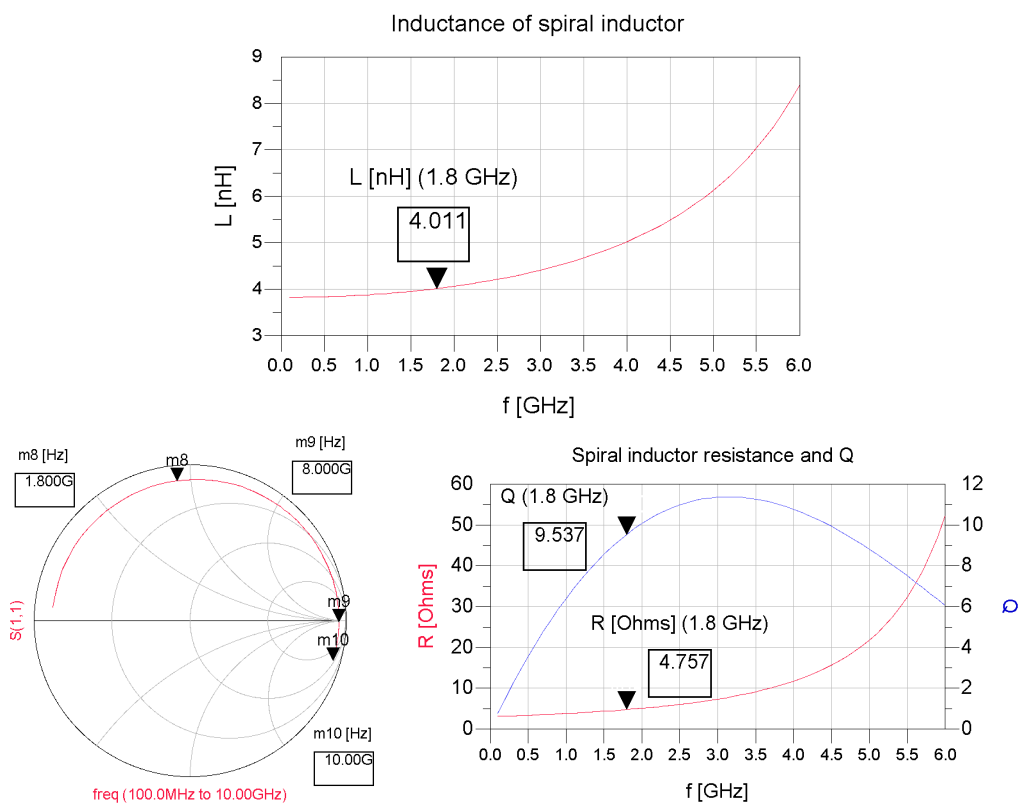


Figure B.1: Simulated S parameter, inductance, resistance and Q of input series spiral inductor on CC44.

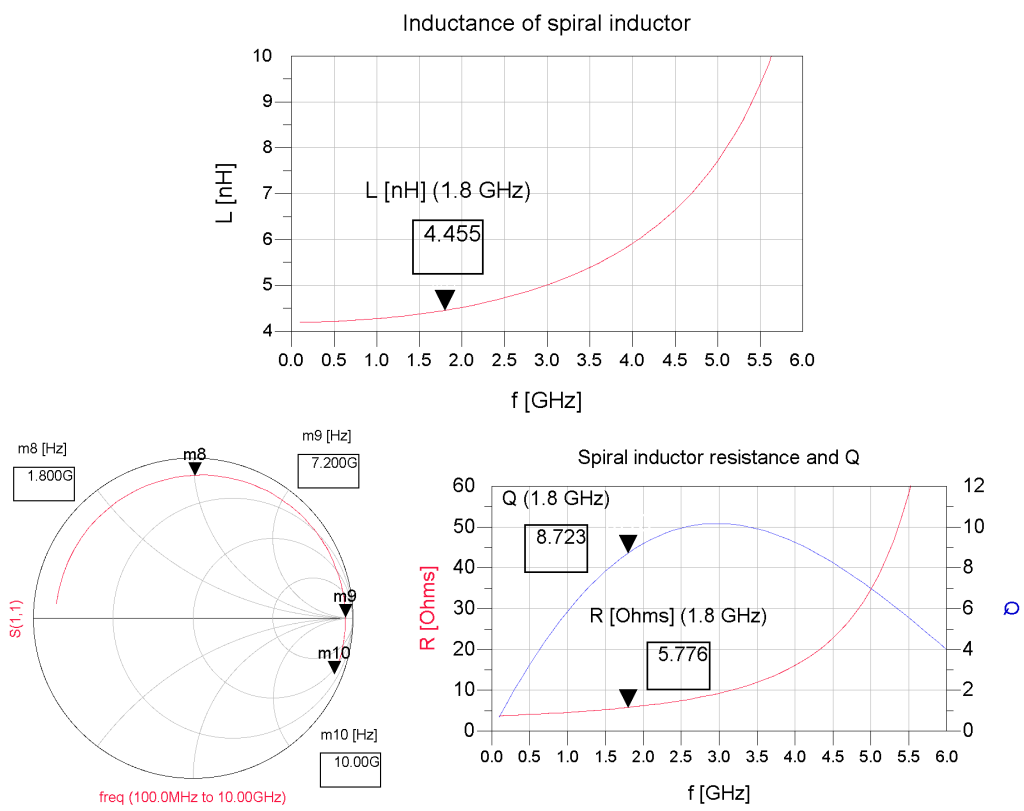


Figure B.2: Simulated S parameter, inductance, resistance and Q of input shunt spiral inductor on CC44.

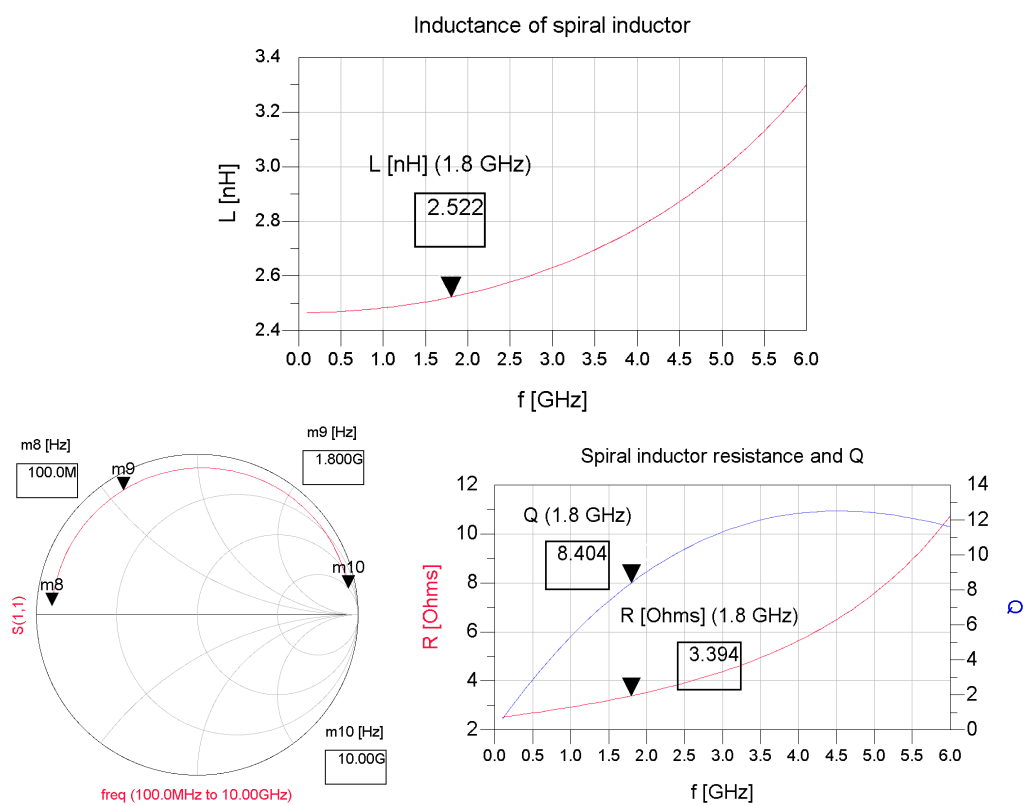


Figure B.3: Simulated S parameter, inductance, resistance and Q of input series spiral inductor on CC88.

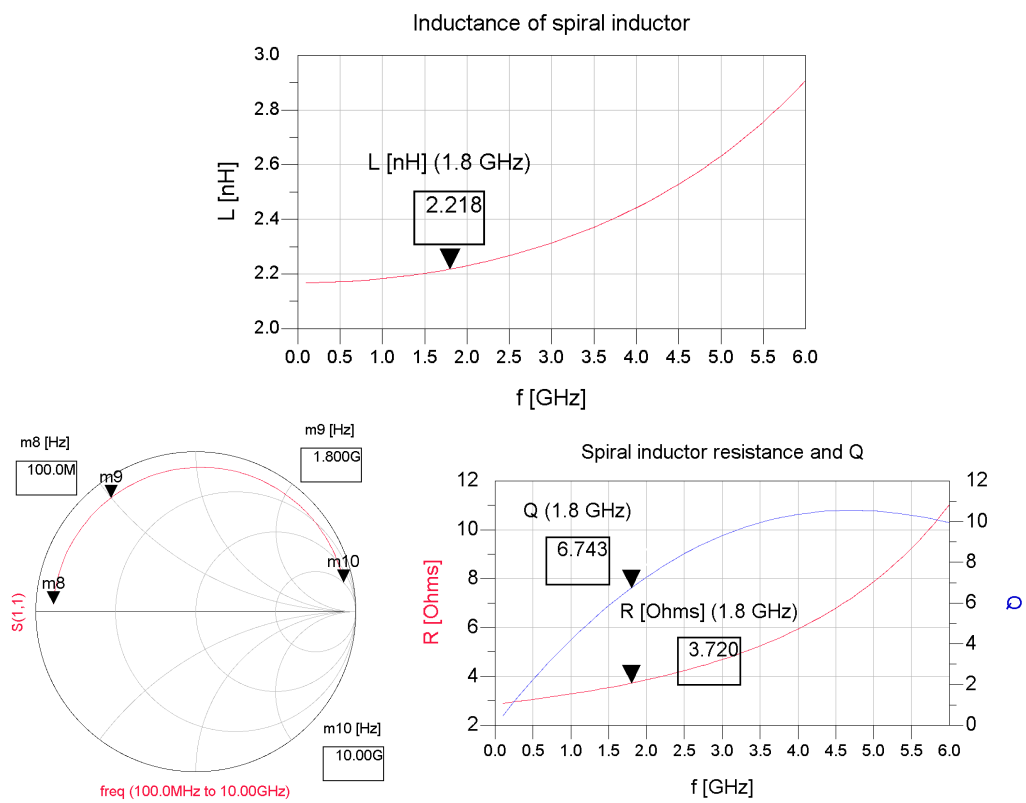


Figure B.4: Simulated S parameter, inductance, resistance and Q of input shunt spiral inductor on CC88.

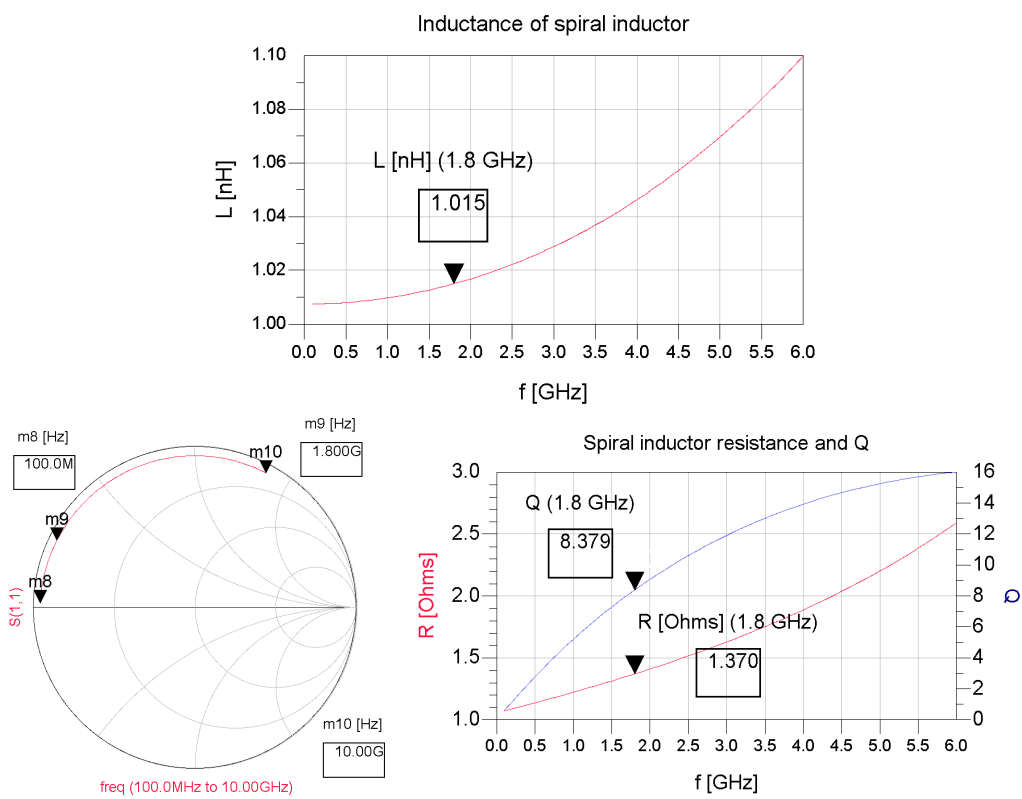
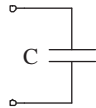


Figure B.5: Simulated S parameter, inductance, resistance and Q of input shunt spiral inductor on CE88.

Appendix C

LC networks



$$Z = \frac{1}{j\omega C} \quad (\text{C.1})$$

$$p_1 = 0 \quad (\text{C.2})$$

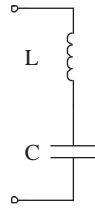
$$Q = \omega R_{shu} C \quad (\text{C.3})$$



$$Z = j\omega L \quad (\text{C.4})$$

$$z_1 = 0 \quad (\text{C.5})$$

$$Q = \omega \frac{L}{R_{ser}} \quad (\text{C.6})$$

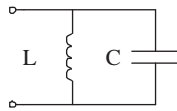


$$Z = \frac{1 - \omega^2 LC}{j\omega C} \quad (\text{C.7})$$

$$z_1 = \frac{1}{\sqrt{LC}} \quad (\text{C.8})$$

$$p_1 = 0 \quad (\text{C.9})$$

$$Q = \frac{\sqrt{L/C}}{R_{ser}} \quad (\text{C.10})$$

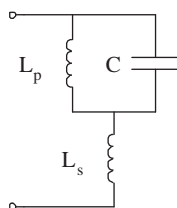


$$Z = \frac{j\omega L}{1 - \omega^2 LC} \quad (\text{C.11})$$

$$z_1 = 0 \quad (\text{C.12})$$

$$p_1 = \frac{1}{\sqrt{LC}} \quad (\text{C.13})$$

$$Q = \sqrt{C/L} R_{shu} \quad (\text{C.14})$$

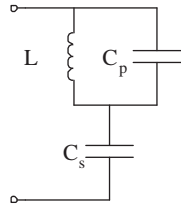


$$Z = j\omega \frac{L_p + L_s - \omega^2 L_p L_s C}{1 - \omega^2 L_p C} \quad (\text{C.15})$$

$$z_1 = 0 \quad (\text{C.16})$$

$$z_2 = \sqrt{\frac{L_p + L_s}{L_p L_s C}} \quad (\text{C.17})$$

$$p_1 = \frac{1}{\sqrt{L_p C}} \quad (\text{C.18})$$

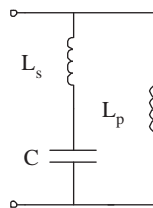


$$Z = \frac{1 - \omega^2 L (C_s + C_p)}{j\omega C_s (1 - \omega^2 L C_p)} \quad (\text{C.19})$$

$$z_1 = \frac{1}{\sqrt{L (C_s + C_p)}} \quad (\text{C.20})$$

$$p_1 = 0 \quad (\text{C.21})$$

$$p_2 = \frac{1}{\sqrt{L C_p}} \quad (\text{C.22})$$

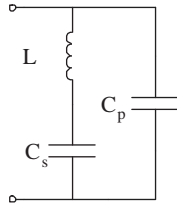


$$Z = j\omega L_p \frac{1 - \omega^2 C L_s}{1 - \omega^2 C (L_s + L_p)} \quad (\text{C.23})$$

$$z_1 = 0 \quad (\text{C.24})$$

$$z_2 = \frac{1}{\sqrt{L_s C}} \quad (\text{C.25})$$

$$p_1 = \frac{1}{\sqrt{(L_s + L_p) C}} \quad (\text{C.26})$$



$$Z = \frac{1 - \omega^2 L C_s}{j\omega (C_s + C_p - \omega^2 L C_s C_p)} \quad (\text{C.27})$$

$$z_1 = \frac{1}{\sqrt{L C_s}} \quad (\text{C.28})$$

$$p_1 = 0 \quad (\text{C.29})$$

$$p_2 = \sqrt{\frac{C_s + C_p}{C_s C_p L}} \quad (\text{C.30})$$

List of Figures

1.1	Schematic of a push-pull common-drain class B power amplifier [2, 12].	3
1.2	Voltage transfer function of the structure in Fig. 1.1 under different bias conditions [2, 12].	3
2.1	Very simplified diagram of a single stage power amplifier.	7
2.2	PA schematic.	9
2.3	Simplified small signal equivalent circuit of the CE a) and the CC b) architecture.	12
2.4	Normalized voltage (V_{be} , V_{ce}) and current (I_{ce}) waveforms for Classes A, AB, B and C.	15
2.5	Normalized ($I_{max} = 1$) collector emitter current decomposed into Fourier components versus a sweep over the conduction angle.	17
2.6	RF output power and efficiency versus a sweep over the conduction angle.	17
2.7	Conjugate match and load-line match.	19
2.8	Load line in a I_{ce} versus V_{ce} plot.	20
2.9	I_{ce} versus V_{ce} plot to determine the knee voltage.	21
2.10	Ideal, loss less, input and output coupler allowing to determine the large signal S-parameters in ADS.	24
3.1	Layout view of the test board.	31
3.2	Layout view of a q56p0re horse shoe ring emitter HBT with collector, emitter and heat shunt, base and ballast resistor. Metal 2 is invisible.	34
3.3	Detail layout view of an array of q56p0re HBTs. Metal 2 is yellow, metal 1 is gray.	35
3.4	Setup of a bondwire connecting bond pads on the die and the laminate board.	41

3.5	Simulated inductance of an Au bondwire, diameter 30 μm , die height 100 μm	42
3.6	Simulated inductance of an Au bondwire, diameter 30 μm , die height 100 μm , detailed.	43
3.7	Simulated resistance (m1) and Q (m2) of a gold bondwire, diameter 30 μm , die height 100 μm	44
4.1	I_{ce} versus V_{be} of 88 HBTs in parallel with V_{dd} from 4 V to 2 V (step size 0.5 V) at $R_b = 300 \Omega$	53
4.2	I_{ce} versus V_{be} of 88 HBTs in parallel with R_b from 300 Ω to 900 Ω (step size 150 Ω) at $V_{dd} = 4$ V.	53
4.3	Linear and log plot of I_{ce} versus V_{be} of a single HBT ($V_{dd} = 2$ V).	55
4.4	Determining the Class B bias point via the odd component of the transfer function.	56
4.5	Voltage current transfer function and its odd part for 1.20 V to 1.50 V (step 0.05 V) bias voltage, $V_{dd} = 2$ V, $R_b = 300 \Omega$	57
4.6	Detailed view of the voltage current transfer function, its odd part and the second derivative thereof for 1.32 V to 1.36 V (step 0.01 V) bias voltage, $V_{dd} = 2$ V, $R_b = 300 \Omega$	58
4.7	Sweep over input power and at various bias voltages (1.28 V to 1.36 V) at $R_b = 300 \Omega$ and $V_{dd} = 4$ V.	59
4.8	CC (a,b,c) and CE (d,e,f) PA schematic for dc, fundamental and even harmonics.	61
4.9	The twice three schematics from figure 4.8 realized in a CC (a) and CE (b) design.	62
4.10	Matching L network in low pass configuration for impedance transformation.	65
4.11	A series LC network	65
4.12	Network performing the harmonic termination.	67
4.13	The complete output network.	67
4.14	Schematic of the input network of the common collector amplifier.	69
4.15	Schematic of the input network of the common emitter amplifier.	69
4.16	Three ways to achieve an ac ground at the collector.	70
4.17	Reflection coefficients and load / source plane stability circles for CC44 with stabilization resistors of 30 Ω ($V_{dd} = 4$ V, $R_b = 300 \Omega$) from 100 MHz to 10 GHz.	73
4.18	Reflection coefficients and load / source plane stability circles for CE88 ($V_{dd} = 4$ V, $R_b = 300 \Omega$) from 100 MHz to 10 GHz.	73
4.19	Schematic of the CC44/88 chip mounted on the laminate board.	74
4.20	Schematic of the CE88 chip mounted on the laminate board.	75

4.21	Layout of the common collector chip with 44 HBTs in parallel and the option for a single bondwire measurement	77
4.22	Layout of common collector chip with 88 HBTs in parallel . . .	78
4.23	Layout of common emitter chip with 88 HBTs in parallel . . .	79
4.24	Layout of laminate board for CC44 and CC88 chip	82
4.25	Layout of laminate board for CE88 chip	83
4.26	Layout of laminate board for test structures	84
B.1	Simulated S parameter, inductance, resistance and Q of input series spiral inductor on CC44.	91
B.2	Simulated S parameter, inductance, resistance and Q of input shunt spiral inductor on CC44.	92
B.3	Simulated S parameter, inductance, resistance and Q of input series spiral inductor on CC88.	93
B.4	Simulated S parameter, inductance, resistance and Q of input shunt spiral inductor on CC88.	94
B.5	Simulated S parameter, inductance, resistance and Q of input shunt spiral inductor on CE88.	95

List of Tables

1.1	Class B power amplifier specifications, defined at -1 dB compression.	5
2.1	Normalized current magnitude of individual frequency components at a conduction angle of 180° (class B).	18
3.1	Material configuration of AlGaAs and InGaP HBTs [37]	31
3.2	Emitter area and maximum current for the q56p0re and q117p0re HBT [34].	32
3.3	Breakdown voltages for the q56p0re HBT at 25°C [34].	32
3.4	HBT transit frequency f_T at $V_{CE} = 1.5$ V, $T = 27^\circ\text{C}$ [34]	33
3.5	HBT gain at $0.1\text{ mA}/\mu\text{m}^2$, $V_{CE} = 1.5$ V, $T = 27^\circ\text{C}$ [34]	33
3.6	Maximum dc current densities	36
3.7	Metal layer specifications	37
3.8	Specifications for the Through Waver Via (TWV) [34]	38
3.9	Accounted bondwire properties in the model and implemented values.	41
3.10	Capacitance values for an LC resonator with $L = 0.4$ nH.	43
4.1	Matched input impedance at 1.8 GHz.	69
4.2	Implemented on-chip capacitances	76
4.3	Implemented filter on-chip capacitances	76
4.4	Implemented input matching on-chip spiral inductors	80

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