Eidgenössische Technische Hochschule Zürich
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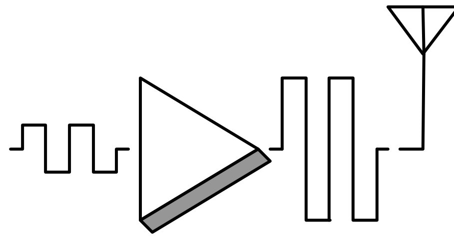
Device Evaluation for Current-Mode Class-D RF Power Amplifiers

Diploma Thesis by

Thomas Dellsperger



Diploma thesis written at the University of California, Santa Barbara

Tutored by Prof. S. Long (UCSB)
and R. Negra (ETHZ)

Submitted to Prof. W. Bächtold
Institute for Electromagnetic Fields and Microwave Electronics
Department of Information Technology and Electrical Engineering
ETH Zürich

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Abstract

Radio-frequency power amplifiers (RF PAs) are among the key building blocks for wireless communication systems. They are used to amplify the RF signal at the output of the transmitter before the RF signal is fed into the antenna. This study evaluates the Si MOSFET, the Si LDMOS FET, the SiGe HBT, and the AlGaAs/InGaAs pHEMT as switches for use in a current-mode class-D (CMCD) RF switching-mode PA. The goal of this study was to determine which of the above devices delivers the highest efficiency at 0.8-1.0 GHz and 1.8-2.2 GHz for 10-20 W of output power, and at 5.8 GHz for 3 W of output power. The study presents a detailed analysis of a CMCD PA based upon spectrum-limited waveforms for the device voltage and current. An analytical expression for the power added efficiency (PAE) of a CMCD PA employing FET devices is derived as a function of the mobility μ_n, oxide cap. C_{ox}, overlap cap. C_{ov}, gate sheet res. $R_{g,sheet}$, gate contact res. $R_{g,contact}$, source res. R_s, number of fingers F, gate width W, gate length L, the supply voltage V_{dd}, the shunt-tank res. R, and the input voltage amplitude $\hat{V}_{in}$. A sensitivity analysis revealed that C_{ox}, F, W, L, R, and $\hat{V}_{in}$ must be optimized, that V_{dd} must be maximized, and that C_{ov}, $R_{g,sheet}$, and R_s must be minimized for a reference LDMOS FET in order to maximize the PAE. To identify the differences in device parameters between the devices of interest, commercially available packaged devices are investigated followed by a theoretical analysis of the breakdown phenomena, the switching performance, and the on-resistance for the devices of interest. An expression for the maximum achievable drain-efficiency as a function of V_{dd}, R_s, and the output power was derived, which shows that a low breakdown voltage fundamentally limits the achievable PAE. Harmonic-balance simulations for CMCD PAs with ideal passive circuitry are performed for packaged LDMOS FETs (Motorola MRF281SR1), packaged pHEMTs (Filtronic LP3000P100), and packaged SiGe HBTs (Infineon BFP690) at 900 MHz, 1.8 GHz, and 5.8 GHz following well-defined optimization guidelines for $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$. The same is done for CMCD PAs employing pHEMTs and InGaP HBTs of Triquint's TQPHT and TQHBT2 process, respectively. Based upon the results from the analytical analysis and the simulations, the study recommends using LDMOS FETs for hybrid solutions (simulated $PAE \approx 70$ %) and pHEMTs for integrated solutions (simulated $PAE \approx 90$ %) when the target output power is 10-20 W and the target frequency is below 2 GHz. Above 2 GHz, pHEMTs are recommended for hybrid (simulated $PAE \approx 35$ % for 1 W of output power) and integrated solutions (simulated $PAE \approx 90$ % for 3 W of output power).

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Thomas Dellsperger
thomasd@ieee.org

Chapter 1

Introduction

1.1 Motivation and Objectives

RF power amplifiers field of application Radio-frequency power amplifiers (RF PAs) are among the key building blocks for wireless communication systems. As shown in Fig. 1.1 depicting a simplified RF section of a heterodyne transceiver, a PA is employed in the transmitting path of a transceiver. The purpose of a PA is to amplify the power of the RF signal before it is fed into the antenna. Besides achieving the required amplification, a PA must convert as much DC power into RF power as possible to work efficiently. The ratio of the RF power delivered to the antenna, to the DC power consumed from the power supply, is the efficiency of the PA and its primary performance figure. A comparison between switching-mode PAs that employ the transistors as switches, and traditional linear-mode PAs that employ the transistors as current-sources, shows that the efficiencies of switching-mode PAs are substantially higher. Therefore, switching-mode PAs may rival traditional linear-mode PAs in applications where non-linearities are acceptable. Besides having a higher efficiency, switching-mode PAs are also less susceptible to parameter variations and impose a lower thermal stress on the transistors than linear-mode PAs.

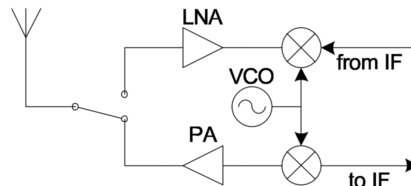


Figure 1.1: Simplified RF section of a heterodyne transceiver.

Table 1.1: Abbreviations of devices investigated.

Abbreviation	Full name
Si MOSFET	Silicon Metal-Oxide-Semiconductor Field-Effect-Transistor
Si LDMOS	Silicon Lateral Double-Diffused Field-Effect-Transistor
SiGe HBT	Silicon-Germanium Hetero-Bipolar-Transistor
AlGaAs/InGaAs pHEMT	Aluminum-Gallium-Arsenic/Indium-Gallium-Arsenic pseudomorphic High-Electron-Mobility-Transistor

Objectives of this study Due to the higher efficiency of switching-mode PAs, their use for lower power portable applications (3 W output power at 5.8 GHz) and higher power fixed applications (base-stations, 10-20 W output power at 0.8-1.0 GHz and 1.8-2.2 GHz) are of interest. Especially current-mode class-D switching-mode PAs are expected to deliver a high efficiency in these applications. There are various types of devices that may serve as switches in current-mode class-D PAs. Linear-mode PAs for cellular handsets and base stations have generally employed either GaAs HBT or Si LDMOS FET devices. This study evaluates the devices Si MOSFET, Si LDMOS FET, SiGe HBT, and AlGaAs/InGaAs pHEMT as switches for use in a current-mode class-D RF switching-mode PA (refer to Tab. 1.1 for the full names of the abbreviations). The goal of this study was to determine which of the above devices delivers the highest efficiency at 0.8-1.0 GHz and 1.8-2.2 GHz for 10-20 W of output power, and at 5.8 GHz for 3 W of output power.

PA performance figures PAs may be characterized by their efficiency, RF output power, linearity, mid-band frequency, relative bandwidth, supply voltage and package size. Several figures to assess the efficiency of a PA are in use. The drain efficiency[1] η is defined as the ratio of the RF output power $P_{out,1}$ delivered to the antenna, to the DC power P_{dc} consumed from the power supply:

$$\eta = \frac{P_{out,1}}{P_{dc}}$$

The power added efficiency PAE also takes into account the RF input power $P_{in,1}$ and is defined as

$$PAE = \frac{P_{out,1} - P_{in,1}}{P_{dc}} = \eta \left(1 - \frac{1}{G}\right)$$

[1]In this report, FET designations are used for general expressions. The drain efficiency corresponds to the collector efficiency in case of a BJT.

where η is the drain efficiency and $G = \frac{P_{out,1}}{P_{in,1}}$ is the power gain. The subscript $_1$ in $P_{out,1}$ and $P_{in,1}$ refers to the Fourier-component at the fundamental frequency. Another figure of merit is the output power capability P_{max} and is defined as

$$P_{max} = \frac{P_{out,1}}{V_{ds,pk} I_{ds,pk}}$$

where $V_{ds,pk}$ and $I_{ds,pk}$ are the peak drain-source voltage and current, respectively. P_{max} measures how much RF output power per Watts of peak power dissipation a PA is capable to deliver. The peak power dissipation directly relates to the peak device stress. As breakdown voltages and maximum allowable currents are limitations when designing PAs, P_{max} is an useful figure of merit besides the PAE to assess the performance of PAs.

Linearity vs. efficiency High linearity and high efficiency are conflicting requirements for a PA. On the one hand, linear-mode PAs provide high linearity but exhibit only a moderate efficiency. On the other hand, switching-mode PAs deliver a high efficiency but are highly non-linear.

The efficiency of the PA in a portable system directly affects the talk time: according to [1], the RF section of a cellular handset eats up somewhat more than half of the overall consumed power for a voice call on a 2G system, and somewhat less than half of the overall consumed power for a video call on a 3G system. The efficiency of PAs employed in base stations is as important as it is for PAs employed in handsets. For base stations, the efficiency of the PA severely affects the operating costs as highly efficient PAs considerably reduce the expenses for electricity. Besides saving battery power and reducing operating costs, highly efficient PAs also increase the reliability due to lower thermal stress.

The linearity of a PA is the degree to which the output and input voltage are linearly related and the degree to which their phases are equal (from [2]). More rigorous definitions of linearity are the ACPR (adjacent channel power ratio) or the IP3 (intercept point 3rd order). The linearity requirements for PAs are determined by the modulation scheme at hand. Generally, bandwidth-efficient modulation schemes demand higher linearity than less bandwidth-efficient ones. Consequently, cellular standards like NADC (North American Digital Cellular) employing $\pi/4$ DQPSK, or UMTS (Universal Mobile Telecommunication System) employing WCDMA and TD-CDMA, all variable-envelope modulation schemes, have higher linearity requirements than cellular standards like GSM employing GMSK, a constant-envelope modulation scheme. The less rigorous linearity requirements of constant-envelope modulation schemes allow to employ switching-mode PAs and thus to trade bandwidth for power consumption. For variable-envelope modulation schemes, two approaches are possible: either to use a low-efficient but linear-mode PA, or to use a high-efficient but non-linear switching-mode PA in conjunction with a linearization technique.

1.2 Document Organization

Chapter 2 reviews existing literature on switching-mode PAs and on devices for switching-mode PAs. 15 recent research designs of switching-mode PAs are compared by plotting the PAE versus the maximum RF output power. A short survey of commercial cellular telephony handset PAs is given.

Chapter 3 presents a detailed analysis of a CMCD PA based upon spectrum-limited waveforms for the device voltage and current. Analytical expressions for the input, output, and DC power as well as for the drain-efficiency and PAE of a current-mode class-D PA employing FET devices are derived. These analytical expressions allow a sensitivity analysis of the PAE towards various device parameters. To identify the differences in device parameters between the devices of interest, commercially available packaged devices are investigated followed by a theoretical analysis of the breakdown phenomena, the switching performance, and the on-resistance for the devices of interest. An expression for the maximum achievable drain-efficiency as a function of V_{dd}, R_s, and the output power is derived. Chapter 3 concludes with recommendations for device selection based upon the maximum achievable drain-efficiency.

Chapter 4 presents the results of harmonic-balance simulations at 900 MHz, 1.8 GHz, and 5.8 GHz for CMCD PAs with ideal passive circuitry for packaged LDMOS FETs (Motorola MRF281SR1), packaged pHEMTs (Filtronic LP3000P100), packaged SiGe HBTs (Infineon BFP690), non-packaged pHEMTs in Triquint's TQPHT process, and non-packaged InGaP HBTs in Triquint's TQHBT2 process. Chapter 4 concludes with recommendations for device selection based upon the simulation results.

Chapter 5 makes recommendations for device selection based upon the results from chapter 3 and 4, summarizes the achievements of this work, and gives suggestions for further study.

Appendix A reprints the original task description by Prof. S. I. Long.

Appendix B provides an overview of the data contained on the enclosed CDROM.

Chapter 2

Literature Review

2.1 Research on Class-E and Class-D PAs

Switching-Mode PAs and research focus on class-E PAs Switching-mode PAs have first been investigated by Baxandall in 1959 [3] discussing a class-D PA. Subsequently, class-D PAs have been employed in AM broadcast transmitters, for DC to DC power conversion, in audio amplifiers, and more recently in hearing aids [2]. With the advent of personal wireless communications, high-efficiency PAs for use at low GHz frequencies became a strong research interest. Particularly interesting for this application are switching-mode PAs that theoretically attain a drain efficiency of 100% at a non-zero RF output power. Recent research publications of switching-mode PAs for personal wireless communications strongly focus on class-E PAs, a switching-mode PA invented in 1975 by A. and N. Sokal [4]. Subsequently, various class-E PA implementations for RF transmitters have been reported. [5, 6, 7, 8, 9, 10, 11, 12, 13] are the most recent ones since 1995. An extensive treatment of class-E PAs is given in D. Choi's Ph.D. dissertation at the UCSB [2]. General treatment of PAs including switching-mode PAs can be found in books by Cripps [14], Kenington [15], Raab [16], or Lee [17].

The advantage of the class-E topology over other switching-mode PAs is mainly twofold [2]: it requires only a single transistor and does without any baluns (BALanced to UNbalanced, a circuit that converts a differential signal to a single-ended signal). In contrast to the class-E topology, the class-D topology employs two transistors and requires input and output baluns. However, the class-E PA heavily suffers from limitations by the output capacitance because $P_{out,1} = \omega C_S V_{dd}^2$ (for a duty cycle of 50%, [2]) with C_S the total switch capacitance and V_{dd} the supply voltage. On the one hand, the parasitic output capacitance of the transistor limits the maximum frequency for a given output power in low-power designs. On the other hand, the maximum realizable output capacitance by purposely adding a shunt capacitor limits the maximum output power for a given frequency. Class-D PAs do not have restrictions of this kind.

Potential of current-mode class-D PAs Both class-E and current-mode class-D (CMCD) PAs are capable of zero-voltage-switching, which means that the voltage across the switch is zero when it closes. Otherwise, the energy of $\frac{1}{2}C_{ds}V^2{}_{ds,off}$ gets dissipated at each switch closure, if C_{ds} is the parasitic output capacitance of the transistor and $V_{ds,off}$ is the voltage across the switch at that time [18]. Zero-voltage-switching however, can not be achieved by the voltage-mode class-D (VMCD) topology that has been nearly exclusively employed in practical class-D PAs up to date. The major advantage of the CMCD PA over both the class-E and VMCD PA is that it allows to accommodate the parasitic output capacitance C_{ds} into the shunt LC-tank at its output simply by subtracting C_{ds} from the tank capacitance. Moreover, CMCD PAs ideally feature a power output capability that is three times higher than for class-E PA which greatly reduces the thermal stress on the devices.

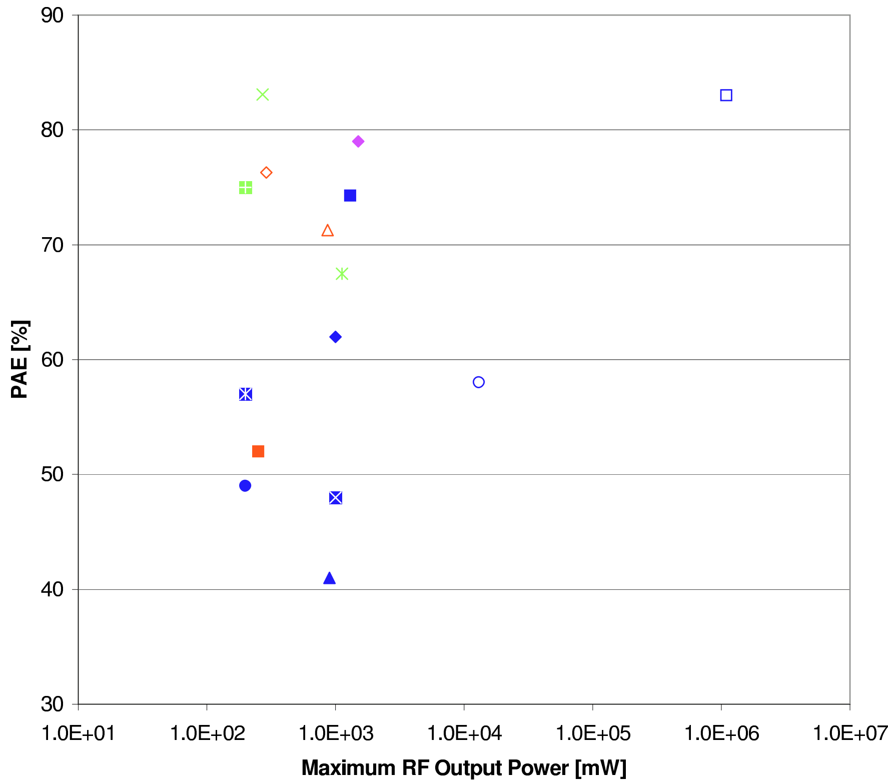
Because of these benefits, CMCD PAs have recently gained in research interest and spawned quite a few research publications [19, 18, 20, 21, 22, 23][1]. However, earlier works like [16, 24] have already dealt with CMCD PAs on a less practical basis. In 2001, H. Kobayashi et al. have reported the first CMCD PA for personal wireless communications in [18]: it features 71.3% PAE and 870mW output power at 900 MHz, uses GaAs MESFETs, and has been successfully applied to a GSM GMSK signal. In 2002, a high-power CMCD PA has been reported by A. Long et al.: it features 58% PAE and 13 W output power at 1 GHz, and uses LDMOS FETs.

To compare the performance of reported CMCD PAs with that of class-E PAs for personal wireless communications published since 1995, their PAE is plotted versus their maximum RF output power in Fig. 2.1. CMCD PAs seem to perform at least as well or slightly better than class-E PAs both in terms of the PAE and the maximum attainable RF output power. For further implementation details of the investigated PAs, refer to Tab. 2.1.

2.2 Research on Devices for Switching-Mode PAs

Device technologies for switching-mode PAs In switching-mode PAs, the transistors are employed as switches. Therefore, one may state that a device performs the better in a switching-mode PA the more it behaves like an ideal switch. Relevant parameters for transistors in switching-mode PAs are the on-resistance R_{on}, the off-resistance R_{off}, the rise time t_r, the fall time t_f, the breakdown voltage $BV_{ds,}$, the maximum allowable current $I_{ds,mr}$, and the parasitic output capacitance C_{ds}. Traditionally, transistors are employed as switches in digital applications. Therefore, well-established transistors intended for use as switches are available for these applications. However, the breakdown voltages of these devices are very low which makes them unsuitable for switching-mode PA applications demanding breakdown voltages way

[1]In some publications the current-mode class-D (CMCD) is also termed inverse class-F. In this report, current-mode class-D refers to a push-pull inverse class-F PA.



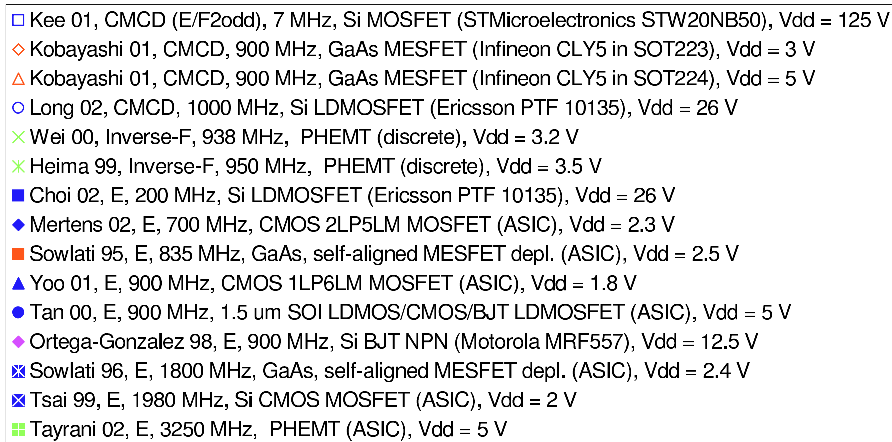


Figure 2.1: PAE versus the maximum RF output power for 15 switching-mode PAs [19, 18, 20, 21, 22, 5, 6, 7, 8, 9, 10, 11, 12, 13] (in this order) published since 1995. CMCD and inverse-F type PAs are designated by non-opaque markers. Class-E type PAs are designated by opaque markers. Blue markers designate MOSFET type, red makers MESFET type, green markers pHEMT type, and pink markers BJT type devices. For further implementation details, refer to Tab. 2.1.

Table 2.1: Performance figures and implementation details for 15 switching-mode PAs [19, 18, 20, 21, 22, 5, 6, 7, 8, 9, 10, 11, 12, 13] (in this order) published since 1995. For an illustration of the performance figures, refer to Fig. 2.1.

Design	Year	Class	Freq. [MHz]	Max. RF Output Power [mW]	PAE [%]	Gain [dB]	Supply Voltage [V]	Technology, Device, Transistor	Gate Length [µm]	Gate Width [mm]	Topology Remarks
Kee 01	2001	CMCD (E/F2odd)	7	1100000	83	17	125	Si MOSFET, STMicroelectr. STW20NB50	na	na	with third harmonic trap
Kobayashi 01	2001	CMCD	900	290	76.3	8.5	3	GaAs MESFET, Infineon CLY5 in SOT223	na	na	
Kobayashi 01	2001	CMCD	900	870	71.3	12	5	GaAs MESFET, Infineon CLY5 in SOT224	na	na	
Long 02	2002	CMCD	1000	13000	58	14	26	Si LDMOSFET, Ericsson PTF 10135	na	na	in- and output ratraces
Wei 00	2000	Inverse-F	938	272	83.1	12	3.2	PHEMT, discrete	na	2	
Heima 99	1999	Inverse-F	950	1122	67.5	9	3.5	PHEMT, discrete	0.5	17.5	
Choi 02	2002	E	200	1310	74.29	18.5	26	Si LDMOSFET, Ericsson PTF 10135	na	na	finite dc-feed inductance, 45% duty cycle
Mertens 02	2002	E	700	1000	62	18	2.3	CMOS 2LP5LM MOSFET, ASIC	0.35	na	differential, bondwire inductors, preceding class-C driver
Sowlati 95	1995	E	835	251	52	20	2.5	GaAs, self-aligned MESFET depl., ASIC	0.8	4	fully integrated with preceding class-F driver
Yoo 01	2001	E	900	900	41	15	1.8	CMOS 1LP6LM MOSFET, ASIC	0.25	na	two-stage, bondwire inductors, finite dc-feed inductance, common-gate switching
Tan 00	2000	E	900	200	49	16	5	1.5 µm SOI LDMOS/CMOS/ BJT LDMOSFET, ASIC	0.35	4.8	fully integrated with on-chip matching networks, preceding class-F driver
Ortega -Gonzalez 98	1998	E	900	1500	79	7.2	12.5	Si BJT NPN, Motorola MRF557	na	na	load-pull design
Sowlati 96	1996	E	1800	200	57	16	2.4	GaAs, self-aligned MESFET depl., ASIC	0.8	5	fully integrated with preceding class-F driver
Tsai 99	1999	E	1980	1000	48	20	2	Si CMOS MOSFET, ASIC	0.35	8.4	two-stage, differential, bondwire inductors, PAE=41% with microstrip balun
Tayrani 02	2002	E	3250	200	92	11	5	PHEMT, ASIC	0.3	1	fully integrated, broadband design, PAE>70% for 3.0-3.7 GHz

in excess of the supply voltage. For example the CMCD PA requires a breakdown voltage $BV_{ds} > \pi V_{dd}$ with V_{dd} the supply voltage. As there are no high-breakdown switching-optimized devices, switching-mode PA designers often use high-breakdown RF transistors with transition frequencies at least an order of magnitude higher than the operation frequency [24] for short switching times.

P. Mudge evaluates in chapter 4 of his UCSB MS thesis [25] five sample devices in different technologies for class-E PAs. Subsequently, he recommends the GaN HEMT and the AlGaAs/GaAs HBT for switching-mode PAs. However, he does not give a reference for the values he bases his conclusions on. R. Magoon draws more or less the same conclusions about device selection as P. Mudge in his UCSB MS thesis [26]. G. Wong investigates bipolar class-E PAs in his UCSB MS thesis [26] and recommends using HBT devices because of their high transit frequency f_T. D. Choi [2] on the other hand argues that topology issues matter more than technology issues and uses a Si LDMOS device throughout his UCSB Ph.D. thesis.

S.L. Delage et al. compare the GaAs HBT, GaAs HEMT, InP HEMT, AlGaN/GaN HEMT, and SiC MESFET with respect to PAE and output power for high-efficiency PAs in [27]. They conclude that the narrow-bandgap III-V devices like the GaAs HBT, GaAs HEMT, and InP HEMT are best suitable for *high-PAE medium output power* requirements whereas the wide-bandgap III-V devices like the AlGaN/GaN HEMT and SiC MESFET are best suitable for *medium-PAE high output power* requirements. They attribute the higher PAE of the GaAs and InP devices to the higher mobility ($\mu_{\text{GaAs}} = 8.5\mu_{\text{GaN, SiC}}$, $\mu_{\text{GaAs}} = 4.5\mu_{\text{GaN, SiC}}$) and thus to the higher transit frequency f_T of these devices compared to GaN and SiC. On the other hand, the higher RF output power of GaN and SiC may be attributed to the 4-10 times higher breakdown field compared to GaAs and InP. Further factors for the various technologies to consider are the wafer robustness, defect density (low for Si, medium for GaAs and InP, and very high for GaN), wafer cost, substrate resistivity, and thermal conductivity.

In [28] C.E. Weitzel investigates the Si LDMOS FET, GaAs MESFET, GaAs HBT and SiGe HBT for RF PAs and concludes that among those, the Si LDMOS FET has the lowest costs, the GaAs MESFET the highest PAE, the GaAs HBT the smallest die size and the SiGe HBT a somewhat lower PAE than the GaAs-based devices. Thus, no single technology dominates for RF PAs.

Y. Tkachenko et al. further show in [29] that pHEMT devices are more susceptible to hot electron degradation than MESFET devices. This of course favors a CMCD implementation with pHEMT devices over a class-E one as the former imposes less device stress.

Returning to Fig. 2.1, one may recognize the following technology trends:

- $PAE_{\text{pHEMT}} > PAE_{\text{BJT}} > PAE_{\text{MESFET}} > PAE_{\text{MOSFET}}$. However, note that no particular technology dominates clearly.
- While pHEMTs and MESFETs are comparable with respect to their output power, MOSFETs seem to deliver more output power though at a

generally lower PAE.

Relation of device parameters to PA performance figures Expressions for the PAE have been analytically derived for the class-E PA employing a Si LDMOS FET by D. Choi in [30], and for the VMCD PA employing complementary MOSFETs by J.S. Chang et al. in [31]. A. Inoue et al. conclude in [23] to move from the VMCD to the CMCD topology with an increasing gain compression (> 2 dB) and load resistance ($> 10\ \Omega$), and a decreasing on-resistance ($< 0.3\ \Omega$). However, no publication has so far analytically derived expressions for the PAE of a CMCD PA. Chapter 3 presents such an analysis for a CMCD PA employing MOSFET/LDMOS FET or HEMT/pHEMT devices.

2.3 Commercial PAs

Current status of commercial RF PAs Key players in the PA market for cellular telephony are RF Microdevices, Hitachi, Motorola, and Skyworks. In the cellular telephony handset PA market, one may recognize two trends:

- The share of PAs with GaAs HBTs is increasing whereas the share of PAs with Si LDMOS FET and especially GaAs MESFET devices is decreasing.
- Multi-chip modules (MCMs) that provide matching circuitry and antenna switches are rapidly gaining in share.

Skyworks employs InGaP/GaAs HBTs for their latest tri- and quad-band PAs. HBTs are also in use for PAs from RF Microdevices, Analog Devices, and Anadigics whereas Hitachi and Motorola favor the Si LDMOS devices for their PAs. Agilent on the other hand promotes its GaAs E-pHEMT technology because of its low current leakage, low on-resistance, and low threshold-voltage. E-pHEMTs employ a buried gate to allow the operation as enhancement-mode devices. Tab. 2.2 compares two state-of-the-art tri-band handset PAs by Skyworks and Agilent. Judging from these performance figures, the GaAs E-pHEMT of Agilent performs significantly better than the GaAs/InGaAs HBT of Skyworks. However, today's commercial PAs are linear-mode PAs in class-AB operation in all cases.

A commercial cellular telephony handset PA nowadays consists of up to 3 dies in a MCM. E. g. the Skyworks SKY77500 quad-band handset PA MCM contains the following dies besides the passive matching circuitry:

- A *GaAs/InGaAs die* incorporating a GSM850/ GSM900 block and a DCS1800/ PCS1900 block with the HBT devices.
- A *Si CMOS die* incorporating a PA control block and the interface circuitry.
- A *GaAs pHEMT die* with pHEMT switches to disable the PA in receive modes.

Table 2.2: Comparison of two state-of-the-art tri-band (GSM900, DCS1800, and PCS1900) handset PAs by Skyworks and Agilent.

Model	Skyworks CX77304-17		Agilent ACPM-7891	
Technology	GaAs/InGaAs HBT		GaAs E-pHEMT	
Figure	PAE	$P_{out,1}$	PAE	$P_{out,1}$
GSM900	55%	35 dBm	60%	35 dBm
DCS1800	50%	32.5 dBm	56%	32.5 dBm
PCS1900	50%	32.5 dBm	56%	32.5 dBm

Chapter 3

Device Evaluation by Analysis

3.1 Generic Power Amplifier Circuit and Class of Operation

Fig. 3.1 displays a generic power amplifier circuit. The analysis of this circuit presented in this section closely follows the one given by F. Raab in [32] and shows that the current-mode class-D PA is a special case of this generic power amplifier circuit. The results gained from the analysis of this generic power amplifier circuit form the basis for the derivation of an analytical model for the CMCD PA in the subsequent sections.

Generic power amplifier circuit In Fig. 3.1, the RF input signal V_{in} is fed through a DC block capacitor to the transistor gate (or base in case of a BJT). Both, the transistor gate and the transistor drain are biased through RF choke inductors. These RF choke inductors supply the DC currents $I_{g,bias}$ and I_{dd}. Because of the DC block capacitor at the output, the DC components of I_{ds} and V_{ds} are I_{dd} and V_{dd}, respectively. The current I_{tot} flows through a bandpass filter at the fundamental frequency. The fundamental Fourier component of I_{tot} is the output current I_{out} flowing into the load resistor R_L. The impedance $\mathbf{Z}$[1] seen into the bandpass filter is made up by the impedance of the bandpass filter itself and potentially by the impedances of additional stages for output matching. For the subsequent analysis, $\mathbf{Z}$ is assumed to include the reactance of the RF choke inductor, the DC block capacitor, and the output capacitance C_{ds} of M1. $\mathbf{Z}$ is further assumed to be linear and to be lossy only at the fundamental frequency and may, with these restrictions, be written as

[1] In this report, complex quantities like impedances (e. g. $\mathbf{Z}$) and complex amplitudes (e. g. $\mathbf{V}$ or $\mathbf{I}$) are written in bold letters. Real-valued amplitudes (e. g. $\hat{V}_{ds,ka}$ or $\hat{I}_{ds,ka}$) are denoted with a hat to distinguish them from time-dependent quantities. Peak values of time-dependent quantities are denoted with the subscript $_{pk}$ (e. g. $V_{ds,pk}$ or $I_{ds,pk}$). DC values are clear from their pertaining subscript (e. g. V_{dc} or V_{dd}).

$$\begin{array}{ll} \mathbf{Z}_1 = R_1 + jX_1 & \text{at the fundamental frequency, and} \\ \mathbf{Z}_k = jX_k,\ k > 1 & \text{at the harmonics.} \end{array} \tag{3.1}$$

The drain-source current I_{ds} is determined by $V_{g,bias}$ and V_{in} in conjunction with the transfer characteristic of M1 to the first order. The drain-source voltage V_{ds} then follows $I_{tot} = I_{dd} - I_{ds}$ and the impedances Z_1 and Z_k presented to I_{tot} at the fundamental frequency and at the harmonics, respectively. V_{ds} and I_{ds} may be written as general Fourier series

$$V_{ds}(\theta) = V_{dd} + \sum_{k=1}^{\infty} \left(\hat{V}_{ds,ka} \cos(k\theta) + \hat{V}_{ds,kb} \sin(k\theta) \right)$$

$$I_{ds}(\theta) = I_{dd} + \sum_{k=1}^{\infty} \left(\hat{I}_{ds,ka} \cos(k\theta) + \hat{I}_{ds,kb} \sin(k\theta) \right)$$

with $\theta = \omega t$ and $\hat{V}_{ds,ka}$, $\hat{I}_{ds,ka}$ and $\hat{V}_{ds,kb}$, $\hat{I}_{ds,kb}$ the in-phase and quadrature-phase Fourier coefficients, respectively. In complex notation, the above relations may be written equivalently as

$$\begin{array}{ll} V_{ds}(\theta) = V_{dd} + \sum_{k=1}^{\infty} \mathrm{Re}\left(\mathbf{V}_k e^{jk\theta}\right), & \mathbf{V}_k = \hat{V}_{ds,ka} - j\hat{V}_{ds,kb} \\ I_{ds}(\theta) = I_{dd} + \sum_{k=1}^{\infty} \mathrm{Re}\left(\mathbf{I}_k e^{jk\theta}\right), & \mathbf{I}_k = \hat{V}_{ds,ka} - j\hat{V}_{ds,kb} \end{array}$$

with $\mathbf{V}_k$ and $\mathbf{I}_k$ the complex voltage and current amplitudes at the k'th frequency. $\mathbf{V}_k$ and $\mathbf{I}_k$ are related by the impedances given in (3.1):

$$\mathbf{V}_k = \mathbf{Z}_k \mathbf{I}_k$$

Therefore, if the waveform of I_{ds} is given, the waveform of V_{ds} follows from the above equation.

Class of operation The class of operation of a power amplifier, denoted by the letters A, B, AB, C, D, E, F, etc, may be determined from the general shape of the drain-source voltage and current waveforms. As evident from the previous paragraph, the general shape of the drain-source voltage and current waveforms depends on

- $V_{g,bias}$ and V_{in} in conjunction with the transfer characteristic of the transistor, as well as on
- the harmonic termination $\mathbf{Z}_k$ at the transistor drain.

As F. Raab points out in [32], for inverse class-F operation, the even-harmonic reactances X_k, $k > 1$ even, must be high and the odd-harmonic reactances X_k, $k > 1$ odd, must be low. For this harmonic termination in conjunction with the assumption of an ideal switch for M1 in Fig. 3.1, the drain-source voltage is

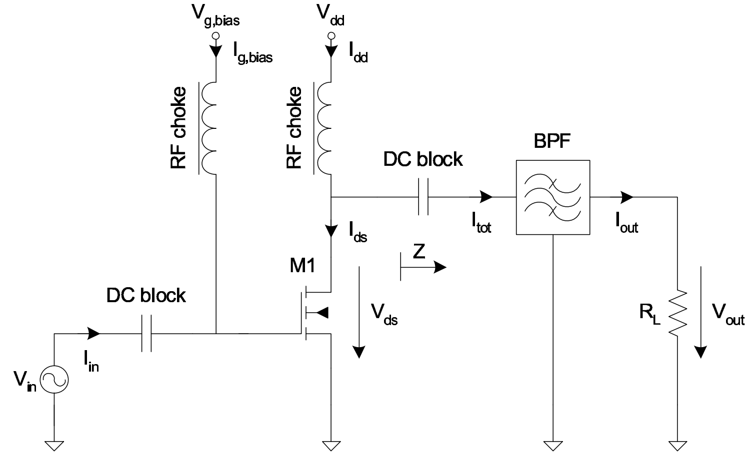


Figure 3.1: Generic power amplifier circuit with a FET as active device.

shaped towards a half-sine wave and the drain-source current towards a square wave as depicted in Fig. 3.2. Not surprisingly, a Fourier-analysis of a half-sine wave reveals that it only contains even harmonics besides the fundamental and a DC component. Doing the same for a square wave shows that it only contains odd harmonics besides the fundamental and a DC component. Fig. 3.3 (reproduced from [32]) provides a broader perspective on the proper harmonic termination for various PA classes. The figure suggests that e. g. for a class-F PA the proper harmonic termination is short at even harmonics and open at odd harmonics which results in a square wave for V_{ds} and a half-sine wave for I_{ds}.

The current-mode class-D PA is the push-pull version of an inverse class-F PA and is analyzed on grounds of the results for an inverse class-F PA in the subsequent sections. As will be shown, the proper harmonic termination is the same as for the inverse class-F PA (open at even harmonics, short at odd harmonics) and is provided inherently in the ideal CMCD PA. However, proper harmonic termination is a major issue in the implementation of a CMCD PA.

3.2 Analysis of Class-D PAs

3.2.1 Transformer-Coupled Class-D PAs

Traditionally, the class-D PA circuits found in literature [16] are the transformer-coupled current-mode class-D (CMCD) PA and the transformer-coupled voltage-mode class-D (VMCD) PA as shown in Fig. 3.4 and 3.5, respectively. These circuits consist of two switching devices, of a RLC tank resonant at the fundamental frequency, and of an output balun transformer. The output balun transformer converts the differential (balanced) voltages across the switching devices

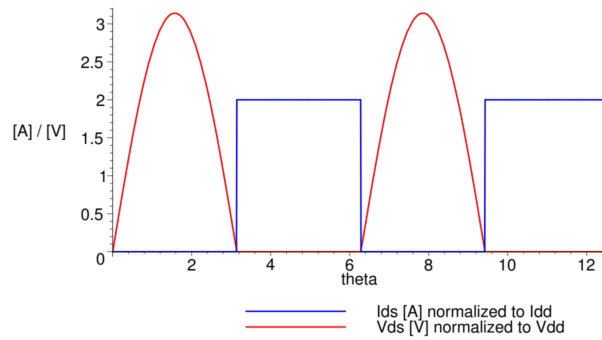


Figure 3.2: Ideal waveforms for the drain-source voltage V_{ds} and current I_{ds} of an inverse class-F PA.

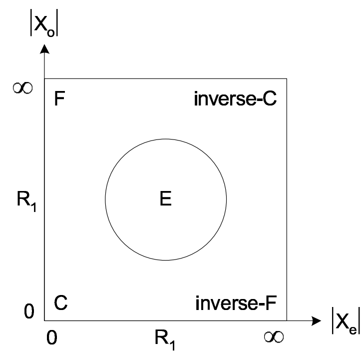


Figure 3.3: Proper harmonic termination for class-F, inverse class-F, class-C, inverse class-C, and class-E PAs as a function of the even harmonics $|X_e|$ and odd harmonics $|X_o|$ (reproduced from [32]).

to a single-ended (unbalanced) voltage across the RLC tank. Fig. 3.6 shows the voltages and currents in a general balun transformer. The two switching devices are driven by inverse signals. This inversion is performed by the input balun transformer. The difference between the CMCD PA and the VMCD PA is the biasing of the output-transformer center tap and the RLC tank configuration. The CMCD PA shows a constant center tap current I_{dd} and employs a parallel RLC tank, whereas the VMCD PA shows a constant center tap voltage V_{dd} and employs a series RLC tank.

The CMCD PA is in fact a push-pull version of the inverse class-F PA, and the VMCD PA a push-pull version of the class-F PA. The proper harmonic termination (open at even harmonics and short at odd harmonics for the CMCD PA, short at even harmonics and open at odd harmonics for the VMCD PA) is provided by the push-pull operation in conjunction with the RLC tanks. In case of the CMCD PA, the RF choke inductor supplies a constant current I_{dd}. Because of the push-pull operation, the drain-source currents through the switching devices are square waves with peak values of 0 and I_{dd}. The current through the parallel RLC tank then is $I_{tot} = \frac{m}{n}\left(I_{ds2} - I_{ds1}\right)$, a square wave with peak values of $-I_{dd}$ and I_{dd}. The parallel RLC tank shorts all harmonics of I_{tot} and ideally just leaves the fundamental frequency of I_{tot}. Therefore, V_R is a sine wave. This sine wave is then transformed back to the left of the output balun transformer and makes V_{ds1} and V_{ds2} look like half sine waves. The resulting drain-source waveforms for a CMCD PA are shown in Fig. 3.9. The waveforms of a VMCD PA may be derived in a similar fashion; the drain-source voltage is a square wave and the current a half sine.

Generally, the parasitic parallel capacitance C_{ds} across the drain-source terminals is much more pronounced than the parasitic series inductance L_d at the drain terminal [18]. This leads to an energy dissipation of $\frac{1}{2}C_{ds}V^2{}_{ds,off}$ whenever the switch closes, if $V_{ds,off}$ is the drain-source voltage at that time. To minimize this energy dissipation, ideally $V_{ds,off}$ must be 0 which is called zero voltage switching (ZVS). The above discussion of the CMCD and VMCD waveforms reveals that the CMCD topology achieves ZVS whereas the VMCD topology does not achieve ZVS. This greatly favors the use of the CMCD circuit over the VMCD circuit. Moreover, the CMCD circuit allows to accommodate C_{ds} into the RLC tank as part of the tank capacitance.

A major drawback of the transformer-coupled CMCD PA as shown in Fig. 3.5 is its linearity requirements for the output balun transformer which make it unsuitable for high-frequency applications. The output balun transformer in the transformer-coupled CMCD PA is required to be linear at least from DC to three times the fundamental frequency if I_{tot} should look like a square wave. Realizing balun transformers for high-frequency applications satisfying this requirement is next to impossible. Therefore, the output balun transformer is moved to the right of the parallel RLC tank which confines the linearity requirement to a narrow band at the fundamental frequency. This CMCD PA, subsequently termed shunt-tank CMCD PA, is investigated in the next section.

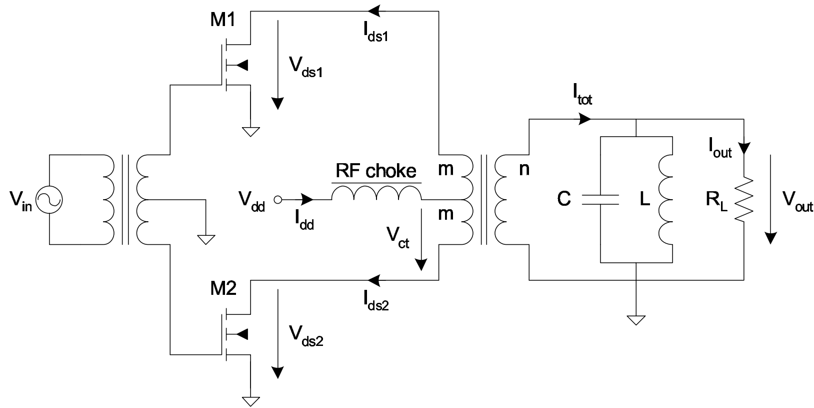


Figure 3.4: Circuit of a transformer-coupled CMCD (current-mode class-D) PA.

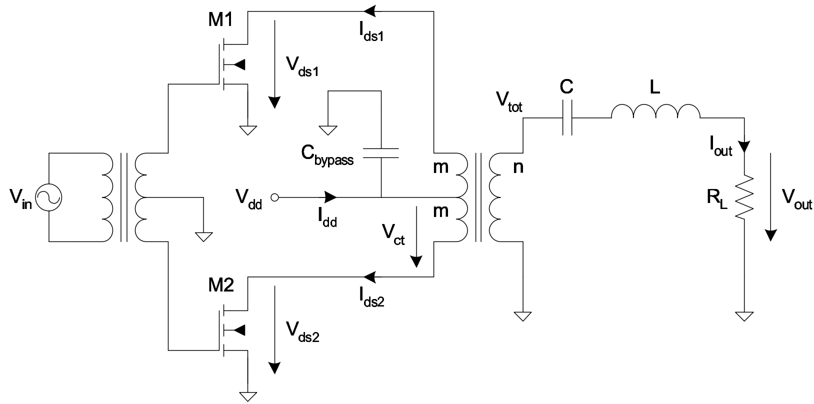


Figure 3.5: Circuit of a transformer-coupled VMCD (voltage-mode class-D) PA.

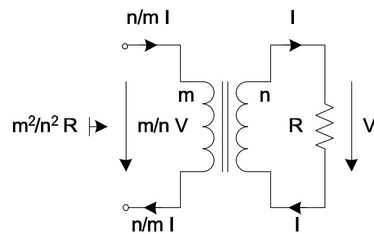


Figure 3.6: Voltages and currents in a general balun transformer.

3.2.2 Shunt-Tank Current-Mode Class-D PA

3.2.2.1 Ideal Waveform Operation

The shunt-tank CMCD PA is shown in Fig. 3.7. The output balun transformer that transforms the differential (balanced) voltage across the parallel LC tank to the single-ended (unbalanced) voltage across the load resistor R_L is omitted in Fig. 3.7 for simplicity. The output balun transformer is shown separately in Fig. 3.8. Therefore, R in Fig. 3.7 represents the transformed resistance of the load resistor R_L. The two switching devices M1 and M2 are driven by two inverse signals $V_{in}^- = -V_{in}$ and $V_{in}^+ = V_{in}$, respectively.

Derivation of waveforms For this analysis of the shunt-tank CMCD PA, the switching devices are assumed to be ideal switches. M1 turns on when $V_{in}^- > 0$ and turns off when $V_{in}^- < 0$, whereas M2 turns on when $V_{in}^+ > 0$ and turns off when $V_{in}^+ < 0$. If V_{in} is a sine, M1 conducts during the negative half cycle of V_{in}, whereas M2 conducts during the positive half cycle of V_{in}. Therefore, the current I_{tot} through the parallel RLC tank is a square wave with peak values of $-I_{dc}$ and I_{dc}.

$$I_{tot}(\theta) = I_{dc} sq(\theta) \tag{3.2}$$

$$sq(\theta) = \begin{cases} 1 & \sin(\theta) > 0 \\ -1 & \sin(\theta) < 0 \end{cases} = \frac{4}{\pi}\left(\sin(\theta) + \frac{1}{3}\sin(3\theta) + \frac{1}{5}\sin(5\theta) + \dots\right)$$

If one assumes that the parallel RLC tank shorts all harmonics of I_{tot}, the voltage V_R across the tank resistor becomes:

$$V_R(\theta) = \hat{V}_R \sin(\theta)$$

$$\hat{V}_R = R I_{dc} \frac{4}{\pi} \tag{3.3}$$

The waveforms of $I_{tot}(\theta)$ and $V_R(\theta)$ are shown in Fig. 3.10. It remains to derive I_{dc}. Due to the DC feed inductors, the average drain voltages of M1 and M2 must be V_{dd}:

$$\frac{1}{2\pi}\int_0^{\pi} \hat{V}_R \sin(\theta) d\theta = \frac{1}{\pi}\hat{V}_R = V_{dd} \Rightarrow \hat{V}_R = \pi V_{dd} \tag{3.4}$$

Solving (3.3)=(3.4) for I_{dc} yields:

$$I_{dc} = \frac{\pi^2}{4}\frac{V_{dd}}{R} \tag{3.5}$$

The drain-source currents I_{ds1} and I_{ds2} are square waves with peak values of 0 and $2I_{dc}$ as depicted in Fig. 3.9. For the drain-source voltages V_{ds1} and V_{ds2}, the on-state must be distinguished from the off-state. For the on-state, the drain-source voltage of the pertaining switch is 0. For the off-state, the

drain-source voltage is a sine with a peak value of $\hat{V}_R$ as the full tank voltage drops between the drain and source. Therefore, the drain-source voltages V_{ds1} and V_{ds2} are half sine waves as shown in Fig. 3.9. With (3.2) and the Fourier series of a half sine wave, the drain-source voltages and currents may be written as follows:

$$V_{ds1}(\theta) = V_{dd} + \frac{\pi}{2} V_{dd} \sin(\theta) - \frac{2}{2^2-1} V_{dd} \cos(2\theta) - \frac{2}{4^2-1} V_{dd} \cos(4\theta) - \frac{2}{6^2-1} V_{dd} \cos(6\theta) - \ldots$$

$$I_{ds1}(\theta) = I_{dc} - I_{tot}(\theta) = I_{dc} - \frac{4}{\pi} I_{dc} \sin(\theta) - \frac{4}{3\pi} I_{dc} \sin(3\theta) - \frac{4}{5\pi} I_{dc} \sin(5\theta) - \ldots$$

$$V_{ds2}(\theta) = V_{dd} - \frac{\pi}{2} V_{dd} \sin(\theta) - \frac{2}{2^2-1} V_{dd} \cos(2\theta) - \frac{2}{4^2-1} V_{dd} \cos(4\theta) - \frac{2}{6^2-1} V_{dd} \cos(6\theta) - \ldots$$

$$I_{ds2}(\theta) = I_{dc} + I_{tot}(\theta) = I_{dc} + \frac{4}{\pi} I_{dc} \sin(\theta) + \frac{4}{3\pi} I_{dc} \sin(3\theta) + \frac{4}{5\pi} I_{dc} \sin(5\theta) + \ldots$$

Note that corresponding harmonics of V_{ds1} and V_{ds2} are the same in amplitude and phase which provides an open-circuit at all even harmonics. Further note that corresponding harmonics of I_{ds1} and I_{ds2} are the same in amplitude but shifted by 180° in phase which provides a short-circuit at all odd harmonics. Therefore, the push-pull operation of a CMCD PA provides exactly the correct harmonic termination for inverse class-F operation. However, the output balun transformer is assumed to be ideal here. Real output balun transformer do not usually provide perfect isolation to ground at the even harmonics.

Efficiency Having established the above relations it is straight-forward to calculate the drain-efficiency:

$$P_{out,1} = \frac{1}{2} \frac{\hat{V}_R^2}{R} = \frac{\pi^2}{2} \frac{V_{dd}^2}{R} \tag{3.6}$$

$$P_{dc} = V_{dd} 2 I_{dc} = \frac{\pi^2}{2} \frac{V^2{}_{dd}}{R}$$

$$\eta = \frac{P_{out,1}}{P_{dc}} = 1$$

Note that the drain-efficiency is 100% for a CMCD PA when the ideal waveforms of Fig. 3.9 are assumed. The output power capability P_{max} for the CMCD PA is:

$$P_{max} = \frac{P_{out,1}}{V_{ds,pk} I_{ds,pk}} = \frac{P_{out,1}}{\pi V_{dd} 2 I_{dc}} = \frac{1}{\pi} = 0.318$$

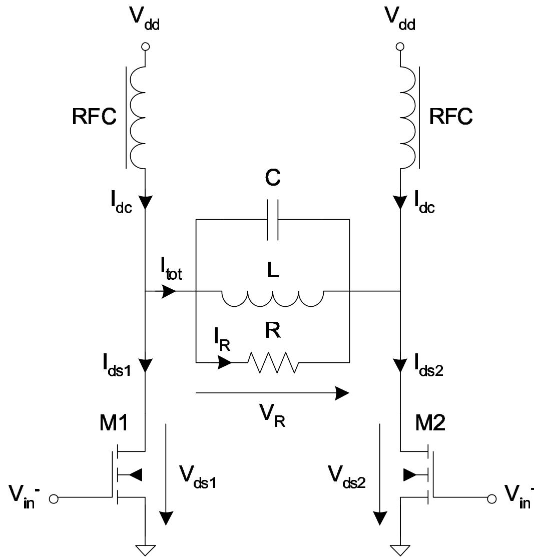


Figure 3.7: Basic circuit of a shunt-tank CMCD PA.

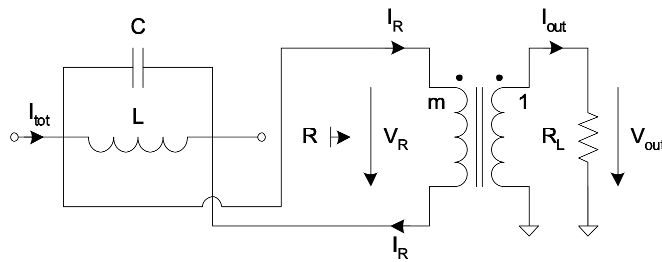


Figure 3.8: Tank circuit of the shunt-tank CMCD PA of Fig. 3.7 with output balun transformer. The transformation ratio must be $m = \sqrt{\frac{R}{R_L}}$.

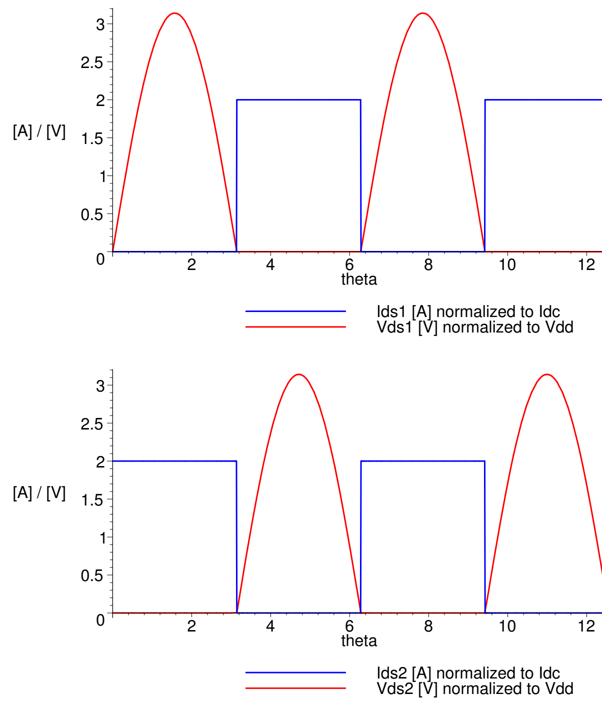


Figure 3.9: Ideal waveforms for the drain-source voltages V_{ds1}, V_{ds2}, and currents I_{ds1}, I_{ds2} of a CMCD PA.

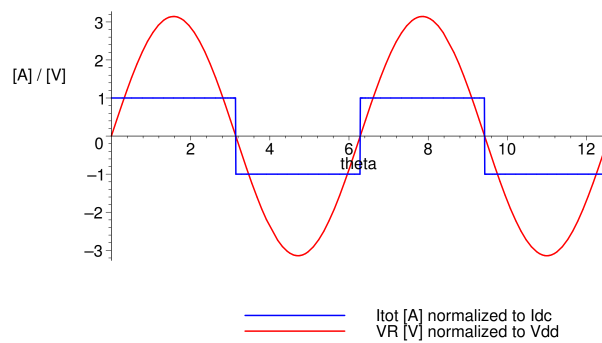


Figure 3.10: Ideal waveforms for the tank current I_{tot} and the load resistor voltage V_R of a CMCD PA.

3.2.2.2 Spectrum-Limited Waveform Operation

Derivation of waveforms The ideal waveforms of Fig. 3.9 suggest that no power is dissipated in the switching devices. At all times, either V_{ds} or I_{ds} is zero, which results in a drain efficiency of 100%. For real switching devices however, one may assume that V_{ds} and I_{ds} are spectrum-limited because of parasitic elements acting as low-pass filters. Therefore, limiting the harmonics of V_{ds} and I_{ds} to the third order better reflects the real waveforms than assuming an infinite spectrum and eases the analysis. A Fourier-analysis of the I_{ds1} square wave reveals that it only contains odd harmonics. Doing the same for the V_{ds1} half sine shows that this waveform only contains even harmonics. Therefore, the spectrum-limited waveforms for V_{ds1} and I_{ds1} may be written as follows:

$$V_{ds1}(\theta) = V_{dd} + \hat{V}_{ds1,1}\sin(\theta) - \hat{V}_{ds1,2}\cos(2\theta)$$

$$I_{ds1}(\theta) = I_{dc} - \hat{I}_{ds1,1}\sin(\theta) - \hat{I}_{ds1,3}\sin(3\theta)$$

The coefficients $\hat{V}_{ds1,1}$, $\hat{V}_{ds1,2}$ and $\hat{I}_{ds1,1}$, $\hat{I}_{ds1,3}$ may be determined by assuming maximally flat waveforms [33]. For a maximally flat waveform, all derivatives are zero at the waveform minimum. The minimum for $V_{ds1}(\theta)$ occurs at $\theta = \frac{3\pi}{2}$. Note that the odd-order derivatives of $V_{ds1}(\theta)$ are inherently zero at this point. Therefore, it is sufficient to require that $V_{ds1}(\frac{3\pi}{2}) = 0$ and $\frac{\partial^2 V_{ds1}}{\partial t^2}(\frac{3\pi}{2}) = 0$ (as also done in [33] and [18]). The first condition yields $\hat{V}_{ds1,1} = \frac{4}{3}V_{dd}$ whereas the second one results in $\hat{V}_{ds1,2} = \frac{1}{4}\hat{V}_{ds1,1} = \frac{1}{3}V_{dd}$. The minimum for $I_{ds1}(\theta)$ occurs at $\theta = \frac{\pi}{2}$ and the odd-order derivatives of $I_{ds1}(\theta)$ are again inherently zero at this point. Therefore, it is sufficient to require that $I_{ds1}(\frac{\pi}{2}) = 0$ and $\frac{\partial^2 I_{ds1}}{\partial t^2}(\frac{\pi}{2}) = 0$. Here, the first condition results in $\hat{I}_{ds1,3} = \frac{1}{8}I_{dc}$ whereas the second one yields $\hat{I}_{ds1,1} = 9\hat{I}_{ds1,3} = \frac{9}{8}I_{dc}$. The full expressions for the drain-source voltages and currents therefore are:

$$V_{ds1}(\theta) = V_{dd} + \frac{4}{3}V_{dd}\sin(\theta) - \frac{1}{3}V_{dd}\cos(2\theta)$$

$$I_{ds1}(\theta) = I_{dc} - \frac{9}{8}I_{dc}\sin(\theta) - \frac{1}{8}I_{dc}\sin(3\theta) \tag{3.7}$$

$$V_{ds2}(\theta) = V_{dd} - \frac{4}{3}V_{dd}\sin(\theta) - \frac{1}{3}V_{dd}\cos(2\theta)$$

$$I_{ds2}(\theta) = I_{dc} + \frac{9}{8}I_{dc}\sin(\theta) + \frac{1}{8}I_{dc}\sin(3\theta) \tag{3.8}$$

Fig. 3.11 plots the above waveforms. I_{dc} remains as an unknown in the above equations. If one again assumes that the parallel RLC tank shorts all

harmonics of $I_{tot}(\theta) = I_{ds2}(\theta) - I_{dc}$, then $V_R(\theta) = R\frac{9}{8}I_{dc}\sin(\theta)$. Equating this result to $V_R(\theta) = V_{ds1}(\theta) - V_{ds2}(\theta)$ yields for I_{dc}:

$$I_{dc} = \frac{64}{27}\frac{V_{dd}}{R}$$

$$\Rightarrow \hat{V}_R = \frac{8}{3}V_{dd} \approx 2.67V_{dd} \tag{3.9}$$

Efficiency Having established the above relations it is straight-forward to calculate the drain-efficiency:

$$P_{out,1} = \frac{1}{2}\frac{\hat{V}_R^2}{R} = \frac{32}{9}\frac{V_{dd}^2}{R} \tag{3.10}$$

$$P_{dc} = V_{dd}2I_{dc} = \frac{128}{27}\frac{V_{dd}^2}{R}$$

$$\eta = \frac{P_{out,1}}{P_{dc}} = 0.75$$

The drain-efficiency drops from 100% for the ideal waveforms to 75% for the spectrum-limited waveforms. Evidently, the drain-efficiency must be lower than 100% for the spectrum-limited waveforms as the drain-source voltages and currents overlap when the devices are switching on and off. This causes a power dissipation in the switching devices. The output power capability P_{max} for the spectrum-limited waveforms is:

$$P_{max} = \frac{P_{out,1}}{V_{ds,pk}I_{ds,pk}} = \frac{P_{out,1}}{\frac{8}{3}V_{dd}2I_{dc}} = \frac{9}{32} = 0.281$$

3.2.2.3 Tank Design Equations

Relevant design variables to determine the capacitance, inductance, and resistance of the parallel RLC tank are:

- the off-state drain-source breakdown voltage of the switching devices $BV_{ds,off}$
- the design output power $P_{out,1,design}$,
- the mid-band frequency f_0,
- the relative bandwidth $B_r = \frac{B}{f_0}$ with B the absolute bandwidth,
- the maximum current rating of the used inductor $I_{L,mr}$ and of the capacitor $I_{C,mr}$, and
- the quality factor of the used inductor Q_L and of the used capacitor Q_C.

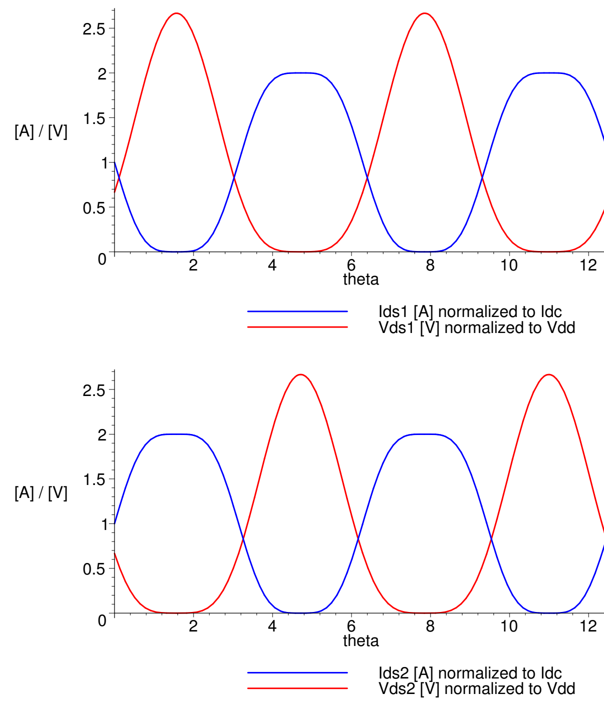


Figure 3.11: Spectrum-limited waveforms for the drain-source voltages V_{ds1}, V_{ds2}, and currents I_{ds1}, I_{ds2} of a CMCD PA.

According to (3.9) the peak drain-source voltage of the switching device is $2.67V_{dd}$. Therefore, the designer has to make sure that $BV_{ds,off} > 2.67V_{dd}$. Having set the supply voltage V_{dd} satisfying the former inequality, the total tank resistance R may be determined from the design output power $P_{out,1,design}$ according to (3.10):

$$R = \frac{32}{9}\frac{V_{dd}^2}{P_{out,1,design}} \tag{3.11}$$

It is important to note that the tank resistance R consists of the parallel combination of the equivalent inductor parallel resistance R_{pL}, the equivalent capacitor parallel resistance R_{pC}, and the resistance R_{load} seen by the parallel LC tank looking into the output balun transformer.

The loaded quality factor of the parallel RLC tank Q_{loaded} is determined by the relative bandwidth B_r and the maximum current rating of the inductor and capacitor. According to [17], $Q_{loaded} = \frac{1}{B_r}$ if $B_r \ll 1$. Therefore, one may require that $Q_{loaded} < \frac{1}{B_r}$, an inequality that is often readily satisfied. However, again according to [17], the absolute current through the inductor at resonance is $|I_L| = \frac{|V_R|}{\omega_0 L} = \frac{R|I_{tot}|}{\omega_0 L} = Q_{loaded}\,|I_{tot}|$, and the one through the capacitor at resonance is $|I_C| = \omega_0 C\,|V_R| = \omega_0 CR\,|I_{tot}| = Q_{loaded}\,|I_{tot}|$. Therefore, with a peak I_{tot} of I_{dc} and a maximum current rating of $I_{L,mr}$ for the inductor and of $I_{C,mr}$ for the capacitor, one has to require that

$$Q_{loaded} < \min\left(\frac{I_{L,mr}}{I_{dc}}, \frac{I_{C,mr}}{I_{dc}}\right)$$

A reasonable strategy for choosing a Q_{loaded} is to use a value close to $\min\left(\frac{I_{L,mr}}{I_{dc}}, \frac{I_{C,mr}}{I_{dc}}\right)$ because a higher Q_{loaded} makes a better short-circuit for the harmonics in I_{tot}. Moreover, the minimum realizable tank inductance L_{min} may limit Q_{loaded} as well.

$$Q_{loaded} < \frac{R}{\omega_0 L_{min}}$$

Having chosen a suitable value for Q_{loaded} it is straight-forward to determine the capacitance and inductance:

$$C = \frac{Q_{loaded}}{\omega_0 R}$$

$$L = \frac{1}{\omega_0^2 C}$$

As $R = R_{pL} \| R_{pC} \| R_{load}$, $G_{load} = G - G_{pL} - G_{pC}$ if G_{load}, G, G_{pL}, and G_{pC} are the corresponding conductances. Using the equations

$$Q_L = \frac{\omega_0 L}{R_{sL}} \approx \frac{R_{pL}}{\omega_0 L} \quad \text{and} \quad Q_C = \frac{1}{\omega_0 C R_{sC}} \approx \omega_0 C R_{pC}$$

(valid if $Q_L \gg 1$ and $Q_C \gg 1$) with R_{sL}, R_{sC} the equivalent series resistances, and R_{pL}, R_{pC} the equivalent parallel resistances, yields for the conductance G_{load} seen by the parallel LC tank looking into the output balun transformer:

$$G_{load} = \frac{1}{R} - \omega_0 C \left(\frac{1}{Q_L} + \frac{1}{Q_C} \right)$$

With $R_{load} = \frac{1}{G_{load}}$, all elements of the parallel RLC tank are specified.

3.3 Analytical Derivation of the PAE for a FET Device

In order to identify the device parameters with a large impact on the PAE, analytical expressions for the input, output, and DC power as well as for the drain-efficiency and PAE are derived. As a first step, the PAE is derived for a MOSFET device and later adapted to a HEMT device. The analytical expressions allow a fast and straight-forward sensitivity analysis that identifies the most relevant device parameters for a CMCD PA. The MOSFET equivalent circuit, the input power expression, and the derivation of the drain-source voltage during the positive half cycle are strongly based on the analysis by D. Choi done for a class-E PA in [30].

3.3.1 Analytical Derivation of the Input, Output, and DC Power for a MOSFET Device

3.3.1.1 Equivalent Circuit and Non-ideal Waveforms

The equivalent large-signal model for a shunt-tank CMCD circuit of Fig. 3.7 is depicted in Fig. 3.12 for MOSFETs as switching devices. The MOSFET large-signal model includes a voltage-dependent current source as well as parasitic resistors and parasitic capacitors. R_g and R_s model the intrinsic gate and intrinsic source resistance, respectively, C_{gs} the gate-source capacitance, C_{gd} the gate-drain capacitance, and C_{ds} the output capacitance. Note that C_{gs} and C_{ds} bypass R_s and directly connect to the ground potential to simplify the subsequent analysis.

The voltage-dependent current sources I_{ds1} and I_{ds2} model the DC output characteristic of the transistors. Fig. 3.13 shows the simulated DC output characteristic of a Motorola MRF21010S LDMOS FET. We anticipate that the FET operates in its triode region during the on-state and in its cut-off region during the off-state. For the on-state, V_{ds} does not drop to 0 but remains at a voltage V_{dsmin} that depends on the imposed $I_{ds} = 2I_{dc}$ and the defined gate-drive V_{gs}.

V_{dsmin} must therefore be accounted for in the spectrum-limited waveforms derived in section 3.2.2.2. Moreover, the drain-source current flows through R_s in the model of Fig. 3.12 thereby provoking a voltage drop that adds to V_{dsmin} in

Figure 3.12: Equivalent large-signal model for the shunt-tank CMCD circuit of Fig. 3.7 for MOSFETs as switching devices.

Figure 3.13: Simulated DC output characteristic of a Motorola MRF21010S LDMOS FET with the anticipated on- and off-states for an imposed I_{ds} of 1 A and for a defined gate-drive V_{gs} of 5.5 V. The breakdown voltage for this device is 65 V.

the drain-ground voltage. To derive the spectrum-limited drain-ground current and voltage waveforms accounting for these two effects, the current waveforms are assumed to remain the same as in (3.7) and (3.8) as a first order approximation: $I_{d1}(\theta) = I_{ds1}(\theta)$ and $I_{d2}(\theta) = I_{ds2}(\theta)$. The drain-ground voltage waveform for transistor M1 is derived as follows:

$$V_{d1}(\theta) = \hat{V}_{d1,0} + \hat{V}_{d1,1}\sin(\theta) - \hat{V}_{d1,2}\cos(2\theta) - R_s I_{d1}(\theta)$$

Because the drain voltage must be V_{dd} on the average, $\hat{V}_{d1,0} = V_{dd} + R_s I_{dc}$. To determine the remaining coefficients for maximally flat waveforms it is reasonable to require that $V_{d1}(\frac{3\pi}{2}) = V_{dsmin} + R_s I_{d1}(\frac{3\pi}{2})$ and $\frac{\partial^2 V_{ds1}}{\partial t^2}(\frac{3\pi}{2}) = 0$. The first condition yields $\hat{V}_{d1,2} = \frac{1}{3}(V_{dd} - V_{dsmin} - R_s I_{dc})$, whereas the second one results in $\hat{V}_{d1,1} = 4\hat{V}_{d1,2} = \frac{4}{3}(V_{dd} - V_{dsmin} - R_s I_{dc})$. The full expressions for the drain-ground voltages therefore are:

$$\begin{aligned} V_{d1}(\theta) &= V_{dd} + \tfrac{4}{3}(V_{dd} - V_{dsmin} - R_s I_{dc})\sin(\theta) - \tfrac{1}{3}(V_{dd} - V_{dsmin} - R_s I_{dc})\cos(2\theta) \\ &\quad -\tfrac{9}{8}R_s I_{dc}\sin(\theta) - \tfrac{1}{8}R_s I_{dc}\sin(3\theta) \end{aligned} \tag{3.12}$$

$$\begin{aligned} V_{d2}(\theta) &= V_{dd} - \tfrac{4}{3}(V_{dd} - V_{dsmin} - R_s I_{dc})\sin(\theta) - \tfrac{1}{3}(V_{dd} - V_{dsmin} - R_s I_{dc})\cos(2\theta) \\ &\quad +\tfrac{9}{8}R_s I_{dc}\sin(\theta) + \tfrac{1}{8}R_s I_{dc}\sin(3\theta) \end{aligned} \tag{3.13}$$

Fig. 3.14 plots the voltage and current waveforms according to these equations. I_{dc} may again be derived by equating $V_R(\theta) = R\frac{9}{8}I_{dc}\sin(\theta)$ to $V_R(\theta) = V_{ds1}(\theta) - V_{ds2}(\theta)$. A first order approximation of I_{dc} is:

$$I_{dc} = \frac{64\,(V_{dd} - V_{dsmin})}{27R + 118R_s} \tag{3.14}$$

3.3.1.2 Input Power

The input power for the circuit of Fig. 3.12 may be derived in the same way as done by D. Choi in [30]. The following shortly presents the basic ideas of the input power derivation; for the full derivation, refer to [30]. The input waveform is assumed to be a sine: $V_{in} = \hat{V}_{in}\sin(\theta)$. The equivalent complex amplitude is $\mathbf{V}_{in} = \hat{V}_{in}e^{j0}$. The input power for the positive half cycle and the negative half cycle of the sine has to be derived separately:

Positive half cycle $0 \leq \theta < \pi$ The input power for the positive half cycle may be calculated as $P_{in,pos} = \frac{1}{4}\mathrm{Re}\left[\mathbf{V}_{in}\mathbf{I}^*_{in}\right]$ with $\mathbf{I}^*_{in}$ the complex-conjugate of $\mathbf{I}_{in}$. If one assumes that the drain-voltage remains constant as a first order approximation during the positive half cycle, then the input impedance my be written as

$$\mathbf{Z}_{in} = R_g + \frac{1}{j\omega\,(C_{gs,pos} + C_{gd,pos})} \tag{3.15}$$

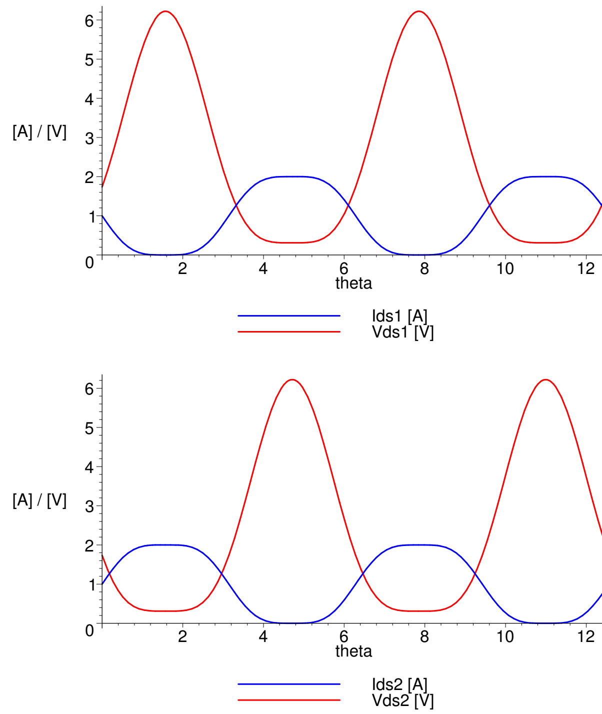


Figure 3.14: Non-ideal waveforms for the drain-ground voltages V_{d1}, V_{d2}, and currents I_{d1}, I_{d2} of a CMCD PA according to (3.12) and (3.13) for $V_{dd} = 2.5\,\text{V}$, $V_{dsmin} = 0.1\,\text{V}$, $R_s = 1\,\Omega$, and $R = 50\,\Omega$.

As $\mathbf{I}_{in} = \frac{\mathbf{V}_{in}}{\mathbf{Z}_{in}}$, the input power for the positive half cycle may now be derived as:

$$P_{in,pos} = \frac{\hat{V}_{in}^2}{4} \frac{\omega^2 R_g \left(C_{gs,pos} + C_{gd,pos}\right)^2}{1 + \left[\omega R_g \left(C_{gs,pos} + C_{gd,pos}\right)\right]^2} \tag{3.16}$$

Since the MOSFET is assumed to operate in its triode region for the positive half cycle, one may approximate $C_{gs,pos}$ and $C_{gd,pos}$ as

$$C_{gs,pos} = C_{gd,pos} = \frac{1}{2} FWLC_{ox} + FWC_{ov}$$

F, W, and L are the number of fingers, the finger-width, and the channel-length, respectively.

Negative half cycle $\pi \leq \theta < 2\pi$ The input power for the negative half cycle is $P_{in,neg} = \frac{1}{4}\mathrm{Re}\left[\mathbf{V}_{in}\mathbf{I}_{in}^*\right]$ with $\mathbf{I}_{in}^*$ the complex-conjugate of $\mathbf{I}_{in}$. If $\mathbf{V}_{C_{gs}}$ is the voltage across C_{gs}, then $\mathbf{I}_{in} = \frac{1}{R_g}\left(\mathbf{V}_{in} - \mathbf{V}_{C_{gs}}\right)$. It remains to derive $\mathbf{V}_{C_{gs}}$. The impedance $\mathbf{Z}$ at the gate, looking into the drain, is

$$\mathbf{Z} = \frac{\mathbf{V}_{C_{gs}}}{\mathbf{I}_{gd}} = \frac{\mathbf{V}_{C_{gs}}}{j\omega C_{gd,neg}\left(\mathbf{V}_{C_{gs}} - \mathbf{V}_d\right)} \tag{3.17}$$

with $\mathbf{V}_d$ the drain-ground voltage. During the negative half cycle, the drain-ground voltage $V_{d2}(\theta)$ given by (3.13) may be approximated by a sine of amplitude $-V_{d2}(\frac{3\pi}{2})$: $V_{d2,approx}(\theta) = -V_{d2}(\frac{3\pi}{2})\sin(\theta)$. It follows that

$$\mathbf{V}_d = -V_{d2}(\frac{3\pi}{2}) = -\left(\frac{8}{3}V_{dd} - \frac{5}{3}V_{dsmin} - \frac{8}{3}R_s I_{dc}\right)$$

Using the voltage-divider formula yields for $\mathbf{V}_{C_{gs}}$:

$$\mathbf{V}_{C_{gs}} = \mathbf{V}_{in} \frac{\frac{1}{j\omega C_{gs,neg}} \| \mathbf{Z}}{R_g + \frac{1}{j\omega C_{gs,neg}} \| \mathbf{Z}} = \mathbf{V}_{in} \frac{1}{1 + \frac{R_g}{\mathbf{Z}} + j\omega R_g C_{gs,neg}}$$

Substituting $\mathbf{Z}$ in the above equation by (3.17) and solving for $\mathbf{V}_{C_{gs}}$ results in the desired formula for $\mathbf{V}_{C_{gs}}$. The input power for the negative half cycle may now be derived as:

$$P_{in,neg} = \frac{\hat{V}_{in}}{4} \frac{\omega^2 R_g \left(C_{gs,neg} + C_{gd,neg}\right)\left[\hat{V}_{in}\left(C_{gs,neg} + C_{gd,neg}\right) - \mathbf{V}_d C_{gd,neg}\right]}{1 + \left[\omega R_g \left(C_{gs,neg} + C_{gd,neg}\right)\right]^2} \tag{3.18}$$

Since the MOSFET is assumed to operate in cut-off for the negative half cycle, one may approximate $C_{gs,neg}$ and $C_{gd,neg}$ as

$$C_{gs,neg} = FWC_{ov} + FWLC_{ox}$$

$$C_{gd,neg} = FWC_{ov}$$

The $FWLC_{ox}$-part in $C_{gs,neg}$ represents the gate-bulk capacitance during cut-off. The gate-bulk capacitance shows up as part of the gate-source capacitance as the bulk is tied to the source - either internally for a LDMOS FET or externally for a MOSFET.

Full cycle and gate resistance The input power for the full cycle is:

$$P_{in,1} = 2\left(P_{in,pos} + P_{in,neg}\right)$$

The factor 2 accounts for the fact that there are two transistors. The gate resistance may be modeled as:

$$R_g = \frac{1}{F}\left(R_{g,poly} + R_{g,contact}\right)$$

$R_{g,poly}$ and $R_{g,contact}$ are the polysilicon gate resistance and the metal-polysilicon contact resistance, respectively [30]. $R_{g,poly} = \frac{W}{3L} R_{g,sheet}$ with $R_{g,sheet}$ the gate sheet resistance.

3.3.1.3 Output and DC Power

Derivation of output and DC power Recall from section 3.3.1.1 that $\hat{V}_R = R\frac{9}{8}I_{dc}$. Together with (3.14) it is straight-forward to calculate the output and DC power:

$$P_{out,1} = \frac{1}{2}\frac{\hat{V}_R^2}{R} = \frac{2592R\left(V_{dd} - V_{dsmin}\right)^2}{\left(27R + 118R_s\right)^2} \tag{3.19}$$

$$P_{dc} = V_{dd} 2 I_{dc} = \frac{128V_{dd}\left(V_{dd} - V_{dsmin}\right)}{27R + 118R_s}$$

Derivation of V_{dsmin} V_{dsmin} remains as an unknown in the above equations. The well-known drain-source current equation for a MOSFET in the triode region may be used to estimate V_{dsmin}.

$$I_{ds}(0 \le \theta < \pi) = 2I_{dc} = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{gs}(0 \le \theta < \pi) - V_{th}\right)V_{dsmin} - \frac{1}{2}V_{dsmin}^2\right] \tag{3.20}$$

A difficulty is to estimate $V_{gs}(0 \le \theta < \pi)$ in the above equation. D. Choi suggests in [30] to estimate it as $V_{gs}(\theta) = \text{abs}(V'_{gs})\sin\left(\theta + \arg(V'_{gs})\right) + V_{th}$ for a gate bias voltage of V_{th} and to use the voltage-divider formula for V'_{gs}:

$$V'_{gs} = \hat{V}_{in}\frac{1}{1 + j\omega\left(C_{gs,pos} + C_{gd,pos}\right)\left(R_g + R_s\right)}$$

In this formula, C_{gs} means the capacitance between the points G and S in Fig. 3.12. $V_{gs}(\theta)$ may now be averaged over $0 \le \theta < \pi$. However, this effort does

not pay off, as the model comparison in Fig. 3.15 shows. Assuming that the input voltage fully drops across C_{gs} and using the average value of a half-sine of amplitude $\hat{V}_{in}$ for $V_{gs}(0 \leq \theta < \pi)$, i. e. $V_{gs}(0 \leq \theta < \pi) = \frac{2}{\pi}\hat{V}_{in} + V_{th}$, yields about the same PAE but greatly simplifies the equations. Therefore, $\frac{2}{\pi}\hat{V}_{in} + V_{th}$ is subsequently used for $V_{gs}(0 \leq \theta < \pi)$ (denoted as the No Input Voltage-Divider model in Fig. 3.15) instead of the Input Voltage-Divider model.

Moreover, the term $\frac{1}{2}V_{dsmin}^2$ in (3.20) causes V_{dsmin} to become imaginary for low input voltages when solving (3.20) for V_{dsmin}. In Fig. 3.15 this happens for input voltages lower than about 5.5 V. Therefore, the drain-source current equation for the *deep* triode region neglecting the quadratic V_{dsmin}-term in the I_{ds}-equation is subsequently used:

$$I_{ds}(0 \leq \theta < \pi) = 2I_{dc} = \mu_n C_{ox}\frac{W}{L}\left[\frac{2}{\pi}\hat{V}_{in}V_{dsmin}\right] \tag{3.21}$$

The comparison in Fig. 3.15 between the model employing the triode current equation and the model employing the deep triode current equation suggests that the PAE for the deep triode model is about the same as for the triode model for large input voltages. However, Fig. 3.15 further suggests that the deep triode model grossly overestimates the PAE for input voltages that yield a lower-than-peak PAE. For input voltages that yield about the peak PAE, the predicted PAE-values for the deep triode model and for the triode model are about the same.

The drain-source current equation for the deep triode region, (3.21), may now be solved for V_{dsmin}:

$$V_{dsmin} = \frac{V_{dd}}{1 + \frac{1}{64\pi}\mu C_{ox}F\frac{W}{L}\hat{V}_{in}\left(27R + 118R_s\right)} \tag{3.22}$$

3.3.2 Analytical Expressions for η and PAE

With the results for P_{in}, P_{out}, and P_{dc} of section 3.3.1, deriving the drain-efficiency η and the PAE just takes some algebraic manipulations.

$$\eta = \frac{P_{out,1}}{P_{dc}} = \frac{81R\left(1 - \frac{V_{dsmin}}{V_{dd}}\right)}{4\left(27R + 118R_s\right)} \tag{3.23}$$

$$\begin{gathered} PAE = \frac{P_{out,1} - P_{in,1}}{P_{dc}} = \eta - \frac{\eta}{G} = \frac{81R\left(1 - \frac{V_{dsmin}}{V_{dd}}\right)}{4(27R + 118R_s)} \\ - \frac{\hat{V}_{in}R_g\omega^2F^2W^2(27R+118R_s)(LC_{ox}+2C_{ov})\left[2\hat{V}_{in}(LC_{ox}+2C_{ov}) - C_{ov}V_d\right]}{256V_{dd}^2\left(1+[\omega FWR_g(LC_{ox}+2C_{ov})]^2\right)\left(1 - \frac{V_{dsmin}}{V_{dd}}\right)} \end{gathered} \tag{3.24}$$

$$V_d = \frac{V_{dd}}{3\left(27R + 118R_s\right)}\left(\frac{V_{dsmin}}{V_{dd}}\left[135R + 78R_s\right] - 216R - 432R_s\right)$$

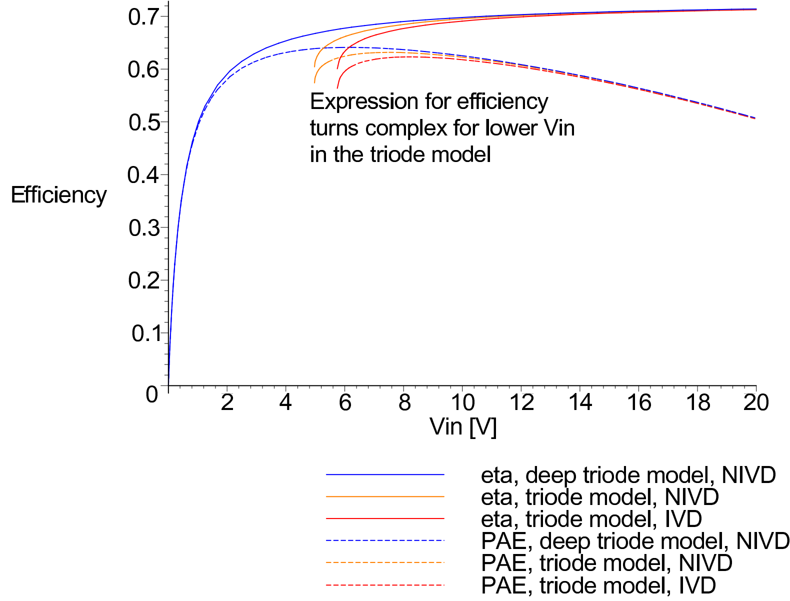


Figure 3.15: Calculated drain-efficiency η and PAE as a function of the input voltage $\hat{V}_{in}$ for three different models of deriving V_{dsmin}. The deep triode model uses (3.21) for I_{ds}. The triode model uses (3.20) for I_{ds}. The argument IVD stands for Input Voltage-Divider and means that $V_{gs}(\theta) = \text{abs}(V'_{gs}) \sin\left(\theta + \arg(V'_{gs})\right) + V_{th}$ is averaged over $0 \leq \theta < \pi$. NIVD (No Input Voltage-Divider) curves just use $V_{gs}(0 \leq \theta < \pi) = \frac{2}{\pi}\hat{V}_{in} + V_{th}$. (The curves are based on a sample CMCD PA employing Ericsson PTF10135 LDMOS devices.)

The derivation of the PAE outlined in the last two sections has been implemented as a Maple[2] worksheet. This worksheet allows to plot the drain-efficiency η, the PAE, the input, output, and DC power versus various parameters. The worksheet e. g. makes it possible to determine the device dimensions for a MOSFET that maximize the PAE for a given PA specification and a given MOSFET manufacturing process.

3.3.3 Comparison to Harmonic-Balance Simulations

To verify the adequacy of the derived equations for the drain-efficiency and the PAE, harmonic-balance simulations in ADS[3] were performed. The ADS schematics of Fig. 3.16 and Fig. 3.17 correspond to the shunt-tank CMCD PA of Fig. 3.12 (on page 27). For the switching devices, a SPICE LEVEL 3 model of the Ericsson PTF10135 LDMOS FET was used. The SPICE LEVEL 3 model and the package parasitics for this device have been extracted by D. Choi in [2]. To directly compare the simulated and calculated efficiencies, input matching and output matching circuitry is omitted. The calculated efficiencies and powers are based upon the parameters of the Ericsson PTF10135 LDMOS FET given in Tab. 3.1a and upon the parameters of a CMCD PA reference design given by Tab. 3.1b. The data given in Tab. 3.1a was extracted from the SPICE LEVEL 3 model.

Fig. 3.18 plots the calculated and simulated drain-efficiency η and PAE versus the input voltage amplitude $\hat{V}_{in}$. As predicted in section 3.3.1.3, the calculated efficiencies grossly overestimate the simulated efficiencies for very low input voltage amplitudes (for $\hat{V}_{in} < 2.5$ V in Fig. 3.18). However, the calculated peak-PAE for $R_{g,sheet} = 0.56\,\frac{\Omega}{\square}$ deviates by merely 0.5 V from the simulated peak-PAE. Doubling e. g. the value of the poorly measurable gate sheet resistance from $R_{g,sheet} = 0.56\,\frac{\Omega}{\square}$ (as given in [2]) to $R_{g,sheet} = 1.12\,\frac{\Omega}{\square}$ shifts the peak-PAE by more than 1 V. From the data given in Fig. 3.18, we may conclude that the PAE-formula given by (3.24) is adequate to assess the impact of the parameters shown in the equivalent CMCD PA circuit of Fig. 3.12. However, the PAE-formula is not adequate for accurately predicting the PAE. Fig. 3.19 provides some indications where the errors for accurately predicting the PAE are made. While the input power is predicted fairly accurate, large errors are made in estimating the output and DC power.

3.3.4 Discussion and Conclusions from Analytical Expressions

3.3.4.1 Sensitivity Analysis

Looking at the PAE-formula (3.24), no parameter that obviously optimizes the PAE can be identified. Therefore, the sensitivity of the PAE towards the different parameters has been investigated. Fig. 3.20, Fig. 3.21, and Fig. 3.22 plot

[2]Maple 8 by Waterloo Maple Inc.
[3]Advanced Design System 2002C by Agilent Technologies

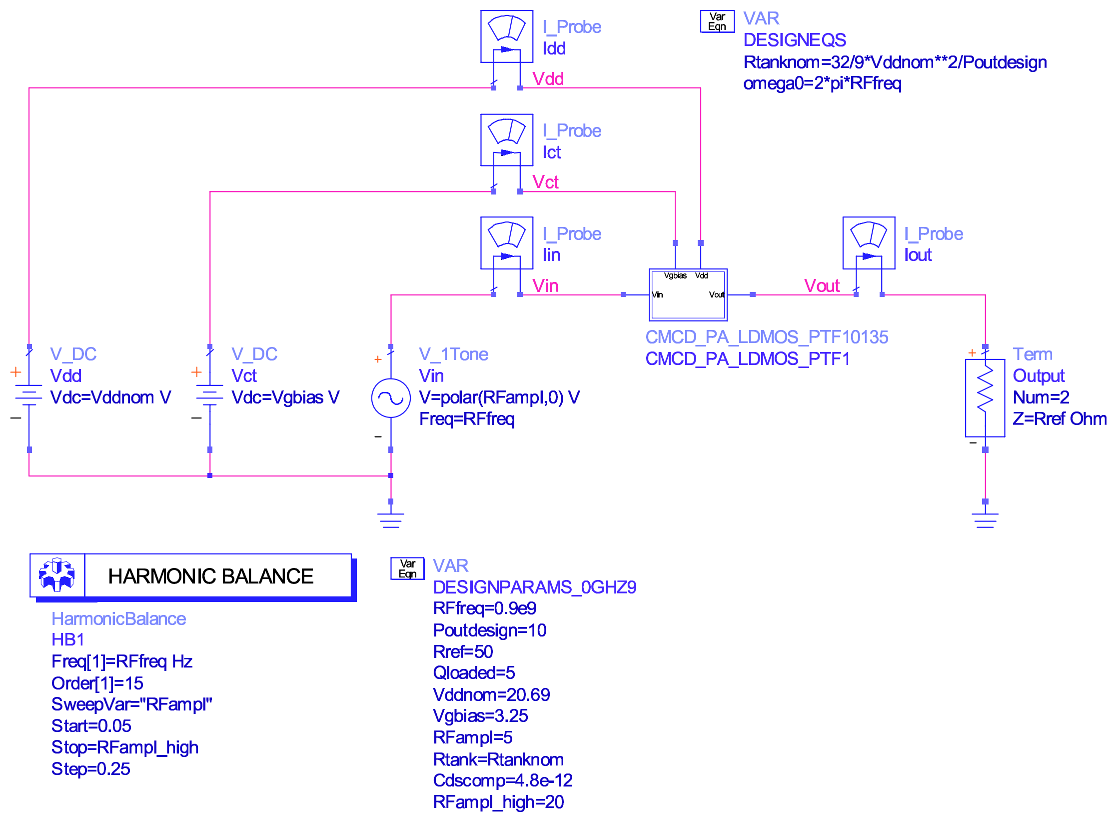


Figure 3.16: ADS schematic for the harmonic-balance simulations. Refer to Fig. 3.17 for the CMCD_PA_LDMOS_PTF10135 block.

Table 3.1: Parameters of the Ericsson PTF10135 LDMOS FET (a) and parameters of a CMCD PA reference design (b).

(a)

$R_s = 0.565\,\Omega$	$R_{g,sheet} = 0.55836\,\frac{\Omega}{\square}$	$R_{g,contact} = 0$
$C_{ox} = 40 \cdot 10^{-6}\,\frac{\mathrm{F}}{\mathrm{m}^2}$	$C_{ov} = 0.2037 \cdot 10^{-9}\,\frac{\mathrm{F}}{\mathrm{m}}$	$\mu_n = 0.045\,\frac{\mathrm{m}}{\mathrm{Vs}}$
$F = 180$	$W = 250 \cdot 10^{-6}\,\mathrm{m}$	$L = 0.5 \cdot 10^{-6}\,\mathrm{m}$

(b)

$f = 900\,\mathrm{MHz}$	$V_{dd} = 20.69\,\mathrm{V}$	$R = 152\,\Omega$	$\hat{V}_{in} = 4.4\,\mathrm{V}$

$V_{dd} = \frac{BV}{\pi}$ with $BV = 65\,\mathrm{V}$ the breakdown voltage of the PTF10135 LDMOS FET. R was calculated from (3.11). $\hat{V}_{in}$ corresponds to the calculated maximum PAE.

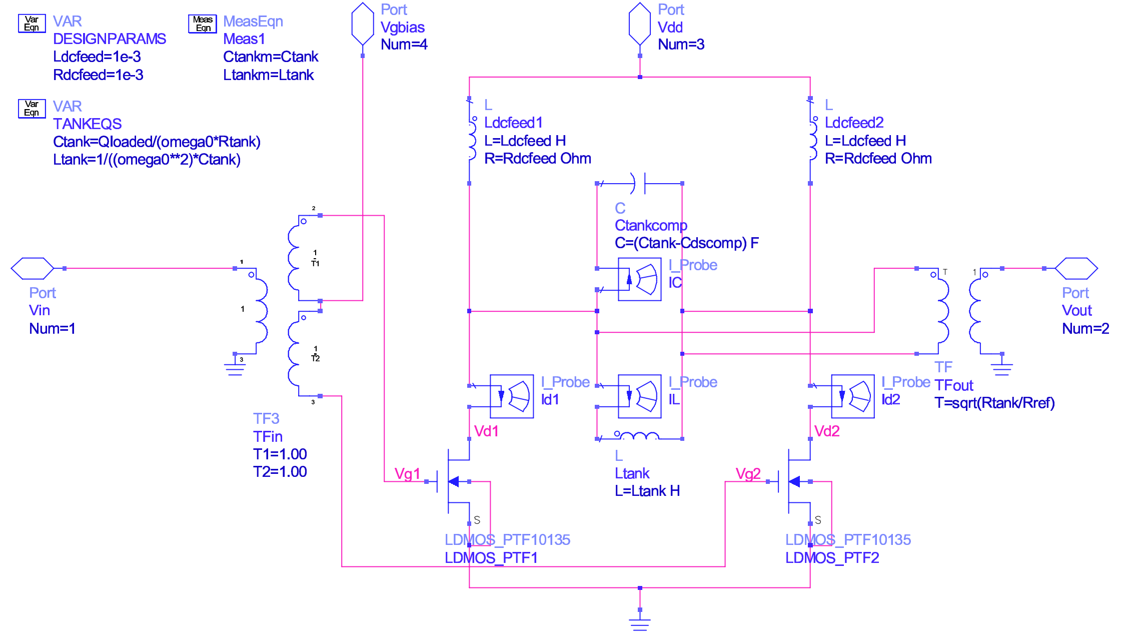


Figure 3.17: ADS schematic for the CMCD_PA_LDMOS_PTF10135 block of Fig. 3.16.

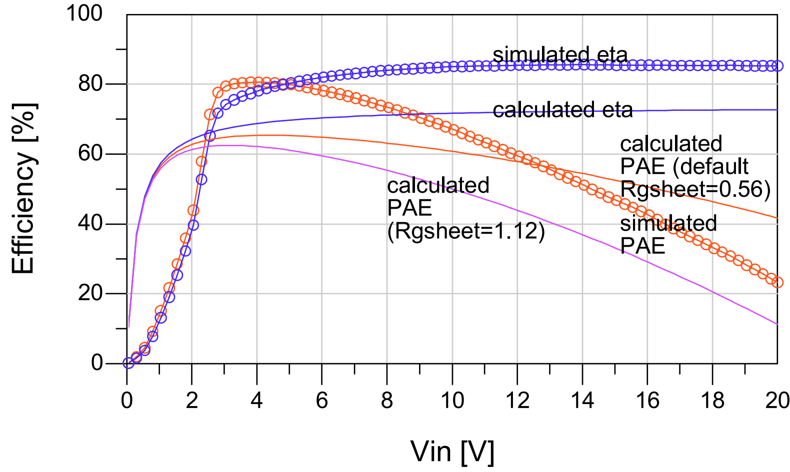


Figure 3.18: Drain-efficiency η and PAE versus the input voltage amplitude $\hat{V}_{in}$ as calculated by the analytical model and as simulated by harmonic-balance simulations with a SPICE LEVEL 3 model of the PTF10135 LDMOS FET for the CMCD PA reference design of Tab. 3.1b.

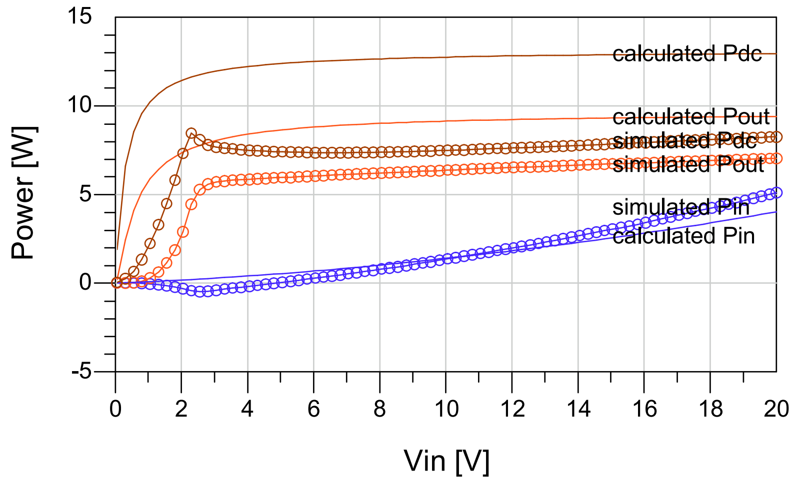


Figure 3.19: DC power, output power, and input power versus the input voltage amplitude $\hat{V}_{in}$ as calculated by the analytical model and as simulated by harmonic-balance simulations with a SPICE LEVEL 3 model of the PTF10135 LDMOS FET for the CMCD PA reference design of Tab. 3.1b.

the normalized PAE value versus the normalized parameter values for different ranges. For these sensitivity plots, the PAE was normalized to the PAE of the CMCD PA reference design given in Tab. 3.1 employing PTF10135 LDMOS FETs. By looking at the sensitivity plots, we may classify the parameters into three categories:

- Parameters that show a *nearby maximum*: $\hat{V}_{in}$, R, C_{ox}, and the dimension parameters F, W, and L.

- Parameters that *maximize the PAE when increasing* (positive sensitivity): V_{dd} and μ_n. To maximize the PAE, it is therefore advisable to pick the highest V_{dd} that still fulfills $BV_{ds,off} > \pi V_{dd}$. μ_n however, is often not subject to optimization as it is a fixed manufacturing process parameter.

- Parameters that *maximize the PAE when decreasing* (negative sensitivity): R_s, $R_{g,sheet}$, and C_{ov}. The normalized sensitivity of the PAE increases in this order. Note that HEMT/pHEMT devices may gain an edge over MOSFET devices from this point of view as HEMTs/pHEMTs do not suffer from an overlap capacitance. Moreover, the gate sheet resistance for HEMTs/pHEMTs is substantially lower than the gate sheet resistance for MOSFETs as HEMTs/pHEMTs employ a metal gate instead of a polysilicon gate.

To maximize the PAE, it therefore pays most besides finding an optimum for $\hat{V}_{in}$, R, C_{ox}, F, W, and L to minimize C_{ov} (normalized sensitivity of $S_N = -0.17$), to maximize V_{dd} ($S_N = 0.11$), to minimize $R_{g,sheet}$ ($S_N = -0.09$), and to minimize R_s ($S_N = -0.02$) in this order.

However, the normalized sensitivities given here are only valid for this particular reference PAE. They may change significantly if a different CMCD PA reference design with other parameters than those given in Tab. 3.1 is selected. Note that the normalized sensitivity of the parameter x was computed as follows:

$$S_N(x) = \frac{x}{PAE}\frac{\partial PAE}{\partial x}$$

3.3.4.2 Resulting Design Guidelines

The above sensitivity analysis suggests the following design guidelines for the design parameters V_{dd}, $\hat{V}_{in}$, and R:

- $V_{dd} = \frac{BV_{ds,off}}{\pi}$

- Find $\hat{V}_{in}$ and R that maximize the PAE.

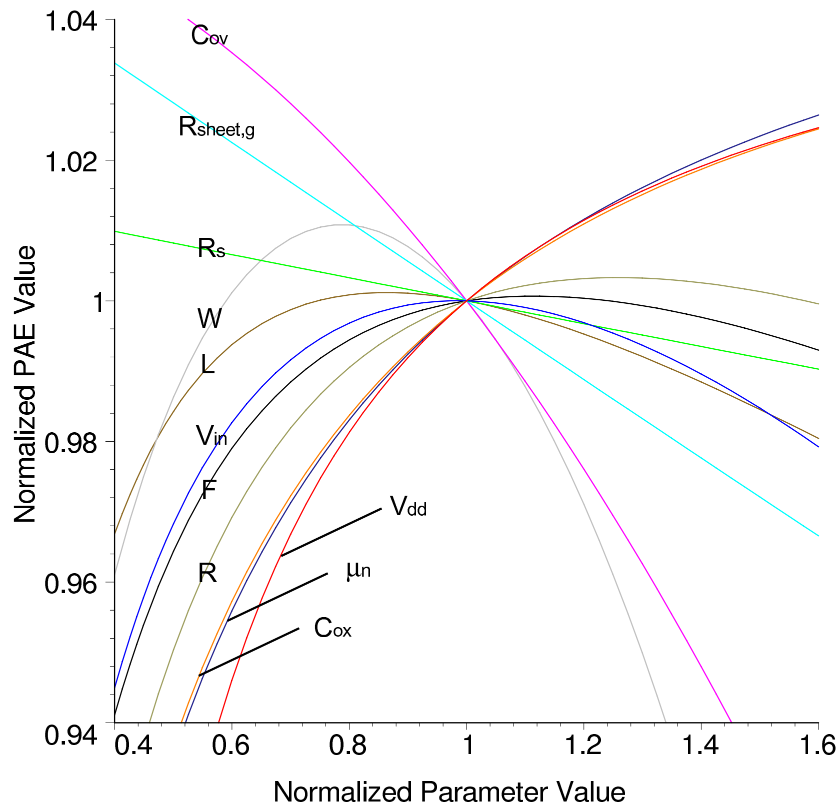


Figure 3.20: Calculated normalized PAE values versus normalized parameter values between 0.4 and 1.6 for the CMCD PA reference design given in Tab. 3.1 employing Ericsson PTF10135 LDMOS FETs.

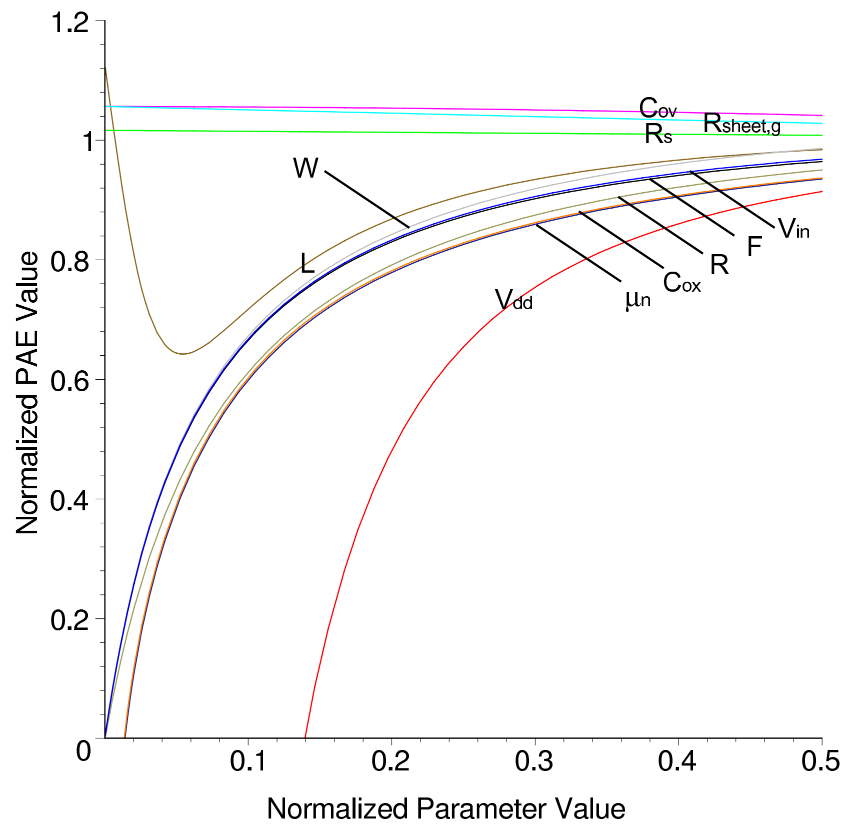


Figure 3.21: Calculated normalized PAE values versus normalized parameter values between 0 and 0.5. The parameters of the reference design are given in Tab. 3.1.

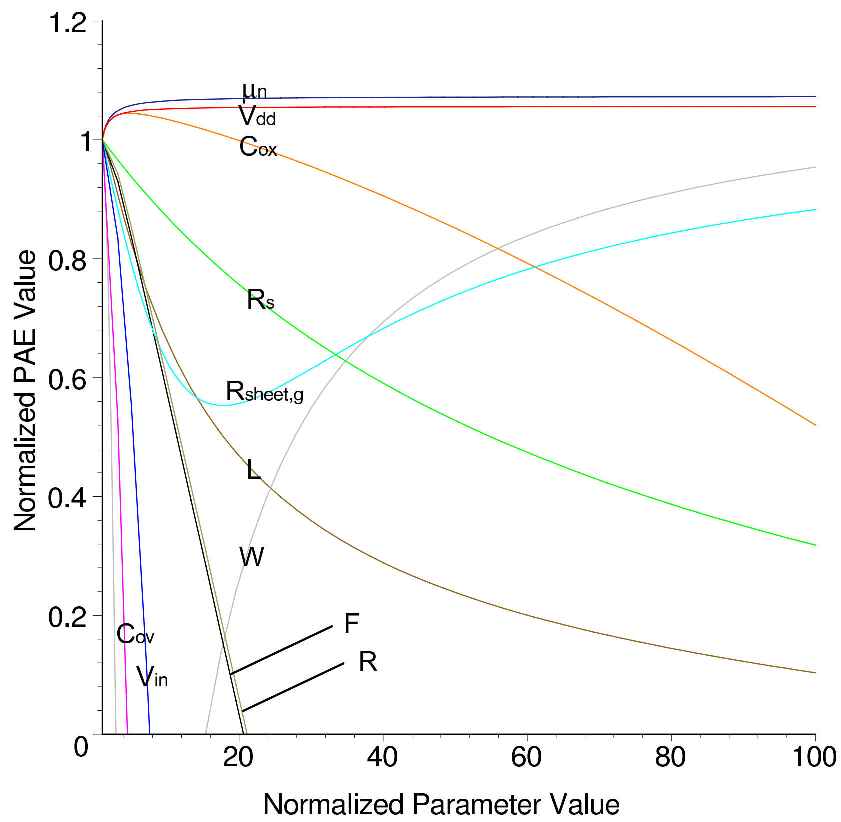


Figure 3.22: Calculated normalized PAE values versus normalized parameter values between 1 and 100. The parameters of the reference design are given in Tab. 3.1.

Increasing V_{dd} maximizes the PAE and the output power $P_{out,1}$ at the same time as the above sensitivity analysis and (3.19) (on page 31) for $P_{out,1}$ show. However, a $\hat{V}_{in}$ or a R that maximizes the PAE does not necessarily maximize the output power $P_{out,1}$ at the same time.

Fig. 3.23 plots among other quantities the calculated PAE and output power $P_{out,1}$ as a function of $\hat{V}_{in}$ for the CMCD reference design. As may be seen from the expression for $P_{out,1}$ (3.19) in conjunction with the expression for V_{dsmin} (3.22), $\hat{V}_{in}$ must be maximized in order to maximize $P_{out,1}$. Looking at Fig. 3.23, a reasonable strategy for selecting $\hat{V}_{in}$ is to choose the one that maximizes the PAE.

Fig. 3.24 plots the calculated PAE and output power $P_{out,1}$ as a function of R. In contrast to selecting $\hat{V}_{in}$, picking the R that maximizes the PAE may result in a very low output power $P_{out,1}$. In Fig. 3.24 the maximum PAE occurs for $R = 191\,\Omega$, whereas the maximum $P_{out,1}$ occurs for $R = 13\,\Omega$. Therefore, sacrificing e. g. 1 % of PAE by selecting a lower-than-optimum R in return of a greatly improved output power seems justifiable. This results in the following design guidelines for V_{dd}, $\hat{V}_{in}$, and R:

- $V_{dd} = \frac{BV_{ds,off}}{\pi}$
- Select $\hat{V}_{in}$ that maximizes the PAE.
- Find R that maximizes the PAE and lower R to a value that yields a PAE 1 % lower than before. Select the R that gives the best trade-off between the PAE and $P_{out,1}$ over this range.

Note that the output power cannot be increased indefinitely as (3.11) (on page 25) suggests. (3.11) is an approximation that is only valid if R is large compared to R_s, and $\hat{V}_{in}$ is very large. Even if $\hat{V}_{in}$ is infinite, the output power expression (3.19) converges to zero if R is small compared to R_s. Therefore, $P_{out,1}$ always shows a maximum as a function of R.

3.3.5 Adaption to HEMT Devices

The analysis of section 3.3.1 is easily adapted to HEMT devices as the triode region I_{ds}-equation for the HEMT is of the same form as for the MOSFET. The triode region I_{ds}-equation for the HEMT may be written as [34]:

$$I_{ds} = \mu_n C_i \frac{W}{L} \left[(V_{gs} - V_{th})\, V_{ds} - \frac{1}{2} V_{ds}^2 \right]$$

$C_i = \frac{\varepsilon_s}{d_{2DEG}}$ is the gate-to-channel capacitance, ε_s the permittivity and d_{2DEG} the distance of the two-dimensional electron gas (2DEG) from the gate. The form of the above equation is exactly the same as of (3.20) for a MOSFET. V_{dsmin} may therefore be calculated with (3.22) by replacing C_{ox} with C_i. What remains is to formulate the HEMT C_{gs} and HEMT C_{gd} for the positive and

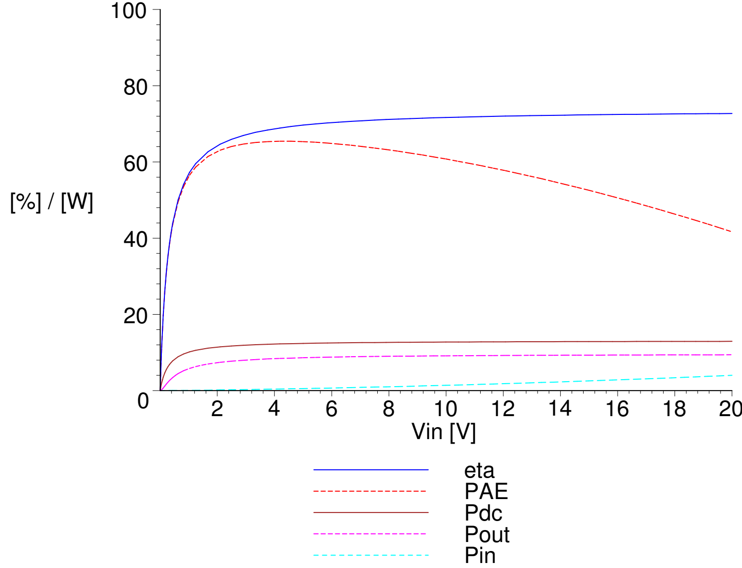


Figure 3.23: Calculated drain-efficiency η , PAE, DC power, output power, and input power as a function of the input voltage amplitude $\hat{V}_{in}$ for the CMCD PA reference design given in Tab. 3.1.

negative half cycle to calculate the input power with (3.16) and (3.18). During the positive half cycle, when the HEMT operates in the triode region, the gate-to-channel capacitance may be assumed to be evenly distributed between the source and the drain: $C_{gs,pos} = C_{gd,pos} = \frac{1}{2}C_i$. During the negative half cycle, when the HEMT operates in cut-off, the capacitances reduce to zero: $C_{gs,neg} = C_{gd,neg} = 0$. Note that the HEMT does not suffer from an overlap capacitance as the MOSFET does. However, there are fringing capacitances $C_{gs,fringe}$ and $C_{gd,fringe}$. These capacitances are neglected above for simplicity.

3.4 Comparison of MOSFET-, HBT-, and HEMT-Parameters

The most relevant device parameters for a CMCD PA have been identified by the sensitivity analysis. They include the drain-source breakdown voltage (because the breakdown voltage imposes an upper limit on V_{dd}), the mobility μ_n, the source resistance R_s, the gate sheet resistance $R_{g,sheet}$, and the overlap capacitance C_{ov}. Further important device parameters are the transit frequency f_T, the maximum oscillation frequency f_{max}, and the maximum drain-source current rating $I_{ds,mr}$. To identify the differences in device parameters between the devices of interest, commercially available packaged devices are investigated

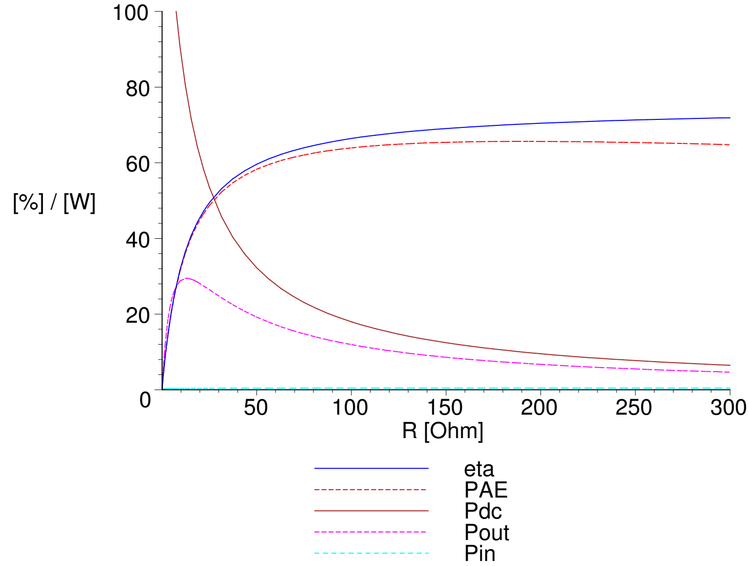


Figure 3.24: Calculated drain-efficiency η , PAE, DC power, output power, and input power as a function of the total tank resistance R for the CMCD PA reference design given in Tab. 3.1.

in this section followed by a theoretical analysis of the breakdown phenomena, the switching performance, and the on-resistance for the devices of interest.

3.4.1 Comparison of Selected Commercial Devices

For a first impression of how the device parameters for different technologies compare to each other, the device parameters of 16 commercial packaged RF transistors are summarized in Tab. 3.2. The selection includes LDMOS FET, HBT, HEMT, pHEMT, E-pHEMT, and MESFET devices. Evidently, this selection is not necessarily fully representative for the specific device families. However, it is possible to identify some of the striking properties. Fig. 3.25 provides a good means to do so: it illustrates the fraction of the table maximum a certain device achieves for four different parameters. The device with the best overall performance is the one with the largest area obtained from connecting the corresponding points on the four axes. With this figure of merit, we may conclude:

- The LDMOS FET devices are unrivaled in their high breakdown voltage. A high breakdown voltage benefits the PAE very much. Therefore, LDMOS FET devices may be the best choice for a CMCD PA but only if the frequency is low as they have a low f_{max}.

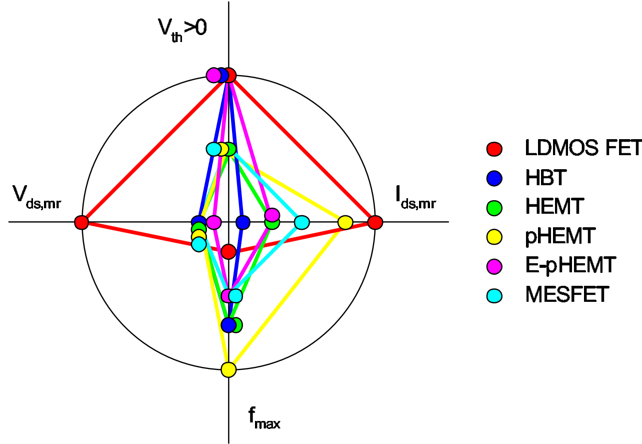


Figure 3.25: Relative fractions of table maxima in Tab. 3.2 for $V_{ds,mr}$, $I_{ds,mr}$, and f_{max} . Additionally, it is indicated whether it is possible to bias the device with a positive voltage (100% mark on the $V_{th} > 0$ axis) or not (50% mark on the $V_{th} > 0$ axis). (f_{max} for the LDMOS FET is an estimate.)

- The HBT devices generally suffer from both a low breakdown voltage and a low maximum current rating. The area of the connected points is low, the overall performance therefore probably poor for a CMCD PA.
- The HEMT and the MESFET devices seem to perform similarly average.
- The pHEMT devices show a very large f_{max} and a fairly large maximum current rating but suffer from a low breakdown voltage. Therefore, pHEMT devices may be the best choice for a CMCD PA but only if the frequency is high.
- The advantage of a positive threshold voltage for the E-pHEMT is offset by its very low breakdown voltage.

3.4.2 Breakdown Phenomena

The off-state breakdown voltage of a switching device is a very important device parameter as the supply voltage V_{dd} must be maximized to maximize the PAE. Therefore, the breakdown phenomena for the MOSFET, LDMOS FET, HBT and HEMT/pHEMT are compared to each other in the following. For the MOSFET, LDMOS FET, and HBT, the dominant breakdown phenomena are

- the avalanche breakdown of a reverse-biased pn-junction and
- the punch-through of a PN depletion region.

Table 3.2: Selected commercial LDMOS FET, HBT, HEMT, pHEMT, E-pHEMT, and MESFET devices (all data are from the corresponding data sheets).

Manufacturer	Model	Technology	Spec. Freq. [GHz]	Spec. V_{dd} [V]	Spec. I_{ds} [mA]	P_{out1dB} [W]	$V_{ds,max\ rating}$ [V]	$I_{ds,max\ rating}$ [mA]	$V_{gs,min\ rating}$ [V]	$V_{gs,max\ rating}$ [V]	V_{th} [V]	f_{max} [GHz]	Model	Package
LDMOS														
Motorola	MRF9045MR1	Si	0.945	26	na	na	65	6321[a]	-0.5	15	2.8	na	MET/Root	TO-270
Motorola	MRF281SR1	Si	2	26	na	na	65	769[a]	-20	20	3.2	na	Root	458C-03
Motorola	MRF282SR1	Si	2	26	na	na	65	1154[a]	-20	20	3	na	Root	458C-03
Motorola	MRF21010LSR1	Si	2.17	28	na	na	65	1563[a]	-0.5	15	3	na	MET/Root	360C-05
	Average		1.78	26.50	na	na	65.00	2452	-10.3	17.50	3.00	na		
	Fraction of Table Max.		0.15	1.00	na	na	1.00	1.00	1.00	1.00	1.00	na		
HBT														
Infineon	BFP650	SiGe	1.8	3	80	0.06	13[b]	150	-1.2[c]	na	0.7	13.5[d]	Gummel	SOT343
Infineon	BFP690	SiGe	1.8	3	200	0.09	13[b]	350	-1.2[c]	na	0.7	5.5[e]	Gummel	SOT343
	Average		1.80	3.00	140	0.08	13.00	250	-1.2	na	0.70	9.50		
	Fraction of Table Max.		0.16	0.11	0.29	0.02	0.20	0.10	0.12	na	0.23	0.70		
HEMT														
Triquint	TGF4230-SCC	GaAs	12	8	96	0.6	12	294[f]	-5	0	-1.85[g]	13[h]	na	not pack.
Triquint	TGF4240-SCC	GaAs	12	8	192	1.5	12	588[f]	-5	0	-1.85[g]	9[h]	na	not pack.
Triquint	TGF4250-SCC	GaAs	10.5	8	384	3.1	12	1176[f]	-5	0	-1.85[g]	5.5[h]	na	not pack.
	Average		11.50	8.00	224	1.73	12.00	686	-5.0	0.00	-1.85	9.17		
	Fraction of Table Max.		1.00	0.30	0.46	0.39	0.18	0.28	0.49	0.00	na	0.67		
pHEMT														
Motorola	MRFG35030	GaAs	3.5	12	180	10	15	2358[a]	-5	na	-0.8	na	na	360D-02
Filtronic	LP3000P100	GaAs	15	8	na	2	12	2200	-4	na	-1.2[g]	7.2[i]	Curtice 3	P100
Filtronic	LP1500P100	GaAs	15	8	na	1.2	12	980	-4	na	-1.2[g]	18[j]	Curtice 3	P100
	Average		11.17	9.33	180	4.40	13.00	1846	-4.3	na	-1.07	13.60		
	Fraction of Table Max.		0.97	0.35	0.37	1.00	0.20	0.75	0.42	na	na	1.00		
E-pHEMT														
Agilent	ATF-511P8	GaAs	2	4.5	200	1	7	1000	-5	0.8	0.28	4[k]	Curtice 2	LPCC
Agilent	ATF-521P8	GaAs	2	4.5	200	0.45	7	500	-5	0.8	0.28	7[l]	Curtice 2	LPCC
Agilent	ATF-531P8	GaAs	2	4	135	0.28	7	300	-5	0.9	0.3	10[m]	Curtice 2	LPCC
	Average		2.00	4.33	178	0.58	7.00	600	-5.0	0.83	0.29	7.00		
	Fraction of Table Max.		0.17	0.16	0.36	0.13	0.11	0.24	0.49	0.05	0.10	0.51		
MESFET														
Fujitsu	FLL357ME	GaAs	2.3	5	800	3.5	15	1800[f]	-5	na	-2[g]	5[n]	na	ME
Fujitsu	FLL107ME	GaAs	2.3	10	180	0.9	15	450[f]	-5	na	-2[g]	5[o]	na	ME
	Average		2.30	7.50	490	2.20	15.00	1125	-5.0	na	-2.00	5.00		
	Fraction of Table Max.		0.20	0.28	1.00	0.50	0.23	0.46	0.49	na	na	0.37		

[a] calculated from maximum DC power dissip. and spec. V_{dd}

[b] V_{ces}

[c] V_{ebo}

[d] from meas. S-param. for V_{ce}=3V and I_c=50mA

[e] from meas. S-param. for V_{ce}=3V and I_c=56mA

[f] assumed to be I_{dss}

[g] pinch-off voltage V_p

[h] from modeled S-param. for V_{ds}=8V and I_d=0.3I_{dss}

[i] from meas. S-param. for V_{ds}=8V and I_d=251.9mA

[j] >18GHz, from meas. S-param. for V_{ds}=8.07V and I_d=254mA

[k] from meas. S-param. for V_{ds}=5V and I_d=300mA

[l] from meas. S-param. for V_{ds}=4.5V and I_d=280mA

[m] from meas. S-param. for V_{ds}=5V and I_d=135mA

[n] >5GHz, from meas. S-param. for V_{ds}=10V and I_d=720mA

[o] >>5GHz, from meas. S-param. for V_{ds}=10V and I_d=180mA

Avalanche breakdown occurs when the reverse-bias voltage of a pn-junction is high enough to start an avalanche impact ionization by free electrons. The breakdown voltage mainly depends on the critical electric field E_c and on the background doping concentration. The background doping concentration is the minimum of the p- and n-doping concentration. Solving the one-dimensional Poisson equation for a pn-junction yields [35]

$$x_p = \frac{E(0)\varepsilon_s}{qN_A}, \quad x_n = -\frac{E(0)\varepsilon_s}{qN_D} \tag{3.25}$$

and

$$V_{bi} + V_r = \frac{x_p E(0)}{2} - \frac{x_n E(0)}{2} \tag{3.26}$$

where x_p and x_n are the depletion region borders for the p- and n-region, respectively. $E(0)$ is the electric field at the pn-interface, N_A and N_D the acceptor and donator doping concentration, respectively, V_{bi} the built-in voltage, and V_r the reverse-bias voltage. Using (3.25) and (3.26), it is straight-forward to derive the avalanche breakdown voltage BV_{av} for $E(0) = E_c$ by ignoring V_{bi} as $V_r \gg V_{bi}$:

$$BV_{av} = \frac{E_c^2 \varepsilon_s}{2q} \frac{N_A + N_D}{N_A N_D} \tag{3.27}$$

For the above derivation, planar pn-junctions have been assumed. However, for cylindrical junctions and even more for spherical junctions, the breakdown voltage may be considerably lower. The field lines converge at these structures which causes devices to breakdown at diffusion-edges first. Moreover, E_c is a function of the doping concentration, increasing with an increasing background doping concentration. Generally, the critical field for GaAs is about 10% higher than the critical field for Si.

Punch-through occurs when the depletion region of a reverse-biased pn-junction gets wide enough to hit the contacts of the p- or n-region. Again using (3.25) and (3.26), the punch-through voltage BV_{pt} may be derived by ignoring V_{bi} as before

$$BV_{pt,\text{towards p contact}} = \frac{x_{p,max}^2 q}{2\varepsilon_s} \frac{N_A (N_A + N_D)}{N_D} \tag{3.28}$$

$$BV_{pt,\text{towards n contact}} = \frac{x_{n,max}^2 q}{2\varepsilon_s} \frac{N_D (N_D + N_A)}{N_A} \tag{3.29}$$

where $x_{p,max}$ and $x_{n,max}$ mark the diffusion-ends in the p-region and n-region, respectively.

3.4.2.1 MOSFET/LDMOS FET

Fig. 3.26 shows the simplified cross-sections of a conventional Si MOSFET device and of a Si LDMOS FET. The LDMOS FET employs a p-base and a n-well diffusion in addition to the source- and drain-contacts of the conventional MOSFET which allows for a higher breakdown voltage. The inversion channel is formed beneath the gate in the p-base region. The n-well region serves as a drift region for the electrons traveling from the source to the drain. The fundamental advantage of this structure over the conventional MOSFET of Fig. 3.26a is that it minimizes the electric field immediately under the gate and therefore increases the breakdown voltage. The bulk contact is internally shorted to the source-contact to disable the parasitic n-well/p-base/n+ structure. This n-p-n structure may still trigger a bipolar common-emitter breakdown: The horizontal current flowing in the p-base from the n-well to the p+ contact may cause a voltage drop along the p-base that forward-biases the p-base/n+ diode. If this happens, the bipolar common-base breakdown voltage BV_{CB} reduces to the bipolar common-emitter breakdown voltage BV_{CE}, a value only about $0.6BV_{CB}$ [36].

Generally, the MOSFET and the LDMOS FET suffer from the following breakdown phenomena:

- *Avalanche breakdown* of the drain-bulk diode in the MOSFET case and of the n-well/p-base diode in the LDMOS FET case.

- *Punch-through* of the drain-bulk depletion region towards the source for the MOSFET and of the n-well/p-base depletion region towards the source in the LDMOS FET case. Moreover, the depletion region may also punch-through towards the n+ drain contact for the LDMOS FET. However, this kind of punch-through may be tolerated since it does not mean a loss of current control as in a punch-through towards the source.

- *Time-dependent dielectric breakdown (TDDB)*: TDDB refers to charge carriers being permanently trapped in the gate oxide due to exposure to high fields. The trapped charge carriers modify the threshold voltage.

- *Oxide rupture*: If the gate is at a very low and the drain at a very high potential an irreversible gate-to-channel short may result. Oxide rupture is particularly a problem with ever-thinner gate oxides.

The avalanche breakdown voltages may be calculated by (3.27), whereas (3.28) and (3.29) serve to calculate the punch-through voltages. In the case of the LDMOS FET, several measures may be taken to increase the breakdown voltage. Some of these are a staggered (dual-)gate to minimize the field towards the drain, a metal plate above the gate acting as a Faraday shield to minimize the field at the edges of the gate [36], or lightly doped drain extensions [37].

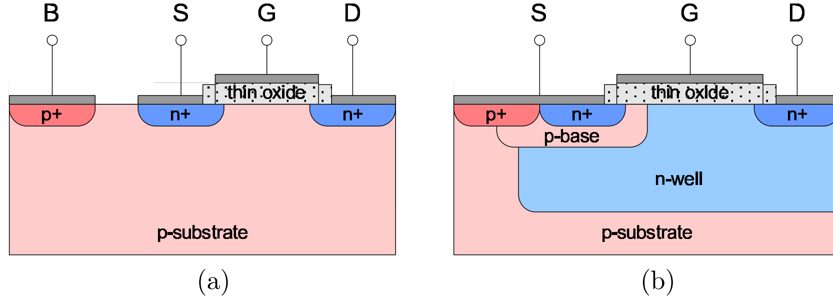


Figure 3.26: Simplified cross-sections of a conventional Si MOSFET device (a) and of a Si LDMOS FET (b, according to [38]).

3.4.2.2 HBT

Fig. 3.27a shows the simplified cross-section of a SiGe HBT. When using a hetero-contact base-emitter junction it is possible to reduce the base resistance $R_{bb'}$ by increasing the base doping without sacrificing the current gain. Reducing $R_{bb'}$ greatly improves the maximum oscillation frequency f_{max}.

The breakdown phenomena of a HBT are similar to a homo-junction bipolar transistor:

- *Avalanche breakdown in the common-base configuration*: The common-base configuration corresponds to the off-state of a switching device in a CMCD PA. The collector-emitter voltage drops across the collector-base junction. The common-base avalanche breakdown voltage $BV_{ce,CB}$ is that of the base-collector pn-junction.

- *Avalanche breakdown in the common-emitter configuration*. The avalanche breakdown voltage $BV_{ce,CE}$ for the common-emitter configuration is considerably lower than $BV_{ce,CB}$ [39]:

  $$BV_{ce,CE} = BV_{ce,CB}\beta_0^{-1/n},\ 3 < n < 6$$

  The common-emitter configuration is not encountered by a switching device in a CMCD PA theoretically. However, it may be entered practically at turn-on and turn-off for a short time.

- *Punch-through* of the collector-base depletion region towards the emitter-contact and towards the subcollector (see Fig. 3.27a). However, this kind of punch-through may be tolerated since it does not mean a loss of current control.

- Generally, HBTs suffer from *thermal runaway*, i. e. the current increases if the temperature increases which may form a positive feedback loop. For HBT switching devices in a CMCD PA, thermal runaway is not expected

to be a problem as the HBT switching devices do not enter the forward-active region theoretically.

(3.27), (3.28), and (3.29) may be employed to calculate the sketched breakdown voltages for HBT devices. Tab. 3.3 compares the breakdown voltages of a Si BJT, GaAs HBT, SiGe HBT, Si MOSFET, and Si LDMOS FET. From this data, we conclude that the LDMOS FET exhibits a breakdown voltage about 2 times higher than for BJTs/HBTs and about 10 times higher than for a conventional MOSFET. The data is in fairly good agreement with the data given in section 3.4.1 for selected commercial devices. Especially the LDMOS FET breakdown voltages agree very well, whereas the breakdown voltages for the BJTs/HBTs appear rather high in Tab. 3.3.

3.4.2.3 pHEMT

The HEMT is in fact a MESFET (metal-semiconductor or Schottky junction FET) that employs an additional hetero-junction in its channel area. The simplified cross-section of an AlGaAs/InGaAs pHEMT is shown in Fig. 3.27b. The hetero-junction allows to separate the donors from the electron-channel, which increases the electron-mobility in the channel and in turn reduces the channel resistance. As for the HBT, this greatly improves the maximum transition frequency f_T. The energy band diagram shows that the energy band-gap difference confines the electrons to a narrow channel, referred to as the two-dimensional electron gas (2DEG). The sheet charge n_s of the 2DEG is controlled by the gate voltage according to $n_s = C_i\,(V_{gs} - V_{th})$ with $C_i = \frac{\varepsilon_s}{d_{2DEG}}$ [34].

Besides the well-known AlGaAs/GaAs HEMT, there is the AlGaAs/InGaAs pHEMT and the AlInAs/GaInAs HEMT (referred to as the InP HEMT). The AlGaAs/InGaAs HEMT is referred to as pHEMT - p for pseudomorphic - as the InGaAs channel-layer avoids lattice dislocations and thus allows a pseudomorphic transition to the AlGaAs barrier material. As the maximum realizable fraction of Al in GaAs or InAs is limited, a further increase in the energy band-gap difference is possible by using a lower band-gap material for the channel layer. The energy band-gap difference is increased from 0.22eV for the conventional AlGaAs/GaAs HEMT to 0.42eV for the pHEMT and to 0.51eV for the InP HEMT. Moreover, the InP HEMT shows a mobility that is twice as high as for the pHEMT [41] and therefore features excellent high-frequency performance. However, the Schottky barrier height of the InP HEMT is only 0.45eV - less than half of the Schottky barrier height of the pHEMT which is 1 eV. This greatly degrades the already-low breakdown voltage of the InP HEMT. pHEMTs feature breakdown voltages of typically 10-15V. The data presented in [42] clearly shows the superiority of the pHEMT over the InP HEMT when it comes to the breakdown voltage. For these reasons, pHEMTs are preferred to InP HEMTs for power amplifiers in the low-GHz range.

To achieve a high output power, the pHEMT of Fig. 3.27b employs a double-hetero-junction structure. The InGaAs layer is bordered by a sheet charge Si doping layer (δ-Si) from above and from below which increases the channel sheet

Table 3.3: Breakdown voltages calculated using (3.27), (3.28), and (3.29) for a Si BJT, GaAs HBT, SiGe HBT, Si MOSFET, and Si LDMOS FET. The doping profile and dimensions were taken from [40] for the BJT/HBTs, and from [38] for the MOSFET/LDMOS FET (however, $N_{Ab} = 10^{-17}\,\mathrm{cm}^{-3}$ is assumed). The critical field values are from [34].

NPN Bipolar

Specifications

			Si BJT	**GaAs HBT**	**SiGe HBT**
Emitter doping	N_{De}	cm^{-3}	5.00E+18	5.00E+18	5.00E+18
Base doping	N_{Ab}	cm^{-3}	1.00E+18	4.50E+19	4.50E+19
Collector doping	N_{Dc}	cm^{-3}	2.00E+16	2.00E+16	2.00E+16
Subcollector doping	N_{Dsc}	cm^{-3}	5.00E+18	5.00E+18	5.00E+18
Base width	W_b	m	8.00E-08	8.00E-08	8.00E-08
Collector width	W_c	m	7.00E-07	7.00E-07	7.00E-07
Critical field for $N=10^{16}cm^{-3}$	E_c	V/cm	4.50E+05	5.00E+05	4.50E+05
Relative permittivity	ε_r	-	11.9	12.4	11.9

Breakdown Voltages

			Si BJT	**GaAs HBT**	**SiGe HBT**
Avalanche breakdown	$BV_{ce,ab}$	V	34.0	42.9	33.3
Punch-through towards base	$BV_{ce,pt,b}$	V	247.9	472599.2	492456.3
Punch-through towards collector	$BV_{ce,pt,c}$	V	7.6	7.1	7.4

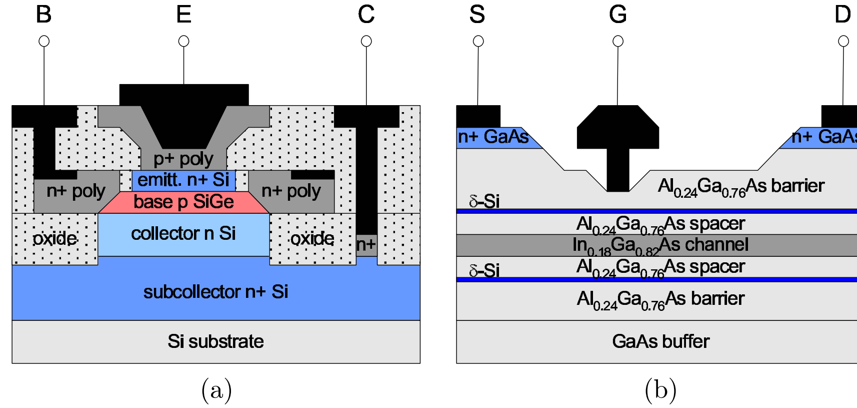
MOSFET/LDMOS FET

Specifications

			Si MOSFET	**Si LDMOS**
Source/drain doping	N_{Dd}	cm^{-3}	5.00E+18	
N-well doping	N_{Dw}	cm^{-3}		1.00E+16
P-bulk/base doping	N_{Ab}	cm^{-3}	1.00E+17	1.00E+17
Channel length	L	m	3.00E-07	3.00E-07
N-well length	L_w	m		4.50E-07
Critical field for $N=10^{16}cm^{-3}$	E_c	V/cm	4.50E+05	4.50E+05
Relative permittivity	ε_r	-	11.9	11.9

Breakdown Voltages

			Si MOSFET	**Si LDMOS**
Avalanche breakdown	$BV_{ds,ab}$	V	6.8	73.3
Punch-through towards source	$BV_{pt,s}$	V	7.0	75.2
Punch-through towards drain	$BV_{pt,d}$	V		1.7



(a) (b)

Figure 3.27: Simplified cross-sections of a SiGe HBT (a, according to [44]) and an AlGaAs/InGaAs pHEMT (b, according to [45]).

charge n_s. A higher n_s leads to an increased channel current density and in turn to an increased output power density.

The breakdown phenomena for HEMT devices are a combination of two effects [42]:

- *Electron tunneling from the gate* (also referred to as *thermionic-field emission*): High-energy electrons may jump over the Schottky barrier and being injected the barrier layer. For the pHEMT, the off-state breakdown is dominated by this effect. Besides constituting a leakage current, the injected electrons may trigger multiplicative impact ionization in the high-field region of the channel towards the drain.

- *Impact ionization in the channel*: For the pHEMT, this is the dominant effect in the on-state. High-energy channel-electrons may cause multiplicative impact ionization in the channel-region towards the drain.

For the pHEMT, it is not possible to easily estimate the off-state breakdown voltage as for the MOSFET/LDMOS FET or HBT. Even fairly simple breakdown voltage models are very cumbersome for hand-calculations [43].

3.4.3 Switching Performance

In order to maximize the PAE of a CMCD PA, the power dissipation in the switching devices must be minimized. The spectrum-limited non-ideal waveforms of Fig. 3.14 (on page 29) allow to identify four different regions for the power dissipation in the switching devices:

- *Turn-on crossbar dissipation* at switch turn-on due to the overlap of V_{ds} and I_{ds}.

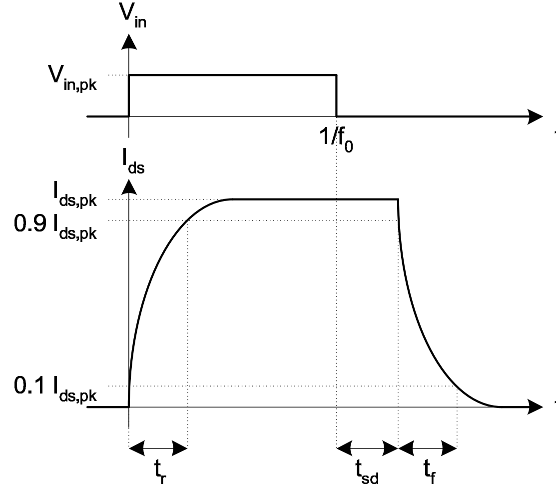


Figure 3.28: Switching transients for a general switching device.

- *On-resistance power dissipation* during the positive half cycle due to a non-zero V_{dsmin}.
- *Turn-off crossbar dissipation* at switch turn-off due to the overlap of V_{ds} and I_{ds}.
- *Off-resistance power dissipation* during the negative half cycle due to off-state leakage current. This type of power dissipation is generally negligible.

Low turn-on and -off crossbar power dissipation asks for fast switching devices: the rise and fall times must be as small as possible. Fig. 3.28 defines three time delays for a general switching device: the rise time t_r, the fall time t_f, and the storage delay t_{sd} at turn-off. The following three sections compare these three time delays for the MOSFET, HBT, and pHEMT.

3.4.3.1 MOSFET/LDMOS FET

To estimate the rise time and fall time for a MOSFET/LDMOS FET we assume that they are dominated by the input RC-delay [36].

Rise time Recalling the MOSFET equivalent circuit of a CMCD PA of Fig. 3.12 (page 27), the input impedance may be approximated as the series combination of R_g with the parallel combination of C_{gs} and C_{gd} as given by (3.15) (page 28). The current flowing into the gate resistor may then be written as $\frac{V_{in}-V_{gs}}{R_g} = (C_{gs} + C_{gd}) \frac{\partial V_{gs}}{\partial t}$. When assuming a unit step of $V_{in,pk}$ for the input voltage V_{in}, this equation may be transformed into the Laplace-domain, solved

for $\mathcal{L}\left\{V_{gs}(t)\right\}$, and transformed back into the time-domain to get $V_{gs}(t) = V_{in,pk}\left(1 - \mathrm{e}^{-\frac{t}{R_g\left(C_{gs}+C_{gd}\right)}}\right)$. Solving $V_{gs}(t)$ for t then yields for the rise time

$$t_r = -R_g\left(C_{gs} + C_{gd}\right)\ln\left(1 - \frac{V_{gs,0.9I_{ds,pk}}}{V_{in,pk}}\right)$$

It remains to determine $V_{gs,0.9I_{ds,pk}}$, the gate-source voltage corresponding to a drain-source current of $0.9I_{ds,pk}$. Assuming that the MOSFET operates in the triode region, the corresponding gate-source voltage $V_{gs,0.9I_{ds,pk}}$ may be determined from $0.9I_{ds,pk} = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{gs,0.9I_{ds,pk}} - V_{th}\right)V_{dsmin} - \frac{1}{2}V_{dsmin}^2\right]$ with V_{dsmin} given by (3.22) (on page 32). The capacitances may be approximated as $C_{gs} = C_{gd} = \frac{1}{2}FWLC_{ox} + FWC_{ov}$.

Storage delay For MOSFET/LDMOS FET devices, the storage delay t_{sd} is zero.

Fall time The fall time is derived in a similar way as the rise time as

$$t_f = -R_g\left(C_{gs} + C_{gd}\right)\ln\left(\frac{V_{gs,0.1I_{ds,pk}}}{V_{in,pk}}\right)$$

3.4.3.2 HBT

As opposed to the MOSFET/LDMOS FET, minority charge carriers are involved in the current transport for a BJT/HBT. According to [46, 47] the switching transients of a BJT/HBT are dominated by storage processes of these minority charge carriers in the base.

Rise time The rise time for a NPN BJT/HBT may be derived from the continuity equation $I_b(t) = \frac{Q_b(t)}{\tau_n} + \frac{\partial Q_b(t)}{\partial t}$ [47]. $I_b(t)$ is the base current, $Q_b(t)$ the stored charge in the base, and τ_n the minority charge carrier lifetime in the base. When assuming a unit step of $I_{b,pk}$ for the input current $I_b(t)$, this equation may be transformed into the Laplace-domain, solved for $\mathcal{L}\left\{Q_b(t)\right\}$, and transformed back into the time-domain to get $Q_b(t) = I_{b,pk}\tau_n\left(1 - \mathrm{e}^{-\frac{t}{\tau_n}}\right)$. With an increasing $Q_b(t)$, the collector current increases with $I_c(t) = \frac{Q_b(t)}{\tau_t}$, where τ_t is the transit time [47]. Substituting $Q_b(t)$ and solving for t then yields for the rise time

$$t_r = -\tau_n \ln\left(1 - \frac{I_{c,pk}}{\beta I_{b,pk}}\right)$$

$I_{c,pk}$ corresponds to $I_{ds,pk}$ in Fig. 3.28 and $\beta = \frac{\tau_n}{\tau_t}$. When driving the BJT/HBT with a voltage source as in the CMCD PA circuit of Fig. 3.7 (on page 20), a difficulty is to estimate $I_{b,pk}$. Using the Ebers-Moll equations with $V_{be} \approx$

V_{bc} (remember the zero-voltage-switching of a CMCD PA) gives an estimate for $I_{b,pk}$ as

$$I_{b,pk} = \left(\mathrm{e}^{\frac{V_{be,pk}}{V_T}} - 1\right) \left[I_{es}\left(1 - \alpha_F\right) + I_{cs}\left(1 - \alpha_R\right)\right]$$

In addition to the above rise time t_r, we must also consider the time for charging the base-emitter capacitor to the turn-on voltage V_{bi}. An approximation for this time may be derived analogously to the rise time for the MOSFET/LDMOS FET to $t_r' = R_{bb'}C_{b'e'} \ln\left(1 - \frac{V_{bi}}{V_{be,pk}}\right)$. However, $t_r \gg t_r^{'}$ is assumed and $t_r^{'}$ neglected.

Storage delay If the BJT/HBT is driven into its saturation region, there is a storage delay t_{sd} as indicated in Fig. 3.28. Before switching $I_b(t)$ from $I_{b,pk}$ to zero, the stored charge in the base is $Q_b(0) = I_{b,pk}\tau_n$. After switching, the stored charge decays from this value with $Q_b(t) = I_{b,pk}\tau_n \mathrm{e}^{-\frac{t}{\tau_n}}$ [47]. However, the collector current $I_c(t)$ remains at its value of $I_{c,pk}$ until the stored charge has fallen to its minimum value for saturation $Q_b(t_{sd}) = I_{c,sat}\tau_t$ [47]. Solving for t_{sd} yields

$$t_{sd} = \tau_n \ln\left(\frac{\beta I_{b,pk}}{I_{c,sat}}\right)$$

We use the Ebers-Moll equations for I_c with $V_{be} = V_{be,pk}$ and $V_{bc} = 0$ to estimate $I_{c,sat}$ to

$$I_{c,sat} = \alpha_F I_{es}\left(\mathrm{e}^{\frac{V_{be,pk}}{V_T}} - 1\right)$$

As evident from the derived equations, to minimize the rise time and the storage delay for BJT/HBT devices the minority charge carrier lifetime τ_n must be as small as possible. However, to maintain the β of the device, the base width must be decreased accordingly.

Fall time After the storage delay t_{sd} the collector current decays with $I_c(t) = I_{c,sat}\mathrm{e}^{-\frac{t}{\tau_n}}$ [47]. Requiring that $I_c(t_f) = 0.1 I_{c,pk}$ and solving for t_f yields

$$t_f = -\tau_n \ln\left(\frac{0.1 I_{c,pk}}{I_{c,sat}}\right)$$

3.4.3.3 HEMT/pHEMT

The rise and fall times for a HEMT/pHEMT may be estimated in the same way as for a MOSFET/LDMOS FET.

Rise time

$$t_r = -R_g\left(C_{gs} + C_{gd}\right)\ln\left(1 - \frac{V_{gs,0.9I_{ds,pk}}}{V_{in,pk}}\right)$$

$V_{gs,0.9I_{ds,pk}}$ may be determined by solving

$$0.9I_{ds,pk} = \mu_n C_i \frac{W}{L}\left[\left(V_{gs,0.9I_{ds,pk}} - V_{th}\right)V_{dsmin} - \frac{1}{2}V_{dsmin}^2\right]$$

V_{dsmin} is derived from (3.22) (on page 32) by substituting C_{ox} with $C_i = \frac{\varepsilon_s}{d_{2DEG}}$. The capacitances may be approximated as $C_{gs} = C_{gd} = \frac{1}{2}WLC_i$.

Storage delay As for the MOSFET/LDMOS FET there is no storage delay for the HEMT/pHEMT.

Fall time The fall time is derived analogously to the rise time as

$$t_f = -R_g\left(C_{gs} + C_{gd}\right)\ln\left(\frac{V_{gs,0.1I_{ds,pk}}}{V_{in,pk}}\right)$$

3.4.3.4 Numerical Examples and Comparison

Tab. 3.4 shows numerical examples of the rise, storage, and fall times for the Ericsson PTF10135 LDMOS FET and the Infineon BFP690 SiGe HBT. Although the numbers base on the first order approximations derived before and although somewhat arbitrary assumptions were made, they may give valuable indications. The most striking difference between the LDMOS FET and the HBT is the storage delay present for the HBT. Moreover, the fall time of the HBT seems to be somewhat larger than that of the LDMOS FET while the rise times of the two devices appear to be of the same order. From the data given in Tab. 3.4, FETs like the LDMOS FET and the HEMT/pHEMT are likely to perform better than BJTs when it comes to switching off as the former do not suffer from minority charge carrier transport delays and recombination effects.

Moreover, FETs show a larger transconductance at turn-on than BJTs. For a short time after turn-on, the FETs still operate in their saturation region and the BJTs in their forward-active region - this is true even if $V_{dsmin} = 0$ as $V_{ds} > V_{gs} - V_{th}$ in the FET case and $V_{be} < V_{bi}$ in the BJT case if the gate/base voltage is close to 0. At this time, the transconductance of the FETs is $g_m = \frac{2I_{ds}}{V_{gs}-V_{th}}$ and the transconductance of the BJTs $g_m = \frac{I_c}{V_T}$. Solving for the I_{ds} and I_c and equating $I_{ds} = I_c$ results in:

$$\frac{g_{m,BJT}}{g_{m,FET}} = \frac{V_{gs} - V_{th}}{2V_T}$$

It follows that $g_{m,FET} > g_{m,BJT}$ as long as $V_{gs} - V_{th} < 2V_T \approx 52\text{mV}$.

Table 3.4: Numerical examples of the rise, storage, and fall times for the Ericsson PTF10135 LDMOS FET and the Infineon BFP690 SiGe HBT. The parameters for the LDMOS FET have been taken from the SPICE LEVEL 3 model in [2] and those for the HBT from the Gummel-Poon model given in the data sheet of the BFP690 HBT.

	PTF10135 LDMOS FET	BFP690 HBT
Rise time t_r	5 ps	10 ps
Storage delay t_{sd}	0	4 ns
Fall time t_f	11 ps	2 ns
$I_{ds,pk} = I_{c,pk}$	100 mA	100 mA
Parameters	$V_{in,pk} = 10\,\mathrm{V}$ $V_{dd} = 20\,\mathrm{V},\ R = 152\,\Omega$	$I_{b,pk} = I_{b,mr} = 20\,\mathrm{mA}$

3.4.4 On-Resistance

The on-resistance of a switching device must be as low as possible to minimize the power dissipation in the switches during the positive half cycle. The on-resistance for MOSFET/LDMOS FET and HEMT/pHEMT devices can be determined from their deep triode I_{ds}-equations to $R_{on,FET} = \frac{1}{g_{m,FET,sat}}$. $g_{m,FET,sat}$ is the FET transconductance in the saturation region. The on-resistance for BJT/HBT devices can be derived from the Ebers-Moll equations:

$$I_c = \alpha_F I_{es}\left(\mathrm{e}^{\frac{V_{be}}{V_T}} - 1\right) - I_{cs}\left(\mathrm{e}^{\frac{V_{be}-V_{ce}}{V_T}} - 1\right)$$

Using the approximation $\mathrm{e}^{-\frac{V_{ce}}{V_T}} \approx 1 - \frac{V_{ce}}{V_T}$ yields

$$R_{on,BJT} = \left(\frac{\partial I_c}{\partial V_{ce}}\right)^{-1} = \frac{V_T}{I_{cs}\mathrm{e}^{\frac{V_{be}}{V_T}}}$$

Interpreting the denominator as I_c results in $R_{on,BJT} = \frac{V_T}{I_c} = \frac{1}{g_{m,BJT,act}}$. Hence, the on-resistance in the saturation region is the inverse of the transconductance in the forward-active region $g_{m,BJT,act}$.

As the transconductance in the forward-active region for a BJT is normally larger than the transconductance in the saturation region for a MOSFET/LDMOS FET, the on-resistance of a BJT can be expected to be lower than the on-resistance of a MOSFET/LDMOS FET.

3.4.5 Discussion and Conclusions from Comparison

3.4.5.1 Discussion of Striking Properties

Tab. 3.2 and Tab. 3.3 indicate that LDMOS FETs remain unrivaled in their high breakdown voltages. As increasing the supply voltage V_{dd} greatly increases the

Table 3.5: Striking properties of the LDMOS FET, HBT, and pHEMT as discussed in this section and in section 3.4.1.

Device	BV	t_{sd}	g_m at turn-on	R_{on}	f_{max}	$I_{ds,mr}$
LDMOS FET	very high	none	high	high	low	high
HBT	very low	possible	low	low	high	low
pHEMT	low	none	high	low	high	high

PAE, a high breakdown voltage is very desirable if the requirement $BV_{ds,off} > \pi V_{dd}$ is a restriction. LDMOS FETs may achieve breakdown voltages up to 65 V. pHEMT devices and HBT devices have a significantly lower breakdown voltage. However, pHEMTs still have an edge over HBTs as they do away with the common-emitter breakdown and the thermal runaway - two effects only HBTs suffer from.

While the rise times of MOSFETs, HBTs, and pHEMTs are expected to be comparable, HBTs potentially have considerably larger turn-off times. They suffer from minority charge carrier transport effects in their base causing a storage delay at turn-off - a delay not present for MOSFETs and pHEMTs. Moreover, the transconductance at turn-on is larger by definition for MOSFETs and pHEMTs than for HBTs.

When it comes to the on-resistance, the HBT devices are expected to show a lower on-resistance than MOSFET/LDMOS FET devices. This advantage may vanish when competing with pHEMTs as they show a considerably higher g_m than MOSFETs/LDMOS FETs. A white paper by Agilent Technologies [48] e.g. says that their E-pHEMTs exhibit a lower on-resistance than HBTs. The sensitivity analysis of section 3.3.4 shows, that it pays more to increase V_{dd} than to decrease R_s in order to maximize the PAE. Therefore, LDMOS FETs may still perform better than HBTs as the larger breakdown voltage may offset the gains in the PAE from a lower on-resistance for HBTs. Tab. 3.5 shows the most striking properties of each device as discussed above and in section 3.4.1.

3.4.5.2 Conclusions for Device Selection

The following shows that the breakdown voltage in conjunction with R_s imposes a fundamental upper limit for the drain-efficiency η and thus for the PAE of a CMCD PA. The maximum achievable η may be derived from (3.23) (on page 32) by assuming $\hat{V}_{in}$ to be infinite. V_{dsmin} in (3.23) then becomes zero and the maximum achievable η becomes

$$\eta_{max} = \frac{81}{4}\frac{1}{27+118r_s},\ r_s = \frac{R_s}{R} \tag{3.30}$$

Substituting R with (3.11) (on page 25) results in the following intuitive expression for r_s:

$$r_s = \frac{9}{32} \frac{R_s P_{out,1}}{V_{dd}^2}$$

However, substituting R with the value given by solving (3.19) (on page 31) for R, results in an even lower maximum achievable η. Using this bulkier expression for R, the maximum achievable drain-efficiencies as a function of $P_{out,1}$ for three sample devices (with different breakdown voltages) taken from Tab. 3.2 (on page 46) were plotted in Fig. 3.29. Note that if $P_{out,1}$ is increased, the maximum achievable drain-efficiencies deteriorate very fast from the maximum value of 0.75 for the low-supply-voltage devices.

An expression for the minimum required supply voltage $V_{dd,min}$ to achieve a certain η_{max} may be derived from (3.30) and (3.19) by setting $V_{dsmin} = 0$ again:

$$V_{dd,min} = \frac{\sqrt{177 P_{out,1} R_s}}{8\sqrt{\eta_{max}(3 - 4\eta_{max})}}$$

Fig. 3.30 plots the above $V_{dd,min}$ as a function of $P_{out,1}$ for $\eta_{max} = 0.70$ and $R_s = 1\,\Omega$. This plot shows that CMCD PAs greatly favor devices with high supply voltages and thus with high breakdown voltages. Tab. 3.6 lists selected $(P_{out,1}, V_{dd,min})$-pairs from this plot. From the data presented in this section and from the discussion on striking properties of the LDMOS FET, HBT, and pHEMT we may conclude:

- A low breakdown voltage severely limits the PAE for CMCD PAs.
- For a CMCD PA at a moderate frequency with a target output power of above 1 W, only LDMOS FETs are an option because of their very high breakdown voltage. However, their performance may degrade if the frequency is high. A target output power of 20 W is the upper limit for the LDMOS FETs of Tab. 3.2. Therefore, for base station CMCD PAs requiring a target output power of 10-20 W, only LDMOS FETs are an option.
- For a CMCD PA at a very high frequency with a target output power of below 1 W, pHEMTs may perform better than LDMOS FETs if the advantage of a very high breakdown voltage for the LDMOS FET is offset by the higher f_T for the pHEMT.

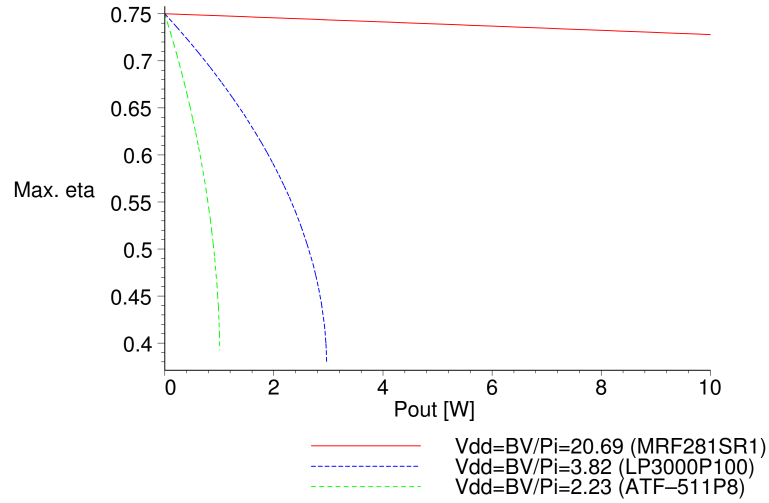


Figure 3.29: Maximum achievable drain-efficiencies η_{max} as a function of $P_{out,1}$ for three sample devices (with different breakdown voltages) taken from Tab. 3.2. R_s is assumed to be 1 Ω for all three devices.

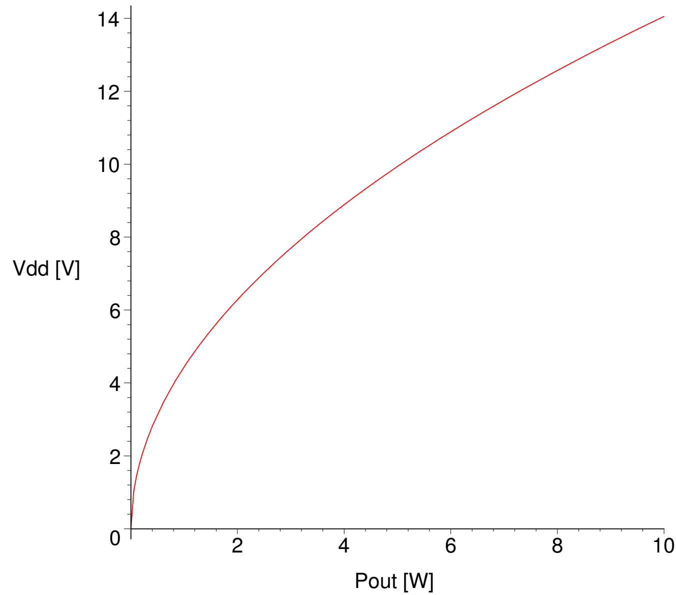


Figure 3.30: Minimum required supply voltage $V_{dd,min}$ as a function of $P_{out,1}$ ($\eta_{max} = 0.70$ and $R_s = 1\,\Omega$).

$P_{out,1}$	$V_{dd,min}$
1 W	4.4 V
3 W	7.7 V
10 W	14.1 V
20 W	19.9 V

Table 3.6: Minimum required supply voltage $V_{dd,min}$ for selected values of $P_{out,1}$ ($\eta_{max} = 0.70$ and $R_s = 1\,\Omega$).

Chapter 4

Device Evaluation by Simulation

4.1 Simulation Circuit

To assess the performance of commercially available devices in a CMCD PA, harmonic-balance simulations at 900 MHz, 1.8 GHz, and 5.8 GHz for an ideal switch model, for three packaged devices, and for two non-packaged devices were performed. The packaged devices include the Motorola MRF281SR1 LDMOS FET, the Filtronic LP3000P100 pHEMT, and the Infineon BFP690 SiGe HBT of Tab. 3.2 (on page 46). The non-packaged devices include a pHEMT in Triquint's TQPHT process and a InGaP HBT in Triquint's TQHBT2 process.

Fig. 4.1 and Fig. 4.2 depict the ADS schematics used for all harmonic-balance simulations (here depicted for the MRF281SR1 LDMOS FET). Note that the devices are driven by an ideal voltage source in order to eliminate the impact of the input matching circuitry that would have to be used if the devices were driven by a non-ideal voltage source. The tank capacitor and inductor, the DC feed inductors as well as the input and output balun transformers are further assumed to be ideal (or almost ideal for the DC feed inductors).

Choosing the tank capacitor and inductor The tank capacitor and inductor are determined by the equations given in section 3.2.2.3. Q_{loaded} is determined by the assumed realizable range of the tank capacitor ($C = 1\text{pF} \ldots 10\text{nF}$), by the assumed realizable range of the tank inductor ($L = 0.5\text{nH} \ldots 100\text{nH}$), and by the assumed maximum current rating of the tank inductor ($I_{L,mr} = 5$ A). Note that $I_{L,mr} = 5$ A is a rather large value for commercially available packaged chip-inductors. The actually employed tank capacitor is $C - C_{ds,comp}$. $C_{ds,comp}$ is the transistor drain-source capacitance that contributes to the tank capacitance. $C_{ds,comp}$ is a tuning value.

Stabilizing the PA with R_b Instability may result from drain-to-gate coupling through the drain-gate capacitor C_{gd}. With drain-to-gate coupling, the input resistance of the PA may become negative. To prevent this instability, a ballast resistor R_b is added at the PA input as depicted in Fig. 4.2. The value of the ballast resistor R_b was determined for each CMCD PA to lift the input resistance to at least $R_{in} = 100\,\mathrm{m}\Omega$ over the interesting range of the input voltage amplitudes.

Optimization Guidelines Whenever the device or the frequency is changed the following variables may be optimized to yield the maximum PAE:

- $V_{g,bias}$, the gate bias voltage
- R_{tank}, the total tank resistance (previously denoted as R)
- $C_{ds,comp}$, the transistor drain-source capacitance that contributes to the tank capacitance
- $\hat{V}_{in}$, the input voltage amplitude

For all simulations, the following procedure was followed:

1. Set the supply voltage to $V_{dd} = \frac{BV_{ds,off}}{\pi}$.
2. Determine initial values for $V_{g,bias}$, R_{tank}, and $C_{ds,comp}$
   (a) Set $V_{g,bias}$ to the V_{gs} in the transistor transfer characteristic that yields a drain-source current of $I_{ds} \approx 1$ mA for $V_{ds} = 0.05BV_{ds,off}$.
   (b) Set R_{tank} to $R_{tank,nom}$ given in Fig. 4.1.
   (c) Set $C_{ds,comp}$ to the output capacitance of the transistor for $V_{d,bias} = 2V_{dd}$ and $V_{g,bias} \ll V_{th}$ determined by an AC simulation. Note that the output capacitance of the transistor is heavily dependent on the drain and gate voltages.
3. Sweep $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$ over reasonable ranges including the before established values thereby optimizing the PAE. Set $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$ to values that yield a PAE deviating by no more than 1 % from the maximum PAE. This allows to trade 1 % of the PAE for a possibly substantial increase in the output power $P_{out,1}$ or the gain G as suggested in section 3.3.4.2. Note that the optimum $\hat{V}_{in}$ changes substantially when sweeping $V_{g,bias}$. Therefore sweeping $\hat{V}_{in}$ with $V_{g,bias}$ as parameter better allows to select the optimum $V_{g,bias}$. Fig. 4.3, Fig. 4.4, and Fig. 4.5 show sweeps of $V_{g,bias}$, R_{tank}, and $C_{ds,comp}$ as well as corresponding sweeps of $\hat{V}_{in}$ with $V_{g,bias}$, R_{tank}, and $C_{ds,comp}$ as parameter for MRF281SR LDMOS FETs at 900 MHz to illustrate this. Note that a $V_{g,bias}$ (in this case of 5 V) slightly higher than V_{th} (in this case determined to be 3.75 V) results not only in a higher PAE but also in a higher output power. This behavior is generally encountered for all devices simulated.

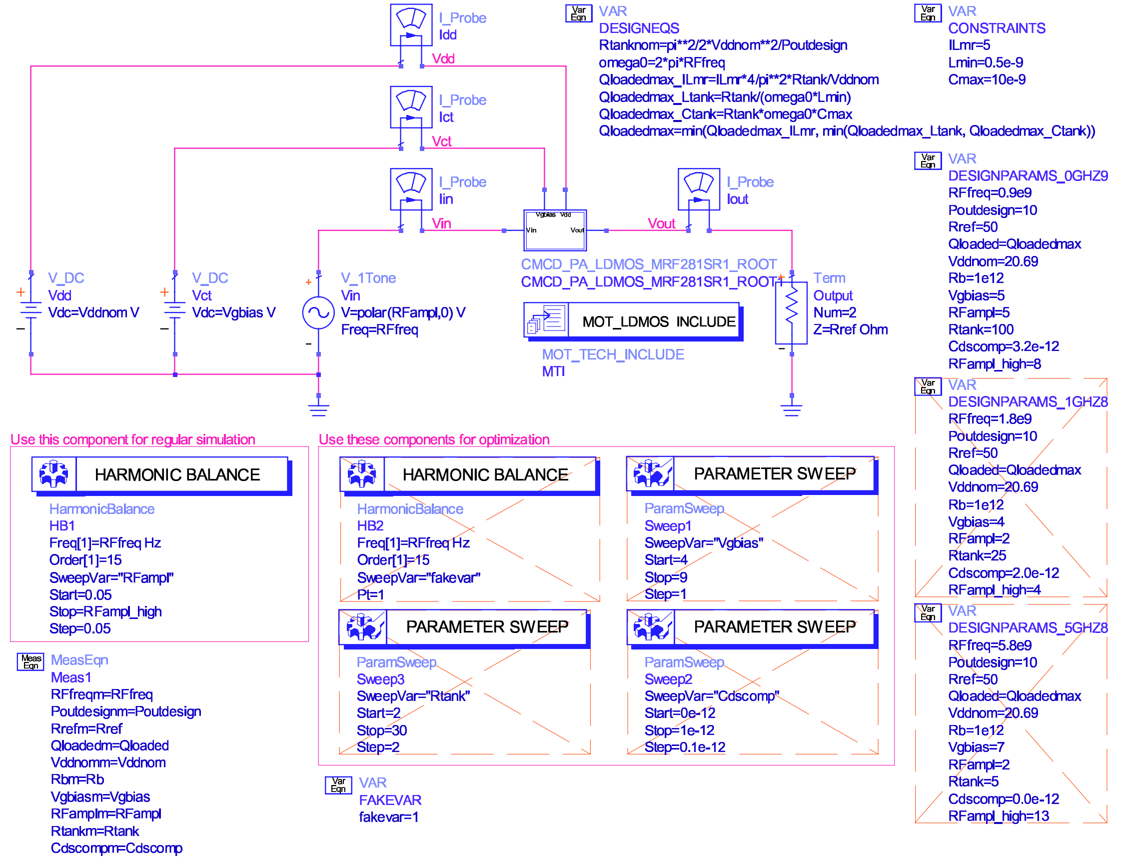


Figure 4.1: ADS schematic for the harmonic-balance simulations. See Fig. 4.2 for the CMCD_PA_LDMOS_MRF281SR1 block.

4. If the input resistance becomes negative in the interesting range of input voltage amplitudes $\hat{V}_{in}$, lower the ballast resistor R_b to lift the input resistance to at least $R_{in} = 100\,\mathrm{m}\Omega$. Adjusting R_b often means a change in the optimum $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$ values, which necessitates going back to point 3.

4.2 Switch Simulations

Initially, simulations using switches instead of transistors were performed. The on-resistance of the switches was set to $R_{on} = 1\ \Omega$ and the off-resistance to $R_{off} = 1\ \mathrm{T}\Omega$. The switches feature a continuous transition from their on-state to their off-state over a input voltage range of $V_{tran} = 0.05$ V. Fig. 4.6 shows

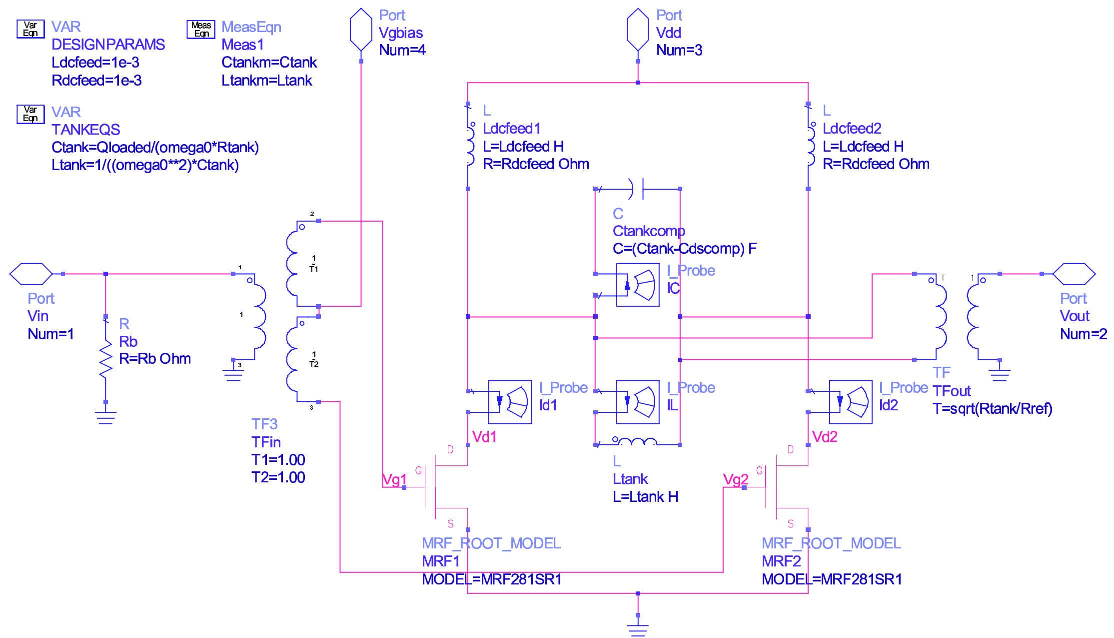
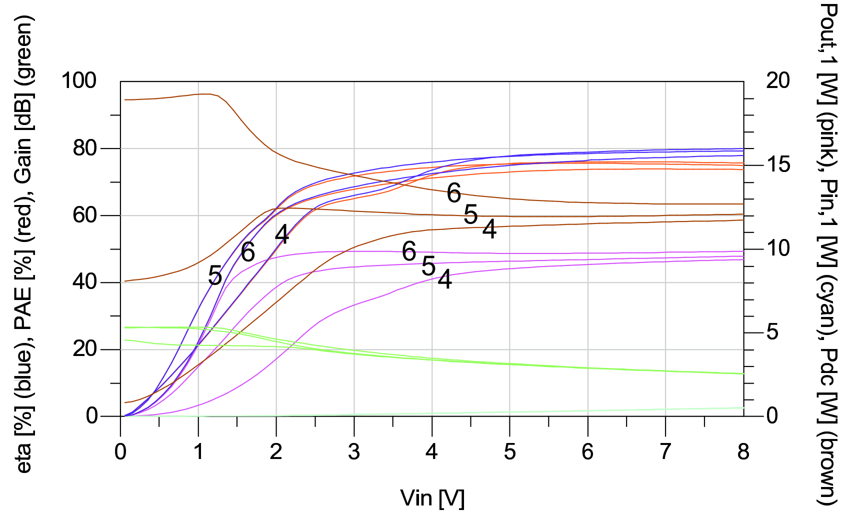
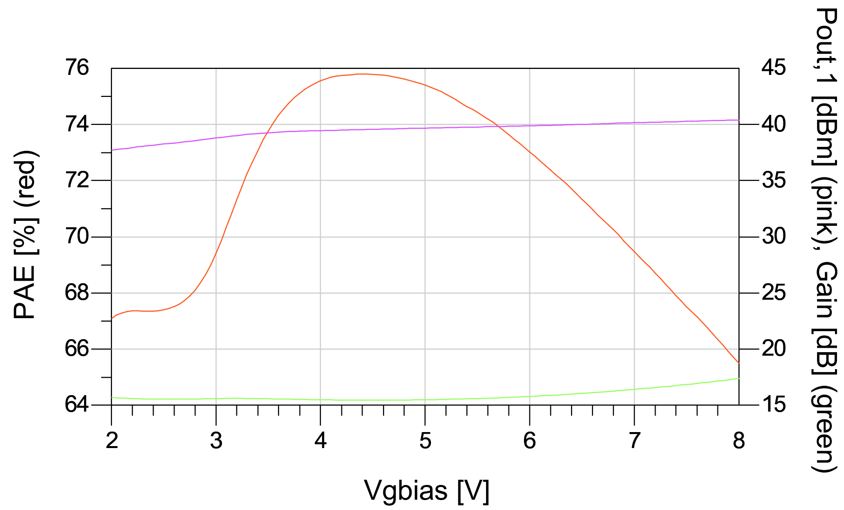


Figure 4.2: ADS schematic for the CMCD_PA_LDMOS_MRF281SR1 block of Fig. 4.1.

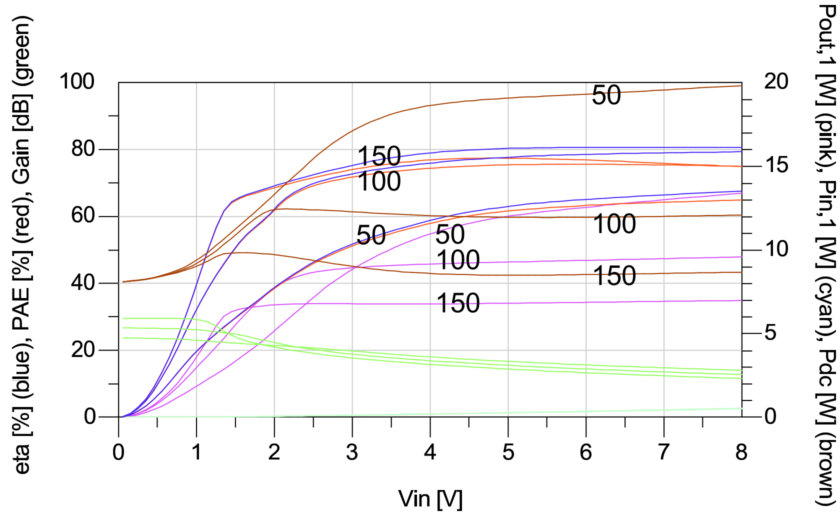


(a)

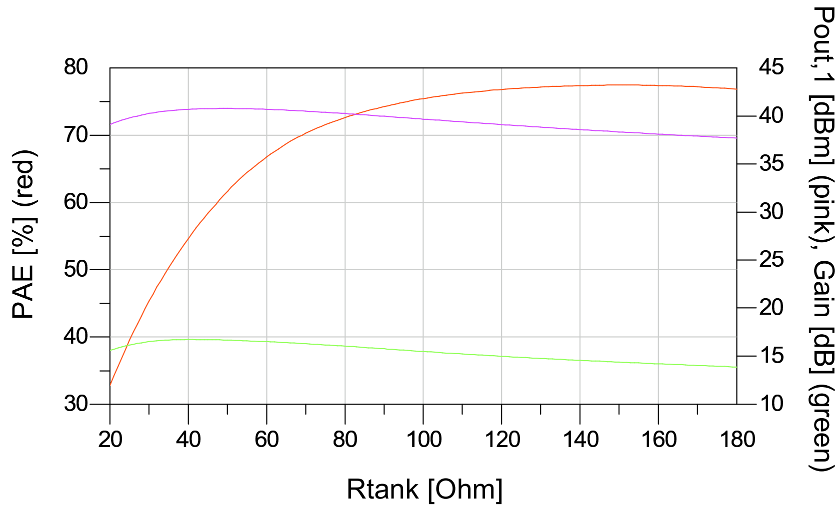


(b)

Figure 4.3: Sweep of $\hat{V}_{in}$ with $V_{g,bias}$ as parameter (a) and sweep of $V_{g,bias}$ (b) for MRF281SR LDMOS FETs at 900 MHz. The numbers in (a) refer to $V_{g,bias}$ [V]. Note that all sweeps were made at the otherwise optimum values of $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$.

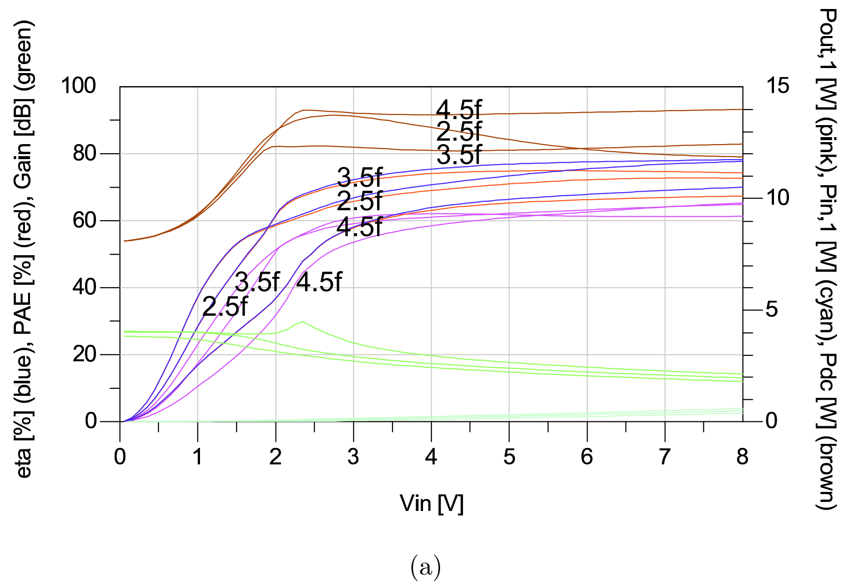


(a)

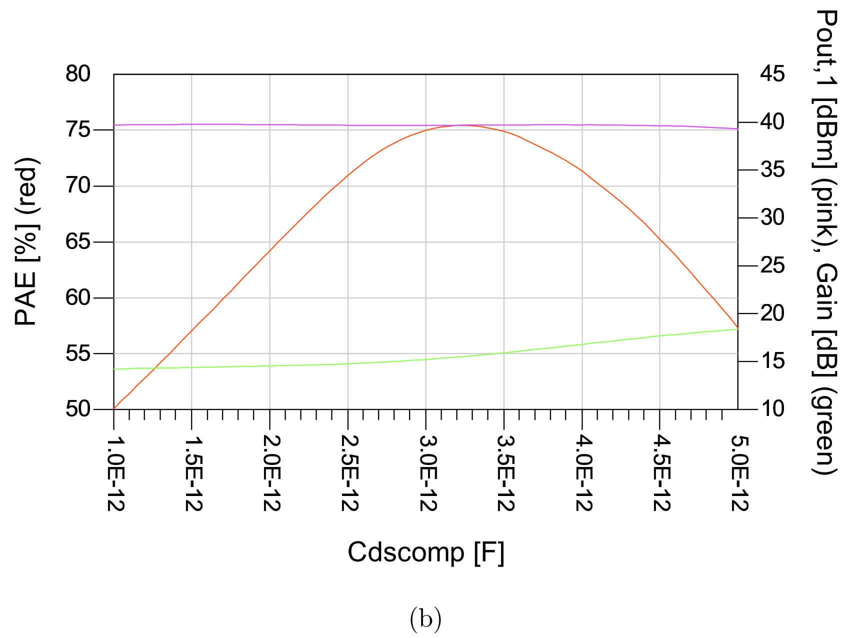


(b)

Figure 4.4: Sweep of $\hat{V}_{in}$ with R_{tank} as parameter (a) and sweep of R_{tank} (b) for MRF281SR LDMOS FETs at 900 MHz. The numbers in (a) refer to R_{tank} [Ω]. Note that all sweeps were made at the otherwise optimum values of $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$.



(a)



(b)

Figure 4.5: Sweep of $\hat{V}_{in}$ with $C_{ds,comp}$ as parameter (a) and sweep of $C_{ds,comp}$ (b) for MRF281SR LDMOS FETs at 900 MHz. The numbers in (a) refer to $C_{ds,comp}$ [F]. Note that all sweeps were made at the otherwise optimum values of $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$.

the results of HB simulations for this set-up. Reducing the on-resistance from $R_{on} = 1\,\Omega$ to $R_{on} = 100\,\mathrm{m}\Omega$ raises the maximum PAE from $PAE = 97.6\%$ to $PAE = 99.7\%$. Reducing R_{on} below $100\,\mathrm{m}\Omega$ and V_{tran} below 0.05 V prevents HB simulations from converging. Q_{loaded} only starts degrading the efficiency significantly if it drops below 2. For $Q_{loaded} = 2$ (and $R_{on} = 1\,\Omega$), the efficiency is still 96.8 %.

Note that the voltage waveform at marker m2 exhibits spikes at turn-on and -off which are not present in the voltage waveform at marker m1. These spikes result from the lower slope of the input voltage at turn-on and -off for lower input voltage amplitudes as V_{tran} is held constant at 0.05 V. A lower slope of the input voltage amplitude at turn-on and -off means that at these times the current $2I_{dc}$ is imposed on a high-resistance switch, which causes the observed voltage spikes. This behavior will also be observed more or less pronounced in simulations with packaged transistors.

4.3 Packaged Device Simulations

The circuit of Fig. 4.2 was simulated employing

- Motorola MRF281SR1 LDMOS FETs,
- Filtronic LP3000P100 pHEMTs, and
- Infineon BFP690 SiGe HBTs

at 900 MHz, 1.8 GHz, and 5.8 GHz. Refer to Tab. 3.2 (on page 46) for the properties of these packaged devices. Each circuit was optimized according to the procedure outlined in section 4.1. The results of this optimization are presented in Tab. 4.1.

Motorola MRF281SR1 LDMOS FET Fig. 4.7 and Fig. 4.8 show the results of the HB simulations for this device at 900 MHz and 1.8 GHz, respectively. The output power of the MRF281SR1 is the highest one attained by any of the packaged devices investigated. At the same time, the PAE at 900 MHz and at 1.8 GHz is high. However, at 5.8 GHz, the PAE drops to zero and the MRF281SR1 becomes useless. Note that very similar results were achieved from simulations with the Ericsson PTF10135 SPICE LEVEL 3 model (at 900 MHz: $PAE = 74.1$ %, $P_{out,1} = 10.6\,\mathrm{W}$, $G = 11.2\,\mathrm{dB}$; at 1.8 GHz: $PAE = 69.3$ %, $P_{out,1} = 17.6\,\mathrm{W}$, $G = 11.3\,\mathrm{dB}$; useless at 5.8 GHz).

Filtronic LP3000P100 pHEMT Fig. 4.9 and Fig. 4.10 show the results of the HB simulations for this device at 900 MHz and 5.8 GHz, respectively. While the PAE of the LP3000P100 is significantly lower than the PAE of the MRF281SR1 at 900 MHz and 1.8 GHz, the LP3000P100 still attains a PAE of 34.1 % at 5.8 GHz. However, the general performance measured as the attainable PAE and attainable output power is disappointing. Three reasons are identified for this in the following:

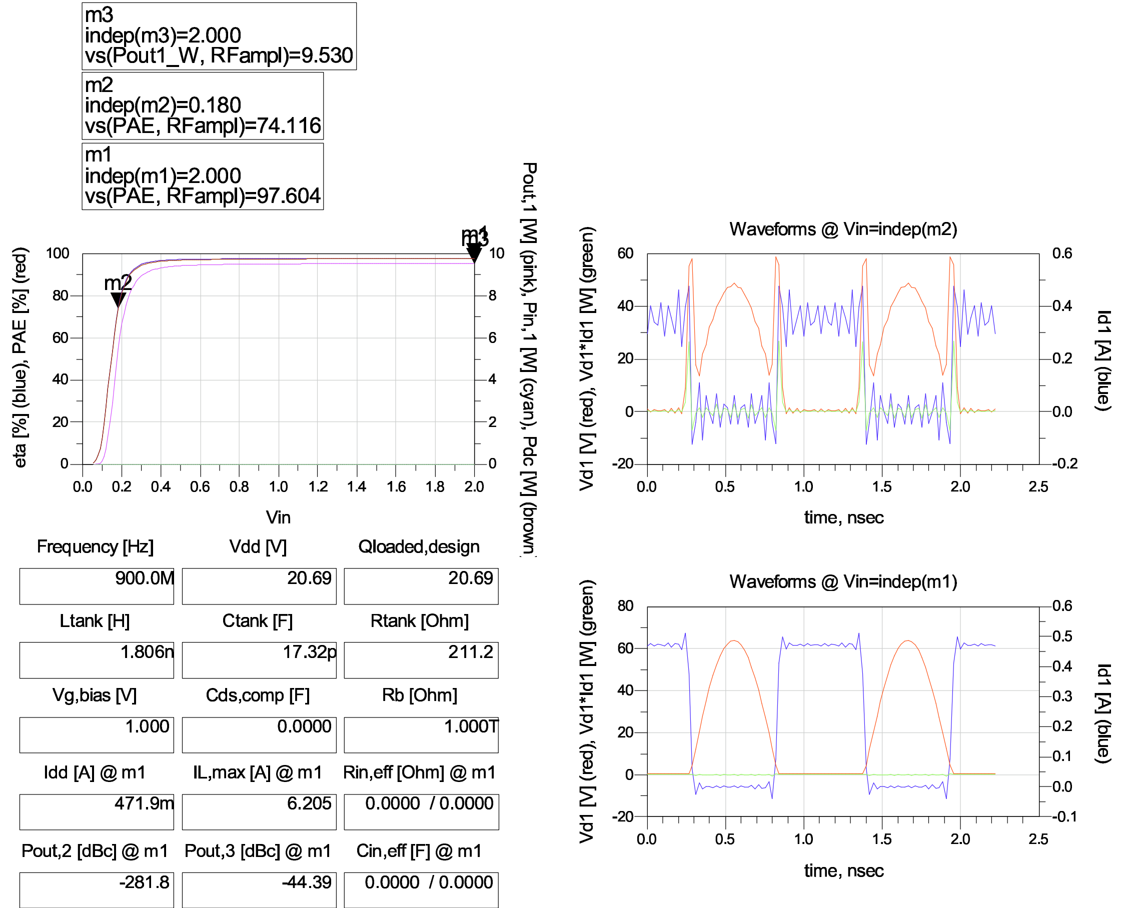


Figure 4.6: Results of HB simulations for switches with an on-resistance of 1 Ω at 900 MHz (see Fig. 4.2 for circuit).

- *Low breakdown voltage*: Recall from Fig. 3.29 (on page 60) that the maximum achievable drain-efficiency degrades very quickly as a function of the output power for the LP3000P100. E.g. for $P_{out,1} = 1.3\,\mathrm{W}$, $\eta_{max} =$ 65.6 % if R_s is assumed to be 1 Ω, which severely limits the PAE. The DC output characteristic of the LP3000P100 in Fig. 4.11 shows that the assumption of $R_s = 1\,\Omega$ is a reasonable assumption for the LP3000P100.

- *Drain-induced barrier lowering (DIBL)*: Note from the instantaneous power dissipation waveform $V_d I_d$ of Fig. 4.9 (green curve) that there is a substantial amount of DC power dissipation during cut-off. This may be explained when looking at the DC output characteristic of the LP3000P100 in Fig. 4.11. If the gate-source voltage is only slightly below the threshold voltage the device may start conducting again for high drain-source voltages. This behavior is called drain-induced barrier lowering (DIBL) and is responsible for the DC power dissipation during cut-off in the CMCD PA.

- *High on-resistance for $V_{gs} \approx V_{th}$ at very low V_{ds}*: Comparing the DC output characteristic of the LP3000P100 in Fig. 4.11 with the DC output characteristic of the MRF281SR1 in Fig. 4.12 for a very low V_{ds} (lower plots), we note that the on-resistance of the LP3000P100 is potentially substantially higher than the on-resistance of the MRF281SR1 for a very low V_{ds}. Therefore, as shown by the instantaneous power dissipation waveform $V_d I_d$ of Fig. 4.9 (green curve), a substantial amount of DC power is dissipated at turn-on and -off.

Infineon BFP690 SiGe HBT Fig. 4.13 shows the results of the HB simulations for this device at 1.8 GHz. HB simulations at 900 MHz were impossible as the HB engine of ADS was reporting an overflow in the KCL check for reasonable high values of $\hat{V}_{in}$. The discontinuity in the efficiency-plot of Fig. 4.13 renders the attained results very questionable. The HB engine of ADS appears to have serious difficulties in simulating a CMCD PA with a Gummel-Poon model.

4.4 Non-Packaged Device Simulations

The circuit of Fig. 4.2 was simulated employing

- pHEMTs of Triquint's TQPHT process, and

- InGaP HBTs of Triquint's TQHBT2 process

at 900 MHz, 1.8 GHz, and 5.8 GHz. Refer to Tab. 4.2 for an overview of some relevant parameters of these processes. Each circuit was optimized according to the procedure outlined in section 4.1. The results of this optimization are presented in Tab. 4.3.

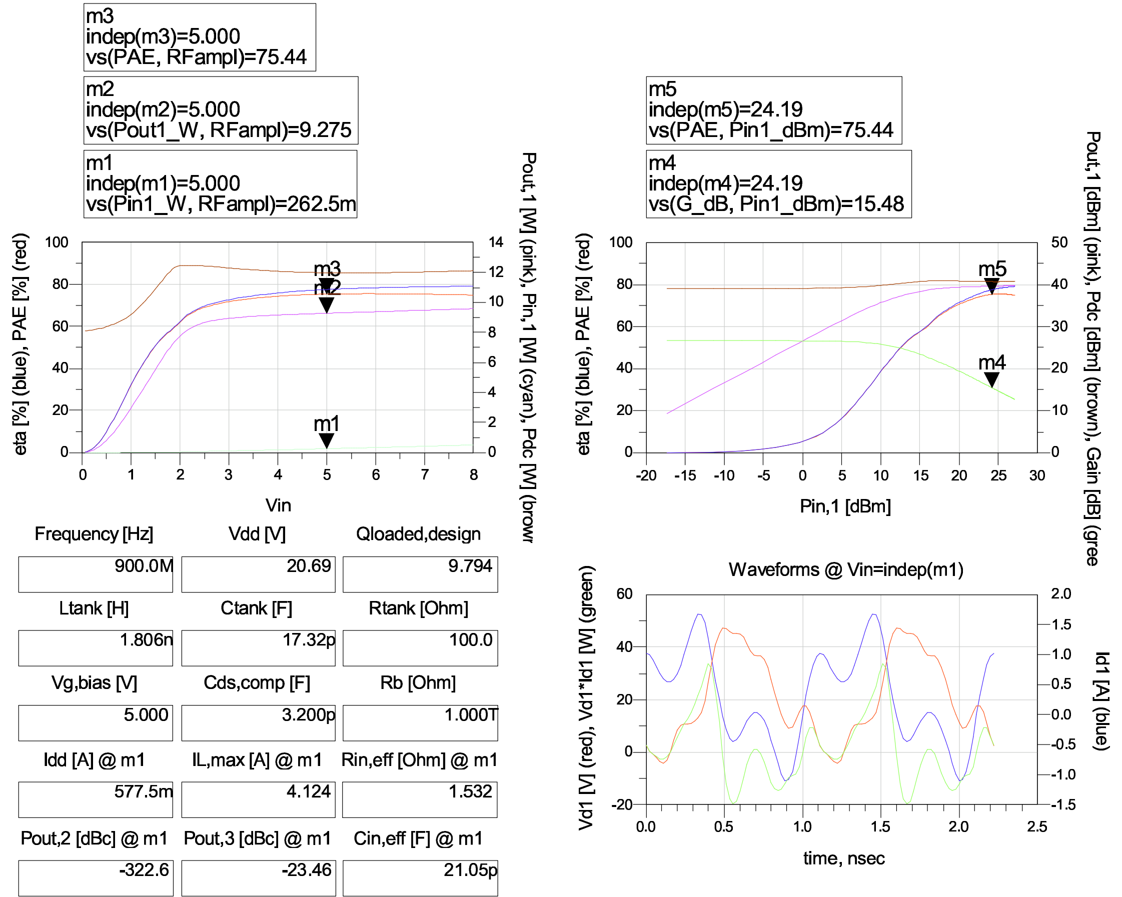


Figure 4.7: Results of HB simulations for *MRF281SR LDMOS FETs* at 900 MHz (see Fig. 4.2 for circuit).

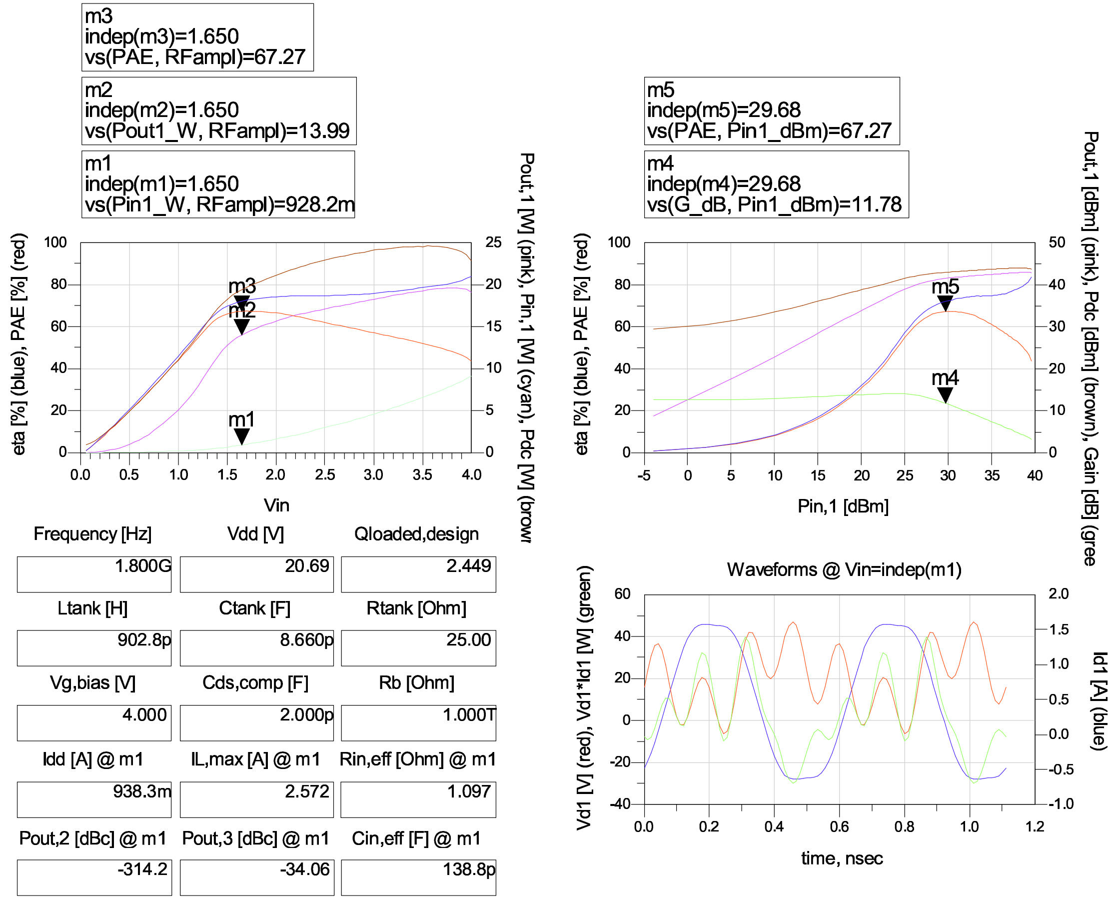


Figure 4.8: Results of HB simulations for *MRF281SR LDMOS FETs* at 1.8 GHz (see Fig. 4.2 for circuit).

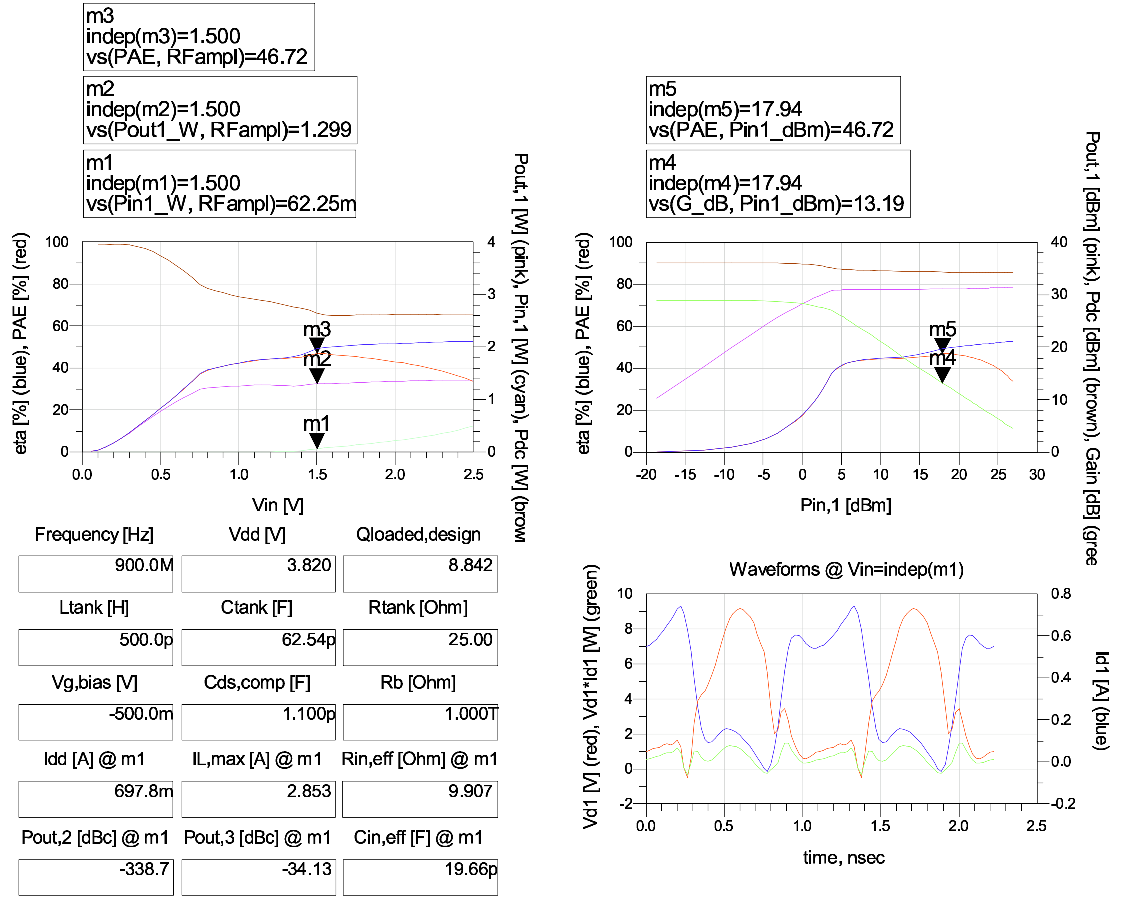


Figure 4.9: Results of HB simulations for *LP3000P100 pHEMTs* at 900 MHz (see Fig. 4.2 for circuit).

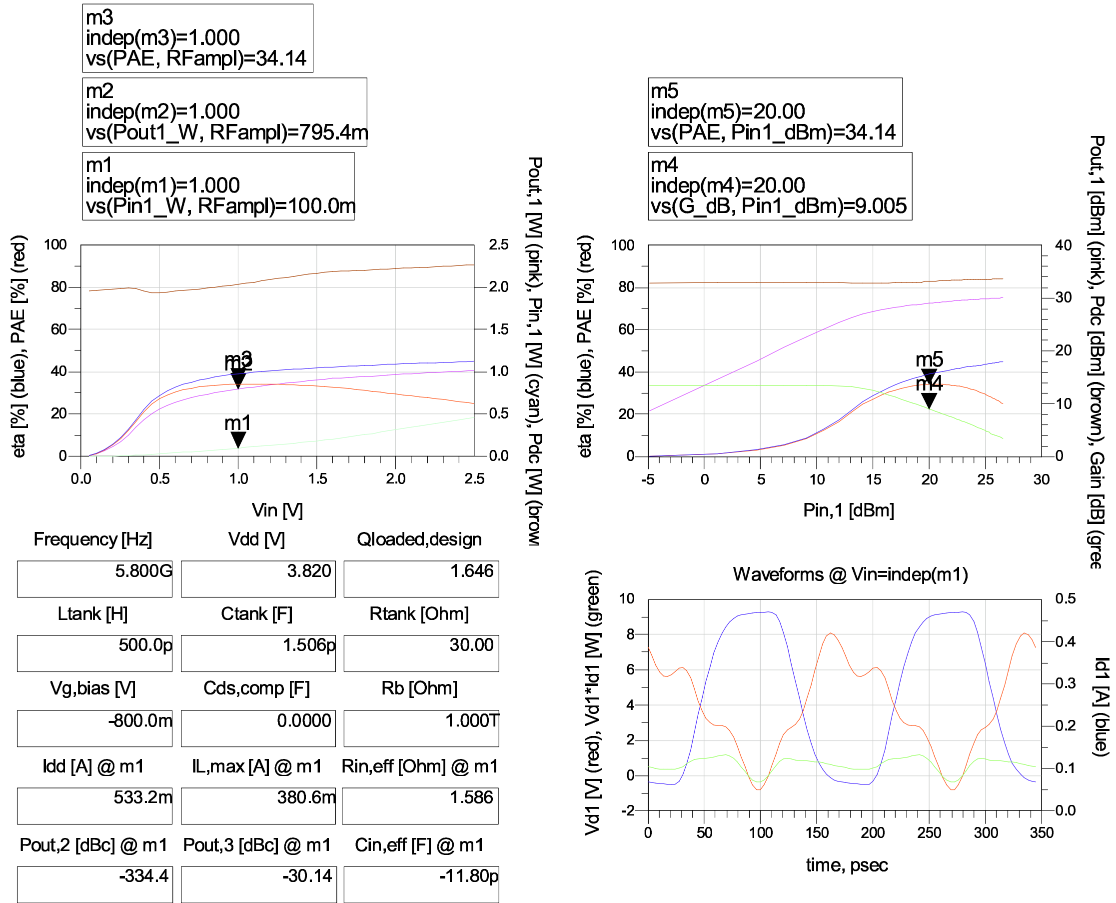


Figure 4.10: Results of HB simulations for *LP3000P100 pHEMTs* at 5.8 GHz (see Fig. 4.2 for circuit).

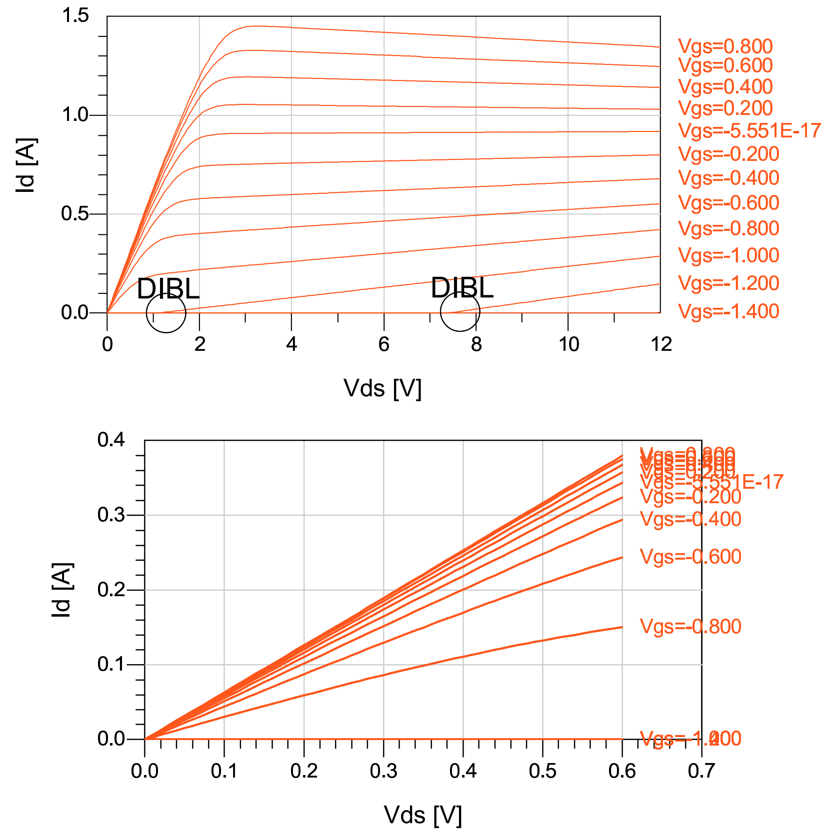


Figure 4.11: DC output characteristics of the LP3000P100 pHEMT for two different ranges of V_{ds}. Note that the upper limit of V_{ds} in the lower plot corresponds to about $0.015BV_{ds,off}$.

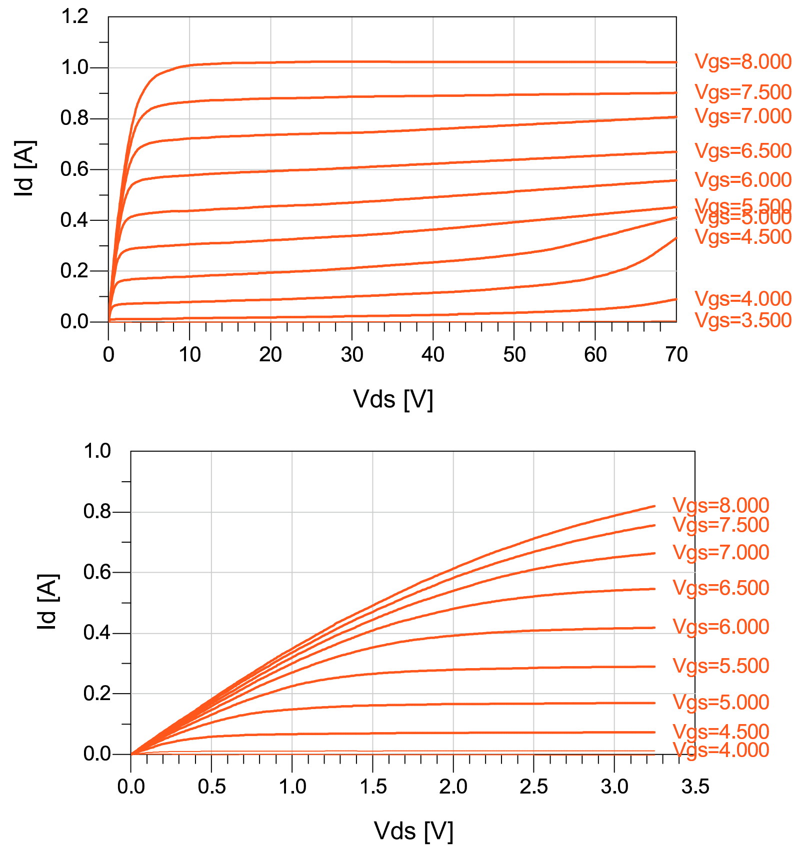


Figure 4.12: DC output characteristics of the MRF281SR1 LDMOS FET for two different ranges of V_{ds}. Note that the upper limit of V_{ds} in the lower plot corresponds to about $0.015BV_{ds,off}$.

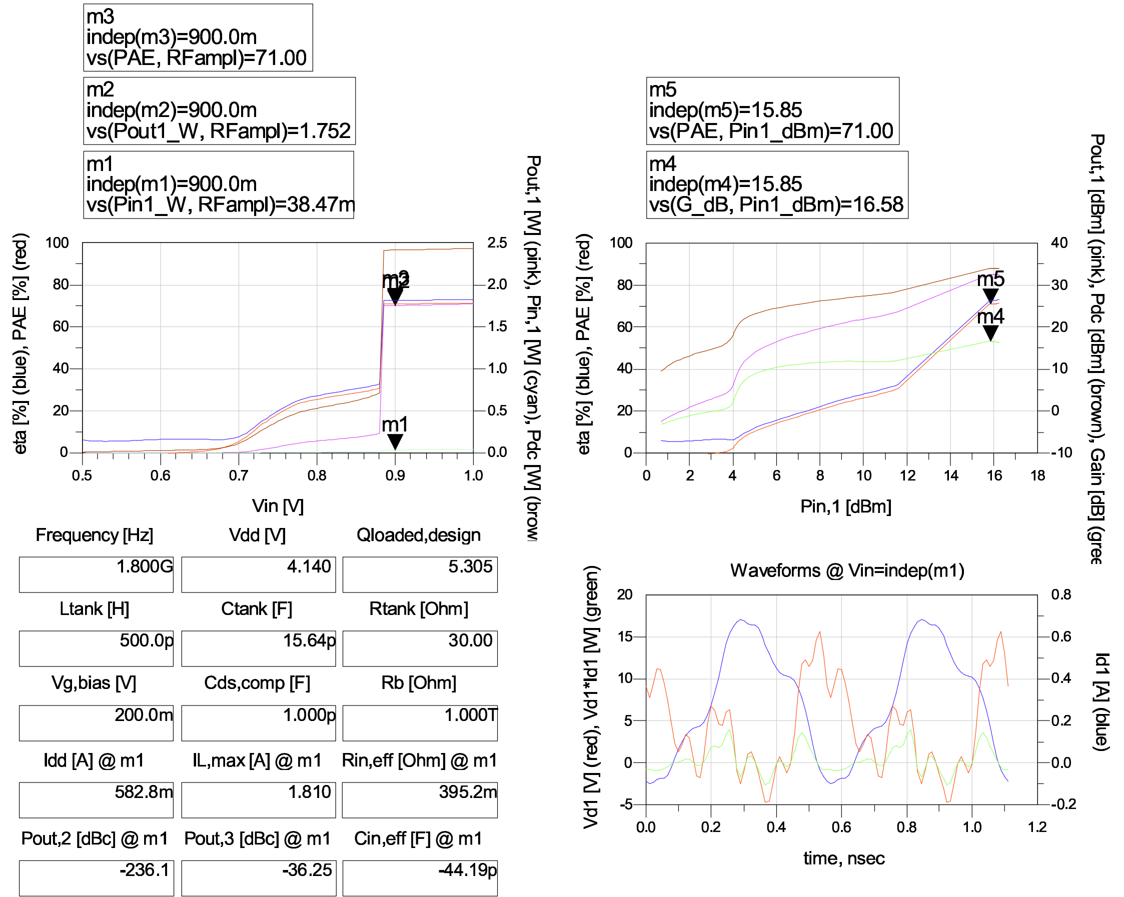


Figure 4.13: Results of HB simulations for *BFP690 SiGe HBTs* at 1.8 GHz (see Fig. 4.2 for circuit).

Freq. [GHz]	PAE [%]	$P_{out,1}$ [W]	G [dB]
Motorola MRF281SR1 LDMOS FET, $V_{dd} = 20.69$ V, Root model			
0.9	75.4	9.3	15.5
1.8	67.3	14.0	11.8
5.8	0		
Filtronic LP3000P100 AlGaAs/InGaAs pHEMT, $V_{dd} = 3.82$ V, Curtice3 model			
0.9	46.7	1.3	13.2
1.8	41.6	1.2	17.7
5.8	34.1	0.8	9.0
Infineon BFP690 SiGe HBT, $V_{dd} = 4.14$ V, Gummel-Poon model			
0.9	no simulation possible		
1.8	71.0	1.75	16.6
5.8	0		

Table 4.1: Maximum PAE, output power $P_{out,1}$, and gain G of the investigated packaged devices.

TQPHT pHEMT As the transistor size is variable now, a reasonable transistor size has to be chosen. The applications of interest are 10 W of output power at 900 MHz and 1.8 GHz, and 3 W of output power at 5.8 GHz. (3.5) (on page 18) together with (3.6) gives I_{dc} for these output powers. Remember that each device is required to sink $2I_{dc}$. The number of fingers is now increased until the DC output characteristic allows to sink a current of $2I_{dc}$ for $V_{ds} = 0.01BV_{ds,off}$ and $V_{gs} \approx 0.8$ V. $V_{gs} \approx 0.8$ V is about the Schottky diode turn-on voltage. This procedure results in 250 fingers for a 10 W output power device, and in 75 fingers for a 3 W output power device. Fig. 4.14 and Fig. 4.15 show the results of the HB simulations for the 10 W-device at 900 MHz and and for the 3 W-device at 5.8 GHz, respectively. Even at 5.8 GHz, the TQPHT pHEMTs achieve a PAE of around 90 %. The reason why the TQPHT pHEMTs perform much better than the LP3000P100 pHEMTs primarily is a 10-20 times lower on-resistance for $V_{gs} \approx V_{th}$ at very low V_{ds}. Note that by increasing the number of fingers further, the PAE increases up to 99 %. However, it remains questionable whether the TOM3 model scales correctly. Moreover, the TOM3 model often aborts with the error message 'SYM error: attempted logarithm of zero'.

TQHBT2 InGaP HBT The current $2I_{dc}$ that has to be sinked is determined as outlined for the TQPHT pHEMT. However, it is not the DC output characteristic that limits the sinkable current for the TQHBT2 HBT but the maximum allowable current density as given by the design manual. This limitation results in a HBT-multiplicity of 19 for the 10 W output power device, and

Triquint TQPHT AlGaAs/InGaAs pHEMT		Triquint TQHBT2 InGaP HBT	
Gate Length	0.5 μm	Emitter Size	3 x 3 μm x 45 μm
Pinch-Off Volt.	-0.8 V	Turn-On Volt.	1.15 V
f_T	30 GHz	f_T	28 GHz
$BV_{ds,off}$	17 V	$BV_{ds,off}$	21 V
I_{dss}	200 mA/μm	$I_{ds,mr}$	80 mA

Table 4.2: Some relevant parameters of Triquint's TQPHT and TQHBT2 processes.

Freq. [GHz]	PAE [%]	$P_{out,1}$ [W]	G [dB]	Transistor Size	Active Area
Triquint TQPHT AlGaAs/InGaAs pHEMT, $V_{dd} = 5.41$ V, TOM3 model					
0.9	90.8	10.3	20.2	250 x 50 μm	0.026 mm^2
1.8	89.9	10.0	16.5	250 x 50 μm	0.026 mm^2
5.8	90.7	3.0	11.9	75 x 50 μm	0.008 mm^2
Triquint TQHBT2 InGaP HBT, $V_{dd} = 6.68$ V, Gummel-Poon model					
0.9	94.8	10.4	21.5	Multiplicity = 19	0.049 mm^2
1.8	93.2	10.8	19.3	Multiplicity = 19	0.049 mm^2
5.8	87.6	3.7	12.5	Multiplicity = 6	0.016 mm^2

Table 4.3: Maximum PAE, output power $P_{out,1}$, and gain G of the investigated non-packaged devices.

in a HBT-multiplicity of 6 for the 3 W output power device. In the case of the TQPHT PHEMT, the maximum allowable current density is high enough not be a restriction. Fig. 4.14 and Fig. 4.17 show the results of the HB simulations for the 10 W-device at 900 MHz and the 3 W-device at 5.8 GHz, respectively. Even at 5.8 GHz, the TQHBT2 HBTs achieve a PAE of around 90 %. The storage delay t_{sd}, that was shown in section 3.4.3 to have a potentially very detrimental impact on the efficiency of a CMCD PA, is not pronounced neither for the BFP690 HBT CMCD PA circuits investigated nor for the TQHBT2 HBT CMCD PA circuits investigated as the corresponding I_{ds}-waveforms show. That the storage delay t_{sd} is modeled by the Gummel-Poon model was verified by different HB simulations, though. As for the BFP690 HBT, the HB engine of ADS kept reporting an overflow in the KCL check, which made these simulations very time-consuming.

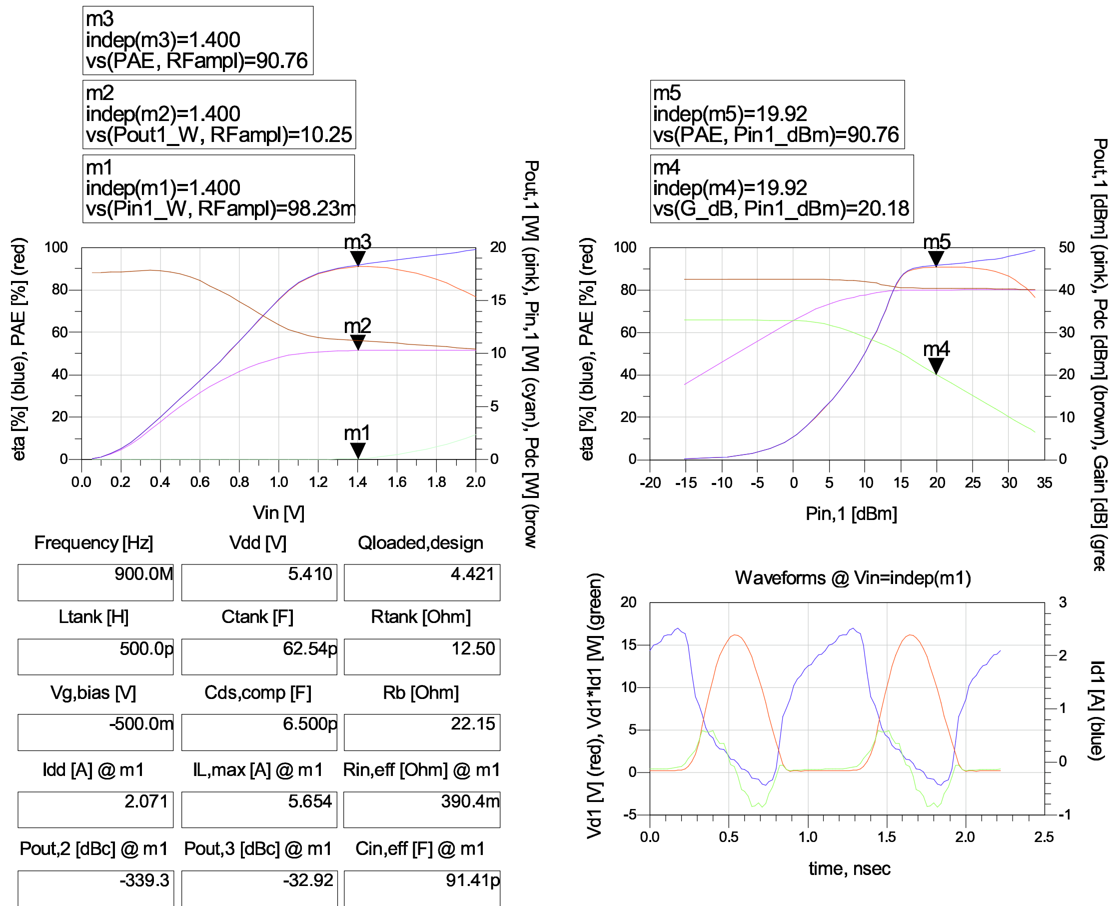


Figure 4.14: Results of HB simulations for *TQPHT pHEMTs* (250 fingers) at 900 MHz (see Fig. 4.2 for circuit).

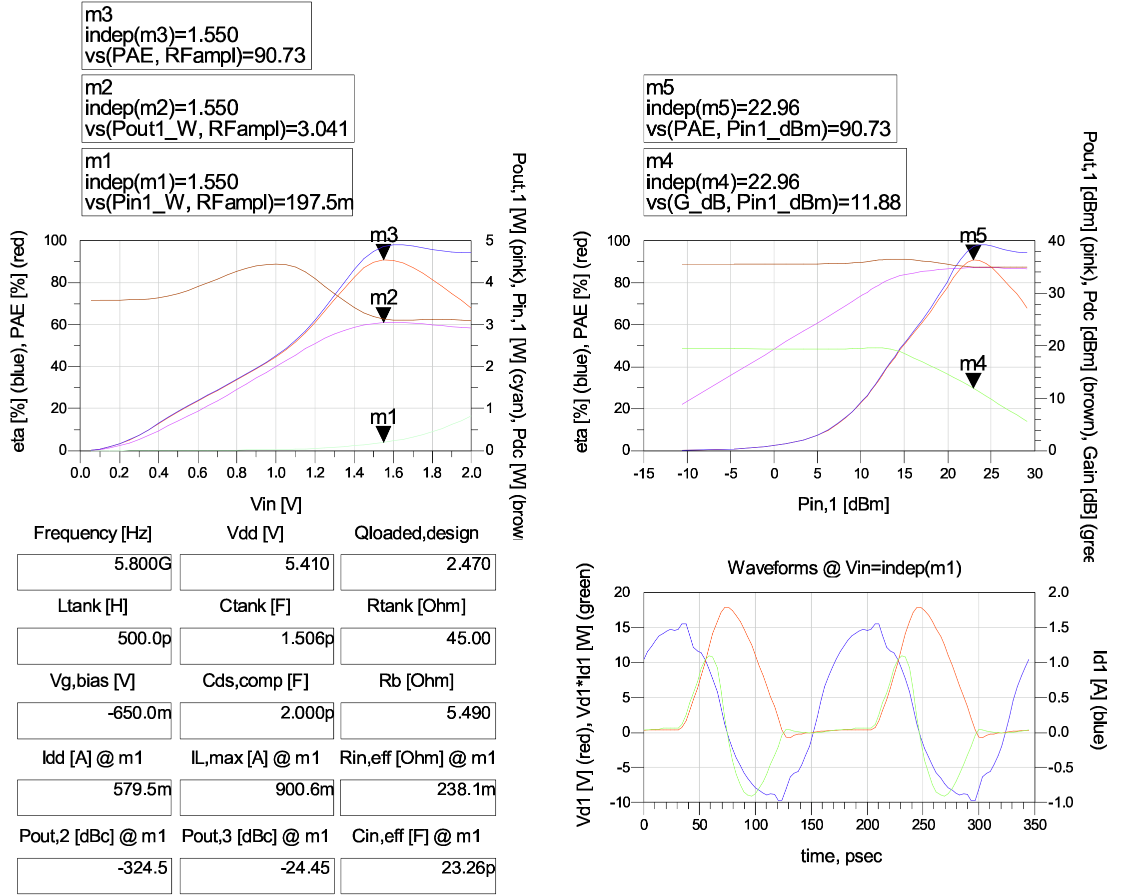


Figure 4.15: Results of HB simulations for *TQPHT pHEMTs* (75 fingers) at 5.8 GHz (see Fig. 4.2 for circuit).

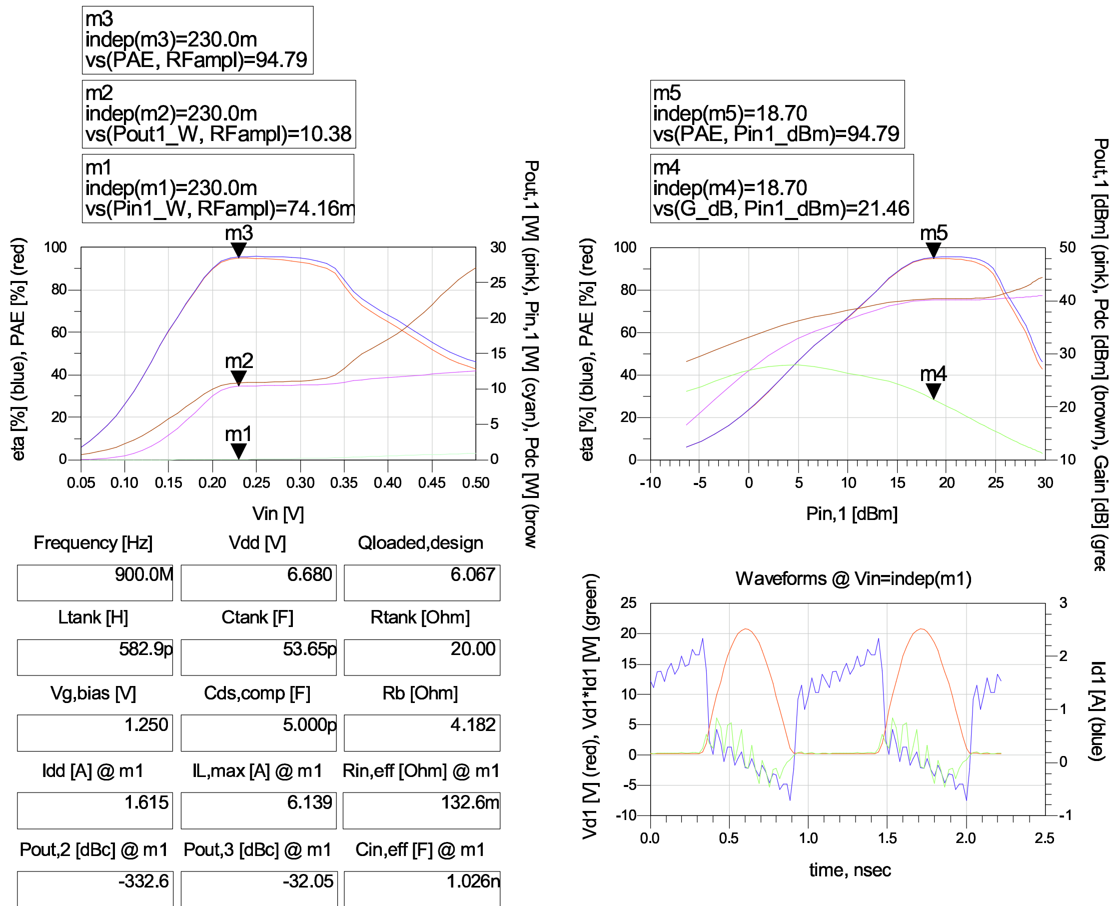


Figure 4.16: Results of HB simulations for *TQHBT2 InGaP HBTs* (Multiplicity = 19) at 900 MHz (see Fig. 4.2 for circuit).

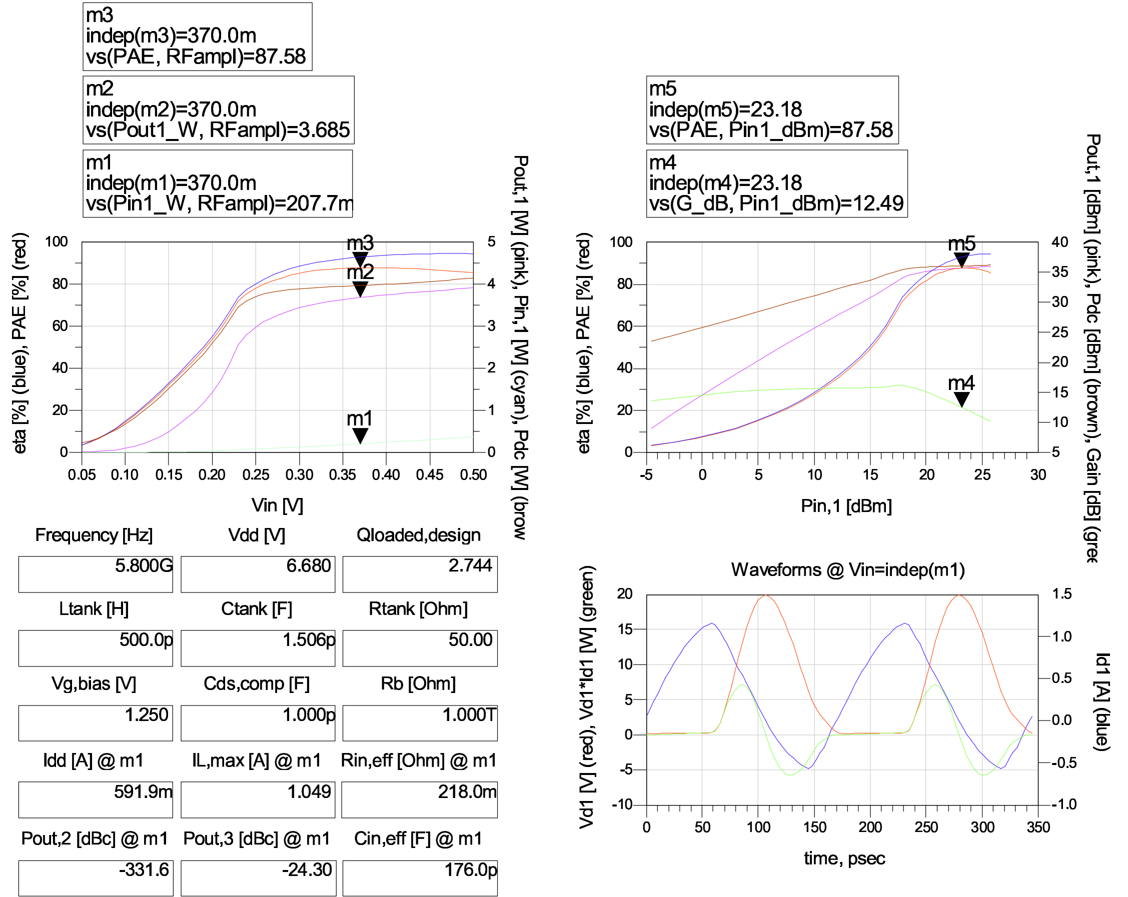


Figure 4.17: Results of HB simulations for *TQHBT2 InGaP HBTs* (Multiplicity = 6) at 5.8 GHz (see Fig. 4.2 for circuit).

4.5 Discussion and Conclusions from Simulations

When targeting an implementation of a CMCD PA with packaged devices and an output power of above 1.5 W, only LDMOS FETs are an option. However, they only are an option below 2 GHz where the achieved PAE is around 70 % if the passive circuitry is ideal. Above 2 GHz, the PAE of a LDMOS FET CMCD PA starts deteriorating substantially. At 5.8 GHz, the devices are useless. Available packaged pHEMTs achieve an output power of only about 1.5 W. The PAE of a CMCD PA employing available packaged pHEMTs is around 45 % below 2 GHz. However, the available packaged pHEMTs are the only devices among the investigated ones delivering a non-zero PAE at 5.8 GHz, where the LP3000P100 pHEMTs achieve a PAE of 35 %. An implementation of a CMCD PA employing LP3000P100 pHEMTs would show whether the on-resistance for $V_{gs} = V_{th}$ and very low V_{ds} is in fact as high as predicted by the DC output characteristic or whether it is merely inadequately modeled by the Curtice 3 model. HB simulations of CMCD PAs employing HBTs have proven awkward because of overflows in the KCL check. Therefore, the achieved PAE of 71 % at 1.8 GHz for the BFP690 HBTs seems arguable.

When targeting an integrated implementation of a CMCD PA, a high PAE and a high output power may be achieved at the same time by making the devices very wide. Both, TQPHT pHEMTs and TQHBT2 HBTs achieve a PAE of around 90 % for 10 W of output power below 2 GHz and for 3 W of output power at 5.8 GHz if the passive circuitry is ideal. However, TQHBT2 HBTs occupy two times the area of TQPHT pHEMTs for the same output power as shown in Tab. 4.3. A better area-efficiency means a better cost-efficiency for an implementation with the pHEMTs than for an implementation with the HBTs. However, it remains questionable whether a pHEMT with 250 fingers and a HBT with a multiplicity of 19 are still modeled correctly.

Regardless whether a discrete or an integrated implementation of a CMCD PA is envisioned, the input impedance of the CMCD PA must be matched to the source impedance for maximum power transfer. However, 1 Ω of input resistance marks the lower limit for a input resistance that is still matchable to a 50 Ω source impedance by an Ell-network (series-shunt/shunt-series combination of an inductor and capacitor, or of two inductors, or of two capacitors). The simulations for the BFP690 SiGe HBT and for the TQHBT2 InGaP HBT show that the input resistance of HBTs tends to be smaller than the input resistance of LDMOS FETs or pHEMTs. Therefore, the input matching for HBTs may be expected to be more difficult. Moreover, the input impedance of bipolar devices is very non-linear because of their base-emitter diode.

The above discussions allows the following conclusions:

- For a CMCD PA implementation with packaged devices, LDMOS FETs are the best choice. A PAE of around 70 % may be achieved below 2 GHz. At 5.8 GHz, pHEMTs should be chosen. However, a PAE of only around 35 % may be achieved.
- For a CMCD PA implementation with integrated devices, pHEMTs provide the better area-efficiency than HBTs. By making the devices very wide, a high PAE and a high output power may be achieved at the same time.
- HB simulations for CMCD PAs employing HBTs are very time-consuming because of a divergence in the KCL checks. Moreover, input matching is expected to be more difficult for HBTs.

Chapter 5

Conclusions

5.1 Recommendations for Device Selection

Combining the conclusions from the sensitivity analysis in section 3.3.4, the device comparison in section 3.4.5, and the simulation results in section 4.5, results in the following recommendations for device selection for the intended applications stated in section 1.1:

- For higher power fixed applications (base-stations) with a target output power of 10-20 W below 2 GHz
  - LDMOS FETs are the best choice for a discrete implementation. Their high breakdown voltage enables them to deliver 10-20 W of output power with a PAE of around 70 % ideally.
  - pHEMTs are the best choice for an integrated implementation. Wide pHEMTs are capable to deliver 10-20 W of output power with a PAE of around 90 % ideally. HBTs are less area-efficient and more time-consuming to simulate but capable to deliver 10-20 W of output power with a PAE of around 90 % as well.

- For lower power portable applications with a target output power of 3 W at 5.8 GHz
  - pHEMTs are the best choice for a discrete implementation. However they are only capable to deliver about 1.5 W of output power with a PAE of around 35%. The investigated packaged LDMOS FETs and HBTs are useless at 5.8 GHz.
  - pHEMTs are the best choice for an integrated implementation. They are capable to deliver the full target output power of 3 W with a PAE of around 90 %.

- For an integrated solution
  - C_{ox}, the number of fingers F, W, and L, must be optimized,
  - C_{ov}, $R_{g,sheet}$, and R_s must be minimized, and
  - the breakdown voltage must be maximized, in order to maximize the PAE.

5.2 Achievements

This study evaluated the Si MOSFET, the Si LDMOS FET, the SiGe HBT, and the AlGaAs/InGaAs pHEMT as switches for use in a CMCD RF switching-mode PA. The goal of this study was to determine which of the above devices delivers the highest efficiency at 0.8-1.0 GHz and 1.8-2.2 GHz for 10-20 W of output power, and at 5.8 GHz for 3 W of output power. The recommendations for device selection have been presented in the previous section. The following achievements eventually led to these recommendations:

- A thorough literature review revealed that no study was published so far evaluating different devices for switching-mode PAs.
- A detailed analysis of a CMCD PA based upon spectrum-limited waveforms for the device voltage and current was performed.
- An analytical expression for the power added efficiency (PAE) of a CMCD PA employing FET devices was derived as a function of the mobility μ_n, oxide cap. C_{ox}, overlap cap. C_{ov}, gate sheet res. $R_{g,sheet}$, gate contact res. $R_{g,contact}$, source res. R_s, number of fingers F, gate width W, gate length L, the supply voltage V_{dd}, the shunt-tank res. R, and the input

voltage amplitude $\hat{V}_{in}$. The analytical CMCD PA model was proven to be adequate by harmonic-balance simulations for a sensitivity analysis of the PAE towards the various device parameters.

- To identify the differences in device parameters between the devices of interest, commercially available packaged devices were investigated followed by a theoretical analysis of the breakdown phenomena, the switching performance, and the on-resistance for the devices of interest. The results from these investigations are summed up in Tab. 3.5 (on page 58).

- Based upon the analytical CMCD PA model an upper limit for the achievable drain-efficiency and thus an upper limit for the achievable PAE was derived. The derived maximum achievable drain-efficiency revealed that a low breakdown voltage fundamentally limits the maximum achievable PAE of a CMCD PA.

- Harmonic-balance simulations for CMCD PAs with ideal passive circuitry were performed for packaged LDMOS FETs (Motorola MRF281SR1), packaged pHEMTs (Filtronic LP3000P100), and packaged SiGe HBTs (Infineon BFP690) at 900 MHz, 1.8 GHz, and 5.8 GHz following well-defined optimization guidelines for $V_{g,bias}$, R_{tank}, $C_{ds,comp}$, and $\hat{V}_{in}$. The same was done for CMCD PAs employing pHEMTs and InGaP HBTs of Triquint's TQPHT and TQHBT2 process, respectively. The simulation results are summed up in Tab. 4.1 (for the packaged devices, on page 79) and Tab. 4.3 (for the non-packaged devices, on page 80).

- Combining the results from analyses and simulations made it possible to deduct the concise recommendations for device selection given in the previous section.

5.3 Outlook

The analyses and simulations in this study have shown that selecting the switching devices is a major issue when designing a CMCD PA. However, choosing the right output balun transformer is as important as choosing the right switching device as is shown in this section. Up to now, the output balun transformer was assumed to be ideal and to present an open-circuit at the drain for even harmonics. However, real output balun transformers may present finite impedances at the drain at even harmonics thereby degrading the PAE. A possible output balun structure is a microstrip rat race [20]. A less bulky output balun structure is the microstrip Marchand balun depicted in Fig. 5.1 which was designed according to [49] for a FR4 substrate. However, the Marchand balun presents low impedances at the even harmonics and high impedances at the odd harmonics as shown in Tab. 5.1a, which is exactly the wrong harmonic termination for a CMCD PA. Introducing $\lambda/8$-transformers as shown in Fig. 5.1b allows to invert the low impedance to a high impedance at the second harmonic. Tab. 5.1b shows the resulting harmonic termination after adding the $\lambda/8$-transformers.

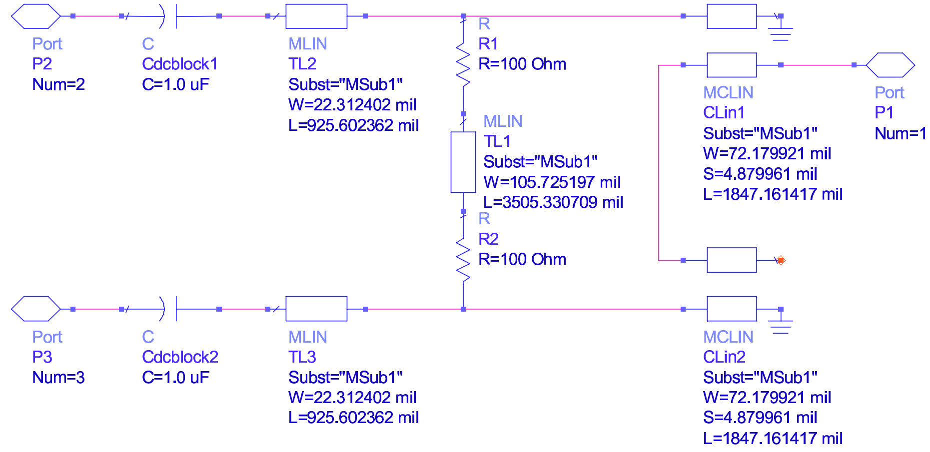


Figure 5.1: Microstrip Marchand balun with preceding $\lambda/8$-transformers and DC block capacitors for a FR4 substrate. Refer to [49] for design equations.

Note that the Marchand balun allows impedance transformation, whereas the rat race just figures as a balun and requires an additional impedance transformer to transform the 50 Ω load to the required tank resistor value [49]. Replacing the ideal output balun transformer of Fig. 4.2 with the Marchand balun of Fig. 5.1 and simulating the CMCD PA with the MRF281SR1 LDMOS FETs results in $PAE = 62.0$ %, $P_{out,1} = 4.7$ W, and $G = 11.9$ dB. The PAE drops by more than 10 % and the output power is halved compared to the simulation with the ideal output balun transformer.

Avoiding the need for an output balun transformer by implementing a single-ended inverse-F PA may be a possible way to present a better harmonic termination. Simulating the inverse-F PA of Fig. 5.2 at 900 MHz with optimized values for $L_{res,1}$ and $L_{res,2}$ results in $PAE = 94.9$ % and $P_{out,1} = 9.6$ W. However, substituting the 1 Ω on-resistance switch by a Motorola MRF281SR1 LDMOS FET results in $PAE = 41.3$ %, $P_{out,1} = 4.0$ W, and $G = 13.4$ dB. A possible reason for the very disappointing PAE of the inverse-F PA employing a MRF281SR1 LDMOS FET is that C_{ds} may detune the resonators considerably.

The above investigations show that a future focus for research on CMCD PAs may lie in output balun transformers.

Table 5.1: Presented drain impedances of the microstrip Marchand balun of Fig. 5.1 without preceding $\lambda/8$-transformers and DC block capacitors (a) and with preceding $\lambda/8$-transformers and DC block capacitors (b).

(a)

freq	Vd1/Itot1.i	Vd2/Itot2.i
900.0MHz	94.369 / 6.045	96.652 / -3.749
1.800GHz	6.844 / 73.317	6.708 / 74.785
2.700GHz	79.568 / 10.374	91.356 / -15.256
3.600GHz	19.323 / 72.011	16.353 / 74.884
4.500GHz	68.737 / 6.306	85.800 / -30.619

(b)

freq	Vd1/Itot1.i	Vd2/Itot2.i
900.0MHz	110.834 / 3.527	92.521 / 2.560
1.800GHz	1.351E3 / -61.388	1.375E3 / -62.466
2.700GHz	85.340 / -10.481	128.283 / -6.858
3.600GHz	21.484 / 65.607	18.736 / 66.874
4.500GHz	116.562 / 18.042	58.980 / 14.157

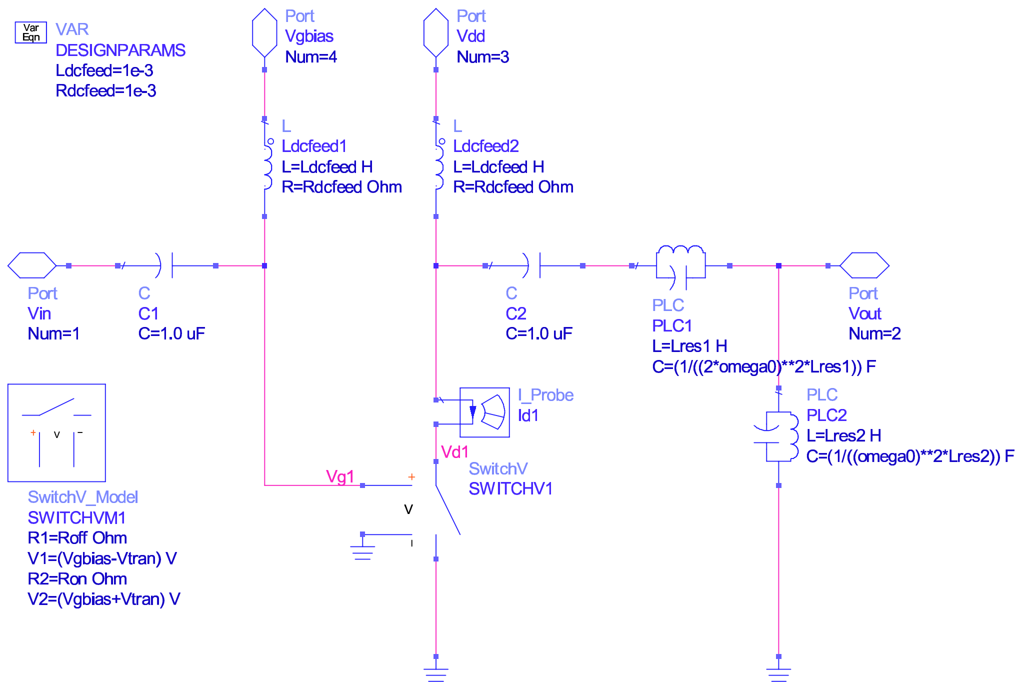


Figure 5.2: ADS schematic of an inverse-F PA.

Appendix A

Task Description by Prof. S. I. Long

The RF power amplifier is a very critical component in portable communications systems. Linear power amplifiers are needed for modulation standards such as North American Digital Cellular ($\pi/4$ DQPSK) and CDMA. These generally include Class A or AB amplifiers which are linear or can be linearized and provide low to moderate efficiencies. Constant envelope modulations such as FM or GMSK (GSM) can employ nonlinear amplifiers without generation of severe distortion. A review of tuned power amplifiers reveals that switching-mode amplifiers are capable of providing higher efficiencies than their linear-mode counterparts. They also exhibit lower power dissipation, low active device thermal stress, and lower sensitivity to component value variations. Therefore, the use of switching-mode power amplifier circuits for low power (up to 3W peak) for portable applications (5.8 GHz ISM band) and higher power (10 20W peak at 0.8 1.0 GHz and 1.8 2.2 GHz) for fixed applications are of interest.

There are many devices which are potential candidates for PA applications. Most cellular applications have utilized either Si LDMOS or GaAs HBT transistors. Switching mode amplifiers such as the current-mode Class D (Inverse F) amplifiers are very promising for high efficiency. A comparative study is needed that will evaluate the distinctive properties of Si MOSFET, GaAs MESFET or HBT, SiGe HBT, and GaN HEMT devices as switches with particular emphasis on switching mode PA applications. In particular, properties such as the relationship between maximum current, drive impedance, and output capacitance will affect power added efficiency and impedance levels required. The project will determine which device provides the best performance at frequencies of 1, 2, and 5.8 GHz.

Project Timeline

Month 1: Review the operation principles and study device characteristics and models for the MOSFET, SiGe HBT, and one other device of choice. Review previous literature and work at UCSB on current-mode Class D/Inverse F power amplifiers.

Month 2: Determine limitations of each device for power, frequency, efficiency and relate these limitations to device parameters. Write a report on the first 2 months work that will be included in the diploma thesis.

Month 3: Design (through simulation) amplifiers at 1, 2 and 5.8 GHz.

Month 4: Write the complete report including amplifier designs. Draw conclusions and make recommendations for further study.

Appendix B

CDROM

`/ADS/cmcd_pa_prj` contains all ADS schematics, data sets, and data displays

`/ADS/Models` contains the device models and design kits used

`/Bibliography` contains nearly all referenced papers classified in corresponding categories

`/Bibliography/Datasheets` contains all data sheets of the investigated packaged devices

`/Excel` contains Microsoft Excel spreadsheets that have been incorporated into the report

`/Maple` contains all Maple worksheets developed

`/Report` contains this report as PDF file and PS file

`/Report/Latex` contains the latex sources of this report

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