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High Voltage GaN Variable Capacitance Diode

A Thesis submitted in partial satisfaction of the  
requirements for the degree; Master's of Science  
in the field of Electrical and Computer Engineering

by

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# **Abstract**

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The research of this report focuses on solid state microwave engineering with correlations to materials science. GaN is the newest and hottest material that is being used to ‘reinvent’ several new semiconductor devices. In this study, GaN was used in the design of a high breakdown voltage variable capacitor. The usable tuning capacitance of this device began at a predetermined 100 V. The capacitance tuning range of the traditional varactor diode begins at 0 V and continues to the just below the breakdown voltage of the device. These types of devices are limited to mostly small signal applications. The GaN device of this study will be capable of high voltages and hence a wider range of applications including high power VCOs and radar systems.

The design procedure consisted of rigorous simulations which were later confirmed through mathematical analysis. It was later determined that the simulator need only be used as a confirming tool in the design process and that the mathematical analysis was accurate enough. In this study, a GaN varactor diode is presented capable of 4:1 capacitance tuning in the bias range of 100 – 250 V. The total common cathode device resistance did not exceed 0.5  $\Omega$ . Methods of maintaining the peak electric field well below breakdown were achieved.

# Contents

|   |    |
|---|----|
| <b>Chapter 1 Motivation, Background, and Applications</b> ..... | 1  |
| <b>Chapter 2 Literature Review</b>                              |    |
| 2.1 Research Publications.....                                  | 4  |
| 2.2 Commercial Products.....                                    | 7  |
| <b>Chapter 3 Theoretical Schottky Varactor Operation</b>        |    |
| 3.1 Device Components.....                                      | 9  |
| 3.2 Equilibrium Conditions of Schottky Varactor.....            | 16 |
| 3.3 Applying Reverse Bias.....                                  | 19 |
| 3.4 Device Resistance.....                                      | 22 |
| 3.5 Hi Lo and Lo Hi Lo Doping Analysis.....                     | 25 |
| <b>Chapter 4 Simulation Results and Comparisons</b>             |    |
| 4.1 Simulator Setup.....  | 36 |
| 4.2 C-V Results and Equivalent Circuits.....                    | 40 |
| 4.3 Q and Power Dissipation.....                                | 44 |
| 4.4 Field Plate and Notching for Electric Field Reductions..... | 47 |
| 4.5 Electric Fields of Notched Hi Lo and Lo Hi Lo Devices.....  | 50 |
| <b>Chapter 5 Conclusions</b>                                    |    |
| 5.1 Feasibility of Proposed Device.....                         | 55 |
| 5.2 Problems Encountered.....                                   | 56 |
| 5.3 Recommended Next Steps.....                                 | 57 |
| <b>Appendix</b>   |    |
| Silvaco Code for Simulations.....                               | 59 |
| <b>Bibliography</b> .....                                       | 63 |

# Chapter 1

## Motivation, Background, and Applications

The primary goal of this research effort was the design and analysis of a high breakdown voltage varactor diode. The material system used in this analysis was GaN, a III – V widebandgap semiconductor which has gained much attention over the last few years for its optoelectronic and high power potentials. Several electronic and optoelectronic devices have been realized over the last few years including metal-semiconductor field effect transistors (MESFETs), high electron mobility transistors (HEMTs), and light emitting diodes (LEDs).

The material parameters of GaN are appealing to the RF design engineer. With a bandgap of 3.4 eV, high bulk mobility, piezo-electric properties, high electron velocity, and high breakdown voltage, GaN promises to become an excellent material for high power RF applications. It should be pointed out that GaN forms valuable alloys with AlN and InN. 32.2 Watts/mm have been reported in [1] through a HEMT based power amplifier using GaN/AlGaN epilayers. High output voltages were achieved in this case through the implementation of a field plate structure which lowered the electric field between the drain and gate contacts.

The design goals of this project were to successfully and accurately design and simulate a varactor diode layout with a minimum of three to one capacitance tuning ratio and the highest possible bias voltages. To achieve the high breakdown voltage, the device structure was designed such that the electric field was minimized.

High voltages are desired in the fields of RF communications, specifically in power amplification and antenna transmission. Figure 1.1 [2] illustrates one possible application of the high voltage varactor diode. Tuned capacitance at the edges of a radiating patch antenna allow for a frequency tunable antenna. In this case, high amounts of RF power could be radiated from the patch antenna without breaking down the varactor diodes. High voltage varactors will allow for simplified and miniaturized transmitter and radar design.

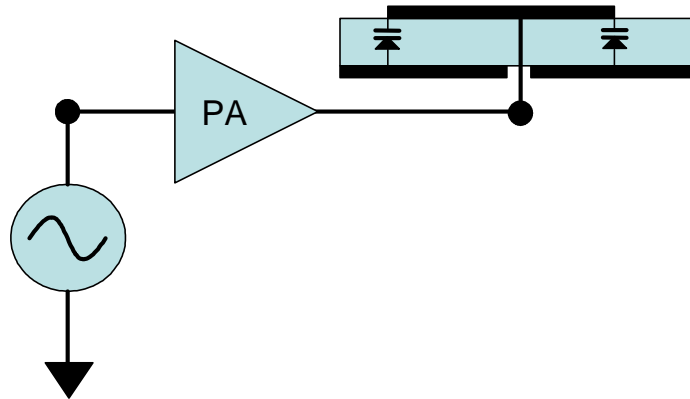


Figure 1.1: Microstrip patch antenna loaded with varactor diodes

The arrangement which was analyzed in this study was the series combination, common cathode configuration of two devices. The varactors were designed with phased array, spaced-based radar antenna in mind. The antenna configuration consisted of a horn antenna with an array inside, capable of steering a beam  $\pm 20^\circ$  at L-band. The tuned elements must be able to withstand up to 150 Watts of RF power. Two varactors, placed in series were part of a tunable tank circuit

(figure 1.2). The device was designed to have the highest possible  $Q$  in an effort to reduce the power dissipation. The low thermal conductivity properties of the sapphire substrate required that the device dissipate minimum amounts of power. There were several tradeoffs and tuning aspects in the design including doping profiles and contact sizes. Several different device layouts were considered, simulated, and compared.

Performance requirements were specified for series resistance and capacitive tuning ratio. The  $Q$  and power dissipation came out of these two specs. For the application in mind, the total resistance of two varactors in series was not to exceed  $1 \Omega$ . It was desired to have a minimum tuning ratio 3:1 with capacitances on the order of 20 pF. With the prerequisites of the device defined, the varactor was designed such that the simulated measurements exceeded the expectations.

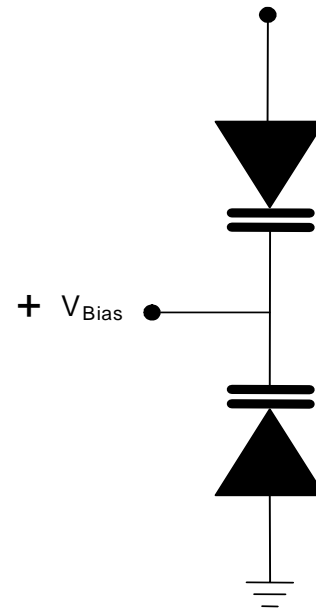


Figure 1.2: Common cathode series combination of two varactors

# Chapter 2

## Literature Review

### 2.1 Research Publications

The varactor diode is a commonly used electronic device for microwave and millimeter wave applications. The varactor diode can be fabricated from either p-n or Schottky junctions and both cases are under research today. SiC is a widebandgap semiconductor with  $E_G = 3.0$  eV and this material may also be suitable for high voltage microwave tuning. The AlGaIn/GaN heterojunction and two dimensional electron gas (2DEG) formation are the building blocks of the HEMT. In order for a high voltage varactor to be fabricated as part of a tuning network for a HEMT based power amplifier or VCO tank component, the varactor must be composed of the same epilayers as the HEMT. It is for this reason that heterostructure varactor diodes have been investigated. Si varactors have been under investigation for decades and many of the profiles used today were first fabricated with this material. There is much to be learned from prior art done in Si.

The SiC varactor diode presented in [4] shows that devices made in this material system are capable of bias voltages over 130V. The device consisted of a highly n-doped ( $N_D = 1 \times 10^{18} \text{ cm}^{-3}$ ) substrate and a moderately doped ( $N_D = 2.45 \times 10^{17} \text{ cm}^{-3}$ ) 5  $\mu\text{m}$  thick epitaxial layer. Ni/Au ohmic contacts were deposited on the backside of the wafer. Ti/Au was deposited to form the Schottky contacts to the device. C-V measurements revealed that the device was capable of

10:1 tuning between 0 and 130 V of reverse bias. I - V measurements revealed the poor nature of ohmic contacts to SiC, which is under investigation by a number of researchers worldwide. An ohmic contact resistance of  $10^{-3} \Omega \text{ cm}^2$  was measured for the Ni/Au metal layers in this study. The quality factor was directly affected by the high series resistance of the device. At 10 GHz, a Q of 0.4 was reported which corresponds to  $R_S = 39 \Omega$ , assuming 1 pF of capacitance. Researchers have begun to investigate the implantation of highly doped  $n^+$  regions on the backside of the device in order to reduce the specific contact resistance. In [17], improvements were made to the SiC ohmic contact resistance. For highly doped 4H-SiC,  $1.17 \times 10^{-6} \Omega \text{ cm}^2$  was reported using Ni/C60 films followed by a two hour anneal at 800°C. While the material properties of SiC are favorable for such an application, there are many unknowns regarding the nature and physics of ohmic contact formation to this material.

The metal semiconductor metal (MSM) 2DEG varactor diode operates in a unique way as described in [5]. Two Ni/Au Schottky contacts were deposited on a traditional AlGaIn/GaN HEMT structure. The epilayers consisted of a 3  $\mu\text{m}$  thick UID GaN layer and a 20 nm UID  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$  layer. Hall measurements made at room temperature revealed a mobility of 1180  $\text{cm}^2/\text{Vs}$  and a 2DEG sheet charge concentration of  $n_S = 5.6 \times 10^{12} \text{ cm}^{-2}$ . The capacitance of a single electrode remained constant for small reverse biases and is given by:

$$C_{Schottky} = \frac{\epsilon A}{d} \quad (2.1)$$

Where  $d$  is the distance between the contact and the 2DEG. The capacitance of the reverse biased electrode remained unchanged until the depletion region punched through the 2DEG channel. Beyond this punch through voltage the UID GaN depleted vertically and the 2DEG channel between the two electrodes depleted laterally. This lateral depletion distance was given by:

$$x_D = \frac{2\epsilon V}{qn_s} \quad (2.2)$$

This depth added an additional series capacitance to the device:

$$C_{2DEG} = \frac{w\epsilon}{\pi} \ln \left\{ \frac{\sqrt{d^2 + x_D^2} + d}{\sqrt{d^2 + x_D^2} - d} \right\} \quad (2.3)$$

where  $w$  is the width of the electrode. These characteristics lead to a device that experienced dramatic capacitance drops for very small bias voltages. For an electrode width of 7  $\mu\text{m}$ , a tuning ratio of 3.5:1 was reported between 0 and 2 Volts of reverse bias at 2 GHz. There was no record of series resistance or  $Q$  in the documentation of this device.

Silicon, with a critical breakdown field of  $2 \times 10^5$  V/cm [4] is not the ideal material for the high voltage varactor diode. In [8], a high Q and high voltage varactor diode was fabricated with silicon and the critical components to this design were the thick layers of material. The doping profile consisted of a traditional lo hi lo doping profile and the total device thickness was over 15  $\mu\text{m}$ . The thickness and low doping levels of the device allowed for tuning voltage up to 120 V. Since the critical breakdown field of GaN is more than an order of magnitude larger than that of silicon, one would assume that 900 – 1000 V of bias would be possible for a GaN varactor given the ability to grow thick epilayers. With the current MOCVD technology at UCSB, the thickest possible GaN structure is around 10  $\mu\text{m}$ . Etching of the mesas introduces an additional problem since the deepest possible photoresist etch is 7  $\mu\text{m}$ . The use of an  $\text{SiO}_2$  mask would allow for a 10  $\mu\text{m}$  etch, but this type of process would add complications. The combination of thick GaN layers and low UID would create many more opportunities for this design.

## **2.2 Commercial Products**

The GaAs varactor diode is not as readily available on shelf as its Si counter part. The quality factor of the few GaAs varactors found was consistently higher than those fabricated from Si. Bulk mobility is considerably higher in GaAs, which contributes to the much lower series resistance and higher Q. Data compiled from [6] and [7] are presented in table 1.1.

| Supplier | Part #  | Device Description | R(V) $\Omega$ | C(V) pF | Q (V) @1.2GHz | C <sub>Max</sub> /C <sub>Min</sub> |
|----------|---------|--------------------|---------------|---------|---------------|------------------------------------|
| Sanyo    | ESGD100 | GaAs Sch.          | R(0) = 1.5    | 0.2     | 442           | NA                                 |
| Sanyo    | EC2C03C | Si Hyp.            | R(0) = 0.55   | 7.35    | 33            | NA                                 |
| Skyworks | GMV9821 | GaAs Hyp.          | R(4) = 2.3    | 0.35    | 166           | 13.8                               |
| Skyworks | SMV1247 | Si Hyp.            | R(3) = 6      | 1.0     | 22            | 7.1                                |

Table 1.1: Data found for various varactors available on the market today.

It was of little surprise to discover that there are no varactor devices currently being fabricated from GaN or SiC. These materials are still in their infancy stages and it will take time for them to fully develop the way that GaAs and Si have.

# Chapter 3

## Theoretical Schottky Varactor Operation

### 3.1 Device Components

The Schottky varactor consists of three basic components: the Schottky contact, the ohmic contact, and the semiconductor material. The Schottky metal represents the  $p^+$  region, or anode, of a p-n junction diode. The semiconductor material represents the n type region of the p-n diode. Finally, the ohmic contact metal serves the same purpose in a Schottky diode as in the p-n junction diode. The ohmic contact is the low impedance interface between the n region and the outside world. Figure 3.1 represents the basic building blocks of the Schottky varactor diode, positive potentials applied to the ohmic metal results in a reverse bias between the

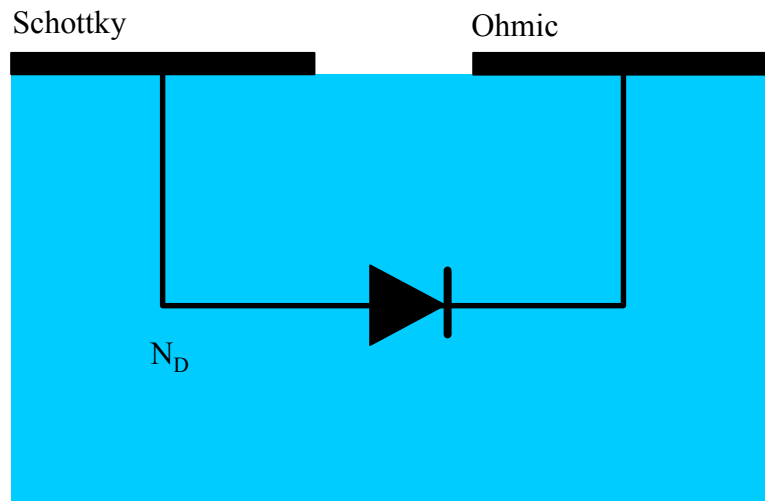


Figure 3.1: Basic varactor layout with diode equivalent

Schottky metal – semiconductor heterojunction.

The basis behind rectifying or Schottky contacts comes from the fact that in equilibrium and before joining the two materials, the metal has a work function,  $\Phi_m$ , which is greater than the work function of the semiconductor,  $\Phi_s$ . Shown below is the simplest model of the Schottky barrier before and after the metal deposition.

Figure 3.2 depicts the work functions and electron affinity of the metal and semiconductor relative to the vacuum level. As the two are brought into contact, a barrier is formed on both the metal and semiconductor sides. For highly doped material, the barrier can be assumed to be equal on both sides. Electrons in the semiconductor are transferred to the metal until the Fermi levels on either side of the

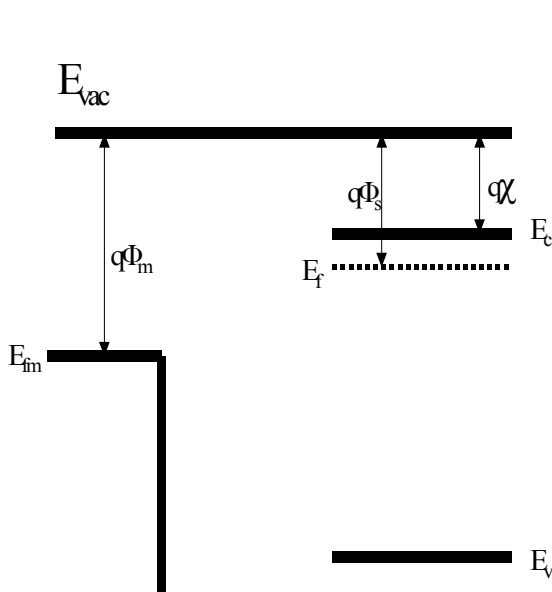


Figure 3.2: Band alignment prior to metal deposition

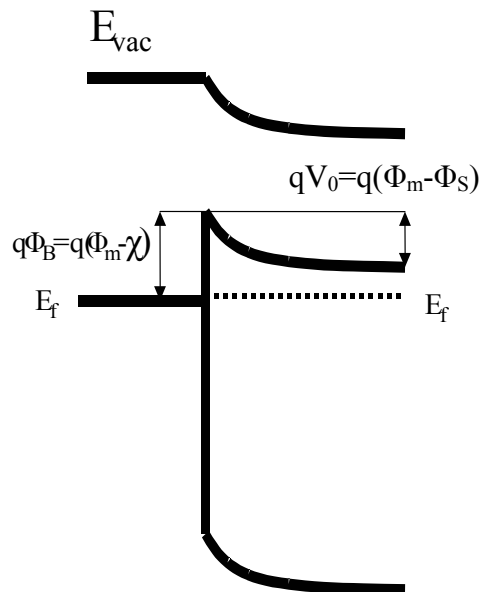


Figure 3.3: Band alignment after metal deposition

junction are aligned. The positive charge of the ionized donors in the semiconductor is enough to compensate the excess electrons at the surface of the metal. Figure 3.3 shows how the valence and conduction bands bend so that the fermi levels of the two materials line up.

The much more accurate model of the barrier height in GaN includes surface state [9], image force charges [10], and the piezo electric charges [11] at the interface. The surface state effect is dependant upon the semiconductor. At the surface of the semiconductor, there are free or dangling bonds which slightly alter the equilibrium conditions of the semiconductor itself. Prior to coming into contact with the metal, the conduction and valence bands bend at the surface of the semiconductor to compensate for the additional charge from the surface states. If the surface state density is large enough to accommodate the additional charges brought about by bringing the metal into contact with the semiconductor, the barrier height is determined by the total band bending at the surface of the semiconductor prior to metal contact. Clearly the barrier height is determined by the properties of the semiconductor and not the metal work function. Image barrier lowering occurs for the following reason: when a charge is brought into close proximity of an infinite metal sheet (the Schottky metal), the sheet can be removed and an equal in magnitude, opposite charge can be placed behind the plane of the metal. The potential  $V(x)$  between the two charges can then be written as:

$$V(x) = \frac{q^2}{16\pi\epsilon x} \quad (3.1)$$

This inverse x potential must be superimposed on the original band diagram potential and will reduce the barrier between the metal-semiconductor junctions.

The piezoelectric properties of GaN allow for advanced, undoped HEMT design, using only the charges provided by the lattice mismatch of the AlGaIn/GaN heterojunction. For the varactor design, additional charges will appear at the surface of the semiconductor due to the lattice mismatch between the sapphire substrate and GaN. Surface Fermi level pinning positions of 0.9 – 1.0 eV were recorded for GaN in [11]. The effects of these charges will be minimal for this type of device and will only affect the barrier height of the Schottky metal. It is interesting to note that even though metals with workfunctions varying between 5.1 and 5.65 eV were deposited on GaN, the barrier height of these metals is consistently within a tenth of an eV. Once again it is the properties of the semiconductor which determine the barrier height of the junction.

Barrier heights of 0.99 eV have been reported [12] for Ni and GaN. The work function of Ni is 5.15 eV and the electron affinity of GaN is 4.1 eV. For n-GaN doped ( $2 \times 10^{17} \text{ cm}^{-3}$ ), the electron affinity is  $\sim 4.39 \text{ eV}$ . Using the Anderson method, barrier heights of 0.29 eV are expected. The above stated mechanisms must therefore contribute to an overall barrier height increase.

Typical Schottky contacts to GaN consist of Ni/Au (500/2000 Å) metal layers.

The Ni sets up the barrier on the interface while the Au and Ni/Au alloy allow for both a low resistance probe pad and a contact immune to oxidation. An approximation of the current density for Schottky tunneling can be written as:

$$J = \exp\left(-\frac{qV_{Bi}}{E_\infty}\right) \quad (3.2)$$

$$\text{where } E_\infty = \frac{qh}{4\pi} \sqrt{\frac{N_D}{\epsilon m^*}} \quad (3.3)$$

The ideal ohmic contact consists of a metal whose work function is lower than that of the semiconductor, so that the band bending at the junction does not create a barrier on the semiconductor side. Figures 3.4 and 3.5 show the before and after band

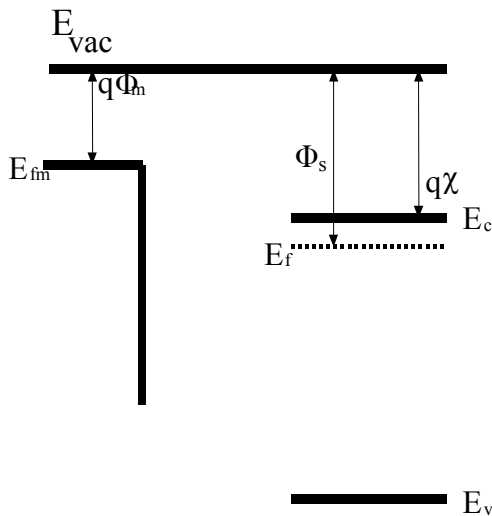


Figure 3.4: Band alignment prior to metal deposition

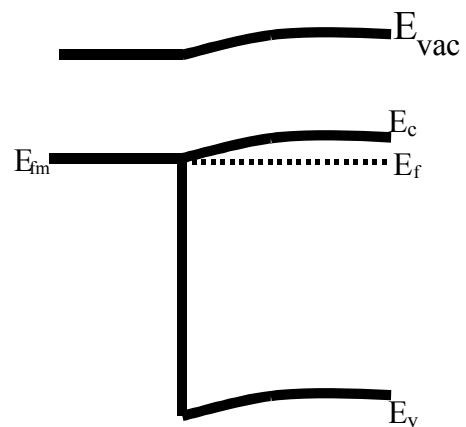


Figure 3.5: Band alignment after metal deposition

diagram alignments for an ideal ohmic contact.

Real ohmic contacts to GaN are much more complicated than the simplified models shown above and include phenomena such as thermionic emission and quantum mechanical tunneling [9]. The tunneling mechanism is what makes ohmic contacts possible. The metal layer deposited on the GaN surface is annealed at a high temperature so that it creates a highly doped region under the contact. As the doping in the semiconductor increases, the barrier or depletion region width decreases. Thin barriers equate to a higher probability of tunneling, or better ohmic contacts. Regions underneath ohmic contacts tend to be highly doped to aid in this effect. The exaggerated drawing in figure 3.6 shows how the barrier thickness is modified through annealing. The barrier height may be unchanged, but the electrons undergo higher probability of tunneling due to the reduction in barrier thickness. Far from the junction, the Fermi level returns to its equilibrium position based on the electron

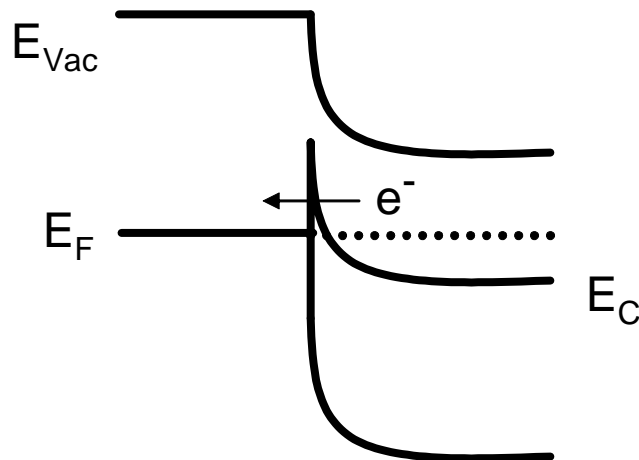


Figure 3.6: Highly n-doped region underneath contact due to annealing

concentration in the semiconductor.

Low contact resistance to GaN was observed in [13] through the use of a specific multilayer metal stack annealed at just the right temperature. The Ti/Al/Ni/Au combination shown below in figure 3.7 represents the metal layers used in the contact resistance study. The metals were annealed at 900°C for 30 seconds, allowing for the formation of TiN, which improved the quality of the interface between the GaN and metal. The alloy formed from gold and nickel was robust, allowing for excellent contacts over a range of temperature. This alloy also

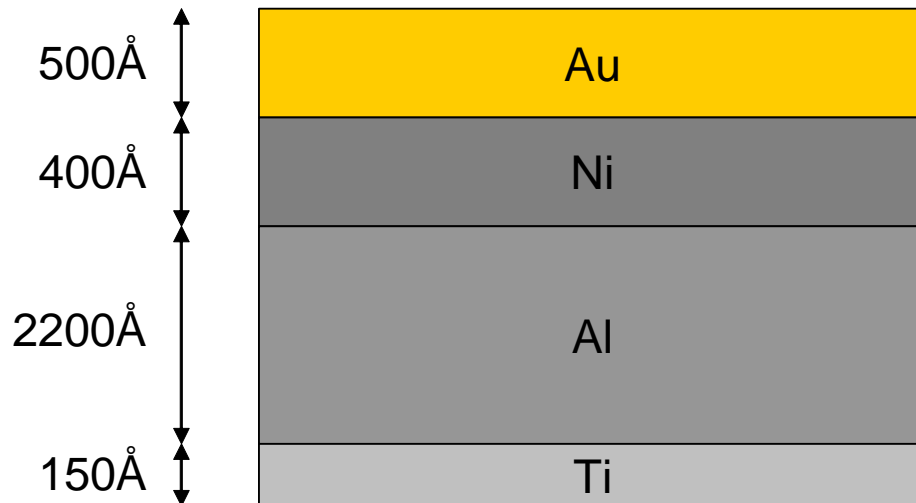


Figure 3.7: Metal layer thicknesses of ohmic contacts to GaN

eliminated the chance of oxidation at the GaN – Ti interface, which would increase the contact resistance over time. It is important to note that the surface of the GaN was damaged with an RIE prior to metal deposition. Damaged samples consistently yielded ohmic contact resistances 2 – 5 times lower than undamaged samples.

The TLM method of ohmic contact analysis is accurate all the way down to about  $10^{-7} \Omega \text{ cm}^2$ . In the mentioned study, specific contact resistances of  $R_c = 8.9 \times 10^{-8} \Omega \text{ cm}^2$  on samples doped  $N_D = 1 \times 10^{17} \text{ cm}^{-3}$  were reported using the TLM method. Though the numbers may not be exact due to the precision of TLM at low contact resistances, it can be assured that excellent contact resistances were achieved. With an increase in doping (up to  $5 \times 10^{18} \text{ cm}^{-3}$ ) underneath the contact, one can assume that the ohmic contact performance will at the least match or even exceed the reported data.

### 3.2 Equilibrium Conditions of Schottky Varactor

In equilibrium, the potential difference between the Schottky metal and semiconductor workfunctions sets up a built in electric field and depleted region in the semiconductor [16]. The width of the depletion region is given by the equation:

$$W_0 = \sqrt{\frac{2\epsilon V_{Bi}}{qN_D}} \quad (3.4)$$

Now imagine the ionized donors on the n side of the junction which provide a net positive charge and an equal and opposite sheet charge in the metal. It is the formation of this dipole of charge across the depletion region which gives rise to the junction capacitance, which is dominant in the reverse bias case. Figure 3.8, shown below, represents the charge distribution of the zero bias junction. Holes in the metal

diffuse to the semiconductor and electrons from the semiconductor pass to the metal. Since the concentration of carriers in the metal is very high, the charge distribution in the metal only builds up at the surface and can be modeled as a delta spike. On the other hand, in the semiconductor, there are fewer electrons so the charge region is free to extend to a distance  $W_0$ .  $W_0$  is a function of built in voltage which is dependant upon the barrier setting mechanisms mentioned earlier in section 3.1. With equal and opposite charges across the fixed distance  $W_0$ , an electric field is formed.

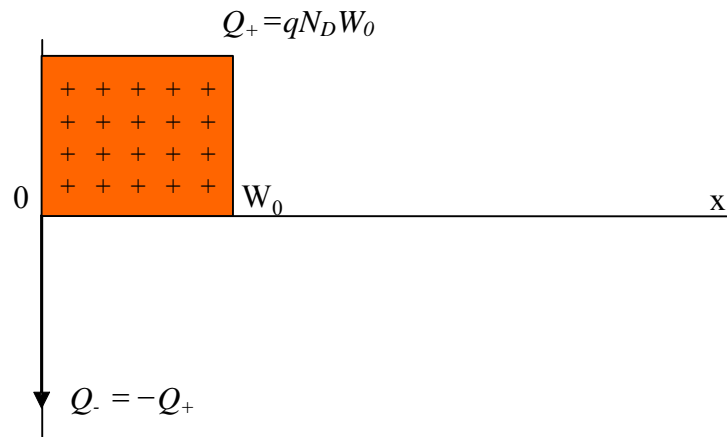


Figure 3.8: Equilibrium charge distribution of Schottky metal – semiconductor junction

The electric field distribution is obtained through the integration of the charge profile in the semiconductor over the variable  $x$ , or Poisson's equation.

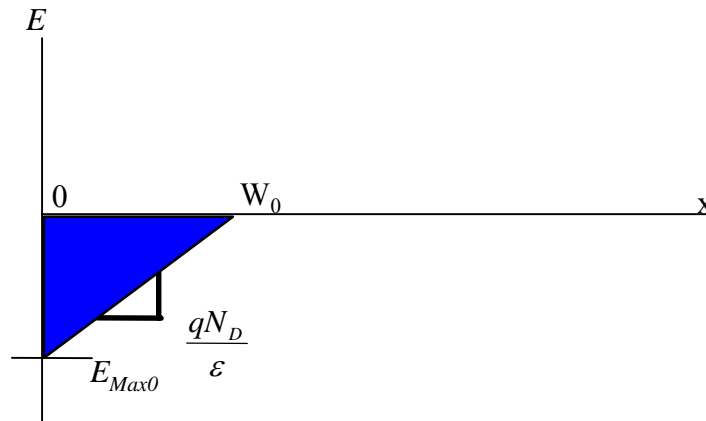


Figure 3.9: Electric field at equilibrium

Therefore the change in the electric field is given by:

$$E = -\int \frac{qN_D}{\epsilon} dx \quad (3.5)$$

$$\frac{dE}{dx} = -\frac{qN_D}{\epsilon} \quad (3.6)$$

and is simply the slope of the triangle shown in figure 3.9. Integration of the electric field profile gives the built in voltage of the junction. Using all of the knowns thus far, it is possible to solve for  $E_{Max0}$ , a critical parameter in the design of a reverse bias junction.

The general, the nonlinear definition of capacitance is given by the expression:

$$C_J = \left| \frac{dQ}{dV} \right| \quad (3.7)$$

With a few steps it can be proven that the capacitance of a junction behaves like a parallel plate capacitor. Beginning with a revisit of the expression for  $Q_+$ :

$$Q_+ = qN_D W_0 \quad (3.8)$$

Substituting for  $W_0$  and plugging equation 3.8 into 3.7 we obtain:

$$\frac{dQ}{dV} = \frac{d}{dV} qN_D W(V) \quad (3.9)$$

$$C_J = \frac{dQ}{dV} = \varepsilon \sqrt{\frac{qN_D}{2\varepsilon V}} = \frac{\varepsilon}{W_0} F/cm^2 \quad (3.10)$$

With equation 3.10, it is possible to approximate the equilibrium capacitance of the reverse bias Schottky junction. This solution is an approximation because it does not take into account fringing capacitance at the edges of the Schottky contact.

## 3.2 Applying Reverse Bias

With the application of a positive voltage to the ohmic contact of the device, the depletion layer depth underneath the Schottky contact increases. This in turn

decreases the capacitance described in equation 3.10. Solutions for the applied reverse bias capacitance, depletion depth, and electric field are all derived from the equilibrium conditions. The equations are modified so that the built in voltage term of the equations becomes the addition of  $V_{Bi}$  and  $V_{Rb}$ .

$$W(V_{Rb}) = \sqrt{\frac{2\epsilon(V_{Bi} + V_{Rb})}{qN_D}} \quad (3.11)$$

As far as the semiconductor is concerned, there is no difference between applying reverse bias and increasing the barrier height.

The net positive charge in the semiconductor increases because it is compensated by an increased negative charge in the metal. The only way for the semiconductor to compensate is through the depletion of additional charge carriers. Once again, ionized donors in the material are left behind resulting in the net positive

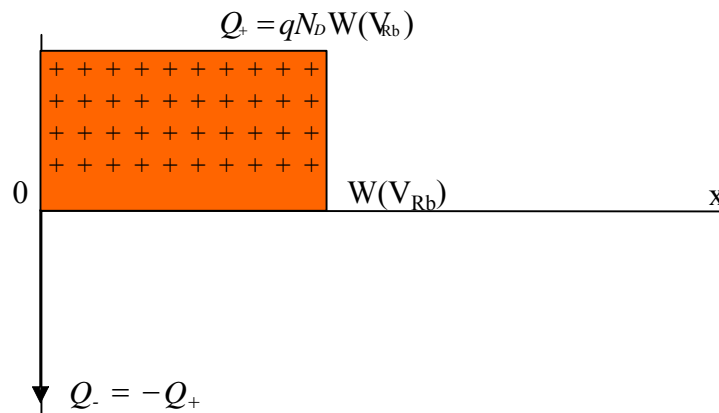


Figure 3.10: Reverse bias charge distribution of Schottky metal – semiconductor junction

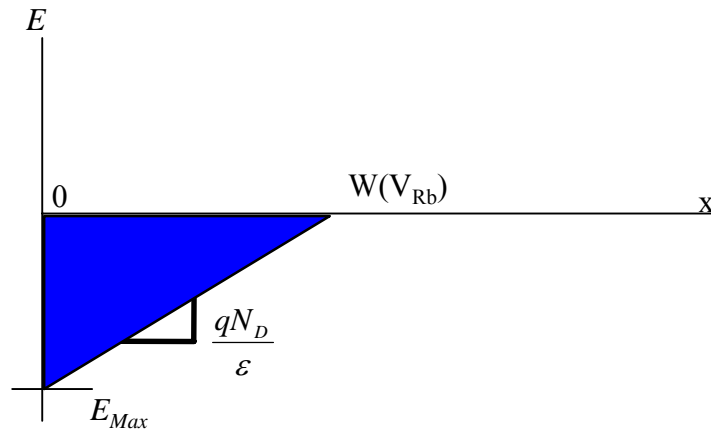


Figure 3.11: Electric field under reverse bias

charge in the semiconductor. Figures 3.10 and 3.11 depict the charge distribution and electric field under reverse bias conditions.

At this point, it would be desirable to obtain an expression for the maximum electric field. Using simple geometry,  $E_{Max}$  can be approximated with the following equation:

$$E_{Max} = -\frac{qN_D x}{\epsilon} \quad (3.12)$$

In most cases, the doping profile of the voltage variable capacitor is non-uniform, so the equations describing the depletion depth and electric field need additional modifications. The equations solved up to this point are required in order to carry on with the more advanced calculations for the profiled doping scenarios. Some of the profiles that will be investigated and compared within this report are the

hi lo and lo hi lo doping distributions. Low doping levels are desired underneath the Schottky contact to minimize the electric field build-up at that location.

### 3.4 Device Resistance

The device will be fabricated in the common cathode configuration, two diodes for every mesa. There will be two sets of interdigitated Schottky - ohmic stripes on each mesa structure. There are several components to the series resistance of the device. They include: stripe metal resistance ( $R_S$ ), ohmic contact resistance ( $R_C$ ), semiconductor gap resistance ( $R_G$ ), and the spreading resistance under the Schottky metal ( $R_{Sp}$ ) [18]. With every part of device resistance accounted for, it will be possible to estimate the total resistance of a single device. Shown below in figure

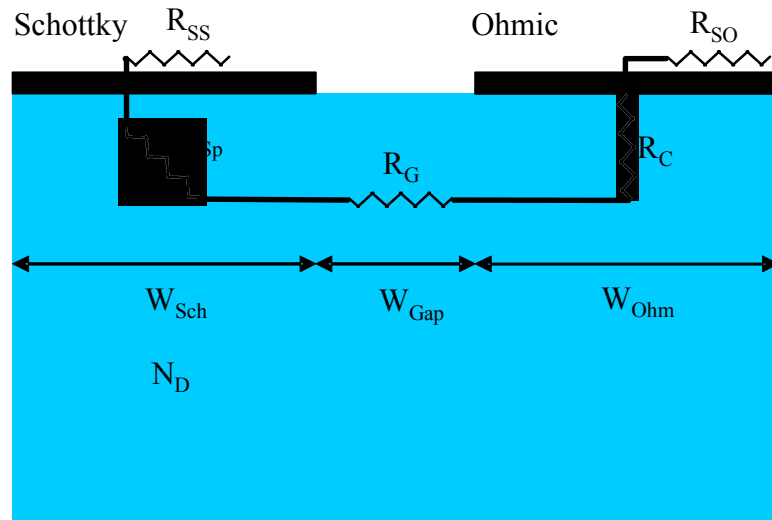


Figure 3.12: Elevation view with equivalent series resistor network

3.12 is a cross section view of the device illustrating the different resistances which need to be accounted for. Figure 3.13 is an overhead view of the device structure. The transverse length of the stripe,  $L$ , is shown for clarity. Neglected in this evaluation are the metal traces which feed the stripes.

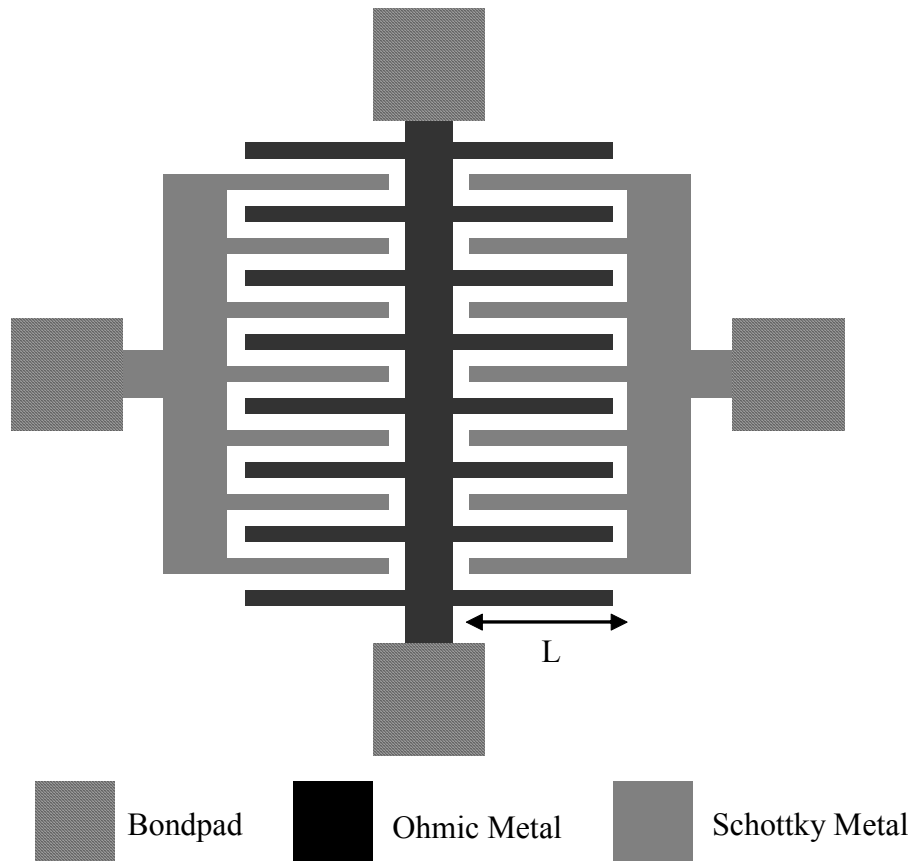


Figure 3.13: Top view of device structure.

The individual expressions for the resistances displayed in figure 3.12 are as follows:

$$R_C = \frac{r_c}{LW_{Ohm}} \quad (3.13)$$

where:

$r_c$  = Specific contact resistance ( $\Omega\text{cm}^2$ ) and,

The next component of resistance comes from the semiconductor material in between the ohmic and Schottky contacts. This is a variable resistance since the thickness of the conducting region decreases as the depletion depth increases. There is a factor of  $\frac{1}{2}$  in equation 3.14 because each Schottky stripe effectively sees two ohmic contacts on either side and therefore two semiconductor gap regions, halving the resistance.

$$R_G = \frac{\rho_S W_{Gap}}{2L} \quad (3.14)$$

where,

$$\rho_S = \frac{1}{q\mu_n N_{D1} t_1} = \text{Sheet resistance of topmost GaN layer } (\Omega/\square)$$

By growing a highly doped region at the bottom of the device, the gap resistance will be reduced since the parallel resistance of this bottom layer will dominate the structure. Next, the spreading resistance underneath the Schottky contact must be accounted for:

$$R_{Sp} = \frac{\rho_s W_{Sch}}{12L} \quad (3.15)$$

Finally, the high aspect ratio metal stripes will have some series resistance as well.

$$R_S = \frac{\rho_{Au} L}{3W_{Sch} t_{Au}} \quad (3.16)$$

The calculation of this resistance takes into account the assumption that the stripes are fed from one end. To reduce this resistance, thick layers of gold can be deposited to the final choice of Schottky metal contact layers. The highly conductive, thick layers of gold will dominate the resistance of a single stripe.

The resistance evaluation consists of a single “cell block” of the total device. In order to find the total device resistance, proper scaling is necessary using the number of stripes, Schottky width, ohmic width, and gap width. These will become critical variables in designing the structure for an optimized series resistance. Tradeoffs between capacitance, resistance, and Q are obvious.

### **3.5 Hi Lo and Lo Hi Lo Doping Analysis**

Two different doping profiles were examined and compared as potential candidates for the final varactor design. The hi lo doping profile consisted of a highly n-doped region at the surface of the device followed by a thick UID region below.

The lo hi lo doping profile consisted of a thin UID layer at the surface, followed by a thin highly n-doped region, and finally a thick UID region. For this study the desired tuning voltage range of the device was to be 100 - 250 V. The top regions were only used as ‘voltage buffers’. In other words, the top regions of the device were designed such that minimal amounts of depletion depth were consumed for the first 100 V of reverse bias. Large capacitance tuning ranges were achieved given that the top layer thicknesses were minimized. Note that for the lo hi lo profile the ‘top layer’ actually consisted of the top two regions. Also, it was proven through initial simulations that notching out the top layer between the two contacts significantly reduced the total electric field of the device (see chapter 4). In order to reduce the gap resistance,  $R_G$ , a highly doped  $0.9 \mu\text{m}$  thick  $n^{++}$  region was added to the bottom of the device as described in section 3.3. The thickness of the UID region was chosen such that at 250 V of reverse bias, the depletion region extended to just above the  $n^{++}$  layer. This would make the bottom region as effective as possible. The device was designed for a punch through voltage and depletion depth of 100 V and  $0.8 \mu\text{m}$  respectively. Punch through refers the point at which the depletion layer broke through the top layers and into the UID layer. All of the usable capacitance tuning occurred within the UID layer. Given the region thicknesses and doping levels, 1 dimensional calculations of depletion depth, electric field, and capacitance were possible using Poisson’s equation. The 2D effects would be modeled in a sophisticated device simulator and compared to the results obtained from calculations.

Shown below in figure 3.14 is the hi lo doping profile under analysis with  $N_{D1} = 1.9 \times 10^{17} \text{ cm}^{-3}$ ,  $t_1 = 0.8 \text{ }\mu\text{m}$ ,  $N_{D2} = 1.0 \times 10^{16} \text{ cm}^{-3}$ ,  $t_2 = 4.1 \text{ }\mu\text{m}$ ,  $N_{D3} = 5 \times 10^{18} \text{ cm}^{-3}$ , and  $t_3 = 5.0 \text{ }\mu\text{m}$ .

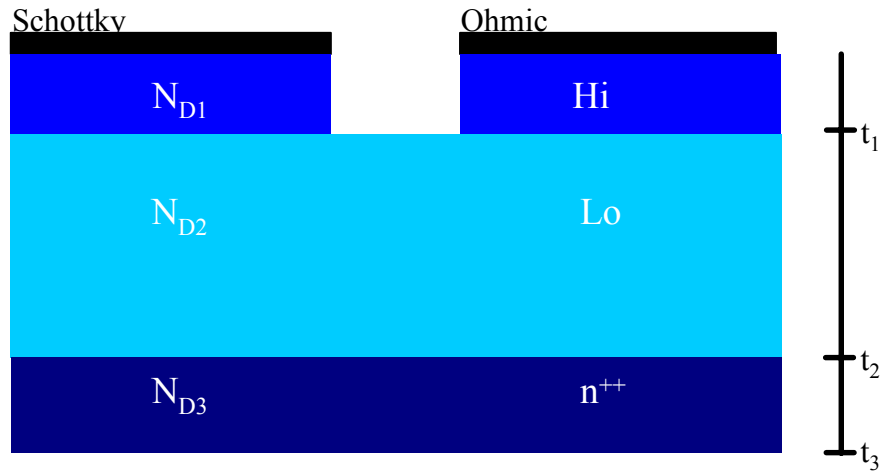


Figure 3.14: Hi lo device profile

Beginning with the electric field profile of figure 3.15, the punch through voltage can be solved for:

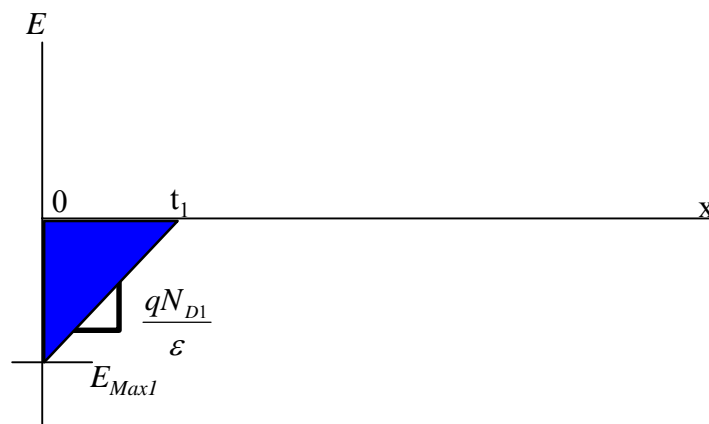


Figure 3.15: Electric field profile up to punch through voltage for hi lo

$$V_{Punch} = \frac{qN_{D1}}{2\epsilon}(t_1)^2 = 110 \text{ V} \quad (3.17)$$

$$E_{Max1} = -\frac{qN_{D1}}{\epsilon}t_1 = -2.75 \times 10^6 \frac{\text{V}}{\text{cm}} \quad (3.18)$$

With the electric field profile of figure 3.16, it was possible to calculate the approximate depletion depth and electric field of the device for 250 V of reverse bias.

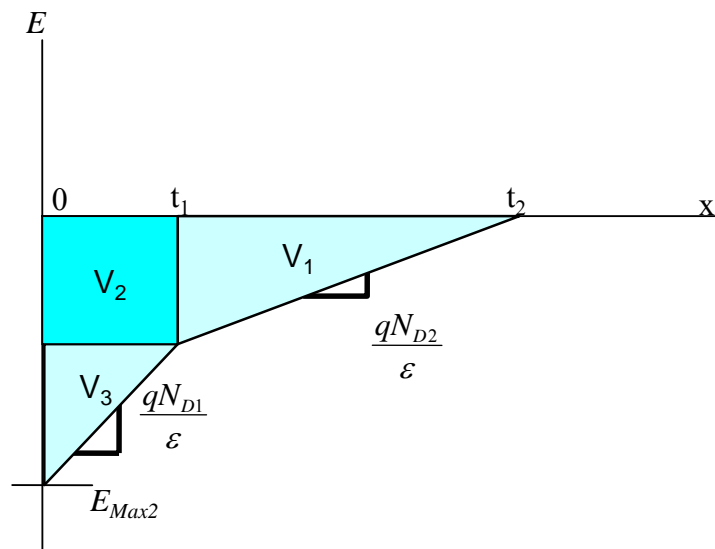


Figure 3.16: Electric field profile up to 250V of reverse bias for hi lo

The sum of  $V_1$ ,  $V_2$ , and  $V_3$  must equal the total reverse bias of 250 V.

$$V_1 + V_2 + V_3 = 250 \text{ V} \quad (3.19)$$

$$\frac{qN_{D2}}{2\varepsilon}(t_2 - t_1)^2 + t_1 \frac{qN_{D2}}{\varepsilon}(t_2 - t_1) + \frac{qN_{D1}}{2\varepsilon}(t_1)^2 = 250 \text{ V} \quad (3.20)$$

$$t_2 = \sqrt{\frac{500\varepsilon}{qN_{D2}} - \frac{N_{D1}}{N_{D2}}t_1^2 + t_1^2} = 4.02 \text{ } \mu\text{m} \quad (3.21)$$

$$E_{Max2} = -\frac{q}{\varepsilon}[N_{D2}(t_2 - t_1) + N_{D1}t_1] = -3.3 \times 10^6 \frac{\text{V}}{\text{cm}} \quad (3.22)$$

With equations 3.20 through 3.22 it was possible to estimate the depletion depth and electric field for 250 V of reverse bias. The high electric field estimation showed that the hi lo doping profile may be an inadequate design. The capacitance tuning ratio of the varactor was then estimated using the depletion depths at 100 and 250 V.

Assuming 30 stripes, a stripe length of 300  $\mu\text{m}$ , and a Schottky stripe width of 15  $\mu\text{m}$ :

$$C_{Max} = \frac{\varepsilon A}{t_1} = 15 \text{ pF}$$

$$C_{Min} = \frac{\varepsilon A}{t_2} = 3 \text{ pF}$$

$$\frac{C_{Max}}{C_{Min}} = \frac{t_2}{t_1} = \frac{4.02}{0.8} = 5 \quad (3.23)$$

Since the capacitance tuning ratio is high, the maximum tuning voltage could be reduced which will also lower the peak electric field.

Similar techniques were used to estimate the electric field and depletion depths of the lo hi lo [19] doping profile. The desired characteristic of this type of profile was electric field reduction. Beyond 0.8  $\mu\text{m}$ , the profile of the lo hi lo varactor was identical to that of the hi lo. The punch through voltages and hence tuning ratios were designed to be identical so that an unbiased comparison between the two layouts could be performed. Figure 3.17 is a schematic of the lo hi lo profile with  $t_1 = 0.4 \mu\text{m}$ ,  $t_2 = 0.8 \mu\text{m}$ ,  $t_3 = 4.1 \mu\text{m}$ ,  $t_4 = 5.0 \mu\text{m}$ ,  $N_{D1} = 1.0 \times 10^{16} \text{ cm}^{-3}$ ,  $N_{D2} = 2.4 \times 10^{17} \text{ cm}^{-3}$ ,  $N_{D3} = 1.0 \times 10^{16} \text{ cm}^{-3}$ , and  $N_{D4} = 5 \times 10^{18} \text{ cm}^{-3}$ .

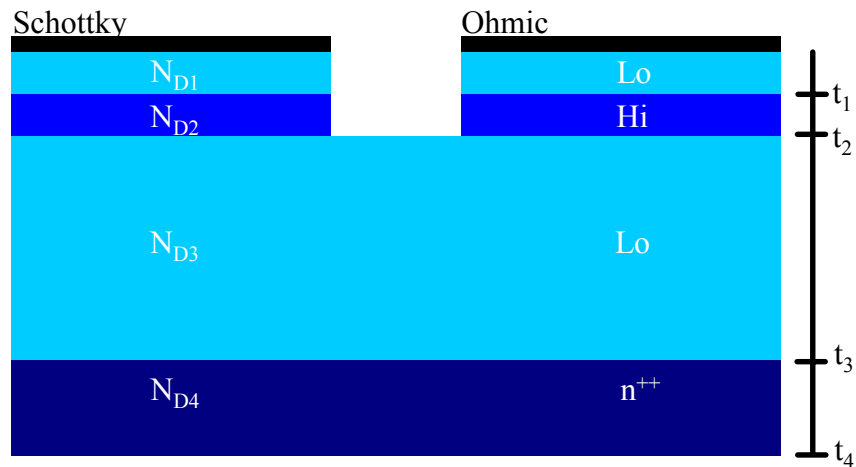


Figure 3.17: Lo hi lo device profile

Inspection of the electric field profile of the lo hi lo device up to the punch through voltage revealed the advantages that it had over the hi lo profile. Referring back to the electric field profile for the hi lo layout, notice that the area of the triangle was 110 volts and that the tip of the triangle represented the peak electric field. With the addition of the lo region above the hi region, the shape of the electric field profile

was altered to that in figure 3.18, and the same area was contained within a shape that had a much lower peak  $E_{Max1}$ . It became obvious that the best layout for electric field reduction was the lo hi lo profile with the thinnest possible hi region and the highest doping possible in said region, so that the original triangular shaped electric field profile approached that of a rectangle.

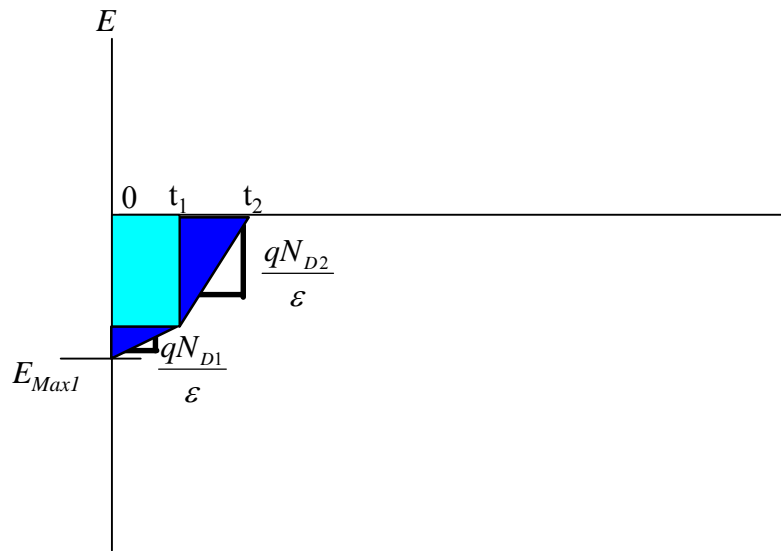


Figure 3.18: Electric field profile up to punch through voltage for lo hi lo

Equation 3.19 was modified to calculate the punch through voltage for the given

$$\frac{qN_{D2}}{2\epsilon} (t_2 - t_1)^2 + t_1 \frac{qN_{D2}}{\epsilon} (t_2 - t_1) + \frac{qN_{D1}}{2\epsilon} (t_1)^2 = 106 \text{ V} \quad (3.24)$$

$$E_{Max1} = -\frac{q}{\epsilon} [N_{D2} (t_2 - t_1) + N_{D1} t_1] = -1.8 \times 10^6 \frac{\text{V}}{\text{cm}} \quad (3.25)$$

dimensions and  $E_{Max1}$  was easily solved for by inspection.

The electric field was much lower for the lo hi lo case and can be reduced even further through the optimization of  $t_1$  and  $N_{D2}$ . By setting  $N_{D2}$  in equation 3.24 equal to the maximum doping level of  $5.0 \times 10^{18} \text{ cm}^{-3}$ , it was possible to calculate the thickest possible  $t_1$  assuming  $N_{D1} = 1.0 \times 10^{16} \text{ cm}^{-3}$ :

$$\frac{q(5 \times 10^{18})}{2\epsilon}(0.8 \mu m - t_1)^2 + t_1 \frac{q(5 \times 10^{18})}{\epsilon}(0.8 \mu m - t_1) + \frac{qN_{D1}}{2\epsilon}(t_1)^2 = 106 \text{ V} \quad (3.26)$$

$$t_1 = 785 \text{ nm}$$

The ‘delta doping’ approach to the lo hi lo design allowed for the lowest possible electric field thus far. Using the electric field profile of figure 3.19,  $E_{MAX1}$  of the optimized structure was calculated up to punch through:

$$E_{Max1} = -\frac{q}{\epsilon}[N_{D2}(t_2 - t_1) + N_{D1}t_1] = -1.5 \times 10^6 \frac{\text{V}}{\text{cm}}$$

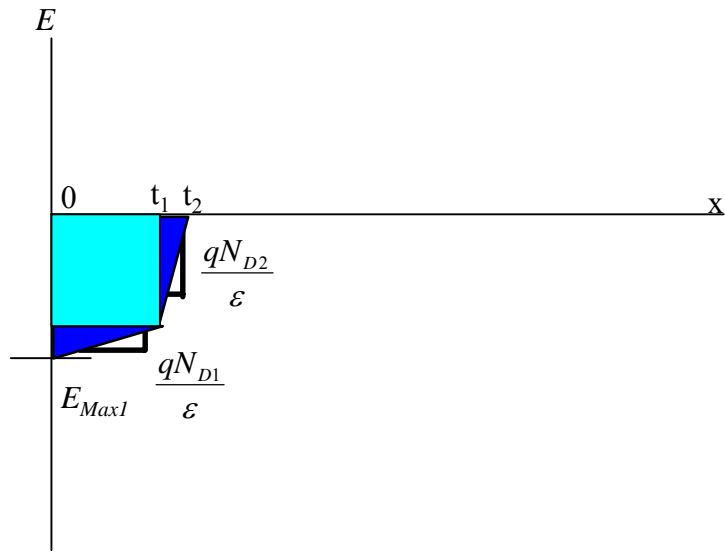


Figure 3.19: Electric field profile up to punch through voltage for optimized lo hi lo

The C-V and depletion depth analysis of the optimized lo hi lo varactor beyond punch through was identical to that of the hi lo design. The maximum electric field of the optimized device at 250 V of reverse bias was calculated using figure 3.20:

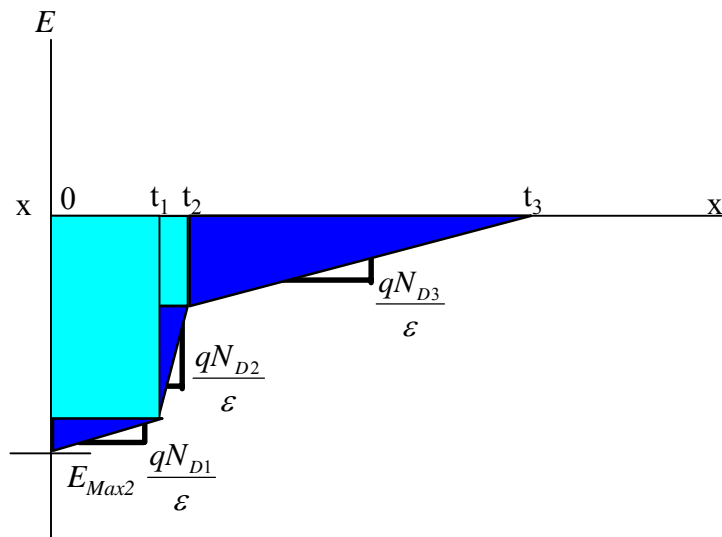


Figure 3.20: Electric field profile up to 250 V for optimized lo hi lo

$$E_{MAX2} = -\frac{q}{\epsilon} [N_{D3}(t_3 - t_2) + N_{D2}(t_2 - t_1) + N_{D1}(t_1)] = -2.08 \times 10^6 \frac{V}{cm} \quad (3.27)$$

For the exact same capacitance tuning ratio, the peak electric field of the lo hi lo design was over 1 MV less than the hi lo design.

The equations given in section 3.4 were used to estimate the total device resistance of the varactor diode. It was assumed that the resistances of the hi lo and lo hi lo designs were similar and this was justified since the  $n^{++}$  and middle lo regions were the same for both devices. It was assumed that the ohmic contact width was 7.5  $\mu\text{m}$ , the Schottky width was 15  $\mu\text{m}$ , the gap width was 3  $\mu\text{m}$ , the stripe length was 300  $\mu\text{m}$ , and there were 30 Schottky stripes. The mobility of GaN varies with ion implantation and threading dislocation density. In this study, the mobility parameters were based on calculated results incorporating only ion impurity scattering [3]. As processing techniques mature with time, measured Hall mobility data will approach the calculated data that was found. The following mobilities were used for the resistance calculations:

|         |                                    |                                    |
|---------|------------------------------------|------------------------------------|
| $N_D$   | $5 \times 10^{18} \text{ cm}^{-3}$ | $1 \times 10^{16} \text{ cm}^{-3}$ |
| $\mu_n$ | $350 \text{ cm}^2/\text{Vs}$       | $1350 \text{ cm}^2/\text{Vs}$      |

Table 3.1: Mobility parameters used for calculations

$$R_T(100 \text{ V}) = R_C + R_G + R_S + R_{Sp} = 0.23 \text{ } \Omega \quad (3.28)$$

For the stripe metal resistance,  $R_S$ , 10,000 Å gold layers were assumed for both the Schottky and ohmic contacts. In summary, the results, final layout dimensions, and dopant levels for the lo hi lo and hi lo are presented in tables 3.2 and 3.3:

|          | $E_{MAX2}$             | $R_T$  | $C_{MAX}/C_{MIN}$ |
|----------|------------------------|--------|-------------------|
| Hi Lo    | $3.3 \times 10^6$ V/cm | 0.23 Ω | 15pF/3pF          |
| Lo Hi Lo | $2.1 \times 10^6$ V/cm | 0.23 Ω | 15pF/3pF          |

Table 3.2: Electric field, C-V, and  $R_T$  results for lo hi lo and hi lo

|              | $t_1, N_{D1}$                                  | $t_2, N_{D2}$                                | $t_3, N_{D3}$                                | $t_4, N_{D4}$                              |
|--------------|--|--|--|--|
| Hi – Lo      | 0.8 μm<br>$2.4 \times 10^{17} \text{ cm}^{-3}$ | 4.1 μm<br>$1 \times 10^{16} \text{ cm}^{-3}$ | 5 μm<br>$5 \times 10^{18} \text{ cm}^{-3}$   | NA   |
| Lo – Hi – Lo | 0.785 μm<br>$1 \times 10^{16} \text{ cm}^{-3}$ | 0.8 μm<br>$5 \times 10^{18} \text{ cm}^{-3}$ | 4.1 μm<br>$1 \times 10^{16} \text{ cm}^{-3}$ | 5 μm<br>$5 \times 10^{18} \text{ cm}^{-3}$ |

Table 3.3: Device dimensions and dopant levels for lo hi lo and hi lo

# Chapter 4

## Simulation Results and Comparisons

### 4.1 Simulator Setup

Silvaco Atlas was selected as the simulator of choice and extra care was taken in setting it up for the most realistic results possible. Code defining the desired simulation was entered into the Deckbuild text editor. The single cell block of the simulated device consisted of half of the Schottky contact, the entire ohmic contact, the gap in between them, and the epilayers underneath. The simulated space region was defined through the creation of a triangulated mesh of user defined resolution. The default length of the device was set to 1  $\mu\text{m}$  by the simulator. The extremely thin highly doped region of the lo hi lo design required extra precision. Figure 4.1 shows the triangular mesh assignment for the lo hi lo design. The hi lo design did not require a special mesh because the feature sizes were all much larger. Coarse triangular mesh spacing was used in the regions with larger features.

Once the triangulation was complete, the space was divided into several regions: two for each top layer underneath the contacts, one for the air between the contacts, one for the thick lo region, and one for the bottom conductive layer. The air region between the two contacts is colored purple in figure 4.1. Each region was given specific material parameters which defined the electron mobility, ion implantation, bandgap, saturation velocity, affinity, and dielectric constant. Data for mobility vs.  $N_D$  was taken from [3].

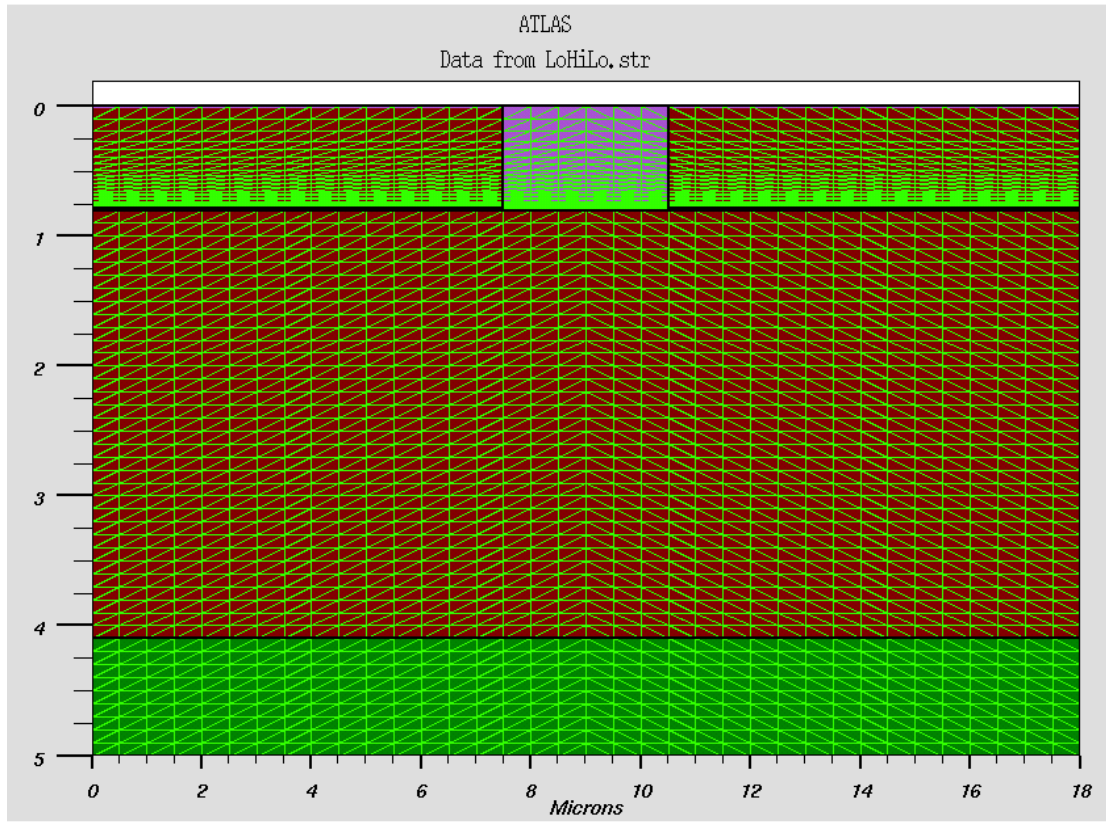


Figure 4.1: Mesh assignment for lo hi lo design

The ohmic contact assignment statement only required the contact resistance and it was set to  $5 \times 10^{-6} \Omega\text{-cm}^2$ . Data from [13] suggested much lower values of contact resistance but the ohmic contacts were not the source of resistance in this device, so the modest value used was acceptable. The Schottky contact statement required the assignment of the workfunction of the metal. The proper barrier height was set using the metal workfunction and electron affinity of the material. The electron affinity of GaN and workfunction of the metal were set to 4.1 eV and 5.0 eV respectively, which set the barrier height to 0.9 eV.

Simple statements defining the DC voltage sweep and small signal AC analysis were used to extract the desired conductance and capacitance data. Large voltage steps (22.5 V) were taken between 0 and 90 V. In between 90 and 110 V, the sweep step was reduced to 5 V so that the punch through voltage could accurately be observed. Beyond 110 V, the step size was increased to 20V. The target AC frequency for this project was 1.2 GHz.

Modifications to the lo hi lo doping profile were required to achieve the desired punch through voltage of 100 V. Recall that calculations were made and the hi region thickness and concentration level was set to 15 nm and  $5 \times 10^{18} \text{ cm}^{-3}$  respectively. The simulator automatically added a doping profile to the lo regions modeling the effects that the lo – hi – lo interface would have. Electrons in the hi region diffused into the lo regions causing enough band bending in the lo regions for the Fermi levels to align. This was the source of the added doping profile that the simulator took into account. Some fiddling with numbers gave a new thickness of 10 nm and a concentration of  $1.2 \times 10^{18} \text{ cm}^{-3}$ . Figures 4.2 and 4.3 show the net doping for each device and the depletion depth at 250 V of reverse bias. The depletion depth is illustrated with a red line and can be found underneath the Schottky contact, or anode.

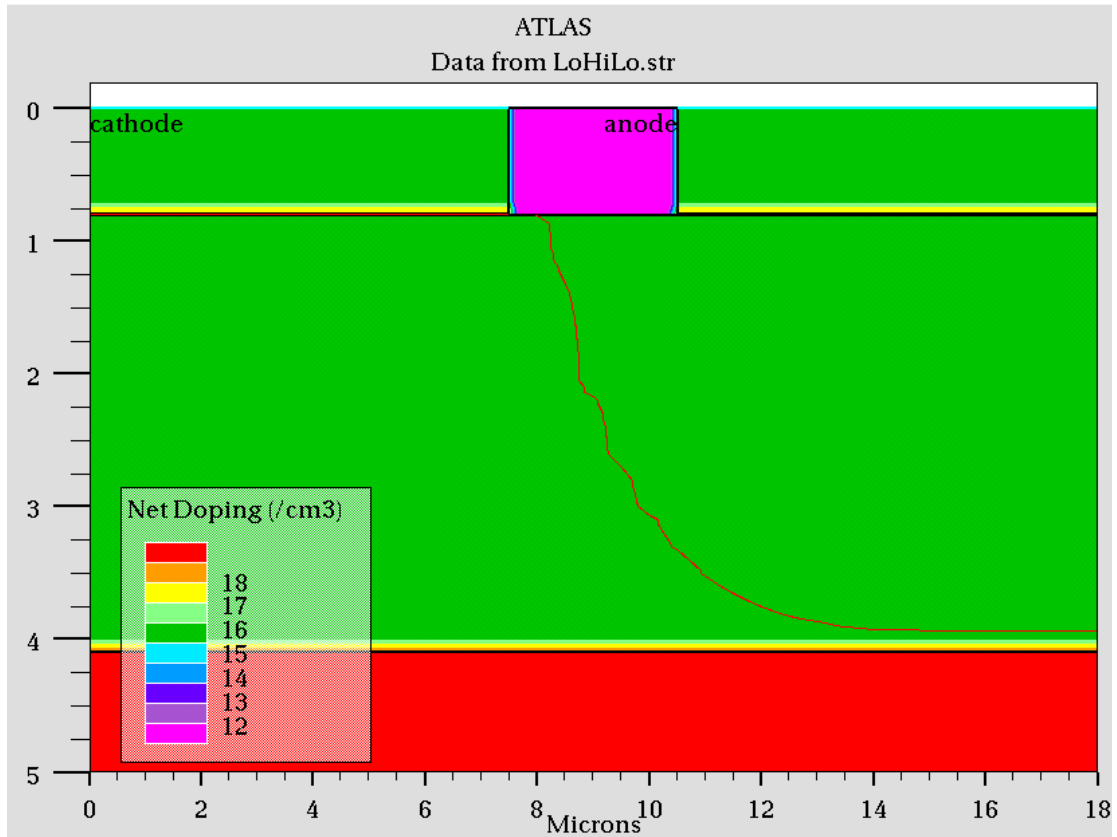


Figure 4.2: Ion implantation and 250V depletion depth for lo hi lo design (curved red line represents depletion depth)

Previous calculations gave excellent approximations to the total depletion depth at 250 V of reverse bias. It was desired to have the depletion region right up against the bottom n<sup>++</sup> region at 250 V. Since both devices were identical beyond 0.8  $\mu\text{m}$ , nearly identical depletion depths were observed at 250 V.

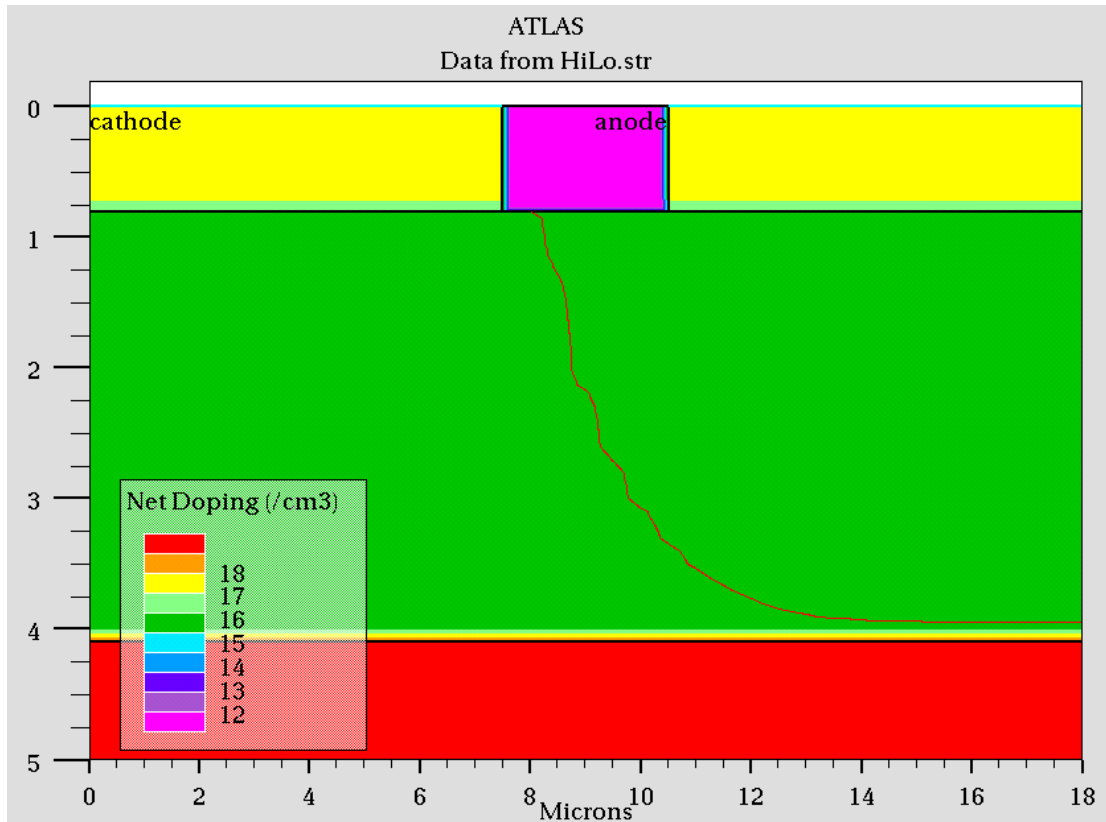


Figure 4.3: Ion implantation and 250V depletion depth for hi lo design (curved red line represents depletion depth)

## 4.2 C-V Results and Equivalent Circuits

The outputs of the AC portion of the simulation consisted of a series capacitance with shunt conductance between the two electrodes. The desired circuit format was the series combination of the two components. Figures 4.4 and 4.5 show the two equivalent circuits. The desired equivalent network was obtained through a few simple calculations. The objective was to convert the shunt conductance into a series resistance through the following relations:

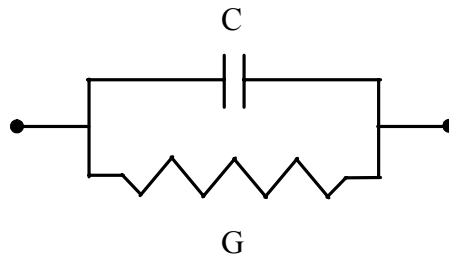


Figure 4.4: Simulator's output equivalent circuit

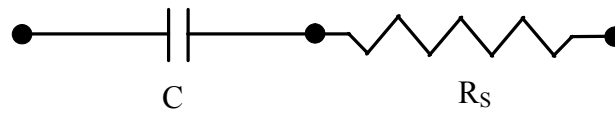


Figure 4.5: Desired equivalent circuit

$$X^2 = \left( \frac{1}{\omega C} \right)^2 \quad (4.1)$$

$$R_s = G \cdot X^2 \quad (4.2)$$

Once the conversion was made, the values required proper scaling to take in to account the actual dimensions of the device. The default units that the simulator used were  $\Omega \cdot \mu\text{m}$  and  $\text{F}/\mu\text{m}$ . For 30 stripes of length  $300 \mu\text{m}$ , the total resistance and capacitance,  $R_T$  and  $C_T$ , were found using:

$$C_T = 2 \cdot 30 \cdot 300 \cdot C \quad (4.3)$$

$$R_T = \frac{1}{2} \cdot \frac{1}{30} \cdot \frac{1}{300} \cdot R \quad (4.4)$$

With everything in place, the data was plotted for both the hi lo and lo hi lo cases (figure 4.6). There was a slightly lower value of capacitance for the lo hi lo device at the punch through voltage for the following reason: punch through for the hi lo device actually occurred at a slightly smaller depth because the charge exchange between the hi and lo region depleted more of the hi region in this device because it was not as heavily doped. In the lo hi lo design, the charge exchange at the hi lo interface did not deplete as much space in the hi region because the hi region was doped much heavier. At 100 V of reverse bias, a 50 nm difference in depletion depths translated into a 1.3 pF discrepancy. The hi lo device could have easily been tailored so that the 100 V punch through depletion depth was also exactly 0.8  $\mu\text{m}$ .

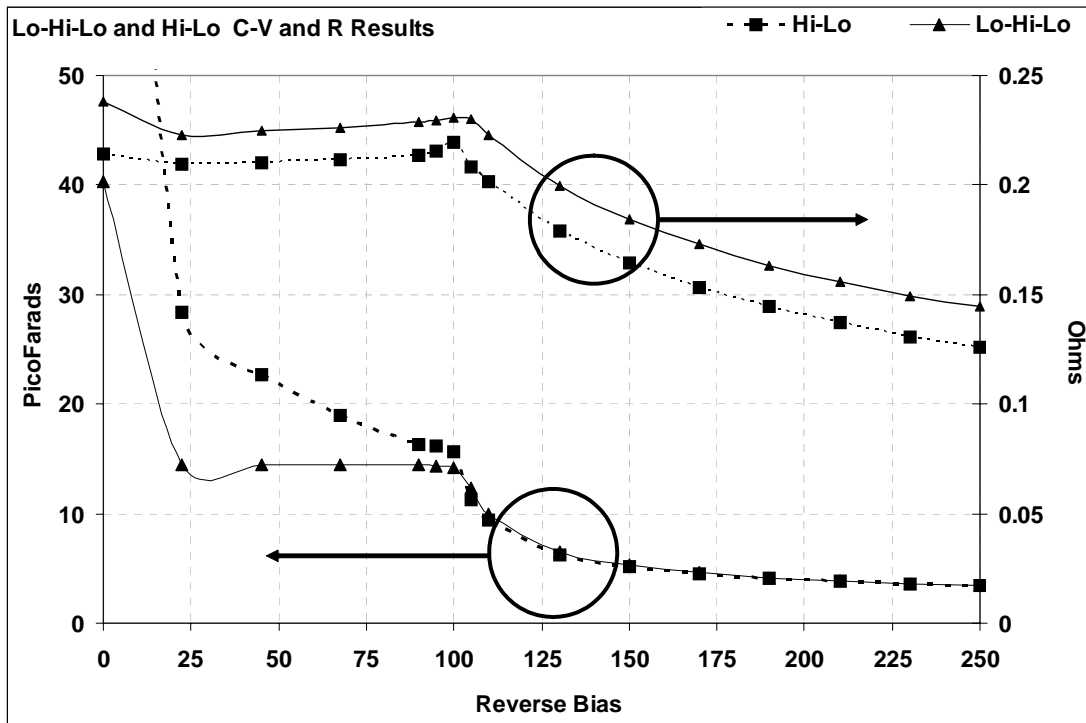


Figure 4.6: C-V and Resistance data for the lo hi lo and hi lo cases

|          | Calculated $R_T$ | Simulated $R_T$      | Calculated $C_T$ | Simulated $C_T$ |
|----------|------------------|----------------------|------------------|-----------------|
| Lo Hi Lo | 0.23 $\Omega$    | 0.23 – 0.14 $\Omega$ | 15 – 3 pF        | 14.4 – 3.5 pF   |
| Hi Lo    | 0.23 $\Omega$    | 0.22 – 0.12 $\Omega$ | 15 – 3 pF        | 15.7 – 3.4 pF   |

Table 4.1: C-V and Resistance data for the lo hi lo and hi lo cases

The data shown above in table 4.1 shows that the calculated data, which did not take into account fringing, was relatively close to the data taken with the simulator. It is safe to say that the simulator need only be used as a confirmation tool for calculations that have already been done by hand. The simulator also took time to

run so writing code in a mathematical software package would speed up the design process.

### 4.3 Q & Power Dissipation

All of the Q calculations were based upon two devices in series and at a center frequency of 1.2 GHz. Putting the two devices in series would half the capacitance and double the resistance found from the previous simulations. The power dissipation calculations were based upon the shunt conductance model and a 100 V input signal, again at 1.2 GHz. Both Q and power dissipation were calculated at 100 and 250 V of reverse bias.

| Lo Hi Lo Device | Total Series Resistance ( $R_{ts}$ ) | Total Capacitance ( $C_t$ ) |
|-----------------|--------------------------------------|-----------------------------|
| 100 V           | 0.46 $\Omega$                        | 7.2 pF                      |
| 250 V           | 0.29 $\Omega$                        | 1.75 pF                     |

Table 4.2: Capacitance and resistance of common cathode lo hi lo device based on C-V simulations

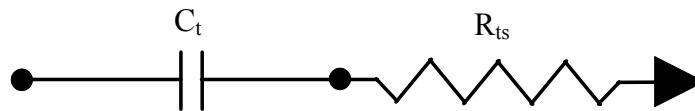


Figure 4.7: Equivalent series circuit

The techniques which were used earlier to convert the shunt conductance to a series resistance were used to convert the series resistance back to a shunt. In the

common cathode arrangement, the anode of one of the devices will always be connected to ground. The conversion from series to shunt resistance went as follows:

$$Q_S = \frac{X_S}{R_{ts}} \quad (4.5)$$

$$R_{tp} = Q_S^2 R_{ts} = \frac{X^2}{R_{ts}} \quad (4.6)$$

which changed the equivalent series circuit model to that shown in figure 4.8.

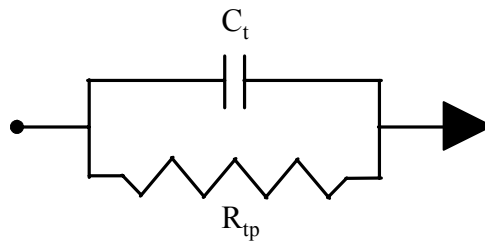


Figure 4.8: Equivalent shunt circuit

| Lo Hi Lo Device | Total Parallel Resistance ( $R_{tp}$ ) | Total Capacitance ( $C_t$ ) |
|-----------------|--|-----------------------------|
| 100 V           | 738 $\Omega$                           | 7.2 pF                      |
| 250 V           | 1,167 $\Omega$                         | 1.75 pF                     |

Table 4.3: Total capacitance and resistance of common cathode lo hi lo device based on C-V

The power dissipated due to resistive losses was calculated based upon a 1.2 GHz, 100 V peak signal. The complex current was calculated using the equivalent impedance of the varactor. The time average power was found using the following equations:

$$I^* = \frac{V}{Z} = V \left( \frac{1}{X} + \frac{1}{R_p} \right) \quad (4.7)$$

$$P_{Avg} = \frac{1}{2} \text{Re}\{V \cdot I^*\} \quad (4.8)$$

| <b>Lo Hi Lo Device</b> | <b>Q</b> | <b>Average Power</b> |
|------------------------|----------|----------------------|
| 100 V                  | 40       | 6.75 Watts           |
| 250 V                  | 270      | 0.24 Watt            |

Table 4.4: Q and average power for 100 V and 250 V of reverse bias

The stripe dimensions were critical in maximizing Q and minimizing the average power. Reducing the stripe size decreased the total capacitance of the device while increasing the total resistance. The high power dissipation was a consequence of the high capacitance of these devices relative to the frequency of operation. Halving the capacitance through stripe modifications ultimately doubled the total resistance and cut the average power dissipated in half.

## 4.4 Field Plate and Notching for Electric Field Reductions

In an effort to reduce the electric field of the device, two techniques were investigated: the notched architecture and the field plate. The original device that was under investigation is pictured in figure 4.9. It represents the simplest form of the device, a hi lo doping profile with the entire top layer intact (no notch). The electric field build up of this device was high and improvements were necessary.

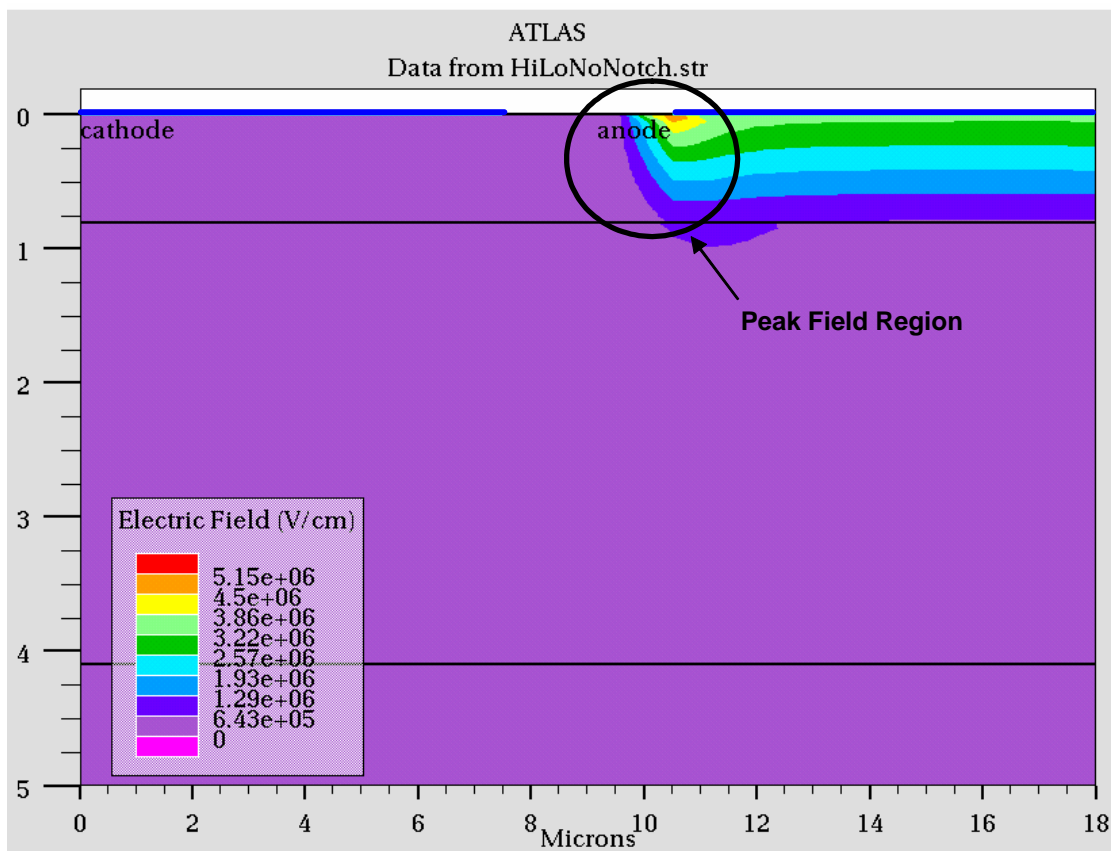


Figure 4.9: Cross section of the hi lo device without the notch removed

The field plate is used in GaN HEMTs to increase RF power output. SiN is deposited over the gate metal, touching both the source and drain. The SiN above the gate is then covered with metal which is electrically connected to the gate. The field plate reduces the electric field underneath the gate contact. The same concept was implemented in the varactor design. The GaN region between the anode and cathode was not notched for the field plate simulations. The cross section of the field plate device is shown below in figure 4.10. The two electrodes named anode are in electrical contact. The SiN layer was 250 nm thick and the top anode extended an additional 1.5  $\mu\text{m}$  past the bottom anode. High fields appeared in the SiN layer,

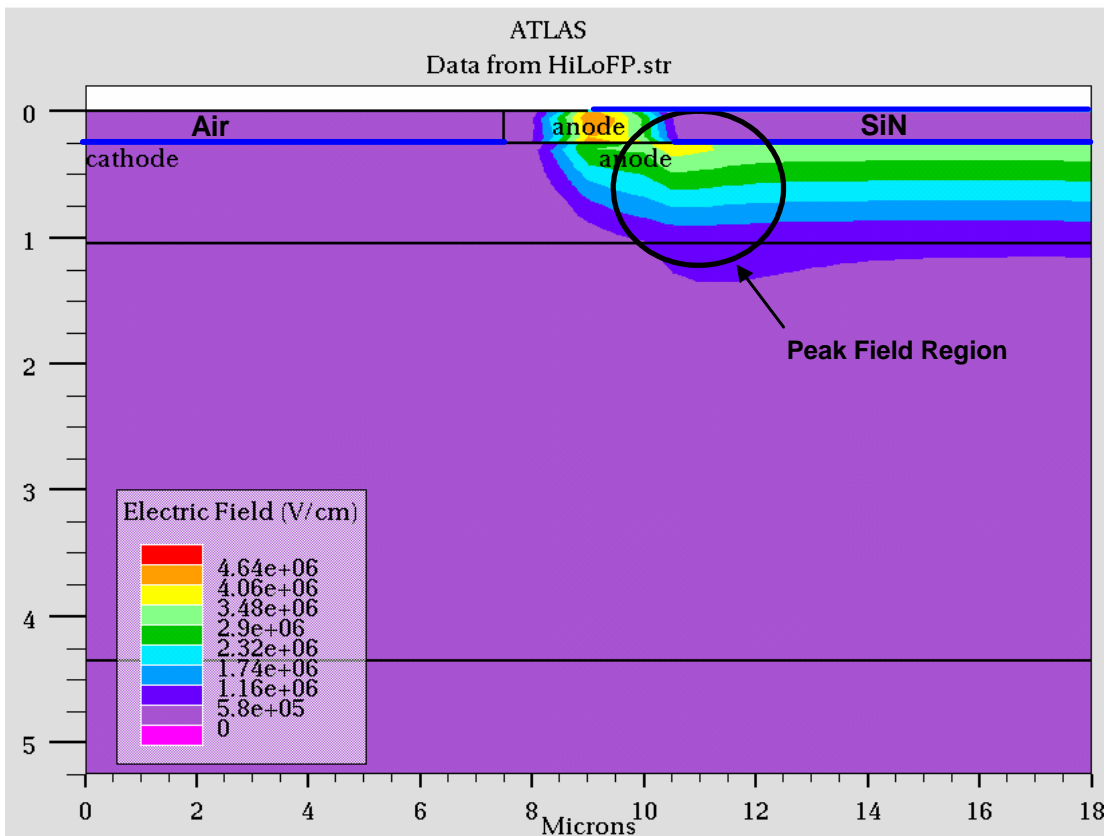


Figure 4.10: Cross section of the hi lo device with the added field plate. Note that the notch was not used.

but the fields in the GaN, which was what we were concerned with, were reduced.

The final method of field reduction was the familiar notched architecture, where the top layer of GaN in between the anode and cathode was removed. The cross section of a notched device is shown in figure 4.11. Recall that drawings of this type of architecture were used earlier to present the device in chapter 3.

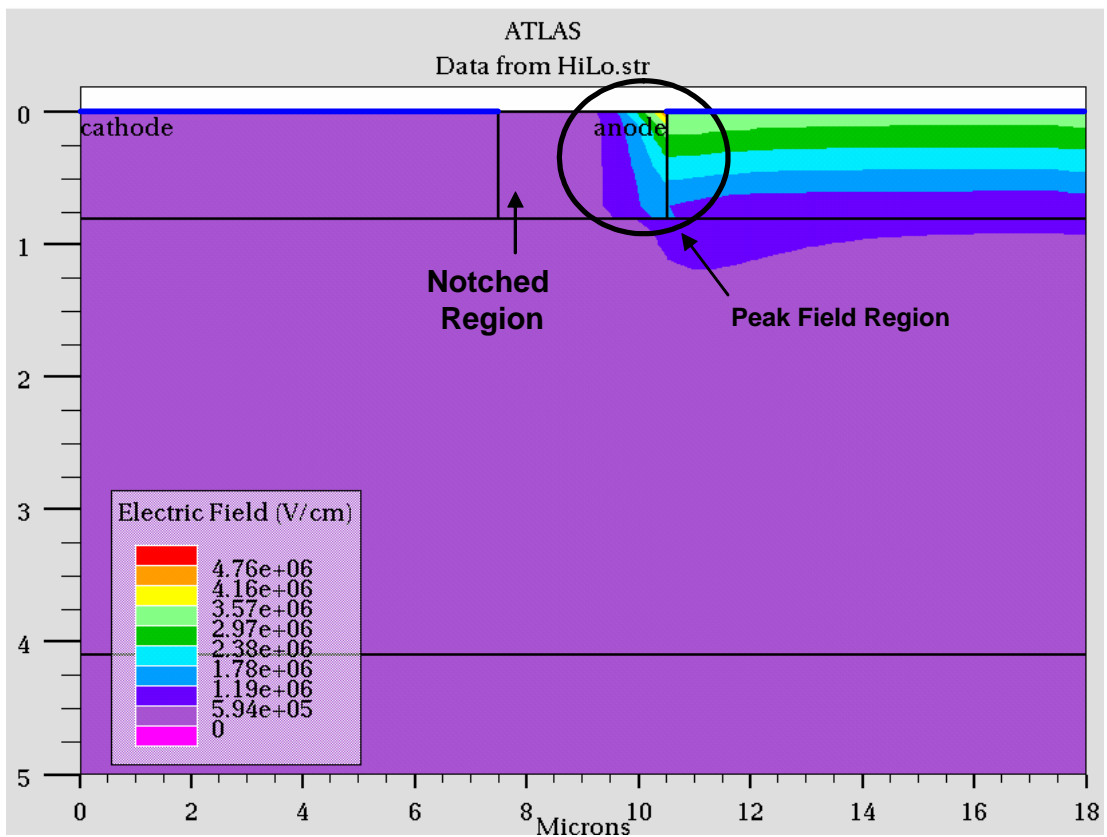


Figure 4.11: Cross section of the hi lo device with the notch removed.

Table 4.5 presents the results of the electric field simulations and compares the notched hi lo, no notch hi lo, and field plate hi lo designs. It was clear through

simulation that the notched architecture was the most effective at reducing the electric field in this device.

|                          | Peak $E_{Max}$ at 250 V Reverse bias |
|--------------------------|--------------------------------------|
| Notched Hi Lo Device     | $3.5 \times 10^6$ V/cm               |
| Field Plate Hi Lo Device | $4.0 \times 10^6$ V/cm               |
| No Notch Hi Lo Device    | $5.0 \times 10^6$ V/cm               |

Table 4.5: Summary of peak electric fields for different field reducing techniques

## 4.5 Electric Fields of Notched Hi Lo and Lo Hi Lo Devices

The maximum breakdown field of GaN is  $3 \times 10^6$  V/cm as reported in [20]. Electric field profiles were plotted underneath the edge of the Schottky contact where high fringing fields built up. The electric field far from the Schottky contact edge was examined and presented in table 4.6. Figure 4.12 gives an example of where the electric fields were analyzed. The cuts taken at the edge of the anode (dashed line) are plotted in figures 4.13 and 4.14 for the hi lo and lo hi lo devices.

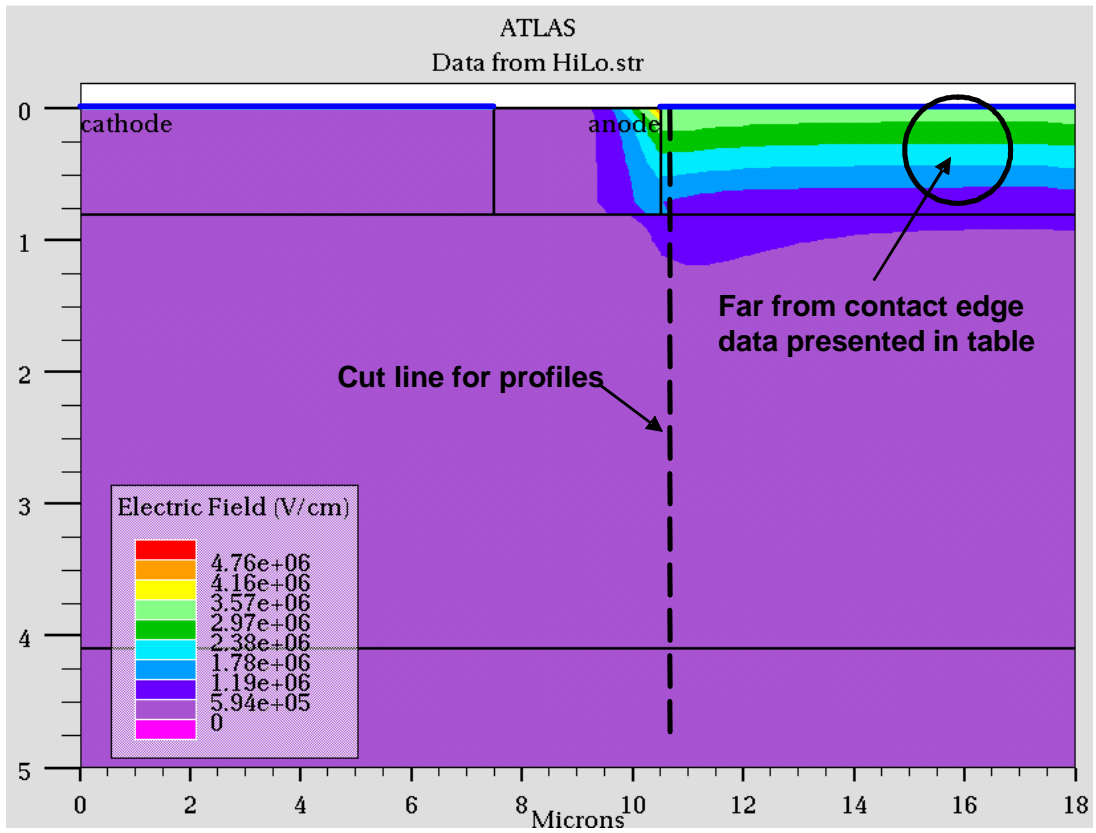


Figure 4.12: View of where cut line was made for the electric field profiles. Circled region is where far from contact edge data was taken.

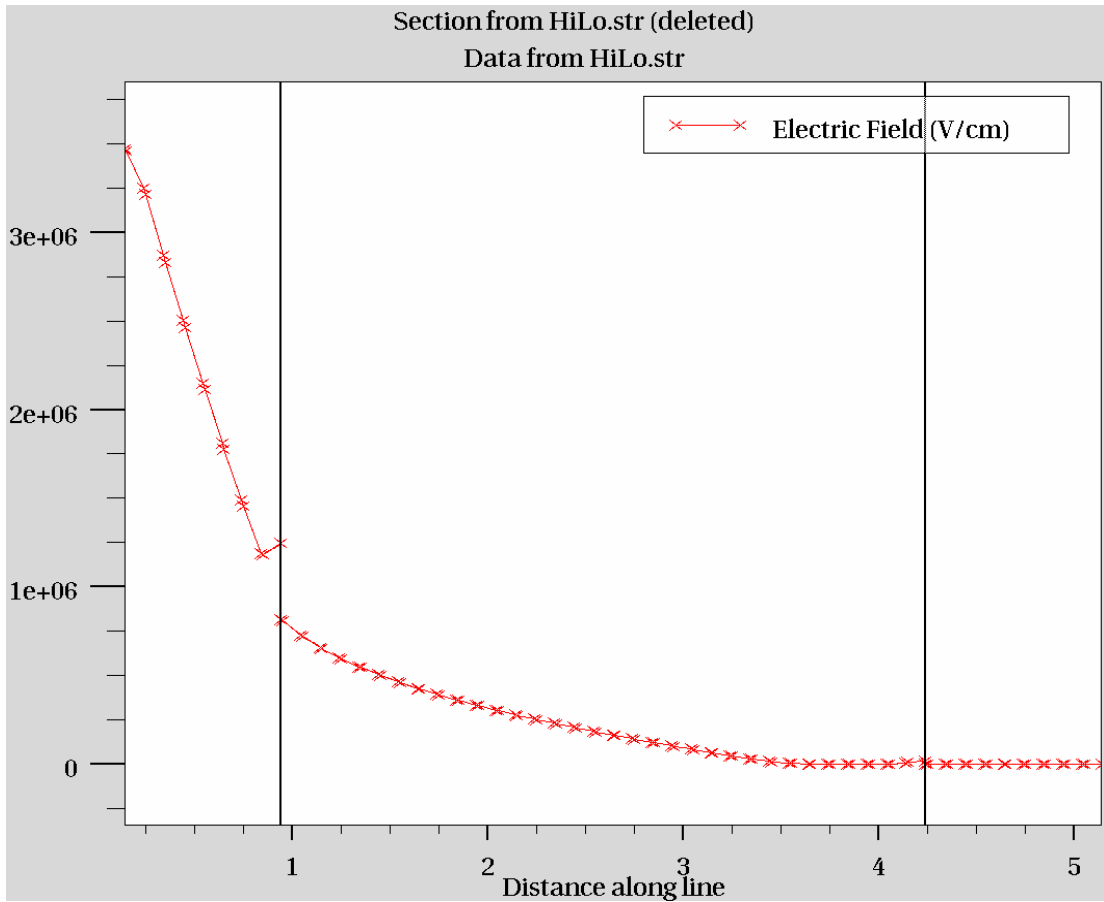


Figure 4.13: Electric field profile at the edge of the Schottky contact for hi lo device

The figure above shows a peak field of  $3.5 \times 10^6$  V/cm underneath the Schottky contact. The steep slope in between 0 and 0.8  $\mu\text{m}$  was a consequence of the relatively strong doping in the hi region. In the lo region, the slope is much more gradual due to the UID in this layer.

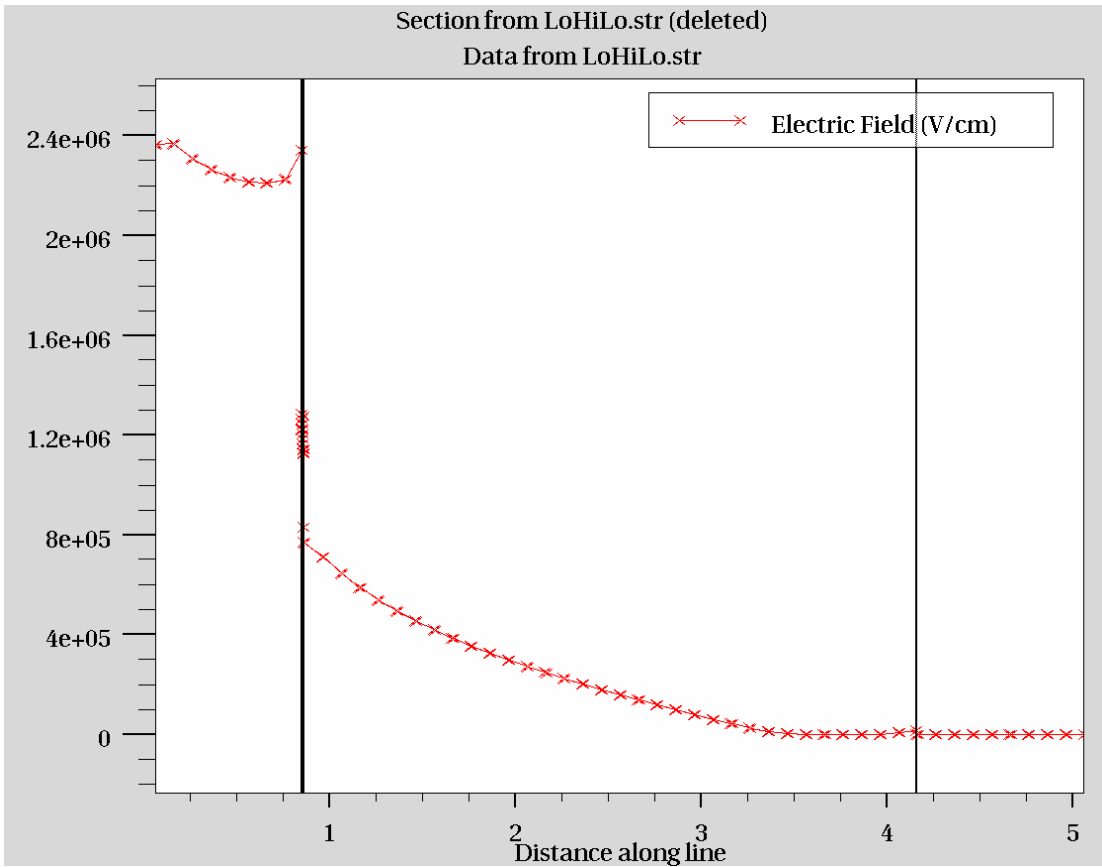


Figure 4.14: Electric field profile at the edge of the Schottky contact for lo hi lo device

As expected, the peak electric field of the lo hi lo device was much lower, only  $2.4 \times 10^6$  V/cm. The slope of the profile is for the most part flat, or rectangular, in the thick lo region, while the slope in the thin hi region is extremely steep.

The values far from the edge of the junction were in much closer agreement to the calculated values. Table 4.6 summarizes the calculated and simulated electric field data far from the edge of the Schottky contact.

|          | Calculated $E_{Max}$    | Simulated $E_{Max}$             |
|----------|-------------------------|---------------------------------|
| Lo Hi Lo | $2.08 \times 10^6$ V/cm | $2.0 \times 10^6$ V/cm $\Omega$ |
| Hi Lo    | $3.30 \times 10^6$ V/cm | $3.17 \times 10^6$ V/cm         |

Table 4.6: Calculated and simulated peak electric fields far from Schottky edge

# Chapter 5

## Conclusions

### 5.1 Feasibility of Proposed Device

The device structure proposed in this report was designed with an optimistic outlook. Nearly all of the GaN varactor designs used the absolute minimum and maximum levels of doping, tall mesa structures, and deep mesa etches. An unintentional doping (UID) level of  $1 \times 10^{16} \text{ cm}^{-3}$  [3] was used for the analysis of all varactor designs. Typically, there are higher tolerances towards the low end of the doping spectrum. For a feasible design, it would be wise to use a doping level slightly higher than the UID. This would allow for greater consistency between device batches, with the cost being increased electric fields and hence premature breakdown. The thicknesses of the epitaxial layers are a bit thick but if the  $i_0$  regions are doped slightly above the UID for tolerance control; the overall thickness of the device will be reduced.

The lowest possible doping was desired because low doping concentrations translate into larger changes in depletion depth for a given voltage step. As a result of using low doping levels, the mesa structures needed to support the amount of depletion depth for high voltages were large, up to  $6 \mu\text{m}$  tall if a buffer region is included. With reductions in the UID, the current varactor design has room for improvements. In conclusion, one possible research area in the field of material science is the investigation of UID reduction in GaN.

There does remain some uncertainties in the mesa etch for this structure. It will take some experimentation to develop the techniques required for the deep mesa etch. Another area which may need some development is the method of contacting the device. It may be possible to planarize the structure with a spin on polymer. Bond pads could then be deposited right next to the mesa structures, and in the same plane.

## **5.2 Problems Encountered**

There were a few problems which arose in this design project involving the limited amount of information on GaN in literature and the feasibility of the proposed device layout. GaN is a relatively new material in the electronics world and there is a limited amount of information for it. Some consultation with material growers was necessary in order to determine the limitations of GaN growth. There was a generous supply of journal papers available, but with the advancements in research taking place today, many of them were outdated.

Schottky gate leakage could create some hurdles in the design of this device. In a paper published in 1996 [12], 250  $\mu\text{m}$  circular Ni dots were deposited on n-GaN ( $1 \times 10^{17} \text{ cm}^{-3}$ ). For a reverse bias of 90 V, 1 mA of leakage current was observed. Scaling the area up to  $1 \text{ cm}^2$ , the leakage current would be 2 Amps or 2 Amps/ $\text{cm}^2$ . Similarly, at 45 V of reverse bias, the scaled current would be 100 mA/ $\text{cm}^2$ . The quality of GaN in 1996 was not as good as it is today. Epitaxial defects result from the lack of GaN substrates and from contaminants in MOCVD reactors. Defects in

GaN films can be traps or scattering centers and may cause premature device degradation [14]. With increasing reverse bias, the suspected trap levels consume charge and current spikes were observed. With improvements in material growth, the Schottky leakage current will decrease, but in the meantime, some methods to reduce the reverse current have been developed [14]. KOH etch prior to Ni deposition reduced the reverse current in GaN to  $10^{-10}$  Amps/cm<sup>2</sup> at a reverse bias of 5 V. The experiment did not comment on reverse bias greater than 5 V. In [15], the GaN samples were allowed to oxidize in a dry O<sub>2</sub> chamber and this method also reduced the amount of reverse current. As the material fabrication processes matures, the problem of reverse current will subside.

### **5.3 Recommended Next Steps**

It has been proven that the notched lo hi lo doping profile outperforms the hi lo profile in voltage breakdown. The equations given in this report provide the designer with fairly accurate methods of analysis. Basically every parameter can be set (punch through voltage, punch through thickness, etc) and then the doping levels and top layer thicknesses can be solved for. An interesting study would be to solve for the highest punch through voltage that still allows for useable  $C_{Max}/C_{Min}$  before breakdown.

Once the method of mesa etching is determined, the device would be ready for fabrication and testing. The test that stands out the most at this point is the reverse

current leakage and breakdown voltage and these should be tested immediately on a semiconductor parameter analyzer.

## Appendix

```
#Code for Lo Hi Lo device
go atlas
```

```
#Section 1: Mesh definition
```

```
MESH SPACE.MULT = 1
X.MESH LOCATION = 0.0 SPACING = 0.5
X.MESH LOCATION = 18.0 SPACING = 0.5
```

```
Y.MESH LOCATION = 0.0 SPACING = 0.1
Y.MESH LOCATION = 0.7 SPACING = 0.1
Y.MESH LOCATION = 0.79 SPACING = 0.001 #Mesh with tight
Y.MESH LOCATION = 0.8 SPACING = 0.001 # triangulation
Y.MESH LOCATION = 0.801 Spacing = 0.1
Y.MESH LOCATION = 5.0 SPACING = 0.1
```

```
#Section 2 Regions and Electrodes
```

```
region num=1 mat=GaN x.min=0.0 x.max=7.5 y.min=0.0 y.max=0.79 #lo
region num=2 mat=AIR x.min=7.5 x.max=10.5 y.min=0.0 y.max=0.8 #notch
region num=3 mat=GaN x.min=10.5 x.max=18.0 y.min=0.0 y.max=0.79 #lo
region num=4 x.min=0.0 x.max=7.5 y.min=0.79 y.max=0.8 #hi
region num=5 x.min=10.5 x.max=18.0 y.min=0.79 y.max=0.8 #hi
region num=6 mat=GaN x.min=0.0 x.max=18.0 y.min=0.8 y.max=4.1 #lo
region num=7 x.min=0.0 x.max=18.0 y.min=4.1 y.max=5.0 #n++
```

```
electrode num=1 name = cathode x.min=0.0 x.max=7.5
electrode num=2 name = anode x.min= 10.5 x.max=18.0
```

```
contact name = cathode con.resistance = 5.0e-6 #contact resistance
contact name = anode workfunction =5.0 #metal workfunction
```

```
#Section 3: Doping Definition
```

```
doping region = 1 uniform concentration=1E16 n.type #lo
doping region = 3 uniform concentration=1E16 n.type #lo
doping region = 4 uniform concentration=1.2E18 n.type #hi
doping region = 5 uniform concentration=1.2E18 n.type #hi
doping region = 6 uniform concentration=1E16 n.type #lo
doping region = 7 uniform concentration=5E18 n.type #n++
```

#### #Section 4 Material & Model Definitions

```
material material=GaN mun=1350 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \  
  copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \  
  nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
material region=4 mun=700 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \  
  copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \  
  nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
material region=5 mun=700 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \  
  copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \  
  nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
material region = 7 mun=350 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \  
  copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \  
  nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
method newton
```

```
output con.band val.band #included total electric field in profile
```

```
# DC Sweep and Small signal AC analysis
```

```
log outfile = LoHiLo.log
```

```
solve init #zero bias solution
```

```
solve vcathode = 0 vstep=22.5 vfinal=90 name = cathode AC FREQ = 1200e6
```

```
solve vcathode = 95 vstep=5 vfinal=100 name = cathode AC FREQ = 1200e6
```

```
solve vcathode = 130 vstep=20 vfinal=250 name = cathode AC FREQ = 1200e6
```

```
save outfile=LoHiLo.str #save the structure file which contains doping, fields, etc
```

```
tonyplot LoHiLo.str
```

```
quit
```

```
#Code for Hi Lo device
go atlas
```

```
#Section 1: Mesh definition
```

```
MESH SPACE.MULT = 1
X.MESH LOCATION = 0.0 SPACING = 0.5
X.MESH LOCATION = 18.0 SPACING = 0.5
```

```
Y.MESH LOCATION = 0.0 SPACING = 0.1
#Y.MESH LOCATION = 1.0 SPACING = 0.1
#Y.MESH LOCATION = 10.5 SPACING = 0.1
Y.MESH LOCATION = 5.0 SPACING = 0.1
```

```
#Section 2 Regions and Electrodes
```

```
region num=1 x.min=0.0 x.max=7.5 y.min=0.0 y.max=0.8 #hi
region num=2 mat=AIR x.min=7.5 x.max=10.5 y.min=0.0 y.max=0.8 #notch
region num=3 x.min=10.5 x.max=18.0 y.min=0.0 y.max=0.8 #hi
region num=4 mat=GaN x.min=0.0 x.max=18.0 y.min=0.8 y.max=4.1 #lo
region num=5 x.min=0.0 x.max=18.0 y.min=4.1 y.max=5.0 #n++
```

```
electrode num=1 name = cathode x.min=0.0 x.max=7.5
electrode num=2 name = anode x.min= 10.5 x.max=18.0
```

```
contact name = cathode con.resistance = 5.0e-6 #contact resistance
contact name = anode workfunction =5.0 #metal workfunction
```

```
#Section 3: Doping Definition
```

```
doping region = 1 uniform concentration=1.9E17 n.type #hi
doping region = 3 uniform concentration=1.9E17 n.type #hi
doping region = 4 uniform concentration=1E16 n.type #lo
doping region = 5 uniform concentration=5E18 n.type #n++
```

```
#Section 4 Material & Model Definitions
```

```
material region = 1 mun=750 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \
copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \
nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
material region = 3 mun=750 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \
copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \
nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
material material=GaN mun=1350 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \  
  copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \  
  nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
material region = 5 mun=350 mup=10 affinity=4.1 eg300=3.4 vsatn=2.0e7 \  
  copt=6.84e-10 taun0=1.e-9 taup0=2.e-8 permittivity=9.5 \  
  nc300=2.07e18 nv300=1.16e19 arichp=72 arichn=23 edb=0.025 eab=0.16
```

```
method newton  
output con.band val.band
```

```
# DC Sweep and Small signal ac analysis with s-parameter calculation  
log outfile = HiLo.log  
solve init  
solve vcathode = 0 vstep=22.5 vfinal=90 name = cathode AC FREQ = 1200e6  
solve vcathode = 95 vstep=5 vfinal=100 name = cathode AC FREQ = 1200e6  
solve vcathode = 130 vstep=20 vfinal=250 name = cathode AC FREQ = 1200e6  
save outfile=HiLo.str
```

```
tonyplot HiLo.str  
quit
```

```
#Variable assignments for material statements (relevant for both code sets):  
#mun = electron mobility, mup = hole mobility, affinity = material electron affinity,  
#eg300 = room temperature bandgap, vsatn = electron saturation velocity, taun0 =  
#electron lifetime, taup0 = hole filetime, permittivity = permittivity (dimensionless),  
#nc300 = electron concentration at edge of conduction band, arichn=electron  
#Richardson constant, edb = donor energy level
```

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