University of California, Santa Barbara
Dept. of Electrical and Computer Engineering
ECE154 - Computer Architecture
Syllabus

Instructor:	Professor Ryan Kastner (kastner@ece)	
TA:	Shahnam Mirzaei (shahnam@umail)	
Lecture Schedule:	Tuesday/Thursday 5:00-6:15pm, Phelps 1508	
Discussion:	Wednesday 6-6:50pm 387 101 Wednesday 7-7:50pm 387 103	
Quizzes	In class, Tuesday October 30 In class, Tuesday November 21	
Final Exam	7:30-10:30pm Thursday, December 14	
Office Hours	Instructor Office Hours:	Instructor Office Hours: Tuesday 4-5pm, Thursday 2-3pm @ Harold Frank Hall, Room 4123
	TA Office Hours:	Shahnam: ???, Phelps 1435
Grading:	Homework Assignments: 30% Quiz #1: 15% Quiz #2: 15% Final: 40% Class Participation 5%	
Text Book:	*Computer Organization and Design: The Hardware/Software Interface*, Third Edition By David A. Patterson and John L. Hennessy ISBN 1558606041	
Homework:	There will be approx. 6 homework assignments	

Calendar – subject to change

Date	Topic	Announcements	Reading
September 27	Lecture 1 - Introduction to Computer Architecture	Homework #0 assigned	P+H Chapter 1, Moore's original article
October 2	Lecture 2 - Instruction Set Architecture	Homework #0 due Homework #1 assigned	P+H 2.1-2.3
October 4	Lecture 3 - Addressing Modes and MIPS ISA		P+H 2.4-2.6, 2.8-2.10, 2.13, 2.15-2.18
October 9	Lecture 4 - Computer Arithmetic I: Addition	Homework #2 assigned	P+H 3.1-3.3
October 11	Lecture 5 - Computer Arithmetic II: Multiply & Shift	Homework #1 due	P+H 3.4
October 16	Lecture 6 - Computer Arithmetic III: Division	Homework #3 assigned	P+H 3.5
October 18	Lecture 7 - Performance	Homework #2 due	P+H Chapter 4, Characterizing performance article
October 23	Lecture 8 - Single Cycle Processor I: Datapath		P+H 5.1-5.3
October 25	Lecture 9 - Single Cycle Processor II: Control	Homework #3 due	P+H 5.4
October 30	Quiz #1	Homework #4 assigned	
November 1	Lecture 10 - Multiple Cycle Processor I: Datapath		P+H 5.5
November 6	Lecture 11 - Multiple Cycle Processor II: Control	Homework #5 assigned	P+H 5.7
November 8	Lecture 12 - Pipelined Processor I	Homework #4 due	P+H 6.1, 6.2
November 13	Lecture 13 - Pipelined Processor II		P+H 6.3-6.6
November 15	Lecture 14 - Pipelined Processor III	Homework #5 due	
November 20	Quiz #2	Homework #6 assigned	
November 22	No Class - Thanksgiving		
November 27	Lecture 15 - Memory Hierarchy I		P+H 7.1-7.3, 7.5
November 29	Lecture 16 - Memory Hierarchy II	Homework #6 due	
December 4	Lecture 17 – Memory Hierarchy III		P+H 7.4
December 6	Lecture 18 - Final Review		
December 13	Final		