

University of California, Santa Barbara

Department of Electrical and Computer Engineering

Course Syllabus

ECE 152B

Digital Design Methodologies

5 units

Catalog description:

Design methodologies of digital systems, the register and processor levels. Design of functional subsystems, including arithmetic processors, hardwired and microprogrammed control units, memory systems, and bussing systems. System organization including communication, input/output systems, and multiple CPU systems. (S)

Prerequisites: ECE 152A

Text, References, and Software:

Text: Computer Systems Design and Architecture, 2nd Edition, V.P. Heuring and H. F. Jordan, Pearson Prentice Hall, 2004. ISBN: 0-13-048440-7

Reference: Digital Design, Preview Edition, Frank Vahid, John Wiley & Sons, 2006. ISBN 0-471-46784-7 (Chapters 5, 6.5 and 6.6 of this book are covered in lecture. Reprints of these chapters are made available at UCSB Bookstore for purchase.)

Software: Altera FPGA design environment, Quartus-II and ModelSim simulator

Website: <http://cadlab.ece.ucsb.edu/ece152B/ece152B.html>

Course Goals

1. Top-down design methodologies for computer design:
 - a. Master the RTL design methodology from constructing high-level state machine, to creating datapath, to connecting datapath to controller, and to deriving the controller FSM.
 - b. Able to design a computer system starting from informal description, to formal Register Transfer Notation (RTN) description, to block diagram architecture, to concrete RTN steps, to hardware design of blocks, to generation of control sequences and finally to the control unit design with proper consideration of timing and clocking
2. Understand the timing and clocking issues for modern digital system design:
 - a. Understand the delay modeling of cells and interconnects
 - b. Understand clock skew problems and how to utilize clock skew for clock period minimization
 - c. Understand various timing optimization techniques: pipelining, retiming, clock-tree buffering
3. Design, implementation and testing of a simple RISC processor:
 - a. Able to design 1-bus, 2-bus and 3-bus RISC processor
 - b. Able to design fixed-point and floating-point arithmetic units
 - c. Able to design control units

- d. Able to design memory system

Class/Laboratory hours

Two 75-minutes lectures per week. 3-hour scheduled lab per week. Laboratory is open by card key access. Minimum of 6 hours per week is required.

Contribution to program outcomes

Course Goals	P1	P2	P3	P4	P5	P6
1.a		X	X	X	X	
1.b		X	X	X	X	
2.a		X	X		X	
2.b		X	X		X	
2.c		X	X	X	X	
3.a		X	X	X	X	
3.b		X				
3.c		X	X	X	X	
3.d		X				

Professional component

Lab projects 1 and 2 require the design, implementation and testing of a simple 4-bit RISC processor with given specifications, constraints (economic and environmental) and design tradeoffs using a set of given components. Successful demonstration of running a specified test program and a detailed design report are required. The material builds upon the basic logic design techniques from ECE152A.

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