Hybrid III-V and IV lasers and amplifiers

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(Invited Paper)

Abstract *Silicon evanescent lasers and amplifiers have been demonstrated utilizing low temperature wafer bonding technology. This approach enables the creation of high performance, small footprint active devices on silicon for photonic integrated circuits.*

Introduction

Photonic integration has progressed greatly in realizing various functions for optical interconnects as well as long haul communication systems. Silicon photonics is a promising platform to fabricate dense photonic integrated circuits on a large silicon wafer using highly accurate silicon processing technology. Raman lasers [1,2] and amplifiers [3], high speed modulators [4,5], and photo detectors [6,7] have been successfully demonstrated and have widened the applications of silicon as an optoelectronic material. However, a key hurdle for realizing practical silicon based photonic integrated circuit is achieving electrically pumped silicon lasers and amplifiers due to silicon's indirect bandgap. Recently, electrically pumped silicon evanescent lasers [8,9] and amplifiers [10] have been demonstrated utilizing low temperature wafer bonding technology. This approach has led to the realization of active devices with compact size and high performance on silicon for photonic integrated circuits.

Silicon evanescent device platform and general fabrication process

The silicon evanescent device is a hybrid structure that consists of an offset multiple quantum well region bonded to a silicon waveguide which is fabricated on a silicon-on-insulator (SOI) wafer. With this architecture, the optical mode can obtain electrically pumped gain from the III-V region while being guided by the underlying silicon waveguide region. Silicon waveguide dimensions primarily determine the confinement factor of each region, i.e., quantum well or silicon waveguide region. In general, a wider or higher waveguide confines more of the optical mode in the silicon waveguide, while reducing the optical mode overlap with the quantum wells.

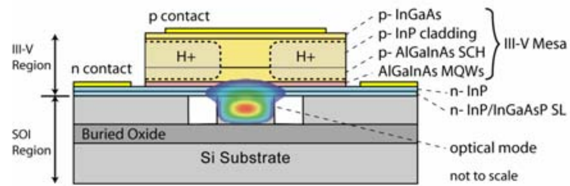


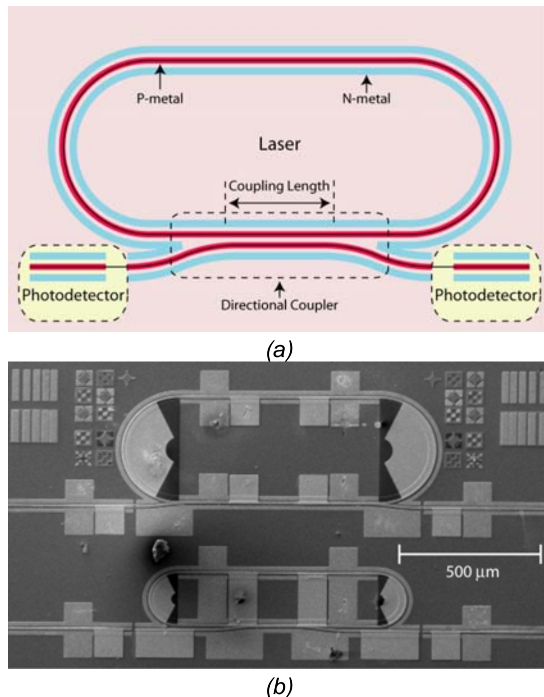
Fig.1. Cross sectional structure of silicon evanescent devices

The general fabrication process is described as follows. The silicon waveguide is first fabricated using standard lithography and dry etching process on a Silicon-on-insulator (SOI) wafer. The III-V structure containing AlGaInAs quantum wells grown on a InP substrate is transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding at a 300 ºC annealing temperature. After removal of the InP substrate, a mesa is formed on the III-V layer (Fig.1) using standard lithography, and wet and dry etching processes. After Ni/AuGe/Ni/Au and Pd/Ti/Pd/Au contacts are deposited for n-contact and p-contact respectively, proton (H+) implantation on the p doped layers of the mesa is performed to create a current channel for carrier confinement and to electrically isolate different device regions. Ti/Au probe pads are then deposited on the top of the mesa. If necessary, the sample is dice and polished to create facets to couple the light into or out of the device. More information on epitaxial structure and device fabrication process can be found in Ref. 8.

Silicon evanescent racetrack lasers

Ring and racetrack resonator structures are attractive to build onchip lasers that do not rely on facet polishing and dicing for cavity definition. The layout of the silicon evanescent racetrack laser is shown in Fig. 2a. It consists of a racetrack ring resonator with a straight waveguide length of 700 microns. Two device set with different radii of 100 and 200 microns are fabricated. A 400 microns long directional coupler is formed on the bottom arm by placing a bus

waveguide 0.5 micron away from the racetrack. The laser power is collected into the two 440 micron long photodetectors placed at the two outputs of the directional coupler. These photo-detectors have the same waveguide architecture as the hybrid laser. The only difference is that they are reverse-biased to collect photo-generated carriers. The silicon waveguide has a final height, width, and rib-etch depth of 0.69 μm, 1.65 μm, and 0.5 μm, respectively. The calculated overlap of the optical mode with the silicon waveguides is 64 % while there is a 4.2 % overlap in the quantum wells. The top view of the fabricated device is shown in Fig. 2b.



(a)

(b)

Fig.2. (a) cross sectional structure (b) layout of the racetrack laser with two photodetectors.

The laser is driven by applying a positive bias voltage to the top p-probe contact while the optical power is measured by the two photodetectors on each side of the coupler. The photocurrent is measured while reverse biasing the photodetectors at -5V. Since the testing of the lasers are done all on chip without polishing and dicing the lasing spectrum is measured by collecting scattered light near the bends of the ring through a fiber probe. The entire silicon chip is mounted on a TEC controller which allows the operating temperature of the laser to be varied from 0 °C to 80 °C. A responsivity of 1.25 A/W (100 % quantum efficiency) to convert the measured photocurrent to the laser output power. Measurements of individual photodetectors indicate the quantum efficiency is in excess of 90%[11]. Figure 3 shows the measured total c.w. laser output power which is the sum of the optical power measured at both detectors as a function of injected current for various operating temperatures ranging from 15 to 60 °C for the laser with a ring radius of 200 microns. As can be seen from Fig. 3, the laser threshold is 175 mA with a maximum output power of 29 mW at 15 °C. The maximum power is limited by the available drive current to the device. The laser has a 60 °C maximum lasing temperature with a characteristic temperature of 55 K. The laser has a threshold voltage of 1.75V and a series resistance of 3.5 ohms.

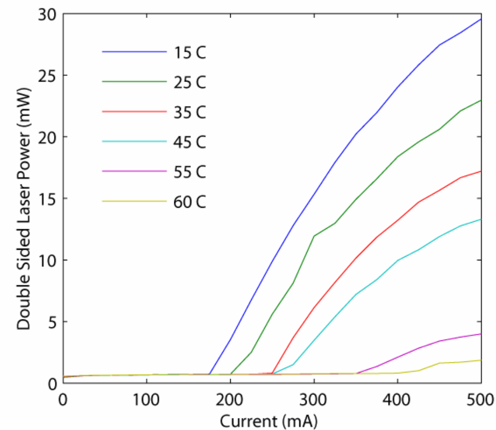


Fig. 3 The LI curve for a laser with radius R = 200 microns, and coupler length of 400 microns for various temperature.

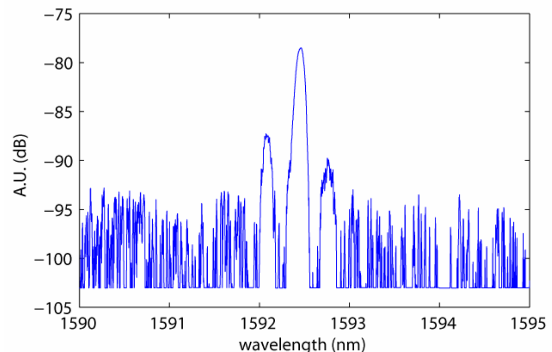


Fig. 4 The hybrid laser spectrum taken at 240 mA for a R = 100, coupler length = 400 microns

Figure 4 shows the measured multi-mode lasing spectrum from a laser with a ring radius of 100 microns driven at 240 mA. The spectrum was measured with a resolution bandwidth of 0.1 nm. The lasing wavelength is 1592.5 nm with a 0.21 nm mode spacing corresponding to a group index of 3.67.

Silicon evanescent amplifiers

Optical amplifiers are also important components in realizing high levels of photonic integration as they compensate for optical losses from individual photonic elements. Silicon evanescent amplifiers are fabricated with the same fabrication process described above with the sample facets being

polished at an angle of 7 ° to the optical waveguides before antireflection coatings Ta_2O_5 (~5 %) are applied. The final device length is ~ 1.36 mm. The cross sectional SEM image is shown in Fig. 5. A silicon strip waveguide with a width of 2 µm and a height of 0.76 µm is used. The calculated overlap of the optical mode for the fabricated device dimensions are 74 % in the silicon waveguide and 3.4 % in the AlGaInAs quantum wells.

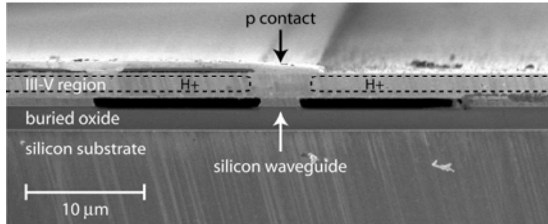


Fig. 5. Cross sectional SEM image of the fabricated amplifier.

The device gain is measured by launching and collecting the signal through lensed fibers at both the input and output facets at a temperature of 15 °C. The coupling efficiency from the device to the fiber is measured to be -5 dB by measuring the insertion loss at long wavelengths. Figure 6 shows the measured small-signal fiber-to-fiber gain and, on the second y-axis, the estimated chip gain using 5 dB coupling loss per fiber. The maximum fiber-to-fiber gain is 3 dB corresponding to a chip gain of 13 dB at 1575 nm. The inset of the figure represents the net modal gain, Γg-α, where Γ is the QW confinement factor, g is the material gain, and α is the waveguide loss. The dotted line of the inset is a data fit using the logarithmic function between the material gain and the current density at the active region. At lower current densities, the gain increases logarithmically while at higher current densities it saturates due to device heating caused by the series resistance (7.5 Ω) and thermal impedance (40 K/W). The maximum gain occurs at 1575 nm with a spectral full-width at half-maximum of 62 nm at 200 mA.

The 3 dB output saturation power from the chip is measured to be 11 dBm as shown in Fig. 7. The evanescent coupling scheme of the device structure typically provides 2 % to 3 % of QW confinement factor, resulting in higher output saturation powers than amplifiers with centered quantum wells whose typical confinement factor is around 5 % to 15 %.

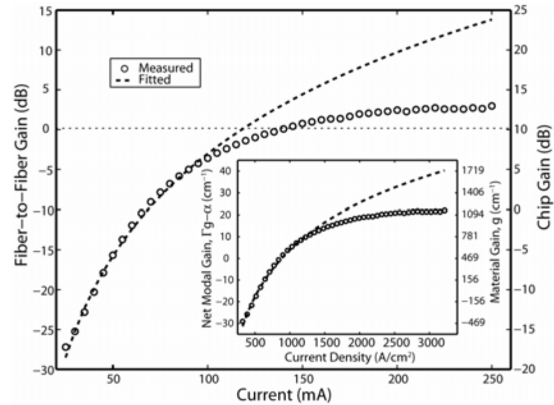


Fig. 6. Amplifier gain vs current (inset) Net modal gain extracted from the chip gain vs current density at 1575 nm

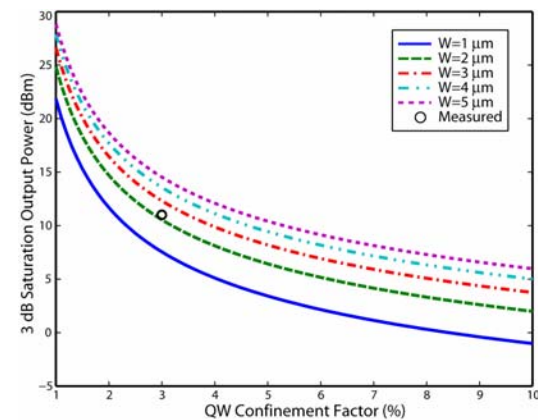


Fig. 7. 3dB saturation output power vs. confinement factor and different optical mode width.

The measured noise figure varies between 13 dB and 10 dB depending on the current level. The internal noise figure of the device can be between 8 dB and 5 dB, considering the 5 dB coupling loss.

In the case of preamplification applications, dynamic characteristics and power penalty are also important for high speed data detection. To investigate the dynamic performance of the device, BER measurements are employed at 3 different data rates, 2.5Gbps NRZ, 10Gbps NRZ and 40Gbps RZ. A PRBS of 2^{31}-1 was used to carry out the measurements for 10 Gbps and 40 Gbps, while a shorter sequence of 2^{10}-1 is chosen for 2.5 Gbps. The average input power is -16 dBm to keep the device unsaturated. A variable optical attenuator (VOA) is inserted between the output of the amplifier and the receiver to adjust the received power. The power penalty of the amplifier is extracted by comparing the BER performances of the transmitter-amplifier-receiver link with the back-to-back transmitter. As shown in Fig. 8, a low power penalty of 0.5 dB for all three data rates is achieved and it is mainly induced from the ASE noise. To compare the distortion due to the pattern effect, another BER curve with a higher

input power of 2 dBm is also plotted in Fig. 8. An additional power penalty of 0.5 dB is required when pattern effects start to reduce the Q-factor of the signal.

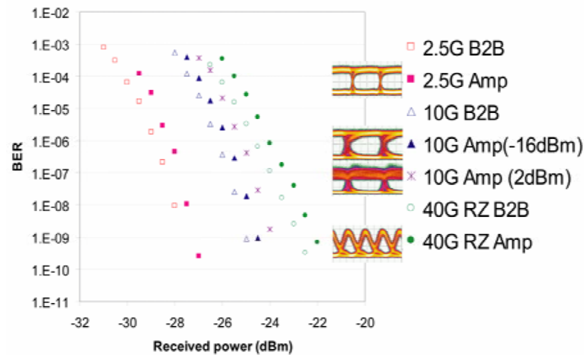


Fig.8. BER and eye diagrams. From left to right: 2.5G back-to-back (B2B), 2.5G amplified (Amp),10G B2B, 10G Amp (low input, -16dBm), 10G Amp (high input, 2dBm), 40G RZ B2B, 40G RZ Amp.

Conclusions

The hybrid silicon evanescent waveguide architecture has been used to demonstrate amplifiers, photodetectors, and lasers. The amplifiers operated with maximum on chip gains of ~13 dB and 11dBm saturation power. The racetrack lasers demonstrated operated up to 60 ^{o}C with 29 mW output power. This active device platform can be used in conjunction with silicon multiplexers/de-multiplexers, add-drops, and high speed modulators without suffering the high coupling losses between active and passive sections leading to a highly integrated photonic circuit.

Acknowledgement

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