Highly Efficient Vertical Outgassing Channels for Robust, Void-Free, Low-Temperature Direct Wafer Bonding

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Low-temperature direct wafer bonding is favored for dissimilar materials integration, particularly in III-V compound semiconductors-to-silicon integration for attraction from desirable functionalities of direct-bandgap materials and standard low-cost CMOS manufacturing technologies. Unlike mature silicon-to-silicon or SiO_2 bonding techniques, however, low-temperature anneal (<400 °C) in compound semiconductor-to-silicon bonding is rigorously required to minimize thermal expansion mismatch-induced stress and potential thermal material degradation. Interfacial voids are likely to form at the bonding interface due to lack of high anneal temperature to drive gas byproducts (H_2O vapor mostly and some H_2, N_2 and CO_2) out of the bonding interface effectively.

In this paper we propose and demonstrate an efficient approach to achieve void-free, low-temperature direct wafer bonding on the *non-amorphous material-on-amorphous material* substrate, e.g., silicon-on-insulator (SOI) in this work by employing a vertical outgassing channel (VOC) design. Fig. 1 shows the schematic of VOCs which are essentially etched holes through the top non-amorphous material layer to lead gas byproducts diffusing into the underneath amorphous layer for efficient outgassing. In this work, InP epitaxial material is directly bonded onto the SOI wafer, and H_2O molecules migrating to the closest VOC are quenched in the buried oxide layer quickly by combining with bridging oxygen ions and forming pairs of stable nonbridging hydroxyl groups (Si-OH). In order to study the effectiveness of this approach, VOC (6×6 μm in dimension) regions with variable channel spacing of 50, 100, 200, and 400 μm in Fig. 2 are patterned on 1.1×1.1 cm^2 SOI samples with 1 mm wide VOC-free surrounding boundaries to eliminate potential interaction from the adjacent sections and edges. O_2 plasma-assisted wafer bonding process after sample cleaning is then performed to enable InP-SOI spontaneous attachment at room temperature. Following a short anneal (10-120 min.) at 300 °C with 1.5 MPa external pressure, InP substrate is selectively removed in HCl solution, resulting in a ~ 2 μm thick epitaxial layer transfer onto SOI. A microscopic image (50×) in Nomaski mode in Fig. 3 shows a drastic contrast on a 2 hour anneal sample, where bubble-free bonding is achieved at area with VOCs (100 μm spacing) while high-density (average 9×10^4 cm^2) voids distribute in boundary area uniformly, exhibiting a highly efficient outgassing capability. In VOC region InP epitaxial layer is tightly bonded to SOI as shown in a scanning electron microscopic cross-sectional image (Fig. 4) of a cleaved sample, where no InP deformation is observed in VOC area. Compared with VOC-free, directly bonded sample, interfacial void density has been reduced enormously from a conservative count of 9236 cm^{-2} down to zero in Fig. 5 with little different in term of channel spacing. A small real-state footprint of <1.5% of the total bonding area is also noticed, indicating negligible impact to bonding strength and great freedom in device layout design. The inset photograph of a 2×2 cm^2 InP epitaxial layer bonded on SOI exhibits the same void-free bonding, revealing a promising perspective in bonding scalability since SiO_2 accommodation capacity per unit volume to H_2O byproduct is identical regardless of the size of wafers. Another merit of VOC design is to enable dramatic reduction in anneal time (Fig. 6) owing to the fast gas molecules diffusion at bonding interface to VOCs. Conventional anneal time of 12-18 hours required to bond the same 1 cm^2 InP sample onto SOI in our lab has been reduced to 30 min while void-free bonding is still attainable in VOC region with 50 μm spacing. Further anneal time reduction is limited by gas molecules migration to VOCs, which can be accomplished by decreasing the channel spacing. It is finally noted that VOC approach is as well applicable in a variety of other bonding situations where gas byproducts need to be removed before strong bond is initiated.

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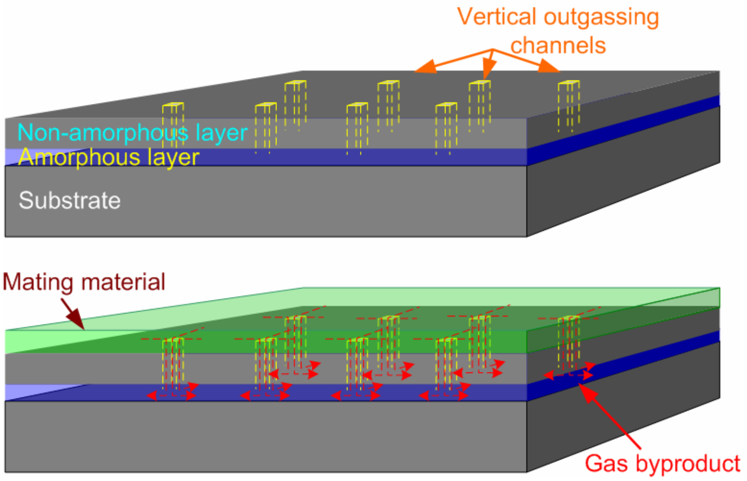

Fig. 1. Schematic of vertical outgassing channel in direct wafer bonding.

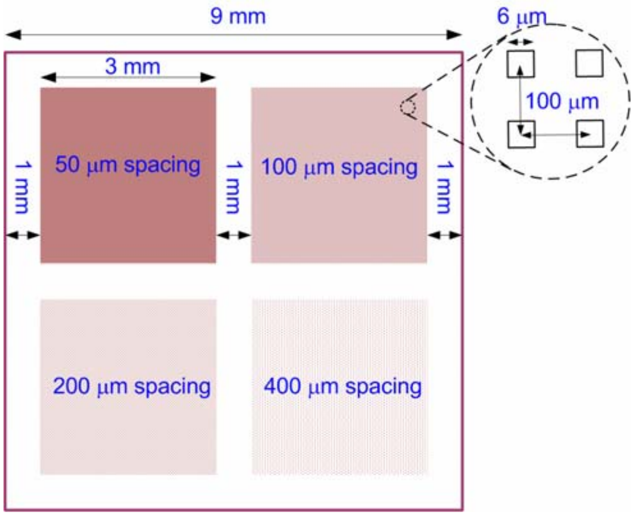

Fig. 2. Mask design for vertical channel spacing (i.e., density) study.

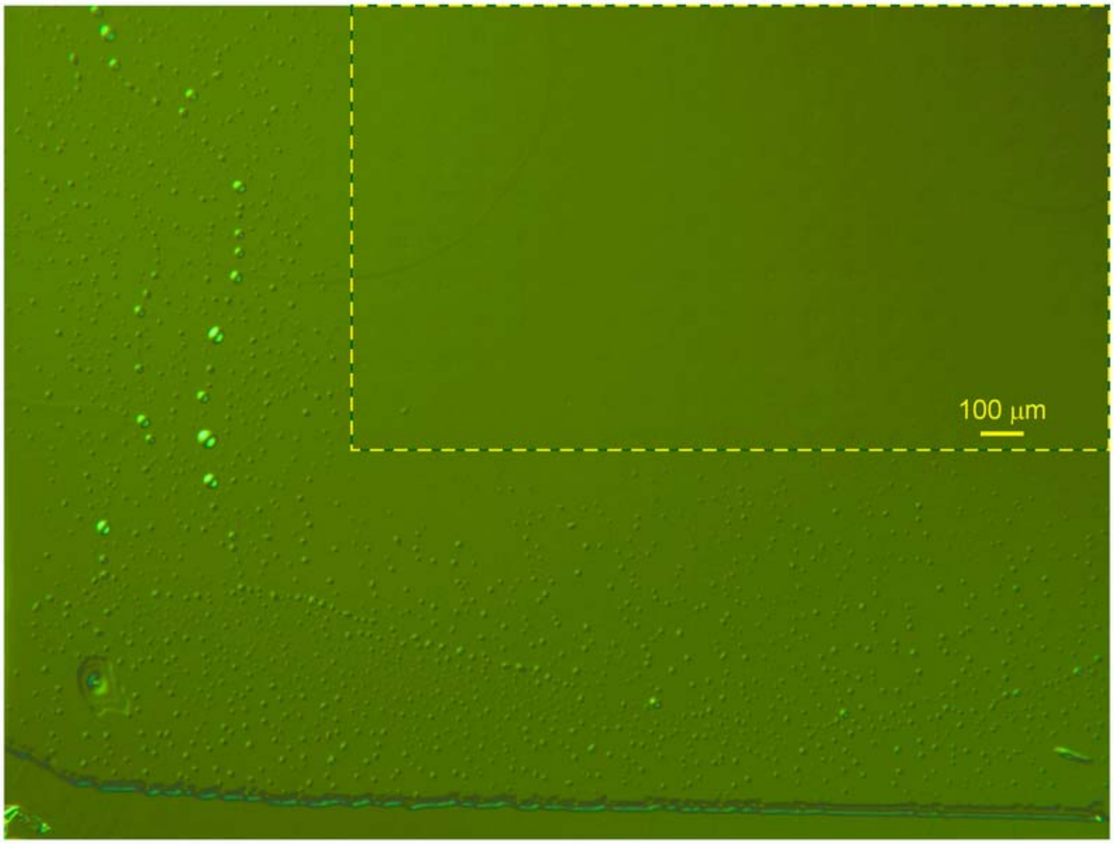

Fig. 3. Nomaski mode microscopic image of a directly bonded 2 μm thick InP epitaxial layer attached on the SOI substrate after selectively removing the InP substrate, showing void-free bonding at highlighted area where vertical outgassing channels with 100 μm spacing locate, while a great number of Interface voids (average density of 9×10^{3} cm^{-2}, up to $1\text{x}10^{6}$ cm^{-2}, diameter 2-20 μm) appear at boundary where no outgassing channels exist.

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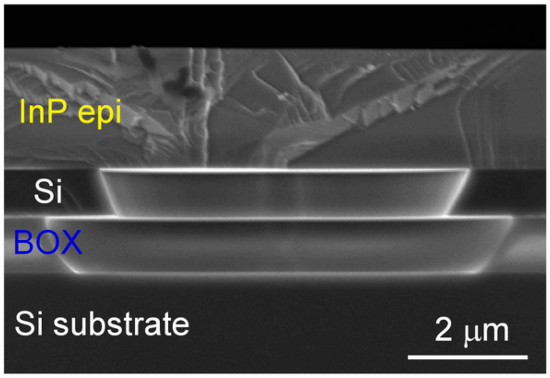

Fig. 4. SEM cross-sectional image of a 6 μm wide vertical outgassing channel with InP epitaxial material directly bonded on the top after 2 hour anneal at 300 °C.

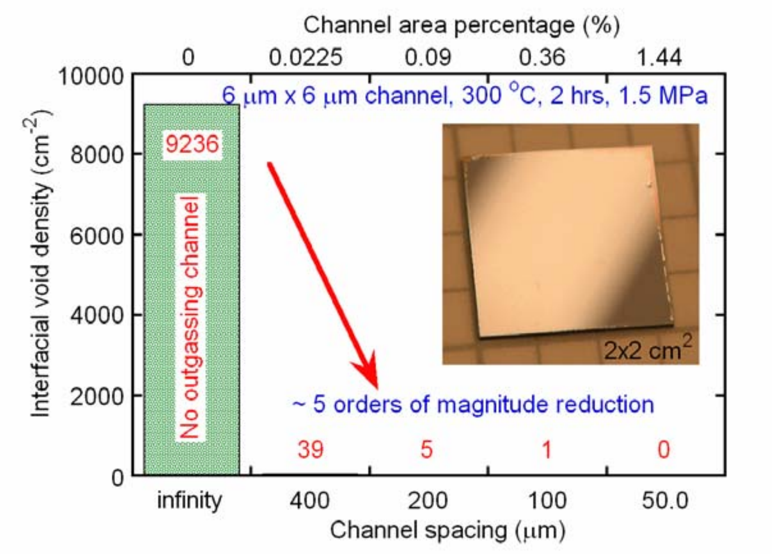

Fig. 5. Interfacial void density vs. channel spacing and channel area percentage for InP epitaxial layer directly bonded on SOI with variable outgassing channel spacing.

Inset: The photograph of a directly bonded 2×2 cm^2 InP epitaxial material on SOI with vertical outgassing channel design, showing mirror-like, void-free epitaxial layer transfer.

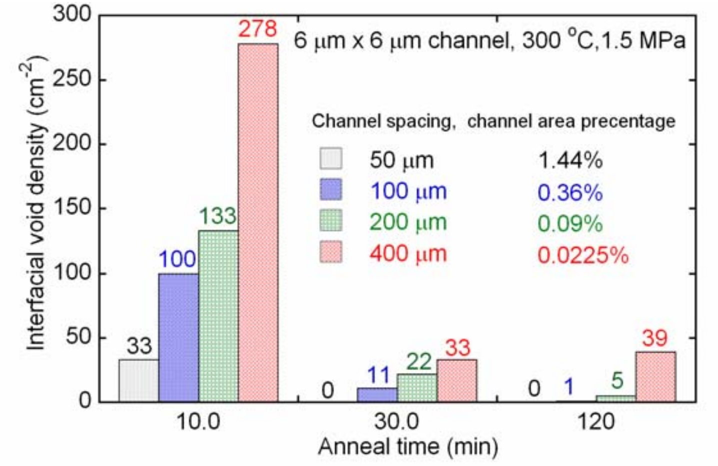

Fig. 6. Interfacial void density vs. anneal time, showing that short anneal is achievable while low void density is still maintained.