Integrated Optical Amplifiers on Silicon Waveguides

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Abstract: Optical amplifiers are important elements of photonic integrated circuits. We present a hybrid silicon evanescent amplifier utilizing a wafer bonded structure of silicon waveguide and AlGaInAs quantum wells. A chip gain of 13 dB with a power penalty of 0.5 dB at 40 Gb/s data amplification is demonstrated.

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1. Introduction

Recent progress in silicon photonics has been motivated by mature silicon processing technology for photonic integrated circuits with low cost and high functionality. Optical amplifiers are key components in realizing high levels of photonic integration as they compensate for optical losses from individual photonic elements. An optically pumped Raman amplifier has been demonstrated [1], but an electrically pumped silicon optical amplifier is yet to be realized, primarily due to the indirect nature of the silicon bandgap. As an alternative approach, a die of III-V based amplifiers can be attached to a silicon passive waveguide circuit, but their gain and noise figure are limited by reflections from interfaces and coupling loss to the silicon waveguide. Recently we demonstrated a silicon evanescent amplifier [2] to address this problem by wafer bonding a high gain layer to a silicon waveguide. The amplifier can be used as a postamplifier integrated with silicon evanescent lasers [3] or used as an integrated preamplifier with silicon evanescent waveguide photodetectors [4]. In the case of preamplification, dynamic characteristics and power penalty are also important for high speed data detection. The device was also characterized with bit error rate (BER) measurements. The results exhibit only 0.5 dB power penalty for data rates up to 40 Gbps [5].

2. Device Structure and Fabrication

The silicon evanescent amplifier is a hybrid structure that consists of an offset multiple quantum well region bonded to a silicon waveguide fabricated on a silicon-on-insulator wafer. Details of the structure are shown in Fig.1a. With this architecture, the optical mode can obtain electrically pumped gain from the III-V region while being guided by the underlying silicon waveguide region.

The silicon strip waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate with a 2 μm thick buried oxide using standard photolithography and Cl2/Ar/HBr-based plasma reactive ion etching. The silicon waveguide was fabricated with a final height of 0.76 μm and width of 2 μm resulting in a mode that exists predominantly in the silicon waveguide. The calculated overlap of the optical mode with the silicon waveguide is 74 % while there is a 3.4 % overlap in the AlGaInAs quantum wells.

The III-V epitaxial structure is grown on an InP substrate. The active layer containing eight quantum wells is bounded by a p-type AlGaInAs SCH layer and n-type InP and InP/InGaAsP superlattice layers to enable current injection. This III-V structure is then transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding with 300 °C annealing temperature. The specific epitaxial structure and bonding process can be found in Ref. 3. The III-V layer containing a p-type layer of InGaAsP is then bonded to the silicon waveguide. After removal of the InP substrate with a mixture of HCl/H2O, 75 μm wide mesas are formed by dry-etching the p-type layers using a CH4/H/Ar-based plasma reactive ion etch. Subsequent wet-etching of the quantum well layers to the n-type layers is then performed to produce the evanescent waveguide.

Fig. 1. (a) Device structure (b) SEM image of fabricated device.
performed using \( \text{H}_3\text{PO}_4/\text{H}_2\text{O}_2 \). Ni/AuGe/Ni/Au alloy contacts are deposited onto the exposed n-type InP layer 38 µm away from the center of the silicon waveguide. 4 µm wide Pd/Ti/Pd/Au p-contacts are then deposited on the center of the mesas. Proton (H\(^+\)) implantation on the two sides of the p-type mesa creates a 4 µm wide current channel and prevents lateral current spreading, ensuring a large overlap between the carriers and the optical mode. Ti/Au probe pads are then deposited on the top of the mesa. To minimize the optical feedback due to facet reflection, the sample is diced orienting the waveguides at an angle of 7° with the normal to the facet plane. After the facets are polished, an antireflection coating of Ta_2O_5 (~5%) is applied to each facet. The final device length is ~ 1.36 mm. A cross-sectional SEM image of the final fabricated hybrid amplifier is shown in Fig. 1b.

3. Experiment and Results

The device, mounted on a temperature controlled stage set to 15 °C, is driven by applying a positive voltage at the p-contact. The device gain is measured by launching and collecting the signal through lensed-fibers at both the input and output facets. The angle between the fiber and the normal to the facet is ~25° to maximize the coupling of output light from the 7° angled waveguide. Coupling efficiency from the device to the fiber is measured to be -5 dB by measuring insertion loss at long wavelengths. Figure 2 shows the measured small-signal fiber-to-fiber gain and, on the second y-axis, the estimated chip gain using 5 dB coupling loss. The maximum fiber-to-fiber gain is 3 dB corresponding to a chip gain of 13 dB at 1575 nm. The inset of the figure represents the net modal gain, \( \Gamma g - \alpha \), where \( \Gamma \) is the QW confinement factor, \( g \) is the material gain, and \( \alpha \) is the waveguide loss. The dotted line of the inset is a data fit using the logarithmic function between the material gain and the current density at the active region. At lower current densities, the gain increases logarithmically while at higher current densities it saturates due to device heating caused by the series resistance (7.5 Ω) and thermal impedance (40 K/W). It is possible to circumvent some of these heating effects by reducing the distance between the n-contact and the active region to 10 µm, and decreasing the buried oxide thickness to 1 µm [3]. With these improvements, we expect to increase the chip gain to more than 20 dB. The maximum gain occurs at 1575 nm with a spectral full-width at half-maximum of 62 nm at 200 mA.

The 3 dB output saturation power from the chip is measured to be 11 dBm as shown in Fig. 3. The evanescent coupling scheme of the device structure typically provides 2 % to 3 % of QW confinement factor, resulting in higher output saturation powers than amplifiers with centered quantum wells whose typical confinement factor is around 5 % to 15 %. Moreover, the tapered or flared waveguide structure demonstrated with III-V amplifiers [6] can also be applied to this device by manipulating the silicon waveguide width without changing the III-V region for better output saturation output power. The noise figure (NF) is measured from the spontaneous emission density at the signal wavelength. The measured NF varies between 13 dB and 10 dB depending on the current level. The internal NF of the device can be between 8 dB and 5 dB considering 5 dB coupling loss.

Figure 3 shows the measured 10 Gbps NRZ eye diagrams with three different input power levels. The measured data agrees well with simulated eye diagrams, which are calculated using the rate equation model for multiple quantum wells. A carrier lifetime is used as a fitting parameter and 1.1 ns of carrier life time yields the best agreement with the measured eye diagrams. The degradation of the Q-factor of the signal can be observed with input power above -4 dBm, which is higher than centered quantum well amplifiers due to the lower optical confinement in the device.
To investigate the dynamic performance of the device, BER measurements are employed at 3 different data rates, 2.5G NRZ, 10G NRZ and 40G RZ. PRBS of $2^{31}-1$ was used to carry out the measurements for 10 Gbps and 40 Gbps, while a shorter sequence of $2^{10}-1$ is chosen for 2.5 Gbps. The average input power is -16 dBm to keep the device unsaturated. A variable optical attenuator (VOA) is inserted between the output of the amplifier and the receiver to adjust the received power. Power penalty of the amplifier is extracted by comparing the BER performances of the transmitter-amplifier-receiver link with the back-to-back transmitter. As shown in Fig.5, a low power penalty of 0.5 dB for all three data rates is achieved. This penalty comes in majority from the amplified spontaneous emission (ASE) of the amplifier, which is not related to the data rate or the pulse duration. To compare the distortion due to the pattern effect, another BER curve with a higher input power of 2 dBm is also plotted in Fig. 5. An additional power penalty of 0.5 dB is required when pattern effect starts to reduce the Q-factor of the signal.

5. Conclusion
We have demonstrated an electrically pumped hybrid silicon evanescent amplifier incorporating AlGaInAs quantum wells with a silicon waveguide. The amplifier combines efficient optical gain from III-V materials with silicon waveguides that control the characteristics of the optical mode. The demonstrated chip gain is 13 dB which can be improved beyond 20 dB with optimization of thermal and electrical properties of the device. The 3 dB output saturation of the device is 11 dBm. The evanescent coupling scheme uses offset quantum wells, which provide lower quantum well confinement factor leading to higher output saturation powers than a conventional semiconductor optical amplifier. The BER measurements show that only 0.5 dB power penalty occurs for data rates up to 40 Gbps. The signal distortion due to pattern effects can be observed for input power of -4 dBm and higher. With further optimization of the optical confinement factor and device length, higher saturation output can be achieved. This amplifier design utilizes a silicon evanescent platform that allows for efficient integration with silicon evanescent lasers, photodetectors and mode converters.

6. References

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