

# Integration of SiON gratings with SOI

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## Abstract

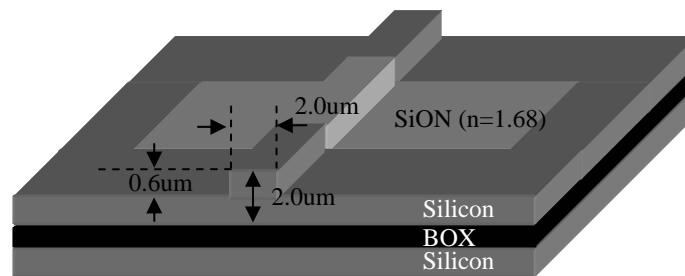
In this paper we discuss integrating silicon oxynitride (SiON) waveguides onto silicon-on-insulator and demonstrate the thermal advantages of a grating fabricated using this technology.

## I. Introduction

Silicon has many material attributes that make it the ideal choice for optical integration: its high refractive index can result in small footprint devices; high thermal conductivity and a relatively large thermo-optic coefficient mean fast and efficient thermally driven devices. While for some applications these attributes are an advantage for others they can cause difficulties: high refractive index may cause high scattering losses, large thermal conductivity means difficulty isolating many devices on a single chip and a large thermo-optic coefficient may cause problems for un-cooled applications. For these reasons we have been investigating the integration of different materials onto a silicon-on-insulator (SOI) platform. SiON was chosen as it is widely used in a CMOS fabrication facility, has a tunable refractive index from 1.44-2.0 ( $\text{SiO}_2\text{-Si}_3\text{N}_4$ ) and has a reduced thermo-optic coefficient  $\sim 8$  times less than silicon thus making it more suitable for un-cooled applications. Being able to define areas of the die which can be composed of different CMOS friendly materials aids in the flexibility and design of placing optical components on a photonic chip while still allowing them to be fabricated on an SOI platform.

## II. Results & Discussion

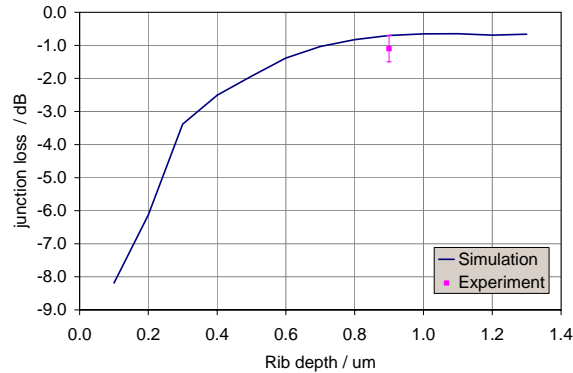
Figure 1 shows a schematic of the hybrid waveguide platform to be fabricated. The process flow to create this type of structure is as follows. The region associated with the SiON is patterned and the silicon on the SOI wafer is etched down to the buried oxide (BOX) using a highly selective plasma etch that uses the BOX as an etch stop layer, SiON is then deposited into the trench and planarized. The rib waveguides for both silicon and SiON are then patterned using the same mask, in two sequential etch steps. This self aligned waveguide patterning process allows different etch depths to be used for the two different material waveguides.



**Figure 1.** Schematic of SiON waveguide integrated onto SOI.

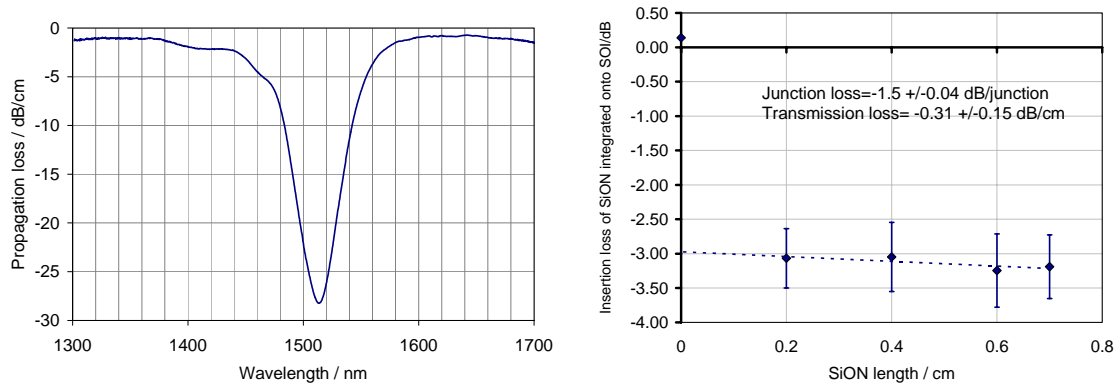
In order to understand the loss of the above structure we split the contributions of loss into two parts; the loss due to the junction between the silicon and SiON and the loss due to propagating in the SiON region. An important contribution to the junction loss is the Fresnel loss at the interface between the two materials, for our process the SiON was deposited using PECVD with an index close to 1.68. Using the beam propagation method to determine the effect index of the two waveguides involved we obtain a reflection of 13% at the interface corresponding to a loss of -0.6dB. Above this there is a loss associated with the modal mismatch at the interface.

Assuming the waveguide width and height is fixed at 2.0um for both waveguides, and the rib etch depth for the silicon waveguide is 0.6um (ensuring single mode operation) the simulated junction loss as a function of etch depth of the SiON waveguide rib is shown in Figure 2a. As can be seen due to the lower confinement of the SiON waveguide its rib etch depth needs to be deeper than the silicon rib ( $\sim 0.8\mu\text{m}$ ) to ensure the junction loss is dominated by Fresnel reflection. By selecting a SiON rib etch depth of 0.9-um we have demonstrated a minimum junction loss of  $-1.1\pm 0.4\text{dB}$  which is close to the limit set by the Fresnel reflectivity.



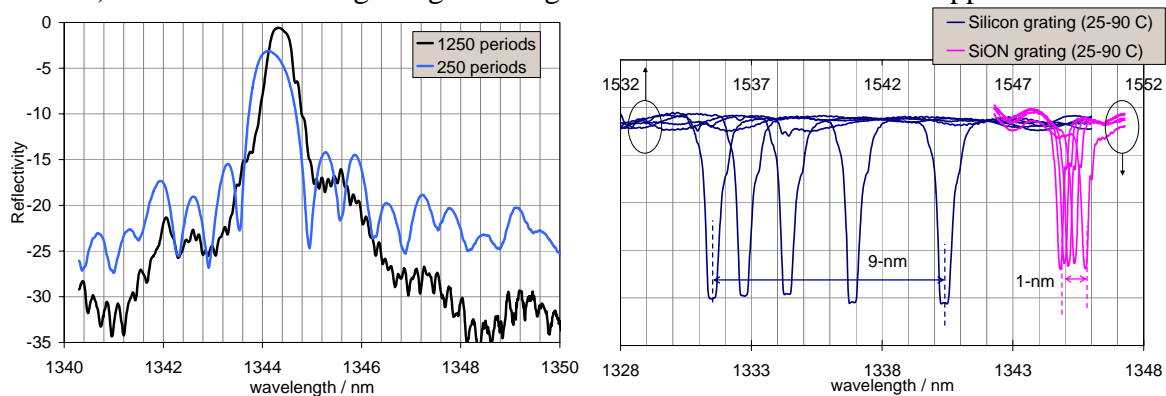
**Figure 2.** Simulated junction loss as a function of SiON rib etch-depth between a SiON and a silicon waveguide with 0.6-um rib etch depth (both waveguides are 2-um wide and 2-um high)

In addition to the loss due to the interface between the two material systems propagation loss in the SiON region has to be minimized to similar levels as a silicon waveguide. The two main contributions to the transmission loss of the SiON waveguide are leakage into the silicon substrate and material absorption. In terms of the leakage into the slab care needs to be taken that the BOX is thick enough to fully confine the light in the waveguide. SOI wafers with 0.35-um BOX are not suitable when working with the lower refractive index of SiON as the leakage loss is too high, in fact to minimize leakage loss when using SiON waveguides with an index of 1.68 BOX thicknesses  $> 1.5\text{-um}$  have to be used. As an example SOI wafers with 1.0um BOX were initially used for this experiment resulting in a SiON propagation loss of  $3.0\pm 1.0\text{dB/cm}$  at a wavelength of 1.31um, when the BOX thickness was increased to 3.0um the SiON propagation loss reduced to  $0.4\pm 0.1\text{dB/cm}$ . Another issue is the absorption of as deposited SiON around 1550-nm [1]. Figure 3a shows the propagation loss of an un-annealed SiON waveguide around 1550-nm. As can be seen there is an absorption resonance around 1515-nm which can be attributed to the first overtone of the N-H stretching vibration. To decrease this loss the SiON needs to be annealed to remove hydrogen from the lattice. The loss of un-annealed SiON waveguide integrated onto SOI has been measured at 1310-nm and a cut-back measurement is shown in Figure 3b. This displays a junction loss of  $1.5\pm 0.04\text{ -dB}$  and a transmission loss of  $0.3\pm 0.15\text{-dB/cm}$ .



**Figure 3.** a) Measured propagation loss for an un-annealed SiON waveguide as a function of wavelength; b) Cut-back measurement for a SiON waveguide integrated onto SOI at a wavelength of 1.31 $\mu$ m.

Finally as an example of device level integration we demonstrate a SiON grating integrated onto an SOI wafer. Here the gratings are patterned on top of the SiON waveguide by etching to a depth of 0.7 $\mu$ m. To control the strength of the grating the etched SiON ( $n=1.68$ ) was then filled with SiON of index 1.69 before planarisation and rib etch as described above. The reflection spectrum of a 3.28- $\mu$ m period grating is shown in Figure 4a. The peak reflectivity is 90% and the 3-dB bandwidth is 0.5-nm at 1344.4nm for a 1250 period grating, oscillations are seen as the gratings are not apodized. To demonstration the diversity using different materials brings we show the difference between the thermal behavior of two sets of gratings: one fabricated from silicon (designed for 1537-nm), see ref [2] and the other fabricated in SiON (designed for 1345-nm) both sets of gratings being fabricated on an SOI wafer. As the temperature is varied from 25-90C the SiON grating shows  $\sim 8x$  lower thermal sensitivity (due to its lower thermo-optic coefficient) than silicon based gratings making it more useful for un-cooled applications.



**Figure 4.** a) Measured reflection spectra for a SiON grating integrated onto SOI; b) Thermal shift of the reflection spectra of two gratings integrated onto SOI one made of silicon and one SiON.

### III. Conclusion

In this paper we demonstrate the feasibility of integrating SiON waveguides with silicon waveguide on SOI. We demonstrate the advantages using different materials gives by comparing the thermal performance of silicon and SiON gratings fabricated on SOI.

<sup>1</sup> G.-L. Bona, R. Germann and B. J. Offrein, "SiON high-refractive-index waveguide and planar lightwave circuits" IBM J. Res. & Dev. 47 (28) 239-249 (2003)

<sup>2</sup> Liao, Ansheng Liu, Song Pang and Mario Paniccia, "Tunable Bragg grating filters in SOI waveguide" OSA Integrated Photonics Research, San Francisco, CA, USA (2004).