J Mater Sci: Mater Electron
DOI 10.1007/s10854-007-9418-y

Hybrid silicon integration

R. Jones · H. D. Park · A. W. Fang · J. E. Bowers · O. Cohen · O. Raday · M. J. Paniccia

Received: 20 July 2007 / Accepted: 19 September 2007
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Abstract An overview is presented of the hybrid AlGaInAs-silicon platform that enables wafer level integration of III-V optoelectronic devices with silicon photonic devices based on silicon-on-insulator (SOI). Wafer bonding AlGaInAs quantum wells to an SOI wafer allows large scale hybrid integration without any critical alignment steps. Discrete hybrid silicon optical amplifiers, lasers and photodetectors are described, and the integration of a ring laser with on-chip and photo-detector and amplified spontaneous emission (ASE) seed to enable unidirectional lasing.

1 Introduction

Silicon photonics has the potential to provide highly integrated, low-cost, optical components using the same CMOS-based manufacturing techniques that revolutionized the micro-electronics industry. This is important as lowering the cost of optical interconnects would enable high-bandwidth optical communication links in and around personal computers and servers where their cost today is prohibitively expensive. Silicon has many properties that make it ideal as a material for integrated optics. Silicon's band edge at 1.1 μm makes it compatible with long wavelength infra-red communication links, its high refractive index contrast with its native oxide ($\Delta n \sim 2$) enables small-footprint integrated optical devices, and of course high volume manufacturing techniques can be used to fabricate silicon photonic chips at low cost [1, 2].

Both passive and active photonic devices have been demonstrated built on silicon-on-insulator (SOI) substrates such as WDM splitters for fiber to the home applications [3] and high speed optical modulators [4]. As silicon is transparent above 1.1 μm it cannot be used as a photodetector in the 1.31 μm and 1.55 μm communication windows but other CMOS compatible group IV materials have been suggested for this role, e.g. germanium [5]. The key issue for material compatibility is the ability to process devices on the same SOI wafer as other silicon components simultaneously across the wafer. In fact all the devices needed for an optical link can be fabricated from silicon or compatible materials apart from the laser. Due to silicon's indirect band gap light emission is very inefficient [2] and currently the preferred method of integrating lasers with silicon chips is to align and then attach individual prefabricated lasers to silicon waveguides one at a time. This has the key drawback that the assembly time increases as the required number of lasers increases. Consider, for example, a typical 6-inch SOI wafer containing 44 silicon die each requiring eight lasers, individually attaching 352 lasers to each wafer is clearly not a time- or cost-efficient solution. A better approach would be to use the same wafer-scale fabrication techniques to manufacture both the silicon photonic components and the laser. That is the aim of the hybrid laser work discussed here.

R. Jones (✉) · M. J. Paniccia
Intel Corporation, 2200 Mission College Blvd, SC12-326, Santa Clara, CA 95054, USA
e-mail: Richard.jones@intel.com

H. D. Park · A. W. Fang · J. E. Bowers
Department of Electrical and Computer Engineering, University of California, Santa Barbara, Santa Barbara, CA 93106, USA

O. Cohen · O. Raday
Intel Corporation, S.B.I. Park Har Hotzvim, Jerusalem 91031, Israel

2 Hybrid silicon device architecture

The hybrid-silicon platform allows silicon photonic devices to be integrated with active optoelectronic devices more commonly associated with III–V materials such as: electrically pumped lasers; amplifiers; wavelength converters; and photo-detectors.

A typical device cross-section is shown in Fig. 1, with the SOI and III–V regions labeled on the left-hand side of the schematic. An unprocessed III–V wafer is first bonded to a silicon wafer patterned with optical waveguides, followed by the III–V processing using standard planar-fabrication techniques. Because bonding is done before laser fabrication, there is no alignment needed between the un-patterned III–V wafer and the patterned silicon wafer. Wafer bonding the two material systems addresses the difficulties of lattice mismatch that occur when trying to grow III–V materials directly onto silicon. The low-temperature bonding allows for the different thermal expansion coefficients of the two materials, and eliminates any pronounced stress in the final bonded system. Bonding may be done at the wafer, partial-wafer or die-level, depending on the exact application and economics of the device being fabricated.

The vertical refractive index profile of the hybrid waveguide is shown in Fig. 2a along with a cross-section of the mode profile. Strong coupling occurs between the silicon waveguide and the active region due to their similar refractive indices resulting in the formation of a hybrid mode which strongly overlaps both the silicon waveguide and the quantum wells in the III–V material. The overlap of the optical mode with the quantum well active region is a key device parameter as it dictates the modal gain for lasers and amplifiers, and the responsivity for hybrid photo-detectors.

The epitaxial structure of the InP wafer is shown in Table 1. The eight quantum well active region is bounded by the n-layers and the separate confinement heterostructure region. The SCH layer allows for an increase in the overlap of the quantum well region with the optical mode. The superlattice region is used to inhibit the propagation of defects from the bonded layer into the quantum well region [6].

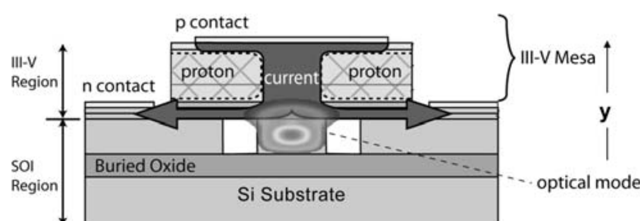

Fig. 1 Schematic cross-section of the hybrid silicon laser

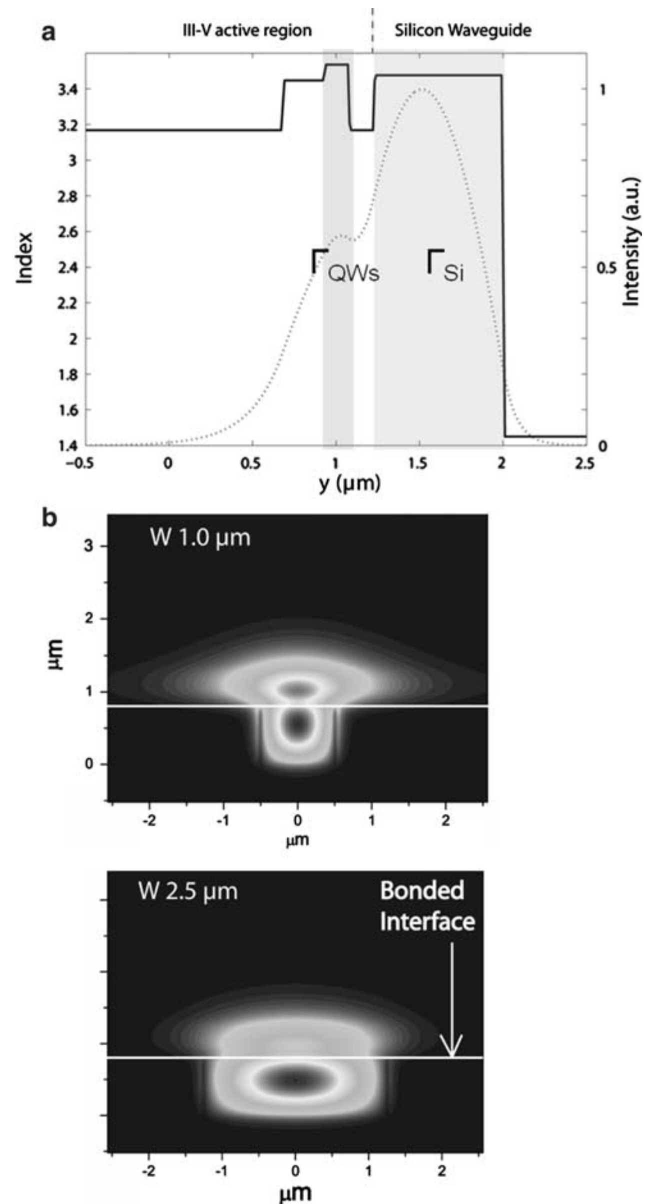

Fig. 2 (**a**) Vertical refractive index profile of hybrid silicon waveguide and mode profile; (**b**) 2D mode profiles of hybrid silicon waveguide with width 1.0 μm and 2.5 μm

Figure 3 plots the confinement factor of the optical mode in both the silicon and the quantum well portion of the hybrid waveguide as a function of the silicon waveguide width, for a silicon waveguide height of 0.76 μm. Decreasing the silicon waveguide width pushes the mode up into the quantum well region providing higher modal gain. Counteracting this benefit is the reduction of the silicon confinement factor which reduces the amount of coupling from the hybrid waveguide to passive, silicon only, waveguides on the same chip. The control of the quantum well confinement factor with lithographically defined waveguide width is a novel and flexible way to alter device performance across the photonic chip.

Table 1 Epitaxial structure of InP wafer

Name	Composition	Doping Concentration	Thickness
P contact layer	P-type $In_{0.53}$ $Ga_{0.47}$ As	1×10^{19} cm^{-3}	0.1 μm
Cladding	P-type lnP	1×10^{18} cm^{-3}	1.5 μm
Separate Confinement Heterostructure	P-type $Al_{0.131}Ga_{0.34}As$,1.3 μm	1×10^{17} cm^{-3}	0.25 μm
Quantum wells	$Al_{0.089}Ga_{0.461}In_{0.45}As$, 1.3 μm (9x)	Undoped	10 nm
	$Al_{0.055}Ga_{0.292}In_{0.653}As$, 1.7 μm (8x)	Undoped	7 nm
N layer	N-type lnP	1×10^{18} cm^{-3}	110 nm
Supper lattice	N-type $In_{0.85}Ga_{0.15}In_{0.653}As_{0.327}P_{0.673}$ (2x)	1×10^{18} cm^{-3}	7.5 nm
	N-type lnP(2x)	1×10^{18} cm^{-3}	7.5 nm
N bonding layer	N-type lnP	1×10^{18} cm^{-3}	10 nm

3 Device fabrication

Fabry–Perot lasers at 1326 nm [7] and 1577 nm [8] have been fabricated using this hybrid waveguide architecture as well as optical amplifiers [9], photodetectors [10] and ring lasers [11]. The generic device process flow is as follows.

First waveguides are patterned on the (100) surface of an undoped SOI substrate with a 1 μm thick buried oxide layer using standard projection photolithography and Cl_2/Ar/HBr- based plasma reactive ion etching. These waveguides may include passive components such as optical (de)multiplexers, or ring resonators or simply straight waveguides used to demonstrate Fabry–Perot lasers.

Next the InP wafer and the SOI wafer undergo a rigorous surface clean, oxygen plasma surface treatment, and wash in deionised water prior to bonding. During the plasma treatment a thin hydrophilic (<5 nm) oxide layer is grown on the surface of each wafer which is then terminated by highly reactive polar hydroxyl groups during the deionised water dip. When the two wafers are subsequently placed together the hydroxyl groups form bridging bonds between the two surfaces resulting in weak spontaneous bonding of the two wafers. To enhance the strength of this spontaneous bond the wafer are then placed in an annealing chamber at 300 °C at a pressure of 2 MPa for 12 h. This slow bake helps out diffusion of interface trapped molecules and activates the formation of stronger covalent bonds, resulting in stronger bonding of the two materials. After bonding the InP is patterned into mesa's; the N- and P-metals are deposited followed by proton implantation of the mesa to form a conductive channel in the center of the mesa through which current can flow. A typical hybrid silicon active cross-section is shown in Fig 1. More details of device fabrication are given in [7–11].

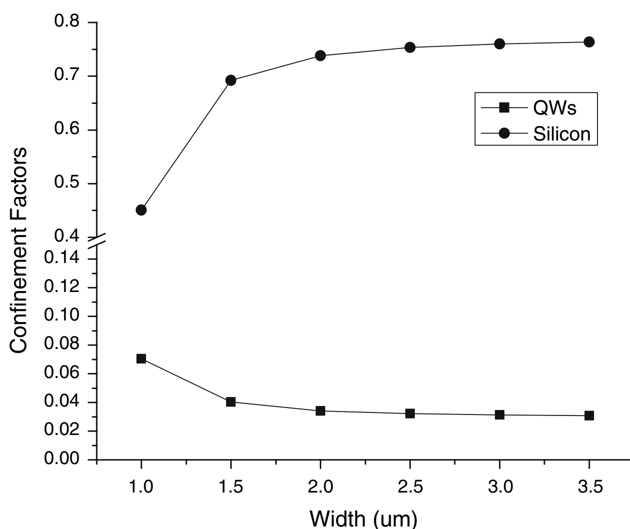

Fig. 3 Confinement factor of mode with quantum well and silicon region as a function of silicon waveguide width

3.1 Hybrid silicon amplifiers

A good example of the use of this novel platform is in the fabrication of an optical amplifier [9]. Currently the only silicon based amplifier has been demonstrated using the Raman Amplification [12]. Integration of InP quantum wells with the silicon waveguide allows electrically pumped gain compatible with silicon photonics. A SEM cross-section of the amplifier is shown in Fig. 4. The silicon strip waveguide height is 0.76 μm and its width is 2 μm. The total amplifier length is 1.36 mm long. For these waveguide dimensions the overlap of the optical mode with the quantum wells is 3.4%.

Devices were characterized by angle polishing (7°) and AR-coating the facets and coupling the light into and out of the amplifier with lensed single mode fiber, with a measured coupling loss of –5 dB. The amplifier gain as a function of bias current is shown in Fig. 5a. The maximum fiber-fiber gain for TE polarized light is 3 dB corresponding to an on-chip gain of 13 dB at a wavelength of 1575 nm. Due to the compressive strain on the quantum

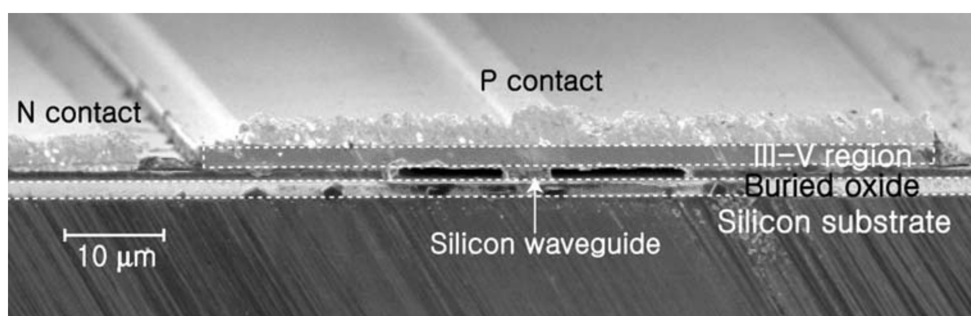

Fig. 4 SEM cross-section of hybrid silicon optical amplifier

wells these devices work predominantly on TE polarization with only 1 dB on-chip gain for TM polarization. Fig. 5b shows the on-chip gain as a function of chip output power, the 3 dB output saturation power is 11dBm which is higher than centered quantum well optical amplifiers due to the reduced mode overlap with the off-center, evanescently-coupled, quantum wells.

3.2 Hybrid silicon lasers

Of course demonstrating net gain allows one to fabricate a laser. Both Fabry–Perot and ring lasers have demonstrated using this hybrid platform, at both 1326 nm and 1577 nm wavelength. 1577 nm Fabry–Perot lasers have been fabricated from hybrid waveguides polished to a length of 850 μm [7, 8]. Again coupling from the laser was done using lensed fiber with a coupling loss of 6 dB to the hybrid waveguides with silicon dimensions of 2.5 μm, 0.76 μm and for the silicon strip waveguide width and height. The mode overlap with the silicon waveguide and quantum wells is calculated to be 75% and 3% respectively. The hybrid waveguide facets were polished to give ~30% reflectivity end mirrors.

The L–I curves for the light coupling to the single mode optical fiber is shown in Fig. 6. The laser threshold is 65 mA at a temperature of 15 °C. The laser emits light up to a temperature of 40 °C and taking into account the 6 dB coupling loss and that light is only collected from one side of the laser the total maximum power emitted is 14 mW corresponding to a differential efficiency of 12.7%.

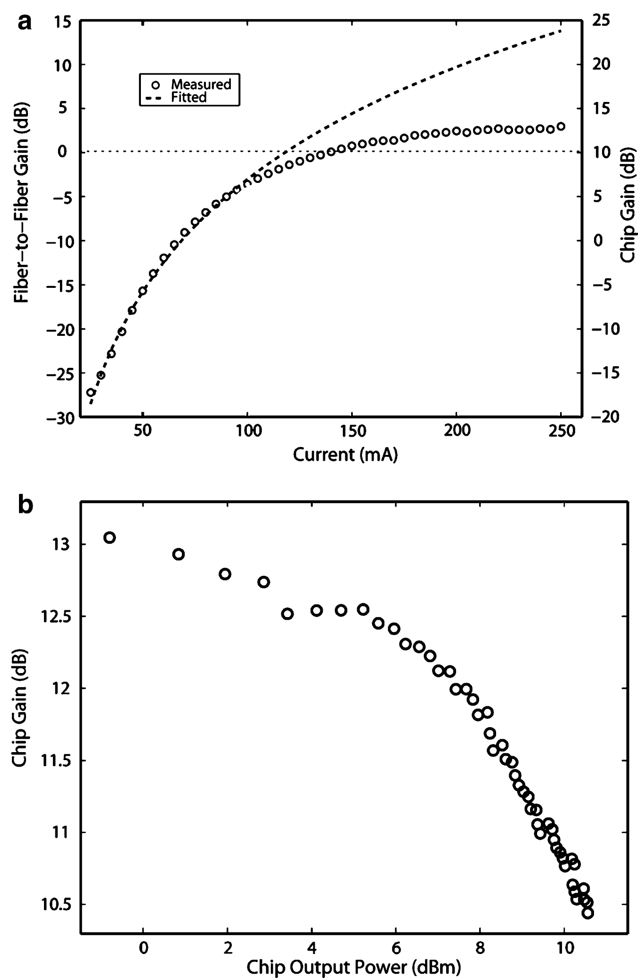

Fig. 5 (**a**) Hybrid silicon amplifier gain versus bias current and (**b**) gain versus output power

3.3 Hybrid silicon photodetectors

The same basic device architecture that is used to fabricate lasers can also be used to fabricate hybrid silicon photodetectors when the quantum wells are operated under reverse bias [10]. The device schematic and SEM are shown in Fig. 7a and b. The 400 μm long hybrid photo-detector is coupled to a 100 μm long passive silicon waveguide. The mesa at the interface is angled at 7° to reduce the reflection at the passive/active device junction. The silicon rib waveguide dimensions are 0.5 μm, 0.69 μm and 0.19 μm for the width, waveguide height and slab height. The mode overlap with the silicon waveguide and quantum wells is calculated to be 74% and 3.4% respectively.

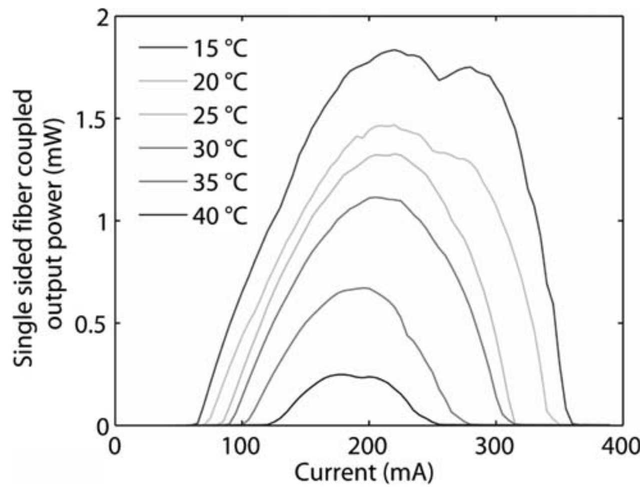

Fig. 6 L–I curve for hybrid silicon laser

The responsivity of the detector was measured by coupling TE light into the silicon waveguide. Figure 8 shows the photodetector's external responsivity as a function of wavelength. Taking into account the –5.5 dB coupling loss into the detector the device has a relatively flat responsivity of 1.13 A/W from 1500–1600 nm at 3.0 V, this corresponds to an internal quantum efficiency of ~90%. Again due to the compressive strain in the quantum wells TM responsivity is much lower and measured at 0.23 A/W. The frequency response of the detector was measured using a network analyzer to be 470 MHz. Currently this is limited by the large capacitance of the long device and can be scaled up to 10 GHz with a responsivity of 60% by reducing the device length and width.

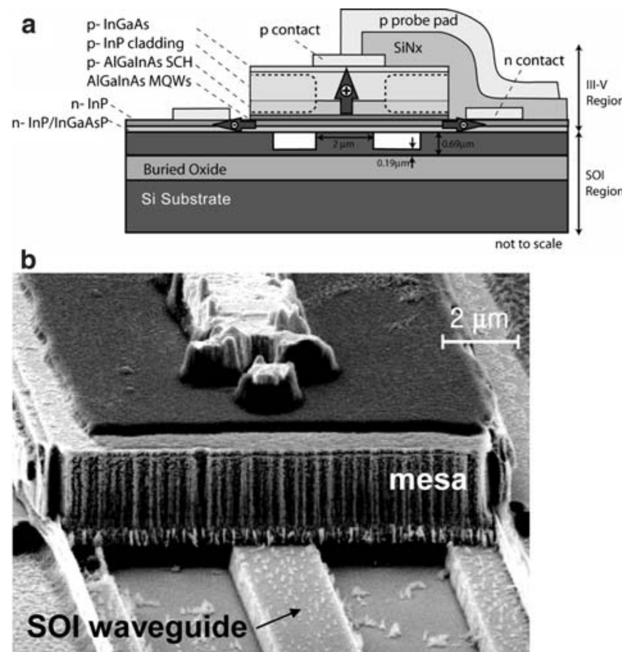

Fig. 7 (**a**) Schematic and (**b**) cross-section SEM of hybrid silicon photo-detector

3.4 Integrated hybrid silicon chip

In general ring lasers suffer from bi-directional lasing, that is lasing occurs in the clockwise and anti-clockwise direction in the ring [13]. Coupling between the degenerate clockwise and anti-clockwise modes results in instability and kinks in the L–I curve of the single sided laser output, see for example the dotted grey curve in Fig. 10. One way to force unidirectional lasing is to seed the cavity in the preferred direction with an external light source. Here we integrate an ASE seed with the ring laser to obtain unidirectional lasing and an on-chip power monitor to ease device testing using the hybrid silicon platform.

The ring laser is fabricated with silicon waveguide of width, height, and slab height of 1.65, 0.69 and 0.19 μm respectively. The calculated overlap of the optical mode with the silicon waveguides is 64% while there is a 4.2% overlap in the quantum wells. The radius of curvature of the ring resonator is 100 μm, and the evanescent couplers are fabricating of two 100 μm long waveguides placed 0.6 μm apart. This coupler corresponds to 85% of light being fed back into the ring. The ASE source and power monitor were both fabricated from a straight hybrid waveguide with a 400 μm length. Reverse biasing a section resulted in it being a photo-detector, forward biasing it allowed it to emit spontaneous radiation and act as an ASE source. A schematic and top-down SEM of the integrated circuit is shown in Fig. 9.

The responsivity of the photodetectors was measured by dicing and polishing a discrete detector in the same chip and launching laser light into the detector through a lensed fiber. The fiber coupled responsivity was measured to be

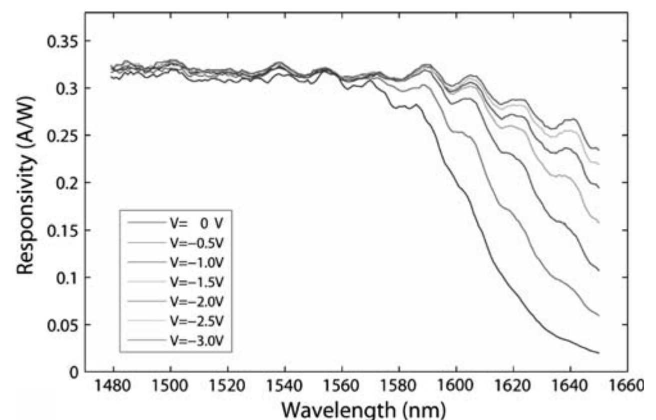

Fig. 8 Responsivity as a function of wavelength for bias voltages between 0 and 3.0V

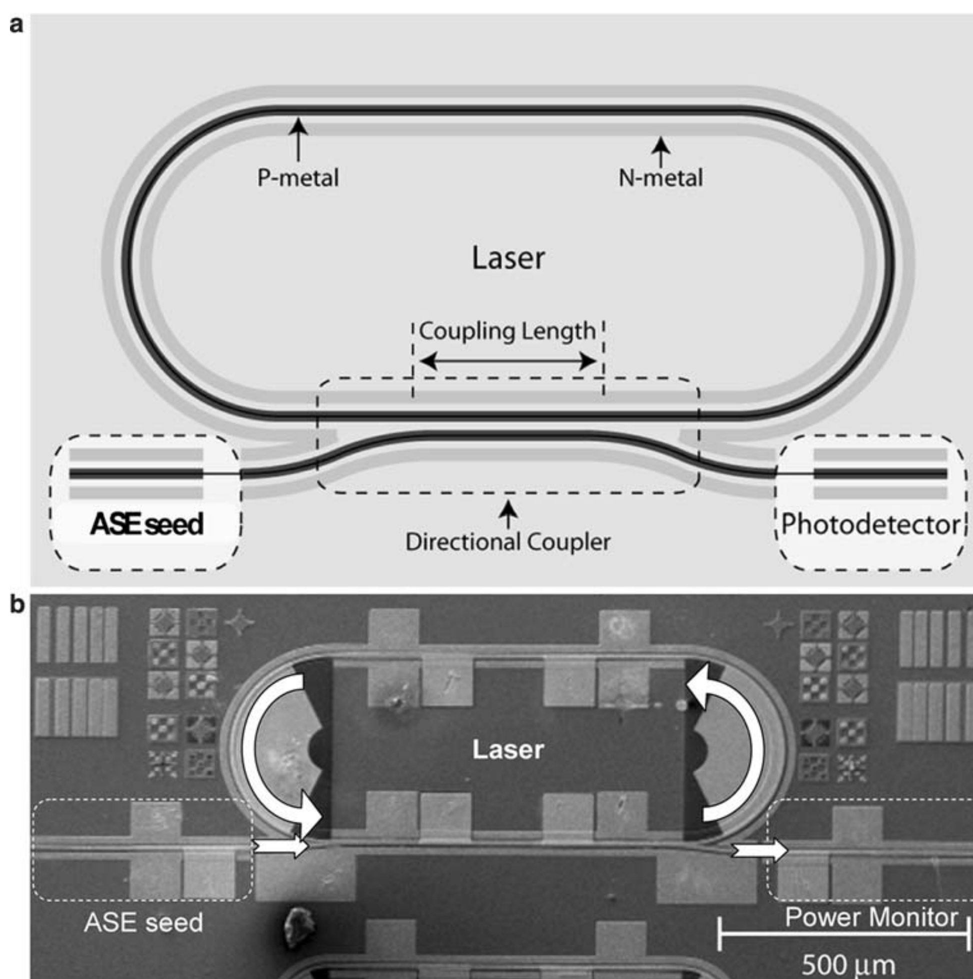

Fig. 9 (**a**) Schematic and (**b**) top down SEM of ring laser integrated with ASE seed and power monitor

0.25 A/W at 1580 nm. Taking into consideration the ~30% reflection off the waveguide facet and an estimated 5.25 ± .25 dB coupling loss, we estimate the photodetector responsivity to be in the range of 1.25–1.11 A/W. This corresponds to a quantum efficiency between 97–86%. We use a responsivity of 1.25 A/W in the remainder of this section such that the laser power values are on the conservative side. The detector dark current was measured to be 200 μA.

Figure 10 shows the LI curve for the ring laser with different biases being applied to the ASE seed. With no seed bias the ring laser output is very erratic due to mode hopping as the laser output switches between clockwise and anticlockwise lasing as the laser bias is varied. At 75 mA forward detector current, this LI becomes smoother, and at 100 mA, the anticlockwise propagating mode achieves stable unidirectional lasing. The laser runs continuous mode with a maximum output power of the ring laser is 2 mW, with a threshold of 150 mA.

Figure 11 shows the measured multi-mode lasing spectrum of the laser driven at 240 mA. The lasing wavelength is 1592.5 nm with a 0.21 nm mode spacing corresponding to a group index of 3.67.

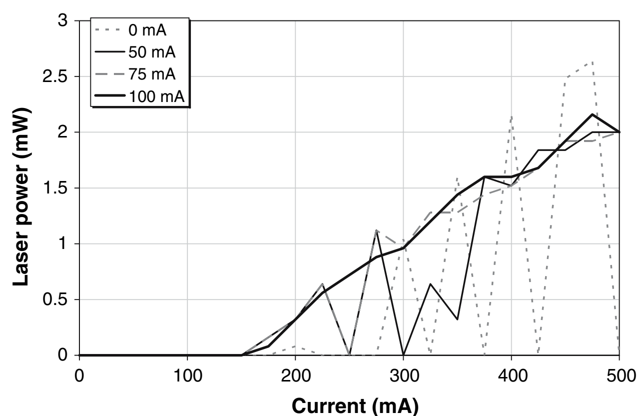

Fig. 10 L–I curve for ring laser as for 0; 50; 75 and 100 mA bias on ASE seed.

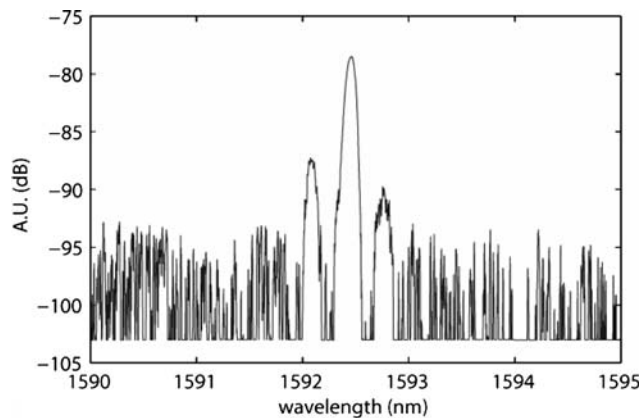

Fig. 11 Lasing spectrum of ring laser

4 Wafer level processing

The experiments run so far have been fabricated using die to die bonding of 8×8 mm^2 InP die. To scale this processing up to whole SOI wafer level there are two basic approaches to consider:

(1) Wafer to wafer bonding: here bonding would be done using whole InP wafers, which has the advantage that the surface treatment and bonding is done on a complete III–V wafer easing the handling. Disadvantages include the disparity between commercially available SOI and InP wafers. 12-inch SOI wafers are readily available whereas InP wafers are only now becoming available at 6-inch size, although at high cost. Obviously this disparity in size of the available wafers reduces the attractiveness of this approach as it does not allow the full usage, and hence economics of the large SOI wafers.

(2) Given that a significant amount of the III–V wafer will be etched away during device fabrication a better approach might be bonding multiple III–V die to an SOI wafer. This has the key advantage that scaling can be done to any SOI wafer size irrespective of the III–V wafer availability, and the III–V die size can be set to efficiently use the InP material. All this comes at the cost of processing complexity, as every die needs to undergo its own surface treatment before bonding, followed by rough alignment of the die to SOI wafer. However, in general the economic advantages of being able to buy smaller III–V wafers to process large SOI wafers makes this approach more attractive.

5 Conclusion

The hybrid silicon platform is described which can be used to integrated III–V optoelectronic components with silicon photonics. The novelty of this approach lies in the wafer scale fabrication it opens up for lasers and other active devices on a silicon platform. Amplifiers with 13 dB on-chip gain, photo-detectors with 90% quantum efficiency and lasers with output powers of 14 mW are described. As proof of the integration potential of this platform a unidirectional laser is presented by integrating an ASE seed with a ring laser and on-chip power monitor. This wafer scale approach to integration of active components onto silicon will enable optical interconnects around PC's and servers where their current price is too expensive.

Acknowledgements This work was supported by DARPA through contracts W911NF-05-1-0175 and W911NF-04-9-0001, and by Intel. The authors thank Jag Shah, Mike Haney, Matt Sysak, Ying-Hao Kuo, Di Liang, Brian Koch and Emily Burmeister for useful discussions and K. Callegari and G. Zeng for sample preparation.

References

1. G.T. Reed, A.P. Knights, *Silicon Photonics: An Introduction* (John Wiley, Chichester, West Sussex, 2004)
2. L. Pavesi, D.J. Lockwood (eds.), *Silicon Photonics* (Springer-Verlag, Berlin, 2004)
3. S. Bidnyk, D. Feng, A. Balakrishnam, M. Pearson, M. Gao, H. Liang, W. Qian, C.-C. Kung, J. Fong, J. Yin, M. Ashgari, Phot. Tech. Lett. **18**(22), 2392–2394 (2006)
4. A. Liu, L. Liao, D. Rubin, H. Nguyen, B. Ciftcioglu, Y. Chetrit, N. Izhaky, M. Paniccia, Opt. Express **15**, 660–668 (2007)
5. M. Morse, O. Dosunmu, G. Sarid, Y. Chetrit, Phot. Tech. Lett. **18**(23), 2442–2444 (2006)
6. A. Karim, K.A. Black, P. Abraham, D. Lofgreen, Y.J. Chiu, J. Piprek, J.E. Bowers, Phot. Tech. Lett. **12**(11), 1438–1440 (2000)
7. H-H Chang, A.W. Fang, M.N. Sysak, H. Park, R. Jones, O. Cohen, O. Raday, M.J. Paniccia, J.E. Bowers, 1310 nm silicon evanescent laser, submitted for publication
8. A.W. Fang, H. Park, O. Cohen, R. Jones, M.J. Paniccia, J.E. Bowers, Opt. Express **14**, 9203–9210 (2006)
9. H. Park, A.W. Fang, O. Cohen, R. Jones, M.J. Paniccia, J.E. Bowers, Phot. Tech. Lett. **19**(4), 230–232 (2007)
10. H. Park, A.W. Fang, R. Jones, O. Cohen, O. Raday, M.N. Sysak, M.J. Paniccia, J.E. Bowers, Opt. Express. **15**(10), 6044–6052 (2007)
11. A.W. Fang, R. Jones, H. Park, O. Cohen, O. Raday, M.J. Paniccia, J.E. Bowers, Opt. Express **15**(5), 2315–2322 (2007)
12. R. Jones, H. Rong, A. Liu, A. Fang, M. Paniccia, D. Hak, O. Cohen, Opt. Express **13**, 519–525 (2005)
13. J.P. Hohimer, G.A. Vawter, Appl. Phys. Lett. **63**(18), 2457–2459 (1993)