

Low Temperature, Large Wafer-Scale InP-to-Si Direct Bonding with Vertical Outgassing Channels for Silicon Photonic Integrated Circuits

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Abstract

Advances in microelectronics are often motivated by the need for increasing circuit complexity and chip functionality while attaining lower manufacturing cost. Wafer-scale processing of Si-based photonics is already attainable on passive devices, but progress in active components for photonic integrated circuits (PICs) through compound semiconductors-Si integration is normally reported on individual chips of small scale. The hybrid Si evanescent platform has been used to demonstrate a wide range of devices including linear and ring cavity lasers, optically preamplified receivers and integrated mode locked lasers. This platform for PICs uses wafer bonding of a III-V compound semiconductor to the silicon-on-insulator (SOI) substrate. The transfer size of the InP epitaxial layers to the SOI substrate is the limiting factor in scaling this device platform to wafer-level, CMOS compatible processing for mass production.

In this paper, a robust, wafer scale-independent InP-to-SOI direct wafer bonding method is demonstrated by employing vertical outgassing channels. Due to the inherent polymerization reactions in converting surface Hydroxyl (-OH) groups to strong covalent Si-to-In (or -P) bonds, gas byproducts of H₂O and H₂ need to be removed out of the bonding interface in an efficient fashion. Uniform interfacial void distribution $>55,000 /\text{cm}^2$ (2~20 μm in diameter) is observed on a bonded pair at 300 °C when no any sort of outgassing approach is utilized, resulting in the fundamental obstacle for high device yield and large production volume. By etching an array of through-holes (called vertical outgassing channels (VOCs) in this work) on the Si device layer down to the buried oxide (BOX) layer of the SOI substrate, gas byproducts are found to be able to migrate to the VOCs and be absorbed by the BOX efficiently. Open network and high gas permeability of SiO₂ contribute to the high outgassing efficiency. With the best VOC scheme of 8 μm square channel size and 50 μm center to center spacing, void-free bonding interface is achieved, resulting in more than 5 orders of magnitude reduction in interfacial void density. An important result allowing greater throughput is that the anneal time can be reduced to 30 min, which is a 100X anneal time reduction.

Experimental finding shows that interfacial void density increases with the increasing of VOC spacing, indicating an effective coverage per VOC. It also forms the foundation to apply this approach to any SOI-based wafer bonding regardless of wafer size, as long as the effective coverage overlaps, eliminating the outgassing “dead zone”. We have achieved good bonding of 50, 75 and 100 mm InP-to-SOI direct wafer bonding with same bonding quality in term of interfacial voids and bonding strength, even after substrate removal leaving epitaxial films on the order of 2 μm thick. An X-ray reciprocal map measurement on a 1 cm^2 bonded pair shows no strain occurrence at III-V active region. Thermal expansion mismatch-induced strain is likely to concentrate at VOC sites only, resulting in strain-free bonding in the rest of area. X-ray rocking curve measurement at different locations of the 100 mm In-to-SOI bonding shows consistent strong InP and Si peaks with small FWHM values. Device results using VOC bonding will be reported.

Keywords: wafer bonding, photonic integrated circuits, silicon-on-insulator.