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Low-Temperature, Strong SiO_2-SiO_2 Covalent Wafer Bonding for III–V Compound Semiconductors-to-Silicon Photonic Integrated Circuits

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We report a low-temperature process for covalent bonding of thermal SiO_2 to plasma-enhanced chemical vapor deposited (PECVD) SiO_2 for Si-compound semiconductor integration. A record-thin interfacial oxide layer of 60 nm demonstrates sufficient capability for gas byproduct diffusion and absorption, leading to a high surface energy of 2.65 J/m^2 after a 2-h 300°C anneal. O_2 plasma treatment and surface chemistry optimization in dilute hydrofluoric (HF) solution and NH_4OH vapor efficiently suppress the small-size interfacial void density down to 2 voids/cm^2, dramatically increasing the wafer-bonded device yield. Bonding-induced strain, as determined by x-ray diffraction measurements, is negligible. The demonstration of a 50 mm InP epitaxial layer transferred to a silicon-on-insulator (SOI) substrate shows the promise of the method for wafer-scale applications.

Key words: Wafer bonding, hybrid integration, compound semiconductors, silicon-on-insulator, photonic integrated circuits

INTRODUCTION

Wafer bonding is an increasingly popular approach for a variety of heterogeneous material system integration and microelectromechanical system (MEMS) applications.[1,2] The number of threading dislocations and misfits at the bonding interface is much smaller than for InP-based heteroepitaxial growth,[3,4] resulting in high-performance electronic and optoelectronic devices.[5–9] High-quality wafer-bonded silicon-on-insulator (SOI) substrates up to 300 mm in diameter have been available commercially since 2000,[10] showing wafer bonding to be a highly manufacturable and high-yield fabrication process. The key challenge for heterogeneous compound semiconductor-to-silicon wafer bonding is the mismatch in thermal expansion coefficient. This can be overcome by utilizing low-temperature (<400°C) wafer-bonding processes, which is an attractive approach since it is intrinsically independent of sample size and geometry, in contrast to strain-relief techniques such as prebonding substrate thinning.[11] Recently a new device platform for the realization of electrically driven gain and detection devices on silicon was developed by evanescent coupling between silicon optical waveguides and wafer-bonded III–V materials.[12] As shown by the ongoing demonstration of various components required for Si-based all-optical communications,[13–20] developing a reliable and scalable wafer bonding process is also necessary for upcoming high-yield, low-cost Si photonic integrated circuits.[21]

Compared to other forms of direct wafer bonding, in which no interfacial layer is involved between mating materials, embedding an intervening oxide layer has several merits. Owing to the reactive hydrophilic surface and structural porosity of the

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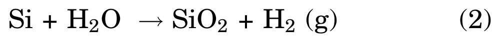
oxide, oxide bonding normally results in a lower required temperature for strong covalent bond formation and greater diffusion efficiency of gas byproducts from polymerization reactions during the bonding process shown in Eqs. 1 and 2;[22] M in Eq. 1 refers to metals with relative high electronegativity.[22] Conventional SiO_2 wafer bonding relies on interfacial layers that are 500 nm thick or more[23] because the thick oxide layer offers a large gas diffusion cross-section, resulting in high outgassing efficiency. However, many devices such as evanescent silicon devices require a thin SiO_2 layer, less than 100 nm thick. Flexible control of the oxide layer thickness down to the nanometer regime is easily attainable in both thermal oxidation and chemical vapor deposition, a major advantage over spin-coating of interfacial bonding material.[24] Oxide interfacial bonding is also largely independent of the mating materials, providing a more universal and flexible approach for the integration of dissimilar materials. It is therefore an inherently more flexible approach.

$$\text{Si-OH} + \text{OH-M} \rightarrow \text{Si-O-M} + \text{H}_2\text{O (g)} \tag{1}$$



$$\text{Si} + \text{H}_2\text{O} \rightarrow \text{SiO}_2 + \text{H}_2 \text{ (g)} \tag{2}$$

In this study a low-temperature thermal SiO_2-PECVD SiO_2 covalent wafer-bonding process to achieve InP-based expitaxial layer transfer to the SOI substrate is described. An ultrathin interfacial 60 nm SiO_2 layer is embedded between the Si and III–V layers to serve as an efficient outgassing quenching medium, while still achieving the high optical coupling required by the device characteristics. It also enables the true integration of InP to Si with close proximity for effective heat conduction. Detailed fabrication flow and optimization process are discussed, followed by extensive bonding characterization. In addition to the most common approaches for analyzing bond quality and strength after wafer bonding (infrared transmission imaging and crack-opening testing),[25] more attention was applied in this study to evaluating the quality of transferred thin epitaxial layers after selectively removing the InP substrate. This allows better analysis of local bond quality, which ultimately affects device yield, since the infrared camera usually does not have high enough resolution to reveal interfacial voids smaller than 200 μm in diameter, and the crack-opening test only provides the average bond strength across the wafer since it is conducted with both substrates intact. The transferred thin expitaxial layers on SOI allow close studies of the effective bonding area and interfacial void density under the microscope. X-ray diffraction (XRD) measurements were also performed to study the potential bonding-stress-induced degradation of the quantum-well active region. Finally, the successful transfer of a 50-mm-diameter InP epitaxial structure to an SOI substrate is described, demonstrating the scalability of this oxide bonding process.

STRUCTURE DESIGN

Since this bonding process aims to realize a hybrid waveguide structure in which the optical mode lies in both the bottom high-refractive-index Si (n = 3.45) waveguide and top III–V ($n \sim 3.0$ to 3.6) layers (Fig. 1), the low-refractive-index oxide layer (n_{SiO_2} = 1.46) has to be thin enough to permit evanescent optical coupling at the bonding interface. By using interfacial SiO_2 layers thinner than 100 nm (data not shown), only slight perturbations of the silicon waveguide and III–V quantum-well confinement factors are made. As an example, the optical-mode amplitude (λ = 1.55 μm) at each layer of a hybrid waveguide structure (Si thickness H = 0.4 μm, rib etch depth t = 0.3 μm, and waveguide width w = 1.5 μm) with 60 nm of interfacial oxide (this work) is shown in Fig. 1, equal to about ~57% power confined in the SOI waveguide and 12% power in the active region (quantum wells and barriers) of the III–V layers. The 60 nm oxide layer, transparent at 1.55 μm, does not contribute noticeably to optical confinement.

Unlike the clean, smooth, and reactive native SiO_2 oxide on Si, the InP native oxide formed in a general air environment or through thermal oxidation falls short of the high oxide quality needed for oxide bonding.[22] To overcome this, we deposit a high-quality SiO_2 layer onto the InP to facilitate bonding. Plasma-enhanced chemical vapor deposited (PECVD) SiO_2 is selected for its low deposition temperature (260°C in this study), which prevents the dissociation of InP. The surface roughness of

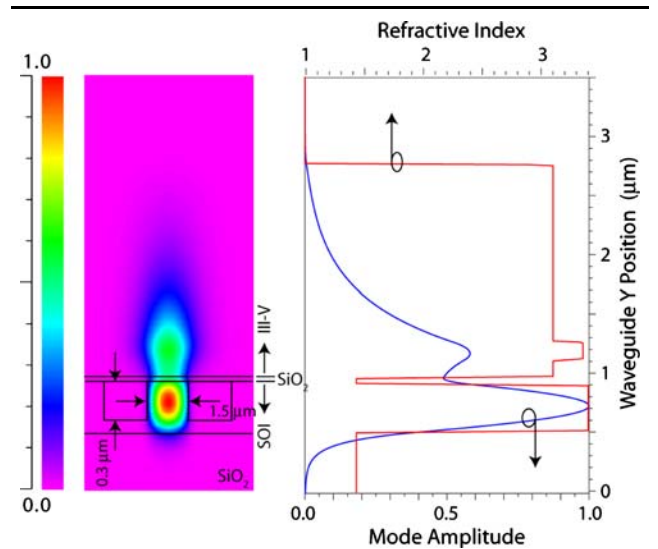


Fig. 1. Refractive indices and simulated optical-mode amplitude of a hybrid waveguide structure with III–V epitaxial layers bonded on a SOI substrate. A 60 nm interfacial oxide layer is included in the simulation.

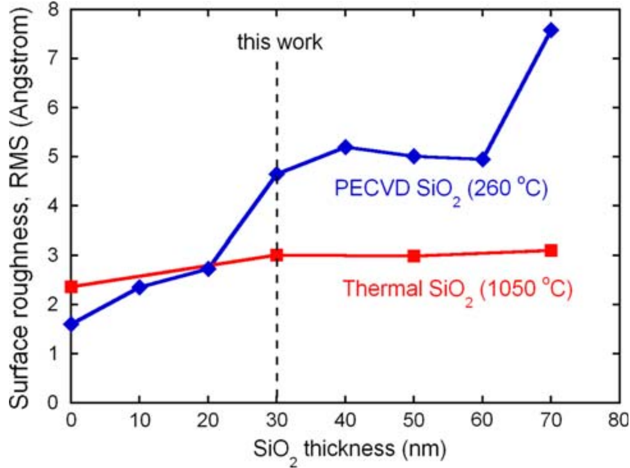


Fig. 2. Surface roughness of PECVD SiO_2 deposited on the InP substrate at 260°C and thermal SiO_2 grown on the SOI substrate at 1050°C as a function of SiO_2 thickness.

PECVD SiO_2 on an as-grown InP substrate with the native oxide removed in NH_4OH prior to deposition was measured by an atomic force microscope (AFM) and is shown in Fig. 2. It can be seen that, although the root-mean-square (RMS) roughness values for PECVD SiO_2 increase with thickness, they are all below 10 Å; a maximum empirical surface roughness value allowed for good bonding,[26] eliminating the need for chemical mechanical planarization (CMP). In this work, 30 nm of PECVD SiO_2 is chosen to keep peak-to-peak roughness below 10 Å while attaining a repeatable, uniform, thin film deposition. The surface roughness of thermally grown SiO_2 on a SOI substrate at 1050°C is well maintained below 3 Å. About 30 nm of thermal SiO_2 is also fixed in this work to give a total interfacial oxide layer thickness of 60 nm.

WAFER-BONDING PROCESS

Commercial prime-grade epitaxial wafers with the structure detailed in Table I were used to replicate the active region transfer process. SOI wafers from Ultrasil, Inc. and Soitec, Inc. used in this work were composed of a 2 μm Si device layer and a 1 μm buried oxide layer. The bonding process started with rigorous cleaning of cleaved SOI and III–V samples in a modified RCA cleaning solution of $HCl:H_2O_2:H_2O$ = 0.2:1:5 at 80°C for 10 min and

Table I. InP Epitaxial Structure for Wafer Bonding Experiments in This Work

Layer Type	Thickness
InGaAs cap layer	200 nm
InP bonding layer	2 μm
InGaAs etch-stop layer	200 nm
InP substrate	400 μm

solvent solutions of acetone and isopropyl alcohol, respectively. Gentle physical swab cleaning on the sample surface was generally necessary to remove inorganic surface contamination until a particle-free surface was obtained under 200× microscopic inspection. After dipping the SOI samples in a 1% HF solution for 20 s to remove the native oxide, dry oxidation was then performed to grow 30 nm of SiO_2. The 200 nm InGaAs cap layer was selectively removed on the III–V samples in a solution of $H_3PO_4:H_2O_2:H_2O$ = 1:1:38 for 5 min at room temperature. This was followed by a 30 nm PECVD SiO_2 deposition. Due to the inhomogeneous nature of the PECVD process,[27,28] a degassing bake at 250°C for 1 h to 2 h was carried out after deposition to drive undesirable gas molecules out of the thin film. Next, an O_2 plasma surface treatment was conducted on the SOI and III–V samples as this was found to suppress the interfacial void formation but has been reported not to contribute to bonding strength enhancement in SiO_2-SiO_2 covalent bonding of Si wafers.[28] The O_2 plasma process was performed in a reactive ion etching (RIE) tool with 39 W radiofrequency power, 26 sccm O_2 flow rate, and 15 mTorr chamber pressure for 45 s. A detailed discussion is provided in the next section. Immediately after the O_2 plasma surface treatment, the second surface activation step was to dip SOI and III–V samples in very dilute HF solution (0.025%) for 1 min to form a more porous fluorinated oxide network.[28] The last activation step involved further conversion of Si-OH to Si-NH_2 bonds in NH_4OH.[28,29] Instead of dipping the samples in NH_4OH solution directly,[29] an NH_4OH vaporization process was found to result in a more uniform and cleaner surface activation. The SOI and III–V samples were placed on a 125°C hotplate with a glass cover for 5 min to reduce the H_2O monolayers on the sample surface while NH_4OH vapor was introduced simultaneously. Spontaneous mating at room temperature was then carried out manually when samples had cooled to room temperature. Further annealing at 300°C was conducted in a commercial Suss SB6E wafer bonder with 1.5 MPa pressure applied to the samples to obtain strong covalent bonding. The InP substrate was finally etched off in a solution of $HCl:H_2O$ = 3:1 at room temperature with an etch rate of ~6 μm/min, leaving 200 nm InGaAs and 2 μm InP epitaxial layers plus an interfacial oxide layer with a total thickness of 60 nm on the SOI substrate.

RESULTS AND DISCUSSION

Surface Energy Characterization

As the most critical factor in bonding quality characterization, the surface energies of bonded pairs were measured by the conventional crack-opening method[25] in a class 2000 cleanroom environment. Two opposite edges of the 1 cm^2 SOI samples used in this measurement were angularly

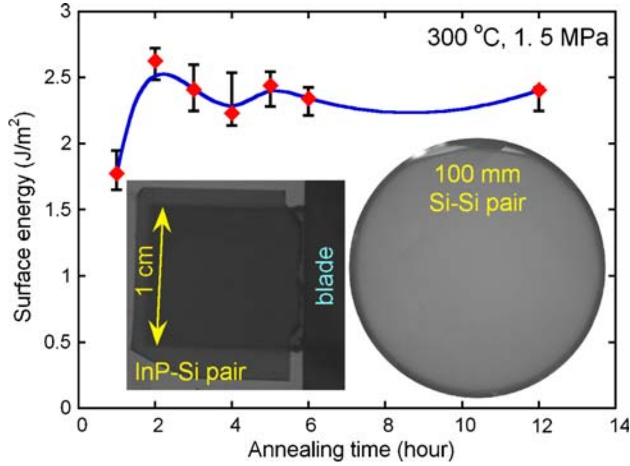


Fig. 3. The surface energies of 100 mm Si-Si bonded pairs as a function of annealing time. Left inset: infrared transmission image of a 1 cm^2 SOI sample bonded with a slightly larger InP piece after a 2-h anneal, showing its right edge broken as the blade was inserted. Right insert: a 100 mm Si-Si pair annealed for 2 h, showing a void-free bonding interface.

polished to 45 deg to the bonding surface, allowing a thin 100 μm blade to be inserted into the bonding interface easily, correctly, and repeatable. The top InP samples with the ~400 μm InP substrate remained but were are all broken less than 1 mm away from the Si edge (see the left inset of Fig. 3) when it was attempted to insert the blade, resulting in failure to determine the equilibrium crack length.

As an alternative method, 100 mm Si-Si pairs were bonded in an identical process by treating one Si wafer as a III–V material, i.e., covered by 30 nm of PECVD SiO_2. Void-free bonding was achieved, as shown by the infrared transmission image in the right inset of Fig. 3. The surface energy measurement was performed at three different positions on the bonded pairs, and two bonded pairs were prepared for each annealing time, leading to the average surface energies and maximum and minimum values in Fig. 3. A high average surface energy up to 2.63 J/m^2 was achieved after only a 2-h anneal at 300°C. Longer anneal times up to 12 h resulted in average surface energies between 2.23 J/m^2 to 2.44 J/m^2. The error bars only include the scatter in the measured crack lengths. The crack length measurement is very sensitive to atmospheric conditions and each measurement is conducted at a different time, leading to an increased error in the measurement that was not quantified. We expect the behavior to be the following: at short anneal times, the surface energy is low; as the anneal time increases, this surface energy increases rapidly until it saturates. Based on Fig. 3 saturation of the surface energy occurs after 2 h of annealing. Since the oxide bonding is relatively independent of the substrate material at low temperatures (e.g., 300°C) where oxidation of Si with the H_2O byproduct at the bonding interface is negligible, the H_2O byproduct has to be partially absorbed by the oxide and diffuse through the oxide and bonding interface, instead of being consumed to form new SiO_2 as per Eq. 2 above. The actual surface energy of Si-InP bonded pairs after 2 h of annealing is therefore likely to be very close to 2.63 J/m^2 for the Si-Si pairs, over four times larger than the bulk InP fracture energy of 0.63 J/m^2.[11] This can explain the fracture of InP in the measurement.[30] Accurate crack-opening measurement requires a larger InP wafer with a thinner substrate thickness, which is beyond the scope of the present work. Alternative bonding strength characterization is under development.

Other than the conventional method to determine the bonding strength, III–V–SOI bonded samples also experience a harsh dicing test, which is also a standard process for fabricating Fabry-Pérot cavity devices. The bonded samples with only InGaAs and InP epitaxial layers on a SOI substrate are normally cut into 1 mm bars (Fig. 4a) by a 100-μm-thick blade with a spin rate of more than 10,000 rev/min. Though the III–V side is up and there is no surface protection during dicing, the chipping of the III–V epitaxial layer is no more than 15 μm and follows the SOI fringe consistently, as shown in Fig. 4b. Figure 4c,d represents scanning electron microscopic (SEM) cross-sectional views of a further polished bar, showing III–V epitaxial layers tightly bonded onto the SOI substrate with a 60 nm interfacial SiO_2 layer. Survival after harsh dicing and polishing also indicates strong bonding between the III–V material and the SOI substrate.

Interfacial Void Density Study

It has been reported that trapped gas byproducts can build up a high internal pressure,[31] which can easily deform the thin epitaxial layers. Since high-density active optoelectronic components in the micrometer regime are built on this hybrid waveguide platform, the interfacial void density has a large impact on device yield. O_2 plasma treatment of the SiO_2 surface on both the SOI and III–V samples was found to be very helpful for the suppression of interfacial voids as shown by the direct comparison in Fig. 5. As shown by the photograph (Fig. 5a) and the close-up (100×) Nomaski-mode microscopic image (Fig. 5c) of a bonded sample without O_2 plasma surface treatment, interfacial voids in the diameter range of 1 mm down to 2 μm appear after removing the thick InP substrate, resulting in about 138 cm^{-2} of void density. The void size difference is related to the surface defect distribution and size[32] when gas byproduct transportation is inefficient, and some possible contamination around the sample edges. In contrast, the O_2-plasma-treated sample in Fig. 5b and c demonstrates nearly void-free III–V epitaxial bonding. The void density of 2 cm^{-2} is likely due to surface defects or cleaning. The few voids visible close to the sample edge are believed to be due to contamination from sample handling with tweezers. To further simulate the actual device post processing and enlarge the tiny voids, bonded

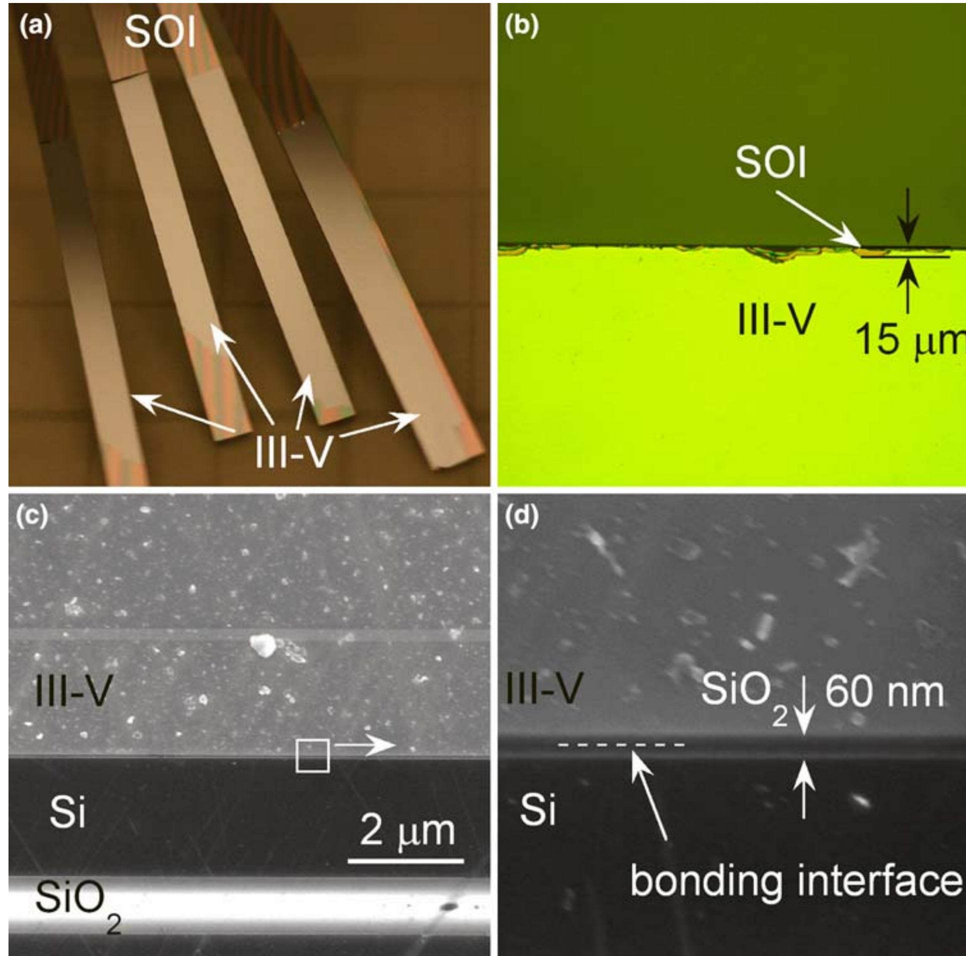


Fig. 4. (a) Photograph of diced 1-mm-wide bars with III–V epitaxial layers transferred to an SOI substrate after 2-h annealing at 300°C. (b) Microscopic (200×) top view of a diced bar showing ≤15 μm III–V chipping due to dicing. (c) SEM cross-sectional view of a polished bar, showing III–V epitaxial layers tightly bonded to the SOI substrate with a 60 nm interfacial SiO_2 layer, which is clearly seen in the high-magnification SEM image (d).

samples were baked to 250°C on a hotplate for 10 min and then re-inspected for interfacial voids under microscope. The slight increase in void density to ≤5 cm^{-2} was probably due to residual gas molecules in the PECVD SiO_2, which is tolerable for device fabrication. It is well known that O_2 plasma treatment can grow a highly strained, thin (<5 nm) oxide on hydrophobic surfaces,[4] resulting in a very reactive hydrophilic surface and subsequently high Si-OH density after contact with a solution rich in hydroxyl groups (–OH), for example, H_2O. The same plasma process on SiO_2 is believed to have no effect on additional oxide growth, but can break the Si-O bonds, leading to temporarily unstable surface states[33] for more effective and uniform Si-O to Si-F and Si-NH_2 conversion in the following HF and NH_4OH activation. The plasma also causes deformation and decomposition of the microcrystalline region in the thermal oxide, resulting in a more amorphous oxide network.[33] It subsequently reduces the generation of the H_2O byproduct, and fluorinated oxide with larger rings also enhances gas diffusion and absorption,[28] both resulting in a reduction in the void density.

X-Ray Diffraction (XRD) Measurement

It is known that there are many fewer threading dislocations at a wafer-bonding interface than in heteroepitexial growth, particularly for InP-based narrow-bandgap compound semiconductor growth on Si,[3] however the difference in the thermal expansion coefficient of InP (4.8×10^{-6}/K), Si (2.6×10^{-6}/K), and SiO_2 (0.56×10^{-6}/K) could cause nonnegligible stress after 300°C annealing, degrading device performance or potentially lifetime. It is therefore of interest to study the bonding-induced stress, especially since most of the stress is concentrated in thin III–V layers rather than the thick SOI substrate. XRD provides an accurate and nondestructive method to reveal the stress within the bonded pairs. In order to pinpoint the stress-induced material degradation, a metalorganic chemical vapor deposition (MOCVD)-grown multiple-quantum-well (MQW) device structure (λ = 1.55 μm)

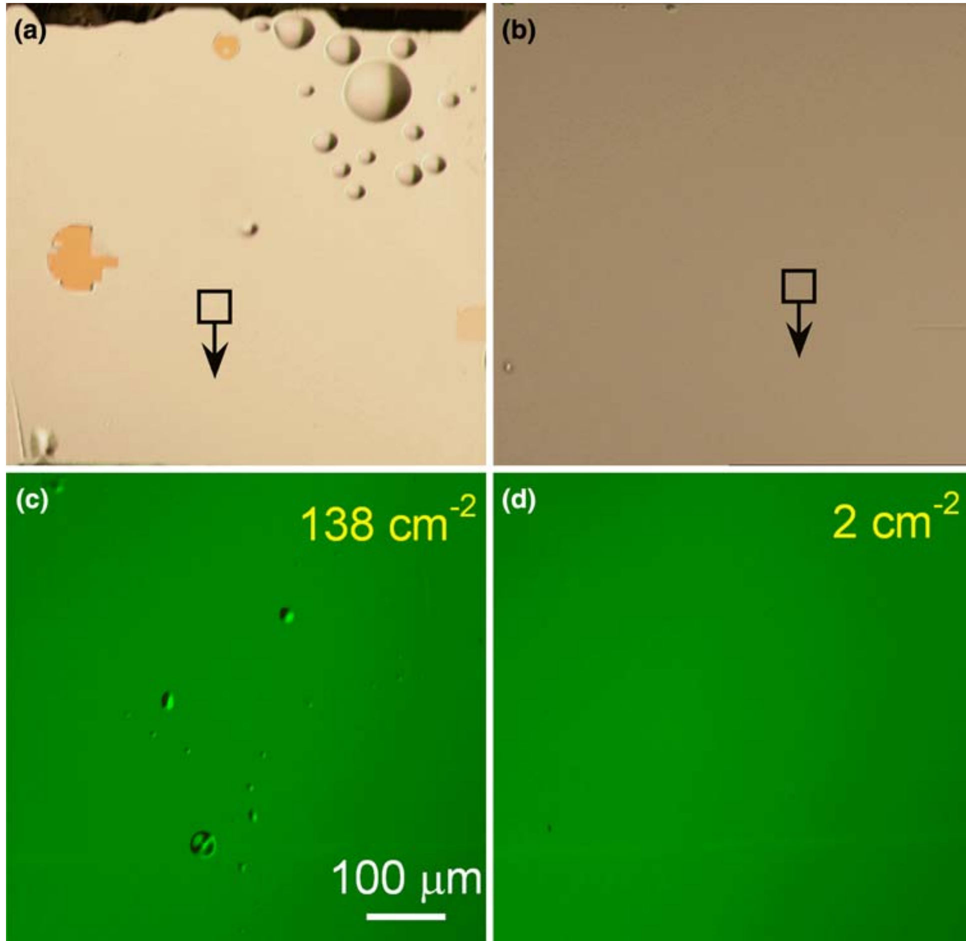


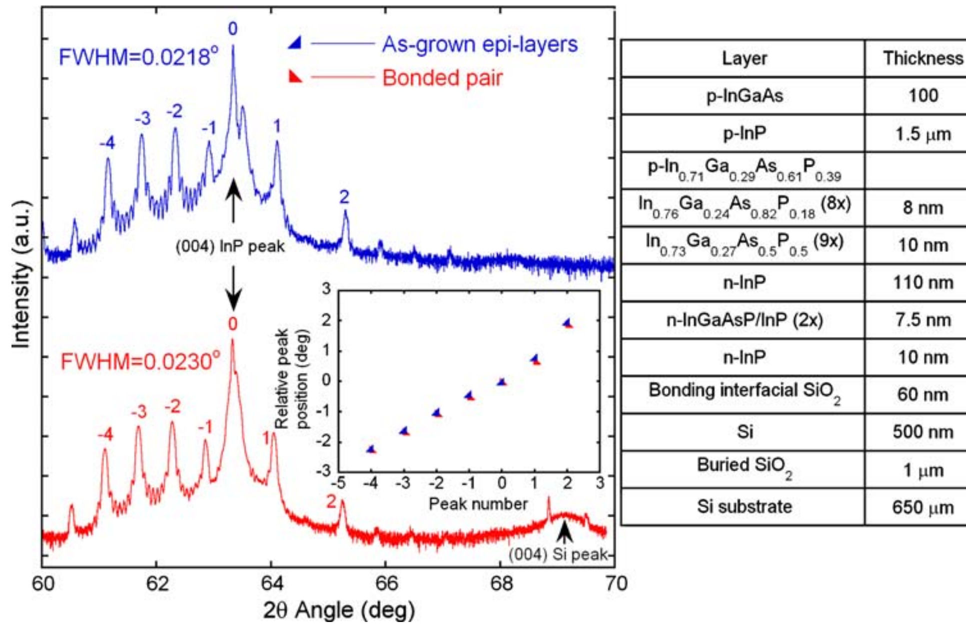
Fig. 5. Photographs of bonded samples (a) without and (b) with O_2 plasma surface treatment. (c) and (d) correspond to Nomaski-mode microscopic (100×) images of the highlighted square regions in (a) and (b), respectively.

was bonded onto a SOI substrate after a 2-h anneal at 300°C. Figure 6 shows the rocking curve θ–2θ XRD scans of the as-grown and the bonded sample with the same piece of III–V epitaxial layers after InP substrate removal. The layer structure is detailed in the table on the right-hand side in Fig. 6. In this complicated structure a 1.5 μm *p*-type InP layer and an active region of eight 8 nm $In_{0.71}Ga_{0.29}As_{0.61}P_{0.39}$ alternating with nine 10 nm $In_{0.73}Ga_{0.27}As_{0.5}P_{0.5}$ layers represent the most significant signatures, appearing as the main (004) InP peak and major superlattice satellites in Fig. 6. It is clear that both the intensity and contrast of the (004) InP main peak and the satellite peaks are essentially unchanged after epitaxial transfer. By naming them as "–4" to "2" peaks in the figure, their relative peak positions normalized to the (004) InP peak "0" are plotted in the inset of Fig. 6, showing extremely small relative peak position shifts. The full-width at half-maximum (FWHM) of the (004) InP peak increases only slightly from 0.0218 deg to 0.0230 deg after bonding.

The positions and width of the MQW peaks and the (004) InP main peak are well maintained, indicating negligible stress effects in the MQW active region. As the stress due to the thermal expansion mismatch is a function of layer volume, the 60-nm-thick interfacial oxide layer has a very limited negative impact. Low-temperature annealing and the superlattice layers underneath the MQW active region also contribute to minimizing the bonding stress and stopping bonding defect propagation towards the MQW.[34]

Wafer-Scale Oxide Bonding

Scalability is the next key problem to demonstrate the large-scale manufacture potential of this oxide bonding process. In order to eliminate surface contamination from wafer handling and activation processing steps in a class 100–1000 cleanroom, a microcleanroom[35] was built and modified to enable dilute HF and NH_4OH activation in the same housing after initial cleaning and O_2 plasma surface treatment. Figure 7 demonstrates a 50 mm (2 inch) InP epitaxial structure successfully bonded to a SOI substrate after 2-h annealing at 300°C. Void-free bonding and nearly 100% epitaxial transfer are achieved. A small III–V open spot was caused



Layer	Thickness
p-InGaAs	100
p-InP	1.5 μm
p-$In_{0.71}Ga_{0.29}As_{0.61}P_{0.39}$	
$In_{0.76}Ga_{0.24}As_{0.82}P_{0.18}$ (8x)	8 nm
$In_{0.73}Ga_{0.27}As_{0.5}P_{0.5}$ (9x)	10 nm
n-InP	110 nm
n-InGaAsP/InP (2x)	7.5 nm
n-InP	10 nm
Bonding interfacial SiO_2	60 nm
Si	500 nm
Buried SiO_2	1 μm
Si substrate	650 μm

Fig. 6. XRD θ–2θ scans of as-grown and bonded epitaxial layers (see the table on the right-hand side), showing the maintenance of the strong (004) InP peak and the MQW satellite peaks. Inset: MQW peak (–4, –3, –2, –1, 1, 2) positions relative to the (004) InP main peak (0), indicating the very small peak position shift after annealing.

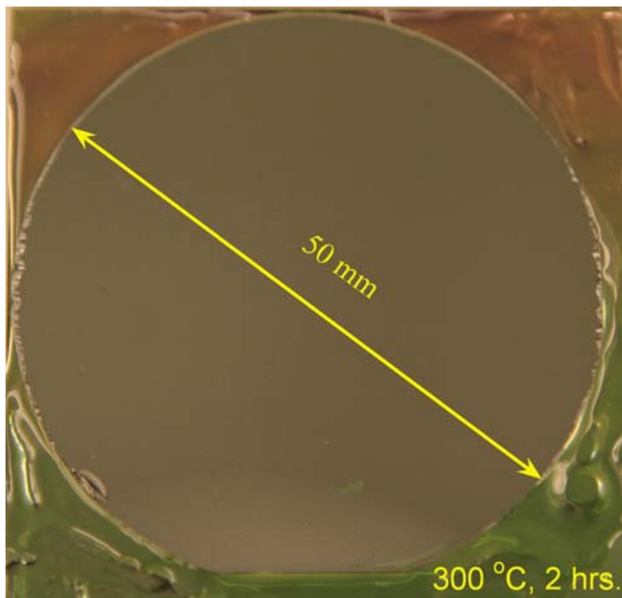


Fig. 7. Photograph of a 50 mm (2 inch) InP epitaxial layers transferred to an SOI substrate after 2-h annealing at 300°C.

because of a 32 μm surface defect on the III–V wafer surface. Imperfections around the flat edge are due to tweezer handling as well. Prior to InP substrate removal, CrystalBond™ wax was used to cover and protect the edge of the III–V wafer, preventing HCl solution from etching the 2 μm InP bonding layer laterally. The same bonding quality was obtained when scaled to 50 mm wafers from 1 cm^2 samples for an identical bonding process, which demonstrates the great potential to scale up to even larger sizes.

CONCLUSION

Low-temperature, ultrathin oxide SOI-InP bonding has been demonstrated, primarily for a hybrid Si evanescent device platform. The 60 nm interfacial oxide layer composed of 30 nm thermal SiO_2 on SOI and 30 nm PECVD SiO_2 on III–V compound semiconductors is the thinnest interfacial dielectric reported to date for the oxide bonding of dissimilar materials to the best of our knowledge. With proper surface cleaning and activation in dilute HF solution and NH_4OH vapor, an average surface energy up to 2.65 J/m^2 was achieved after 2-h annealing at 300°C. Additional O_2 plasma treatment of the SiO_2 surfaces was found to be helpful for the suppression of small interfacial voids which only become visible on thin epitaxial layers after removing the thick InP substrate. XRD measurements showed nearly unchanged θ–2θ scans, indicating negligible bonding-strain-induced degradation of structure integrity. Promising scalability was demonstrated by attaining identically high bonding quality in a 50 mm InP epitaxial structure transferred to the SOI substrate. About 2-h annealing also implies that the 60-nm-thick interfacial oxide layer is sufficient to diffuse and absorb gas byproducts from bonding polymerization reactions. It is finally noted that this ultrathin oxide bonding process could be directly transferable to other applications where dielectric isolation is needed, such as high-power and high-voltage device integration.[36] Due to the well-known high-quality thermal SiO_2 grown in dry O_2

primarily for transistor gate oxides,[37] the interfacial oxide in this work is expected to experience low leakage current and high breakdown voltage. Actual oxide leakage current and breakdown voltage will be measured with doped InP and Si bonded pairs in the near future.

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REFERENCES

1. U. Gösele and Q.Y. Tong, *Annu. Rev. Mater. Sci.* 28, 215 (1998). doi:10.1146/annurev.matsci.28.1.215.
2. U. Gösele, M. Alexe, P. Kopperschmidt, and Q.Y. Tong, Paper Presented at International Semiconductor Conference, CAS '97 Proceedings, Sinaia (Romania, October, 1997), pp. 7–11. http://ieeexplore.ieee.org.
3. D. Fehly, A. Schlachetzki, A.S. Bakin, A. Guttzeit, and H.H. Wehmann, *IEEE J. Quantum Electron.* 37, 1246 (2001). doi:10.1109/3.952535.
4. D. Pasquariello and K. Hjort, *IEEE J. Sel. Top. Quantum Electron.* 8, 118 (2002). doi:10.1109/2944.991407.
5. K. Won-Gu, L. Jong-Sun, K. Sang-Won, and L. KwyRo, *IEEE Electron. Dev. Lett.* 16, 2 (1995).
6. T. Yamagata and K. Shimomura, *IEEE Photonic Tech. Lett.* 9, 1143 (1997). doi:10.1109/68.605530.
7. A. Karim, J. Piprek, P. Abraham, D. Lofgreen, C. Yi-Jen, and J.E. Bowers, *IEEE J. Sel. Top. Quantum Electron.* 7, 178 (2001). doi:10.1109/2944.954127.
8. K.D. Choquette, K.M. Geib, B. Roberds, H.Q. Hou, R.D. Twesten, and B.E. Hammons, *Electron. Lett.* 34, 1404 (1998). doi:10.1049/el:19981002.
9. G. Roelkensa, J.V. Campenhouta, J. Brouckaerta, D.V. Thourhouta, R. Baetsa, P.R. Romeob et al., *Mater. Today* 10, 36 (2007). doi:10.1016/S1369-7021(07)70178-5.
10. http://soitec.com/en/about/.
11. Q.Y. Tong, Q. Gan, G. Hudson, G. Fountain, and P. Enquist, *Appl. Phys. Lett.* 84, 732 (2004). doi:10.1063/1.1644615.
12. H. Park, A.W. Fang, S. Kodama, and J.E. Bowers, *Opt. Exp.* 13, 9460 (2005). doi:10.1364/OPEX.13.009460.
13. H.-H. Chang, A.W. Fang, M.N. Sysak, H. Park, R. Jones, O. Cohen et al., *Opt. Exp.* 15, 11466 (2007). doi:10.1364/OE.15.011466.
14. H. Park, Y.-H. Kuo, A.W. Fang, R. Jones, O. Cohen, M.J. Paniccia et al., *Opt. Exp.* 15, 13539 (2007). doi:10.1364/OE.15.013539.
15. H. Park, A.W. Fang, R. Jones, O. Cohen, O. Raday, M.N. Sysak et al., *Opt. Exp.* 15, 6044 (2007). doi:10.1364/OE.15.006044.
16. Y.-H. Kuo, H.-W. Chen, and J.E. Bowers, Paper Presented at The Optical Fiber Communication Conference (2008).
17. B.R. Koch, A.W. Fang, O. Cohen, and J.E. Bowers, *Opt. Exp.* 15, 11225 (2007). doi:10.1364/OE.15.011225.
18. A.W. Fang, R. Jones, H. Park, O. Cohen, O. Raday, M.J. Paniccia et al., *Opt. Exp.* 15, 2315 (2007). doi:10.1364/OE.15.002315.
19. H. Park, A.W. Fang, O. Cohen, R. Jones, M.J. Paniccia, and J.E. Bowers, *IEEE J. Sel. Top. Quantum Electron.* 12, 1657 (2006). doi:10.1109/JSTQE.2006.884064.
20. A.W. Fang, H. Park, O. Cohen, R. Jones, M.J. Paniccia, and J.E. Bowers, *Opt. Exp.* 14, 9203 (2006). doi:10.1364/OE.14.009203.
21. D. Liang, H. Park, A.W. Fang, J.E. Bowers, Paper Presented at the 49th Electronic Materials Conference 2007 (Notre Dame, IN, June 20–22, 2007).
22. Q.Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology* (Wiley: New York, 1998).
23. K. Schjolberg-Henriksen, S. Moe, M.M. Visser Taklo, P. Storas, and J.H. Ulvensoen, *Sen. Act. A Phys.* 142, 413 (2008). doi:10.1016/j.sna.2007.02.020.
24. D. Goustouridis, K. Minoglou, S. Kolliopoulou, S. Chatzandroulis, P. Morfouli, P. Normand et al., *Sen. Act. A Phys.* 110, 401 (2004). doi:10.1016/j.sna.2003.09.011.
25. W.P. Maszara, G. Goetz, A. Caviglia, and J.B. McKitterick, *J. Appl. Phys.* 64, 4943 (1988). doi:10.1063/1.342443.
26. C. Gui, M. Elwenspoek, N. Tas, and J.G.E. Gardeniers, *J. Appl. Phys.* 85, 7448 (1999). doi:10.1063/1.369377.
27. C.S. Tan, A. Fan, K.N. Chen, and R. Reif, *Appl. Phys. Lett.* 82, 2649 (2003). doi:10.1063/1.1569657.
28. Q.-Y. Tong, G. Fountain, and P. Enquist, *Appl. Phys. Lett.* 89, 042110 (2006). doi:10.1063/1.2240232.
29. Y.L. Chao, Q.Y. Tong, T.H. Lee, M. Reiche, R. Scholz, J.C.S. Woo et al., *Electrochem. Solid-State Lett.* 8, G74 (2005). doi:10.1149/1.1857671.
30. W.P. Maszara, *J. Electrochem. Soc.* 1, 341 (1991). doi:10.1149/1.2085575.
31. S. Mack, H. Baumann, and U. Gösele, *Sen. Act. A Phys.* 56, 273 (1996). doi:10.1016/S0924-4247(96)01320-9.
32. Z.X. Xiong and J.P. Raskin, *J. Microelectromech. Syst.* 14, 368 (2005). doi:10.1109/JMEMS.2004.839027.
33. L.I. Popova, E.D. Atanassova, S.K. Peneva, and E.A. Tcukeva, *Cryst. Res. Technol.* 23, 979 (1988). doi:10.1002/crat.2170230806.
34. K.A. Black, P. Abraham, A. Karim, J.E. Bowers, and E.L. Hu, Paper Presented at the 11th International Conference on Indium Phosphide and Related Materials 1999 (Davos, Switzerland, May 7–11, 1999).
35. R. Stengl, K.-Y. Ahn, and U. Gösele, *Jpn. J. Appl. Phys.* 27, L2364 (1988). doi:10.1143/JJAP.27.L2364.
36. H. Ohashi, J. Ohura, T. Tsukakoshi, and M. Simbo, Paper Presented at the International Electron Devices Meeting 1986 (Los Angeles, CA, December 7–10, 1986).
37. M. Itsumi, *SiO_2 in Si Microdevices* (Springer: Berlin, 2003).