Scalable Wafer Bonding for Active Photonic Devices on Silicon

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(Invited Paper)

Recent progress in silicon photonics has generated interest in low cost and high volume integration of photonic devices on silicon wafers. One of the main reasons is the possibility of integration of photonic and electronic devices on silicon wafers through a monolithic fabrication process. Recently we demonstrated silicon evanescent lasers using a new architecture as one way to build photonic active devices on a silicon-on-insulator (SOI) wafer via low temperature wafer bonding [1, 2]. This approach adopts a wafer bonded structure between a silicon passive waveguide and III-V offset quantum wells as shown in Fig.1. The optical mode is predominantly confined in the silicon waveguide and a small percentage of the mode evanescently coupled into the III-V gain region. With this structure, optical gain can be achieved by electrical injection of the III-V active quantum well region. The symmetry of the III-V region leads to the definition of the optical mode by processing in the silicon region, allowing for bonding to be done without any critical alignment. Moreover, as shown in Fig. 2, the waveguide fabrication of passive device regions and active regions can be done simultaneously on the SOI wafer enabling self aligned coupling of the optical mode from the active device to the passive silicon waveguide very efficiently. This is a key advantage of this approach, allowing for large scale photonic integration on a silicon substrate.

Figure 3 shows a proposed structure of a WDM transmitter integrated with multiple laser sources and modulators as an example of photonic integration using this platform. First, the silicon waveguides are fabricated together with electronic circuitry through standard CMOS processing. Typical waveguide dimensions are in the range of 1~5 microns wide which can be easily fabricated by a conventional optical lithography and can be formed by a simple etch step. Then the III-V layer structure is bonded to the silicon wafer at the wafer or die level followed by the substrate removal and is etched off except for the active device regions as indicated in Fig. 3 as III-V gain or III-V phase modulator. After passing the III-V region through mesa etching, implantation, and metal deposition, electrical connects are formed between the electronic circuit region and active photonic device region.

To realize this high level of integration the post processing steps, including the bonding process and backside III-V processing, must not impair the electronics fabricated prior to the bonding process. For this reason, we developed a low temperature bonding process. The oxide meditated wafer bonding has been investigated because the hydrophilic oxide surface can form strong chemical bonds at low annealing temperature in the range of 100 ºC ~ 300 ºC [3]. A ~5 nm thick oxide layer created by oxygen plasma is used for our devices [1, 2]. K. Warner *et al*. have demonstrated a similar process, used in SOI wafer manufacturing, utilizing ~1500 nm thick oxide with chemical mechanical polishing (CMP) process to achieve 150 mm wafer bonding between InP based detectors and CMOS circuits [4]. Low temperature bonding with other plasma treatments, such as B_2H_6, has also been demonstrated [5]. Moreover, this low temperature process does not cause any significant wafer bowing or cracking associated with the high thermal mismatch of III-V materials with silicon; a typical problem in direct wafer bonding seen after high temperature annealing [6]. We will report on bonding to CMOS wafers, and how the electrical characteristics were modified by the bonding process.

The evanescently coupled structure enables the realization of electrically driven active photonic devices. Furthermore, its self-aligned structure and fabrication process, consisting of CMOS compatible waveguide formation and low temperature wafer bonding process, make this approach more promising for photonic-electronic integrated circuits with low cost and high functionality.

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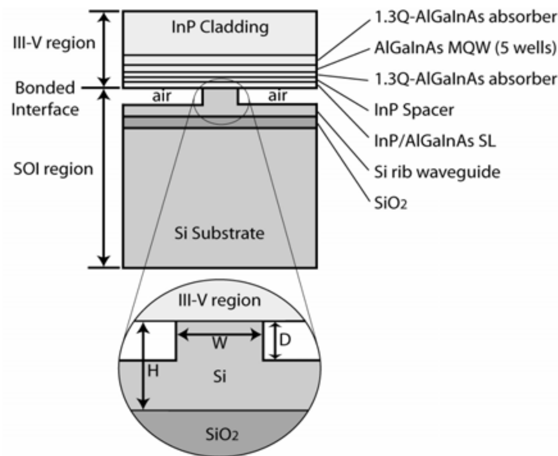

Fig. 1. Device structure of silicon evanescent lasers.

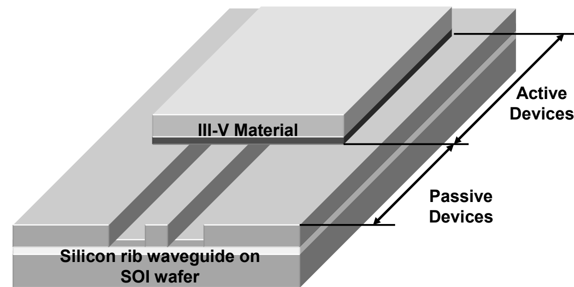

Fig. 2. General platform of photonic integration on a SOI wafer

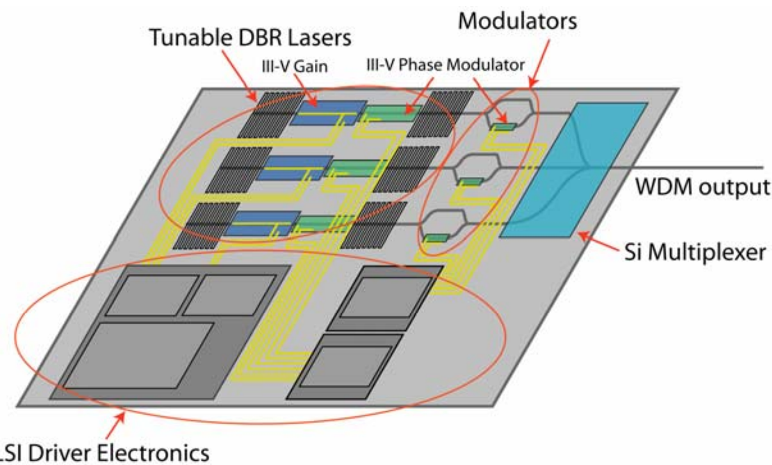

Fig.3. Proposed structure of WDM transmitter fabricated with silicon electronics