

# A Technology for Integrating Active Photonic Devices on SOI Wafers

John E. Bowers<sup>a</sup>, Hyundai Park<sup>a</sup>, Alexander W. Fang<sup>a</sup>, Richard Jones<sup>b</sup>,  
Oded Cohen<sup>c</sup>, and Mario J. Paniccia<sup>b</sup>

<sup>a</sup>University of California Santa Barbara, ECE Department, Santa Barbara, CA 93106, USA

<sup>b</sup>Intel Corporation, 2200 Mission College Blvd, SC-12-326, Santa Clara, CA 95054, USA

<sup>c</sup>Intel Corporation, SBI Park Har Hotzvim, Jerusalem, 91031, Israel

Email: [bowers@ece.ucsb.edu](mailto:bowers@ece.ucsb.edu)

(Invited Paper)

## Abstract

We present an integration technology for building active photonic devices on a Silicon-On-Insulator (SOI) based platform by using plasma assisted wafer bonding of III-V quantum wells to passive devices fabricated on SOI. Using this technique we have demonstrated an optically pumped silicon evanescent laser operating continuous wave (CW) up to 60 °C. The lasers emit at 1.5  $\mu\text{m}$  with a minimum threshold of  $\sim 25\text{mW}$  and a maximum single-sided fiber-coupled CW output power at room temperature of 4.5 mW.

## I. Introduction

Silicon photonics has received a lot of attention in recent years due to silicon's promise to be the platform for the integration of photonic and electronic circuits. This has been driven by the maturity and well understanding of silicon VLSI processing and silicon's transparency at the communication wavelengths of 1.3 $\mu\text{m}$  and 1.5 $\mu\text{m}$ . However, silicon's inefficient light generation has been a major obstacle towards building active photonic devices. Several approaches have been used to overcome this intrinsic obstacle such as Raman lasers [1, 2] and LEDs [3] with material engineering. Recently we demonstrated an alternative approach, hybrid silicon evanescent lasers, in which III-V based quantum wells are bonded to silicon rib waveguides [4]. This approach can be directly extended to electrically driven active photonic devices and also raises the potential of photonic integration with silicon CMOS circuits on SOI wafers. In this paper, we discuss this integration technology including performance and yield of hybrid silicon evanescent lasers fabricated through this technology is reviewed.

## II. General platform and process

Figure 1 shows the proposed platform of photonic integration on a SOI wafer. The platform consists of passive device regions and active device regions. The active regions consist of III-V materials bonded to silicon rib waveguides in order to provide optical gain. The III-V materials can be bonded at the wafer scale and etched away in passive regions or selectively bonded to the active device regions. This approach is advantageous to that of other flip-chip bonded approaches because the optical mode is self aligned and therefore does not have the tight alignment requirements more commonly associated

with coupling external optical sources to photonic integrated circuits.

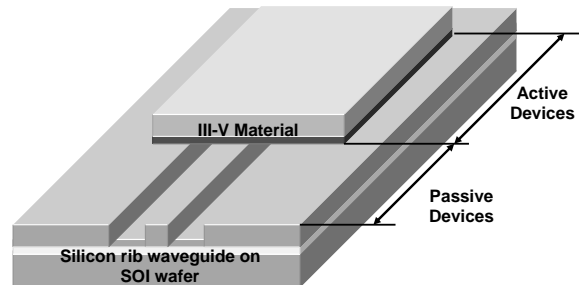


Fig. 1. General platform of photonic integration on a SOI wafer

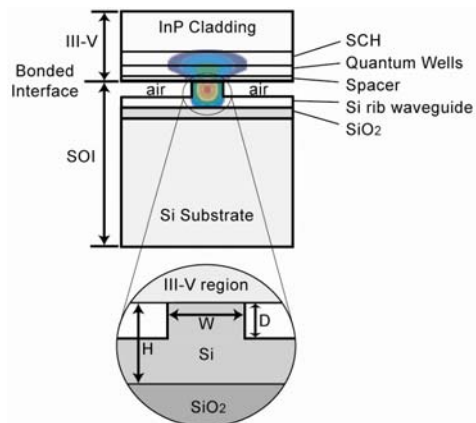


Fig. 2. General structure of active devices on a SOI wafer

Figure 2 shows the general structure of active devices based on this technology. The structure is divided into two regions: the silicon-on-insulator (SOI) passive-waveguide region and the III-V active region

that provides optical gain. Most of the optical mode is confined in a silicon waveguide while a small portion of the mode is evanescently coupled into the active region. The optical properties are defined by

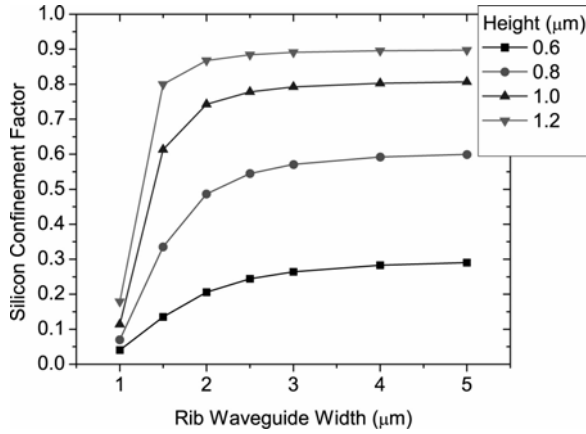


Fig. 3. Calculated silicon confinement factor as a function of waveguide height and width.

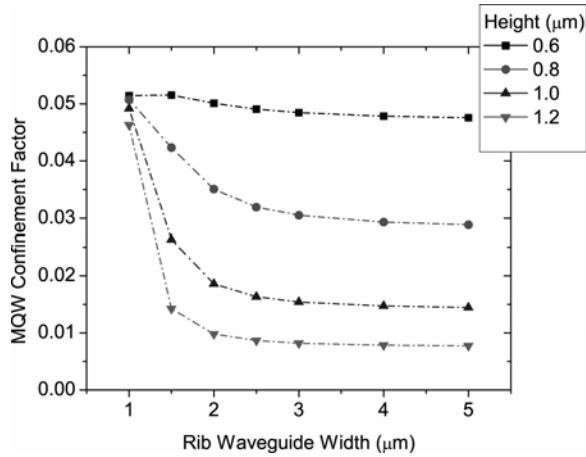


Fig. 4. Calculated quantum well confinement factor as a function of waveguide height and width.

the dimensions of the silicon rib waveguides. Figures 3 and 4 show the confinement factor in the silicon and quantum well region's dependence on the width and height of the silicon rib waveguide. In general, the optical mode has greater confinement in the silicon region with wider or higher waveguide dimensions. Waveguide dimensions can be tailored to achieve the desired confinement factors and resulting gain depending upon the specific application..

Passive regions in this platform consist of Silicon Rib waveguides without the III-V layers. At the junction of the active and passive sections, a mode mismatch exists leading to coupling loss. The coupling

efficiency due to modal mismatch as a function of waveguide width and height are shown in Figure 5. Coupling losses are less than 3 dB from waveguides taller than 0.8 µm and wider than 1 µm. It is seen by comparing Figure 5 with Figure 3 that the coupling

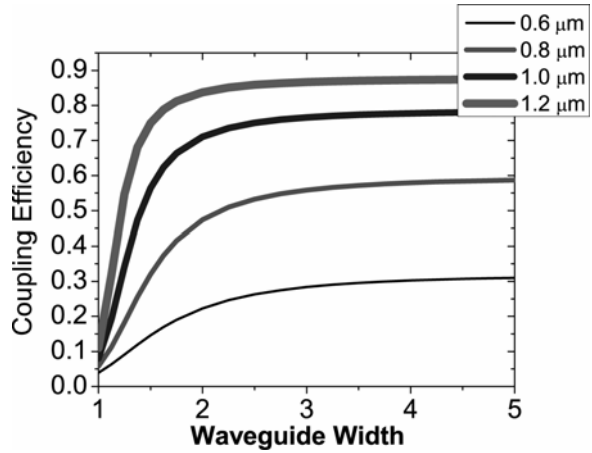


Fig. 5. Calculated active region to passive region fundamental mode coupling loss as a function of height and width

efficiency is almost identical to the silicon region confinement factor.

General processing steps are broken into three major steps: fabricating silicon passive devices, bonding silicon with III-V materials via low temperature plasma assisted wafer bonding [5, 6] and backside processing of the III-V region. Backside processing of the III-V region is carried out to achieve two things: manipulation of current flow and removal of active materials in passive regions.

The large mismatch in thermal expansion coefficients between Si ( $2.6 \times 10^{-6} \text{ K}^{-1}$ ) and InP ( $4.8 \times 10^{-6} \text{ K}^{-1}$ ) can introduce dislocations or cracks at temperatures above 300 °C for the substrate thicknesses of 500 µm and 350 µm for Si and InP respectively. Annealed devices at 600 °C without plasma treatment commonly show surface non-uniformities when observed through a microscope after InP substrate removal as shown in Figure 6a.

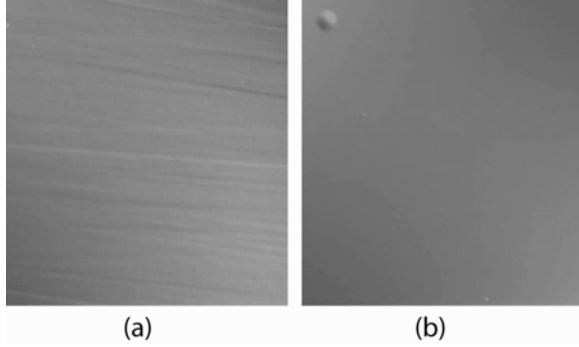


Fig. 6. Nomarski Images of III-V epi surface after bonding and subsequent InP substrate removal (a) annealed at 600 °C (b) annealed at 250 °C after oxygen plasma treatment.

Moreover, the high temperature bonding process results in a reduction of photoluminescence intensity by a factor of six relative to low-temperature oxygen plasma assisted bonding. Figure 6b shows the smooth III-V epi-surface after bonding and InP substrate removal annealed at 250 °C. The low temperature annealing process after plasma treatment alleviates the surface non-uniformity problems observed in high temperature bonding and preserves the optical gain of the quantum wells.

### III. Optically pumped silicon evanescent lasers

Optically pumped silicon evanescent lasers have been fabricated to show the feasibility of this new platform. The SOI structure consists of a Si substrate, a 1  $\mu\text{m}$  thick  $\text{SiO}_2$  lower cladding layer, and a Si rib waveguide with a height (H) and rib-etch depth (D) of 0.7  $\mu\text{m}$  and 0.6  $\mu\text{m}$  respectively. The waveguide width (W) is varied from 1  $\mu\text{m}$  to 5  $\mu\text{m}$ . Confinement factors of silicon is varied from 5 % to 41 % with waveguide width variation of 1  $\mu\text{m}$  to 5  $\mu\text{m}$  and correspondingly, quantum well confinement factors are varied from 5.1 % to 4.1 % for five quantum wells. The waveguides are fabricated by standard photolithography and reactive ion etching (RIE) plasma of  $\text{Cl}_2/\text{HBr}/\text{Ar}$ . The structure of III-V quantum well materials and other fabrication process are described in [4] except for 300 °C of annealing temperature. The final device length is 800  $\mu\text{m}$ . An image of an 8x8  $\text{mm}^2$  bonded sample after InP substrate removal is shown in Figure 7. The bonded III-V layer is homogenous across the entire sample and is robust enough to stand up to dicing and polishing of the facets. The inset of Figure 7 shows a scanning electron microscope (SEM) image of the fabricated device cross section.

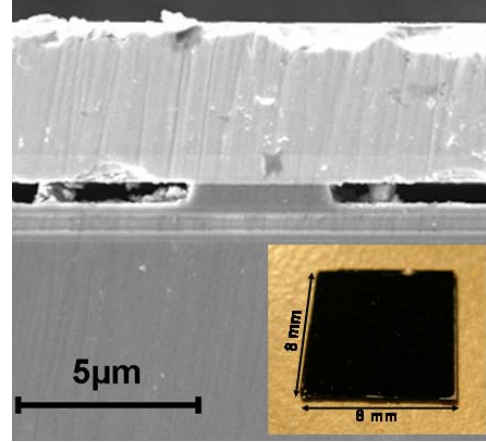


Fig. 7 SEM of the structure. (inset) 8x8  $\text{mm}^2$  bonded sample

The devices are lasing at 1.5  $\mu\text{m}$  and LL curves for a 4  $\mu\text{m}$  wide device are depicted in Figure 8. Kinks in the curves are due to multimode operation of the devices. Maximum fiber-coupled output power is 4.5 mW at 20 °C and maximum operating temperature is 60 °C. Sixty devices (ten devices at each of six widths) were characterized. 47 of the sixty devices are lasing with a variation of threshold power for each waveguide width of less than  $\pm 9\%$  as shown in Figure 9. It is seen from Figure 10 that the yield of the four wider widths is 98%, but the yield is lower for the narrower stripe widths. Inspection of the waveguide facets allowed this to be attributed to damage during polishing. HR coated lasers were also fabricated and tested. They had a maximum output power of 2.7 mW at 20 °C and operated up to 60 °C for wider devices. They showed similar high yield, low device-to-device variation, and threshold behavior with waveguide widths to that of the 800  $\mu\text{m}$ . The bonding process can be directly applied to 2 inch wafers even though 8x8  $\text{mm}^2$  bonding is demonstrated here.

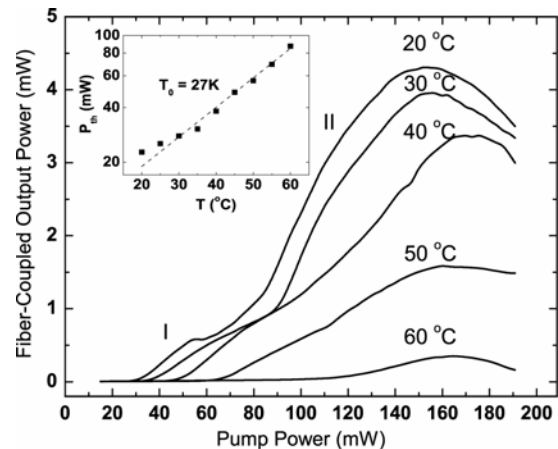


Fig. 8. LL Curves for 4  $\mu\text{m}$  wide device

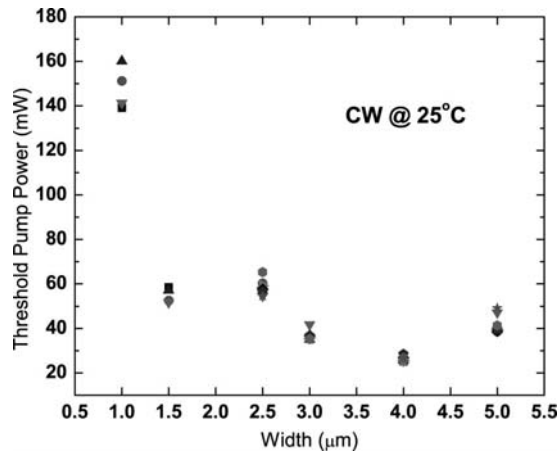


Fig. 9 Device threshold variation for 800  $\mu\text{m}$  length device.

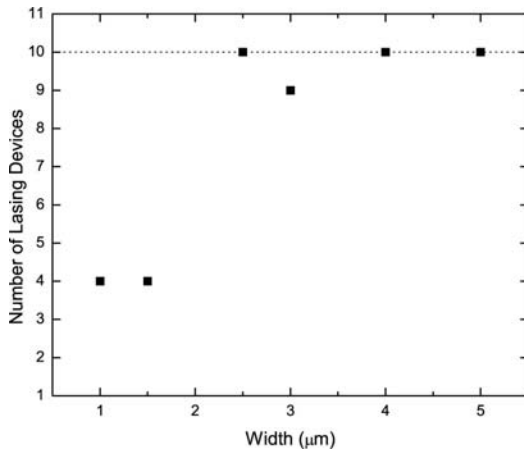


Fig. 10. Device yield. The number at each width represents the number of lasing devices out of 10.

#### IV. Conclusion

A new platform utilizing evanescent coupling of a silicon waveguide mode into a III-V gain region has been presented. This approach combines the benefits of mature silicon processing technology and the high optical gain of III-V materials. Moreover high performance active optical circuits can be integrated with silicon VLSI electronics on SOI wafers. Low threshold and high yield optically pumped hybrid silicon evanescent lasers have been realized, demonstrating the feasibility of this new platform. This work can be extended directly into electrically driven active devices by providing doped layers and patterning mesa structures in III-V region to flow electrical currents through the III-V active region.

#### V. References

[1] H. Rong *et al.*, "A continuous-wave Raman silicon laser," *Nature* **433**, 725, (2005).

[2] O. Boyraz *et al.*, "Demonstration of a silicon Raman laser," *Opt. Express* **12**, 5269, (2004).

[3] W. L. Ng *et al.*, "An efficient room-temperature silicon-based light-emitting diode," *Nature* **410**, 192, (2001).

[4] H. Park *et al.*, "Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells," *Opt. Express* **13**, 9460 (2005).

[5] D. Pasquariello *et al.*, "Plasma-Assisted InP-to-Si Low Temperature Wafer Bonding," *IEEE J. Sel. Topics Quantum Electron.* **8**, 118, (2002).

[6] Q. Tong *et al.*, "Low temperature InP/Si wafer bonding," *Appl. Phys. Lett.* **84**, 732 (2004).