

# Design of Hybrid Silicon Evanescent Amplifiers

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(Invited Paper)

## Abstract

**The structure and design of a hybrid silicon evanescent amplifier, incorporating III-V offset quantum wells bonded on a silicon waveguide, is proposed and discussed.**

## 1 Introduction

Silicon-based photonic integrated circuits have great potential in next generation optical networks because of the integration capability with CMOS electronics and the maturity of silicon fabrication technology. However, the lack of sufficient optical gain in silicon limits its scope of applications. In particular, optical amplifiers are key components to realize dense photonic integration by compensating for optical losses. Silicon Raman amplifiers have been demonstrated recently [1], but electrically driven silicon amplifiers have yet to be realized. We recently demonstrated hybrid silicon evanescent lasers using a wafer bonded structure with silicon waveguides and AlGaInAs offset quantum wells [2]. This technology enables optical amplifiers as well as lasers to be fabricated on a silicon-on-insulator (SOI) wafer. In this paper, the general structure and design of hybrid silicon evanescent amplifiers is discussed.

## 2 Device Structure

Device structure is represented in Fig. 1. The III-V region consists of a p-InGaAs contact layer, a p-InP clad, an AlGaInAs separate confinement heterostructure (SCH) layer, 8 AlGaInAs quantum wells, an n-InP layer, and n-InP/n-InGaAsP super lattice (SL) layers. The quantum wells consist of

alternating 7nm thick 1.5Q-AlGaInAs well layers and 10nm thick 1.3Q-AlGaInAs barrier layers. The thickness of the SCH layer is 0.25  $\mu\text{m}$  thick and the total thickness of n-layer including the InP and the SL layer is 0.15  $\mu\text{m}$ . The silicon waveguide is formed on an SOI wafer. This structure can be realized by low temperature oxygen assisted wafer bonding [3] and backside processing of III-V region after bonding process. Electrical current flows vertically through the mesa structure formed on the III-V region, and then flows laterally through n-InP and n-type SL layers.

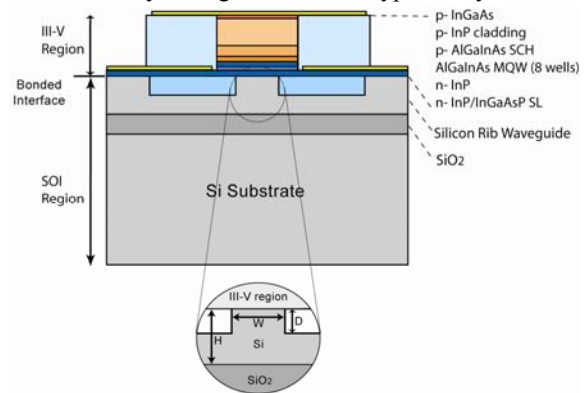


Fig. 1. Device structure.

## 3 Device Design

Figure 2 shows the modeled silicon confinement factor ( $\Gamma_{\text{Si}}$ ) and quantum well confinement factor ( $\Gamma_{\text{QW}}$ ), with various silicon waveguide dimensions. In general, wider or taller silicon waveguides increases  $\Gamma_{\text{Si}}$  while reducing  $\Gamma_{\text{QW}}$ . Therefore, silicon waveguide dimensions should be chosen carefully considering the tradeoff between 1) total achievable gain, 2) the saturation power of the optical amplifier and 3) ensuring single mode operation. The single mode operation regime is depicted by the dotted line in Fig 2.

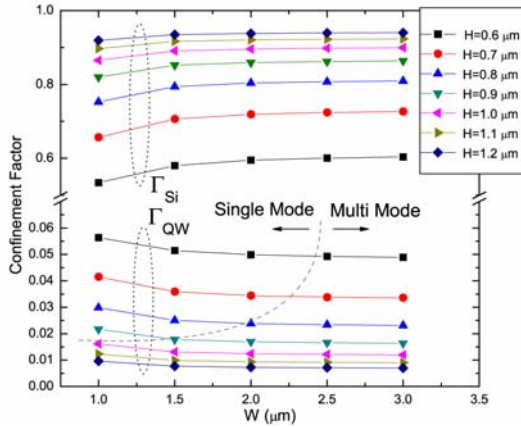


Fig. 2. Calculated confinement factors for silicon region (upper 7 lines) and quantum well region (lower 7 lines)

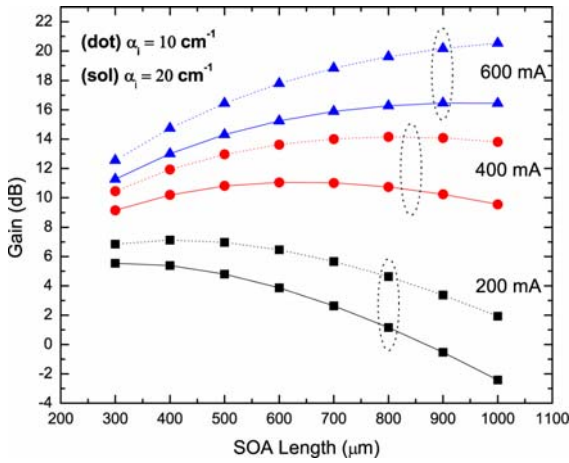


Fig. 3a. Amplifier gains vs device lengths. Waveguide dimensions: (H) 0.9  $\mu\text{m}$ , (W) 1  $\mu\text{m}$ , (D) 0.4  $\mu\text{m}$ , Active region width: 5  $\mu\text{m}$ ,  $\Gamma_{\text{QW}}$ : 2 %,  $\Gamma_{\text{Si}}$ : 85 %.

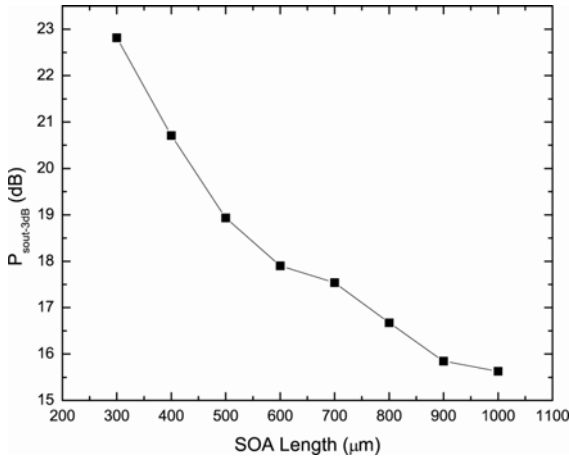


Fig. 3b. 3dB output saturation power vs device lengths. Waveguide dimensions: (H) 0.9  $\mu\text{m}$ , (W) 1  $\mu\text{m}$ , (D) 0.4  $\mu\text{m}$ , Active region width: 5  $\mu\text{m}$ ,  $\Gamma_{\text{QW}}$ : 2 %,  $\Gamma_{\text{Si}}$ : 85 %.

The calculated amplifier gain and 3dB output saturation power is shown in Fig. 3a and Fig. 3b with

different lengths of amplifiers using the rate equation model for multiple quantum wells [4]. The modeled waveguide dimensions are a height of 0.9  $\mu\text{m}$ , a width of 1  $\mu\text{m}$ , and an etch depth of 0.4  $\mu\text{m}$ . With these waveguide dimensions,  $\Gamma_{\text{QW}}$  and  $\Gamma_{\text{Si}}$  are calculated to be 2 % and 85 % respectively. The active region width is 5  $\mu\text{m}$  which corresponds to the actual optical mode width. The internal efficiency of the given epitaxial structure is calculated to be 80 % with Simwindows, a 1D drift and diffusion simulator. The calculation uses a material gain of  $g(N) = g_0 \ln(N/N_i)$ , where  $g_0 = 2000 \text{ cm}^{-1}$  and  $N_i = 2 \times 10^{18} \text{ cm}^{-3}$ . The modal losses are assumed to be 10  $\text{cm}^{-1}$  and 20  $\text{cm}^{-1}$ . These characteristics are based on previous Hakki-Paoli measurements made on optically pumped silicon evanescent lasers. Fig. 3a and 3b show that amplifier length is also an important parameter to determine the achievable gain and output saturation power. The simulation suggests that a gain of 10 dB with 3 dB output saturation of 19 dBm is achievable with a 500  $\mu\text{m}$  long amplifier. We neglect the impact of heating effect on the device is not considered in the simulations, but it will cause gain saturation at high current density. The series resistance of the device should be minimized to reduce the gain saturation from device heating.

The interface between the amplifier region and passive waveguide region is also important. Wider waveguide widths result in higher confinement factors in the silicon waveguide and less mode mismatch between the active and passive regions. The calculated coupling efficiency due to modal mismatch as a function of width is shown in Figure 4a. Figure 4b shows one approach to reduce the mode mismatch coupling loss and reflection at the interface by tapering the waveguide width. Reflections need to be kept as low as possible to prevent gain distortion in the frequency domain. From the calculated modal index difference for tapering the width from 1  $\mu\text{m}$  to 2  $\mu\text{m}$ , the power reflection is around  $6 \times 10^{-6}$  which causes a gain ripple of 0.01 dB with 20 dB gain.

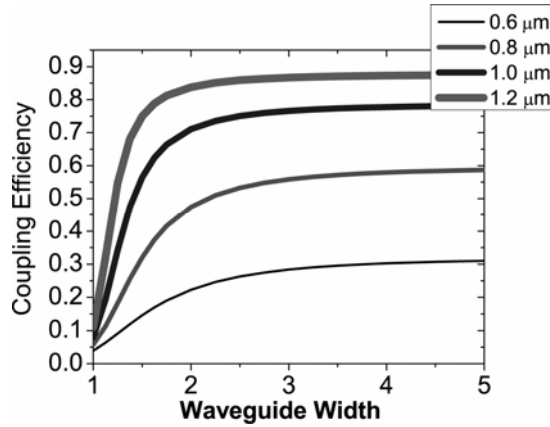


Fig. 4a. Calculated coupling efficiency between active and passive regions with different waveguide dimensions.

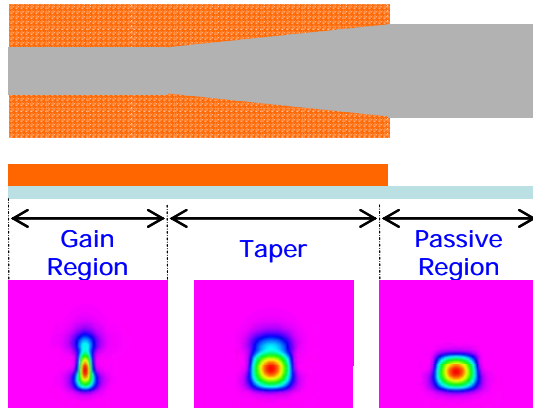


Fig. 4b. A tapering scheme between active and passive regions with mode profiles.

#### 4 Conclusion

Hybrid silicon evanescent amplifiers are proposed and their feasibility is theoretically shown. The fabrication of the device involves forming silicon waveguides on a SOI wafer, followed by low temperature oxygen plasma wafer bonding and backside processing of the III-V region. Optical amplifiers are a key element in photonic integrated circuits and raise the possibility of photonic integrated devices with low cost and high functionality on a silicon photonics platform for telecommunication and optical interconnects.

#### References

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