Hybrid Silicon Evanescent Laser in a Silicon-on-Insulator Waveguide

John E. Bowers, Alexander W. Fang, Hyundai Park
University of California Santa Barbara, ECE Department, Santa Barbara, CA 93106, USA
bowers@ece.ucsb.edu

Richard Jones, Mario J. Paniccia
Intel Corporation, 2200 Mission College Blvd, SC-12-326, Santa Clara, CA 95054, USA

Oded Cohen
Intel Corporation, SBI Park Har Hotzvim, Jerusalem, 91031, Israel
(Invited)

Abstract: We demonstrate electrically pumped silicon evanescent lasers operating cw at 40°C. Light is confined by SOI waveguides, and the evanescent tail is amplified by AlGaInAs quantum wells. This process is applicable to silicon-evanescent-photonic-integrated circuits.

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1. Introduction
In recent years, there has been tremendous work to realize a laser source on silicon due to the potential for high volume, low cost, manufacturability of photonics on a silicon platform. Work in silicon based light sources comes in the form of Raman lasers [1], silicon nano-patterning [2], and erbium doped silicon rich oxides [3]. These approaches have enabled optically pumped lasers and reports of electro-luminescence, but electrically pumped lasing has yet to be achieved. Hybrid integration, that is transferring III-V epitaxial structures onto silicon or even the transfer of entire III-V lasers to silicon, are other approaches able to capable of producing electrically pumped lasers on silicon. An overview of lasers on silicon is given in Table 1. We recently reported a continuous wave electrically pumped hybrid silicon evanescent laser [4], where AlGaInAs quantum wells are bonded to silicon waveguides, to achieve lasing at 1577 nm, with an output of 1.8mW up to 40°C. This structure is unique to other hybrid integration approaches since most of the mode resides inside the silicon waveguide and is defined by processing in the silicon region only. This leads to a process where many lasers can be fabricated with a single bond step and these devices can be integrated with other active and passive devices on the wafer.

Table 1: Overview of lasers on silicon

<table>
<thead>
<tr>
<th>Laser Type</th>
<th>Wavelength</th>
<th>Threshold</th>
<th>Output power</th>
<th>Cavity length</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monolithic integrated</td>
<td>1686 nm</td>
<td>200 mW</td>
<td>30 mW</td>
<td>30 mm</td>
<td>CW optically pumped Raman laser, Room temperature operation</td>
</tr>
<tr>
<td>Raman silicon laser [1]</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Periodic nano-patterned crystalline</td>
<td>1278 nm</td>
<td>12 W cm²</td>
<td>30 nW</td>
<td>1 mm</td>
<td>CW Optically pumped band-to-band emission 70K &gt; operating temperature</td>
</tr>
<tr>
<td>silicon laser [2]</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>InP/InGaAsP laser coupled to</td>
<td>1550 nm</td>
<td>180 mA</td>
<td>0.9 mW</td>
<td>.5 mm</td>
<td>Pulsed electrically pumped InP laser Fabry-Perot laser bonded to BCB on SOI, coupled with inverted taper.</td>
</tr>
<tr>
<td>silicon waveguides [5]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hybrid silicon evanescent laser [4]</td>
<td>1577 nm</td>
<td>65 mA</td>
<td>1.8 mW single fiber coupled</td>
<td>.8 mm</td>
<td>CW electrically pumped operation up to 40 C. Hybrid mode lies predominantly in silicon</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14.4 mW total</td>
<td></td>
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</table>

2. Device Structure and Fabrication
The hybrid silicon evanescent laser is fabricated using an AlGaInAs quantum well epitaxial structure that is bonded to a low-loss silicon strip waveguide as shown in Figure 1a. The silicon strip waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate with a 2 μm thick buried oxide using standard projection photolithography and Cl₂/Ar/HBr based plasma reactive ion etching. The silicon waveguide was fabricated with a final height of 0.76 μm and width of 2.5 μm resulting in a mode that exists predominantly in the silicon waveguide. The calculated overlap of the optical mode with the silicon waveguides is 75 % while there is a 3 % overlap in the quantum wells.

Fig. 1 (a) Schematic drawing of the hybrid laser structure with the optical mode superimposed (b) A scanning electron microscope (SEM) cross sectional image of a fabricated hybrid silicon evanescent laser.
The III-V epitaxial structure is grown on an InP substrate and is transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding [6]. The low temperature process consists of a thorough solvent cleaning procedure, and surface treatments with buffered HF for silicon and NH4OH for InP. The samples then undergo an additional surface treatment in an oxygen plasma reactive ion etch chamber. The sample surfaces are placed in physical contact at room temperature and subsequently annealed at 300 °C with an applied pressure of 1.5 MPa for 12 hours.

After InP substrate removal with a mixture of HCl/H2O, 75 µm wide mesas are formed using photolithography and by CH4/H/Ar- based plasma reactive ion etching through the p-type layers and H3PO4/H2O selective wet etching of the quantum well layers to the n-type layers. Ni/AuGe/Ni/Au alloy n-contacts are deposited onto the exposed n-type InP layer 38 µm away from the center of the silicon waveguide. 4 µm wide Pd/Ti/Pd/Au p-contacts are then deposited on the center of the mesas. The p-region on the two sides of the mesa are implanted with protons (H+) which electrically insulates the p-type InP [7] resulting in a ~ 4 micron wide p-type current channel down through the non conductive p-type mesa, preventing lateral current spreading in the p-type mesa. The electrical current flows through the center of the mesa to achieve a large overlap with the optical mode. Ti/Au probe pads are deposited on the top of the mesa. The wafer is then diced and the waveguide facets are polished forming ~ 860 µm long Fabry Perot laser cavity. A cross-sectional SEM image of the final fabricated hybrid laser is shown in Fig. 1b.

3. Experimental Results

The laser is driven by applying a positive bias voltage to the top p contact. The laser output from one waveguide facet is collected by a lensed single mode fiber and then characterized by using a spectrum analyzer or photodetector while simultaneously imaging the laser mode exiting the opposite facet with an infrared camera. The entire silicon chip is mounted on a TEC controller which allows the operating temperature of the laser to be varied from 0 °C to 80 °C.

![Fig. 2. The single sided fiber coupled laser output as a function of drive current for various operating temperatures.](image)

![Fig. 3. An infrared image taken from one of the polished facets showing seven c.w. hybrid silicon evanescent lasers operating simultaneously.](image)

Figure 2 shows the measured c.w. laser output power from one facet as a function of injected current for various operating temperatures ranging from 15 to 40 °C. As can be seen from Fig. 2, the laser threshold is 65 mA with a maximum output power of 1.8 mW at 15 °C. The laser has a 40 °C maximum lasing temperature with a characteristic temperature of 39 K. We have measured laser outputs from both facets and have found that they both have similar output powers and thresholds. Using the measured 6 dB coupling loss from waveguide to fiber, and the fact that light is only collected from one facet, we calculate a differential quantum efficiency of 12.7 %. A 15 cm⁻¹ modal loss was measured using the Hakki-Paoli method in the long wavelength regime [8]. The laser has a threshold voltage of 2 V and a series resistance of 7.5 ohms. These results are typical of other hybrid silicon evanescent lasers tested.

To demonstrate the scalable nature of this hybrid laser approach, Figure 3 shows the imaged output facet using an infrared camera of seven c.w. hybrid silicon evanescent lasers operating simultaneously from a single bonded silicon chip. The lasers were fabricated on an 8 mm wide silicon chip containing 36 devices of varying waveguide widths from 1-3.5µm. The number of evanescent laser devices running simultaneously is only limited by the electrical contact configuration of the current experimental set up (i.e. the number of electrical probes that could be placed simultaneously onto the test chip rather then the number of functional devices). The yield of this process is reasonable with 26 of the 36 lasers on this chip lasing. The yield is dominated by waveguide chipping and bond delamination during polishing of the bonded waveguide facets. This should be greatly improved by utilizing monolithic laser feedback schemes, such as ring resonator cavities or gratings in the silicon region, removing the dependence of device performance on facet polishing.

This bonding process can be applied to wafer scale, partial wafer scale or die attach, and the optimum size to use depends on economics and other issues. Bonding would be done after most of the silicon processing is complete. Three methods of introducing the III-V materials to the silicon fabrication process are shown in Figure 4. Depending on the active device density on the wafer, bonding may be done at the die level to silicon wafers to maximize the III-V material utilization as shown in Figure 4a. This could still be done in parallel
by using a fixture that holds the dies in place such that they can be bonded in a single bond step. Figure 4b shows the wafer to wafer bonding approach we are using now where a planar III-V wafer is bonded to a silicon waveguide wafer without significant alignment. This level of bonding would typically be done right after silicon waveguides are etched but before any oxides or metals are deposited. Figure 4c shows a wafer level bonding approach that can be done as a backend process by etching windows in the final processed planarized CMOS wafer, exposing the active silicon photonics region. The III-V wafer is etched such that only the active regions contact the exposed silicon and bonding can be achieved with very rough alignment. All three approaches require further backside processing of the III-V for proper electrical injection and metal interconnect deposition and definition to the silicon circuitry.

6. Conclusion

The electrically pumped silicon evanescent laser combines the mature, low cost manufacturability of silicon and the high optical gain of III-V materials to realize a high performance, electrically pumped laser for high level photonic integration with silicon photonics. The low temperature bonding process and the ability to create hundreds of lasers without a sophisticated alignment or optical coupling schemes make it a cost effective and CMOS friendly backend process.

References


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